Agilex™ 7 FPGA M-Series HBM2e Development Kit User Guide

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Contents

1. Overview

The Agilex™ 7 FPGA M-Series HBM2e Development Kit is a complete design environment that includes both hardware and software you need to develop Agilex 7 FPGA M-Series HBM2e designs. The board provides a wide range of peripherals and memory interfaces to facilitate the development of Agilex 7 FPGA M-Series HBM2e designs.

Table 1. Ordering Information

Development Kit Version	Ordering Code	Device Part Number	Serial Number Identifier
Agilex 7 FPGA M-Series Development Kit - HBM2e Edition	DK-DEV-AGM039EA	AGMF039R47A1E1VC	AGM82DK0001001
Agilex 7 FPGA M-Series Development Kit - HBM2e Edition (ES1 3x F-Tile and 1x R-Tile)	DK-DEV-AGM039FES	AGMF039R47A1E2VR0	AGM82DK0000001

For the board and FPGA capabilities, refer to the *Agilex 7 FPGA and SoC FPGA M-Series* page on the Altera® website.

Figure 1. Agilex 7 FPGA M-Series HBM2e Development Kit—Top View

Refer to the *Appendix A—Development Kit Components* section for more details about the components on the Agilex 7 FPGA M-Series HBM2e Development Kit.

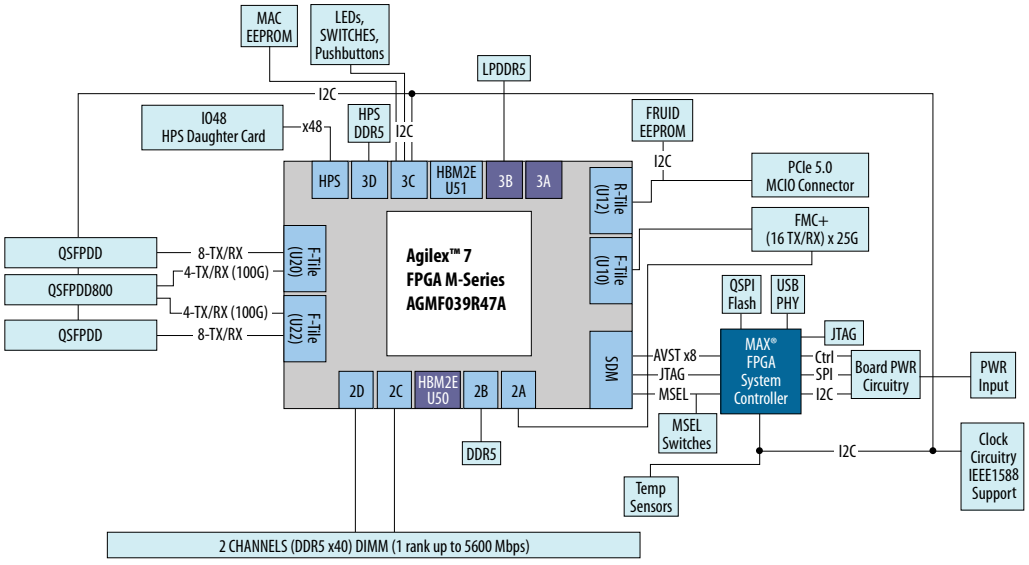
Related Information

- Development Kit Components on page 54
- Agilex 7 FPGA and SoC FPGA M-Series Webpage
- Agilex 7 M-Series ES Device Errata and User Guidelines
  Agilex 7 M-Series ES Device Errata and User Guidelines (RDC Item #776353)
- Agilex 7 M-Series Known Issue List

1.1. Block Diagram

Figure 2. Agilex 7 FPGA M-Series HBM2e Development Kit Block Diagram

Note: Avalon® streaming interface x8 configuration mode (AVST x8)



1.2. Feature Summary

- Agilex 7 FPGA M-Series (AGM039) device in 4700A BGA package
  - Quad-core 64-bit Arm* Cortex*-A53 hard processor (HPS)
  - 0.8 V VID-adjustable VCC core
  - F-Tile x3, R-Tile x1, and HBM2E
  - F-Tile 32G NRZ (58G PAM4) / High-Speed Transceiver 58G NRZ (116G PAM4) / R-Tile 32G PCIe* (CXL) Lanes
  - 3.9M logic elements (LE)
  - 1.3M adaptive logic modules (ALM)
  - 12.3K digital signal processing (DSP) blocks
- FPGA configuration
  - Avalon streaming interface x8 configuration mode support
  - 2 Gb flash for Avalon streaming interface x8 configuration mode
  - JTAG header for device programming
  - Built-in Altera FPGA Download Cable II for device programming
- Programmable clock sources
- Transceiver interfaces
  - PCI Express* (PCIe) x16 interface supporting 5.0 endpoint connected to an MCIO connector
  - 2x QSFPDD optical module interface connected to F-Tile transceiver
  - 1x QSFPDD 800 optical module interface connected to F-Tile transceiver
  - 16 F-Tile transceiver connect to FMC+ connector
- Memory interfaces
  - 2 x40 DIMM sockets supporting DDR5-5600
  - 1 x40 DDR5-5600 component interface for HPS processor memory
  - 1 x40 DDR5-5600 component interface for fabric I/O memory
  - 2 x16 LPDDR5 component, 2 channels and each is 16 bit data line interface
- Communication ports
  - JTAG header
  - Micro USB on-board Altera FPGA Download Cable II
  - System I^2C header

- Buttons, switches, and LEDs
  - CPU reset push button
  - PCIe reset push button
  - CXL reset push button
  - HPS reset push button
  - Four dedicated user LEDs
  - Board power good LED
  - BMC MAX® 10 configuration done LED
  - FPGA configuration done LED
- Heatsink and fan
  - Air-cooled heatsink assembly for FPGA
  - Air-cooled heatsink assembly for 1 port of QSFPDD-800 and 2 ports of QSFPDD, and all 3 ports support class 8
  - Red over-temperature warning LED
- Power
  - PCIe input power including required 2x4 auxiliary power connector
  - Blue power-good status LED
  - On/Off slide power switch for benchtop operation
  - On-board power and temperature measurement circuitry
- Mechanical
  - 4.375" x 10.0" board size
- Operating environment
  - Maximum ambient temperature of 0°C–30°C

1.3. Box Contents

- Agilex 7 FPGA M-Series HBM2e Development Kit
- 1x DDR5 DIMM module
- 1x IO48 HPS daughter board
- USB 2.0 MicroUSB cable
- 240W power adapter and NA/EU/JP/UK cords

Related Information

Agilex 7 FPGA M-Series HBM2e Development Kit Webpage

1.4. Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Operating Condition	Range of Values
Ambient operating temperature range	0°C to 30°C
ICC load current	195 A
ICC load transient percentage	200 A/µs
FPGA maximum power supported by active heatsink/fan	410 W

Related Information

Handling the Board on page 9

2. Getting Started

2.1. Before You Begin

You must check the kit contents and inspect the boards to verify that you received all of the items in the box before using the kit and installing the software.

In case any of the items are missing, you must contact Altera before you proceed.

Important: Read the Appendix C.1—Safety and Regulatory Information for safe operation and regulatory adherence.

2.2. Handling the Board

When handling the board, it is important to observe static discharge precautions.

Caution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Caution: This development kit should not be operated in a vibration environment.

2.3. Quartus® Prime Software and Driver Installation

This section explains how to install the following software and driver:

- Quartus® Prime Pro Edition software
- Ashling* RiscFree* Integrated Development Environment (IDE)
- Agilex 7 FPGA M-Series HBM2e Development Kit software
- Altera FPGA Download Cable II driver

2.3.1. Installing the Quartus Prime Pro Edition Software

1. Download the Quartus Prime Pro Edition software from the FPGA Software Download Center webpage of the Altera website.
2. Follow the on-screen instructions to complete the installation process. Choose an installation directory that is relative to the Quartus Prime Pro Edition software installation directory.

If you have difficulty installing the Quartus Prime software, refer to the *Altera FPGA Software Installation and Licensing*.

Related Information

- Quick-Start for Quartus Prime Pro Edition Software
- Quartus Prime Pro Edition User Guide: Getting Started

- Altera FPGA Software Installation and Licensing

2.3.2. Installing the Ashling* RiscFree Integrated Development Environment (IDE)

RiscFree is Ashling's Eclipse* C/C++ Development Toolkit (CDT) based integrated development environment (IDE) for Altera FPGAs Arm*-based HPS and RISC-V based Nios® V processors. The RiscFree IDE provides a complete, seamless environment for C and C++ software development.

RiscFree IDE has two types of installation options:

- Bundled installation option when installing the Quartus Prime software
- Standalone installation which requires you to install one of the following to use the debugger:
  - The Quartus Prime Programmer and Tools
  - The Quartus Prime software

For the installation instructions of the RiscFree IDE, refer to the *Ashling* RiscFree* Integrated Development Environment (IDE) for Altera FPGAs User Guide*.

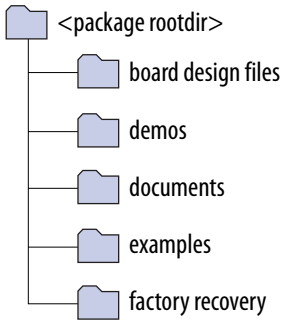
Related Information

Ashling* RiscFree* Integrated Development Environment (IDE) for Altera FPGAs User Guide

2.3.3. Installing the Development Kit

1. Download the Agilex 7 FPGA M-Series HBM2e Development Kit installer package from the Agilex 7 FPGA M-Series HBM2e Development Kit webpage on the Altera website.
2. Unzip the Agilex 7 FPGA M-Series HBM2e Development Kit installer package. The package creates the directory structure shown in the figure below.

Figure 3. Agilex 7 FPGA M-Series HBM2e Development Kit Directory Structure



3. For the latest issues and release notes, Altera recommends that you review the `readme.txt` located in the root directory of the kit installation.

Table 3. Installed Development Kit Directory Description

Directory Name	Description of Directory Contents
`board_design_files`	Contains schematic, layout, assembly, and Bill of Material (BOM) board design files. Use these files as a starting point for a new prototype board design.
`demos`	Contains demonstration applications based on Nios V, which shows how to access the QSFPDD modules through the I^2C multiplexer.
`documents`	Contains the development kit documentation.
`examples`	Contains the sample design files for the Agilex 7 FPGA M-Series HBM2e Development Kit: • Board Test System: BTS GUI, Power GUI, and Clock GUI • Golden Top project for pinout assignments management • Design Examples: Memory, XCVR, and GPIO
`factory_recovery`	Contains the original image/binary programmed onto the board before shipment. Use this image to restore the board with its original factory content.

2.3.4. Installing the Altera FPGA Download Cable II Driver

The Agilex 7 FPGA M-Series HBM2e Development Kit includes onboard Altera FPGA Download Cable II circuits for FPGA and system MAX 10 programming. However, for the host computer and board to communicate, you must install the Altera FPGA Download Cable II driver on the host computer.

Installation instructions for the Altera FPGA Download Cable II driver for your operating system are available on the Altera website.

On the Altera website, navigate to the *Cable and Adapter Drivers Information* link to locate the table entry for your configuration and click the link to access the instructions.

Related Information

- Cable and Adapter Drivers Information
- Altera FPGA Download Cable II User Guide

3. Development Kit Setup

The instructions in this chapter explain how to setup the Agilex 7 FPGA M-Series HBM2e Development Kit for specific use cases.

3.1. Default Settings

The Agilex 7 FPGA M-Series HBM2e Development Kit ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be correctly configured with the default settings, follow the instructions in the factory default switch settings table to return to its factory settings before proceeding ahead.

Table 4. Factory Default Switch Settings

Note: "X" refers to Don't Care in the table below.

Note: Do not set the switches when the power is on. Only set the switches after the power is off.

Switch	Default Position	Notes
S24[1:4]	ON/OFF/OFF/ON	S24[1:3] Set MSEL mode: • 111: JTAG • 011: Avalon streaming interface x8 configuration mode S24[4]: • OFF—FPGA can access three QSFPDD modules • ON—system_info_0_slv_data_write_0[2] determines if FPGA can access three QSFPDD modules or not. — system_info_0_slv_data_write_0[2] = 0 (by default): FPGA cannot access the modules. — system_info_0_slv_data_write_0[2] = 1: FPGA can access modules. *Note:* Nios in MAX 10 would access three QSFPDD modules for thermal control only when S24[4] set as ON and system_info_0_slv_data_write_0[2] is 0. The FPGA can access modules when S24.4 set as OFF or S24[4] set as ON and system_info_0_slv_data_write_0[2] is 1. system_info_0_slv_data_write_0 is a register of the MAX 10 design and its address offset is 0x38.
S25	OFF	• OFF—HPS is not in the JTAG chain • ON—HPS is in the JTAG chain
S3	OFF	• OFF—FMC+ is not in the JTAG chain • ON—FMC+ is in the JTAG chain

continued...

Switch	Default Position	Notes
S26	ON	• ON—MAX 10 programming via on-board Altera FPGA Download Cable • OFF—MAX 10 programming via external Altera FPGA Download Cable
S28[1:4]	OFF/ON/OFF/OFF	S28[1:2] Select the clock source for EU122: • ON:ON—Disabled • OFF:ON—Internal crystal (default) • ON:OFF—CLKIN2 (MCIO) • OFF:OFF—CLKIN3 (SMP) S28[3:4] Set SSC: • ON:X—Disabled (default) • OFF:X—AND OUT0 • X:ON—Disabled (default) • X:OFF—Enable SS on N1 divider OUT6, OUT7
S6	OFF	MAX 10 JTAG Enable switch when the JTAG pin sharing is enabled: • ON—JTAG pins function as dual-purpose pins • OFF—JTAG pins function as JTAG dedicated pins This switch can be set to either ON or OFF with the current MAX 10 design because the JTAG pin sharing is not enabled in the design.
S4	ON	Select configuration image in the dual-configuration images mode: • ON—The first configuration image is **configuration image 0** • OFF—The first configuration image is **configuration image 1** This switch can be set to either ON or OFF with the current MAX 10 design because single image mode is used in the design.
S16	[1]/[0]	Controls the configuration for the U35 clock device
	OFF/OFF (default)	Input clock from XTAL
	OFF/ON	Input clock from IN2
	ON/OFF	Input clock from IN1
	ON/ON	Not connected
S20	[1]/[0]	Controls the configuration for the U93 clock device
	OFF/OFF(default)	Input clock from XTAL
	OFF/ON	Input clock from IN2
	ON/OFF	Input clock from IN1
	ON/ON	Not connected

3.2. Powering Up the Development Kit

To power up the development kit, follow these steps:

1. Use the provided 300 W power adapter to supply power through J12 and J3.
2. After the power adapter is plugged into J12 and J3, and switch S7 is set to the **ON** position, the LED DS15 illuminates, indicating that the board powered up successfully. If the LED DS15 is not turned **ON**, it indicates that one of the voltage regulators is not turned on.

   Note: All the QSFPDD and QSFPDD800 ports can support up to class 8, meaning each port consumes 18 W. Two power supplies are needed to provide sufficient power for peak performance.

   The Agilex 7 FPGA M-Series HBM2e Development Kit can run the loop back test or memory test using only one power adapter connected to J12. Since one power adapter can provide 300 W maximum, the Agilex 7 FPGA M-Series HBM2e Development Kit can only run diagnostic tests.

3.3. Performing Board Restore

The Agilex 7 FPGA M-Series HBM2e Development Kit (DK-DEV-AGM039FES) ships with 4 pages of bts_config design examples stored in the QSPI flash device U98.

The Agilex 7 FPGA M-Series HBM2e Development Kit (DK-DEV-AGM039EA) ships with GHRD design examples stored in the QSPI flash device U98. Refer to RocketBoards.org to recover and update GHRD image on QSPI flash.

You can perform board restore by following the instructions through the Quartus Prime Programmer GUI.

3.3.1. Restoring Board QSPI Flash with Default Factory Image

Follow the steps to overwrite the Avalon streaming interface x8 configuration mode image.

1. Ensure that MSEL[2:0] is OFF (JTAG mode) before powering up the board.
2. Open Quartus Prime Programmer GUI, detect JTAG chain.
3. Change VTAP10 to 10M50DAF256, attach flash device of QSPI_2Gb.
4. Attach the Avalon streaming interface x8 configuration mode image to QSPI_2Gb.
5. Select program/configure options and click **Start** button.
6. Power off the board after programming the flash successfully, set MSEL[2:0] OFF OFF ON (Avalon streaming interface x8 configuration mode).

4. Board Test System

The Agilex 7 FPGA M-Series HBM2e Development Kit includes design examples and the board test system (BTS) GUI to test the functionality of this board. The BTS provides an easy-to-use interface to alter functional settings and observe results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage.

While using the BTS, you can reconfigure the FPGA several times with test designs specific to the functionality that you are testing. The BTS is also useful as a reference for designing systems. The BTS communicates over the JTAG bus to a test design running in the Agilex 7 FPGA.

The BTS checks for hardware faults before you can use the board. If one or more BTS test items fail, it implies either a wrong hardware setting or hardware fault on specific interface.

The following figure shows the graphical user interface (GUI) of a board that is in factory configuration.

Figure 4. BTS GUI

4.1. Set Up the BTS GUI Running Environment

You need to download and install **Java runtime environment** and Quartus Prime software on your systems to run the BTS GUI, including the Power Monitor and Clock Controller GUI. **Java runtime environment** includes **OpenJDK** and **OpenJFX**, whose installation is a one-time procedure. If you have completed it before, you do not need to do it again unless the Java version upgrade is needed.

4.1.1. Downloading OpenJDK

1. Download the Temurin* OpenJDK. Refer to the related information for the download link.
2. Select Architecture x64, Package Type JRE, and Version 11.
   a. For the **Windows** system, choose the `JRE.zip` format file.
   b. For the **Linux** system, choose the `JRE.tar.gz` format file.

   Note: Download the latest version to update the JDK version. The following version was tested: 11.0.21+9

Related Information

Temurin* OpenJDK

4.1.2. Downloading OpenJFX

1. Download the Gluon* OpenJFX. Refer to the related information for the download link.
2. Select JavaFX version 17.0.2.
   a. For the **Windows** system, download the JavaFX Windows x64 SDK.
   b. For the **Linux** system, download the JavaFX Linux x64 SDK.

Related Information

Gluon* OpenJFX

4.1.3. Installing OpenJDK and OpenJFX

You have two downloaded compressed files. Follow these steps to install them.

Follow these steps to install the downloaded zip files:

1. On **Windows** system, Altera recommends you to unzip the files and put them in the following directory:
   - `C:\Program Files\Java\jre`
   - `C:\Program Files\Java\jfx`

Note: The unzipped folder name of JRE is `jdk-11.0.xx+x-jre` (for example, `jdk-11.0.15+10-jre`). Rename it to *jre*.

The unzipped folder name of JFX is `javafx-sdk-17.0.2`. Rename it to *jfx*.

2. On the **Linux** system, Altera recommends that you unzip the files and rename the folders using the following commands:

```
# unzip openjfx-17.0.2_linux-x64_bin-sdk.zip -d /opt/Java/
# tar zxvf OpenJDK11U-jre_x64_linux_hotspot_11.0.15_10.tar.gz -C /opt/Java/
# cd /opt/Java
# mv javafx-sdk-17.0.2 jfx
# mv jdk-11.0.15+10-jre jre
```

You have the following two directories on your **Linux** system:

- `/opt/Java/jre`
- `/opt/Java/jfx`

4.1.4. Setting Up the Quartus Prime Software for BTS Operation

You must install the Quartus Prime software to support the silicon on the development kit. The recommended version is located in the `README.txt` file in the `examples\board_test_system` directory. If you choose to install individual files, you must install Agilex 7 Device Support.

The BTS communicates over JTAG to a test design running in the FPGA. The BTS shares the JTAG with other applications such as the Programmer, the System Console, and the Signal Tap Logic Analyzer. Altera recommends closing other applications before using BTS, as the GUI is designed based on the Quartus Prime software.

The BTS relies on the Quartus Prime software's specific library. Before running the BTS, open the Quartus Prime software to automatically set the environment variable `QUARTUS_ROOTDIR`. You can also change it through **Environment Variables** in the **System Properties** in Windows*. The BTS uses this environment variable to locate the Quartus Prime library.

4.1.5. Running the BTS GUI

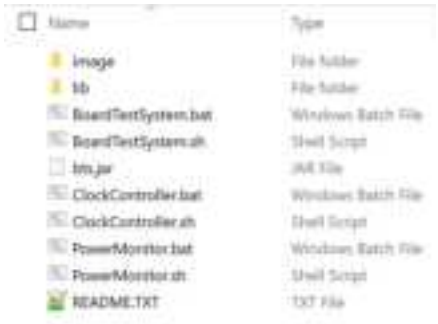
With the power to the board off, follow these steps:

1. Connect the USB cable to your PC and the board.
2. Check that the development board switches and jumpers are set according to your preferences. Refer to the Development Kit Setup section. BTS requires the system MAX 10 and the Agilex 7 FPGA on the JTAG chain.
3. Check the external modules status: QSFPDD800/QSFPDD/FMC+/DIMM.
4. Turn on the board power switch.

Note: To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The BTS cannot run correctly unless the USB cable is attached, and the board is on.

To run the BTS, navigate to the <*package dir*>\examples\board_test_system directory. The BTS release folder always includes the following files:

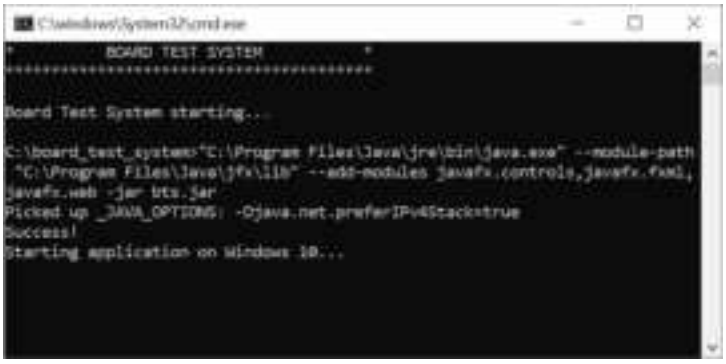
Figure 5. BTS Folder



You can run BTS GUI with the following scripts:

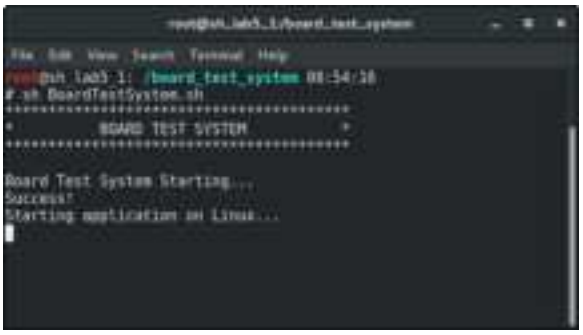
1. On the **Windows** system, double-click the `.bat` files to run BTS, Clock Controller, or Power Monitor GUI.

Figure 6. Windows Console



2. On the **Linux** system, run the shell script with root privilege.

Figure 7. Linux Console



Note: The `.bat` or shell script checks the Java environment settings, copies necessary files, and prompts if the environment is not set up correctly.

The GUI displays the application tab corresponding to the design running in the FPGA. If the design loaded in the FPGA is not supported by the BTS GUI, a message prompting you to configure your board with a valid BTS design appears. Refer to the The Configure Menu section.

Related Information

Development Kit Setup on page 12

4.2. Test the Functionality of the Development Kit

This section describes each control in the BTS.

4.2.1. The Bottom Information Bar

The bottom information bar shows the status of the system connection, Quartus Prime version, and the JTAG clock.

- **System Connected/Disconnected**: Shows if the board is connected to the system. The green sign turns gray if the board becomes disconnected.
- **Quartus Prime Version**: Displays the current Quartus Prime version installed and active on your system. The text turns red if your version is older than the required version. Change the environment variable *QUARTUS_ROOTDIR* if you have installed the right version, but the active version does not meet the requirement.
- **JTAG:** Displays the JTAG clock frequency.

4.2.2. The Configure Menu

Use the **Configure** menu to select the design you want to use. Each design example tests different functionality that corresponds to different application tab.

Figure 8. The Configure Menu

Follow these steps to configure the FPGA with a test system design:

1. On the **Configure** menu, click the **Configure** command that corresponds to the functionality you wish to test.
2. Click **Configure** in the dialog box that appears to download the corresponding design's SRAM Object File (`.sof`) to the FPGA. The download process usually takes less than a minute.
3. The design begins running in the FPGA after completion of the configuration. The corresponding GUI application tabs that interface with the design are now enabled. If you use the Quartus Prime Programmer for configuration, instead of the BTS GUI, you might need to restart the GUI.

4.2.3. The Sys Info Tab

The **Sys Info** tab shows information about the board's current configuration. The tab displays the board information, JTAG chain devices, and other details stored on the board.

Figure 9. The Sys Info Tab

The following sections describe the controls on the **Sys Info** tab:

Board Information

The board information control displays static information about your board.

- **Board Name**: Indicates the official name of the board given by the BTS.
- **Board Revision**: Indicates the revision of the board.
- **MAX Version**: Indicates the version of the system MAX 10.

JTAG Chain

The JTAG chain control shows all the devices currently in the JTAG chain.

Note: Both of the system MAX 10 and the FPGA must be both in the JTAG chain when you are running the BTS GUI.

4.2.4. The GPIO Tab

The **GPIO** tab allows you to interact with the general-purpose user I/O components on your board. You can turn LEDs on or off.

Figure 10. The GPIO Tab

The following sections describes the controls on the **GPIO** tab:

User LEDs

The **User LEDs** control displays the current state of the user LEDs. Toggle the LED buttons to turn the board LEDs on and off. Click the **All** button to reverse the state of all the LEDs.

Qsys Memory Map

The **Qsys Memory Map** control shows the memory map of `bts_config.sof` design running on your board.

4.2.5. The XCVR Tab

The **XCVR** tab allows you to run transceiver tests on your board. You can run the test using either electrical loopback modules or optical fiber modules.

4.2.5.1. The QSFPDD NRZ Tab

Figure 11. The QSFPDD NRZ Tab

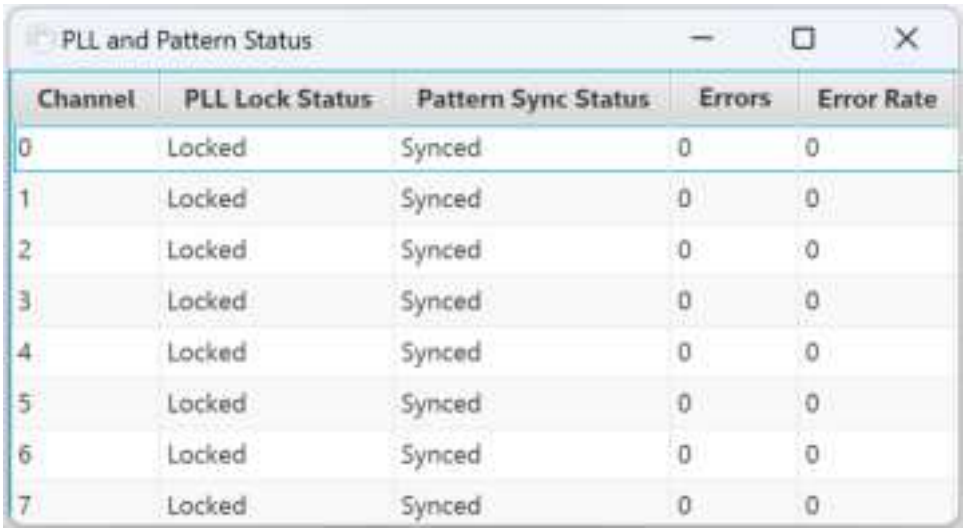
The following sections describe controls in the **QSFPDD NRZ** tab:

Status

The **Status** control displays the following status information during the loopback test:

- **PLL Lock**: Shows the PLL locked or unlocked state.
- **Pattern Sync**: Shows the pattern synced or not state. The pattern is considered synced when the start of the data sequence is detected.
- **Detail**: Shows the PLL lock and pattern sync status of each channel. The number of the error bits of each channel can be found here.

Figure 12. QSFPDD NRZ—PLL and Pattern Status



Channel	PLL Lock Status	Pattern Sync Status	Errors	Error Rate
0	Locked	Synced	0	0
1	Locked	Synced	0	0
2	Locked	Synced	0	0
3	Locked	Synced	0	0
4	Locked	Synced	0	0
5	Locked	Synced	0	0
6	Locked	Synced	0	0
7	Locked	Synced	0	0

Control

Use the following controls to select an interface to apply PMA settings, data type, and error control:

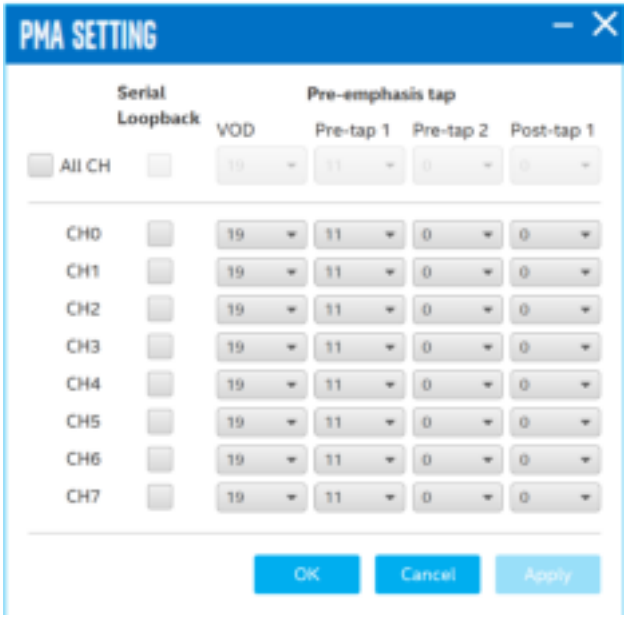
- **QSFPDD0x8**
- **QSFPDD1x8**

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**: Displays the signal status between the transmitter and the receiver.
- **VOD**: Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**:
  - Pre-tap 1: Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
  - Pre-tap 2: Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - Post-tap 1: Specifies the amount of pre-emphasis on the post-tap of the transmitter buffer.

Figure 13. QSFPDD NRZ—PMA Setting



Data Type

The **Data Type** control specifies the type of data pattern contained in the transactions. Select the following available data types for analysis:

- **PRBS7**: Pseudo-random 7-bit binary sequences.
- **PRBS15**: Pseudo-random 15-bit binary sequences.
- **PRBS23**: Pseudo-random 23-bit binary sequences.
- **PRBS31**: Pseudo-random 31-bit binary sequences (default).

Error Control

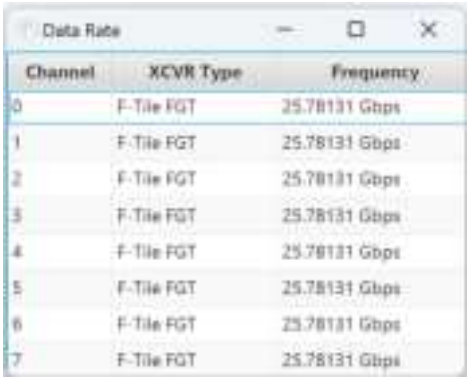
This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors**: Displays the number of data errors detected in the received bitstream.
- **Inserted Errors**: Displays the number of errors inserted into the transmit data stream.
- **Bit Error Rate**: Calculates the bit error rate of the transmit data stream.
- **Inserts**: Inserts a one-word error into the transmit data stream each time you click the button. Insert error is only enabled during transaction performance analysis.
- **Clear**: Resets the **Detected Errors** counter and **Inserted Errors** counter to zero.

Run Control

- **TX and RX performance bars**: Show the percentage of the maximum theoretical data rate that the requested transactions are able to achieve.
- **Start**: Initiates the loopback tests.
- **Data Rate**: Displays the XCVR type and data rate of each channel.

Figure 14. QSFPDD NRZ—Data Rate



4.2.5.2. The QSFPDD PAM4 Tab

Figure 15. The QSFPDD PAM4 Tab

Note: This tab has similar control functions as the **QSFPDD NRZ** tab.

4.2.5.3. The FMC+ NRZ Tab

Figure 16. The FMC+ Tab

Note: This tab has similar control functions as the **QSFPDD NRZ** tab.

4.2.5.4. The QSFPDD800 PAM4 Tab

Figure 17. The QSFPDD800 PAM4 Tab

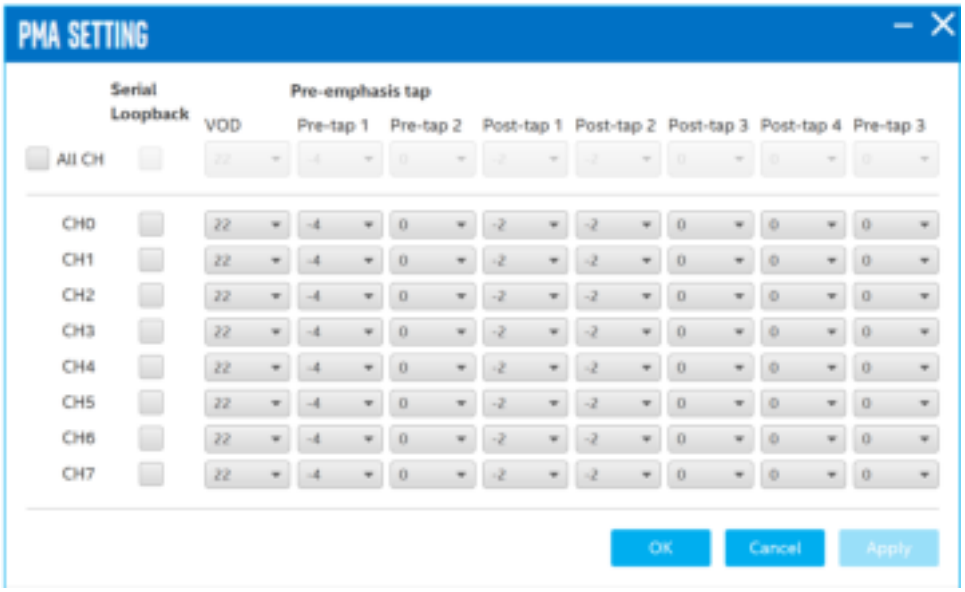
Note: This tab has similar control functions as the **QSFPDD NRZ** tab.

PMA Setting

In addition to the PMA settings listed in the QSFPDD NRZ—PMA Setting figure, additional settings are available for the F-Tile FHT PMA. The PMA is set to the default values in the PAM4 designs.

- **Pre-emphasis tap**:
  - **Post-tap 2**: Specifies the amount of pre-emphasis on the second post-tap of the transmitter buffer.
  - **Post-tap 3**: Specifies the amount of pre-emphasis on the third post-tap of the transmitter buffer.
  - **Post-tap 4**: Specifies the amount of pre-emphasis on the fourth post-tap of the transmitter buffer.
  - **Pre-tap 3**: Specifies the amount of pre-emphasis on the third pre-tap of the transmitter buffer.

Figure 18. QSFPDD800PAM4 Tab—PMA Setting



Related Information

The QSFPDD NRZ Tab on page 23

4.2.6. The Memory Tab

The **Memory** tab allows you to read and write DDR5-COMP, LPDDR5-COMP, DDR5-RDIMM memory, and High Bandwidth Memory (HBM) memory on your board. Download the design through the BTS **Configure** menu.

4.2.6.1. The DDR5 COMP Tab

Figure 19. The DDR5 COMP Tab

The following sections describe controls on this tab.

Start

Initiates DDR5 memory transaction test.

Stop

Terminates transaction test.

Test times

Number of times that write and read DDR once.

Test Control

- **Test Size**: You can choose the size of the memory to test. The available options are 64 KB, 256 KB, 1 MB, 4 MB, 16 MB, 64 MB, 256 MB, 1 GB, and 4 GB (default).
- **Offset (Hex)**: You can define the memory start address to test.
- **Test Mode**: Infinite Read and Write (default), Single Read and Write.
- **Test Pattern**: PRBS (default), User Defined Constant, Walking '0', Walking '1'.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors**: Displays the number of data errors detected in the hardware.
- **Inserted Errors**: Displays the number of errors inserted into the transaction stream.
- **Insert**: Insert a one-word error into the transaction stream each time you click the button. The **Insert** error is only enabled during transaction performance analysis.
- **Clear**: Resets the **Detected Errors** counter and **Inserted Errors** counter to zeros.

Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **Write**, **Read**, and **Total** performance bars: Show the percentage (%) of maximum theoretical data rate that the requested transactions are able to achieve.
- **Write (MBps)**, **Read (MBps)**, and **Total (MBps)**: Show the number of bytes analyzed per second.

4.2.6.2. The LP DDR5 COMP Tab

Figure 20. The LP DDR5 COMP Tab

Note: This tab has similar control functions as the **DDR5 COMP** tab.

4.2.6.3. The HPS DDR5 COMP Tab

Figure 21. The HPS DDR5 COMP Tab

Note: This tab has similar control functions as the **DDR5 COMP** tab.

4.2.6.4. The DDR5 RDIMM Tab

Figure 22. The DDR5 RDIMM Tab

Note: This tab has similar control functions as the **DDR5 COMP** tab.

4.2.6.5. The HBM2 Tab

The **HBM2** tab allows you to read and write the top and bottom bank of HBM2 on your board.

4.2.6.5.1. The HBM2 Top Tab

Figure 23. The HBM2 Top Tab

The following sections describe controls on this tab.

Status Indicators

- **HBM2 Size**: Indicates the memory size of HBM2.
- **Test Status**: Indicates the status of the overall test, the table shows each channel status of HBM2.

4.2.6.5.2. The HBM2 Bottom Tab

Figure 24. The HBM2 Bottom Tab

Note: This tab has similar control functions as the **HBM2 Top** tab.

4.3. Control the On-board Clock through Clock Controller GUI

The Clock Controller GUI can control the outputs of on-board Si5391-1/Si5391-2/ Si5392/ Si5395/Si5332/Si5518. The instructions to run Clock Controller GUI are stated in the Running the BTS GUI section. Alternatively, you can start using the Clock Controller feature by selecting the **Clock** icon on the BTS GUI.

The Clock Controller communicates with the system MAX 10 device through 10-pin JTAG header J7 or USB port J1. Then, the system MAX 10 controls the programmable clock part through a 2-wire I^2C bus.

Note: You cannot run the stand-alone Clock Controller GUI application when the BTS or Power Monitor GUI is running at the same time.

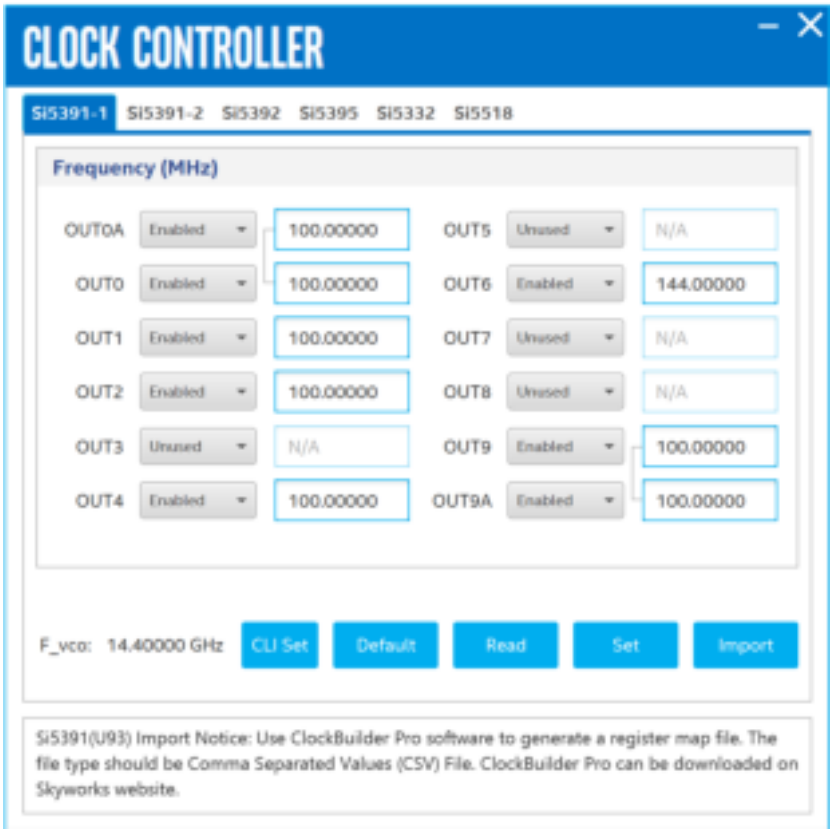
Note: Si5518 can be controlled only when a design in which the SPI interface is instantiated, such as the `bts_config.sof` under the `board_test_system\image\ES` folder that has been downloaded to the FPGA.

Related Information

Skyworks Solution
More information about the Clockbuilder Pro software.

4.3.1. Si5391-1

Figure 25. Si5391-1



The following sections describe the **Clock Controller** buttons.

Read

Reads the current frequency setting for the oscillator associated with the active tab.

Default

Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

Set

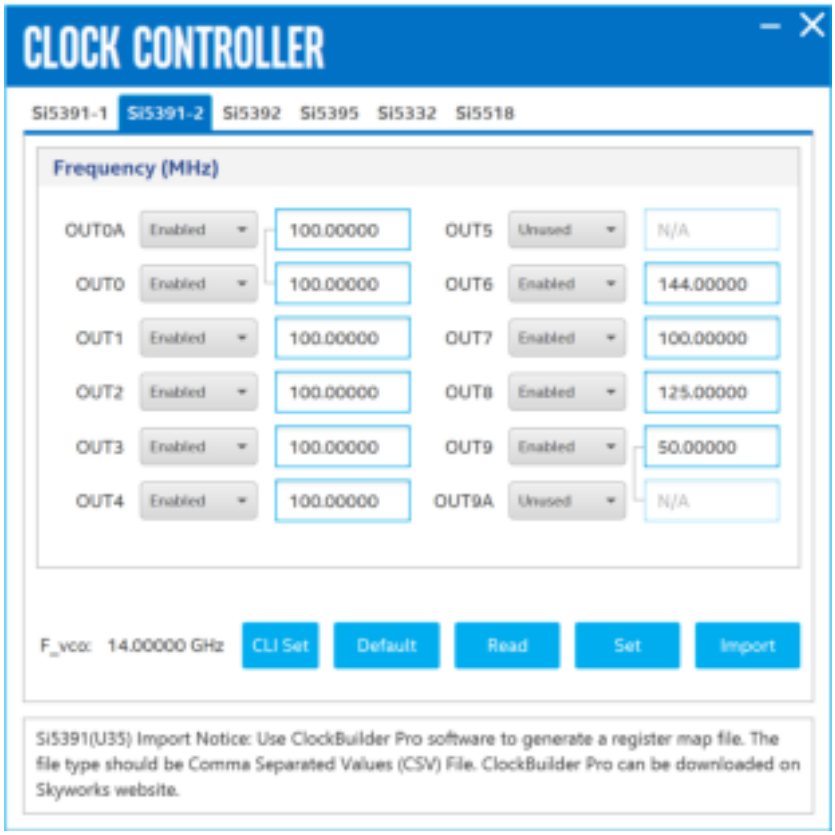
Sets the programmable oscillator frequency for the selected clock to the value in the OUTx output controls for Si5391. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Altera recommends resetting the FPGA logic after changing frequencies.

Import

You can generate the register list from the Skyworks* ClockBuilder Pro tool and import it into Si5391 to update the settings of the output clocks. Register changes are volatile after power cycling.

4.3.2. Si5391-2

Figure 26. Si5391-2



Note: This tab has similar control functions as the **Si5391-1** tab.

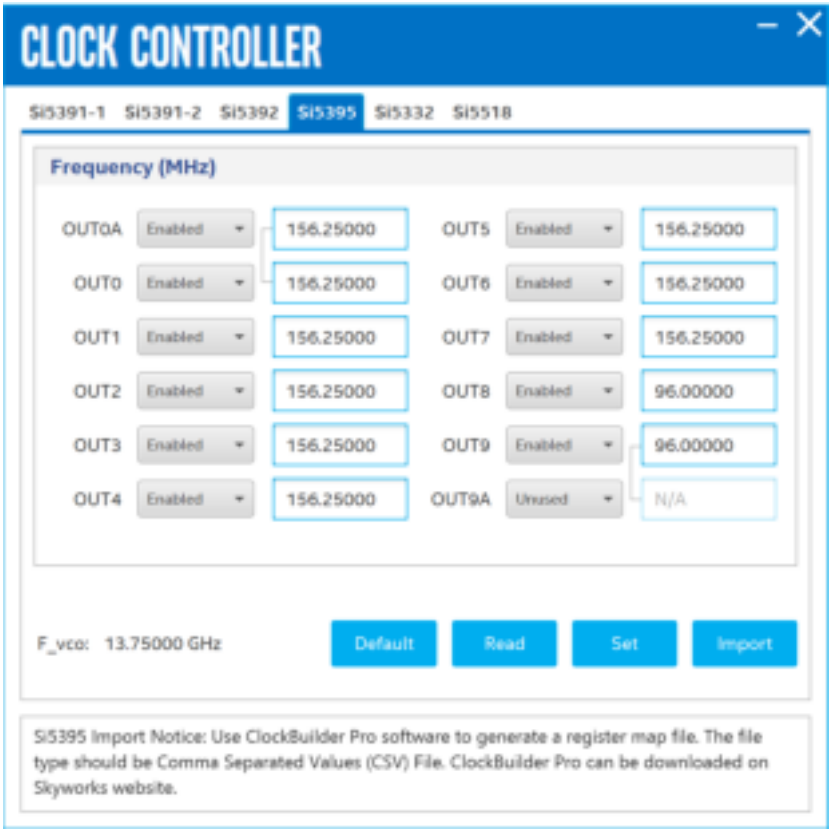
4.3.3. Si5392

Figure 27. Si5392

Note: This tab has similar control functions as the **Si5391-1** tab.

4.3.4. Si5395

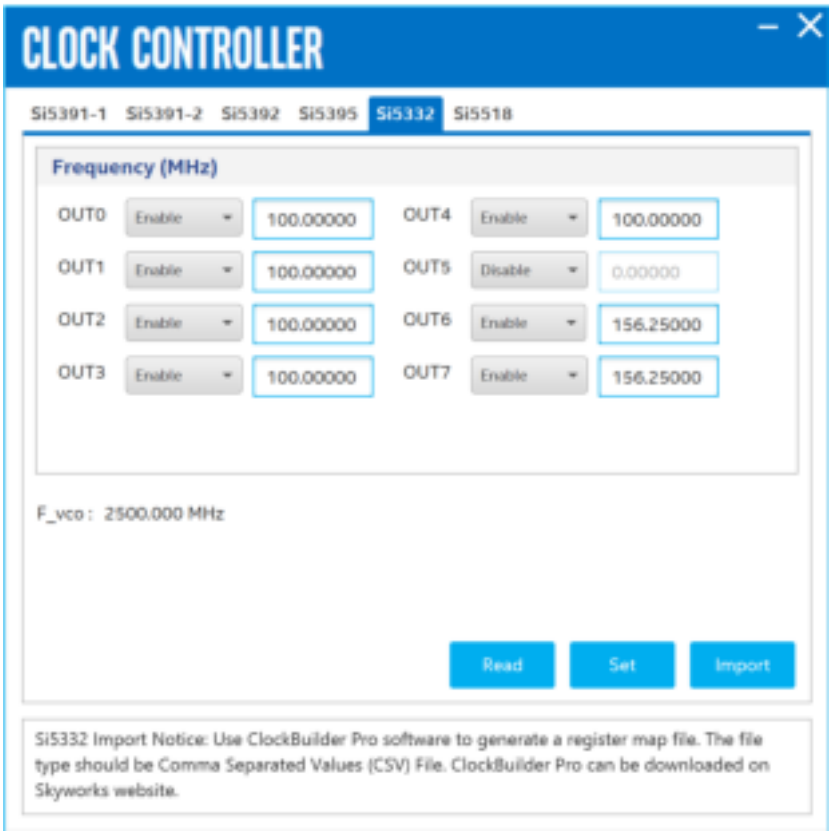
Figure 28. Si5395



Note: This tab has similar control functions as the **Si5391-1** tab.

4.3.5. Si5332

Figure 29. Si5332



Note: This tab has similar control functions as the **Si5391-1** tab. There is no default button for this clock but you can use **Import** or power cycle the board to get default clock frequencies.

4.3.6. Si5518

Figure 30. Si5518

Import

You can generate the firmware and user boot binary files from the Skyworks* Clockbuilder Pro tool and import them into Si5518 to update the settings of RAM. The clock output frequency value is displayed after the import is successful. Register changes are volatile after power cycling.

Default

Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

Soft Reset

Initiates a global soft reset. The global soft reset does not download the firmware and frequency plan from the NVM. Instead, it starts the firmware and frequency plan currently running on the device. The device behaves like it has been rebooted.

Related Information

Skyworks Solution
More information about the Clockbuilder Pro software.

4.4. Monitor On-Board Power Regulator through Power Monitor GUI

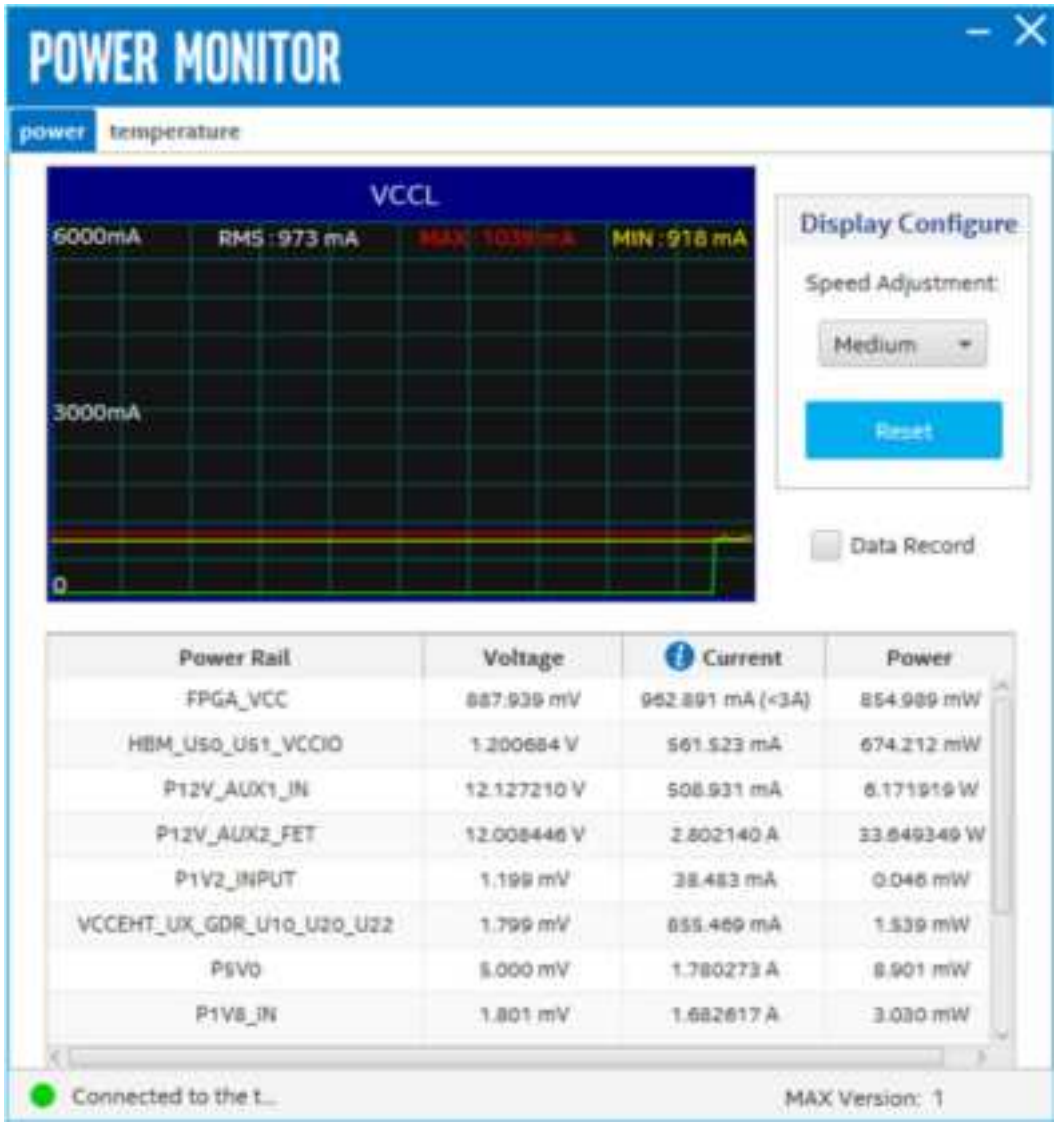
The **Power Monitor** GUI reports most power rails' voltage, current, and power information on the board. It also collects temperature from FPGA die, power modules, and diodes assembled on PCB.

The **Power Monitor** GUI communicates with the system MAX 10 through a 10-pin JTAG header J7 or USB port J1. The system MAX 10 monitors and controls power regulator, temperature/voltage/current sensing chips through a 2-wire I^2C bus.

The instructions to run the **Power Monitor** GUI are stated in the Running the BTS GUI section. Alternatively, you can start using the **Power Monitor** feature by selecting the **Power** icon on the BTS GUI.

Note: You cannot run the stand-alone **Power Monitor** GUI when the BTS or the **Clock Controller** GUI is running at the same time.

Figure 31. Power Monitor GUI—The Power Tab



The following sections describe the details of the **Power Monitor** GUI.

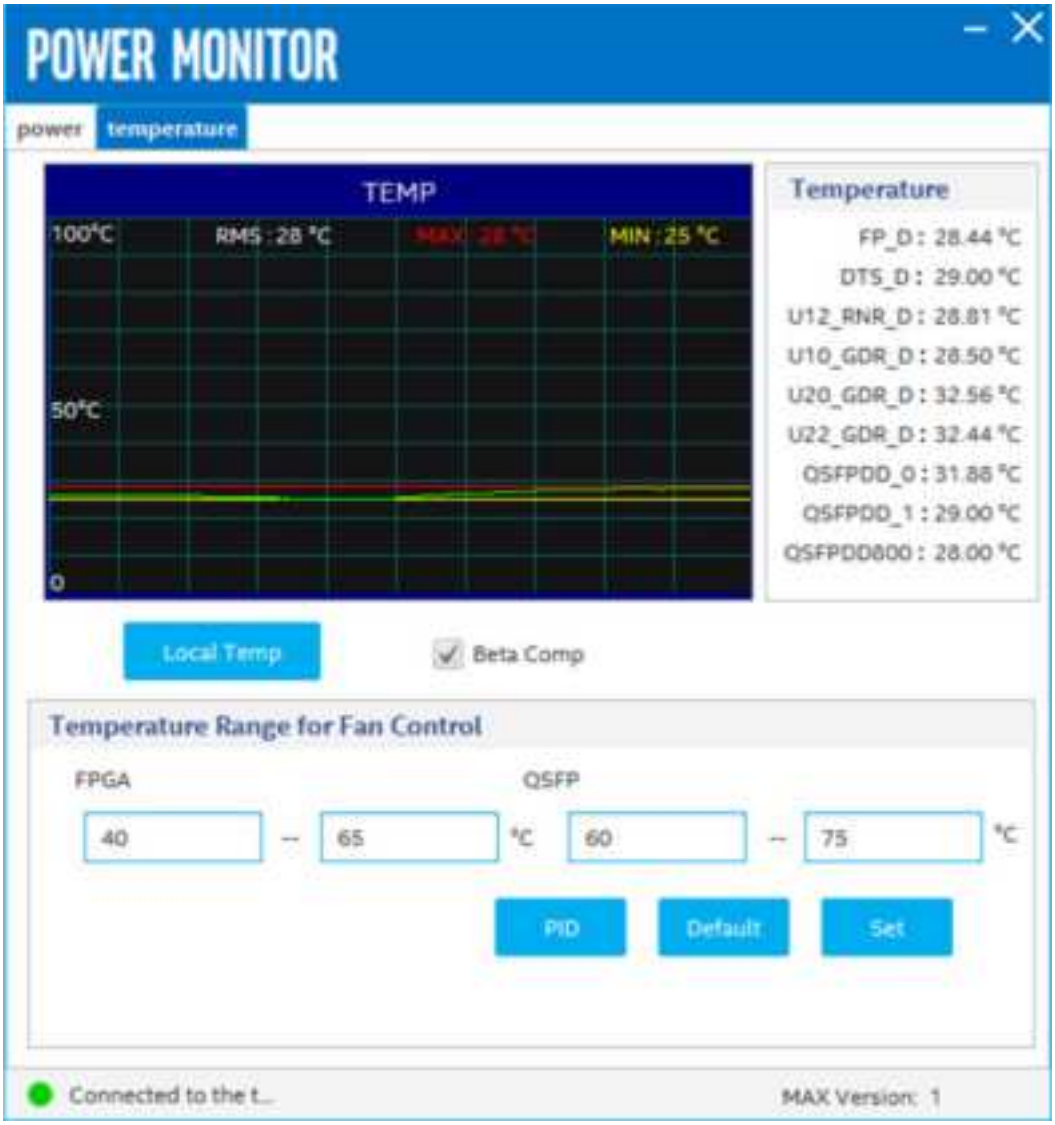
Display Configure

- **Speed Adjustment**: Adjusts the update rate of the current curve.
- **Reset**: Regenerates the graph.

Data Record

When the box is checked, the telemetry data of the selected power rail can be recorded. It saves the data into a `.csv` file in the `log` directory.

Figure 32. Power Monitor GUI—The Temperature Tab



Temperature

Reads the temperature data from the FPGA die, diodes assembled on the PCB, and the QSFPDD modules.

Local Temp

Shows the temperature comparison of the FPGA local temperature sensors and equivalent remote sensors.

Beta Comp

Enables Beta Compensation for the temperature sensing chips.

Temperature Range for Fan Control

Sets and displays the temperature range for the fan control.

Note: To make the temperature range effective, you must set S24[4] based on the instructions in the Default Settings section.

Related Information

Running the BTS GUI on page 17

4.5. Identify Test Pass or Fail based on BTS GUI Test Status

QSFPDD0/QSFPDD1

Plug QSFPDD0/QSFPDD1 loopback module in J16/J17 before you configure the QSFPDD NRZ/PAM4 example build through the BTS GUI.

QSFPDD800

Plug QSFPDD800 loopback module in J18 before you configure the QSFPDD800 PAM4 example build through the BTS GUI.

FMC+

Plug FMC+ loopback module in J34 before you configure the FMC+ NRZ example build through the BTS GUI.

DDR5 DIMM

Plug the DIMM module, which is shipped alone with this development kit, in J13.

5. Development Kit Hardware and Configuration

The Agilex 7 FPGA M-Series HBM2e Development Kit can support multiple application scenarios and configuration modes. You need to change hardware setting for these cases.

Table 5. Supported Configuration Modes

S24 [1:4]	MSEL [2:0]	Configuration Mode
OFF/OFF/OFF/X	111	JTAG
ON/OFF/OFF/X	110	Avalon streaming interface x8 configuration mode

5.1. Configuring FPGA and Accessing HPS Debug Access Port by JTAG

1. JTAG access does not rely on switch S24 settings and system image.
2. Plug the USB cable to J1 or Altera FPGA Download Cable to J7 (set S26 on).
3. Open the Quartus Prime Programmer to configure the Agilex 7 FPGA.
4. Open the RiscFree IDE to connect to and communicate with the HPS Debug Access Port (DAP) through the same JTAG interface.

5.2. Configuring FPGA Device Using the Avalon Streaming Interface x8 Configuration Mode

1. Set S24 to Avalon streaming interface x8 configuration mode first.
2. Default MAX 10 image and hardware design supports the Avalon streaming interface x8 configuration mode only.
3. Power on the board, if the image stored in the QSPI flash U98 has more than one page. Then, use push button S2 to choose page, and S1 to configure the FPGA. The default page is 0.

5.3. Daughter Card

The Agilex 7 FPGA M-Series HBM2e Development Kit supports the HPS OOBE daughter card. You can demonstrate HPS functions through these daughter card and cables.

5.3.1. HPS Out of Box Experience (OOBE) Daughter Card

1. Plug HPS OOBE daughter card in J9.
2. To test HPS Ethernet capability, connect OOBE's RJ45 port J3 to the Internet.
3. To test HPS USB 2.0 capability, connect OOBE's J4 port to a USB cable.
4. To debug HPS from UART terminal applications, use a USB cable to connect to OOBE's J7.
5. OOBE's MicroSD card is pre-programmed with GSRD and OS.
6. General I/O access is provided by push buttons and LED indicators.

6. Custom Projects for the Development Kit

6.1. Add SmartVID Settings in the Quartus Prime QSF File

Agilex 7 silicon assembled on this development kit enables SmartVID feature by default. In order to avoid a Quartus Prime from generating an error due to incomplete SmartVID settings, you must put constraints outlined below into Quartus Prime project QSF file.

Open your Quartus Prime project QSF file, copy and paste the following constraint scripts into the file. Ensure there are no other similar settings with different values.

```
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE LTC3888
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS 55
set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT "LINEAR FORMAT"
set_global_assignment -name PWRMGT_LINEAR_FORMAT_N "-12"
set_global_assignment -name PWRMGT_PAGE_COMMAND_ENABLE ON
set_global_assignment -name PWRMGT_PAGE_COMMAND_PAYLOAD 0
set_global_assignment -name STRATIXV_CONFIGURATION_SCHEME "AVST X8"
set_global_assignment -name USE_PWRMGT_SCL SDM_IO0
set_global_assignment -name USE_PWRMGT_SDA SDM_IO16
set_global_assignment -name USE_CONF_DONE SDM_IO5
set_global_assignment -name USE_NCATTRIP SDM_IO7
set_global_assignment -name USE_HPS_COLD_RESET SDM_IO12
```

6.2. Golden Top

You can use the Golden Top project as the starting point for your designs. It comes loaded with constraints, pin locations, defined I/O standard, direction, and general termination.

7. Document Revision History for the Agilex 7 FPGA M-Series HBM2e Development Kit User Guide

Document Version	Changes
2025.07.30	• Updated *Overview*. • Updated the notes for the S16 and S20 switches in Table: *Factory Default Switch Settings*. • Updated *Performing Board Restore*. • Updated *Restoring Board QSPI Flash with Default Factory Image*. • Updated the steps in *Configuring FPGA Device Using the Avalon Streaming Interface x8 Configuration Mode*. • Updated the *Development Kit Components* appendix chapter: — Updated information about 2x MCIO x8 connector in *Communication Interfaces*. — Updated the table in *Connectors and Cables* • Updated the MCIO cable part number from "HMC74-0631" to "HMC74-1492". • Removed Notes column.
2025.04.07	• Updated the device part number for DK-DEV-AGM039EA in Table: *Ordering Information*. • Updated the *Getting Started* chapter: — Added new topic—*Installing the Ashling* RiscFree Integrated Development Environment (IDE)*. — Removed *Installing the Intel® SoC EDS*. — Updated `demos` and `examples` directory descriptions in Table: *Installed Development Kit Directory Description*. • Updated Table: *Factory Default Switch Settings* in the *Development Kit Setup* chapter. • Updated the *Board Test System* chapter: — Updated *Setting Up the Quartus Prime Software for BTS Operation*. — Updated step 2 in *Running the BTS GUI*. — Updated all figures. — Removed the **QSFPDD PRESENT STATUS** control information in *The GPIO Tab*. — Updated and retitled topic *Transceiver Designs* to *The XCVR Tab*. — Updated the **Detail** description in *The QSFPDD NRZ Tab*. — Added new section—*The Memory Tab*. — Updated the **Import** description in *Si5518*. — Updated *Monitor On-Board Power Regulator through Power Monitor GUI*: • Updated the **Local Temp** description. • Added a note for the **Temperature Range for Fan Control**. • Updated *Configuring FPGA and Accessing HPS Debug Access Port by JTAG* in the *Development Kit Hardware and Configuration* chapter. • Updated Table: *Agilex 7 FPGA M-Series HBM2e Development Kit References* in the *Developer Resources* chapter. • Updated the description for FPGA and HPS shared external memory interface (LPDDR5 component) in the *Memory Interfaces* appendix chapter. • Made editorial edits throughout the document. • Updated the document for the latest branding standards.

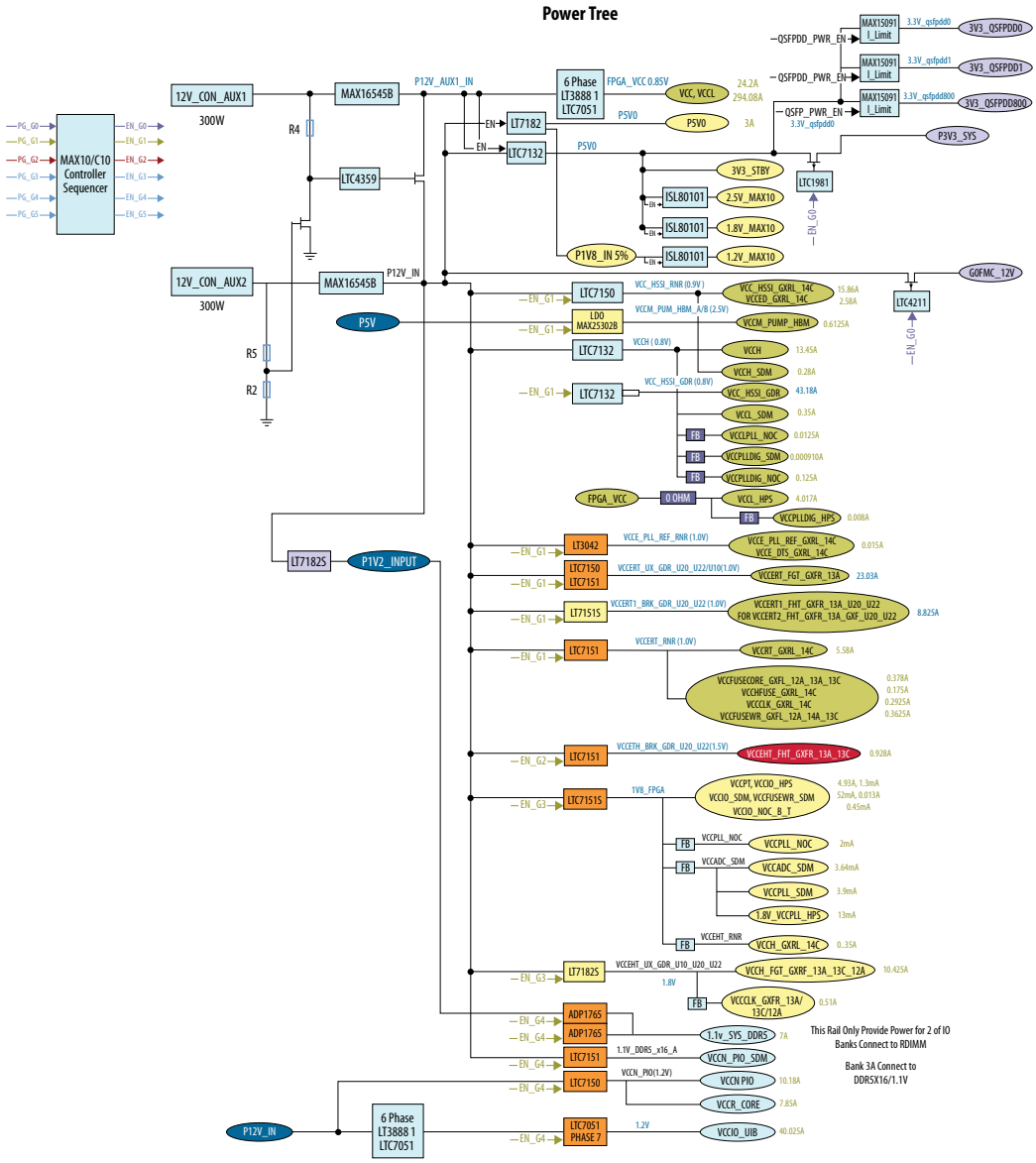
continued...

Document Version	Changes
2024.12.04	• Updated the *Overview* chapter: — Updated Table: *Ordering Information*. — Retitled figure *Agilex 7 FPGA M-Series HBM2e Development Kit Top* to Agilex 7 FPGA M-Series HBM2e Development Kit—Top View. • Updated the *Getting Started* chapter: — Added new topics: • *Before You Begin* • *Handling the Board* • *Installing the Quartus Prime Pro Edition Software* • *Installing the Intel SoC EDS* • *Installing the Development Kit* • *Installing the Altera FPGA Download Cable II Driver* — Updated *Quartus Prime Software and Driver Installation*. — Removed *Design Examples*. • Updated the *Board Test System* chapter: — Updated the following topics: • *Downloading OpenJDK* • *Installing OpenJDK and OpenJFX* • *Transceiver Designs* • *Control the On-board Clock through Clock Controller GUI* • *Monitor On-Board Power Regulator through Power Monitor GUI* — Retitled topic *Installing the Quartus Prime Software* to *Setting Up the Quartus Prime Software for BTS Operation*. • Updated information about MCIO port in the *Appendix A.5—Communication Interfaces*. • Added new appendix chapter—*Developer Resources*. • Retitled appendix chapter *Additional Information* to *Safety and Regulatory Compliance Information*. • Restructured the document to improve clarity and for ease of reference. • Updated the document for the latest branding standards.
2024.05.14	• Retitled the document from *Intel Agilex® 7 M-Series HBM2e Development Kit User Guide* to *Agilex 7 FPGA M-Series HBM2e Development Kit User Guide*. • Removed mention of Agilex 9 from the document. • Removed information related to 256 MB QSPI flash daughter card in Appendix: *Daughter Cards*. • Updated document per latest branding standards.
2024.01.24	Updated Figure: *Intel Agilex 7 FPGA M-Series HBM2e Development Kit Block Diagram*.
2023.11.03	Initial release.

A. Development Kit Components

A.1. Power

Figure 33. Power Tree



Onboard hot-plug circuit shuts down all power rails when the total power is over 360 W (30 A).

UB2/PWR MAX 10 shuts down significant power rails when one or more good power indicators is low due to a power fault.

UB2/PWR MAX 10 also shuts down significant power rails when temperature cross the acceptable range.

A.2. Clocks

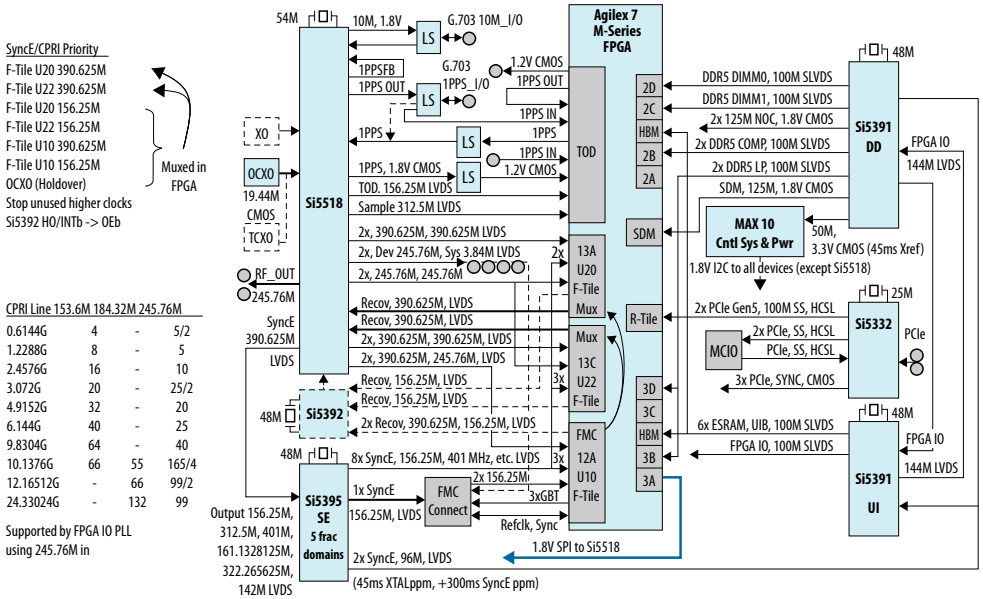
Table 6. Default Clock Frequency

Schematic Signal Name	Default Frequency (MHz)
SAMPLE_CLK_312_50MHZ_P/N	312.50
TOD_MASTER_156_25MHZ_P/N	156.25
1PPS_SI5518	100
SI5518_10MHZ_OUT	10
CLK_156_25MHZ_5391_P/N	156.25
CLK_390_625MHZ_1P/1N	390.625
CLK_390_625MHZ_2P/2N	390.625
CLK_390_625MHZ_3P/3N	390.625
CLK_3_84MHZ_SMA_P/N	3.84
CLK_245_76MHZ_SMA_P/N	245.76
CLK_245_76MHZ_1P/1N	245.76
CLK_245_76MHZ_2P/2N	245.76
CLK_245_76MHZ_3P/3N	245.76
CLK_245_76MHZ_4P/4N	245.76
CLK_390_625MHZ_4P/4N	390.625
CLK_390_625MHZ_5P/5N	390.625
CLK_156_25MHZ_U22_P/N	156.25
CLK_156_25MHZ_1_FMC_P/N	156.25
CLK_156_25MHZ_2_FMC_P/N	156.25
CLK_156_25MHZ_3_FMC_P/N	156.25
CLK_156_25MHZ_4_U22_P/N	156.25
CLK_156_25MHZ_5_U22_P/N	156.25
CLK_156_25MHZ_6_U20_P/N	156.25
CLK_156_25MHZ_7_U20_P/N	156.25
CLK_156_25MHZ_8_FMC_CON_P/N	156.25
CLK_156_25MHZ_SI5391_1_P/N	156.25

continued...

Schematic Signal Name	Default Frequency (MHz)
CLK_156_25MHZ_SYNCE_DDR_P/N	156.25
CLK_156_25_MHZ_SI5392	156.25
CLK_UIB0_P/N	100
CLK_UIB0_FBR0_P/N	100
CLK_UIB0_FBR1_P/N	100
CLK_UIB1_P/N	100
FPGA_IO_CLK0_P/N	100
FPGA_IO_CLK5_P/N	100
CLK_UIB1_FBR0_P/N	100
CLK_UIB1_FBR1_P/N	100
CLK_100M_RP_0_P/N	100
CLK_100M_PCIE1_P/N	100
CLK_100M_PCIE0_P/N	100
CLK_100M_RP_1_P/N	100
CLK_100M_RP_2_P/N	100
CLK_SI5332_U10_IO_PLL_DP	100
CLK_SI5332_U20_IO_PLL_DP	100
CLK_SI5332_U22_IO_PLL_DP	100
CLK_DDR5_RDIMM_A0_DP/DN	100
CLK_DDR5_RDIMM_A1_DP/DN	100
CLK_DDR5_COM_DP/DN	100
CLK_DDR5_COM_HPS_DP/DN	100
CLK_LP5_B1_P/N	100
CLK_LP5_A1_P/N	100
FPGA_IO_CLK_2_P/N	100
CLK_NOC_PLL0	100
CLK_NOC_PLL1	100
FPGA_SDM_1V8_125M_CLK	125

Figure 34. Clock Tree



A.3. General Input/Output

Table 7. MAX 10 and FPGA

Schematic Signal Name	Description
FP8_GPIO0	Controls the video FMC card PPM up
FP8_GPIO1	Controls the video FMC card PPM down
FP8_GPIO2	MAX10_SI5518_1V2_RSTN
FP8_GPIO3	FP_CPU_RESETN
FP8_GPIO4	USER_RESETN
FP8_GPIO [10:5]	Si5518 SPI interface (FPGA interface 1588 clock)
FP8_GPIO [18:11]	Any desired bus communication between Agilex 7 FPGA M-Series HBM2e Development Kit and MAX 10
FP8_GPIO19	FMC_PERSTN in RP mode
Other FP8_GPIO	Controls the 1588 clock

Table 8. System MAX 10

Schematic Signal Name	Description
FPGA_3V3_LED0/DS2	Reserved
FPGA_3V3_LED01/DS1	Reserved
FPGA_3V3_LED02/DS3	Reserved
FPGA_3V3_LED03/DS4	Reserved
QFPDD_0_3V3_LED0/DS5	QSFPDD PORT 0 LED0

continued...

Schematic Signal Name	Description
QFPDD_0_3V3_LED1/DS6	QSFPDD PORT 0 LED1
QFPDD_1_3V3_LED0/DS11	QSFPDD PORT 1 LED0
QFPDD_1_3V3_LED1/DS12	QSFPDD PORT 1 LED1
QFPDD800_3V3_LED0/DS13	QSFPDD800 LED0
QFPDD800_3V3_LED1/DS14	QSFPDD800 LED1
MAX10_USER_LED0	Reserved
OVERTEMP_N/D10,D19	F-Tile die, R-Tile die, core die, board overtemp red LED is on
MAX_CONFIG_DONE/DS10	LED is on when MAX 10 configuration is done
S12	FPGA_RESETn
S13	HPS_COLD_RESETn
S9	PCIE_PERST_N
S15	USER RESETN
S2	MAX10 (USER_PB0)
S1	MAX10 (USER_PB1)
S21	CLK_SI5392_RST_R_N
S18	CLK_SI5391_2_RESET_N
S23	CLK_SI5391_RESET_N
SW7	Power recycle
QSFPDD_I2C_3V3_EN_N	• 0: MAX 10 access to QSFPDD/QSFPDD800 EEPROM • 1: Agilex 7 M-Series HBM2e access to QSFPDD/QSFPDD800 EEPROM
MAX10_1V8__SI5391_1_RSTN	• 0: SI5391 U14 RESETN mode • 1: Normal (default)
HPS_RESETN	• 0: HPS RESETN • 1: Normal (default)
FMC_12v_EN	0: FMC_12V OFF 1: FMC_12V ON (DEFAULT)
SVID_I2C_EN	• Before power OK: 0 • After power OK: S_control_gui[1], = 1 by default
PWRGD_DDR5_MAX_RD	• Before power OK: 0 • After power OK: 1
MAX10_SI5518_1V2_RSTN (control by FP8)	• Before power OK: 0 • After power OK: 1
CLKMUX_OE_1V8_EN	Enable all the clocks on the development kit. It is always 0.
CLK_SI5392_RST_R_N	• Before power OK: 0 • After power OK: 1
Clk_si5391_2_reset_n	• Before power OK: 0 • After power OK: 1

continued...

Schematic Signal Name	Description
usb_disablen	• 0: external Altera FPGA Download Cable is inserted • 1: no external Altera FPGA Download Cable inserted
Fx2_resetn	• 0: On-board Altera FPGA Download Cable II is under reset • 1: 0: On-board Altera FPGA Download Cable II is out of reset
BOARD_PWR_GOOD_LED/DS15	FPGA Power Good, Agilex 7 M-Series HBM2e power sequences are successful and all the power rails on board are good.
MAX_1V2_FPGA_SPARE[7:0]	Reserved GPIO between the system MAX 10 and Agilex 7 M-Series HBM2e. All 8 signals have option pull up and pull down, all can be GPIO signals, I^2C, SPI bus between MAX 10 and Agilex 7 M-Series HBM2e, or any status, alert, and other signals between MAX 10 and Agilex 7 M-Series HBM2e. By default, all 8 signals have pull up 4.7K.

A.4. Memory Interfaces

FPGA Dedicated External Memory Interface (DDR5 RDIMM)

Agilex 7 M-Series HBM2e Development Kit supports 16 GB DDR5 RDIMM MTC10F1084S1RC56BG1. It is single slot. It targets up to 5600 Mbps.

FPGA Dedicated External Memory Interface (DDR5 Component)

DDR5 component interface is a 40 bit, including 8-bit ECC support, single rank configuration based on x16 component. It targets up to 5600 Mbps. It targets up to 5600 Mbps. Three MT60B1G16HC-56B:G from Micron are soldered down on the development kit.

FPGA and HPS Shared External Memory Interface (LPDDR5 Component)

LPDDR5 component interface is a 16 bit, two channels configuration. It targets up to 5500 Mbps. MT62F512M32D2DS-031 AUT:B from Micron is soldered down on the development kit.

FPGA and HPS Shared External Memory Interface (DDR5 Component)

DDR5 component interface is a 40 bit, including 8-bit ECC support, single rank configuration based on x16 component. It targets up to 5600 Mbps. Three MT60B1G16HC-56B:G from Micron are soldered down on the development kit. Both Agilex 7 FPGA fabric and HPS can access this external memory interface. However, they cannot be accessed at the same time.

A.5. Communication Interfaces

MCIO Port

The MCIO slot is a PCIe 5.0 x16 port which fans out from Agilex 7 FPGA M-Series R-Tile. This port is designed to meet the standard MCIO pinout. PCIE1_PERST0_N signal can act as output and input respectively.

Table 9. MCIO Port

Schematic Signal Name	Description
PCIE_PERSTn_A	PCIe endpoint/root port reset
PCIE_ALERTn_A	PCIe Alert
PCIE_100M_REF_AP/AN	PCIe reference clock
PCIE_SCL_A/SDA_A	PCIe I^2C bus
PCIE_TX_P/N[15:0]	Transceiver TX
PCIE_RX_P/N[15:0]	Transceiver RX

2x MCIO x8 Connector

The recommended MCIO cable to use with MCIO connector (Uxx) is not included as part of the development kit and must be acquired directly from third party supplier (Amphenol p/n = HMC74-1492).

QSFPDD

The Agilex 7 FPGA M-Series HBM2e Development Kit supports 2x QSFPDD ports. The QSFDD port fans out from Agilex 7 FPGA M-Series F-Tile (FGT). All 8 channels per QSFPDD can run up to 32G NRZ and 58G PAM4.

QSFPDD800

The Agilex 7 FPGA M-Series HBM2e Development Kit supports 1X QSFPDD800 port. The QSFDD800 port fans out from Agilex 7 FPGA M-Series F-Tile (FHT). All 8 channels per QSFPDD800 can run up to 32G NRZ, 58G PAM4, and 116G.

Table 10. QSFPDD Connector 0 (J16)

Schematic Signal Name	Description
QSFPDD0_3V3_MODPRS_L	Module present
QSFPDD0_3V3_RESET_L	Module reset
QSFPDD0_3V3_MODSEL_L	Mode select
QSFPDD0_3V3_LPMODE	Initial mode
QSFPDD0_3V3_INT_L	Interrupt
I2C_QSFPDD0_3V3_SCL	I^2C clock
I2C_QSFPDD0_3V3_SDA	I^2C data
QSFPDD0_TX_P/N[0:7]	Transceiver TX
QSFPDD0_RX_P/N[0:7]	Transceiver RX

Table 11. QSFPDD Connector 1 (J17)

Schematic Signal Name	Description
QSFPDD1_3V3_MODPRS_L	Module present
QSFPDD1_3V3_RESET_L	Module reset

continued...

Schematic Signal Name	Description
QSFPDD1_3V3_MODSEL_L	Mode select
QSFPDD1_3V3_LPMODE	Initial mode
QSFPDD1_3V3_INT_L	Interrupt
I2C_QSFPDD1_3V3_SCL	I^2C clock
I2C_QSFPDD1_3V3_SDA	I^2C data
QSFPDD1_TX_P/N[0:7]	Transceiver TX
QSFPDD1_RX_P/N[0:7]	Transceiver RX

Table 12. QSFPDD800 (J18)

Schematic Signal Name	Description
QSFPDD800_3V3_MODPRS_L	Module present
QSFPDD800_3V3_RESET_L	Module reset
QSFPDD800_3V3_MODSEL_L	Mode select
QSFPDD800_3V3_LPMODE	Initial mode
QSFPDD800_3V3_INT_L	Interrupt
I2C_QSFPDD800_3V3_SCL	I^2C clock
I2C_QSFPDD800_3V3_SDA	I^2C data
QSFPDD800_TX_P/N[0:3]	Transceiver TX
QSFPDD800_RX_P/N[0:3]	Transceiver RX

FMC+ Connector

The Agilex 7 FPGA M-Series HBM2e Development Kit supports FMC+ slots for functional expandability. The x16 FGT lanes from bank 12A are terminated to the FMC + (J34) connector and the 64 I/O signals from bank 2A connect to the FMC+ (J34) connector. Auxiliary signals are controlled by the system MAX 10.

USB Type-C Connector

The Agilex 7 FPGA M-Series HBM2e Development Kit has hardware support for the USB Type-C connector, which supports DP1.4 specification or USB 3.1 functionality through MUX (TUSB1146). This feature is yet to be validated and implemented.

Serial Buses

The SDM I/Os (SDM_IO16/0) and MAX 10 I/Os (VCCL_SDA/SCL) share the same I^2C bus which communicate with Agilex 7 FPGA core regulators. By default, SDM acts as SmartVID master and system MAX 10 act as Power GUI master in this chain.

The system MAX 10 I/Os (PMB_SDA/SCL) manages the second I^2C bus which access all I^2C slave regulator except Agilex 7 FPGA core regulators.

The system MAX 10 supports I^2C master dedicated to clock-related devices (CLK_I2C_SDA/SCL), which manages 3# clock devices and also connected to the HPS I/Os (HPS_GPIO30/31) through level translator.

Another I2C master instance from the system MAX 10 (VCXO_I2C_SDA/SCL) controls the on board VCXO and Si5394 clock generator.

The Agilex 7 FPGA also manages QSFPDD800, 2x QSFPDD, 1 RDIMM DDR5 I2C buses, SDI transceivers, and ZL30733 clock synthesizer device.

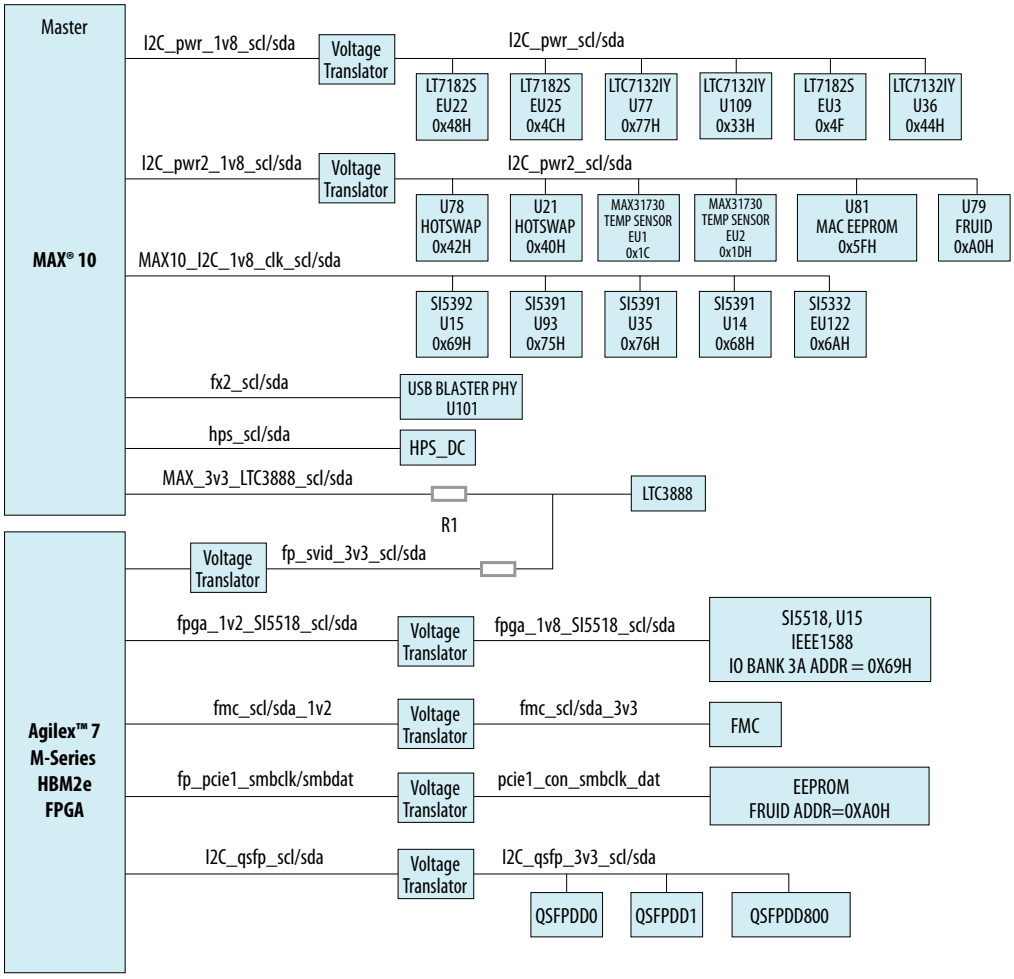
Table 13. I2C Debug Headers

Schematic Signal Name	Description
PMB_SCL/SDA	VRs I2C header J5 and J91
CLK_I2C_SDA/SCL_3V3	All clock devices I2C header J40
HPS_SCL/HPS_SDA	HPS I2C interface MAX 10
FMC_SCL_1V2 FMC_SDA_1V2	FMC+ I2C interface Agilex 7 M-Series HBM2e
FP_I3C_2C_DIMM_SCL FP_I3C_2C_DIMM_SDA	DDR5_I3C_RDIMM interface Agilex 7 M-Series HBM2e
MAX10_I2C_2C_DIMM_SCL MAX10_I2C_2C_DIMM_SDA	DDR5_I3C_RDIMM interface Agilex 7 M-Series HBM2e
I2C_PWR2_SCL I2C_PWR2_SDA	Agilex 7 M-Series HBM2e R-Tile die, 3 F-Tile die, I/O core die board temperature sense, I2C interface MAX 10
FX2_SCL/FX2_SDA	USB PHY I2C interface MAX 10
MAX2237B_SCL/SDA	SI569_148.50 MHz interface MAX 10 can adjust the frequency for FMC+ video interface card

Table 14. SPI Debug Headers for SI5518 Clocks

Schematic Signal Name	Description
FPGA_SI5518_1V8_GPIO3	Si5518 SPI bus, debug connector J22 and J41
FPGA_SI5518_A0_1V8_CSB	
I2C_1V8_CLK_GUI_SDA	
I2C_1V8_CLK_GUI_SCL	

Figure 35. I²C Serial Bus



A.6. Daughter Card

HPS IO48 OOBE Daughter Card

- 1x RGMII 10/100/1000 Mbps Ethernet port: Standard RJ-45
- 1x UART port: Standard USB Mini-B Receptacle
- 1x Micro SD Card Connector: Standard Micro SD Card Socket
- 1x USB 2.0 port: Standard USB Micro-AB Receptacle
- 1x Mictor 38-pin connector (JTAG only without Trace signals)
- HPS dedicated JTAG pins are connected with both mother board JTAG chain and Mictor 38-pin header

- I^2C: HPS I^2C port
- GPIO
  - 2x Push buttons
  - 3x LEDs
  - 1x Ethernet Interrupt from Ethernet PHY
  - 1x USB over-current indicator
- HPS Clock: 25 MHz oscillator

A.7. Connectors and Cables

Table 15. Connectors and Cables

Connectors and Cables	Part Number	Switch Reference
QSFPDD loopback module	NLNAMB0001 (Amphenol)	J16 J17
QSFP-DD800 loopback type 1	ML4062-LB-112 (Multilane)	J18
MCIO cable	HMC74-1492 (Amphenol)	J10 J11

B. Developer Resources

Use the following links to check the Altera website for other related information.

Table 16. Agilex 7 FPGA M-Series HBM2e Development Kit References

Reference	Description
Agilex 7 FPGA M-Series HBM2e Development Kit page	Latest board design files, reference designs, and kit installation for Windows* and Linux*.
Rocketboard.org	Open-source community website supporting SoC development including Altera and Partner SoC development kit targets and related designs and documentation.
Ashling* RiscFree* Integrated Development Environment (IDE) for Altera FPGAs User Guide	Describes the RiscFree integrated development environment (IDE) for Altera FPGAs Arm-based HPS and Nios V core processors.
Agilex 7 FPGA Design Hub	The Agilex 7 FPGA Design Hub is a comprehensive resource hub that provides a structured approach for developing FPGA-based platforms.
AN 958: Board Design Guidelines	Board design-related resources for Altera devices. Its goal is to help you implement successful high-speed PCBs that integrate device(s) and other elements.
Agilex 7 Power Management User Guide	Describes the Agilex 7 devices power-optimization features, power-up and power-down sequences, power distribution network, voltage and temperature monitoring systems with a design example to read the TSDs, and power optimization techniques.
Agilex 7 Power Distribution Network Design Guidelines	Provides information for the Agilex 7 device family power distribution network (PDN) design guidelines.
FPGA SmartVID	SmartVID is a feature on select Altera FPGAs where the device identifies the optimal voltage that it should be operated at, and provides this information to the power regulator via the PMBus. The term represents Smart Voltage IDentification (SmartVID).
SmartVID Debug Checklist and Voltage Regulator Guidelines	Provides the checklist to assist you to rule out the possible causes of configuration failure due to SmartVID.
Agilex 7 Configuration User Guide	Provides the configuration process, the device pins required for configuration, the available configuration schemes, remote system updates, and debugging. This user guide also provides an overview of the secure device manager (SDM) which manages security for the configuration bitstream.
Documentation: Agilex 7	Agilex 7 device documentation.
Cadence* Capture CIS Schematic Symbols	Agilex 7 OrCAD symbols.

C. Safety and Regulatory Compliance Information

C.1. Safety and Regulatory Information

ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE & UKCA mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

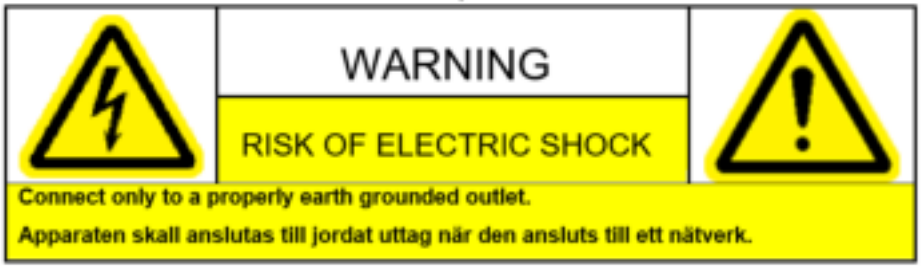
C.1.1. Safety Warnings

Power Supply Hazardous Voltage

AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.

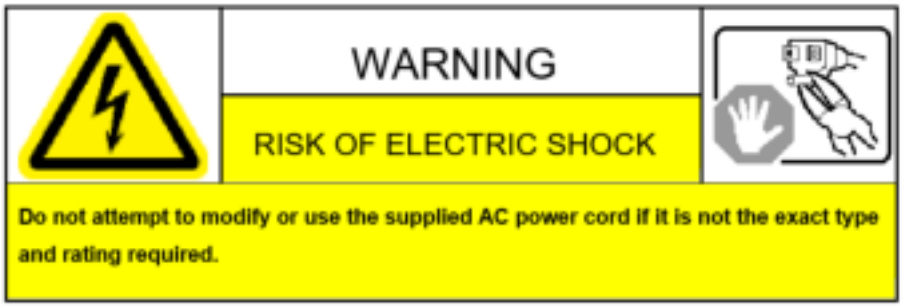
Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.



System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product is attached to is also connected to properly wired and grounded receptacles.



Power Cord Requirements

The plug on the power cord must be a grounding-type male plug designed for use in your region. It must have certification marks showing certification by an agency in your region. The connector that plugs into the appliance inlet of the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord, and do not use it with adapters. Use only certified power supply cord with appropriate gauge, designed for use in your region.

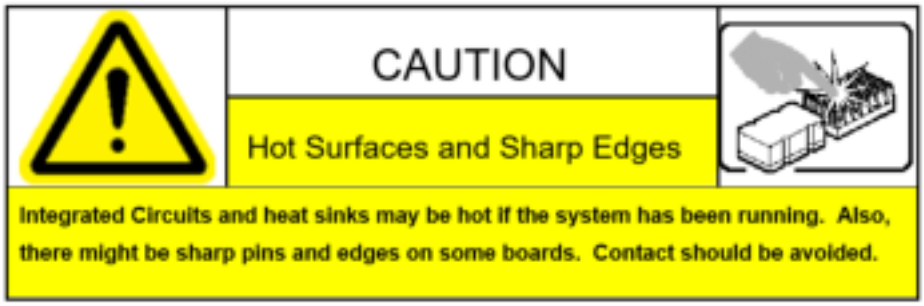
Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

C.1.2. Safety Cautions



Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.

Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, you are required to take measures to eliminate this interference.

Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.

Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

Attention: Please return this product to Altera for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

Lithium Ion Battery Warnings

Lithium Battery: Risk of explosion if the lithium battery is replaced by an incorrect type. Risk of fire, explosion, or chemical burn if the battery is mistreated (punctured or crushed). Do not attempt to disassemble. Do not incinerate. Observe proper polarity when replacing battery. Do not dispose—the battery is intended to be serviced and disposed by qualified Altera service personnel only.

Perchlorate Material: Special handling may apply. For more details, refer to www.dtsc.ca.gov/hazardouswaste/perchlorate. This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best Management Practices for Perchlorate Materials. This product includes a battery which contains perchlorate material.

Taiwan battery recycling:

(Translation - please recycle batteries)

Please return this product to Altera for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of product in unsorted municipal waste.

C.2. Compliance Information

CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2014/30/EU. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.

Mouser Electronics

Authorized Distributor

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Altera:

DK-DEV-AGM039FES