EC2x&EG2x Series

PCB Design Guide

LTE Standard Module Series

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	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
1.0	2020-07-23	Lim PENG	Initial
1.1	2020-07-24	Lim PENG	Revised few typos.
1.2	2024-05-27	Harry HA	1. Added applicable modules EG21-GL and EG25-GL. 2. Updated the overview of TE-A 1st layer (Figure 1). 3. Updated high-priority signals to be designed (TE-A 1st layer) (Figure 2). 4. Updated the capacitance value of VBAT_BB according to different modules (Chapter 3.1.2). 5. Updated the VBAT and sensitive signal traces (TE-A 1st layer) (Figure 7). 6. Added the notification about PWRKEY and RESET_N signal traces (Chapter 3.2). 7. Deleted the information about GPIO interfaces 8. Deleted the detailed information about reference design of RF layout which is introduced in the hardware design of each module (Chapter 3.10.2).

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1 Introduction

This document mainly introduces the PCB reference design for Quectel LTE standard EC2x and EG2x families, and it takes EC25-TE-A, FC20-TE-A and UMTS&LTE EVB as examples.

1.1. Applicable Modules

Table 1: Applicable Modules

Module Family	Module series	Model
EC2x	-	EC20-CE
	EC21	EC21-E/-A/-V/-AU/-EU/-AUT/-J/-KL/-AUX/-EUX/-IN
	EC25	EC25-E/-A/-V/-J/-AU/-AUX/-AF/-AFX/-AFXD/-EU/-EUX/-EM/ -ADL/-AFDL
EG2x	-	EG21-G
		EG25-G
	-	EG21-GL
		EG25-GL

1.2. Special Mark

Table 2: Special Mark

Mark	Definition
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 PCB Design Overview

2.1. Footprint and Keepout Area

- A 4-layer PCB is strongly recommended.
- First, check whether the module's footprint is of the latest version provided by Quectel. For specific footprint of each module, please refer to ***documents [1]***, ***[2]***, ***[3]***, ***[4]*** or ***[5]***.
- Do not design pins 73–84 and do not route the keepout area with any traces or copper.

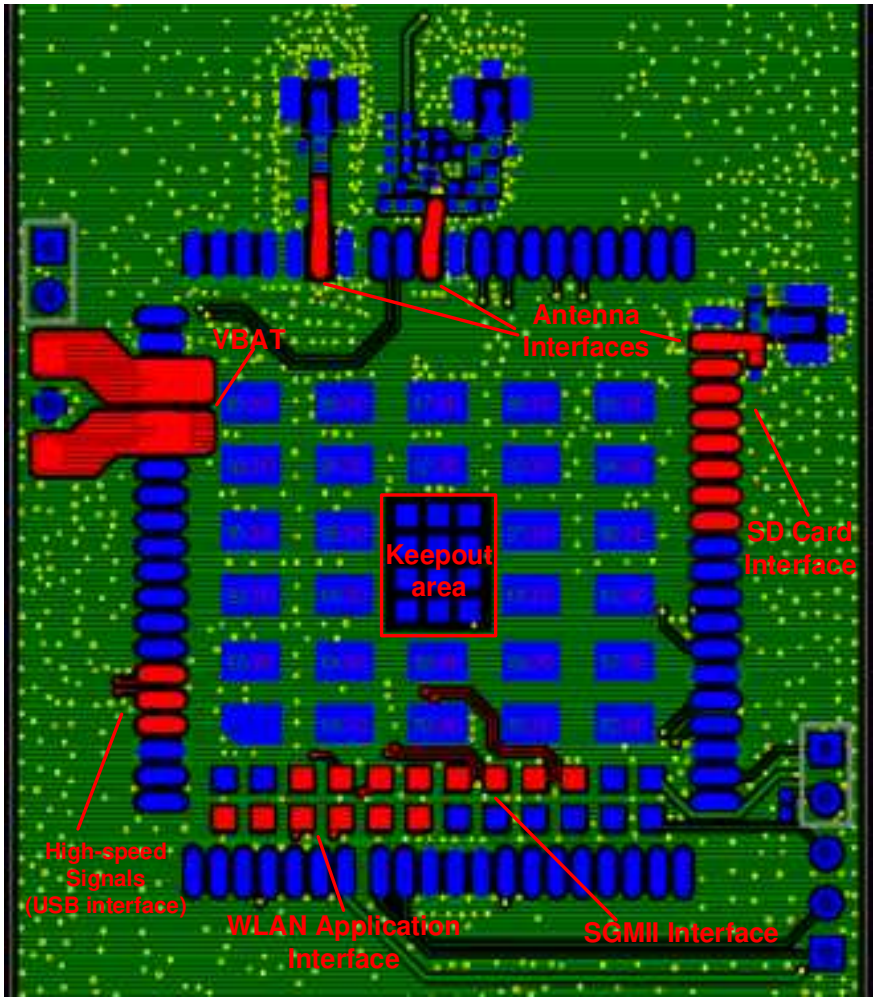

Figure 1: Overview of TE-A 1st Layer

2.2. Design Priorities and Considerations for PCB Traces

2.2.1. Design Priorities

Design the PCB traces according to the recommended order as follows:

- Antenna traces.
- High-speed signal (SGMII, SDIO and USB) traces.
- Power supply traces, such as VBAT_BB, VBAT_RF, USIM_VDD, VDD_EXT, SD_PU_VDD for EG2x-GL and VDD_SDIO for EG2x-G and EC2x family.
- Other traces.

2.2.2. Design Considerations

- The radiation of PCM interface and power supply could affect RF performance, so keep them away from RF signal traces and components.
- Drill as fewer vias as possible for high-speed signal traces (SGMII, SDIO and USB interfaces) since vias will affect the continuity of the impedance. Route the differential pair traces on the same layer.
- To minimize the signal return path, the GND vias for signals such as USB, SDIO, SGMII, PWRKEY and RESET_N should be close to the vias when the traces change layers.

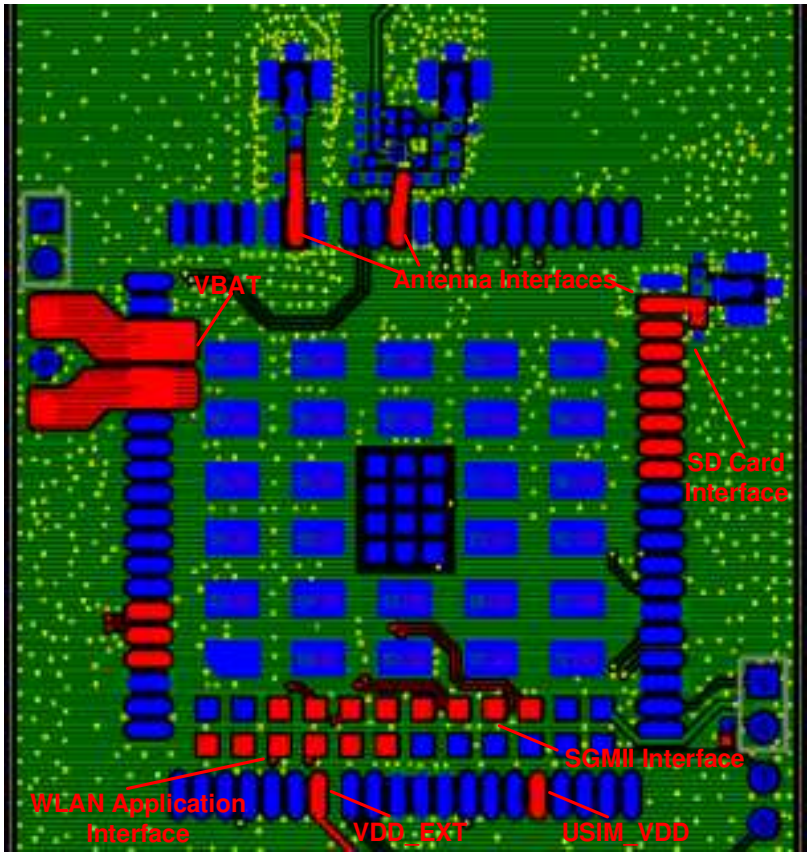

Figure 2: High-priority Signals to Be Designed (TE-A 1st Layer)

3 Interface Design

3.1. Power Supply

3.1.1. DC-DC Converter

- Place the DC-DC converter away from the sensitive signal traces such as SDIO, USB, SGMII, audio and RF. If possible, shield DC-DC converter with shielding cover and reserve spacing for shielding frame.
- Place the capacitor and inductor for the DC-DC converter as close as possible to the corresponding pins of the DC-DC converter to minimize the loop area.
- Place output capacitors near input capacitors to share common ground area on outer layers.
- Provide adequate thermal relief area at the gound area on outer layers along with any additional inner ground planes.

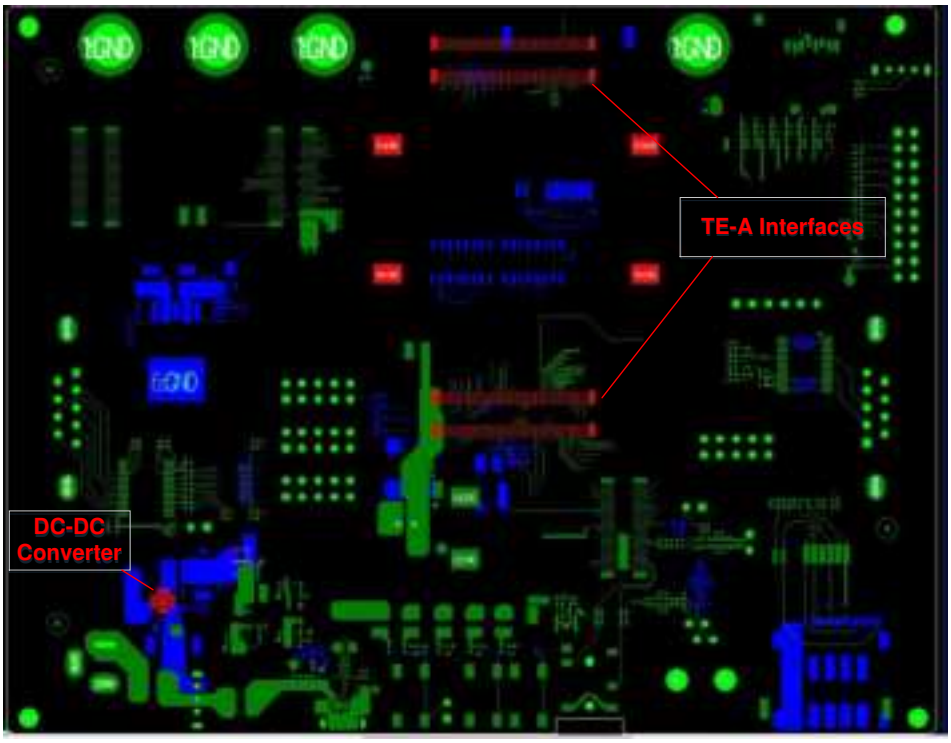

Figure 3: DC-DC Converter (EVB 4th Layer) and Module Interfaces On TE-A (EVB 1st Layer)

3.1.2. VBAT

- Place 100 μF, 100 nF, 33 pF and 10/100 pF [1] for VBAT_BB, and 100 μF, 100 nF, 33 pF and 10 pF for VBAT_RF. The smaller the capacitance is, the closer the compositors are to the four VBAT pins.
- The maximum power consumption of VBAT_RF is 1.8 A and its trace width is recommended to be no less than 2 mm. The maximum power consumption of VBAT_BB is 0.8 A and its trace width is recommended to be no less than 1 mm. Moreover, please pay attention to the capability and quantity of vias in the traces. The GND vias of the filter capacitors for VBAT should be drilled down to the nearest main ground.

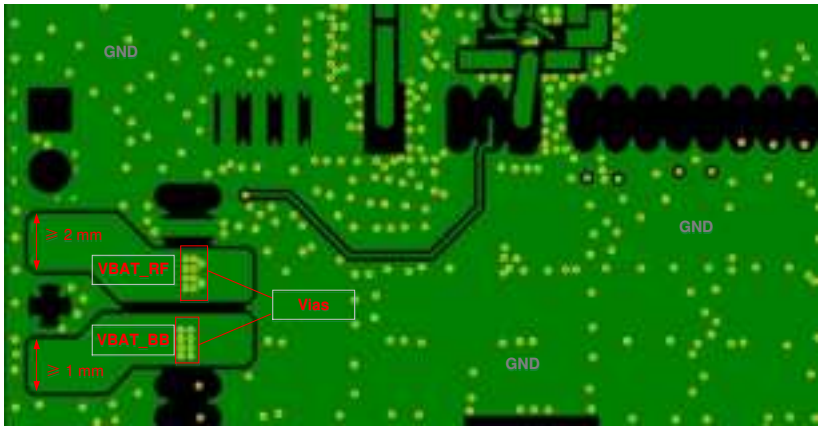

Figure 4: VBAT Traces (TE-A 1st Layer)

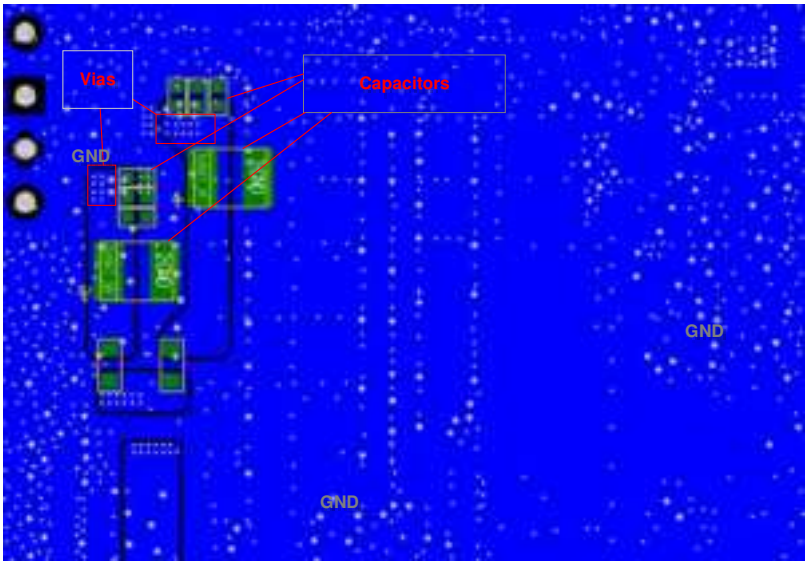

Figure 5: Traces of VBAT with Capacitors (TE-A 4th Layer)

[1] For EC20-CE, EC21-E/-AU/-EU/-AUT/-J/-KL/-AUX/-EUX/-IN, EC25-E/-J/-AU/-AUX/-EU/-EUX/-EM, the capacitance value is 10 pF. For EC21-A/-V, EC25-A/-V/-AF/-AFX/-AFXD/-ADL/-AFDL, EG2x series, the capacitance value is 100 pF.

- Place the TVS components for VBAT close to the module's VBAT_BB and VBAT_RF pins.
- VBAT traces should be away from sensitive signal traces such as SDIO, USB, SGMII, USB audio and RF to avoid paralleling or crossing with them.
- A layer with VBAT traces and reference ground plane is recommended. When a power plane is used, a complete ground plane should be added in adjacent layer as the reference plane.

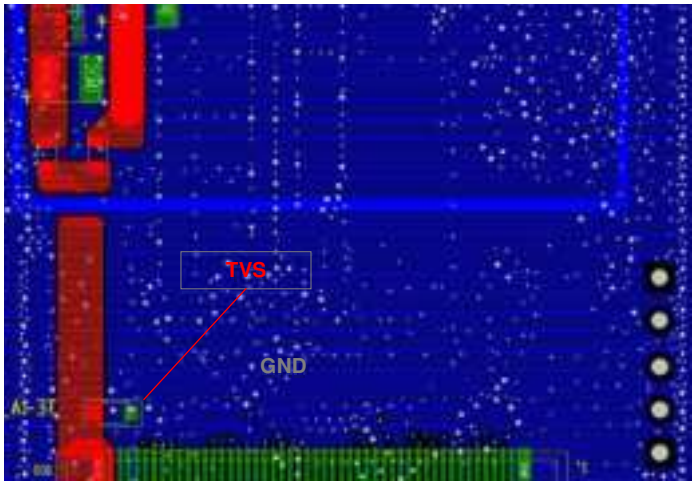

Figure 6: Traces of VBAT with a TVS (TE-A 4th Layer)

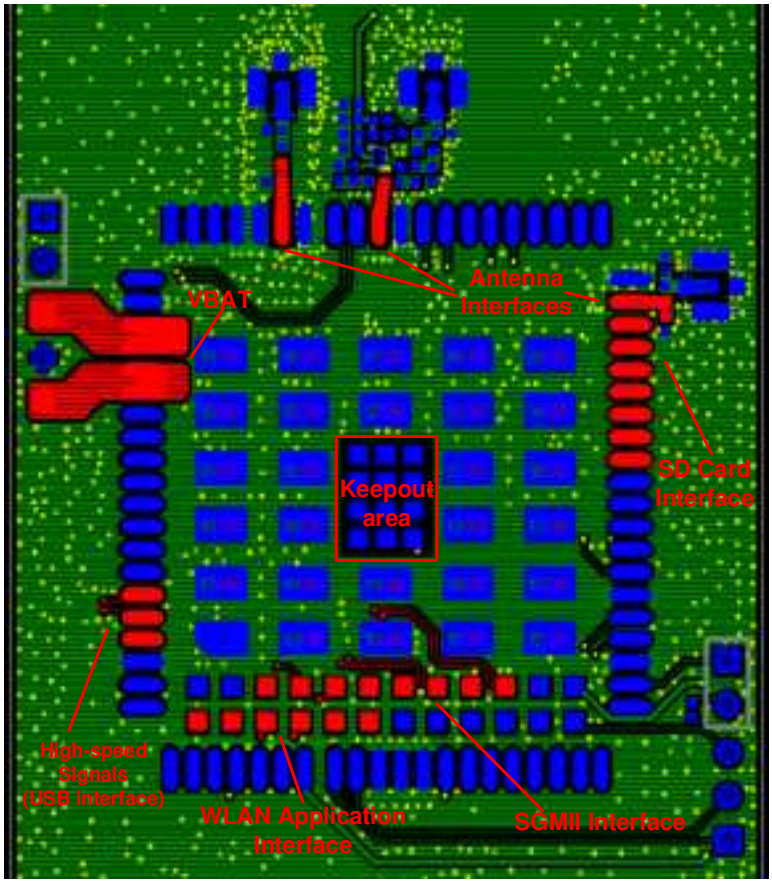

Figure 7: VBAT & Sensitive Signal Traces (TE-A 1st Layer)

3.2. PWRKEY & RESET_N

- PWRKEY and RESET_N signal traces are recommended to be surrounded with ground.
- If filter capacitors for PWRKEY and RESET_N are required, put them near the two pins.
- Keep PWRKEY and RESET_N signal traces away from high current and interference sources.

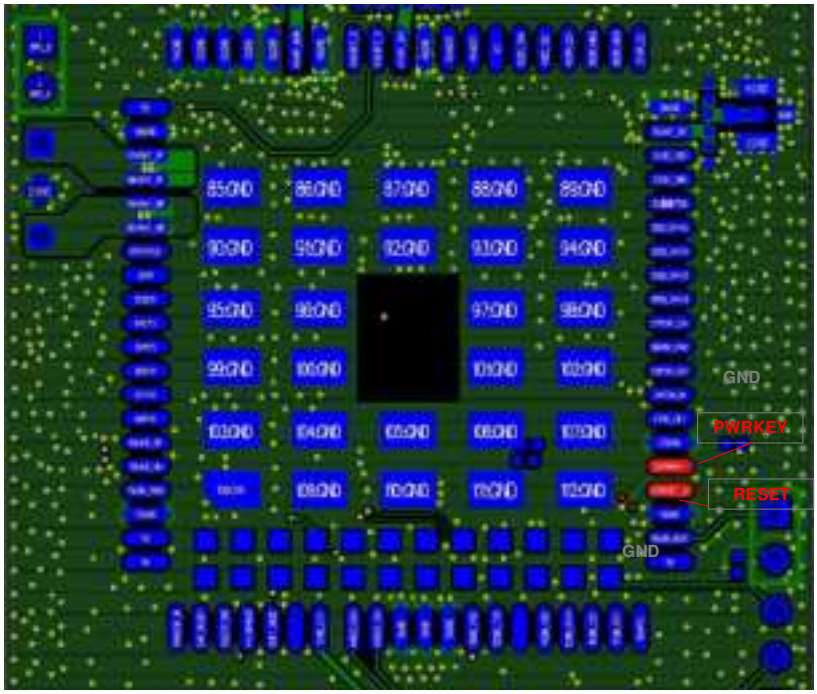

Figure 8: PWRKEY and RESET_N Traces (TE-A 1st Layer)

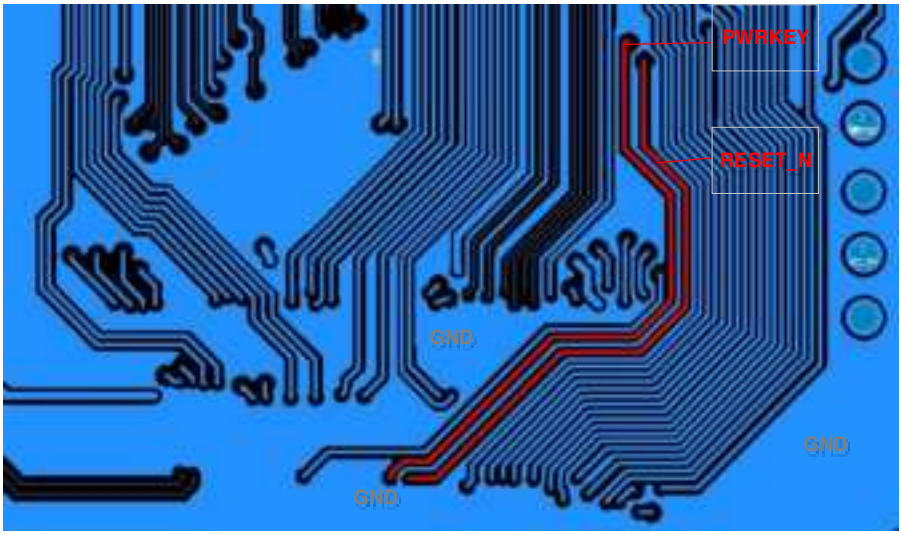

Figure 9: PWRKEY and RESET_N Traces (TE-A 3rd Layer)

3.3. USB Interface

3.3.1. USB_DM & USB_DP Signals

- The spacing between USB_DP/USB_DM and other signal traces should be greater than 0.5 mm
- Maintain the integrity of the reference plane and avoiding crossing with signal traces on adjacent layers.
- USB_DP and USB_DM are recommended to be routed on the inner layer, with the differential impedance controlled to 90 Ω. Keep the spacing and length between traces comparatively equal, with the length tolerance less than 2 mm and the total length less than 120 mm.
- When a TVS needs to be added for USB_DP and USB_DM signal traces, it should be close to USB connector and the junction capacitance of the TVS should be less than 2 pF.

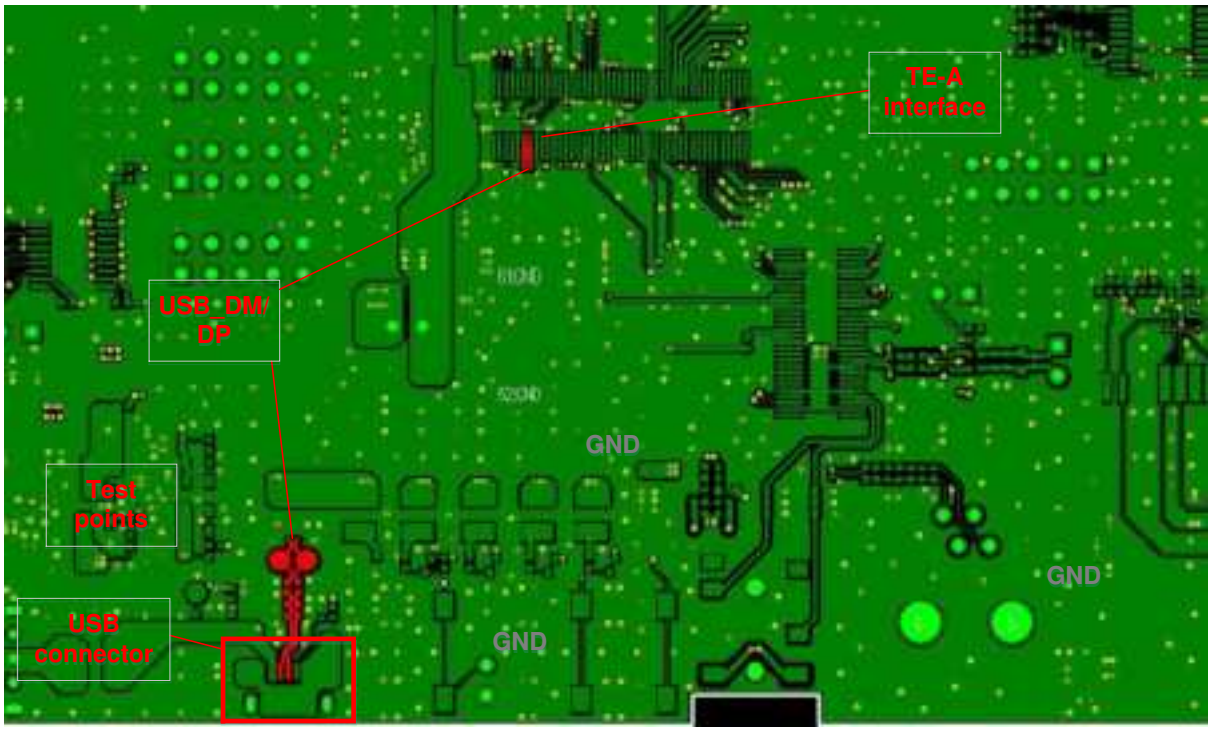

Figure 10: Overview of USB_DM/DP Signal Traces (EVB 1st Layer)

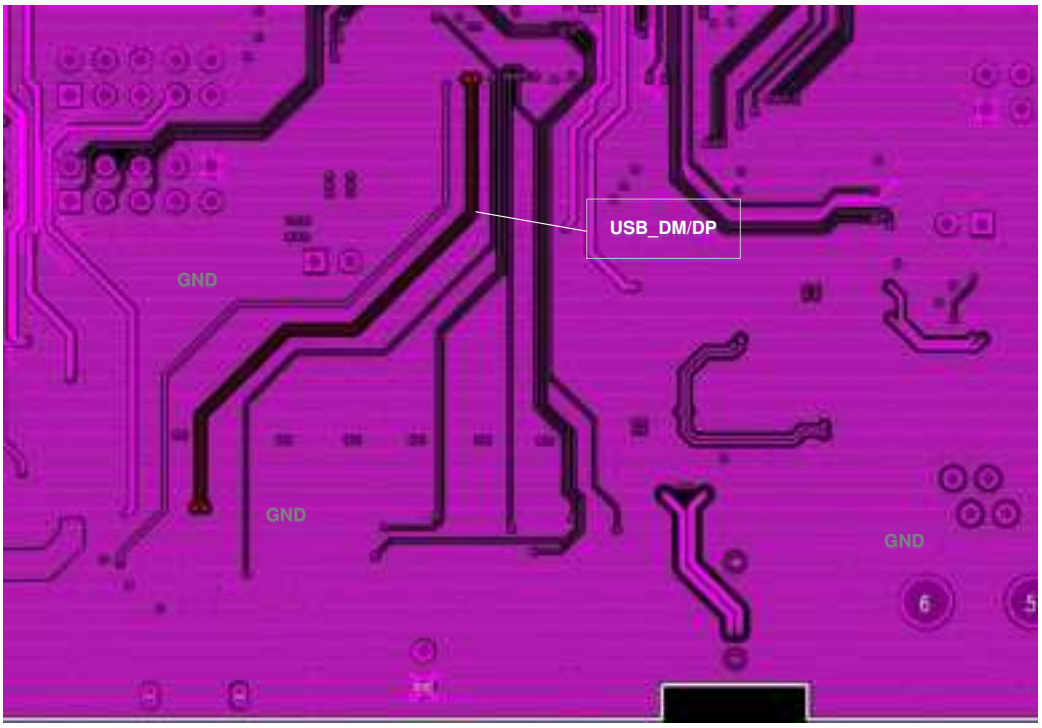

Figure 11: Overview of USB_DM/DP Signal Traces (EVB 3rd Layer)

3.3.2. USB_VBUS Signal

USB_VBUS is a USB detection signal, with maximum current of 1 mA. In general, a trace width of 0.1 mm is sufficient.

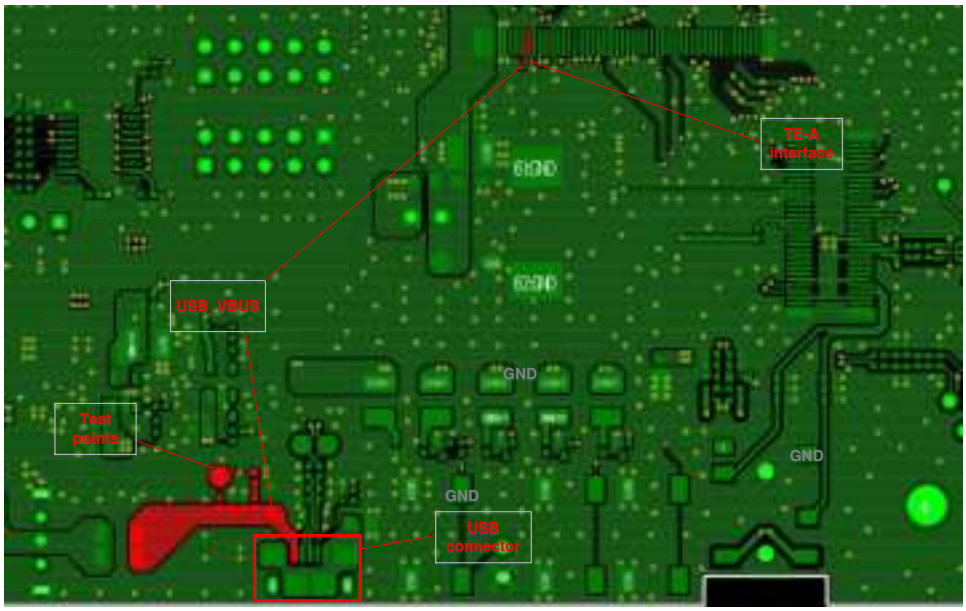

Figure 12: Overview of USB_VBUS Signal Trace (EVB 1st Layer)

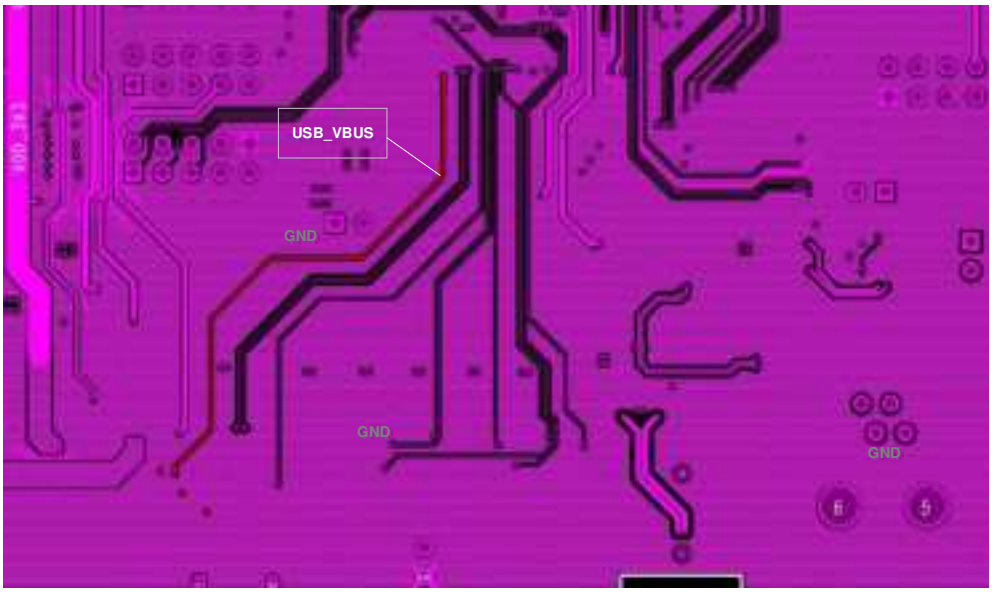

Figure 13: Overview of USB_VBUS Signal Trace (EVB 3rd Layer)

3.4. Ethernet PHY

3.4.1. SGMII Interface

- Signal traces of SGMII_MCLK/SGMII_MDC, SGMII_MDATA/SGMII_MDIO, EPHY_RST_N/ SGMII_RST_N and EPHY_INT_N/SGMII_INT_N should be surrounded with ground.
- The spacing between SGMII_TX_M, SGMII_TX_P, SGMII_RX_M, SGMII_RX_P traces should be at least 3 times wider than the traces, and that between the SGMII signal traces and other signal traces should also be at least 3 times wider than SGMII traces.
- Keep the maximum length of the SGMII signal traces less than 10 inches and the difference between signals of the differential pairs (SGMII_TX_P and SGMII_TX_M, SGMII_RX_P and SGMII_RX_M) less than 20 mil.
- The differential impedance of SGMII signal traces is 100 Ω ±10 %, and the reference ground of the area should be complete.
- The series capacitors for SGMII_TX_M, SGMII_TX_P should be close to PHY component, while the series capacitors for SGMII_RX_M, SGMII_RX_P should be close to the two pins.

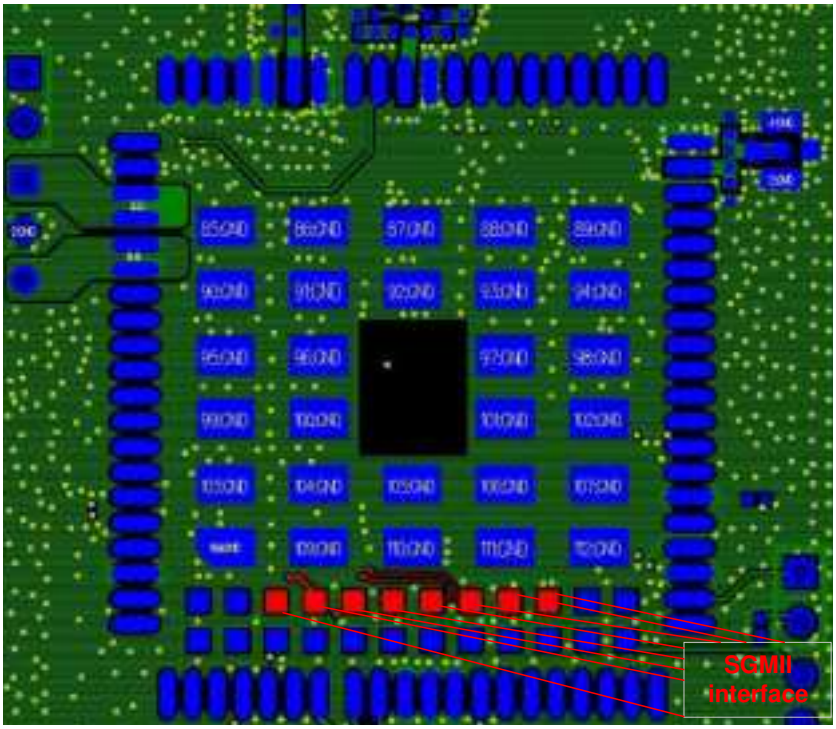

Figure 14: Overview of SGMII Signal Traces (TE-A 1st Layer)

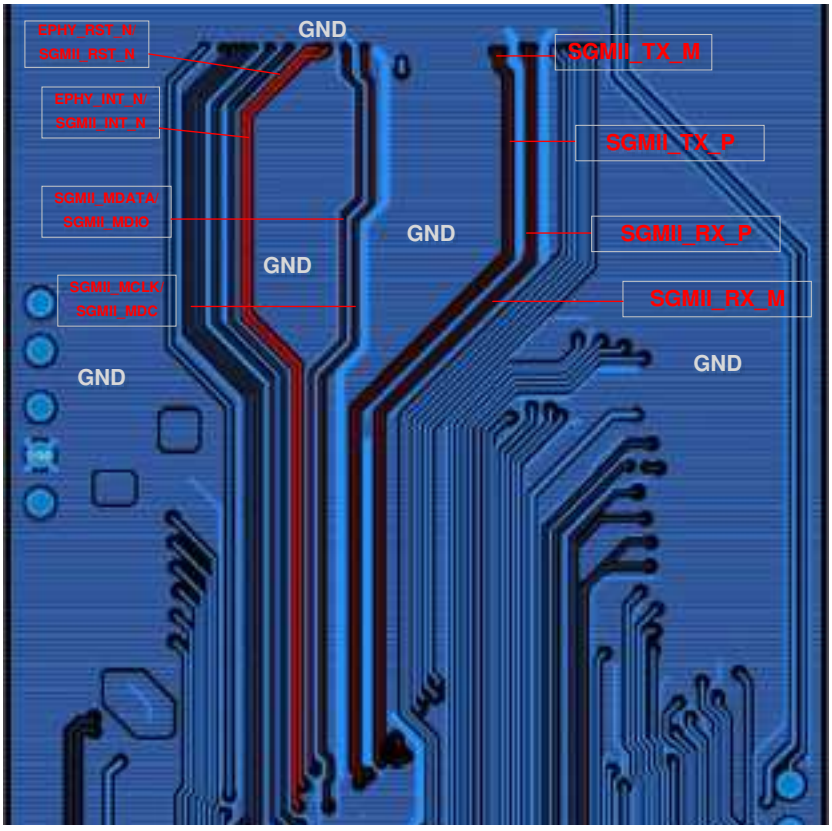

Figure 15: Overview of SGMII Signal Traces (TE-A 3rd Layer)

3.4.2. Ethernet Components

A four-layer PCB should be used when using the SGMII interface to implement the Ethernet function in the application.

- The first layer is for non-sensitive traces and 1.1 V power supply traces.
- The second layer is strongly recommended for 3.3 V and 2.5 V power supply traces and ground plane.
- The third layer should be a reference ground.
- The fourth layer is used for main signal traces.

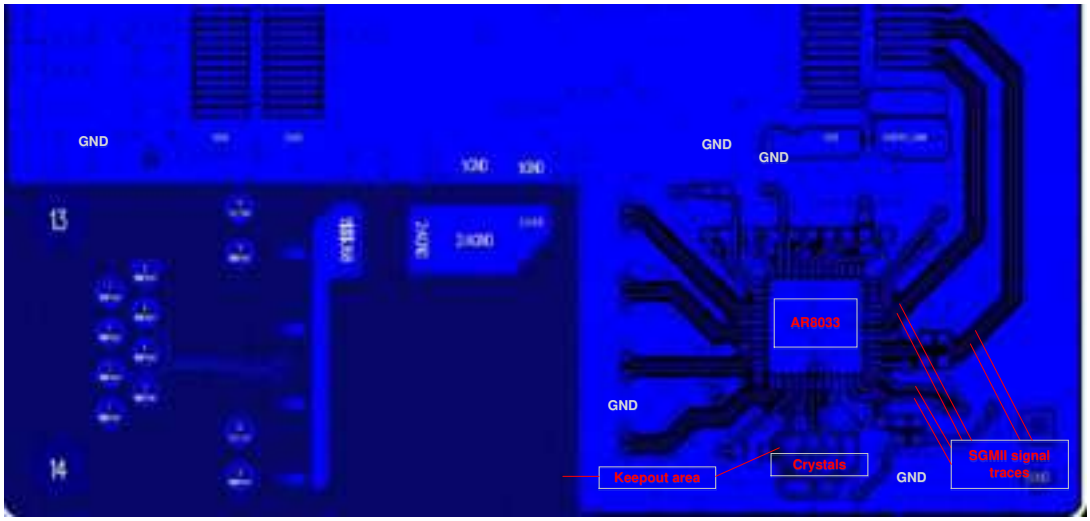

Figure 16: Recommended PCB Layout of SGMII Interface (TE-A 4th Layer)

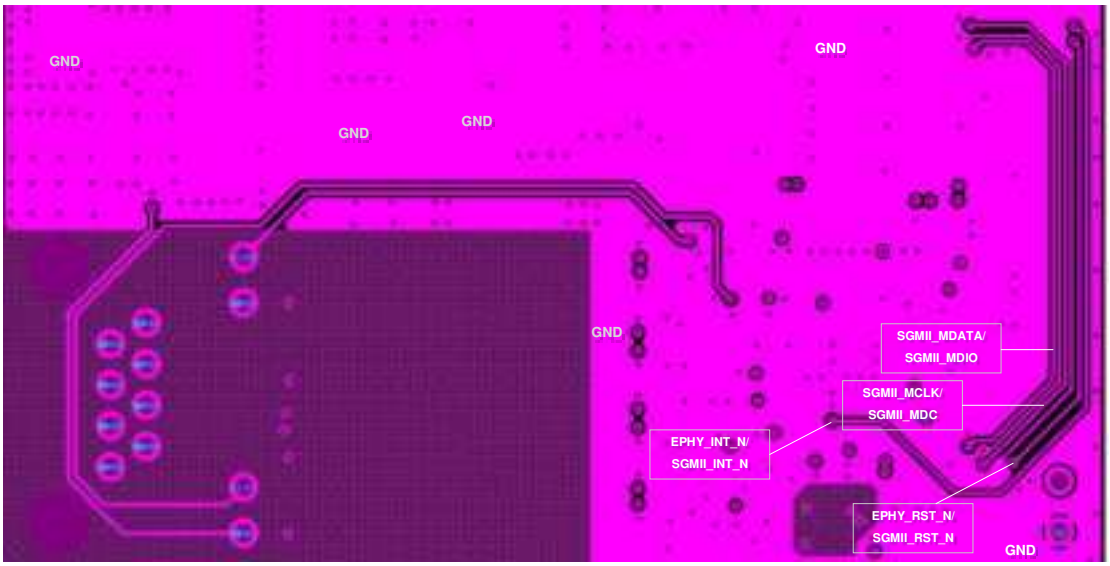

Figure 17: Recommended Reference PCB Layout of SGMII Interface (EVB 3rd Layer)

DVDD_1V1 is output by AR8033's LX pin through an LC circuit. The 4.7 μH inductor in the LC circuit should be able to provide 1 A current with low direct current resistance. The trace width for the inductor is recommended to be at least 1 mm. Besides, there is a reference ground plane needed for inductance isolation near the 4.7 μH inductor The following figure shows the recommended inductor placement as well as trace routing and trace width for AR8033 pins.

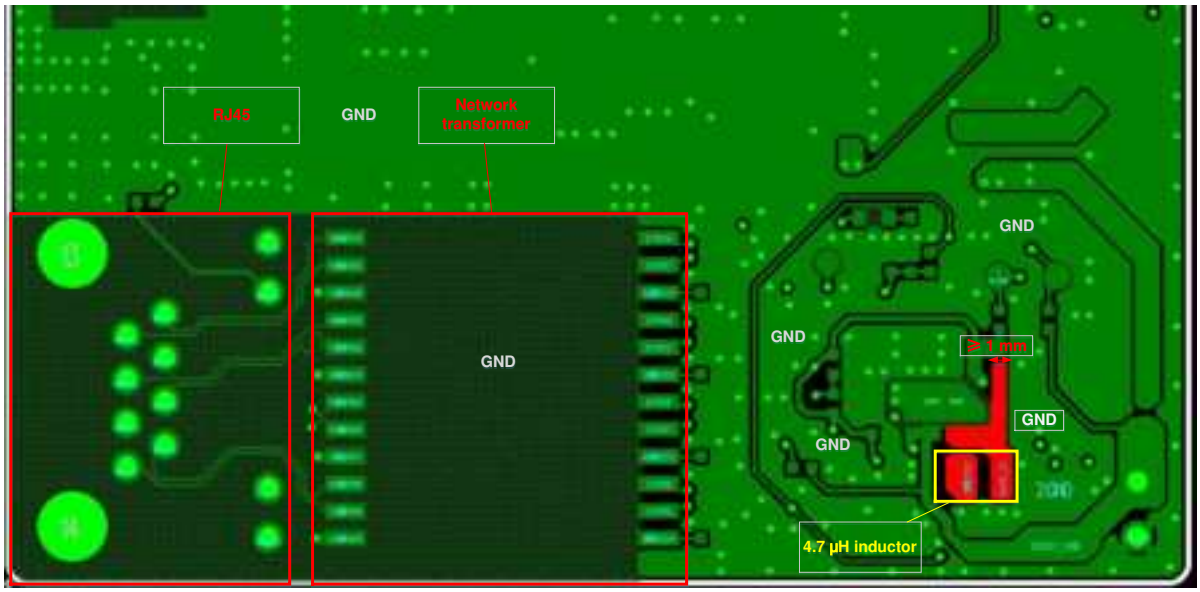

Figure 18: Layout of Recommended 4.7 μH Inductor, GND and Traces of AR8033 (EVB 1st Layer)

3.5. Audio Interfaces

3.5.1. PCM Interface

- The filter capacitors for PCM_CLK/PCM_SYNC should be placed close to the two pins.
- The PCM bus is recommended to be routed on inner layers, and it is recommended that each trace be surrounded by ground traces separately. If there are limits of space, at least ensure PCM_CLK is surrounded by ground traces, and other three signal traces can be surrounded together by ground traces.
- PCM traces should be kept away from interference sources such as clock, RF, crystals and power supplies.

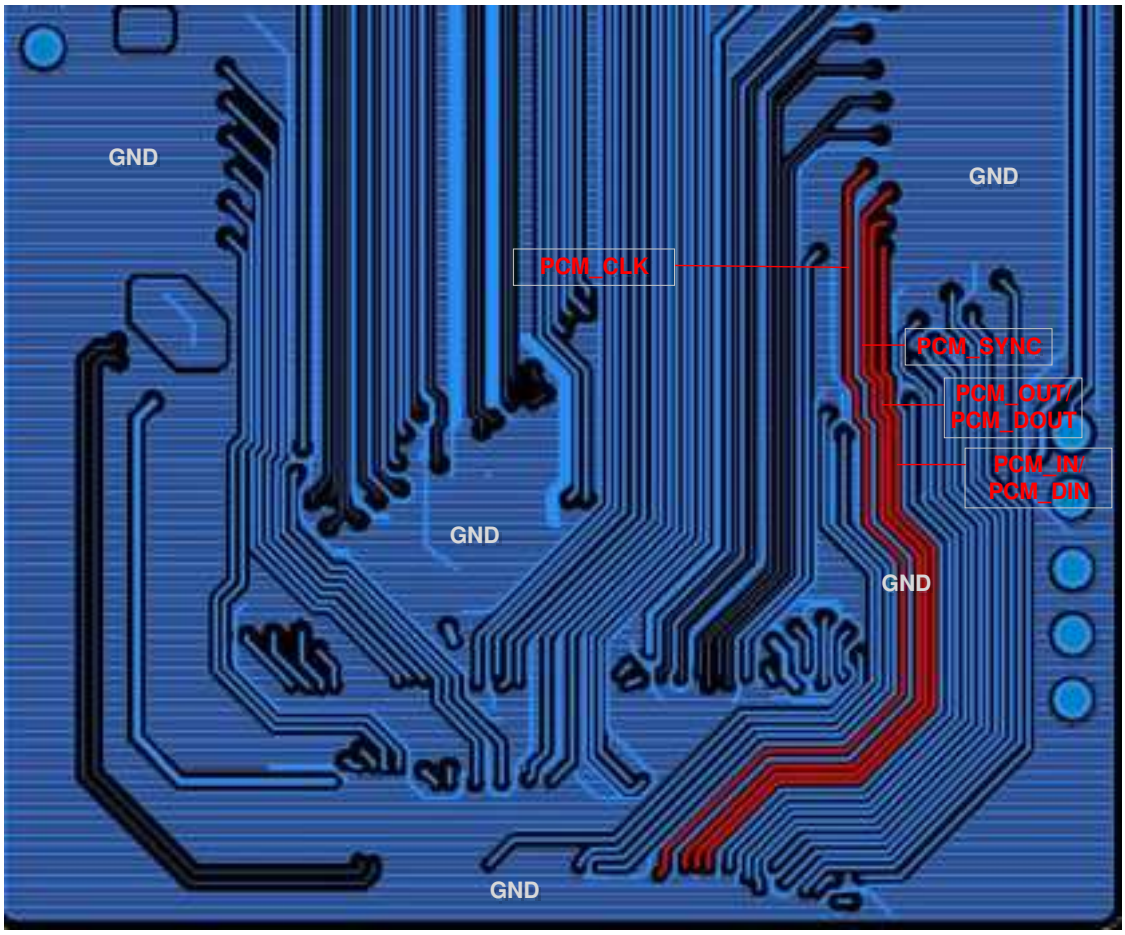

Figure 19: Overview of PCM Signal Traces (TE-A 3rd Layer)

3.5.2. Codec & Microphone & Speaker

The codec should be kept away from interference sources such as high-power components, power sources, CPU, DRAM, Flash, PMU, LCD, RF antennas and other high-frequency components, and should be isolated and close to one of the edges or corners of the board, and could be shielded if there is sufficient space.

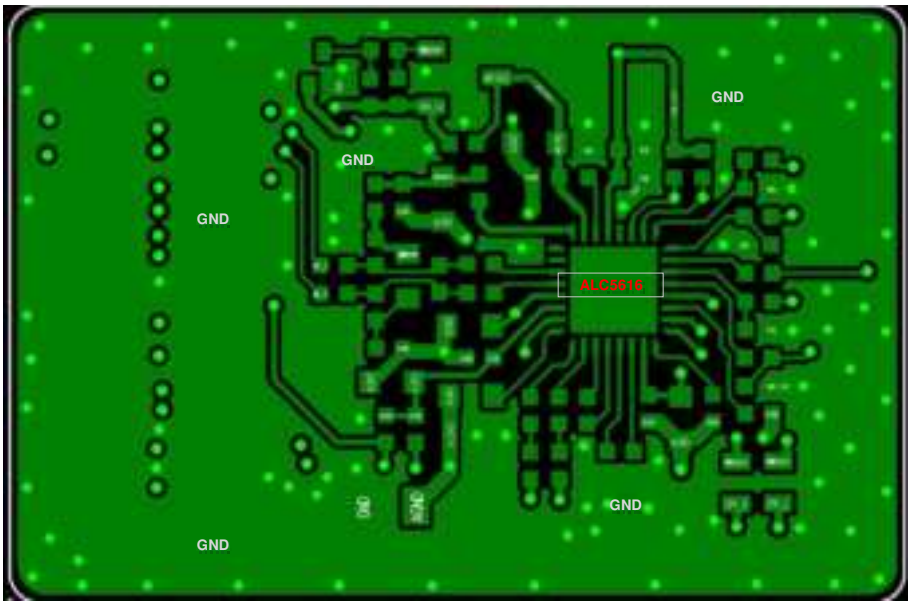

Figure 20: Overview of Codec ALC5616 (EVB 1st Layer)

- Keep the traces for microphone and speaker as short as possible. For MIC signals, it is recommended to design differential pairs.
- The analog output signals only drives handset and headset. For larger power loads such as loudspeakers, an audio power amplifier should be added in the design.
- All MIC and SPK signal traces should be surrounded with ground on that layer and with ground planes above and below, and it should be far away from interference sources.
- The spacing between MIC_P and MIC_N should be more than 0.25 mm. To avoid cross-talk, the spacing between the differential pair traces should exceed 1.5 mm. To avoid interference between different MIC traces, MIC1 and MIC2 traces should be routed on different layers as much as possible.
- For signal traces of speaker, the length should be more than 0.5 mm and requires low impedance.
- The reference ground for microphone, speaker and MICBIAS should be analog ground while for PCM interface should be digital ground. Besides, pay attention to the integrity of the analog signal reference plane.

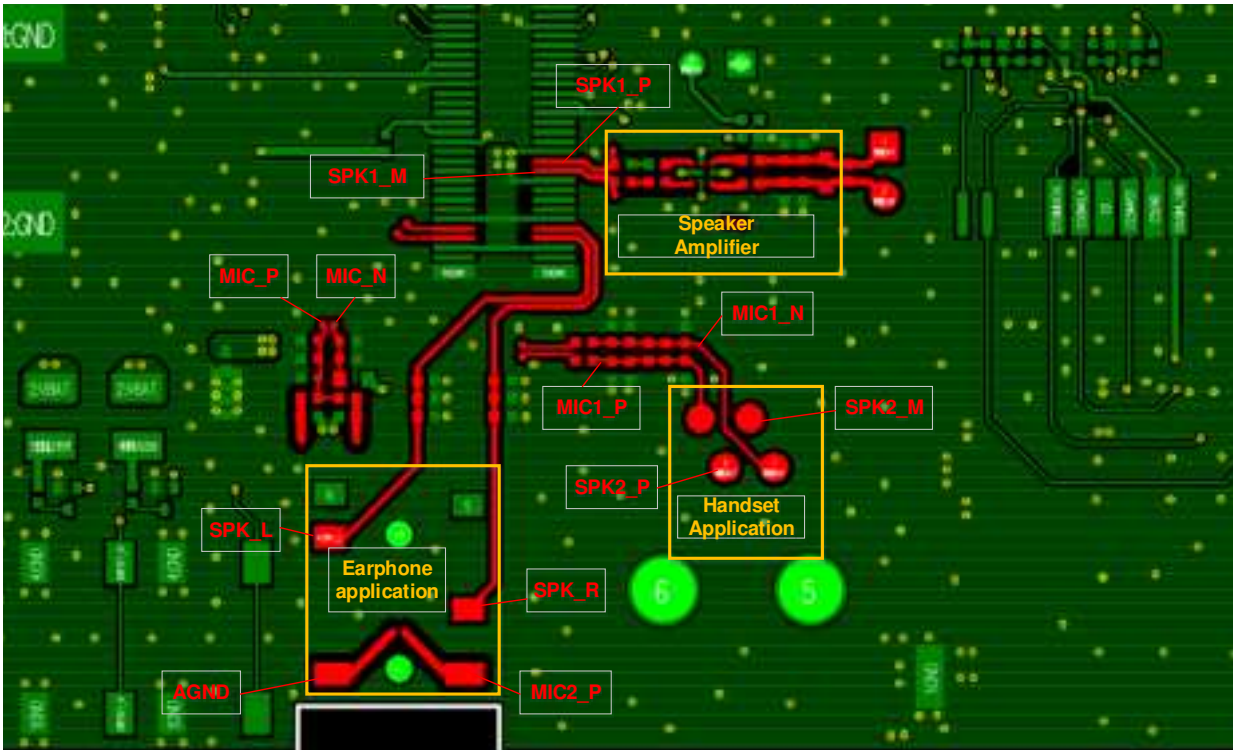

Figure 21: Overview of Analog Audio Signal Traces (EVB 1st Layer)

3.6. SD Card Interface

- Keep SDIO signals far away from other sensitive circuits or signals such as RF circuits and analog signals, as well as noisy signals such as clock and DC-DC signals.
- Keep the impedance of SDIO signal traces at 50 Ω ±10 %.
- Maintain the integrity of the reference plane. SDC2_CLK/SD_CLK and SDC2_CMD/SD_CMD should be surrounded with ground on the layer and ground planes above and below. If the space is limited, SDC2_DATA[0:3]/SD_DATA[0:3] could be surrounded with ground together.
- The total length of each SDIO signal trace should be less than 50 mm, and the difference between them should be less than 1 mm.
- The load capacitance for SD card signals should be less than 15 pF.
- If a SD card is applied, a TVS should be placed close to the SD card connector.

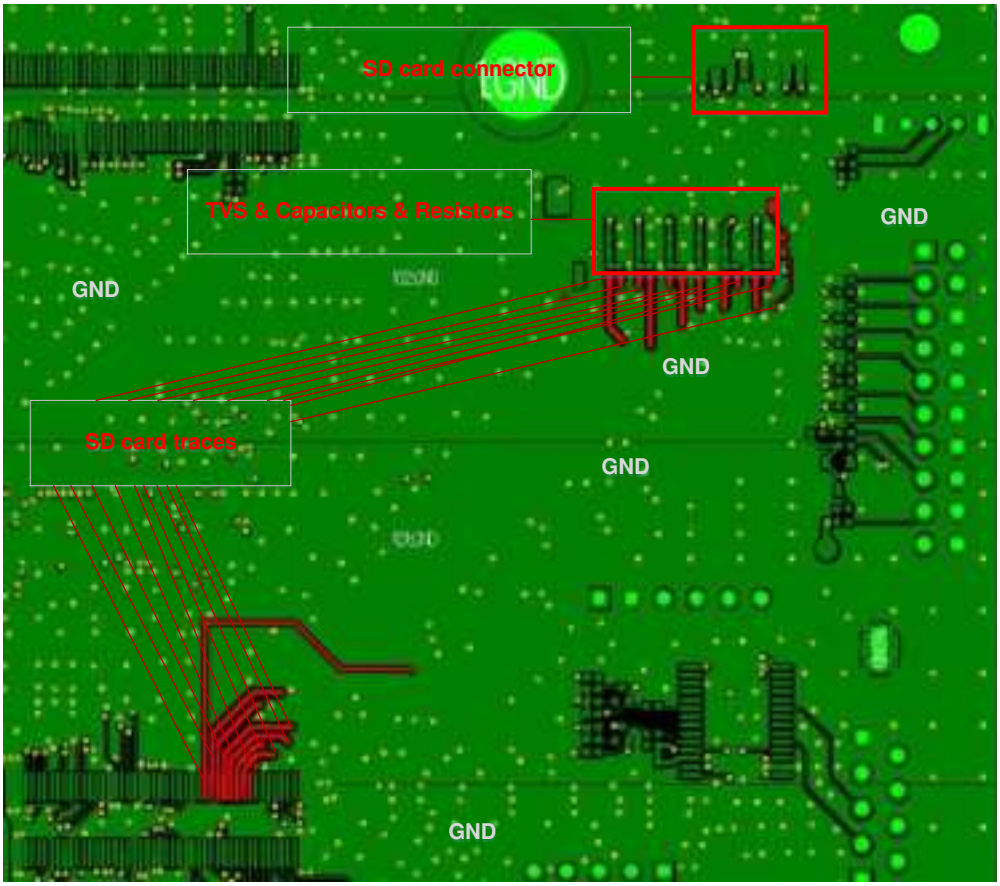

Figure 22: Overview of SD Card Signal Traces (EVB 1st Layer)

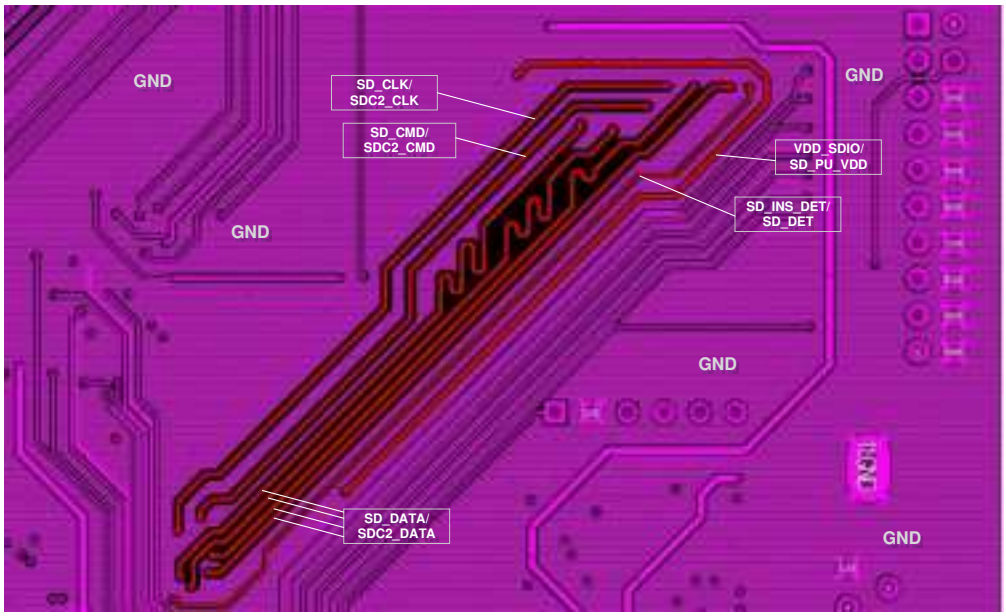

Figure 23: Overview of SD Card Signal Traces (EVB 3rd Layer)

3.7. WLAN Application Interface

- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noisy signals such as clock and DC-DC signals.
- The total length of each SDIO signal trace should be less than 23 mm, and the difference between them should be less than 1 mm.
- The load capacitance for SDIO signal traces should be less than 15 pF.
- Keep the impedance of SDIO signal traces at 50 Ω ±10 %, maintaining the integrity of the reference plane. SDC1_CLK/SDC_CLK and SDC1_CMD/SDC_CMD should be surrounded with ground on the layer and adjacent ground planes If limited by space, SDC1_DATA[0:3]/SDC_DATA[0:3] should be surrounded with ground together.

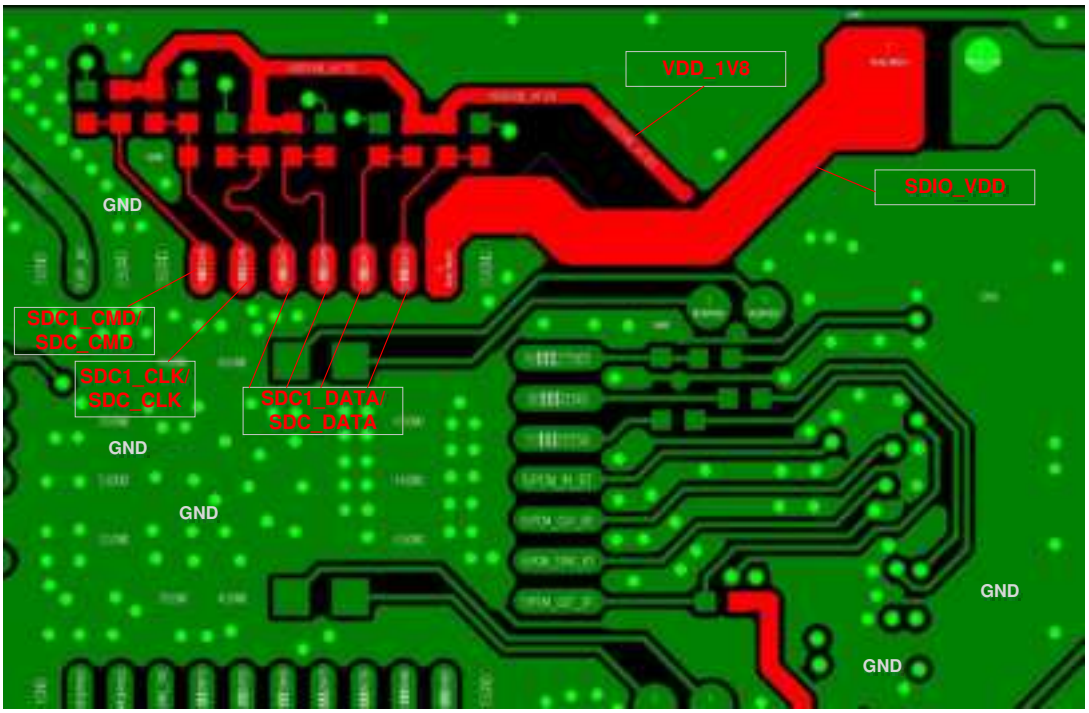

Figure 24: Overview of SDIO Signal Traces (FC20 TE-A 1st Layer)

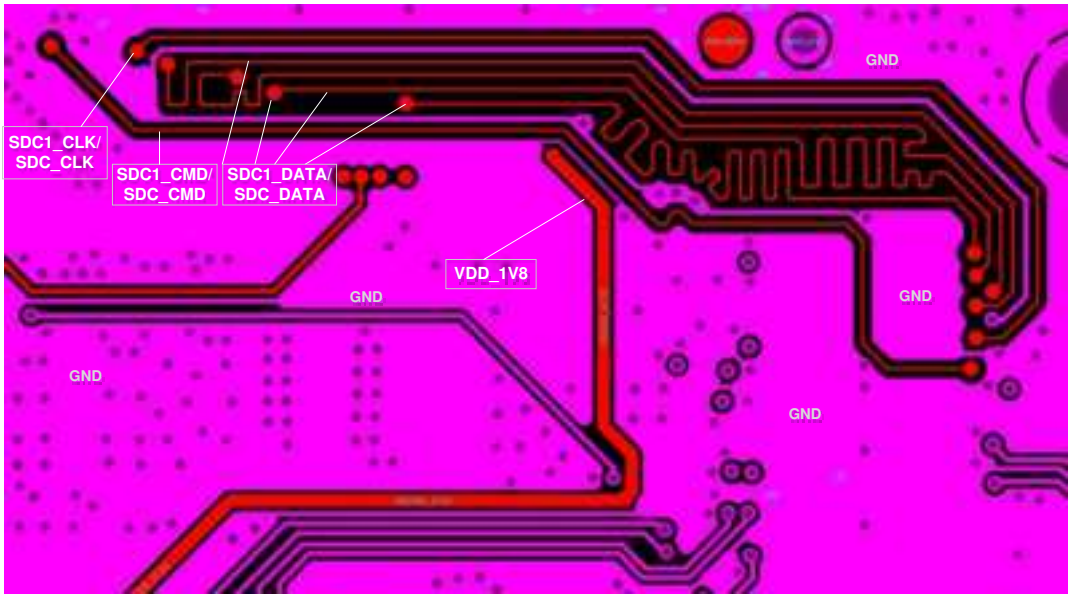

Figure 25: Overview of SDIO Signal Traces (FC20 TE-A 3rd Layer)

3.8. (U)SIM Interface

- The total length of each (U)SIM signal trace should be less than 200 mm.
- Isolate USIM_CLK and USIM_DATA with ground plane to avoid the interference between each other.
- The peripheral components such as TVS, capacitors and resistors should be put near the (U)SIM card connector.

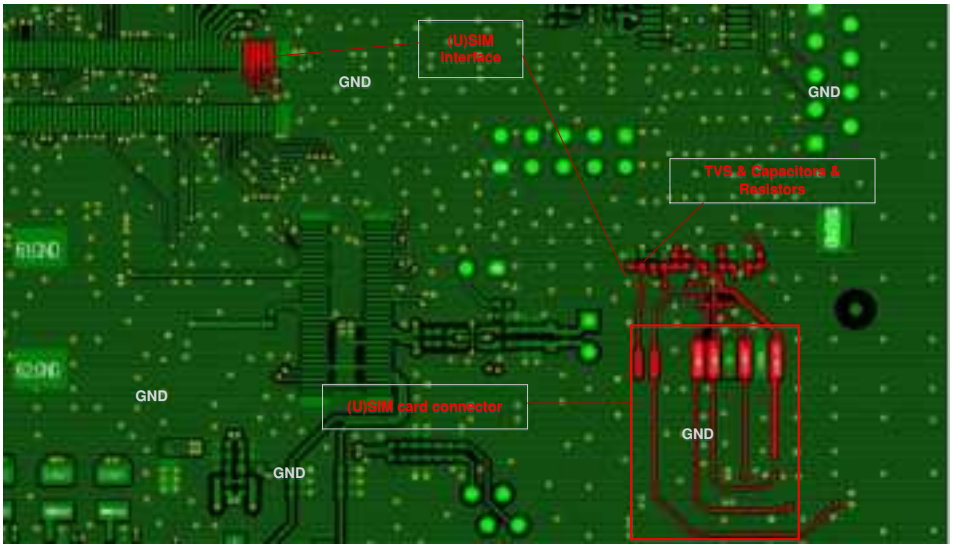

Figure 26: Overview of (U)SIM Signal Traces (EVB 1st Layer)

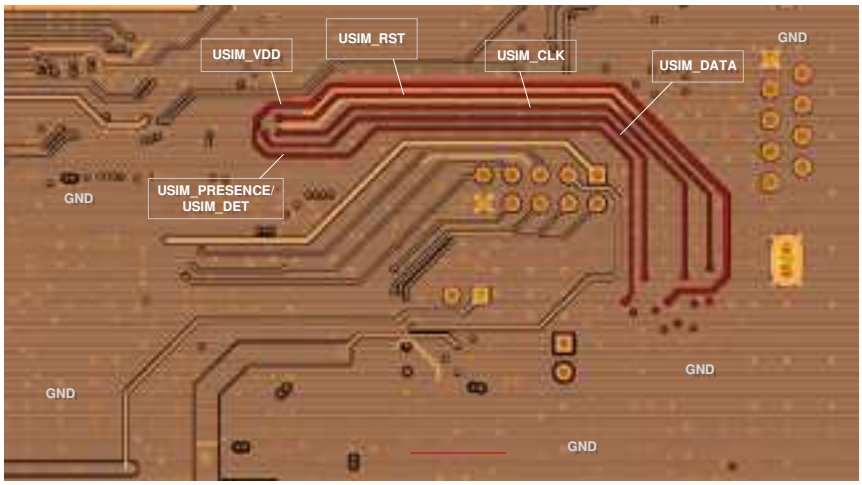

Figure 27: Overview of (U)SIM Signal Traces (EVB 2nd Layer)

3.9. ADC Interface

All ADC signal traces should be surrounded with ground.

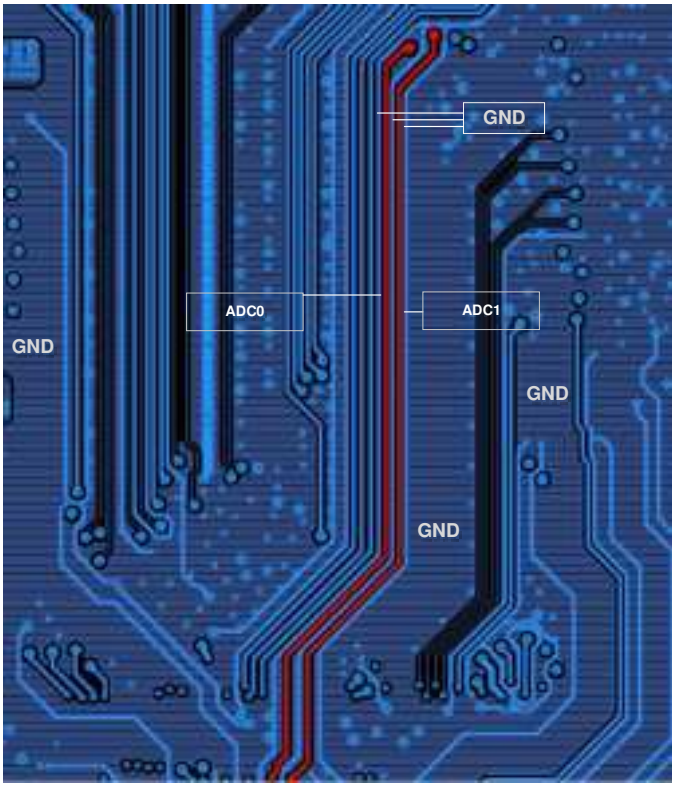

Figure 28: Overview of ADC Signal Traces (EVB 3rd Layer)

3.10. Antenna Interfaces

3.10.1. PCB Structures of Microstrip And Coplanar Waveguide

3.10.1.1. PCB Structure of Microstrip Waveguide

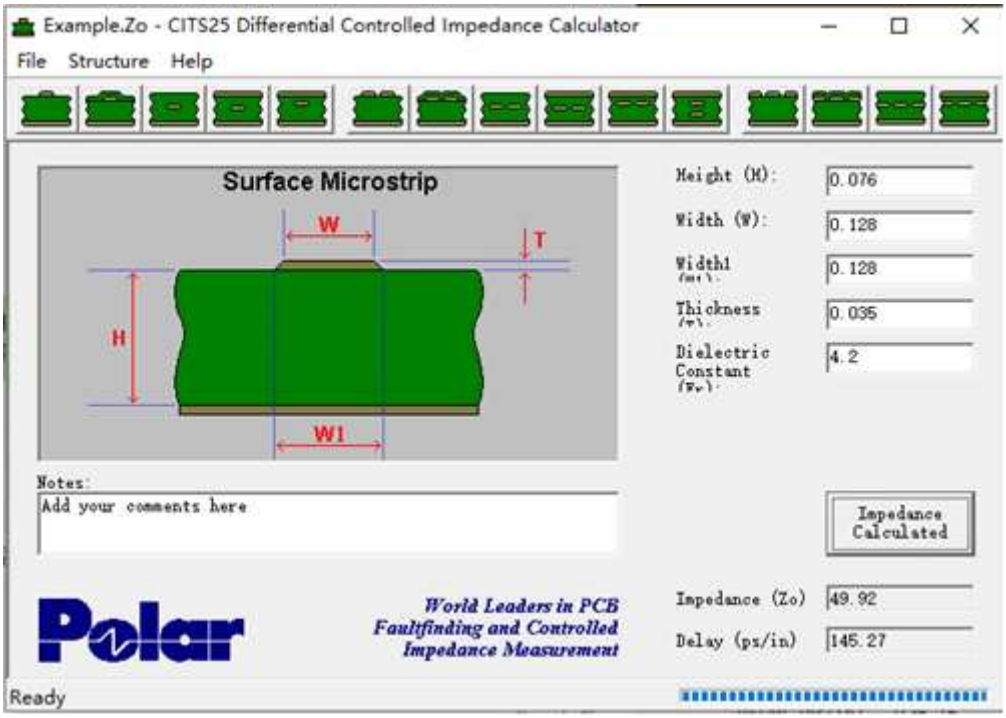

Figure 29: PCB Structure of Microstrip Waveguide

3.10.1.2. PCB Structure of Coplanar Waveguide

Factors affecting impedance include dielectric constant (usually 4.2–4.6, here 4.4), dielectric layer height (H), RF trace width (W), the spacing between RF traces and the ground (S) and copper thickness (T). When T = 0.035 mm, the following table lists the recommended values of W and S for 50 Ω coplanar waveguide under different PCB structures.

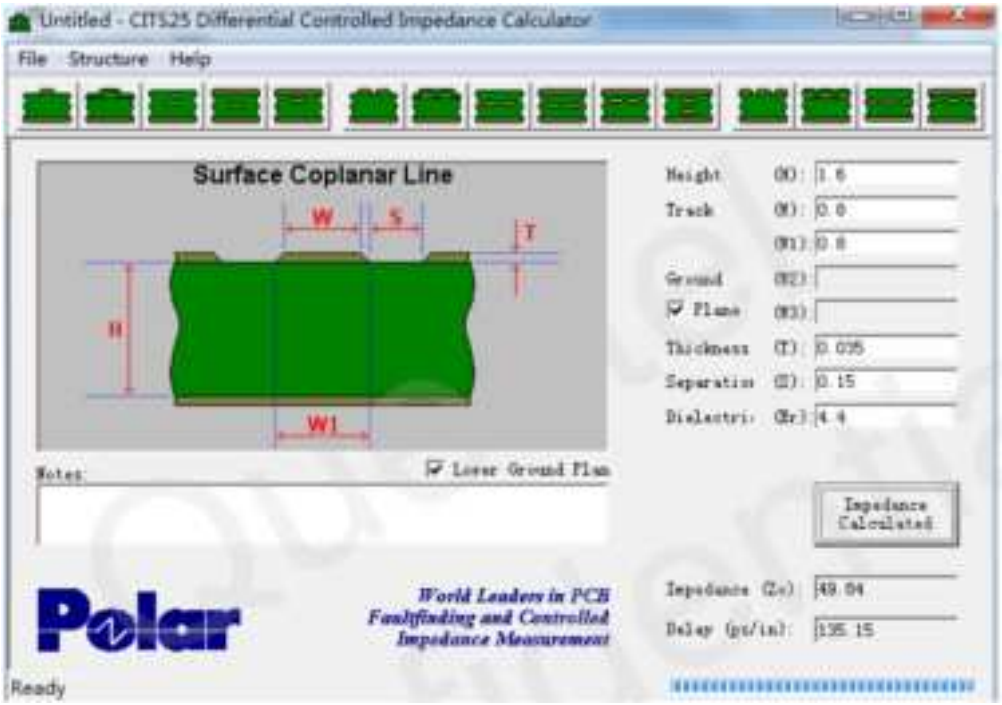

Figure 30: PCB Structure of Coplanar Waveguide

Table 3: W and S Recommendations for 50 Ω Coplanar Waveguide Under Different PCB Structures

Dielectric Height (H)	RF Trace Width (W)	Spacing Between RF Trace and The Ground (S)
0.076 mm	0.1188 mm	0.15 mm
0.1 mm	0.1623 mm	0.2 mm
0.15 mm	0.24 mm	0.2 mm
0.8 mm	0.8 mm	0.18 mm
1.0 mm	0.8 mm	0.17 mm
1.2 mm	0.8 mm	0.16 mm
1.6 mm	0.8 mm	0.15 mm
2 mm	0.8 mm	0.14 mm

3.10.2. Reference Design of RF Layout

For the reference design of RF layout, please refer to the RF routing guidelines introduced in the hardware design of each module.

3.10.3. PCB Layout Considerations of Coplanar Waveguide

There are 6 guidelines of the PCB layout should be taken into consideration. Each guideline is corresponding to the marks in the following two figures respectively.

1. Control the trace width (W) and the spacing between RF traces and grounds (S) corresponding to the 50 Ω coplanar waveguide. Taking common PCB board with FR4 medium (dielectric constant 4.2) and copper thickness of 35 μm as an example, the W and S corresponding to the thickness between different signal layers and reference grounds are shown in ***Table 3.*** It is particularly reminded that PCB manufacturers need to control the accuracy of the W and S.
2. Fully contact the GND pin pad next to the RF trace with ground plane and not design it as design thermal relief pad.
3. Leave a small keepout area for the RF traces on the top layer to reduce parasitic effects. Keep the traces as short as possible. Avoid right-angle routing for RF traces and 135 degrees is recommended when traces turn corner.
4. Keep a certain distance between signal pad and ground when packaging the component. If the signal pad is SMD type, pour the copper on the corresponding signal pad.
5. Make sure that reference ground planes corresponding to RF traces are complete. Increase the number of GND vias for current reflow of RF signal, and the spacing between GND vias and RF traces should be more than twice of trace width. Keep the ground plane area for RF traces within the same layer be as large as possible and the reference ground plane in the other layer complete as well. Besides, the number of through vias for those two ground planes should be sufficient.
6. The pads for PI type matching circuit consisting of a resistor and two capacitors should be near the module's antenna pins.

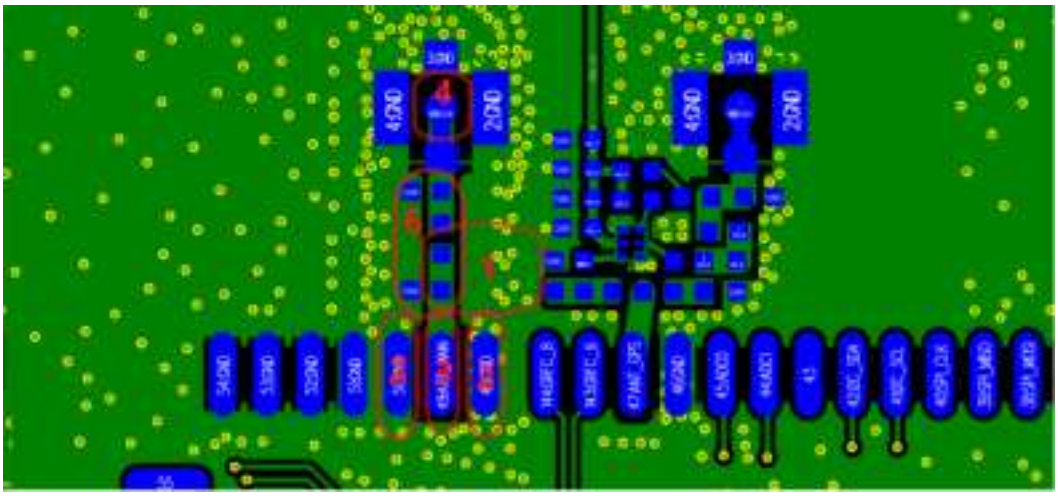

Figure 31: Overview of RF Traces (EVB 1st Layer)

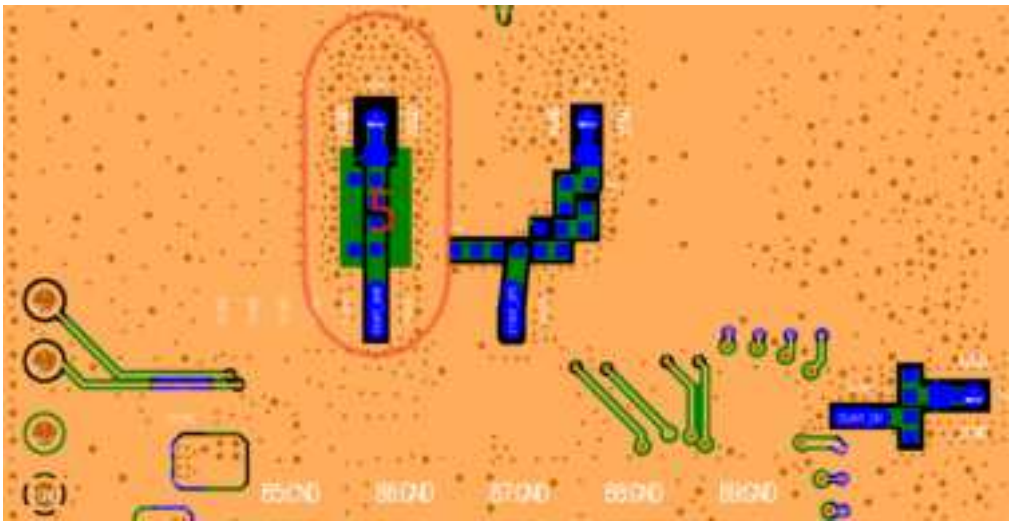

Figure 32: Overview of RF Traces (EVB 1st and 2nd Layers)

4 Thermal Design

For more details of the thermal design of the PCB, please refer to the thermal dissipation outlined in the hardware design of each module.

5 Appendix References

Table 4: Related Documents

Document Name
[1] Quectel_EC21_Footprint&Part
[2] Quectel_EC25_Footprint&Part
[3] Quectel_EC20_R2.1_Footprint&Part
[4] Quectel_EG25-G&EG21-G_Footprint&Part
[5] Quectel_EG2x-GL_Footprint&Part_V1.0

Table 5: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
LTE	Long Term Evolution
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PHY	Physical Layer
RF	Radio Frequency
SD	Secure Digital
SGMII	Serial Gigabit Media Independent Interface
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
VBAT	Voltage at Battery
WLAN	Wireless Local Area Network