Data sheet for the LTD-VL3020

Product: LTE Wireless Modem

Model name: LTD-VL3020

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LG Innotek

1. Overview

The LTD-VL3020 is a personal mobile communication device that incorporates the latest compact radio technology, including smaller and lighter components and support LTE Band 2,4,5,13. This device acts as the vehicle's telematics system and connects to LTE wireless networks and wireless modules to allow voice and data communication. Furthermore, this device can operate on land and water as well as other similar areas.

In LTE mode (CAT4), the device provides uplink speeds of up to 50 Mbps and downlink speeds of up to 150 Mbps for seamless transfer of data such as movies and video calls. The device also supports the transfer of large amounts of data.

The device communicates with the host system via a standard RS-232 or USB port, and AT commands and control commands can be used to send data. Voice calls are also possible.

2. Major features

Mechanical	Dimensions	34.0 x 40.0 x 3.5 mm (L x W x T) (Tolerance – width, length: ±0.15 / height: ±0.2)
	Weight	Max. 10.6 grams
	Interface	USB, general purpose I/O pins
	Temperature*	Operation: -20 ℃ - +70 ℃ Storage: -40 ℃ - +85 ℃
Technology	Main chipset	MDM9628
	Memory	4Gb(NAND) / 2Gb(SDRAM)
	Standard	LTE - DL Speed : 150 Mbps - UL Speed : 50 Mbps
	Band	LTE B2, B4, B5, B13
	Power	LTE : Typ. 23dBm (Power Class 3)
ETC	DC power	4 V
	Functions	Voice, data, SMS

3. Interface

3.1 LGA Pad Layout (Top View)

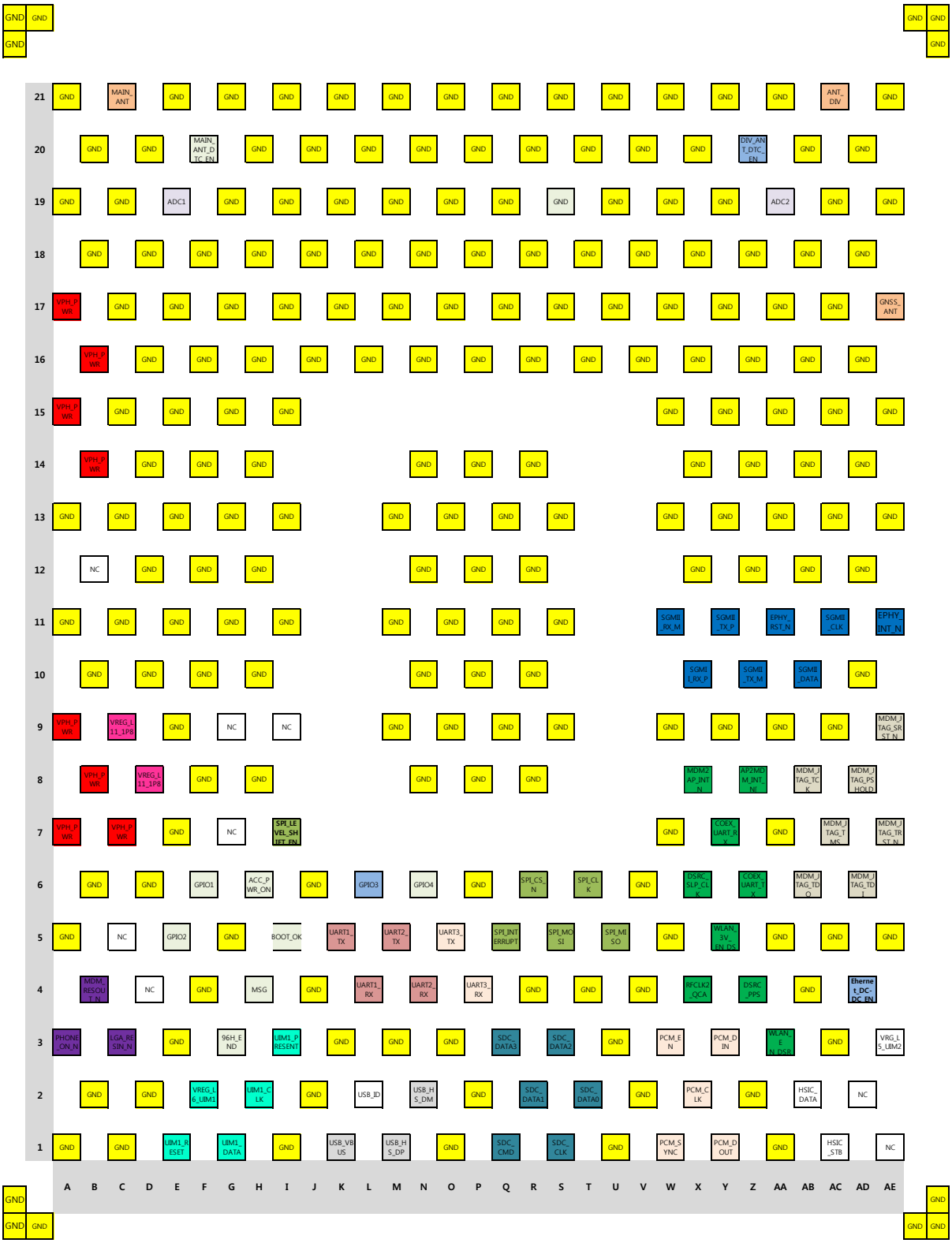

Figure 1. LGA Pin map

3.2 Pin description

PAD.	NAME	DIRECTION	DESCRIPTION
Antenna Interface Pads			
C21	MAIN_ANT	Input/Output	RF Main Antenna
AC21	DIV_ANT	Input	RF Diversity Antenna
AE17	GNSS_ANT	Input	GNSS Antenna
User Interface Pads			
H6	ACC_PWR_ON	Input	ACC_PWR_ON
I5	BOOT_OK	Output	BOOT_OK
H4	MSG	Output	MSG
G3	168H_END	Output	Remote standby mode end
F20	MAIN_ANT_DTC_EN	Output	Main ANT Detect Enable
Z20	DIV_ANT_DTC_EN	Output	Diversity ANT Detect Enable
I7	SPI_LEVEL_SHIFT_EN	Output	SPI LEVEL SHIFT Enable
AD4	ETHERNET_DCDC_ENABLE	Output	Ethernet power enable
F6	GPIO1	Input/Output (Do not use with External PU)	General purpose I/O
E5	GPIO2		General purpose I/O
L6	GPIO3	Input/Output (Not support INTERRUPT)	General purpose I/O
N6	GPIO4		General purpose I/O
ADC Interface Pads			
E19	ADC1	Input	ADC Convertor input for main antenna detect
AA19	ADC2	Input	ADC Convertor input for diversity antenna detect
PCM Interface Pads			
W3	PCM_EN	Output	PCM 3.3 Level Shifter Enable
X2	PCM_CLK	Input	PCM Clock
W1	PCM_SYNC	Input	PCM Frame Sync
Y3	PCM_DIN	Input	PCM Data In
Y1	PCM_DOUT	Output	PCM Data Out
JTAG Pin Description			
AC7	MDM_JTAG_TMS	Input/Output	JTAG mode select input
AD8	MDM_JTAG_PS_HOLD	input	JTAG PS HOLD detect
AD6	MDM_JTAG_TDI	Input	JTAG data input
AE7	MDM_JTAG_TRST_N	Input	JTAG reset for debug
AB6	MDM_JTAG_TDO	Output	JTAG debugging
AB8	MDM_JTAG_TCK	Input	JTAG clock input
AE9	MDM_JTAG_SRST_N	Input	JTAG reset
USB Interface Pads			
N2	USB_HS_DM	Input/Output	USB high speed data (minus)
M1	USB_HS_DP	Input/Output	USB high speed data (plus)
K1	USB_VBUS	Input	USB power
L2	USB_ID	Input	USB ID
SDIO Interface Pads			
S1	SDC_CLK	Output	Secure digital controller clock
Q1	SDC_CMD	Output	Secure digital controller command
T2	SDC_DATA0	Input/Output	Secure digital controller data bit 0
R2	SDC_DATA1	Input/Output	Secure digital controller data bit 1
S3	SDC_DATA2	Input/Output	Secure digital controller data bit 2

Table 1. Pin descriptions

Q3	SDC_DATA3	Input/Output	Secure digital controller data bit 3
SGMMI Interface Pads			
AA11	EPHY_RST_N or UIM2_RESET	Output	Ethernet PHY reset
AE11	EPHY_INT_N or UIM2_DETECT	Input	Ethernet PHY interrupt
AB10	SGMII_DATA or UIM2_CLK	Input/Output	SGMII input Output data
AD10	GND		Ground
X10	SGMII_RX_P	Input	SGMII receive - plus
W11	SGMII_RX_M	Input	SGMII receive -minus
Z10	SGMII_TX_M	Output	SGMII transmit - plus
Y11	SGMII_TX_P	Output	SGMII transmit -minus
AC11	SGMII_CLK or UIM2_DATA	Output	SGMII clock
SPI Interface Pads			
S5	SPI_MOSI	Output	SPI Serial Output
T6	SPI_CLK	Output	SPI Serial Clock
R6	SPI_CS_N	Output	SPI Chip Select
U5	SPI_MISO	Input	SPI Serial input
Q5	SPI_INTERRUPT	Input	MICOM → LGA SPI interrupt
UART Interface Pads			
M5	UART2_TX	Output	UART2 Transmit data
N4	UART2_RX	Input	UART2 Receive data
K5	UART1_TX	Output	Debug UART5 Transmit Data
L4	UART1_RX	Input	Debug UART5 Receive Data
O5	UART3_TX	Output	UART6 Transmit data
P4	UART3_RX	Input	UART6 Receive data
USIM Interface Pads			
I3	UIM1_PRESENT	Input	Detection of an external UIM card
H2	UIM1_CLK	Output	Clock Output to an external UIM card
E1	UIM1_RESET	Output	Reset Output to an external UIM card
G1	UIM1_DATA	Input/Output	Data connection with an external UIM card
F2	VREG_L6_UIM1	Output	Supply Output for an external UIM card
E3	GND		Ground
D2	GND		Ground
A1	GND		Ground
C1	GND		Ground
B2	GND		Ground
HSIC Pin Description			
AB2	HSIC_DATA	Input/Output	HSIC data
AC1	HSIC_STB	Input/Output	HSIC Strobe signal
AD2	NC		No Connect
AE1	NC		No Connect
DSRC Pin Description			
Y7	COEX_UART_RX	Input	LTE receiver sync for coexistence with UART
Z6	COEX_UART_TX	Output	LTE transmitter sync for coexistence with UART
X4	RFCLK2_QCA	Output	Low noise RF clock Output
AA3	NC	Output	No Connect

Table 1. Pin descriptions

X6	DSRC_SLP_CLK	Output	DSRC sleep clock
Y5	WLAN_3V_EN_DSRC	Output	Used for WLAN enable
Z4	DSRC_PPS	Input/Output	Pulse Per Second
X8	MDM2AP_INT_N	Output	MDM to AP interrupt, PCM_LDO_EN
Z8	AP2MDM_INT_N	Input	AP to MDM interrupt
Control Pads			
A3	LGA_PHONE_ON	Input	ON/OFF Control
B4	MDM_RESOUT_N	Output	Reset Output
C3	LGA_RESIN_N	Input	External Reset Input
Power Supply Pads			
A17	VPH_PWR for PAM	Input	power supply (4.0V)
B16	VPH_PWR for PAM	Input	power supply (4.0V)
A15	VPH_PWR for PAM	Input	power supply (4.0V)
B14	VPH_PWR for PAM	Input	power supply (4.0V)
A9	VPH_PWR for PMIC	Input	power supply (4.0V)
B8	VPH_PWR for PMIC	Input	power supply (4.0V)
A7	VPH_PWR for PMIC	Input	power supply (4.0V)
C7	VPH_PWR for PMIC	Input	power supply (4.0V)
Voltage Reference Pad			
C9	VREG_L11_1P8	Output	LDO out for 1.8V pull up
D8	VREG_L11_1P8	Output	LDO out for 1.8V pull up
AE3	Voltage Reference for SGMII (VREG_L5_UIM2) – Ethernet IO전압 level	Output	Ethernet I/O voltage
NC Pads			
G9	NC		No Connect
B12	NC		No Connect
I9	NC		No Connect
G7	NC		No Connect
C5	NC		No Connect
D4	NC		No Connect
A21	GND		Ground
E21	GND		Ground
G21	GND		Ground
I21	GND		Ground
K21	GND		Ground
M21	GND		Ground
O21	GND		Ground
Q21	GND		Ground
S21	GND		Ground
U21	GND		Ground
W21	GND		Ground
Y21	GND		Ground
AA21	GND		Ground
AE21	GND		Ground
B20	GND		Ground
D20	GND		Ground
H20	GND		Ground
J20	GND		Ground

Table 1. Pin descriptions

L20	GND		Ground
N20	GND		Ground
P20	GND		Ground
R20	GND		Ground
T20	GND		Ground
V20	GND		Ground
X20	GND		Ground
AB20	GND		Ground
AD20	GND		Ground
A19	GND		Ground
C19	GND		Ground
G19	GND		Ground
I19	GND		Ground
K19	GND		Ground
M19	GND		Ground
O19	GND		Ground
Q19	GND		Ground
S19	GND		Ground
U19	GND		Ground
W19	GND		Ground
Y19	GND		Ground
AC19	GND		Ground
AE19	GND		Ground
B18	GND		Ground
D18	GND		Ground
F18	GND		Ground
H18	GND		Ground
J18	GND		Ground
L18	GND		Ground
N18	GND		Ground
P18	GND		Ground
R18	GND		Ground
T18	GND		Ground
V18	GND		Ground
X18	GND		Ground
Z18	GND		Ground
AB18	GND		Ground
AD18	GND		Ground
C17	GND		Ground
E17	GND		Ground
G17	GND		Ground
I17	GND		Ground
K17	GND		Ground
M17	GND		Ground
O17	GND		Ground
Q17	GND		Ground
S17	GND		Ground
U17	GND		Ground
W17	GND		Ground
Y17	GND		Ground

Table 1. Pin descriptions

AA17	GND		Ground
AC17	GND		Ground
D16	GND		Ground
F16	GND		Ground
H16	GND		Ground
J16	GND		Ground
L16	GND		Ground
N16	GND		Ground
P16	GND		Ground
R16	GND		Ground
T16	GND		Ground
V16	GND		Ground
X16	GND		Ground
Z16	GND		Ground
AB16	GND		Ground
AD16	GND		Ground
C15	GND		Ground
E15	GND		Ground
G15	GND		Ground
I15	GND		Ground
W15	GND		Ground
Y15	GND		Ground
AA15	GND		Ground
AC15	GND		Ground
AE15	GND		Ground
D14	GND		Ground
F14	GND		Ground
H14	GND		Ground
X14	GND		Ground
Z14	GND		Ground
AB14	GND		Ground
AD14	GND		Ground
A13	GND		Ground
C13	GND		Ground
E13	GND		Ground
G13	GND		Ground
I13	GND		Ground
W13	GND		Ground
Y13	GND		Ground
AA13	GND		Ground
AC13	GND		Ground
AE13	GND		Ground
D12	GND		Ground
F12	GND		Ground
H12	GND		Ground
X12	GND		Ground
Z12	GND		Ground
AB12	GND		Ground
AD12	GND		Ground

Table 1. Pin descriptions

A11	GND		Ground
C11	GND		Ground
E11	GND		Ground
G11	GND		Ground
I11	GND		Ground
B10	GND		Ground
D10	GND		Ground
F10	GND		Ground
H10	GND		Ground
E9	GND		Ground
W9	GND		Ground
Y9	GND		Ground
AA9	GND		Ground
AC9	GND		Ground
F8	GND		Ground
H8	GND		Ground
E7	GND		Ground
W7	GND		Ground
AA7	GND		Ground
B6	GND		Ground
D6	GND		Ground
J6	GND		Ground
P6	GND		Ground
V6	GND		Ground
A5	GND		Ground
W5	GND		Ground
AA5	GND		Ground
AC5	GND		Ground
AE5	GND		Ground
F4	GND		Ground
J4	GND		Ground
R4	GND		Ground
T4	GND		Ground
V4	GND		Ground
AB4	GND		Ground
K3	GND		Ground
M3	GND		Ground
O3	GND		Ground
U3	GND		Ground
AC3	GND		Ground
J2	GND		Ground
P2	GND		Ground
V2	GND		Ground
Z2	GND		Ground
I1	GND		Ground
O1	GND		Ground
U1	GND		Ground
AA1	GND		Ground
GND1	GND		Ground
GND2	GND		Ground

Table 1. Pin descriptions

GND3	GND		Ground
GND4	GND		Ground
GND5	GND		Ground
GND6	GND		Ground
GND7	GND		Ground
GND8	GND		Ground
GND9	GND		Ground
GND10	GND		Ground
GND11	GND		Ground
GND12	GND		Ground
N14	GND		Ground
P14	GND		Ground
R14	GND		Ground
M13	GND		Ground
O13	GND		Ground
Q13	GND		Ground
S13	GND		Ground
N12	GND		Ground
P12	GND		Ground
R12	GND		Ground
M11	GND		Ground
O11	GND		Ground
Q11	GND		Ground
S11	GND		Ground
N10	GND		Ground
P10	GND		Ground
R10	GND		Ground
M9	GND		Ground
O9	GND		Ground
Q9	GND		Ground
S9	GND		Ground
N8	GND		Ground
P8	GND		Ground
R8	GND		Ground
G5	GND		Ground

Table 1. Pin descriptions

3.3 USB

This device supports universal serial bus (USB) connections for high-speed data communication. The relevant hardware satisfies the USB 2.0 specifications and supports maximum communications speeds of 480 Mbps

Pin NO.	Signal Name	Pin I/O (Modem host)	Function Description
M1	USB_D+	IO	USB Differential data line (+)
N2	USB_D-	IO	USB Differential data line (-)
K1	USB_VBUS	I	USB Power Supply

Table 2. USB Pin descriptions

3.4 Audio

This module includes a PCM interface. The pull-up and pull-down resistors attached to these pin must provide more than 50 Kohm of resistance.

Pin NO.	Signal Name	Pin I/O (Modem host)	Function Description
W1	PCM_SYNC	I	PCM Interface sync
X2	PCM_CLK	I	PCM Interface clock
Y1	PCM_TXD	O	PCM Interface digital audio data out
Y3	PCM_RXD	I	PCM Interface digital audio data in

Table 3. PCM Pin descriptions

3.5 User interface

Pin No.	Signal Name	Direction	Function
I5	BOOT_OK	O	Indicates that the Modem boot is complete.
C3	RESET_IN	I	Control line to unconditionally restart the module.
H4	MSG	O	Indicates that the Modem receive Urgent message.
G3	168H_END	O	Indicates that the 168hr sleep mode is end.
H6	ACC_ON_SLEEP	I	Control line to power on or 168hr sleep mode.
A3	Phone_ON	I	Control line to power on / off

Table 4. User interface Pin descriptions

4. Electrical specifications

4.1 Power supply specifications

The host system provides the power supply (VPH_PWR)DC 4 V, 2.5 A to the device. The internal power supply module manages the power supplied to the integral circuits and maintains constant voltages. This module also controls each power block to minimize power consumption.

In particular, the PAM (power amplifier module) consumes a lot of power, so it receives a direct power supply of 4 V from the VPH_PWR. Therefore the VPH_PWR signal inputs only the supply power of the PAM, even when the absolute rating is higher. In addition, the entire power input module blocks and protects against high surges and ESD in the NAD module.

Pin No.	Signal Name	Direction	MIN	TYP	MAX
A7,C7,B8,A9, B14,A15,B16, A17	VPH_PWR (for PAM / for PMIC)	I	3.9 V	4 V	4.1 V

Table 5. Power supply specifications

4.2 Logic level specifications

4.2.1 Digital logic level specifications

Signal Name	Type	Low		High		Unit
		Min	Max	Min	Max	
BOOT_OK	O	0	0.45	1.35	1.8	V
RESET_IN	I	-0.3	0.63	1.17	1.8	
MSG	O	0	0.45	1.35	1.8	
96H_END	O	0	0.45	1.35	1.8	
ACC_ON_SLEEP	I	0	0.63	1.17	1.8	

Table 6. Digital logic level specifications

5. RF specifications

5.1 LTE

5.1.1 Receiver

.- Bandwidth: 3GPP TS 36.521-1 Table 5.4.2.1-1
.- Frequency: B2(1930~1990 MHz), B4(2110~2155 MHz), B5(869~894 MHz),
B13(746~756 MHz)
.- Modulation method: QPSK, 16QAM and 64QAM
.- RX Sensitivity : B2, B5 (≤-94.3dBm @QPSK, BW: 10MHz)
B4 (≤-96.3dBm @QPSK, BW: 10MHz)
B13 (≤-93.3dBm @QPSK, BW: 10MHz)

5.1.2 Transmitter

.- Frequency: B2(1850~1910 MHz), B4(1710~1755 MHz), B5(824~849 MHz)
B13(777~787 MHz)
.- Maximum RF Output: Power class 3, 20.3dBm ~ 25.7dBm max.
.- Modulation method: QPSK and 16QAM
.- Baseband to RF Direct conversion (Zero IF)

6. Mechanical specifications

6.1 Environment specifications

.- Storage temp.: -40 ℃ - +85 ℃

.- Operating temp.: -20 ℃ - +70 ℃

(-20 ℃ - +70 ℃ : 3GPP specifications are satisfied

-30 ℃ - -20 ℃, +70 ℃ - +80 ℃ : May cause performance degradation)

.- Operating humidity: 80% (60℃) relative humidity

6. Mechanical specifications

6.1 Mechanical dimensions

Dimensions	34.0 x 40.0 x 3.5 mm (L x W x T) (Tolerance – width, length: ±0.15 / height: ±0.2)
Weight	Max. 10.6 grams

Table 7. Mechanical specification

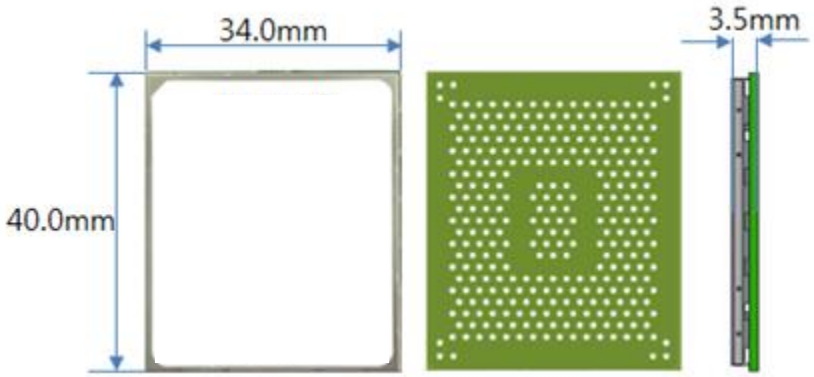

Figure 2. Mechanical dimension

7. General specifications

7.1 LTE (B2, B4 ,B5, B13)

시험 항목		Spec.	Test Temperature	Frequency	TX Channel		
					Low	Mid.	High
Maximum Output Power(class 3) CTQ		20.3~25.7dBm	Normal, Temp L, Temp H	Low, Mid, High	PASS	PASS	PASS
Frequency Error		±0.1ppm	Normal, Temp L, Temp H	Low, Mid, High	PASS	PASS	PASS
Error Vector Magnitude(EVM)		12.5%↓ (16QAM, 50 RB)	Normal	Low, Mid, High	PASS	PASS	PASS
Relative Carrier Leakage Power	Carrier Leakage (3.2dBm ± 3.2dB)	-24.2 dBc	Normal, Temp L, Temp H	Low, Mid, High	PASS	PASS	PASS
In-band emission	In-band emission (3.2dBm ± 3.2dB)	-24.2 dBc	Normal, Temp L, Temp H	Low, Mid, High	PASS	PASS	PASS
EVM equalizer spectrum flatness	EVM equalizer spectrum flatness Range1	5.4 dB ↓	Normal, Temp L, Temp H	Low, Mid, High	PASS	PASS	PASS
Spectrum emission mask	Spectrum Emission Mask upper/lower Area 1	-16.5 dBm ↓	Normal	Low, Mid, High	PASS	PASS	PASS
	Spectrum Emission Mask upper/lower Area 2	-8.5 dBm ↓			PASS	PASS	PASS
	Spectrum Emission Mask upper/lower Area 3	-11.5 dBm ↓			PASS	PASS	PASS
	Spectrum Emission Mask upper/lower Area 4	-23.5 dBm ↓			PASS	PASS	PASS
Adjacent Channel Leakage Power Ratio (ACLR)	ACLR E-UTRA ±	-29.2dB ↓	Normal, Temp L, Temp H	Low, Mid, High	PASS	PASS	PASS
	ACLR UTRA Offset 1 ±	-32.2dB ↓			PASS	PASS	PASS
	ACLR UTRA Offset 2 ±	-35.2dB ↓			PASS	PASS	PASS
Reference Sensitivity Level @ 10MHz CTQ	Ref Sense throughput shall be ≥ 95%	≤-96.3dBm (B4) ≤-93.3dBm (B13) ≤-94.3dBm (B2, B5) @ QPSK, BW: 10MHz Rx Chain=Dual	Normal, Temp L, Temp H	Low, Mid, High	PASS	PASS	PASS

8. RFx information

The strength of the RF field produced by the wireless module or modules embedded in the TCU is well within all international RF exposure limits known at this time. Because the wireless modules embedded in the TCU emit less than the maximum amount of energy permitted in radio frequency safety standards and recommendations, the manufacturer believes these modules are safe for use.

Regardless of the power levels, care should be taken to minimize human contact during normal operation. This module should be remain more than 20 cm (8 inches) from the body when wireless devices are on and transmitting.

This transmitter must not be collocated or operated in conjunction with any other antenna or transmitter. Operation is subject to the following two conditions: (1) this module does not cause interference , (2) this module accepts any interference that may cause undesired operation.

8.1 Information for the integrator

The integrator must not provide information to the end user regarding how to install or remove this RF module in the user manual of the end product. The user manual that is provided by the integrator for end users must include the following information in a prominent location. To comply with FCC RF exposure requirements, the antenna used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be collocated or operated in conjunction with any other antenna or transmitter.