PowerPC 440GP Embedded Processor Data Sheet

Features

- PowerPC® 440 processor core operating up to 400 MHz with 32 KB I- and D-caches
- Selectable processor:bus clock ratios of 3:1, 4:1, 5:2, 7:2
- Double Data Rate (DDR) Synchronous DRAM (SDRAM) interface operating up to 133 MHz
- On-chip 8 KB SRAM
- External Peripheral Bus for up to eight devices with external mastering
- DMA support for external peripherals, internal UART and memory
- PCI-X V1.0 Interface (32 or 64 bits, up to 133 MHz) with support for conventional PCI V2.2
- Two Ethernet 10/100 Mbps half- or full-duplex with support for MII or RMII or SMII interfaces
- Programmable Interrupt Controller supports interrupts from a variety of sources
- Programmable Timers
- Two serial ports (16750 compatible UART)
- Two IIC interfaces
- General Purpose I/O (GPIO) interface available
- JTAG interface for board level testing
- Internal Processor Local Bus (PLB) runs at DDR SDRAM interface frequency
- PowerPC processor boot from PCI memory

Description

Designed specifically to address high-end embedded applications, the PowerPC 440GP (PPC440GP) provides a high-performance, low power solution that interfaces to a wide range of peripherals by incorporating on-chip power management features and lower power dissipation.

This chip contains a high-performance RISC processor core, DDR SDRAM controller, PCI-X bus interface, Ethernet interface, control for external ROM and peripherals, DMA with scatter-gather support, serial ports, IIC interface, and general purpose I/O.

Technology: IBM CMOS SA-27E, 0.18 µm (0.11 Leff), 5-layer metal

Package: 25 mm, 552-ball Ceramic Ball Grid Array (CBGA)

Power (estimated): Less than 4.0 W. Less than 1.0 W in sleep mode

Voltages: 3.3 V I/O (except memory), 2.5 V memory interface, 1.8 V core logic and analog circuits

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Ordering and PVR Information

For information on the availability of the following parts, contact your local IBM sales office.

Product Name	Order Part Number[1]	Processor Frequency	Package	Rev Level	PVR Value	JTAG ID
PPC440GP	IBM25PPC440GP-3CC400C	400 MHz	25 mm, 552 CBGA	A	0x40120400	0x02052049
PPC440GP	IBM25PPC440GP-3CC400CZ	400 MHz	25 mm, 552 CBGA	A	0x40120400	0x02052049

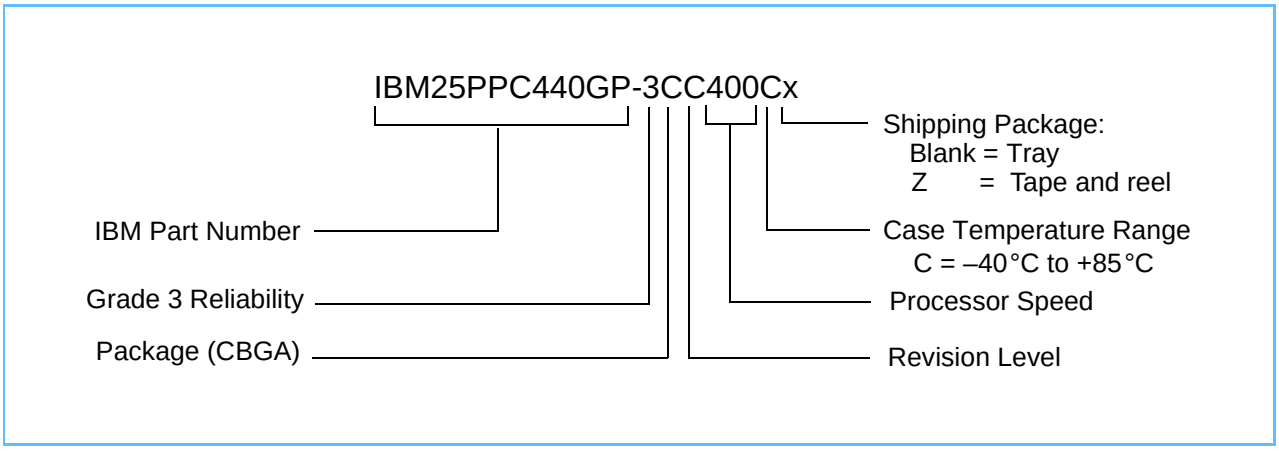
Notes:

1. Z at the end of the Order Part Number indicates a tape-and-reel shipping package. Otherwise, the chips are shipped in a tray.

Each part number contains a revision code. This is the die mask revision number and is included in the part number for identification purposes only.

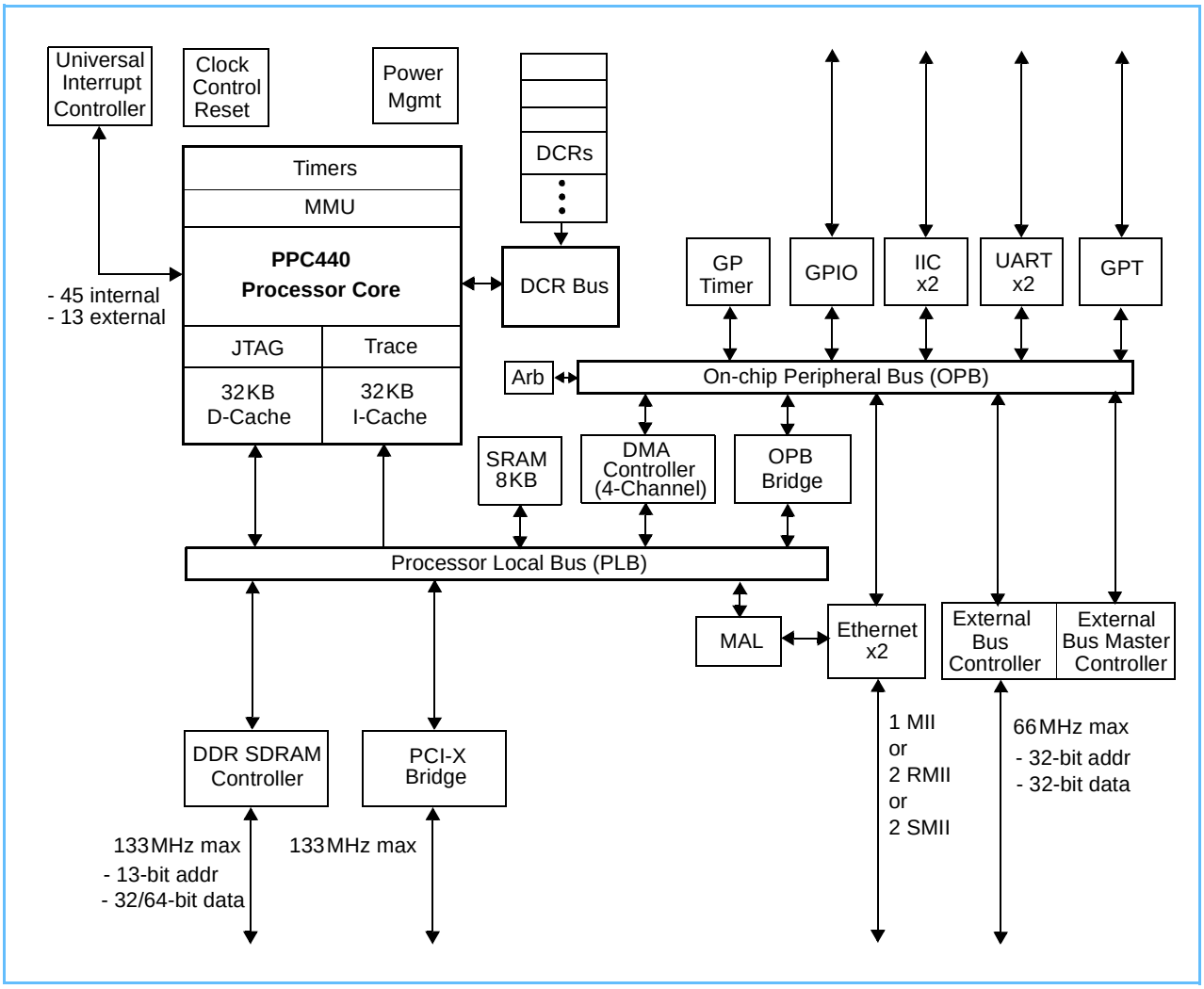
The PVR (Processor Version Register) is software accessible and contains additional information about the revision level of the part. Refer to the *PPC440GP User's Manual* for details on the register content.

Order Part Number Key



PowerPC 440GP Embedded Processor Data Sheet

PPC440GP Embedded Controller Functional Block Diagram



The PPC440GP is designed using the IBM Microelectronics Blue Logic™ methodology in which major functional blocks are integrated together to create an application-specific product (ASIC). This approach provides a consistent way to create complex ASICs using IBM CoreConnect Bus™ Architecture.

Note: IBM CoreConnect busses provide:

- 128-bit PLB interfaces up to 133.33MHz, 2.1GB/s
- 32-bit OPB interfaces up to 66.66MHz, 266MB/s

Address Map Support

The PPC440GP incorporates two address maps. The first is a fixed processor system memory address map that serves the PowerPC family of processors. This address map defines the possible contents of various address regions which the processor can access. The second address map is for Device Configuration Registers (DCRs). The DCRs are accessed by software running on the PPC440GP processor through the use of **mtdcr** and **mfdcr** instructions.

System Memory Address Map

Function	Sub Function	Start Address	End Address	Size
Local Memory[1]	DDR SDRAM	0 0000 0000	0 7FFF FFFF	2GB
	SRAM	0 8000 0000	0 8000 1FFF	8KB
	Reserve	0 8000 2000	0 FFFF FFFF	
Internal Peripherals	EBC	1 0000 0000	1 3FFF FFFF	1GB
	Reserved	1 4000 0000	1 4000 01FF	
	UART0	1 4000 0200	1 4000 0207	8B
	Reserved	1 4000 0208	1 4000 02FF	
	UART1	1 4000 0300	1 4000 0307	8B
	Reserved	1 4000 0308	1 4000 03FF	
	IIC0	1 4000 0400	1 4000 041F	32B
	Reserved	1 4000 0420	1 4000 04FF	
	IIC1	1 4000 0500	1 4000 051F	32B
	Reserved	1 4000 0520	1 4000 05FF	
	OPB Arbiter	1 4000 0600	1 4000 063F	64B
	Reserved	1 4000 0640	1 4000 06FF	
	GPIO Controller	1 4000 0700	1 4000 077F	128B
	Ethernet PHY ZMII	1 4000 0780	1 4000 078F	16B
	Reserved	1 4000 0790	1 4000 07FF	
	Ethernet MAC0 Controller	1 4000 0800	1 4000 08FF	256B
	Ethernet MAC1 Controller	1 4000 0900	1 4000 09FF	
	General Purpose Timer	1 4000 0A00	1 4000 0AFF	256B
	Reserved	1 4000 0B00	1 EFFF FFFF	
Expansion ROM[2]		1 F000 0000	1 FFDF FFFF	254MB
Boot ROM[2, 3]		1 FFE0 0000	1 FFFF FFFF	2MB
PCI	Reserved	2 0000 0000	2 07FF FFFF	
	PCI I/O	2 0800 0000	2 0800 FFFF	64KB
	Reserved	2 0801 0000	2 0EBF FFFF	
	PCI External Configuration Registers	2 0EC0 0000	2 0EC0 0007	8B
	Reserved	2 0EC0 0008	2 0EC7 FFFF	
	PCI Bridge Core Configuration Registers	2 0EC8 0000	2 0EC8 00FF	256B
	Reserved	2 0EC8 0100	2 0EC8 00FF	
	PCI Special Cycle	2 0ED0 0000	2 0EDF FFFF	1MB
	PCI Memory	2 0EE0 0000	F FFFF FFFF	55.76GB

Notes:

1. The Local Memory area of the memory map can be configured for DDR SDRAM or on-chip SRAM.
2. The Boot ROM and Expansion ROM areas of the memory map are intended for use by ROM or Flash-type devices. While locating volatile DDR SDRAM and SRAM in this region is supported by the controller, it is not recommended that these regions be used for this purpose.
3. When the optional boot from PCI memory is selected, the PCI Boot ROM address space begins at 2 FFFE 0000 (128 KB).

DCR Address Map 4KB Device Configuration Register

Function	Base Address Strap/Parameter	Start Address(0:9)	End Address(0:9)	Size
DCR Address Space[1]		000	3FF	1KW (4KB)[1]
Reserved		000	00F	16W
Memory Controller		010	011	2W
External Bus Controller		012	013	2W
External Bus Master I/F		014	015	2W
PLB Performance Monitor		016	01F	10W
SRAM		020	02F	16W
Reserved		030	07F	80W
PLB		080	08F	16W
PLB to OPB Bridge Out		090	09F	16W
Reserved		0A0	0A7	8W
OPB to PLB Bridge In		0A8	0AF	8W
Power Management		0B0	0B7	8W
Reserved		0B8	0BF	8W
Interrupt Controller 0		0C0	0CF	16W
Interrupt Controller 1		0D0	0DF	16W
Clock, Control, and Reset		0E0	0EF	16W
Reserved		0F0	0FF	16W
DMA Controller		100	13F	64W
Reserved		140	17F	64W
Ethernet MAL		180	1FF	128W
Reserved		200	3FF	512W

Notes:

1. DCR address space is addressable with up to 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register, or 1 kiloword (KW) (which equals 4 KB).

PowerPC 440 Processor Core

The PowerPC 440 processor core is designed for high-end applications: RAID controllers, routers, switches, printers, set-top boxes, etc. It is the first processor core to implement the new Book E PowerPC embedded architecture and the first to use the 128-bit version of IBM's on-chip CoreConnect Bus Architecture.

Features include:

- 400 MHz operation
- 3X PPC 405 performance
- 32 KB I-cache, 32 KB D-cache
- Three logical regions in D-cache: locked, transient, normal
- 41-bit virtual address, 36-bit (64 GB) physical address
- Superscalar, out-of-order execution
- 7-stage pipeline
- Three execution pipelines
- Dynamic branch prediction
- Memory management unit
  - 64-entry, full associative, unified TLB
  - Separate instruction and data micro-TLBs
  - Storage attributes for write-through, cache-inhibited, guarded, and big or little endian
- Debug facilities
  - Multiple instruction and data range breakpoints
  - Data value compare
  - Single step, branch, and trap events
  - Non-invasive real-time trace interface
- PowerPC Book E architecture
  - 24 DSP instructions
  - Single cycle multiply and multiply-accumulate
  - 32 x 32 integer multiply
  - 16 x 16 -> 32-bit MAC

Internal Buses

The PowerPC 440GP features three IBM standard on-chip buses: the Processor Local Bus (PLB), the On-Chip Peripheral Bus (OPB), and the Device Control Register Bus (DCR). The high performance, high bandwidth cores such as the PowerPC 440 processor core, the DDR SDRAM memory controller, and the PCI-X bridge connect to the PLB. The OPB hosts lower data rate peripherals. The daisy-chained DCR provides a lower bandwidth path for passing status and control information between the processor core and the other on-chip cores.

Features include:

- PLB
  - 128-bit implementation of the PLB architecture
  - Separate and simultaneous read and write data paths
  - 36-bit address
  - Simultaneous control, address, and data phases
  - Four levels of pipelining
  - Byte enable capability supporting unaligned transfers
  - 32- and 64-byte burst transfers
  - 133 MHz, maximum 4.2 GB/s (simultaneous read and write)
  - Processor:bus clock ratios of 3:1, 4:1, 5:2, and 7:2

- OPB
  - Dynamic bus sizing 32-, 16-, and 8-bit data path
  - Separate and simultaneous read and write data paths
  - 36-bit address
  - 66.66 MHz, maximum 266 MB/s
- DCR
  - 32-bit data path
  - 10 bit address

PCI-X Interface

The PCI-X interface allows connection of PCI and PCI-X devices to the PowerPC processor and local memory. This interface is designed to Version 1.0 of the PCI-X Specification and supports 32- and 64-bit PCI-X buses. PCI 32/64-bit legacy mode, compatible with PCI Version 2.2, is also supported.

Reference Specifications:
- PowerPC CoreConnect Bus (PLB) Specification Version 3.1
- PCI Specification Version 2.2
- PCI Bus Power Management Interface Specification Version 1.1

Features include:
- PCI-X 1.0
  - Split transactions
  - Frequency to 133 MHz
  - 32- and 64-bit bus
- PCI 2.2 backward compatibility
  - Frequency to 66 MHz
  - 32- and 64-bit bus
- Can be the PCI Host Bus Bridge or an Adapter Device's PCI interface
- Optional internal PCI arbitration function (up to five external devices) that can be disabled for use with an external arbiter
- Support for external I2O
- Support for Message Signaled Interrupts
- Simple message passing capability
- Asynchronous to the PLB
- PCI Power Management 1.1
- PCI register set addressable both from on-chip processor and PCI device sides
- Ability to boot from PCI-X bus memory
- Error tracking/status
- Supports initiation of transfer to the following address spaces:
  - Single beat I/O reads and writes
  - Single beat and burst memory reads and writes
  - Single beat configuration reads and writes (type 0 and type 1)
  - Single beat special cycles

DDR SDRAM Memory Controller

The Double Data Rate (DDR) SDRAM memory controller supports industry standard 184-pin DIMMS. Up to four 512 MB logical banks are supported in limited configurations. Global memory timings, address and bank sizes, and memory addressing modes are programmable.

Features include:

- Registered and non-registered industry standard DIMMs
- 32- or 64-bit memory interface with optional 8-bit ECC (SEC/DED)
- Sustainable 2.1GB/s peak bandwidth at 133MHz
- SSTL_2 logic
- 1 to 4 chip selects
- CAS latencies of 2, 2.5 and 3 supported
- PC200/266 support
- Page mode accesses (up to eight open pages) with configurable paging policy
- Programmable address mapping and timing
- Hardware and software initiated self-refresh
- Power management (self-refresh, suspend, sleep)

On-chip SRAM

- One physical bank of 8KB
- Memory cycles supported
  - Single beat read and write, one to 16 bytes
  - 32 and 64 byte burst transfers
  - Guarded memory accesses
- Sustainable 2.1GB/s peak bandwidth at 133MHz

External Peripheral Bus Controller (EBC)

- Up to eight ROM, EPROM, SRAM, Flash memory, and slave peripheral I/O banks supported
- Up to 66MHz operation (266MB/s)
- Burst and non-burst devices
- 8-, 16-, 32-bit byte-addressable data bus
- 32-bit address, 4GB address space
- Latch data on Ready, Synchronous or Asynchronous
- Programmable access timing per device
  - 256 Wait States for non-burst
  - 32 Burst Wait States for first access and up to 8 Wait States for subsequent accesses
  - Programmable CSon, CSoff relative to address
  - Programmable OEon, WEon, WEoff (1 to 4 clock cycles) relative to CS
- Programmable address mapping
- Peripheral Device pacing with external “Ready”
- External master interface
  - Write posting from external master
  - Read prefetching on PLB for external master reads
  - Bursting capable from external master
  - Allows external master access to all non-EBC PLB slaves
  - External master can control EBC slaves for own access and control

Ethernet Controller Interface

- One or two ethernet interfaces provided to the physical layer (PHY not included on the chip)
  - One full Media Independent Interface (MII) with 4-bit parallel data transfer
  - Two Reduced Media Independent Interfaces (RMII) with 2-bit parallel data transfer
  - Two Serial Media Independent Interfaces (SMII)
- Each interface full and half duplex at 10Mb/s or 100Mb/s

DMA Controller

- Supports the following transfers:
  - Memory-to-memory transfers
  - Buffered peripheral to memory transfers
  - Buffered memory to peripheral transfers
- Four channels
- Scatter/Gather capability for programming multiple DMA operations
- 8-, 16-, 32-bit peripheral support (OPB and external)
- 64-bit addressing
- Address increment or decrement
- Supports internal and external peripherals
- Support for memory mapped peripherals
- Support for peripherals running on slower frequency buses

Serial Port

- One 8-pin UART and one 4-pin UART interface provided
- Selectable internal or external serial clock to allow wide range of baud rates
- Register compatibility with NS16750 register set
- Complete status reporting capability
- Fully programmable serial-interface characteristics
- Supports DMA using internal DMA engine

IIC Bus Interface

- Two IIC interfaces provided
- Support for Phillips® Semiconductors I^2C Specification, dated 1995
- Operation at 100kHz or 400kHz
- 8-bit data
- 10- or 7-bit address
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Supports fixed V_{DD} IIC interface
- Two independent 4 x 1 byte data buffers
- Twelve memory-mapped, fully programmable configuration registers
- One programmable interrupt request signal
- Provides full management of all IIC bus protocols
- Programmable error recovery

General Purpose Timers

Provides a separate time base counter and additional system timers in addition to those defined in the processor core.

- 32-bit Time Base Counter driven by the OPB bus Clock
- Five 32-bit compare timers

General Purpose IO (GPIO) Controller

- Controller functions and GPIO registers are programmed and accessed via memory-mapped OPB bus master accesses.
- 31 GPIOs are pin-shared with other functions. DCRs control whether a particular pin that has GPIO capabilities acts as a GPIO or is used for another purpose.
- Each GPIO output is separately programmable to emulate an open drain driver (that is, drives to zero, tri-stated if output bit is 1).

Universal Interrupt Controller

Two Universal Interrupt Controllers (UIC) are available. They provide control, status, and communications necessary between the external and internal sources of interrupts and the on-chip PowerPC processor.

Note: Processor specific interrupts (for example, page faults) do not use UIC resources.

Features include:

- 13 external interrupts
- 45 internal interrupts
- Edge triggered or level-sensitive
- Positive or negative active
- Non-critical or critical interrupt to the on-chip processor core
- Programmable interrupt priority ordering
- Programmable critical interrupt vector for faster vector processing

JTAG

- IEEE 1149.1 Test Access Port
- IBM RISCWatch Debugger support
- JTAG Boundary Scan Description Language (BSDL)

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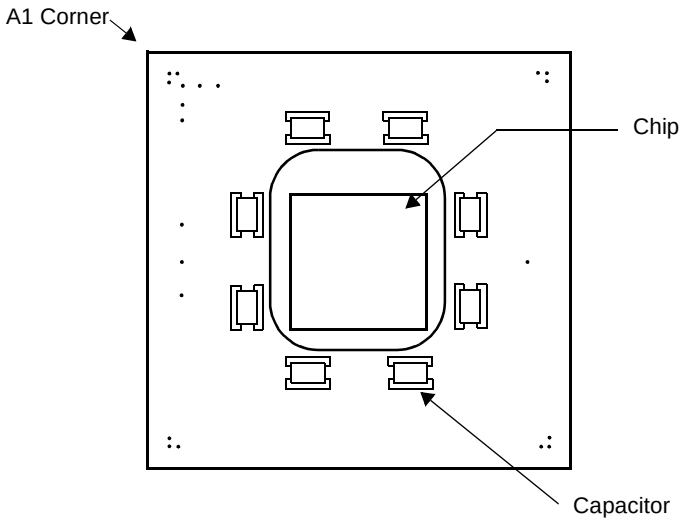
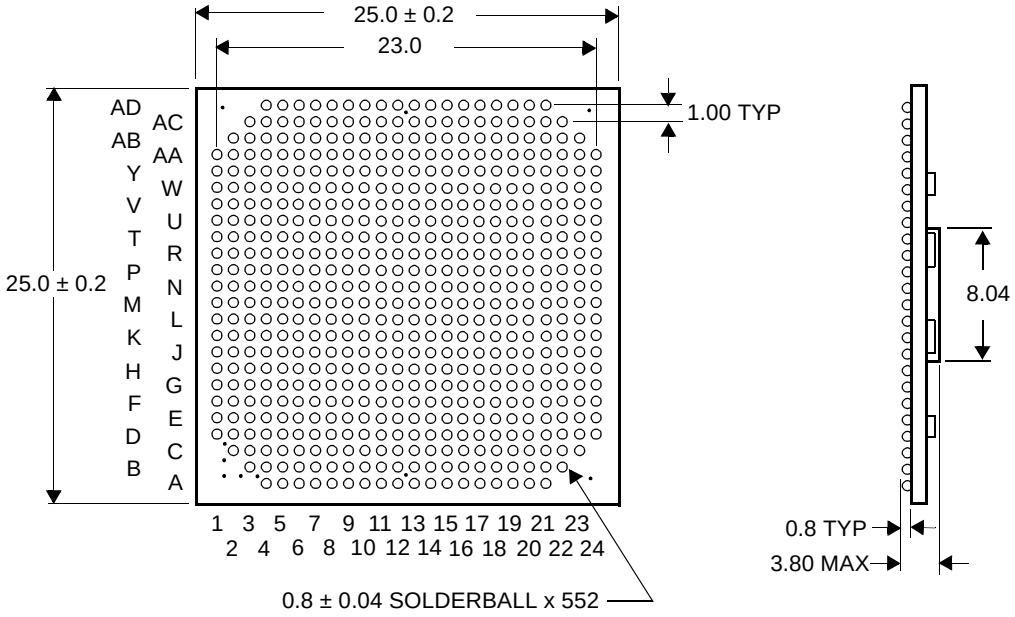
25mm, 552-Ball CBGA Package

Top View



Note: All dimensions are in mm.

Bottom View



Signal Lists

The following table lists all the external signals in alphabetical order and shows the ball number on which the signal appears. Multiplexed signals are shown with the default signal (following reset) *not* in brackets and the alternate signal in brackets. Multiplexed signals appear alphabetically multiple times in the list—once for each signal name on the ball. The page number listed gives the page in "Signal Functional Description" on page 35 where the signals in the indicated interface group begin.

Signals Listed Alphabetically (Part 1 of 14)

Signal Name	Ball	Interface Group	Page
AGND	J01 J24 AA11	Power	41
AMV_{DD}	AB11	Power MemClkOut PLL analog voltage	41
APV_{DD}	G01	Power PCI PLL analog voltage	41
ASV_{DD}	G24	Power SysClk PLL analog voltage	41
BA0 BA1	AA16 AD09	DDR SDRAM	36
$\overline{\text{BankSel0}}$ $\overline{\text{BankSel1}}$ $\overline{\text{BankSel2}}$ $\overline{\text{BankSel3}}$	AB15 W14 AD11 AD05	DDR SDRAM	36
[$\overline{\text{BE0}}$]PCIXC0 [$\overline{\text{BE1}}$]PCIXC1 [$\overline{\text{BE2}}$]PCIXC2 [$\overline{\text{BE3}}$]PCIXC3 [$\overline{\text{BE4}}$]PCIXC4 [$\overline{\text{BE5}}$]PCIXC5 [$\overline{\text{BE6}}$]PCIXC6 [$\overline{\text{BE7}}$]PCIXC7	F14 E16 C19 F20 C08 C03 G09 F09	PCI	35
BusReq	AA24	External Master Peripheral	38
$\overline{\text{CAS}}$	AB05	DDR SDRAM	36
ClkEn0 ClkEn1 ClkEn2 ClkEn3	AD17 AB10 Y09 W09	DDR SDRAM	36
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7 DM8	T16 AA18 AB14 P13 AA09 AA07 Y03 V03 AC05	DDR SDRAM	36
DMAAck0 DMAAck1 DMAAck2 DMAAck3	N05 P07 P06 P11	External Slave Peripheral	37

Signals Listed Alphabetically (Part 2 of 14)

Signal Name	Ball	Interface Group	Page
DMAReq0 DMAReq1 DMAReq2 DMAReq3	R03 M11 N11 P01	External Slave Peripheral	37
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7 DQS8	AC20 AC16 AC14 AB13 AC11 AC09 Y04 T01 AA05	DDR SDRAM	36
DrvrInh1 DrvrInh2	L07 A05	System	40
ECC0 ECC1 ECC2 ECC3 ECC4 ECC5 ECC6 ECC7	AB07 AB06 AD06 W07 U09 AC03 AB04 AD04	DDR SDRAM	36
EMCCD[EMC1RxErr]	J07	Ethernet	36
EMCCRS[EMC0CRSDV]	K07	Ethernet	36
EMCMDClk	J08	Ethernet	36
EMCMDIO	L05	Ethernet	36
EMCRxClk	J02	Ethernet	36
EMCRxD0[EMC0RxD0][EMC0RxD] EMCRxD1[EMC0RxD1][EMC1RxD] EMCRxD2[EMC1RxD0] EMCRxD3[EMC1RxD1]	G03 E01 A07 H09	Ethernet	36
EMCRxDV[EMC1CRSDV]	K01	Ethernet	36
EMCRxErr[EMC0RxErr]	K03	Ethernet	36
EMCTxClk[EMCRefClk]	J06	Ethernet	36
EMCTxD0[EMC0TxD0][EMC0TxD] EMCTxD1[EMC0TxD1][EMC1TxD] EMCTxD2[EMC1TxD0] EMCTxD3[EMC1TxD1]	L09 K05 J04 J03	Ethernet	36
EMCTxEn[EMC0TxEn][EMCSync]	L06	Ethernet	36
EMCTxErr[EMC1TxEn]	C05	Ethernet	36
EOT0/TC0 EOT1/TC1 EOT2/TC2 EOT3/TC3	R16 P15 P16 M16	External Slave Peripheral	37
$\overline{\text{ExtAck}}$	AA22	External Master Peripheral	38
$\overline{\text{ExtReq}}$	AB23	External Master Peripheral	38
$\overline{\text{ExtReset}}$	T17	External Master Peripheral	38

Signals Listed Alphabetically (Part 3 of 14)

Signal Name	Ball	Interface Group	Page
GND	B06 B10 B13 B17 B21 D04 D08 D12 D15 D19 D23 F02 F06 F10 F13 F17 F21 H04 H08 H12 H15 H19 H23 K02 K06 K10 K13 K17 K21 M04 M08 M12 M15 M19 M23 N02 N06 N10 N13 N17 N21 R04 R08 R12 R15 R19 R23 U02 U06 U10 U13 U17 U21\	Power	41

Signals Listed Alphabetically (Part 4 of 14)

Signal Name	Ball	Interface Group	Page
GND	W04 W08 W12 W15 W19 W23 AA02 AA06 AA10 AA13 AA17 AA21 AC04 AC08 AC12 AC15 AC19	Power	41
[GPIO0]IRQ0	N18	System	40
[GPIO1]IRQ1	L20		
[GPIO2]IRQ2	P20		
[GPIO3]IRQ3	L18		
[GPIO4]IRQ4	N14		
[GPIO5]IRQ5	M20		
[GPIO6]IRQ6	M14		
[GPIO7]IRQ7	P18		
[GPIO8]IRQ8	N20		
[GPIO9]IRQ9	P22		
[GPIO10]IRQ10	V18		
GPIO11	P14		
[GPIO12]UART1_Rx	C18		
[GPIO13]UART1_Tx	J16		
[GPIO14]$\overline{\text{UART1\_DSR/CTS}}$	G06		
[GPIO15]$\overline{\text{UART1\_RTS/DTR}}$	E05		
[GPIO16]IIC1SClk	H11		
[GPIO17]IIC1SDA	H14		
[GPIO18]TrcBS0	N16		
[GPIO19]TrcBS1	P17		
[GPIO20]TrcBS2	T20		
[GPIO21]TrcES0	T21		
[GPIO22]TrcES1	P23		
[GPIO23]TrcES2	N09		
[GPIO24]TrcES3	P08		
[GPIO25]TrcES4	T05		
[GPIO26]TrcTS0	T04		
[GPIO27]TrcTS1	P03		
[GPIO28]TrcTS2	R07		
[GPIO29]TrcTS3	P09		
[GPIO30]TrcTS4	R09		
[GPIO31]TrcTS5	T06		
$\overline{\text{Halt}}$	V05	System	40
HoldAck	Y21	External Master Peripheral	38
HoldReq	Y23	External Master Peripheral	38

Signals Listed Alphabetically (Part 5 of 14)

Signal Name	Ball	Interface Group	Page
IIC0SClk	G11	IIC Peripheral	38
IIC0SDA	G13	IIC Peripheral	38
IIC1SClk[GPIO16]	H11	IIC Peripheral	38
IIC1SDA[GPIO17]	H14	IIC Peripheral	38
IRQ0[GPIO0] IRQ1[GPIO1] IRQ2[GPIO2] IRQ3[GPIO3 IRQ4[GPIO4] IRQ5[GPIO5] IRQ6[GPIO6] IRQ7[GPIO7] IRQ8[GPIO8] IRQ9[GPIO9] IRQ10[GPIO10] [IRQ11]$\overline{\text{PCIReq1}}$ [IRQ12]$\overline{\text{PCIGnt1}}$	N18 L20 P20 L18 N14 M20 M14 P18 N20 P22 V18 E21 C22	Interrupts	39
MemAddr0 MemAddr1 MemAddr2 MemAddr3 MemAddr4 MemAddr5 MemAddr6 MemAddr7 MemAddr8 MemAddr9 MemAddr10 MemAddr11 MemAddr12	Y19 AD20 Y20 AB20 AD18 AD16 AB18 Y14 V13 V11 W16 Y11 V10	DDR SDRAM	36
$\overline{\text{MemClkOut0}}$ $\overline{\text{MemClkOut0}}$	V09 V08	DDR SDRAM	36

Signals Listed Alphabetically (Part 6 of 14)

Signal Name	Ball	Interface Group	Page
MemData0	AD21	DDR SDRAM	36
MemData1	AB21		
MemData2	AC22		
MemData3	AA20		
MemData4	U16		
MemData5	V17		
MemData6	AD19		
MemData7	AB19		
MemData8	W18		
MemData9	V16		
MemData10	Y17		
MemData11	AB16		
MemData12	AC18		
MemData13	Y18		
MemData14	R14		
MemData15	AB17		
MemData16	AA14		
MemData17	AD15		
MemData18	T15		
MemData19	V15		
MemData20	Y16		
MemData21	U14		
MemData22	T13		
MemData23	Y15		
MemData24	AD13		
MemData25	AD14		
MemData26	V14		
MemData27	Y13		
MemData28	P12		
MemData29	AB12		
MemData30	Y12		
MemData31	V12		

Signals Listed Alphabetically (Part 7 of 14)

Signal Name	Ball	Interface Group	Page
MemData32	W11	DDR SDRAM	36
MemData33	AD12		
MemData34	Y10		
MemData35	T12		
MemData36	U11		
MemData37	T11		
MemData38	T10		
MemData39	AD10		
MemData40	AB08		
MemData41	AD08		
MemData42	R11		
MemData43	Y07		
MemData44	AC07		
MemData45	AB09		
MemData46	Y06		
MemData47	Y08		
MemData48	AA01		
MemData49	AA03		
MemData50	AB02		
MemData51	Y01		
MemData52	AB03		
MemData53	Y02		
MemData54	V07		
MemData55	V01		
MemData56	T08		
MemData57	U07		
MemData58	W01		
MemData59	W03		
MemData60	V06		
MemData61	T07		
MemData62	W05		
MemData63	U05		
MemVRef1	T14	DDR SDRAM	36
MemVRef2	T09		

Signals Listed Alphabetically (Part 8 of 14)

Signal Name	Ball	Interface Group	Page
No ball	A01 A02 A03 A22 A23 A24 B01 B02 B23 B24 C01 C24 AB01 AB24 AC01 AC02 AC23 AC24 AD01 AD02 AD03 AD22 AD23 AD24	A physical ball does not exist at these ball coordinates.	
OV_{DD}	B04 B12 B19 D02 D10 D17 F08 F15 F23 H06 H10 H13 H21 K04 K08 K19 M02 M17 N08 N23 R06 R17 R21 U04 U19 W02 AA23	Power	41
$\overline{\text{PCIXAck64}}$	D09	PCI-X	35

Signals Listed Alphabetically (Part 9 of 14)

Signal Name	Ball	Interface Group	Page
PCIXAD0	C17	PCI-X	35
PCIXAD1	B09		
PCIXAD2	G10		
PCIXAD3	E10		
PCIXAD4	C10		
PCIXAD5	A10		
PCIXAD6	F11		
PCIXAD7	G12		
PCIXAD8	G14		
PCIXAD9	A15		
PCIXAD10	C15		
PCIXAD11	E15		
PCIXAD12	G15		
PCIXAD13	B16		
PCIXAD14	C16		
PCIXAD15	D16		
PCIXAD16	E18		
PCIXAD17	E19		
PCIXAD18	F18		
PCIXAD19	G18		
PCIXAD20	D20		
PCIXAD21	A20		
PCIXAD22	A21		
PCIXAD23	C21		
PCIXAD24	F22		
PCIXAD25	B22		
PCIXAD26	G21		
PCIXAD27	E23		
PCIXAD28	C23		
PCIXAD29	F24		
PCIXAD30	D22		
PCIXAD31	D24		

Signals Listed Alphabetically (Part 10 of 14)

Signal Name	Ball	Interface Group	Page
PCIXAD32	H03	PCI-X	35
PCIXAD33	H01		
PCIXAD34	L08		
PCIXAD35	F01		
PCIXAD36	D01		
PCIXAD37	J05		
PCIXAD38	H05		
PCIXAD39	G02		
PCIXAD40	E02		
PCIXAD41	C02		
PCIXAD42	A08		
PCIXAD43	G05		
PCIXAD44	F03		
PCIXAD45	D03		
PCIXAD46	B03		
PCIXAD47	H07		
PCIXAD48	G04		
PCIXAD49	E04		
PCIXAD50	C04		
PCIXAD51	A04		
PCIXAD52	F05		
PCIXAD53	D05		
PCIXAD54	B05		
PCIXAD55	C09		
PCIXAD56	E06		
PCIXAD57	C06		
PCIXAD58	A06		
PCIXAD59	F07		
PCIXAD60	E07		
PCIXAD61	D07		
PCIXAD62	B07		
PCIXAD63	E08		
PCIXC0[$\overline{\text{BE0}}$]	F14	PCI-X	35
PCIXC1[$\overline{\text{BE1}}$]	E16		
PCIXC2[$\overline{\text{BE2}}$]	C19		
PCIXC3[$\overline{\text{BE3}}$]	F20		
PCIXC4[$\overline{\text{BE4}}$]	C08		
PCIXC5[$\overline{\text{BE5}}$]	C03		
PCIXC6[$\overline{\text{BE6}}$]	G09		
PCIXC7[$\overline{\text{BE7}}$]	F09		
PCIXClk	E03	PCI-X	35
$\overline{\text{PCIXDevSel}}$	E13	PCI-X	35
$\overline{\text{PCIXFrame}}$	A11	PCI-X	35
$\overline{\text{PCIXGnt0}}$	E22	PCI-X	35
$\overline{\text{PCIXGnt1}}$[IRQ12]	C22		
$\overline{\text{PCIXGnt2}}$	N22		
$\overline{\text{PCIXGnt3}}$	M18		
$\overline{\text{PCIXGnt4}}$	R22		
$\overline{\text{PCIXGnt5}}$	P19		
PCIXIDSel	G07	PCI-X	35
$\overline{\text{PCIXINT}}$	M07	PCI-X	35
$\overline{\text{PCIXIRDY}}$	E12	PCI-X	35

Signals Listed Alphabetically (Part 11 of 14)

Signal Name	Ball	Interface Group	Page
PCIXM66En	A14	PCI-X	35
PCIXParHigh	L04	PCI-X	35
PCIXParLow	F16	PCI-X	35
$\overline{\text{PCIXPErr}}$	A17	PCI-X	35
$\overline{\text{PCIXReq0}}$ $\overline{\text{PCIXReq1}}$[IRQ11] $\overline{\text{PCIXReq2}}$ $\overline{\text{PCIXReq3}}$ $\overline{\text{PCIXReq4}}$ $\overline{\text{PCIXReq5}}$	E24 E21 E20 R20 G23 R18	PCI-X	35
$\overline{\text{PCIXReq64}}$	E09	PCI-X	35
$\overline{\text{PCIXReset}}$	M24	PCI-X	35
$\overline{\text{PCIXSErr}}$	A18	PCI-X	35
$\overline{\text{PCIXStop}}$	L12	PCI-X	35
$\overline{\text{PCIXTRDY}}$	C12	PCI-X	35
PCIX133Cap	G08	PCI-X	35
PCIXCap	L23	PCI-X	35
PerAddr0 PerAddr1 PerAddr2 PerAddr3 PerAddr4 PerAddr5 PerAddr6 PerAddr7 PerAddr8 PerAddr9 PerAddr10 PerAddr11 PerAddr12 PerAddr13 PerAddr14 PerAddr15 PerAddr16 PerAddr17 PerAddr18 PerAddr19 PerAddr20 PerAddr21 PerAddr22 PerAddr23 PerAddr24 PerAddr25 PerAddr26 PerAddr27 PerAddr28 PerAddr29 PerAddr30 PerAddr31	D11 C11 B11 A12 A19 D18 E11 M03 N01 E14 C20 A16 A13 B14 C14 D14 B20 L15 L21 L22 M22 M01 L24 P24 T19 R24 U22 U24 N03 V20 V23 V21	External Slave Peripheral **Note:** PerAddr0 is the most significant bit (msb) on this bus.	37

Signals Listed Alphabetically (Part 12 of 14)

Signal Name	Ball	Interface Group	Page
PerBE0 PerBE1 PerBE2 PerBE3	T18 V19 W22 W24	External Slave Peripheral	37
PerBLast	C07	External Slave Peripheral	37
PerClk	U18	External Master Peripheral	38
PerCS0 PerCS1 PerCS2 PerCS3 PerCS4 PerCS5 PerCS6 PerCS7	E17 L10 V04 T24 L03 T03 L13 U03	External Slave Peripheral	37
PerData0 PerData1 PerData2 PerData3 PerData4 PerData5 PerData6 PerData7 PerData8 PerData9 PerData10 PerData11 PerData12 PerData13 PerData14 PerData15 PerData16 PerData17 PerData18 PerData19 PerData20 PerData21 PerData22 PerData23 PerData24 PerData25 PerData26 PerData27 PerData28 PerData29 PerData30 PerData31	H24 H22 H20 G20 G19 H18 J23 J22 J21 J20 J19 J18 J17 J15 J14 J13 J12 J11 J10 J09 L14 K24 K22 K20 K18 K16 K14 K11 K09 L19 L17 L16	External Slave Peripheral **Note:** PerData0 is the most significant bit (msb) on this bus.	37
PerErr	P21	External Master Peripheral	38
PerOE	M09	External Slave Peripheral	37
PerPar0 PerPar1 PerPar2 PerPar3	T23 T22 W20 U20	External Slave Peripheral	37

Signals Listed Alphabetically (Part 13 of 14)

Signal Name	Ball	Interface Group	Page
PerR/$\overline{W}$	P05	External Slave Peripheral	37
PerReady[RcvrInh]	N07	External Slave Peripheral	37
$\overline{PerWE}$	P02	External Slave Peripheral	37
$\overline{RAS}$	AD07	DDR SDRAM	36
[RcvrInh]PerReady	N07	System	40
RefVEn	L02	System	40
Reserved	L01 P04	Reserved	41
SV_{DD}	U12 U15 W10 W17 AA08 AA15 AC06 AC13 AC21	Power	41
SysClk	G22	System	40
SysErr	T02	System	40
$\overline{SysReset}$	P10	System	40
TCK	V22	JTAG	40
TDI	Y24	JTAG	40
TDO	Y22	JTAG	40
TestEn	M05	System	40
TmrClk	U01	System	40
TMS	AB22	JTAG	40
TrcBS0[GPIO18] TrcBS1[GPIO19] TrcBS2[GPIO20]	N16 P17 T20	Trace	41
TrcClk	R05	Trace	41
TrcES0[GPIO21] TrcES1[GPIO22] TrcES2[GPIO23] TrcES3[GPIO24] TrcES4[GPIO25]	T21 P23 N09 P08 T05	Trace	41
TrcTS0[GPIO26] TrcTS1[GPIO27] TrcTS2[GPIO28] TrcTS3[GPIO29] TrcTS4[GPIO30] TrcTS5[GPIO31] TrcTS6	T04 P03 R07 P09 R09 T06 R01	Trace	41
$\overline{TRST}$	N24	JTAG	40
$\overline{UART0\_CTS}$	C13	UART Peripheral	38
$\overline{UART0\_DCD}$	V24	UART Peripheral **Note:** Used as initialization strapping input.	38
$\overline{UART0\_DSR}$	V02	UART Peripheral **Note:** Used as initialization strapping input.	38
$\overline{UART0\_DTR}$	B18	UART Peripheral	38

Signals Listed Alphabetically (Part 14 of 14)

Signal Name	Ball	Interface Group	Page
UART0_RI	H16	UART Peripheral	38
UART0_RTS	G16	UART Peripheral	38
UART0_Rx	G17	UART Peripheral	38
UART0_Tx	L11	UART Peripheral	38
UART1_DSR/CTS[GPIO14]	G06	UART Peripheral	38
UART1_RTS/DTR[GPIO15]	E05	UART Peripheral	38
UART1_Rx[GPIO12]	C18	UART Peripheral	38
UART1_Tx[GPIO13]	J16	UART Peripheral	38
UARTSerClk	A09	UART Peripheral	38
V_{DD}	B08 B15 D06 D13 D21 F04 F12 F19 H02 H17 K12 K15 K23 M06 M10 M13 M21 N04 N12 N15 N19 R02 R10 R13 U08 U23 W06 W13 W21 AA04 AA12 AA19 AC10 AC17	Power	41
WE	Y05	DDR SDRAM	36

Signals Listed by Ball Assignment (Part 1 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A01	No ball	B01	No ball	C01	No ball	D01	PCIXAD36
A02	No ball	B02	No ball	C02	PCIXAD41	D02	OV_{DD}
A03	No ball	B03	PCIXAD46	C03	PCIXC5[$\overline{BE5}$]	D03	PCIXAD45
A04	PCIXAD51	B04	OV_{DD}	C04	PCIXAD50	D04	GND
A05	DrvrInh2	B05	PCIXAD54	C05	EMCTxErr [EMC1TxEn]	D05	PCIXAD53
A06	PCIXAD58	B06	GND	C06	PCIXAD57	D06	V_{DD}
A07	EMCRxD2 [EMC1RxD0]	B07	PCIXAD62	C07	$\overline{PerBLast}$	D07	PCIXAD61
A08	PCIXAD42	B08	V_{DD}	C08	PCIXC4[$\overline{BE4}$]	D08	GND
A09	UARTSerClk	B09	PCIXAD1	C09	PCIXAD55	D09	$\overline{PCIXAck64}$
A10	PCIXAD5	B10	GND	C10	PCIXAD4	D10	OV_{DD}
A11	$\overline{PCIXFrame}$	B11	PerAddr2	C11	PerAddr1	D11	PerAddr0
A12	PerAddr3	B12	OV_{DD}	C12	$\overline{PCIXTRDY}$	D12	GND
A13	PerAddr12	B13	GND	C13	$\overline{UART0\_CTS}$	D13	V_{DD}
A14	PCIXM66En	B14	PerAddr13	C14	PerAddr14	D14	PerAddr15
A15	PCIXAD9	B15	V_{DD}	C15	PCIXAD10	D15	GND
A16	PerAddr11	B16	PCIXAD13	C16	PCIXAD14	D16	PCIXAD15
A17	$\overline{PCIXPErr}$	B17	GND	C17	PCIXAD0	D17	OV_{DD}
A18	$\overline{PCIXSErr}$	B18	$\overline{UART0\_DTR}$	C18	UART1_Rx[GPIO12]	D18	PerAddr5
A19	PerAddr4	B19	OV_{DD}	C19	PCIXC2[$\overline{BE2}$]	D19	GND
A20	PCIXAD21	B20	PerAddr16	C20	PerAddr10	D20	PCIXAD20
A21	PCIXAD22	B21	GND	C21	PCIXAD23	D21	V_{DD}
A22	No ball	B22	PCIXAD25	C22	$\overline{PCIXGnt1}$[IRQ12]	D22	PCIXAD30
A23	No ball	B23	No ball	C23	PCIXAD28	D23	GND
A24	No ball	B24	No ball	C24	No ball	D24	PCIXAD31

Signals Listed by Ball Assignment (Part 2 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
E01	EMCRxD1 [EMC0RxD1] [EMC1RxD]	F01	PCIXAD35	G01	APV_{DD} for PCI PLL	H01	PCIXAD33
E02	PCIXAD40	F02	GND	G02	PCIXAD39	H02	V_{DD}
E03	PCIXClk	F03	PCIXAD44	G03	EMCRxD0 [EMC0RxD0] [EMC0RxD]	H03	PCIXAD32
E04	PCIXAD49	F04	V_{DD}	G04	PCIXAD48	H04	GND
E05	$\overline{\text{UART1\_RTS/DTR}}$ [GPIO15]	F05	PCIXAD52	G05	PCIXAD43	H05	PCIXAD38
E06	PCIXAD56	F06	GND	G06	$\overline{\text{UART1\_DSR/CTS}}$ [GPIO14]	H06	OV_{DD}
E07	PCIXAD60	F07	PCIXAD59	G07	PCIXIDSel	H07	PCIXAD47
E08	PCIXAD63	F08	OV_{DD}	G08	PCIX133Cap	H08	GND
E09	$\overline{\text{PCIXReq64}}$	F09	PCIXC7[$\overline{\text{BE7}}$]	G09	PCIXC6[$\overline{\text{BE6}}$]	H09	EMCRxD3 [EMC1RxD1]
E10	PCIXAD3	F10	GND	G10	PCIXAD2	H10	OV_{DD}
E11	PerAddr6	F11	PCIXAD6	G11	IIC0SClk	H11	IIC1SClk[GPIO16]
E12	$\overline{\text{PCIXIRDY}}$	F12	V_{DD}	G12	PCIXAD7	H12	GND
E13	$\overline{\text{PCIXDevSel}}$	F13	GND	G13	IIC0SDA	H13	OV_{DD}
E14	PerAddr9	F14	PCIXC0[$\overline{\text{BE0}}$]	G14	PCIXAD8	H14	IIC1SDA[GPIO17]
E15	PCIXAD11	F15	OV_{DD}	G15	PCIXAD12	H15	GND
E16	PCIXC1[$\overline{\text{BE1}}$]	F16	PCIXParLow	G16	$\overline{\text{UART0\_RTS}}$	H16	$\overline{\text{UART0\_RI}}$
E17	$\overline{\text{PerCS0}}$	F17	GND	G17	UART0_Rx	H17	V_{DD}
E18	PCIXAD16	F18	PCIXAD18	G18	PCIXAD19	H18	PerData5
E19	PCIXAD17	F19	V_{DD}	G19	PerData4	H19	GND
E20	$\overline{\text{PCIXReq2}}$	F20	PCIXC3[$\overline{\text{BE3}}$]	G20	PerData3	H20	PerData2
E21	$\overline{\text{PCIXReq1}}$[IRQ11]	F21	GND	G21	PCIXAD26	H21	OV_{DD}
E22	$\overline{\text{PCIXGnt0}}$	F22	PCIXAD24	G22	SysClk	H22	PerData1
E23	PCIXAD27	F23	OV_{DD}	G23	$\overline{\text{PCIXReq4}}$	H23	GND
E24	$\overline{\text{PCIXReq0}}$	F24	PCIXAD29	G24	ASV_{DD} for SysClk PLL	H24	PerData0

Signals Listed by Ball Assignment (Part 3 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
J01	AGND	K01	EMCRxDV [EMC1CRSDV]	L01	Reserved	M01	PerAddr21
J02	EMCRxClk	K02	GND	L02	RefVEn	M02	OV_{DD}
J03	EMCTxD3 [EMC1TxD1]	K03	EMCRxErr [EMC0RxErr]	L03	$\overline{\text{PerCS4}}$	M03	PerAddr7
J04	EMCTxD2 [EMC1TxD0]	K04	OV_{DD}	L04	PCIXParHigh	M04	GND
J05	PCIXAD37	K05	EMCTxD1 [EMC0TxD1] [EMC1TxD]	L05	EMCMDIO	M05	TestEn
J06	EMCTxClk [EMCRefClk]	K06	GND	L06	EMCTxEn [EMC0TxEn] [EMCSync]	M06	V_{DD}
J07	EMCCD[EMC1RxErr]	K07	EMCCRS [EMC0CRSDV]	L07	DrvrInh1	M07	$\overline{\text{PCIXINT}}$
J08	EMCMDClk	K08	OV_{DD}	L08	PCIXAD34	M08	GND
J09	PerData19	K09	PerData28	L09	EMCTxD0 [EMC0TxD0] [EMC0TxD]	M09	$\overline{\text{PerOE}}$
J10	PerData18	K10	GND	L10	$\overline{\text{PerCS1}}$	M10	V_{DD}
J11	PerData17	K11	PerData27	L11	UART0_Tx	M11	DMAReq1
J12	PerData16	K12	V_{DD}	L12	$\overline{\text{PCIXStop}}$	M12	GND
J13	PerData15	K13	GND	L13	$\overline{\text{PerCS6}}$	M13	V_{DD}
J14	PerData14	K14	PerData26	L14	PerData20	M14	IRQ6[GPIO6]
J15	PerData13	K15	V_{DD}	L15	PerAddr17	M15	GND
J16	UART1_Tx[GPIO13]	K16	PerData25	L16	PerData31	M16	EOT3/TC3
J17	PerData12	K17	GND	L17	PerData30	M17	OV_{DD}
J18	PerData11	K18	PerData24	L18	IRQ3[GPIO3]	M18	$\overline{\text{PCIXGnt3}}$
J19	PerData10	K19	OV_{DD}	L19	PerData29	M19	GND
J20	PerData9	K20	PerData23	L20	IRQ1[GPIO1]	M20	IRQ5[GPIO5]
J21	PerData8	K21	GND	L21	PerAddr18	M21	V_{DD}
J22	PerData7	K22	PerData22	L22	PerAddr19	M22	PerAddr20
J23	PerData6	K23	V_{DD}	L23	PCIXCap	M23	GND
J24	AGND	K24	PerData21	L24	PerAddr22	M24	$\overline{\text{PCIXReset}}$

Signals Listed by Ball Assignment (Part 4 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
N01	PerAddr8	P01	DMAReq3	R01	TrcTS6	T01	DQS7
N02	GND	P02	$\overline{\text{PerWE}}$	R02	V_{DD}	T02	SysErr
N03	PerAddr28	P03	TrcTS1[GPIO27]	R03	DMAReq0	T03	$\overline{\text{PerCS5}}$
N04	V_{DD}	P04	Reserved	R04	GND	T04	TrcTS0[GPIO26]
N05	DMAAck0	P05	PerR/$\overline{\text{W}}$	R05	TrcClk	T05	TrcES4[GPIO25]
N06	GND	P06	DMAAck2	R06	OV_{DD}	T06	TrcTS5[GPIO31]
N07	PerReady[RcvrInh]	P07	DMAAck1	R07	TrcTS2[GPIO28]	T07	MemData61
N08	OV_{DD}	P08	TrcES3[GPIO24]	R08	GND	T08	MemData56
N09	TrcES2[GPIO23]	P09	TrcTS3[GPIO29]	R09	TrcTS4[GPIO30]	T09	MemVRef2
N10	GND	P10	$\overline{\text{SysReset}}$	R10	V_{DD}	T10	MemData38
N11	DMAReq2	P11	DMAAck3	R11	MemData42	T11	MemData37
N12	V_{DD}	P12	MemData28	R12	GND	T12	MemData35
N13	GND	P13	DM3	R13	V_{DD}	T13	MemData22
N14	IRQ4[GPIO4]	P14	GPIO11	R14	MemData14	T14	MemVRef1
N15	V_{DD}	P15	EOT1/TC1	R15	GND	T15	MemData18
N16	TrcBS0[GPIO18]	P16	EOT2/TC2	R16	EOT0/TC0	T16	DM0
N17	GND	P17	TrcBS1[GPIO19]	R17	OV_{DD}	T17	$\overline{\text{ExtReset}}$
N18	IRQ0[GPIO0]	P18	IRQ7[GPIO7]	R18	$\overline{\text{PCIXReq5}}$	T18	$\overline{\text{PerBE0}}$
N19	V_{DD}	P19	$\overline{\text{PCIXGnt5}}$	R19	GND	T19	PerAddr24
N20	IRQ8[GPIO8]	P20	IRQ2[GPIO2]	R20	$\overline{\text{PCIXReq3}}$	T20	TrcBS2[GPIO20]
N21	GND	P21	PerErr	R21	OV_{DD}	T21	TrcES0[GPIO21]
N22	$\overline{\text{PCIXGnt2}}$	P22	IRQ9[GPIO9]	R22	$\overline{\text{PCIXGnt4}}$	T22	PerPar1
N23	OV_{DD}	P23	TrcES1[GPIO22]	R23	GND	T23	PerPar0
N24	$\overline{\text{TRST}}$	P24	PerAddr23	R24	PerAddr25	T24	$\overline{\text{PerCS3}}$

Signals Listed by Ball Assignment (Part 5 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
U01	TmrClk	V01	MemData55	W01	MemData58	Y01	MemData51
U02	GND	V02	UART0_DSR	W02	OV_{DD}	Y02	MemData53
U03	PerCS7	V03	DM7	W03	MemData59	Y03	DM6
U04	OV_{DD}	V04	PerCS2	W04	GND	Y04	DQS6
U05	MemData63	V05	Halt	W05	MemData62	Y05	WE
U06	GND	V06	MemData60	W06	V_{DD}	Y06	MemData46
U07	MemData57	V07	MemData54	W07	ECC3	Y07	MemData43
U08	V_{DD}	V08	MemClkOut0	W08	GND	Y08	MemData47
U09	ECC4	V09	MemClkOut0	W09	ClkEn3	Y09	ClkEn2
U10	GND	V10	MemAddr12	W10	SV_{DD}	Y10	MemData34
U11	MemData36	V11	MemAddr9	W11	MemData32	Y11	MemAddr11
U12	SV_{DD}	V12	MemData31	W12	GND	Y12	MemData30
U13	GND	V13	MemAddr8	W13	V_{DD}	Y13	MemData27
U14	MemData21	V14	MemData26	W14	BankSel1	Y14	MemAddr7
U15	SV_{DD}	V15	MemData19	W15	GND	Y15	MemData23
U16	MemData4	V16	MemData9	W16	MemAddr10	Y16	MemData20
U17	GND	V17	MemData5	W17	SV_{DD}	Y17	MemData10
U18	PerClk	V18	IRQ10[GPIO10]	W18	MemData8	Y18	MemData13
U19	OV_{DD}	V19	PerBE1	W19	GND	Y19	MemAddr0
U20	PerPar3	V20	PerAddr29	W20	PerPar2	Y20	MemAddr2
U21	GND	V21	PerAddr31	W21	V_{DD}	Y21	HoldAck
U22	PerAddr26	V22	TCK	W22	PerBE2	Y22	TDO
U23	V_{DD}	V23	PerAddr30	W23	GND	Y23	HoldReq
U24	PerAddr27	V24	UART0_DCD	W24	PerBE3	Y24	TDI

Signals Listed by Ball Assignment (Part 6 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AA01	MemData48	AB01	No ball	AC01	No ball	AD01	No ball
AA02	GND	AB02	MemData50	AC02	No ball	AD02	No ball
AA03	MemData49	AB03	MemData52	AC03	ECC5	AD03	No ball
AA04	V_{DD}	AB04	ECC6	AC04	GND	AD04	ECC7
AA05	DQS8	AB05	$\overline{CAS}$	AC05	DM8	AD05	$\overline{BankSel3}$
AA06	GND	AB06	ECC1	AC06	SV_{DD}	AD06	ECC2
AA07	DM5	AB07	ECC0	AC07	MemData44	AD07	$\overline{RAS}$
AA08	SV_{DD}	AB08	MemData40	AC08	GND	AD08	MemData41
AA09	DM4	AB09	MemData45	AC09	DQS5	AD09	BA1
AA10	GND	AB10	ClkEn1	AC10	V_{DD}	AD10	MemData39
AA11	AGND	AB11	AMV_{DD} for MemClk PLL	AC11	DQS4	AD11	$\overline{BankSel2}$
AA12	V_{DD}	AB12	MemData29	AC12	GND	AD12	MemData33
AA13	GND	AB13	DQS3	AC13	SV_{DD}	AD13	MemData24
AA14	MemData16	AB14	DM2	AC14	DQS2	AD14	MemData25
AA15	SV_{DD}	AB15	$\overline{BankSel0}$	AC15	GND	AD15	MemData17
AA16	BA0	AB16	MemData11	AC16	DQS1	AD16	MemAddr5
AA17	GND	AB17	MemData15	AC17	V_{DD}	AD17	ClkEn0
AA18	DM1	AB18	MemAddr6	AC18	MemData12	AD18	MemAddr4
AA19	V_{DD}	AB19	MemData7	AC19	GND	AD19	MemData6
AA20	MemData3	AB20	MemAddr3	AC20	DQS0	AD20	MemAddr1
AA21	GND	AB21	MemData1	AC21	SV_{DD}	AD21	MemData0
AA22	$\overline{ExtAck}$	AB22	TMS	AC22	MemData2	AD22	No ball
AA23	OV_{DD}	AB23	$\overline{ExtReq}$	AC23	No ball	AD23	No ball
AA24	BusReq	AB24	No ball	AC24	No ball	AD24	No ball

Signal Description

The PPC440GP embedded controller is packaged in a 552-ball enhanced ceramic ball grid array (CBGA). The following tables describe the package level pinout.

Pin Summary

Group	No. of Pins
Signal pins, non-multiplexed	343
Signal pins, multiplexed	61
Total Signal Pins	**404**
AxV_{DD}	3
AGnd	3
OV_{DD}	27
SV_{DD}	9
V_{DD}	34
Gnd	70
Total Power Pins	**146**
Reserved	2
Total Pins	**552**

In the table “Signal Functional Description” on page 35, each I/O signal is listed along with a short description of its function. Some signals are multiplexed onto the same pin so that the pin can be used for different functions. In most cases, the signal name is shown in this table unaccompanied by multiplexed signal names that may be associated with it. Multiplexed signals are shown in square brackets following the default signal (for example, PCIXC0:7[$\overline{\text{BE0:3}}$]). Active-low signals such as $\overline{\text{BE0:3}}$ are marked with an overline.

It is expected that in any single application a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

In addition to multiplexing, some pins are also multi-purpose. For example, the EBC peripheral controller address pins (PerAddr0:31) are used as outputs by the PPC440GP to broadcast an address to external slave devices when the PPC440GP has control of the external bus. When during the course of normal chip operation an external master gains ownership of the external bus, these same pins are used as inputs which are driven by the external master and received by the EBC in the PPC440GP. In this example, the pins are also bidirectional, serving both as inputs and outputs.

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Strapping” on page 54). Note that these are *not multiplexed* pins since the function of the pins is not programmable.

The following table lists all of the I/O signals provided by the PPC440GP. Please refer to “Signals Listed Alphabetically” on page 14 for the pin number to which each signal is assigned. In cases where a multiplexed signal (indicated by the square brackets) is shown without the other signals that are assigned to that pin, you can see what the other signals are by referring to the same table.

Signal Functional Description (Part 1 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
PCI-X Interface				
PCIXAD0:63	Address/Data bus (bidirectional).	I/O	3.3V PCI	
PCIXC0:7[$\overline{\text{BE0:7}}$]	PCI-X Command[Byte Enables].	I/O	3.3V PCI	
PCIXClk	Provides timing to the PCI interface for PCI transactions.	I	3.3V PCI	
$\overline{\text{PCIXDevSel}}$	Indicates the driving device has decoded its address as the target of the current access.	I/O	3.3V PCI	
$\overline{\text{PCIXFrame}}$	Driven by the current master to indicate beginning and duration of an access.	I/O	3.3V PCI	
$\overline{\text{PCIXGnt0}}$	Indicates that the specified agent is granted access to the bus.	O	3.3V PCI	
$\overline{\text{PCIXGnt1}}$	Indicates that the specified agent is granted access to the bus.	I/O	3.3V PCI	
$\overline{\text{PCIXGnt2:5}}$	Indicates that the specified agent is granted access to the bus.	O	3.3V PCI	
PCIXIDSel	Used as a chip select during configuration read and write transactions.	I	3.3V PCI	
$\overline{\text{PCIXINT}}$	Level sensitive PCI interrupt.	O	3.3V PCI	
$\overline{\text{PCIXIRDY}}$	Indicates initiating agent's ability to complete the current data phase of the transaction.	I/O	3.3V PCI	
PCIXM66En	Capable of 66MHz operation.	I	5V tolerant 3.3V LVTTL	
PCIXParHigh	Even parity across PCIAD32:63 and PCIXC0:3[BE4:7].	I/O	3.3V PCI	
PCIXParLow	Even parity across PCIAD0:31 and PCIXC0:3[BE0:3].	I/O	3.3V PCI	
$\overline{\text{PCIXPErr}}$	Reports data parity errors during all PCI transactions except a Special Cycle.	I/O	3.3V PCI	
$\overline{\text{PCIXReq0:5}}$	An indication to the PCI-X arbiter that the specified agent wishes to use the bus.	I	3.3V PCI	
$\overline{\text{PCIXReq64}}$	Asserted by the current bus master, indicating a 64-bit transfer.	I/O	3.3V PCI	
$\overline{\text{PCIXAck64}}$	Indicates the target can transfer data using 64 bits.	I/O	3.3V PCI	
$\overline{\text{PCIXReset}}$	Brings PCI device registers and logic to a consistent state.	O	3.3V PCI	
$\overline{\text{PCIXSErr}}$	Reports address parity errors, data parity errors on the Special Cycle command, or other catastrophic system errors.	I/O	3.3V PCI	
$\overline{\text{PCIXStop}}$	Indicates the current target is requesting the master to stop the current transaction.	I/O	3.3V PCI	
$\overline{\text{PCIXTRDY}}$	Indicates the target agent's ability to complete the current data phase of the transaction.	I/O	3.3V PCI	

Signal Functional Description (Part 2 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
PCIXCap	Capable of PCI-X operation.	I	5V tolerant 3.3V LVTTL	5
PCIX133Cap	PCI-X devices are 133 MHz capable.	I	3.3V PCI	
DDR SDRAM Interface				
BA0:1	Bank Address supporting up to four internal banks.	O	2.5V SSTL_2	
$\overline{\text{BankSel0:3}}$	Selects up to four external DDR SDRAM banks.	O	2.5V SSTL_2	
$\overline{\text{CAS}}$	Column Address Strobe.	O	2.5V SSTL_2	
ClkEn0:3	Clock Enable. One for each bank.	O	2.5V SSTL_2	
DM0:8	Memory write data byte lane masks. MEMDM8 is the byte lane mask for the ECC byte lane.	O	2.5V SSTL_2	
DQS0:8	Byte lane data strobe. DQS8 is the data strobe for the ECC byte lane.	I/O	2.5V SSTL_2	
ECC0:7	ECC check bits 0:7.	I/O	2.5V SSTL_2	4
MemAddr0:12	Memory address bus.	O	2.5V SSTL_2	
MemClkOut0 $\overline{\text{MemClkOut0}}$	Subsystem clock.	O	2.5V SSTL_2	
MemData0:63	Memory data bus.	I/O	2.5V SSTL_2	4
MemVRef1 MemVRef2	Memory reference voltages (SV_{REF}).	I	Voltage Ref Receiver	
$\overline{\text{RAS}}$	Row Address Strobe.	O	2.5V SSTL_2	
$\overline{\text{WE}}$	Write Enable.	O	2.5V SSTL_2	
Ethernet Interface				
EMCCD[EMC1RxErr]	Collision Detection[Receive error] (MII[RMII 1]).	I/O	5V tolerant 3.3V LVTTL	
EMCCRS[EMC0CRSDV]	Carrier Sense[Receive data valid] (MII[RMII 0]).	I/O	5V tolerant 3.3V LVTTL	
EMCMDClk	Management Data Clock (MII and RMI 0 and 1).	O	5V tolerant 3.3V LVTTL	
EMCMDIO	Transfer command and status information between MII and PHY (MII and RMII 0 and 1).	I/O	5V tolerant 3.3V LVTTL	
EMCRxClk	Receive Clock (MII).	I	5V tolerant 3.3 V LVTTL	
EMCRxD0[EMC0RxD0][EMC0RxD] EMCRxD1[EMC0RxD1][EMC1RxD] EMCRxD2[EMC1RxD0] EMCRxD3[EMC1RxD1]	Received Data (MII[RMII 0 and 1][SMII 0 and 1]).	I/O	5V tolerant 3.3V LVTTL	
EMCRxDV[EMC1CRSDV]	Receive Data Valid (MII[RMII 1]).	I	5V tolerant 3.3V LVTTL	

Signal Functional Description (Part 3 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
EMCRxErr[EMC0RxErr]	Receive Error (MII[RMII 0]).	I	5V tolerant 3.3V LVTTL	
EMCTxClk[EMCRefClk]	Transmit Clock (MII[RMI 0 and 1, and SMII]).	I	5V tolerant 3.3V LVTTL	
EMCTxD0[EMC0TxD0][EMC0TxD] EMCTxD1[EMC0TxD1][EMC1TxD] EMCTxD2[EMC1TxD0] EMCTxD3[EMC1TxD1]	Transmitted Data (MII[RMII 0 and 1][SMII 0 and 1]).	O	5V tolerant 3.3V LVTTL	
EMCTxEn[EMC0TxEn][EMCSync]	Transmit data Enabled (MII[RMII 0][SMII]).	O	5V tolerant 3.3V LVTTL	
EMCTxErr[EMC1TxEn]	Transmit Error (MII) or Transmit data Enabled (RMII1).	O	5V tolerant 3.3V LVTTL	
External Slave Peripheral Interface				
DMAAck0:3	Used by the PPC440GP to indicate that data transfers have occurred.	O	5V tolerant 3.3V LVTTL	
DMAReq0:3	Used by slave peripherals to indicate they are prepared to transfer data.	I	5V tolerant 3.3V LVTTL	1, 5
EOT0:3/TC0:3	End Of Transfer/Terminal Count.	I/O	5V tolerant 3.3V LVTTL	1, 5
PerAddr0:31	Peripheral address bus used by PPC440GP when not in external master mode, otherwise used by external master. **Note:** PerAddr0 is the most significant bit (msb) on this bus.	I/O	5V tolerant 3.3V LVTTL	1
$\overline{\text{PerBE0:3}}$	External peripheral data bus byte enables.	I/O	5V tolerant 3.3V LVTTL	1, 2
$\overline{\text{PerBLast}}$	Used by either the peripheral controller, DMA controller, or external master to indicates the last transfer of a memory access.	I/O	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{PerCS0:7}}$	External peripheral device select.	O	5V tolerant 3.3V LVTTL	2
PerData0:31	Peripheral data bus used by PPC440GP when not in external master mode, otherwise used by external master. **Note:** PerData0 is the most significant bit (msb) on this bus.	I/O	5V tolerant 3.3V LVTTL	1
$\overline{\text{PerOE}}$	Used by either peripheral controller or DMA controller depending upon the type of transfer involved. When the PPC440GP is the bus master, it enables the selected DDR SDRAMs to drive the bus.	O	5V tolerant 3.3V LVTTL	2
PerPar0:3	External peripheral data bus byte parity.	I/O	5V tolerant 3.3V LVTTL	1

Signal Functional Description (Part 4 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
PerReady[RcvrInh]	Used by a peripheral slave to indicate it is ready to transfer data.	I	5V tolerant 3.3V LVTTL	
PerR/$\overline{W}$	Used by the PPC440GP when not in external master mode, as output by either the peripheral controller or DMA controller depending upon the type of transfer involved. High indicates a read from memory, low indicates a write to memory. Otherwise, it used by the external master as an input to indicate the direction of transfer.	I/O	5V tolerant 3.3V LVTTL	1, 2
$\overline{\text{PerWE}}$	Write Enable. Low when any of the four $\overline{\text{PerBE0:3}}$ signals are low.	O	5V tolerant 3.3V LVTTL	2
External Master Peripheral Interface				
BusReq	Bus Request. Used when the PPC440GP needs to regain control of peripheral interface from an external master.	O	5V tolerant 3.3V LVTTL	
$\overline{\text{ExtAck}}$	External Acknowledgement. Used by the PPC440GP to indicate that a data transfer occurred.	O	5V tolerant 3.3V LVTTL	
$\overline{\text{ExtReq}}$	External Request. Used by an external master to indicate it is prepared to transfer data.	I	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{ExtReset}}$	Peripheral Reset. Used by an external master and by synchronous peripheral slaves.	O	5V tolerant 3.3V LVTTL	
HoldAck	Hold Acknowledge. Used by the PPC440GP to transfer ownership of peripheral bus to an external master.	O	5V tolerant 3.3V LVTTL	
HoldReq	Hold Request. Used by an external master to request ownership of the peripheral bus.	I	5V tolerant 3.3V LVTTL	1, 5
PerClk	Peripheral Clock. Used by an external master and by synchronous peripheral slaves.	O	5V tolerant 3.3V LVTTL	
PerErr	External Error. Used as an input used to record external master errors and external slave peripheral errors.	I/O	5V tolerant 3.3V LVTTL	1, 5
UART Peripheral Interface				
UARTSerClk	Serial Clock used to provide an alternative clock to the internally generated serial clock. Used in cases where the allowable internally generated baud rates are not satisfactory. This input can be individually connected to either or both UART0 and UART1.	I	5V tolerant 3.3V LVTTL	1, 4
UART0_Rx	UART0 Receive data.	I	5V tolerant 3.3V LVTTL	1, 4
UART0_Tx	UART0 Transmit data.	O	5V tolerant 3.3V LVTTL	4
$\overline{\text{UART0\_DCD}}$	UART0 Data Carrier Detect.	I	5V tolerant 3.3V LVTTL	6
$\overline{\text{UART0\_DSR}}$	UART0 Data Set Ready.	I	5V tolerant 3.3V LVTTL	6

Signal Functional Description (Part 5 of 7)

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
$\overline{\text{UART0\_CTS}}$	UART0 Clear To Send.	I	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{UART0\_DTR}}$	UART0 Data Terminal Ready.	O	5V tolerant 3.3V LVTTL	4
$\overline{\text{UART0\_RTS}}$	UART0 Request To Send.	O	5V tolerant 3.3V LVTTL	4
$\overline{\text{UART0\_RI}}$	UART0 Ring Indicator.	I	5V tolerant 3.3V LVTTL	1, 4
UART1_Rx	UART1 Receive data.	I/O	5V tolerant 3.3V LVTTL	1, 4
UART1_Tx	UART1 Transmit data.	I/O	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{UART1\_DSR}}$/$\overline{\text{CTS}}$	UART1 Data Set Ready or Clear To Send. The choice is determined by a DCR register bit setting.	I/O	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{UART1\_RTS/DTR}}$	UART1 Request To Send or Data Terminal Ready. The choice is determined by a DCR register bit setting.	I/O	5V tolerant 3.3V LVTTL	1, 4
IIC Peripheral Interface				
IIC0SClk	IIC0 Serial Clock.	I/O	5V tolerant 3.3V LVTTL	1, 2
IIC0SDA	IIC0 Serial Data.	I/O	5V tolerant 3.3V LVTTL	1, 2
IIC1SClk	IIC1 Serial Clock.	I/O	5V tolerant 3.3V LVTTL	1, 2
IIC1SDA	IIC1 Serial Data.	I/O	5V tolerant 3.3V LVTTL	1, 2
Interrupts Interface				
IRQ0:10	Interrupt Requests 0 through 10.	I	5V tolerant 3.3V LVTTL	1, 5
[IRQ11]	Interrupt Request 11.	I	5V tolerant 3.3V LVTTL	1, 5
[IRQ12]	Interrupt Request 12.	I	5V tolerant 3.3V LVTTL	1, 5

Signal Functional Description (Part 6 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
JTAG Interface				
TCK	Test Clock.	I	3.3V CMOS w/pull-up	1
TDI	Test Data In.	I	3.3V CMOS w/pull-up	4
TDO	Test Data Out.	O	3.3V LVTTL	
TMS	Test Mode Select.	I	3.3V CMOS w/pull-up	1
$\overline{\text{TRST}}$	Test Reset.	I	3.3V CMOS w/pull-up	5
System Interface				
$\overline{\text{ExtReset}}$	External reset	O	5V tolerant 3.3V LVTTL	
SysClk	Main system clock input.	Clock	5V tolerant 3.3V LVTTL	
SysErr	Set to 1 when a machine check is generated.	O	5V tolerant 3.3V LVTTL	
$\overline{\text{SysReset}}$	Main system reset.	I/O	5V tolerant 3.3V LVTTL	1, 2
TmrClk	Processor timer external input clock.	I	5V tolerant 3.3V LVTTL	
$\overline{\text{Halt}}$	Halt from external debugger.	I	5V tolerant 3.3V LVTTL	1, 4
[GPIO0:10]	General purpose I/O 0 through 10. To access these functions, software must toggle DCR register bits.	I/O	5V tolerant 3.3V LVTTL	
GPIO11	General purpose I/O 11. To access this function, software must toggle a DCR register bit.	I/O	5V tolerant 3.3V LVTTL	
[GPIO12:31]	General purpose I/O 12 through 31. To access these functions, software must toggle a DCR register bit.	I/O	5V tolerant 3.3V LVTTL	
TestEn	Test Enable.	I	1.8V CMOS w/pull-down	3
[RcvrInh]	Receiver Inhibit. Active only when TestEn is active.	I	5V tolerant 3.3V LVTTL	
RefVEn	Reference Voltage Enable. Used for wafer testing. Do not connect for normal operation.	I	1.8V CMOS w/pull-down	
DrvrInh1:2	Driver Inhibit. Used for test purposes only. Tie up for normal operation	I	5V tolerant 3.3V LVTTL	2

Signal Functional Description (Part 7 of 7)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
Trace Interface				
TrcBS0:2	Branch execution status.	I/O	5V tolerant 3.3V LVTTL	
TrcClk	Trace data capture clock, runs at 1/4 the frequency of the processor.	O	5V tolerant 3.3V LVTTL	
TrcES0:4	Trace Execution Status is presented every fourth processor clock cycle.	I/O	5V tolerant 3.3V LVTTL	
TrcTS0:6	Additional information on trace execution and branch status.	I/O	5V tolerant 3.3V LVTTL	
Power Pins				
AGND	PLL (analog) voltage ground.	n/a	n/a	
GND	Ground.	n/a	n/a	
AxV_{DD}	Filtered voltages input for PLLs (analog circuits) **Note:** A separate filter for each of the three voltages is recommended.	n/a	n/a	
OV_{DD}	I/O (except DDR SDRAM) voltage—3.3V.	n/a	n/a	
SV_{DD}	DDR SDRAM voltage—2.5V.	n/a	n/a	
V_{DD}	Logic voltage—1.8V.	n/a	n/a	
Reserved Pins				
Reserved	Do not connect signals, voltage, or ground to these balls.	n/a	n/a	

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device

Characteristic	Symbol	Value	Unit	Notes
Supply Voltage (Internal Logic)	V_{DD}	0 to +1.95	V	1
Supply Voltage (I/O Interface, except DDR SDRAM)	OV_{DD}	0 to +3.6	V	1
PLL Supply Voltages	AxV_{DD}	0 to +1.95	V	
Supply Voltage (DDR SDRAM Logic)	SV_{DD}	0 to +2.7	V	
Input Voltage (3.3V LVTTL receivers)	V_{IN}	0 to +3.6	V	
Input Voltage (5.0V LVTTL receivers)	V_{IN}	0 to +5.5	V	
Storage Temperature Range	T_{STG}	-55 to +150	°C	
Case temperature under bias	T_C	-40 to +120	°C	

Note:

1. If $OV_{DD} \leq 0.4$V it is required that $V_{DD} \leq 0.4$V. Supply excursions not meeting this criteria must be limited to less than 25ms duration during each power up or power down event.

Package Thermal Specifications

The PPC440GP is designed to operate within a case temperature range of -40°C to 120°C. Thermal resistance values for the CBGA package in a convection environment are as follows:

Parameter	Symbol	Airflow ft/min (m/sec)			Unit
		0 (0)	100 (0.51)	200 (1.02)	
Junction-to-case thermal resistance	θ_{JC}	<0.1	<0.1	<0.1	°C/W
Case-to-ambient thermal resistance (without heat sink)	θ_{CA}	18.9	17.7	16.3	°C/W

Notes:

1. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.
2. $T_A = T_C - P \times \theta_{CA}$, where T_A is ambient temperature and P is power consumption.
3. $T_{CMax} = T_{JMax} - P \times \theta_{JC}$, where T_{JMax} is maximum junction temperature and P is power consumption.
4. The above assumes that the chip is mounted on a card with at least one signal and two power planes.

Recommended DC Operating Conditions

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage	V_{DD}	1.7	1.8	1.9	V	2
I/O Supply Voltage	OV_{DD}	3.0	3.3	3.6	V	2
DDR SDRAM Supply Voltage	SV_{DD}	2.3	2.5	2.7	V	2
PLL Supply Voltages	AxV_{DD}	1.65	1.8	1.95	V	4
DDR SDRAM Reference Voltage	SV_{REF}	1.15	1.25	1.35	V	3
Input Logic High (2.5V SSTL receiver)	V_{IH}	SV_{REF} + 0.18		SV_{DD} + 0.3	V	
Input Logic High (3.3V PCI-X receiver)		$0.5OV_{DD}$		OV_{DD} + 0.5	V	1
Input Logic High (3.3V LVTTL, 5V tolerant receiver)		2.0		5.5	V	
Input Logic Low (2.5V SSTL receiver)	V_{IL}	– 0.3		SV_{REF} – 0.18	V	
Input Logic Low (3.3V PCI-X receiver)		– 0.5		$0.35OV_{DD}$		1
Input Logic Low (3.3V LVTTL, 5V tolerant receiver)		0		0.8		
Output Logic High (2.5V SSTL receiver)	V_{OH}	1.95		SV_{DD}	V	
Output Logic High (3.3V PCI-X receiver)		$0.9OV_{DD}$		OV_{DD}	V	1
Output Logic High (3.3V LVTTL, 5V tolerant receiver)		2.4		OV_{DD}	V	
Output Logic Low (2.5V SSTL receiver)	V_{OL}	0		0.55		
Output Logic Low (3.3V PCI-X receiver)		– 0.5		$0.35OV_{DD}$		1
Output Logic Low (3.3V LVTTL, 5V tolerant receiver)		0		0.4	V	
Input Leakage Current (No pull-up or pull-down)	I_{IL1}	0		0	µA	
Input Leakage Current for Pull-Down	I_{IL2}	0 (LPDL)		200 (MPUL)	µA	
Input Leakage Current for Pull-Up	I_{IL3}	–150 (LPDL)		0 (MPUL)	µA	
Input Max Allowable Overshoot (3.3V LVTTL, 5V tolerant receiver)	V_{IMAO}			5.5	V	
Input Max Allowable Undershoot (3.3V LVTTL, 5V tolerant receiver)	V_{IMAU}	– 0.6			V	
Output Max Allowable Overshoot (3.3V LVTTL, 5V tolerant receiver)	V_{OMAO}			5.5	V	
Output Max Allowable Undershoot (3.3V LVTTL, 5V tolerant receiver)	V_{OMAU3}	– 0.6			V	
Case Temperature	T_C	– 40		85	°C	

Notes:

1. PCI-X drivers meet PCI-X specifications.
2. Power supply sequencing is required.
3. $SV_{REF} = SV_{DD}/2$
4. The analog voltage used for the on-chip PLLs can be derived from the logic voltage, but must be filtered before entering the PPC440GP. A separate filter for each voltage is recommended.

Input Capacitance

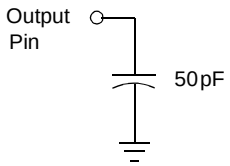
Parameter	Symbol	Maximum	Unit	Notes
Group 1 (2.5V SSTL I/O)	C_{IN1}	12	pF	
Group 2 (5V tolerant LVTTL I/O)	C_{IN2}	12	pF	
Group 3 (PCI I/O)	C_{IN3}	12	pF	
Group 4 (Rx only pins)	C_{IN4}	9	pF	

DC Power Supply Loads

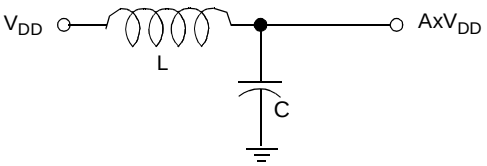
Parameter	Symbol	Minimum	Typical	Maximum	Unit
V_{DD} (1.8V) active operating current	I_{DD}		915		mA
OV_{DD} (3.3V) active operating current	I_{ODD}		125		mA
SV_{DD} (2.5V) active operating current	I_{SDD}		560		mA
AxV_{DD} (1.8V) input current	I_{ADD}		33		mA

Test Conditions

Clock timing and switching characteristics are specified in accordance with operating conditions shown in the table “Recommended DC Operating Conditions.” AC specifications are characterized with V_{DD} = 1.8V, T_J = 100 °C and a 50pF test load as shown in the figure to the right.



Each of the analog voltages for the internal PLL circuits are individually filtered using the following circuit:



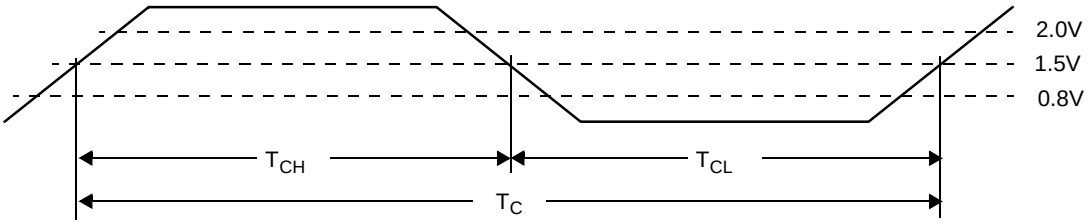
L – SMT chip ferrite bead for:
APV_{DD} (PCI) – Murata BLM31A700S
ASV_{DD} (SysClk) – Murata BLM31A700S
AMV_{DD} (MemClkOut) – Murata BLM32A06

C – 0.1µF ceramic

Clocking Specifications

Symbol	Parameter	Min	Max	Units
SysClk Input				
F_C	SysClk clock input frequency	33.33	66.66	MHz
T_C	SysClk clock period	15	30	ns
T_{CS}	Clock edge stability	–	0.15	ns
T_{CH}	Clock input high time	40% of nominal period	60% of nominal period	ns
T_{CL}	Clock input low time	40% of nominal period	60% of nominal period	ns
Note: Input slew rate ≥ 1 V/ns				
MemClkOut				
F_C	Frequency	100	133.33	MHz
T_C	Period	7.5	10	ns
T_{CH}	Output high time	35% of nominal period	65% of nominal period	ns
PLL VCO				
F_C	Frequency	500	1000	MHz
T_C	Period	2	1	ns

Timing Waveform



Spread Spectrum Clocking

Care must be taken when using a spread spectrum clock generator (SSCG) with the PPC440GP. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is referred to as tracking skew. The PLL bandwidth and phase angle determine how much tracking skew there is between the SSCG and the PLL for a given frequency deviation and modulation frequency. When using an SSCG with the PPC440GP the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the PPC440GP with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation cannot exceed –3%, and the modulation frequency cannot exceed 40 kHz. In some cases, on-board PPC440GP peripherals impose more stringent requirements.
- Use the Peripheral Bus Clock for logic that is synchronous to the peripheral bus since this clock tracks the modulation.
- Use the DDR SDRAM MemClkOut since it also tracks the modulation.

Notes:

1. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur. The 1.5% tolerance assumes that the connected device is running at precise baud rates.
2. Ethernet operation in unaffected.
3. IIC operation is unaffected.

Caution: It is up to the system designer to ensure that any SSCG used with the PPC440GP meets the above requirements and does not adversely affect other aspects of the system.

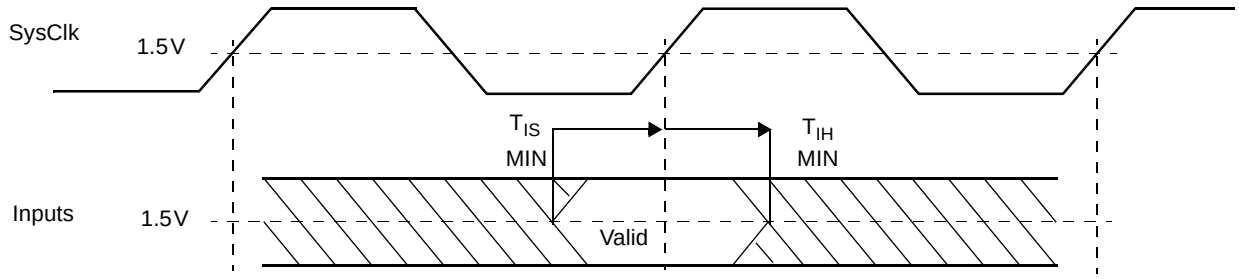
Peripheral Interface Clock Timings

Parameter	Min	Max	Units	Notes
PCIXClk input frequency (asynchronous mode)[2]	–	133.33	MHz	
PCIXClk period (asynchronous mode)	7.5	–	ns	
PCIXClk input high time	40% of nominal period	60% of nominal period	ns	
PCIXClk input low time	40% of nominal period	60% of nominal period	ns	
EMCMDClk output frequency	–	2.5	MHz	
EMCMDClk period	400	–	ns	
EMCMDClk output high time	160	–	ns	
EMCMDClk output low time	160	–	ns	
EMCTxClk input frequency MII(RMII)	2.5(5)	25(50)	MHz	
EMCTxClk period MII(RMII)	40(20)	400(200)	ns	
EMCTxClk input high time	35% of nominal period	–	ns	
EMCTxClk input low time	35% of nominal period	–	ns	
EMCRxClk input frequency MII(RMII)	2.5(5)	25(50)	MHz	
EMCRxClk period MII(RMII)	40(20)	400(200)	ns	
EMCRxClk input high time	35% of nominal period	–	ns	
EMCRxClk input low time	35% of nominal period	–	ns	
PerClk output frequency (for ext. master or sync. slaves)	–	66.66	MHz	
PerClk period	15	–	ns	
PerClk output high time	50% of nominal period	66% of nominal period	ns	
PerClk output low time	33% of nominal period	50% of nominal period	ns	
UARTSerClk input frequency)	–	$1000/(2T_{OPB}$[1]$+2ns)$	MHz	1
UARTSerClk period	$2T_{OPB}+2$	–	ns	1
UARTSerClk input high time	$T_{OPB}+1$	–	ns	1
UARTSerClk input low time	$T_{OPB}+1$	–	ns	1
TmrClk input frequency	–	100	MHz	
TmrClk period	10	–	ns	
TmrClk input high time	40% of nominal period	60% of nominal period	ns	
TmrClk input low time	40% of nominal period	60% of nominal period	ns	

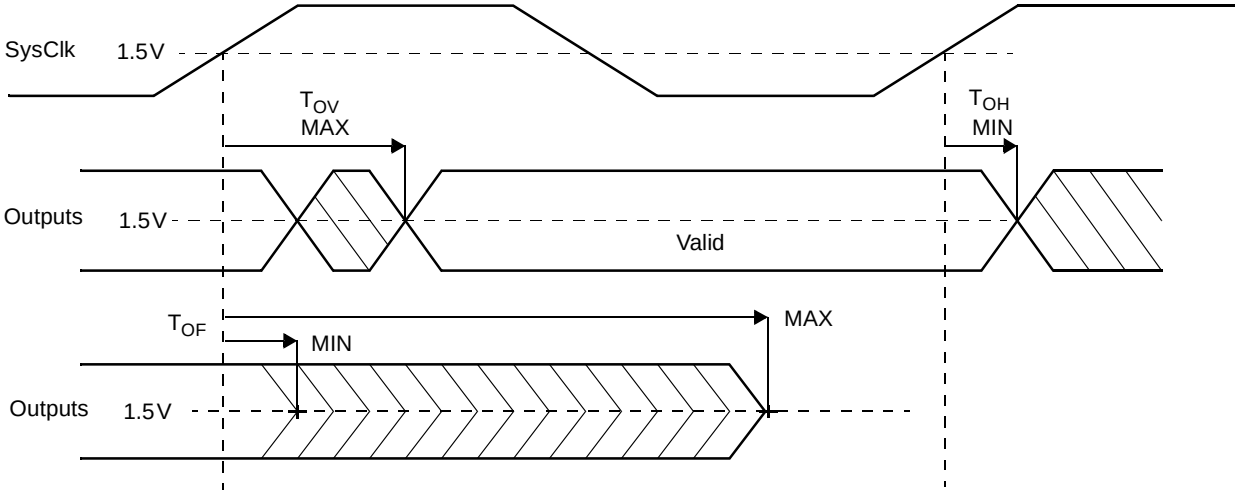
Notes:

1. T_{OPB} is the period in ns of the OPB clock. The internal OPB clock runs at 1/2 the frequency of the PLB clock. The maximum OPB clock frequency is 66.66 MHz.
2. When the PCI-X interface is used to support a legacy PCI interface, the maximum PCIXClk is 66.66MHz.

Input Setup and Hold Waveform



Output Delay and Float Timing Waveform



I/O Specifications—400MHz (Part 1 of 3)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 1.3ns.
3. PCI-X timings are for asynchronous operation up to 133MHz. PCI-X input setup time requirement is 1.2ns for 133MHz and 1.7ns for 66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
PCI-X Interface								
PCIXAD31:0	Note 3 (3)	0.5 (0)	3.8 (6)	0.7 (Note 3)	0.5	1.5	PCIXClk	3
PCIXC3:0[$\overline{\text{BE3:0}}$]	Note 3 (3)	0.5 (0)	3.8 (6)	0.7 (Note 3)	0.5	1.5	PCIXClk	3
PCIXParLow	Note 3 (3)	0.5 (0)	3.8 (6)	0.7 (Note 3)	0.5	1.5	PCIXClk	3
PCIParHigh	Note 3 (3)	0.5 (0)	3.8 (6)	0.7 (Note 3)	0.5	1.5	PCIXClk	
$\overline{\text{PCIXFrame}}$	Note 3 (3)	0.5 (0)	3.8 (6)	0.7 (Note 3)	0.5	1.5	PCIXClk	3
$\overline{\text{PCIXINT}}$	n/a	n/a	dc	dc	0.5	1.5	PCIXClk	async
$\overline{\text{PCIXIRDY}}$	Note 3 (3)	0.5 (0)	3.8 (6)	0.7 (Note 3)	0.5	1.5	PCIXClk	3
$\overline{\text{PCIXTRDY}}$	Note 3 (3)	0.5 (0)	3.8 (6)	0.7 (Note 3)	0.5	1.5	PCIXClk	3
$\overline{\text{PCIXStop}}$	Note 3 (3)	0.5 (0)	3.8 (6)	0.7 (Note 3)	0.5	1.5	PCIXClk	3
$\overline{\text{PCIXDevSel}}$	Note 3 (3)	0.5 (0)	3.8 (6)	0.7 (Note 3)	0.5	1.5	PCIXClk	3
PCIXIDSel	Note 3 (3)	0.5 (0)	n/a	n/a	n/a	n/a	PCIXClk	3
$\overline{\text{PCIXPErr}}$	Note 3 (3)	0.5 (0)	3.8 (6)	0.7 (Note 3)	0.5	1.5	PCIXClk	3
$\overline{\text{PCIXSErr}}$	Note 35 (3)	0.5 (0)	3.8 (6)	0.7 (Note 3)	0.5	1.5	PCIXClk	3
PCIXClk	dc	dc	n/a	n/a	n/a	n/a		async
$\overline{\text{PCIXReset}}$	n/a	n/a	n/a	n/a	n/a	n/a	PCIXClk	
$\overline{\text{PCIXReq64}}$	Note 3 (3)	0.5 (0)	3.8 (6)	0.7 (Note 3)	0.5	1.5	PCIXClk	3
$\overline{\text{PCIXAck64}}$	Note 3 (3)	0.5 (0)	3.8 (6)	0.7 (Note 3)	0.5	1.5	PCIXClk	3
PCIXCap	Note 3 (3)	0.5 (0)	n/a	n/a	n/a	n/a	PCIXClk	3
PCIX133Cap	Note 3 (3)	0.5 (0)	n/a	n/a	n/a	n/a	PCIXClk	3
PCIXM66En	Note 3 (3)	0.5 (0)	n/a	n/a	n/a	n/a	PCIXClk	3
$\overline{\text{PCIXReq0:5}}$	Note 3 (5)	0.5 (0)	n/a	n/a	n/a	n/a	PCIXClk	3
$\overline{\text{PCIXGnt0:5}}$	n/a)	n/a	3.8 (6)	0.7 (Note 3)	0.5	1.5	PCIXClk	3
Ethernet MII Interface								
EMCRxD0:3	4	1	n/a	n/a	n/a	n/a	EMCRxClk	1
EMCRxDV	4	1	n/a	n/a	n/a	n/a	EMCRxClk	1
EMCRxClk	n/a	n/a	n/a	n/a	n/a	n/a		1, async
EMCRxErr	4	1	n/a	n/a	n/a	n/a	EMCRxClk	1
EMCTxD3:0	n/a	n/a	15	2	10.3	7.1	EMCTxClk	1
EMCTxEn	n/a	n/a	15	2	10.3	7.1	EMCTxClk	1
EMCTxClk	n/a	n/a	n/a	n/a	n/a	n/a		1, async
EMCTxErr	n/a	n/a	15	2	10.3	7.1	EMCTxClk	1
EMCCRS			n/a	n/a	n/a	n/a		1, async
EMCCD			n/a	n/a	n/a	n/a		1, async
EMCMDIO					10.3	7.1	EMCMDClk	1
EMCMDClk	n/a	n/a	n/a	n/a	n/a	n/a		1, async
Dual Ethernet RMII Interface								
EMC0RxD0:1	2	1	n/a	n/a	n/a	n/a	EMCRxClk	
EMC0RxErr	2	1	n/a	n/a	n/a	n/a	EMCRxClk	
EMC0CRSDV			n/a	n/a	n/a	n/a	EMCRxClk	
ENET0RxDV	2	1	n/a	n/a	10.3	7.1	EMCRxClk	

I/O Specifications—400MHz (Part 2 of 3)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 1.3ns.
3. PCI-X timings are for asynchronous operation up to 133MHz. PCI-X input setup time requirement is 1.2ns for 133MHz and 1.7ns for 66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
EMC0TxD0:1	n/a	n/a	15	2	10.3	7.1	EMCTxClk	
ENET0TxEn	n/a	n/a	15	2	10.3	7.1	EMCTxClk	
EMC1RxD0:1			n/a	n/a	10.3	7.1	EMCRxClk	
EMC1RxErr			n/a	n/a	n/a	n/a	EMCRxClk	
EMC1CRSDV			n/a	n/a	n/a	n/a	EMCRxClk	
EMC1TxD0:1	n/a	n/a	15	2	10.3	7.1	EMCTxClk	
EMC1TxEn	n/a	n/a	15	2	10.3	7.1	EMCTxClk	
EMCRefClk	n/a	n/a	n/a	n/a	10.3	7.1		async
EMCMDIO					10.3	7.1	EMCTxClk	
EMCMDClk			n/a	n/a	10.3	7.1		async
Internal Peripheral Interface								
IICxSClk	n/a	n/a	n/a	n/a	15.3	10.2		
IICxSDA					15.3	10.2		
UARTSerClk	n/a	n/a	n/a	n/a	n/a	n/a		
UART0_Rx			n/a	n/a	n/a	n/a		
UART0_Tx	n/a	n/a			10.3	7.1		
$\overline{\text{UART0\_DCD}}$			n/a	n/a	n/a	n/a		
$\overline{\text{UART0\_DSR}}$			n/a	n/a	n/a	n/a		
$\overline{\text{UART0\_CTS}}$			n/a	n/a	n/a	n/a		
$\overline{\text{UART0\_DTR}}$	n/a	n/a			10.3	7.1		
$\overline{\text{UART0\_RI}}$			n/a	n/a	n/a	n/a		
$\overline{\text{UART0\_RTS}}$	n/a	n/a			10.3	7.1		
UART1_Rx			n/a	n/a	n/a	n/a		
UART1_Tx	n/a	n/a			10.3	7.1		
$\overline{\text{UART1\_DSR/CTS}}$			n/a	n/a	n/a	n/a		
$\overline{\text{UART1\_RTS/DTR}}$	n/a	n/a			10.3	7.1		
Interrupts Interface								
IRQ0:12					n/a	n/a		
JTAG Interface								
TDI					n/a	n/a		async
TMS					n/a	n/a		async
TDO					15.3	10.2		async
TCK					n/a	n/a		async
$\overline{\text{TRST}}$					n/a	n/a		async

I/O Specifications—400MHz (Part 3 of 3)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 1.3ns.
3. PCI-X timings are for asynchronous operation up to 133MHz. PCI-X input setup time requirement is 1.2ns for 133MHz and 1.7ns for 66MHz. PCI timings (in parentheses) are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I/O H (minimum)	I/O L (minimum)		
System Interface								
SysClk			n/a	n/a	n/a	n/a		
TmrClk			n/a	n/a	n/a	n/a		async
$\overline{\text{SysReset}}$					n/a	n/a		async
$\overline{\text{Halt}}$			n/a	n/a	n/a	n/a		async
SysErr	n/a	n/a			10.3	7.1		async
$\overline{\text{TestEn}}$			n/a	n/a	n/a	n/a		async
DrvrInh1:2			n/a	n/a	n/a	n/a		
GPIO0:31					10.3	7.1		
Trace Interface								
TrcClk	n/a	n/a			10.3	7.1		
External Slave Peripheral Interface								
PerData0:31	3	1	9	0	15.3	10.2	PerClk	
PerAddr0:31	3	1	7.6	0	15.3	10.2	PerClk	
PerPar0:3	4	1	8.4	0	15.3	10.2	PerClk	
$\overline{\text{PerBE0:3}}$	2.5	1	6.5	0	15.3	10.2	PerClk	
$\overline{\text{PerCS0:7}}$	n/a	n/a	6	0	15.3	10.2	PerClk	
$\overline{\text{PerOE}}$	n/a	n/a	6	0	15.3	10.2	PerClk	
$\overline{\text{PerWE}}$	n/a	n/a	7	0	15.3	10.2		
$\overline{\text{PerBLast}}$	2.5	1	5	n/a	15.3	10.2	PerClk	
PerReady[RcvrInh]	5	1	n/a	n/a	n/a	n/a	PerClk	
PerR/$\overline{\text{W}}$	2.5	1	5.6	n/a	15.3	10.2	PerClk	
DMAReq0:3	dc	dc	n/a	n/a	n/a	n/a	PerClk	
DMAAck0:3	n/a	n/a	7	0	15.3	10.2	PerClk	
EOT0:3/TC0:3	dc	dc	6.8	0	15.3	10.2	PerClk	
External Master Peripheral Interface								
PerClk	n/a	n/a	n/a	n/a	15.3	10.2	PLB Clk	2
$\overline{\text{ExtReset}}$	n/a	n/a	6.2	0	15.3	10.2	PerClk	
HoldReq	3.5	1	n/a	n/a	n/a	n/a	PerClk	
HoldAck	n/a	n/a	6.4	0	15.3	10.2	PerClk	
$\overline{\text{ExtReq}}$	2.5	1	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{ExtAck}}$	n/a	n/a	6.2	0	15.3	10.2	PerClk	
BusReq	n/a	n/a	6.2	0	15.3	10.2	PerClk	
PerErr	4.5	1	n/a	n/a	15.3	10.2	PerClk	

DDR SDRAM I/O Timing

The DDR SDRAM controller times its operation with internal PLB and 2xPLB clock signals and generates MemClkOut from the PLB clock. MemClkOut is the same frequency as the PLB clock signal. The alignment of MemClkOut with the PLB clock signal is delayed a maximum of 3ns by driver circuits.

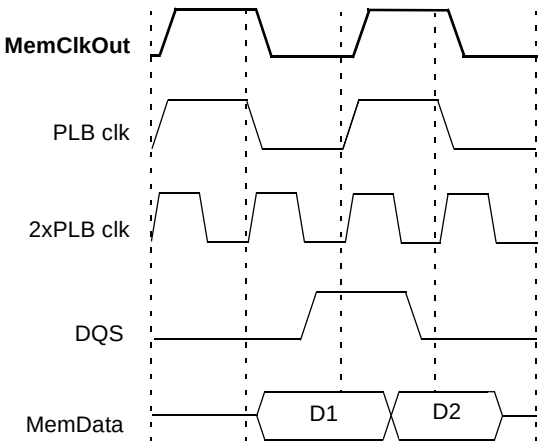
Note: MemClkOut may be advanced or delayed with respect to the PLB clock by means of the SDRAM0_CFGn programming registers. Users might need to advance MemClkOut for their applications. This depends on the specific application and requires a thorough understanding of the memory system in general (refer to the DDR SDRAM controller chapter in the *PowerPC 440GP User's Manual*).

I/O Specifications—DDR SDRAM Write Delay

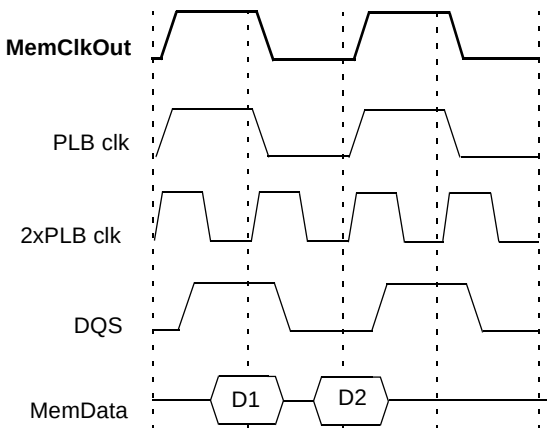
Notes:
1. 3.225 + 1/4 T_{CYC} where T_{CYC} = 7.5ns for a 133MHz clock.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
DDR SDRAM								
ECC0:7 MemData0:63 DM0:8			3				2xPLB	
MemClkOut0			2.6				PLB	
MemAddr0:12 BA0:1 $\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$ $\overline{BankSel0:3}$ ClkEn0:3			3.8				PLB	
DQS0:8			5.1				2xPLB	1

DDR SDRAM Write Cycle Timing



DDR SDRAM Read Cycle Timing



For DDR SDRAM read operations, MemData must be valid by no later than 1/4 T_{CYC} - 0.5ns (1.375ns at 133MHz) from the rising edge of DQS, and must be held valid until 1/4T_{CYC} + 0.4ns (2.275ns at 133 MHz) from the rising DQS at the chip pins. Data D2 must have the same relationship to falling DQS. In addition, there is a setup time with respect to the PLB clock of 2.375ns, unless the read data clock has been delayed by programming the SDRAM0_CFGn register.

Initialization

The PPC440GP provides the option for setting initial parameters based on a set of default values or reading the initial parameters from a slave ROM attached to the IIC0 bus.

Strapping

While the $\overline{\text{SysReset}}$ input pin is low (system reset), the state of certain I/O pins is read to enable default initial conditions prior to PPC440GP start-up. The actual capture instant is the nearest reference clock edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. These pins are used for strap functions only during reset. Following reset they are used for normal functions. At the de-assertion of reset, if the bootstrap controller is enabled, it sequentially reads 16 bytes from the external IIC slave and uses the first 8 bytes to set the SYS0 and SYS1 registers accordingly. Otherwise, the default values set in the STRP0 and STRP1 are used for initialization.

The following table lists the strapping pins along with their functions and strapping options:

Strapping Pin Assignments

Function	Option	Ball Strapping
IIC0 slave address that will respond with boot data		**V02** ($\overline{\text{UART0\_DSR}}$)
	0x54	0
	0x50	1
Bootstrap controller		**V24** ($\overline{\text{UART0\_DCD}}$)
	Disabled	0
	Enabled	1

EEPROM

During reset, initial conditions other than those obtained from the strapping pins can be read from a ROM device connected to the IIC0 port. The association of bits in the external ROM with the initialization settings and their default values are covered in detail in the *PowerPC 440GP User's Manual*.

Inside of back cover

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Preliminary Edition (3/4/02)
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