AN 876: JESD204C Intel® FPGA IP and ADI AD9081 MxFE* ADC Interoperability Report for Intel® Agilex® F-Tile Devices

Contents

1. JESD204C Intel® FPGA IP and ADI AD9081 MxFE* ADC Interoperability Report for Intel® Agilex™ F-tile Devices

The JESD204C Intel® FPGA IP is a high-speed point-to-point serial interface intellectual property (IP).

The JESD204C Intel FPGA IP has been hardware-tested with several selected JESD204C compliant analog-to-digital converter (ADC) devices.

This report highlights the interoperability of the JESD204C Intel FPGA IP with the AD9081 Mixed Signal Front End (MxFE*) evaluation module (EVM) from Analog Devices Inc. (ADI). The following sections describe the hardware checkout methodology and test results.

Related Information

F-tile JESD204C Intel FPGA IP User Guide

1.1. Hardware and Software Requirements

The interoperability test requires the following hardware and software tools:

Hardware

- Intel Agilex™ I-Series F-tile Demo Board (AGIB027R29A1E2VR0) with 12V power adapter
- Analog Devices (ADI) AD9081 MxFE* EVM (AD9081-FMCA-EBZ, Rev C)
- Skywork Si5345-D Evaluation Board (Si5345-D-EVB)
- SMA male to SMP male
- SMP male to SMP cable

Software

- Intel Quartus® Prime Pro Edition software version 21.4
- AD9081_API version 1.1.0 or newer (Linux application, required for AD9081 EVM configuration)

Related Information

- AD9081/AD9082 System Development User Guide
- Skyworks Si5345-D Evaluation Board User Guide

1.2. Hardware Setup

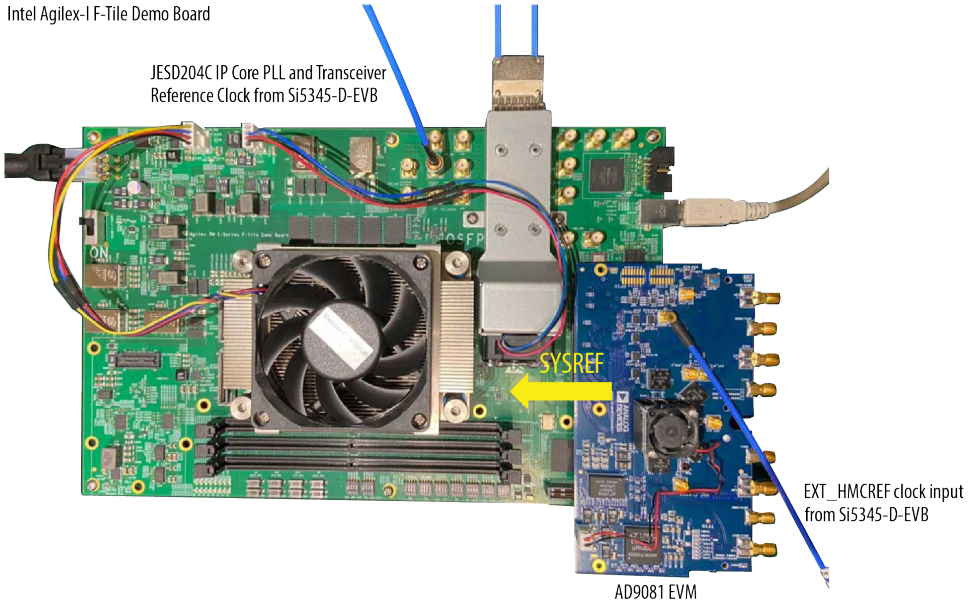
The JESD204C Intel FPGA IP is instantiated in Duplex mode but only the receiver path is used. For FCLK_MULP =1, WIDTH_MULP = 8, S = 1, the core PLL generates a 375 MHz link clock and a 375 MHz frame clock.

An Intel Agilex I-Series F-Tile Demo Board is used with the ADI AD9081-FMCA-EBZ EVM connected to the FMC+ connector of the development board. The hardware setup for the ADC interoperability test is shown in the *Hardware Setup* figure.

- The AD9081-FMCA-EBZ EVM derives power from Intel Agilex I-Series F-Tile Demo Board through FMC+ connector.
- The F-tile transceiver and JESD204C Intel FPGA IP core PLL reference clocks are supplied by Si5345-D-EVB through SMA to SMP cable. Set MUX_DIP_SW0 to high on Agilex-I F-Tile Demo Board to ensure U22 is taking CLKIN1 that is connected to the SMP cable.
- The Si5345-D-EVB provides a reference clock to the HMC7044 programmable clock generator present in the AD9081 EVM through SMP to SMP cable.
- The management clock for JESD204C Intel FPGA IP core is supplied by Silicon Labs Si5332 programmable clock generator present in the Intel Agilex I-Series F-tile Demo Board.
- The HMC7044 programmable clock generator provides the AD9081 device reference clock. The phase-locked loop (PLL) present in the AD9081 device generates the desired ADC sampling clock from the device reference clock.
- For Subclass 1, the HMC7044 clock generator generates the SYSREF signal for the AD9081 device and for the JESD204C Intel FPGA IP through the FMC+ connector.

Note: Intel recommends the SYSREF to be provided by the clock generator that sources the JESD204C Intel FPGA IP device clock.

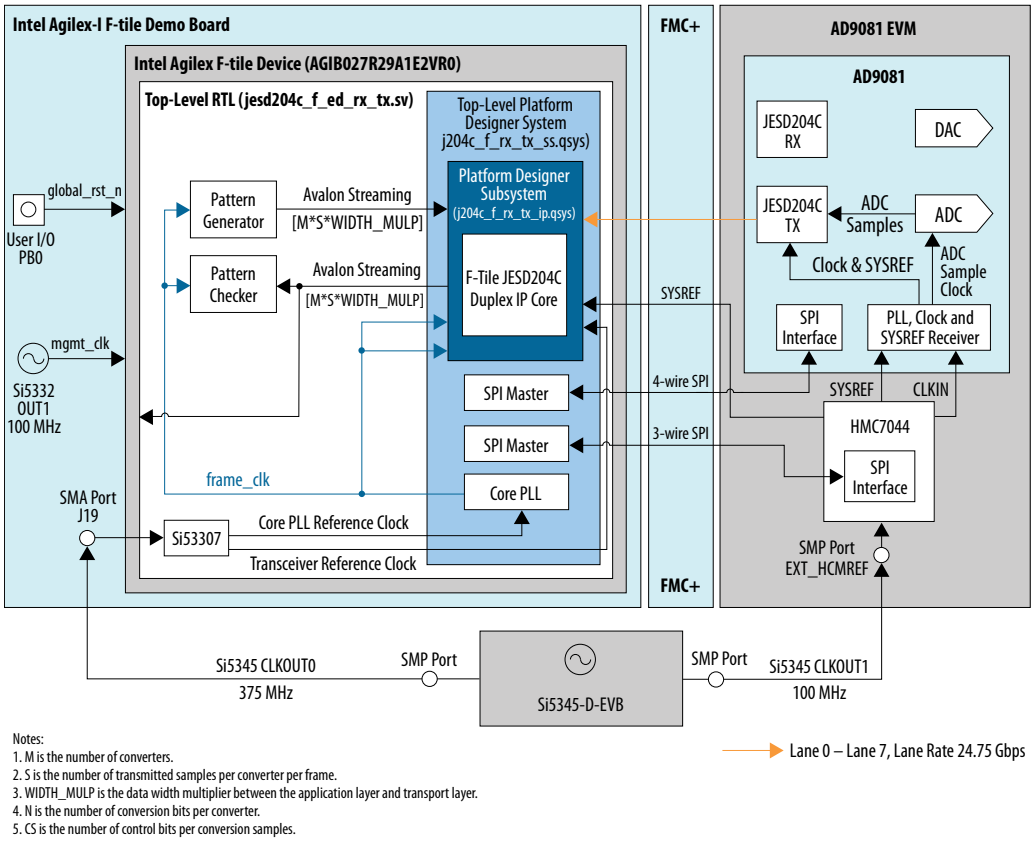
Figure 1. Hardware Setup



1.3. System Description

The following system-level diagram shows how the different modules are connected in this design.

Figure 2. System Diagram



Notes:
1. M is the number of converters.
2. S is the number of transmitted samples per converter per frame.
3. WIDTH_MULP is the data width multiplier between the application layer and transport layer.
4. N is the number of conversion bits per converter.
5. CS is the number of control bits per conversion samples.

In this setup, for example L = 8, M = 4, and F = 1, the data rate of transceiver lanes is 24.75 Gbps.

The Si5332 OUT1 generates 100 MHz clock to `mgmt_clk`. Si5345-D-EVB generates two clock frequencies, 375 MHz and 100 MHz. The 375 MHz is supplied to the embedded multiplexer in the Intel Agilex I-Series F-tile Demo Board through the J19 SMA port. The output clock of the embedded multiplexer drives the F-tile transceiver reference clock (`refclk_xcvr`) and JESD204C Intel FPGA IP core PLL reference clock (`refclk_core`). 100 MHz from Si5345-D-EVB is connected to the HMC7044 programmable clock generator present in the AD9081 EVM as the clock input (EXT_HMCREF).

The HCM7044 generates a periodic SYSREF signal of 11.71875 MHz through the FMC Connector.

The JESD204C Intel FPGA IP is instantiated in Duplex mode but only the receiver path is used.

1.4. Interoperability Methodology

The following section describes the test objectives, procedure, and the passing criteria. The test covers the following areas:

- Receiver data link layer
- Receiver transport layer

1.4.1. Receiver Data Link Layer

This test area covers the test cases for sync header alignment (SHA) and extended multiblock alignment (EMBA).

On link start up, after the receiver reset, the JESD204C Intel FPGA IP starts looking for the sync header stream that is transmitted by the device. The following registers from data link layer are read during the test, written into log files, and verified for passing criteria through TCL scripts.

Related Information

F-tile JESD204C Intel FPGA IP User Guide

1.4.1.1. Sync Header Alignment (SHA)

Table 1. Sync Header Alignment Test Cases

Test Case	Objective	Description	Passing Criteria
SHA.1	Check if Sync Header Lock is asserted after the completion of the reset sequence.	The following signals are read from registers: • `CDR_Lock` is read from the `rx_status3` (0x8C) register. • `SH_Locked` is read from `rx_status4` (0x90) register. • `jrx_sh_err_status` is read from the `rx_err_status` (0x60) register.	• `CDR_Lock` and `SH_LOCK` should be asserted to high corresponding to the number of lanes. • `jrx_sh_err_status` should be 0. The bit fields in `jrx_sh_err_status` checks for `sh_unlock_err`, `rx_gb_overflow_err`, `rx_gb_underflow_err`, `invalid_sync_header`, `src_rx_alarm`, `syspll_lock_err`, and `cdr_locked_err`.
SHA.2	Check Sync Header Lock status after sync header lock is achieved (or during the Extended Multi-Block Alignment phase) and stable.	`invalid_sync_header` is read for Sync Header lock status from register (0x60[8]).	`invalid_sync_header` status should be 0.

1.4.1.2. Extended Multiblock Alignment (EMBA)

Table 2. Extended Multiblock Alignment Test Cases

Test Case	Objective	Description	Passing Criteria
EMBA.1	Check if the Extended Multiblock Lock is asserted only after the assertion of Sync Header Lock.	The following signals are read through registers:	• The `EMB_Locked_1` value should be equal to 1 corresponding to each lane. `EMB_Lock_err` should be 0.

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Test Case	Objective	Description	Passing Criteria
		• EMB_Locked_1 is read from the rx_status5 (0x94) register. • EMB_Lock_err is read from the rx_err_status (0x60[19]) register.	
EMBA.2	Check if the Extended Multiblock Lock status is stable (after extended multiblock lock or until the elastic buffer is released) along with no invalid multiblock.	invalid_eomb_eoemb is read from the rx_err_status (0x60[10:9]) register.	invalid_eomb_eoemb should be "00".
EMBA.3	Check the lane alignment.	The following values are read from registers: • elastic_buf_over_flow is read from the rx_err_status (0x60[20]) register. • elastic_buf_full is read from the rx_status6 (0x98) register.	• elastic_buf_over_flow should be 0. • The elastic_buf_full value should be equal to 1 corresponding to each lane.

1.4.2. Receiver Transport Layer (TL)

To check the data integrity of the payload data stream through the receiver (RX) JESD204C Intel FPGA IP and transport layer, the ADC is configured to ramp/PRBS test pattern. The ADC is also set to operate with the same configuration as set in the JESD204C Intel FPGA IP. The ramp/PRBS checker in the FPGA fabric checks the ramp/PRBS data integrity for one minute. The RX JESD204C Intel FPGA IP register rx_err is polled continuously for zero value for one minute.

The figure below shows the conceptual test setup for data integrity checking.

Figure 3. Data Integrity Check Using Ramp/PRBS15 Checker

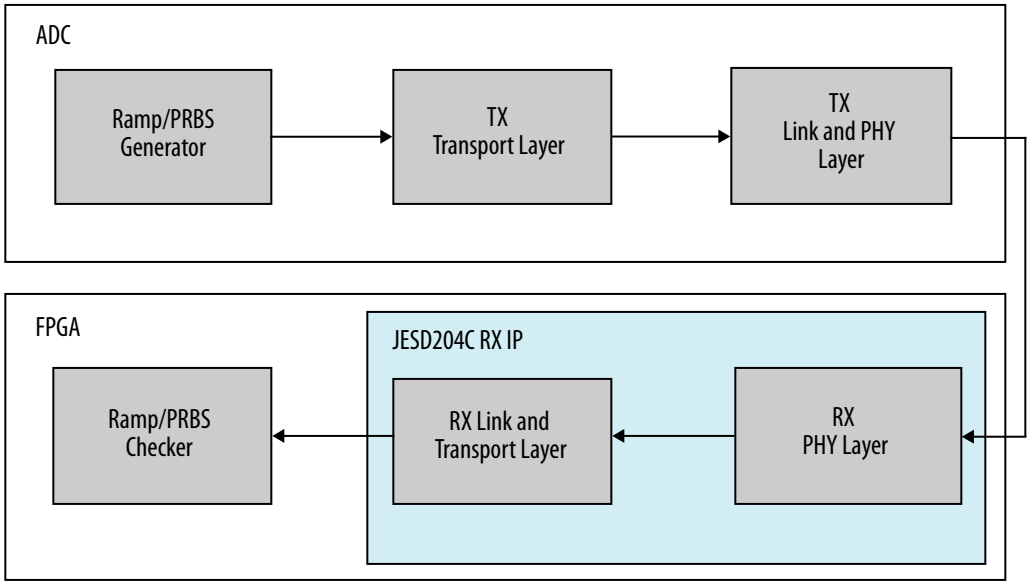

Table 3. Transport Layer Test Cases

Test Case	Objective	Description	Passing Criteria
TL.1	Check the transport layer mapping of the data channel using ramp test pattern.	Data_mode is set to Ramp_mode. The following signals are read through registers: • `crc_err` is read from the `rx_err_status` (0x60[14]). • `jrx_patchk_data_error` is read from the `tst_err0` register.	• `crc_err` should be low to pass. • `jrx_patchk_data_error` should be low.
TL.2	Check the transport layer mapping of the data channel using the PRBS15 test pattern.	Data_mode is set to prbs_mode. The following values are read from registers: • `crc_err` is read from the `rx_err_status` (0x60[14]). • `jrx_patchk_data_error` is read from the `tst_err0` register.	• `crc_err` should be low to pass. • `jrx_patchk_data_error` should be low.

1.5. JESD204C Intel FPGA IP and ADC Configurations

The JESD204C Intel FPGA IP parameters (L, M, and F) in this hardware checkout are natively supported by the AD9081 device. The transceiver data rate, sampling clock, and other JESD204C parameters comply with the AD908D1 operating conditions.

The hardware checkout testing implements the JESD204C Intel FPGA IP with the following parameter configuration.

Global setting for all configuration:

- E = 1
- CF = 0
- CS = 0
- Subclass = 1
- FCLK_MULP = 1
- WIDTH_MULP = 8
- SH_CONFIG = CRC-12
- FPGA Management Clock (MHz) = 100

1.6. Test Results

The following table contains the possible results and their definition.

Table 4. Results Definition

Result	Definition
PASS	The Device Under Test (DUT) was observed to exhibit conformant behavior.
PASS with comments	The DUT was observed to exhibit conformant behavior. However, an additional explanation of the situation is included (example: due to time limitations, only a portion of the testing was performed).

continued...

Result	Definition
FAIL	The DUT was observed to exhibit non-conformant behavior.
Warning	The DUT was observed to exhibit behavior that is not recommended.
Refer to comments	From the observations, a valid pass or fail could not be determined. An additional explanation of the situation is included.

The following table shows the results for test cases SHA.1, SHA.2, EMBA.1, EMBA.2, EMBA.3, TL.1, and TL.2 with respective values of L, M, F, data rate, sampling clock, link clock, and SYSREF frequencies.

Table 5. Result for Test Cases SHA.1, SHA.2, EMBA.1, EMBA.2, EMBA.3, TL.1, and TL.2

No.	L	M	F	S	HD	E	N	NP	ADC Sampling Clock (MHz)	FPGA Device Clock (MHz)	FPGA Frame Clock (MHz)	FPGA Link Clock (MHz)	Lane Rate (Gbps)	Result
1	8	4	1	1	0	1	16	16	3000.00	375.00	375.00	375.00	24.75	Pass

1.7. Test Result Comments

In each test case, the RX JESD204C Intel FPGA IP successfully establishes the sync header alignment, extended multiblock alignment, and until user data phase.

No data integrity issue is observed by the Ramp and PRBS checker for JESD configurations covering all physical lanes, also no cyclic redundancy check (CRC) and command parity error is observed.

During certain power cycles, lane deskew error might appear with the parameter configurations. To avoid this error, the LEMC offset values should be programmed or you can automate this with the calibration sweep procedure. For more information on the legal values of LEMC offset, refer to RBD Tuning Mechanism in F-tile JESD204C IP User Guide.

Related Information

RBD Tuning Mechanism

1.8. Summary

This report shows validation of the JESD204C Intel FPGA IP and PHY electrical interface with the AD9081/9082 (R2 Silicon) device up to 24.75 Gbps for ADC. The complete configuration and hardware setup are shown to provide confidence in the interoperability and performance of the two devices.

1.9. Document Revision History for AN 927: JESD204C Intel FPGA IP and ADI AD9081 MxFE* ADC Interoperability Report for Intel Agilex F-Tile Devices

Document Version	Changes
2022.04.25	Initial release.