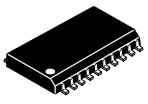
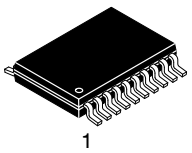
Low Voltage Octal Buffer/Line Driver with 5 V Tolerant Inputs and Outputs

74LVX273



SOIC-20W
CASE 751BJ



TSSOP-20
CASE 948AQ

The LVX273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (MR) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the MR input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements. The inputs tolerate up to 5.5 V allowing interface of 5 V systems to 3 V systems.

Features

- Input Voltage Translation From 5 V to 3 V
- Ideal for Low Power/low Noise 3.3 V Applications
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

PIN DESCRIPTION

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

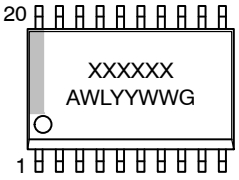
TRUTH TABLE

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load '1'	H		H	H
Loard '0'	H		L	L

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

MARKING DIAGRAMS

SOIC-20W



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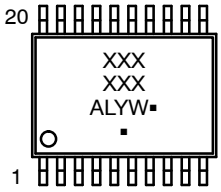


XXXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb-Free Package

(Note: Microdot may be in either location)

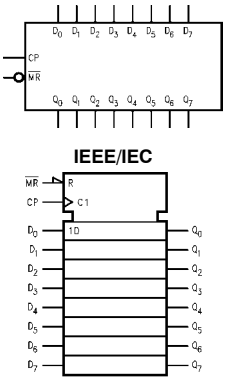


Figure 1. Logic Symbols

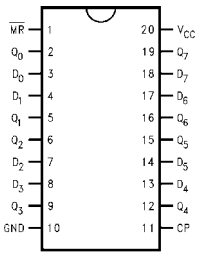
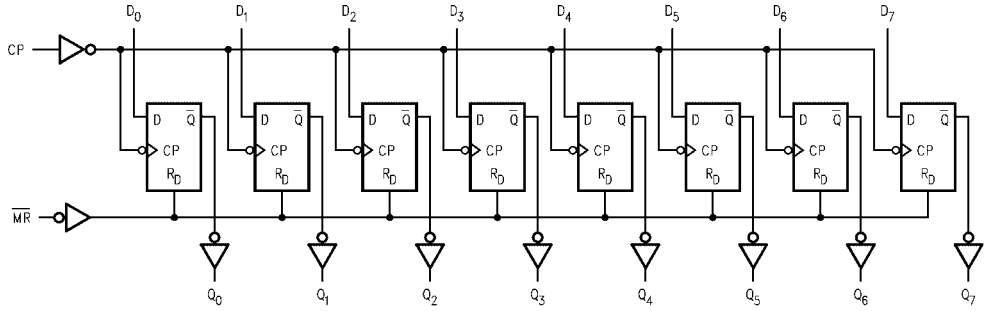


Figure 2. Connection Diagram

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to +6.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} + 0.5	V
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
I_{IK}	Input Clamp Current		−20	mA
I_{OK}	Output Clamp Current		±20	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SOIC-20W	96	°C/W
		TSSOP-20	150	
P_D	Power Dissipation in Still Air at 25 °C	SOIC-20W	1302	mW
		TSSOP-20	833	
MSL	Moisture Sensitivity	SOIC-20W	Level 3	–
		All Other Packages	Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.573 in	–
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model	2000	V
		Charged Device Model	N/A	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{IN}	DC Input Voltage (Note 4)	0	5.5	V
V_{OUT}	DC Output Voltage (Note 4)	0	V_{CC}	V
T_A	Operating Temperature	−40	+85	°C
t_r, t_f	Input Rise or Fall Rate	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40 °C to +85 °C			T_A = −40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High-Level Input Voltage		2.0	1.5			1.5		V
			3.0	2.0			2.0		
			3.6	2.4			2.4		
V_{IL}	Low-Level Input Voltage		2.0		0.5			0.5	V
			3.0		0.8			0.8	
			3.6		0.8			0.8	
V_{OH}	High-Level Output Voltage	V_{IN} = V_{IH} or V_{IL}							V
		I_{OH} = −50 μA	2.0	1.9	2.0		1.9		
		I_{OH} = −50 μA	3.0	2.9	3.0		2.9		
		I_{OH} = −4 mA	3.6	2.58			2.48		
V_{OL}	Low-Level Output Voltage	V_{IN} = V_{IH} or V_{IL}							V
		I_{OH} = −50 μA	2.0		0	0.1		0.1	
		I_{OH} = −50 μA	3.0		0	0.1		0.1	
		I_{OL} = −4 mA	3.6			0.36		0.44	
I_{OZ}	3-State Output Leakage Current	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = VCC or GND	3.6			±0.25		±2.5	μA
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	3.6			±0.1		±1.0	
I_{CC}	Quiescent Supply Current	V_{IN} = 5.5 V or GND	3.6			±4.0		40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	C_L (pF)	V_{CC} (V)	T_A = −40 °C to +85 °C			T_A = −40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay CP to Q_n	15	2.7		9.0	16.9	1.0	20.5	ns
		50			11.5	20.0	1.0	24.0	
		15	3.3 ± 0.3		7.1	11.0	1.0	13.0	
		50			9.6	14.5	1.0	16.5	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	15	2.7		9.3	17.8	1.0	20.5	ns
		50			11.8	21.1	1.0	24.0	
		15	3.3 ± 0.3		7.3	11.5	1.0	13.5	
		50			9.8	15.0	1.0	17.0	
t_S	Setup Time D_n to CP		2.7	8.0			9.5		ns
			3.3 ± 0.3	5.5			6.5		
t_H	Hold Time D_n to CP		2.7	1.0			1.0		ns
			3.3 ± 0.3	1.0			1.0		
t_{REC}	Removal Time $\overline{MR}$ to Q_n		2.7	4.0			4.0		ns
			3.3 ± 0.3	2.5			2.5		
t_W	Clock Pulse Width		2.7	8.0			9.5		ns
			3.3 ± 0.3	5.5			6.5		

AC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	C_L (pF)	V_{CC} (V)	T_A = −40 °C to +85 °C			T_A = −40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	
t_W	$\overline{MR}$ Pulse Width		2.7	7.5			8.5		
			3.3 ± 0.3	5.0			6.0		
f_{MAX}	Maximum Clock Frequency	15	2.7	55	110		45		MHz
		50		45	60		40		
		15	3.3 ± 0.3	95	150		80		
		50		60	90		50		
t_{OSLH}, t_{OSHL}	Output to Output Skew (Note 5)	50	2.7			1.5		1.5	ns
			3.3 ± 0.3			1.5		1.5	

5. Parameter guaranteed by design. $t_{OSLH} = | t_{PLHm} = t_{PLHn} |$, $t_{OSHL} |t_{PHLm} = t_{PHLn}|$.

NOISE CHARACTERISTICS

Symbol	Characteristic	C_L (pF)	V_{CC} (V)	T_A = +25 °C		Unit
				Typ	Limit	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	50	3.3	0.5	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	50	3.3	0.5	0.8	V
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	50	3.3		2.0	V
V_{ILD}	Maximum HOW Level Dynamic Input Voltage	50	3.3		0.8	V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	T_A = +25 °C			T_A = −40 °C to +125 °C		Unit
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{OUT}	Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 6)		31				pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the following equation:

$$ICC(opr.) = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8\ (\text{per F/F})} \qquad \text{(eq. 1)}$$

ORDERING INFORMATION

Device	Marking	Package	Shipping†
74LVX273MTCX	LCX 273	TSSOP-20 (Pb-Free)	2500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

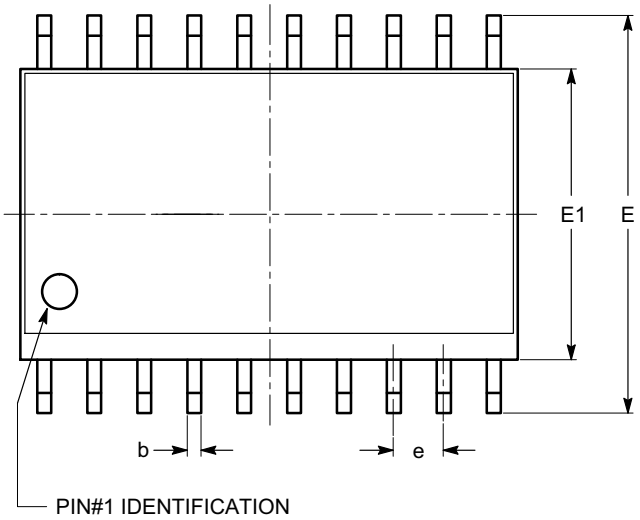
REVISION HISTORY

Revision	Description of Changes	Date
2	Converted the Data Sheet to **onsemi** format with the updates to Ordering Information and Maximum Ratings tables.	09/15/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

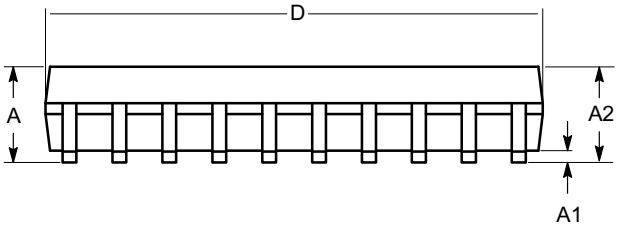
SOIC−20, 300 mils
CASE 751BJ
ISSUE O

DATE 19 DEC 2008

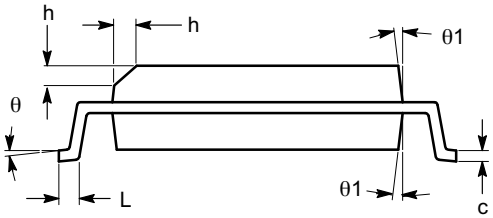


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.36	2.49	2.64
A1	0.10		0.30
A2	2.05		2.55
b	0.31	0.41	0.51
c	0.20	0.27	0.33
D	12.60	12.80	13.00
E	10.01	10.30	10.64
E1	7.40	7.50	7.60
e		1.27 BSC	
h	0.25		0.75
L	0.40	0.81	1.27
θ	0°		8°
θ1	5°		15°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
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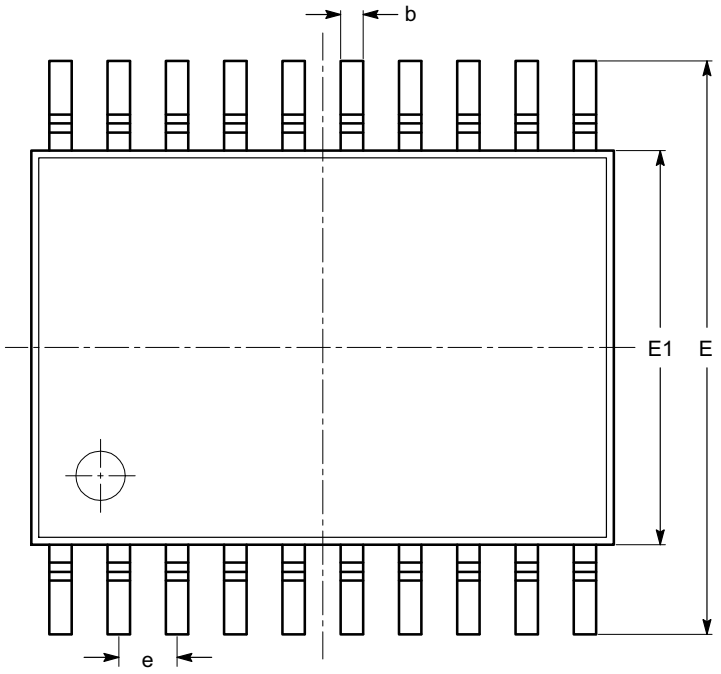
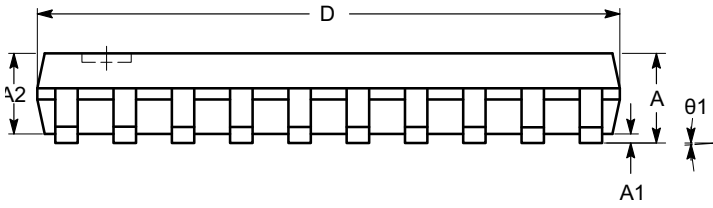
TSSOP20, 4.4x6.5
CASE 948AQ
ISSUE A

DATE 19 MAR 2009



TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°		8°



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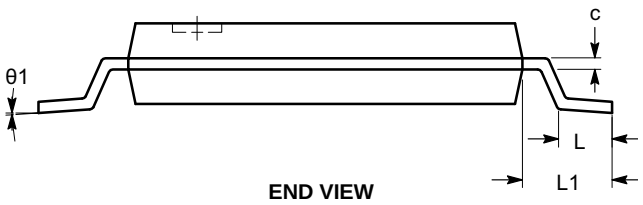

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