AG555Q-GL QuecOpen Hardware Design

Automotive Module Series

Version: 1.0.2

Date: 2022-12-05

Status: Preliminary

At Quectel, our aim is to provide timely and comprehensive services to our customers. If you require any assistance, please contact our headquarters:

Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local offices. For more information, please visit:
http://www.quectel.com/support/sales.htm.

For technical support, or to report documentation errors, please visit:
http://www.quectel.com/support/technical.htm.
Or email us at: support@quectel.com.

Legal Notices

We offer information as a service to you. The provided information is based on your requirements and we make every effort to ensure its quality. You agree that you are responsible for using independent analysis and evaluation in designing intended products, and we provide reference designs for illustrative purposes only. Before using any hardware, software or service guided by this document, please read this notice carefully. Even though we employ commercially reasonable efforts to provide the best possible experience, you hereby acknowledge and agree that this document and related services hereunder are provided to you on an “as available” basis. We may revise or restate this document from time to time at our sole discretion without any prior notice to you.

Use and Disclosure Restrictions

License Agreements

Documents and information provided by us shall be kept confidential, unless specific permission is granted. They shall not be accessed or used for any purpose except as expressly provided herein.

Copyright

Our and third-party products hereunder may contain copyrighted material. Such copyrighted material shall not be copied, reproduced, distributed, merged, published, translated, or modified without prior written consent. We and the third party have exclusive rights over copyrighted material. No license shall be granted or conveyed under any patents, copyrights, trademarks, or service mark rights. To avoid ambiguities, purchasing in any form cannot be deemed as granting a license other than the normal non-exclusive, royalty-free license to use the material. We reserve the right to take legal action for noncompliance with abovementioned requirements, unauthorized use, or other illegal or malicious use of the material.

Trademarks

Except as otherwise set forth herein, nothing in this document shall be construed as conferring any rights to use any trademark, trade name or name, abbreviation, or counterfeit product thereof owned by Quectel or any third party in advertising, publicity, or other aspects.

Third-Party Rights

This document may refer to hardware, software and/or documentation owned by one or more third parties ("third-party materials"). Use of such third-party materials shall be governed by all restrictions and obligations applicable thereto.

We make no warranty or representation, either express or implied, regarding the third-party materials, including but not limited to any implied or statutory, warranties of merchantability or fitness for a particular purpose, quiet enjoyment, system integration, information accuracy, and non-infringement of any third-party intellectual property rights with regard to the licensed technology or use thereof. Nothing herein constitutes a representation or warranty by us to either develop, enhance, modify, distribute, market, sell, offer for sale, or otherwise maintain production of any our products or any other hardware, software, device, tool, information, or product. We moreover disclaim any and all warranties arising from the course of dealing or usage of trade.

Privacy Policy

To implement module functionality, certain device data are uploaded to Quectel's or third-party's servers, including carriers, chipset suppliers or customer-designated servers. Quectel, strictly abiding by the relevant laws and regulations, shall retain, use, disclose or otherwise process relevant data for the purpose of performing the service only or as permitted by applicable laws. Before data interaction with third parties, please be informed of their privacy and data security policy.

Disclaimer

a) We acknowledge no liability for any injury or damage arising from the reliance upon the information.
b) We shall bear no liability resulting from any inaccuracies or omissions, or from the use of the information contained herein.
c) While we have made every effort to ensure that the functions and features under development are free from errors, it is possible that they could contain errors, inaccuracies, and omissions. Unless otherwise provided by valid agreement, we make no warranties of any kind, either implied or express, and exclude all liability for any loss or damage suffered in connection with the use of features and functions under development, to the maximum extent permitted by law, regardless of whether such loss or damage may have been foreseeable.
d) We are not responsible for the accessibility, safety, accuracy, availability, legality, or completeness of information, advertising, commercial offers, products, services, and materials on third-party websites and third-party resources.

Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-03-25	Liam CAO/ Brain WANG	Creation of the document
1.0.0	2022-03-25	Liam CAO/ Brian WANG	Preliminary
1.0.1	2022-11-02	Liam CAO/ Benjamin CHAI	Preliminary: 1. Updated the information related to the Recovery NAND interface and changed the pin name, as follows: Updated the pin name of pin 65 from EBI2_WE_N to RESERVED; Updated the pin name of pin 82 from EBI2_ALE_N to RESERVED; Updated the pin name of pin 74 from EBI2_CLE_N to RESERVED; Updated the pin name of pin 99 from EBI2_AD_0 to RESERVED; Updated the pin name of pin 97 from EBI2_AD_1 to RESERVED; Updated the pin name of pin 96 from EBI2_AD_2 to RESERVED; Updated the pin name of pin 94 from EBI2_AD_3 to RESERVED; Updated the pin name of pin 64 from EBI2_BUSY_N to GPIO13. Updated the pin name of pin 77 from EBI2_OE_N to CDC_RST_N. Updated the pin name of pin 88 from EBI2_AD_7 to USB_SS_RX_M. Updated the pin name of pin 90 from EBI2_AD_6 to USB_SS_RX_P.

			Updated the pin name of pin 91 from EBI2_AD_5 to USB_SS_TX_M. Updated the pin name of pin 93 from EBI2_AD_4 to USB_SS_TX_P. 2. Added the RFFE MIPI interface and updated the pin name, as follows: Updated the pin name of pin 157 from RESERVED to RFFE0_CLK; Updated the pin name of pin 154 from RESERVED to RFFE0_DATA; Updated the pin name of pin 178 from RESERVED to RFFE1_CLK; Updated the pin name of pin 175 from RESERVED to RFFE1_DATA. 3. Added the pin 404 (VBAT_RF), pin 412 (VBAT_RF); and added the GND pins of pin 401–403, 405–411, 413 and 414. 4. Updated the module size from 41 × 45 × 2.85 mm to 47.5 × 42 × 3.45 mm, therefore, updated the mechanical information and packaging specifications. 5. Updated the information of USB serial driver (Table 3). 6. Added some note description about the data of Tx power (Chapter 5.13). 7. Updated the table of Rx sensitivity and added some note description about the data of Rx sensitivity (Chapter 5.1.4). 8. Updated the data of GNSS performance and updated the note description (Chapter 5.2.3). 9. Updated the information of manufacturing and soldering (Chapter 8.2).
1.0.2	2022-12-05	Liam CAO/ Benjamin CHAI	Preliminary: 1. Added n14 and n48 bands of 5G NR SA; and deleted B11 of LTE-FDD. 2. Updated the Vmin value of VBAT_BB & VBAT_RF. 3. Added the dual-band: L1 + L2* (optional) (Table 2 & Table 3 & Chapter 5.2). 4. Updated the description of PCM interface (Table 3). 5. Updated the data of USB serial drivers (Table 3). 6. Updated the max. DL transmission data rates of 5G NR SA (Table 3). 7. Added the information of module weight (Table 3). 8. Updated the pin 9 from “RESERVED” to “PWM” (Figure 2 & Table 5)

	9. Updated the comment description of SDC1_DATA_6 & SDC1_DATA_7 (Table 5 & Table 19). 10. Updated the comment description of ADC interfaces (Table 5 & Table 25). 11. Updated the comment description of NAND_CS_N (Table 5 & Table 29). 12. Updated the power-up timing (Figure 11). 13. Updated the pin definition of cellular antenna interfaces (Table 31). 14. Added the test conditions description of receiver sensitivity (Table 34). 15. Updated the 3GPP SIMO data of n5/n8/12/n20 (Table 34). 16. Updated the reference circuit of RF antenna interfaces and added a note description about ESD protection components (Chapter 5.1.5). 17. Updated the GNSS performance note description (Chapter 5.2.3). 18. Updated the reference circuit of GNSS antenna interfaces and added a note description about ESD protection components (Chapter 5.2.4). 19. Updated the information of antenna design requirements and added the related note description (Chapter 5.4). 20. Added the power consumption information of 5G NR SA data transfer (Chapter 6.3). 21. Updated the information of thermal dissipation (Chapter 6.7). 22. Updated the data of cooling down slope in manufacturing and soldering (Chapter 8.2). 23. Added the information of mounting direction (Chapter 8.3.3)

Contents

Table Index

Figure Index

1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio

This document defines the AG555Q-GL in QuecOpen® solution and describes its air interface and hardware interfaces which are connected with your applications. You can use the module as the basis for development of QuecOpen® applications.

This document helps you quickly understand the interface specifications, electrical and mechanical details, as well as other related information of the module. To facilitate application designs, it also includes some reference designs for your reference. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

NOTE

This document is also applicable to the TelSDK solution.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, argument, and so on, it indicates that the function, feature, interface, pin, AT command, argument, and so on, is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

2.1. General Description

AG555Q-GL module is a baseband processor platform based on ARM Cortex A7 kernel. The maximum dominant frequency is up to 1.5 GHz. The module contains global main bands to meet varied market demands.

AG555Q-GL module is one of the automotive-grade 5G NR Sub-6 GHz wireless communication modules, and provides data connectivity on 5G NR, LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, EDGE and GPRS networks. It also provides GNSS function (optional) and audio function to meet specific application demands.

AG555Q-GL module is an SMD type module which can be embedded into applications through its 414 LGA pins. With a compact profile of 47.5 mm × 42.0 mm × 3.45 mm, the module can meet most requirements for automobile applications.

Engineered to meet the demanding requirements in automotive applications and other harsh operating conditions, the module offers a premium solution for high performance automotive and intelligent transportation system (ITS) applications.

2.2. Frequency Bands and Functions

Table 2: Frequency Bands and GNSS Function

Network Type	AG555Q-GL
5G SA	n1/n2/n3/n5/n7/n8/n12/n14/n20/n25/n26/n28/n38/n40/n41/n48/n66/n71/ n77/n78/n79
5G NSA	n1/n2/n3/n5/n7/n8/n12/n20/n25/n28/n38/n40/n41/n66/n71/n77/n78/n79
LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B12/B13/B14/B17/B18/B19/B20/B21/B25/ B26/B28/B29 [1]/B30 [1]/B32 [1]/B66/B71

[1] LTE-FDD B29, B30 and B32 support Rx only, and B30 is subject to carrier's deployment.

LTE-TDD	B34/38/B39/B40/B41/B42/B48
WCDMA	B1/B2/B3/B4/B5/B6/B8/B9/B19
GSM	GSM850/EGSM900/DCS1800/PCS1900
GNSS (optional)	● Constellation: GPS, GLONASS, BDS, Galileo, QZSS ● Single-band GNSS: L1 ● Dual-band GNSS: L1 + L5 (default), L1+L2* (optional)

2.3. Key Features

The following table describes the detailed features of the module.

Table 3: Key Features

Feature	Details
Power Supply	**VBAT_BB/VBAT_RF:** ● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast
(U)SIM Interfaces	● Supports dual (U)SIM cards ● (U)SIM1 and (U)SIM2: 1.8/3.0 V
I2S Interface	● Used for external codec function ● Supports master and slave modes
I2C Interface	● Used for external codec configuration and IMU by default ● Compliant with *The I2C Specification Version 3.0* ● Multi-master is not supported
PCM Interface	PCM is not available by default due to 2nd NAND occupation
USB Interfaces	● Compliant with USB 3.1 Gen 2 and USB 2.0 specifications, with maximum transmission rates up to 10 Gbps on USB 3.1 and 480 Mbps on USB 2.0 ● USB 2.0 and USB 3.1 are used for AT command communication, data transmission, software debugging and GNSS NMEA sentences output. ● Only USB 2.0 can be used for firmware upgrade. ● USB 3.1 can be used for data communication with AP. ● When USB 2.0 and USB 3.1 are connected to the same host, USB 3.1 takes effect by default.

	● Support USB serial drivers for Windows 8/8.1/10/11, Linux 2.6–6.5 and Android 4.x–13.x
UART Interfaces	**2- Wire main UART (UART1):** ● Baud rate can reach up to 921600 bps, 115200 bps baud rate by default **2-Wire debug UART:** ● Used for Linux console and log output ● Supports 115200 bps baud rate
SDIO Interface	Support eMMC 4.5.1
SPI Interfaces	● Support master mode only ● Maximum clock frequency rate: 50 MHz
RGMII Interface	Support 10/100/1000 Mbps Ethernet [2]
PCIe Interface	● Compliant with *PCI Express Base Specification Revision 3.0* ● Supports 1 PCIe lane, with maximum rate of 8 GT/s × 1-lane
Antenna Interfaces	● One main antenna interface (ANT_MAIN) ● One diversity antenna interface (ANT_DRX) ● Two MIMO antenna interfaces (ANT_MIMO3, ANT_MIMO4) ● One GNSS antenna interface (ANT_GNSS) [3]
5G NR Features	● Support 3GPP Rel-15 ● Supported modulations: Uplink: π/2-BPSK, QPSK, 16QAM, 64QAM and 256QAM Downlink: QPSK, 16QAM, 64QAM and 256QAM ● Support 4 × 4 MIMO for MHB bands in DL direction ● Support SCS 15 kHz (FDD) and 30 kHz (TDD) ● Support option 3x, 3a and option 2 ● Support SA and NSA ● Max. transmission data rates: NSA: 2.4 Gbps (DL)/500 Mbps (UL) SA: 2.8 Gbps (DL)/900 Mbps (UL)
LTE Features	● Support up to 5CA Cat 19 LTE-FDD and TDD ● Support 1.4/3/5/10/15/20 MHz RF bandwidth ● Support 4 × 4 MIMO for MHB bands in DL direction [4] ● Support modulations: Uplink: QPSK, 16QAM, 64QAM, 256QAM* Downlink: QPSK, 16QAM, 64QAM, 256QAM ● LTE-FDD: Max. 1.6 Gbps (DL)/200 Mbps (UL) LTE-TDD: Max. 1.4 Gbps (DL)/120 Mbps (UL)
UMTS Features	● Support 3GPP Rel-8 DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA ● Support QPSK, 16QAM and 64QAM modulation ● DC-HSDPA: Max. 42 Mbps (DL)

[2] The module's RGMII interface supports the Gigabit Ethernet protocol, while actual throughput is subject to testing.
[3] GNSS function is optional.
[4] B21 do not support DL 4 × 4 MIMO, support 2 × 2 MIMO only.

	• HSUPA: Max. 5.76 Mbps (UL) • WCDMA: Max. 384 kbps (DL)/384 kbps (UL)
GSM Features	**GPRS:** • Support GPRS multi-slot class 33 (33 by default) • Coding scheme: CS 1–4 • Max. 107 kbps (DL)/85.6 kbps (UL) **EDGE:** • Support EDGE multi-slot class 33 (33 by default) • Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) • Downlink coding schemes: MCS 1–9 • Uplink coding schemes: MCS 1–9 • Max. 296 kbps (DL)/236.8 kbps (UL)
GNSS (Optional)	• Constellation: GPS, GLONASS, BDS, Galileo, QZSS • Support single-band GNSS: L1 • Support dual-band GNSS: L1 + L5 (default), L1 + L2* (optional) • Protocol: NMEA 0183 • Update rate: 1 Hz by default, max. up to 10 Hz
Audio Features	• Provide one digital audio interface: I2S interface • GSM: HR/FR/EFR/AMR/AMR-WB • WCDMA: AMR/AMR-WB • LTE/5G: AMR/AMR-WB • Support echo cancellation and noise suppression
Rx-diversity	Support 5G NR, LTE and WCDMA Rx-diversity
Temperature Range	• Operating temperature range: -35 °C to +75 °C [5] • Extended temperature range: -40 °C to +85 °C [6] • eCall temperature range: -40 °C to +95 °C [7] • Storage temperature range: -40 °C to +95 °C
Physical Characteristics	• Dimensions: (47.5 ±0.2) mm × (42.0 ±0.2) mm × (3.45 ±0.2) mm • Weight: 16.8 g
Firmware Upgrade	• USB 2.0 interface • DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

[5] Within the operating temperature range, the module meets 3GPP specifications, and eCall can be dialed out with a maximum power and data rate.
[6] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, eCall, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.
[7] Within eCall temperature range, the eCall function must be functional until the module is broken. When the ambient temperature is between 75 °C and 95 °C and the module temperature has reached the threshold value, the module will trigger protective measures (such as reduce power, decrease throughput and unregister the device) to ensure the full function of eCall.

2.4. Pin Assignment

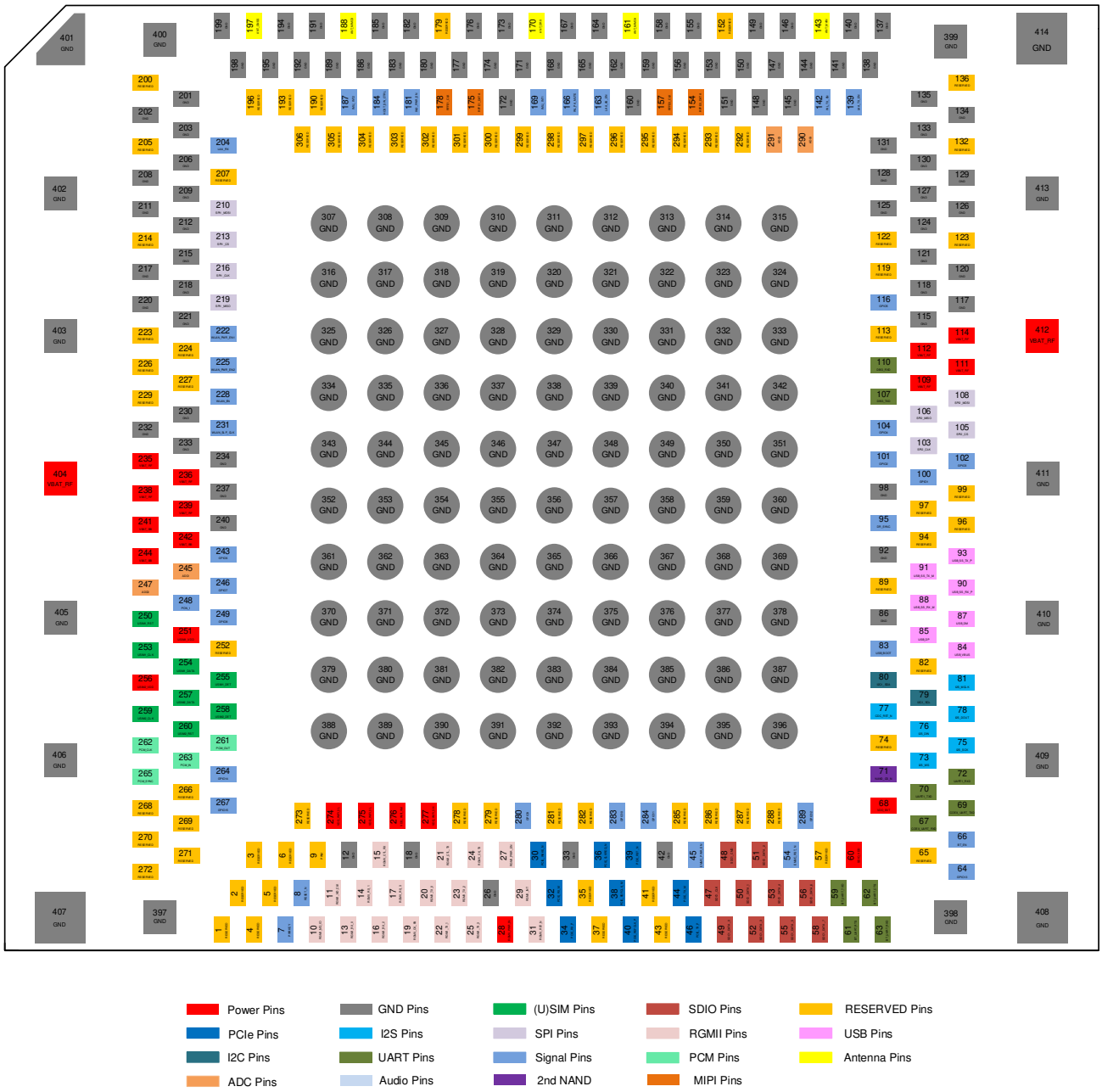


Figure 1: Pin Assignment (Top View)

NOTE

1. Unless otherwise specified, keep all RESERVED and unused pins unconnected.
2. GND pins should be connected to ground in the design.

2.5. Pin Description

2.5.1. Pin Definition

The following tables show the pin definition of the module.

Table 4: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 5: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	241, 242, 244	PI	Power supply for the module's baseband part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 3 A for VBAT_BB + VBAT_RF.
VBAT_RF	109, 111, 112, 114, 235, 236,	PI	Power supply for the module's RF part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	

	238, 239, 404, 412				
VDD_EXT	68	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	This pin can be used to connect with VDD_IO of Quectel AF68E, it also can be used as power supply for external pull up circuits if needed. A test point is recommended to be reserved.
GND	12, 18, 26, 33, 42, 86, 92, 98, 115, 117, 118, 120, 121, 124, 125, 126, 127, 128, 129, 130, 131, 133, 134, 135, 137, 138, 140, 141, 144, 145, 146, 147, 148, 149, 150, 151, 153, 155, 156, 158, 159, 160, 162, 164, 165, 167, 168, 171, 172, 173, 174, 176, 177, 180, 182, 183, 185, 186, 189, 191, 192, 194, 195, 198, 199, 201, 202, 203, 206, 208, 209, 211, 212, 215, 217, 218, 220, 221, 230, 232, 233, 234, 237, 240, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 403, 405, 406, 407, 408, 409, 410, 411, 413, 414				

Turn On/Off

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	7	DI	Turn on/off the module	V_{IH}max = 1.89 V V_{IH}min = 1.17 V V_{IL}max = 0.5 V	Internally pulled up to 1.8 V. The voltage level is about 1.1 V because of the diode drop in the baseband chipset. Active LOW.
PON_1	248	DI	Drive HIGH to initiate power on	V_{IH}max = 4.3 V V_{IH}min = 0.78 V V_{IL}max = 0.42 V	PON_1 is a high-voltage tolerant pin up to VBAT_BB domain, therefore it can be pulled up to VBAT_BB or 1.8 V. Pull down to ground if

					unused.
RESET_N	8	DI	Reset the module	V_{IH}max = 1.89 V V_{IH}min = 0.78 V V_{IL}max = 0.42 V	Pulled up internally to 1.8 V. Active LOW. A test point is recommended to be reserved if unused.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	251	PO	(U)SIM1 card power supply	1.8/3.0 V	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM2_VDD	256	PO	(U)SIM2 card power supply		
USIM1_DATA	254	DIO	(U)SIM1 card data	1.8/3.0 V	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM2_DATA	257	DIO	(U)SIM2 card data		
USIM1_RST	250	DO	(U)SIM1 card reset		
USIM2_RST	260	DO	(U)SIM2 card reset		
USIM1_CLK	253	DO	(U)SIM1 card clock		
USIM2_CLK	259	DO	(U)SIM2 card clock		
USIM1_DET	255	DI	(U)SIM1 card hot-plug detect	1.8 V	If unused, keep them open.
USIM2_DET	258	DI	(U)SIM2 card hot-plug detect		
USB Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	84	DI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	Maximum current: 0.1 mA. Typical 5.0 V.
USB_DP	85	AIO	USB 2.0 differential data (+)		Compliant with USB 2.0 standard specification. Require differential impedance of 90 Ω.
USB_DM	87	AIO	USB 2.0 differential data (-)		

USB_SS_TX_P	93	AO	USB 3.1 SuperSpeed transmit (+)		Compliant with USB 3.1 standard specifications. Require differential impedance of 70–100 Ω, and 85 Ω is recommended.
USB_SS_TX_M	91	AO	USB 3.1 SuperSpeed transmit (-)		
USB_SS_RX_P	90	AI	USB 3.1 SuperSpeed receive (+)		
USB_SS_RX_M	88	AI	USB 3.1 SuperSpeed receive (-)		
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	100	DIO	General-purpose input/output.	1.8 V group 1	Support wake-up interrupt.
GPIO2	101	DIO			
GPIO3	102	DIO			
GPIO4	104	DIO			Support wake-up interrupt.
GPIO5	116	DIO			
GPIO6	243	DIO	General-purpose input/output.	1.8 V group 3	GPIO6 is from internal PMIC, it is only recommended to be used as an output signal.
GPIO7	246	DIO	General-purpose input/output.	1.8 V group 1	
GPIO8	249	DIO			
GPIO9	280	DIO			
GPIO10	283	DIO			Support wake-up interrupt.
GPIO11	284	DIO			Support wake-up interrupt.
GPIO12	289	DIO			Support wake-up interrupt.
GPIO13	64	DIO			

GPIO14	264	DIO			Support wake-up interrupt.
GPIO15	267	DIO			Support wake-up interrupt.
Main UART Interface (UART1)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART1_TXD	70	DO	UART1 transmit	1.8 V group 1	If unused, keep them open.
UART1_RXD	72	DI	UART1 receive		
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	110	DI	Debug UART receive	1.8 V group 1	It is recommended to reserve test points for debug UART.
DBG_TXD	107	DO	Debug UART transmit		
I2C1 Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C1_SCL	79	OD	I2C1 serial clock	1.8 V group 1	External pull-up resistors are required. If unused, keep them open.
I2C1_SDA	80	OD	I2C1 serial data		
I2S Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2S_MCLK	81	DO	Clock output for codec	1.8 V group 1	12.288 MHz clock output
I2S_WS	73	DIO	I2S word select		If unused, keep them open.
I2S_SCK	75	DIO	I2S clock		Serve as output signals in master mode. Serve as input signals in slave mode.
I2S_DIN	76	DI	I2S data in		If unused, keep them open.
I2S_DOUT	78	DO	I2S data out		

CDC_RST_N	77	DO	External codec reset		
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	265	DIO	PCM data frame sync	1.8 V group 1	Serve as output signals in master mode. Serve as input signals in slave mode.
PCM_CLK	262	DIO	PCM clock		
PCM_IN	263	DI	PCM data input		This pin is used as GPIO to detect the chip select signal of the NAND by default. If unused, keep it open.
PCM_OUT	261	DO	PCM data output		If unused, keep it open.
PCIe Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE_REFCLK_P	40	AIO	PCIe reference clock (+)		Serve as output signals in RC mode. Serve as input signals in EP mode.
PCIE_REFCLK_M	38	AIO	PCIe reference clock (-)		The differential impedance should be the same as that for PCIe TX/RX. Require differential impedance of 70–100 Ω, and 85 Ω is recommended.
PCIE_TX_M	44	AO	PCIe transmit (-)		Require differential impedance of 70–100 Ω, and 85 Ω is recommended.
PCIE_TX_P	46	AO	PCIe transmit (+)		
PCIE_RX_M	32	AI	PCIe receive (-)		
PCIE_RX_P	34	AI	PCIe receive (+)		

PCIE_CLKREQ_N	36	DIO	PCIe clock request	1.8 V group 1	Serve as input signals in RC mode. Serve as output signals in EP mode. Require 100 kΩ external pull-up to VDD_EXT.
PCIE_WAKE_N	30	DIO	PCIe wake up		
PCIE_RST_N	39	DIO	PCIe reset	1.8 V group 1	Serves as an output signal in RC mode. Serves as an input signal in EP mode.
RGMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RGMII_MD_IO	10	DIO	RGMII management data	1.8/2.5 V	Add a pull-up resistor to this pin, and place the resistor close to the external PHY end. The power domain depends on RGMII_PWR_IN.
RGMII_MD_CLK	11	DO	RGMII management clock		Do not add any pull-up resistor to this pin, otherwise it may cause higher current consumption during sleep mode. The power domain depends on RGMII_PWR_IN.
RGMII_RX_0	13	DI	RGMII receive data bit 0		The power domain depends on RGMII_PWR_IN. Typ.1.8/2.5 V, and 1.8 V is recommended. The single-ended impedance requires 50 Ω.
RGMII_RX_1	14	DI	RGMII receive data bit 1		
RGMII_CTL_RX	15	DI	RGMII receive control		
RGMII_RX_2	16	DI	RGMII receive data bit 2		
RGMII_RX_3	17	DI	RGMII receive data bit 3		
RGMII_CK_RX	19	DI	RGMII receive clock		

RGMII_TX_0	20	DO	RGMII transmit data bit 0		
RGMII_CTL_TX	21	DO	RGMII transmit control		
RGMII_TX_1	22	DO	RGMII transmit data bit 1		
RGMII_TX_2	23	DO	RGMII transmit data bit 2		
RGMII_CK_TX	24	DO	RGMII transmit clock		
RGMII_TX_3	25	DO	RGMII transmit data bit 3		
RGMII_PWR_EN	27	DO	Enable external LDO to supply power to RGMII_PWR_IN	1.8 V	
RGMII_INT	29	DI	RGMII PHY interrupt output		
RGMII_RST_N	31	DO	Reset output for RGMII PHY		
RGMII_PWR_IN	28	PI	Power input for internal RGMII circuit	1.8/2.5 V	An external power LDO is required to power this pin. Max. 100 mA in operating current. If RGMII interface is not used, connect this pin to VDD_EXT.
SDIO Interface (for eMMC by default)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDIO_VDD	60	PI	SDIO power supply	Vmax = 1.95 V Vmin = 1.65 V Vnom = 1.8 V	Connect to external 1.8 V LDO in eMMC application. If SDIO interface is not used, connect this pin to VDD_EXT.
SDC1_CMD	48	DIO	SDIO command	1.8 V	If unused, keep them open.
SDC1_DATA_0	49	DIO	SDIO data bit 0		

SDC1_DATA_1	50	DIO	SDIO data bit 1		
SDC1_DATA_2	51	DIO	SDIO data bit 2		
SDC1_DATA_3	52	DIO	SDIO data bit 3		
SDC1_DATA_4	53	DIO	SDIO data bit 4	1.8 V	Can be used as GPIO
SDC1_DATA_5	55	DIO	SDIO data bit 5		
SDC1_DATA_6	56	DIO	SDIO data bit 6		Used as BOOT_STS_0 to indicate module boot status by default.
SDC1_DATA_7	58	DIO	SDIO data bit 7		Used as BOOT_STS_1 to indicate module boot status by default.
SDC1_CLK	47	DO	SDIO clock	1.8 V	If unused, keep these pins open.
EMMC_RST_N*	54	DO	eMMC reset	1.8 V group 1	
EMMC_PWR_EN	45	DO	eMMC power supply enable control		
SPI Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI1_CLK	216	DO	SPI1 clock	1.8 V group 1	Supports SPI master mode only. If unused, keep them open. Can be configured to GPIOs.
SPI1_CS	213	DO	SPI1 chip select		
SPI1_MISO	219	DI	SPI1 master-in slave-out		
SPI1_MOSI	210	DO	SPI1 master-out slave-in		
SPI2_CLK	103	DO	SPI2 clock		
SPI2_CS	105	DO	SPI2 chip select		
SPI2_MISO	106	DI	SPI2 master-in slave-out		
SPI2_MOSI	108	DO	SPI2 master-out slave-in		

ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	247	AI	General-purpose ADC interface	Voltage range: 0–1.875 V	ADC0, 1, 3, 4 are used as internal antenna detection by default. General ADC function is required to change the module's BOM.
ADC1	245	AI			
ADC3	291	AI			
ADC4	290	AI			
Other Interface Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	83	DI	Force the module into download mode	1.8 V group 1	Active HIGH. It is recommended to reserve test points.
DR_SYNC	95	DO	Dead reckoning sync		If unused, keep these pins open.
IMU_INT1	169	DI	IMU interrupt 1		
IMU_INT2	187	DI	IMU interrupt 2		
IMU_PWR_EN	181	DO	IMU power enable control		
PWM	9	DO	Pulse-width modulation output	1.8 V group 3	
Recovery NAND Interface					
NAND_CS_N	71	DI	NAND chip select	V_{IH}min = 1.44 V V_{IH}max = 2.1 V V_{IL}max = 0.36 V	Low: Primary NAND; High: Recovery NAND
RFFE Control Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RFFE0_CLK	157	DO	MIPI control clock	1.8 V group 1	Reserved for RFFE control.
RFFE0_DATA	154	DIO	MIPI control data		
RFFE1_CLK	178	DO	MIPI control clock		
RFFE1_DATA	175	DIO	MIPI control data		

RF Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	143	AIO	Main antenna interface		50 Ω impedance.
ANT_DRX	170	AIO	Diversity antenna interface		
ANT_MIMO3	188	AIO	MIMO3 antenna interface		
ANT_MIMO4	161	AI	MIMO4 antenna interface		
ANT_GNSS [8]	197	AI	GNSS antenna		50 Ω impedance.
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	1, 2, 3, 4, 5, 6, 35, 37, 41, 43, 57, 65, 74, 82, 89, 94, 96, 97, 99, 113, 119, 122, 123, 132, 136, 152, 179, 190, 193, 196, 200, 205, 207, 214, 223, 224, 226, 227, 229, 252, 266, 268, 269, 270, 271, 272, 273, 278, 279, 281, 282, 285, 286, 287, 288, 292, 293, 294, 295, 296, 297, 298, 299, 300, 301, 302, 303, 304, 305, 306				Keep these pins open.

NOTE

1. Keep all RESERVED pins and unused pins unconnected.
2. GND pins should be connected to ground in the design.
3. For more details about DC characteristics, see ***Chapter 6.3.***

2.5.2. Pin Multiplexing and BLSP Assignment

See ***document [1]*** for details about pin multiplexing and BLSP assignment of the module.

2.6. EVB Kit

Quectel supplies an evaluation board (V2X&5G EVB) with accessories to develop and test the module. For more details, see ***document [2]***.

[8] GNSS function is optional.

3 Operating Characteristics

3.1. Operating Modes

The table below briefly summarizes the various operating modes of the module.

Table 6: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	The module remains registered on the network, and is ready to send and receive data. In this mode, the software is active.
	Voice/Data	The module is connected to network. Its power consumption varies with the network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** or device management related API function can set the module into a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** or device management related API function can set the module into airplane mode where the RF function is invalid.	
Sleep Mode	The module remains the ability to receive paging message, SMS, voice call and TCP/UDP data from the network normally. In this mode, the power consumption of the module is reduced to a very low level.	
Power Down Mode	The module's power supply is cut off by its power management unit. In this mode, the software is inactive, the serial interfaces are inaccessible, while the operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

NOTE

See ***document [3]*** or ***document [4]*** for details of device management API functions, and ***document [5]*** for details of **AT+CFUN**.

3.2. Power Saving

3.2.1. Low Power Mode (LPM)

The module is able to reduce its power consumption to an ultra-low level during the low power mode. This chapter mainly introduces some ways to enter or exit from low power mode. See ***document [6]*** for details about low power mode of the module. The diagram below illustrates the power consumption of the module during low power mode.

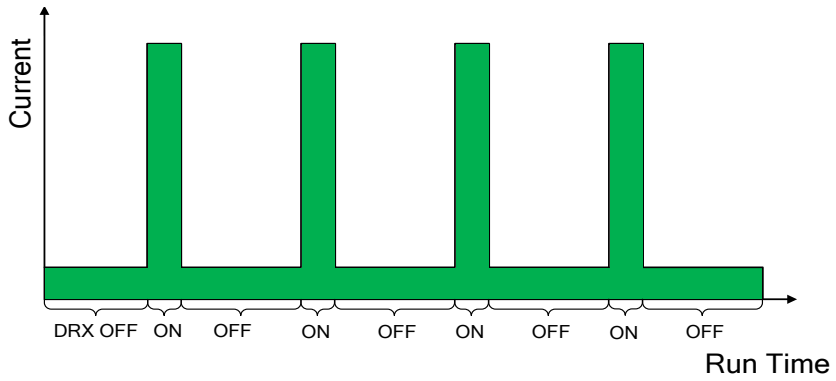


Figure 2: LPM Mode Power Consumption Diagram

NOTE

The DRX cycle values are broadcasted by the wireless network.

3.2.1.1. USB Application without USB Suspend Function

If the host does not support USB suspend function, USB_VBUS should be connected with an external control circuit to set the module into low power mode. In this case, the following three conditions must be met simultaneously to set the module into low power mode:

- Use LPM related API functions to enable the low power mode.
- Ensure that all pins that configured to interrupt the wake-up function are in the non-wakeup state.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

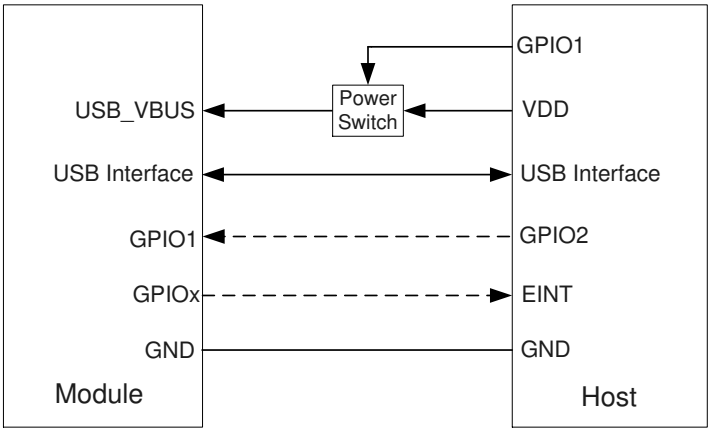


Figure 3: Low Power Mode Application Without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

1. Pay attention to the voltage-level matching of the circuit in dotted line, when the host interface is not 1.8 V power domain.
2. GPIO1 of the module is used as WAKEUP_IN (input signal) by default, through which the host can wake up the module from lower power mode or inform the module to enter into lower power mode
3. GPIOx can be any GPIO of the module. It should be defined into WAKEUP_OUT (output signal), through which the module wakes up the host from lower power mode.

3.2.1.2. LPM and Wakeup Timing

The following figure shows the LPM wakeup sequence of the module.

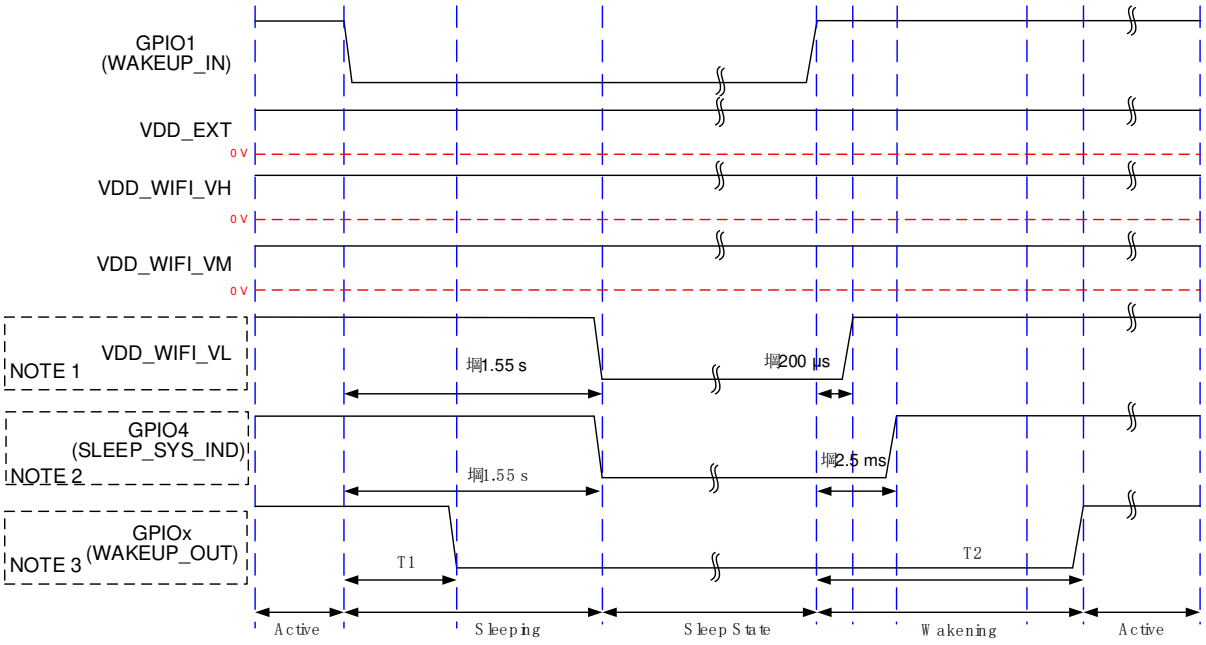


Figure 4: LPM and Wakeup Timing

NOTE

1. The time (T1) between the falling edges of WAKEUP_IN and SLEEP_SYS_IND depends on the real application scenario. If the module needs to process any task during the period, the time will be longer.
2. T1 and T2 depends on the application.

3.2.2. Airplane Mode

When the module enters airplane mode, the RF function does not work, and all AT commands and API functions correlative with RF function will be inaccessible.

AT command:

The mode can be set via **AT+CFUN=<fun>**. The parameter **<fun>** indicates the module's functionality levels, as shown below.

- **AT+CFUN=0:** Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

API functions:

The mode can be set via device management related API functions. For more information about device management API functions, see ***document [3]*** and ***document [4].***

NOTE

The execution of **AT+CFUN** or related API functions will not affect GNSS function.

3.3. Power Supply

3.3.1. Power Supply Pins

The module provides 13 VBAT pins for connection with external power supplies. VBAT pins are separately used to supply power for two parts of the module.

- 10 VBAT_RF pins for module's RF part;
- 3 VBAT_BB pins for module's baseband part.

The following table shows the details of VBAT pins and ground pins.

Table 7: VBAT and GND Pins

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT_BB	241, 242, 244	PI	Power supply for the module's baseband part	3.3	3.8	4.3	V
VBAT_RF	109, 111, 112, 114, 235, 236, 238, 239, 404, 412	PI	Power supply for the module's RF part	3.3	3.8	4.3	V
GND	12, 18, 26, 33, 42, 86, 92, 98, 115, 117, 118, 120, 121, 124, 125, 126, 127, 128, 129, 130, 131, 133, 134, 135, 137, 138, 140, 141, 144, 145, 146, 147, 148, 149, 150, 151, 153, 155, 156, 158, 159, 160, 162, 164, 165, 167, 168, 171, 172, 173, 174, 176, 177, 180, 182, 183, 185, 186, 189, 191, 192, 194, 195, 198, 199, 201, 202, 203, 206, 208, 209, 211, 212, 215, 217, 218, 220, 221, 230, 232, 233, 234, 237, 240, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 403, 405, 406, 407, 408, 409, 410, 411, 413, 414				

3.3.2. Voltage Stability Requirements

The power supply range of VBAT_BB and VBAT_RF is from 3.3 V to 4.3 V. Ensure that the input voltage of VBAT_BB and VBAT_RF will never drop below 3.3 V. The following figure shows the voltage drop during burst transmission in GSM and 5G (NSA) networks. The voltage drop will be less in 3G, 4G and 5G (SA) networks.

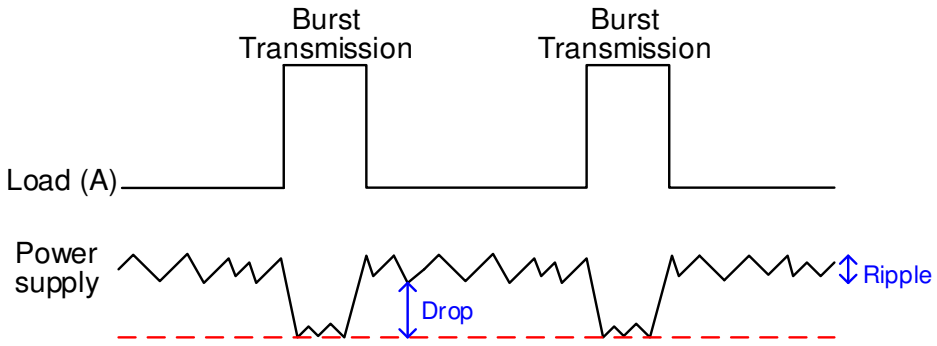


Figure 5: Power Supply Limits During Burst Transmission

To decrease voltage drop, use three groups of at least 100 µF + 47 µF bypass capacitors with low ESR for VBAT_BB and VBAT_RF, and reserve multi-layer ceramic chip capacitor (MLCC) array due to their low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT pins. While connecting the module to an external 3.8 V power supply, route VBAT_BB and VBAT_RF traces in star structure. The width of VBAT_BB trace should be not less than 1.5 mm. The width of VBAT_RF trace should be not less than 3 mm for the main power trace and 2 mm for the branch power trace. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to get a stable power source, it is suggested to use high power TVS component to prevent static electricity, and place them as close to the VBAT pins as possible. The following figure shows a reference design of VBAT power supply pins.

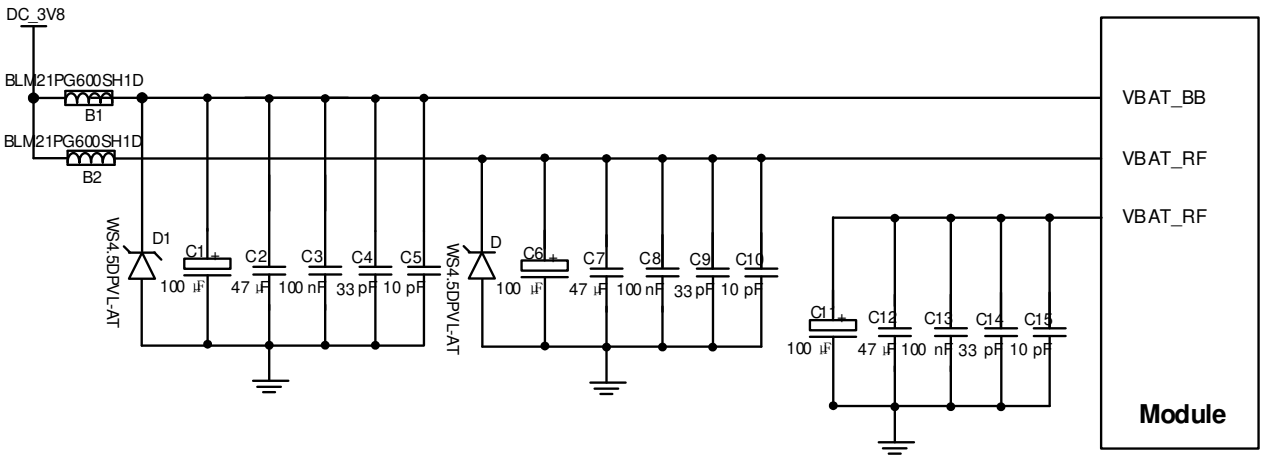


Figure 6: Power Supply Design

3.3.3. Reference Design for Power Supply

The performance of the module largely depends on the power source. If the voltage drop between the input and output is not too high, it is recommended to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +12/+24 V input power source. The designed output for the power supply is about 3.8 V and the maximum rated current is 5 A.

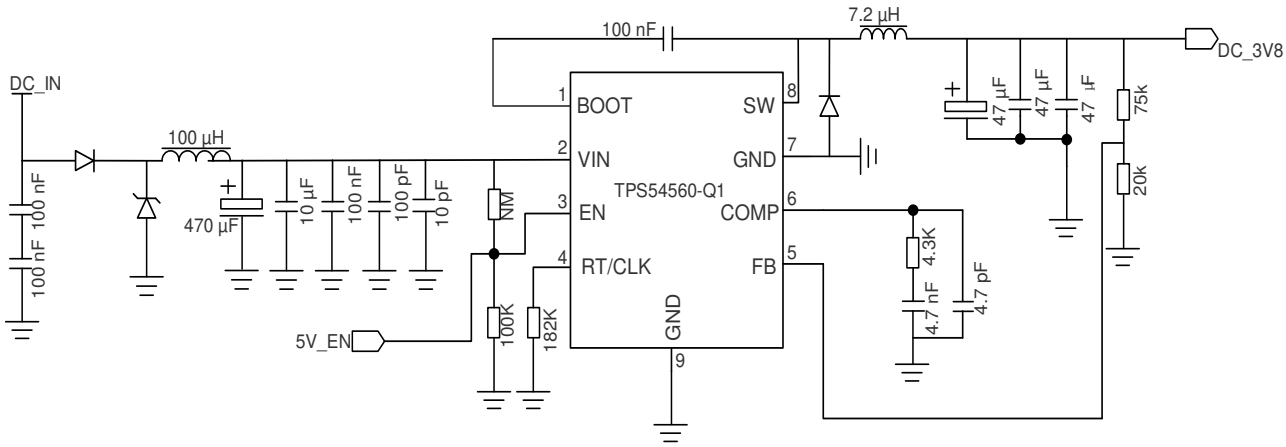


Figure 7: +12/+24 V Power Supply System Reference Design

NOTE

To avoid corrupting the data of internal flash, do not switch off the power supply when the module works

normally. Only after the module is turned off by PWRKEY or Linux commands, the power supply can be cut off.

3.3.4. Power Supply Monitoring

API can be used to monitor the VBAT_BB voltage value. For more details, see ***document [3]*** or ***document [4].***

3.4. Turn On

3.4.1. Turn On with PWRKEY

Table 8: PWRKEY Pin Description

Pin Name	Pin No.	Description	Comment
PWRKEY	7	Turn on/off the module	Internally pulled up to 1.8 V. Active LOW. The output voltage is about 1.1 V because of the diode drop in the baseband chipset.

When the module is in power-off mode, it can be turned on by driving PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY.

A simple reference circuit is illustrated in the following figure.

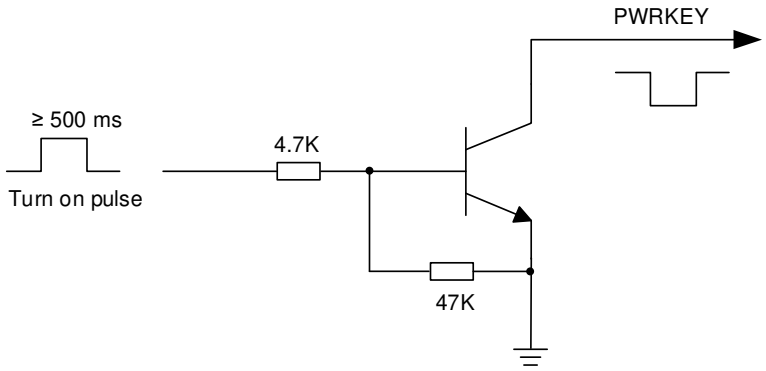


Figure 8: Turn On the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the button, electrostatic strike may generate from the fingers. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

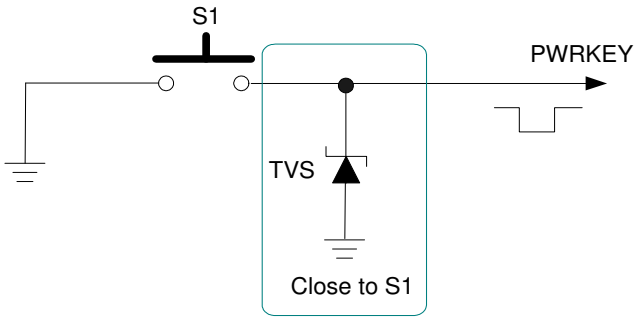


Figure 9: Turn On the Module Using a Button

The power-up timing is illustrated in the following figure.

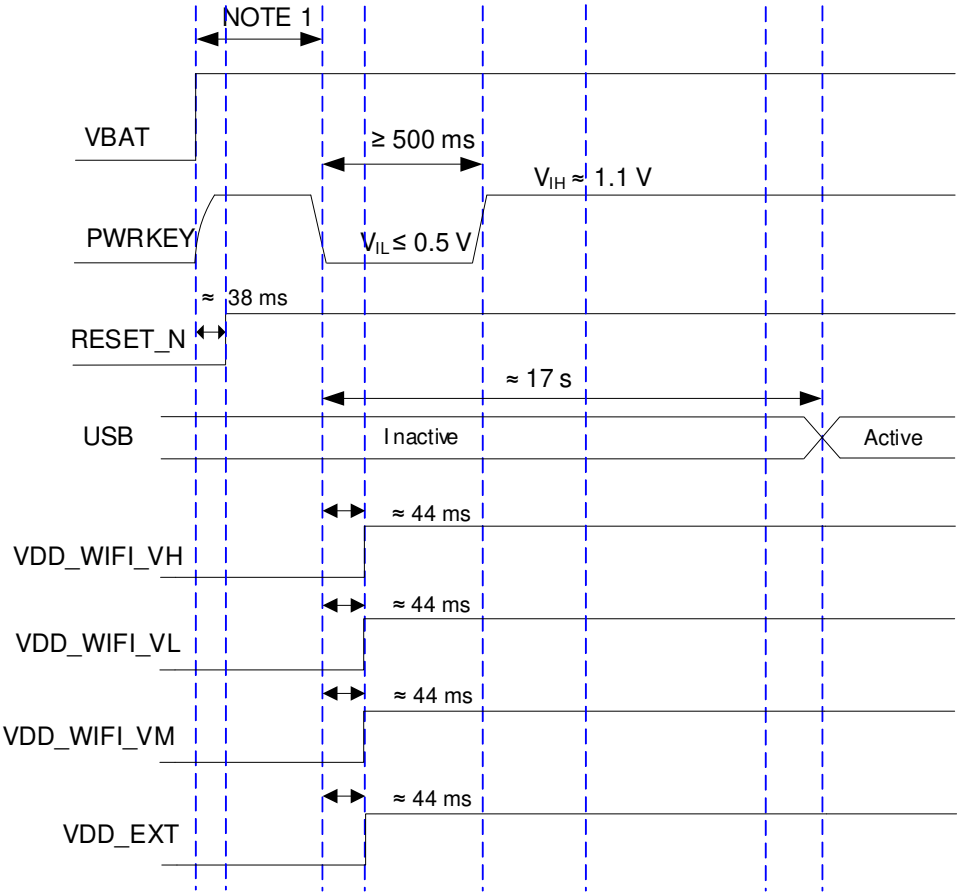


Figure 10: Power-up Timing

NOTE

1. Ensure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin is not less than 50 ms.
2. The RESET_N will be pulled high automatically when the voltage of VBAT is stable for about 38 ms, therefore, MCU does not need to control RESET_N in the power-up process.
3. It is recommended to use an external OD/OC circuit to control the PWRKEY pin.
4. Do not connect PWRKEY or RESET_N to GND permanently. Long press (≥ 16 s) of PWRKEY or RESET_N will trigger mandatory hardware reset.

3.4.2. Turn On with PON_1

The following table shows the pin definition of PON_1.

Table 9: Pin Definition of PON_1

Pin Name	Pin No.	I/O	Description	Comment
PON_1	248	DI	Drive HIGH to initiate power on	PON_1 is a high voltage tolerant pin up to VBAT_BB domain, therefore it can be pulled up to VBAT_BB, or an external 1.8 V power supply.

Connecting PON_1 to VBAT_BB or 1.8 V power supply through a serial resistor (10–100 kΩ) will enable the module to turn on automatically. A simple reference circuit is illustrated in the following figure.

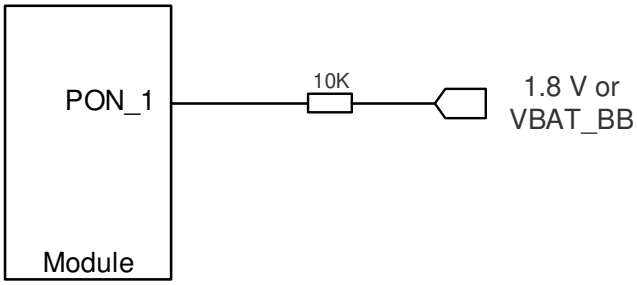


Figure 11: Turn On the Module Using PON_1

NOTE

If PON_1 is unused, it is recommended to connect it to GND via an external pull-down resistor (10–100 kΩ).

3.5. Turn Off

Any of the following methods can be used to turn off the module normally:

- Turn off the module using the PWRKEY pin.
- Turn off the module using Linux commands.

3.5.1. Turn Off with PWRKEY

Driving PWRKEY low for at least 2 s and then releasing it will enable the module to execute power-off procedure.

The power-down timing is illustrated in the following figure.

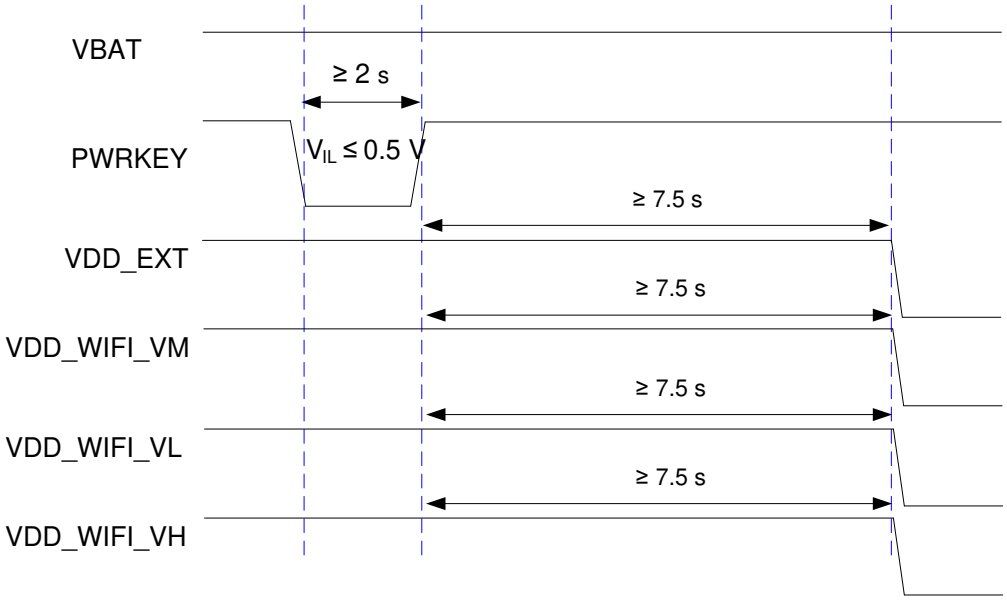


Figure 12: Power-down Timing

3.5.2. Turn Off with Linux Commands

It is also a safe way to use Linux commands, such as **shutdown** and **poweroff**, to turn off the module, which is similar to turning off the module via PWRKEY pin.

NOTE

1. To avoid corrupting the data of the internal flash, do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or Linux commands, the

power supply can be cut off.
2. When turn off module with Linux commands, keep PWRKEY at high level after the execution of power off command. Otherwise, the module will be turned on again after successfully turn-off.

3.6. Reset

The module can be reset by driving RESET_N low for 250–550 ms. As the RESET_N pin is sensitive to interference, the routing trace is recommended to be as short as possible and totally ground surrounded.

Table 10: Pin Definition of RESET_N

Pin Name	Pin No.	Description	Comment
RESET_N	8	Reset the module	Internally pulled up to 1.8 V. Active LOW. A test point is recommended to reserve if unused.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

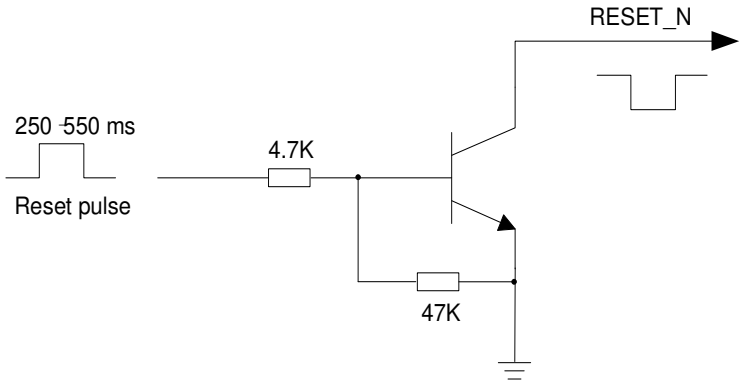


Figure 13: Reference Circuit of RESET_N by Using Driving Circuit

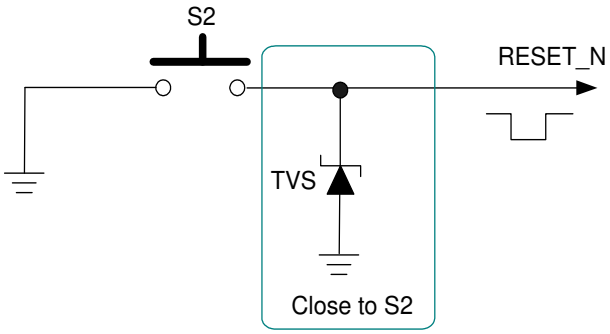


Figure 14: Reference Circuit of RESET_N by Using Button

The reset timing is illustrated in the following figure.

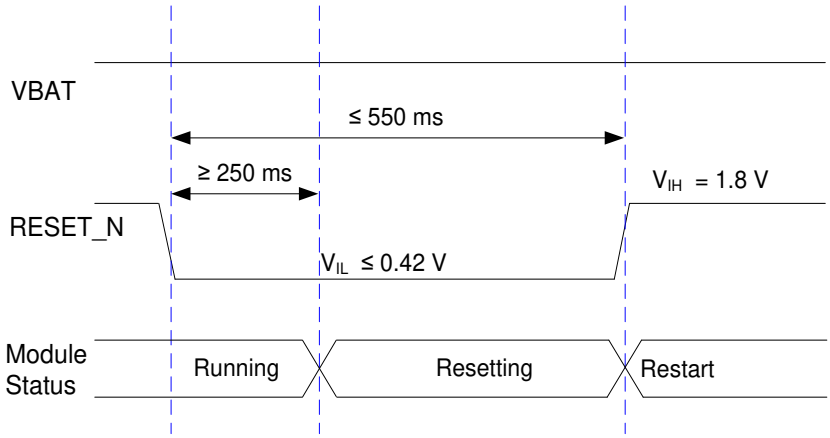


Figure 15: Reset Timing

NOTE

1. Ensure that there is no capacitance larger than 10 nF on PWRKEY and RESET_N pins.
2. RESET_N should only be used when failed to turn off the module by Linux commands and PWRKEY pin.

4 Application Interfaces

4.1. (U)SIM Interfaces

The (U)SIM interfaces circuitry meet ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported. The module supports dual (U)SIM cards, and (U)SIM1 is the primary interface.

Table 11: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	251	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	254	DIO	(U)SIM1 card data	
USIM1_CLK	253	DO	(U)SIM1 card clock	
USIM1_RST	250	DO	(U)SIM1 card reset	
USIM1_DET	255	DI	(U)SIM1 card hot-plug detect	
USIM2_VDD	256	PO	(U)SIM2 card power supply	
USIM2_DATA	257	DIO	(U)SIM2 card data	
USIM2_CLK	259	DO	(U)SIM2 card clock	
USIM2_RST	260	DO	(U)SIM2 card reset	
USIM2_DET	258	DI	(U)SIM2 card hot-plug detect	

The module supports (U)SIM card hot-plug via USIM_DET pins, and either low-level or high-level detection is supported. The function is disabled by default, and can be enabled by related software command. See ***document [5]*** for more details of the command.

The following figure shows a reference design for (U)SIM interfaces with an 8-pin (U)SIM card connector.

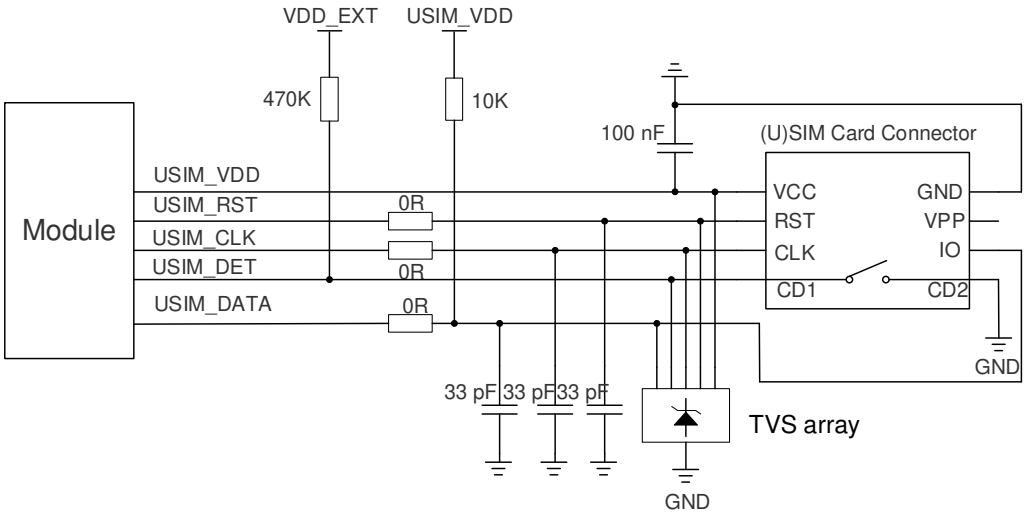


Figure 16: Reference Design of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_DET disconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

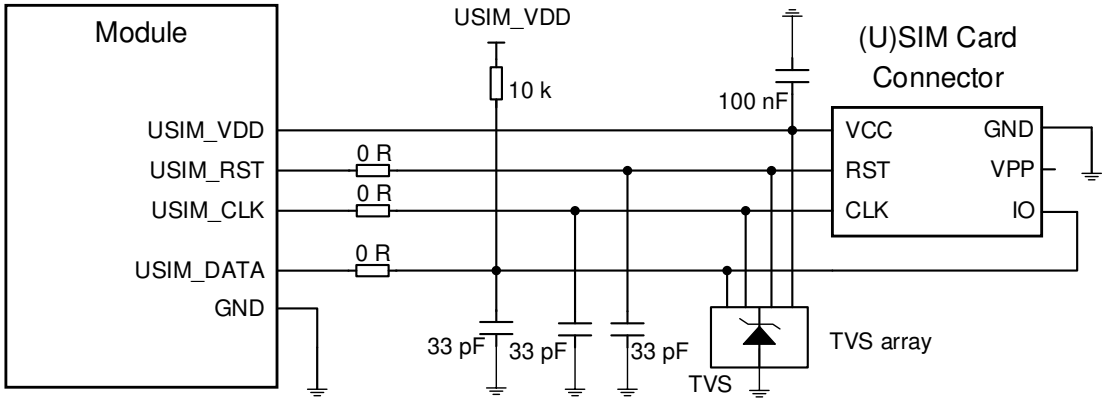


Figure 17: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in the (U)SIM circuit design:

- Keep the placement of (U)SIM card connector as close to the module as possible. Keep the trace length short, at most 200 mm.
- Keep (U)SIM card signals away from RF and power supply traces.
- Assure the trace between the ground of the module and that of the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD not less than 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.

- To offer good ESD protection, it is recommended to add a TVS array with parasitic capacitance not exceeding 10 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card connector to suppress EMI spurious transmission and enhance ESD protection. The 33 pF capacitors are used for RF filtering interference. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The USIM_DATA **MUST** be connected to USIM_VDD with a 10 kΩ pull-up resistor. The pull-up resistor can improve anti-jamming capability when long layout trace and sensitive occasions are applied, and should be placed close to the (U)SIM card connector.

NOTE

The load capacitance of (U)SIM interface will affect the rising and falling time of the data exchange.

4.2. USB Interfaces

The module provides one USB interface. The USB interface complies with the USB 3.1 Gen 2 and USB 2.0 specifications, and supports SuperSpeed (10 Gbps) on USB 3.1, high-speed (480 Mbps) and full-speed (12 Mbps) on USB 2.0.

Both USB 2.0 and USB 3.1 can be used for AT command communication, data transmission, GNSS NMEA sentences output and software debugging.

Only USB 2.0 can be used for firmware upgrade. The USB 3.1 interface can be used for data communication with an external AP.

USB 2.0 and USB 3.1 share the same hardware controller, so USB 2.0 and USB 3.1 cannot be used simultaneously. When USB 2.0 and USB 3.1 are connected to the same host, USB 3.1 takes effect by default.

The following table shows the pin definition of USB interface.

Table 12: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	84	DI	USB connection detect	
USB_DP	85	AIO	USB 2.0 differential data (+)	Compliant with USB 2.0 standard specification. Require differential impedance of 90 Ω.
USB_DM	87	AIO	USB 2.0 differential data (-)	

USB_SS_TX_P	93	AO	USB 3.1 SuperSpeed transmit (+)	Compliant with USB 3.1 standard specifications. Require differential impedance range of 70–100 Ω and 85 Ω is recommended.
USB_SS_TX_M	91	AO	USB 3.1 SuperSpeed transmit (-)	
USB_SS_RX_P	90	AI	USB 3.1 SuperSpeed receive (+)	
USB_SS_RX_M	88	AI	USB 3.1 SuperSpeed receive (-)	

For more details about USB 2.0 specification, visit http://www.usb.org/home.

It is recommended to reserve USB 2.0 for firmware upgrade in application design, and reserve test points for debugging purpose. The following figure is the reference circuit of USB 2.0 interface.

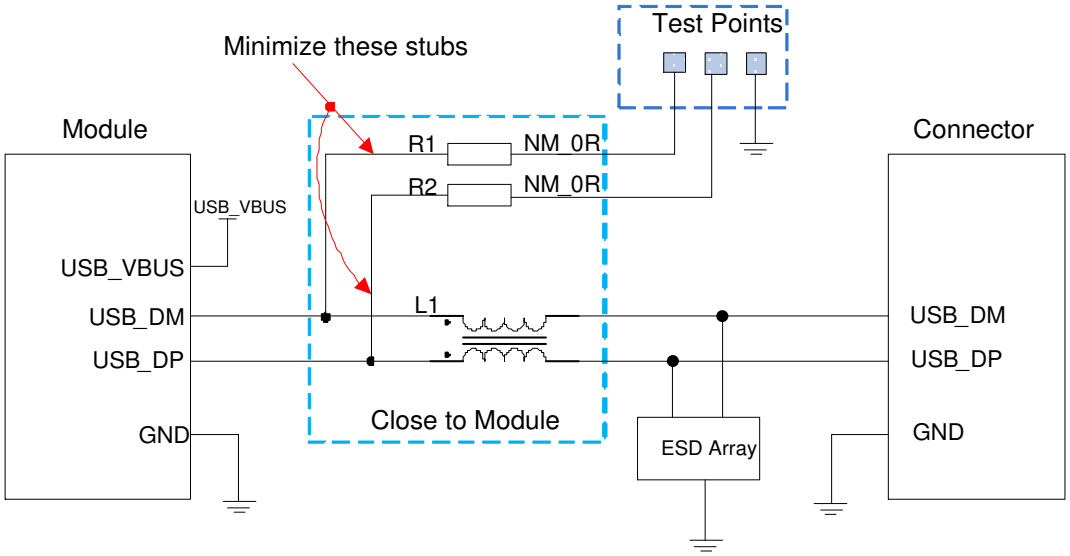


Figure 18: Reference Circuit of USB 2.0 Application

In USB 2.0 applications, a common mode choke L1 is recommended to be added in series between the module and MCU to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points to facilitate debugging, and the resistors are not mounted by default. To ensure signal integrity of USB data traces, place R1, R2 and L1 close to the module, and place these resistors close to each other. The extra stubs of trace must be as short as possible.

To meet USB 2.0 specifications, the following principles of USB interface should be complied with.

- It is important to route the USB 2.0 as differential pairs with total grounding. The USB differential impedance is 90 Ω.
- The length of each trace in USB 2.0 differential pair should be less than 120 mm.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces.

It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.

- Keep the ESD protection devices as close to the USB connector as possible. Junction capacitance of the ESD protection components might cause influences on USB data traces, so you should pay attention to the selection of the device. Typically, the capacitance value should be less than 2.0 pF for USB 2.0.

NOTE

The module supports master mode for USB 2.0, but works in slave mode by default.

4.3. UART Interfaces

The module provides three UART interfaces: main UART and debug UART. The following are the features of these UART interfaces.

- The main UART can be used for data transmission with peripherals. 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800 and 921600 bps baud rates are supported, and the default is 115200 bps.
- The debug UART interface supports 115200 bps baud rate, and is used for Linux console and log output.

Table 13: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
UART1_TXD	70	DO	UART1 transmit	1.8 V power domain. If unused, keep them open.
UART1_RXD	72	DI	UART1 receive	

Table 14: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	107	DO	Debug UART transmit	1.8 V power domain. It is recommended to reserve test points for debug UART.
DBG_RXD	110	DI	Debug UART receive	

The module provides 1.8 V UART interfaces. A voltage-level translator should be used if your application is equipped with a 3.3 V UART interface. It is recommended that the enable pin of the voltage-level translator is controlled by VDD_EXT to eliminate the possible influence of current sinking from its internal circuits (e.g. pull-ups) into the module.

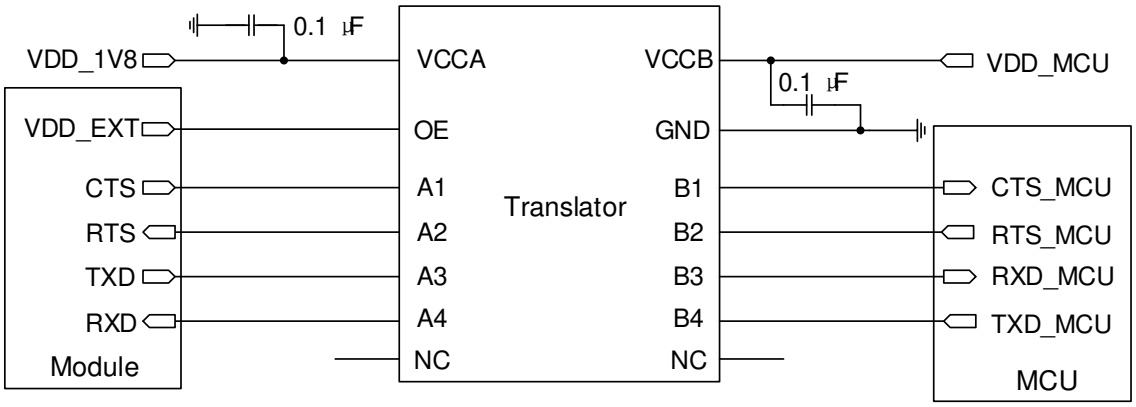


Figure 19: Reference Circuit of UART Interface with Translator Chip

Another example with transistor translation circuit is shown as below. The circuit design of dotted line section can refer to the design of solid line section, in terms of both module input and output circuit designs, but pay attention to the direction of connection.

Please ensure the VDD_1V8 are not powered earlier than VDD_EXT, otherwise the pull-ups may influence the module normal operation.

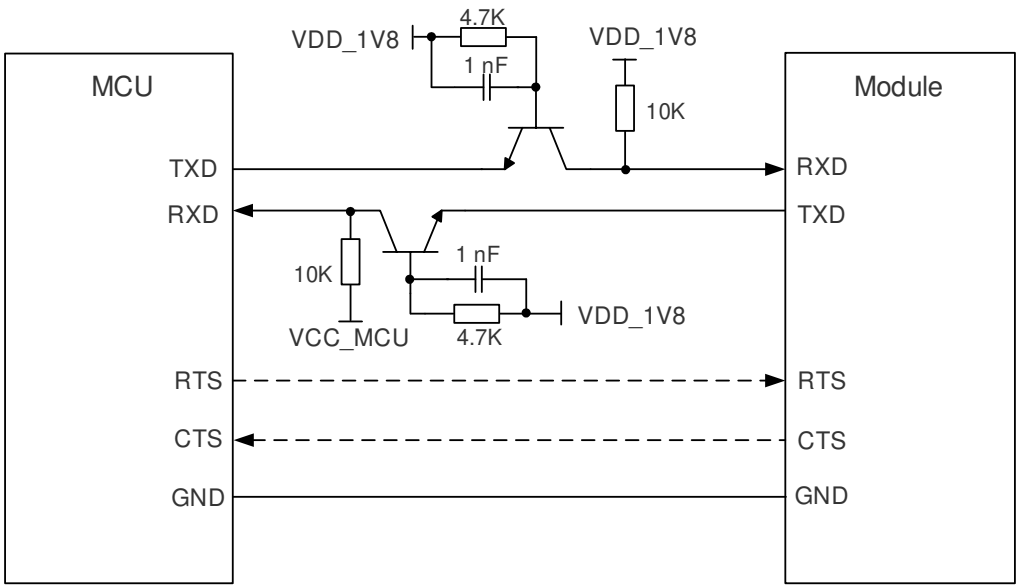


Figure 20: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. When the module enters sleep mode, it is recommended to switch off the power supply for VDD_1V8 to reduce power consumption.
3. If hardware flow control is intended to be used, then CTS and RTS should also be designed with the level shifting circuit.

4.4. I2S and I2C Interfaces

The module provides I2S and I2C interfaces for audio function design.

Table 15: Pin Definition of I2S Interface

Pin Name	Pin No.	I/O	Description	Comment
I2S_MCLK	81	DO	Clock output for codec	1.8 V power domain. 12.288 MHz clock output.
I2S_WS	73	DIO	I2S word select	1.8 V power domain. Serve as output signals in master mode. Serve as input signals in slave mode.
I2S_SCK	75	DIO	I2S clock	
I2S_DIN	76	DI	I2S data in	If unused, keep them open.
I2S_DOUT	78	DO	I2S data out	
CDC_RST_N	77	DO	External codec reset	

Table 16: Pin Definition of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C1_SCL	79	OD	I2C serial clock	External pull-up resistors are required. If unused, keep them open.
I2C1_SDA	80	OD	I2C serial data	

The following figure shows a reference design of I2S and I2C interfaces with an external codec IC.

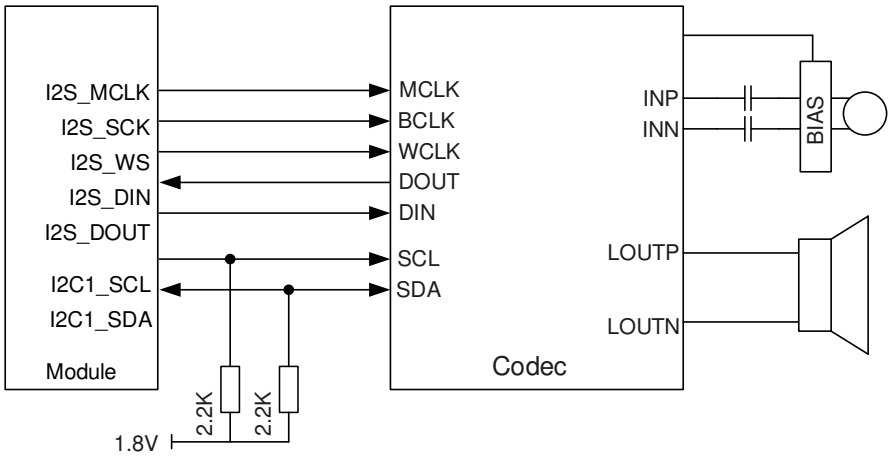


Figure 21: Reference Circuit of I2S and I2C1 Application with Audio Codec

NOTE

1. It is recommended to reserve an RC circuit on the I2S signal traces, especially for I2S_SCK and I2S_MCLK.
2. The module works as a master device in applications pertaining to I2C interface.
3. It is recommended to use 1.8 V VDD_EXT. If the external 1.8 V power supply is used, make sure it powers on later than VDD_EXT.

4.5. PCM Interface

The module provides one PCM interface. PCM function is not available by default due to 2nd NAND occupation. See ***Chapter*** *错误!未找到引用源。***.**

The PCM interface supports the following modes:

- Short frame synchronization
- Long frame synchronization

Table 17: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	265	DIO	PCM data frame sync	1.8 V power domain. Serve as output signals in master mode. Serve as input signals in slave mode.
PCM_CLK	262	DIO	PCM clock	

PCM_IN	263	DI	PCM data input	1.8 V power domain. This pin is used as GPIO to detect the chip select signal of the NAND by default. If unused, keep it open.
PCM_OUT	261	DO	PCM data output	If unused, keep it open.

The module supports 16-bit linear data format. The following figures show the short frame sync mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the long frame sync mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

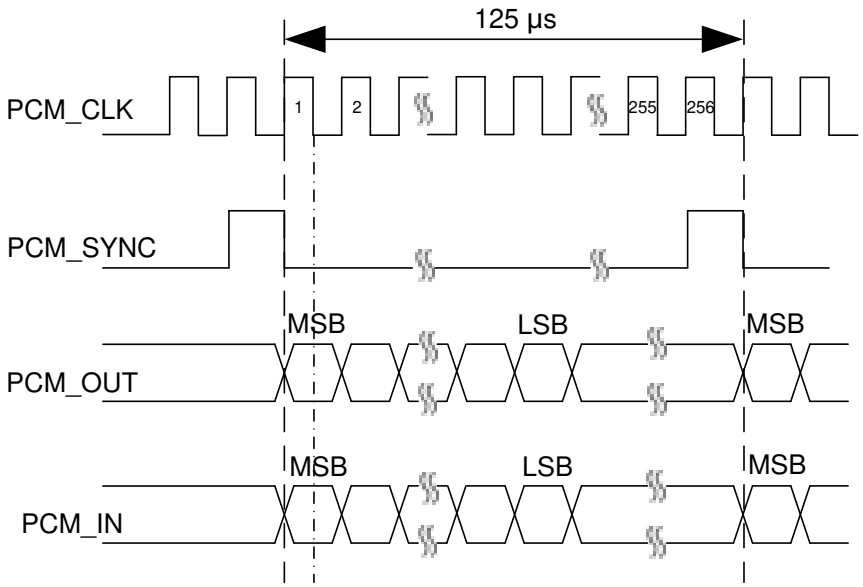


Figure 22: Short Frame Sync Mode Timing

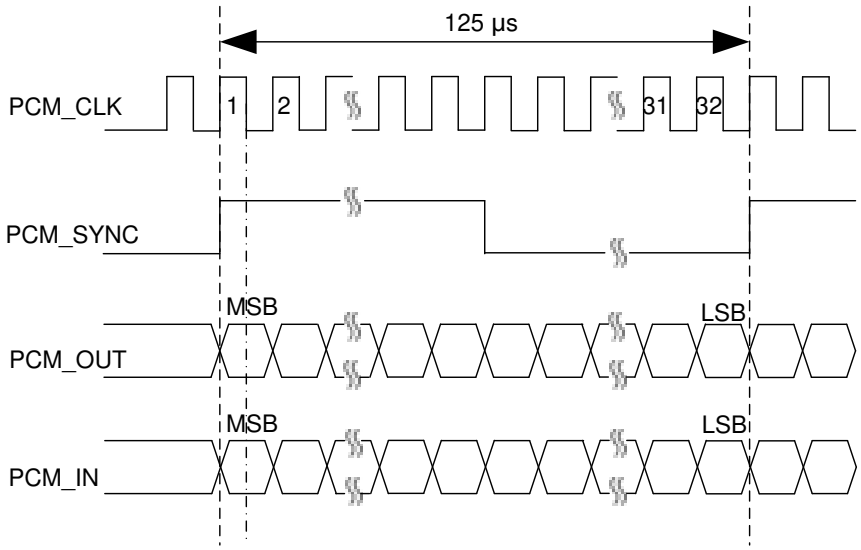


Figure 23: Long Frame Sync Mode Timing

Clock and mode can be configured, and the default configuration is master mode using short frame sync format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC.

NOTE

1. PCM is not available by default due to 2nd NAND occupation.

4.6. SDIO Interface

The module provides one SDIO interface. It is recommended to use the interface for eMMC application.

Table 18: Pin Definition of SDIO Interface

Pin Name	Pin No.	I/O	Description	Comment
SDIO_VDD	60	PI	SDIO power supply	Connect to external 1.8 V LDO in eMMC application. If SDIO interface is not used, connect this pin to VDD_EXT.

SDC1_DATA_0	49	DIO	SDIO data bit 0	1.8 V power domain. If unused, keep them open.
SDC1_DATA_1	50	DIO	SDIO data bit 1	
SDC1_DATA_2	51	DIO	SDIO data bit 2	
SDC1_DATA_3	52	DIO	SDIO data bit 3	
SDC1_CMD	48	DIO	SDIO command	
SDC1_DATA_4	53	DIO	SDIO data bit 4	Used as general GPIO by default.
SDC1_DATA_5	55	DIO	SDIO data bit 5	Used as general GPIO by default.
SDC1_DATA_6	56	DIO	SDIO data bit 6	Used as BOOT_STS_0 to indicate module boot status by default.
SDC1_DATA_7	58	DIO	SDIO data bit 7	Used as BOOT_STS_1 to indicate module boot status by default.
SDC1_CLK	47	DO	SDIO clock	If unused, keep these pins open.
EMMC_RST_N*	54	DO	eMMC reset	
EMMC_PWR_EN	45	DO	eMMC power supply enable control	

The following is a reference design of SDIO interface for eMMC application.

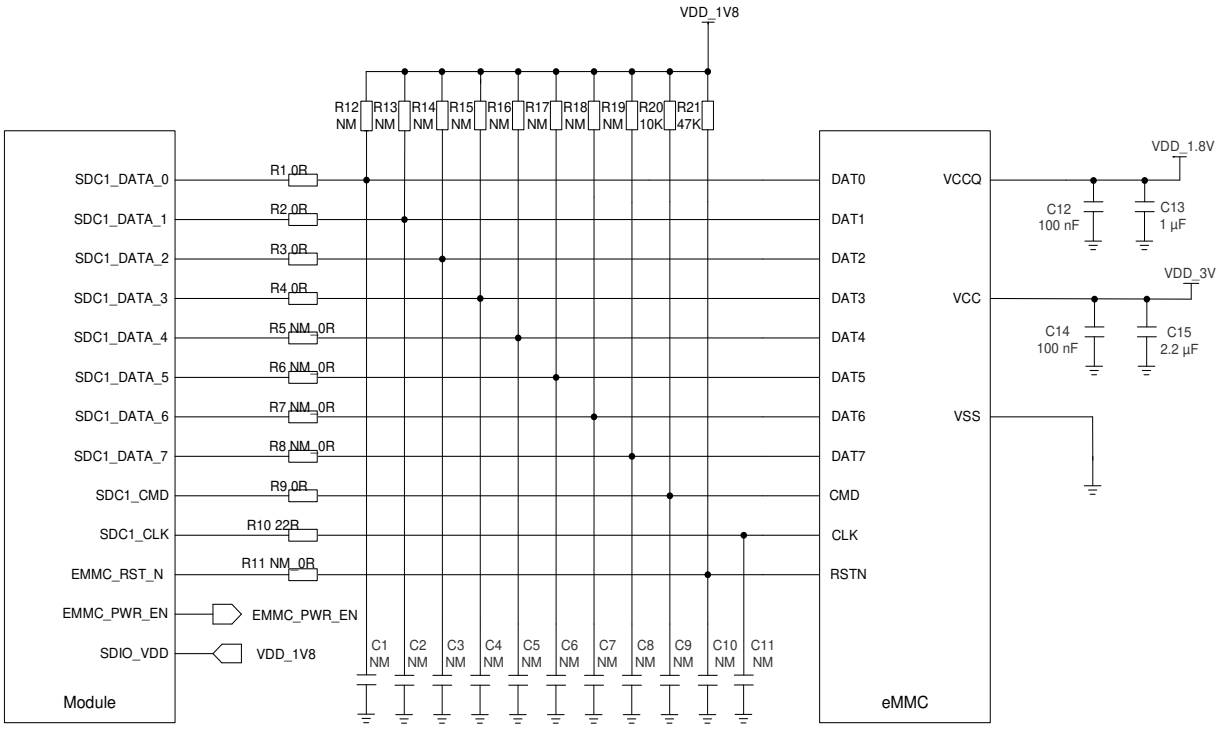


Figure 24: Reference Design of SDIO Interface for eMMC Application

Follow the principles below in eMMC circuit design:

- To avoid jitter of bus, it is recommended to reserve R12–R19 (10–100 kΩ) to pull up SDIO signals to an external 1.8 V LDO. The resistors are not mounted by default, and the recommended value is 100 kΩ.
- To improve signal quality, it is recommended to add resistors R1–R10 in series between the module and eMMC. Resistor R10 should be 20–30 Ω and the other resistors are 0 Ω by default. The bypass capacitors C1–C11 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50 Ω (±10 %).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is recommended to keep the trace length difference between SDC1_CLK and SDC1_DATA_[0:7]/SDC1_CMD less than 1 mm and the total routing length less than 50 mm. The total trace length inside the module is 17 mm, so the exterior total trace length should be less than 33 mm.
- Keep the spacing between SDIO and other signal traces at least twice the trace width and the load capacitance of SDIO bus less than 40 pF.

4.7. SPI Interfaces

The module provides two SPI interfaces by default, which only support master mode. The maximum clock frequency of SPI is up to 50 MHz. SPI2 interface can be multiplexed into I2C2 interface, and see ***document [1]*** for more details.

Table 19: Pin Definition of SPI Interfaces

Pin Name	Pin No.	I/O	Description	Comment
SPI1_CLK	216	DO	SPI1 clock	1.8 V power domain. Support master mode only. If unused, keep them open. Can be configured to GPIOs
SPI1_CS	213	DO	SPI1 chip select	
SPI1_MISO	219	DI	SPI1 master-in slave-out	
SPI1_MOSI	210	DO	SPI1 master-out slave-in	
SPI2_CLK	103	DO	SPI2 clock	

SPI2_CS	105	DO	SPI2 chip select
SPI2_MISO	106	DI	SPI2 master-in slave-out
SPI2_MOSI	108	DO	SPI2 master-out slave-in

The following figure shows the timing relationship of SPI interfaces. The related parameters of SPI timing are shown in the table below.

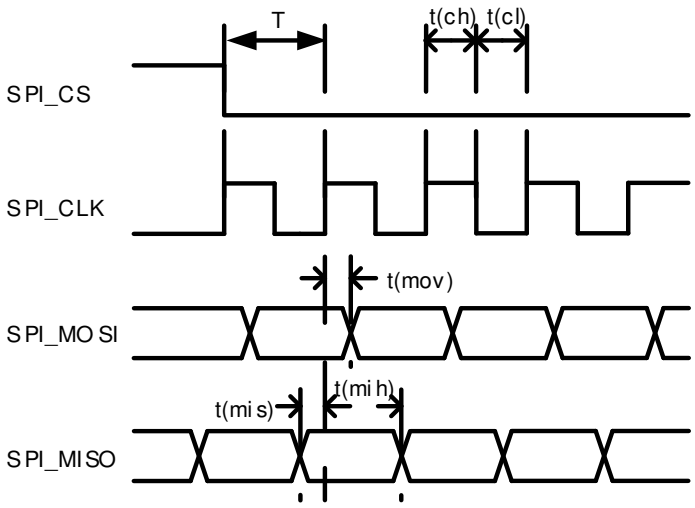


Figure 25: SPI Timing

Table 20: Parameters of SPI Interface Timing

Parameter	Description	Min.	Typ.	Max.	Unit
T	SPI clock period	20.0	-	-	ns
t(ch)	SPI clock high-level time	8.0	-	-	ns
t(cl)	SPI clock low-level time	8.0	-	-	ns
t(mov)	SPI master data output valid time	-5.0	-	5.0	ns
t(mis)	SPI master data input setup time	5.0	-	-	ns
t(mih)	SPI master data input hold time	1.0	-	-	ns

NOTE

The module provides 1.8 V SPI interfaces. A voltage-level translator should be used between the module and the host if the application is equipped with a 3.3 V processor or device interface.

4.8. RGMII Interface

The module includes an integrated Ethernet MAC with a RGMII interface which also supports EAVB. Key features of the RGMII interface are shown below:

- IEEE 802.3 compliant
- Support 10/100/1000 Mbps operation [9]
- Support protocols such as IEEE 1722.A (AVTP), 802.1Qav (FQTSS), 802.1Qat (SRP), 802.1AS (gPTP)
- Support connection to an external Ethernet PHY like Marvell 88Q2112, or an external Ethernet switch
- Support 1.8/2.5 V I/O standards

The following table shows the pin definition of RGMII interface.

Table 21: Pin Definition of RGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
RGMII_MD_IO	10	DIO	RGMII management data	Add a pull-up resistor to this pin, and place the resistor close to the external PHY end. The power domain depends on RGMII_PWR_IN.
RGMII_MD_CLK	11	DO	RGMII management clock	Do not add any pull-up resistor to this pin, otherwise it may cause higher current consumption during sleep mode. The power domain depends on RGMII_PWR_IN.
RGMII_RX_0	13	DI	RGMII receive data bit 0	The power domain depends on RGMII_PWR_IN. Typ.1.8/2.5 V, and 1.8 V is recommended. The single-ended impedance
RGMII_RX_1	14	DI	RGMII receive data bit 1	
RGMII_CTL_RX	15	DI	RGMII receive control	

[9] The module's RGMII interface supports the Gigabit Ethernet protocol, while actual throughput is subject to testing.

RGMII_RX_2	16	DI	RGMII receive data bit 2	requires 50 Ω.
RGMII_RX_3	17	DI	RGMII receive data bit 3	
RGMII_CK_RX	19	DI	RGMII receive clock	
RGMII_TX_0	20	DO	RGMII transmit data bit 0	
RGMII_CTL_TX	21	DO	RGMII transmit control	
RGMII_TX_1	22	DO	RGMII transmit data bit 1	
RGMII_TX_2	23	DO	RGMII transmit data bit 2	
RGMII_CK_TX	24	DO	RGMII transmit clock	
RGMII_TX_3	25	DO	RGMII transmit data bit 3	
RGMII_PWR_EN	27	DO	Enable external LDO to supply power to RGMII_PWR_IN	1.8 V power domain
RGMII_INT	29	DI	RGMII PHY interrupt output	
RGMII_RST_N	31	DO	Reset output for RGMII PHY	
RGMII_PWR_IN	28	PI	Power input for internal RGMII circuit	An external power LDO is required to power this pin. Max. 100 mA in operating current. If RGMII interface is not used, connect this pin to VDD_EXT.

The following figure shows the simplified block diagram for Ethernet application.

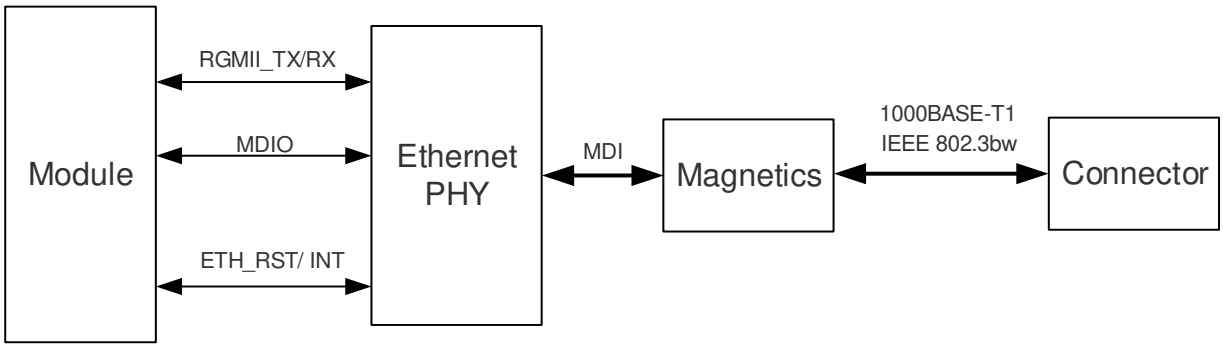


Figure 26: Simplified Block Diagram for Ethernet Application

The following figure shows a reference design of RGMII interface with PHY application. For more details, see ***document [7].***

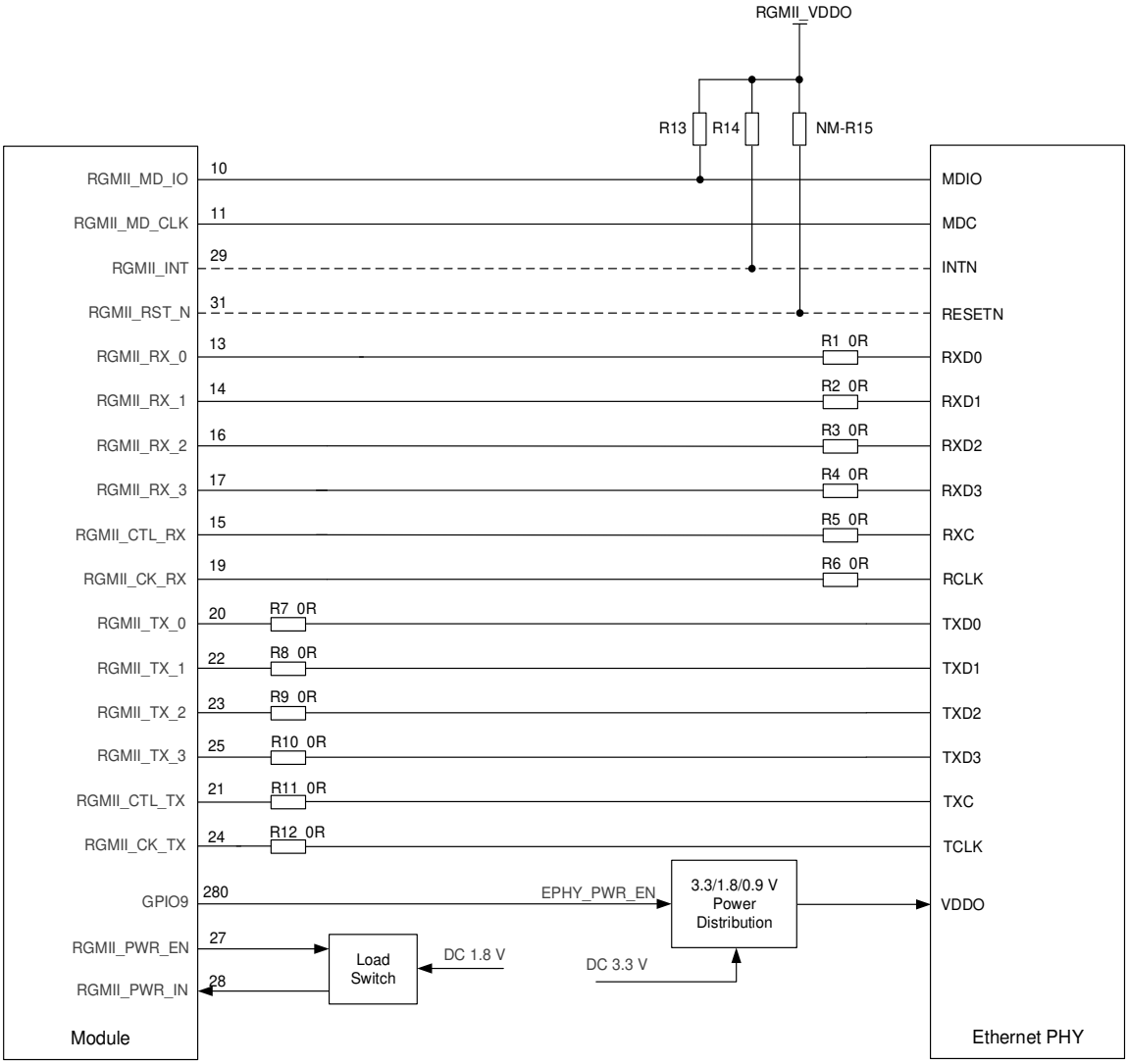


Figure 27: Reference Circuit of RGMII Interface with PHY Application

To enhance the reliability and availability of application designs, follow the criteria below in the Ethernet PHY circuit design:

- Keep RGMII data and control signals away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- The single-ended impedance of RGMII data traces is 50 Ω ±20 %.
- The length matching between Tx signals (RGMII_CK_TX, RGMII_CTL_TX and RGMII_TX_[0:3]) or Rx signals (RGMII_CK_RX, RGMII_CTL_RX and RGMII_RX_[0:3]) is less than 2 mm.
- Keep the spacing between Tx bus traces (RGMII_CK_TX to RGMII_TX_[0:3]/RGMII_CTL_TX) or that between Rx bus traces (RGMII_CK_RX to RGMII_RX_[0:3]/RGMII_CTL_RX) at least 2 times the trace width.
- Keep the spacing between Tx bus and Rx bus traces at least 2.5 times trace width.
- Keep the spacing between RGMII and other signal traces at least 3 times trace width.
- Resistors R7–R12 should be placed near the module. Resistors R1–R6 should be placed near the

Ethernet PHY. The value of R1–R15 varies with the selection of PHY.

- RGMII_INT and RGMII_RST_N are always 1.8 V power domain. A voltage-level translator should be used when module I/O level does not match with PHY.

4.9. PCIe Interface

The module provides one PCIe 3.0 interface. See ***Chapter*** *错误!未找到引用源。* for more details.

- The PCIe interface works in RC mode by default
- Compliant with *PCI Express Base Specification Revision 3.0*
- Maximum rate: 8 GT/s × 1-lane
- Backward compatible

Table 22: Pin Definition of PCIe Interface

Pin Name	Pin No.	I/O	Description	Comment
PCIE_REFCLK_P	40	AIO	PCIe reference clock (+)	Serve as output signals in RC mode. Serve as input signals in EP mode.
PCIE_REFCLK_M	38	AIO	PCIe reference clock (-)	The differential impedance should be the same as that for PCIe TX/RX. Require differential impedance of 70–100 Ω, and 85 Ω is recommended.
PCIE_TX_M	44	AO	PCIe transmit (-)	Require differential impedance of 70–100 Ω, and 85 Ω is recommended.
PCIE_TX_P	46	AO	PCIe transmit (+)	
PCIE_RX_M	32	AI	PCIe receive (-)	
PCIE_RX_P	34	AI	PCIe receive (+)	
PCIE_CLKREQ_N	36	DIO	PCIe clock request	Serve as input signals in RC mode. Serve as output signals in EP mode. Require a 100 kΩ pull-up to VDD_EXT.
PCIE_WAKE_N	30	DIO	PCIe wake up	
PCIE_RST_N	39	DIO	PCIe reset	Serves as an output signal in RC mode. Serves as an input signal in EP mode. 1.8 V power domain.

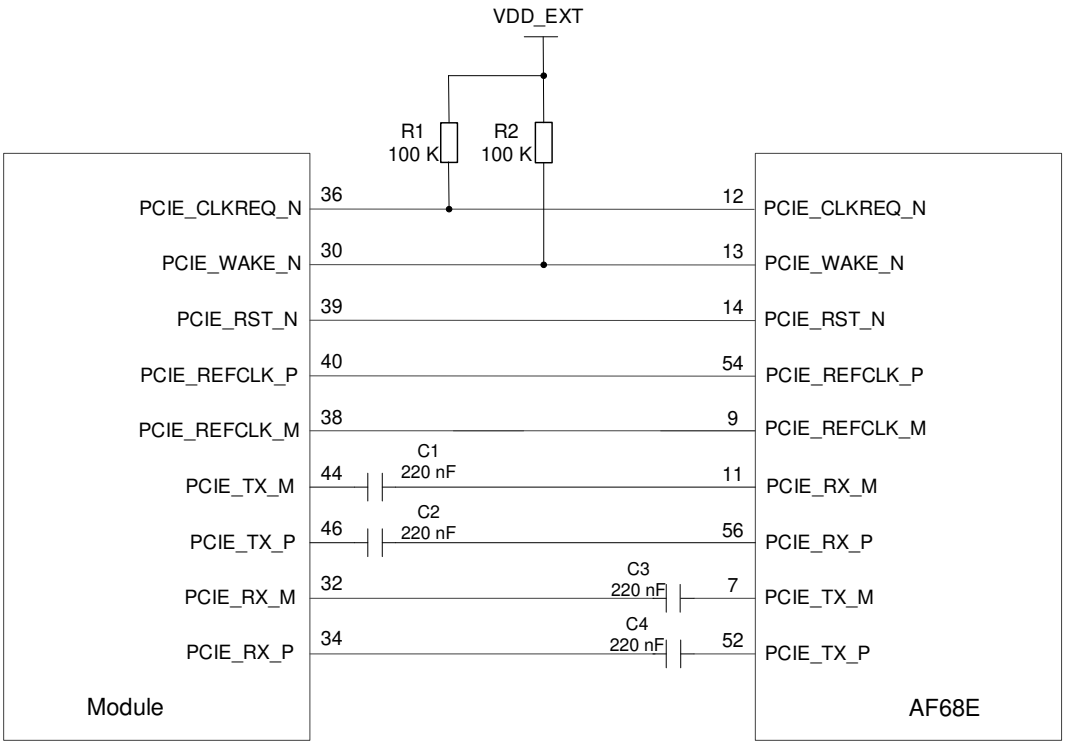


Figure 28: Reference Design of PCIe Interface

To ensure the signal integrity of PCIe interface, C1 and C2 should be placed close to the module. C3 and C4 should be placed close to the device. The extra stubs of trace must be as short as possible.

To meet PCIe specifications, the following principles of PCIe interface design should be complied with.

- It is important to route the PCIe signal traces as differential pairs with ground surrounded. The differential impedance is 70–100 Ω and 85 Ω is recommended.
- For PCIe signal traces, the maximum length of each differential data pair (PCIE_TX/PCIE_RX/ PCIE_REFCLK) is recommended to be less than 300 mm, and each differential data pair matching should be less than 0.7 mm (5 ps).
- Keep the spacing between lane-to-lane PCIe data signal traces four times trace width.
- Keep the spacing between PCIe signal trace and all other signals trace four times trace width.
- Do not route signal traces under crystals, oscillators, magnetic devices or RF signal traces. It is important to route the PCIe differential traces in inner-layer with ground planes above and below.

NOTE

It is recommended to pull up PCIE_CLKREQ_N and PCIE_WAKE_N to VDD_EXT with 100 kΩ resistors.

4.10. ADC Interfaces

The module provides 4 analog-to-digital converter (ADC) interfaces. The voltage value on ADC pins can be read via **AT+QADC=<port>**, through specifying **<port>** as 0, 1, 3, 4. For more details about the AT command, see ***document [8]***.

- **AT+QADC=0**: read the voltage value on ADC0
- **AT+QADC=1**: read the voltage value on ADC1
- **AT+QADC=3**: read the voltage value on ADC3
- **AT+QADC=4**: read the voltage value on ADC4

To improve the accuracy of ADC, the traces of ADC interfaces should be surrounded by ground.

Table 23: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description	Comment
ADC0	247	General purpose ADC interface	ADC0, 1, 3, 4 are used as internal antenna detection by default. General ADC function is required to change the module's BOM.
ADC1	245		
ADC3	291		
ADC4	290		

Table 24: Characteristic of ADC Interface

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0	-	1.875	V
ADC1 Voltage Range	0	-	1.875	V
ADC3 Voltage Range	0	-	1.875	V
ADC4 Voltage Range	0	-	1.875	V
ADC Resolution	-	15	-	bits
ADC Sample Rate	-	4.8	-	MHz

NOTE

1. The input voltage for each ADC interface must not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.

4.11. USB_BOOT Interface

The module provides a USB_BOOT pin. Pulling up the USB_BOOT to VDD_EXT before powering on the module will force the module into download mode when powered on. In forced download mode, the module supports firmware upgrade over USB 2.0 interface.

Table 25: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	83	DI	Force the module into download mode	1.8 V power domain. Active HIGH. It is recommended to reserve test points.

The following figure shows a reference circuit of USB_BOOT interface.

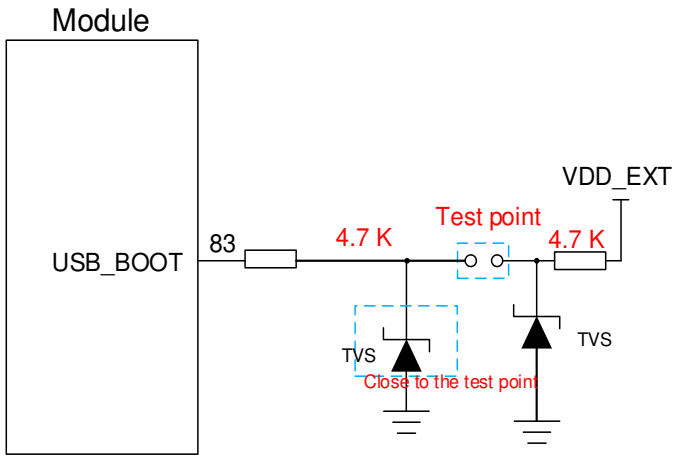


Figure 29: Reference Design of USB_BOOT Interface

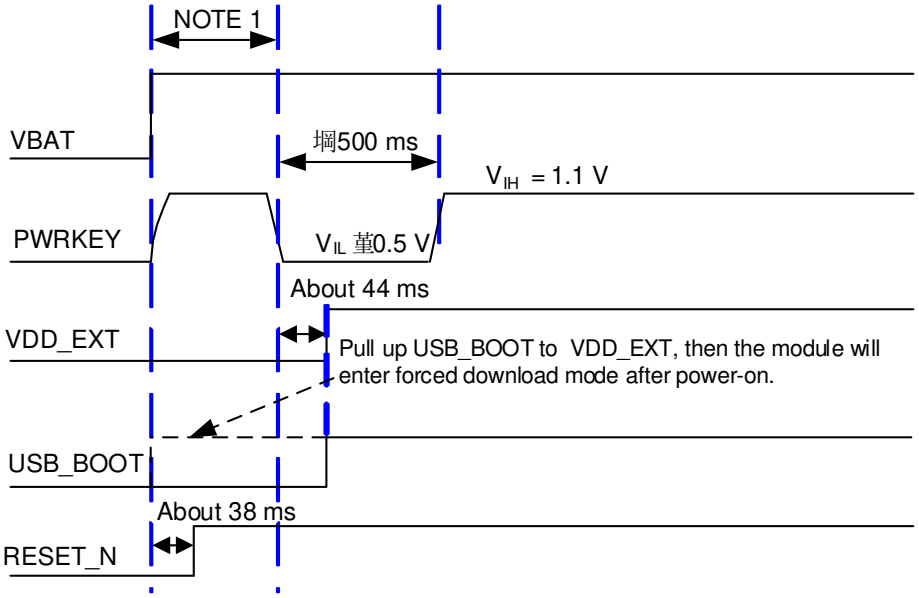


Figure 30: Reference Design of USB_BOOT Interface

NOTE

1. Ensure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin is not less than 30 ms.
2. When using MCU to control the module entering forced download mode, follow the above timing. Connecting the test points as shown in ***Figure 29*** can manually force the module into download mode.

4.12. RTC

The module has a real time clock within the PMIC, but has no dedicated RTC power supply pin. The RTC is powered by VBAT_BB. If VBAT_BB is removed, the RTC will not maintain. If RTC is needed, then VBAT_BB must be powered.

Table 26: RTC Performance Specification

Parameter	Test Condition	Max.	Unit
Accuracy	Power on	24	ppm
	Power down, but with power supply connected	600	ppm

4.13. GPIO Interfaces

The module provides 14 GPIOs.

Table 27: Pin Definition of GPIOs

Pin Name	Pin No.	I/O	Description	Comment
GPIO1	100	DIO	General-purpose input/output.	Support wake-up interrupt.
GPIO2	101	DIO		
GPIO3	102	DIO		
GPIO4	104	DIO		Support wake-up interrupt.
GPIO5	116	DIO		
GPIO6	243	DIO		GPIO6 is from internal PMIC, and it is only recommended to be used as an output signal.
GPIO7	246	DIO		
GPIO8	249	DIO		
GPIO9	280	DIO		
GPIO10	283	DIO		Support wake-up interrupt.
GPIO11	284	DIO		
GPIO12	289	DIO		
GPIO13	64	DIO		
GPIO14	264	DIO		Support wake-up interrupt.
GPIO15	267	DIO		

4.14. Recovery NAND Interface

The recovery NAND interface is used to control the internal 2nd NAND flash (recovery NAND). MCU can control the chip select signal to make the module boot from the recovery NAND mode when the module fails to boot from primary NAND mode.

Table 29: Pin Definition of Recovery NAND Interface

Pin Name	Pin No.	I/O	Description	Comment
NAND_CS_N	71	DI	NAND chip select	Low: primary NAND High: recovery NAND

Table 30: Pin Definition of NAND Control Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_IN	263	DI	Indicates the status of NAND	Pin 263 can be configured as GPIO to obtain the status of NAND_CS_N, the PCM function of this pin is not used by default.
SDC1_DATA_6	56	DO	Indicates the boot status 0	This pin can be configured as GPIO to indicate the boot status to MCU.
SDC1_DATA_7	58	DO	Indicates the boot status 1	This pin can be configured as GPIO to indicate the boot status to MCU.

The following figure shows a reference design of recovery NAND interface. For more details, see ***document [7]***.

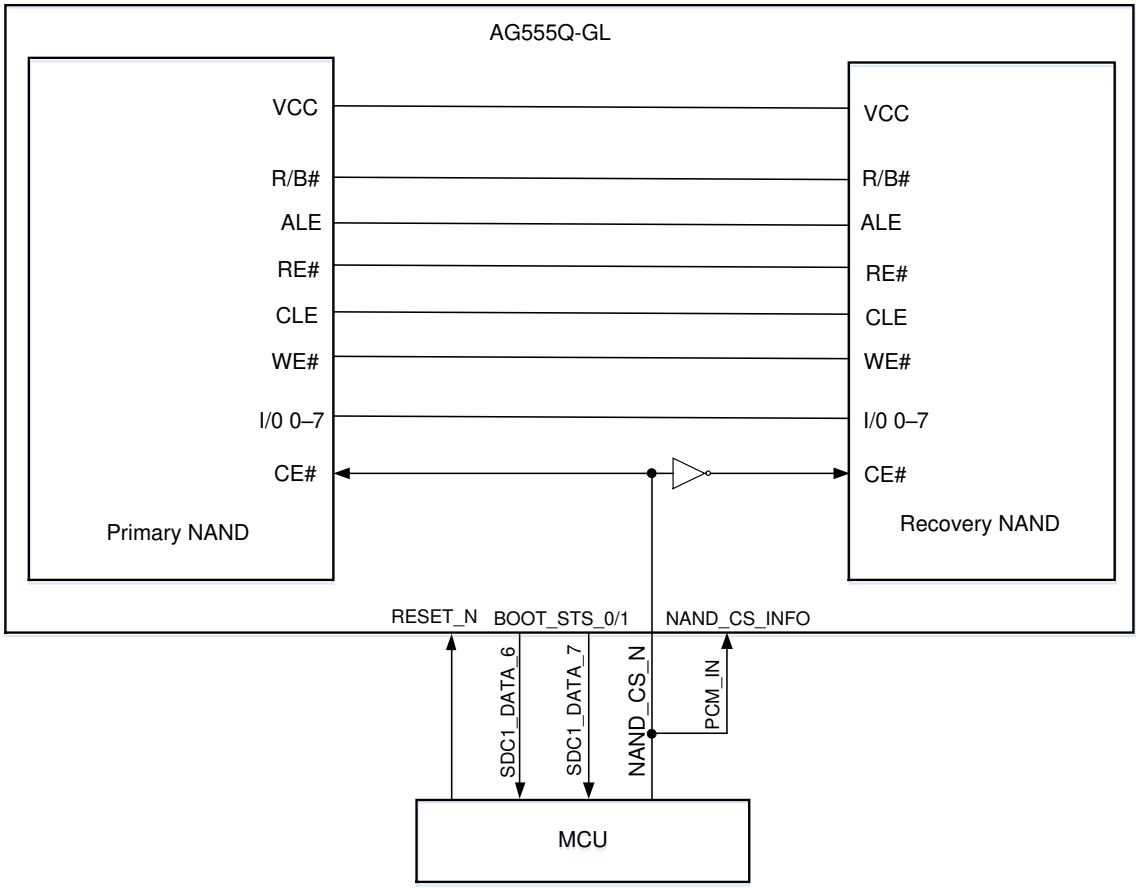


Figure 31: Reference Design of Recovery NAND Interface

4.15. IMU Interrupt Interface

The module realizes DR (dead-reckoning) function through an external IMU (inertial measurement unit).

Table 28: Pin Definition of IMU Interrupt Interface

Pin Name	Pin No.	I/O	Description	Comment
IMU_PWR_EN	181	DO	IMU power enable control	1.8 V power domain. If unused, keep them open.
IMU_INT1	169	DI	IMU interrupt 1	
IMU_INT2	187	DI	IMU interrupt 2	

A reference design of IMU interrupt interface is shown as below:

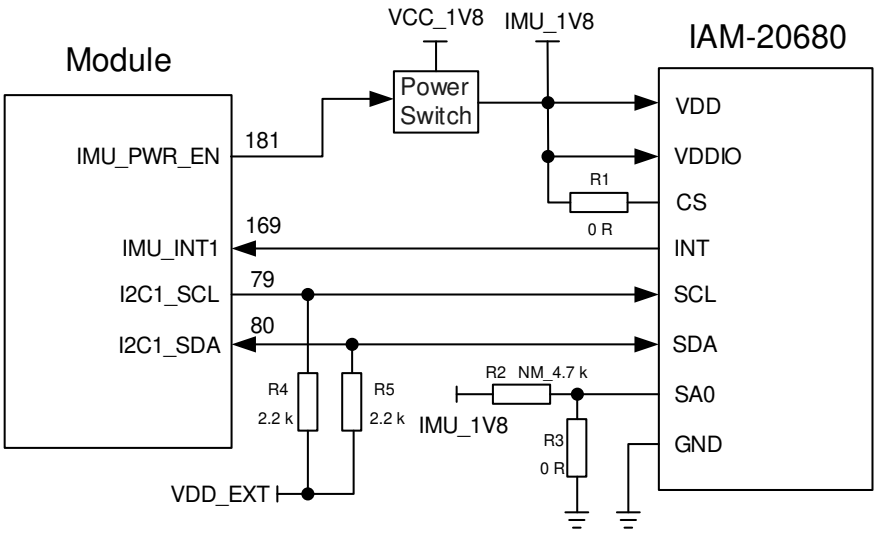


Figure 32: IMU Reference Design

NOTE

The module also supports Bosch SMI130, SMI230 and ST ASM330LHH sensors.

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The antenna interfaces are shown as below, the impedance of antenna ports is 50 Ω.

- One main antenna interface (ANT_MAIN)
- One diversity antenna interface (ANT_DRX)
- Two MIMO antenna interfaces (ANT_MIMO3, ANT_MIMO4)
- One GNSS antenna interface (ANT_GNSS)

5.1. Cellular Antenna Interfaces

5.1.1. Pin Definition [10]

The pin definition of antenna interfaces is shown below.

Table 29: Pin Definition of Cellular Antenna Interfaces

Pin Name	Pin No.	I/O	Description	LB (MHz)	MHB (MHz)	UHB (MHz)
ANT_MAIN	143	AIO	**2G/3G/4G MHB TX/PRX** **5G (SA) MHB TX/PRX** **5G (SA) n77/n78 TX MIMO/PRX MIMO** **5G (NSA) n41/n77/n78 TX @ LTE LB** **5G (Refarming NSA) MHB TX @ LTE LB** 3G LB DRX 4G LB DRX 4G B42/B48 PRX MIMO 5G (SA) LB DRX 5G (SA) n48/n79 PRX MIMO	617–960	1452–2690	3300–5000
ANT_DRX	170	AIO	**2G/3G/4G LB TX/PRX** **5G (SA) LB TX/PRX** **5G (Refarming NSA) LB TX @ LTE MHB**	617–960	1452–2690	3300–5000

[10] Frequency range of LB, MB, HB and UHB:
LB: < 1 GHz;
MB: 1–2.3 GHz;
HB: 2.3–2.7 GHz.
UHB: 3.3–5.0 GHz

			3G MHB DRX 4G MHB DRX 4G B42/B48 DRX MIMO 5G (SA) MHB DRX 5G (SA) n48/n77/n78/n79 DRX MIMO			
ANT_MIMO3	188	AIO	**4G B42/B48 TX/PRX** **5G (SA) n48/n77/n78/n79 TX/PRX** **5G n77/n78/n79 NSA TX @ LTE MHB** 4G/5G (SA) MHB PRX MIMO [11]	-	1452–2690	3300–5000
ANT_MIMO4	161	AI	4G MHB DRX MIMO [11] 4G B42/B48 DRX 5G (SA) MHB DRX MIMO 5G (SA & NSA) n48/n77/n78/n79 DRX	-	1452–2690	3300–5000

NOTE

The frequency bands in bold in the above table support both transmission and reception.

[11] B21 do not support DL 4 × 4 MIMO, support 2 × 2 MIMO only.

5.1.2. Operating Frequencies

Table 30: Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
GSM850	824–849	869–894	MHz
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
PCS1900	1850–1910	1930–1990	MHz
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B2	1850–1910	1930–1990	MHz
WCDMA B3	1710–1785	1805–1880	MHz
WCDMA B4	1710–1755	2110–2155	MHz
WCDMA B5	824–849	869–894	MHz
WCDMA B6	830–840	875–885	MHz
WCDMA B8	880–915	925–960	MHz
WCDMA B9	1750–1785	1845–1880	MHz
WCDMA B19	830–845	875–890	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B2	1850–1910	1930–1990	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B4	1710–1755	2110–2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B12	699–716	729–746	MHz
LTE-FDD B13	777–787	746–756	MHz

LTE-FDD B14	788–798	758–768	MHz
LTE-FDD B17	704–716	734–746	MHz
LTE-FDD B18	815–830	860–875	MHz
LTE-FDD B19	830–845	875–890	MHz
LTE-FDD B20	832–862	791–821	MHz
LTE-FDD B21	1447.9–1462.9	1495.9–1510.9	MHz
LTE-FDD B25	1850–1915	1930–1995	MHz
LTE-FDD B26	814–849	859–894	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-FDD B29 [12]	-	717–728	MHz
LTE-FDD B30 [12]	-	2350–2360	MHz
LTE-FDD B32 [12]	-	1452–1496	MHz
LTE-TDD B34	2010–2025	2010–2025	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B39	1880–1920	1880–1920	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz
LTE-TDD B42	3400–3600	3400–3600	MHz
LTE-TDD B48	3550–3700	3550–3700	MHz
LTE-FDD B66	1710–1780	2110–2200	MHz
LTE-FDD B71	663–698	617–652	MHz
5G NR FDD n1	1920–1980	2110–2170	MHz
5G NR FDD n2	1850–1910	1930–1990	MHz
5G NR FDD n3	1710–1785	1805–1880	MHz

[12] LTE-FDD B29, B30 and B32 support Rx only, and B30 is subject to carrier's deployment.

5G NR FDD n5	824–849	869–894	MHz
5G NR FDD n7	2500–2570	2620–2690	MHz
5G NR FDD n8	880–915	925–960	MHz
5G NR FDD n12	699–716	729–746	MHz
5G NR FDD n14	788–798	758–768	MHz
5G NR FDD n20	832–862	791–821	MHz
5G NR FDD n25	1850–1915	1930–1995	MHz
5G NR FDD n26	814–849	859–894	MHz
5G NR FDD n28	703–748	758–803	MHz
5G NR FDD n66	1710–1780	2110–2200	MHz
5G NR FDD n71	663–698	617–652	MHz
5G NR TDD n38	2570–2620	2570–2620	MHz
5G NR TDD n40	2300–2400	2300–2400	MHz
5G NR TDD n41	2496–2690	2496–2690	MHz
5G NR TDD n48	3550–3700	3500–3700	MHz
5G NR TDD n77	3300–4200	3300–4200	MHz
5G NR TDD n78	3300–3800	3300–3800	MHz
5G NR TDD n79	4400–5000	4400–5000	MHz

5.1.3. Reference Design

A reference design of main and diversity antenna interfaces is shown as below. It is recommended to reserve a π-type matching circuit and a DC blocking capacitor for better RF performance. The π-type matching components (R1/C1/C2 and R2/C3/C4) and the DC blocking capacitor (C5/C6) should be placed as close to the antennas as possible. The paralleling capacitors are not mounted by default.

Additionally, ESD protection components D1 and D2 need to be added near the antenna to effectively prevent static electricity.

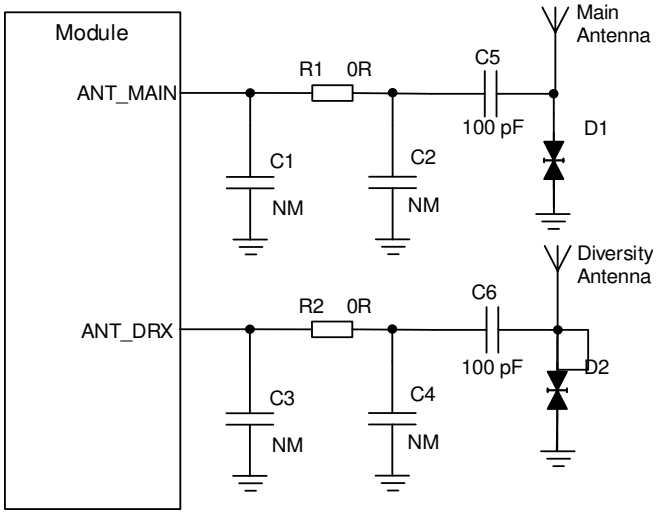


Figure 33: Reference Circuit of RF Antenna Interfaces

NOTE

1. The reference design of MIMO antenna interfaces are the same as that of main antenna interface.
2. Keep a proper distance between each antenna to improve receiving sensitivity.
3. Junction capacitance of ESD protection components on the antenna interface is recommended to be 0.05 pF.

5.2. GNSS Antenna Interface (Optional)

The module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, Galileo and QZSS, and supports L1 + L5 (default) and L1+L2* (optional) dual-band positioning.

The module supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1–10 Hz (1 Hz by default) data update rate via USB interface.

By default, GNSS engine of the module is switched off. It has to be switched on via an API function. For more details about GNSS engine technology and configurations, see ***document [9]***.

5.2.1. Pin Definition

The following tables show the pin definition of GNSS antenna interface.

Table 31: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	GNSS L1 (MHz)	GNSS L5 (MHz)	Comment
ANT_GNSS	197	AI	GNSS antenna interface	1559–1606	1166–1187	50 Ω impedance Supports active antenna only.

5.2.2. Operating Frequency

Table 32: GNSS Operating Frequency

Type	Frequency Band	Unit
GPS	1575.42 ±1.023 (L1) 1176.45 ±10.23 (L5)	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BDS	1561.098 ±2.046	MHz
QZSS	1575.42 (L1) 1176.45 (L5)	MHz

5.2.3. GNSS Performance

The following table shows GNSS performance of the module.

Table 33: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-150	dBm
	Reacquisition	Autonomous	-161	dBm
	Tracking	Autonomous	-158	dBm
TTFF	Cold start @ open sky	Autonomous	33	s
		XTRA enabled	12	s
	Warm start	Autonomous	24	s

	@ open sky	XTRA enabled	1	s
	Hot start @ open sky	Autonomous	1	s
		XTRA enabled	0.8	s
Accuracy	CEP-50	Autonomous @ open sky	1.5	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (within 5 minutes, the GNSS signal lost lock times ≤ 3, and GNSS signal lost lock time cannot exceed 10 seconds each time).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 5 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.
4. The above GNSS performance test data is measured under single-frequency L1.
5. For more details about GNSS performance, please consult Quectel technical Support for GNSS performance test report.

5.2.4. Reference Design

A reference design of GNSS antenna is shown as below.

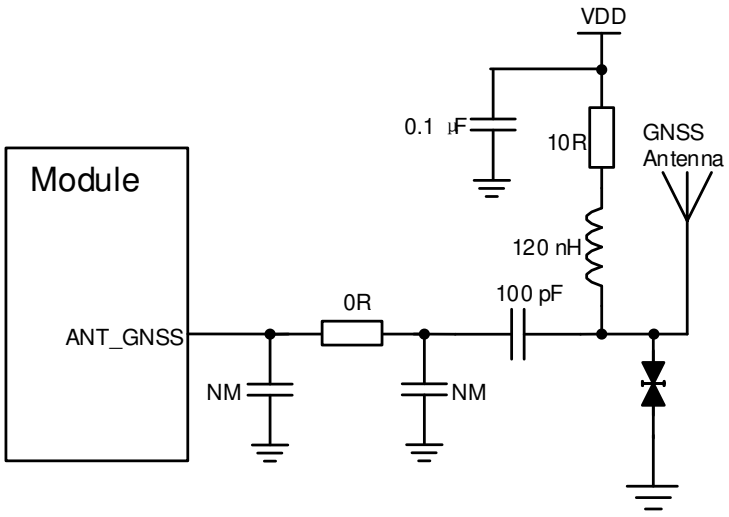


Figure 34: Reference Circuit of GNSS Antenna

NOTE

1. GNSS is an optional function. If the function is not used, keep ANT_GNSS open.
2. An external LDO can be selected to supply power according to the active antenna requirement.
3. Junction capacitance of ESD protection components on the antenna interface is recommended to be 0.05 pF.
4. It is recommended to add a 25 dB notch filter at the LNA input end of the active antenna when LTE B13 or B14 is supported.

5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

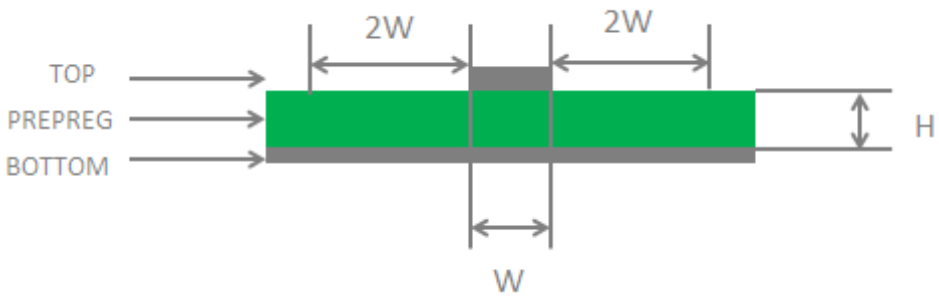


Figure 35: Microstrip Design on a 2-layer PCB

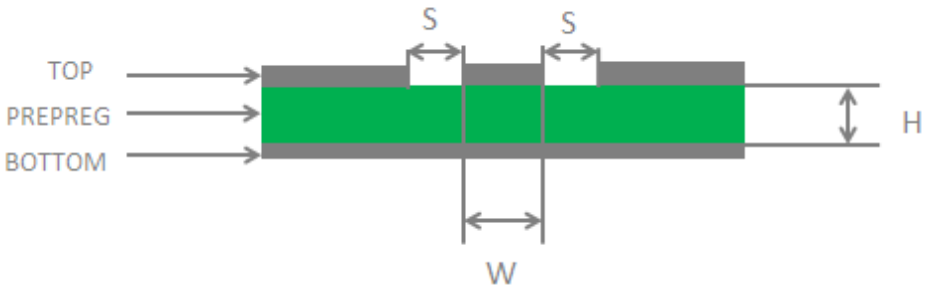


Figure 36: Coplanar Waveguide Design on a 2-layer PCB

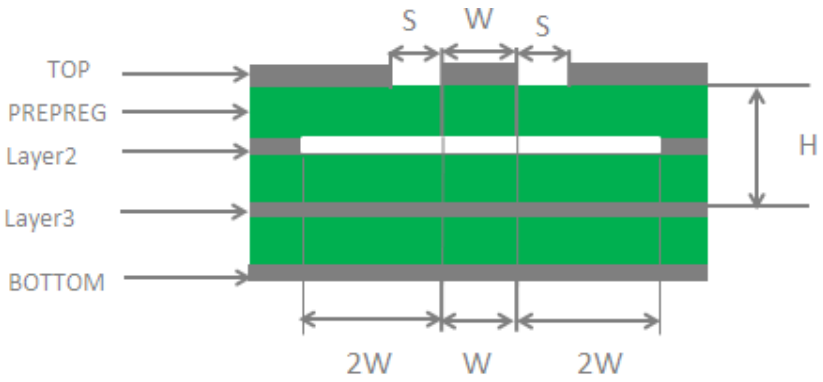


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

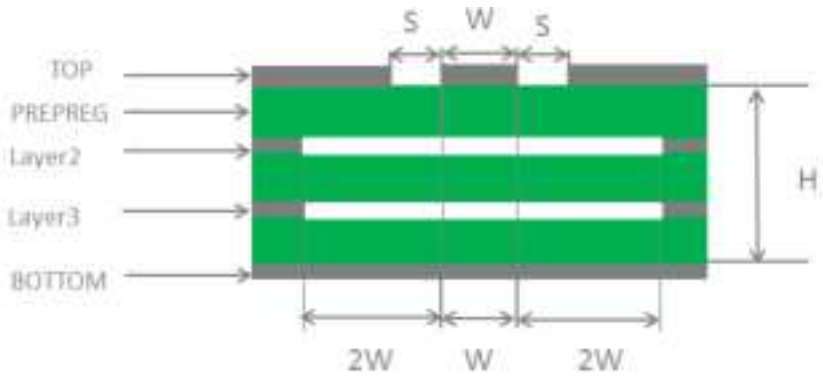


Figure 38: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice as wide as RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [10]***.

5.4. Antenna Design Requirements

The following table shows the requirements on RF antenna.

Table 34: Antenna Design Requirements

Type	Requirements
GNSS	Frequency range: L1: 1559–1606 MHz; L5: 1166–1187 MHz Polarization: RHCP VSWR: ≤ 2 (Typ.) Antenna gain: > 0 dBi Active antenna embedded LNA noise figure: < 1.5 dB Active antenna embedded LNA gain: see **NOTE 4** & **NOTE 5** below for design considerations
Cellular	VSWR: ≤ 2 Efficiency: > 30 % Input impedance: 50 Ω Cable insertion loss: **< 1 dB:** LB (< 1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)

NOTE

1. Maximize the distance among GNSS antenna, main antenna, diversity antenna and MIMO antenna.
2. Antenna isolation:
   > 20 dB @ above 1000 MHz;
   > 15 dB @ 600–1000 MHz;
   > 10 dB @ 400–600 MHz.
3. The isolation between each antenna traces on PCB is recommended to be over 75 dB.
4. GNSS receiver is designed to work with an external LNA (eLNA) in range of 18–20 dB. That is, ensure that the total gain from eLNA to GNSS receiver (including external active antenna, cable loss, connectors, PCB traces, and attenuator) meets 18–20 dB.
5. Attenuator (π-type attenuation circuit) can be used when the total gain exceeds 20 dB.

5.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the HFM connector provided by Rosenberger.

Figure 39: Description of the HFM Connector

For more details, visit https://www.rosenbergerap.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 35: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Voltage at Digital Pins	-0.3	2.13	V
Voltage at ADC0	0	1.91	V
Voltage at ADC1	0	1.91	V
Voltage at ADC3	0	1.91	V
Voltage at ADC4	0	1.91	V

6.2. Power Supply Ratings

Table 36: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT_BB, VBAT_RF	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during burst transmission	Maximum transmitted power on EGSM900.	-	-	400	mV
	Voltage drop during peak data rate	Peak DL data rate on EN-DC	-	-	400	mV
I_{VBAT_BB}, I_{VBAT_RF}	Peak supply current	-	-	-	3.0	A
USB_VBUS	USB connection detection	-	3.0	5.0	5.25	V
VDD_EXT	Provide 1.8 V for external circuits	-	-	1.8	-	V
USIM_VDD	(U)SIM card power supply	1.8 V application	1.65	1.8	1.95	V
		3.0 V application	2.7	2.95	3.05	V
SDIO_VDD	Power supply input for SDIO	1.8 V application	1.65	1.8	1.95	V
RGMII_PWR_IN	RGMII interface power input	1.8 V application	1.7	1.8	1.94	V
		2.5 V application	2.31	2.5	2.69	V

6.3. Digital I/O Characteristics

Table 37: 1.8 V Digital I/O Requirements (Group 1)

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	1.26	2.1	V

V_{IL}	Input low voltage	-0.3	0.54	V
V_{OH}	Output high voltage	1.35	1.8	V
V_{OL}	Output low voltage	0	0.45	V

Table 38: 1.8 V Digital I/O Requirements (Group 2)

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	1.27	2.0	V
V_{IL}	Input low voltage	-0.3	0.58	V
V_{OH}	Output high voltage	1.4	-	V
V_{OL}	Output low voltage	-	0.45	V

Table 39: 1.8 V Digital I/O Requirements (Group 3)

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	1.17	-	V
V_{IL}	Input low voltage	-	0.63	V
V_{OH}	Output high voltage	1.44	1.8	V
V_{OL}	Output low voltage	0.0	0.36	V

Table 40: (U)SIM 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.65	1.95	V
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD + 0.3	V
V_{IL}	Input low voltage	-0.3	0.2 × USIM_VDD	V
V_{OH}	Output high voltage	0.8 × USIM_VDD	USIM_VDD	V
V_{OL}	Output low voltage	0.	0.4	V

Table 41: (U)SIM 3.0 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.05	V
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD + 0.3	V
V_{IL}	Input low voltage	-0.3	0.2 × USIM_VDD	V
V_{OH}	Output high voltage	0.8 × USIM_VDD	USIM_VDD	V
V_{OL}	Output low voltage	0	0.4	V

Table 42: SDIO 1.8 V I/O Requirements

Parameter	Description	Min.	Typ.	Max.	Unit
SDIO_VDD	Power supply	1.65	1.8	1.95	V
V_{IH}	Input high voltage	1.27	-	2	V
V_{IL}	Input low voltage	-0.3	-	0.58	V
V_{OH}	Output high voltage	1.4	-	-	V
V_{OL}	Output low voltage	-	-	0.45	V

Table 43: RGMII 1.8 V I/O Requirements

Parameter	Description	Min.	Typ.	Max.	Unit
RGMII_PWR_IN	Power supply	1.7	1.8	1.94	V
V_{IH}	Input high voltage	1.17	-	2.1	V
V_{IL}	Input low voltage	-0.3	-	0.63	V
V_{OH}	Output high voltage	1.35	-	-	V
V_{OL}	Output low voltage	-	-	0.4	V

Table 44: RGMII 2.5 V I/O Requirements

Parameter	Description	Min.	Typ.	Max.	Unit
RGMII_PWR_IN	Power supply	2.31	2.5	2.69	V
V_{IH}	Input high voltage	1.7	-	-	V
V_{IL}	Input low voltage	-	-	0.7	V
V_{OH}	Output high voltage	2.0	-	2.8	V
V_{OL}	Output low voltage	-0.3	-	0.4	V

6.4. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protective components to the ESD sensitive interfaces and points in the product design.

6.5. Operating and Storage Temperatures

Table 45: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [13]	-35	+25	+75	ºC
Extended Temperature Range [14]	-40	-	+85	ºC
eCall Temperature Range [15]	-40	-	+95	ºC
Storage Temperature Range	-40	-	+95	ºC

[13] Within the operating temperature range, the module meets 3GPP specifications, and eCall can be dialed out with a maximum power and data rate.
[14] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, eCall, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.
[15] Within eCall temperature range, the eCall function must be functional until the module is broken. When the ambient temperature is between 75 °C and 95 °C and the module temperature has reached the threshold value, the module will trigger protective measures (such as reduce power, decrease throughput and unregister the device) to ensure the full function of eCall.

6.6. Thermal Dissipation

The module exhibits the best performance when all internal chips are working within their designated operating temperature ranges. However, if any chip reaches or exceeds its maximum temperature, the module may still work but its performance and functionalities (such as RF output power and data rate) will be compromised. Therefore, the thermal design should be maximally optimized to ensure that all internal chips consistently remain within their recommended operating temperature ranges.

The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on the PCB motherboard, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Expose the copper on the backside of the PCB where the module is mounted.
- Follow the principles below when designing the heatsink:
  - It is recommended to integrate the heatsink with the outer shell of telematic control unit (TCU) according to the module's application scenario. This allows for rapid transfer of the heat generated by the module to the outer shell, thus enhancing heat dissipation efficiency and eliminating the need for fixing the heatsink.
  - The entire shell of the TCU or the shell of the area where the module is located must be made of materials with excellent heat dissipation properties. It is recommended to use die-cast aluminum with higher thermal conductivity.
  - Based on the heat dissipation direction of the module, you can choose either of the following optional heatsink installation positions:
    a) The top surface of the module shielding cover;
    b) The bottom surface of the PCBA under the module;
    c) Both the top surface of the module shielding cover and the bottom surface of the PCBA under the module.

    If the heatsink is located only on one side, option a) is recommended; if the situation allows, option c) is recommended.

  - The heatsink must meet the following requirements:
    a) The base plate area of the heatsink should be larger than the module area for full coverage;
    b) Choose a heatsink with adequate fins to ensure effective heat dissipation. The fins should be located within the area where the module is mounted.
  - Since the heatsink is in contact with either the top surface of the shielding cover or the bottom surface of the PCBA through the thermal interface material (TIM), it is necessary to choose a TIM with high thermal conductivity, good flexibility, and good wettability.
  - Fasten the shell (heatsink) with screws around the TCU to prevent the heatsink from falling off during the drop tests, shock and vibration tests, or transportation.

- Implement other auxiliary cooling methods, such as air cooling or liquid cooling.

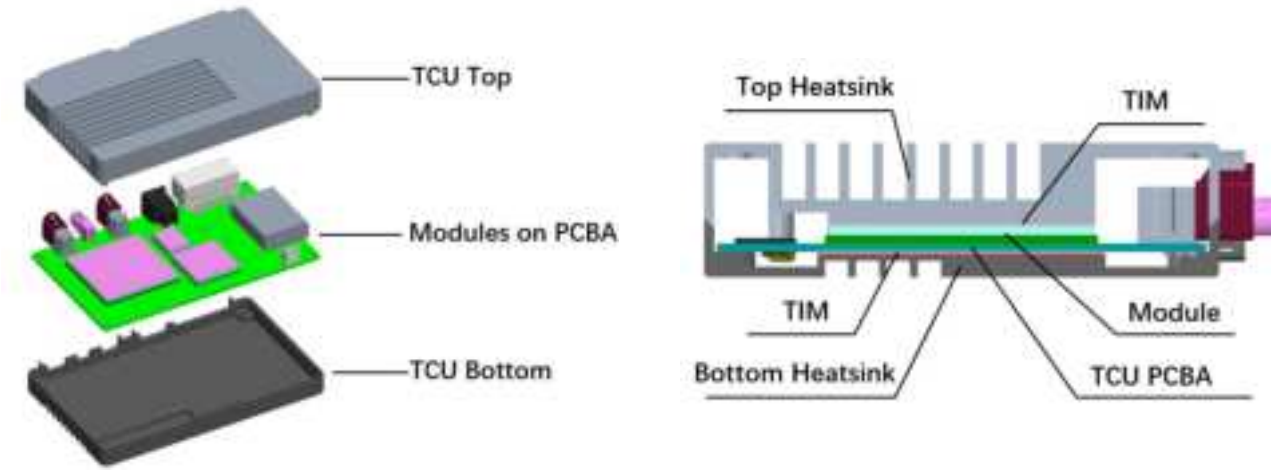


Figure 40: Heatsink Design Example

NOTE

1. The module works normal when the internal BB chip is below 105 °C. When the maximum temperature of the BB chip reaches or exceeds 105 °C, the module detaches from the network and enters Limited Service State in which only eCall is available, and it will recover to network connected state after the maximum temperature falls below 90 °C. Therefore, the thermal design should be maximally optimized to make sure the maximum BB chip temperature always maintains below 105 °C. Specified commands can be used to query the current temperature. See ***document [11]*** for details about the command and the detailed information on software thermal management.
2. For more detailed introduction on thermal design, see ***document [12].***

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

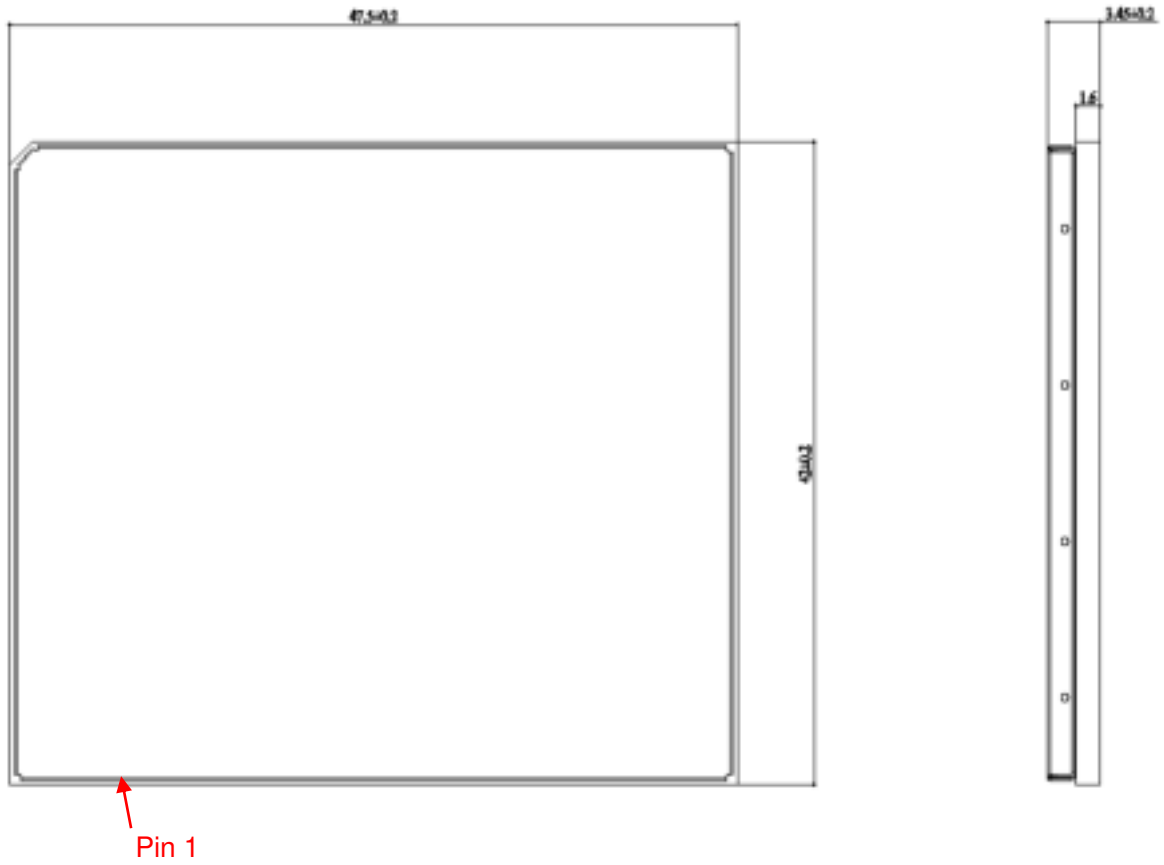


Figure 41: Module Top and Side Dimensions (Unit: mm)

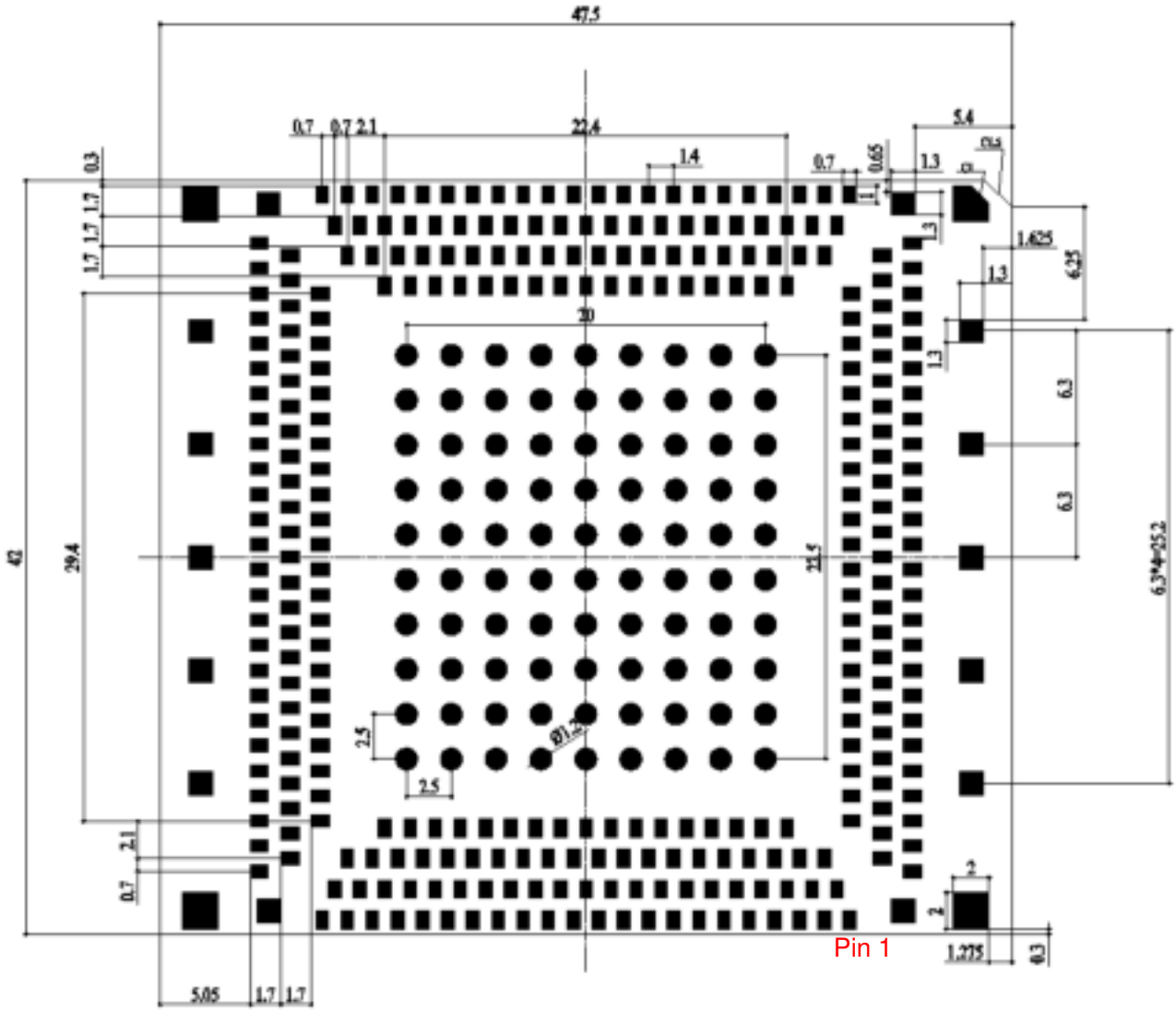


Figure 42: Module Bottom Dimensions (Unit: mm)

NOTE

The package warpage level of the module refers to *JEITA ED-7306* standard.

7.2. Recommended Footprint

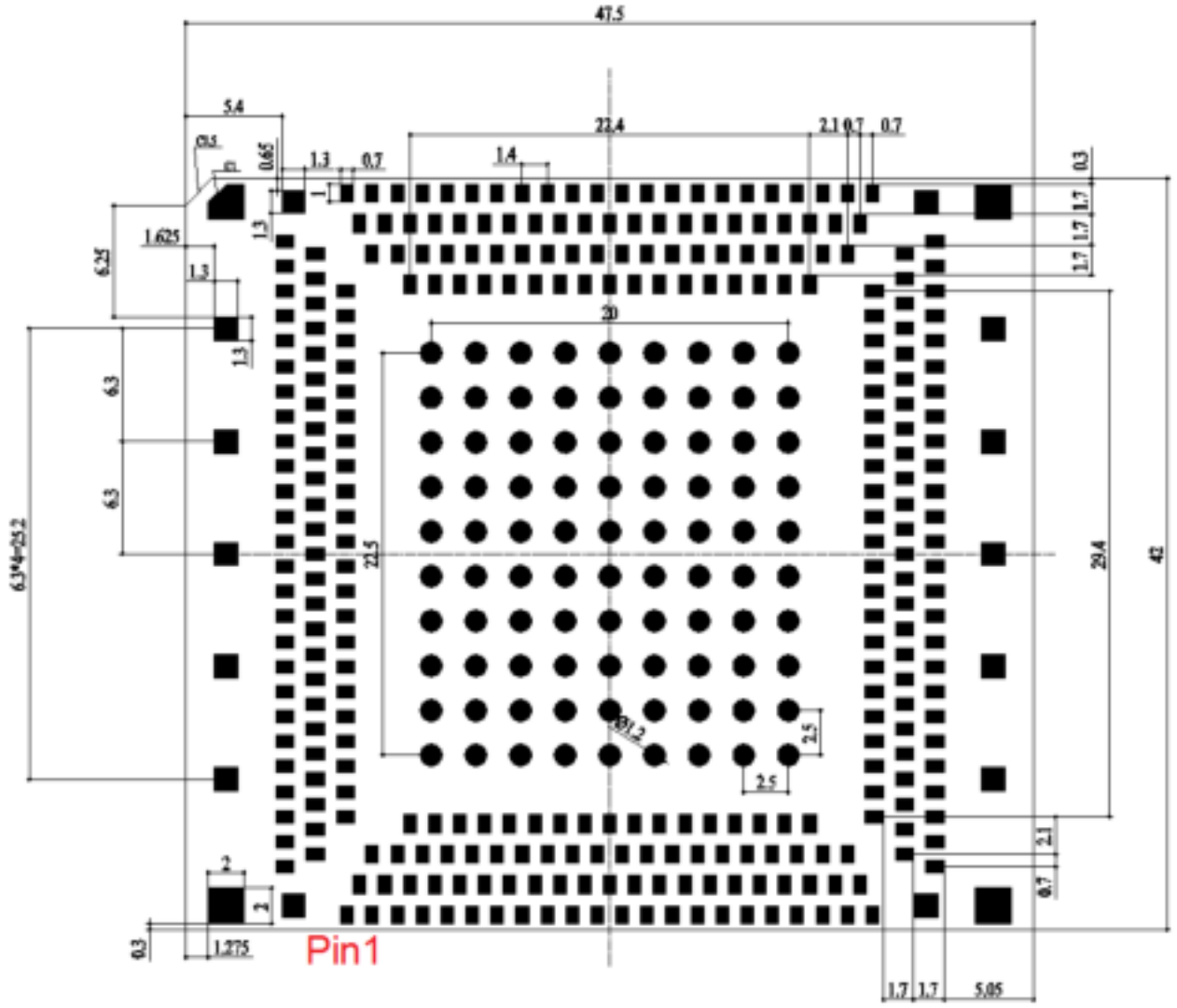


Figure 43: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

Figure 44: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [16] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[16] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [13]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

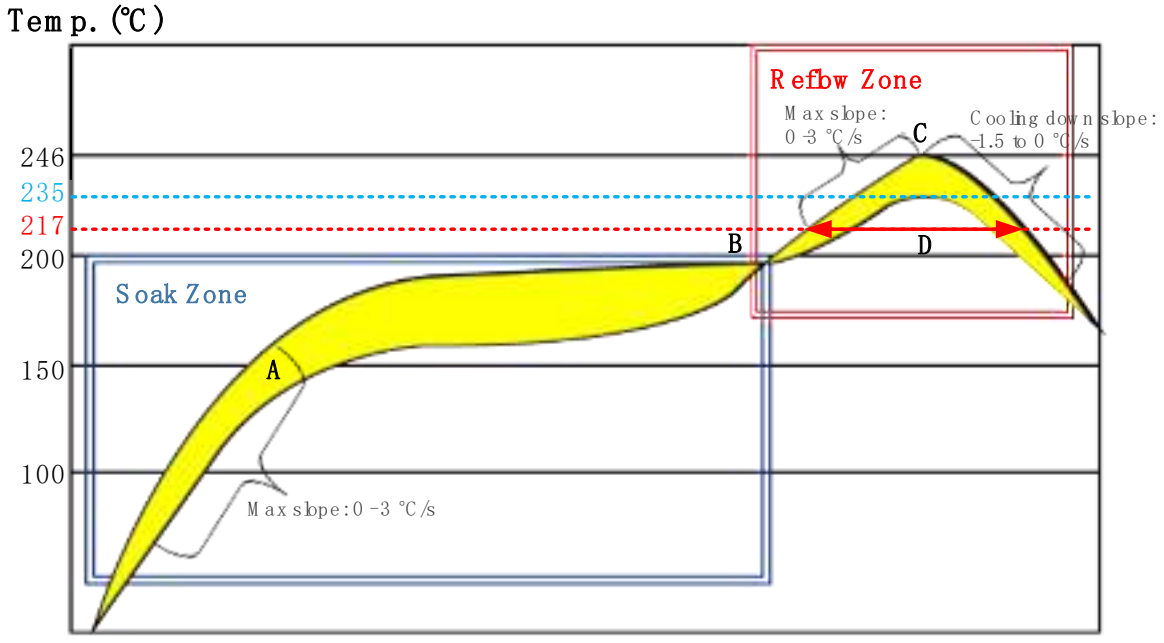


Figure 45: Recommended Reflow Soldering Thermal Profile

Table 46: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235 °C to 246 °C
Cool-down slope	-1.5 to 0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
3. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
4. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
5. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [13]***.

8.3. Packaging Specifications

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

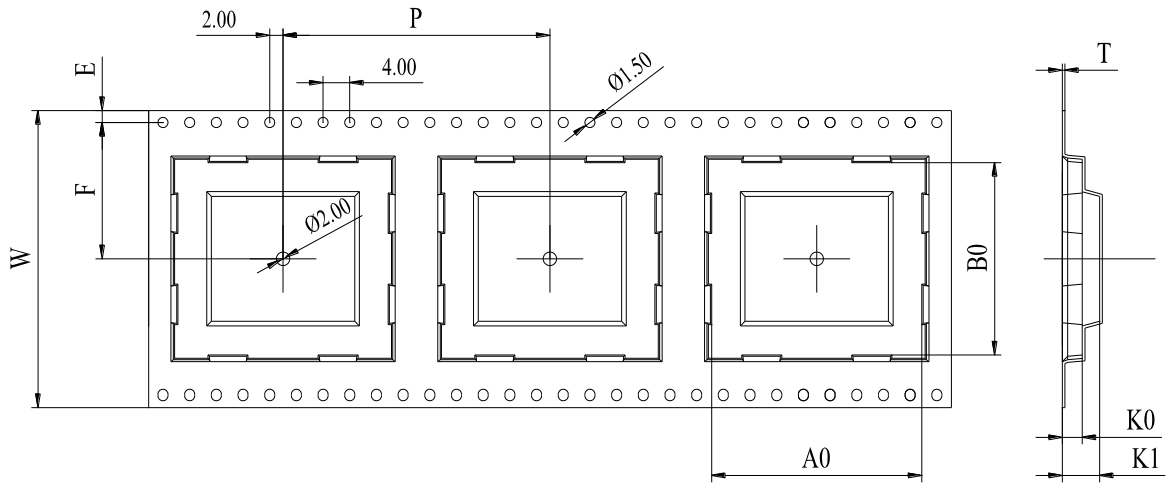


Figure 46: Carrier Tape Dimension Drawing (Unit: mm)

Table 47: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
72	64	0.5	48.1	42.6	4.75	5.9	34.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

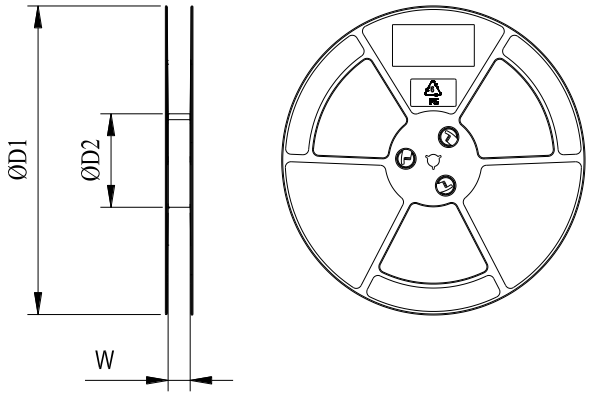


Figure 47: Plastic Reel Dimension Drawing

Table 48: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
380	180	72.5

8.3.3. Mounting Direction

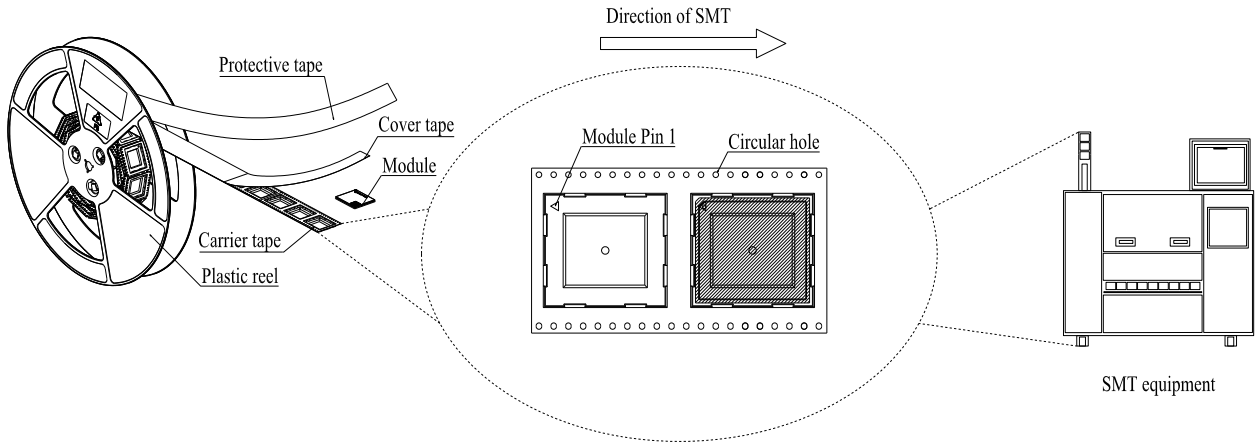
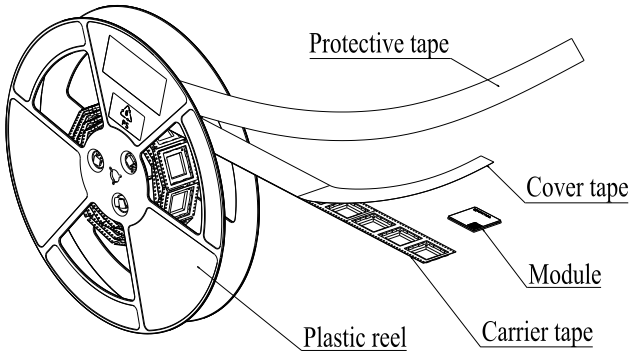


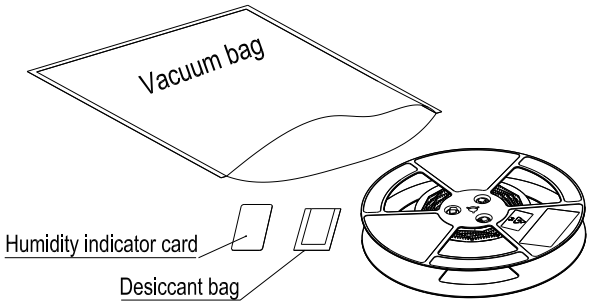
Figure 48: Mounting Direction

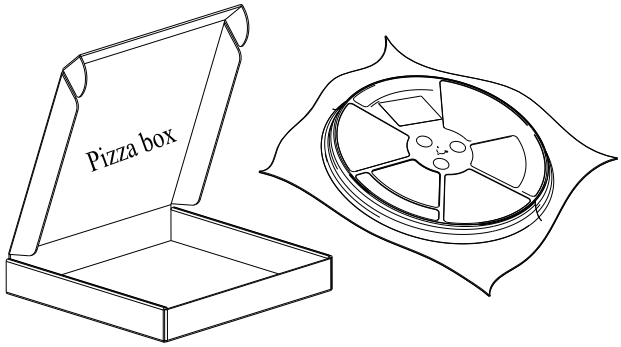
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 150 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 600 modules.

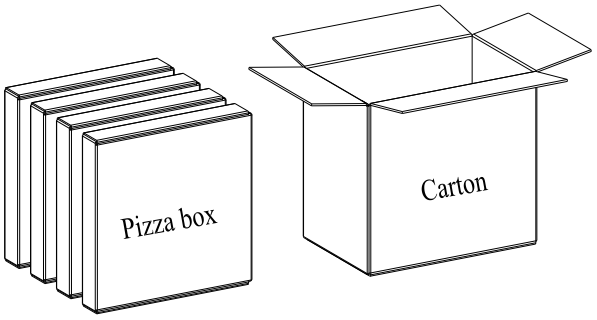


Figure 49: Packaging Process

9 Appendix References

Table 49: Related Documents

Document Name	
[1]	Quectel_AG555Q-GL_QuecOpen_GPIO_Configuration
[2]	Quectel_V2X&5G_EVB_User_Guide
[3]	Quectel_ AG55xQ&AG57xQ_Series_QuecOpen(SDK)_Device_Management_Reference_Design
[4]	Quectel_AG55xQ&AG57xQ_Series(DSDA)_QuecOpen(SDK)_Device_Management_ Reference_Design
[5]	Quectel_AG55xQ&AG57xQ_Series_QuecOpen(SDK)_AT_Commands_Manual
[6]	Quectel_AG55xQ&AG57xQ_Series_QuecOpen(SDK)_Low_Power_Mode_Application_Note
[7]	Quectel_AG555Q-GL_QuecOpen_Reference_Design
[8]	Quectel_AG55xQ_Series_QuecOpen(SDK)_ADC_Development_Guide
[9]	Quectel_AG55xQ&AG57xQ_Series_QuecOpen(SDK)_GNSS_Development_Guide
[10]	Quectel_RF_Layout_Application_Note
[11]	Quectel_AG55xQ&AG57xQ_Series_QuecOpen(SDK)_Software_Thermal_Management_Guide
[12]	Quectel_Module_Thermal_Design_Guide
[13]	Quectel_Module_SMT_Application_Note

Table 50: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
5G NR	5G New Radio

AC	Alternating Current
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-rate
AP	Application Processor
API	Application Program Interface
APT	Average Power Tracking
AVTP	Audio/Video Transport Protocol
ARM	Advanced RISC Machine
BLSP	Bus Access Manager Low-speed Peripheral
bps	Bits Per Second
BPSK	Binary Phase Shift Keying
CS	Coding Scheme
CTS	Clear To Send
DC-HSPA+	Dual-carrier High Speed Packet Access
DCS	Data Communications Equipment
DFOTA	Delta Firmware Upgrade Over the Air
DL	Downlink
DR	Dead Reckoning
DRX	Discontinuous Reception
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EAVB	Ethernet Audio Video Bridging
EDGE	Enhanced Data Rates for GSM Evolution
EFR	Enhanced Full Rate
EGSM	Enhanced GSM

EMI	Electromagnetic Interference
eMMC	Embedded Multimedia Card
EP	Endpoint
ESD	Electrostatic Discharge
EVB	Evaluation Board
FDD	Frequency Division Duplex
FEM	Front-End Module
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP over SSL
FQTSS	Forwarding and Queuing of Time Sensitive Streams
Galileo	Galileo Satellite Navigation System
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPIO	General-purpose Input/Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications
gPTP	General Precise Time Protocol
HPUE	High Power User Equipment
HB	High Band
HR	Half Rate
HSPA+	High Speed Packet Access Plus
HSDPA	High Speed Downlink Packet Access

HSUPA	High Speed Uplink Packet Access
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
ITS	Intelligent Transportation System
I/O	Input/Output
IMU	Inertial Measurement Unit
Inom	Nominal Current
LAA	License Assisted Access
LB	Low Band
LDO	Low-dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPM	Low Power Mode
LTE	Long Term Evolution
MAC	Medium Access Control
MB	Mid-Band
MCS	Modulation and Coding Scheme
MDIO	Management Data Input/Output
ME	Mobile Equipment
MIMO	Multiple Input Multiple Output
MMS	Multimedia Messaging Service
MO	Mobile Originated
MLCC	Multi-layer Ceramic Chip Capacitor
MT	Mobile Terminated

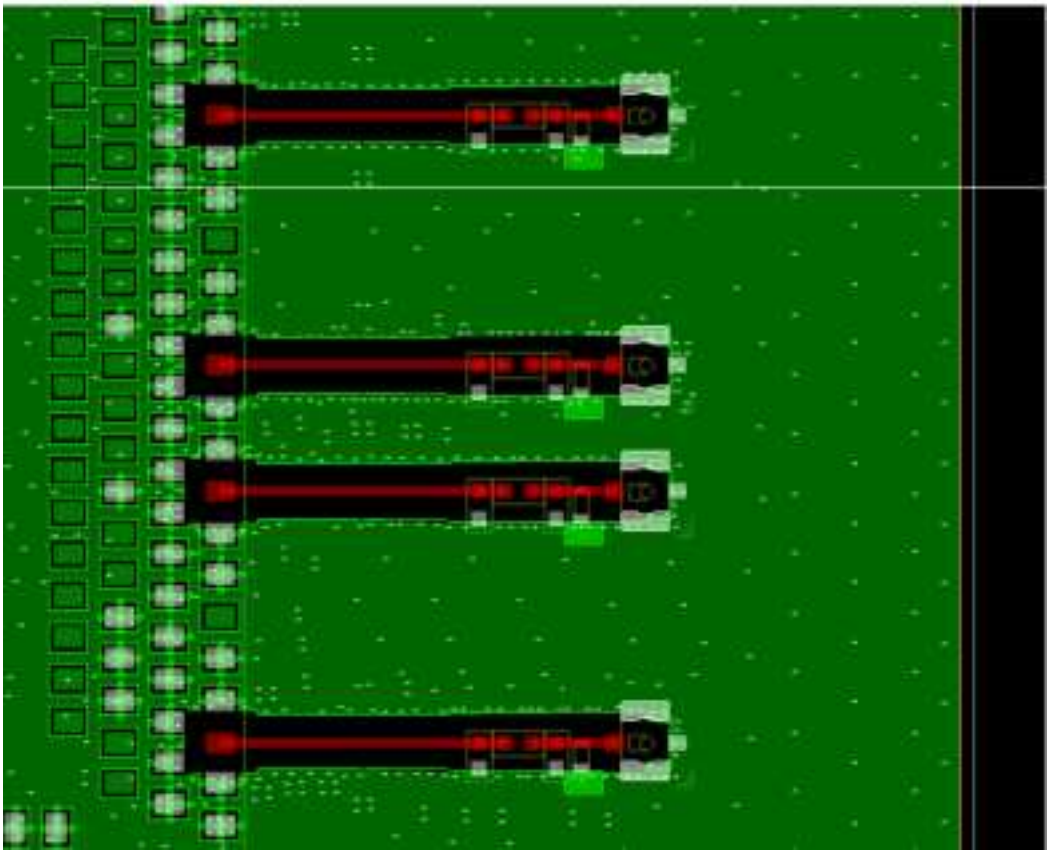
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
NSA	Non-Standalone
NTP	Network Time Protocol
OC	Open Collector
OTA	Over the Air
PA	Power Amplifier
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PHY	Physical
PING	Packet Internet Groper
PMIC	Power Management IC
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RC	PCIe Root Complex
R&D	Research&Development
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RHCP	Right Hand Circularly Polarized
RSU	Roadside Units
RTC	Real-Time Clock

RTS	Request to Send
RoHS	Restriction of Hazardous Substances
Rx	Receive
SA	Standalone
SAW	Surface Acoustic Wave
SCS	Sub-Carrier Space
SDIO	Secure Digital Input/Output
SIM	Subscriber Identity Module
SIMO	Single Input Multiple Output
SMD	Surface Mount Device
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SPI	Serial Peripheral Interface
SSL	Secure Sockets Layer
SRP	Stream Reservation Protocol
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
TLS	Transport Layer Security
TX	Transmitting Direction
t(ch)	Clock high
t(cl)	Clock low
t(mov)	Master output valid
t(mis)	Master input setup
t(mih)	Master input hold
UART	Universal Asynchronous Receiver & Transmitter

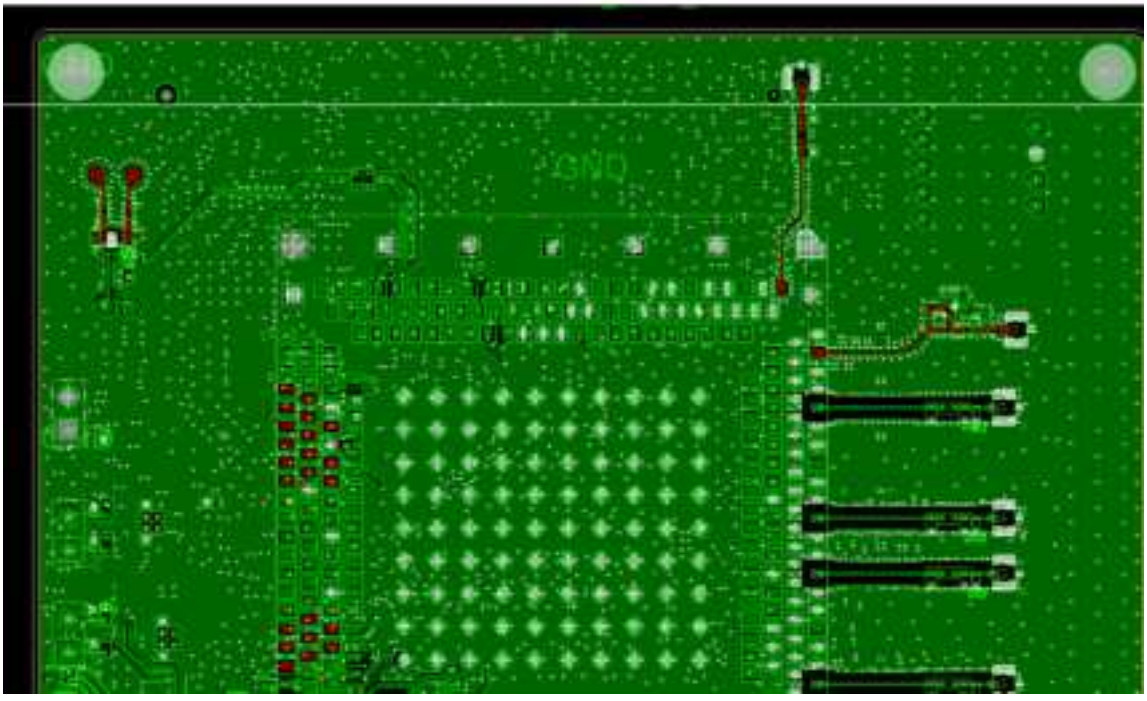
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
$V_I$max	Absolute Maximum Input Voltage
$V_I$min	Absolute Minimum Input Voltage
V_{OH}max	Maximum High-level Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
Wi-Fi	Wireless Fidelity

Trace design

Impedance Layer1 ref to layer3 50Ω ±10% (Layer 1. W=0.3669mm Coated Microstrip)



Impedance Layer 1 ref to layer 2 50Ω±10% (Layer1. W=0.085mm coated Microstrip)



Dielectric constant

品名:				5GHz	5GHz			
Layer	Mother Board	Tolerance (um)	Typical layer thickness (um)	DK	DF	材料型号	材料规格	结构图
	Solder Mask	min10	20	4.1				Image
L1	copper+plating	+/-	34	NA			0.012	
	Prepreg(1067)	+/-	51	3.37	0.012	EM-370	#1067	
L2	copper+plating	+/-	26	NA			0.012	
	Prepreg(2116)	+/-	115	3.82	0.01	EM-370	#2116	
L3	Copper	8oz	14	NA				
	Core	+/-	508	3.8	0.01	EM-390	0.508mm H/H	
L4	Copper	8oz	14	NA				
	Prepreg(2116)	+/-	115	3.82	0.01	EM-370	#2116	
L5	copper+plating	+/-	26	NA			0.012	
	Prepreg(1067)	+/-	51	3.37	0.012	EM-370	#1067	
L6	copper+plating	+/-	34	NA			0.012	
	Solder Mask	min10	20	4.1				
	Total thickness	1+/-0.1mm	1028					

FCC ID: XMR2024AG555QGL

OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part
15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR2024AG555QGL”
“Contains IC: 10224A-024AG555QGL “
The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 13 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location

with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Antenna Type	Max Gain
Dipole	GSM850: 2.68dBi, GSM1900: 0.25dBi WCDMA B2: 0.25dBi, B4: 1.47dBi, B5: 2.68dBi LTE B2: 0.25dBi, B4: 1.47dBi, B5: 2.68dBi, B7: 0.55dBi, B12: -0.2dBi, B13: 1.54dBi, B14: 2.42dBi, B17: -0.2dBi, B25: 0.25dBi, B26: 2.87dBi, B38: -0.23dBi, B41: 0.78dBi, B42: 1.61dBi, B66: 1.47dBi, B71: 1.22dBi 5G NR n2: 0.25dBi, n5: 2.68dBi, n7: 0.55dBi, n12: -0.2dBi, n14: 2.42dBi, n25: 0.25dBi, n26: 2.87dBi, n38: -0.23dBi, n41: 0.78dBi, n66: 1.47dBi, n71: 1.22dBi, n77/78(3450-3550MHz): 1.61dBi, n77/78(3700-3980MHz): 2.59dBi
Monopole	LTE B48 / 5G NR n48: -3.65dBi

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, and part 96 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 13 cm is maintained between the antenna and users, and 2) The transmitter module may not be co-located with any other transmitter or antenna. As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 13 cm between the radiator & your body.

IC: 10224A-024AG555QGL

Industry Canada Statement

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 22 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 22 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 22 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 22 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions cannot be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 22 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 10224A-024AG555QGL”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 22cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 10224A-024AG555QGL ".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.