

F1-22mΩ M3S 6-PACK SiC MOSFET Module

NXH022S120M3F1PTHG

The NXH022S120M3F1PTHG is a power module containing 22mΩ/ 1200 V SiC MOSFET 6-PACK and a thermistor with HPS DBC in an F1 package.

Features

- 22 mΩ / 1200 V M3S SiC MOSFET 6PACK
- HPS DBC
- Thermistor
- Options with Pre-Applied Thermal Interface Material (TIM) and without Pre-Applied TIM
- Press-Fit Pins
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

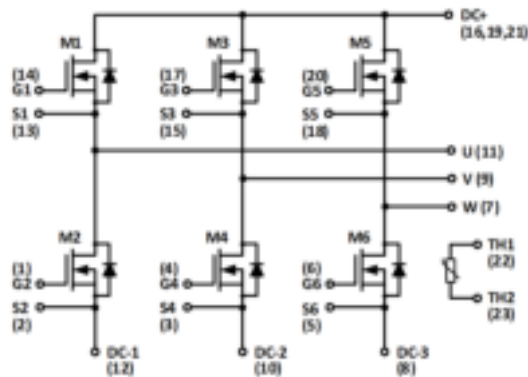
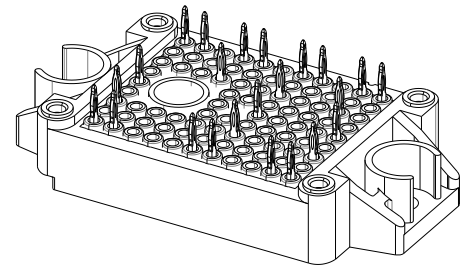


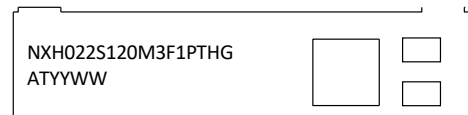
Figure 1. NXH022S120M3F1PTHG Schematic Diagram

PACKAGE PICTURE



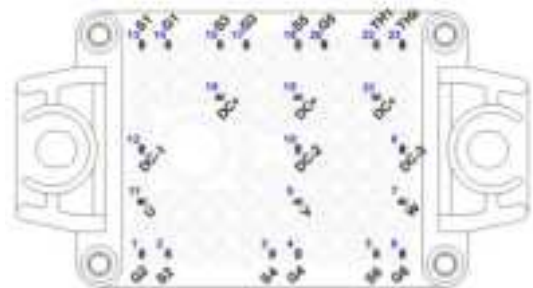
PIM22 33.8x42.5 (PRESS FIT)
CASE 180BX

MARKING DIAGRAM



XXXXX = Specific Device Code
AT= Assembly & Test Site Code
YWW = Year and Work Week Code

PIN CONNECTIONS



See Pin Function Description for pin names

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

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PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	G2	M2 Gate (Low side switch)
2	S2	M2 Kelvin Emitter (Low side switch)
3	S4	M4 Kelvin Emitter (Low side switch)
4	G4	M4 Gate (Low side switch)
5	S6	M6 Kelvin Emitter (Low side switch)
6	G6	M6 Gate (Low side switch)
7	W	W Terminal
8	DC-3	DC Negative Bus Connection
9	V	V Terminal
10	DC-2	DC Negative Bus Connection
11	U	U Terminal
12	DC-1	DC Negative Bus Connection
13	S1	M1 Kelvin Emitter (High side switch)
14	G1	M1 Gate (High side switch)
15	S3	M3 Kelvin Emitter (High side switch)
16	DC+	DC Positive Bus Connection
17	G3	M3 Gate (High side switch)
18	S5	M5 Kelvin Emitter (High side switch)
19	DC+	DC Positive Bus Connection
20	G5	M5 Gate (High side switch)
21	DC+	DC Positive Bus Connection
22	TH1	Thermistor Connection 1
23	TH2	Thermistor Connection 2

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
SiC MOSFET			
Drain–Source Voltage	V_{DS}	1200	V
Gate–Source Voltage	V_{GS}	+22/–10	V
Continuous Drain Current @ $T_c = 80^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	I_D	52	A
Pulsed Drain Current ($T_J = 150^\circ\text{C}$)	I_{Dpulse}	104	A
Maximum Power Dissipation ($T_J = 175^\circ\text{C}$)	P_{tot}	135	W
Minimum Operating Junction Temperature	T_{JMIN}	–40	$^\circ\text{C}$
Maximum Operating Junction Temperature	T_{JMAX}	175	$^\circ\text{C}$

THERMAL PROPERTIES

Storage Temperature range	T_{stg}	–40 to 150	$^\circ\text{C}$
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INSULATION PROPERTIES

Isolation test voltage, $t = 1$ sec, 60 Hz	V_{is}	4800	V_{RMS}
Creepage distance		12.7	mm
CTI		600	
Substrate Ceramic Material		Al_2O_3	
Substrate Ceramic Material Thickness		(0.32)	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Module Operating Junction Temperature	T_J	–40	150	$^\circ\text{C}$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

$T_J = 25^\circ\text{C}$ unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SiC MOSFET CHARACTERISTICS						
Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}$, $V_{DS} = 1200\text{ V}$, $T_J = 25^\circ\text{C}$	I_{DSS}	–	–	100	μA
Drain–Source On Resistance (Note 1)	$V_{GS} = 18\text{ V}$, $I_D = 50\text{ A}$, $T_J = 25^\circ\text{C}$	$R_{DS(ON)}$	–	22.6	–	$\text{m}\Omega$
	$V_{GS} = 18\text{ V}$, $I_D = 50\text{ A}$, $T_J = 125^\circ\text{C}$		–	38.6	–	
	$V_{GS} = 18\text{ V}$, $I_D = 50\text{ A}$, $T_J = 150^\circ\text{C}$		–	43.8	–	
	$V_{GS} = 18\text{ V}$, $I_D = 50\text{ A}$, $T_J = 175^\circ\text{C}$		–	50.6	–	
Gate–Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 30\text{ mA}$	$V_{GS(TH)}$	2.04	2.72	4.4	V
Recommended Gate Voltage		V_{GOP}	–3		+18	V
Gate–to–Source Leakage Current	$V_{GS} = +22/-10\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GSS}		–	(± 1)	μA
Input Capacitance	$V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$, $V_{DS} = 800\text{ V}$	C_{ISS}	–	3106	–	pF
Reverse Transfer Capacitance		C_{RSS}	–	16.5	–	
Output Capacitance		C_{OSS}	–	172.7	–	
Total Gate Charge	$V_{GS} = -3/18\text{ V}$, $V_{DS} = 800\text{ V}$, $I_D = 50\text{ A}$	$Q_{G(TOTAL)}$	–	142	–	nC
Gate–Source Charge		Q_{GS}	–	13	–	nC
Gate–Drain Charge		Q_{GD}	–	37	–	nC

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ELECTRICAL CHARACTERISTICS (continued)

T_J = 25 °C unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SiC MOSFET CHARACTERISTICS						
Turn-on Delay Time	T _J = 25°C V _{DS} = 800 V, I _D = 50 A V _{GS} = -3/18 V, R _G = 10 Ω	t _{d(on)}	—	25.75	—	ns
Rise Time		t _r	—	10.4	—	
Turn-off Delay Time		t _{d(off)}	—	105.98	—	
Fall Time		t _f	—	5.31	—	
Turn-on Switching Loss per Pulse		E _{ON}	—	0.66	—	mJ
Turn-off Switching Loss per Pulse		E _{OFF}	—	0.47	—	
Turn-on Delay Time	T _J = 150°C V _{DS} = 800 V, I _D = 50 A V _{GS} = -3/18 V, R _G = 10 Ω	t _{d(on)}	—	25.61	—	ns
Rise Time		t _r	—	8.73	—	
Turn-off Delay Time		t _{d(off)}	—	117.56	—	
Fall Time		t _f	—	5.17	—	
Turn-on Switching Loss per Pulse		E _{ON}	—	0.83	—	mJ
Turn-off Switching Loss per Pulse		E _{OFF}	—	0.56	—	
Diode Forward Voltage	I _{SD} = 50 A, V _{GS} = -3V, T _J = 25°C,	V _{SD}	—	5.21	—	V
	I _{SD} = 50 A, V _{GS} = -3V, T _J = 125°C		—	5.11	—	
	I _{SD} = 50 A, V _{GS} = -3V, T _J = 150°C		—	5.02	—	
Thermal Resistance – Chip-to-Case	M1, M2	R _{thJC}	—	(0.702)	—	°C/W
Thermal Resistance – Chip-to-Heatsink		R _{thJH}	—	TBD	—	°C/W

THERMISTOR CHARACTERISTICS

Nominal Resistance	T = 25°C	R ₂₅	—	5	—	kΩ
	T = 100°C	R ₁₀₀	—	457	—	Ω
	T = 150°C	R ₁₅₀	—	159.5	—	Ω
Deviation of R ₁₀₀	T = 100°C	ΔR/R	-5	—	5	%
Power Dissipation - Recommended Limit	0.15 mW, Non-self-heating Effect	P _D	—	0.1	—	mW
Power Dissipation - Absolute Maximum	5 mW	P _D	—	34.2	—	mW
Power Dissipation Constant			—	1.4	—	mW/K
B-value	B(25/50), tolerance ±2%		—	3375	—	K
B-value	B(25/100), tolerance ±2%		—	3436	—	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Orderable Part Number	Marking	Package	Shipping
NXH022S120M3F1PTHG	NXH022S120M3F1PTHG	F1: Case 180BY Press-fit Pins with pre-applied thermal interface material (TIM) (Pb-Free / Halide Free)	20 Units / Blister Tray

TYPICAL CHARACTERISTIC

M1/M2 SiC MOSFET CHARACTERISTIC

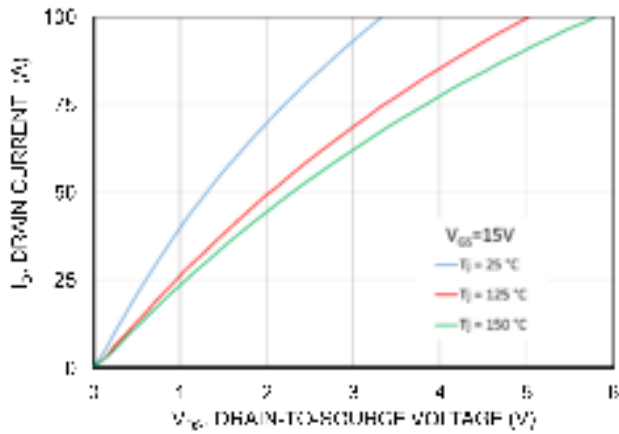


Figure 2. MOSFET Typical Output Characteristic $V_{GS}=15V$

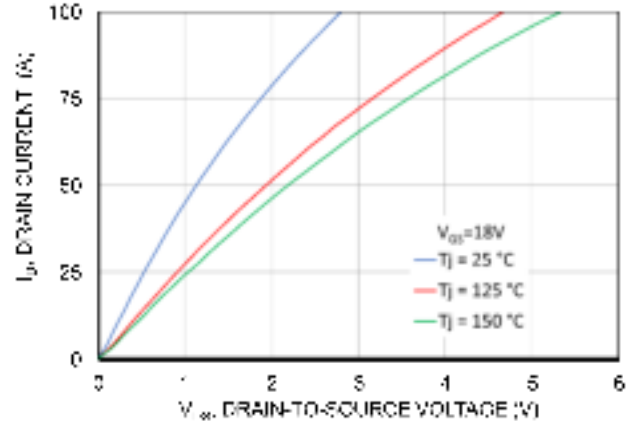


Figure 3. MOSFET Typical Output Characteristic $V_{GS}=18V$

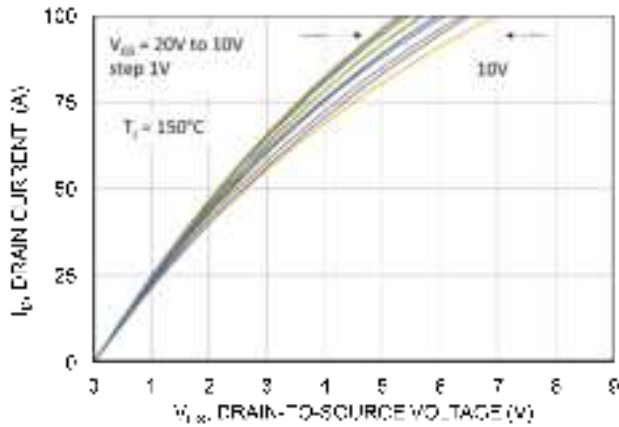


Figure 4. MOSFET Typical Output Characteristic $V_{GS}=var.$

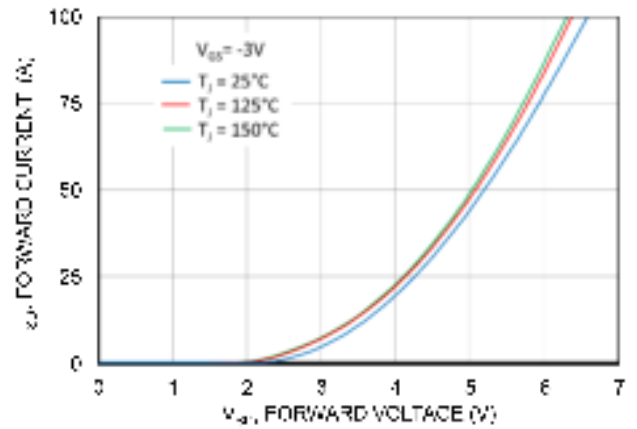


Figure 5. Body Diode Forward Characteristic

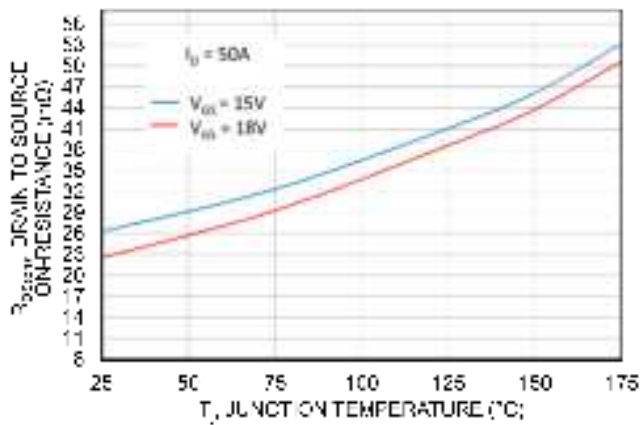


Figure 6. $R_{DS(ON)}$ DRAIN to SOURCE ON RESISTANCE vs. Junction Temperature

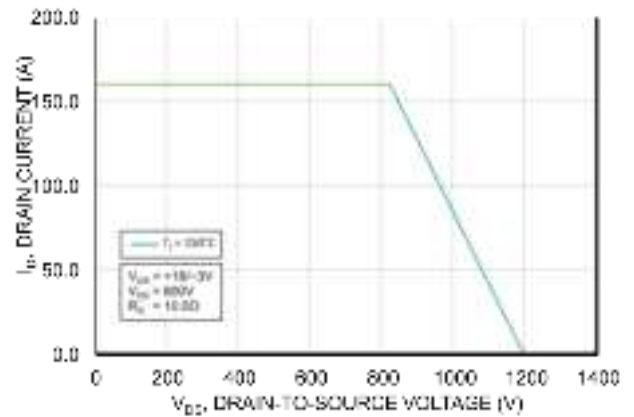


Figure 7. Reverse Bias Safe Operating Area (RBSOA)
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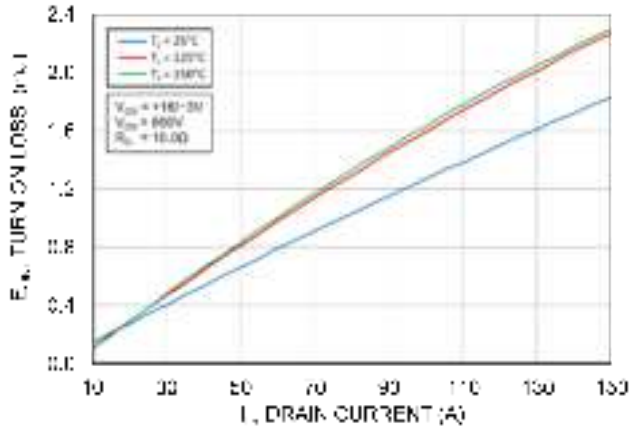


Figure 7. Switching On Loss vs. Drain Current $V_{DS} = 800$ V

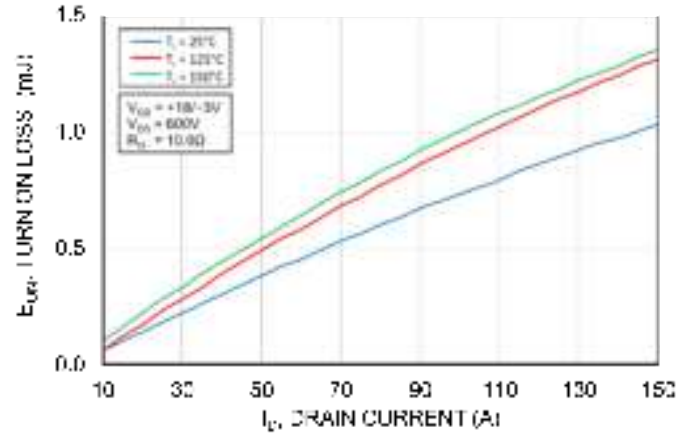


Figure 8. Switching On Loss vs. Drain Current $V_{DS} = 600$ V

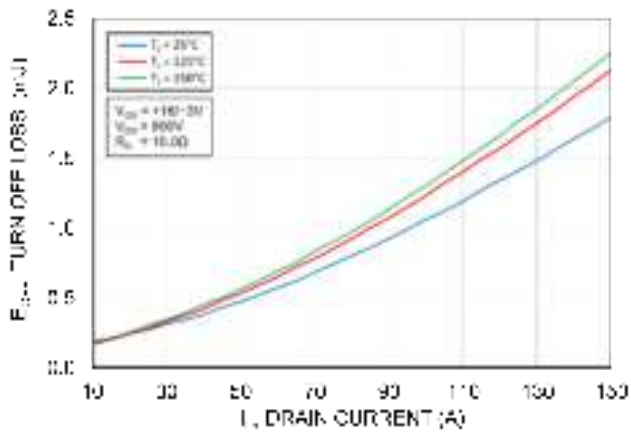


Figure 9. Switching Off Loss vs. Drain Current $V_{DS} = 800$ V

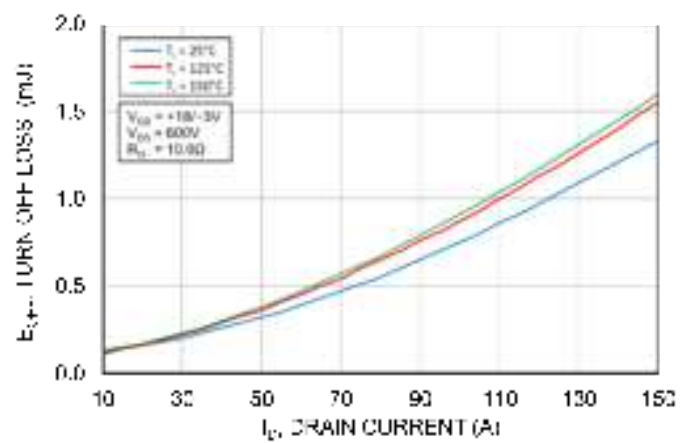


Figure 10. Switching Off Loss vs. Drain Current $V_{DS} = 600$ V

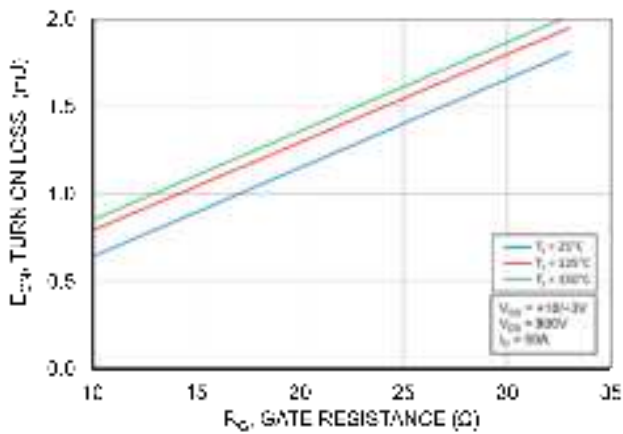


Figure 11. Switching On Loss vs. Gate Resistance $V_{DS} = 800$ V

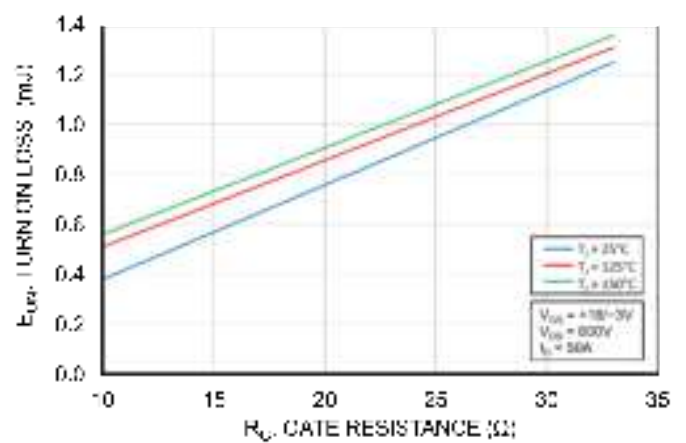


Figure 12. Switching On Loss vs. Gate Resistance $V_{DS} = 600$ V

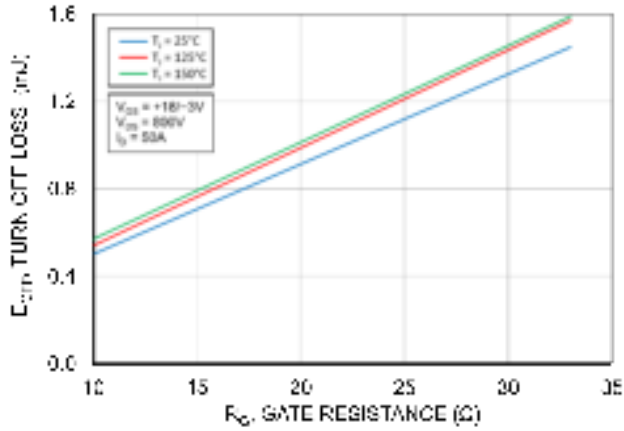


Figure 12. Switching Off Loss vs. Gate Resistance $V_{DS} = 800$ V

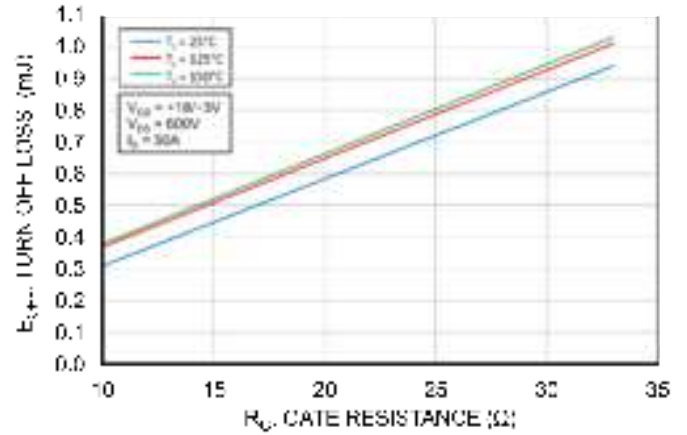


Figure 13. Switching Off Loss vs. Gate Resistance $V_{DS} = 600$ V

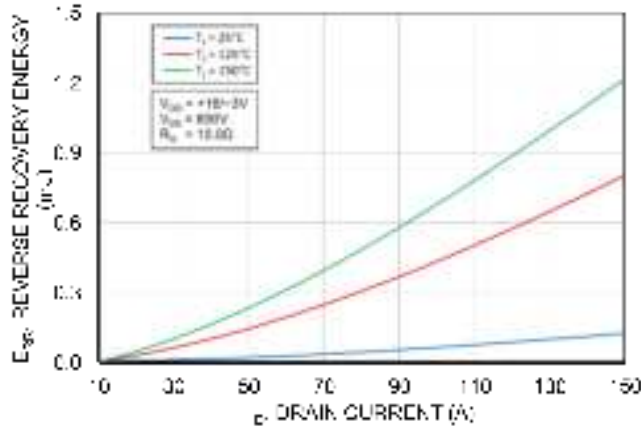


Figure 14. Reverse Recovery Loss vs. Gate Resistance

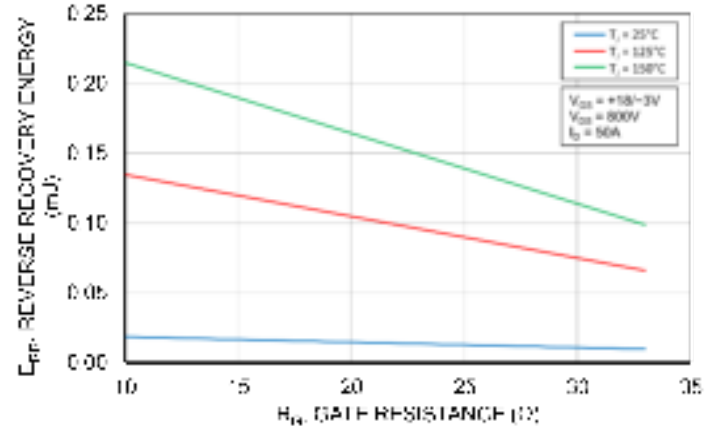


Figure 15. Reverse Recovery Loss vs. Gate Resistance

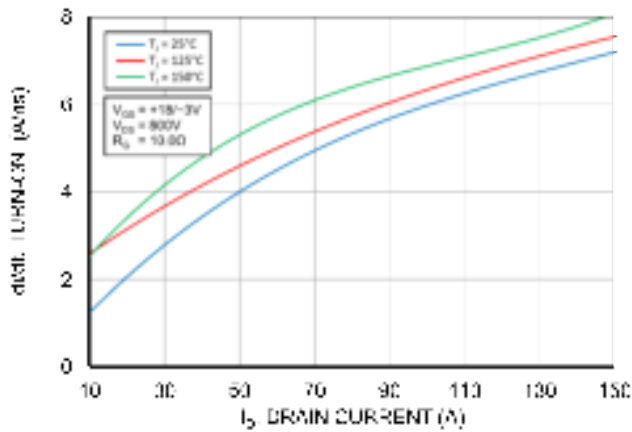


Figure 16. di/dt Turn On vs Drain Current

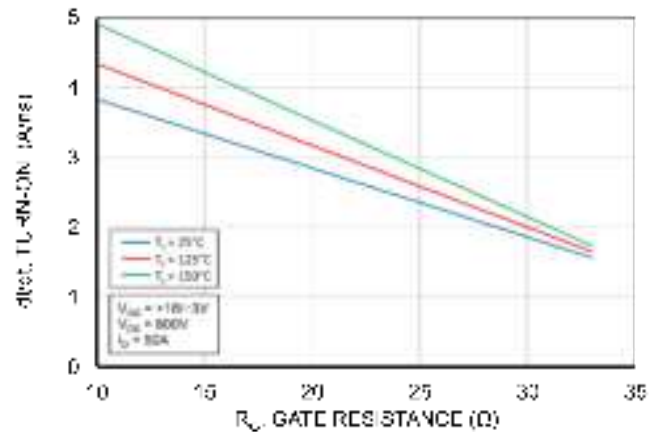


Figure 17. di/dt Turn On vs Gate Resistance

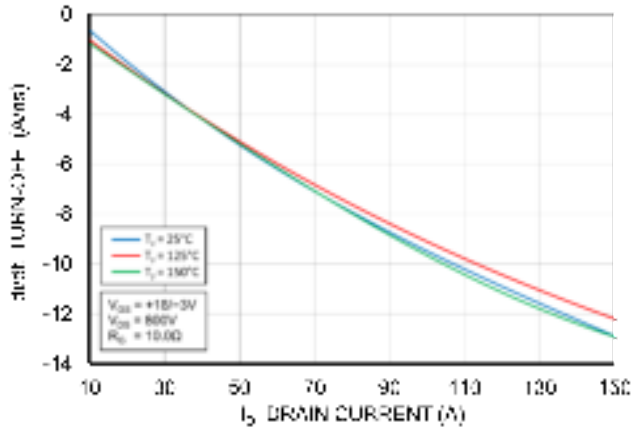


Figure 15. di/dt Turn Off vs Drain Current

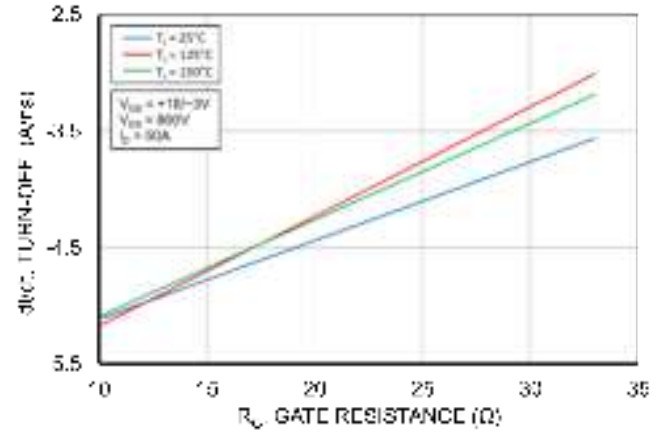


Figure 16. di/dt Turn Off vs Gate Resistance

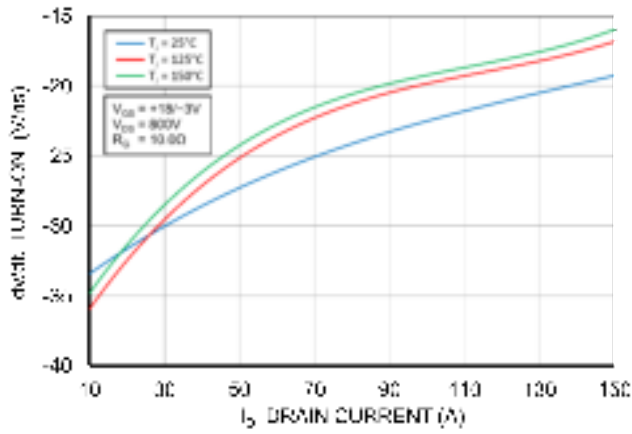


Figure 17. dv/dt Turn On vs Drain Current

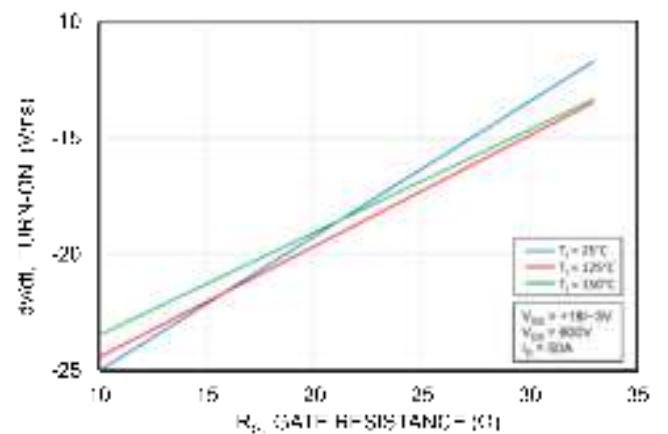


Figure 18. dv/dt Turn On vs Gate Resistance

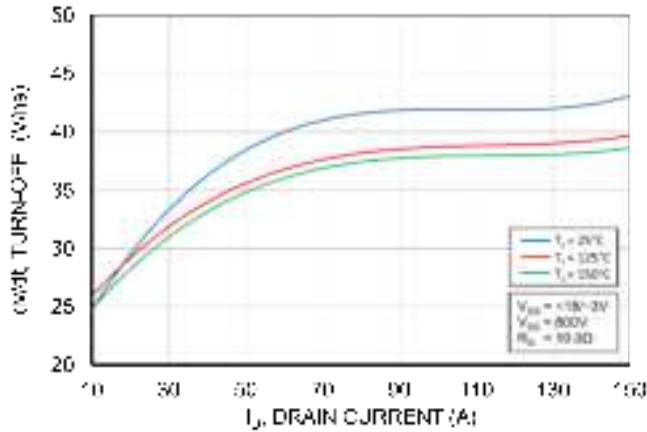


Figure 19. dv/dt Turn Off vs Drain Current

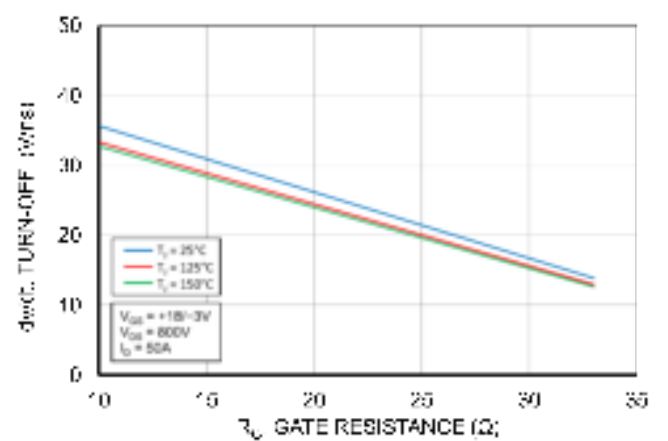
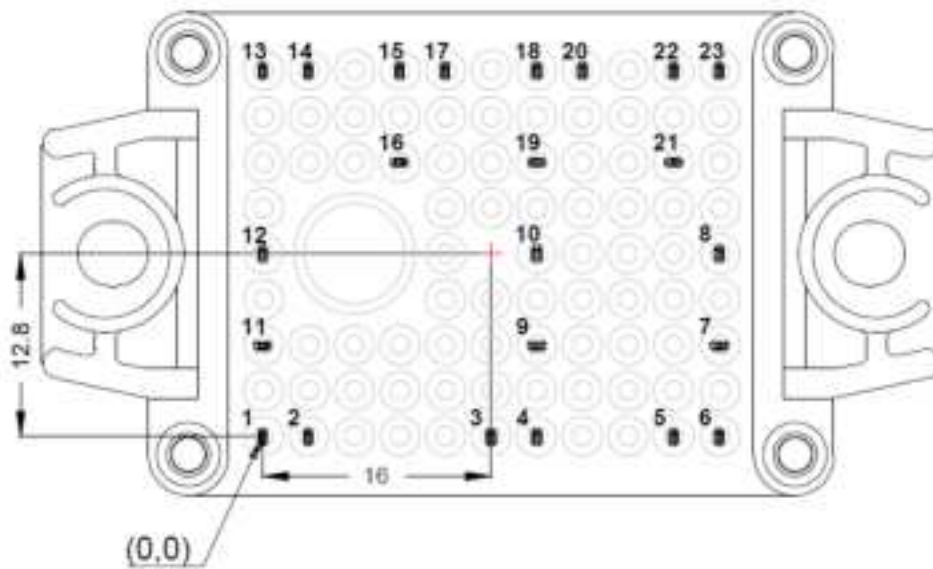


Figure 20. dv/dt Turn Off vs Gate Resistance

Table 1. CAUER NETWORKS

Cauer Element #	Rth (K/W)	Cth (Ws/K)
1	0.0004	0.0006
2	0.0112	0.0003
3	0.0064	0.0006
4	0.105	0.0013
5	0.1388	0.0071
6	0.2554	0.0215
7	0.1847	0.0576

NXH022S120M3F1PTHG



* Pin position

Pin #	X	Y	Function	Pin #	X	Y	Function
1	0	0	G2	13	0	25.6	S1
2	3.2	0	S2	14	3.2	25.6	G1
3	16	0	S4	15	9.6	25.6	S3
4	19.2	0	G4	16	9.6	19.2	DC+
5	28.8	0	S6	17	12.8	25.6	G3
6	32	0	G6	18	19.2	25.6	S5
7	32	6.4	W	19	19.2	19.2	DC+
8	32	12.8	DC-3	20	22.4	25.6	G5
9	19.2	6.4	V	21	28.8	19.2	DC+
10	19.2	12.8	DC-2	22	28.8	25.6	TH1
11	0	6.4	U	23	32	25.6	TH2
12	0	12.8	DC-1				