Design guide for ZVS QR flyback converter using CoolSET™ SiP

About this document

Scope and purpose

This design guide explains the zero-voltage switching (ZVS) quasi-resonant (QR) flyback converter, using Infineon's first fully integrated controller, CoolSET™ SiP ICE18xxM, which offers a highly effective reduction in system complexity. The CoolSET™ System in Package (SiP) features a high-voltage power switch, primary and secondary controller, as well as isolated communication. With this integration, an advanced PWM switching pattern forces a ZVS QR operation, reducing the turn-on switching losses and optimizing the EMI signature. The CoolSET™ SiP also features a sophisticated set of protection features, enabling ease of design-in and allowing customers to create products with a better user experience.

Intended audience

This document is intended for power supply designers and power electronics engineers who wish to design power supplies with ZVS QR controllers, CoolSET™ SiP ICE18xxM.

CoolSET™

Infineon's CoolSET™ AC-DC integrated power stages in fixed frequency and quasi-resonant switching scheme offer increased robustness and outstanding performance. This family offers superior energy efficiency, comprehensive protective features, and reduced system costs and is ideally suited for auxiliary power supply applications in a wide variety of potential applications such as:

- SMPS
- Home appliances
- Server
- Telecom

Table of contents

1. Abstract

In recent years, zero-voltage switching quasi-resonant (ZVS QR) flyback converters have emerged as a preferred choice for many applications, thanks to their exceptional efficiency, minimal electromagnetic interference (EMI), and significantly reduced switching losses. By leveraging these advantages, engineers can create power systems that are not only more efficient but also more reliable and environmentally friendly.

This design guide is specifically tailored for engineers working with Infineon's CoolSET™ SiP ICE18xxM controller, a cutting-edge solution for ZVS QR Flyback converters. The guide provides in-depth coverage of key design considerations, component selection, and PCB layout, empowering designers to create high-performance power converters that meet the demands of industrial and consumer applications.

2. Product description and selection

CoolSET™ SiP family products support a highly effective reduction in system complexity. The System in Package (SiP) integration includes a high-voltage power switch, a primary controller, and a secondary controller as well as isolated communication. The integrated controller enables the creation of more sophisticated end-user products, resulting in a significant reduction in discrete system components and a lower bill of materials (BOM).

An advanced PWM switching pattern forces ZVS QR flyback operation, reducing the turn-on switching losses and optimizing the EMI signature. CoolSET™ SiP also features a sophisticated set of protection features, enabling ease of design-in and allowing customers to create products with a better user experience. The product is qualified for industrial applications according to the relevant tests of JEDEC47/20/22 and is used for auxiliary power supplies in consumer and industrial applications.

Key features:

- Integrated 800 V avalanche rugged CoolMOS™ P7
- Fast start-up with integrated 950 V startup-cell
- Integrated synchronous rectification (SR) driver with typical 10 V output
- Integrated reinforced isolated communication from secondary to primary side
- Integrated general purpose isolated enable signal path from secondary to primary for EM series
- Novel ZVS QR flyback operation for lower switching losses and better EMI signature
- Reliable PWM switching operation by synchronized timing of primary and secondary side SR switch
- Supports primary side wide VCC operating range up to 32 V
- Optimized low supply currents for hysteretic mode operation to reach stand-by power < 30 mW
- Multi-mode control for optimized efficiency across the entire load range
- Minimum switching frequency variation between low and high line to ease design-in
- Maximum on/off time limitation to suppress audible noise during startup and power down
- Primary side cycle-by-cycle maximum peak current limitation
- Primary side 2nd overcurrent protection for entering protection mode
- Auto restart mode for all protections
- Pb-free lead plating, halogen free mold compound, and RoHS compliant

Table 1 Output power of ZVS QR CoolSET™ SiP

Type	Package	Marking	V_{DS}	$R_{DS(on)}$[1]	220 V AC ±20%[2]	85–300 V AC[2]
ICE184LM	PG-DSO-27	E184LM	800 V	0.84 Ω	68 W	45 W
ICE184EM	PG-DSO-27	E184EM	800 V	0.84 Ω	68 W	45 W
ICE186EM	PG-DSO-27	E186EM	800 V	0.48 Ω	89 W	60 W

[1] Max. at T_J = 25°C

[2] Calculated maximum output power rating in an open-frame design at T_a = 50°C, T_J = 125°C (integrated power MOSFET) and using minimum drain pin copper area of 232 mm² in a 2 oz copper single-sided PCB at DRAIN pin and GNDS pin. The output power figure is for selection purposes only. The considered power figure is assuming a system efficiency of 91% and can vary depending on particular system design. Contact a technical expert from Infineon for more information.

3. Overview of ZVS QR flyback converter design

Figure 1 and Figure 2 show a typical circuit of the ICE18xM in a ZVS QR Flyback converter. In this converter, the mains input voltage is rectified by the diode bridge and then smoothed by the capacitor C_{bus} where the bus voltage V_{bus} is available. The transformer has one primary winding W_p, one secondary windings W_s and one auxiliary winding W_a. It does not require an additional circuit to achieve the ZVS function. It is the same as a traditional QR flyback using synchronous rectification.

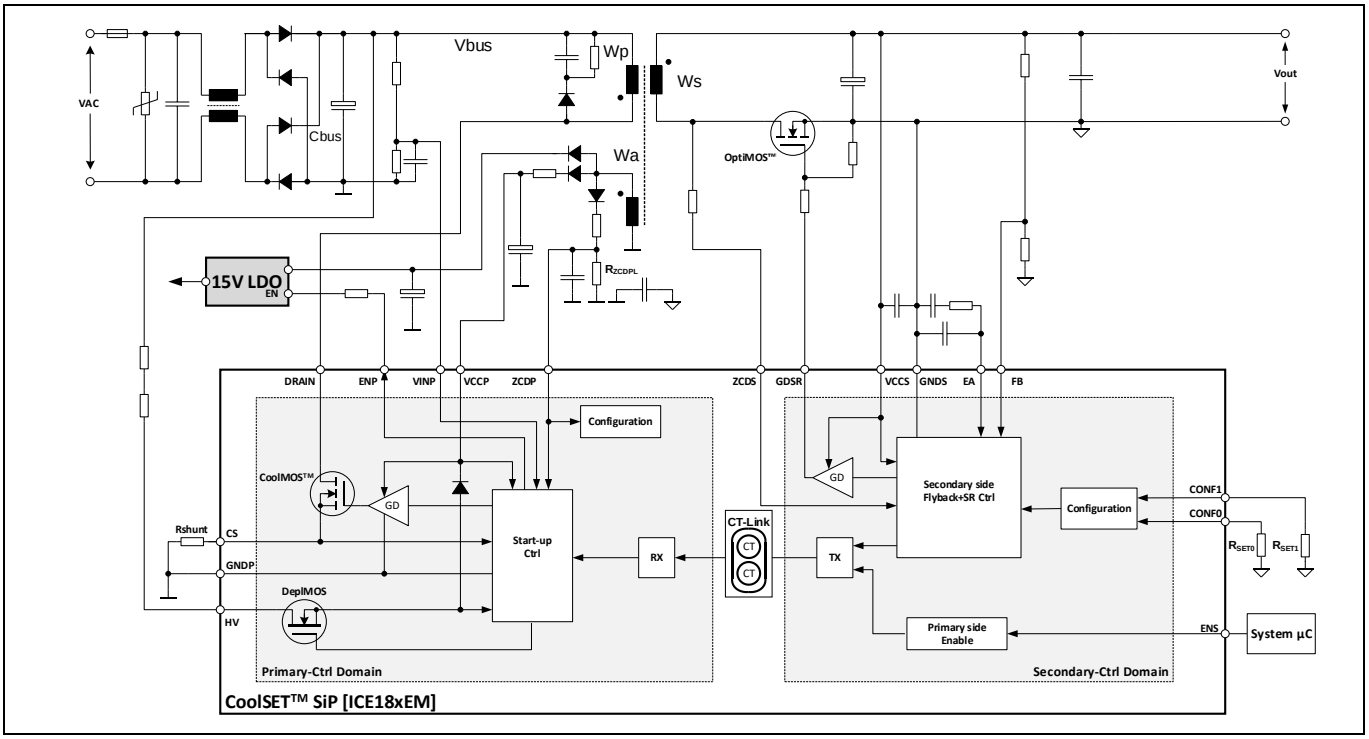


Figure 1 Typical circuit of ICE18xEM

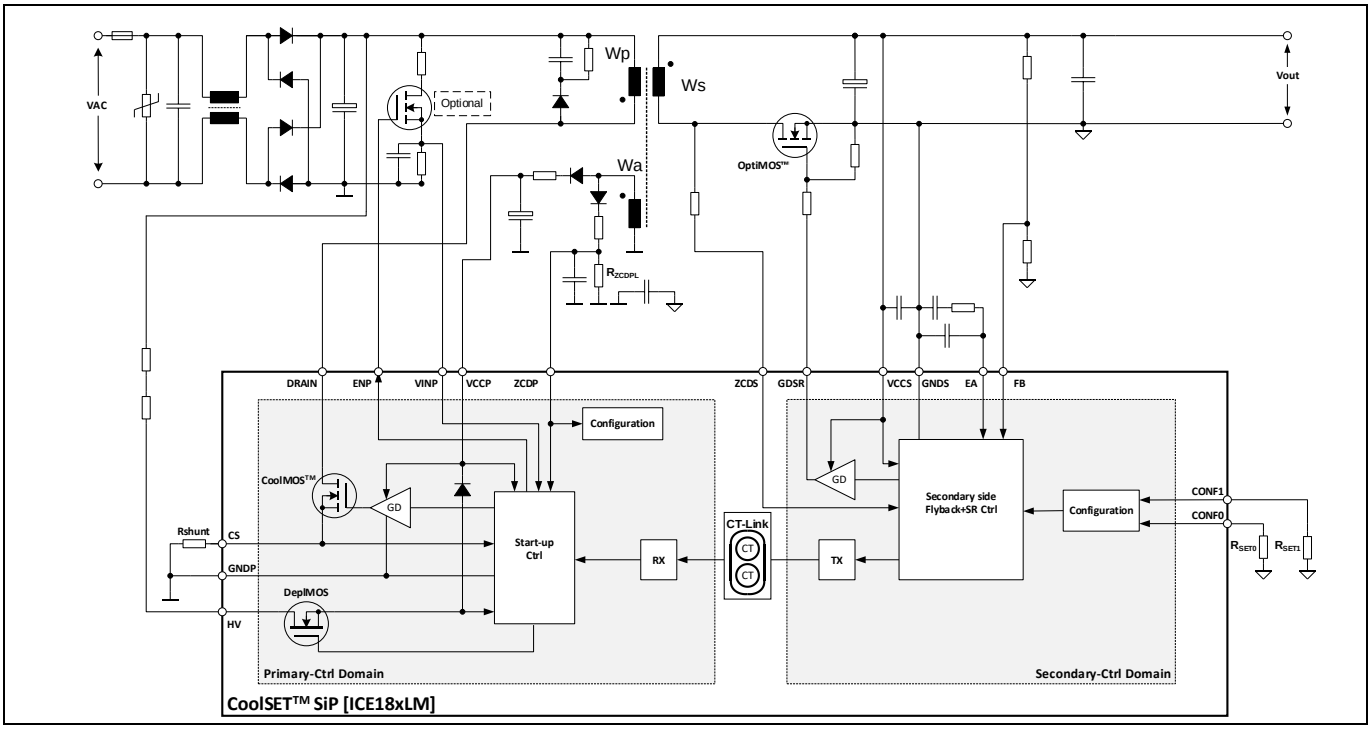


Figure 2 Typical circuit of ICE18xLM

Overview of ZVS QR flyback converter design

The following design guide and calculation will be based on a reference design, REF_60W1_ZVS_186EM, which utilizes the ICE186EM. The design input parameters are as shown in Table 2.

Table 2 Design input parameters

Define input parameters	Parameter	Value	Unit
Minimum AC input voltage	$V_{AC\ Min}$	90	V
Maximum AC input voltage	$V_{AC\ Max}$	264	V
Line frequency	f_{AC}	50/60	Hz
DC ripple voltage at Bulk capacitor	$V_{DC\ Ripple}$	35	V
Output voltage	V_{Out}	12	V
Voltage drop across SR MOSFET	$V_{F\ SR}$	0.1	V
Output current	I_{Out}	5	A
Maximum output power	$P_{Out\ Max}$	72	W (consider overload condition)
Efficiency at low line full load	η	90	% (estimated)
Pre-defined turns ratio	n	8	–
VCCP voltage	V_{VCCP}	18	V
Forward voltage of V_{CC} diode	V_{Daux}	0.3	V
CoolSET™ SiP	CoolSET™	ICE186EM	
Switching frequency at $V_{AC\ Min}$ and $P_{Out\ Max}$	f_s	48	kHz
Total capacitance at MOSFET Drain pin	C_{DS}	200	pF (estimated)

3.1 Primary side design

The primary side design will include the following parts:

- Input capacitance selection
- VCCP capacitance selection
- Transformer design
- Primary side system configuration via resistor R_{ZCDPL}
- HV pin startup resistance selection

3.1.1 Input capacitance selection

To select the input capacitor, we need to calculate the peak voltage of the DC bus at the minimum line voltage. Then, by calculating the discharge time and the RMS current of the circuit, we can calculate the required capacitor value. In the REF_60W1_ZVS_186EM design, the following approach is used:

Min. peak input voltage at no-load condition:

$$V_{DCMinPk} = V_{ACMin} \times \sqrt{2}$$

$$V_{DCMin} = V_{DCMinPk} - V_{DC\_Ripple}$$

$$V_{DCMinPk} = 90V \times \sqrt{2} = 127.28\ V$$

$$V_{DCMin} = 127.28\ V - 35\ V = 92.28\ V$$

Discharging time at each half-line cycle:

$$T_D = \frac{1}{4 \times f_{AC}} \times \left(1 + \frac{sin^{-1}\frac{V_{DCMin}}{V_{DCMinPk}}}{90}\right)$$

$$T_D = \frac{1}{4 \times 60\ Hz} \times \left(1 + \frac{sin^{-1}\frac{92.28\ V}{127.28\ V}}{90}\right) = 6.32\ ms$$

Required energy at discharging time of input capacitor: $W_{IN} = P_{INMax} \times T_D$; $where\ P_{INMax} = \frac{P_{OutMax}}{\eta}$	$W_{IN} = \frac{72\ W}{0.9} \times 6.32\ ms = 0.51\ W \cdot s$
Calculated value of input capacitor: $C_{IN} = \frac{2 \times W_{IN}}{V_{DCMinPk}^2 - V_{DCMin}^2}$	$C_{IN} = \frac{2 \times 0.51\ W \cdot s}{(127.28\ V)^2 - (92.28\ V)^2} = 131.55\ \mu F$
Choose the rated voltage greater than $V_{DCMaxPk}$ $V_{DCMaxPk} = V_{ACMax} \times \sqrt{2}$	$V_{DCMaxPk} = 264\ V \times \sqrt{2} = 373.35\ V$ Choose capacitor rating of 400 V
Choose the capacitance greater than or equal to the calculated C_{IN}	Since C_{IN} = 131.55 µF, choose 68 x 2 µF
Input capacitor:	C_{IN} = 136 µF
Recalculation after input capacitor chosen: $V_{DCMin} = \sqrt{V_{DCMinPk}^2 - \frac{2 \times W_{IN}}{C_{IN}}}$	$V_{DCMin} = \sqrt{(127.28\ V)^2 - \frac{2 \times 0.51\ W \cdot s}{136\ \mu F}} = 93.63\ V$

Note: Special requirements for hold-up time, including cycle skip/drop-out or other factors that affect the resulting minimum DC input voltage and capacitor discharging time, should be considered at this point

3.1.2 VCCP capacitance selection

A 950 V HV start-up cell charges the VCCP capacitor with two constant current sources, $I_{VCCPCharge1}$ and $I_{VCCPCharge2}$, as shown in Figure 3.

- At phase I, a small constant current source, $I_{VCCPCharge1}$, charges the V_{CCP} capacitor until V_{VCCP} reaches $V_{VCCPstart}$, thereby protecting the controller from a VCCP pin short to ground
- At phase II, a higher constant current source, $I_{VCCPCharge2}$, charges the VCCP capacitor until V_{VCCP} exceeds the turn-on threshold, V_{VCCPon}. After that the primary side controller power management module is powered up
- At phase III, the primary controller starts switching with soft-start if V_{BULK} is higher than the brown-in threshold and the primary side controller die junction temperature is lower than the overtemperature threshold, T_{JPOTP}

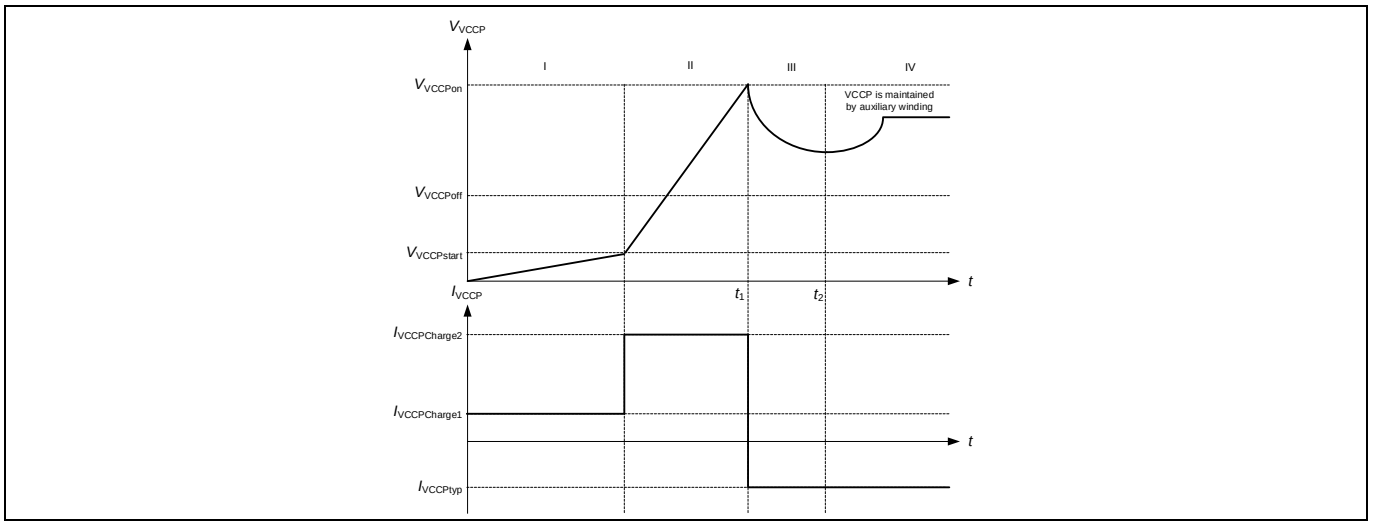


Figure 3 VCCP charging waveform during startup

Overview of ZVS QR flyback converter design

During soft start, the VCCP voltage drops (phase III) due to the IC's power consumption and the initial lack of energy from the auxiliary winding. Once the output voltage is sufficient, the VCCP capacitor is charged by the auxiliary winding, starting at time t2, and supplies $I_{VCCPtyp}$ to the controller. The V_{VCCP} then stabilizes at a constant value, dependent on the output load. When selecting the VCCP capacitance, three key factors should be considered:

- To prevent the VCCP Under Voltage Protection (UVP) during phase III, the capacitance of VCCP capacitor should be selected to store sufficient energy, ensuring that the V_{VCCP} voltage remains above the V_{VCCP} UVP threshold, V_{VCCP_OFF}, until the output voltage is built up after the soft-start time t_{SS}

$$C_{VCCP} > \frac{I_{VCCPtyp} \times t_{ss}}{V_{VCCPon} - V_{VCCPoff}} = \frac{5.1\,mA \times 12\,ms}{20\,V - 9\,V} = 5.6\,uF$$

- To guarantee reliable operation in hysteresis mode, especially under no-load conditions, the chosen capacitance must be sufficient to store enough energy to ensure that the V_{VCCP} voltage remains above the V_{VCCP} UVP threshold, V_{VCCP_OFF} during hysteresis OFF period t_{HMoff}. This value is usually verified through experimentation. In this design, measured t_{HMoff} is about 30ms under no-load condition

$$C_{VCCP} > \frac{I_{VCCPnom} \times t_{HMoff}}{V_{VCCP} - V_{VCCPoff}} = \frac{1.4\,mA \times 30\,ms}{18\,V - 9\,V} = 4.6\,uF$$

- The capacitance of the VCCP capacitor also determines the auto-restart time of a system. This is particularly important in applications where output short conditions can occur, generating excessive heat. To ensure reliable operation, the auto-restart time must be carefully selected to allow sufficient heat dissipation. A typical auto-restart time of 2 seconds is recommended to provide ample time for heat to dissipate, preventing damage to the system (neglect the VCCP charging up time since $I_{VCCPCharge2}$ >> $I_{VCCParm}$)

$$C_{VCCP} > \frac{I_{VCCParm} \times t_{arm}}{V_{VCCPon} - V_{VCCPoff}} = \frac{200\,uA \times 2\,s}{20\,V - 9\,V} = 36.4\,uF$$

Hence, selecting a value of 33uF for VCCP capacitor will be a good choice in this design. To further decouple noise, a 0.1 µF ceramic capacitor should be placed near the VCCP pin.

3.1.3 Transformer design

When designing a flyback transformer, selecting the optimal turns ratio is crucial for efficient and reliable operation. This decision directly impacts the reflected voltage (V_R), which in turn affects the voltage stress on both the primary MOSFET and the secondary rectifier. The key is to strike a balance between these two components. As a starting point, setting V_{RO} around 100 V is suitable for universal input voltage. CoolSET™ SiP products support ZVS QR and valley switching with pre-defined transformer turns ratios. Table 3 lists the supported transformer turns ratios for optimal performance.

Table 3 Option for turns ratio

Option	Turns ratio N_{MAIN} / N_{SEC}
1	5
2	6
3	7
4	8
5	9
6	10

Overview of ZVS QR flyback converter design

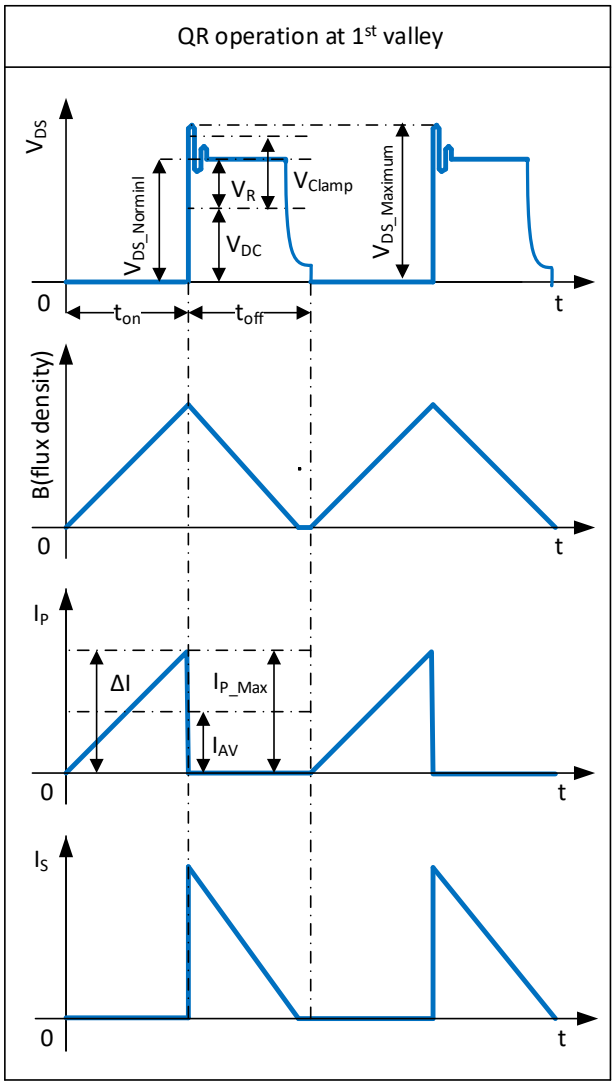


Figure 4 Typical waveforms of QR operation at 1st valley

The REF_60W1_ZVS_186EM design uses a pre-defined turns ratio of 8.

Reflection voltage:

$$V_R = (V_{OUT} + V_{F\,SR}) \times n \qquad V_R = (12\,V + 0.1\,V) \times 8 = 96.8\,V$$

Max. duty cycle:

$$D_{Max} = \frac{V_R}{V_R + V_{DCMin}} \qquad D_{Max} = \frac{96.8\,V}{96.8\,V + 93.63\,V} = 0.51$$

$$L_P = \frac{1}{\left[\frac{1}{V_{DC\,Min}} \times \sqrt{2 \times f_s \times P_{In\,Max}} \times \left(\frac{V_{DC\,Min}}{V_R} + 1\right) + (\pi \times f_s \times \sqrt{C_{DS}})\right]^2} \qquad L_P = \frac{1}{\left[\frac{1}{93.63V} \times \sqrt{2 \times 48kHZ \times 80W} \times \left(\frac{93.63V}{96.8V} + 1\right) + (\pi \times 48kHZ \times \sqrt{100pF})\right]^2} = 280uH$$

$$I_{AV} = \frac{P_{InMax}}{V_{DCMin} \times D_{Max}} \qquad I_{AV} = \frac{80\,W}{93.63\,V \times 0.51} = 1.68\,A$$

Maximum current of primary inductance:

$$I_{PMax} = I_{AV} \times 2 \qquad I_{PMax} = 1.68\,A \times 2 = 3.36\,A$$

RMS current of primary inductance:

Overview of ZVS QR flyback converter design

$$I_{PRMS} = \frac{I_{PMax}}{\sqrt{3}} \times \sqrt{D_{Max}}$$

$$I_{PRMS} = \frac{3.36\ A}{\sqrt{3}} \times \sqrt{0.51} = 1.39\ A$$

Fix max. flux density:
Typically, B_{Max} ≈ 0.3 T–0.4 T for ferrite cross depending on core material.
Choose 350 mT for Material TPW33.

Select core: **RM10**
Material = TPW33
B_S = 400 mT @ 100°C
A_{min} = 98 mm²
BW = 10.5 mm
A_N = 45 mm²
l_N = 38.61 mm

Maximum flux density	B_{Max}	350 mT

Number of primary inductance (cal.):

$$N_{MAIN} \geq \frac{I_{PMax} \times L_p}{B_{Max} \times A_{min}}$$

$$N_{MAIN\_cal} \geq \frac{3.45\ A \times 0.28 \times 10^{-3}\ H}{0.35\ T \times 98 \times 10^{-6}\ m^2} = 28.2\ Turns$$

Number of primary turns:	N_{MAIN}	32 turns

Number of secondary turns (cal.):

$$N_{SEC} = \frac{N_{MAIN} \times (V_{OUT} + V_{F\ SR})}{V_R}$$

$$N_{SEC\_cal} = \frac{32 \times (12\ V + 0.1\ V)}{96.8\ V} = 4\ Turns$$

Number of secondary turns:	N_{SEC}	4 turns

Number of V_{VCCP} turns (cal.):

$$N_{AUX} = \frac{N_{MAIN} \times (V_{VCCP} + V_{Daux})}{V_R}$$

$$N_{AUX\_cal} = \frac{32 \times (18\ V + 0.3\ V)}{96.8\ V} = 6.05\ Turns$$

Number of V_{VCCP} turns:	N_{AUX}	6 turns

Note: The high-voltage V_{VCCP} design is also to supply an external 15 V LDO. If no external supply is required, the number of VCCP turns can be less.

Verification of maximum turn on time, duty cycle and maximum flux density:

Max. turn-on duty cycle:

$$D_{max} = \frac{L_P \times (I_{PMax} - I_{Valley}) \times f_S}{V_{DCmin}}$$

$$D_{max} = \frac{0.28 \times 10^{-3}\ H \times (3.45\ A - 0\ A) \times 48 \times 10^3\ Hz}{93.63\ V} = 0.5$$

Max. flux density:

$$B_{max} = \frac{L_P \times I_{PMax}}{N_{MAIN} \times A_{min}}$$

$$B_{max} = \frac{0.28 \times 10^{-3}\ H \times 3.45\ A}{32 \times 98 \times 10^{-6}\ m^2} = 0.308\ T$$

Max. turn-on time:

$$T_{ON\_max} = \frac{L_P \times (I_{PMax} - I_{Valley})}{V_{DCmin}}$$

$$T_{ON\_max} = \frac{0.28 \times 10^{-3}\ H \times 3.45\ A}{93.63\ V} = 10.33\ us$$

Based on the above system dimensions, Use CoolSET™ SiP calculation tool [2] to get the maximum PWM turn-on time controlled by IC:

$$T_{ON\_max\_controlled} = 11.17\ us$$

Overview of ZVS QR flyback converter design

To deliver full power, make sure:

$$T_{ON\_max} < T_{ON\_max\_controlled}$$

Maximum secondary current:

$$I_{SMax} = I_{PMax} \times \frac{N_{MAIN}}{N_{SEC}}$$

Secondary RMS current:

$$I_{SRMS} = I_{PRMS} \times \sqrt{\frac{1 - D_{Max}}{D_{Max}}} \times \frac{V_R}{V_{Out} + V_{F\,SR}}$$

Refer to CoolSET™ SiP calculation tool [2] to continue wire selection and winding design.

Change switching frequency or turns ratio to iterate if condition on the left is not met.

$$I_{SMax} = 3.45\ A \times \frac{32}{4} = 27.6\ A$$

$$I_{SRMS} = 1.4\ A \times \sqrt{\frac{1 - 0.5}{0.5}} \times \frac{96.8\ V}{12\ V + 0.1\ V} = 11.32\ A$$

3.1.4 Primary side system configuration

The primary side brown-in protection (BI) and brown-out protection (BO) thresholds are configured by the resistor R_{ZCDPL} at the Z_{CDP} pin. Four configurable options are available for setting the paired BI and BO thresholds. The integrated HV start-up cell at the HV pin is used to observe BI and BO, as shown in Figure 5. The external HV start-up resistor at the HV pin forms a resistor divider with the internal shunt resistor $R_{HVshunt}$. The system-level thresholds for BI and BO are set by selecting R_{ZCDPL}. Table 4 shows the options that can be set by R_{ZCDPL}, which is connected between the ZCDP pin and ground.

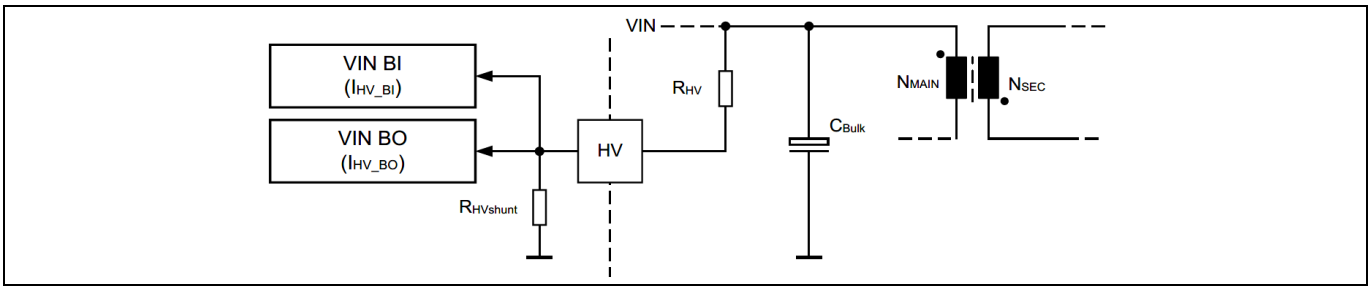


Figure 5 HV pin sensing for brown-in/brownout protection

Table 4 Primary side configuration options

Option	$R_{ZCDPL(min)}$; $R_{ZCDPL(max)}$	Brown-in current threshold I_{HV_BI}	Brownout current threshold I_{HV_BO}	Internal shunt resistor $R_{HVshunt}$
1	[1.00 kΩ; 1.05 kΩ]	2.00 mA	1.40 mA	0.5 kΩ
2	[1.87 kΩ; 2.70 kΩ]	1.00 mA	0.70 mA	1.0 kΩ
3	[4.30 kΩ; 5.00 kΩ]	0.67 mA	0.47 mA	1.5 kΩ
4	[9.20 kΩ; 9.50 kΩ]	0.50 mA	0.35 mA	2.0 kΩ

The different current thresholds for BI and BO enable flexibility in choosing HV start-up resistance, without affecting the BI and BO voltage. However, the HV start-up resistance will limit VCCP charge current at low input voltage, which can impact the overall start-up time. For more information, see the design examples in Section 3.1.5.

3.1.5 HV pin startup resistance selection

The controller monitors the rectified input voltage through the HV pin, using the integrated 950 V start-up cell and the external HV resistor R_{HV}, connected to the input capacitor, as shown in the HV sensing circuitry for HV brown-in/ brownout protection. To conserve power, the sensing is performed periodically, rather than continuously. The input voltage corresponding to the internal brown-in and brownout current thresholds, I_{HV_BI} and I_{HV_BO}, can be adjusted by modifying the external HV resistor R_{HV}.

The design of REF_60W1_ZVS_186EM specifies R_{ZCDPL} as 2 kΩ and the external HV resistor R_{HV} as 115 kΩ (R_{dson} for start-up cell is negligible).

Brown-in voltage:

$$V_{BI} = (R_{HV} + R_{HVshunt}) \times I_{HV\_BI}$$

BI/BO current threshold refer to option 2 in Table 3

$$V_{BI} = (115\ \text{k}\Omega + 1\ \text{k}\Omega) \times 1\ mA = 116\ V$$

Brownout voltage:

$$V_{BO} = (R_{HV} + R_{HVshunt}) \times I_{HV\_BO}$$

$$V_{BO} = (115\ \text{k}\Omega + 1\ \text{k}\Omega) \times 0.7\ mA = 81\ V$$

With an HV resistor R_{HV} = 115 kΩ, the measured total start-up time is around 950 ms in Figure 6.

To achieve a fast start-up and limited impact on existing BI/BO voltage setting, a lower HV start-up resistance can be used here.

Changing R'_{ZCDPL}=1 kΩ and HV resistor R'_{HV}=56 kΩ

Brown-in voltage:

$$V'_{BI} = (R'_{HV} + R'_{HVshunt}) \times I'_{HV\_BI}$$

BI/BO current threshold refer to option 1 in Table 3

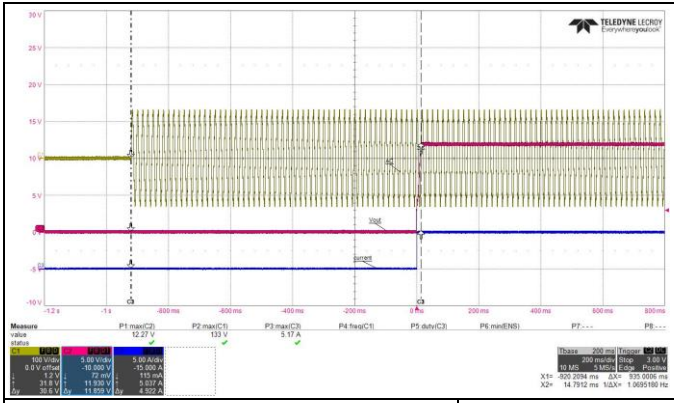
$$V'_{BI} = (56\ \text{k}\Omega + 0.5\ \text{k}\Omega) \times 2\ mA = 113\ V$$

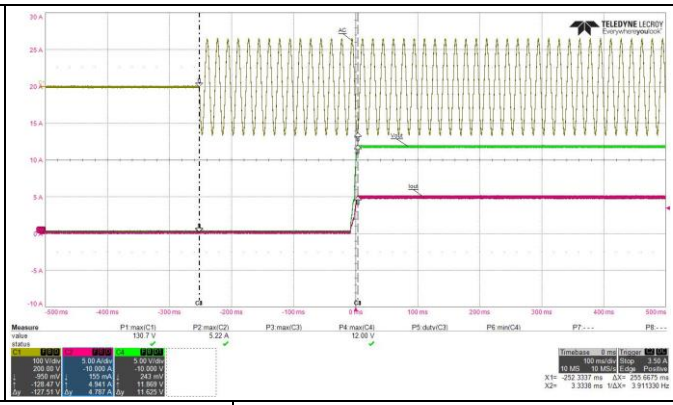
Brownout voltage:

$$V'_{BO} = (R'_{HV} + R'_{HVshunt}) \times I'_{HV\_BO}$$

$$V'_{BO} = (56\ \text{k}\Omega + 0.5\ \text{k}\Omega) \times 1.4\ mA = 79\ V$$

With HV resistor R'_{HV}=56 KΩ, measured total start-up time is reduced to 260 ms in Figure 6 and limited impact on BI/BO voltage.





C1 (yellow) : AC-line voltage	C2 (purple) : +12 V output voltage	C3 (blue) : +12 V output current
90 V AC start-up time at full load is around 950 ms		90 V AC start-up time at full load is around 260 ms
Conditions: R_{HV}=115 kΩ and R_{ZCDPL}=2 kΩ		Conditions: R_{HV}=56 kΩ and R_{ZCDPL}=1 kΩ
Selecting the proper R_{HV} to get the desired start-up time and then choose the appropriate BI/BO current threshold by fitting the right R_{ZCDPL} to determine the BI/BO voltage.		

Figure 6 Start-up time comparison

The combination of R_{HV} and R_{ZCDPL} provides a flexible means of adjusting the start-up time and BI/BO threshold voltage. By fine-tuning these settings, users can tailor the design to meet specific application requirements, resulting in enhanced flexibility and control. In addition, to avoid mis-triggering the brown-out protection, it is required to ensure that the DC bus ripple voltage at brown-in threshold to be smaller than the voltage gap between brown-in voltage and brown-out voltage.

3.1.6 Primary output voltage sensing

The output voltage is sensed indirectly at the ZCDP pin with the relationship shown in the formula after the ringing suppression time in Figure 7.

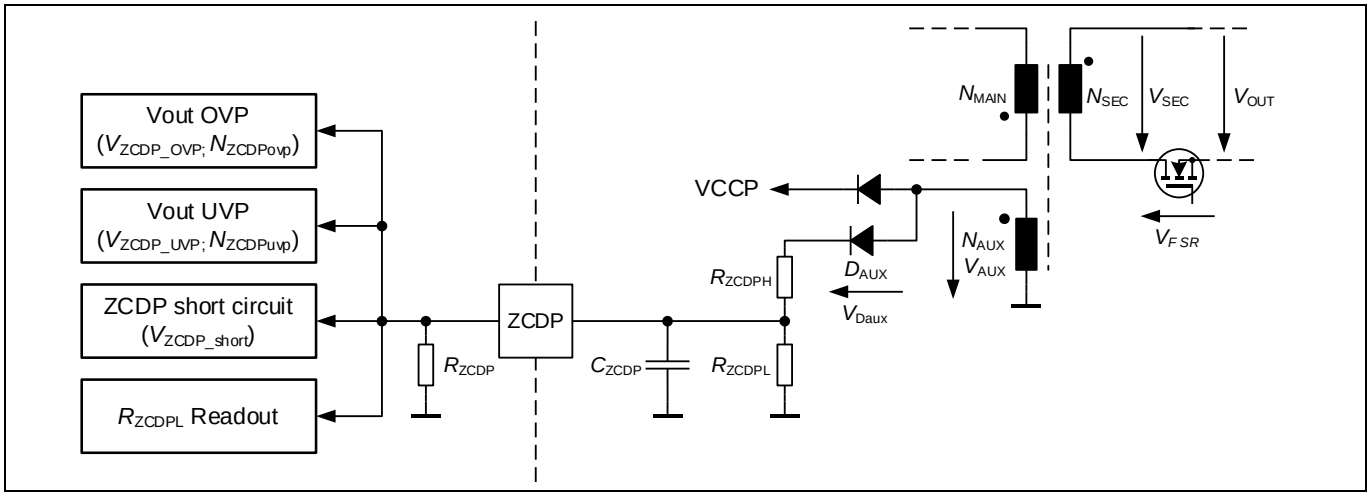


Figure 7 Primary ZCDP pin sensing

$$V_{AUX} = \frac{N_{AUX} \times V_{SEC}}{N_{SEC}} = \frac{N_{AUX}}{N_{SEC}} \times (V_{OUT} + V_{Dsec})$$

During the free-wheeling time and the voltage at the ZCDP pin is given by:

Overview of ZVS QR flyback converter design

$$V_{ZCDP} = R_{ZCDPL} \times (\frac{V_{AUX} - V_{Daux}}{R_{ZCDPH} + R_{ZCDPL}}) = \frac{R_{ZCDPL} \times N_{AUX}}{(R_{ZCDPH} + R_{ZCDPL}) \times N_{SEC}} \times \left(V_{OUT} + V_{F\ SR} - \frac{N_{SEC}}{N_{AUX}} \times V_{Daux}\right)$$

Since R_{ZCDPL} had been already selected in the previous section, choose the right R_{ZCDPH} to set output overvoltage level by solving the equation below.

$$V_{ZCDP\_min} = \frac{R_{ZCDPL} \times N_{AUX}}{(R_{ZCDPH} + R_{ZCDPL}) \times N_{SEC}} \times \left(V_{OUT\_OVP} + V_{F\ SR} - \frac{N_{SEC}}{N_{AUX}} \times V_{Daux}\right)$$

Where, $V_{ZCDP\_OVP\_min}$: Minimum voltage of output overvoltage threshold

V_{OUT_OVP}: user-defined output overvoltage level

The capacitance of C_{ZCDP} is chosen to compensate the delay time which is starting from the drain-source voltage falls below the bus DC voltage level to the ZCDP voltage falls to $V_{ZCDPthr}$ (typical 100 mV). Therefore, the power switch can be turned on at the valley point of the drain-source voltage. The selection of C_{ZCDP} is normally done through experiment.

3.2 Secondary side design

Secondary side design will include the following parts:

- Secondary side system configuration
- ZCDS connection
- Compensation network

3.2.1 Secondary side system configuration

The secondary side controller is configured using two separate resistors connected to the CONF0 and CONF1 pins.

- The CONF0 pin is used to configure the transformer turns ratio, N_{MAIN}/N_{SEC}, between the primary side input winding and the secondary side output winding that supplies VCCS. Refer to Table 5 to select the corresponding resistance for the pre-defined turns ratio. In the REF_60W1_ZVS_186EM design, the transformer turns ratio is fixed at 8. As a result, R_{SET0} should be set to 18 kΩ

Table 5 Resistance for R_{SET0}

Turns ratio N_{MAIN} / N_{SEC}	R_{SET0}
5	3.9 kΩ
6	6.8 kΩ
7	12.0 kΩ
8	18.0 kΩ
9	27.0 kΩ
10	39.0 kΩ

- The CONF1 pin offers six configuration options for optimizing hysteretic mode power

Table 6 Resistance for R_{SET1}

Options	1	2	3	4	5	6
R_{SET1}	3.9 kΩ	6.8 kΩ	12.0 kΩ	18.0 kΩ	27.0 kΩ	39.0 kΩ
EA voltage threshold for entering hysteretic mode (V_{EA_EHM})	0.586 V	0.586 V	0.605 V	0.605 V	0.624 V	0.624 V
EA voltage for pulses during hysteretic mode ($V_{EA\_PWM\_HM}$)	800 mV	900 mV	900 mV	800 mV	900 mV	800 mV
EA voltage hysteretic mode on threshold (V_{EA_HMon})	1.2 V	1.2 V	1.2 V	1.25 V	1.2 V	1.25 V
EA voltage hysteretic mode off threshold (V_{EA_HMoff})	0.9 V	0.9 V	0.9 V	0.8 V	0.9 V	0.8 V

The default selection for R_{SET1} is 3.9 kΩ. The four parameters associated with R_{SET1} are used to optimize hysteretic mode performance. By selecting different V_{EA_EHM} values, users can decide the power level of hysteretic mode; higher V_{EA_EHM} values enable higher hysteretic power. During hysteretic mode, the pulse width is determined by $V_{EA\_PWM\_HM}$, and adjusting this value together with pulse ON/OFF threshold allows for fine-tuning of hysteretic power to achieve optimal standby power.

3.2.2 ZCDS connection

The controller senses the ZCDS pin for SR operation as well as for valley and peak detection. During the primary side turn-on phase, the controller clamps the ZCDS pin to the voltage of the VCCS pin. Therefore, the flowing current represents only the reflected input voltage without output voltage and is determined by the external resistor R_{ZCDS} in this sensing path. This resistor R_{ZCDS} is recommended at 15 kΩ with 1% tolerance.

3.2.3 Compensation network

Figure 8 illustrates the system diagram. An operational transconductance amplifier (OTA) is integrated on the secondary side, and its output voltage is accessible at the EA pin. A Type II compensation network is typically used to ensure sufficient phase margin and bandwidth.

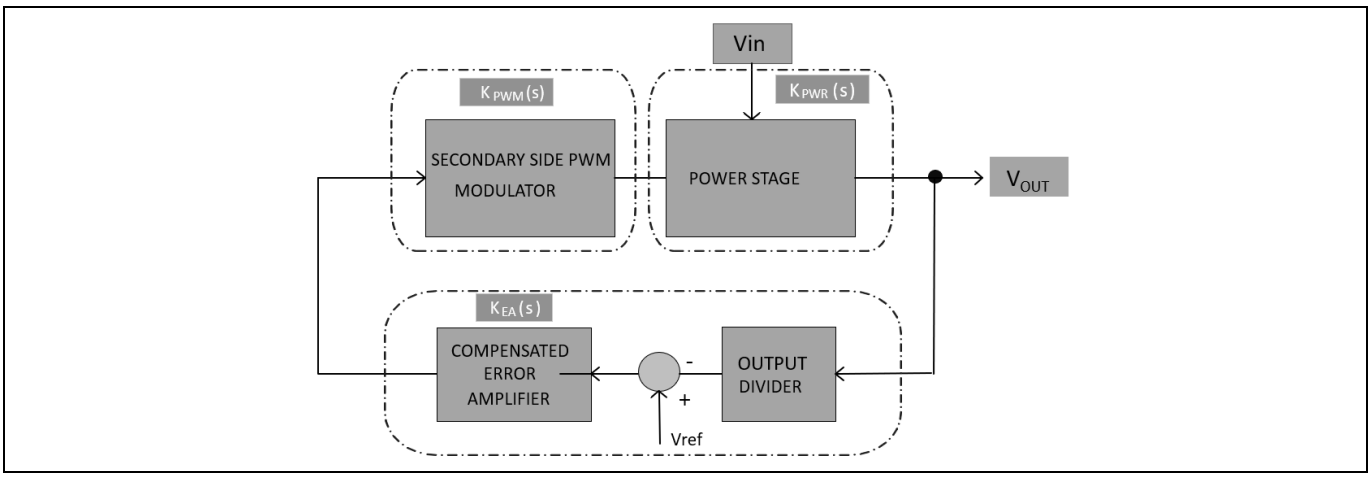


Figure 8 Block diagram of loop element

Overview of ZVS QR flyback converter design

In this system, the open loop function is $K_{OL(s)} = K_{PWR(s)} * K_{EA(s)} * K_{PWM(s)}$

For QR operation, power stage transfer function as follows:

$$K_{PWR}(s) = \frac{\Delta V_{out}}{\Delta I_{peak}} \approx \frac{V_{out}}{I_{peak} \times (1+D)} \times \frac{1 + \frac{s}{2\pi \times f_Z}}{1 + \frac{s}{2\pi \times f_P \times (1+D)}}$$

System zero and pole is as follows:

$$f_Z = \frac{1}{2\pi \times R_{esr} \times C_{out}}$$

$$f_P = \frac{1}{2\pi \times (\frac{R_{out} + R_{esr}}{2}) \times C_{out}} \quad where,\ R_{out} = \frac{V_{out}^2}{P_{out}}$$

For a type II compensation network, the transfer function is as follows:

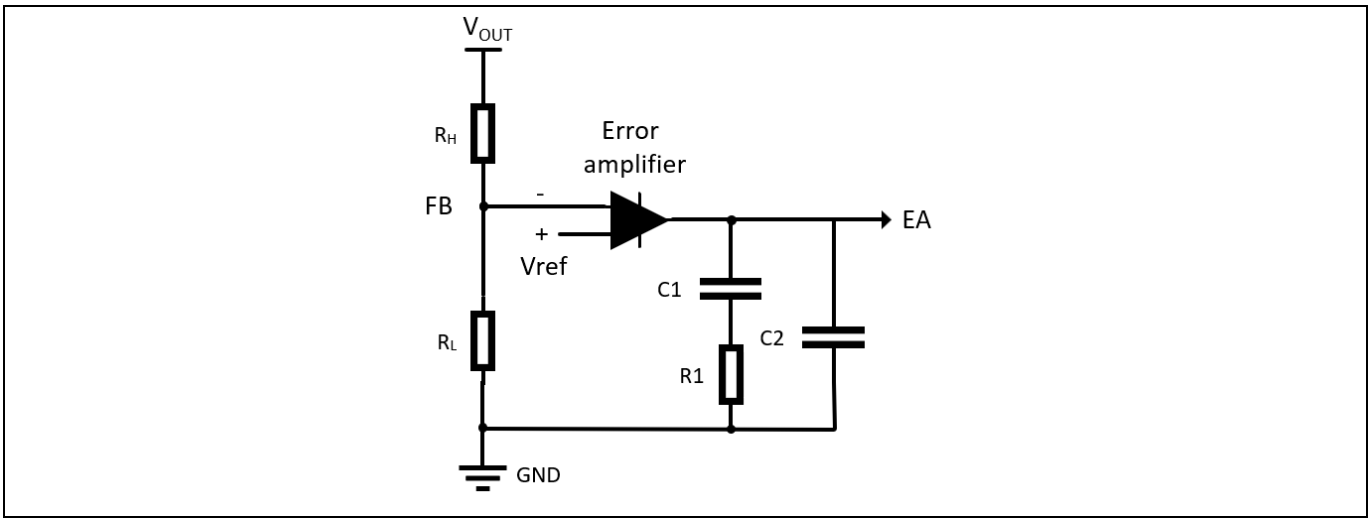


Figure 9 Type II compensation network

$$K_{FB}(s) = \frac{R_L \times G_m}{(R_L + R_H) \times (C_1 + C_2)} \times \frac{1 + \frac{s}{2\pi \times f_{ZC}}}{s \times (1 + \frac{s}{2\pi \times f_{PC}})}$$

Where G_m is the transconductance of error amplifier, typical value 2.8 mA/V.

The Compensator's zero and pole is as follows:

$$f_{ZC} = \frac{1}{2\pi \times R_1 \times C_1}$$

$$f_{PC} = \frac{C_1 + C_2}{2\pi \times R_1 \times C_2 \times C_1} \approx \frac{1}{2\pi \times R_1 \times C_2} \quad (In\ pratice,\ C_1 \gg C_2)$$

For the secondary-side PWM modulator gain, based on the system algorithm, the transfer function as follows:

$$K_{pwm} = \frac{\Delta I_{PK}}{\Delta V_{EA}} = \frac{R_{ZCDS} \times C_{PWM} \times 5696}{L_p} \approx \frac{615}{L_p} \times 10^{-6}\ (Typically\ C_{PWM} = 7.2\ pF\ )$$

The overall open loop transfer function will be rewritten as:

Overview of ZVS QR flyback converter design

$$K_{OL}(s) = \frac{V_{out}}{I_{peak} \times (1+D)} \times \frac{1+\frac{s}{2\pi \times f_Z}}{1+\frac{s}{2\pi \times f_P \times (1+D)}} \times \frac{R_L \times G_m}{(R_L+R_H) \times (C_1+C_2)} \times \frac{1+\frac{s}{2\pi \times f_{ZC}}}{s \times \left(1+\frac{s}{2\pi \times f_{PC}}\right)} \times \frac{615}{L_p} \times 10^{-6}$$

To cancel the pole of plant f_P, place zero of the compensator f_{ZC} in proximity.

The following rules of thumb provide a simple and fast way to iterate f_{cp}, f_{cz}, and f_{cr}:

- Select cross over frequency $f_{cr} < \frac{f_{sw}}{10}$ for general QR flyback
- Choose $f_{ZC} = \alpha^* f_P$ (α=1 to 5) and make sure $f_{ZC} < f_{cr}$
- Choose $f_{PC} = \beta^* f_{cr}$ (β=1 to 5) and make sure $f_{PC} > f_{cr}$
- α and β are the arbitrary value for iteration

By using CoolSET™ SiP calculation tool [2], iteration can be easily processed, and result will be displayed.

Start iteration with the desired cross over frequency f_{cr} = 3 kHz, select α=4, β=2, to calculate unity gain at cross frequency.

$$|K_{OL}(s)| = 1 \; where, \qquad s = 2\pi \times f_{cr}$$

By solving the above equation, the sum of C1 and C2 can be obtained:

$C1_{CAL}$ +$C2_{CAL}$ =102 nF, $R1_{CAL}$=7.27 kΩ;

select C1=68 nF, C2=2.2 nF and R1=20 kΩ.

With the above selected component value, post calculation for compensator zero and pole,

$$f_{PZC} = \frac{1}{2\pi \times R_1 \times C_1} = 120\ Hz$$

$$f_{PPC} = \frac{C_1+C_2}{2\pi \times R_1 \times C_2 \times C_1} \approx \frac{1}{2\pi \times R_1 \times C_2} = 3.73\ kHz$$

substitute the compensator's zero and pole back into the open loop transfer function with unity gain:

Which results $f_{p\_cr} = 3.4\ kHz$.

The lab measurement result, shown in Figure 10, was obtained under the condition of 90 V AC and 60 W load. The results indicate that the actual system cross frequency $f'_{cr} = 2.1\ kHz$, with a phase margin of approximately 52°.

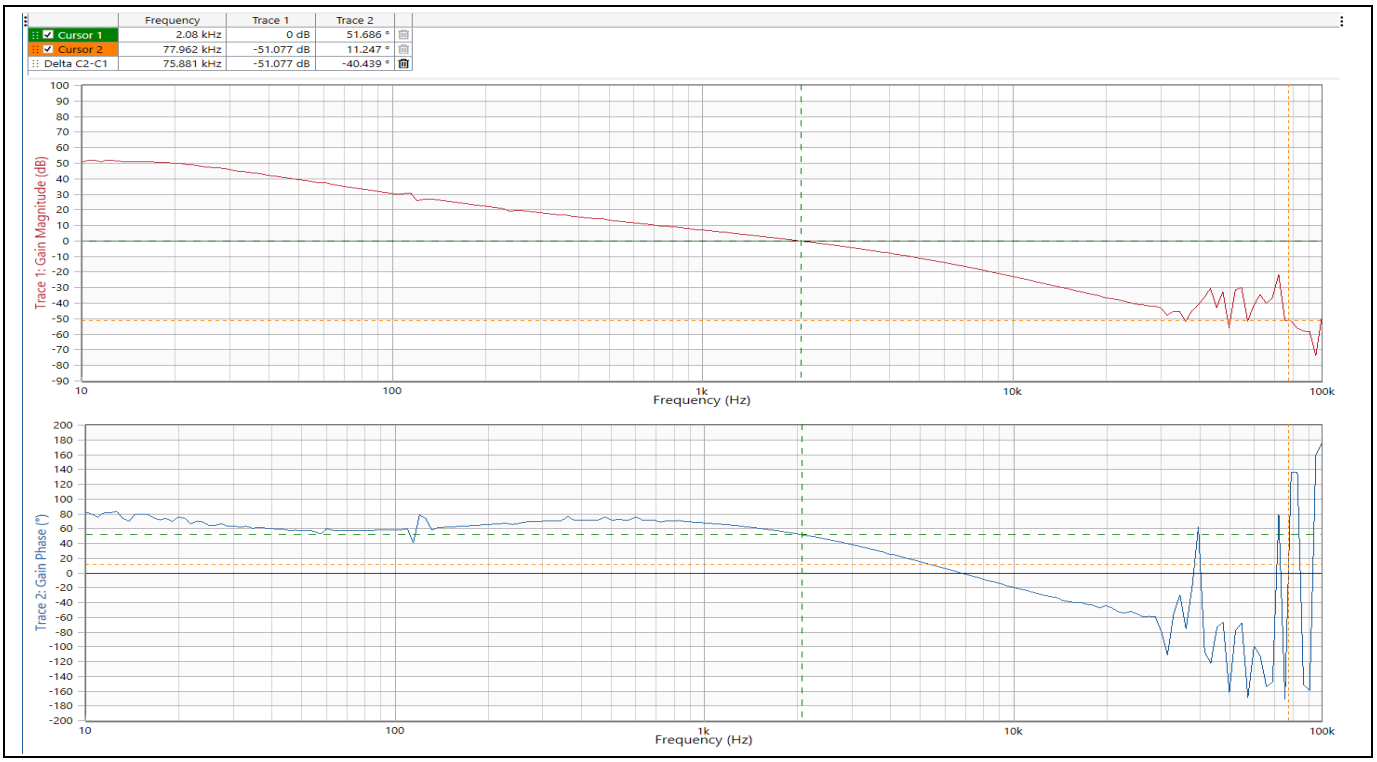


Figure 10 Bode plot of REF_60W1_ZVS_186EM

3.3 Multiple output design considerations

The design for a multiple output power converter is similar to that of a single output converter. The primary side design will remain the same, but attention needs to be paid to the connection of VCCS pin and the selection of R_{SET0} resistor on the secondary side. A dual output design example (V_{OUT1} = 24 V, and V_{OUT2} = 12 V) is introduced here.

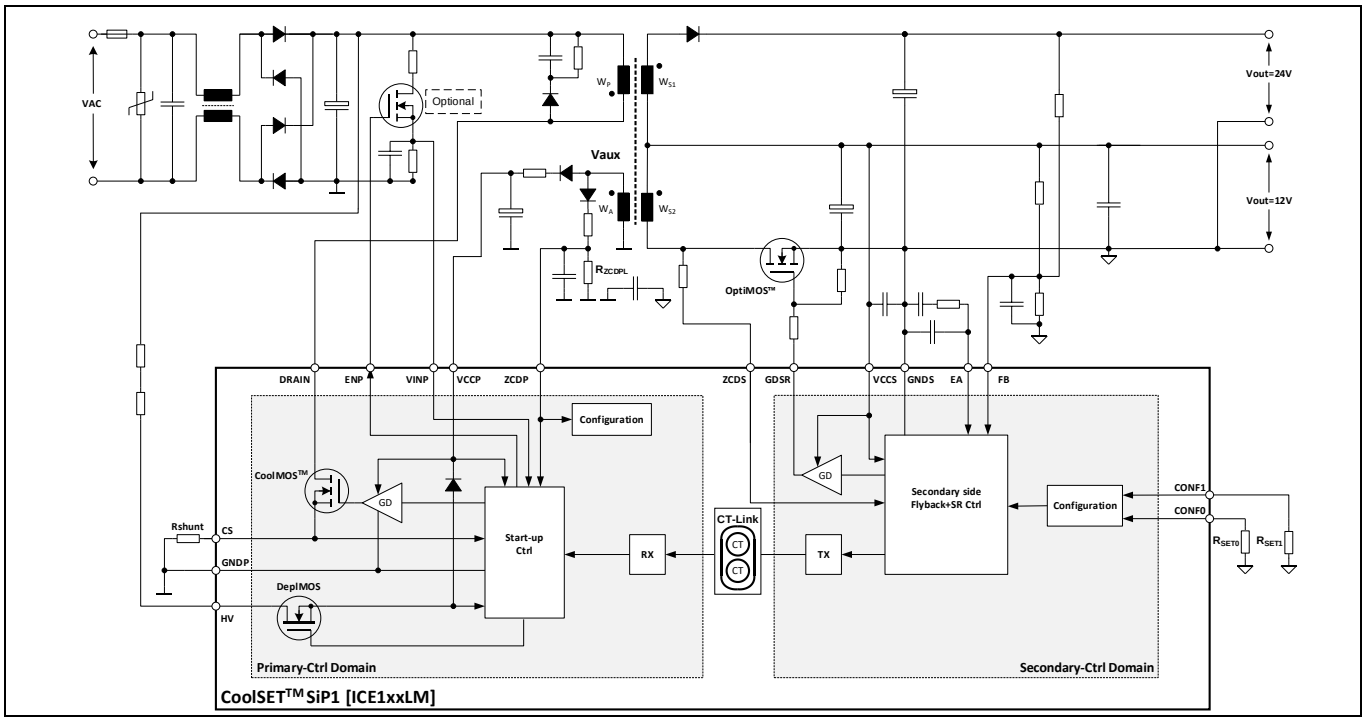


Figure 11 Dual output design circuit

Overview of ZVS QR flyback converter design

In this dual output design, AC-stacked winding is a common choice due to its improved cross-regulation performance. 12 V output voltage is rectified by synchronous rectifier Q1 and 24 V output voltage is rectified by Schottky diode D1. This configuration requires the lower voltage windings (W_{S2}) to carry the combined load current of the entire stack. The gate of Q1 is turned on based on the lower winding voltage sensed via R_{ZCDS} by ZCDS pin of the IC. As a result, the number of turns in the lower stack winding determines the transformer turn ratio. Meantime, the lower stack output is dedicated to supply the VCCS voltage.

In such a case, the turns ratio will be: $n = \frac{W_P}{W_{S2}}$

The resistor R_{SET0} should be selected to follow the above turns ratio.

The resistor R_{FBH1}, R_{FBH2} and R_{FBL} form a voltage divider network which senses the two outputs voltage for better cross regulation. A weight factor should be considered to balance the feedback signals from each output.

When selecting the weight factor, consider the following:

- Output voltage tolerance: If one output voltage has a tighter tolerance requirement, assign a higher weight factor to that output
- Load current: If one output has a higher load current, assign a higher weight factor to that output to ensure adequate voltage regulation
- System performance: If the system performance is more sensitive to one output voltage, assign a higher weight factor to that output

4 PCB layout considerations

For optimal system performance with CoolSET™ SiP, follow these PCB layout recommendations:

- Minimize the loop with pulse-shaped current or voltage; for example, the loop formed by the bus voltage source, primary winding, main power switch and current sense resistor, or the loop consisting of the secondary winding, output diode, and output capacitor, or the loop of the VCC power supply
- Star at the ground of the primary bulk capacitor: all primary grounds should be connected to the ground of the bulk capacitor separately at one point. This can reduce the switching noise entering the sensitive pins of the CoolSET™ SiP device. This can be split into several groups as follows, refer to Figure 12 and Figure 13:
  - Combine the signal grounds (all small-signal grounds connecting to the controller GNDP pin, such as the filter capacitor C7, C8, and C10)
  - Power ground (current sense resistor R9 and R10)
  - The VCCP ground includes the ground of the V_{VCCP} capacitor (C11) and the ground of the auxiliary winding, which is connected to pin 1 of the power transformer
  - The EMI return ground includes the ground of the Y capacitor for isolated flyback applications
  - DC ground from the bridge rectifier BR1
  - To minimize noise and ensure reliable operation, the primary side GNDP pins (2 and 7) are recommended to be connected to a PCB copper plate, and then star connected to the Bulk Cap Ground
- The secondary side GNDS pins (11, 19, and 26) are recommended to be connected jointly to a PCB copper plate, and then star connected to the SR MOSFET source pin
- Place the capacitor (C7, C8, C10, C14 and C15, C17, C21) close to the controller ground (GNDP and GNDS): they should be positioned as close as to the controller ground and the corresponding controller pin to minimize the switching noise coupled into the controller
- High voltage (HV) traces clearance: HV traces, such as startup and drain traces, should maintain sufficient spacing from nearby traces to prevent arcing
- N.C. or N.U. pin can be shorted to GNDS except pin 10 and pin 27 keep opened
- Enough copper area for SR MOS heat dissipation
- A recommended minimum of 232 mm^2 copper area is required at both the primary DRAIN pin and the secondary GNDS pin to ensure better thermal performance of the CoolSET™ SiP

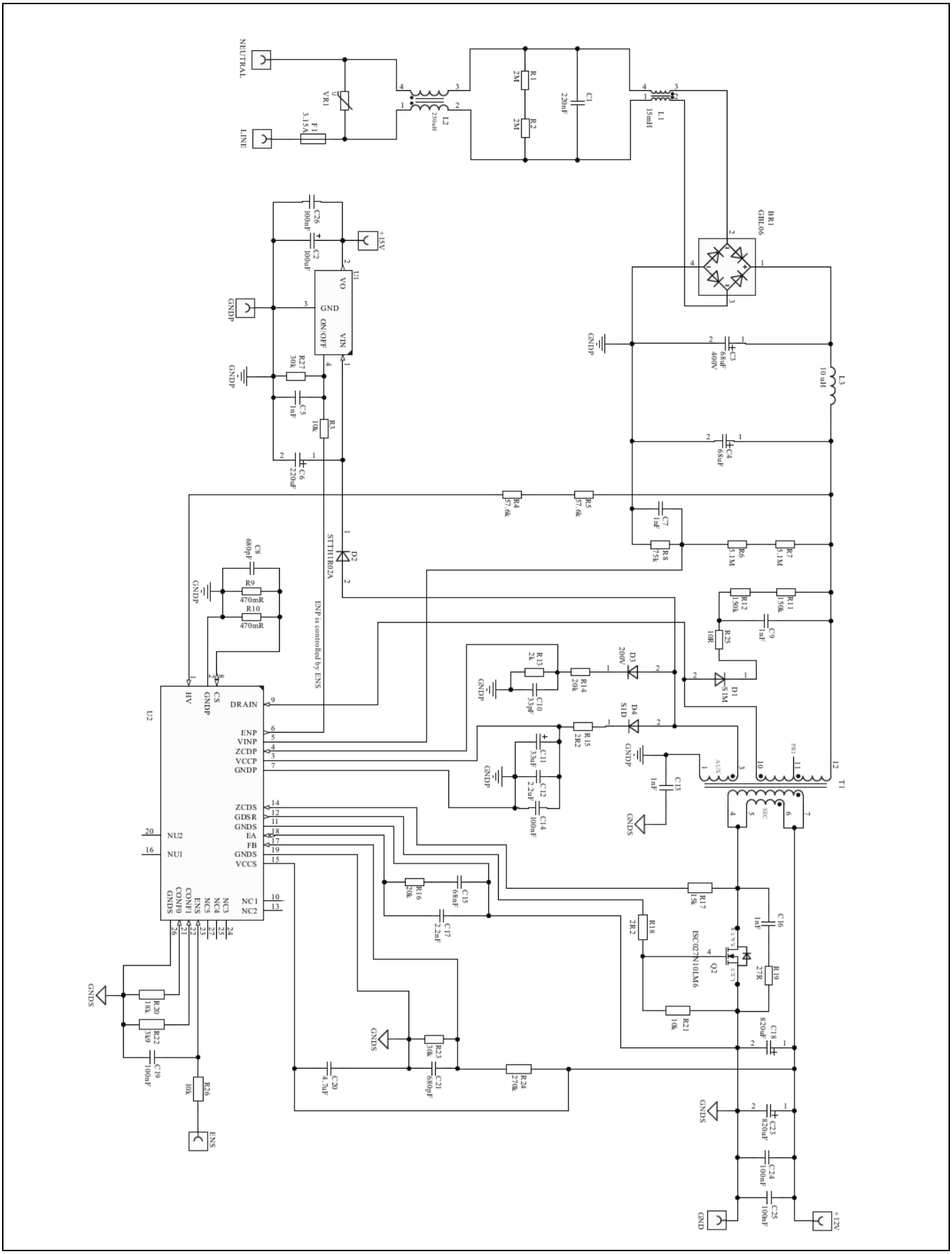


Figure 12 Schematic of REF_60W1_ZVS_186EM

PCB layout considerations

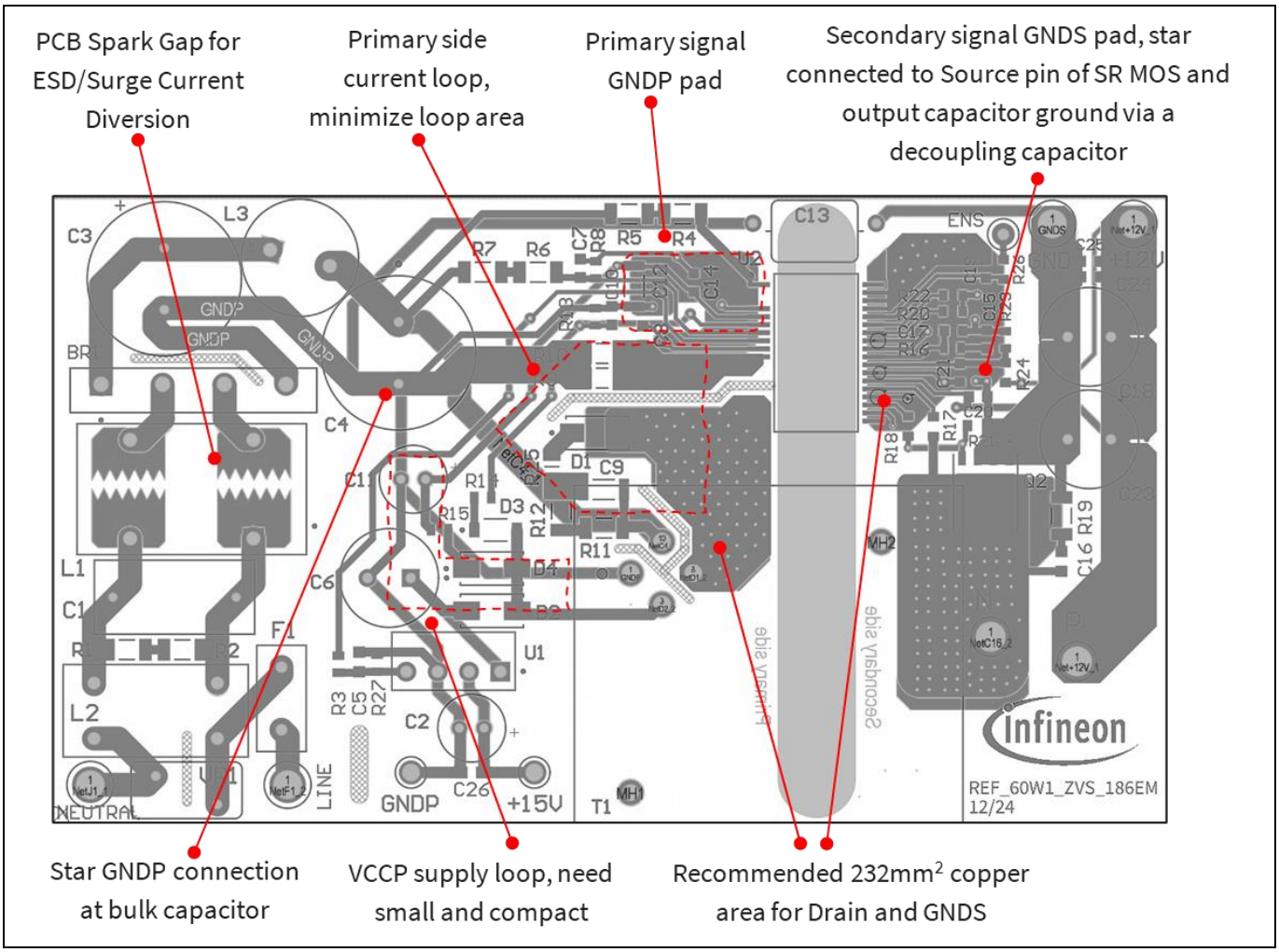


Figure 13 Layout example

References

Contact Infineon Support to obtain these documents.

[1] Infineon Technologies AG: *ICE18xxM datasheet*

[2] Infineon Technologies AG: *Calculation tool CoolSET™ SiP*

Revision history

Document revision	Date	Description of changes
V 1.0	2025-04-14	Initial release

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2025-04-14

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2025 Infineon Technologies AG. All Rights Reserved.

Do you have a question about this document?

Email:

erratum@infineon.com

Document reference

DG033258

Important notice
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings
Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.