

# LTC3644-2

## Quad 17V, 1.25A Synchronous Step-Down Regulator with Ultralow Quiescent Current

### DESCRIPTION

Demonstration circuit 2383A-B features the **LT<sup>®</sup>3644-2**: the wide input and output voltage range, high efficiency and power density, quad 1.25A outputs DC/DC synchronous step-down monolithic regulator. The input voltage range of DC2383A-A is 2.7V to 17V. The default demo board setting of  $V_{OUT1}$ ,  $V_{OUT2}$ ,  $V_{OUT3}$ ,  $V_{OUT4}$  is 1.2V, 3.3V, 2.5V, and 1.8V at 1.25A maximum DC output current per channel. There are two assembly versions. The DC2383A-B features LTC3644-2 which operates at an internally fixed frequency of 2.25MHz (Typ), while the DC2383A-A features LTC3644 which operates at an internally fixed frequency of 1MHz (Typ). Peak current limit is internally fixed at 2.2A typical per channel. Each channel comes with independent run pin control and power good indicators. Phase shift selection of either 0 degree or 180 degrees between switch rising edge of channels 1, 2 and channels 3, 4 is also available.

DC2383A-B provides optional onboard 0Ω jumpers to configure the LTC3644-2 as 4-phase dual 2.5A/2.5A outputs or 4-phase triple 2.5A/1.25A/1.25A outputs. Optional 0Ω jumpers connecting  $V_{IN1}$  to  $V_{IN2}$ ,  $V_{IN3}$ , and

$V_{IN4}$  are available for users to operate selected channels of LTC3644-2 at different input voltages than  $V_{IN1}$ .

A user-selectable MODE/SYNC input is provided to allow users to trade off ripple noise for light load efficiency: pulse-skipping mode (PS) or Burst Mode<sup>®</sup> operation delivers higher efficiency at light load while forced continuous conduction mode (FCM) is preferred for noise sensitive applications. The MODE/SYNC pin can also be used to synchronize the switching frequency to an external clock or set the phase shift between channels 1, 2 and channels 3, 4. Constant frequency, peak current mode control architecture and integrated internal control loop compensation network, allows very fast transient response to line and load changes while maintaining loop stability.

The LTC3644-2 is available in a thermally enhanced, low profile 36-lead 5mm x 5mm BGA package.

It is recommended to read the LTC3644-2 datasheet and demo board manual prior to using or making any changes to DC2383A-B.

**Design files for this circuit board are available.**

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### PERFORMANCE SUMMARY Specifications are at $T_A = 25^\circ\text{C}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range $V_{IN}$		2.7		17	V
Demo Board Default Output Voltages $V_{OUT1}$ , $V_{OUT2}$ , $V_{OUT3}$ , $V_{OUT4}$	$f_{SW} = 2.25\text{MHz}$ Burst Mode $V_{IN} = 2.7\text{V to } 17\text{V}$ ( $V_{OUT} < V_{IN}$ ) $I_{LOAD} = 0\text{A to } 1.25\text{A per Channel}$	1.176 3.234 2.45 1.764	1.2 3.3 2.5 1.8	1.224 3.366 2.55 1.836	V
Default Switching Frequency	Internally Fixed Switching Frequency	1.8	2.25	2.6	MHz
Maximum Continuous Output Current $I_{OUT}$ per Channel $I_{OUT1}$ , $I_{OUT2}$ , $I_{OUT3}$ , $I_{OUT4}$	$f_{SW} = 2.25\text{MHz}$ $V_{IN} = 2.7\text{V to } 17\text{V}$ ( $V_{OUT} < V_{IN}$ ) $V_{OUT} = 1.2\text{V, } 1.8\text{V, } 2.5\text{V, } 3.3\text{V}$	1.25			A
Efficiency at DC	$V_{IN} = 5\text{V}$ $f_{SW} = 2.25\text{MHz}$				%
	$V_{OUT1} = 1.2\text{V at } I_{OUT1} = 1\text{A}$		80.6		
	$V_{OUT2} = 3.3\text{V at } I_{OUT2} = 1\text{A}$		88.1		
	$V_{OUT3} = 2.5\text{V at } I_{OUT3} = 1\text{A}$		86.2		
	$V_{OUT4} = 1.8\text{V at } I_{OUT4} = 1\text{A}$		84.7		

## QUICK START PROCEDURE

Demonstration circuit 2383A-B is easy to set up to evaluate the performance of LTC3644-2. Please refer to Figure 1 for proper measurement equipment setup and follow the test procedures below:

1. With power off, connect the input power supply between  $V_{IN}$  (E1) and GND (E7) turrets.  $V_{IN2}$ ,  $V_{IN3}$  and  $V_{IN4}$  are tied to  $V_{IN1}$  (use onboard  $0\Omega$  jumpers R31, R29 and R30) by default.
2. Connect the first load between  $V_{OUT1}$  (E18) and GND (E20) for channel 1, connect the second load between  $V_{OUT2}$  (E14) and GND (E16) for channel 2, connect the third load between  $V_{OUT3}$  (E15) and GND (E17), connect the fourth load between  $V_{OUT4}$  (E19) and GND (E21). Preset all the loads to 0A.
3. Connect the DMMs between the input test points:  $V_{IN}$  (E1) and GND (E7) to monitor the input voltage. Connect DMMs between  $V_{OUT1}$  (E18) and GND (E20),  $V_{OUT2}$  (E14) and GND (E16),  $V_{OUT3}$  (E15) and GND (E17),  $V_{OUT4}$  (E19) and GND (E21) to monitor the corresponding DC output voltages of channel 1, channel 2, channel 3 and channel 4.
4. Turn on the power supply at the input. Measure and make sure the input supply voltage is 8V. Place the RUN 1 (JP1), RUN2 (JP2), RUN3 (JP5) and RUN4 (JP6) jumpers to the ON position. The output voltages should be 1.2V, 3.3V, 2.5V and 1.8V  $\pm 2\%$  for  $V_{OUT1}$ ,  $V_{OUT2}$ ,  $V_{OUT3}$  and  $V_{OUT4}$ . Four onboard RUN1, RUN2, RUN3 and RUN4 jumpers allow users to enable or disable each channel independently for evaluation purpose. Users need to disable  $V_{OUT2}$  (3.3V) and  $V_{OUT3}$  (2.5V) when varying the input supply voltage down to 2.7V minimum.

**Note on minimum-on time:** In forced continuous mode operation, the minimum on-time of the LTC3644-2 (60ns typical) imposes a minimum duty cycle of 13.5%. For this reason, if lower output channels, such as the default  $V_{OUT1}$  (1.2V) or  $V_{OUT4}$  (1.8V), are enabled and set to forced continuous mode, the input voltage should be limited based on the abovementioned minimum duty cycle requirement. In the rare cases that this minimum on-time is violated, the output voltage may lose regulation. Alternatively, the

user may choose either Burst Mode or pulse-skipping mode operation, or apply a slower external clock to force a slower switching frequency in order to adhere to the minimum on-time limitation.

5. Once the input and output voltages are properly established, adjust the load current within the operating range of 0A to 1.25A max per channel. Observe the output voltage regulation, output voltage ripples, switching node waveform, load transient response and other parameters. Note: To measure the input/output voltage ripples properly, do not use the long ground lead on the oscilloscope probe. Refer to Figure 2 for proper input and output voltage ripple measurement.
6. To program other output voltages for channel 1, channel 2, channel 3 and channel 4, put the RUN1 (JP1), RUN2 (JP2), RUN3 (JP5), RUN4 (JP6) jumpers to the OFF positions, move JP9, JP7, JP8, JP10 to the output voltage marking of USER SEL for each channel. Calculate and insert the bottom feedback resistors at R26, R20, R21 and R27 and repeat step 1 to step 5.
7. **(Option) Operation with Different Input Voltages**

Channel 2, channel 3, and channel 4 can operate with different input voltages than  $V_{IN1}$  and other channels'  $V_{IN}$ . DC2383A-B provides onboard  $0\Omega$  jumpers connecting the main  $V_{IN}$  (or  $V_{IN1}$ ) to  $V_{IN2}$  (R31),  $V_{IN3}$  (R29) and  $V_{IN4}$  (R30) by default. Each of these  $0\Omega$  jumpers can be removed to disconnect  $V_{IN2}$ ,  $V_{IN3}$ ,  $V_{IN4}$  of selected channel from  $V_{IN1}$ . Different input voltages for channel 2, channel 3 and channel 4 should be applied between  $V_{IN2}$  (E23) and GND (E22),  $V_{IN3}$  (E24) and GND (E26),  $V_{IN4}$  (E25) and GND (E26) test points.

Note:  $SV_{IN}$  is the input voltage to power the internal LDO and this pin is tied to  $V_{IN}$  (or  $V_{IN1}$ ) by default. When operating with different channel input voltages, it is important to make sure  $V_{IN1}$  is on and  $INTV_{CC}$  is present.  $SV_{IN}$  can also be disconnected from  $V_{IN1}$  (remove R7) and tied to an external voltage source at test point  $SV_{IN}$  (E2).  $SV_{IN}$  can be a different voltage than  $V_{IN1}$ ,  $V_{IN2}$ ,  $V_{IN3}$ ,  $V_{IN4}$  and should be tied to the highest input supply voltage.

8. **(Option) Frequency Synchronization/Phase Selection:**

## QUICK START PROCEDURE

The MODE/SYNC pin can be used to synchronize the internal oscillator clock frequency to the external clock signal. Place JP3 (MODE/PLLIN) at CLKIN position, apply an external clock signal at CLKIN test point (E10) to vary the switching frequency within  $\pm 50\%$  of the internal programmed frequency.

The MODE/SYNC pin can also be used to set the phase shift between channels 1, 2 and channels 3, 4 while keeping the PHASE pin tied to INTV<sub>CC</sub>. The phase shift can be set by modulating the duty cycle of an external clock on the MODE/SYNC pin. In this case, the phase shift will be determined by the applied external clock rising and falling edges. The switch rising edge of channels 1, 2 is synced to the rising edge of the external clock and switch rising edge of channels 3, 4 synced to the falling edge of the external clock. Crosstalk between channels can be avoided by adjusting the phase shift between channels such that the SW edges do not coincide.

### 9. (Option) 4-Phase Dual 2.5A/2.5A Output Current Configuration:

DC2383A-B can be configured as dual 2.5A/2.5A outputs.

Channel 1 and channel 4 are master channels, channel 2 and channel 3 are slaves.

The following simple modification is required:

1. Tie  $V_{IN1}$ ,  $V_{IN2}$ ,  $V_{IN3}$ ,  $V_{IN4}$  together or tie  $V_{IN1}$  and  $V_{IN2}$ ,  $V_{IN3}$  and  $V_{IN4}$  together if operating channel 1 and channel 2 at different input voltage than that of channel 3 and channel 4. Make sure  $SV_{IN}$  is tied to the highest input supply voltage.
2. Tie SW1 and SW2, SW3 and SW4 together. Since SW1 and SW2, SW3 and SW4 are tied together, there is only one inductor needed for each output voltage rail. Calculate and insert the inductors needed for L1 and L4, remove L2 and L3.
3. Tie FB2 and FB3 to INTV<sub>CC</sub>.

4. Float (do not use) PGOOD2 and PGOOD3. Only PGOOD1 and PGOOD4 are active.
5. Tie RUN1 and RUN2, RUN3 and RUN4 together. Note: Make sure to float all the unused onboard RUN pin jumpers to avoid accidentally shorting  $V_{IN}$  to GND.
6. Tie PHASE pin to INTV<sub>CC</sub>.

Refer to the demo board DC2383A-B schematic for more details.

### 10.(Option) 4-Phase Triple 2.5A/1.25A/1.25A Output Circuit Configuration:

DC2383A-B can be configured as triple 2.5A/1.25A/1.25A outputs.

Channel 1 is master channel, channel 2 is slave. Channel 3 and channel 4 are independent channels.

The following simple modification is required:

1. Tie  $V_{IN1}$ ,  $V_{IN2}$ ,  $V_{IN3}$ ,  $V_{IN4}$  together, or tie  $V_{IN1}$  and  $V_{IN2}$  together, and  $V_{IN3}$  and  $V_{IN4}$  can be at different input voltages than  $V_{IN1}$  and  $V_{IN2}$ . Make sure  $SV_{IN}$  is tied to the highest input supply voltage.
2. Tie SW1 and SW2 together. There is only one inductor needed for this output voltage rail. Calculate and insert the inductor needed for L1 and remove L2.
3. Tie FB2 to INTV<sub>CC</sub>.
4. Float (do not use) PGOOD2. Only PGOOD1, PGOOD3 and PGOOD4 are active.
5. Tie RUN1 and RUN2 together. Note: Make sure to float all unused onboard RUN pin jumpers to avoid accidentally shorting  $V_{IN}$  to GND.
6. Tie PHASE pin to INTV<sub>CC</sub>.
7. Channel 3 and Channel 4 are left unchanged since these two channels operate as independent channels.

Refer to the demo board DC2383A-B schematic for more details.

## QUICK START PROCEDURE

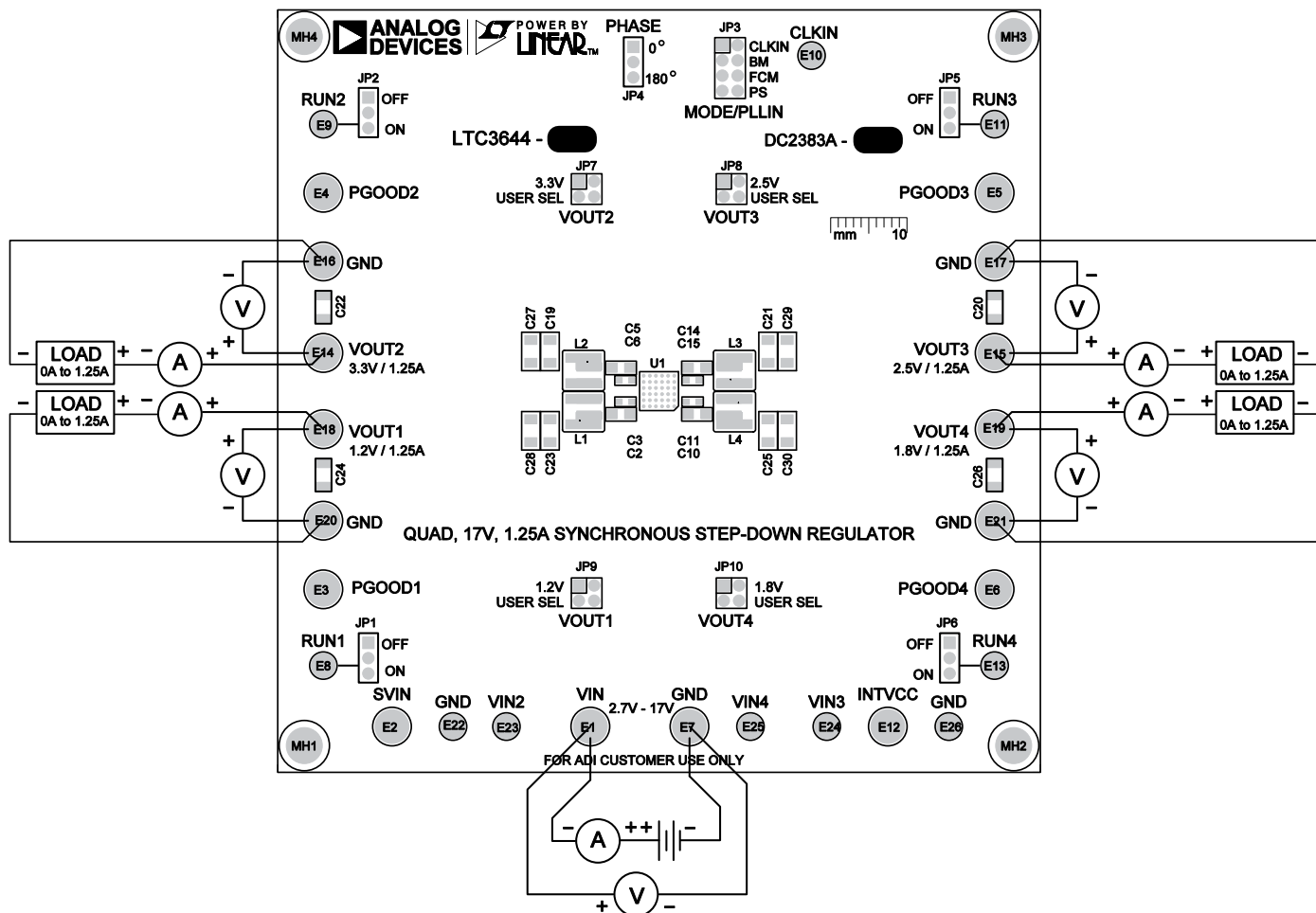


Figure 1. Proper Measurement Equipment Setup

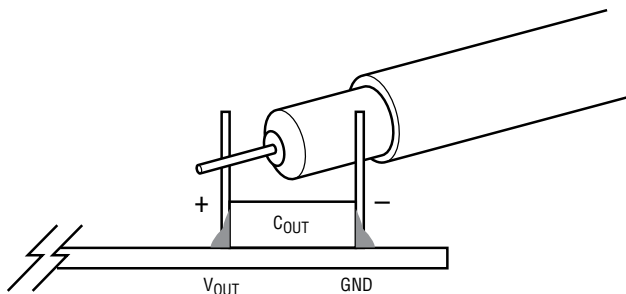
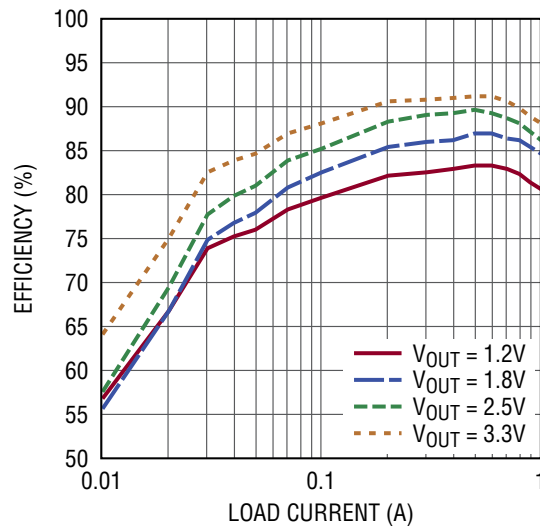
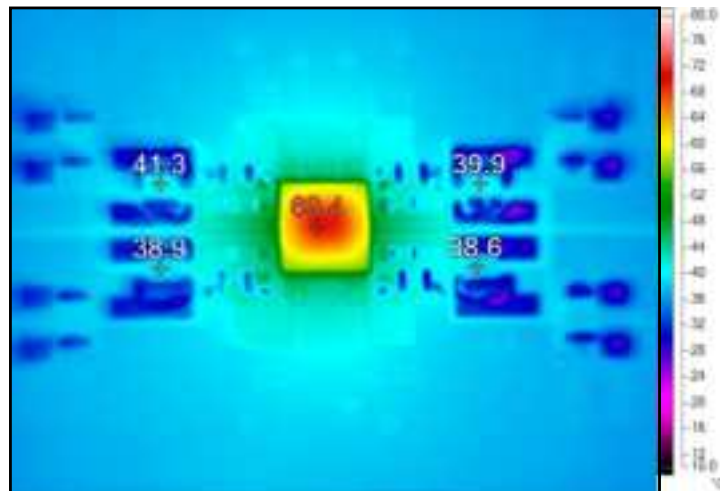


Figure 2. Scope Probe Placement for Measuring Input or Output Voltage Ripples

**QUICK START PROCEDURE**



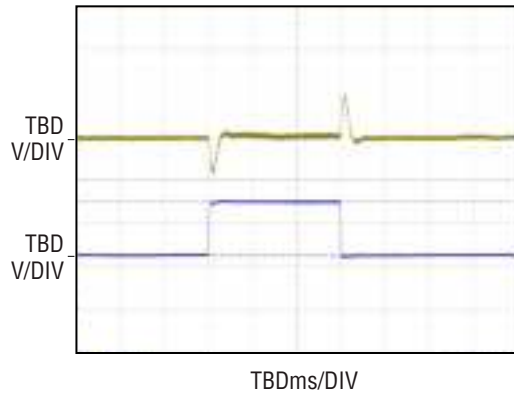
**Figure 3. Measured Efficiency at V<sub>IN</sub> = 5V, f<sub>SW</sub> = 2.25MHz, Burst Mode**



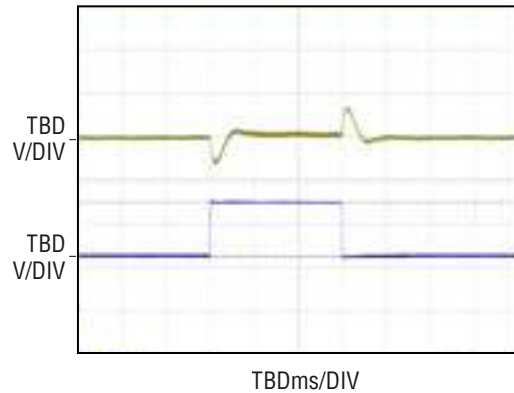
V<sub>OUT1</sub> = 1.2V, V<sub>OUT2</sub> = 3.3V, V<sub>OUT3</sub> = 2.5V, V<sub>OUT4</sub> = 1.8V  
 I<sub>LOAD</sub> = 1.25A per Channel  
 T<sub>A</sub> = 25°C, No Heat Sink, No Forced Airflow

**Figure 4. Thermal Performance at V<sub>IN</sub> = 5V, f<sub>SW</sub> = 2.25MHz**

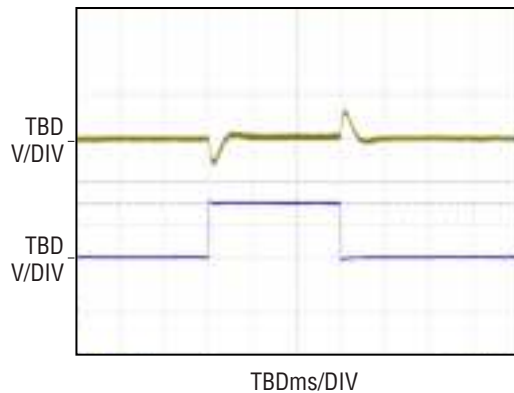
## QUICK START PROCEDURE



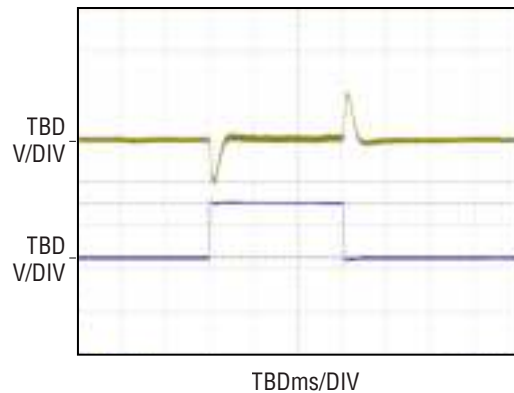
(a) Load Transient Response:  $V_{IN} = 8V$ ,  $V_{OUT} = 1.2V$



(b) Load Transient Response:  $V_{IN} = 12V$ ,  $V_{OUT} = 1.8V$



(c) Load Transient Response:  $V_{IN} = 12V$ ,  $V_{OUT} = 2.5V$



(d) Load Transient Response:  $V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$

Figure 5. Load Transient Responses

Load Transient Response Test Conditions:

$f_{SW} = 2.25MHz$  Typical

$V_{OUT1} = 1.2V$ ,  $V_{OUT2} = 3.3V$ ,  $V_{OUT3} = 2.5V$ ,  $V_{OUT4} = 1.8V$

$L1 = L4 = 1\mu H$

$L2 = L3 = 2.2\mu H$

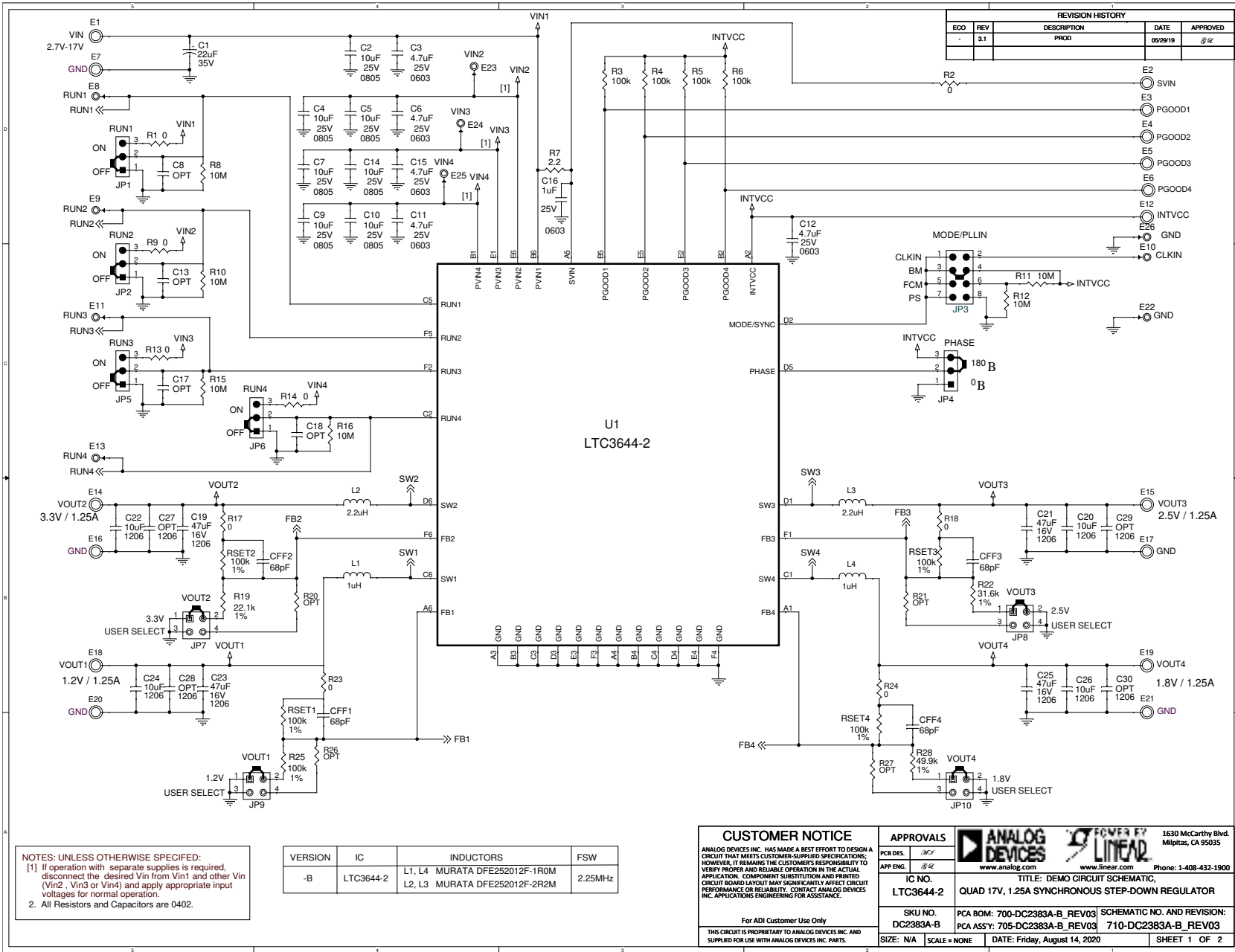
Load Step = 0.625A to 1.25A at  $di/dt = 1A/\mu s$

$CO_{UT\_ceramic} = 1 \times 47\mu F/1206 + 1 \times 10\mu F/1206$  (per Channel)

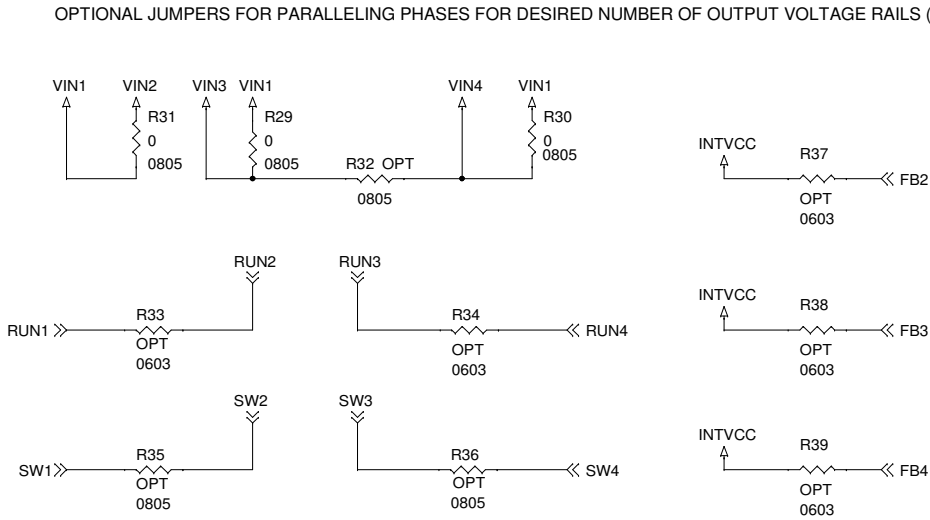
Feedforward Capacitor:  $CFF = 68pF$  (per Channel)

## PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
<b>Required Circuit Components</b>				
1	4	CFF1, CFF2, CFF3, CFF4	CAP, 0402 68pF 5% 50V COG	MURATA, GRM1555C1H680JA01D
2	1	C1	CAP, 2917 22uF 20% 35V TANT	AVX, TPSE226M035R0125
3	7	C2, C4, C5, C7, C9, C10, C14	CAP, 0805 10uF 10% 25V X5R	MURATA, GRM21BR61E106KA73L
4	5	C3, C6, C11, C12, C15	CAP, 0603 4.7uF 20% 25V X5R	MURATA, GRM188R61E475ME11D
5	1	C16	CAP, 0603 1uF 10% 25V X7R	MURATA, GRM188R71E105KA12D
6	4	C19, C21, C23, C25	CAP, 1206 47uF 10% 16V X5R	MURATA, GRM31CR61C476ME44L
7	4	C20, C22, C24, C26	CAP, 1206 10uF 10% 25V X7R	KEMET, C1206C106K3RACTU
8	2	L1, L4	IND, 1uH	MURATA, DFE252012F-1R0M
9	2	L2, L3	IND, 2.2uH	MURATA, DFE252012F-2R2M
10	5	RSET1, RSET2, RSET3, RSET4, R25	RES, 0402 100K OHM 1% 1/16W	PANASONIC, ERJ2RKF1003X
11	9	R1, R2, R9, R13, R14, R17, R18, R23, R24	RES, 0402 0 OHM JUMPER	VISHAY, CRCW04020000Z0ED
12	4	R3, R4, R5, R6	RES, 0402 100k OHMS 1% 1/16W	VISHAY, CRCW0402100KFKED
13	1	R7	RES, 0402 2.2 OHMS 1% 1/16W	VISHAY, CRCW04022R20FNED
14	6	R8, R10, R11, R12, R15, R16	RES, 0402 10M OHMS 1% 1/16W	VISHAY, CRCW040210M0FKED
15	1	R19	RES, 0402 22.1K OHMS 1% 1/16W	VISHAY, CRCW040222K1FKED
16	1	R22	RES, 0402 31.6K OHM 1% 1/16W	VISHAY, CRCW040231K6FKED
17	1	R28	RES, 0402 49.9K OHMS 1% 1/16W	VISHAY, CRCW040249K9FKED
18	3	R29, R30, R31	RES, 0805 0 OHM JUMPER	VISHAY, CRCW08050000Z0EA
19	1	U1	IC, QUAD 17V, 1.25A SYNCHRONOUS STEP-DOWN REGULATOR	ANALOG DEVICES, LTC3644EY-2
<b>Additional Demo Board Circuit Components</b>				
1	0	C8, C13, C17, C18	CAP, 0402 OPTION	OPTION
2	0	C27, C28, C29, C30	CAP, 1206 OPTION	OPTION
3	0	R20, R21, R26, R27	RES, 0402 OPTION	OPTION
4	0	R32	RES, 1206 OPTION	OPTION
5	0	R33, R34, R37, R38, R39	RES, 0603 OPTION	OPTION
6	0	R35, R36	RES, 0805 OPTION	OPTION
<b>Hardware: For Demo Board Only</b>				
1	16	E1, E2, E3, E4, E5, E6, E7, E12, E14, E15, E16, E17, E18, E19, E20, E21	TURRET	MILL-MAX, 2501-2-00-80-00-00-07-0
2	10	E8, E9, E10, E11, E13, E22, E23, E24, E25, E26	TURRET	MILL-MAX, 2308-2-00-80-00-00-07-0
3	5	JP1, JP2, JP4, JP5, JP6	HEADER, 3PIN, 2mm	WURTH, ELEKTRONIK, 62000311121
4	1	JP3	HEADER, 2X4PINS 2mm	WURTH, ELEKTRONIK, 62000821121
5	4	JP7, JP8, JP9, JP10	HEADER, 2PIN, DBL ROW 2mm	WURTH, ELEKTRONIK, 62000421121
6	4	MH1, MH2, MH3, MH4	STANDOFF, SNAP ON 12.7mm	WURTH, ELEKTRONIK, 702935000
7	10	XJP1, XJP2, XJP3, XJP4, XJP5, XJP6, XJP7, XJP8, XJP9, XJP10	SHUNT, 2mm	WURTH, ELEKTRONIK, 60800213421







NUMBER OF OUTPUT VOLTAGE RAILS	Paralleling Channel	Master Channel	0 OHM (Required)	OPT (Do not stuff)	PHASE (JP13)
QUAD 1.25A	4	1/2/3/4		R33, R34, R35, R36, R37, R38, R39	INTVCC
TRIPLE 2.5A/1.25A/1.25A	3	1+2/3/4	1	R33, R35, R37	INTVCC
DUAL 2.5A/2.5A	2	1+2/3+4	1, 4	R33, R34, R35, R36, R37, R38	INTVCC

**NOTE:**  
Please refer to the data sheet and demo board manual for more details and examples of paralleling phases to obtain the desired number of output voltage rails.

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		<p>IC NO. LTC3644-2</p>				
<p>SKU NO. DC2383A-B</p>		<p>PCA BOM: 700-DC2383A-B_REV03 PCA ASSY: 705-DC2383A-B_REV03</p>		<p>SCHEMATIC NO. AND REVISION: 710-DC2383A-B_REV03</p>		
SIZE: N/A	SCALE = NONE	DATE: Friday, August 14, 2020	SHEET 2 OF 2			

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**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS (\$100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.