UCD3138 Control Theory

UCD3138 Digital Controller
Control Theory

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2 Scope

This document provides an overview of digital control and describes fundamental algorithms needed to model the frequency response of a switch mode power supply. It also explains how to use the resulting models and algorithms to calculate the compensation coefficients for a UCD3138 device.

The UCD3138 is optimized for offline and isolated switch mode power conversion applications. It is capable of controlling both single loop and multi-loop systems. Four application examples are given to illustrate the modeling and loop compensation procedures.

1. PFC circuit
2. Buck converter with voltage mode control,
3. Voltage mode control buck converter with internal current loop (to be completed at a later date)
4. Peak current mode control phase shifted full bridge (to be completed at a later date)

Each section will provide the theory as well as the specific algorithms used by the Texas Instruments *Fusion Digital Designer* software [14].

3 Fundamentals of Digital Control

Analog control, as shown in figure 1, uses discrete components, such as resistors, capacitors and operational amplifiers to generate a control effort, u(t). This output is used to command a plant's output, y(t) to match a reference, r(t), through a sensor, H(s). These controllers are continuous in nature and lend themselves to easy analysis with Laplace transforms.

In its simplest form a digital controller implements these analog control laws with difference equations. There are a variety of ways to design a controller for a digital system. The most popular approaches involve approximating differential equations with discrete difference equations. This effectively maps the familiar analog frequency response characteristics of an analog controller into the discrete domain where they can be easily implemented by digital logic. A typical digital power control system is illustrated in figure 2.

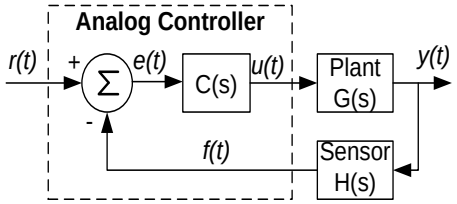


Figure 1: Analog Control Feedback System

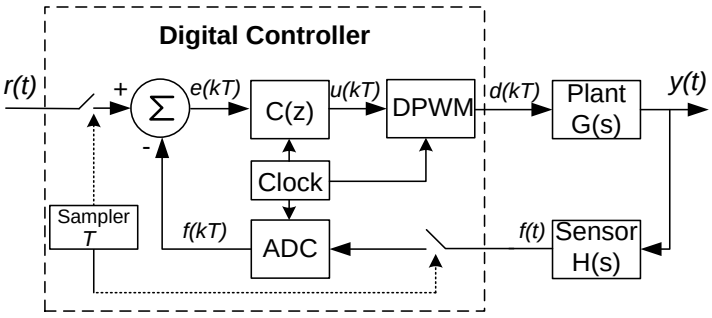


Figure 2: Digital Control Feedback System

3.1 Controller Modeling

In general TI's approach to this problem is to independently model both the plant and the controller. Most often the plant (or power stage) is modeled using the Laplace transform with the appropriate discrete elements added to model system delays and the inherent sampling present in a switch mode power supply [27]. The controller, however, is modeled exactly using difference equations and the z transform. Since the z transform is an exact representation of a digital system, this form of the model is always used to compute performance predictions. An analog representation of the digital filter is used only as an aid to assist the user to configure the controller with more familiar terms. The first part of this paper will explain several methods for approximating discrete time behavior.

3.1.1 Numerical Integration

There are three classic methods for approximating the behavior of a continuous system with a discrete system.

Table 1: Numerical Equivalents

Name	Discrete Approximation	Equation
Forward rectangular rule	$\dot{x(k)} \approx \frac{x(k+1) - x(k)}{T_s}$	(1)

Backward rectangular rule	$\dot{x}(k+1) \approx \frac{x(k+1)-x(k)}{T_s}$	(2)
Bilinear transformation (a.k.a. Tustin's rule, trapezoidal rule)	$\frac{\dot{x}(k)+\dot{x}(k+1)}{2} \approx \frac{x(k+1)-x(k)}{T_s}$	(3)

The next step is to translate equations (1) – (3) into the frequency domain. The derivative operator is replaced by multiplication by the Laplace variable "s" while a unit time delay is replaced by multiplication by the complex variable "z." Appling these rules to the previous three equations yield the following three discrete equivalents.

Table 2: Numerical Equivalents – Transformed

Name	Discrete Approximation	Equation
Forward rectangular rule	$s \approx \frac{z-1}{T_s}$	(4)
Backward rectangular rule	$s \cdot z \approx \frac{z-1}{T_s}$	(5)
Bilinear transformation (a.k.a. Tustin's rule, trapezoidal rule)	$\frac{s+s\cdot z}{2} \approx \frac{z-1}{T_s}$	(6)

Solving equations (4) – (6) for "s" and "z" yields:

Table 3: s and z Approximations

Discrete Approximation	s	z	Equation
Forward rectangular rule	$\frac{z-1}{T_s}$	$s \cdot T_s + 1$	(7)
Backward rectangular rule	$\frac{z-1}{z \cdot T_s}$	$\frac{1}{1-s\cdot T_s}$	(8)
Bilinear transformation (a.k.a. Tustin's rule, trapezoidal rule)	$\frac{2}{T_s}\frac{z-1}{z+1}$	$\frac{s\cdot T_s+2}{2-s\cdot T_s}$	(9)

It should be noted that the bilinear transformation maintains the stability characteristics of the original system. However, this is not necessarily true for the forward and backward transformations. System stability may not match exactly between s domain and z domain. When using the forward difference method, a stable discrete system will yield a stable continuous system; but a stable continuous system can result in an unstable discrete system. When using the backward difference method, a stable continuous system will always yield a stable discrete system. However, a stable discrete system can have an unstable continuous system [13].

3.1.2 Pole Zero Matching

This is an extremely powerful and yet simple method for mapping poles and zeros between the s plane and z plane (and vice versa). The basis for this method uses the exact relationship between z and s.

$$z = e^{s \cdot T_s} \tag{10}$$

Fundamentally, this method forces the pole (or zero) in the s domain to exactly match that pole location in the z domain. A first order Padé approximation of this equation results in the bilinear transform. Details can be found in [21].

3.1.3 Hold Equivalents

3.1.3.1 Zero Order Hold (ZOH)

$$H(z) = (1 - z^{-1}) \cdot Z\left\{\frac{H(s)}{s}\right\} \tag{11}$$

$$ZOH(s) = \frac{(1 - e^{-s \cdot T_s})}{s \cdot T_s} \tag{12}$$

The delay caused by the ZOH, disadvantages the method. It introduces phase lag and distorts the frequency response of the controller. Therefore, it is generally used for plant discretization, where the plant's frequency response is slow, compared with sampling frequency (e.g. 20 times slower).

ZOH has a phase decrease of, $\Delta\varphi = - \omega \cdot T_s / 2$.

3.1.3.2 First Order Hold (FOH) or Triangle-Hold

$$H(z) = \frac{(1 - z^{-1})^2}{z^{-1} \cdot T_s} \cdot Z\left\{\frac{H(s)}{s^2}\right\} \tag{13}$$

3.2 Analog to Digital Conversions

A typical 2 pole 2 zero analog compensator is shown in figure 3.

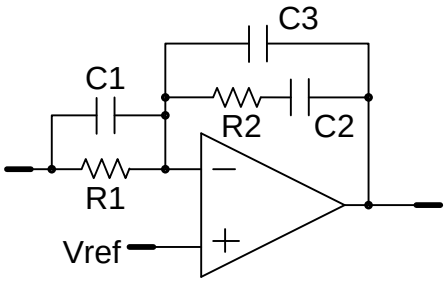


Figure 3: Traditional Analog Compensator

This system has the same number of poles and zeros as the UCD3138 PID based filter. The transfer function of this system is shown in equation (14).

$$G_{AC}(s) = \frac{(R1 \cdot C1 \cdot s + 1)(R2 \cdot C2 \cdot s + 1)}{R1 \cdot s(R2 \cdot C2 \cdot C3 \cdot s + C2 + C3)} \tag{14}$$

A generic second order compensator with real zeros is defined by equations (15).

$$G_{RZ}(s) = K_0 \frac{\left(\frac{s}{\omega_{z1}} + 1\right)\left(\frac{s}{\omega_{z2}} + 1\right)}{s\left(\frac{s}{\omega_{p1}} + 1\right)} \tag{15}$$

A generic second order compensator with complex zeros is defined by equation (16).

$$G_{CZ}(s) = K_0 \frac{\left(\frac{s^2}{\omega_r{}^2} + \frac{s}{Q \cdot \omega_r} + 1\right)}{s\left(\frac{s}{\omega_{p1}} + 1\right)} \tag{16}$$

The variables in these equations are related by equations (17) – (20).

$$\omega_{z1} = \frac{\omega_r}{2 \cdot Q}\left(1 - \sqrt{1 - 4 \cdot Q^2}\right) \tag{17}$$

$$\omega_{z2} = \frac{\omega_r}{2 \cdot Q}\left(1 + \sqrt{1 - 4 \cdot Q^2}\right) \tag{18}$$

$$\omega_r = \sqrt{\omega_{z1} \cdot \omega_{z2}} \tag{19}$$

$$Q = \frac{\sqrt{\omega_{z1} \cdot \omega_{z2}}}{\omega_{z1} + \omega_{z2}} \tag{20}$$

Equation (14) can be equated to equation (15) to derive the following relationships.

$$K_0 = \frac{1}{R1 \cdot (C2 + C3)} \tag{21}$$

$$\omega_{z1} = \frac{1}{R1 \cdot C1} \tag{22}$$

$$\omega_{z2} = \frac{1}{R2 \cdot C2} \tag{23}$$

$$\omega_{p1} = \frac{1}{R2 \cdot \frac{C2 \cdot C3}{C2 + C3}} \tag{24}$$

Equations (21) – (24) can be solved for the resistors and capacitor values shown in figure 3.

$$R1 = \textit{preselected value} \tag{25}$$

$$R2 = \frac{K_0 \cdot R1 \cdot \omega_{p1}}{\omega_{z2} \cdot \left(\omega_{p1} - \omega_{z2}\right)} \tag{26}$$

$$C1 = \frac{1}{R1 \cdot \omega_{z1}} \tag{27}$$

$$C2 = \frac{\omega_{p1} - \omega_{z2}}{K_0 \cdot R1 \cdot \omega_{p1}} \tag{28}$$

$$C3 = \frac{\omega_{z2}}{K_0 \cdot R1 \cdot \omega_{p1}} \tag{29}$$

A generic PID based digital compensator with an extra pole is defined in equation (30).

$$G_{PID}(z) = K_P + K_I \frac{1 + z^{-1}}{1 - z^{-1}} + K_D \frac{1 - z^{-1}}{1 - \alpha \cdot z^{-1}} \tag{30}$$

If equation (30) is converted to the s domain using the bilinear transform and the result equated to equation (15) the following definitions for the PID gain terms can be derived.

$$K_P = \frac{K_0 \cdot \left(\omega_{p1} \cdot \omega_{z1} + \omega_{p1} \cdot \omega_{z2} - \omega_{z1} \cdot \omega_{z2}\right)}{\omega_{p1} \cdot \omega_{z1} \cdot \omega_{z2}} \quad (31)$$

$$K_I = \frac{K_0 \cdot T_s}{2} \quad (32)$$

$$K_D = \frac{2 \cdot K_0 \cdot \left(\omega_{p1} - \omega_{z1}\right)\left(\omega_{p1} - \omega_{z2}\right)}{\omega_{p1} \cdot \omega_{z1} \cdot \omega_{z2}\left(T_s \cdot \omega_{p1} + 2\right)} \quad (33)$$

$$\alpha = \frac{2 - T_s \cdot \omega_{p1}}{T_s \cdot \omega_{p1} + 2} \quad (34)$$

If equation (30) is converted to the s domain using the bilinear transform and the result equated to equation (16) the following definitions for the PID gain terms can be derived.

$$K_P = \frac{K_0 \cdot \left(\omega_{p1} - Q \cdot \omega_r\right)}{Q \cdot \omega_r \cdot \omega_{p1}} \quad (35)$$

$$K_I = \frac{K_0 \cdot T_s}{2} \quad (36)$$

$$K_D = \frac{2 \cdot K_0 \cdot \left(Q \cdot {\omega_{p1}}^2 + Q \cdot {\omega_z}^2 - \omega_{p1} \cdot \omega_z\right)}{Q \cdot \omega_{p1} \cdot {\omega_r}^2\left(T_s \cdot \omega_{p1} + 2\right)} \quad (37)$$

$$\alpha = \frac{2 - T_s \cdot \omega_{p1}}{T_s \cdot \omega_{p1} + 2} \quad (38)$$

Substituting (21) – (24) into (31) – (34) results in the PID coefficients in terms of analog compensator component values:

$$K_P = \frac{C1 \cdot R1(C2 + C3) + C2^2 R2}{R1(C2 + C3)^2} \quad (39)$$

$$K_I = \frac{T_s}{2 \cdot R1(C2 + C3)} \quad (40)$$

$$K_D = \frac{2 \cdot C2^2 R2(C1 \cdot R1(C2 + C3) - C2 \cdot C3 \cdot R2)}{R1(C2 + C3)^2(C2(2 \cdot C3 \cdot R2 + T_s) + C3 \cdot T_s)} \quad (41)$$

$$\alpha = \frac{C2(2 \cdot C3 \cdot R2 - T_s) - C3 \cdot T_s}{C2(2 \cdot C3 \cdot R2 + T_s) + C3 \cdot T_s} \quad (42)$$

For most cases where C2 is very large (i.e. much greater than C1 and C3) the following simplifications result.

$$K_P = \frac{R2}{R1} \quad (43)$$

$$K_I = \frac{T_s}{2 \cdot R1 \cdot C2} \quad (44)$$

$$K_D = \frac{2 \cdot R2(R1 \cdot C1 - R2 \cdot C3)}{R1(2 \cdot R2 \cdot C3 + T_s)} \quad (45)$$

$$\alpha = \frac{2 \cdot C3 \cdot R2 - T_s}{2 \cdot C3 \cdot R2 + T_s} \quad (46)$$

The accuracy of the bilinear approximation is demonstrated in figure 4. The analog compensator's circuit parameters are shown in table 4.

Table 4: Analog Compensation Values

C1	10 nF
R1	15 kΩ
C2	7 nF
R2	2.3 kΩ
C3	700 pF

Using equations (39) – (42) to calculate the PID coefficients yields the results in table 5.

Table 5: Equivalent PID Values

K_P	1.4254
K_I	0.0216
K_D	4.7489
α	-0.2615
f_s	200 kHz

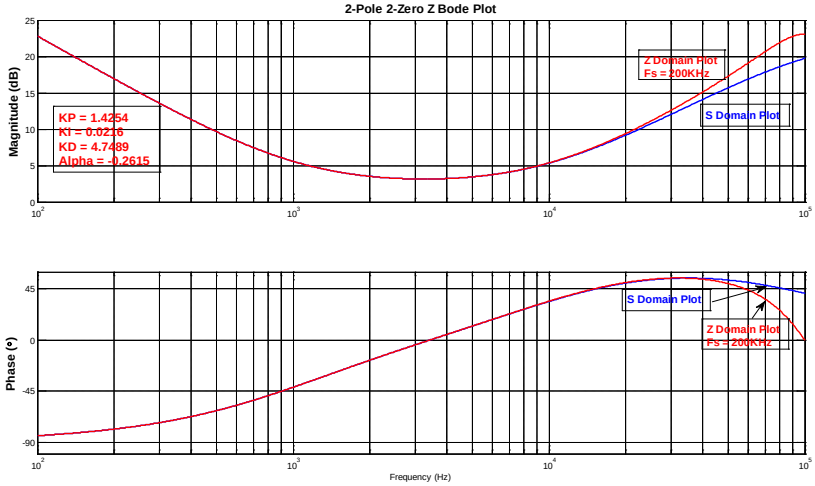


Figure 4: Bilinear Transformation Comparison

The z domain curves match s domain curves very well until the frequency approaches ½ of the sampling rate. Although, the accuracy at high frequencies can be improved by using a higher sampling frequency, the majority of the observed error comes from an inappropriate use of the bi-linear transform. This issue will be discussed in section 3.3.

3.3 z Plane and s Plane Relationships

Figure 5 shows a series of curves from a discrete system with a single pole. Each legend entry shows the value of the pole position in the discrete domain (α) as well as the equivalent pole translated to the frequency domain (f_p) using the bilinear transform.

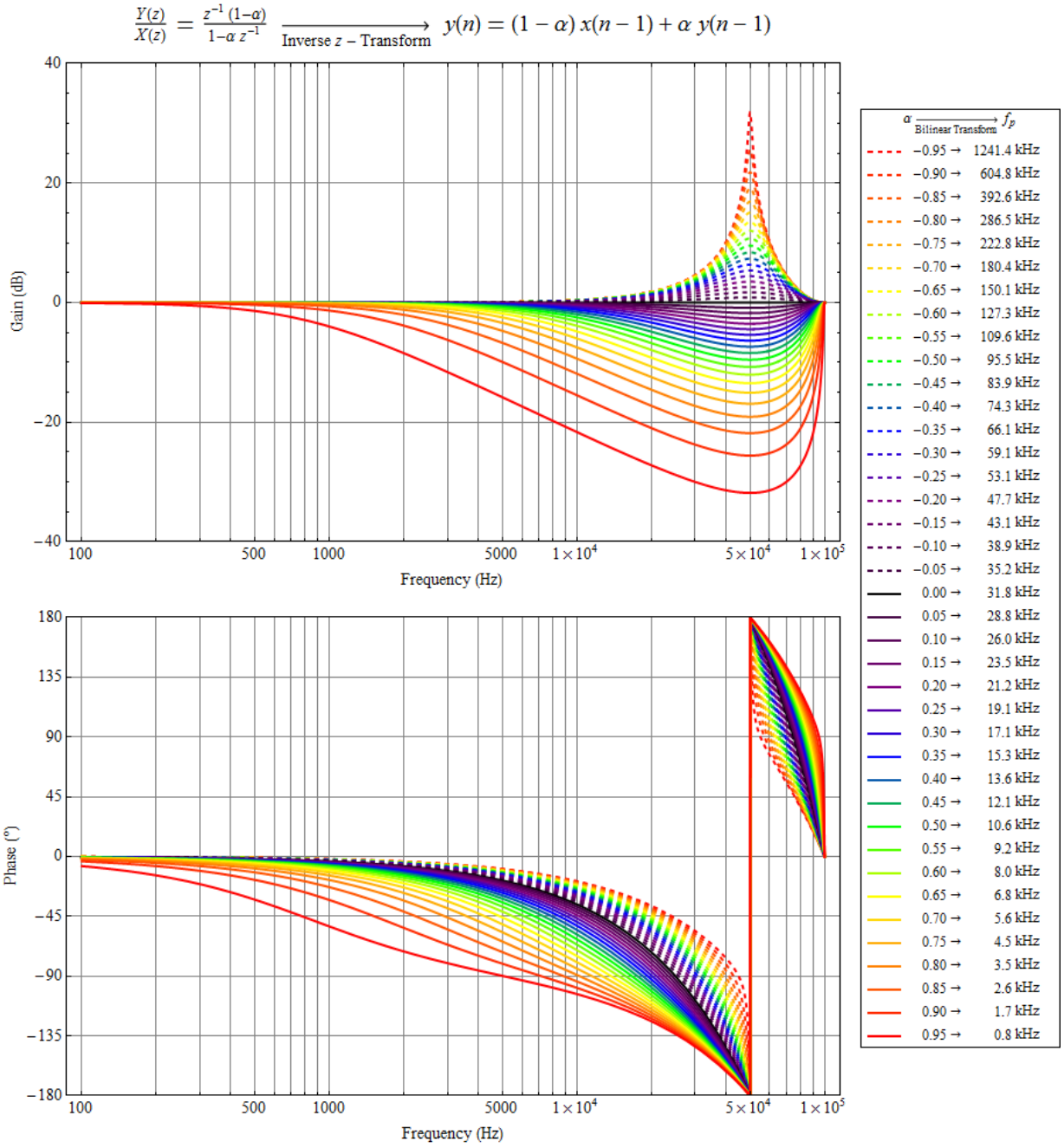


Figure 5: Pole Evaluation of a Discrete Transfer Function

It is essential to notice that the bilinear transform predicts pole locations past the Nyquist point (½ the sample rate) [13]. This is clearly impossible. The resulting curves correctly show that this, in fact, does not happen. On the contrary the system behaves as if there is a pair of complex poles at ½ the sample rate. In order to validate this statement the time domain response of several of the curves from figure 5 are generated and plotted in figure 6. Notice that as α becomes negative the amplitude of the resulting oscillation grows. It could be further shown that the magnitude of this amplitude will increase the closer the excitation frequency gets to ½ the sample rate.

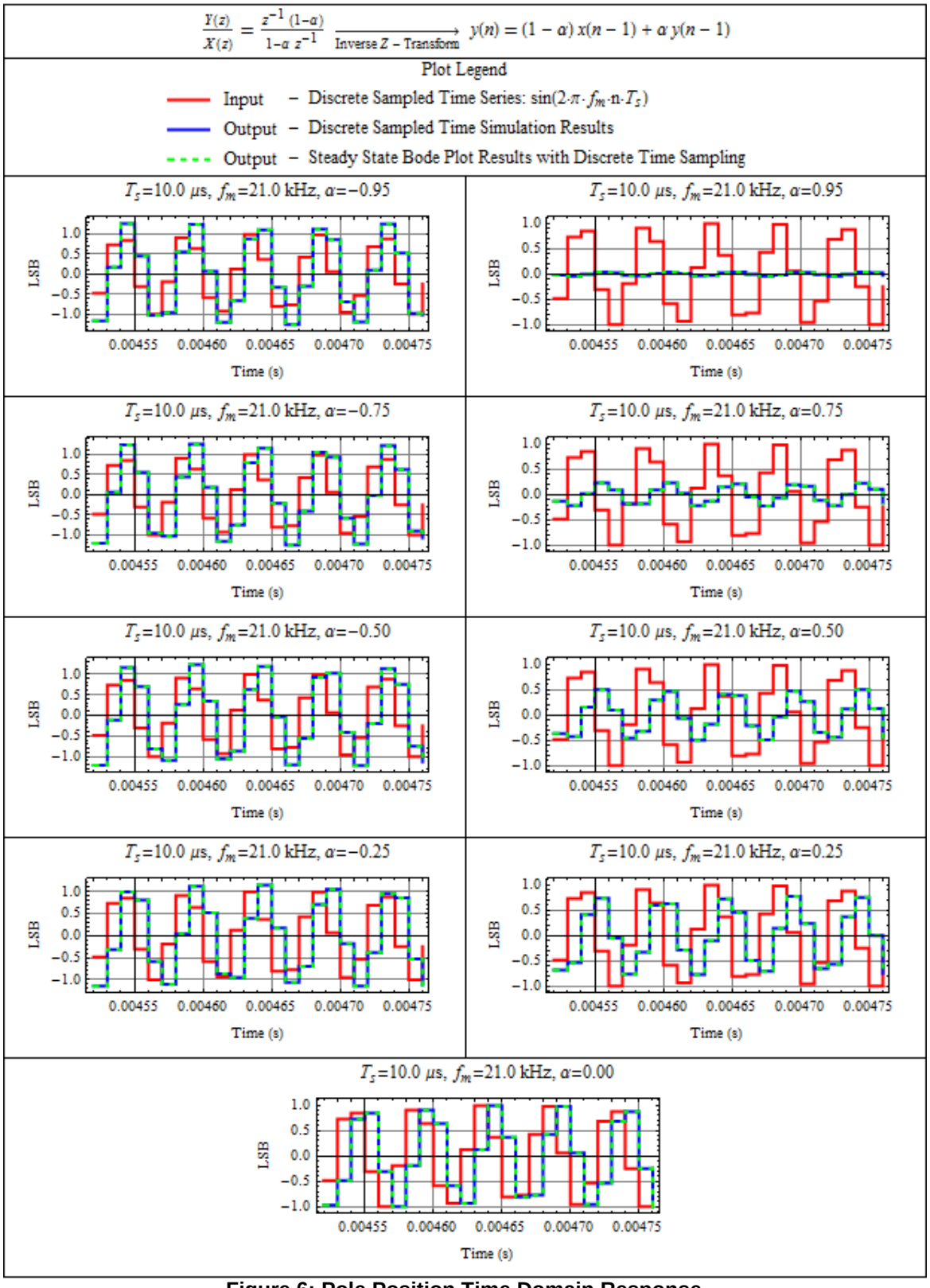


Figure 6: Pole Position Time Domain Response

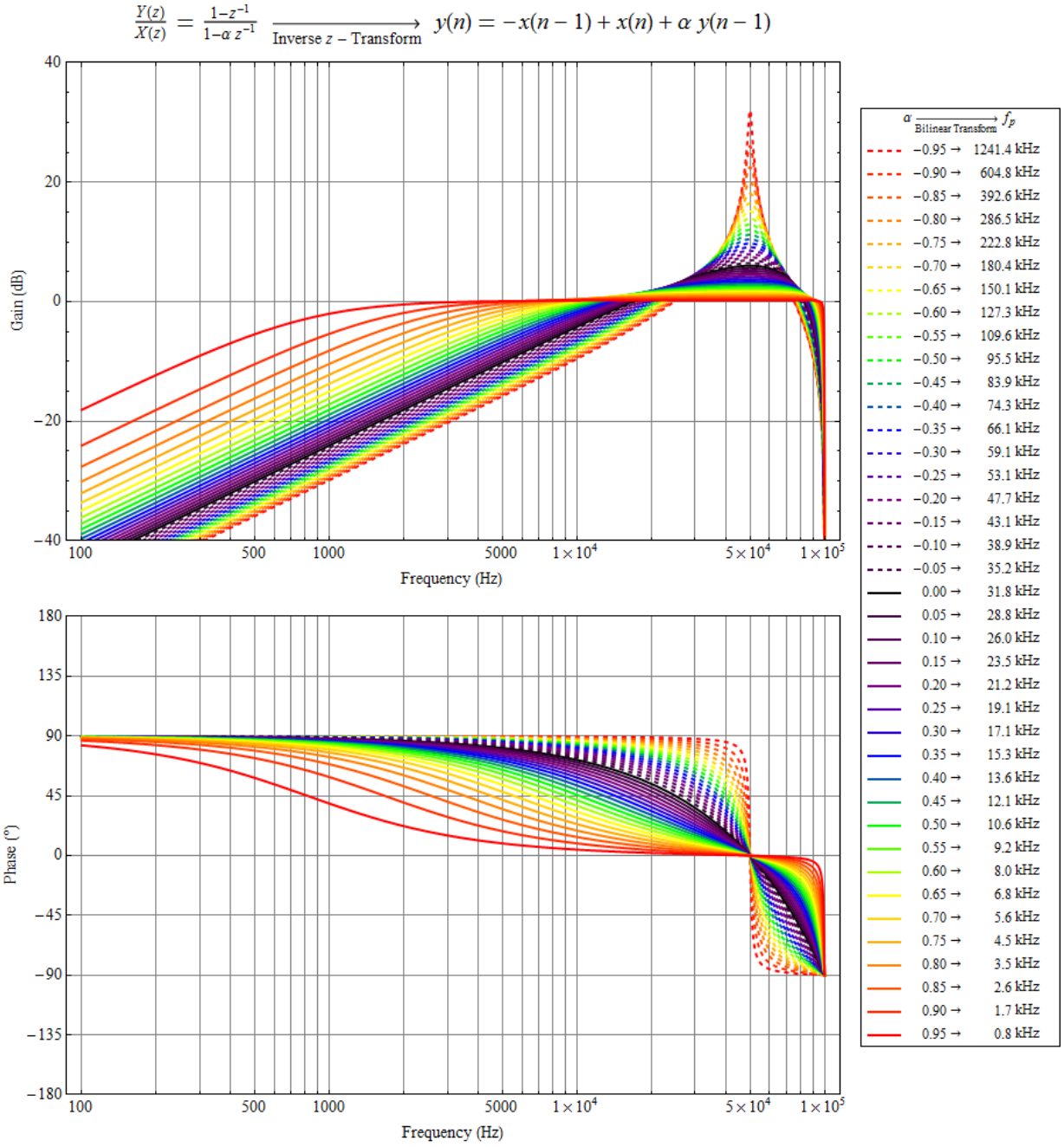


Figure 7: Pole Evaluation of a Discrete Transfer Function (K_D Term)

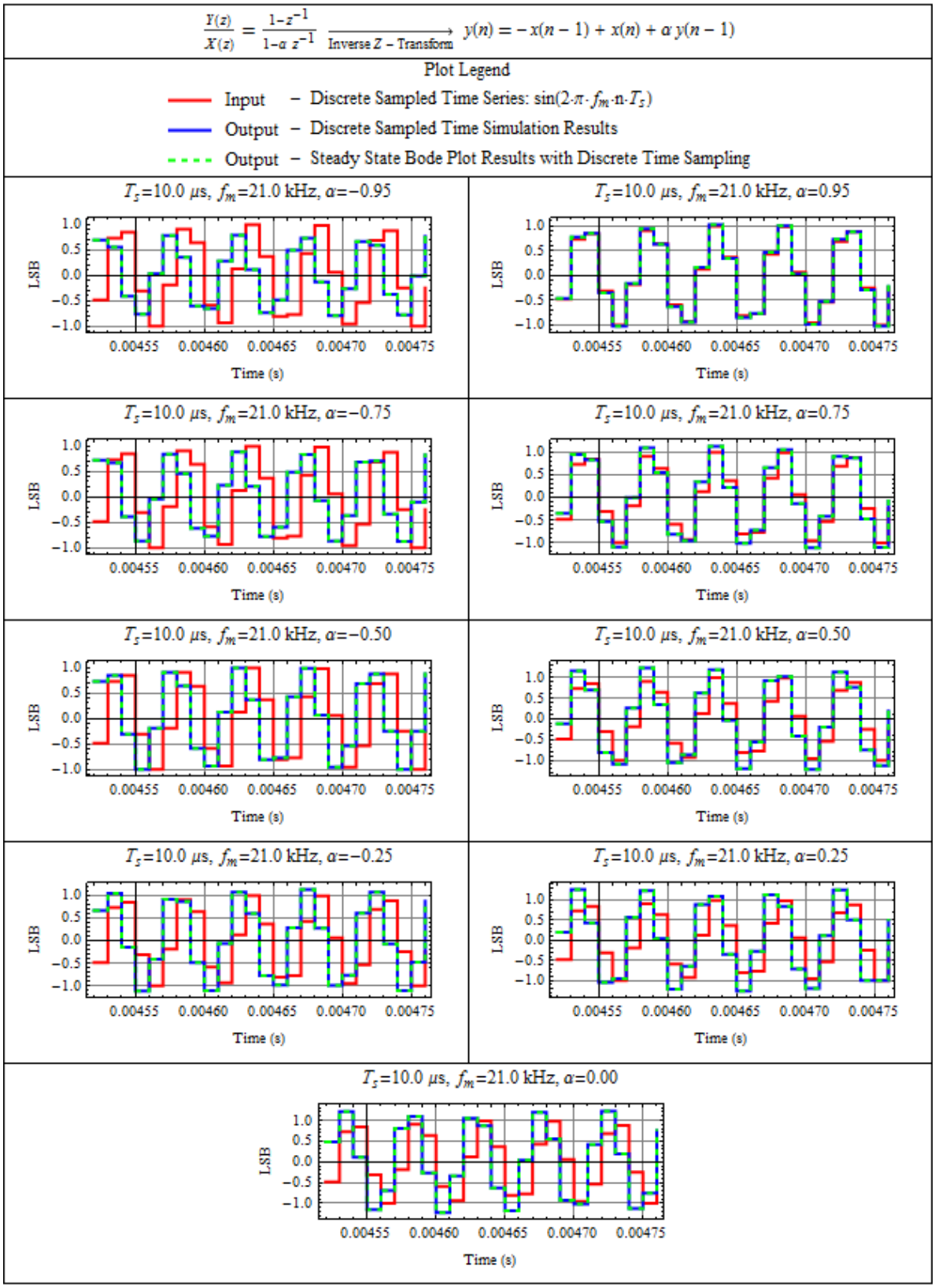


Figure 8: Pole Position Time Domain Response (K_D Term)

Figure 9 uses equation (10) to translate a series of values in the s plane to the z plane [13]. The colors used to plot values in the s plane are equivalent to the colors and values used in the z plane.

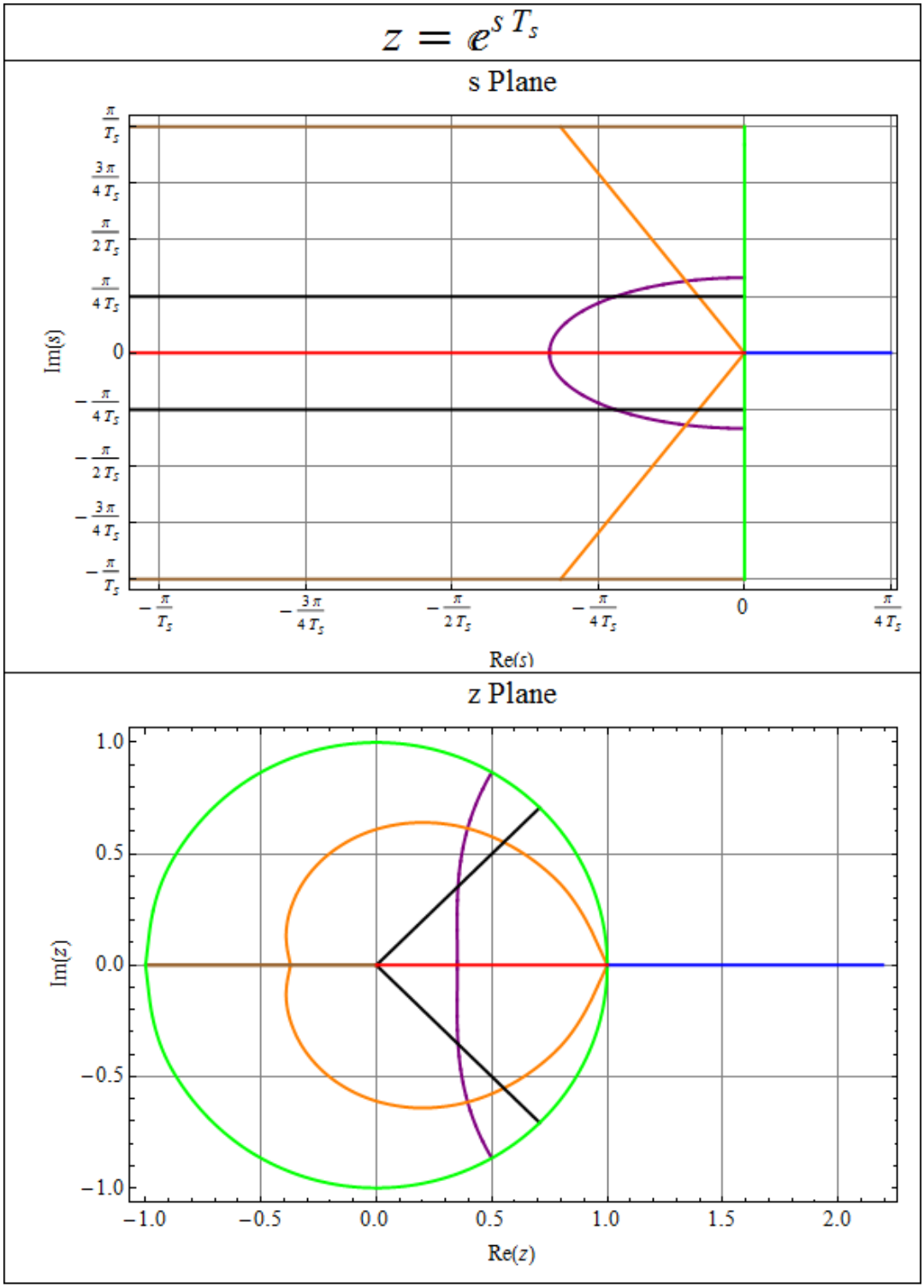


Figure 9: s Plane and z Plane Relationships

Several salient features are noted in table 6.

Table 6: s Plane and z Plane Salient Features

	• All stable real values in the s plane, map between 0 and 1 in the z plane. • A stable real values in the s plane that approaches -∞, approaches 0 in the z plane.
	• Anything outside of the unit circle in the z plane is equivalent to an unstable pole position in the s plane. • Although not explicitly shown, this is also true for complex values.
	• The stability boundary of the imaginary y axis in the s domain is translated to the unit circle in the z domain. • This demonstrates the warping that occurs in the z plane. • The unit circle also shows the effects of aliasing. • As the s domain values exceed ±½ the sample rate, the z plane values continue to map to the unit circle.
	• A diagonal line of stable values in the s plane maps to a decaying spiral centered on 0 in the z plane. • These lines also correspond to a constant damping factor. $\zeta = \frac{1}{2 \cdot Q}$ • This data set further demonstrates the drastic warping that occurs between s plane values and z plane values.
	• These lines are a constant resonant frequency, ω_r. • These lines are a square root function in the s domain, as shown by the squared nature of the plot around the real axis.
	• The s plane horizontal line occurs at ±¼ the sample rate. • The z plane values occur at ±45º.
	• The s plane values each have an imaginary value of ±½ the sample rate. • Stable complex values at ±½ the sample rate in the s plane map between -1 and 0 in the z plane. • If the s plane values have a complex element at ±½ the sample rate then and only then do the z plane values take on a real value between -1 and 0. • In this sense the largest possible stable complex value in the s plane maps to a negative real value in the z plane. • This mapping is consistent with the peaking that occurs at ½ the sample rate in figure 5.

3.4 Effect of PID on Frequency Response

Solving equations (31) – (34) for K_0, ω_{z1}, ω_{z2}, and ω_{p2} results in equations (47) – (50).

$$K_0 = \frac{2 \cdot K_I}{T_s} \tag{47}$$

$$\omega_{z1} = \frac{K_P(1-\alpha) + K_I(1+\alpha) - \sqrt{\left(K_P(1-\alpha) + K_I(1+\alpha)\right)^2 - 8(1-\alpha)K_I \cdot K_D}}{T_s \cdot (K_P(1+\alpha) + 2 \cdot K_D)} \tag{48}$$

$$\omega_{z2} = \frac{K_P(1-\alpha) + K_I(1+\alpha) + \sqrt{\left(K_P(1-\alpha) + K_I(1+\alpha)\right)^2 - 8(1-\alpha)K_I \cdot K_D}}{T_s \cdot (K_P(1+\alpha) + 2 \cdot K_D)} \quad (49)$$

$$\omega_{p1} = \frac{2}{T_s}\frac{1-\alpha}{1+\alpha} \quad (50)$$

If α = 0 equations (51) – (54) result.

$$K_0 = \frac{2 \cdot K_I}{T_s} \quad (51)$$

$$\omega_{z1} = \frac{K_P + K_I - \sqrt{(K_P + K_I)^2 - 8 \cdot K_I \cdot K_D}}{T_s \cdot (K_P + 2 \cdot K_D)} \quad (52)$$

$$\omega_{z2} = \frac{K_P + K_I + \sqrt{(K_P + K_I)^2 - 8 \cdot K_I \cdot K_D}}{T_s \cdot (K_P + 2 \cdot K_D)} \quad (53)$$

$$\omega_{p1} \xrightarrow{Approaches} \infty \quad (54)$$

To understand how each PID parameter affects the frequency response, K_P, K_I, K_D, α and f_s are varied independently and the impact to the Bode plot is discussed.

Figure 10 shows effect of changing K_P. When K_P increases, it pushes gain's valley up and pushes two zeros apart.

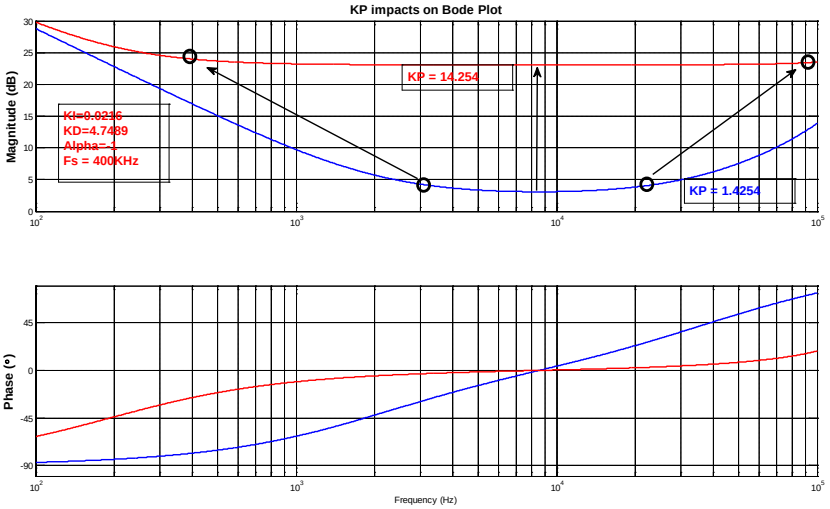


Figure 10: Effect of K_P on Frequency Response.

Increasing K_I shifts the low frequency gain upward and pushes first zero to the right. The second zero stays unchanged until the first zero moves to the right of the second zero.

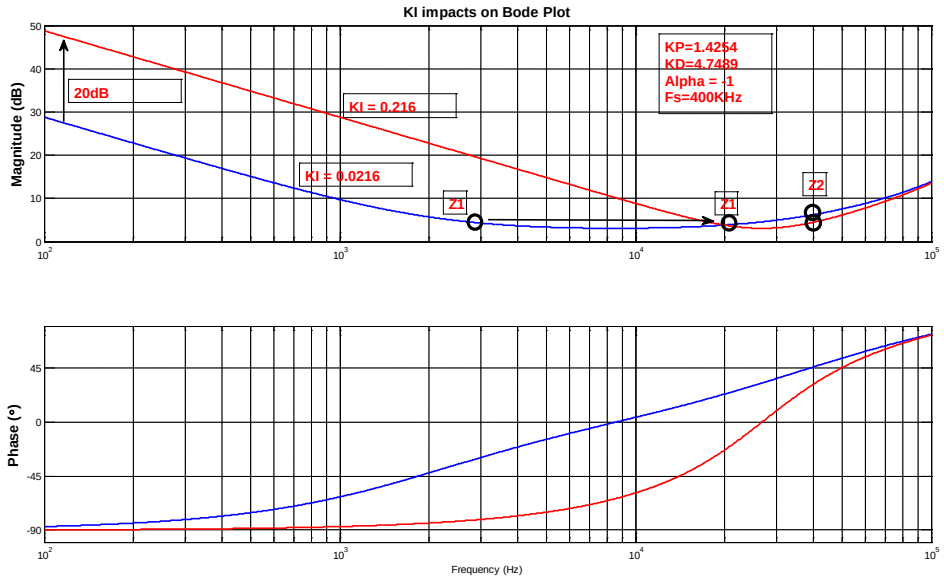


Figure 11: Effect of K_I on Frequency Response.

Increasing K_D causes the second zero to left shift while the first zero and second pole are unchanged.

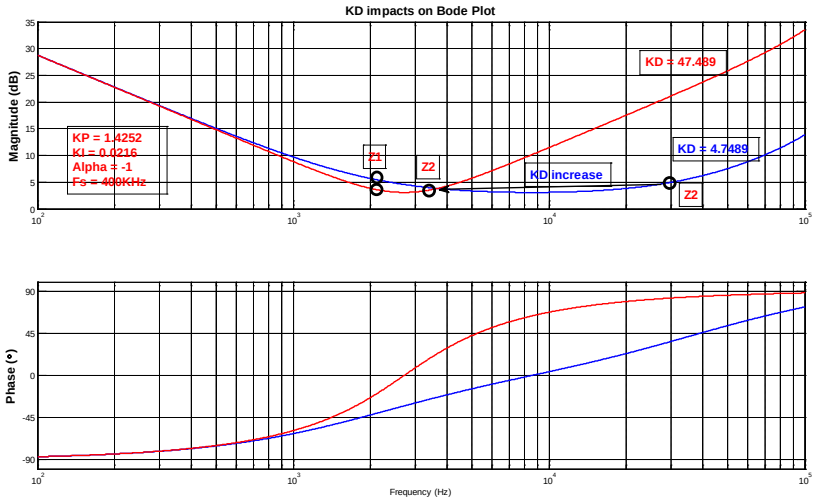


Figure 12: Effect of K_D on Frequency Response.

α has a range from -1 to 1. When α = 0, the second pole is located at ∞ frequency. When α = 1, the compensator's second pole cancels out the second zero and the compensator turns into a 1 pole 1 zero PI type controller. α directly affects the second pole position. Increasing α causes both the second pole and zero to move to the left. See section for a 3.3 discussion on negative values of α.

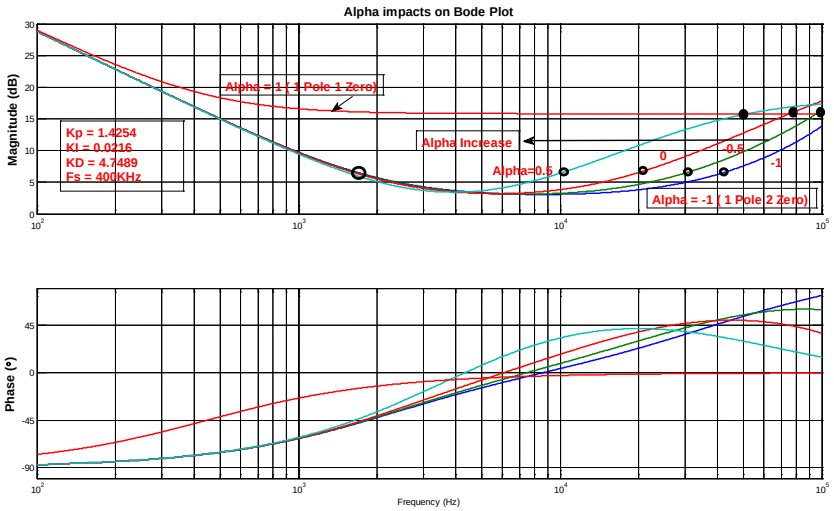


Figure 13: Effect of α on Frequency Response.

Sampling frequency, f_s, has a major impact on frequency response. It affects the low frequency gain and all pole and zero positions. Increasing f_s causes the whole Bode plot to shift to higher frequencies.

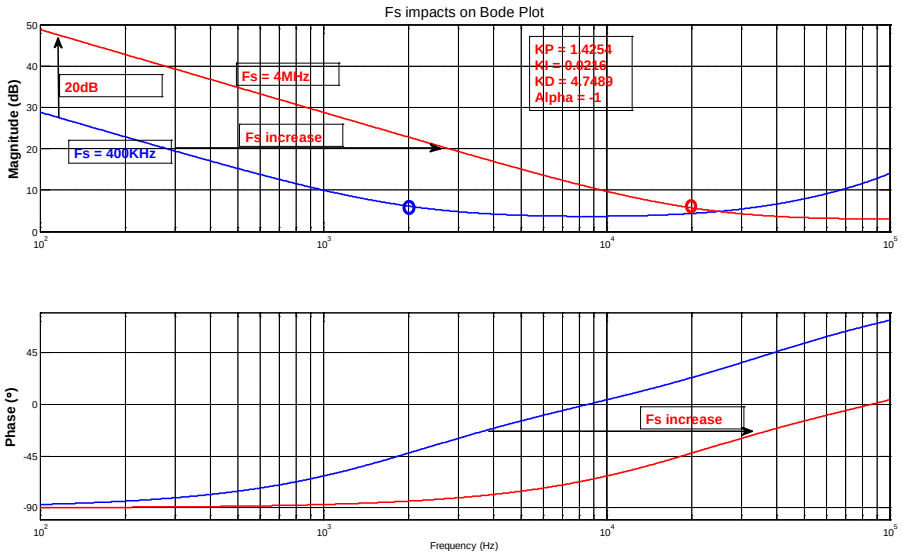


Figure 14: Effect of f_s on frequency response.

Table 7: Summary of PID Parameter Impacts

Control Parameters	Impact on Bode Plot
K_P	Increasing K_P • Pushes up the minimum gain between the two zeros. • Moves the two zeros apart.
K_I	Increasing K_I • Pushes up integration curve at low frequencies. • Gives a higher low frequency gain. • Moves the first zero to the right.

K_D	Increasing K_D • Shifts the second zero left. • Doesn't impact the second pole.
α	Increasing α • Shifts the second pole to the right. • Shifts the second zero to the right.
$T_s = 1 / f_s$	Increase f_s • Causes the whole Bode plot to shift left.

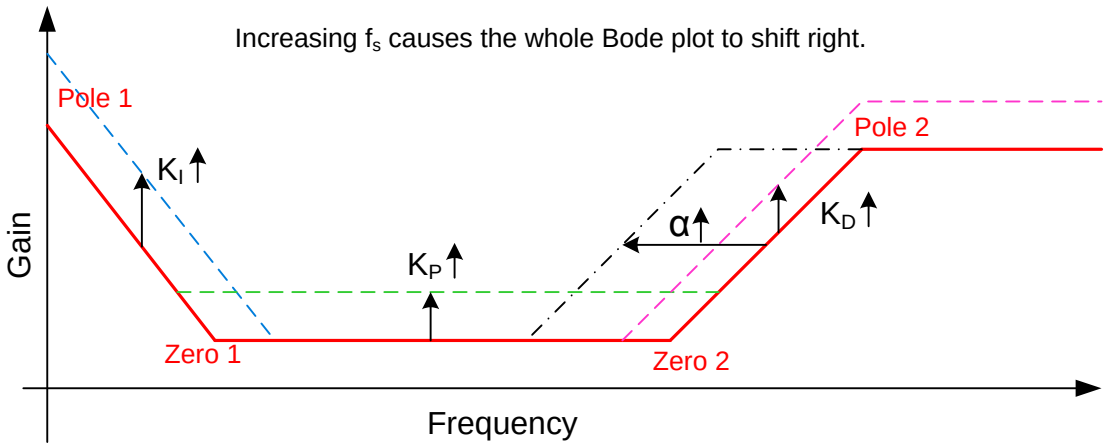


Figure 15: PID Parameter Impact on Frequency Response.

4 Compensation Examples

In any closed loop system, the application of feedback requires an analysis of the stability of the system. For linear systems, this is easily done by determining the open loop gain and plotting its magnitude and phase as a Bode plot [13]. From the Bode plot, the system performance metrics of bandwidth (0 dB crossover), gain margin and phase margin can be determined. To determine the loop gain, each contributor to the open loop gain needs to be understood.

4.1 Example 1: 1ST Order System

Figure 16 shows a boost converter. This discussion centers on the current loop.

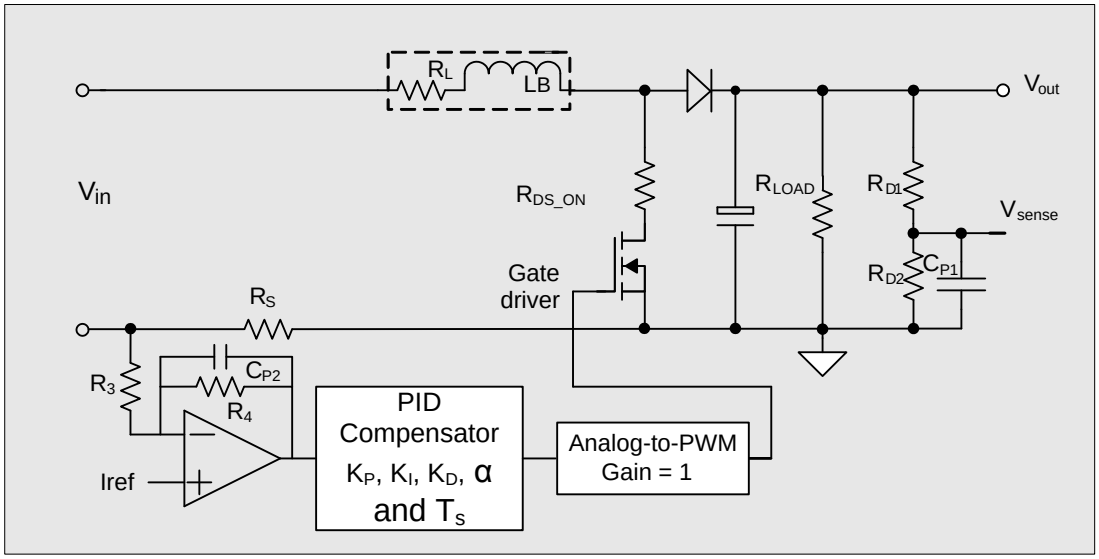


Figure 16: Current Mode Control Boost Converter

Table 8: Boost Converter Component Values

component	Value	description
V_{in}	200V	DC Input voltage.
V_{out}	400V	Nominal output voltage. Needed to determine the nominal duty cycle
R_L	1.48 Ω at 100KHz	Equivalent resistance of the boost inductor at switching frequency.
L_B	330 µH	Boost inductance
R_{DS_ON}	0	MOSFET turn-on resistance
R_S	20 mΩ	Boost current sensing resistor
R_3	2 kΩ	Input resistor of the current amplifier
R_4	49.9 kΩ	Resistor for amplifier gain setting
C_{P2}	100pF	Current amplifier low-pass capacitor
PID	NA	Digital compensator. Its output represents PWM duty cycle.
I_{ref}	NA	Current reference
Other parts	NA	Other parts are not loop related

4.1.1 Power Stage and Current Sensing Transfer Functions

Figure 17 shows a simplified representation of the boost converter power stage shown in figure 16.

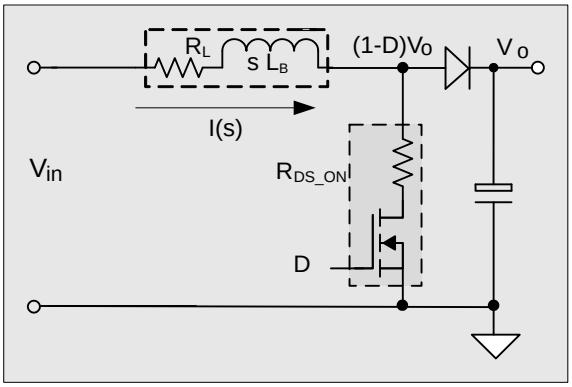


Figure 17: Boost Converter Current Loop.

Given that the system is in CCM there are two operating states for the converter. The equations for these states are shown in equations (55) and (56).

$$I(t) \cdot R_L + \dot{I}(t) \cdot L_B = V_{in}(t) - 0 \quad (55)$$
$$I(t) \cdot R_L + \dot{I}(t) \cdot L_B = V_{in}(t) - V_0(t) \quad (56)$$

The small ripple assumption is applied and the state variables in equations (55) and (56). These variables are then averaged over one switching cycle , resulting in equations (57) and (58).

$$\langle I(t)\rangle_{T_s} \cdot R_L + \langle \dot{I}(t)\rangle_{T_s} \cdot L_B = \langle V_{in}(t)\rangle_{T_s} - 0 \quad (57)$$
$$\langle I(t)\rangle_{T_s} \cdot R_L + \langle \dot{I}(t)\rangle_{T_s} \cdot L_B = \langle V_{in}(t)\rangle_{T_s} - \langle V_0(t)\rangle_{T_s} \quad (58)$$

Averaging equations (57) and (58) over one switching cycle yields equation (59). The system is time varying due to the changing input voltage.

$$\langle I(t)\rangle_{T_s} \cdot R_L + \langle \dot{I}(t)\rangle_{T_s} \cdot L_B = \langle V_{in}(t)\rangle_{T_s} - \langle V_0(t)\rangle_{T_s}(1 - d(t)) \quad (59)$$

The output voltage is assumed to have a negligible impact on the inductor current due to the large amount of the output capacitance. In addition the input voltage is assumed to be constant. Although this is not true, it will be treated as such under the assumption that stability and performance will be evaluated for each real world value of the input voltage. These assumptions allow for generation of the linearized results shown in equations (60) – (62).

$$\hat{I}(t) \cdot R_L + \hat{\dot{I}}(t) \cdot L_B = \hat{V}_{in}(t) - \hat{V}_O(t)(1 - D) + V_O \cdot \hat{d}(t) \quad (60)$$
$$I(s) \cdot R_L + s \cdot I(s) \cdot L_B = V_{in}(s) - V_O(s)(1 - D) + V_O \cdot d(s) \quad (61)$$
$$I(s) = \frac{V_{in}(s) - V_O(s)(1 - D) + V_O \cdot d(s)}{s \cdot L_B + R_L} \quad (62)$$

These assumptions further yield equation (63).

$$\frac{I(s)}{d(s)} = \frac{V_O}{s \cdot L_B + R_L} \quad (63)$$

For the current sensing circuit show in figure 16 the transfer function is shown in equation (65).

$$\omega_{p_{cs}} = \frac{1}{R4 \cdot C_{P2}} \quad (64)$$

$$H_{cs}(s) = R_s \frac{R4}{R3} \frac{1}{\frac{s}{\omega_{p\,cs}} + 1} \tag{65}$$

Current sensing circuit with a low pass filter adds a pole to the loop. The pole position should be placed at between open loop crossover f_c and approximately $10 \cdot f_c$. In the following examples, the pole is located at approximately $5 \cdot f_c$, which gives a good gain roll off and does not significantly degrade the phase.

From loop configuration shown in figure 18, the following open loop transfer function and closed loop transfer functions result.

$$G_{OL}(s) = G_{plant}(s) \cdot H_{cs}(s) \cdot PID(s) \tag{66}$$

$$H_{cs}(s) = \frac{G_{plant}(s) \cdot PID(s)}{1 + G_{plant}(s) \cdot H_{cs}(s) \cdot PID(s)} \tag{67}$$

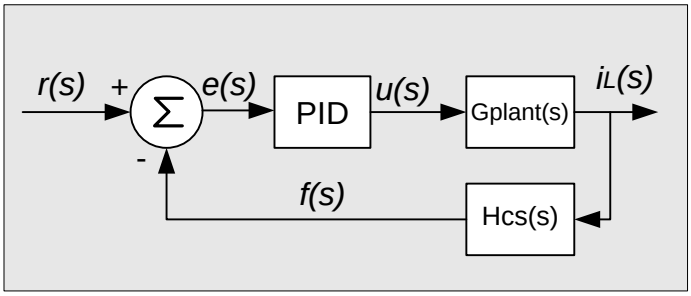


Figure 18: Control Loop Block Diagram

The open loop transfer function is used to generate the Bode plot, phase margin and gain margin. The closed loop transfer function can be used to perform a step response analysis.

4.1.2 Loop Compensation 1: Direct PID Tuning

Current mode control power stages, such as the current loops of PFC and buck converters, are often approximated by a first order system. Since the maximum phase lag of a 1ST order system is 90º no additional zero is needed for stability. A conventional PID tuning method can be used to quickly optimize the loop compensation. The procedure is in the following paragraphs.

4.1.2.1 K_P Tuning (a.k.a. zone 1 tuning)

Set $K_I = 0$ (or a very small value), $K_D = 0$ and $\alpha = 0$ ($\omega_{p2} = \infty$) increase K_P as much as possible until a close-loop step response starts to cause the controlled parameter to overshoot (e.g. input current). Pushing K_I higher will increase bandwidth but at the cost of phase margin. Overshoot becomes more severe as phase margin decreases. The allowable overshoot is generally a system requirement. Some system can tolerate a 5% overshoot, while some others don't allow any.

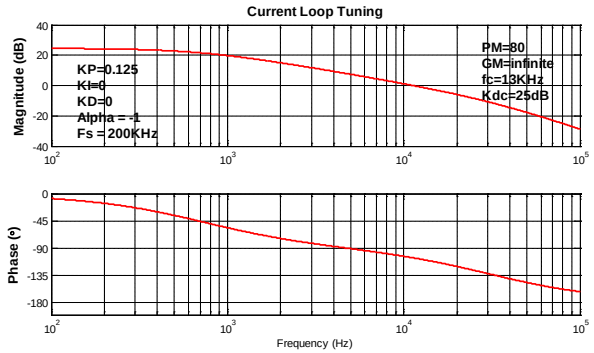


Figure 19: K_P Tuning – Bode Plot

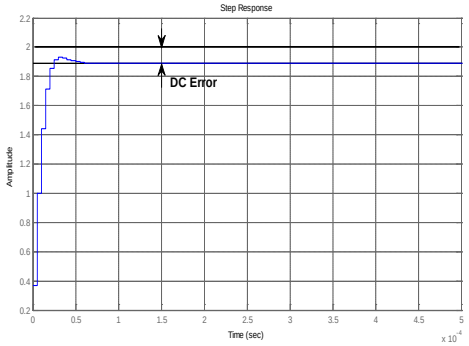


Figure 20: K_P Tuning – Step Response

4.1.2.2 K_I Tuning (a.k.a. zone 2 tuning)

Since K_P cannot be ∞, there will be some dc error between output and the reference command. Integration is necessary to eliminate the steady state error. K_I should be increased as much as the overshoot specification will allow. This pushes the steady state error to 0 and reduces the settling time.

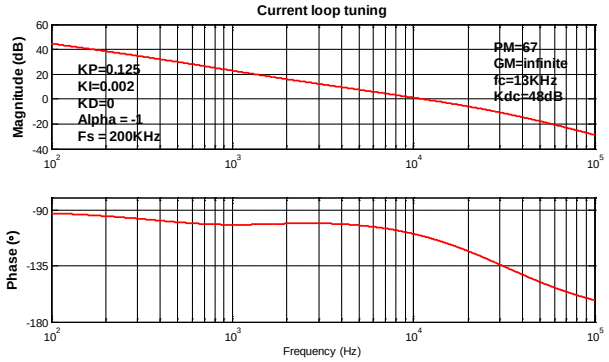


Figure 21: K_I Tuning – Bode Plot

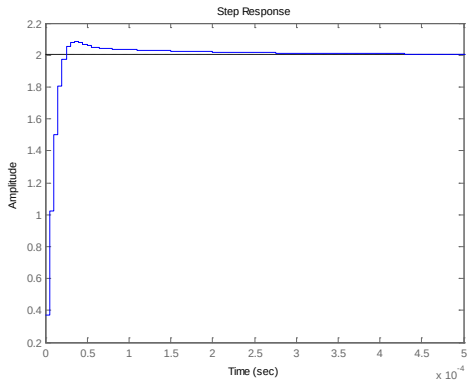


Figure 22: K_I Tuning – Step Response

PI control, can generally get a satisfactory loop response. However, if further damping is needed, K_D can be used. Increasing K_D will shift second zero to the left. It will boost phase margin and will damp the step response. If the phase boost causes the gain margin to become insufficient, then α can be used to provide the necessary roll off after the gain passes crossover point.

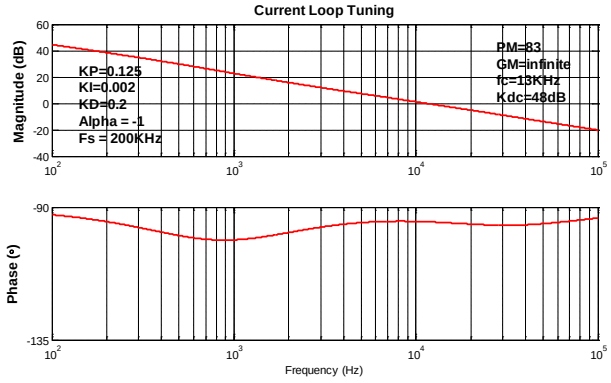


Figure 23: K_D Tuning – Bode Plot

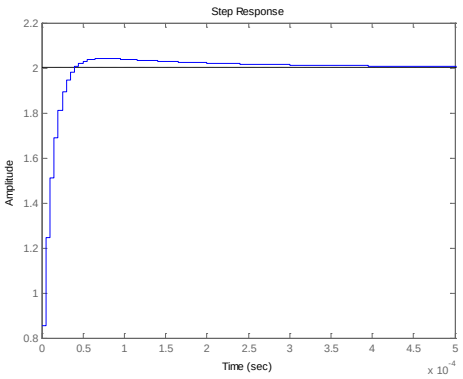


Figure 24: K_D Tuning – Step Response

4.1.3 Loop Compensation 2: Pole and Zero Placement

For this example, the design goal will remain the same, f_c = around 10 kHz and phase margin > 60º.

The Bode plot before a compensator is added is shown in figure 25. In this case the loop has f_c = 52 kHz and the phase margin is 38 º.

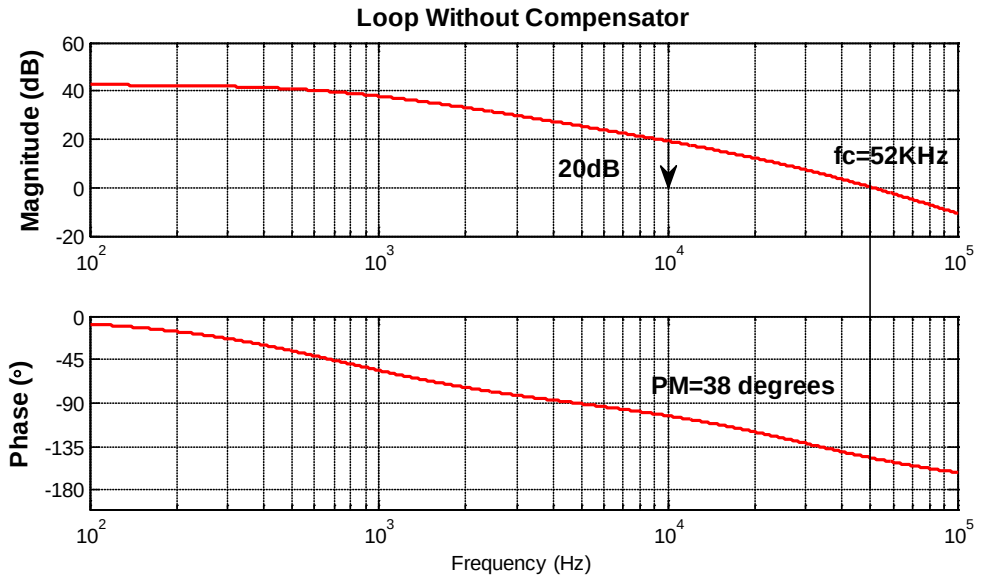


Figure 25: Power Stage

In order for the gain to cross over at 10 kHz, the gain has to be attenuated by 20 dB. Therefore, the compensator has,

K_P = -20 dB = 0.1

As stated above, PI (1 pole, 1 zero) compensation will be sufficient for a 1^{ST} order system, so K_D is set to zero. It can also be treated as a 2 pole 2 zero compensator with second pole and second zero are located at infinite frequency.

$K_0 = K_P \cdot \omega_{z1}$ and $K_I = K_0/f_s/2$

The compensator zero, ω_{z1}, is placed at the same location of boost power stage pole, ω_{p_boost}. Where $\omega_{p\_boost} = R_L/L_B = 4.4848 \cdot 10^3$ (rad/sec) or 714 Hz.

To cancel this pole, ω_{z1} is set at 1 kHz (near or on the pole), then

$K_0 = K_P \cdot \omega_{z1}$ = 628, and

$K_I = K_0/f_s/2 = 1.57 \cdot 10^3$.

Using the K_P and K_I with K_D= 0 and f_s = 200 kHz, the Bode plot shown figure 26 results.

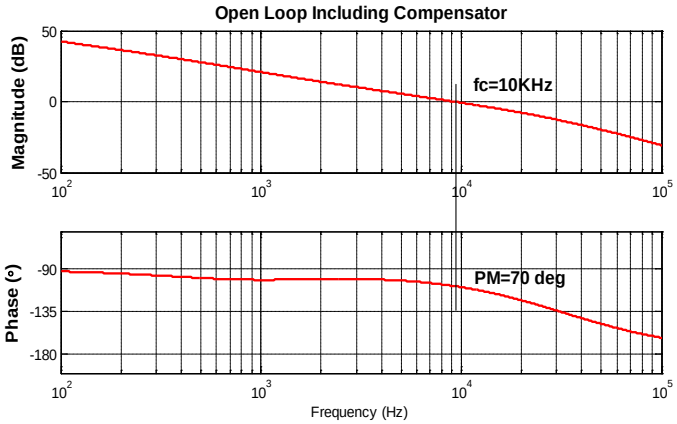


Figure 26: Pole Zero Placement – Bode Plot

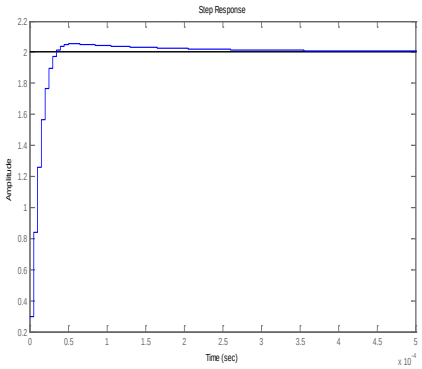


Figure 27: Pole Zero Placement – Step Response

These two examples show that either method can achieve an acceptable response. However, in the following applications, direct PID tuning may be more practical and easier to use.

1. High voltage applications where a network analyzer cannot be easily isolated, such as PFC,
2. Applications where current feedback signal is discontinuous. One such example is bridgeless PFC with current transformer sensing. In this case, a network analyzer is not able to easily extract the frequency response measurement.
3. Power plant transfer function is unknown, etc.

4.2 Example 2: 2ND Order System

A buck type dc/dc converter with voltage mode control is used as an example of a 2ND order system. In order to focus the discussion on loop compensation the converter and control loop are simplified as shown in figure 28. Feedback signal, V_{sense}, is connected to a PID compensator by an amplifier. This amplifier's gain is -1.

The components that need to be defined are as follows:

Table 9: Component Values

Component	Value	Description
V_{in}	48 V	Input voltage. This forms part of the plant DC gain.
N	3:1	Transform turn ratio (Np/Ns)
V_{out}	12 V	Nominal output voltage. Needed to determine the nominal duty cycle

R_D	8 mΩ	This is the total resistance during D period, including reflected primary side FET's resistance, transformer resistance and secondary synchronous MOSFET resistance.
R_{1-D}	8 mΩ	The total combined resistance of synchronous MOSFETs and maybe power transformer secondary winding DC resistance during 1-D period, depended on the given topology.
R_L	2 mΩ	DC resistance of the inductor
L	2 µH	Inductor inductance
C_1	1329 µF	Combined (summed) capacitance of all ceramic caps on the output
R_{C1}	1 mΩ	Parallel combination of ESR for ceramic caps.
L_{C1}	0 µH	Effective series inductance (ESL) of ceramic caps
R_{D1}	11 kΩ	Voltage sensing divider top resistor
R_{D2}	1 kΩ	Voltage sensing divider bottom resistor
C_z	0 µF	Voltage sensing zero capacitor
C_p	1 nF	Voltage sensing low-pass filter cap (pole capacitor)
R_{LOAD}	1 Ω	Load resistance
f_s	200 kHz	Sampling frequency

Note: Parameter values are based on 48 V Hard Switching Full Bridge EVM design.

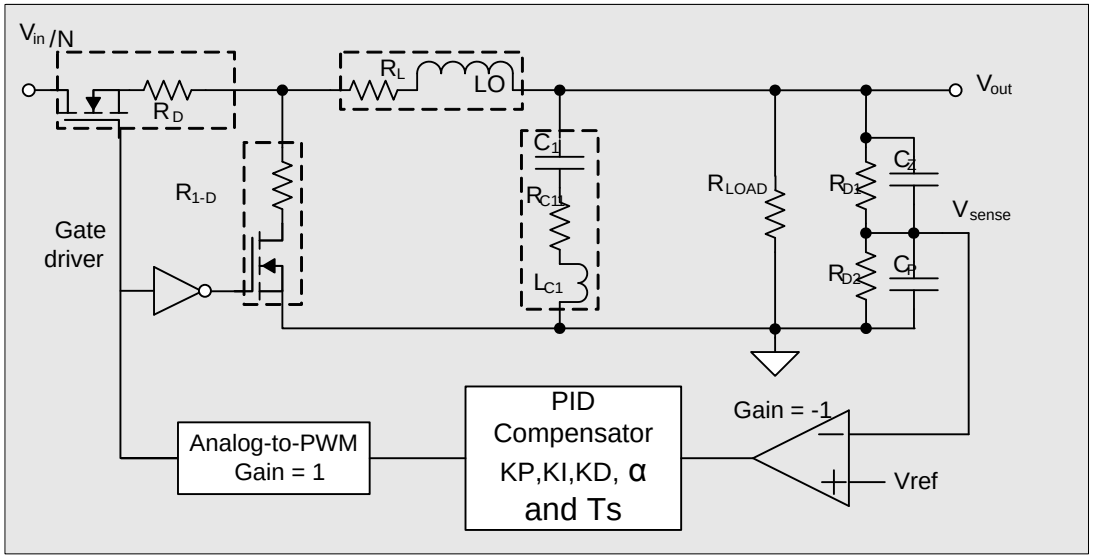


Figure 28: Equivalent Buck Converter

4.2.1 Power Stage and Voltage Sensing Circuit Transfer Function

The effective series resistance, R_s is the total averaged series resistance and consists of the dc resistance of the inductor, R_L, and the equivalent MOSFET resistances R_D. For the small signal ac transfer function, the average resistance presented by the two MOSFET can be calculated as:

$$D = \frac{V_O}{V_{IN}} \tag{68}$$

$$R_{node} = R_D \cdot D + R_{1-D} \cdot (1 - D) \tag{69}$$

$$R_S = R_{node} + R_L \tag{70}$$

There may be several capacitors on the output. Typically there will be large valued capacitors to provide the bulk energy storage and smaller valued ceramic capacitors with lower effective series resistance (esr) and

effective series inductance (esl) values to supply high frequency current. Each capacitor type can be considered by equation (71).

$$Z_{C_n}(s) = \left(\frac{1}{s \cdot C_n} + s \cdot esl_n + esr_n\right)\frac{1}{N_{c_n}} \quad (71)$$

The combined effect of all the different capacitors can be calculated using equation (72).

$$Z_{C_{Total}}(s) = \left(\sum_{n=1}^{N} Z_{C_n}(s)^{-1}\right)^{-1} \quad (72)$$

Using these relationships along with figure 28 the plant transfer function $G_{plant}(s)$ can be determined.

From the loop configuration shown in figure 29 the open loop and closed loop transfer functions can be derived as shown in equations (73) and (74).

$$G_{OL}(s) = G_{plant}(s) \cdot G_{DIV}(s) \cdot PID(s) \quad (73)$$

$$H_{cs}(s) = \frac{G_{plant}(s) \cdot PID(s)}{1 + G_{plant}(s) \cdot G_{DIV}(s) \cdot PID(s)} \quad (74)$$

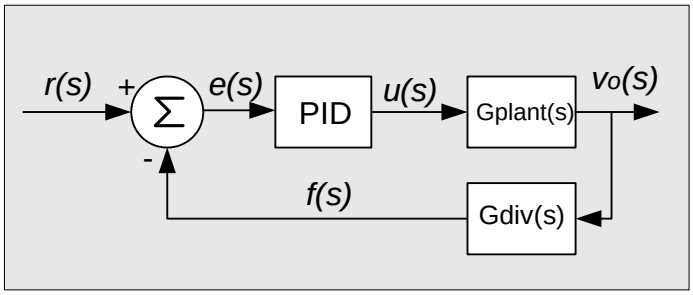


Figure 29: Loop Configuration.

4.2.2 Loop Compensation Procedure by Using 2-Pole 2-Zero Analog Compensator

4.2.2.1 Loop Compensation goals:

- Crossover frequency f_c is about 20 kHz
- Phase margin > 60º.

4.2.2.2 2ND System Tuning Procedure

1. Determine the second order system's resonant frequency.

$$f_r = \frac{1}{2 \cdot \pi \sqrt{Lo \cdot C1}} = 3.08 \text{ kHz} \quad (75)$$

2. Plot Power stage and feedback network frequency response.

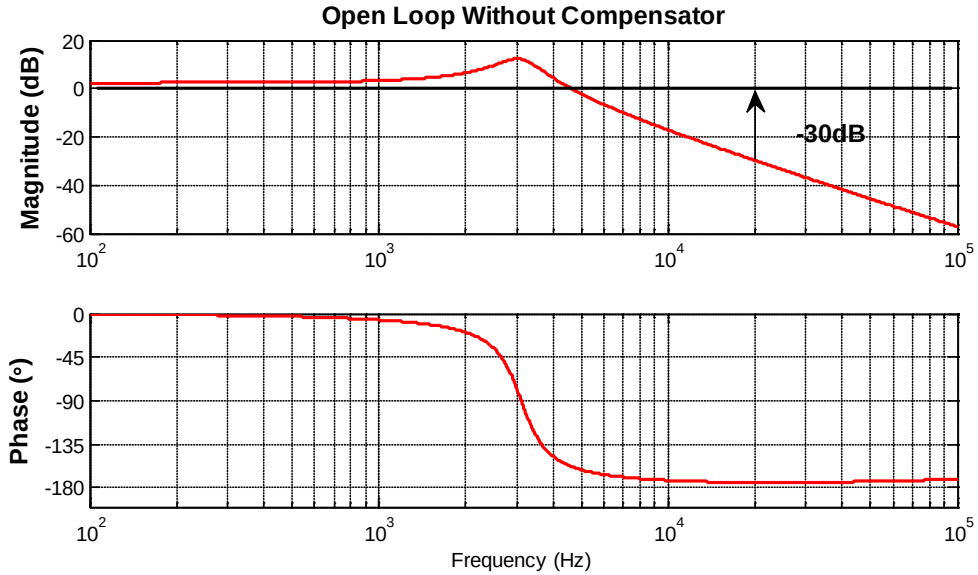


Figure 30: Plant Frequency Response

To get 20 kHz crossover frequency, a compensator should have 30 dB of gain at the desired cross over frequency and a phase boost of 180º.

3. To boost the phase by 180º, a 2 pole 2 zero compensator is needed and should be located at 1/10 of f_c.

   $f_{z1} = f_{z2} = 2\ kHz$

4. Place the second pole of the compensation at a frequency 10 times higher than f_c to start with. This way it will not affect the expected gain and phase at f_c.

5. Plot compensator's frequency response and vary K_0 to get desired gain. Vary K_0 so the gain at f_c is 30 dB,

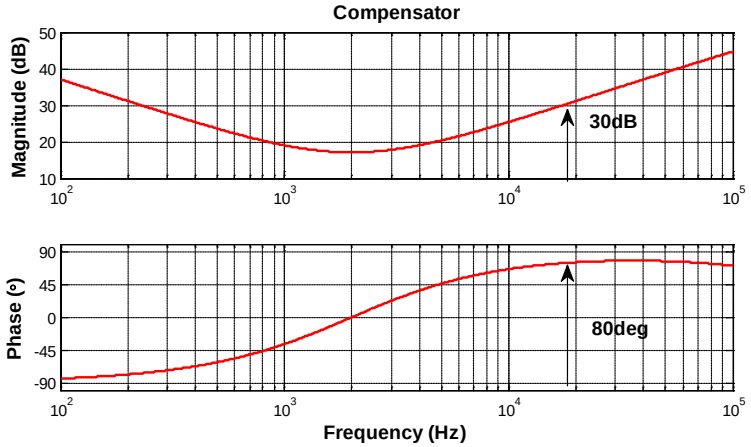


Figure 31: Analog Compensator Plot

6. Plot Open-Loop frequency response,

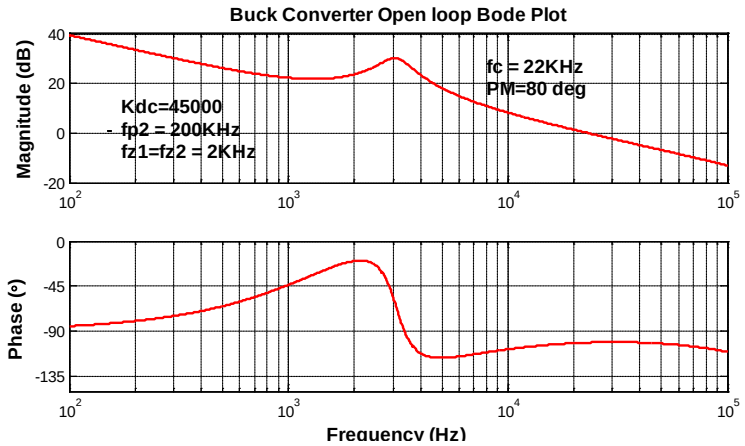


Figure 32: Analog Placement – Bode Plot

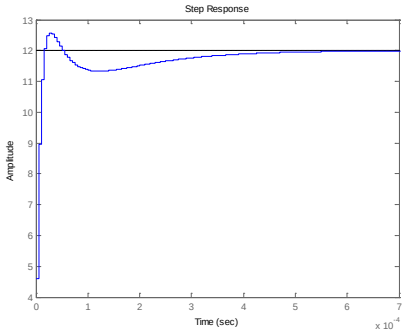


Figure 33: Analog Placement – Step Response

After adding the tuned compensator to the loop, the open loop Bode plot can be generated. It can be seen that both phase margin and crossover frequency design goals were met.

7. Convert control parameters to component values

The compensation above uses real poles and zeros. The control parameters can be converted to circuit component values by using the equations in section 3.2.

Table 10: Resistor and Capacitor Values

R1	1 kΩ
R2	36.2 kΩ
C1	2.2 nF
C2	2.2 nF
C3	22 pF

Compensation parameters designed in s domain can be converted to discrete z domain.

Following parameters are obtained from the analog compensation.

Table 11: Raw Gains

K_0	0.45e5

ω_{z1}	12560
ω_{z2}	12560
ω_{p1}	6.28*200e3

They can be converted PID parameters.

Table 12: PID Values

K_P	7.129777
K_I	0.1125
K_D	0.8481896
α	-0.5169082

4.2.3 Loop Compensation Procedure by Using PID

Procedure of second-order system tuning,

1. Determine the second order system's resonant frequency

$$f_r = \frac{1}{2\cdot\pi\sqrt{Lo\cdot C1}} = 3.08 \text{ kHz} \quad (76)$$

2. If the resonant frequency is beyond of power supply frequency bandwidth, the power plant of the converter basically turns into a 1^{ST} order system. Direct PID tuning can be used to optimize loop compensation.
3. For most cases, power supply bandwidth needs to push higher than power plant resonant frequency. The two system poles cause 180° of phase delay, and a two pole two zero compensator becomes necessary.
4. Preselect the low frequency gain K_0 value to be 10k (most analog amplifier DC gain range is from 10k to 100k). Choose the sampling frequency to be the same as switching frequency, then:

$$K_I = \frac{K_0}{2\cdot f_s} = 0.025 \quad (77)$$

5. Place second pole at infinite frequency ($\omega_{p2} = \infty$) by setting $\alpha = 0$
6. Place the two compensator zeros at 1/10 of expected crossover frequency (20Khz) and calculate K_P and K_D as follows,

   $K_P = K_0 (\omega_{z2}+\omega_{z1})/(\omega_{z1}* \omega_{z2}) = 1.59$

   $K_D = 2\cdot K_0\cdot f_s/(\omega_{z1}* \omega_{z2}) = 101.4$

   If it is not clear where the zeros should be put, a loop frequency response without the compensator should be generated.

   The system with the calculated PID values has the following Bode plot and step response,

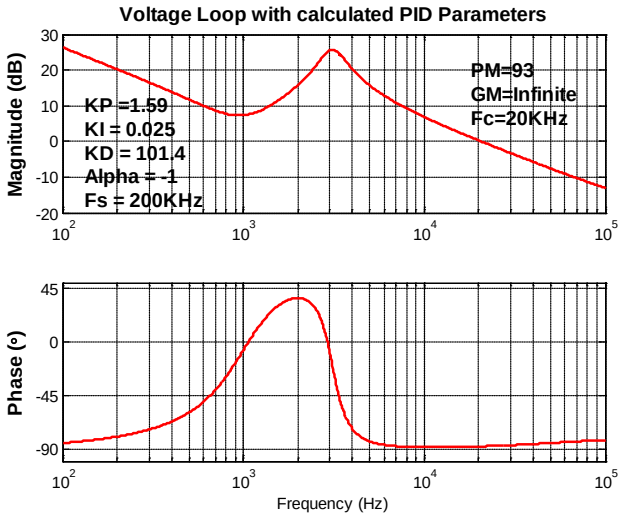


Figure 34: PID – Bode Plot

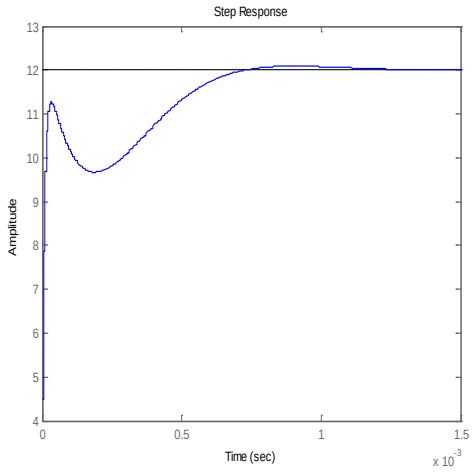


Figure 35: PID – Step Response

7. Now vary K_I and α to fine tune the loop and get the best combination of phase margin, gain margin and crossover frequency. K_I is increased to get a better dc gain. Increase α to move the second pole to the left. The pole will provide additional gain margin but it should not lower phase margin and crossover frequency much.

When using digital PID to compensate loop, the design has more degrees of freedom to place zeros. Complex zeros can be used to achieve an alternate performance. More details on this are discussed in section 5.4.

ω_{z1} = 2.4902e+003 -1.8640e+004i and

ω_{z2} = 2.4902e+003 +1.8640e+004i

Note: A pair of complex zeros means a negative value of C1

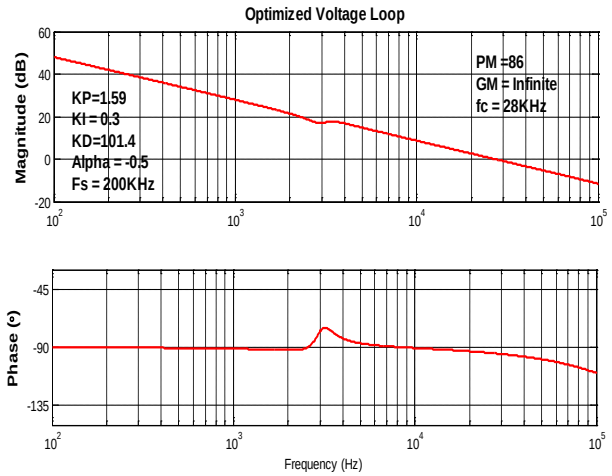


Figure 36: PID – Bode Plot (K_I)

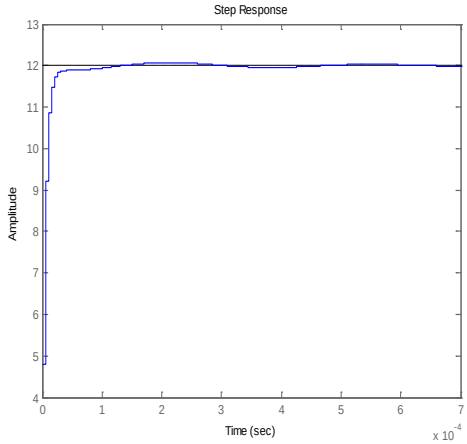


Figure 37: PID – Step Response (K_I)

5 UCD3138 Compensator

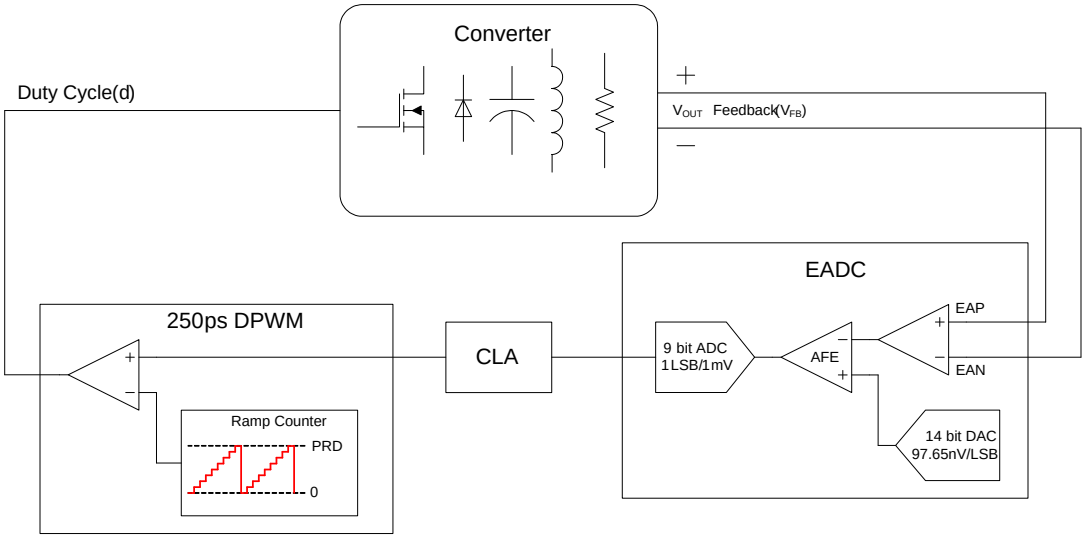


Figure 38: General UCD3138 Block Diagram

5.1 Error ADC Gain

The analog front end has a programmable block that allows the user to configure the resolution of the front end to according to table 13.

Table 13: Front End Resolution

AFE	EADC Resolution
0	8 mV
1	4 mV
2	2 mV
3	1 mV

The actual ADC shown in figure 38, has only 6 bits, however these bits are sign extended to provide a constant gain from the sensed output voltage to the input to the CLA. Again the resolution of the front end with these different AFE settings results as shown in table 13.

$$K_{EADC} = 1000 \tag{78}$$

5.2 CLA Structure and Implementation

5.2.1 CLA Structure: PID Form and Transfer Function

UCD31xx uses a PID form control law accelerator (CLA). The three branches of PID are configured in parallel form as shown in figure 39.

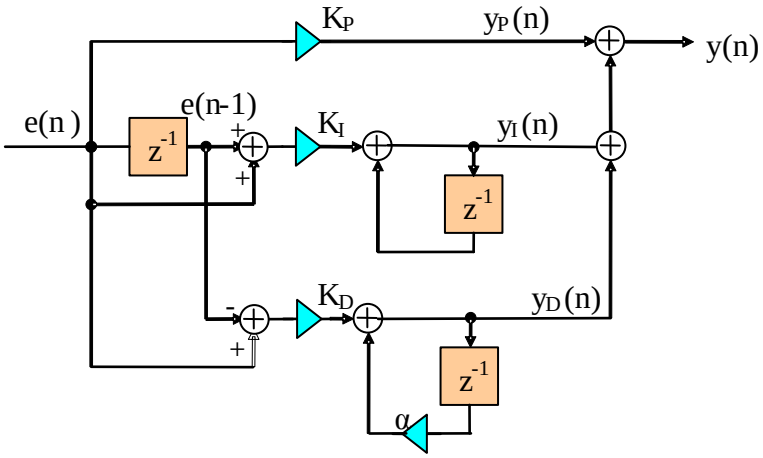


Figure 39: PID Form CLA Structure

A filter output y can be defined from figure 39 that is the sum of a proportional, integral and derivative gain.

$$y(n) = y_P(n) + y_I(n) + y_D(n) \quad (79)$$
$$y_P(n) = K_P \cdot e(n) \quad (80)$$
$$y_I(n) = y_I(n-1) + K_I \cdot (e(n) + e(n-1)) \quad (81)$$
$$y_D(n) = \alpha \cdot y_D(n-1) + K_D \cdot (e(n) - e(n-1)) \quad (82)$$

The z transform of these difference equations is:

$$y(z) = y_P(z) + y_I(z) + y_D(z) \quad (83)$$
$$y_P(z) = K_P \cdot e(z) \quad (84)$$
$$y_I(z) = z^{-1} \cdot y_I(z) + K_I \cdot (e(z) + z^{-1} \cdot e(z)) \quad (85)$$
$$y_D(z) = \alpha \cdot z^{-1} \cdot y_D(z) + K_D \cdot (e(z) - z^{-1} \cdot e(z)) \quad (86)$$

Then the transfer function in the z domain is:

$$\frac{y(z)}{e(z)} = K_P + K_I \frac{1 + z^{-1}}{1 - z^{-1}} + K_D \frac{1 - z^{-1}}{1 - \alpha \cdot z^{-1}} \quad (87)$$

5.2.2 CLA Hardware Implementation

Figures 40 through 42 illustrate the calculation details of the PID CLA. Data formats are given to next to each node. In the notation Sn.m means that the values is signed (if no “S” is present then the data is unsigned), “n” is the number of digits available before the decimal point and “m” is the number after the decimal point. All number formats are in binary.

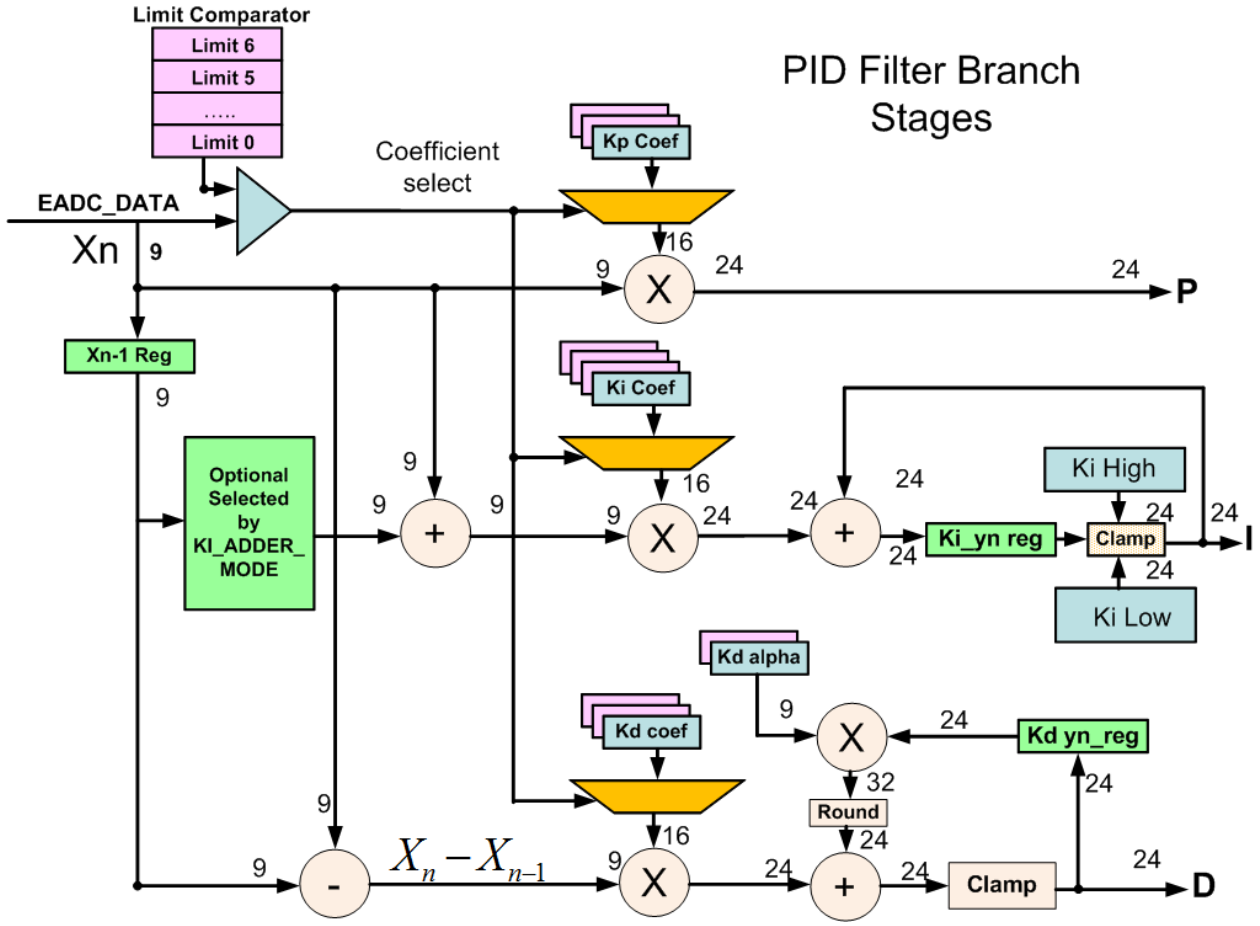


Figure 40: PID Filter Branch and Calculation Implementation

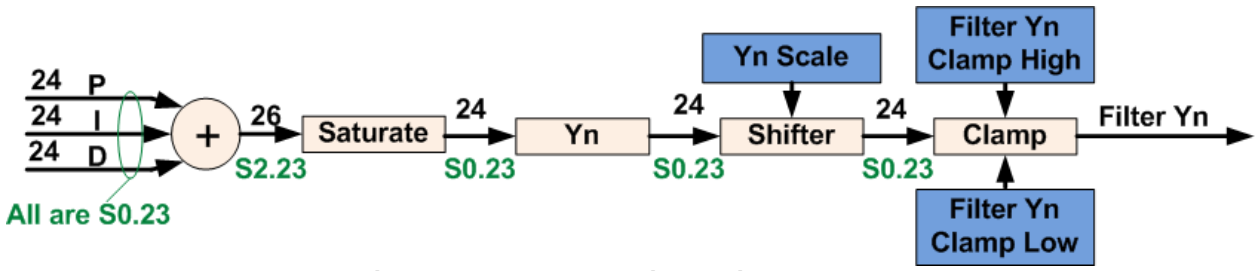


Figure 41: PID Summation and CLA Output

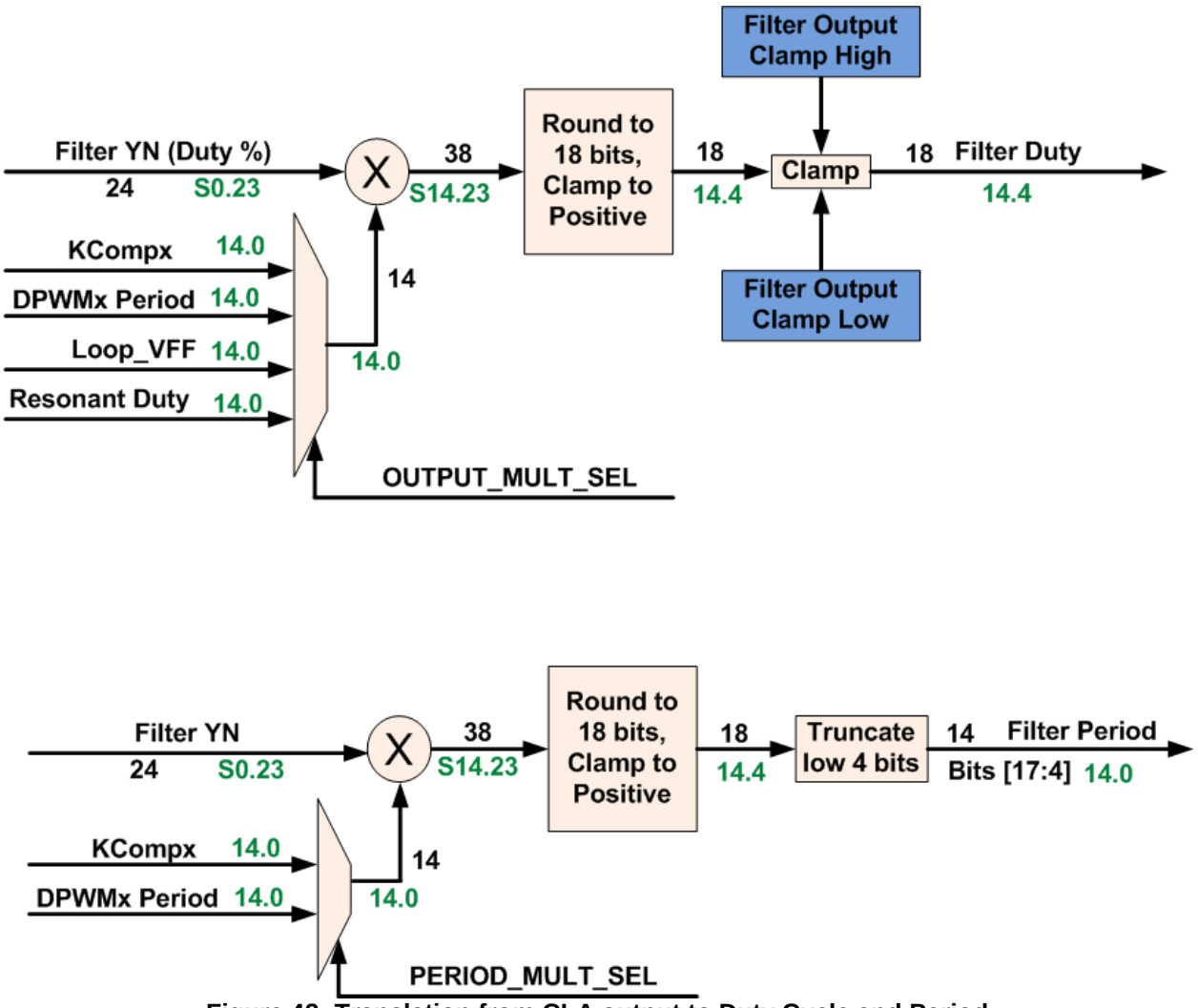


Figure 42: Translation from CLA output to Duty Cycle and Period

At the beginning of the translation stage, the PID output is multiplied by one of several 14 bit unsigned numbers, giving a 38 bit output. This number is right shifted by 19 bits and rounded to give the unsigned 18 bit value. This number is used for DPWM pulse width (250 ns resolution). The DPWM Period is 14 bits with 4 ns resolution. This number should be converted to a value with the same 250nS resolution and then used as an equivalent ramp.

Connecting all EADC, CLA, DPWM and stages together results in equation (88).

$$\frac{d(z)}{v_{fb}(z)} = -1000\left(K_P + K_I\frac{1+z^{-1}}{1-z^{-1}} + K_I\frac{1-z^{-1}}{1-\alpha\cdot 2^{-8}\cdot z^{-1}}\right)\frac{2^{SC}\cdot K_{COMP}\cdot 2^{-19}}{2^4(PRD+1)}e^{-s\cdot T_{delay}} \quad (88)$$

$$T_{delay} = t_d + D\cdot\frac{2^4\cdot(PRD+1)\cdot T_{DPWM}}{2} \quad (89)$$

Equation (89) assumes that the sample trigger point has been placed t_d prior to the end of the period. In addition, it also assumes that the DPWM update window has been set to end of period. Under these conditions t_d, represents the computational delay of the controller. $D\cdot\frac{2^4\cdot(PRD+1)\cdot T_{DPWM}}{2}$ represents the time that elapses before this information impacts the output duty cycle [27]. In normal mode it is possible to get a DPWM update

event at every DPWM edge. This applies to both half cycles of the full bridge and half bridge topologies. If the system does not or cannot support normal mode then this second delay term could be longer by as much as $\frac{2^4 \cdot (PRD+1) \cdot T_{DPWM}}{2}$.

Since α has a valid range is from -1 to 1, it needs to be normalized for transfer function calculation. The normalization is implemented by multiplying the 9 bit signed α and then dropping off 8 bits of the result. In transfer function, α is divided by 2^8 (not including sign bit) for normalization.

5.3 GUI Model Equations

This section provide the GUI model equations (table 14) as well as the transformation equations used to convert between the different models shown in table 14.

Table 14: GUI Transfer Functions

System Name	Transfer Function
Complex Zeros (K0, fz, Qz, fp)	$\frac{2\pi K0\left(\frac{s^2}{4\pi^2 fz^2}+\frac{s}{2\pi fz Qz}+1\right)}{s\left(\frac{s}{2\pi fp}+1\right)}$
Real Zeros (K0, fz1, fz2, fp)	$\frac{2\pi K0\left(\frac{s}{2\pi fz1}+1\right)\left(\frac{s}{2\pi fz2}+1\right)}{s\left(\frac{s}{2\pi fp}+1\right)}$
Device PID (Kp, Ki, Kd, α)	$1000\left(Kp + Ki\,\frac{1+z^{-1}}{1-z^{-1}} + Kd\,\frac{1-z^{-1}}{1-\alpha\,2^{-8}\,z^{-1}}\right)\left(2^{SC}\,KCOMP\,2^{-19}\,\frac{1}{2^4\,(PRD+1)}\right)$

Table 15: Device Registers to Complex Zeros

fz	$\frac{NOS\sqrt{(\alpha-256)(-Ki)}}{(16\pi\,PRD\,TDPWM+16\pi\,TDPWM)\sqrt{512\,Kd+\alpha\,Kp+256\,Kp}}$
Qz	$\frac{\sqrt{(\alpha-256)(-Ki)}\ \sqrt{512\,Kd+(\alpha+256)\,Kp}}{(\alpha+256)\,Ki-(\alpha-256)\,Kp}$
K0	$\frac{125\,KCOMP\,Ki\,NOS\,2^{SC-24}}{\pi\,(PRD+1)^2\,TDPWM}$
fp	$-\frac{(\alpha-256)\,NOS}{16\pi\,(\alpha+256)\,(PRD+1)\,TDPWM}$

Table 16: Real Zeros to Complex Registers

Kp	$\frac{K0\,(PRD+1)\,2^{20-SC}\,(fp-fz\,Qz)}{125\,fp\,fz\,KCOMP\,Qz}$
Ki	$\frac{\pi\,K0\,(PRD+1)^2\,2^{24-SC}\,TDPWM}{125\,KCOMP\,NOS}$
Kd	$\frac{K0\,NOS\,(PRD+1)\,2^{20-SC}\left(fp^2\,Qz-fp\,fz+fz^2\,Qz\right)}{125\,fp\,fz^2\,KCOMP\,Qz\,(16\,\pi\,fp\,(PRD+1)\,TDPWM+NOS)}$
α	$\frac{256\,(NOS-16\,\pi\,fp\,(PRD+1)\,TDPWM)}{16\,\pi\,fp\,(PRD+1)\,TDPWM+NOS}$

Table 17: Device Registers to Real Zeros

fz1	$\frac{NOS\left(\sqrt{2048\,(\alpha-256)\,Kd\,Ki+((\alpha+256)\,Ki+(\alpha-256)\,Kp)^2}+(\alpha+256)\,Ki-\alpha\,Kp+256\,Kp\right)}{32\,\pi\,(PRD+1)\,TDPWM\,(512\,Kd+(\alpha+256)\,Kp)}$
fz2	$-\frac{NOS\left(\sqrt{2048\,(\alpha-256)\,Kd\,Ki+((\alpha+256)\,Ki+(\alpha-256)\,Kp)^2}-(\alpha+256)\,Ki+\alpha\,Kp-256\,Kp\right)}{32\,\pi\,(PRD+1)\,TDPWM\,(512\,Kd+(\alpha+256)\,Kp)}$
K0	$\frac{125\,KCOMP\,Ki\,NOS\,2^{SC-24}}{\pi\,(PRD+1)^2\,TDPWM}$
fp	$-\frac{(\alpha-256)\,NOS}{16\,\pi\,(\alpha+256)\,(PRD+1)\,TDPWM}$

Table 18: Real Zeros to Device Registers

Kp	$\frac{K0\,(PRD+1)\,2^{20-SC}\,(fp\,(fz1+fz2)-fz1\,fz2)}{125\,fp\,fz1\,fz2\,KCOMP}$
Ki	$\frac{\pi\,K0\,(PRD+1)^2\,2^{24-SC}\,TDPWM}{125\,KCOMP\,NOS}$
Kd	$\frac{K0\,NOS\,(PRD+1)\,2^{20-SC}\,(fp-fz1)\,(fp-fz2)}{125\,fp\,fz1\,fz2\,KCOMP\,(16\,\pi\,fp\,(PRD+1)\,TDPWM+NOS)}$
α	$\frac{256\,(NOS-16\,\pi\,fp\,(PRD+1)\,TDPWM)}{16\,\pi\,fp\,(PRD+1)\,TDPWM+NOS}$

In addition to the GUI equations tables 19 and 20 show the formulas for converting between equations (30) and (88).

Table 19: Normalized PID to Register PID

K_p	$\frac{(PRD+1)\,2^{20-SC}\,K_{p_n}}{125\,KCOMP}$
K_i	$\frac{(PRD+1)\,2^{20-SC}\,K_{i_n}}{125\,KCOMP}$
K_d	$\frac{(PRD+1)\,2^{20-SC}\,K_{d_n}}{125\,KCOMP}$
α	$256\,\alpha_n$

Table 20: Register PID to Normalized PID

K_{p_n}	$\frac{125\,KCOMP\,2^{SC-20}\,K_p}{PRD+1}$
K_{i_n}	$\frac{125\,KCOMP\,2^{SC-20}\,K_i}{PRD+1}$
K_{d_n}	$\frac{125\,KCOMP\,2^{SC-20}\,K_d}{PRD+1}$
α_n	$\frac{\alpha}{256}$

Table 21: Allowable Register Integer Values

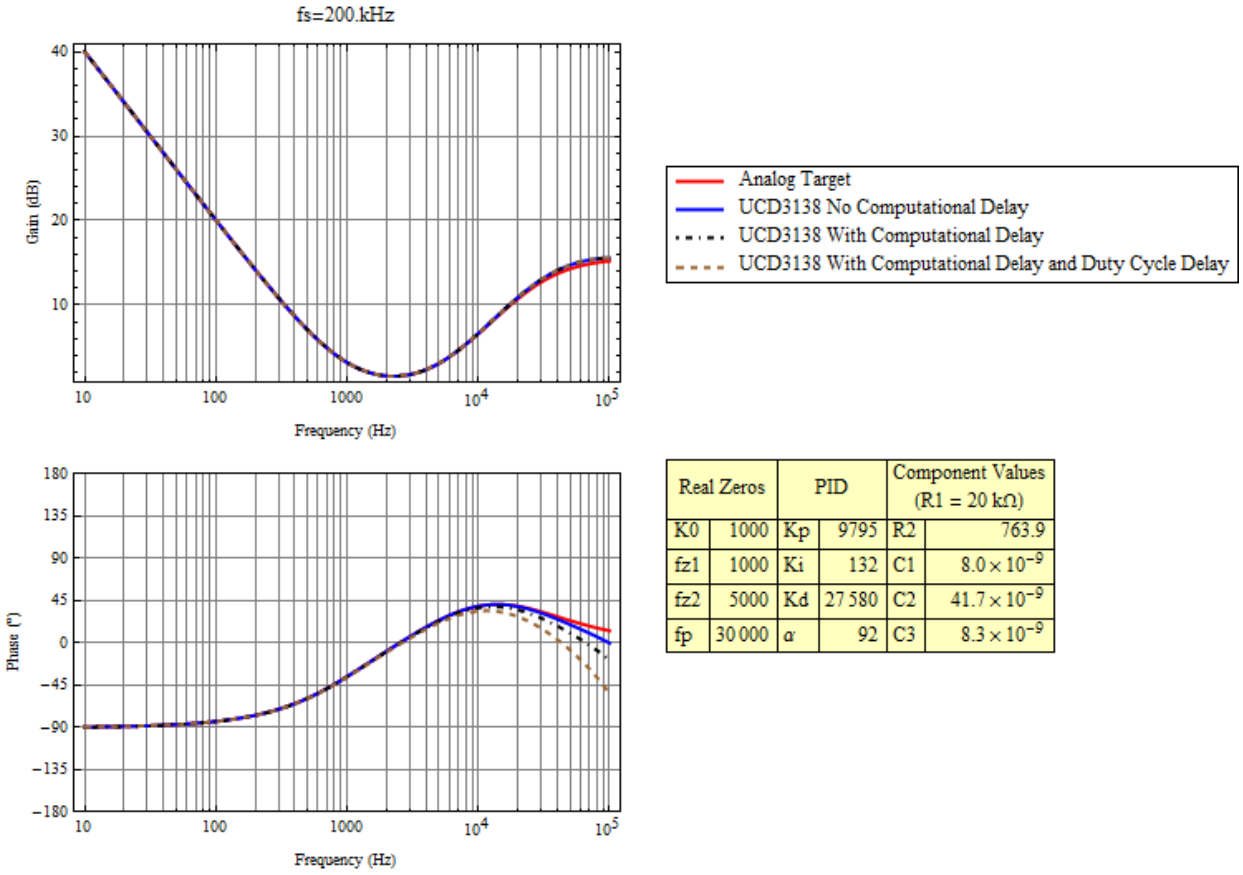
$-32768 \le K_P \le 32767$
$-32768 \le K_I \le 32767$
$-32768 \le K_D \le 32767$
$-256 \le \alpha \le 255$
$0 \le PRD \le 16384$
$0 \le KCOMP \le 16384$
$-4 \le SC \le 3$
$NOS \in \{1, 2, 4, 8\}$

Figure 43 shows a model comparison between the target analog compensator performance and the resulting actual performance of the UCD3138 device. In addition to the constraints shown on the plot the following conditions shown in table 22 were applied.

Table 22: Bode Plot Conditions

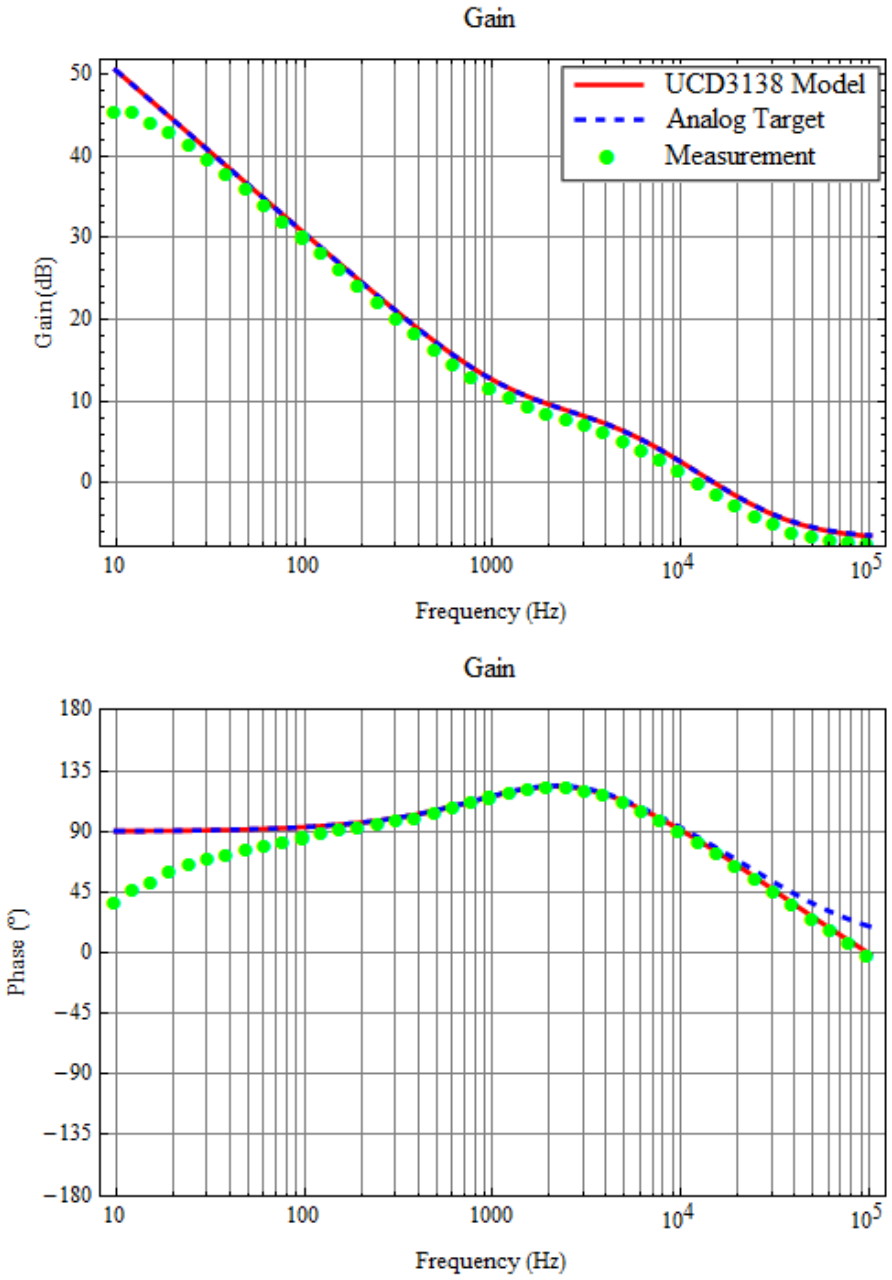
KCOMP = PRD
SC = 0
Over Sampling Rate, NOS = 1
Computation Delay, t_d = 500 ns
Duty Cycle Delay, $D/f_s/2$ = 1 µs

Using figure 3 and equations (21) – (29) are used to generate the analog compensator parameters and performance shown in figure 43.



Real Zeros		PID		Component Values (R1 = 20 kΩ)	
K0	1000	Kp	9795	R2	763.9
fz1	1000	Ki	132	C1	8.0×10^{-9}
fz2	5000	Kd	27 580	C2	41.7×10^{-9}
fp	30 000	α	92	C3	8.3×10^{-9}

Figure 43: UCD3138 Model Comparison



Kp	16797
Ki	176
Kd	−20000
α	240
PRD	499
KCOMP	499
SC	0
NOS	1

Figure 44: Measured Results

Figure 44 shows excellent correlation between the measured results and the model (88). At low frequencies a sizable deviation between the model and measurement is observed. This error is due to the finite limitations of the analyzer to resolve a small signal [22][23]. If a 50 mV disturbance were injected into the loop that would require that the input signal be approximately 0.15 mV on the input. It's not difficult to imagine that the analyzer would have difficulties resolving the magnitude and phase of a signal this small.

5.4 Complex Zeros

The compensation structure of the UCD3138 provides the flexibility to do many things that are not possible with a conventional controller. One such thing is the placement of complex zeros. While advantageous in many applications, care should be used with their application. It would be wrong to assume that nulling out the peaking in a typical second order plant will yield the best load transient response. For example take the plant shown in figure 45.

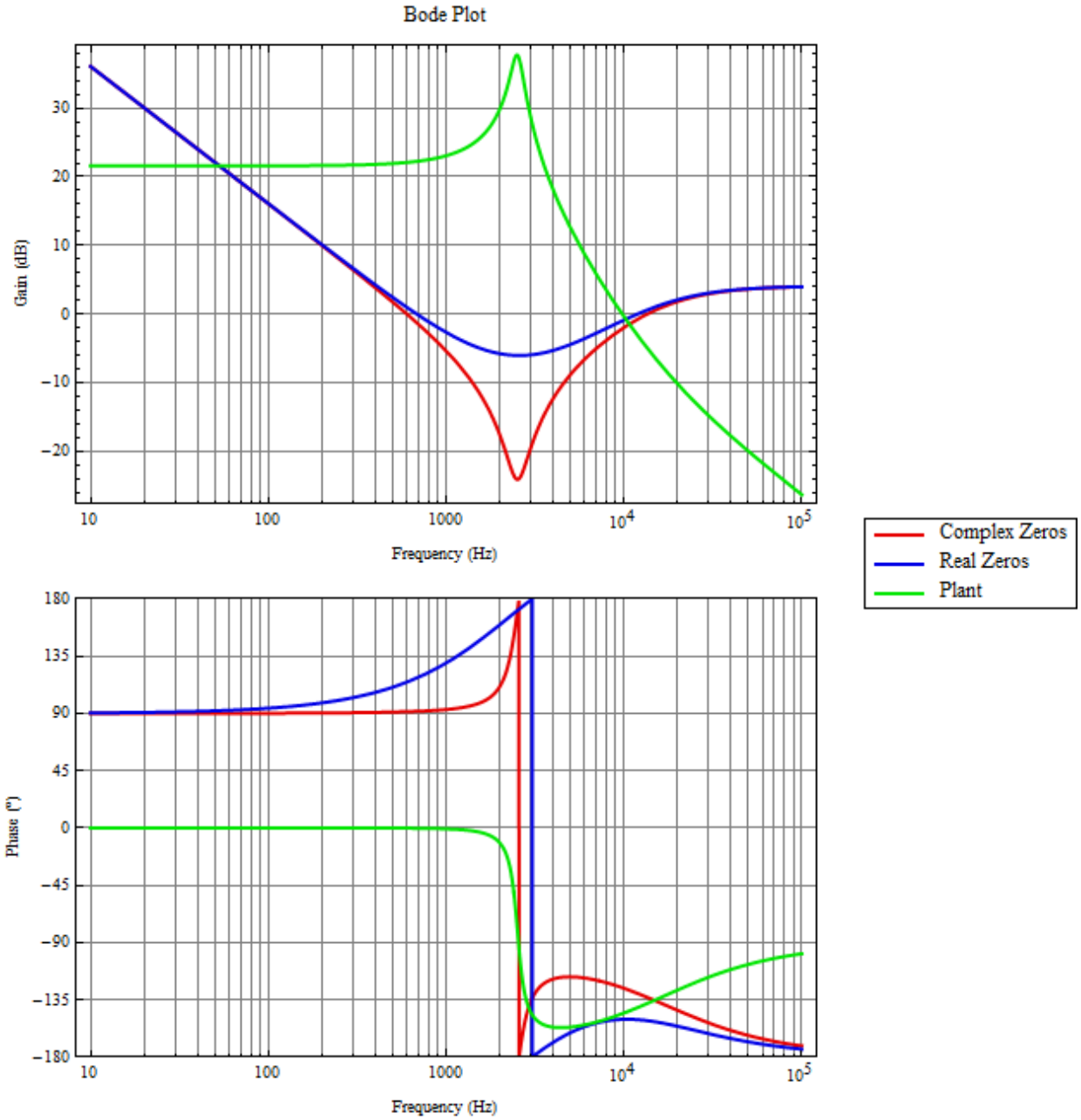


Figure 45: Compensation Comparisons

As shown in figure 45 it is possible to compensate the loop with either complex zeros or real zeros. The complex zeros are capable of completely nulling out the high Q effect of the plant. The results of this compensation are shown in figure 46. Both of these systems have approximately the same bandwidth.

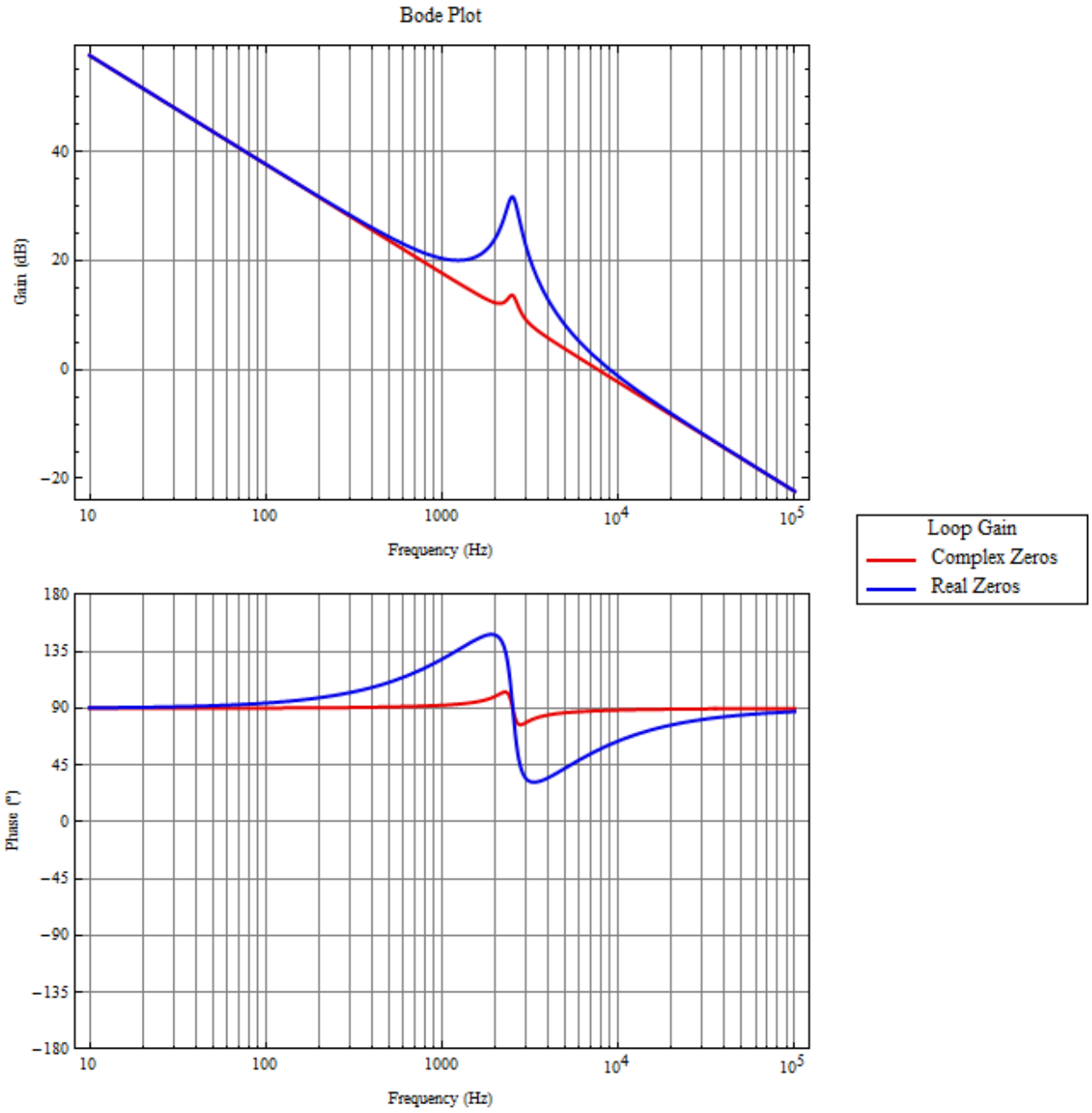


Figure 46: Compensation Comparison – Loop Response

This is a great example of where bandwidth does not adequately describe the targeted closed loop behavior. If bandwidth were the only requirement these two systems would be equivalent. As will be shown shortly the case with the real zeros has far superior performance.

Figure 47 shows the output impedance of each of the open loop system and the closed loop systems with each of the resulting loop gains shown in figure 46. As expected the open loop plant has a large output impedance at

the resonant frequency, owing to the high Q nature of the output filter. This naturally suggests that the addition of loop gain at these critical frequencies can help to reduce this peak. This is in fact what is achieved with the real zeros. By allowing the gain to peak in the loop gain, the compensation offers the system additional “muscle” to reduce the peaking of the output impedance. Reducing the output impedance is directly equivalent to improving the load transient response as is shown in figure 48.

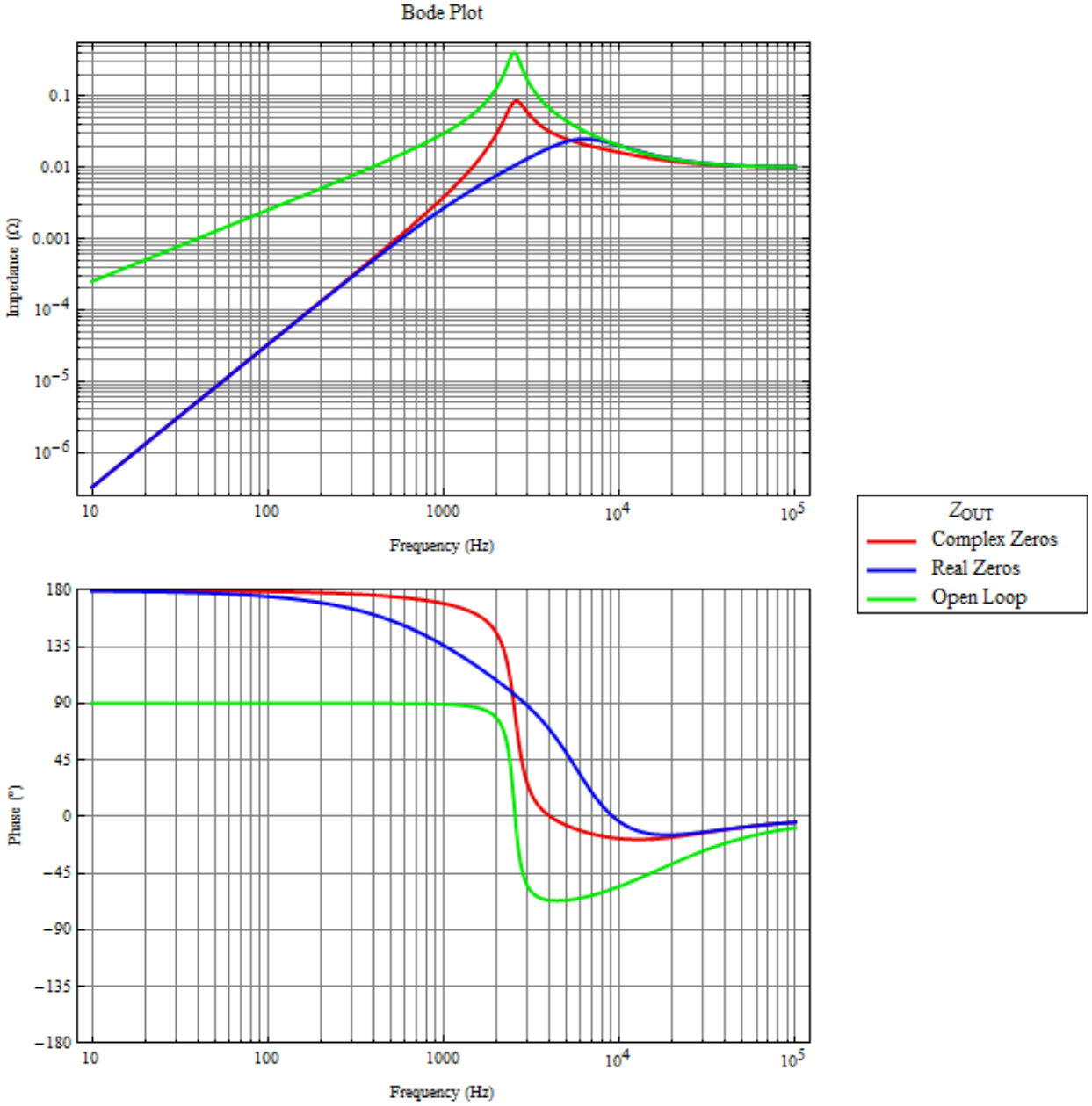


Figure 47: Z_{OUT} Impedance Plots

Figure 48 shows the resulting output voltage disturbance when a step load transient is applied to the output. As the Z_{OUT} plots in figure 47 suggest the resulting output voltage deviation and subsequent settling time are greatly reduced compared to the complex zero compensation. This occurs in spite of the fact that the bandwidth of the two systems is the same.

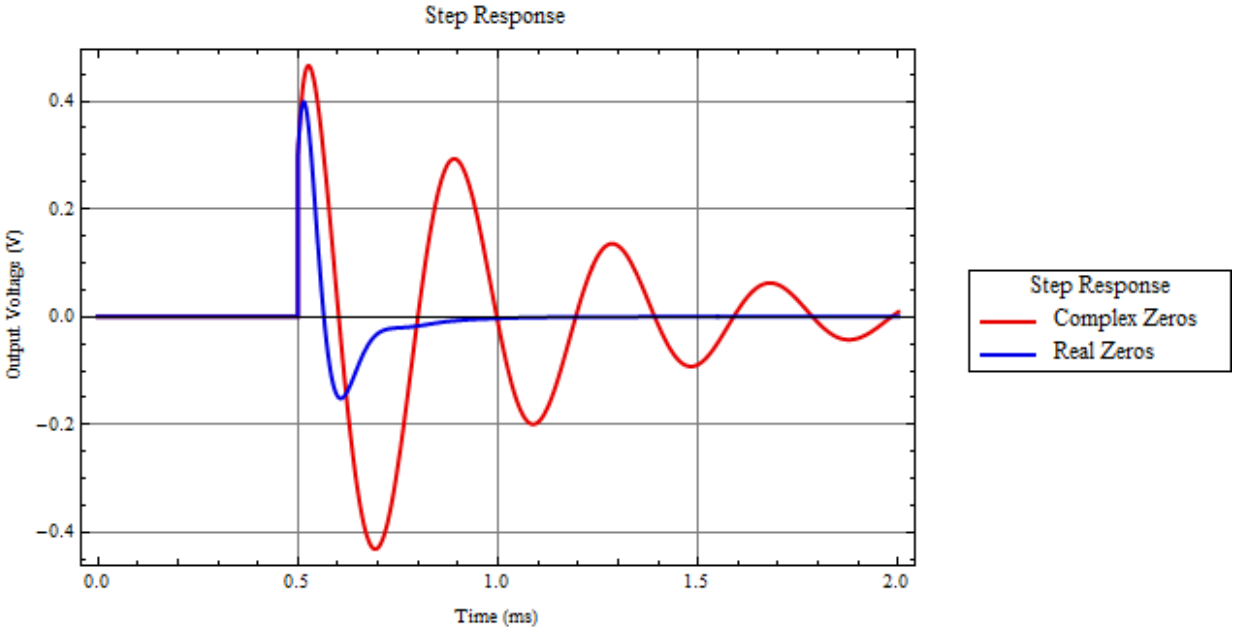


Figure 48: Load Step Response

6 References

6.1 Available UCD3138 Related Literature

- UCD3138 Datasheet, Texas Instruments, 2011
- UCD3138 program manuals
- EVM documentation
- Firmware source code

6.2 References

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