Jetson T5000 and Jetson AGX Orin Series Interface Comparison and Migration

Application Note

DA-11926-001_v1.1 | July 2025

Document History

DA-11926-001_v1.1

Version	Date	Description of Change
1.1	July 17, 2025	Initial release

Table of Contents

List of Figures

List of Tables

Introduction

This application note compares the features and interfaces supported on the NVIDIA® Jetson™ AGX Orin and NVIDIA® Jetson T5000 modules. It describes the migration path for designers familiar with Jetson AGX Orin to design a carrier board for Jetson T5000 that will support the features available on Jetson T5000.

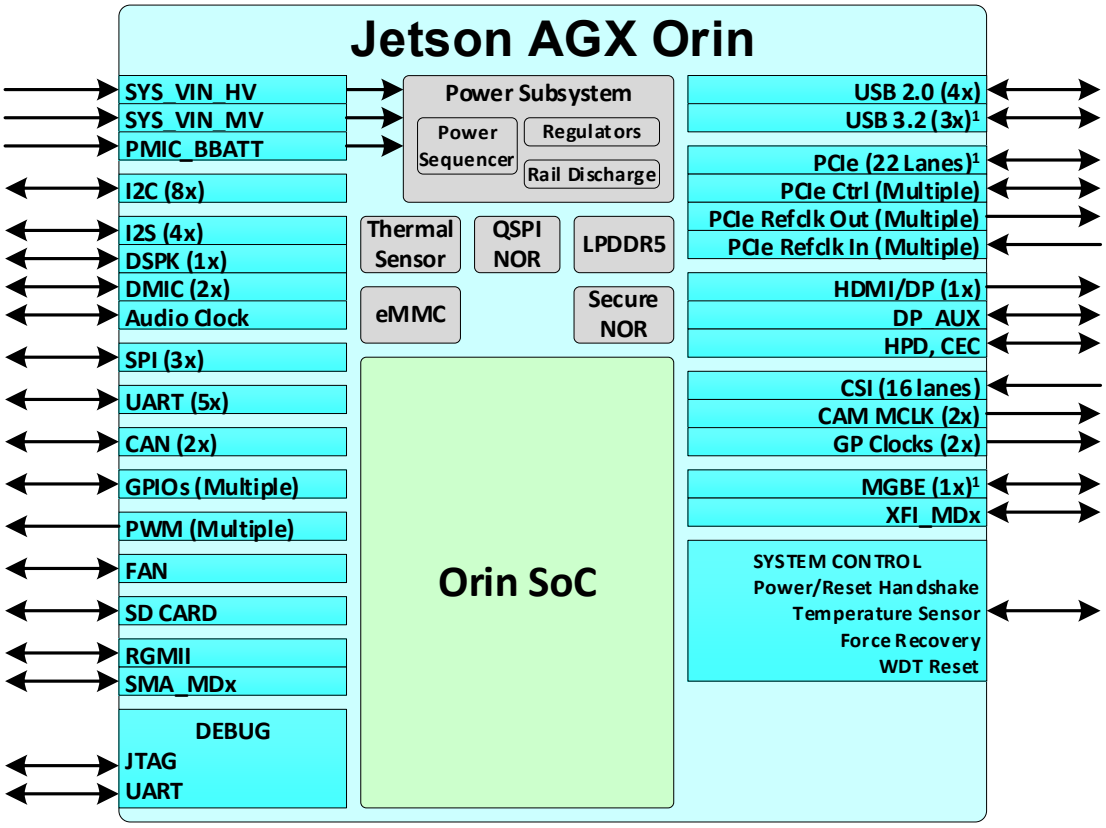
Notes:

- References to Jetson AGX Orin applies to Jetson AGX Orin 64GB except where explicitly noted.

Jetson AGX Orin vs. Jetson T5000

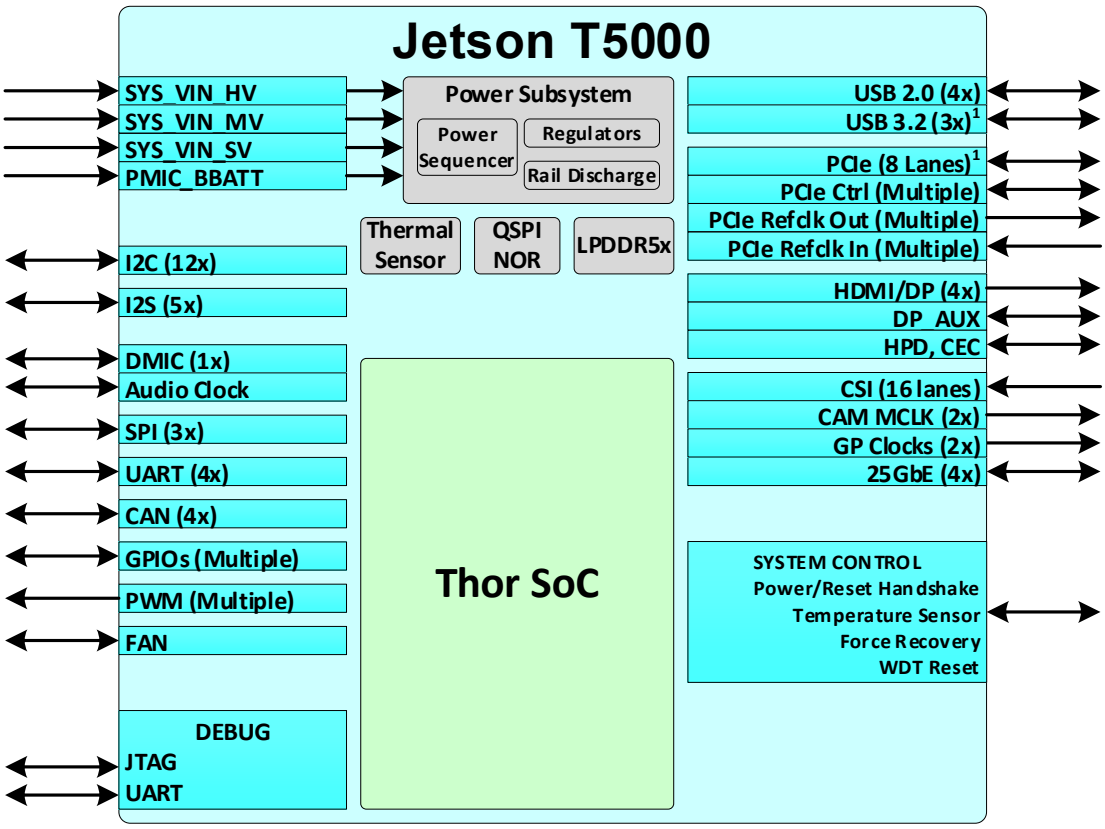
The following figures show the Jetson AGX Orin and Jetson T5000 block diagrams.

Figure 1. Jetson AGX Orin Block Diagram



Note: USB 3.2 ports and MGBE share UPHY lanes with PCIe.

Figure 2. Jetson T5000 Block Diagram



Note: USB 3.2 ports and MGBE share UPHY lanes with PCIe.

Module Interface Comparisons

Table 1 lists the key system specifications, devices, and interfaces that are supported on either the Jetson AGX Orin module or the Jetson T5000 module.

Table 1. Features Comparison

Feature	Jetson AGX Orin 64GB	Jetson T5000
System Specifications and Device on the Module		
AI Performance: Sparse (up to) Dense (up to)	 275 INT8 TOPS 138 INT8 TOPS	 2070 FP4 TFLOPS / 1035 FP8 TFLOPS 1035 FP4 TFLOPS / 517 FP8 TFLOPS
GPU Performance: Tensor Cores (up to) CUDA Cores (up to)	 170 INT8 TOPS or 85 FP16 TFLOPS (sparse) 5.32 FP32 TFLOPS	 2070 FP4 TFLOPS or 1035 FP8 TFLOPS or 517 FP16 TFLOPS (sparse) 8.064 FP32 TFLOPS
DLA Performance	(up to) 105 INT8 TOPS	Not Applicable
GPU	NVIDIA Ampere Architecture with 2048 NVIDIA® CUDA® Cores and 64 Tensor Cores (2 GPC) | 8-TPCs	NVIDIA Blackwell Architecture with 2560 NVIDIA® CUDA® Cores and 96 5th GEN Tensor Cores (3GPC) | 10-TPCs MIG Support
CPU	12x core ARM Cortex A78AE 64-bit CPU, 3 CPU clusters (4 cores/cluster)	14x core Arm® Neoverse V3AE (64-bit) symmetric multi-processing (SMP) CPU architecture | L1 Cache (I, D) per core: 64KB + 64KB | L2 Cache per core: 1MB | L3 Cache 16MB shared System Cache | SPECint@2017_int_base (one core): 6.6 | SPECrate@2017_int_base (all cores): 80
DL Accelerator	2x NVDLA 2.0 Engines	Not Applicable
Vision Accelerator	1x PVA v2	1x PVA v3
Memory	64GB LPDDR5 DRAM 3200 MHz 256-bit, 204 GB/s	128GB LPDDR5x DRAM 4266 MHz 256-bit, 273 GB/s

Feature	Jetson AGX Orin 64GB	Jetson T5000
Storage	64GB eMMC 64MB NOR Boot Flash | 8MB NOR Secure Key Flash	External Storage (NVMe via PCIe) 64MB NOR Boot Flash
Networking:		
RGMII/SGMII	RGMII (10/100/1000 Mbit)	Not Applicable
MGBE	1 x 10Gbps XFI	4x 25Gbps XFI
Video Decode	**1 hardware decoder** AV1 H.264 H.265/HEVC VP9 VP8 VC1 MPEG2 MPEG4	**2 hardware decoders** AV1 H.264 H.265/HEVC VP9 VP8 VC1 MPEG2 MPEG4
Video Encode	**1 hardware encoder** AV1 H.264 H.265/HEVC VP9	**2 hardware encoders** H.264 H.265/HEVC
Video Input:		
CSI	16x lanes MIPI CSI-2 D-PHY 2.1 (40 Gbps) C-PHY 2.0 (164 Gbps)	16x lanes MIPI CSI-2 D-PHY 2.1 (40 Gbps) C-PHY 2.0 (164 Gbps) | 16x trio links
Interfaces		
USB 2.0	4x	
USB 3.x	3x USB 3.2 Gen2 (10 Gbps)	3x USB 3.2 Gen2
PCIe	PCIe Gen 4: 2 x8, 1 x4, 2 x1 Only 2 x8 has Endpoint support | 1 lane of 1 x8 shared with MGBE	(up to) GEN5 | Root Port only – C1 (x1) and C3 (x2) | Dual Mode – C4 (x8), C5 (x4), C2 (x1) Up to 8 lanes PCIe Gen 5
Display	One multi-mode (8K60, 2x4K60) eDP 1.4 (HBR3, MST, DSCT) | HDMI™ 2.1	4x shared VESA DisplayPort 1.4a HBR3 | HDMI™ v2.1
Camera:		
D-PHY	6 x2 or 4 x4	6 x2 or 4 x4
C-PHY	6 x2 or 4 x3 + 2 x1 or 4 x4	6 x2 or 4 x3 + 2 x1 or 4 x4
Virtual Channels (VC)		(up to) 32 cameras using VCs

Feature	Jetson AGX Orin 64GB	Jetson T5000
Audio I2S DMIC DSPK	 4x 2x 1x	 5x 1x Not Supported
SDIO/SD Card	1x SD Card/SDIO	Not Supported
MGBE (Multi-Gigabit Ethernet)	1x 10Gbps XFI (shared with 1 PCIe lane)	4x 25Gbps XFI (see Note 1)
I2C	8x	12x
UART	5x	4x
SPI	3x	3x
CAN	2x	4x
JTAG	Supported	
Fan	PWM and Tach Input	
Miscellaneous		
RTC Back-up	PMIC_BBATT (input only) Supports non-rechargeable cells only	
RTC Accuracy	± 11 sec / day	± 10 sec / day
WiFi	Requires external solution	
Mechanical	100 mm x 87.0 mm x 15.29 mm	
Temperature (Note 1)	-25°C to 80°C	
Power	Max Power Up to 60W 15W | 30W | 50W	75W | 95W | 120W | MAXN
Input Voltage	HV rail: 7V to 20V MV rail: 5V SV rail: 3.3V	

Note:
1. **Measured at Thermal Transfer Plate (TTP) surface.**

Function and Interface Difference Details

Module Power

The following table lists the module power requirement for both the Jetson AGX Orin Module and the Jetson T5000 Module.

Table 2. Module Power Requirement

Parameter	Jetson AGX Orin	Jetson T5000
MAXN (up to)	60W	130W (Note 1)
Note: 1. GPU/CPU clocks are throttled when Total Module Power (TMP) exceeds 130W.		

Input Voltage Rails

Both Jetson AGX Orin and Jetson T5000 have two main input supplies plus an RTC battery back-up supply.

Table 3. Input Voltage Rails Power Supplies

Power Rail	Jetson AGX Orin	Jetson T5000
SYS_VIN_HV	7V to 20V	
SYS_VIN_MV	5V nominal	
SYS_VIN_SV	3.3V nominal	

Power Rail	Jetson AGX Orin	Jetson T5000
PMIC_BBATT (D37)	1.85V-5.5V nom. input for RTC back-up when system is off. Supports only non-rechargeable cells.	

Mechanical Differences

The following table lists the mechanical features for the Jetson T5000 and Jetson AGX Orin. The dimensions of the two modules are the same. The only difference between the two modules is that the spring screws in Jetson T5000 are no longer assessable from the bottom cover.

Table 4. Mechanical Differences

Feature	Jetson AGX Orin	Jetson T5000
Size	100 mm x 87.0 mm x 15.29 mm	
Built-in thermal solution (see note)	Thermal transfer plate (TTP)	
Thermal solution mounting	4x 3.5 mm diameter corner mounting holes	
Note: Additional custom thermal solution required.		

Figure 3. Jetson T5000 Module Drawing

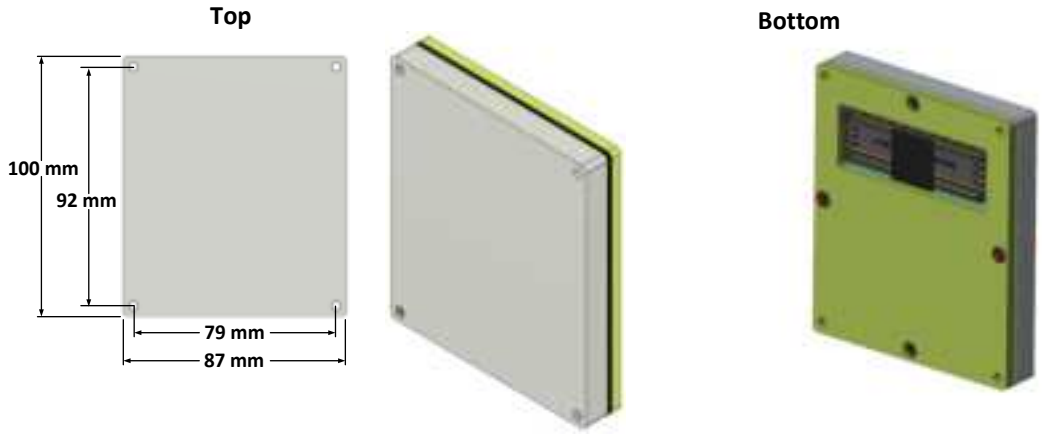
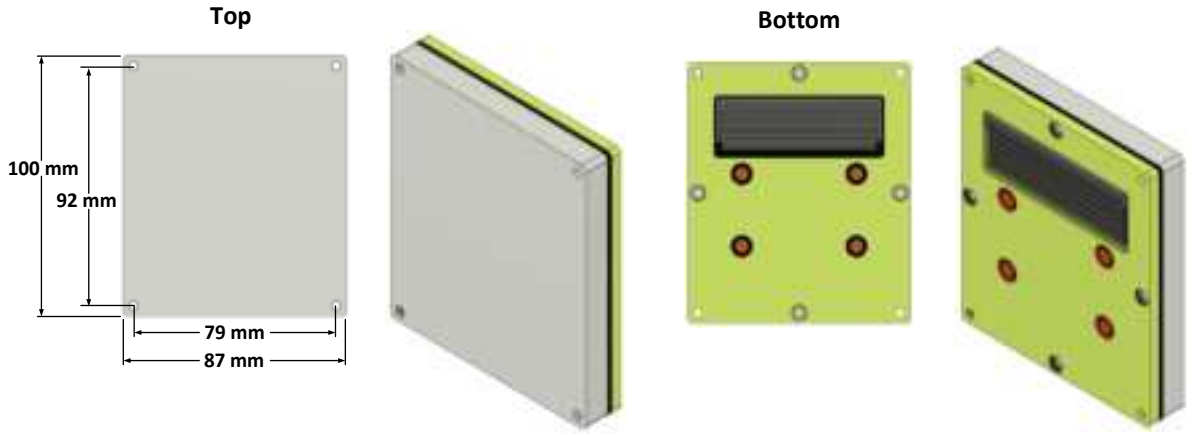


Figure 4. Jetson AGX Orin Module Drawing



Note: The Jetson T5000 does not have the four holes (marked in red in Figure 4) for the spring screws.

Interface Migration

This section shows the functional pin mapping options for the Jetson T5000 and the Jetson AGX Orin and how they align or differ.

UPHY Mapping Options

Jetson T5000 has two UPHY blocks. Jetson AGX Orin has three UPHY blocks. This section details the USB, PCIe, NVMe, and MGBE mapping options for Jetson T5000 and Jetson AGX Orin.

USB 3.x

Jetson T5000 supports three USB 3.2 ports. Jetson AGX Orin also supports three USB 3.2 ports.

PCIe

Jetson T5000 supports up to five PCIe controllers (All up to Gen5 capable).

Jetson AGX Orin supports up to four PCIe controllers (All up to Gen4 capable).

Multi-Gigabit Ethernet

Jetson T5000 has four Multi-Gigabit Ethernet (MGBE) controllers. Jetson AGX Orin has one MGBE controller. Both modules shares UPHY lanes with PCIe in one of the

configurations supported. The modules have XFI MDIO pins to go with the MGBE interface.

Table 5. UPHY Mapping Options

Universal Physical Layer (UPHY)		Jetson AGX Orin		Jetson T5000	
		Config #1	**Config #2**	**Config #1**	**Config #2**
UPHY0	Lane 0	USB 3.2 (P0)	PCIe x1 (C0), RP	USB 3.2 (P0)	USB 3.2 (P0)
	Lane 1	USB 3.2 (P1)	USB 3.2 (P1)	USB 3.2 (P1)	USB 3.2 (P1)
	Lane 2	USB 3.2 (P2)	USB 3.2 (P2)	USB 3.2 (P2)	USB 3.2 (P2)
	Lane 3	PCIe x1 (C1), RP	PCIe x1 (C1), RP	PCIe x1 (C1), RP	PCIe x1 (C1), RP
	Lane 4	PCIe x4 (C4), RP	PCIe x4 (C4), RP	PCIe x1 (C2), DM	PCIe x1 (C2), DM
	Lane 5			SNN	SNN
	Lane 6			PCIe x2 (C3), RP	PCIe x2 (C3), RP
	Lane 7				
UPHY1	Lane 0	PCIe x8 (C5), RP/EP	PCIe x8 (C5), RP/EP	PCIe x8 (C4), DM	PCIe x4 (C5), DM
	Lane 1				
	Lane 2				
	Lane 3				
	Lane 4				MGBE C0 (XFI)
	Lane 5				MGBE C1 (XFI)
	Lane 6				MGBE C2 (XFI)
	Lane 7				MGBE C3 (XFI)
UPHY2	Lane 0		PCIe x8 (C7), RP/EP		
	Lane 1				
	Lane 2				
	Lane 3				
	Lane 4	MGBE (C0)			
	Lane 5				
	Lane 6				
	Lane 7				

HDMI and DisplayPort Mapping Options

Jetson T5000 supports four HDMI™, and VESA® DisplayPort® (DP) interfaces. Jetson AGX Orin supports a single HDMI™, DP, and eDP interface. Both supports multi-head support through MST.

Table 6. HDMI and DisplayPort Mapping Options

Pin #	Jetson AGX Orin Pin Name	Orin SoC Pin Name	Jetson T5000 Pin Name	Thor SoC Pin Name
H48	HDMI_DP0_TX0_N	RSVD	DP1_D0_HDMI_D2_N	HS_DISP1_HDMI_D2_DP0_N
H49	HDMI_DP0_TX0_P		DP1_D0_HDMI_D2_P	HS_DISP1_HDMI_D2_DP0_P
G50	HDMI_DP0_TX1_N		DP1_D1_HDMI_D1_N	HS_DISP1_HDMI_D1_DP1_N
G51	HDMI_DP0_TX1_P		DP1_D1_HDMI_D1_P	HS_DISP1_HDMI_D1_DP1_P
J48	HDMI_DP0_TX2_N		DP1_D2_HDMI_D0_N	HS_DISP1_HDMI_D0_DP2_N
J47	HDMI_DP0_TX2_P		DP1_D2_HDMI_D0_P	HS_DISP1_HDMI_D0_DP2_P
K47	HDMI_DP0_TX3_N		DP1_D3_HDMI_CK_N	HS_DISP1_HDMI_CK_DP3_N
K46	HDMI_DP0_TX3_P		DP1_D3_HDMI_CK_P	HS_DISP1_HDMI_CK_DP3_P
D52	HDMI_DP2_TX0_N	HS_DISP0_HDMI_D2_DP0_N	DP0_D0_HDMI_D2_N	HS_DISP0_HDMI_D2_DP0_N
D51	HDMI_DP2_TX0_P	HS_DISP0_HDMI_D2_DP0_P	DP0_D0_HDMI_D2_P	HS_DISP0_HDMI_D2_DP0_P
B52	HDMI_DP2_TX1_N	HS_DISP0_HDMI_D1_DP1_N	DP0_D1_HDMI_D1_N	HS_DISP0_HDMI_D1_DP1_N
B51	HDMI_DP2_TX1_P	HS_DISP0_HDMI_D1_DP1_P	DP0_D1_HDMI_D1_P	HS_DISP0_HDMI_D1_DP1_P
A50	HDMI_DP2_TX2_N	HS_DISP0_HDMI_D0_DP2_N	DP0_D2_HDMI_D0_N	HS_DISP0_HDMI_D0_DP2_N
A51	HDMI_DP2_TX2_P	HS_DISP0_HDMI_D0_DP2_P	DP0_D2_HDMI_D0_P	HS_DISP0_HDMI_D0_DP2_P
C50	HDMI_DP2_TX3_N	HS_DISP0_HDMI_CK_DP3_N	DP0_D3_HDMI_CK_N	HS_DISP0_HDMI_CK_DP3_N

Pin #	Jetson AGX Orin Pin Name	Orin SoC Pin Name	Jetson T5000 Pin Name	Thor SoC Pin Name
C51	HDMI_DP2_TX3_P	HS_DISP0_HDMI_CK_DP3_P	DP0_D3_HDMI_CK_P	HS_DISP0_HDMI_CK_DP3_P
A14	UPHY_RX8_N	UPHY2	DP2_D0_HDMI_D2_N	HS_DISP2_HDMI_D2_DP0_N
A15	UPHY_RX8_P		DP2_D0_HDMI_D2_P	HS_DISP2_HDMI_D2_DP0_P
J15	UPHY_TX8_N		DP2_D1_HDMI_D1_N	HS_DISP2_HDMI_D1_DP1_N
J14	UPHY_TX8_P		DP2_D1_HDMI_D1_P	HS_DISP2_HDMI_D1_DP1_P
C14	UPHY_RX9_N		DP2_D2_HDMI_D0_N	HS_DISP2_HDMI_D0_DP2_N
C15	UPHY_RX9_P		DP2_D2_HDMI_D0_P	HS_DISP2_HDMI_D0_DP2_P
G14	UPHY_TX9_N		DP2_D3_HDMI_CK_N	HS_DISP2_HDMI_CK_DP3_N
G15	UPHY_TX9_P		DP2_D3_HDMI_CK_P	HS_DISP2_HDMI_CK_DP3_P
D32	UPHY_RX22_N	UPHY0	DP3_D0_HDMI_D2_N	HS_DISP3_HDMI_D2_DP0_N
D33	UPHY_RX22_P		DP3_D0_HDMI_D2_P	HS_DISP3_HDMI_D2_DP0_P
J34	UPHY_TX22_N		DP3_D1_HDMI_D1_N	HS_DISP3_HDMI_D1_DP1_N
J35	UPHY_TX22_P		DP3_D1_HDMI_D1_P	HS_DISP3_HDMI_D1_DP1_P
A35	UPHY_RX23_N		DP3_D2_HDMI_D0_N	HS_DISP3_HDMI_D0_DP2_N
A34	UPHY_RX23_P		DP3_D2_HDMI_D0_P	HS_DISP3_HDMI_D0_DP2_P
H33	UPHY_TX23_N		DP3_D3_HDMI_CK_N	HS_DISP3_HDMI_CK_DP3_N
H32	UPHY_TX23_P		DP3_D3_HDMI_CK_P	HS_DISP3_HDMI_CK_DP3_P

CSI

Jetson T5000 and Jetson AGX Orin both support 16 MIPI CSI lanes and can support the following configurations to cameras or serializers:

- 4 x4
- 3 x4 + 2 x2
- 2 x4 + 4 x2
- 1 x4 + 5 x2
- 6 x2

SDIO and SD Card

Jetson T5000 does not support SDMMC interface. Jetson AGX Orin brings a single SDMMC interfaces to the module pins (SDCARD pins supporting SD Card or SDIO).

Audio

Jetson T5000 supports up to five I2S interfaces. Jetson AGX Orin supports up to four I2S interfaces.

Table 7. Audio Interface Mapping Options

Pin #	Jetson AGX Orin Pin Name	Orin SoC Pin Name	Jetson T5000 Pin Name	Thor SoC Pin Name
L14	I2S1_CLK	GP169	I2S1_CLK	GP156_DAP1_CLK
C7	I2S1_SDOUT	GP170	I2S1_SDOUT	GP157_DAP1_DOUT
H8	I2S1_SDIN	GP171	I2S1_SDIN	GP158_DAP1_DIN
D8	I2S1_FS	GP172	I2S1_FS	GP159_DAP1_FS
G4	I2S2_CLK	GP122	I2S2_CLK	GP184_DAP2_CLK
F5	I2S2_DOUT	GP123	I2S2_DOUT	GP185_DAP2_DOUT
F6	I2S2_DIN	GP124	I2S2_DIN	GP186_DAP2_DIN
E4	I2S2_FS	GP125	I2S2_FS	GP187_DAP2_FS
H16	UPHY_TX7_P	UPHY2	GPIO61	GP272 (I2S3_SCLK)
H17	UPHY_TX7_N		GPIO62	GP273 (I2S3_DOUT)
G19	UPHY_TX5_P		GPIO58	GP274 (I2S3_DIN)
G18	UPHY_TX5_N		GPIO57	GP275 (I2S3_LRCK)

Pin #	Jetson AGX Orin Pin Name	Orin SoC Pin Name	Jetson T5000 Pin Name	Thor SoC Pin Name
C59	I2S3_SCLK	GP206_DAP4_CLK	I2S3_SCLK	GP144_DAP4_CLK (I2S4_SCLK)
K59	I2S3_DOUT	GP207_DAP4_DOUT	I2S3_DOUT	GP145_DAP4_DOUT (I2S4_DOUT)
J59	I2S3_DIN	GP208_DAP4_DIN	I2S3_DIN	GP146_DAP4_DIN (I2S4_DIN)
C60	I2S3_FS	GP209_DAP4_FS	I2S3_FS	GP147_DAP4_FS (I2S4_LRCK)
B58	GPIO21	GP202_DAP6_CLK	GPIO21	Not supported
A59	GPIO05	GP203_DAP6_DOUT	GPIO05	
B59	GPIO04	GP204_DAP6_DIN	GPIO04	
A58	GPIO20	GP205_DAP6_FS	GPIO20	
A7	GPIO29	Misc	GPIO29	GP152 (I2S8_SCLK)
C5	RGMII_RXC		GPIO40	GP153 (I2S8_DOUT)
B8	GPIO11		GPIO11	GP350 (I2S8_DIN)
E10	GPIO12		GPIO12	GP155 (I2S8_LRCK)

DMIC

Jetson T5000 supports a single Digital Microphone (DMIC) interface and Jetson AGX Orin has two.

Table 8. DMIC Interface Mapping Options

Pin #	Jetson AGX Orin Pin Name	Orin SoC Pin Name	Jetson T5000 Pin Name	Thor SoC Pin Name
H53			MCLK03	GP121_CLK2 (DMIC2_CLK)
J54			MCLK02	GP120_CLK1 (DMIC2_DAT)
C61	GPIO9	GP25 (DMIC3_CLK)	GPIO9	Not Supported
B62	GPIO8	GP26 (DMIC3_DAT)	GPIO8	

I2C

Jetson T5000 supports up to twelve I2C interfaces. Jetson AGX Orin supports up to eight I2C interfaces. This includes the DP_AUX pins.

Note: The Jetson T5000 does not have external pull-ups on the DP_AUX pins. Pull-up resistors are required on carrier board.

Table 9. I2C Interface Mapping Options

Pin #	Jetson AGX Orin Pin Name	Orin SoC Pin Name	Jetson T5000 Pin Name	Thor SoC Pin Name
J52	DP1_AUX_CH_P	GP75_I2C4_CLK	I2C0_CLK	GP190_I2C0_CLK
J53	DP1_AUX_CH_N	GP76_I2C4_DAT	I2C0_DAT	GP191_I2C0_DAT
K5	I2C1_CLK	GP126_I2C1_CLK	I2C1_CLK	GP188_I2C1_CLK
L8	I2C1_DAT	GP127_I2C1_DAT	I2C1_DAT	GP189_I2C1_DAT
J61	I2C2_CLK	GP13_I2C2_CLK	I2C2_CLK	GP10_I2C2_CLK
K61	I2C2_DAT	GP14_I2C2_DAT	I2C2_DAT	GP11_I2C2_DAT
D61	I2C4_CLK	GP15_I2C8_CLK	I2C4_CLK	GP12_I2C3_CLK
E60	I2C4_DAT	GP16_I2C8_DAT	I2C4_DAT	GP13_I2C3_DAT
E19	PEX_CLK2_P	PCIE CLK	DP_AUX_CH2_P	SF_DPAUX2_P
E18	PEX_CLK2_N		DP_AUX_CH2_N	SF_DPAUX2_N
G53	DP2_AUX_CH_P	SF_DPAUX01_P	DP_AUX_CH0_P	SF_DPAUX0_P
G54	DP2_AUX_CH_N	SF_DPAUX01_N	DP_AUX_CH0_N	SF_DPAUX0_N
F52	DP0_AUX_CH_P	GP78_I2C7_CLK	I2C8_CLK	GP259_I2C7_CLK
F51	DP0_AUX_CH_N	GP79_I2C7_DAT	I2C8_DAT	GP260_I2C7_DAT
F20	PEX_CLK3_P	PCIE CLK	DP_AUX_CH3_P	SF_DPAUX3_P
F21	PEX_CLK3_N		DP_AUX_CH3_N	SF_DPAUX3_N
A53	I2C5_CLK	GP81_I2C9_CLK	I2C5_CLK	GP261_I2C9_CLK
C53	I2C5_DAT	GP82_I2C9_DAT	I2C5_DAT	GP262_I2C9_DAT
D16	UPHY_RX7_P	UPHY2	DP_AUX_CH1_P	SF_DPAUX1_P
D17	UPHY_RX7_N		DP_AUX_CH1_N	SF_DPAUX1_N
F53	I2C3_CLK	GP54_I2C3_CLK	I2C3_CLK	GP122_I2C12_CLK

Pin #	Jetson AGX Orin Pin Name	Orin SoC Pin Name	Jetson T5000 Pin Name	Thor SoC Pin Name
E53	I2C3_DAT	GP55_I2C3_DAT	I2C3_DAT	GP123_I2C12_DAT
H55	MCLK04	Misc	MCLK04	GP129 (I2C15_CLK)
L57	MCLK05		MCLK05	GP130 (I2C15_DAT)

SPI

Jetson AGX Orin and Jetson T5000 have three SPI interfaces.

Table 10. SPI Interface Mapping Options

Pin #	Function	Jetson AGX Orin Pin Name	Orin SoC Pin Name	Jetson T5000 Pin Name	Thor SoC Pin Name
J57	SPI1	SPI1_CLK	GP47_SPI1_CLK	SPI1_CLK	GP115_SPI1_CLK
D55		SPI1_MOSI	GP49_SPI1_MOSI	SPI1_MOSI	GP117_SPI1_MOSI
A56		SPI1_MISO	GP48_SPI1_MISO	SPI1_MISO	GP116_SPI1_MISO
E55		SPI1_CS0_N	GP50_SPI1_CS0_N	SPI1_CS0_N	GP118_SPI1_CS0_N
B56		SPI1_CS1_N	GP51_SPI1_CS1_N	SPI1_CS1_N	GP119_SPI1_CS1_N
E61	SPI2	SPI2_CLK	GP06_SPI2_CLK	SPI2_CLK	Not Supported
F60		SPI2_MOSI	GP08_SPI2_MOSI	SPI2_MOSI	
D62		SPI2_MISO	GP07_SPI2_MISO	SPI2_MISO	
D60		SPI2_CS0_N	GP09_SPI2_CS_N	SPI2_CS0_N	
F55	SPI3	SPI3_CLK	GP36_SPI3_CLK	SPI3_CLK	GP104_SPI3_CLK
G56		SPI3_MOSI	GP38_SPI3_MOSI	SPI3_MOSI	GP106_SPI3_MOSI
D56		SPI3_MISO	GP37_SPI3_MISO	SPI3_MISO	GP105_SPI3_MISO
C57		SPI3_CS0_N	GP39_SPI3_CS0_N	SPI3_CS0_N	GP107_SPI3_CS0_N
E56		SPI3_CS1_N	GP40_SPI3_CS1_N	SPI3_CS1_N	GP108_SPI3_CS1_N
F10	SPI5	GPIO15	Misc	GPIO15 (SPI5_CLK)	GP148_SPI5_CLK
G7		GPIO13		GPIO13 (SPI5_MOSI)	GP150_SPI5_MOSI
F9		GPIO16		GPIO16 (SPI5_MISO)	GP149_SPI5_MISO

Pin #	Function	Jetson AGX Orin Pin Name	Orin SoC Pin Name	Jetson T5000 Pin Name	Thor SoC Pin Name
L15		GPIO14		GPIO14 (SPI5_CS0_N)	GP151_SPI5_CS0_N

UART

The Jetson T5000 supports up to four UART interfaces. The Jetson AGX Orin supports up to five UART interfaces.

Table 11. UART Interface Mapping Options

Pin #	Jetson AGX Orin Pin Name	Orin SoC Pin Name	Jetson T5000 Pin Name	Thor SoC Pin Name
K53	UART1_TX	GP70_UART1_TXD_ BOOT2_STRAP	UART1_TX	GP134_UART9_TXD
K54	UART1_RX	GP71_UART1_RXD	UART1_RX	GP135_UART9_RXD
L51	UART1_RTS	GP72_UART1_RTS_N	UART1_RTS	GP136_UART9_RTS_N
H54	UART1_CTS	GP73_UART1_CTS_N	UART1_CTS	GP137_UART9_CTS_N
J58	UART5_TX	GP32_UART2_TXD	UART5_TX	GP109_UART5_TXD
H58	UART5_RX	GP33_UART2_RXD	UART5_RX	GP110_UART5_RXD
K58	UART5_RTS	GP34_UART2_RTS_N	UART5_RTS	GP111_UART5_RTS_N
H57	UART5_CTS	GP35_UART2_CTS_N	UART5_CTS	GP112_UART5_CTS_N
H62	UART3_TX_DEBUG	GP11_UART3_TXD	UART3_TX_DEBUG	GP15_UART0_TX
K60	UART3_RX_DEBUG	GP12_UART3_RXD	UART3_RX_DEBUG	GP16_UART0_RX
C58	UART2_TX	GP41_UART5_TXD_ DDRCODE1	UART2_TX	GP100_UART10_TXD
C56	UART2_RX	GP42_UART5_RXD	UART2_RX	GP101_UART10_RXD
G58	UART2_RTS	GP43_UART5_RTS_N_ DDRCODE0	UART2_RTS	GP102_UART10_RTS_ N
A57	UART2_CTS	GP44_UART5_CTS_N	UART2_CTS	GP103_UART10_CTS_ N

Pin #	Jetson AGX Orin Pin Name	Orin SoC Pin Name	Jetson T5000 Pin Name	Thor SoC Pin Name
L5	UART4_TX	GP118_UART4_TXD_ BOOT1_STRAP	UART4_TX	Not Supported
H6	UART4_RX	GP119_UART4_RXD	UART4_RX	
L4	UART4_RTS	GP120_UART4_RTS_N _BOOT0_STRAP	UART4_RTS	
L6	UART4_CTS	GP121_UART4_CTS_N	UART4_CTS	

PWM

Jetson T5000 supports up to six PWM pins and Jetson AGX Orin supports up to four PWM pins.

Table 12. PWM Mapping Options

Pin #	Jetson AGX Orin Pin Name	Orin SoC Pin Name	Jetson T5000 Pin Name	Thor SoC Pin Name
H52	GPIO27	GP88_PWM1	GPIO27	GP257_PWM2
K62	FAN_PWM	GP31_PWM3	FAN_PWM	GP14_PWM4
L49			I2S7_LRCk	GP179_PWM10
L50	GPIO35	GP115		
K57	PWM01	GP68	PWM01	GP132_PWM9
F56			GPIO36	GP258_PWM3
E5			GPIO44	SOC_GPIO177 (PWM5)

CAN

Jetson T5000 supports up to four CAN interfaces and Jetson AGX Orin supports up to two CAN interfaces.

Table 13. CAN Interface Mapping Options

Pin #	Jetson AGX Orin Pin Name	Orin SoC Pin Name	Jetson T5000 Pin Name	Thor SoC Pin Name
G38	FSI_GPIO07		FSI_GPIO07/CAN0_DOUT	GP200_CAN0_DOUT

Pin #	Jetson AGX Orin Pin Name	Orin SoC Pin Name	Jetson T5000 Pin Name	Thor SoC Pin Name
G39	FSI_GPIO08		FSI_GPIO08/CAN0_DIN	GP201_CAN0_DIN
H37	FSI_GPIO09		FSI_GPIO09/CAN1_DOUT	GP205_CAN1_DOUT
H36	FSI_GPIO10		FSI_GPIO10/CAN1_DIN	GP206_CAN1_DIN
J38	FSI_GPIO05		FSI_GPIO05	GP207 (CAN1_STB)
J39	FSI_GPIO06		FSI_GPIO06	GP208 (CAN1_EN)
K36	FSI_GPIO04		FSI_GPIO04	GP209 (CAN1_ERR)
D59	CAN0_DOUT	GP17_CAN0_DOUT	CAN2_DOUT	GP210_CAN2_DOUT
F58	CAN0_DIN	GP18_CAN0_DIN	CAN2_DIN	GP211_CAN2_DIN
B9	PEX_L1_RST_N		FSI_GPIO20	GP212 (CAN2_STB)
H61	CAN1_DOUT	GP19_CAN1_DOUT	CAN3_DOUT	GP215_CAN3_DOUT
B61	CAN1_DIN	GP20_CAN1_DIN	CAN3_DIN	GP216_CAN3_DIN
J10	PEX_L3_CLKREQ_N		FSI_GPIO21	GP217 (CAN3_STB)
K9	PEX_L3_RST_N		FSI_GPIO22	GP218 (CAN3_EN)

Debug

Jetson AGX Orin and Jetson T5000 both support JTAG and a debug UART.

Connector Pin Difference Details

The following table lists the pins that have different functionality between Jetson T5000 and Jetson AGX Orin.

Table 14. Connector Pin Function Differences

Module Pin #	Jetson AGX Orin Pin Name	Orin SoC Signal Name	Jetson T5000 Pin Name	Thor SoC Signal Name
A14	UPHY_RX8_N	UPHY2_RX_N<6>	DP2_D0_HDMI_D2_N	HDMI_DP2_TXD0_N
A15	UPHY_RX8_P	UPHY2_RX_P<6>	DP2_D0_HDMI_D2_P	HDMI_DP2_TXD0_P
A18	UPHY_RX4_P	UPHY2_RX_P<2>	GPIO34	GP133_I2S5_LRCK
A19	UPHY_RX4_N	UPHY2_RX_N<2>	HPD2	DP_HPD2_GP255
A22	UPHY_RX0_P	UPHY0_RX_P<0>	UPHY_RX1_P	UPHY0_RX_P<1>
A23	UPHY_RX0_N	UPHY0_RX_N<0>	UPHY_RX1_N	UPHY0_RX_N<1>
A26	UPHY_RX15_P	UPHY1_RX_P<3>	UPHY_RX11_P	UPHY1_RX_P<3>
A27	UPHY_RX15_N	UPHY1_RX_N<3>	UPHY_RX11_N	UPHY1_RX_N<3>
A30	UPHY_RX19_P	UPHY1_RX_P<7>	UPHY_RX15_P	UPHY1_RX_P<7>
A31	UPHY_RX19_N	UPHY1_RX_N<7>	UPHY_RX15_N	UPHY1_RX_N<7>
A34	UPHY_RX23_P	UPHY0_RX_P<5>	DP3_D2_HDMI_D0_P	HDMI_DP3_TXD2_P
A35	UPHY_RX23_N	UPHY0_RX_N<5>	DP3_D2_HDMI_D0_N	HDMI_DP3_TXD2_N
A38	PEX_C8_CLKREQ_N	UPHY0_GP181_PCIE3_CLKREQ_N	GPIO43	GP283
A39	PEX_C8_RST_N	UPHY0_GP182_PCIE3_RST_N	GPIO37	GP24_DDRCODE1_TSC_EDGE3_BUF
A4	SDCARD_D2	SDCARD_D2_GP133_SDMMC_A2	FSI_GPIO32/SPI4_CS1_N	SPI9_CS1_N_GP243_SDCARD_D2_GP304
A47	GPIO38	GP59	I2C10_CLK	I2C16_CLK_GP270
A48	GPIO37	GP60	I2C10_DAT	I2C16_DAT_GP271
A5	SDCARD_CMD	SDCARD_CMD_GP130_SDMMC_A_CMD	FSI_GPIO34/SPI4_MISO	SPI9_MISO_GP240_SDCARD_CMD_GP301
A50	HDMI_DP2_TX2_N	HDMI_DP0_TXD2_N	DP0_D2_HDMI_D0_N	HDMI_DP0_TXD2_N
A51	HDMI_DP2_TX2_P	HDMI_DP0_TXD2_P	DP0_D2_HDMI_D0_P	HDMI_DP0_TXD2_P
A54	GPIO17	GPIO17_GP56	GPIO46	GP288
A55	GPIO34	GPIO34_M2_EN_GP69	I2C9_CLK	I2C14_CLK_GP138_DMIC1_DAT
A62	GPIO10	GPIO10_GP27_CAN1_GPIO1	GPIO17	GP25_DDRCODE2_TSC_EDGE0_BUF

Module Pin #	Jetson AGX Orin Pin Name	Orin SoC Signal Name	Jetson T5000 Pin Name	Thor SoC Signal Name
B12	UPHY_RX10_P	UPHY0_RX_P<6>	UPHY_RX6_P	UPHY0_RX_P<6>
B13	UPHY_RX10_N	UPHY0_RX_N<6>	UPHY_RX6_N	UPHY0_RX_N<6>
B16	UPHY_RX6_P	UPHY2_RX_P<4>	UPHY_RX16_P	HS_UPHY2_L0_RX_P
B17	UPHY_RX6_N	UPHY2_RX_N<4>	UPHY_RX16_N	HS_UPHY2_L0_RX_N
B20	UPHY_RX2_N	UPHY2_RX_N<0>	UPHY_RX4_N	UPHY0_RX_N<4>
B21	UPHY_RX2_P	UPHY2_RX_P<0>	UPHY_RX4_P	UPHY0_RX_P<4>
B24	UPHY_RX13_N	UPHY1_RX_N<1>	UPHY_RX9_N	UPHY1_RX_N<1>
B25	UPHY_RX13_P	UPHY1_RX_P<1>	UPHY_RX9_P	UPHY1_RX_P<1>
B28	UPHY_RX17_N	UPHY1_RX_N<5>	UPHY_RX13_N	UPHY1_RX_N<5>
B29	UPHY_RX17_P	UPHY1_RX_P<5>	UPHY_RX13_P	UPHY1_RX_P<5>
B3	SYS_VIN_HV21	CONN_VIN_SYS_HV	SYS_VIN_HV_21	CONN_VIN_SYS_HV
B32	UPHY_RX21_N	UPHY0_RX_N<3>	UPHY_RX3_N	UPHY0_RX_N<3>
B33	UPHY_RX21_P	UPHY0_RX_P<3>	UPHY_RX3_P	UPHY0_RX_P<3>
B36	PEX_C7_RST_N	UPHY0_GP178_PCIE1_RST_N	PEX_C1_RST_N	PCIE1_RST_N_GP43
B37	PEX_C7_CLKREQ_N	UPHY0_GP178_PCIE1_CLKREQ_N	PEX_C1_CLKREQ_N	PCIE1_CLKREQ_N_GP42
B5	RGMII_TXC	RGMII_TXC_GP147_RGMII0_TXC	FSI_GPIO26	FSI_GP237
B51	HDMI_DP2_TX1_P	HDMI_DP0_TXD1_P	DP0_D1_HDMI_D1_P	HDMI_DP0_TXD1_P
B52	HDMI_DP2_TX1_N	HDMI_DP0_TXD1_N	DP0_D1_HDMI_D1_N	HDMI_DP0_TXD1_N
B54	WDT_RESET_OUT_N	WDT_RESET_OUT_GP63	GPIO45	GPIO45_GP127_TACH1
B55	GPIO30	GPIO30_IST_DONE_N	GPIO30/IST_DONE_N	GPIO30_IST_DONE_N
B6	SDCARD_CLK	SDCARD_CLK_GP129_SDMMC_A_CLK	FSI_GPIO30/SPI4_CLK	SPI9_CLK_GP239_SDCARD_CLK_L_GP300
B61	CAN1_DIN	CAN1_DIN_GP20_CAN1_DIN	CAN3_DIN	FSI_CAN3_DIN_GP216
B9	PEX_L1_RST_N	UPHY0_GP176_PCIE0_RST_N	FSI_GPIO20	FSI_GP212_CAN2_STB
C14	UPHY_RX9_N	UPHY2_RX_N<7>	DP2_D2_HDMI_D0_N	HDMI_DP2_TXD2_N
C15	UPHY_RX9_P	UPHY2_RX_P<7>	DP2_D2_HDMI_D0_P	HDMI_DP2_TXD2_P
C18	UPHY_RX5_N	UPHY2_RX_N<3>	HPD1	DP_HPD1_GP254
C19	UPHY_RX5_P	UPHY2_RX_P<3>	HPD3	DP_HPD3_GP256
C22	UPHY_RX1_N	UPHY0_RX_N<1>	UPHY_RX2_N	UPHY0_RX_N<2>
C23	UPHY_RX1_P	UPHY0_RX_P<1>	UPHY_RX2_P	UPHY0_RX_P<2>
C26	UPHY_RX14_N	UPHY1_RX_N<2>	UPHY_RX10_N	UPHY1_RX_N<2>
C27	UPHY_RX14_P	UPHY1_RX_P<2>	UPHY_RX10_P	UPHY1_RX_P<2>
C30	UPHY_RX18_N	UPHY1_RX_N<6>	UPHY_RX14_N	UPHY1_RX_N<6>
C31	UPHY_RX18_P	UPHY1_RX_P<6>	UPHY_RX14_P	UPHY1_RX_P<6>

Module Pin #	Jetson AGX Orin Pin Name	Orin SoC Signal Name	Jetson T5000 Pin Name	Thor SoC Signal Name
C34	UPHY_RX20_P	UPHY0_RX_P<2>	UPHY_RX0_P	UPHY0_RX_P<0>
C35	UPHY_RX20_N	UPHY0_RX_N<2>	UPHY_RX0_N	UPHY0_RX_N<0>
C38	UPHY_REFCLK4_N	UPHY1_REFCLK1_N	GPIO32	GP125_I2S5_SCLK
C39	UPHY_REFCLK4_P	UPHY1_REFCLK1_P	GPIO18	GPIO18_GP128_I2S5_DIN
C4	RGMII_RD0	RGMII_RD0_GP153_RGMII0_RD0	GPIO47	GP287
C5	RGMII_RXC	RGMII_RXC_GP158_RGMII0_RXC	GPIO40	GPIO40_GP153
C50	HDMI_DP2_TX3_N	HDMI_DP0_TXD3_N	DP0_D3_HDMI_CK_N	HDMI_DP0_TXD3_N
C51	HDMI_DP2_TX3_P	HDMI_DP0_TXD3_P	DP0_D3_HDMI_CK_P	HDMI_DP0_TXD3_P
C54	GPIO33	GPIO33_GP87_XFI1_MDIO	GPIO33/XFI1_MDIO	GPIO33_GP68_XFI1_MDIO
C55	GPIO18	GPIO18_GP64	GPIO39/BOOT_CHAIN_0	GPIO39_GP278_BOOT_CHAIN_0
C8	PEX_C5_CLKREQ_N	UPHY1_GP210_PCIE5_CLKREQ_N	PEX_C4_CLKREQ_N	PCIE4_CLKREQ_N_GP60
D10	PEX_L0_RST_N	UPHY2_GP188_PCIE7_RST_N	PEX_C2_RST_N	PCIE2_RST_N_GP45
D12	UPHY_RX11_P	UPHY0_RX_P<7>	UPHY_RX7_P	UPHY0_RX_P<7>
D13	UPHY_RX11_N	UPHY0_RX_N<7>	UPHY_RX7_N	UPHY0_RX_N<7>
D16	UPHY_RX7_P	UPHY2_RX_P<5>	DP_AUX_CH1_P	DP_AUX_CH1_P_I2C10_CLK
D17	UPHY_RX7_N	UPHY2_RX_N<5>	DP_AUX_CH1_N	DP_AUX_CH1_N_I2C10_DAT
D20	UPHY_RX3_P	UPHY2_RX_P<1>	UPHY_RX5_P	UPHY0_RX_P<5>
D21	UPHY_RX3_N	UPHY2_RX_N<1>	UPHY_RX5_N	UPHY0_RX_N<5>
D24	UPHY_RX12_P	UPHY1_RX_P<0>	UPHY_RX8_P	UPHY1_RX_P<0>
D25	UPHY_RX12_N	UPHY1_RX_N<0>	UPHY_RX8_N	UPHY1_RX_N<0>
D28	UPHY_RX16_P	UPHY1_RX_P<4>	UPHY_RX12_P	UPHY1_RX_P<4>
D29	UPHY_RX16_N	UPHY1_RX_N<4>	UPHY_RX12_N	UPHY1_RX_N<4>
D32	UPHY_RX22_N	UPHY0_RX_N<4>	DP3_D0_HDMI_D2_N	HDMI_DP3_TXD0_N
D33	UPHY_RX22_P	UPHY0_RX_P<4>	DP3_D0_HDMI_D2_P	HDMI_DP3_TXD0_P
D48	PEX_CLK6_N	UPHY0_SF_PCIE1_CLK_N	UPHY_REFCLK6_N	HS_UPHY0_REFCLK2_N
D49	PEX_CLK6_P	UPHY0_SF_PCIE1_CLK_P	UPHY_REFCLK6_P	HS_UPHY0_REFCLK2_P
D5	RGMII_RX_CTL	RGMII_RX_CTL_GP157_RGMII0_RX_CTL	GPIO48	GPIO48_GP279
D51	HDMI_DP2_TX0_P	HDMI_DP0_TXD0_P	DP0_D0_HDMI_D2_P	HDMI_DP0_TXD0_P
D52	HDMI_DP2_TX0_N	HDMI_DP0_TXD0_N	DP0_D0_HDMI_D2_N	HDMI_DP0_TXD0_N
D54	GPIO03	GPIO03_GP84_XFI2_MDC	GPIO03/XFI2_MDC	GPIO03_GP71_XFI2_MDC
D59	CAN0_DOUT	CAN0_DOUT_GP17_CAN0_DOUT	CAN2_DOUT	FSI_CAN2_DOUT_GP210
D6	SDCARD_D3	SDCARD_D3_GP134_SDMMC_A3	FSI_GPIO33/SPI4_CS2_N	SPI9_CS2_N_GP244_SDCARD_D3_GP305
D9	PEX_L1_CLKREQ_N	UPHY0_GP175_PCIE0_CLKREQ_N	FSI_GPIO25	FSI_GP219

Module Pin #	Jetson AGX Orin Pin Name	Orin SoC Signal Name	Jetson T5000 Pin Name	Thor SoC Signal Name
E11	PEX_L0_CLKREQ_N	UPHY2_GP187_PCIE7_CLKREQ_N	PEX_C2_CLKREQ_N	PCIE2_CLKREQ_N_GP44
E14	PEX_CLK0_N	UPHY2_SF_PCIE7_CLK_N	UPHY_REFCLK5_N	HS_UPHY0_REFCLK3_N
E15	PEX_CLK0_P	UPHY2_SF_PCIE7_CLK_P	UPHY_REFCLK5_P	HS_UPHY0_REFCLK3_P
E18	PEX_CLK2_N	UPHY2_SF_PCIE8_CLK_N	DP_AUX_CH2_N	DP_AUX_CH2_N_I2C4_DAT
E19	PEX_CLK2_P	UPHY2_SF_PCIE8_CLK_P	DP_AUX_CH2_P	DP_AUX_CH2_P_I2C4_CLK
E22	PEX_CLK4_N	UPHY0_SF_PCIE4_CLK_N	UPHY_REFCLK4_N	HS_UPHY0_REFCLK4_N
E23	PEX_CLK4_P	UPHY0_SF_PCIE4_CLK_P	UPHY_REFCLK4_P	HS_UPHY0_REFCLK4_P
E26	UPHY_REFCLK1_N	UPHY2_REFCLK1_N	I2C7_DAT	I2C11_DAT_GP161
E27	UPHY_REFCLK1_P	UPHY2_REFCLK1_P	I2C7_CLK	I2C11_CLK_GP160
E30	UPHY_REFCLK0_P	UPHY1_REFCLK0_P	FSI_GPIO24	FSI_GP235
E31	UPHY_REFCLK0_N	UPHY1_REFCLK0_N	FSI_GPIO23	FSI_GP236
E34	FSI_GPIO15	GP198_SPI7_CS0_N	FSI_GPIO15/SPI5_CS0_N	FSI_GPIO15_GP224_SPI7_CS0_N
E35	FSI_GPIO14	GP197_SPI7_MOSI	FSI_GPIO14/SPI5_MOSI	FSI_GPIO14_GP223_SPI7_MOSI
E5	RGMII_RD3	RGMII_RD3_GP156_RGMII0_RD3	GPIO44	GP177_PWM5
E50	FSI_GPIO19	GP215	FSI_GPIO19/SGMII1_MDIO	FSI_GP245_SGMII1_MDIO
E51	FSI_GPIO18	GP214	FSI_GPIO18/SGMII1_MDC	FSI_GP246_SGMII1_MDC
E59	GPIO06	GPIO6_GP21_CAN0_GPIO0	GPIO38	GP23_DDRCODE0_TSC_EDGE2_BUF
E6	RGMII_SMA_MDC	RGMII_SMA_MDC_GP160_RGMII0_SMA_MDC	SGMII0_MDC/GPIO52	SGMII0_MDC_GP51
E7	RGMII_SMA_MDIO	RGMII_SMA_MDIO_GP159_RGMII0_SMA_MDIO	SGMII0_MDIO/GPIO53	SGMII0_MDIO_GP50
E8	SDCARD_D0	SDCARD_D0_GP131_SDMMC_A0	FSI_GPIO35/SPI4_MOSI	SPI9_MOSI_GP241_SDCARD_D0_GP302
F16	PEX_CLK1_P	UPHY0_SF_PCIE0_CLK_P	UPHY_REFCLK0_P	HS_UPHY1_REFCLK0_P
F17	PEX_CLK1_N	UPHY0_SF_PCIE0_CLK_N	UPHY_REFCLK0_N	HS_UPHY1_REFCLK0_N
F20	PEX_CLK3_P	UPHY2_SF_PCIE10_CLK_P	DP_AUX_CH3_P	DP_AUX_CH3_P_I2C8_CLK
F21	PEX_CLK3_N	UPHY2_SF_PCIE10_CLK_N	DP_AUX_CH3_N	DP_AUX_CH3_N_I2C8_DAT
F24	PEX_CLK5_P	UPHY1_SF_PCIE5_CLK_P	UPHY_REFCLK1_P	HS_UPHY1_REFCLK2_P
F25	PEX_CLK5_N	UPHY1_SF_PCIE5_CLK_N	UPHY_REFCLK1_N	HS_UPHY1_REFCLK2_N
F36	FSI_GPIO13	GP196_SPI7_MISO	FSI_GPIO13/SPI5_MISO	FSI_GPIO13_GP222_SPI7_MISO
F37	FSI_GPIO12	GP195_SPI7_CLK	FSI_GPIO12/SPI5_CLK	FSI_GPIO12_GP221_SPI7_CLK
F51	DP0_AUX_CH_N	DP2_AUX_CH_N_I2C7_DAT	I2C8_DAT	I2C7_DAT_GP260
F52	DP0_AUX_CH_P	DP2_AUX_CH_P_I2C7_CLK	I2C8_CLK	I2C7_CLK_GP259
F58	CAN0_DIN	CAN0_DIN_GP18_CAN0_DIN	CAN2_DIN	FSI_CAN2_DIN_GP211
F59	GPIO07	GPIO7_GP24_CAN0_GPIO1	GPIO42	GP26_DDRCODE3_TSC_EDGE1_BUF

Module Pin #	Jetson AGX Orin Pin Name	Orin SoC Signal Name	Jetson T5000 Pin Name	Thor SoC Signal Name
F8	SDCARD_D1	SDCARD_D1_GP132_SDMMC_A1	FSI_GPIO31/SPI4_CS0_N	SPI9_CS0_N_GP242_SDCARD_D1_GP303
G14	UPHY_TX9_N	UPHY2_TX_N<7>	DP2_D3_HDMI_CK_N	HDMI_DP2_TXD3_N
G15	UPHY_TX9_P	UPHY2_TX_P<7>	DP2_D3_HDMI_CK_P	HDMI_DP2_TXD3_P
G18	UPHY_TX5_N	UPHY2_TX_N<3>	GPIO57	GPIO57_GP275_I2S3_LRCK
G19	UPHY_TX5_P	UPHY2_TX_P<3>	GPIO58	GPIO58_GP274_I2S3_DIN
G22	UPHY_TX1_N	UPHY0_TX_N<1>	UPHY_TX2_N	UPHY0_TX_N<2>
G23	UPHY_TX1_P	UPHY0_TX_P<1>	UPHY_TX2_P	UPHY0_TX_P<2>
G26	UPHY_TX14_N	UPHY1_TX_N<2>	UPHY_TX10_N	UPHY1_TX_N<2>
G27	UPHY_TX14_P	UPHY1_TX_P<2>	UPHY_TX10_P	UPHY1_TX_P<2>
G30	UPHY_TX18_N	UPHY1_TX_N<6>	UPHY_TX14_N	UPHY1_TX_N<6>
G31	UPHY_TX18_P	UPHY1_TX_P<6>	UPHY_TX14_P	UPHY1_TX_P<6>
G34	UPHY_TX21_N	UPHY0_TX_N<3>	UPHY_TX3_N	UPHY0_TX_N<3>
G35	UPHY_TX21_P	UPHY0_TX_P<3>	UPHY_TX3_P	UPHY0_TX_P<3>
G38	FSI_GPIO07	GP90_CAN2_DOUT	FSI_GPIO07/CAN0_DOUT	FSI_GPIO07_GP200_CAN0_DOUT
G39	FSI_GPIO08	GP91_CAN2_DIN	FSI_GPIO08/CAN0_DIN	FSI_GPIO08_GP201_CAN0_DIN
G4	I2S2_CLK	I2S2_CLK_GP122	I2S2_CLK/BOOT_CHAIN_1	I2S2_CLK_GP184_BOOT_CHAIN_1
G5	RGMII_TD1	RGMII_TD1_GP149_RGMII0_TD1	GPIO56/BOOT_CHAIN_SEL	GPIO56_GP277_BOOT_CHAIN_SEL
G50	HDMI_DP0_TX1_N	SNN	DP1_D1_HDMI_D1_N	HDMI_DP1_TXD1_N
G51	HDMI_DP0_TX1_P	SNN	DP1_D1_HDMI_D1_P	HDMI_DP1_TXD1_P
G53	DP2_AUX_CH_P	DP_AUX_CH0_P	DP_AUX_CH0_P	DP_AUX_CH0_P_I2C6_CLK
G54	DP2_AUX_CH_N	DP_AUX_CH0_N	DP_AUX_CH0_N	DP_AUX_CH0_N_I2C6_DAT
G6	RGMII_TD3	RGMII_TD3_GP151_RGMII0_TD3	GPIO49	GP286
G8	PEX_L4_CLKREQ_N	UPHY0_GP183_PCIE4_CLKREQ_N	PEX_C3_CLKREQ_N	PCIE3_CLKREQ_N_GP46
H10	PEX_C5_RST_N	UPHY1_GP211_PCIE5_RST_N	PEX_C4_RST_N	PCIE4_RST_N_GP61
H12	UPHY_TX11_P	UPHY0_TX_P<7>	UPHY_TX7_P	UPHY0_TX_P<7>
H13	UPHY_TX11_N	UPHY0_TX_N<7>	UPHY_TX7_N	UPHY0_TX_N<7>
H16	UPHY_TX7_P	UPHY2_TX_P<5>	GPIO61	GPIO61_GP272_I2S3_SCLK
H17	UPHY_TX7_N	UPHY2_TX_N<5>	GPIO62	GPIO62_GP273_I2S3_DOUT
H20	UPHY_TX3_P	UPHY2_TX_P<1>	UPHY_TX5_P	UPHY0_TX_P<5>
H21	UPHY_TX3_N	UPHY2_TX_N<1>	UPHY_TX5_N	UPHY0_TX_N<5>
H24	UPHY_TX12_P	UPHY1_TX_P<0>	UPHY_TX8_P	UPHY1_TX_P<0>
H25	UPHY_TX12_N	UPHY1_TX_N<0>	UPHY_TX8_N	UPHY1_TX_N<0>

Module Pin #	Jetson AGX Orin Pin Name	Orin SoC Signal Name	Jetson T5000 Pin Name	Thor SoC Signal Name
H28	UPHY_TX16_P	UPHY1_TX_P<4>	UPHY_TX12_P	UPHY1_TX_P<4>
H29	UPHY_TX16_N	UPHY1_TX_N<4>	UPHY_TX12_N	UPHY1_TX_N<4>
H32	UPHY_TX23_P	UPHY0_TX_P<5>	DP3_D3_HDMI_CK_P	HDMI_DP3_TXD3_P
H33	UPHY_TX23_N	UPHY0_TX_N<5>	DP3_D3_HDMI_CK_N	HDMI_DP3_TXD3_N
H36	FSI_GPIO10	GP96_CAN3_DIN	FSI_GPIO10/CAN1_DIN	FSI_GPIO10_GP206_CAN1_DIN
H37	FSI_GPIO09	GP95_CAN3_DOUT	FSI_GPIO09/CAN1_DOUT	FSI_GPIO09_GP205_CAN1_DOUT
H48	HDMI_DP0_TX0_N	SNN	DP1_D0_HDMI_D2_N	HDMI_DP1_TXD0_N
H49	HDMI_DP0_TX0_P	SNN	DP1_D0_HDMI_D2_P	HDMI_DP1_TXD0_P
H5	ENET_RST_N	ENET_RST_GP112	GPIO59	GPIO59_GP175
H51	GPIO26	GPIO26_GP86_XFI0_MDC	GPIO26/XFI0_MDC	GPIO26_GP65_XFI0_MDC
H6	RGMII_RD2	RGMII_RD2_GP155_RGMII0_RD2	UART4_RX	UART4_RX_GP181
H60	GPIO31	GPIO31_IST_REQ	GPIO31/IST_REQ_N	GPIO31_IST_REQ_N_GP131
H61	CAN1_DOUT	CAN1_DOUT_GP19_CAN1_DOUT	CAN3_DOUT	FSI_CAN3_DOUT_GP215
J10	PEX_L3_CLKREQ_N	UPHY2_GP193_PCIE10_CLKREQ_N	FSI_GPIO21	FSI_GP217_CAN3_STB
J11	PEX_L2_CLKREQ_N	UPHY2_GP189_PCIE8_CLKREQ_N	FSI_GPIO29/I2C6_DAT	FSI_I2C13_DAT_GP232
J14	UPHY_TX8_P	UPHY2_TX_P<6>	DP2_D1_HDMI_D1_P	HDMI_DP2_TXD1_P
J15	UPHY_TX8_N	UPHY2_TX_N<6>	DP2_D1_HDMI_D1_N	HDMI_DP2_TXD1_N
J18	UPHY_TX4_P	UPHY2_TX_P<2>	GPIO50	GP276
J19	UPHY_TX4_N	UPHY2_TX_N<2>	GPIO67	GP00
J22	UPHY_TX0_P	UPHY0_TX_P<0>	UPHY_TX1_P	UPHY0_TX_P<1>
J23	UPHY_TX0_N	UPHY0_TX_N<0>	UPHY_TX1_N	UPHY0_TX_N<1>
J26	UPHY_TX15_P	UPHY1_TX_P<3>	UPHY_TX11_P	UPHY1_TX_P<3>
J27	UPHY_TX15_N	UPHY1_TX_N<3>	UPHY_TX11_N	UPHY1_TX_N<3>
J30	UPHY_TX19_P	UPHY1_TX_P<7>	UPHY_TX15_P	UPHY1_TX_P<7>
J31	UPHY_TX19_N	UPHY1_TX_N<7>	UPHY_TX15_N	UPHY1_TX_N<7>
J34	UPHY_TX22_N	UPHY0_TX_N<4>	DP3_D1_HDMI_D1_N	HDMI_DP3_TXD1_N
J35	UPHY_TX22_P	UPHY0_TX_P<4>	DP3_D1_HDMI_D1_P	HDMI_DP3_TXD1_P
J47	HDMI_DP0_TX2_P	SNN	DP1_D2_HDMI_D0_P	HDMI_DP1_TXD2_P
J48	HDMI_DP0_TX2_N	SNN	DP1_D2_HDMI_D0_N	HDMI_DP1_TXD2_N
J5	ENET_INT	ENET_INT_GP111	GPIO63	GPIO63_GP174
J51	GPIO24	GPIO24_GP83_XFI2_MDIO	GPIO24/XFI2_MDIO	GPIO24_GP70_XFI2_MDIO
J52	DP1_AUX_CH_P	DP1_AUX_CH_P_I2C4_CLK	I2C0_CLK	I2C0_CLK_GP190
J53	DP1_AUX_CH_N	DP1_AUX_CH_N_I2C4_DAT	I2C0_DAT	I2C0_DAT_GP191

Module Pin #	Jetson AGX Orin Pin Name	Orin SoC Signal Name	Jetson T5000 Pin Name	Thor SoC Signal Name
J55	GPIO32	GPIO32_GP58	I2C9_DAT	GP284
J6	RGMII_TD0	RGMII_TD0_GP148_RGMII0_TD0	GPIO64	GPIO64_GP171
J7	RGMII_TD2	RGMII_TD2_GP150_RGMII0_TD2	GPIO65	GPIO65_GP285
J9	PEX_L4_RST_N	UPHY0_GP184_PCIE4_RST_N	PEX_C3_RST_N	PCIE3_RST_N_GP47
K10	PEX_L2_RST_N	UPHY2_GP190_PCIE8_RST_N	FSI_GPIO28/I2C6_CLK	FSI_I2C13_CLK_GP231
K12	UPHY_TX10_N	UPHY0_TX_N<6>	UPHY_TX6_N	UPHY0_TX_N<6>
K13	UPHY_TX10_P	UPHY0_TX_P<6>	UPHY_TX6_P	UPHY0_TX_P<6>
K16	UPHY_TX6_N	UPHY2_TX_N<4>	UPHY_TX16_N	HS_UPHY2_L0_TX_N
K17	UPHY_TX6_P	UPHY2_TX_P<4>	UPHY_TX16_P	HS_UPHY2_L0_TX_P
K20	UPHY_TX2_N	UPHY2_TX_N<0>	UPHY_TX4_N	UPHY0_TX_N<4>
K21	UPHY_TX2_P	UPHY2_TX_P<0>	UPHY_TX4_P	UPHY0_TX_P<4>
K24	UPHY_TX13_N	UPHY1_TX_N<1>	UPHY_TX9_N	UPHY1_TX_N<1>
K25	UPHY_TX13_P	UPHY1_TX_P<1>	UPHY_TX9_P	UPHY1_TX_P<1>
K28	UPHY_TX17_N	UPHY1_TX_N<5>	UPHY_TX13_N	UPHY1_TX_N<5>
K29	UPHY_TX17_P	UPHY1_TX_P<5>	UPHY_TX13_P	UPHY1_TX_P<5>
K32	UPHY_TX20_P	UPHY0_TX_P<2>	UPHY_TX0_P	UPHY0_TX_P<0>
K33	UPHY_TX20_N	UPHY0_TX_N<2>	UPHY_TX0_N	UPHY0_TX_N<0>
K37	FSI_GPIO03	GP100_SOC_ERROR_N	FSI_GPIO03/SOC_ERROR	FSI_GPIO03_GP220_SOC_ERROR_N
K46	HDMI_DP0_TX3_P	SNN	DP1_D3_HDMI_CK_P	HDMI_DP1_TXD3_P
K47	HDMI_DP0_TX3_N	SNN	DP1_D3_HDMI_CK_N	HDMI_DP1_TXD3_N
K49	GPIO25	GPIO25_GP85_XFI0_MDIO	GPIO25/XFI0_MDIO	GPIO25_GP64_XFI0_MDIO
K50	DP2_HPD	DP_AUX_CH0_HPD_N	HPD0	DP_HPD0_GP253
K51	DP1_HPD	DP1_HPD_GP77_XFI3_MDIO	GPIO69/XFI3_MDIO	GPIO69_GP66_XFI3_MDIO
K52	DP0_HPD	DP2_HPD_GP80_XFI3_MDC	GPIO70/XFI3_MDC	GPIO70_GP67_XFI3_MDC
K56	GPIO19	GPIO19_GP89_XFI1_MDC	GPIO19/XFI1_MDC	GPIO19_GP69_XFI1_MDC
K6	RGMII_RD1	RGMII_RD1_GP154_RGMII0_RD1	GPIO60	GP192
K7	RGMII_TX_CTL	RGMII_TX_CTL_GP152_RGMII0_TX_CTL	FSI_GPIO27	FSI_GP238
K9	PEX_L3_RST_N	UPHY2_GP194_PCIE10_RST_N	FSI_GPIO22	FSI_GP218_CAN3_EN
L18	PEX_C6_RST_N	NC_01_UPHY1_GP213_PCIE6_RST_N	PEX_C5_RST_N	PCIE5_RST_N_GP63
L19	PEX_C6_CLKREQ_N	NC_02_UPHY1_GP212_PCIE6_CLKREQ_N	PEX_C5_CLKREQ_N	PCIE5_CLKREQ_N_GP62
L48	UART4_RX	UART4_RX_GP119	I2S7_DIN	I2S7_DIN_GP170
L49	UART4_CTS	UART4_CTS_N_GP121	I2S7_LRCK	I2S7_LRCK_GP179_PWM10

Module Pin #	Jetson AGX Orin Pin Name	Orin SoC Signal Name	Jetson T5000 Pin Name	Thor SoC Signal Name
L50	GPIO35	GPIO35_GP115	I2S7_SCLK	I2S7_SCLK_GP176
L6	GPIO02	MCLK05_GP66	UART4_CTS	UART4_CTS_GP183
L9	GPIO28	GPIO28_GP116	I2S7_DOUT	I2S7_DOUT_GP178

Notice

This document is provided for information purposes only and shall not be regarded as a warranty of a certain functionality, condition, or quality of a product. NVIDIA Corporation (“NVIDIA”) makes no representations or warranties, expressed or implied, as to the accuracy or completeness of the information contained in this document and assumes no responsibility for any errors contained herein. NVIDIA shall have no liability for the consequences or use of such information or for any infringement of patents or other rights of third parties that may result from its use. This document is not a commitment to develop, release, or deliver any Material (defined below), code, or functionality.

NVIDIA reserves the right to make corrections, modifications, enhancements, improvements, and any other changes to this document, at any time without notice.

Customer should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

NVIDIA products are sold subject to the NVIDIA standard terms and conditions of sale supplied at the time of order acknowledgement, unless otherwise agreed in an individual sales agreement signed by authorized representatives of NVIDIA and customer (“Terms of Sale”). NVIDIA hereby expressly objects to applying any customer general terms and conditions with regards to the purchase of the NVIDIA product referenced in this document. No contractual obligations are formed either directly or indirectly by this document.

Unless specifically agreed to in writing by NVIDIA, NVIDIA products are not designed, authorized, or warranted to be suitable for use in medical, military, aircraft, space, or life support equipment, nor in applications where failure or malfunction of the NVIDIA product can reasonably be expected to result in personal injury, death, or property or environmental damage. NVIDIA accepts no liability for inclusion and/or use of NVIDIA products in such equipment or applications and therefore such inclusion and/or use is at customer’s own risk.

NVIDIA makes no representation or warranty that products based on this document will be suitable for any specified use. Testing of all parameters of each product is not necessarily performed by NVIDIA. It is customer’s sole responsibility to evaluate and determine the applicability of any information contained in this document, ensure the product is suitable and fit for the application planned by customer, and perform the necessary testing for the application in order to avoid a default of the application or the product. Weaknesses in customer’s product designs may affect the quality and reliability of the NVIDIA product and may result in additional or different conditions and/or requirements beyond those contained in this document. NVIDIA accepts no liability related to any default, damage, costs, or problem which may be based on or attributable to: (i) the use of the NVIDIA product in any manner that is contrary to this document or (ii) customer product designs.

No license, either expressed or implied, is granted under any NVIDIA patent right, copyright, or other NVIDIA intellectual property right under this document. Information published by NVIDIA regarding third-party products or services does not constitute a license from NVIDIA to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property rights of the third party, or a license from NVIDIA under the patents or other intellectual property rights of NVIDIA.

Reproduction of information in this document is permissible only if approved in advance by NVIDIA in writing, reproduced without alteration and in full compliance with all applicable export laws and regulations, and accompanied by all associated conditions, limitations, and notices.

THIS DOCUMENT AND ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, “MATERIALS”) ARE BEING PROVIDED “AS IS.” NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY, OR OTHERWISE WITH RESPECT TO THE MATERIALS, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES OF NONINFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE. TO THE EXTENT NOT PROHIBITED BY LAW, IN NO EVENT WILL NVIDIA BE LIABLE FOR ANY DAMAGES, INCLUDING WITHOUT LIMITATION ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES, HOWEVER CAUSED AND REGARDLESS OF THE THEORY OF LIABILITY, ARISING OUT OF ANY USE OF THIS DOCUMENT, EVEN IF NVIDIA HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. Notwithstanding any damages that customer might incur for any reason whatsoever, NVIDIA’s aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms of Sale for the product.

Trademarks

NVIDIA, the NVIDIA logo, CUDA, Jetson, Jetson AGX, NVIDIA AGX, NVIDIA Orin, NVIDIA Volta, and Xavier are trademarks and/or registered trademarks of NVIDIA Corporation in the U.S. and other countries. Other company and product names may be trademarks of the respective companies with which they are associated.

VESA DisplayPort

DisplayPort and DisplayPort Compliance Logo, DisplayPort Compliance Logo for Dual-mode Sources, and DisplayPort Compliance Logo for Active Cables are trademarks owned by the Video Electronics Standards Association in the United States and other countries.

HDMI

HDMI, the HDMI logo, and High-Definition Multimedia Interface are trademarks or registered trademarks of HDMI Licensing LLC.

Arm

Arm, AMBA and Arm Powered are registered trademarks of Arm Limited. Cortex, MPCore and Mali are trademarks of Arm Limited. All other brands or product names are the property of their respective holders. ”Arm” is used to represent Arm Holdings plc; its operating company Arm Limited; and the regional subsidiaries Arm Inc.; Arm KK; Arm Korea Limited.; Arm Taiwan Limited; Arm France SAS; Arm Consulting (Shanghai) Co. Ltd.; Arm Germany GmbH; Arm Embedded Technologies Pvt. Ltd.; Arm Norway, AS and Arm Sweden AB.

Copyright

NVIDIA Corporation | 2788 San Tomas Expressway, Santa Clara, CA 95051
http://www.nvidia.com