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Comparing Power Supply Technologies in AI Data Centers and Telecom

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Why SiC is the Right Fit

With the onset of 5G Networks, we can expect a massive build out worldwide, requiring many high-quality telecom rectifiers to provide the needed power. To meet the need for improved efficiency, lower operating and lower BOM costs, there is renewed interest in WBG (Wide Bandgap) solutions. The same can be said for the efforts to push Server power supplies to ever increasing levels of efficiency with minimal heat loss. Hyperscale data centers that power the digital economy, big data, IoT and artificial intelligence (AI) now operate with >30 kW server racks, and highly sophisticated cooling management systems.

5G networks with larger antenna arrays (up to 64 Transmit / 64 Receive), facilitating 100−1000X higher data rates, and serving the trillions of devices forming the Internet of Things, would appear to need a great deal more power. Many technological improvements have been made to cut the power required for each base station, but it is clear that a much greater number of base stations are necessary. To serve the sophisticated methods of power management, power supplies for these base stations must meet ever more stringent efficiency requirements from standby to full load conditions.

New offerings of SiC FETs make it possible to hit previously unachievable efficiency targets, and we examine the main topologies and device capabilities in this article. We discuss what we might see in this space where Si Superjunction MOSFET, SiC Cascode JFETs (CJFET) and GaN FETs all compete.

Some Basics

What these power supplies all have in common is a power-factor-correction PFC section, that rectifies the AC to DC at near unity power factor with an output voltage of 400 V, followed by a DC−DC converter which converts this 400 V to 48 V or 12 V for use within the system. Further point-of-load converters are then used to power the CPUs and Memory banks.

If one examines the usage profile of data center server power supplies, it becomes clear that a large portion of their operating life is spent at light to medium load. Therefore, the PFC and DC−DC sections must perform at high efficiency at all load conditions, while meeting the thermal constraints of peak load operation. This is captured by the well-known 80plus standard used for computing power supplies, shown in Figure 1. Servers must meet the Titanium standard, which maintains high efficiency even at 10% load. Figure 2 shows a typical specification taken

from the Open Compute Project, which features a Titanium+ requirement for a 3.3 kW class power supply.

80 Plus test type[4]	115 V internal non-redundant				230 V internal redundant				230 V EU internal non-redundant			
Percentage of rated load	10%	20%	50%	100%	10%	20%	50%	100%	10%	20%	50%	100%
80 Plus		80%	80%	80%						82%	85%	82%
80 Plus Bronze		82%	85%	82%		81%	85%	81%		85%	88%	85%
80 Plus Silver		85%	88%	85%		85%	89%	85%		87%	90%	87%
80 Plus Gold		87%	90%	87%		88%	92%	88%		90%	92%	89%
80 Plus Platinum		90%	92%	89%		90%	94%	91%		92%	94%	90%
80 Plus Titanium	90%	92%	94%	90%	90%	94%	96%	91%	90%	94%	96%	94%

Figure 1. 80 Plus Standard for Testing Compute Power Supplies

Mechanical PSU Dimensions:	65mm x 165mm x 529.5mm (HxWxD)
AC Input Range (rated):	200V_{AC} to 277V_{AC}
Outputs:	12.6V_{DC}/265A (droop) 52.5V_{DC}/5A (0.2% output precision)
Efficiency:	Titanium+ Efficiency (230V_{AC}, fan powered internally, and connector losses included) 90% at 10% of the load 94% at 20% of the load 96% at 50% of the load 91% at 100% of the load
Holdup Time:	20ms @100% loading (worst case scenario)
Sharing:	±5% when load >20% ±1% when load at 100%
Redundancy:	Output ORing device for 12.6V_{DC} Hot Swappable
Communication:	RS485-Modbus PSU output SMBus between PSU and BBU CANbus between PSUs
Protection:	OCP, OTP, OVP, UVP, BBU Protection Signals
LEDs:	Green/Amber Bi-color LED for PWR OK / BKP Red LED for FAIL

Figure 2. Open Compute Project's Data Center Server Power Supply Standard (80 Plus Titanium)

Figure 3 shows a typical power supply architecture with its EMI filter, input bridge rectifier, a simple dual interleaved boost converter (PFC) with a 650 V / 750 V FET and SiC JBS (Junciton-Barrier-Schottky) diode as well as a full-bridge LLC stage for the DC−DC converter. Typical switching frequencies of 65−150 kHz are used for the PFC stage. Here, the need for power density is traded off against higher efficiency at lower frequencies, since the inductor can be made much smaller, switching at 150 kHz instead of 30 kHz. This leads to the use of Silicon superjunction MOSFETs with SiC JBS diodes to maintain high efficiency while hard switching at 65−150 kHz. Highly advanced Si Superjunction MOSFETs can switch fast, while the SiC Schottky diode helps minimize the Eon losses in the MOSFET.

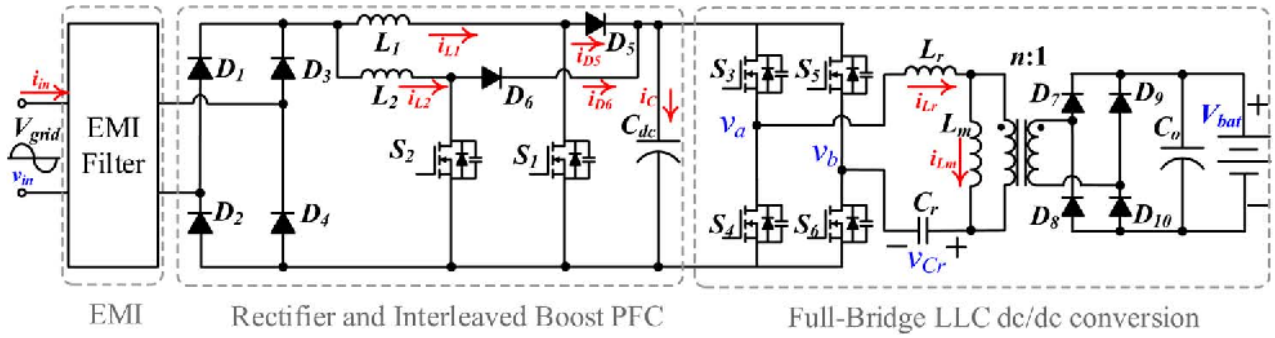

Figure 3. Typical Data Center Power Supply Architecture

In the LLC part of the circuit, 650 V MOSFETs are also commonly used. The circuit maintains ZVS (zero voltage switched) operation, as well as reduced turn-off currents, so losses are much lower, and the circuit can be operated at 100−500 kHz, allowing the transformer to be made smaller. On the secondary side, very low on-resistance 80−150 V Silicon MOSFETs are used to rectify the high frequency secondary AC voltage to provide the regulated output DC voltage. The 650 V FETs used are selected so that in the event ZVS is lost under some operating conditions, the body diode recovery is not destructive.

Semiconductor Devices

Focusing on the transistors, on the high voltage side of the PFC and DC−DC units, 650 V / 750 V class devices are commonly used for 48 V and 12 V architectures

Table 1 shows a comparison of some industry equivalent products in the commonly used TO247 package. The Silicon Superjunction (Si SJ) device and the **onsemi** SiC CJFET can be driven by 0 to 10 V drive. The SiC MOS options require different voltages (for e.g. −4 V to 18 V). The SiC devices all offer lower gate charge and much reduced diode recovery charge Qrr. The body diode conduction losses of the Silicon Superjunction and SiC CJFET are lower than those of SiC MOSFETs.

Table 1. COMPARISON OF SIMILAR DEVICES IN A TO247 PACKAGE

Parameter	Units	SCT3017AL	UF4C075016K3S	SCTW100N65G2AG	IPW65R019C7
Technology		SiC MOS	SiC CJFET	SiC MOS	Si SJ
Vdsmax	V	650	750	650	650
Vgsmax	V	−4 to 22	−20 to 20	−10 to 22	−20 to 20
Id 100C	A	49	50?	70	62
RTHJC max	°C/W	0.35	0.34	0.42	0.28
Rds	mΩ	17	16	20	17
Rds 125	mΩ	22.4	22	26	34
Rds 175	mΩ	27	36	32	45
RG	Ω	4	4.5	2	0.85
Ciss 400 V	pF	2884	1500	3315	10000

Table 1. COMPARISON OF SIMILAR DEVICES IN A TO247 PACKAGE (continued)

Parameter	Units	SCT3017AL	UF4C075016K3S	SCTW100N65G2AG	IPW65R019C7
Coss 400 V	pF	148	?	267	170
Crss 400 V	pF	65	?	46	27
Coss(er)	pF	397	?	?	338
Coss(tr)	pF	?	?	?	3320
Eoss(400V)	μJ	34	?	?	13.2
Qg	nC	172 (18 V)	43 (12 V)	162 (18 V)	210 (10 V)
Vsd	V	3.2	1.3	3.5	0.9
Qrr (400V, 150C)	V	?	?	370? Need hot	20000

Table 2 shows a comparison of similar devices in DFN8x8 footprint. The Silicon SJ, SiC CJFET and GaN device can all be driven by standard Silicon gate drives. **onsemi** SiC CJFETs offer very low on-resistances. Comparing devices with different 150C Rds(on) is best done using the figures of merit in the bottom three rows. The WBG solutions offer better figures of merit, especially for Rds*Coss(tr) and Rds*Qrr.

Table 2. COMPARISON OF SIMILAR DEVICES IN DFN8x8 PACKAGE

Parameter	Units	IPL65R070C7	STL57N65M5	TP65H070LDG	UF3SC065030-D8S	UF3SC065040-D8S
Technology		Si−SJ	Si−SJ	GaN	SiC CJFET	SiC CJFET
Id	A	20	22	16	20	20
Vdsmax	V	650	650	650	650	650
RthJC	°C/W	0.74	0.66	1.3	0.47	0.64
Eas	mJ	171	960	NA	120	76
Rds(25C)	mΩ	62	61	72	27	42
Rds(150C)	mΩ	140	134	150	43	78
Rg	Ω	0.85	1.4		4.5	4.5
Ciss	pF	3020	4200	600	1500	1500
Coss(er)	pF	100	97	131	230	146
Coss(tr)	pF	1110	344	217	520	325
Qrr	nC	10000	9500	89	280	137
Rds*Coss(er)	mΩ.pF	14900	12998	19650	9890	11388
Rds*Coss(tr)	mΩ.pF	165390	46096	32550	22360	25350
Rds*Qrr	mΩ.nC	1490000	1273000	13350	12040	10686

Figure 4 shows the cross-sectional architecture of commonly used configurations of SiC, GaN and Si Superjunction FETs. GaN HEMTs are lateral devices, while the other device types are vertical current flow devices. Vertical current flow allows higher voltage devices to be implemented more compactly, since the source and drain terminals are on opposite sides of the

wafer, and not both on the top surface. In the GaN HEMT, conduction is confined to the 2DEG channel, while the SiC devices use a short surface channel, but mostly the bulk for carrying current. The SiC JFET has a bulk channel, which along with its vertical nature, results in the lowest drain-source on-resistance per unit area (RdsA) and allows the lowest chip size. It is then cascoded with a low voltage Si MOSFET (which adds 10% to the resistance), to form the SiC CJFET.

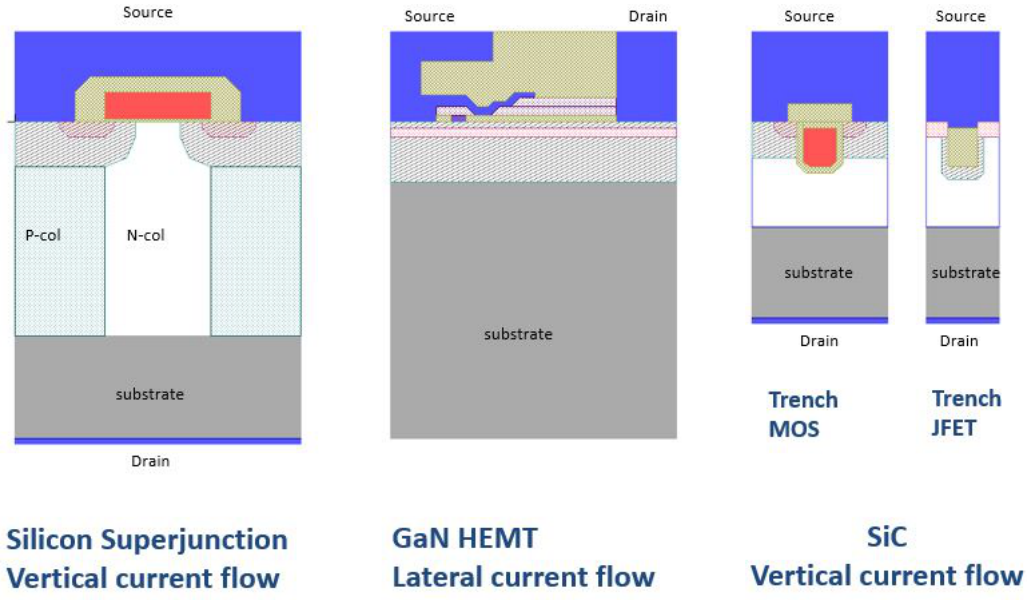

Figure 4. Architecture of Si Superjunction, GaN HEMT, and SiC CJFET Devices

As devices improve, the ultimate switching speed limit is set by the load current charging the device Coss. A low value of Coss(tr) for a given on-resistance gives the fastest slew rate, as well as the shortest delay time to reach 400 V. It is clear that the SiC CJFET is excellent in this regard, and a good choice for high frequency power conversion.

In terms of Qrr, the WBG options all offer much improved performance compared to Superjunction Silicon devices. Therefore, these devices are selected whenever the circuit actually uses hard-switched turn-on as in a continuous current mode (CCM) totem pole PFC. If these circuits use body diode conduction in the freewheeling state, the on-state drop of the body diode leads to conduction losses. Therefore, synchronous conduction is generally used, turning on the FET channel to reduce these losses. There is usually a delay between detecting the current reversal and turning on the FET channel, and this time becomes a significant fraction of the switching period at high frequencies. For example, a 100 ns dead time where the diode conducts matters little if the switching frequency is 100 kHz (10 μs period). But it becomes 10% during a 1 MHz (100 ns period) switching cycle. Therefore, low body diode VFSD together with low Qrr is a useful characteristic and SiC CJFETs excel in this regard.

Moreover, the most efficient circuit options avoid hard switched turn-on, because while turn-off losses can be made negligible with WBG devices, this is not the case for turn-on losses. With

the low gate charge of available CJFETs, and low on-resistance and turn-off losses, frequencies in soft-switched circuits can be pushed up by 5−10X.

In terms of device robustness, SiC CJFETs all offer excellent avalanche capability, which enhances the system reliability of the converter. Despite their smaller chip sizes, they can often exceed the capability of Superjunction FETs especially at high current levels. GaN devices cannot handle avalanche, and are therefore designed with high breakdown voltages to avoid this operating zone.

Gate Drive Considerations

A key simplification using SiC CJFETs is that in the low voltage MOSFET has a 5 V Vth, and a Vgsmax rating of ±20 V. It can be driven like a Silicon Superjunction MOSFET from 0 to 10 V, or 0 to 12 V. Figure 5 shows a comparison of the recommended gate drive voltage for various technologies and the gate absolute maximum ratings. SiC MOSFETs usually employ negative and positive gate drive, and need a 20 to 25 V total swing in gate voltage. The gate voltages are often quite close to the absolute maximum ratings, which requires careful attention to gate spikes. The large gate swing can add up to considerable gate charge loss at higher frequencies. Furthermore, to manage the Vth hysteresis issues, the manufacturers' recommendations have to be carefully followed for gate drive voltage levels. SiC CJFETs are flexible in this regard, and can also be driven at gate voltages compatible with silicon power switches.

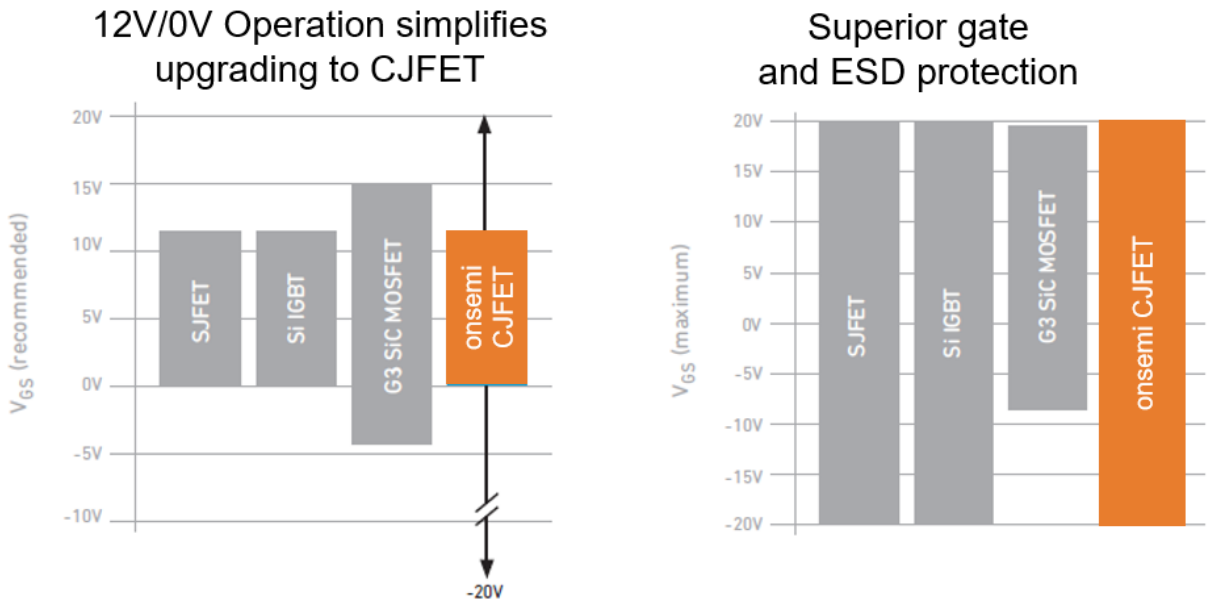

Figure 5. Comparisons between Power Device Technologies' Recommended Gate Drive Voltages and Absolute Maximum Voltage Ratings

GaN enhancement mode devices generally have a low Vth, and are driven in a narrow gate voltage range, which is often quite close to the absolute maximum VGS limits. This requires specialized drivers and careful layout to avoid damage to the switches. The cascode option can

circumvent some of these difficulties. The lower gate voltage swing is beneficial in reducing gate losses at higher frequencies.

In all instances, as the devices are used at higher speeds, holding the devices off at high dV/dt becomes increasingly challenging. As does the management of gate voltage spikes from the power loop and gate drive loop inductances. Introduction of packages with source kelvin pins has helped, but we look at other options in a later section of this article.

Circuit Topologies – PFC Stage

Figure 6 shows a Totem-Pole PFC (TPPFC) circuit, and the measured efficiency at 100 kHz on an **onsemi** demonstration board at 1.5 kW. This circuit eliminates all the diode conduction losses, both from the input diode bridge and the SiC PFC diode. In this case, the converter operates in CCM mode, and the devices are hard switched. It is clear that the Totem Pole PFC has much reduced losses, making it possible to achieve Titanium power efficiency targets.

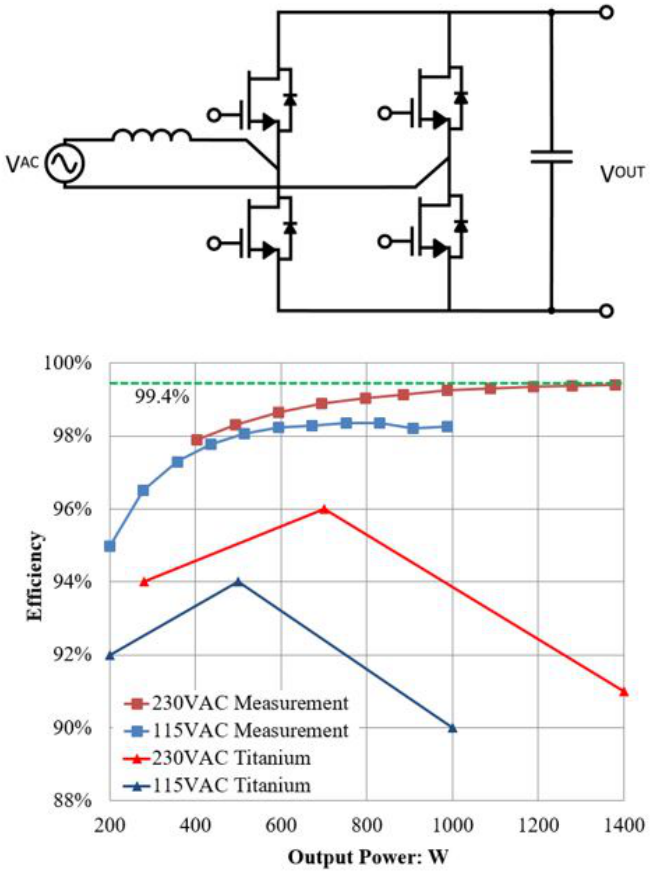

Figure 6. Efficiency of a Totem-Pole PFC Circuit

A very high-power density can be achieved using SiC CJFETs without sacrificing efficiency, although the complexity in control and magnetics design is greater. An alternate method that does not require detection of current crossings uses additional auxiliary switches to achieve zero voltage transitions at turn-on. Similar or better results can be obtained using resonant

techniques such as the auxiliary resonant commutated pole (ARCP) that eliminate both turn-on and turn-off losses. However, the cost-performance benefits of the more advanced techniques seem to be favorable at power levels well above 5 kW.

Circuit Topologies: DC−DC Stage

Since the output voltage is fixed, the full-bridge LLC converter offers excellent power density and efficiency, and is presently the industry workhorse at higher power levels. As power levels get lower, a half-bridge LLC implementation may be used. Frequencies in the 100−500 kHz range are commonly used, and the key effort in loss reduction actually shifts to the transformer secondary and low voltage secondary MOSFETs, given the high current levels at the 12 V output.

For the high voltage FETs, the V_{DS} transition from its off-state to diode conduction requires charging the output capacitance, and in order to do it quickly, a low $C_{OSS(TR)}$ is necessary. However, users must then minimize the dead time before gating on the FET for synchronous conduction to reduce the loss from body diode conduction. A low Rds in the on-state minimizes conduction losses, and the low E_{OFF} of most Superjunction and WBG switches helps keep losses at a minimum.

If under light load conditions, ZVS is lost, diode hard recovery can occur. With WBG switches such as the SiC CJFET, this poses no risk, but can damage Silicon Superjunction MOSFETs. To minimize this possibility, fast recovery versions of Superjunction FETs are often used, but no such precaution is needed with SiC CJFETs.

Outlook for the Near Future

While improvements in Si Superjunction FETs continues, the levels of improvements possible for SiC and GaN devices in the next few years far outstrips what can be achieved with Silicon. In addition to improvements in RdsA (improvements of 30−50% every 2−3 years), many improvements in package technology are to be expected. The main challenges being addressed are low inductance, and more efficient heat removal in small surface mount options.

One likely path is the migration to half-bridge elements designed either for direct surface mount use, or as an embedded element in the PCB. This simplifies PCB layout and allows the implementation of lower inductance power and gate loops.

Another emerging path as the integration of the driver with the power device, either as a single driver + switch, or as a half-bridge element (Watch this webinar for more on pairing gate drivers with EliteSiC FETs). Since most SiC and GaN devices need unique driving voltage levels and circuits, this complexity can be absorbed into the co-packaged or integrated product, making this easier for users. In addition, each device can then be better utilized to its full potential. This will no doubt lead to greater savings in system cost and power losses, and drive WBG adoption.

Along these lines, the SIP half-bridge with an integrated half-bridge gate drive using 35 mΩ, 1200 V SiC CJFETs was described in previous articles in this series. Surface mount options are emerging from various suppliers, and the trend is likely to accelerate.

The cost of 650 V wide bandgap switches are now dropping rapidly. **onsemi**'s 650 V / 750 V CJFETs are expected to reach price parity within the next two years. Along with the ease of use, this is expected to rapidly accelerate the deployment of WBG devices in data center server and telecom power supply applications.

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document version release.	6/12/2025

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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