DOC200103
CMOS/SINE Hybrid TCXO
Hi-Rel Standard

General

	Rev	Cage Code
Vectron® Oscillators	**L**	**00136**

This specification defines the design, assembly, and functional evaluation of high reliability, Space qualified, hybrid TCXOs produced by Microchip. Devices delivered to this specification represent the standardized Parts, Materials and Processes (PMP) Program developed, implemented, and certified for advanced applications and extended environments.

For more information see www.microchip.com/en-us/products/clock-and-timing/components/oscillators/space.

Applications Overview

The designs represented by these products were primarily developed for the MIL-Aerospace community. The lesser Design Pedigrees and Screening Options imbedded within DOC200103 bridge the gap between Space and COTS hardware by providing custom hardware with measures of mechanical, assembly and reliability assurance needed for Military, Ruggedized COTS, or Commercial environments.

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1. Applicable Documents

1.1. Specifications and Standards

The following specifications and standards form a part of this document to the extent specified herein. The issue currently in effect on the date of quotation will be the product baseline, unless otherwise specified. In the event of conflict between the texts of any references cited herein, the text of this document shall take precedence.

Table 1-1. Military

Document	Title
MIL-PRF-55310	Oscillators, Crystal Controlled, General Specification For
MIL-PRF-38534	Hybrid Microcircuits, General Specification For

Table 1-2. Standards

Document	Title
MIL-STD-202	Test Method Standard, Electronic and Electrical Component Parts
MIL-STD-883	Test Methods and Procedures for Microelectronics

Table 1-3. Other

Document	Title
QSP-90100	Quality Systems Manual, Vectron
DOC011627	Identification Common Documents, Materials and Processes, Hi-Rel XO
DOC203982	DPA Specification
QSP-91502	Procedure for Electrostatic Discharge Precautions
DOC208191	Enhanced Element Evaluation for Space Level Hybrid Oscillators
DOC220429	Packaging Standards, Hi-Rel Series

2. General Requirements

2.1. Classification

All devices delivered to this specification are of hybrid technology conforming to Type 3, Class 2 of MIL-PRF-55310. Devices carry a Class 1C ESDS classification per MIL-PRF-38534 and are marked with a single equilateral triangle at pin 1 per MIL-PRF-55310.

2.2. Item Identification

External packaging choices are either metal flatpacks or DDIP with either Sinewave or CMOS logic output. Unique Model Number Series are utilized to identify device package configurations and output waveform as listed in Table 6-1.

2.3. Absolute Maximum Ratings

Table 2-1. Absolute Maximum Ratings

Parameter	Value
Supply Voltage Range (V_{CC})	–0.5Vdc to +5.0Vdc (Vcc = +3.3V) –0.5Vdc to +7.0Vdc (Vcc = +5V) –0.5Vdc to +16.5Vdc (Vcc = +12V) –0.5Vdc to +18Vdc (Vcc = +15V)
Storage Temperature Range (TSTG)	-65 °C to +125 °C
Junction Temperature (TJ)	+150 °C
Lead Temperature (soldering, 10 seconds)	+300 °C

2.4. Design, Parts, Materials and Processes, Assembly, Inspection, and Test

2.4.1. Design

The ruggedized designs implemented for these devices are proven in military and space applications under extreme environments. All designs utilize a 4-point crystal mount. For radiation characteristics, see 3.1.5. Radiation for details on the component requirements for the various oscillator design pedigrees.

2.4.1.1. Design and Configuration Stability

Barring changes to improve performance by reselecting passive chip component values to offset component tolerances, there will not be fundamental changes to the design or assembly or parts, materials and processes after first product delivery of that item without notification.

2.4.1.2. Environmental Integrity

Designs have passed the environmental qualification levels of MIL-PRF-55310. These designs have also passed extended dynamic levels of at least:

a. Sine Vibration: MIL-STD-202, Method 204, Condition G (30g pk.)

b. Random Vibration: MIL-STD-202, Method 214, Condition II-J (43.92g rms, three-minute duration in each of three mutually perpendicular directions) except model numbers 2105, 2115, 2205 and 2215 which are rated at Condition II-F (24.06g rms)

c. Mechanical Shock: MIL-STD-202, Method 213, Condition F (1500g, 0.5ms)

2.4.2. Prohibited Parts, Materials and Processes

The items listed are prohibited for use in high reliability devices produced to this specification.

a. Gold metallization of package elements without a barrier metal.

b. Zinc chromate as a finish.

c. Cadmium, zinc, or pure tin external or internal to the device.

d. Plastic encapsulated semiconductor devices.

e. Ultrasonically cleaned electronic parts.

f. Heterojunction Bipolar Transistor (HBT) technology.

2.4.3. Assembly

Manufacturing utilizes standardized procedures, processes, and verification methods to produce MIL-PRF-55310 Class S/MIL-PRF-38534 Class K equivalent devices. MIL-PRF-38534 Group B Option 1 in-line inspection is included on design pedigrees E and R per paragraph 7.1 to further verify lot pedigree. Devices are handled in accordance with the Microchip document QSP-91502 (Procedure for Electrostatic Discharge Precautions). Element replacement will be as specified in MIL-PRF-38534, Rev L.

2.4.4. Inspection

The inspection requirements of MIL-PRF-55310 apply to all devices delivered to this document. Inspection conditions and standards are documented in accordance with the Quality Assurance, ISO-9001 and AS9100 derived, System of QSP-90100.

2.4.5. Test

The Screening test matrix of Table 6-8 is tailored for selectable-combination testing to eliminate costs associated with the development/maintenance of device-specific documentation packages while maintaining performance integrity.

2.4.6. Marking

Device marking shall be in accordance with the requirements of MIL-PRF-55310. In addition, when devices are identified with laser marking, the Resistance to Solvents test specified in MIL-PRF-55310 Group C, MIL-PRF-55310 Qualification or MIL-PRF-38534 Group B Inspection will not be performed.

2.4.7. Ruggedized COTS Design Implementation

Design Pedigree “D” devices (see 4.2. Optional Design, Test, and Data Parameters) use the same robust designs as the other device pedigrees. They do not include the provisions of traceability or the Class-qualified componentry noted in 2.4.3. Assembly and 3.1. Components.

3. Detail Requirements

3.1. Components

3.1.1. Crystals

Cultured quartz crystal resonators are used to provide the selected frequency for the devices. Premium Q swept quartz is standard for all Design Pedigrees E, R and B because of its superior radiation tolerance. The manufacturer has a documented crystal evaluation program in accordance with MIL-PRF-55310.

3.1.2. Passive Components

3.1.2.1. Design Pedigree E

For Design Pedigree E, where available, resistors shall be Established Reliability, Failure Rate R (as a minimum) and capacitors shall be Failure Rate S. Where resistors and capacitors are not available as ER parts, and for all other passive components, the parts shall be from homogeneous manufacturing lots that have successfully completed the Enhanced Element Evaluation of DOC208191 which meets the requirements of MIL-PRF-38534 Revision L for Class K.

3.1.2.2. Design Pedigree R

For Design Pedigree R, where available, resistors shall be Established Reliability, Failure Rate R (as a minimum) and capacitors shall be Failure Rate S. Where resistors and capacitors are not available as ER parts, and for all other passive components, the parts shall be from homogeneous manufacturing lots that have successfully completed the Class K Element Evaluation of MIL-PRF-38534 Revision K for Class K.

3.1.2.3. Design Pedigrees B and C

For Design Pedigrees B and C, all passive elements shall comply with the Element Evaluation requirements of MIL-PRF-55310 Class B as a minimum.

3.1.2.4. Design Pedigree D

For Design Pedigree D, the passive elements will be COTS level or higher.

3.1.3. Microcircuits (Voltage Regulators, CMOS Devices, etc.)

3.1.3.1. Design Pedigree E

For Design Pedigree E, the microcircuits shall be from homogeneous wafer lots that meet the Enhanced Element Evaluation requirements in DOC208191 and meet the requirements of MIL-PRF-38534 Revision L for Class K.

3.1.3.2. Design Pedigree R

For Design Pedigree R, microcircuits shall be from homogeneous wafer lots that have successfully completed the MIL-PRF-38534, Revision K Lot Acceptance Tests for Class K.

3.1.3.3. Design Pedigrees B and C

For Design Pedigrees B and C, microcircuits are procured from wafer lots that have successfully completed the MIL-PRF-55310 Lot Acceptance Tests for Class B as a minimum.

3.1.3.4. Design Pedigree D

For Design Pedigree D, microcircuits can be COTS level or higher.

3.1.4. Semiconductors (Transistors, Diodes, etc.)

3.1.4.1. Design Pedigree E

For Design Pedigree E, the semiconductors shall be from homogeneous wafer lots that meet the Enhanced Element Evaluation requirements in DOC208191 and meet the requirements of MIL-PRF-38534 Revision L for Class K.

3.1.4.2. Design Pedigree R

For Design Pedigree R, semiconductors shall be from homogeneous wafer lots that have successfully completed the MIL-PRF-38534, Revision K Lot Acceptance Tests for Class K devices as a minimum.

3.1.4.3. Design Pedigrees B and C

For Design Pedigree B and C, semiconductors are procured from wafer lots that have successfully completed the MIL-PRF-55310 Lot Acceptance Tests for Class B devices as a minimum.

3.1.4.4. Design Pedigree D

For Design Pedigree D, semiconductors can be COTS level or higher.

3.1.5. Radiation

Microcircuits and semiconductors for Design Pedigrees E and R are from wafer lots that are certified to 100 krad (Si) total dose minimum. Sinewave devices are assembled with all bipolar semiconductors and bipolar constructed microcircuits. ACMOS devices are assembled with all bipolar semiconductors and bipolar constructed microcircuits, except for the ACMOS chip used to provide the CMOS output. In addition, the bipolar transistors are considered insensitive to Single Event Effects. The ACMOS die is from a certified wafer lot that is radiation tested to a minimum of 100 krad. NSC, the 54ACT designer, has characterized the SET LET up to 40 MeV and SEL LET up to 120 MeV for the FACT™ family (AN-932). Microchip conducted additional SEE testing in 2008 to verify this performance since our lot wafer testing does not include these parameters and determinations.

3.1.6. Packages

Packages are procured that meet the construction, lead materials and finishes as specified in MIL-PRF-55310. All leads are Kovar with gold plating over a nickel underplate. Package lots are evaluated in accordance with the requirements of MIL-PRF-38534. Microchip will not perform Salt Spray testing as part of MIL-PRF-55310 Group C/Qualification. In accordance with MIL-PRF-55310, package evaluation results for salt atmosphere will be substituted for Salt Spray testing during MIL-PRF-55310 Group C/Qualification.

3.1.6.1. Traceability and Homogeneity

All design pedigrees except option D have active device lots that are homogeneous and traceable to the manufacturer's individual wafer. Swept Quartz crystals are traceable to the quartz bar and the processing details of the autoclave lot; however, multiple lots of un-plated crystals, bases, and covers may be combined into a single sealed crystal manufacturing lot. For design pedigrees E and R only, passive elements, crystals, and materials are traceable to their manufacturing lots. Manufacturing lot and date code information shall be recorded, by TCXO serial number, of every component and all materials used in the manufacture of those TCXOs. A production lot, as defined by Microchip, is all oscillators that have been kitted and built as a single group. The maximum deliverable quantity with a single lot date code is 100 units. Order quantities that exceed 100 units will be delivered in multiple lot date codes with deliveries separated by 4 weeks. If applicable, each production lot will be kitted with homogeneous material which is then allocated across multiple lot date code builds to satisfy the deliverable order quantity. When ordered, Group C Inspection, lot qualifications, and/or DPA will be performed on the first build lot within the production lot unless otherwise stated on the purchase order.

3.2. Mechanical

3.2.1. Package Outline

Table 6-1 links each Hi-Rel Standard Model Number of this specification to a corresponding package style. Mechanical Outline information of each package style is found in the referenced figure.

3.2.2. Thermal Characteristics

Because these TCXOs are multichip hybrid designs, the actual θ_{jc} to any one given semiconductor die will vary, but the combined average for all active devices results in a θ_{jc} of approximately 40 °C/W. The typical die temperature rise at any one given semiconductor is 2 °C to 4 °C. With the oscillator operating at +125 °C, the average junction temperature is approximately +129 °C and under no circumstance will it ever exceed the maximum manufacturer's rated junction temperature.

3.2.3. Lead Forming

When the lead forming option is specified, the applicable leak test specified in screening will be performed after forming.

3.3. Electrical

3.3.1. Supply Voltages

CMOS devices are designed for 3.3 or 5 Vdc ±5% operation. Sinewave devices are designed for 3.3, 5, 12 or 15 Vdc ±5% operation.

3.3.2. Temperature Range

Operating range is IAW the chosen temperature stability code.

3.3.3. Frequency Tolerance

Temperature stability includes initial accuracy at +25 °C (with EFC), load ±10% and supply ±5%.

3.3.4. Frequency Set

All devices include an External Frequency Control (EFC) pin for the purpose of externally setting each TCXO to its nominal frequency. The EFC shall be accomplished by connecting a resistor or trimmer potentiometer from that Pin to GND. The EFC resistance adjustment range is 0Ω or GND to 20 kΩ max with nominal frequency typically occurring in the 3 kΩ to 13 kΩ range. Customers will be furnished with the applicable EFC resistor value that can be used to set each individual device within ±0.2 ppm of nominal frequency at time of shipment.

3.3.5. Frequency Aging

Aging limits, when tested in accordance with MIL-PRF-55310 Group B inspection, shall not exceed ±1 ppm for the first year and ±5 ppm for 15 years for oscillators that use crystals in the 10 MHz to 75 MHz range. For oscillators that use crystals greater than 75 MHz, the aging shall not exceed ±2 ppm for the first year and ±10 ppm for 15 years.

3.3.5.1. Frequency Aging Duration Option

For Screening Option F, the Aging test will be terminated after 15 days if the aging projection is less than the specified aging limit. This is a common method of expediting 30-day Aging without incurring risk to the hardware and used quite successfully for numerous customers. It is based on the 'least squares fit' determinations of MIL-PRF-55310 paragraph 4.8.35. Microchip's automated aging systems acquire data every four hours, compared to the minimum MIL-PRF-55310 requirement of once every 72 hours. This makes an extensive amount of data available to perform very accurate aging projections. The delivered data would include the Aging plots projected to 30 days. If the units would not perform within that limit then they would continue to the full 30-day term. For all other screening options, please advise by purchase order text if this is an acceptable option to exercise as it assists in Production Test planning.

3.3.6. Operating Characteristics

See Table 6-2 and Table 6-3. Waveform measurement points and logic limits are in accordance with MIL-PRF-55310. Start-up time is 10 ms typical and 30 ms maximum.

3.3.7. Outputs and Loads

Standard Sinewave (50 Ω) and CMOS (10 kΩ, 15 pF) test loads are in accordance with MIL-PRF-55310. Note that the sinewave outputs are AC coupled.

3.3.8. Phase Noise

Contact the factory for typical performance. If custom and/or guaranteed performance is required, Microchip can assign a custom part number.

4. Quality Assurance Provisions and Verification

4.1. Verification and Test

Device lots shall be tested prior to delivery in accordance with the applicable Screening Option letter as stated by the 16th character of the part number. Table 6-8 tests are conducted in the order shown and annotated on the appropriate process travelers and data sheets of the governing test procedure. For devices that require Screening Options that include MIL-PRF-55310 Group A Testing, the Post-Burn-In Electrical Test and the Group A Electrical Test are combined into one operation.

4.1.1. Screening Options

The Screening Options, by letter, are summarized as:

Table 4-1. Screening Options

Screening Option	Description
K	Modified MIL-PRF-38534 Class K Screening, Group A QCI and 30-day aging
F	MIL-PRF-55310, Rev F, Class S Screening, Groups A & B QCI
S	MIL-PRF-55310, Rev E, Class S Screening, Groups A & B QCI
C	Modified MIL-PRF-55310 Class B Screening, Groups A & B QCI
B	MIL-PRF-55310, Class B Screening, Groups A & B QCI
X	Engineering Model (EM)

4.2. Optional Design, Test, and Data Parameters

The following is a list of design, assembly, inspection, and test options that can be added by explicit purchase order request.

a. Design Pedigree (choose one as the 5th character in the part number):

Table 4-2. Design Pedigree

Design Pedigree	Description
E	Enhanced Element Evaluation (MIL-PRF-38534 Rev L for Class K components as specified in DOC208191), 100 krad die, Premium Q Swept Quartz
R	MIL-PRF-38534 Rev K element evaluation for Class K components,100 krad die, Swept Quartz
B	Class B components, Swept Quartz
C	Class B components, Non-Swept Quartz
D	COTS components, Non-Swept Quartz

b. Input Voltage as the 15th character

c. Not Used

d. Radiographic Inspection

e. Group C Inspection: MIL-PRF-55310, Rev E (requires 8 destruct specimens)

f. Group C Inspection: MIL-PRF-55310, Rev F (requires 8 destruct specimens, includes Random Vibration, MIL-STD-883, Method 1014 Leak Test and Life Test)

g. Group C Inspection: In accordance with MIL-PRF-38534, Table C-Xc, Condition PI (requires 8 destruct specimens – 5 pc. Life, 3 pc. RGA). Subgroup 1 fine leak test to be performed per MIL-STD-202, Method 112, Condition C.

h. Internal Water-Vapor Content (RGA) samples and test performance

i. MTBF Reliability Calculations

j. Worst Case Circuit Analysis (unless otherwise specified, MIL-HDBK-1547)

k. Derating and Thermal Analysis (unless otherwise specified, MIL-HDBK-1547 with T_j Max = +105 °C; Case Temperature = +85 °C)

l. Process Identification Documentation (PID)

m. Customer Source Inspection (pre-cap/final) [Note: Model numbers 2105, 2205, 2115 and 2215 require two pre-cap inspections.]

n. Destruct Physical Analysis (DPA): MIL-STD-1580 with exceptions as specified in Microchip DOC203982.

o. Qualification: In accordance with MIL-PRF-55310, Rev F, Table IV (requires 16 destruct specimens). Includes Group III, SG1 through SG6 only. ESD (SG7) not performed.

p. Qualification: In accordance with EEE-INST-002, Section C4, Table 3, Level 1 or 2 (requires 11 destruct specimens)

q. High Resolution Digital Pre-Cap Photographs (20 Megapixels minimum)

r. Hot solder dip of leads with Sn63/Pb37 solder prior to shipping.

s. As Designed Parts, Materials and Processes List

4.2.1. NASA EEE-INST-002

A combination of Design Pedigree R, Option F Screening, and Qualification per EEE-INST-002, Section C4, Table 3 meet the requirements of Level 1 and Level 2 device reliability.

4.3. Test Conditions

Unless otherwise stated herein, inspections are performed in accordance with those specified in MIL-PRF-55310. Process travelers identify the applicable methods, conditions and procedures to be used. Examples of electrical test procedures that correspond to MIL-PRF-55310 requirements are shown in Table 6-7.

4.4. Delta Limit Exception

When MIL-PRF-55310, Revision F was being reviewed for release by manufacturers and users, Microchip and other organizations recommended that burn-in delta limits not be applied to logic level measurements due to the inconsistency in attempting to measure small changes in logic levels which inherently have ringing in the signal. This is especially true in higher frequency oscillators measured in automated test systems that are affected by cable length that is not representative of the user's application and contact resistance in test fixtures that do not provide a consistent Vcc or Ground connection. The exact test setup conditions may vary slightly from pre-burn-in to post-burn-in and cause small artificial deltas in logic level measurements that are not indicative of an issue. Any significant changes in logic levels will be reflected in supply current deltas and/or logic levels that exceed the min/max limits. As a result, we take exception to MIL-PRF-55310, Revision F, Para. 4.4.5 and the delta limit for Output Low Level as specified in 4.4.5(c) shall not be applied to Burn-in PDA.

4.5. Deliverable Data

The manufacturer supplies the following data, as a minimum, with each lot of devices:

a. As applicable to the Screening Option chosen, completed assembly and screening lot travelers, screening data, including radiographic images, and rework history.

b. Electrical test variables data, identified by unique serial number.

c. Special items when required by purchase order such as Group C, DPA, and RGA data.

d. For Design Pedigrees E and R, traceability, component LAT, enclosure LAT, and wafer lot specific RLAT data for non-SMD active devices (if applicable).

e. Certificate of Conformance.

4.6. Discrepant Material

All MRB authority resides with the procuring activity.

4.7. Failure Analysis

Any failure during Qualification or Group C Inspection will be evaluated for root cause. The customer will be notified after occurrence and upon completion of the evaluation.

5. Preparation for Delivery

5.1. Packaging

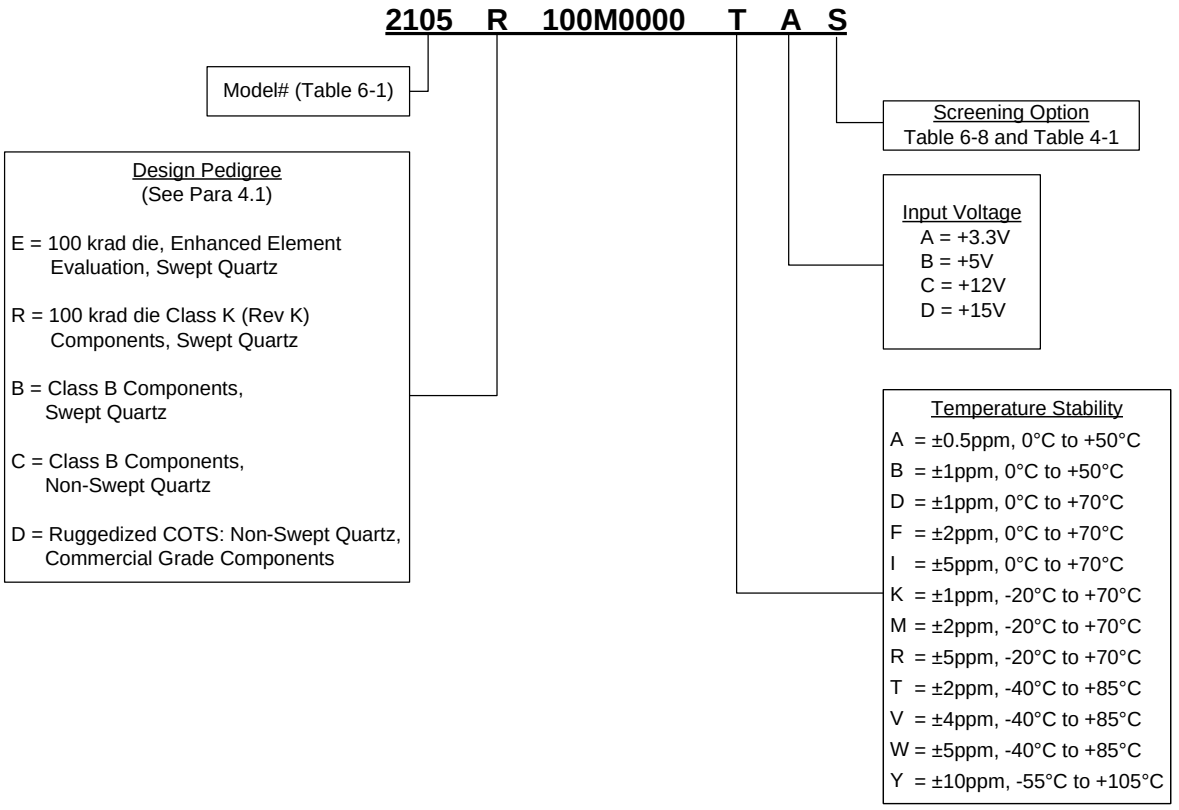
Devices will be packaged in a manner that prevents handling, ESD and transit damage during shipping. Devices will be packaged for transport in accordance with DOC220429. Please note that “one unit per package” is available for a fee; however, this service must be requested as part of the official RFQ.

6. Ordering Information

6.1. Ordering Part Number

The ordering part number is made up of an alphanumeric series of 16 characters. Design-affected product options, identified by the parenthetic letter on the Optional Parameters list (4.2. Optional Design, Test, and Data Parameters), are included within the device part number.

The Part Number breakdown is described as:



6.1.1. Model Number

The device model number is the four (4) digit number assigned to a corresponding package and output combination per Table 6-1.

6.1.2. Design Pedigree

Class S designs correspond to letters “E” and “R” and are described in 4.2. Optional Design, Test, and Data Parameters. Class B variants correspond to either letter “B” or “C” and are described in 4.2. Optional Design, Test, and Data Parameters. Ruggedized COTS, using commercial grade components, correspond to letter “D”.

6.1.3. Output Frequency

The nominal output frequency is expressed in the format as specified in MIL-PRF-55310 utilizing eight (8) characters.

6.1.4. Input Voltage

Voltage is the 15th character. Voltage availability is dependent on platform.

6.1.5. Screening Options

The 16th character is the Screening Option selected from Table 6-8.

6.2. Optional Design, Test and Data Parameters

Test and documentation requirements above that of the standard high reliability model shall be specified by separate purchase order line items (4.2. Optional Design, Test, and Data Parameters).

Table 6-1. Item Identification and Package Outline

Model #	Package	Output	Mechanical Outline and I/O Connections
2101	24 Pin DDIP	CMOS	Figure 6-1
2102	32 Lead Flatpack	CMOS	Figure 6-2
2103	24 Lead Flatpack	CMOS	Figure 6-3
2104	14 Lead Flatpack	CMOS	Figure 6-4
2105	14 Lead Flatpack	CMOS	Figure 6-5
2202[1]	32 Lead Flatpack	CMOS	Figure 6-6
2203[1]	24 Lead Flatpack	CMOS	Figure 6-7
2204[1]	14 Lead Flatpack	CMOS	Figure 6-8
2205[1]	14 Lead Flatpack	CMOS	Figure 6-9
2111	24 Pin DDIP	Sine	Figure 6-1
2112	32 Lead Flatpack	Sine	Figure 6-2
2113	24 Lead Flatpack	Sine	Figure 6-3
2114	14 Lead Flatpack	Sine	Figure 6-4
2115	14 Lead Flatpack	Sine	Figure 6-5
2212[1]	32 Lead Flatpack	Sine	Figure 6-6
2213[1]	24 Lead Flatpack	Sine	Figure 6-7
2214[1]	14 Lead Flatpack	Sine	Figure 6-8
2215[1]	14 Lead Flatpack	Sine	Figure 6-9

Note: [1] Models 2202 through 2205 and 2212 through 2215 represent lead formed versions.

Table 6-2. Typical Weight

Model #	Package	Typical Weight (grams)
2101, 2111	24 Pin DDIP	21
2102, 2202, 2112, 2212	32 Lead Flatpack	10
2103, 2203, 2113, 2213	24 Lead Flatpack	16
2104, 2204, 2114, 2214	14 Lead Flatpack	19
2105, 2205, 2115, 2215	14 Lead Flatpack	8

Table 6-3. Electrical Performance Characteristics–Models 2101, 2102, 2103, 2104, 2105, 2202, 2203, 2204, 2205

Supply Voltage Options[1]: +3.3V or +5V						
Frequency Range (MHz)	Max Current (mA)		Max Rise/Fall Times[2] (ns)	Duty Cycle[2] (%)	Max CMOS Load (pF)	
0.300–100	5.25V	3.465V	5	40 to 60	5.25V	3.465V
	50	35			50	35

Note:
[1] Waveform measurement points and logic limits are in accordance with MIL-PRF-55310, Para 3.6.20.3.
[2] Tested with 15 pF.

Table 6-4. Electrical Performance Characteristics–Model 2111

Supply Voltage Options: +3.3V, +5V, +12V or +15V						
Frequency Range (MHz)	Max Current (mA)		Min Power Out (dBm)		Harmonics/ Subharmonics (>75 MHz) (dBc)	Spurious (dBc)
10–225	3.3V/5V	12V/15V	3.3V/5V	12V/15V	< -20	< -70
	20	35	+3	+7		

Table 6-5. Electrical Performance Characteristics–Models 2112, 2114, 2115, 2212, 2214, 2215

Supply Voltage Options: +3.3V, +5V, +12V or +15V							
Frequency Range (MHz)	Max Current (mA)		Min Power Out (dBm)			Harmonics/ Subharmonics (>75 MHz) (dBc)	Spurious (dBc)
10–150	3.3V/5V	12V/15V	3.3V	5V	12V/15V	< -20	< -70
	20	35	0	+3	+7		

Table 6-6. Electrical Performance Characteristics–Models 2113, 2213

Supply Voltage Options: +12V or +15V						
Frequency Range (MHz)	Max Current (mA)		Min Power Out (dBm)		Harmonics/ Subharmonics (>75 MHz) (dBc)	Spurious (dBc)
10–500	12V	15V	12V	15V	< -20	< -70
	25	35	+5	+7		

Table 6-7. Electrical Test Parameters

Operation Listing	Requirements and Conditions
Input Current	MIL-PRF-55310, Para 4.8.5.1
Initial Accuracy at Reference Temperature	MIL-PRF-55310, Para 4.8.6
Output Logic Voltage Levels	MIL-PRF-55310, Para 4.8.21.3
Rise and Fall Times	MIL-PRF-55310, Para 4.8.22
Duty Cycle	MIL-PRF-55310, Para 4.8.23
Overvoltage Survivability	MIL-PRF-55310, Para 4.8.4
Initial Frequency – Temperature Accuracy	MIL-PRF-55310, Para 4.8.10.1
Frequency – Voltage Tolerance	MIL-PRF-55310, Para 4.8.14
Start-up Time (Fast/Slow Start)	MIL-PRF-55310, Para 4.8.29

Table 6-8. Screening and Test Matrix

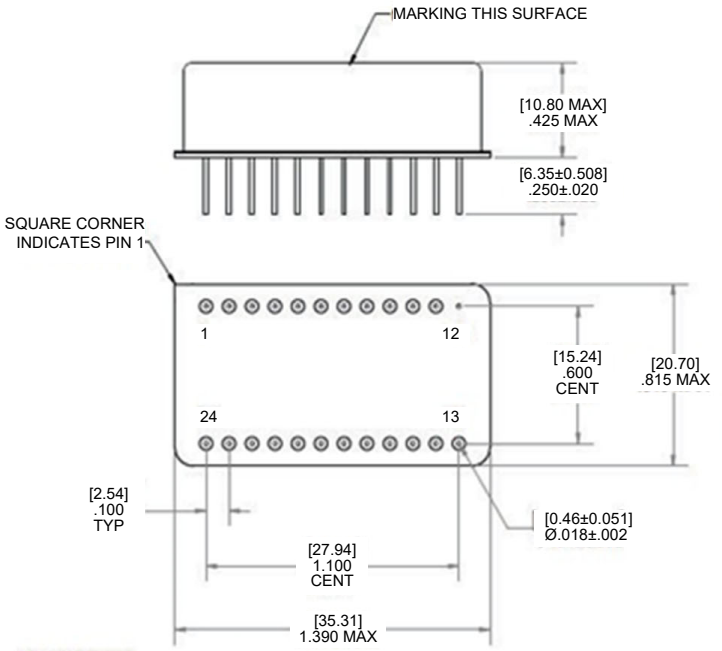
OPN. NO.	Operation Listing	Requirements and Conditions	Option K	Option F	Option S	Option C	Option B	Option X
	SCREENING	MIL Class Similarity (MIL-PRF-55310, Class S/B or MIL-PRF-38534, Class K)	M38534K K	M55310F S	M55310E S	M55310F B+	M55310F B	EM
1	Non-Destruct Bond Pull	MIL-STD-883, Method 2023	X	X	X	NR	NR	NR
2	Internal Visual	MIL-STD-883, Method 2017 Class K or H, Method 2032 Class K or H	X K	X K	X K	X H	X H	X H
3	Stabilization (Vacuum) Bake	MIL-STD-883, Method 1008, Cond. C, 150 °C	X 48 hrs.	X 48 hrs.	X 48 hrs.	X 48 hrs.	X 48 hrs.	X 24 hrs.
4	Random Vibration	MIL-STD-883, Method 2026, Cond. I-B, 15 mins in each axis	NR	X	NR	NR	NR	NR
5	Thermal Shock	MIL-STD-883, Method 1011, Cond. A	X	X	X	NR	NR	NR
6	Temperature Cycle	MIL-STD-883, Method 1010, Cond. B 10 cycles min. MIL-STD-883, Method 1010, Cond. C 10 cycles min.	X NR	NR X	X NR	X NR	X NR	NR NR
7	Constant Acceleration	MIL-STD-883, Method 2001, Cond. A,Y1 plane only, 5000g	X	X	X	X	X	NR
8	Particle Impact Noise Detection	MIL-STD-883, Method 2020, Cond. B MIL-STD-883, Method 2020, Cond. A	X NR	NR X	X NR	X NR	NR NR	NR NR
9	Electrical Testing, Pre Burn-In	Nominal Vcc, +25 °C	X	X	X	X	X	X
10	1st Burn-In	MIL-STD-883, Method 1015, Cond. B	X 160 hrs.	X 240 hrs.	X 240 hrs.	X 160 hrs.	X 160 hrs.	NR
11	Electrical Testing, Intermediate	Nominal Vcc, +25°C and Op Temp Extremes	X	NR	NR	NR	NR	NR
12	2nd Burn-In	MIL-STD-883, Method 1015, Cond. B	X 160 hrs.	NR	NR	NR	NR	NR
13	Electrical Testing, Post Burn-In	Nominal Vcc and extremes, nominal temperature and extremes	X	X	X	X	X	NR
14	Seal: Fine Leak	MIL-STD-202, Method 112, Cond. C (5×10^{-8} atm cc/sec max) MIL-STD-883, Method 1014, TC A2 or B1	X NR	NR X	X NR	X NR	X NR	X NR
15	Seal: Gross Leak	MIL-STD-202, Method 112, Cond. D MIL-STD-883, Method 1014, TC B2 or B3	X NR	NR X	X NR	X NR	X NR	X NR
16	Radiographic Inspection	MIL-STD-883, Method 2012	X	X	X	X	NR	NR
17	Solderability	MIL-STD-883, Method 2003	1	1	1	1	1	1
18	External Visual	MIL-STD-883, Method 2009	X	X	X	X	X	NR
19	Group A Electrical Test[3]	MIL-PRF-55310	X	X	X	Sample	Sample	NR
20	Aging, 30 Day[2] (M55310 Group B)	MIL-PRF-55310, para. 4.8.35.1	X	X	X	Sample	Sample	NR
21	Group C Inspection (optional)	See 4.2. Optional Design, Test, and Data Parameters for details of supplier recommended Group C Inspection options	4.2(g)	4.2(f)	4.2(e)	4.2(e)	4.2(e)	NR

LEGEND: X = Required, NR = Not Required

Notes:

1. Performed at package LAT. Include LAT data sheet.
2. See 3.3.5.1. Frequency Aging Duration Option.
3. See 4.4. Delta Limit Exception.

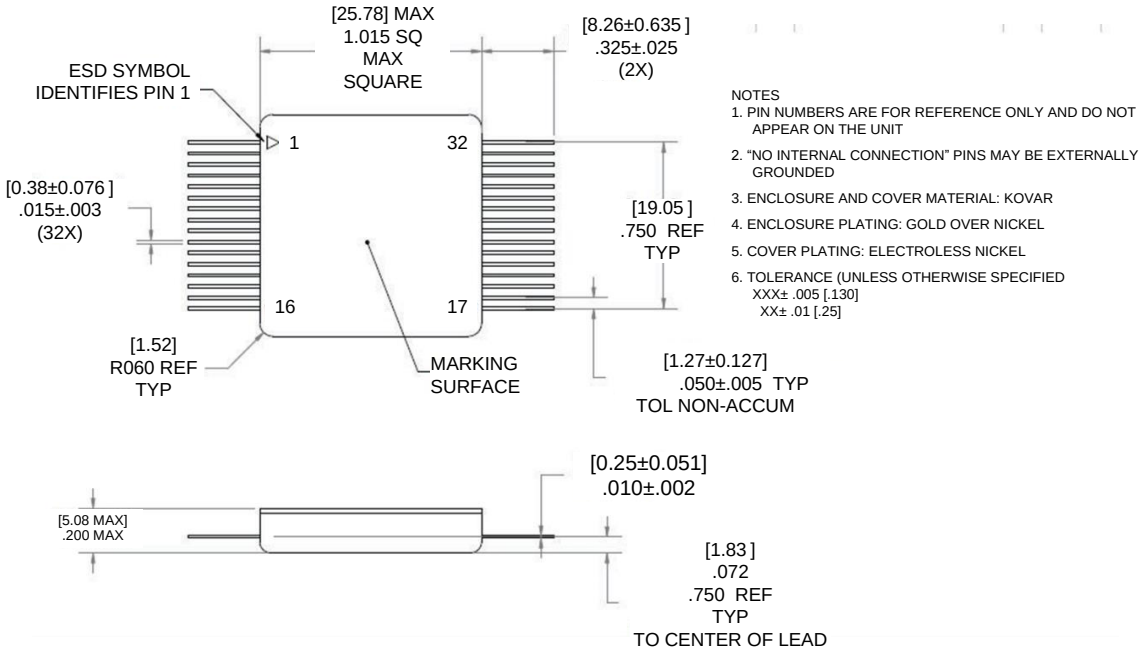
Figure 6-1. Models 2101 and 2111 Package Outline



NOTES
1. PIN NUMBERS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON THE UNIT
2. "NO INTERNAL CONNECTION" PINS MAY BE EXTERNALLY GROUNDED
3. ENCLOSURE AND COVER MATERIAL: KOVAR
4. ENCLOSURE PLATING: GOLD OVER NICKEL
5. COVER PLATING: ELECTROLESS NICKEL
6. TOLERANCE (UNLESS OTHERWISE SPECIFIED
   XXX± .005 [.130]
   XX± .01 [.25]

Pin	Function
1	External Frequency Control
12	GND/Case
13	RF Output
24	Vcc
All Others	No Internal Connection

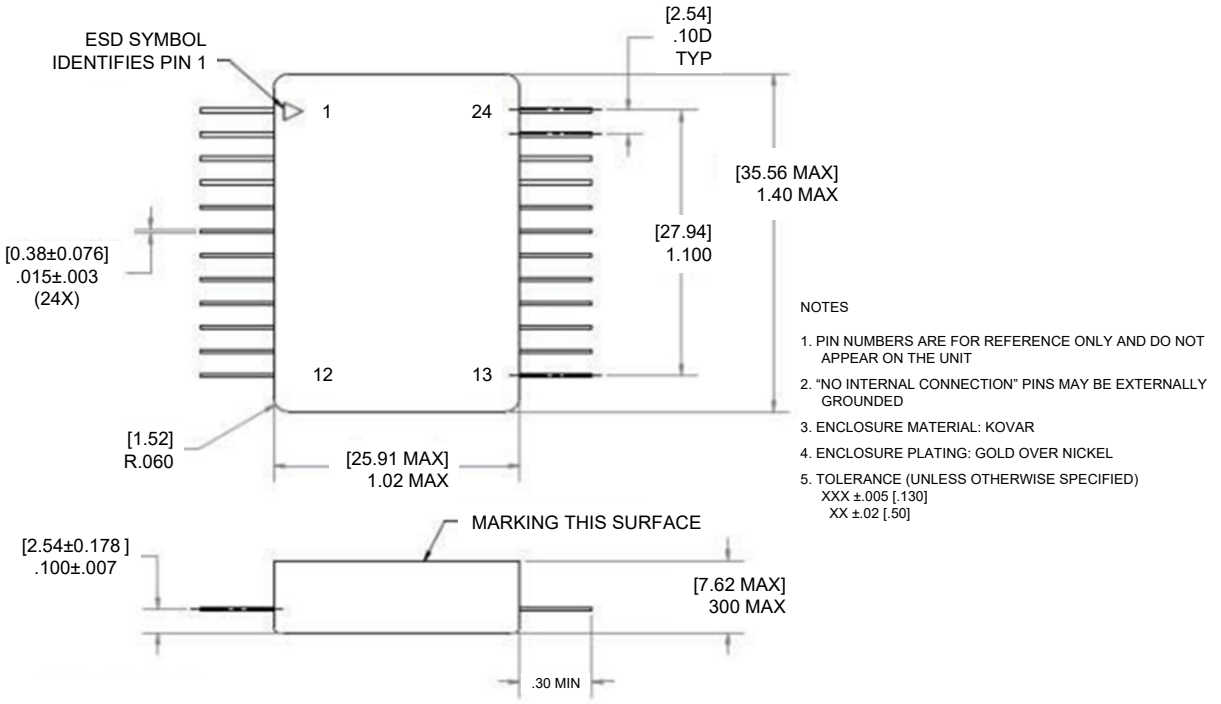
Figure 6-2. Models 2102 and 2112 Package Outline



Pin	Function
4	External Frequency Control
5	GND/Case
11	Vcc
12	RF Output
13	Vcc
All Others	No Internal Connection

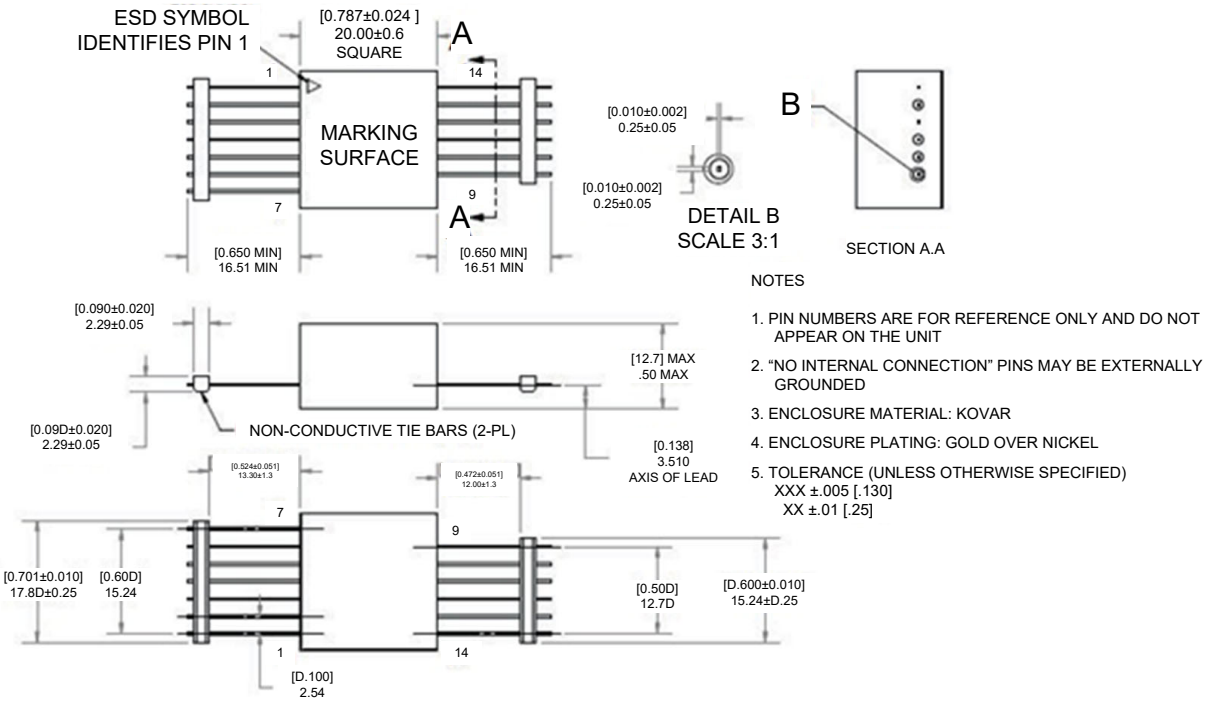
Note: Leads 11 and 13 are connected internally. Either or both can be used.

Figure 6-3. Models 2103 and 2113 Package Outline



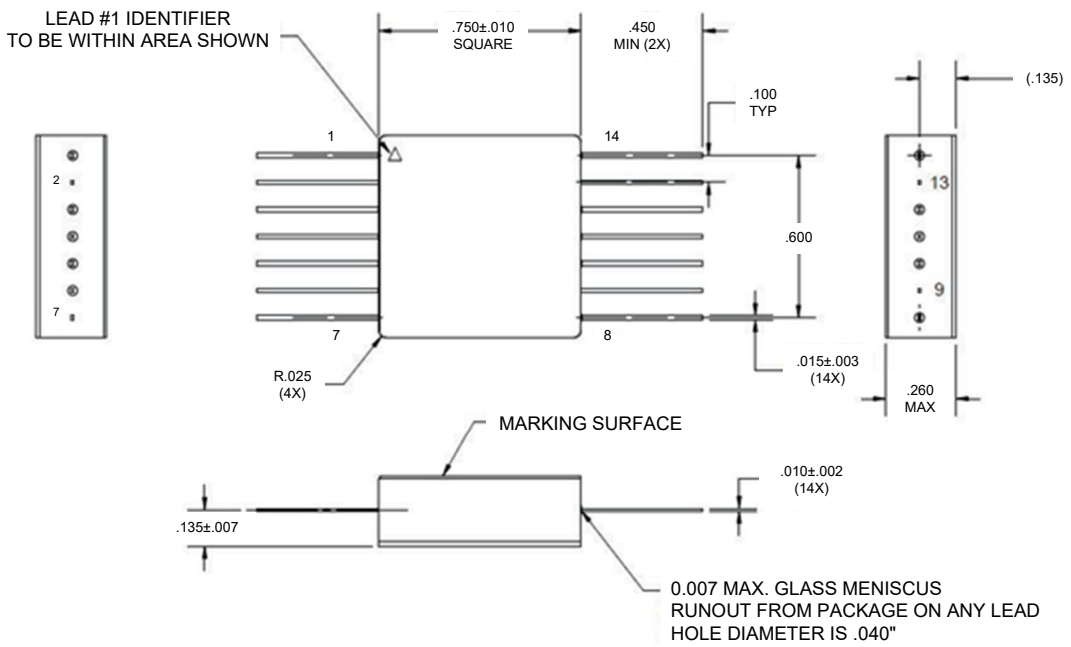
Pin	Function
1	External Frequency Control
2–11	No Internal Connection
12	GND/Case
13	RF Output
14–23	No Internal Connection
24	Vcc

Figure 6-4. Models 2104 and 2114 Package Outline



Pin	Function
1, 3, 7, 12, and 14	GND/Case
2	Vcc
4, 5, 9, 10, and 11	No Internal Connection
6	External Frequency Control
13	RF Output

Figure 6-5. Model 2105 and 2115 Package Outline

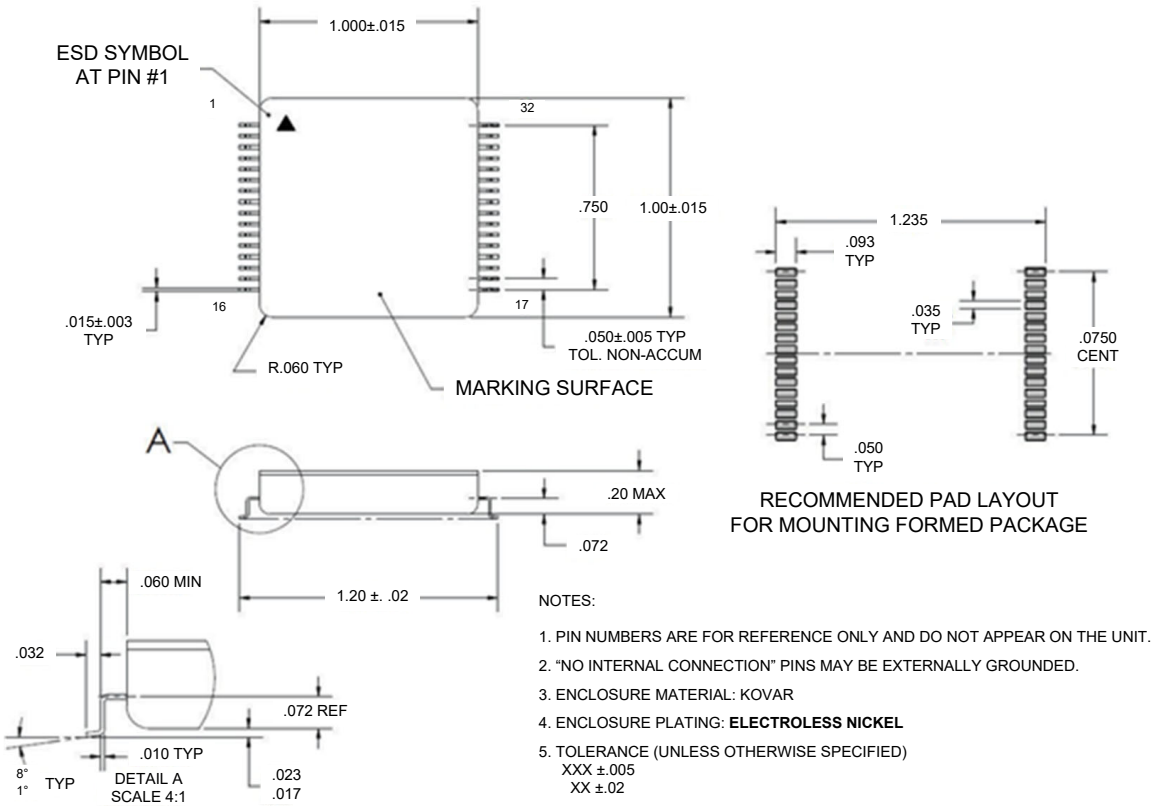


NOTES:

1. PIN NUMBERS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON THE UNIT.
2. "NO INTERNAL CONNECTION" PINS MAY BE EXTERNALLY GROUNDED.
3. ENCLOSURE MATERIAL: KOVAR
4. ENCLOSURE PLATING: GOLD OVER NICKEL
5. TOLERANCE (UNLESS OTHERWISE SPECIFIED)
   XXX ±.005
   XX ±.02

Pin	Function
1	EFC
2	GND/Case
3–6	No Internal Connection
7	GND/Case
8	RF Output
9	GND/Case
10–12	No Internal Connection
13	GND/Case
14	Vcc

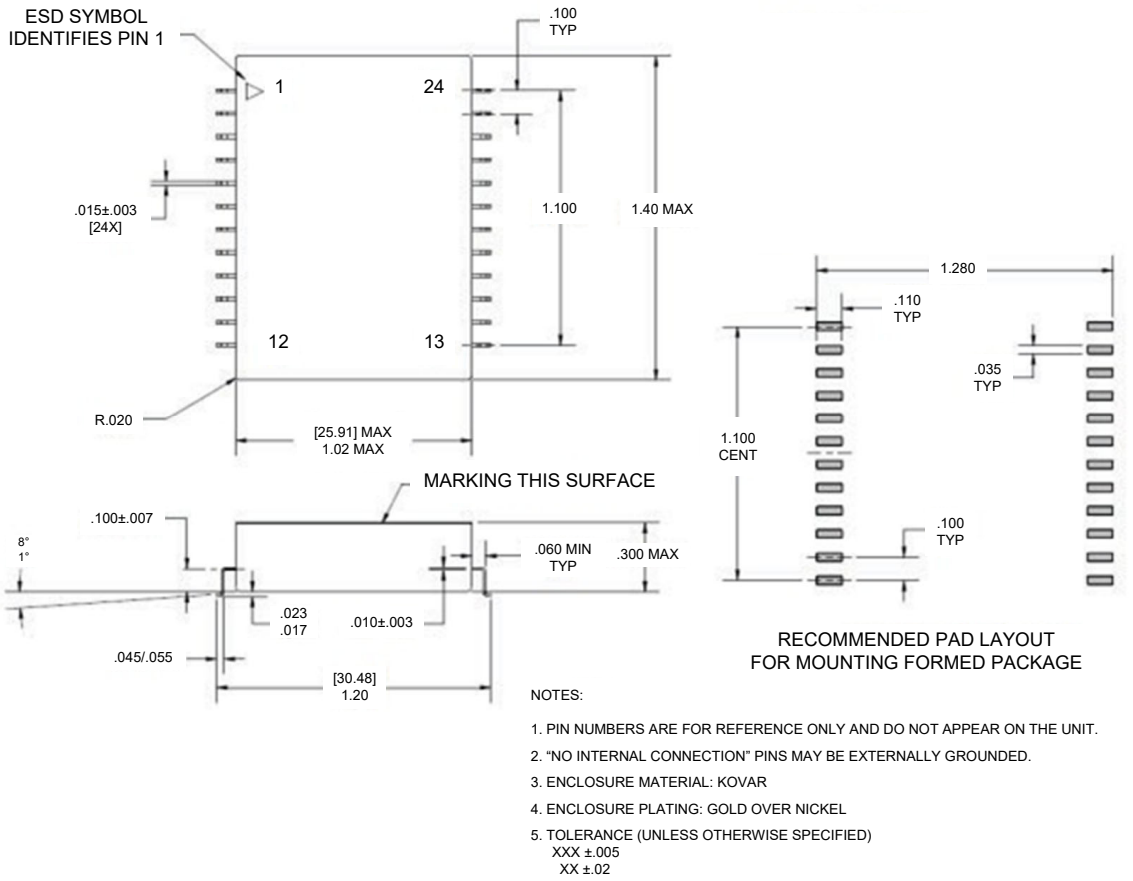
Figure 6-6. Models 2202 and 2212 Package Outline and Land Pattern



Pin	Function
4	External Frequency Control
5	GND/Case
11	Vcc
12	RF Output
13	Vcc
All Others	No Internal Connection

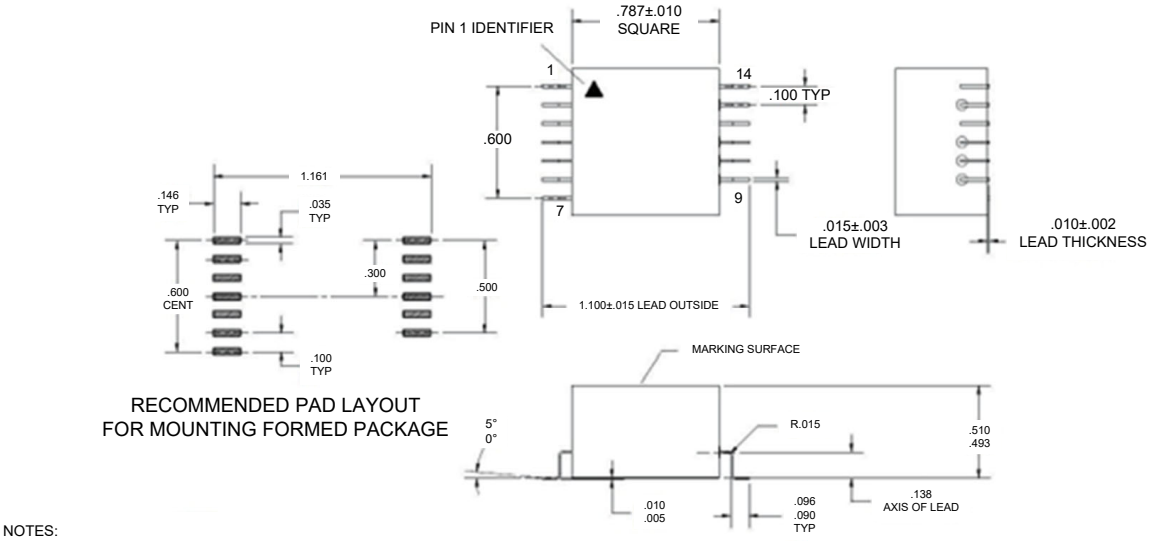
Note: Leads 11 and 13 are connected internally. Either or both can be used.

Figure 6-7. Models 2203 and 2213 Package Outline and Land Pattern



Pin	Function
1	External Frequency Adjust
2–11	No Internal Connection
12	GND/Case
13	RF Output
14–23	No Internal Connection
24	Vcc

Figure 6-8. Models 2204 and 2214 Package Outline and Land Pattern

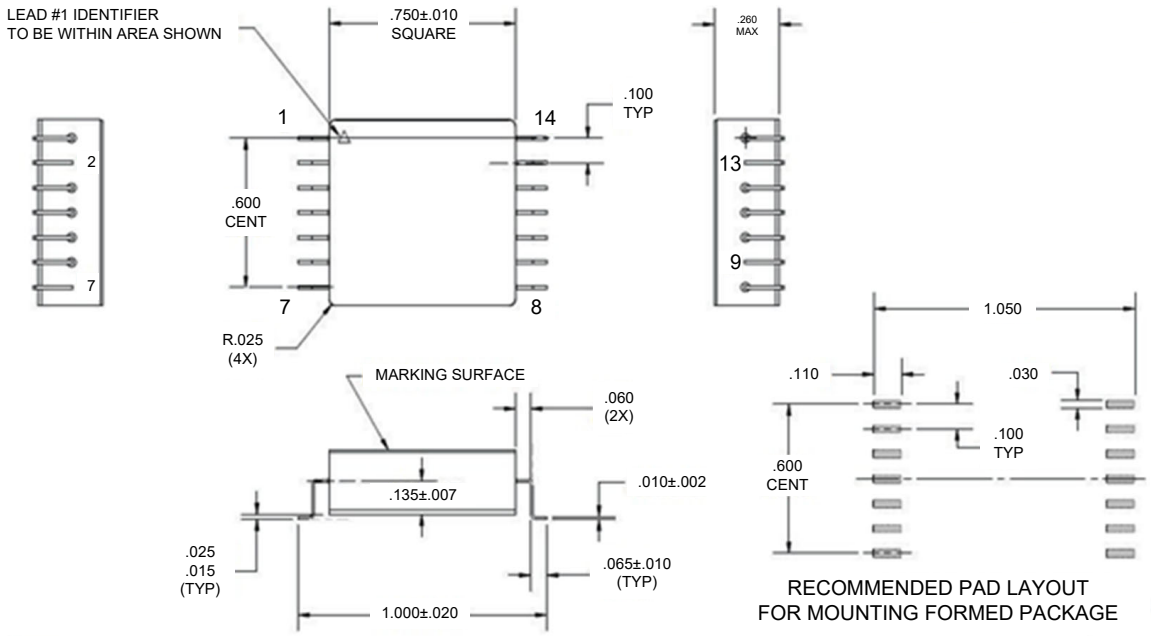


NOTES:

1. PIN NUMBERS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON THE UNIT.
2. “NO INTERNAL CONNECTION” PINS MAY BE EXTERNALLY GROUNDED.
3. ENCLOSURE MATERIAL: KOVAR
4. ENCLOSURE PLATING: GOLD OVER NICKEL
5. TOLERANCE (UNLESS OTHERWISE SPECIFIED)
   XXX ±.005
   XX ±.02

Pin	Function
1, 3, 7, 12, and 14	GND/Case
2	Vcc
4, 5, 9, 10, and 11	No Internal Connection
6	External Frequency Control
13	RF Output

Figure 6-9. Model 2205 and 2215 Package Outline and Land Pattern



NOTES:

1. PIN NUMBERS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON THE UNIT.
2. “NO INTERNAL CONNECTION” PINS MAY BE EXTERNALLY GROUNDED.
3. ENCLOSURE MATERIAL: KOVAR
4. ENCLOSURE PLATING: GOLD OVER NICKEL
5. TOLERANCE (UNLESS OTHERWISE SPECIFIED)
   XXX ±.005
   XX ±.02

Pin	Function
1	EFC
2	GND/Case
3–6	No Internal Connection
7	GND/Case
8	RF Output
9	GND/Case
10–12	No Internal Connection
13	GND/Case
14	Vcc

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