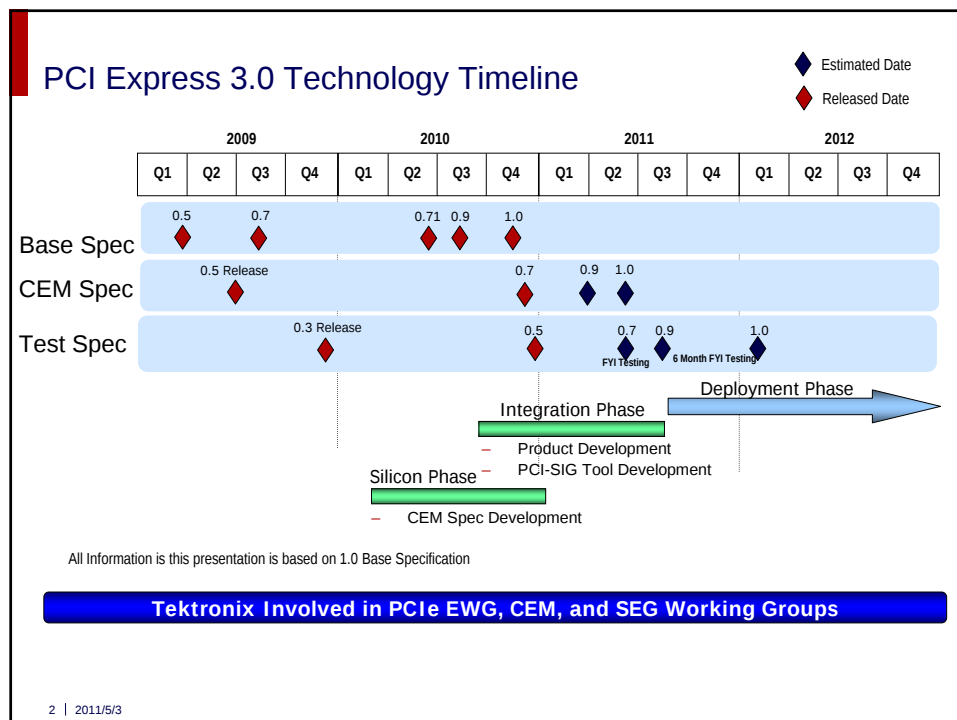




PCI Express 3.0 Testing Approaches for PHY Layer



PCI Express 3.0 Trends and Implications

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Industry/Technology Trends

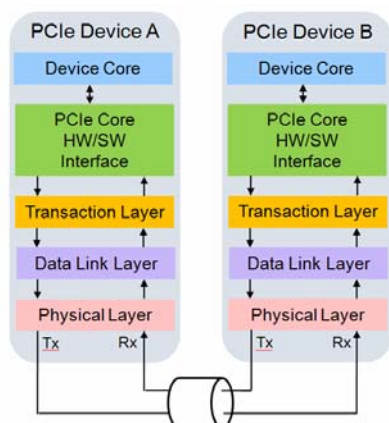
- 8GB/s using the same board material (FR4) and connectors results in increased channel loss
- Probing access at the silicon transmitter pins is typically not available
- Receiver equalization can only compensate for channel loss
- Receiver Testing is a requirement and is critical to ensure system interoperability
- Energy efficiency (Lower mW/Gb/s)

Implications

- Closed data eyes requiring new techniques for transmitter and receiver equalization
- Higher data rate signals have less margin – requires de-embedding for base specification measurements
- New Jitter Separation Measurements are required
- Back channel negotiation to equalize the receiver
- Link training and power management continue to be the most difficult logic layer challenges

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Testing Challenges with PCI Express 3.0



Transaction Layer

- Creates Request/Completion Transactions
- Messaging
- TLP Flow Control

Data Link Layer

- Flow control information
- Data Integrity, Error Checking/Correction
- Calculates/Check TLP Sequence Number
- Calculate/Check CR

Physical Layer – Logical Sub Block

- Link Initialization and Training
- Distribution of packet information over multiple lanes
- Power management and link power state transitions

Physical Layer – Electrical Sub Block

- Transmitter Signal Quality and Ref Clock Testing
- Receiver Testing
- Interconnect Testing
- PLL Loop BW

1

4

Transmitter PHY Layer Analysis for PCIe 3.0

Tektronix DPO/DSA/MSO70000C Series Oscilloscopes

PCI
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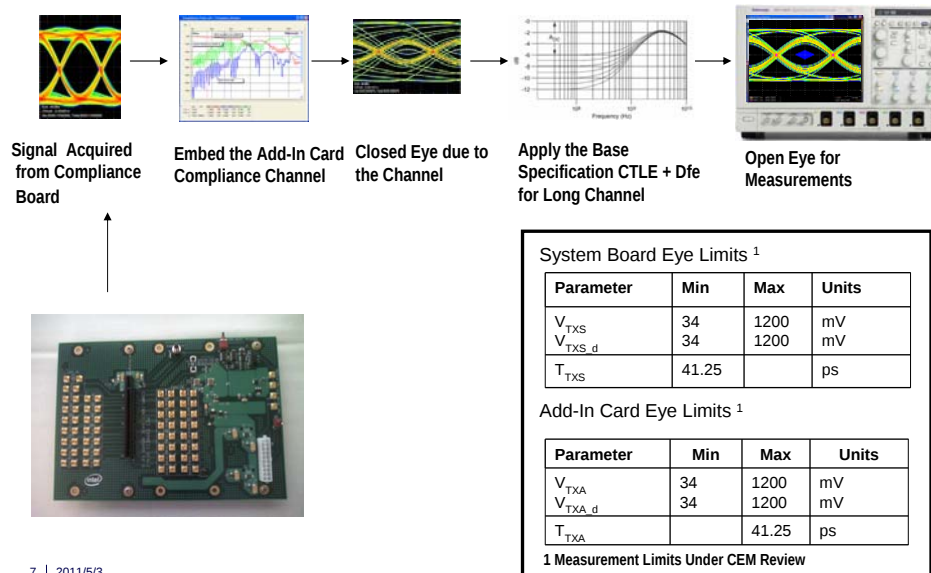
PCIe 3.0 Transmitter Compliance Testing

- Compliance testing is based on the CEM Specification, which is under development
- New compliance 128b/130b data pattern
- Two Tests
 - Electrical: Eye Height and Width must pass one pre-set value
 - Preset Test: all Pre-sets are tested to be within their limits
- Measurements are taken after the Compliance channel and RX Equalization using the Compliance Base or Load Board



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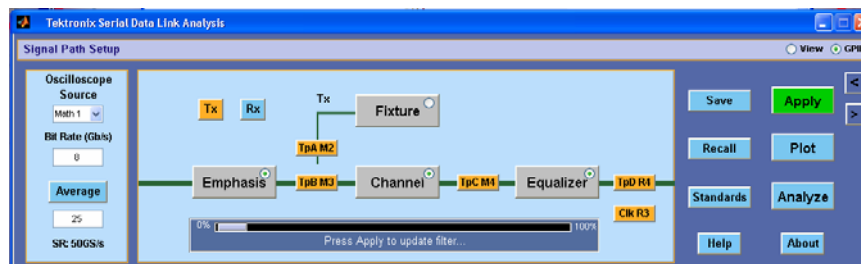
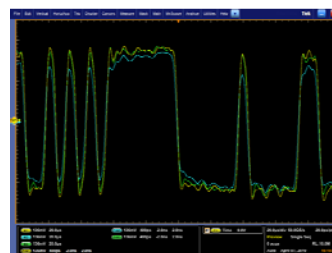
Add-In Card Compliance Signal Acquisition and Processing



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Serial Data Link Analysis

- De-embed the effects of a fixture
- Embed the effects of the channel
- Equalize the waveform using CTLE, FFE, and/or Dfe

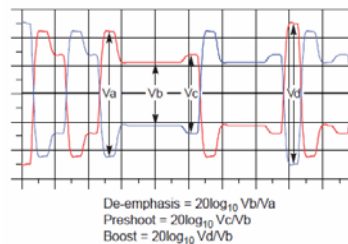
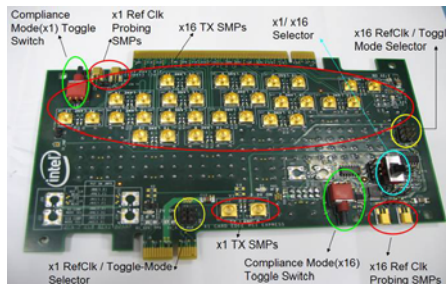


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Transmitter Equalization For Compliance

- Transmitter equalization now requires pre-shoot to compensate for channel loss
- Transmitters must support all defined Pre-Sets
- Pre-sets are toggled on the CLB or CBB the same way as Gen 2 CLB/CBB
- All pre-sets are acquired to verify that Pre-shoot and De-emphasis are within the spec limits

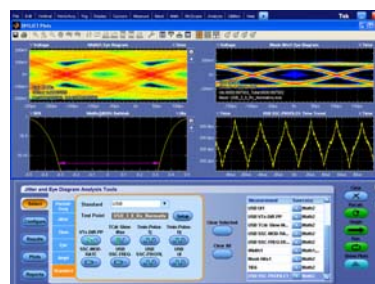
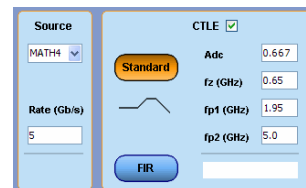
Preset Number	Preshoot (dB)	De-emphasis (dB)
P4	0.0	0.0
P1	0.0	-3.5 ± 1 dB
P0	0.0	-6.0 ± 1.5 dB
P9	3.5 ± 1 dB	0.0
P8	3.5 ± 1 dB	-3.5 ± 1 dB
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB
P5	1.9 ± 1 dB	0.0
P6	2.5 ± 1 dB	0.0
P3	0.0	-2.5 ± 1 dB
P2	0.0	-4.4 ± 1.5 dB
P10	0.0	See Note 2.



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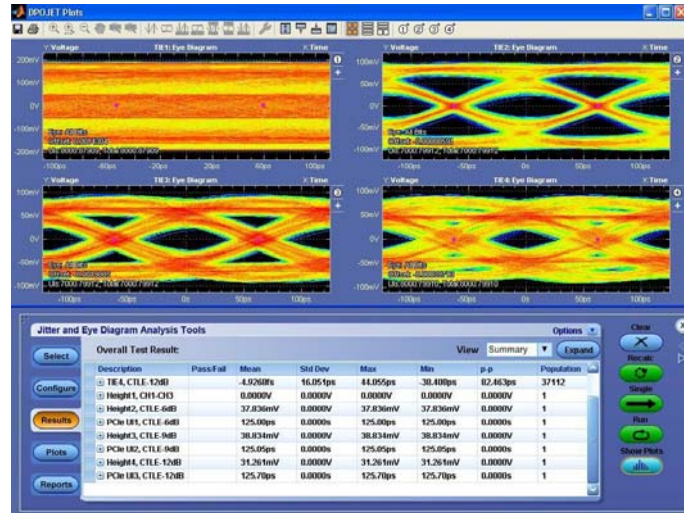
Testing Beyond Compliance

- What happens if a measurement fails SigTest?
- Could it be the channel?
 - Measurements can be taken before the channel to evaluate results
 - Different channel models can be created using Serial Data and Link Analysis
- How does the optimized RX setting compare to other settings?
 - Easily compare the results of multiple Equalization settings
- Does deeper analysis of the waveform need to be done?
 - PCIe specific measurements can be taken in Tektronix' measurement system DPOJET
 - Determine if data dependent, uncorrelated or pulse width jitter is in spec
 - Measurements filters and settings can be adjusted to get to root cause, but remember you must pass SigTest to be certified for compliance
- Is the TX compliant?
 - NEW PCIe 3.0 base spec measurements are available to verify TX compliance



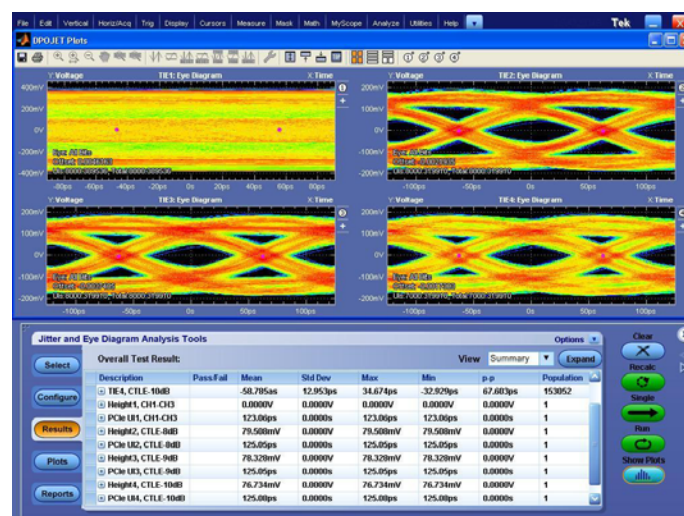
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Optimizing Receiver Equalization



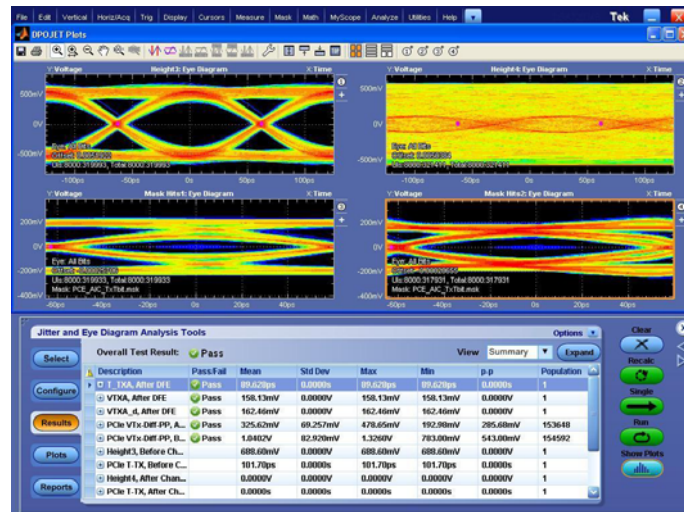
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Optimize Receiver Equalization



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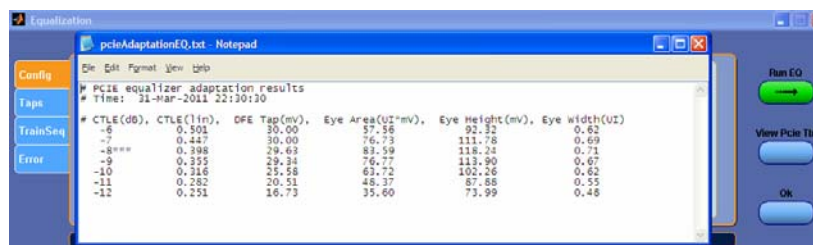
CEM Measurements with Optimized RX Settings



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Automated Receiver Optimization

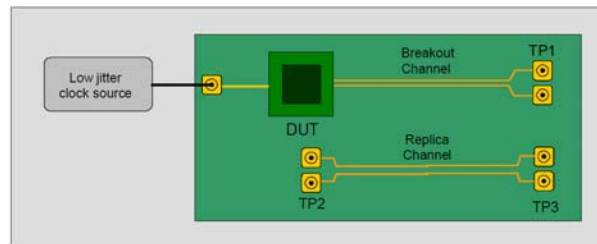
- Manually optimizing over 7 CTLE settings is time consuming
- Optimization is automated with SDLA
- Optimization is done on a short record across all settings, the setting with the best eye opening is then computed and measurements can be taken
- Results from RX Optimization



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Transmitter Characterization

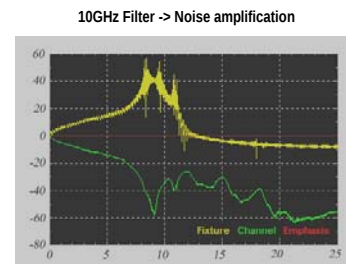
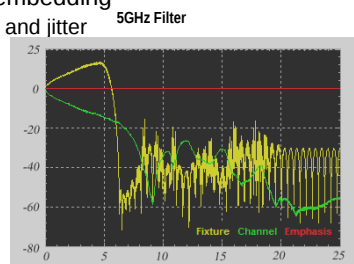
- Base Specification Measurements are defined at the pins of the transmitter
- Signal access at the pins is often not assessable
 - PCIe Base Specification outlines guidelines for designing the test board with a breakout channel to acquire the signal
- De-embedding is required to see what the signal look liked at the pins of the TX, without the added effects of the channel
- Sparameters are acquired on the replica channel



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De-embedding Considerations

- De-embedding amplifies high frequency noise, thus requiring a bandwidth filter
 - This also impacts the required bandwidth for a RT Scope
 - Bandwidth is dependent on board material
- Successful de-embedding starts with good quality board design and S-Parameter data
 - Matched impedance, low loss structures
 - No gain, significant resonances, or large dips
- Quality of de-embedding
 - Eye height and jitter
 - Signal to Noise Ratio



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Base Specification Transmitter Measurements

- Channel must be de-embedded before measurements can be taken
- Tektronix has a PCIe 3.0 De-embed MOI available

The diagram illustrates the process of de-embedding channel effects from a transmitter measurement. It consists of four sequential eye diagrams and a central schematic diagram.

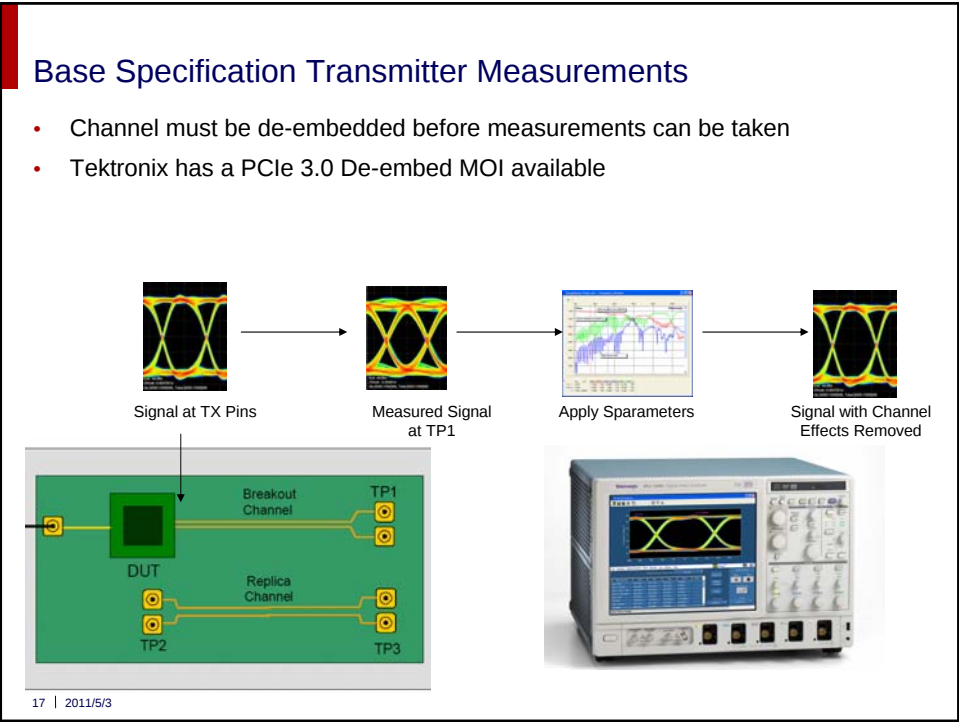
- Signal at TX Pins:** The first eye diagram shows the signal as it appears at the transmitter pins.
- Measured Signal at TP1:** The second eye diagram shows the signal as measured at a test point (TP1), where channel effects are present.
- Apply Sparameters:** A graph showing the application of Sparameters to the measured signal to de-embed the channel effects.
- Signal with Channel Effects Removed:** The final eye diagram shows the signal after the channel effects have been removed, resulting in a cleaner signal.

The schematic diagram below the eye diagrams shows a test setup. A DUT (Device Under Test) is connected to a Breakout Channel and a Replica Channel. The Breakout Channel is connected to TP1 and TP2. The Replica Channel is connected to TP2 and TP3. The signal path is shown as a yellow line.

A photograph of a Tektronix oscilloscope is shown at the bottom right, displaying an eye diagram on its screen.

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NEW PCI Express Base Specification Measurements

- Voltage
- Package Loss
- Transmitter Equalization
- Jitter

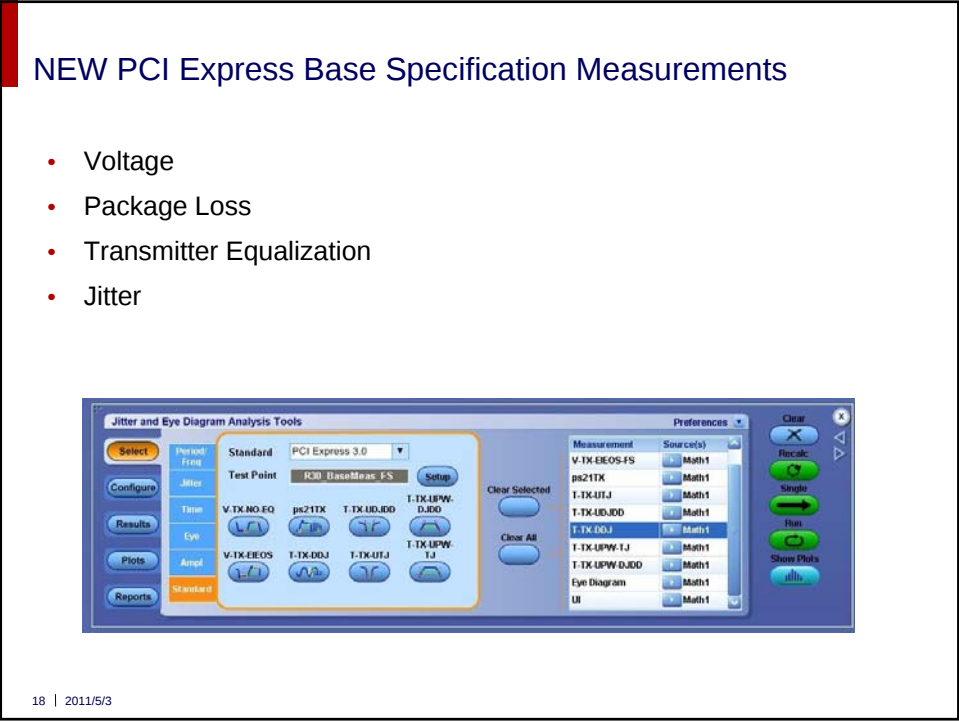
The screenshot displays the 'Jitter and Eye Diagram Analysis Tools' software. The interface is divided into several sections:

- Left Sidebar:** Contains buttons for 'Select', 'Period/Freq', 'Configure', 'Jitter', 'Results', 'Eye', 'Plots', and 'Reports'.
- Main Configuration Area:**
 - Standard:** A dropdown menu currently set to 'PCI Express 3.0'.
 - Test Point:** A dropdown menu currently set to 'R30 BaseMeas ES'.
 - Measurement Icons:** A grid of icons representing different measurements: V-TX-NO-EQ, ps21TX, T-TX-U0J00, T-TX-UPW-DJ00, V-TX-EIOS, T-TX-D0J, T-TX-UTJ, and T-TX-UPW-TJ.
 - Clear Selected:** A button to clear the selected measurements.
- Preferences Panel (Right):** A table listing measurements and their sources.

Measurement	Source(s)
V-TX-EIOS-FS	Math1
ps21TX	Math1
T-TX-UTJ	Math1
T-TX-U0J00	Math1
T-TX-D0J	Math1
T-TX-UPW-TJ	Math1
T-TX-UPW-DJ00	Math1
Eye Diagram	Math1
UI	Math1
- Far Right Toolbar:** Contains buttons for 'Clear', 'Recall', 'Single', 'Run', 'Show Plots', and a plot icon.

- ## NEW PCI Express Base Specification Measurements
- Voltage
 - Package Loss
 - Transmitter Equalization
 - Jitter
-
- The screenshot displays the 'Jitter and Eye Diagram Analysis Tools' software interface. The main window is divided into several sections:
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 - Measurements:** A grid of icons representing different measurement types: V-TX-NO-EQ, ps21TX, T-TX-U0J00, T-TX-UPW-DJ00, V-TX-EIOS, V-TX-D0J, T-TX-U0J, T-TX-UPW-TJ, and T-TX-U0J.
 - Buttons:** 'Setup' button next to the Test Point dropdown, and 'Clear Selected' and 'Clear All' buttons.
 - Right Panel:**
 - Preferences:** A table listing measurements and their sources.

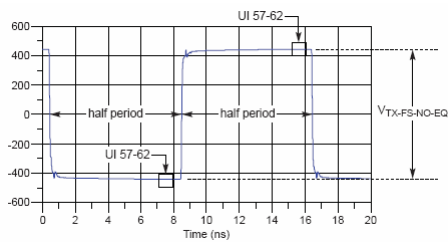
Measurement	Source(s)
V-TX-EIOS-FS	Math1
ps21TX	Math1
T-TX-U0J	Math1
T-TX-U0J00	Math1
T-TX-D0J	Math1
T-TX-UPW-TJ	Math1
T-TX-UPW-DJ00	Math1
Eye Diagram	Math1
UI	Math1
 - Far Right:** A vertical toolbar with buttons for 'Clear', 'Recall', 'Single', 'Run', 'Show Plots', and a plot icon.



Transmitter Equalization Measurements

VTX-BOOST-FS / VTX-BOOST-RS

- What's new for Gen 3.0
 - De-Emphasis (V_a) and pre-shoot (V_c)
 - Transmitters must support 11TX equalization pre-sets
- The high frequency nature of 8.0 GT/s signaling makes measurement of single UI pulse heights impractical due to attenuation by the package and breakout channel
 - Amplitude measurements are taken on low frequency waveforms (64 ones/ 64 zeros in the compliance pattern) using last few UI of each half period
 - V_a and V_c values are obtained by setting the DUT to a different preset value where the desired V_a or V_c voltage occurs during the V_b interval.



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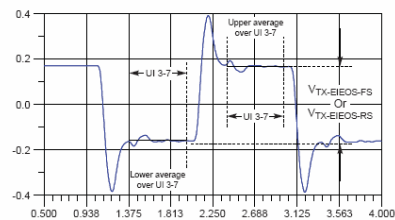
Preset Number	Preshoot (dB)	De-emphasis (dB)
P4	0.0	0.0
P1	0.0	-3.5 ± 1 dB
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P5	1.9 ± 1 dB	0.0
P6	2.5 ± 1 dB	0.0
P3	0.0	-2.5 ± 1 dB
P2	0.0	-4.4 ± 1.5 dB
P10	0.0	See Note 2.

Preset Number	De-emphasis (dB) $20\log_{10}(V_b(i)/V_b(j))$	Preshoot (dB) $20\log_{10}(V_b(i)/V_b(j))$
P4	N/A	N/A
P1	P1/P4	N/A
P0	P0/P4	N/A
P9	N/A	P4/P9
P8	P8/P6	P3/P8
P7	P7/P5	P2/P7
P5	N/A	P4/P5
P6	N/A	P4/P6
P3	P3/P4	N/A
P2	P2/P4	N/A
P10	P10/P4	N/A

Transmitter Voltage Measurements

VTX-EIEOS-FS / VTX-EIEOS-RS

- Launch Voltage of Electrical Idle Exit Ordered Set
- Required to ensure that the RX can properly detect an exit from electrical idle
- Taken on a pattern of eight ones followed by eight zeros repeated 128 times included in the compliance pattern
 - Taken on the middle five UI to reduce attenuation effects of the channel
- VTX-EIEOS-FS - Full Swing Signaling
 - Measured by Preset 10
- VTX-EIEOS-RS – Reduced Swing Signaling
 - Measured by Preset 1



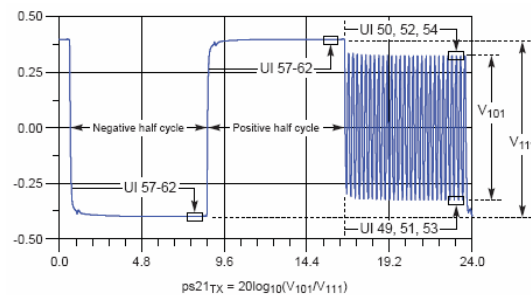
$V_{TX-EIEOS-FS}$	Min swing during EIEOS for full swing	250 (min)	mVPP
$V_{TX-EIEOS-RS}$	Min swing during EIEOS for reduced swing	232 (min)	mVPP

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Package Loss Measurements

PS21

- Can be taken at TP1 while capturing silicon package loss and drive characteristics, but due to the high frequency content of the 1010 pattern the measurement must be de-embedded back to the TX pins
- Measured by comparing 64 zeros and 64 ones PP voltage against a 1010 pattern
- Measured with de-emphasis and pre-shoot set to 0 at the end of each interval to minimize ISI and low frequency effects



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Transmitter Jitter Measurements

- Necessary to take transmitter jitter measurements with all lanes operating in order to capture crosstalk effects
- Measurements are taken at TP1 and de-embedded back to the pins of the TX
- Necessary to separate uncorrelated and data dependent jitter in order to ensure that jitter that can be recovered is not budgeted as uncorrelated jitter

Jitter measurements	Data Dependent Jitter	Uncorrelated Jitter
Cause	Due to package loss and reflections (dynamics in the channel, ISI)	Uncorrelated - PLL jitter, crosstalk, noise conversion (amplitude to phase)
How to compensate	Can be reduced by equalization	Difficult to remove (better components, layout)

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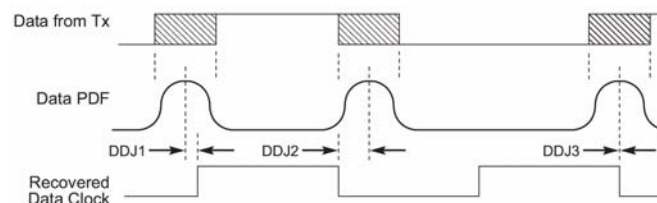
Transmitter Jitter Measurements: Data Dependent Jitter

TTX-DDJ

DDJ Measurement Process

T_{TX-DDJ}	Data dependent jitter	18 (max)	ps PP
--------------	-----------------------	----------	-------

- Measurement taken on multiple repeats of the compliance pattern using a 1st order CDR function representing a high pass filter
- A PDF is created for each edge crossing of the compliance pattern
- DDJ is calculated as the difference of the mean of each PDF and the recovered clock edge
- Measurement is defined as the absolute value of $DDJ(\max) - DDJ(\min)$



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Uncorrelated Jitter Example

TTX-UTJ / TTX-UDJDD

- DDJ is removed from the PDF of each edge
- Data is converted to Q-Scale
- Uncorrelated Deterministic Jitter Dual Dirac (UDJDD)
 - Accounts for Periodic Jitter and Crosstalk Convert the PDF to Q-Scale
- Random Jitter is implied by subtracting UDJDD from UTJ

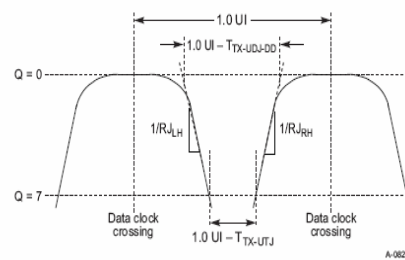
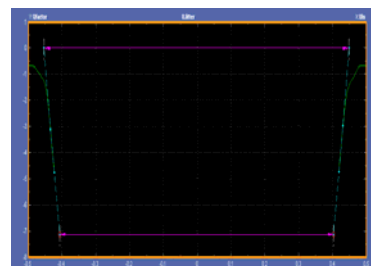


Figure 4-53: Derivation of T_{TX-UTJ} and $T_{TX-UDJDD}$

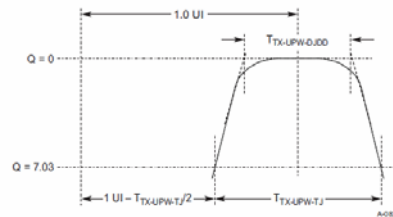


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Uncorrelated Total and Deterministic PWJ

TTX-UPW-TJ / TTX-UPW-DJDD

- Pulse Width Jitter
 - Addresses lone bits that are attenuated the most in lossy channel and could likely cause bit errors
- DDJ is removed to accurately quantify PWJ
- Calculate edge-to-edge jitter
- Construct Q-scale PDF curve and Extrapolate to $\text{BER} = 10^{-12}$ ($Q = 7.03$) to determine Uncorrelated Pulse Width Jitter (containing F/2 or Odd/Even Jitter) and Deterministic Pulse Width Jitter
- Final measurements are calculated by looking at the left hand side of the PDF curve

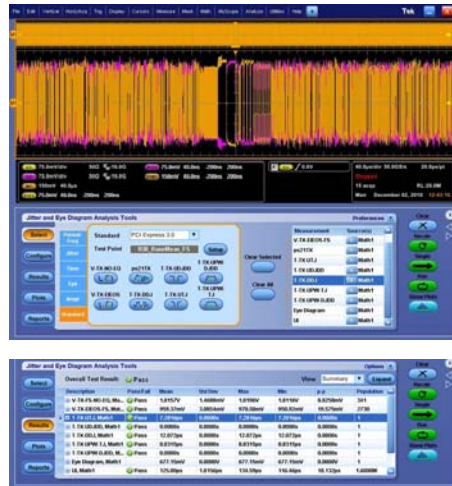


Recommended Bandwidth for PCI Express 3.0

- Balance instrument bandwidth with application requirements
 - Noise increases with bandwidth, too much bandwidth reduces the accuracy and the margin of your measurements
 - PCIe requires the analysis of signals with amplitudes as low as 34mV for compliance testing
 - Ensure enough bandwidth to capture the high frequency content of the signal
 - Need to consider how the channel effects the harmonic content and rise time of the signal
 - De-embedding requires bandwidth limit to reduce the effect of high frequency noise amplification
 - Flexibility for different tasks
 - Characterization and debug vs. compliance
- Recommended bandwidth of 16 GHz
 - Recommended: 16 GHz best balance for PCI Express 3.0 Measurements
 - Minimum: 12 GHz

Tektronix Solutions for PCI Express 3.0 Measurements

- Introducing option PCE3 for DSA/DPO/MSO70K Scopes
- Support for NEW Base Spec measurements
- Support for CEM Specification
- Supports all versions of PCI Express



Considerations for Test Equipment Selection

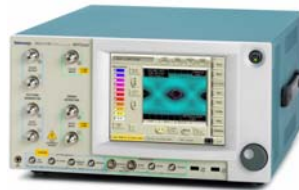
- Test solutions need to go beyond compliance to enable enable root cause analysis
- Channel Embedding and Receiver equalization require new solutions that enable characterizing the optimal settings
- Solutions need to evolve as the test specifications are under development
- Tektronix' has the solutions you need to begin your PCIe 3.0 testing today
 - Active participation in industry working groups enable software updates as the specification evolves
 - PCE3 is not just a compliance solution - spans multiple tasks from Compliance, Characterization, and Debug
 - Complete tools for channel modeling (embedding / de-embedding) and receiver equalization Serial Data and Link Analysis Software (SDLA)
 - New DPO/DSA/MSO70000C Series Oscilloscopes
 - Provides lower noise and jitter with 100GS/s acquisition
 - New Compute Platform reduces overall test time



Receiver PHY Layer Analysis for PCIe 3.0

Tektronix BSA85C Bit Error Rate Tester

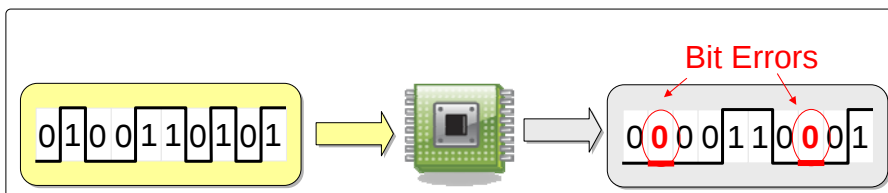
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PCIe 3.0 Implications for Receiver Testing

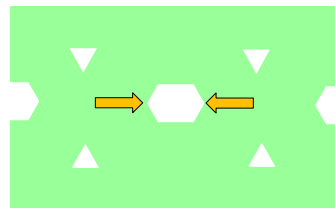
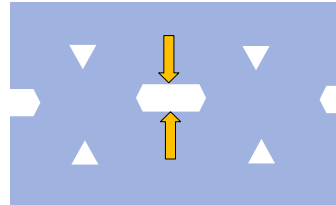
- System margins are decreasing, testing the transmitter only does not imply interoperability
- Receiver testing is expected to be mandatory and will include testing with a Stressed Voltage and Stressed Jitter Eye
 - Differential and Common Mode Interference are new impairment requirements
- Transmitter Equalization requires De-Emphasis and Pre-Shoot
- Receiver Equalization is more sophisticated
 - Behavior equalizers (Continuous Time Linear and Decision Feedback Equalization) must be used to compensate for channel loss
 - Transmitters must support back channel negotiation to auto-negotiate with Receivers to determine optimal equalization settings for testing



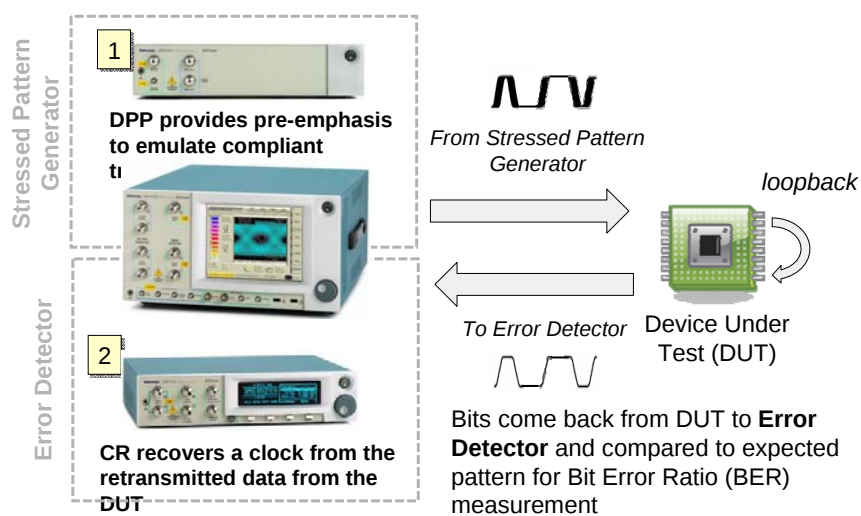
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PCIe Gen3 Receiver Testing

- Two types of tests
 1. Stressed Voltage Eye
 - Achieved by adding interference
 2. Stressed Jitter Eye
 - Achieved by adding jitter



Receiver Test Made Easy the BERTScope



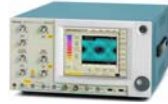
Stressed Voltage Eye

Stressed Pattern Generation



DPP125A
Pre-Emphasis

Stressed
Pattern
Generator



BERTScope

Pre-emphasis presets and coefficient space supported by BERTScope DPP125A

Built-in compliant Random and Sinusoidal Jitter – models support 2.5, 5, 8 and 16 GT/s

Sinusoidal Interference (for DM/CM Interference) available externally (individually) for combining after pre-emphasis

Stressed Voltage Eye

Channel

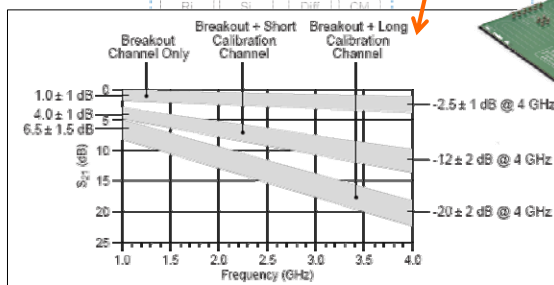


BERTScope
Pre-Emphasis

3 channel lengths =
3 different stressed eyes

Channel

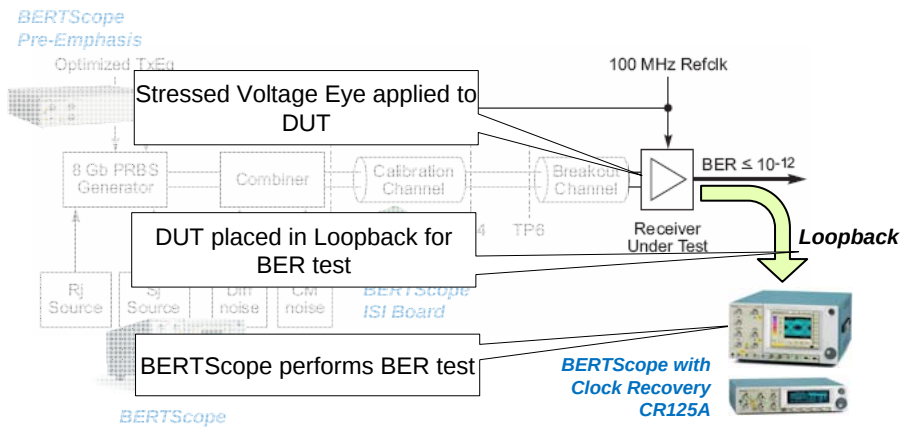
20 dB, -12 dB, -2.5 dB IL at 4 GHz



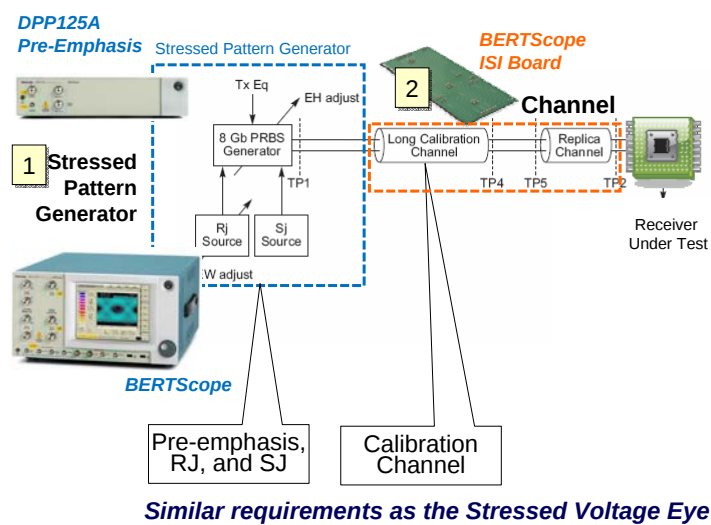
BERTScope ISI Board
For Calibration Channel

Taken from Figure 4-66: Insertion Loss Guidelines for Calibration/Breakout Channels, Base Specification v0.9, © PCI-Sig

Stressed Voltage Test

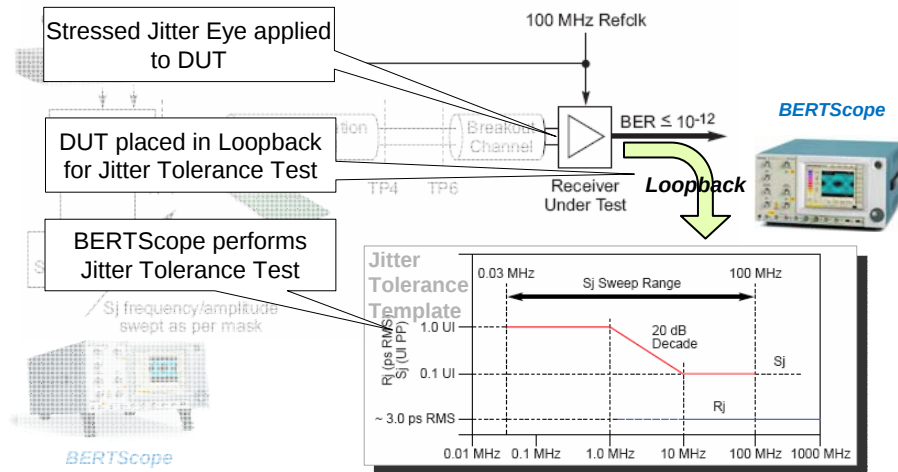


Stressed Jitter Pattern Generation



Stressed Jitter Test

Jitter Tolerance



Taken from Figure 4-74: Swept S_j Mask, Base Specification v0.9, © PCI-Sig

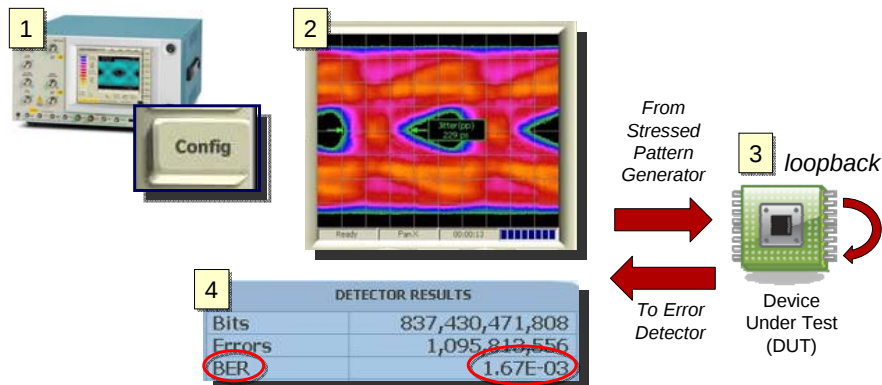
Automated Jitter Tolerance Test on the BERTScope, with Search Mode to find device limits

Requirements for PCI Express 3.0 Receiver Compliance Testing

- Receiver compliance is tested with a worse case eye to ensure BER 10^{-12} with a short and long channel
 - Channel definitions are defined as part of the CEM specification
- Before testing is started, the eye is calibrated with the optimal TX equalization settings for each channel with the 128b/130b Compliance Pattern
 - De-emphasis/Pre-shoot, S_j, R_j, 100Mhz DJ, and Differential Noise are applied
- Receiver's ability to change equalization settings is tested by applying a sub-optimal TX equalization setting to determine the equalization setting for the RX test
 - Some receivers may have RX equalization capability that is more capable than the reference equalizer and may not require the TX to change its equalization setting and thus the sub-optimal TX equalization setting is used for the test
- Device is put into loopback following the loopback procedure in the base specification

Jitter Tolerance Test

- Once the link is in loopback and the optimal equalization settings have been determined the Jitter Tolerance Test Starts
- BERTScope counts any errors
- What if errors occur?



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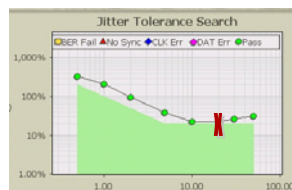
Advanced debug tools to determine cause of RX errors

- **Pattern Sensitivity**: Quickly determine if the source of receiver errors are pattern dependent
- **Error Statistics**: A tabular display of bit and burst error counts and rates
- **Strip Chart**: Determine timing relationships of errors
- **Burst Length**: Determine occurrence of errors of different lengths
- **Error Free Interval**: Number of occurrences of different error-free intervals

1. Basic BER Statistics are OK if everything is passing

DETECTOR RESULTS	
Bits	17,531,077,248
Errors	0
BER	0.00E+00
Resyncs	0
Elapsed Time	00:00:02
Error Free	1.75E+10, 00:00:02

2. But what if the Jitter Tolerance Fails?



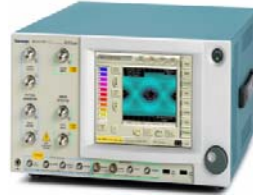
3. Pattern Sensitivity enables root cause of pattern dependent errors



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Considerations for Receiver Test Equipment Selection

- Test solutions need to go beyond compliance to enable root cause analysis
- Transmitter Equalization requires generators that provide spec compliant De-emphasis and Pre-shoot
- Solutions need to evolve as the test specifications are under development
- Tektronix' has the solutions you need to begin your PCIe 3.0 testing today
 - Advanced impairments enable verification of potential interoperability problems
 - Debug Tools enable root cause analysis of receiver errors
 - Quickly determine the margin of the DUT with user selectable jitter tolerance algorithms
 - Loopback training sequence and compliance test patterns are available today
 - PCIe 3.0 Transmitter De-emphasis and Pre-shoot supported today



Important Resources

- **Complete Solutions Available on www.tek.com**
 - Solutions available today for PCIe 1.0, 2.0, 3.0 Transmitter, Receiver, PLL Loop bandwidth and Protocol Testing
- **Support & Resource Links**
 - Recommended Equipment Configurations
 - www.tek.com/serial_data
 - Access to new PCE3 Software Downloads & Free Trial
 - www.tek.com/software (search for PCE3)
 - PCI Express Base Specification (members only)
 - <http://www.pcisig.com/specifications/pciexpress/>