Digital Output Temperature Sensor with On-board SPD EEPROM

N34TS04

TDFN8
MT SUFFIX
CASE 511AK

UDFN8
MU SUFFIX
CASE 517AZ

Description

The N34TS04 is a combination Temperature Sensor (TS) and 4−Kb of Serial Presence Detect (SPD) EEPROM, which implements the JEDEC TSE2004av DDR4 specification and supports the Standard (100 kHz), Fast (400 kHz) and Fast Plus (1 MHz) I^2C protocols.

The TS measures temperature at least 10 times every second. Temperature readings can be retrieved by the host via the serial interface, and are compared to high, low and critical trigger limits stored into internal registers. Over or under limit conditions can be signaled on the open−drain $\overline{EVENT}$ pin.

One of the two available 2−Kb SPD EEPROM banks (referred to as SPD pages in the TSE2004av specification) is activated for access at power−up. After power−up, banks can be switched via software command. Each of the four 1−Kb SPD EEPROM blocks can be Write Protected by software command.

Features

- JEDEC TSE2004av Compliant Temperature Sensor
- DDR4 DIMM Compliant SPD EEPROM
- Temperature Range: −20°C to +125°C
- Supply Range: 1.7 V − 5.5 V (SPD EEPROM) and 2.2 V − 5.5 V (TS)
- I^2C / SMBus Interface
- Schmitt Triggers and Noise Suppression Filters on SCL and SDA Inputs
- 16−Byte Page Write Buffer
- Low Power CMOS Technology
- 2 x 3 x 0.75 mm TDFN Package and 2 x 3 x 0.5 mm UDFN Package
- These Devices are Pb−Free and are RoHS Compliant

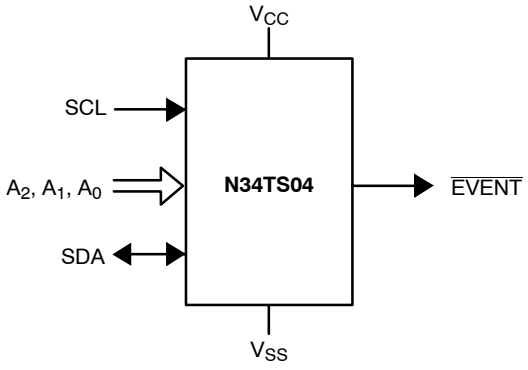
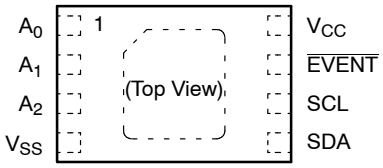


Figure 1. Functional Symbol

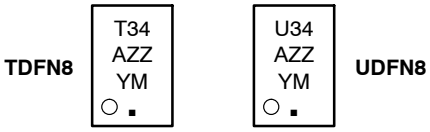
PIN CONFIGURATION



TDFN (MT), UDFN (MU)

For the location of Pin 1, please consult the corresponding package drawing.

MARKING DIAGRAMS



T34, U34 = Specific Device Code
A = Assembly Location Code
ZZ = Assembly Lot Number (Last Two Digits)
Y = Production Year (Last Digit)
M = Production Month (1 − 9, O, N, D)
▪ = Pb−Free Package
○ = Pin 1 Indicator

PIN FUNCTIONS

Pin Name	Function
A_0, A_1, A_2	Device Address Input
SDA	Serial Data Input/Output
SCL	Serial Clock Input
$\overline{EVENT}$	Open−drain Event Output
V_{CC}	Power Supply
V_{SS}	Ground
DAP	Backside Exposed DAP at V_{SS}

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Operating Temperature	−45 to +130	°C
Storage Temperature	−65 to +150	°C
Voltage on any pin (except A_0) with respect to Ground (Note 1)	−0.5 to +6.5	V
Voltage on pin A_0 with respect to Ground	−0.5 to +10.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. The A_0 pin can be raised to a HV level for SWP command execution. SCL and SDA inputs can be raised to the maximum limit, irrespective of V_{CC}.

Table 2. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Units
N_{END} (Note 2)	Endurance (EEPROM)	1,000,000	Write Cycles
T_{DR}	Data Retention (EEPROM)	100	Years

2. Page Mode, V_{CC} = 2.5 V, 25°C

Table 3. TEMPERATURE CHARACTERISTICS (V_{CC} = 2.2 V to 3.6 V, T_A = −20°C to +125°C, unless otherwise specified)

Parameter	Test Conditions/Comments	Max	Unit
Temperature Reading Error	+75°C ≤ T_A ≤ +95°C, active range	±1.0	°C
	+40°C ≤ T_A ≤ +125°C, monitor range	±2.0	°C
	−20°C ≤ T_A ≤ +125°C, sensing range	±3.0	°C
ADC Resolution		12	Bits
Temperature Resolution		0.0625	°C
Conversion Time		100	ms
Thermal Resistance (Note 3) θ_{JA}	Junction−to−Ambient (Still Air)	92	°C/W

3. Power Dissipation is defined as $P_J = (T_J - T_A)/\theta_{JA}$, where T_J is the junction temperature and T_A is the ambient temperature. The thermal resistance value refers to the case of a package being used on a standard 2−layer PCB.

Table 4. D.C. OPERATING CHARACTERISTICS (V_{CC} = 1.7 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified)

Symbol	Parameter	Test Conditions/Comments	Min	Max	Unit
I_{CC}	Supply Current	TS active, SPD and Bus idle		1000	μA
		SPD Write, TS shut−down		1000	μA
I_{SHDN}	Standby Current	TS shut−down; SPD and Bus idle		10	μA
I_{LKG}	I/O Pin Leakage Current	Pin at GND or V_{CC}		2	μA
V_{IL}	Input Low Voltage	V_{CC} ≥ 2.2 V	−0.5	0.3 x V_{CC}	V
		V_{CC} < 2.2 V	−0.05	0.25 x V_{CC}	
V_{IH}	Input High Voltage	V_{CC} ≥ 2.2 V	0.7 x V_{CC}	V_{CC} + 0.5	V
		V_{CC} < 2.2 V	0.75 x V_{CC}	V_{CC} + 0.5	
V_{OL} (Note 4)	Output Low Voltage	I_{OL} = 3 mA, V_{CC} ≥ 2.2 V		0.4	V
		I_{OL} = 1 mA, V_{CC} < 2.2 V		0.2	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The device is able to handle R_L values corresponding to the specified rise time (see Figure 2).

Table 5. A.C. CHARACTERISTICS (V_{CC} = 1.7 V to 5.5 V, T_A = −40°C to +125°C)

Symbol	Parameter	Min	Max	Units
F_{SCL} (Note 5)	Clock Frequency	0.01	1	MHz
t_{HIGH}	High Period of SCL Clock	260		ns
t_{LOW}	Low Period of SCL Clock	500		ns
$t_{TIMEOUT}$ (Note 6)	SMBus SCL Clock Low Timeout	25	35	ms
t_R (Note 7)	SDA and SCL Rise Time		120	ns
t_F (Note 7)	SDA and SCL Fall Time		120	ns
$t_{SU:DAT}$	Input Data Setup Time	50		ns
$t_{SU:STA}$	START Condition Setup Time	260		ns
$t_{HD:STA}$	START Condition Hold Time	260		ns
$t_{SU:STO}$	STOP Condition Setup Time	260		ns
t_{BUF}	Bus Free Time Between STOP and START	500		ns
$t_{HD:DAT}$	Input Data Hold Time	0		ns
t_{DH} (Note 7)	Output Data Hold Time	120	300	ns
T_i	Noise Pulse Filtered at SCL and SDA Inputs		50	ns
t_{WR}	Write Cycle Time		5	ms
t_{PU} (Note 8)	Power-Up Delay to Valid Temperature Recording		100	ms

5. Test conditions according to AC Test Conditions table. Bus loading must be such as to allow meeting the V_{IL} and V_{OL} as well as all other timing requirements. The minimum clock frequency of 10 kHz is an SMBus recommendation; the minimum operating clock frequency is limited only by the SMBus time−out. The device also meets the Fast and Standard I^2C specifications, except that T_i and t_{DH} are shorter, as required by the 1 MHz Fast Plus protocol.
6. For the N34TS04, the interface will reset itself and will release the SDA line if the SCL line stays low beyond the $t_{TIMEOUT}$ limit. The time−out count takes place when SCL is low in the time interval between START and STOP.
7. In a “Wired−OR” system (such as I^2C or SMBus), SDA rise time is determined by bus loading. Since each bus pull−down device must be able to sink the (external) bus pull−up current (in order to meet the V_{IL} and/or V_{OL} limits), it follows that SDA fall time is inherently faster than SDA rise time. SDA rise time can exceed the standard recommended t_R limit, as long as it does not exceed $t_{LOW} - t_{DH} - t_{SU:DAT}$, where t_{LOW} and t_{DH} are actual values (rather than spec limits). A shorter t_{DH} leaves more room for a longer SDA t_R, allowing for a more capacitive bus or a larger bus pull−up resistor.
8. The first valid temperature recording can be expected after t_{PU} at nominal supply voltage.

Table 6. PIN CAPACITANCE (T_A = 25°C, V_{CC} = 3.6 V, f = 1 MHz)

Symbol	Parameter	Test Conditions/Comments	Min	Max	Unit
C_{IN}	SDA, $\overline{\text{EVENT}}$ Pin Capacitance	V_{IN} = 0		8	pF
	Input Capacitance (other pins)	V_{IN} = 0		6	pF

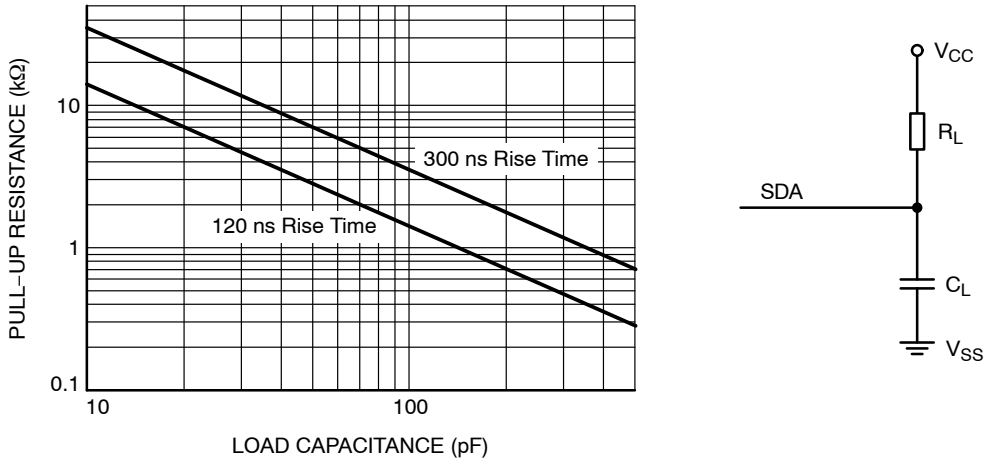


Figure 2. Pull−up Resistance vs. Load Capacitance

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master (Host).

SDA: The Serial Data I/O pin receives input data and transmits data stored in SPD memory or in the TS registers. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A0, A1 and A2: The Address pins accept the device address. These pins have on−chip pull−down resistors.

$\overline{\text{EVENT}}$: The open−drain $\overline{\text{EVENT}}$ pin can be programmed to signal over/under temperature limit conditions.

Power−On Reset (POR)

The N34TS04 incorporates Power−On Reset (POR) circuitry which protects the device against powering up to an undetermined logic state. As V_{CC} exceeds the POR trigger level, the TS component will power up into conversion mode and the SPD component will power up into standby mode. Both the TS and SPD components will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi−directional POR behavior protects the N34TS04 against brown−out failure following a temporary loss of power. The POR trigger level is set below the minimum operating V_{CC} level.

Device Interface

The N34TS04 supports the Inter−Integrated Circuit (I^2C) and the System Management Bus (SMBus) data transmission protocols. These protocols describe serial communication between transmitters and receivers sharing a 2−wire data bus. Data flow is controlled by a Master device, which generates the serial clock and the START and STOP conditions. The N34TS04 acts as a Slave device. Master and Slave alternate as transmitter and receiver. Up to 8 N34TS04 devices may be present on the bus simultaneously, and can be individually addressed by matching the logic state of the address inputs A0, A1, and A2.

I^2C/SMBus Protocol

The I^2C/SMBus uses two ‘wires’, one for clock (SCL) and one for data (SDA). The two wires are connected to the V_{CC} supply via pull−up resistors. Master and Slave devices connect to the bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to ‘transmit’ a ‘0’ and releases it to ‘transmit’ a ‘1’.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 3).

START

The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a ‘wake−up’ call to all Slaves. Absent a START, a Slave will not respond to commands.

STOP

The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP tells the Slave that no more data will be written to or read from the Slave.

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8−bit serial Slave address. The first 4 bits of the Slave address (the preamble) determine whether the command is intended for the Temperature Sensor (TS) or the EEPROM. The next 3 bits, A2, A1 and A0, select one of 8 possible Slave devices. The last bit, R/$\overline{\text{W}}$, specifies whether a Read (1) or Write (0) operation is being performed.

Acknowledge

A matching Slave address is acknowledged (ACK) by the Slave by pulling down the SDA line during the 9^{th} clock cycle (Figure 4). After that, the Slave will acknowledge all data bytes sent to the bus by the Master. When the Slave is the transmitter, the Master will in turn acknowledge data bytes in the 9^{th} clock cycle. The Slave will stop transmitting after the Master does not respond with acknowledge (NoACK) and then issues a STOP. Bus timing is illustrated in Figure 5.

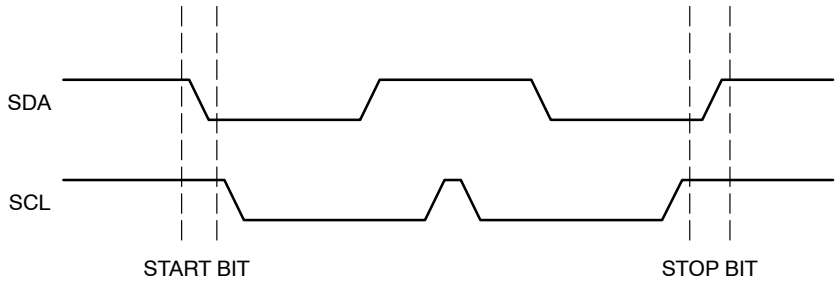


Figure 3. Start/Stop Timing

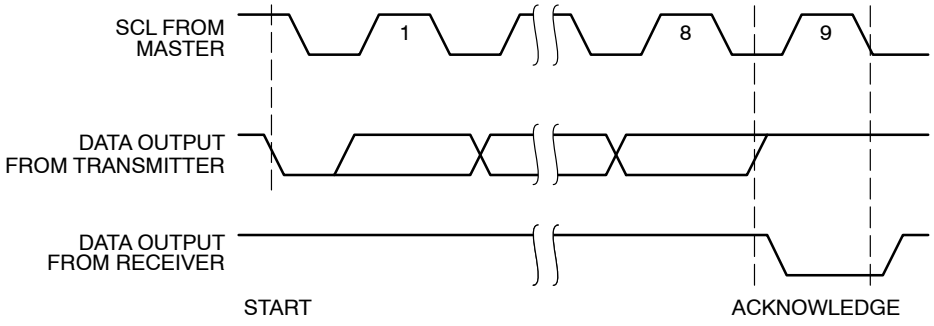


Figure 4. Acknowledge Timing

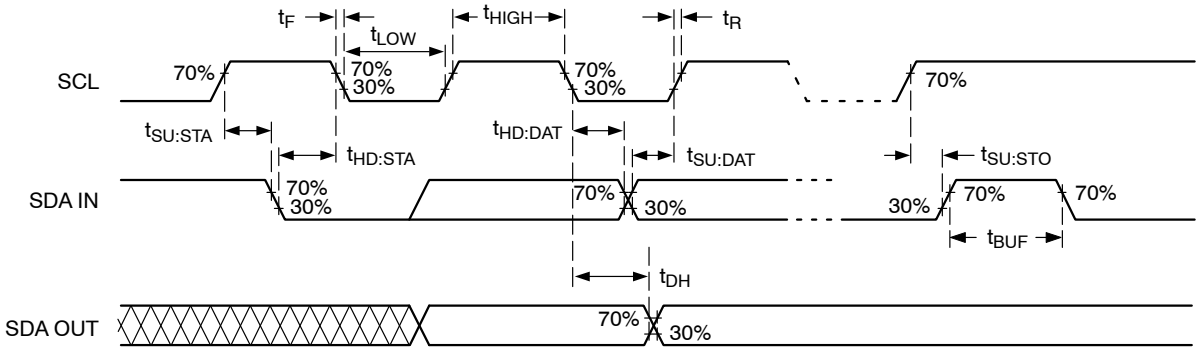


Figure 5. Bus Timing

Table 7. COMMAND SET (Notes 9, 10)

Function	Abbr	Function Specific Preamble				Select Address			R/W_n	A0 Pin
		b7	b6	b5	b4	b3	b2	b1	b0	
Read Temperature Registers	RTR	0	0	1	1	LSA2	LSA1	LSA0	1	0 or 1
Write Temperature Registers	WTR								0	
Read EE Memory	RSPD	1	0	1	0	LSA2	LSA1	LSA0	1	0 or 1
Write EE Memory	WSPD								0	
Set Write Protection, block 0	SWP0	0	1	1	0	0	0	1	0	V_{HV}
Set Write Protection, block 1	SWP1					1	0	0	0	V_{HV}
Set Write Protection, block 2	SWP2					1	0	1	0	V_{HV}
Set Write Protection, block 3	SWP3					0	0	0	0	V_{HV}
Clear All Write Protection	CWP					0	1	1	0	V_{HV}
Read Protection Status, block 0	RPS0					0	0	1	1	0, 1 or V_{HV}
Read Protection Status, block 1	RPS1					1	0	0	1	0, 1 or V_{HV}
Read Protection Status, block 2	RPS2					1	0	1	1	0, 1 or V_{HV}
Read Protection Status, block 3	RPS3					0	0	0	1	0, 1 or V_{HV}
Set SPD Page Address to 0 (Select Lower Bank)	SPA0					1	1	0	0	0, 1 or V_{HV}
Set SPD Page Address to 1 (Select Upper Bank)	SPA1					1	1	1	0	0, 1 or V_{HV}
Read SPD Page Address	RPA					1	1	0	1	0, 1 or V_{HV}
Reserved	–					All Other Encodings				

9. LSAx stands for Logic State of Address pin x.
10. If V_{HV} is not applied on the A0 pin during SWP/CWP commands, the N34TS04 will respond with NoACK after the 3rd byte and will not execute the SWP/CWP instruction. During RPS/SPA/RPA commands the state of pin A0 must be stable for the duration of the sequence.

SPD EEPROM Bank Selection

Upon power−up, the address pointers for both the Temperature Sensor (TS) and on−board EEPROM are initialized to 00h. The TS address pointer will thus point to the Capability Register and the EEPROM address pointer will point to the first location in the lower 2−Kb bank (SPD page 0).

Only one SPD page is visible (active) at any given time. The lower SPD page is automatically selected at power−up. The upper SPD page can be activated (and the lower one implicitly de−activated) by executing the SPA1 utility command. The SPA0 utility command can then be used to re−activate the lower SPD page without powering down. The identity of the active SPD page can be retrieved with the RPA command.

SPD page selection related command details are presented in Table 9c, Table 9d, Figure 13 and Figure 14.

Write Operations

EEPROM Byte and TS Register Write

To write data to a TS register, or to the on−board EEPROM, the Master creates a START condition on the bus, and then sends out the appropriate Slave address (with the R/$\overline{W}$ bit set to '0'), followed by a starting data byte address or TS register address, followed by data. The matching Slave will acknowledge the Slave address, EEPROM byte address or TS register address and the data byte(s), one for EEPROM data (Figure 6) and two for TS register data (Figure 7). The Master then ends the session by creating a STOP condition on the bus. The STOP completes the (volatile) TS register update or starts the internal Write cycle for the (non−volatile) EEPROM data (Figure 8).

EEPROM Page Write

Each of the two 2−Kb banks is organized as 16 pages of 16 bytes each (not to be confused with the SPD page, which refers to the entire 2−Kb bank). One of the 16 memory pages is selected by the 4 most significant bits of the byte address, while the 4 least significant bits point to the byte position within the page. Up to 16 bytes can be written in one Write cycle (Figure 9).

During data load, the internal byte position pointer is automatically incremented after each data byte is loaded. If the Master transmits more than 16 data bytes, then earlier data will be replaced by later data in a 'wrap−around' fashion within the 16−byte wide data buffer. The internal Write cycle then starts following the STOP.

Acknowledge Polling

Acknowledge polling can be used to determine if the N34TS04 is busy writing to EEPROM, or is ready to accept commands. Polling is executed by interrogating the device with a 'Selective Read' command (see READ OPERATIONS). The N34TS04 will not acknowledge the Slave address as long as internal EEPROM Write is in progress.

Delivery State

The N34TS04 is shipped 'unprotected', i.e. none of the Software Write Protection (SWP) flags is set. The entire memory is erased, i.e. all bytes are 0xFF.

Read Operations

Immediate Read

A N34TS04 presented with a Slave address containing a '1' in the R/$\overline{W}$ position will acknowledge the Slave address and will then start transmitting SPD data or respectively TS register data from the current address pointer location. The Master stops this transmission by responding with NoACK, followed by a STOP (Figures 10a, 10b).

Selective Read

The Read operation can be started from a specific address, by preceding the Immediate Read sequence with a 'data less' Write sequence. The Master sends out a START, Slave address and byte or register address, but rather than following up with data (as in a Write operation), the Master then issues another START and continuous with an Immediate Read sequence (Figures 11a, 11b).

Sequential EEPROM Read

EEPROM data can be read out indefinitely, as long as the Master responds with ACK (Figure 12). The internal address pointer is automatically incremented after every data byte sent to the bus. If the end of the active 2−Kb bank is reached during continuous Read, then the address count 'wraps−around' to the beginning of the active 2−Kb bank, etc. Sequential Read works with either Immediate Read or Selective Read, the only difference being that in the latter case the starting address is intentionally updated.

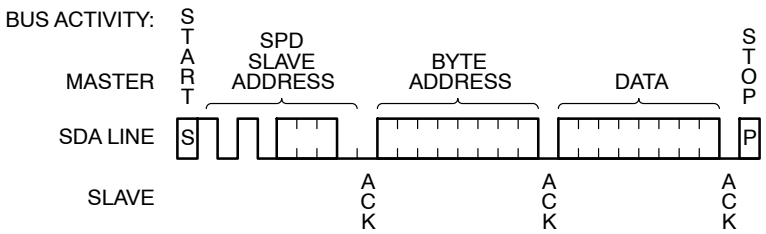


Figure 6. EEPROM Byte Write

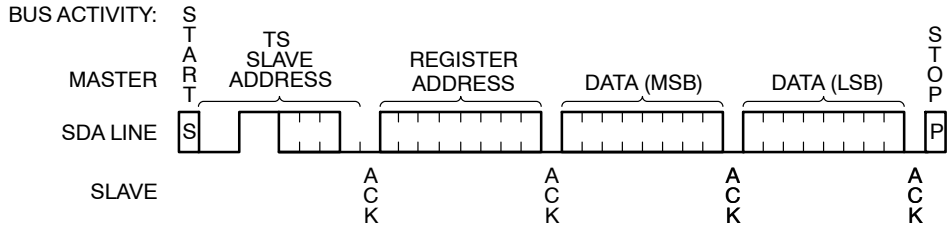


Figure 7. Temperature Sensor Register Write

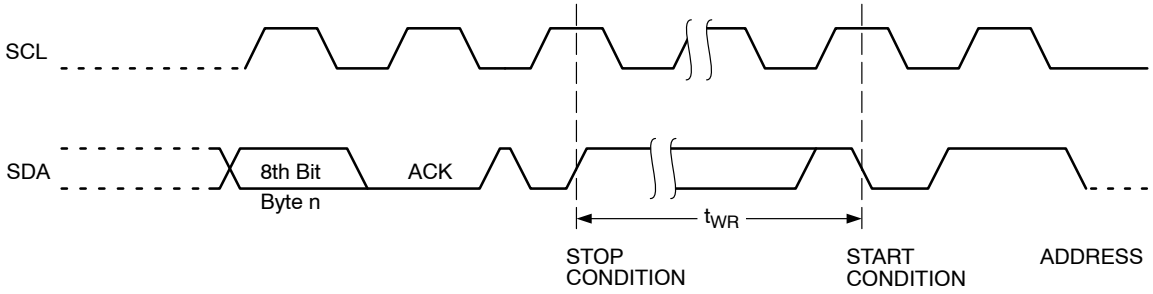
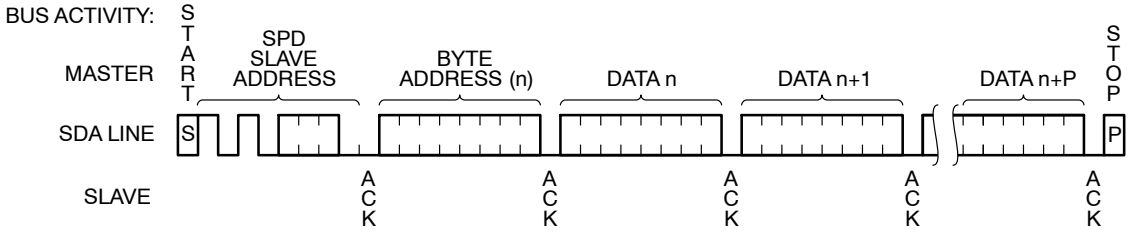


Figure 8. EEPROM Write Cycle Timing



NOTE: In this example n = XXXX 0000(B); X = 1 or 0

Figure 9. EEPROM Page Write

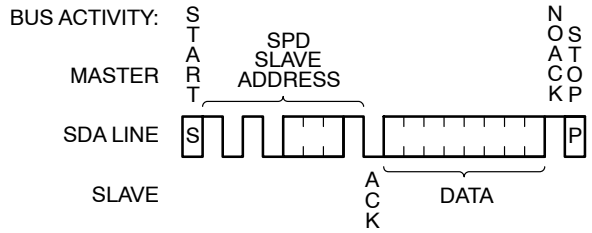


Figure 10a. EEPROM Immediate Read

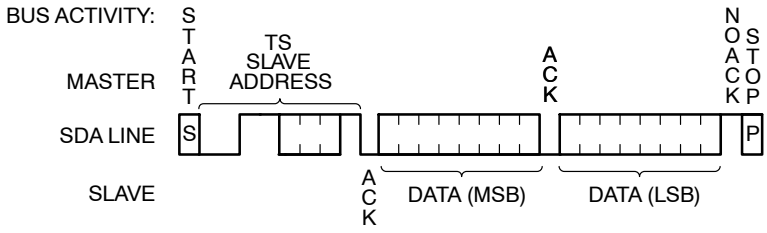


Figure 10b. Temperature Sensor Immediate Read

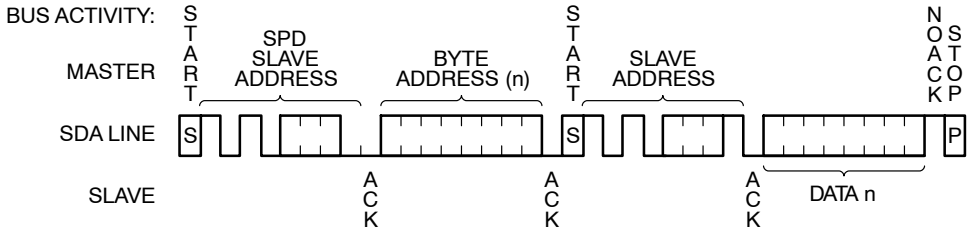


Figure 11a. EEPROM Selective Read

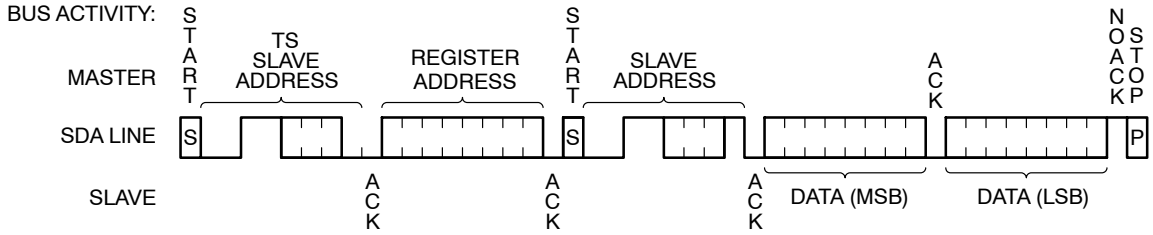


Figure 11b. Temperature Sensor Selective Read

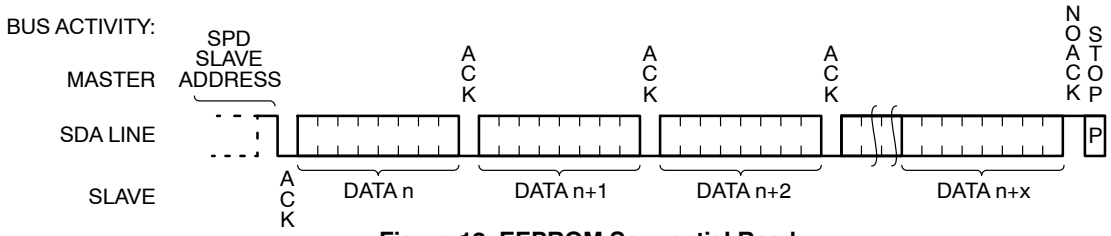


Figure 12. EEPROM Sequential Read

Software Write Protection

Each 1−Kb memory block can be individually protected against Write requests. Block identities are:

Block 0: byte address 0x00...0x7F (SPD page address = 0)
Block 1: byte address 0x80...0xFF (SPD page address = 0)
Block 2: byte address 0x00...0x7F (SPD page address = 1)
Block 3: byte address 0x80...0xFF (SPD page address = 1)

Block Software Write Protection (SWP) flags can be set or cleared in the presence of a very high voltage V_{HV} on address pin A0. The V_{HV} condition must be established on pin A0 before the START and maintained just beyond the STOP. The D.C. OPERATING CONDITIONS for SWP operations are shown in Table 8.

SWP command details are listed in Tables 9a and 9b.

SWP Slave addresses follow the standard I^2C convention, i.e. to read the state of a SWP flag, the LSB of the Slave address must be '1', and to set or clear a flag, it must be '0'. For Set/Clear commands a dummy byte address and dummy data byte must be provided (Figure 13). In contrast to a regular memory Read, a SWP Read does not return data. Instead the N34TS04 will respond with NoACK if the flag is set and with ACK if the flag is not set (Figure 14).

Table 8. SWPn AND CWP D.C. OPERATION CONDITION

Symbol	Parameter	Test Conditions	Min	Max	Units
ΔV_{HV}	A_0 Overdrive (V_{HV} − V_{CC})	1.7 V < V_{CC} < 3.6 V	4.8		V
I_{HVD}	A_0 High Voltage Detector Current			0.1	mA
V_{HV}	A_0 Very High Voltage		7	10	V

Table 9a. SWP SET COMMAND DETAIL

Command	Block(x) Protection	Slave Response	Address Byte	Slave Response	Data Byte	Slave Response	Write Cycle
SWPx(Note 11)	Not Set	ACK	(Dummy)	ACK	(Dummy)	ACK	Yes
	Set	NoACK	(Dummy)	NoACK	(Dummy)	NoACK	No
CWP	X	ACK	(Dummy)	ACK	(Dummy)	ACK	Yes

Table 9b. SWP QUERRY COMMAND DETAIL

Command	Block(x) Protection	Slave Response	Data Byte	Master (Response)	Data Byte	Master (Response)	
RPSx (Nots 11, 12)	Not Set	ACK	Dummy	(NoACK)	Dummy	(NoACK)	
	Set	NoACK	Dummy	(NoACK)	Dummy	(NoACK)	

Table 9c. SPD PAGE SELECT COMMAND DETAIL

Command	SPD Active Page	Slave Response	Address Byte	Slave Response	Data Byte	Slave Response	Write Cycle
SPAx (Notes 13, 14)	X	ACK	(Dummy)	ACK	(Dummy)	NoACK	No

Table 9d. SPD ACTIVE PAGE QUERRY COMMAND DETAIL

Command	SPD Active Page	Slave Response	Data Byte	Master (Response)	Data Byte	Master (Response)	
RPA (Notes 11, 12, 15)	0	ACK	Dummy	(NoACK)	Dummy	(NoACK)	
	1	NoACK	Dummy	(NoACK)	Dummy	(NoACK)	

11. The Master can terminate the sequence by issuing a STOP once the N34TS04 responds with NoACK
12. The Master can terminate the sequence by responding with (NoACK) followed by STOP after any dummy data byte.
13. Setting the SPD Page Address to ‘0’ selects the lower 2−Kb EEPROM bank, setting it to ‘1’ selects the upper 2−Kb EEPROM bank.
14. The lower 2−Kb EEPROM bank (corresponding to SPD page address ‘0’) is active (visible) immediately following power−up.
15. The device will respond with ACK when the lower 2−Kb EEPROM bank is active and with NoACK when the upper 2−Kb EEPROM bank is active.

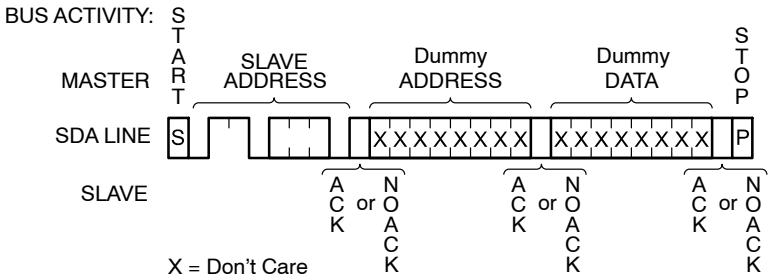


Figure 13. SWP & SPA Timing

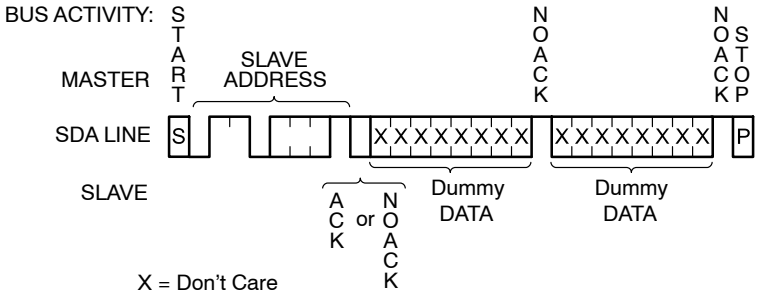


Figure 14. RPS & RPA Timing

Temperature Sensor Operation

The TS component in the N34TS04 combines a Proportional to Absolute Temperature (PTAT) sensor with a Σ−Δ modulator, yielding a 12 bit plus sign digital temperature representation.

The TS runs on an internal clock, and starts a new conversion cycle at least every 100 ms. The result of the most recent conversion is stored in the **Temperature Data Register (TDR)**, and remains there following a TS Shut−Down. Reading from the **TDR** does not interfere with the conversion cycle.

The value stored in the **TDR** is compared against limits stored in the **High Limit Register (HLR),** the **Low Limit Register (LLR)** and/or **Critical Temperature Register (CTR)**. If the measured value is outside the alarm limits or above the critical limit, then the $\overline{\text{EVENT}}$ pin may be asserted. The $\overline{\text{EVENT}}$ output function is programmable, via the **Configuration Register** for interrupt mode, comparator mode and polarity.

The temperature limit registers can be Read or Written by the host, via the serial interface. At power−on, all the (writable) internal registers default to 0x0000, and should therefore be initialized by the host to the desired values. The $\overline{\text{EVENT}}$ output starts out disabled (corresponding to polarity active low); thus preventing irrelevant event bus activity before the limit registers are initialized. While the TS is enabled (not shut−down), event conditions are normally generated by a change in measured temperature as recorded in the TDR, but limit changes can also trigger events as soon as the new limit creates an event condition, i.e. asynchronously with the temperature sampling activity.

In order to minimize the thermal resistance between sensor and PCB, it is recommended that the exposed backside die attach pad (DAP) be soldered to the PCB ground plane.

Registers

The N34TS04 contains eight 16−bit wide registers allocated to TS functions, as shown in Table 10. Upon power−up, the internal address counter points to the capability register.

Capability Register (User Read Only)

This register lists the capabilities of the TS, as detailed in the corresponding bit map.

Configuration Register (Read/Write)

This register controls the various operating modes of the TS, as detailed in the corresponding bit map.

Temperature Trip Point Registers (Read/Write)

The N34TS04 features 3 temperature limit registers, the **HLR**, **LLR** and **CLR** mentioned earlier. The temperature value recorded in the **TDR** is compared to the various limit values, and the result is used to activate the $\overline{\text{EVENT}}$ pin. To avoid undesirable $\overline{\text{EVENT}}$ pin activity, this pin is automatically disabled at power−up to allow the host to initialize the limit registers and the converter to complete the first conversion cycle under nominal supply conditions. Data format is two's complement with the LSB representing 0.25°C, as detailed in the corresponding bit maps.

Temperature Data Register (User Read Only)

This register stores the measured temperature, as well as trip status information. B15, B14, and B13 are the trip status bits, representing the relationship between measured temperature and the 3 limit values; these bits are not affected by EVENT status or by Configuration register settings regarding $\overline{\text{EVENT}}$ pin. Measured temperature is represented by bits B12 to B0. Data format is two's complement, where B12 represents the sign, B11 represents 128°C, etc. and B0 represents 0.0625°C.

Manufacturer ID Register (Read Only)

The manufacturer ID assigned by the PCI−SIG trade organization to the N34TS04 device is fixed at 0x1B09.

Device ID and Revision Register (Read Only)

This register contains manufacturer specific device ID and device revision information.

Table 10. THE TS REGISTERS

Register Address	Register Name	Power−On Default	Read/Write
0x00	Capability Register	0x007F	Read
0x01	Configuration Register	0x0000	Read/Write
0x02	High Limit Register	0x0000	Read/Write
0x03	Low Limit Register	0x0000	Read/Write
0x04	Critical Limit Register	0x0000	Read/Write
0x05	Temperature Data Register	Undefined	Read
0x06	Manufacturer ID Register	0x1B09	Read
0x07	Device ID/Revision Register	0x2230	Read

Table 11. CAPABILITY REGISTER

B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
RFU (Note 16)	RFU	RFU	RFU	RFU	RFU	RFU	RFU
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
EVSD	TMOUT	VHV	TRES [1:0]		RANGE	ACC	EVENT

16. RFU stands for Reserved for Future Use

Bit	Description
B15:B8	Reserved for future use; can not be written; should be ignored; will read as 0
B7 (Note 17)	0: Configuration Register bit 4 is frozen upon Configuration Register bit 8 being set (i.e. a TS shut−down freezes the $\overline{\text{EVENT}}$ output) 1: Configuration Register bit 4 is cleared upon Configuration Register bit 8 being set (i.e. a TS shut−down de−asserts the $\overline{\text{EVENT}}$ output)
B6	0: Not used 1: The TS implements SMBus time−out within the range 25 to 35 ms
B5	0: Not used 1: Defined for compatibility with CAT34TS02 device (V_{HV} is supported)
B4:B3	00: LSB = 0.50°C (9 bit resolution) 01: LSB = 0.25°C (10 bit) 10: LSB = 0.125°C (11 bit) 11: LSB = 0.0625°C (12 bit)
B2	0: Not used 1: The temperature monitor can read temperatures below 0°C and sets the sign bit appropriately
B1	0: Not used 1: The temperature monitor has ±1°C accuracy over the active range (75°C to 95°C) and ±2°C accuracy over the monitoring range (40°C to 125°C)
B0	0: Not used 1: The device supports interrupt capabilities

17. Configuration Register bit 4 can be cleared (but not set) after Configuration Register bit 8 is set, by writing a “1” to Configuration Register bit 5 ($\overline{\text{EVENT}}$ output can be de−asserted during TS shut−down periods)

Table 12. CONFIGURATION REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
RFU	RFU	RFU	RFU	RFU	HYST [1:0]		SHDN
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
TCRIT_LOCK	ALARM_LOCK	CLEAR	EVENT_STS	EVENT_CTRL	TCRIT_ONLY	EVENT_POL	EVENT_MODE

Bit	Description
B15:B11	Reserved for future use; can not be written; should be ignored; will read as 0
B10:B9 (Note 18)	00: Disable hysteresis 01: Set hysteresis at 1.5°C 10: Set hysteresis at 3°C 11: Set hysteresis at 6°C
B8 (Note 22)	0: Thermal Sensor is enabled; temperature readings are updated at sampling rate 1: Thermal Sensor is shut down; temperature reading is frozen to value recorded before SHDN
B7 (Note 21)	0: Critical trip register can be updated 1: Critical trip register cannot be modified; this bit can be cleared only at POR
B6 (Note 21)	0: Alarm trip registers can be updated 1: Alarm trip registers cannot be modified; this bit can be cleared only at POR
B5 (Note 20)	0: Always reads as 0 (self−clearing) 1: Writing a 1 to this position clears an event recording in interrupt mode only
B4 (Note 19)	0: EVENT output pin is not being asserted 1: EVENT output pin is being asserted
B3 (Note 18)	0: EVENT output disabled; *polarity dependent*: open−drain for **B1** = 0; grounded for **B1** = 1 1: EVENT output enabled
B2 (Note 24)	0: event condition triggered by alarm or critical temperature limit crossing 1: event condition triggered by critical temperature limit crossing only
B1 (Notes 18, 23)	0: EVENT output active low 1: EVENT output active high
B0 (Note 18)	0: Comparator mode 1: Interrupt mode

18. Can not be altered (set or cleared) as long as either one of the two lock bits, B6 or B7 is set.
19. This bit is a *polarity independent* 'software' copy of the $\overline{\text{EVENT}}$ pin, i.e. it is under the control of B3. This bit is read−only.
20. Writing a '1' to this bit clears an event condition in Interrupt mode, but has no effect in comparator mode. When read, this bit always returns 0. Once the measured temperature exceeds the critical limit, setting this bit has no effect (see Figure 15).
21. Cleared at power−on reset (POR). Once set, this bit can only be cleared by a POR condition.
22. The TS powers up into active mode, i.e. this bit is cleared at power−on reset (POR). When the TS is shut down the ADC is disabled and the temperature reading is frozen to the most recently recorded value. The TS can not be shut down (B8 can not be set) as long as either one of the two lock bits, B6 or B7 is set. However, the bit can be cleared at any time.
23. The $\overline{\text{EVENT}}$ output is "open−drain" and requires an external pull−up resistor for either polarity. The "natural" polarity is "active low", as it allows "wired−or" operation on the EVENT bus.
24. Can not be set as long as lock bit B6 is set.

Table 13. HIGH LIMIT REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	0

Table 14. LOW LIMIT REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	0

Table 15. TCRIT LIMIT REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	0

Table 16. TEMPERATURE DATA REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
TCRIT	HIGH	LOW	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C (Note 25)	0.125°C (Note 25)	0.0625°C (Note 25)

25. When supported – as defined by Capability Register bits TRES (1:0); unsupported bits will read as 0

Bit	Description
B15	0: Temperature is below the TCRIT limit 1: Temperature is equal to or above the TCRIT limit
B14	0: Temperature is equal to or below the High limit 1: Temperature is above the High limit
B13	0: Temperature is equal to or above the Low limit 1: Temperature is below the Low limit
B12	0: Positive temperature 1: Negative temperature

Register Data Format

The values used in the temperature data register and the 3 temperature trip point registers are expressed in two's complement format. The measured temperature value is expressed with 12−bit resolution, while the 3 trip temperature limits are set with 10−bit resolution. The total temperature range is arbitrarily defined as 256°C, thus yielding an LSB of 0.0625°C for the measured temperature and 0.25°C for the 3 limit values. Bit B12 in all temperature registers represents the sign, with a '0' indicating a positive, and a '1' a negative value. In two's complement format, negative values are obtained by complementing their positive counterpart and adding a '1', so that the sum of opposite signed numbers, but of equal absolute value, adds up to zero.

Note that trailing '0' bits, are '0' irrespective of polarity. Therefore the don't care bits (B1 and B0) in the 10−bit resolution temperature limit registers, are always '0'.

Table 17. 12−BIT TEMPERATURE DATA FORMAT

Binary (B12 to B0)	Hex	Temperature
1 1100 1001 0000	1C90	−55°C
1 1100 1110 0000	1CE0	−50°C
1 1110 0111 0000	1E70	−25°C
1 1111 1111 1111	1FFF	−0.0625°C
0 0000 0000 0000	000	0°C
0 0000 0000 0001	001	+0.0625°C
0 0001 1001 0000	190	+25°C
0 0011 0010 0000	320	+50°C
0 0111 1101 0000	7D0	+125°C

Event Pin Functionality

The $\overline{\text{EVENT}}$ output reacts to temperature changes as illustrated in Figure 15, and according to the operating mode defined by the Configuration register.

In **Interrupt Mode**, the (enabled) $\overline{\text{EVENT}}$ output will be asserted every time the temperature crosses one of the alarm window limits, and can be de−asserted by writing a '1' to the clear event bit (B5) in the configuration register. Once the temperature exceeds the critical limit, the $\overline{\text{EVENT}}$ remains asserted as long as the temperature stays above the critical limit and cannot be cleared. A clear request sent to the N34TS04 while the temperature is above the critical limit will be acknowledged, but will be executed only after the temperature drops below the critical limit.

In **Comparator Mode**, the $\overline{\text{EVENT}}$ output is asserted outside the alarm window limits, while in **Critical Temperature Mode**, $\overline{\text{EVENT}}$ is asserted only above the critical limit. Clear requests are ignored in this mode. The exact trip limits are determined by the 3 temperature limit settings and the hysteresis offsets, as illustrated in Figure 16.

Following a TS shut−down request, the converter is stopped and the most recently recorded temperature value present in the TDR is frozen; the $\overline{\text{EVENT}}$ output will continue to reflect the state immediately preceding the shut−down command. Therefore, if the state of the $\overline{\text{EVENT}}$ output creates an undesirable bus condition, appropriate action must be taken either before or after shutting down the TS. This may require clearing the event, disabling the $\overline{\text{EVENT}}$ output or perhaps changing the $\overline{\text{EVENT}}$ output polarity.

In normal use, events are triggered by a change in recorded temperature, but the N34TS04 will also respond to limit register changes. Whereas recorded temperature values are updated at sampling rate frequency, limits can be modified at any time. The enabled $\overline{\text{EVENT}}$ output will react to limit changes as soon as the respective registers are updated. This feature may be useful during testing.

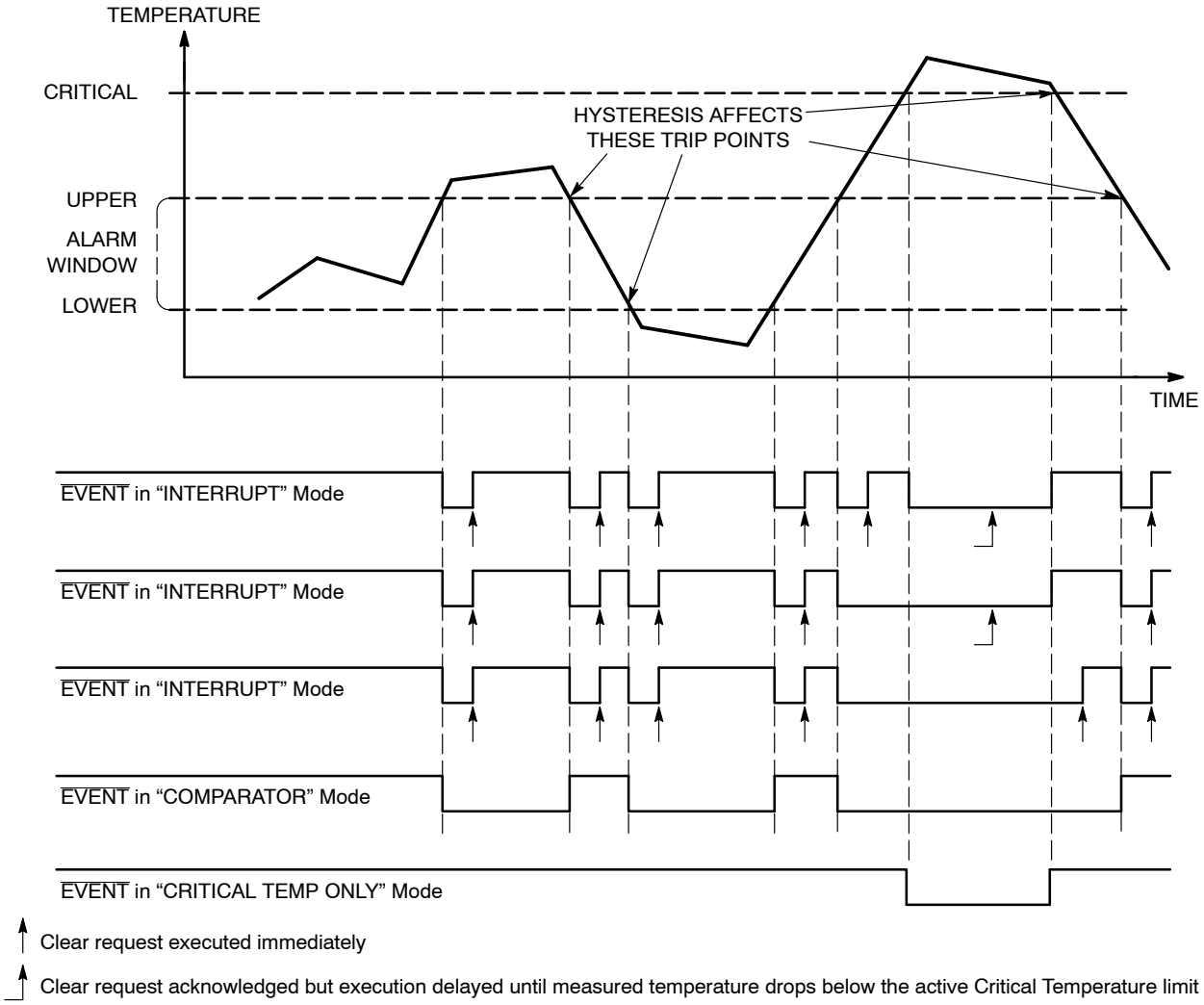


Figure 15. Event Detail

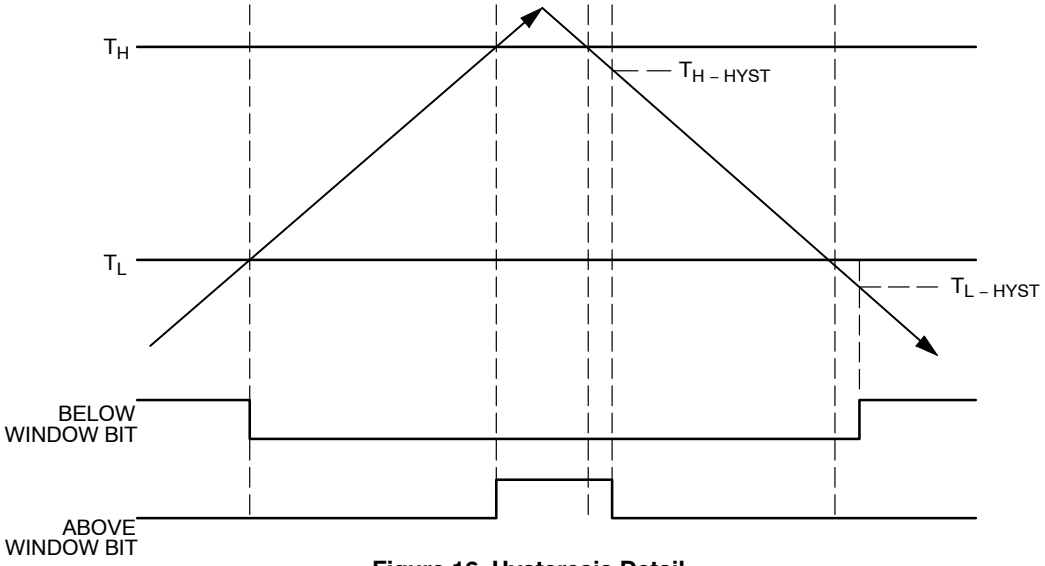


Figure 16. Hysteresis Detail

Example of Ordering Information

Device Order Number	Specific Device Marking	Package Type	Lead Finish	Shipping	Device Revision
N34TS04MT3ETG	T34	TDFN8	NiPdAu	Tape & Reel, 4,000 Units / Reel	A
N34TS04MU3ETG	U34	UDFN8	NiPdAu	Tape & Reel, 4,000 Units / Reel	A

26. All packages are RoHS−compliant (Lead−free, Halogen−free)
27. The standard lead finish is NiPdAu.
28. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

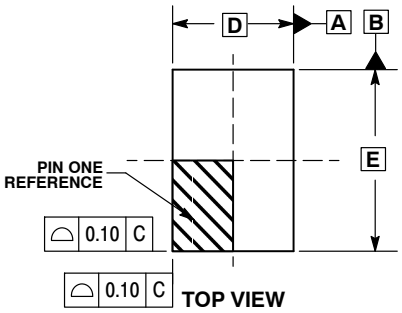
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

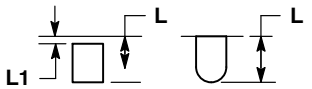
ON Semiconductor®

SCALE 2:1

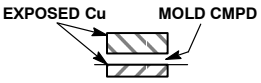
TDFN8, 2x3, 0.5P
CASE 511AK
ISSUE B

DATE 18 MAR 2015

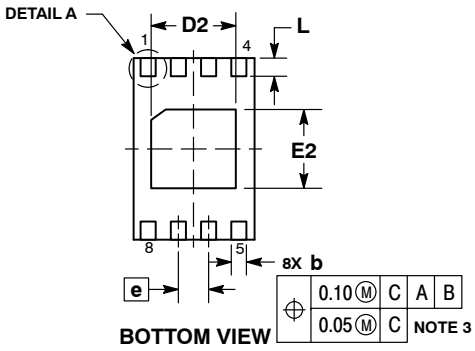




DETAIL A
ALTERNATE CONSTRUCTIONS



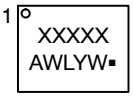
DETAIL B
ALTERNATE CONSTRUCTION



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.30	1.50
E	3.00 BSC	
E2	1.20	1.40
e	0.50 BSC	
L	0.20	0.40
L1	---	0.15

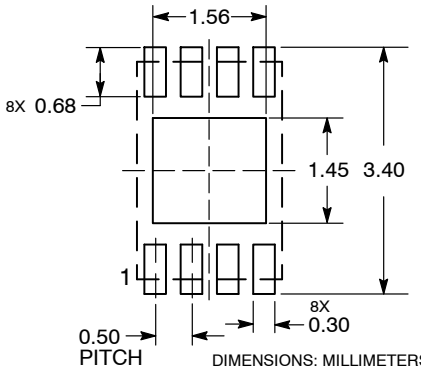
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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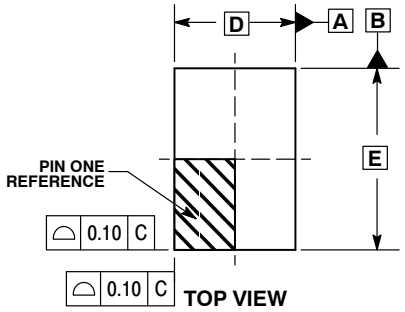
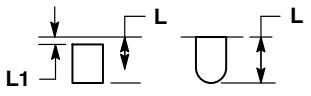
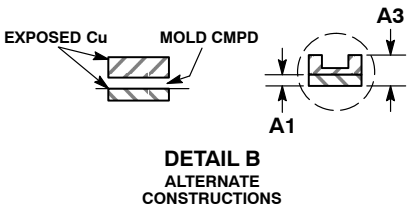
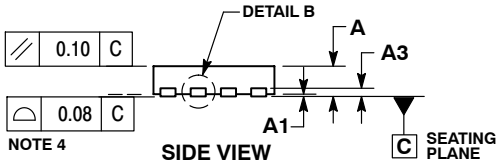
UDFN8, 2x3 EXTENDED PAD
CASE 517AZ
ISSUE A

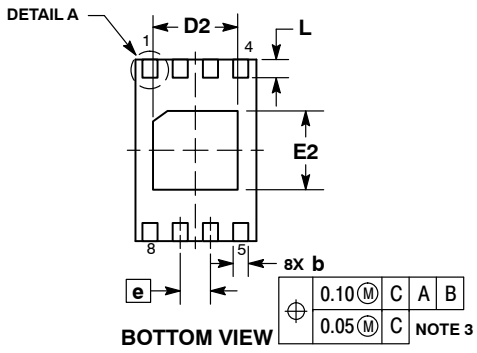
DATE 23 MAR 2015











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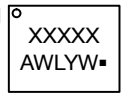
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.35	1.45
E	3.00 BSC	
E2	1.25	1.35
e	0.50 BSC	
L	0.25	0.35
L1	---	0.15

GENERIC MARKING DIAGRAM*



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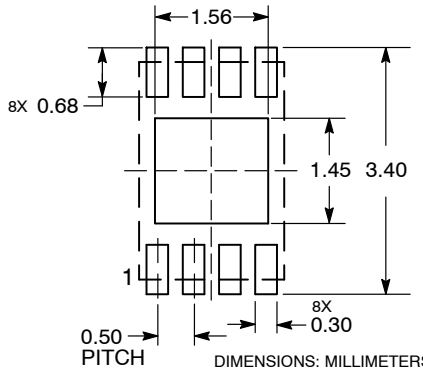

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