DisplayPort Intel® Agilex™ F-Tile FPGA IP Design Example User Guide

Updated for Intel® Quartus® Prime Design Suite: **21.4**

IP Version: **21.0.0**

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1. DisplayPort Intel FPGA IP Design Example Quick Start Guide

The DisplayPort Intel® FPGA IP design examples for Intel Agilex™ F-tile devices feature a simulating testbench and a hardware design that supports compilation and hardware testing

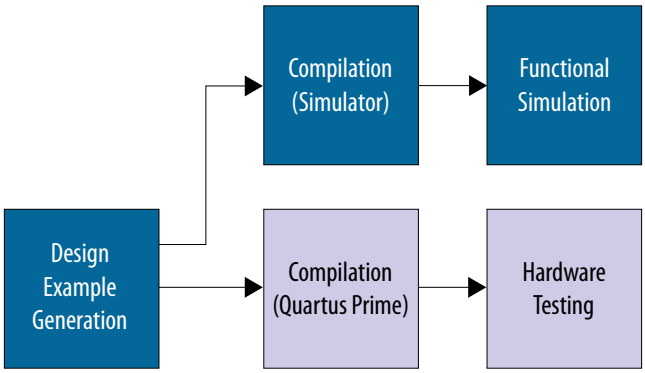
The DisplayPort Intel FPGA IP offers the following design examples:

- DisplayPort SST parallel loopback without a Pixel Clock Recovery (PCR) module at static rate

When you generate a design example, the parameter editor automatically creates the files necessary to simulate, compile, and test the design in hardware.

Note: Intel Quartus® Prime 21.4 software version only supports Preliminary Design Example for Simulation, Synthesis, Compilation, and Timing analysis purposes. Hardware functionality is not fully verified.

Figure 1. Development Stages



Related Information

- DisplayPort Intel FPGA IP User Guide
- Migrating to Intel Quartus Prime Pro Edition

1.1. Directory Structure

Figure 2. Directory Structure

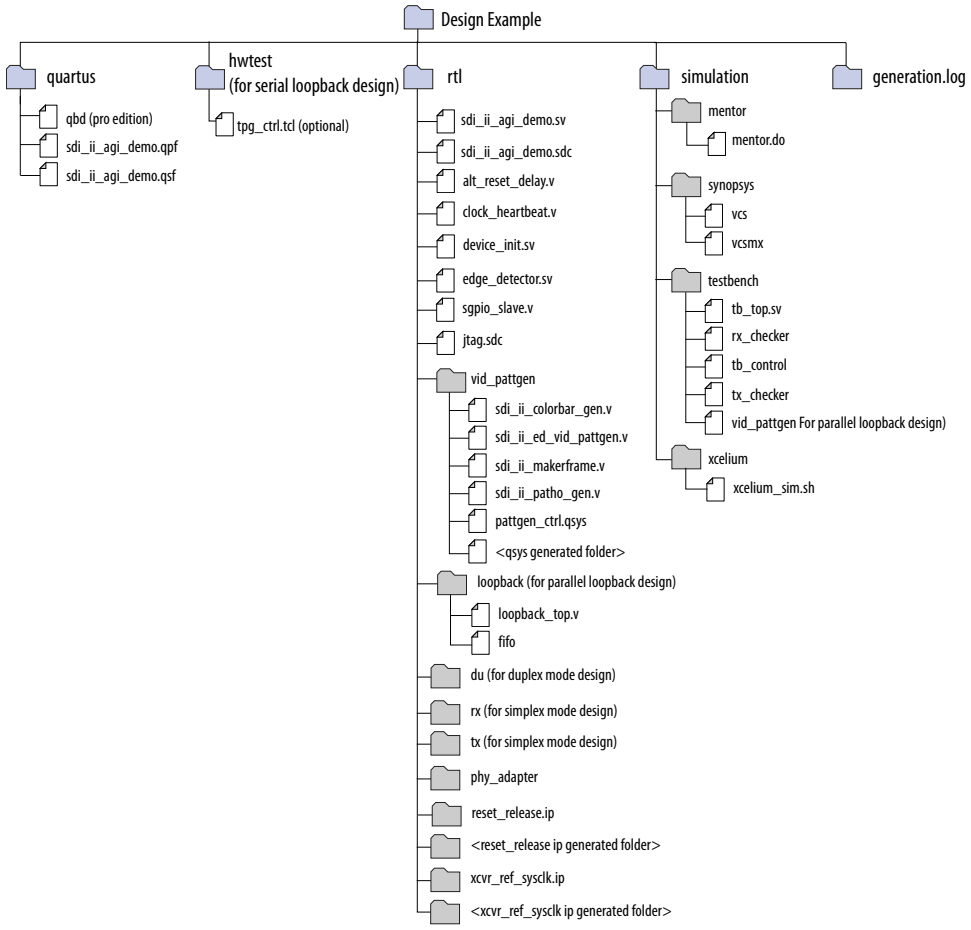


Table 1. Design Example Components

Folders	Files
rtl/core	dp_core.ip
	dp_rx.ip
	dp_tx.ip
rtl/rx_phy	dp_gxb_rx/ ((DP PMA UX building block)
	dp_rx_data_fifo.ip
	rx_top_phy.sv
rtl/tx_phy	dp_gxb_rx/ ((DP PMA UX building block)
	dp_tx_data_fifo.ip
	dp_tx_data_fifo.ip

1.2. Hardware and Software Requirements

Intel uses the following hardware and software to test the design example:

Hardware

- Intel Agilex I-Series Development Kit

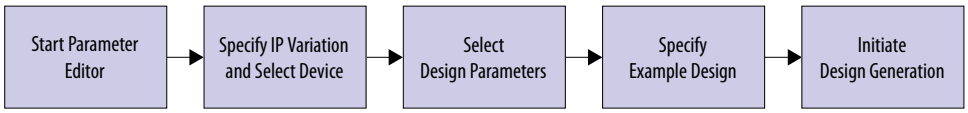
Software

- Intel Quartus Prime
- Synopsys* VCL Simulator

1.3. Generating the Design

Use the DisplayPort Intel FPGA IP parameter editor in Intel Quartus Prime software to generate the design example.

Figure 3. Generating the Design Flow



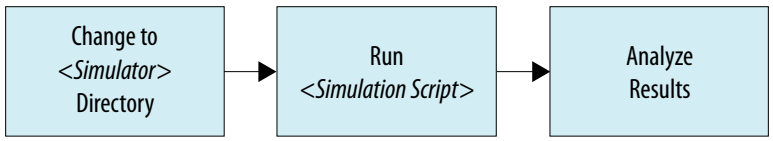
1. Select **Tools ➤ IP Catalog**, and select Intel Agilex F-tile as the target device family.

   Note: The design example only supports Intel Agilex F-tile devices.
2. In the IP Catalog, locate and double-click **DisplayPort Intel FPGA IP**. The **New IP Variation** window appears.
3. Specify a top-level name for your custom IP variation. The parameter editor saves the IP variation settings in a file named <your_ip>.ip.
4. You may select a specific Intel Agilex F-tile device in the **Device** field, or keep the default Intel Quartus Prime software device selection.
5. Click OK. The parameter editor appears.
6. Configure the desired parameters for both TX and RX
7. On the Design Example tab, select **DisplayPort SST Parallel Loopback Without PCR**.
8. Select **Simulation** to generate the testbench, and select **Synthesis** to generate the hardware design example. You must select at least one of these options to generate the design example files. If you select both, the generation time is longer.
9. Click **Generate Example Design**.

1.4. Simulating the Design

The DisplayPort Intel FPGA IP design example testbench simulates a serial loopback design from a TX instance to an RX instance. An internal video pattern generator module drives the DisplayPort TX instance and the RX instance video output connects to CRC checkers in the testbench.

Figure 4. Design Simulation Flow



1. Go to Synopsys simulator folder and select VCS.
2. Run simulation script.

```
Source vcs_sim.sh
```

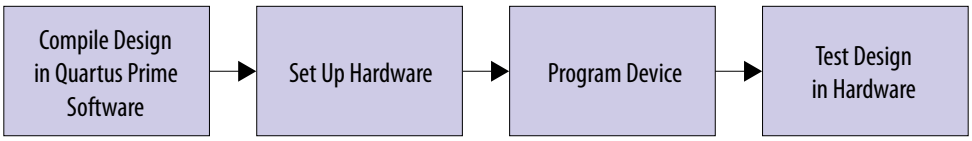
3. The script performs Quartus TLG, compiles and run the testbench in the simulator.
4. Analyze the result.

A successful simulation ends with Source and Sink SRC comparison.

```
# SINK CRC_R = ac9c, CRC_G = ac9c, CRC_B = ac9c,
# SOURCE CRC_R = ac9c, CRC_G = ac9c, CRC_B = ac9c,
# Pass: Test Completed
```

1.5. Compiling and Simulating the Design

Figure 5. Compiling and Simulating the Design



To compile and run a demonstration test on the hardware example design, follow these steps:

1. Ensure hardware example design generation is complete.
2. Launch the Intel Quartus Prime Pro Edition software and open `<project>/quartus/agi_dp_demo.qpf`.
3. Click **Processing ➤ Start Compilation**.
4. Wait until **Compilation** completes.

   Note: The design example does not functionally verify Preliminary Design Example on hardware in this Quartus release.

Related Information

Intel Agilex I-Series FPGA Development Kit User Guide

1.6. DisplayPort Intel FPGA IP Design Example Parameters

Table 2. DisplayPort Intel FPGA IP Design Example Parameters for Intel Agilex F-tile Device

Parameter	Value	Description
Available Design Example		
Select Design	• None • DisplayPort SST Parallel Loopback without PCR	Select the design example to be generated. • None: No design example is available for the current parameter selection • DisplayPort SST Parallel Loopback without PCR: This design example demonstrates parallel loopback from DisplayPort sink to DisplayPort source without a Pixel Clock Recovery (PCR) module when you turn on the **Enable Video Input Image Port parameter**.
Design Example Files		
Simulation	On, Off	Turn on this option to generate the necessary files for the simulation testbench.
Synthesis	On, Off	Turn on this option to generate the necessary files for Intel Quartus Prime compilation and hardware design.
Generated HDL Format		
Generate File Format	Verilog, VHDL	Select your preferred HDL format for the generated design example fileset. *Note:* This option only determines the format for the generated top level IP files. All other files (e.g. example testbenches and top level files for hardware demonstration) are in Verilog HDL format.
Target Development Kit		
Select Board	• No Development Kit • Intel Agilex I-Series Development Kit	Select the board for the targeted design example. • No Development Kit: This option excludes all hardware aspects for the design example. The IP core sets all pin assignments to virtual pins. • Intel Agilex I-Series FPGA Development Kit: This option automatically selects the project's target device to match the device on this development kit. You may change the target device using the **Change Target Device** parameter if your board revision has a different device variant. The IP core sets all pin assignments according to the development kit. *Note:* Preliminary Design Example is not functionally verified on hardware in this Quartus release. • Custom Development Kit: This option allows the design example to be tested on a third-party development kit with an Intel FPGA. You may need to set the pin assignments on your own.
Target Device		
Change Target Device	On, Off	Turn on this option and select the preferred device variant for the development kit.

2. Parallel Loopback Design Examples

The DisplayPort Intel FPGA IP design examples demonstrate parallel loopback from DisplayPort RX instance to DisplayPort TX instance without a Pixel Clock Recovery (PCR) module at static rate.

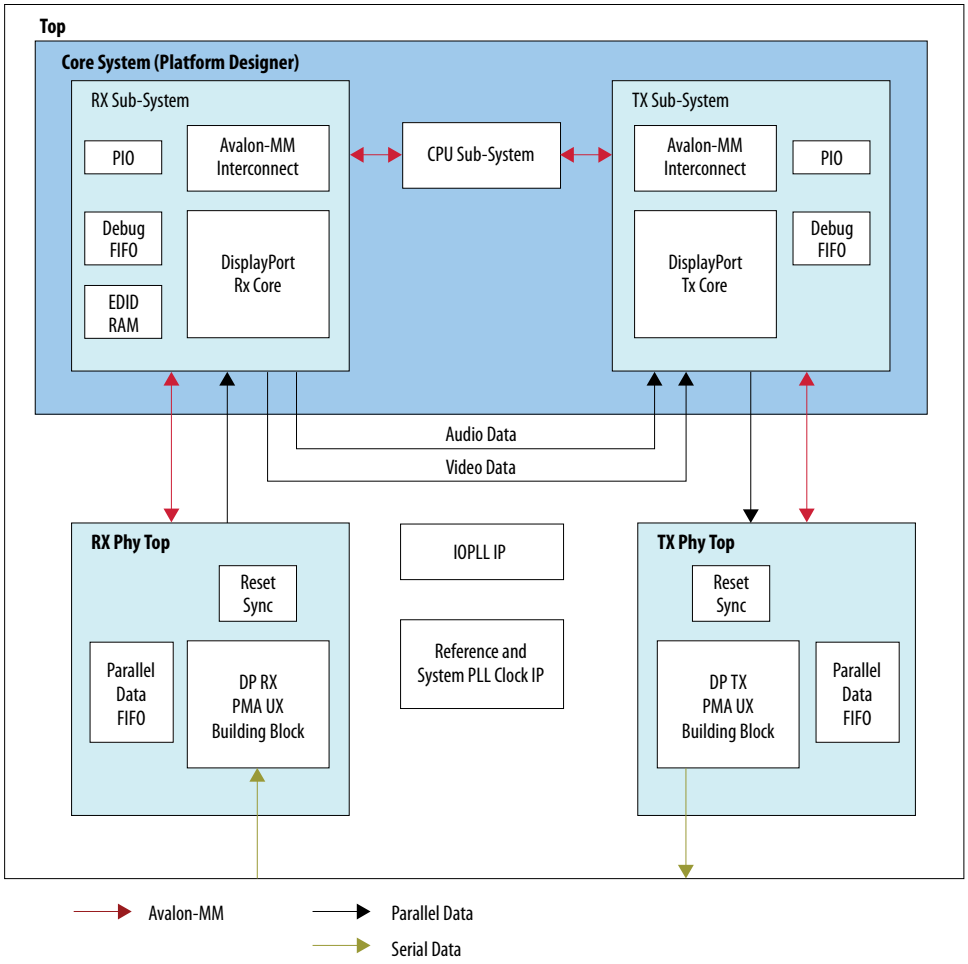
Table 3. DisplayPort Intel FPGA IP Design Example for Intel Agilex F-tile Device

Design Example	Designation	Data Rate	Channel Mode	Loopback Type
DisplayPort SST parallel loopback without PCR	DisplayPort SST	HBR3	Simplex	Parallel without PCR

2.1. Intel Agilex F-tile DisplayPort SST Parallel Loopback Design Features

The SST parallel loopback design examples demonstrate the transmission of a single video stream from DisplayPort sink to DisplayPort source without Pixel Clock Recovery (PCR) at static rate.

Figure 6. Intel Agilex F-tile DisplayPort SST Parallel Loopback without PCR



- In this variant, the DisplayPort source's parameter, **TX_SUPPORT_IM_ENABLE**, is turned on and the video image interface is used.
- The DisplayPort sink receives video and or audio streaming from external video source such as GPU and decodes it into parallel video interface.
- The DisplayPort sink video output directly drives the DisplayPort source video interface and encodes to the DisplayPort main link before transmitting to the monitor.
- The IOPLL drives both the DisplayPort sink and source video clocks at a fixed frequency.
- If DisplayPort sink and source's **MAX_LINK_RATE** parameter is configured to **HBR3** and **PIXELS_PER_CLOCK** is configured to **Quad**, the video clock runs at 300 MHz to support 8Kp30 pixel rate (1188/4 = 297 MHz).

2.2. Clocking Scheme

The clocking scheme illustrates the clock domains in the DisplayPort Intel FPGA IP design example.

Figure 7. Intel Agilex F-tile DisplayPort Transceiver clocking scheme

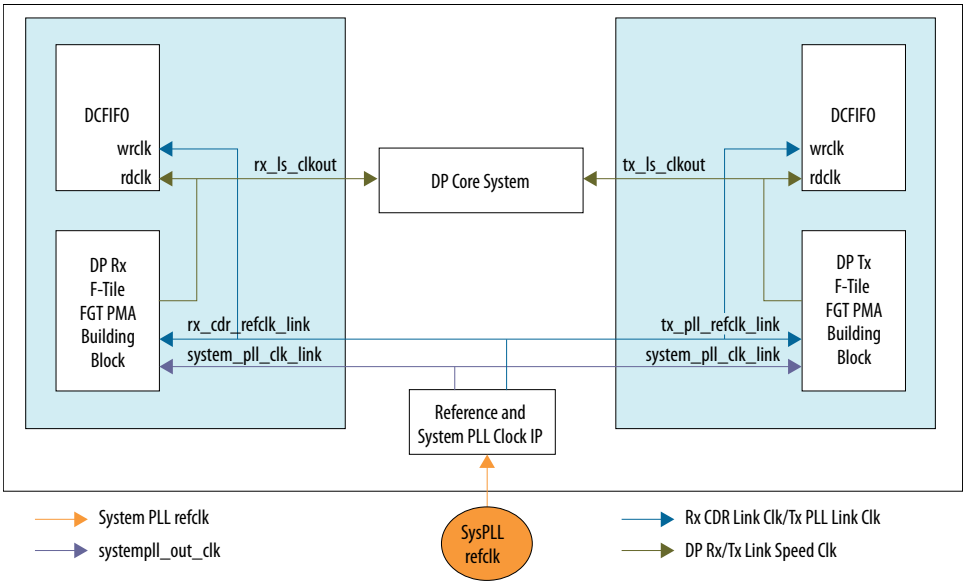


Table 4. Clocking Scheme Signals

Clock in diagram	Description
SysPLL refclk	F-tile System PLL reference clock which can be any clock frequency that is dividable by System PLL for that output frequency. In this design example, system_pll_clk_link and rx/tx refclk_link is sharing same SysPLL refclk which is **150Mhz**. It must be a free running clock which is connected from a dedicated transceiver reference clock pin to the input clock port of Reference and System PLL Clocks IP, before connecting the corresponding output port to DisplayPort Phy Top.
system_pll_clk_link	The minimum System PLL output frequency to support all DisplayPort rate is 320Mhz. This design example uses **900 Mhz** (highest) output frequency so that SysPLL refclk can be shared with rx/tx refclk_link which is 150 Mhz.
rx_cdr_refclk_link / tx_pll_refclk_link	Rx CDR and Tx PLL Link refclk which fixed to **150 Mhz** to support all DisplayPort data rate.
rx_ls_clkout / tx_ls_clkout	DisplayPort Link Speed Clock to clock DisplayPort IP core. Frequency equivalent to Data Rate divide by parallel data width. Example: Frequency = data rate / data width = 8.1G (HBR3) / 40bits = 202.5 Mhz

2.3. Simulation Testbench

The simulation testbench simulates the DisplayPort TX serial loopback to RX.

Figure 8. DisplayPort Intel FPGA IP Simplex Mode Simulation Testbench Block Diagram

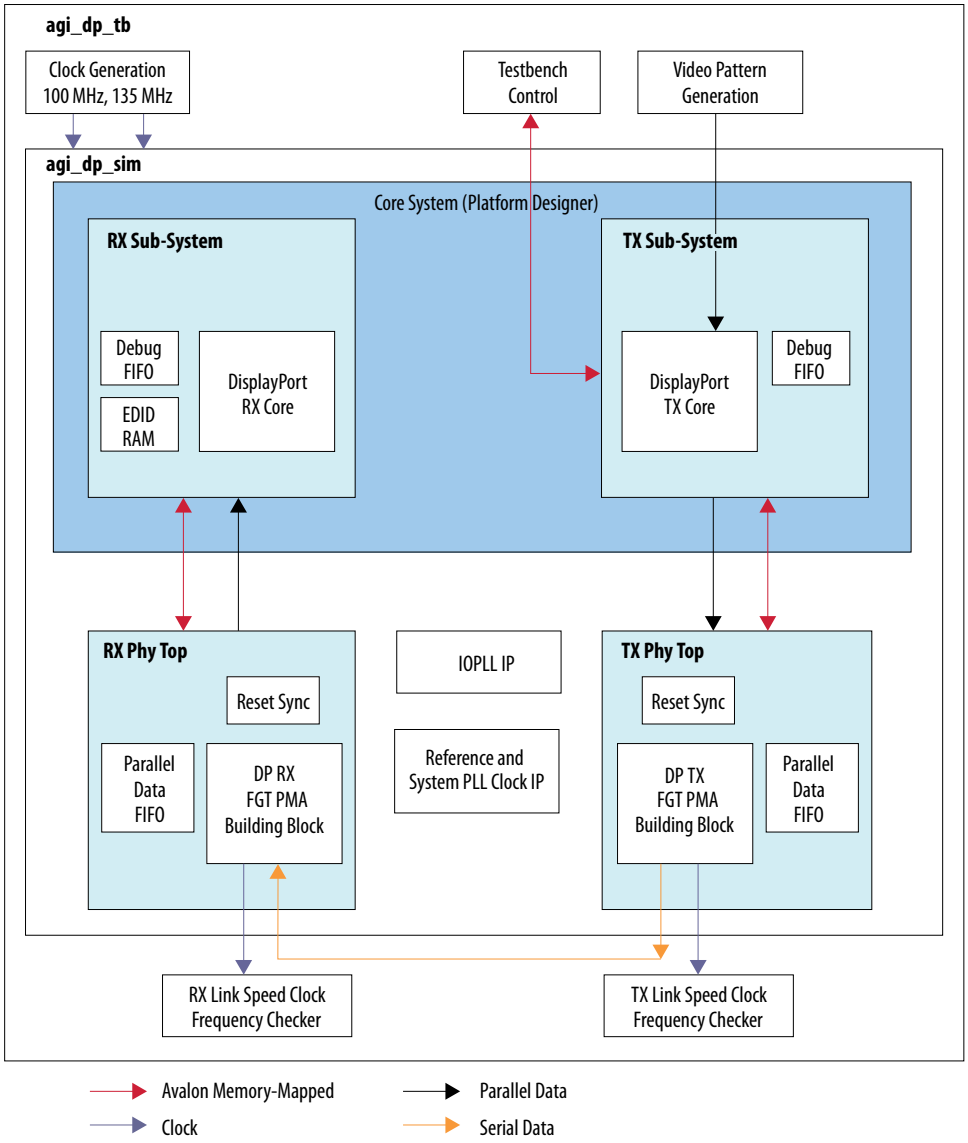


Table 5. Testbench Components

Component	Description
Video Pattern Generator	This generator produces color bar patterns that you can configure. You can parameterize the video format timing.
Testbench Control	This block controls the test sequence of the simulation and generates the necessary stimulus signals to the TX core. The testbench control block also reads the CRC value from both source and sink to make comparisons.
RX Link Speed Clock Frequency Checker	This checker verifies if the RX transceiver recovered clock frequency matches the desired data rate.
TX Link Speed Clock Frequency Checker	This checker verifies if the TX transceiver recovered clock frequency matches the desired data rate.

The simulation testbench does the following verifications:

Table 6. Testbench Verifications

Test Criteria	Verification
• Link Training at Data Rate HBR3 • Read the DPCD registers to check if the DP Status sets and measures both TX and RX Link Speed frequency.	Integrates Frequency Checker to measure the Link Speed clock's frequency output from the TX and RX transceiver.
• Run video pattern from TX to RX. • Verify the CRC for both source and sink to check if they match	• Connects video pattern generator to the DisplayPort Source to generate the video pattern. • Testbench control next reads out both Source and Sink CRC from DPTX and DPRX registers and compares to ensure both CRC values are identical. *Note:* To ensure CRC is calculated, you must enable the **Support CTS test automation** parameter.

3. Document Revision History for the DisplayPort Intel Agilex F-tile FPGA IP Design Example User Guide

Document Version	Intel Quartus Prime Version	IP Version	Changes
2021.12.13	21.4	21.0.0	Initial release.