

# Wireless Gecko™ EFR32FG28 Errata



This document contains information on the EFR32FG28 errata. The latest available revision of this device is revision A.

Errata that have been resolved remain documented and can be referenced for previous revisions of this device.

The device data sheet explains how to identify the chip revision, either from the package marking or electronically.

Errata effective date: June, 2025.

# 1. Errata Summary

The following table lists all the known and unresolved errata for the EFR32FG28.

Table 1.1. Errata Overview

Designator	Title/Problem	Workaround Exists	Exists on Revision
			Α
LCD_E301	LOADBUSY Status Goes Inactive Early With Prescaled Clock	Yes	Х
SE_E302	DPA Countermeasure Unavailable for Some Operations	Yes	Х
USART_E304	PRS Transmit Unavailable in Synchronous Secondary Mode	No	Х

# 2. Current Errata Descriptions

### 2.1 LCD\_E301 — LOADBUSY Status Goes Inactive Early With Prescaled Clock

## Description of Errata

The LCD\_STATUS\_LOADBUSY bit erroneously reports completion of writes to the LCD\_BACTRL, LCD\_AREGA, LCD\_AREGB, and LCD\_SEGDn registers before synchronization is complete when LCD\_CTRL\_PRESCALE > 3.

#### Affected Conditions / Impacts

If LOADBUSY is used to gate consecutive writes to one of the affected registers, only the data associated with the last write is guaranteed to be latched into the register.

#### Workaround

For each write to one of the affected registers, insert a delay equal to LCD\_CTRL\_PRESCALE  $\div$  f<sub>LCDCLK</sub> after LOADBUSY transitions from 1 to 0 before issuing the next write to the same register.

**Note:** LOADBUSY reports when data written from the PCLK register domain into the LCD controller's low-frequency clock domain has been synchronized. It does not indicate when data written into one of the affected registers is actually driven on the LCD controller pins.

In cases where writes to these registers, such as LCD\_SEGDn, are intended to have the change in pin state be observable on the connected display, LOADBUSY should not be used to gate consecutive writes. Instead, the CPU should issue the register write and wait to issue the next write until a display update event or frame counter update event occurs as reported by the LCD\_IF register DISPLAY or FC flag bits. Interrupts associated with these flags can and should be enabled in such cases to minimize energy use by keeping the CPU in a low-energy mode (e.g., EM2) between such consecutive register writes.

#### Resolution

There is currently no resolution for this issue.

#### 2.2 SE\_E302 - DPA Countermeasure Unavailable for Some Operations

# Description of Errata

Differential power analysis (DPA) countermeasures for ECDH on Curve25519, ECDH on Curve448, and EdDSA signing on Curve25519 are unavailable due to a lack of hardware support on all Series 2 devices with a Hardware Secure Engine (HSE).

#### Affected Conditions / Impacts

A successful DPA attack may be possible if the impacted algorithms are implemented in a customer's product. However, a DPA attack is not an easy/straightforward attack as it requires specific equipment, many traces, physical access to the device, and some control over device operation.

If a successful DPA attack occurs, an attacker may be able to gain access to confidential information, such as private keys or encrypted communications between devices.

#### Workaround

No fix is available to provide the affected DPA countermeasures on Series 2 devices. Refer to Security Advisory A-00000534 for mitigation recommendations, which include refreshing key pairs or using a key pair only once to reduce the risk of a successful DPA attack.

#### Resolution

There is currently no resolution for this issue.

# 2.3 USART\_E304 — PRS Transmit Unavailable in Synchronous Secondary Mode

### Description of Errata

When the USART is configured for synchronous secondary operation, the transmit output (MISO) is not driven if the signal is routed to a pin using the PRS producer (e.g., SOURCESEL = 0x20 and SIGSEL = 0x4 for USART0).

### Affected Conditions / Impacts

Systems cannot operate the USART in synchronous secondary mode if the PRS is used to route the transmit output to the RX (MISO) pin. Operation is not affected in main mode when the transmit output is routed to the TX (MOSI) pin using the PRS producer nor is operation affected in any mode when the GPIO\_USARTn\_RXROUTE and GPIO\_USARTn\_TXROUTE registers are used.

### Workaround

There is currently no workaround for this issue.

#### Resolution

There is currently no resolution for this issue.

# 3. Revision History

# Revision 0.2

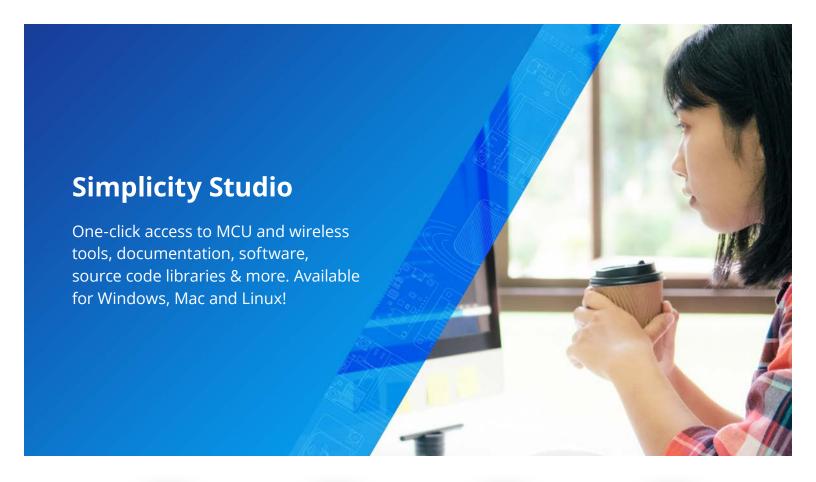
June, 2025

- Added SE\_E302.
- Added USART\_E304.

# Revision 0.1

February, 2023

· Initial release.





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