User Guide

BL653 Development Kit

Part # 453-00039-K1 and 453-00041-K1

Version 1.2

Revision History

Version	Date	Notes	Contributor(s)	Approver
1.0	25 March 2020	Initial version	Raj Khatri	Jonathan Kaye
1.1	14 December 2021	Updates to Table 5.	Raj Khatri	Erik Lins
1.2	7 Feb 2024	Corrected LED info in Table 13	Skofiar Kamberi	Raj Khatri

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1 Overview

The Laird BL653 Development Kit provides a platform for rapid wireless connectivity prototyping, providing multiple options for the development of Bluetooth Low Energy (BLE) plus Near Field Communication (NFC) applications.

The Laird BLE development kit is designed to support the rapid development of applications and software for the BL653 series of BLE modules featuring Laird's innovative event driven programming language – *smart*BASIC, At command set, Zephyr RTOS or for use with the Nordic SDK for C development. More information regarding this product series including a detailed module user's guide and *smart*BASIC user guides are available on Laird's BL653 product page: https://www.lairdconnect.com/wireless-modules/bluetooth-modules/bluetooth-5-modules/bl653-series-bluetooth-51-802154-nfc-module

This document is applicable to the version of development board which has PCB silk screen text DVK-BL653-2.0.

2 Laird BL653 Development Kit Part Numbers

Part Number	Product Description
453-00039-K1	Development kit for Bluetooth + 802.15.4 + NFC module – Integrated antenna
453-00041-K1	Development kit for Bluetooth + 802.15.4 + NFC module – Trace pin (external antenna)

Applicable to the following BL653 module part numbers:

Part Number	Product Description
453-00039	BLE module (Nordic nRF52833) – Integrated antenna
453-00041	BLE module (Nordic nRF52833) – Trace pin

3 Package Contents

All kits contain the following items:

Development Board	The development board has the required BL653 module soldered onto it and exposes all available hardware interfaces.
Power Options	▪ USB cable – Type A to micro type B. The cable also provides serial communications via the FTDI USB – RS232 converter chip on the board. ▪ DC barrel plug for connection to external power supply (5.5 VDC max) ▪ 3x AAA battery holder fitted on underside of development board ▪ Coin-cell holder (powers module only) fitted on underside of development board
Two-pin jumpers for pin headers (5)	Five jumpers for 2.54 mm pitch headers used on BL653 development board.
Fly leads (6)	Supplied (1 by 1 female to female jumper cable) to allow simple connection of any BL653 module pins (available on plated though holes or headers on J44, J47, J48, J41, J29, J1, J12, J1, J5, J17, J21, J6 and J36).
External BLE dipole antenna	Supplied with development kit part # 453-00041-K1 only. External antenna, 2 dBi, FlexPIFA (Laird part #001-0022) with integral RF coaxial cable with 100 mm length and IPEX-4 compatible RF connector.
External NFC antenna	Supplied with development kit part # 453-00041-K1 and #453-00039-K1 Laird NFC flexi-PCB antenna – Part # 0600-00061
Web link card	Provides links to additional information including the BL653 user guide, firmware, terminal utilities, schematics, quick start guides, firmware release notes, and more. **Note:** Sample *smart*BASIC applications are available to download from the Laird BL653 GitHub repository.

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4 BL653 Development Kit – Main Development Board

This section describes the BL653 development board hardware. The BL653 development board is delivered with the BL653 series module loaded with integrated *smart*BASIC runtime engine firmware but no onboard *smart*BASIC; because of this it starts up in AT command mode by default.

Applications in *smart*BASIC are simple and easy to develop for any BLE application. Sample *smart*BASIC applications scripts are available to download from the Laird GitHub repository on the BL653 product page at https://www.lairdconnect.com/wireless-modules/bluetooth-modules/bluetooth-5-modules/bl653-series-bluetooth-51-802154-nfc-module. The development board also can be used with Nordic SDK or Zephyr RTOS.

The BL653 development board is a universal development tool that highlights the capabilities of the BL653 module. The development kit is supplied in a default configuration which should be suitable for multiple experimentation options. It also offers several header connectors that help isolate on-board sensors and UART from the BL653 module to create different configurations. This allows you to test different operating scenarios.

The board allows the BL653 series module to physically connect to a PC via the supplied USB cable for development purposes. The development board provides USB-to-Virtual COM port conversion through a FTDI chip – part number FT232R. Any Windows PC (XP or later) should auto-install the necessary drivers; if your PC cannot locate the drivers, you can download them from http://www.ftdichip.com/Drivers/VCP.htm

4.1 Key Features

The BL653 development board has the following features:

- BL653 series module soldered onto the development board
- The following power supply options for powering the development board:
  - USB (micro-USB, type B)
  - External DC supply (3.5-5.5V)
  - AAA batteries (three AAA battery holder fitted on underside of development board)
  - USB (micro-USB, type B) –for direct use of BL653 USB interface as well
- Powering the BL653 module in Normal Voltage mode (OPTION1) via selection switch (SW7). Regulated 3.3V or Regulated 1.8V via selection switch (SW5).
- Powering the BL653 module in High Voltage mode (OPTION2) via selection switch (SW7). Regulated 2.5V or 4.5V (from 3x AAA battery – 4.5V) via selection switch (SW8). Option to inject external voltage anywhere between 3.5V to 5.5V for the High Voltage mode (via J28).
- Power supply option for coin-cell (CR2032) operation of the BL653 module *only* (not development board)
- USB to UART bridge (FTDI chip)
- BL653 UART can be interfaced to:
  - USB1 (PC) using the USB-UART bridge (FTDI chip)
  - External UART source (using IO break-out connectors J1 – No-Pop, Plated Through Holes) when the development board is powered from a DC jack or AAA batteries) or from USB1 (when jumper fitted in J35).
  - Atmel MCU by use of an analog switch to route the BL653 UART (for those customers working with Nordic SDK). USB2 to Atmel to Atmel UART (via open solderbridges) to BL653 UART.
- Current measuring options (BL653 module only):
  - Pin header (Ammeter)
  - 10R Series resistor for differential measurement (oscilloscope)
- IO break-out 2.54 mm pitch pin header connectors (plated through-holes) that bring out all interfaces of the BL653 module – UART, SPI, I2C, SIO [DIO or AIN (ADCs)], PWM, FREQ, NFC – and allow for plugging in external modules/sensors.
- Pin headers jumpers that allow the on-board sensors (I2C sensor, LEDs) to be disconnected from BL653 module (by removing jumpers).
- Four on-board sensors:
  - Analog output temperature sensor via header in series (no jumper by default)
  - I2C device (RTC chip U16) via headers in series (no jumper by default)
  - SPI device (EEPROM)
- Four buttons and four LEDs for user interaction
- One reset button (via an analog switch)
- NFC antenna connector on-board development board for use with supplied flexi-PCB NFC antenna

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- *Optional* external 32.768 kHz crystal oscillator and associated load capacitors. Not required for operation of the BL653; is disconnected by open solder bridges by default.
- Access to BL653 JTAG – also known as Serial Wire Debug (SWD)
- RF connector (IPEX MHF4 receptacle) for an external antenna. This is only applicable to BL653 RF pad variant (453-00041) module (which brings out RF (pin72) on module to the devbaord (453-00041-K1) via 50Ohms GCPW track and series RF 2nH RF inductor.
- On-board SWD (JTAG) programmer circuitry (USB2 to BL653 module SWD interface)
- *smart*BASIC runtime engine FW upgrade capability:
  - Via UART (using the FTDI USB1-UART)
  - Via SWD (USB2 to BL653 SWD) using on-board JTAG programmer circuitry on the BL653 Development Kit
- *smart*BASIC application upgrade capability:
  - Via UART (using the FTDI USB-UART)
  - Via OTA (Over-the-Air)

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5 Understanding the Development Board

Development board 453-00039-K1 (fitted with 453-00039 BLE module with integrated antenna)

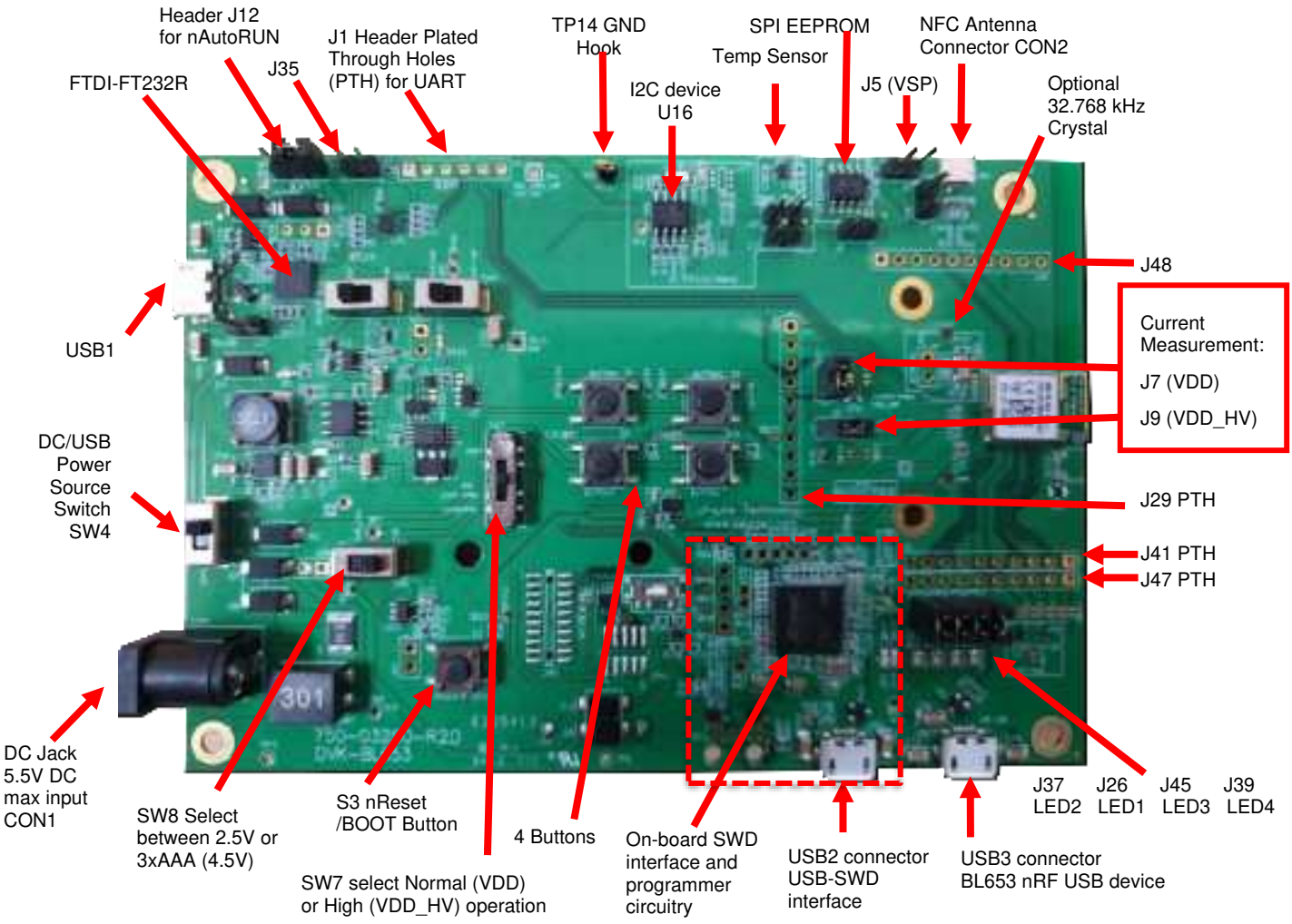

Figure 1: Dev board contents and locations

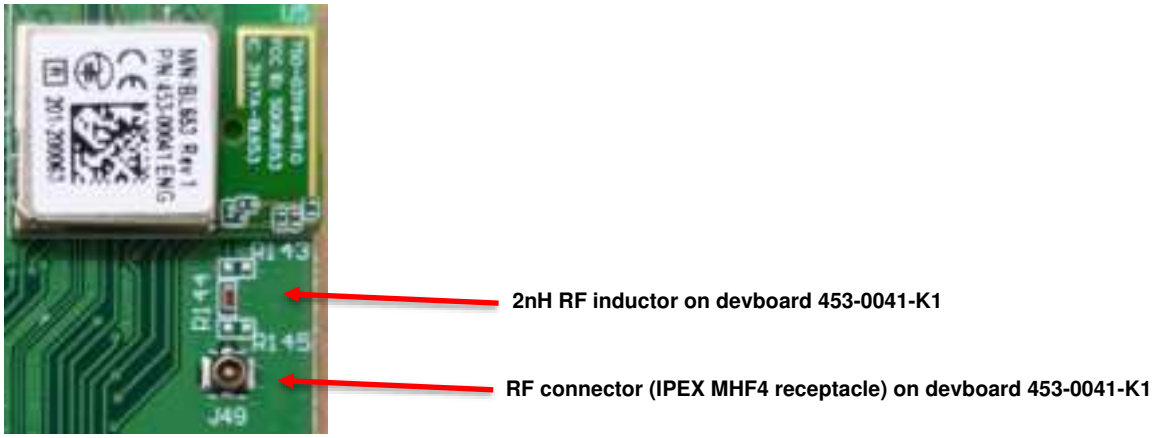

Figure 2: zoomed area of Development board 453-00041-K1 with mandatory RF GCPW RF track and series 2nH RF inductor (fitted with 453-00041 BL653 BLE module with RF pad variant)

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5.1 BL653 Default Configuration and Jumper Settings

Important! To ensure correct out-of-the-box configuration, the **BL653** development board switches and jumpers must be configured as shown in Figure 3.

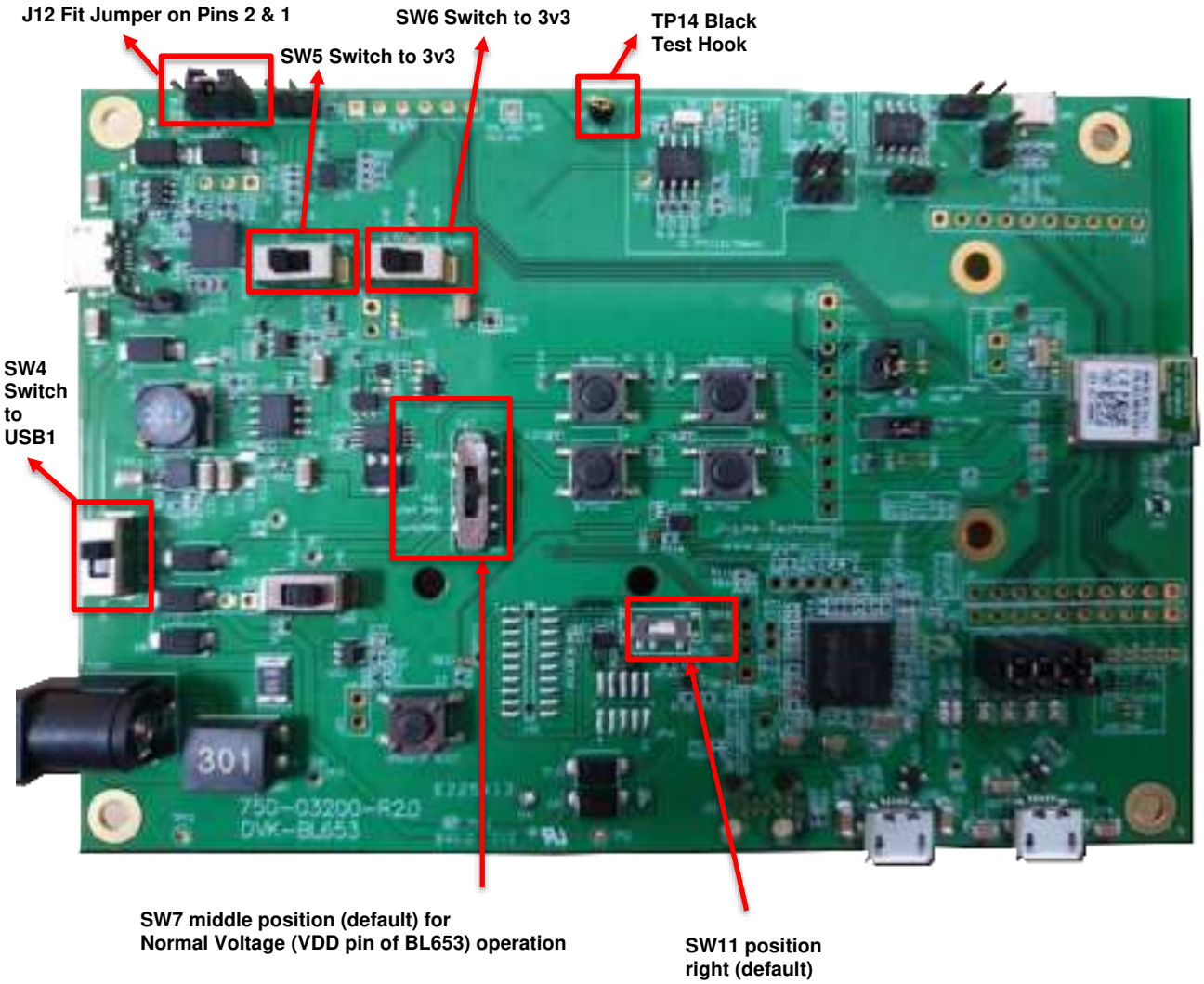

Figure 3: Correct BL653 development board 453-00039-K1 or 453-00041-K1 jumper and switch settings (image for 453-00039-K1)

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6 FUNCTIONAL BLOCKS

6.1 Power Supply

Figure 4 shows the BL653 development board Power Supply block.

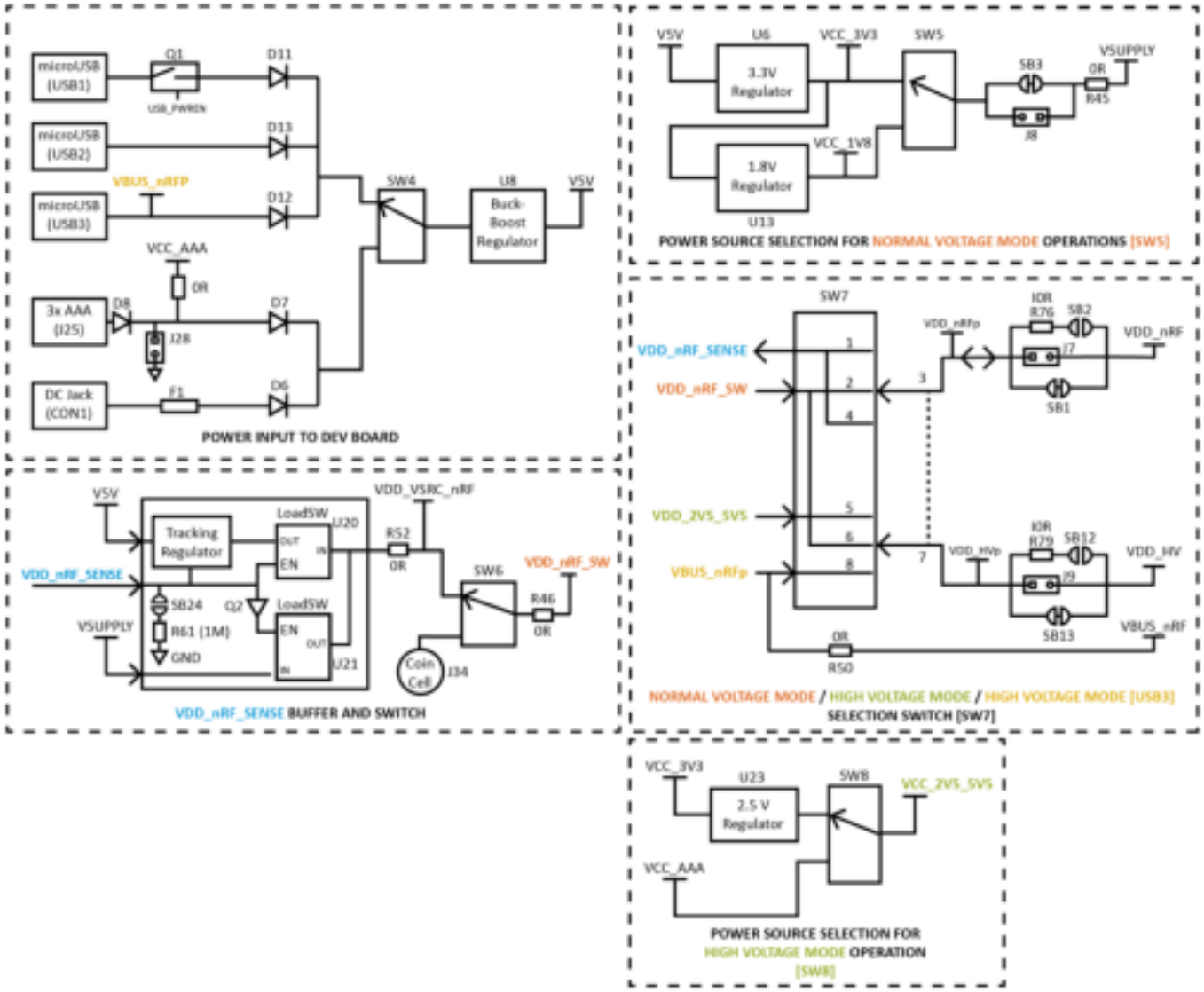

Figure 4: BL653 development Kit power supply

There are five options for powering the development board:

- USB1 USB type micro-B connector – If it requires the FTDI USB1-UART (BL653) path
- USB2 USB type micro-B connector – If it requires the Atmel USB2-SWD (BL653) path
- USB3 USB type micro-B connector – If it requires the USB3 to USB (BL653) path
- External DC supply (2.5V-5.5VV), into DC jack connector (CON1),
- AAA batteries – Three AAA (4.5V) battery holder (J25) fitted on underside of development board

The external power sources are fed into selection switch SW4 which allows a selection between either USB sources or the DC jack/AAA.

All the external power sources listed above are buck-boost regulated to a fixed 5V on the development board.

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The BL653 module has the following power supply pins:

- VDD pin (operating range of 1.7V to 3.6V) – Used for Normal Voltage mode
- VDD_HV pin (operating range of 2.5V to 5.5V) – Used for High Voltage mode
- VBUS pin (operating range of 4.35V to 5.5V) – Used for BL653 USB mode

It can be powered in the following ways:

- **Normal Voltage mode operation**

  Option 1 – Normal voltage power supply mode entered when the external supply voltage is connected to both the VDD and VDD_HV pins (so that VDD equals VDD_HV). Connect external supply within a 1.7V to 3.6V range to the BL653 VDD and VDD_HV pins.

  For Normal Voltage mode operation, the BL653 Development Board power supply section generates the following:

  – Regulated 3.3V
  – Regulated 1.8V

  and then via selection switch SW5 (default is 3.3V position), you can select whether to use 3.3V or 1.8V.

- **High Voltage mode operation**

  Option 2 – High voltage mode power supply mode (using BL653 VDD_HV pin) entered when the external supply voltage in ONLY connected to the VDD_HV pin and the VDD pin is not connected to any external voltage supply. Connect external supply within a 2.5V to 5.5V range to the BL653 VDD_HV pin. Leave the BL653 VDD pin unconnected.

  For High Voltage mode operation, the BL653 Development Board power supply section generates the following:

  – Regulated 2.5V
  – 3 x AAA generated 4.5V (or inject external voltage into J28pin1 up to 5.5V)

  and then via selection switch SW8 (default is 2.5V position), you can select whether to use 2.5V or 4.5V.

  Option 3 – High voltage mode with voltage via USB3

  – For either option, if you use the BL653 USB interface, the BL653 VBUS pin must be connected to an external supply within the range of 4.35V to 5.5V.

The BL653 development board power supply section is designed to cater to the above. Follow the following steps:

1. Set SW7 – Select one of the following three positions:
   - High Voltage mode operation and BL653 USB (connect USB cable to USB3 connector) – Top position. Source from USB3.
   - Normal Voltage mode operation – Middle position (default). Source from SW5.
   - High Voltage mode operation – Bottom position. Source from SW8.
2. Depending on chosen SW7 position, select one of the following three positions:
   - Plug in USB cable into USB3 – If SW7 is set to Top position.
   - SW5 (either 3.3V or 1.8V) – Default SW5 on 3.3V position. If SW7 set to Middle position.
   - SW8 (either 2.5V or 4.5V (3xAAA)) – Default SW8 on 2.5V position. If SW7 set to Bottom position.

Table 1 summarises the dev-board on-board power sources and switch positions.

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Table 1: Dev board power sources and switch positions

Selection Switch SW7 positions (silk screen) Source Voltage Operating mode		Dev Board Power Supply Switch Positions		
		SW5 Selects between 1.8V or 3.3V	SW8 Selects between 2.5V or 4.5V (3xAAA)	Connect USB cable into USB3
		Present selected voltage to the BL653 pin		
		BL653 VDD pin	**BL653 VDD_HV pin**	**BL653 VBUS pin**
SW7 Top position – Silkscreen: USB3 (Source from USB3) **High Voltage Mode with BL653 USB used (USB3)**		Note 1:	USB3 voltage	USB3 voltage
SW7 Middle position – Silkscreen: SW5 SW6 (Source from SW5, Note 2:) **Normal Voltage Mode**		Decided by SW5 (default SW5 on 3.3V position)	N/A	N/A
SW7 Bottom position – Silkscreen: AAA (SW8) (Source from SW8) **High Voltage Mode**		Note 1	Decided by SW8 (default SW8 on 2.5V position)	N/A

Power Source and Switch Location Notes:

Note 1: In High voltage mode, the VDD pin becomes an output voltage pin. **I**n High Voltage mode (VDD_HV), no external current draw (from VDD pin) allowed (limitation of the nRF52833 chipset). The VDD output voltage (and hence GPIO IO voltage) is configurable from 1.8V to 3.3V with possible settings (X) of 1.8V, 2.1V, 2.4V, 2.7V, 3.0V, and 3.3V. The default voltage is 1.8V.

AT command “AT+REGOUT0 X” can be used to set the output voltage where X is used to specify the voltage. The REGOUT0 register can only be written once so if a new value is required the BL654 needs to be erased and reprogrammed with a recent firmware image. Command **AT I 2026** can be used to read back the voltage level.

Example AT sequence:

at+regout0 5	Send command at+regout0 5 to set VDD output voltage and therefore GPIO I/O voltage to 3.3V
00	Module reacts after command is entered which is expected
ati 2026	Send command at I AT I 2026 to read back the set VDD pin voltage level
10 2026 3276	Module replies to show VDD output voltage hence GPIO I/O voltage is at 3.3V
00	

Note 2: When SW6 is set to position “coin-cell,” then the voltage selected with SW5 (default position 3V3) does not get presented to the BL653. The CR2032 coin cell (in J34) voltage is not regulated but is fed directly to the BL653

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module supply pin. Switch SW6 selects between the regulated 3V3V/1V8 and coin cell. The coin cell powers only the BL653 module directly (on the development board); this is power domain VDD_nRF_SW through R46 0R.

Note: The development board for BL653 has on-board circuitry to allow access to BL653 SWD interface (via USB connector USB2). Use USB2 only to power the development board when BL653 SWD interface is needed. Refer to SWD Interface. When USB2 is used, USB1 does not need to be used for DC power.

The development board power supply circuitry special feature is it resolves whether the BL653 VDD pin is an input supply pin (in Normal Voltage mode) or becomes an output supply voltage pin (in High Voltage mode).

On the development board, the power circuity net names are as follows:

- VCC_3V3 – Supplies regulated 3.3V power to the FTDI chip as well as temperature sensor (U1).
- VSUPPLY – Supplies regulated 3.3V or 1.8V via selection switch SW5 to net VSUPPLY which is connected to input of Load switch U21.
- VCC_2V5_5V5 – Selection switch SW8 supplies either regulated 2.5V or 3x AAA battery voltage (4.5V) can be used for when BL653 is powered in High Voltage mode (using the VDD_HV pin).
- V5V – The main development board power supply's buck-boosted output (that is 5V) supplies a discrete regulator made up of Q3 and U19. U19 OpAmp drives Q3 to generate regulated voltage (that then is connected to input of load switch U20) that tracks control signal VDD_nRF_SENSE.
- VDD_VSRC_nRF – Supplies the FTDI chip IO and all other sensors and circuitry. VDD_VSRC_nRF is generated from load switches U20 or U19.
- VDD_nRF_SENSE – Used as control signal to drive control pin of load switches U20 and U19. The source of VDD_nRF_SENSE is the BL653 VDD pin. When BL653 is powered in High Voltage mode (using the VDD_HV pin), the BL653 VDD pin becomes an output.
- VDD_nRF_SW – Selection switch SW6 supplies either VDD_SRC_nRF or coin-cell (J34). When the BL653 operated in Normal Voltage mode (SW7 in middle position and voltage source is either 1.8V or 3.3V selected by SW5). Also supplies the I2C RTC chip (U16). The use case for powering this is that the RTC chip can be configured so that, after the pre-determined time, the RTC chip outputs (via RTC_ALARM pin) a transition level that can be used to wake up the BL653 module up from deep sleep.
- VDD_nRFp – Supplies the BL653 series module only. Current measuring block on the development board only measures the current into power domain VDD_nRFp (that is current going into header J7 pin 1).
- VDD_nRF – Supplies the BL653 series module only and is to the current that has come out of the current measuring block on the development board on header connector J7 pin 2.
- VDD_HVp – Supplies the BL653 series module only. Current measuring block on the development board only measures the current into power domain VDD_nRFp (that is current going into header J9 pin1).
- VDD_HV – Supplies the BL653 series module only and is to the current that has come out of the current measuring block on the development board on header connector J9pin2.
- VBUS_nRFp – This voltage from USB cable plugged into connector USB3, that is directly fed to BL653 VBUS pin (via 0R resistor R50) on net VBUS_nRF.

TIP: If operating the development board at temperature of 75°C or above (upto +85°C) there is an issue related to Q2 (it starts turning on) which results in VDD_VSRC_nRF supplying heading towards 0V or turning off. To overcome this issue 75°C or above (upto +85°C) issue, bridge with solder the open-solderbridge SB24 which connects 1MOhms resistor to ground onto the gate of Q2.
The 1-MOhm resistor results in extra current consumption of (= VDD_nRF_SENSE/1Mohms) added to any current measurements made when operating the BL653 module on devboard in High voltage mode (VDD_HV pin) ONLY which is when SW7 in Top position or Bottom position (and in that case by default VDD_nRF_SENSE is 1.8V). Figure 5 shows PCB location of SB24 and schematic showing SB24.

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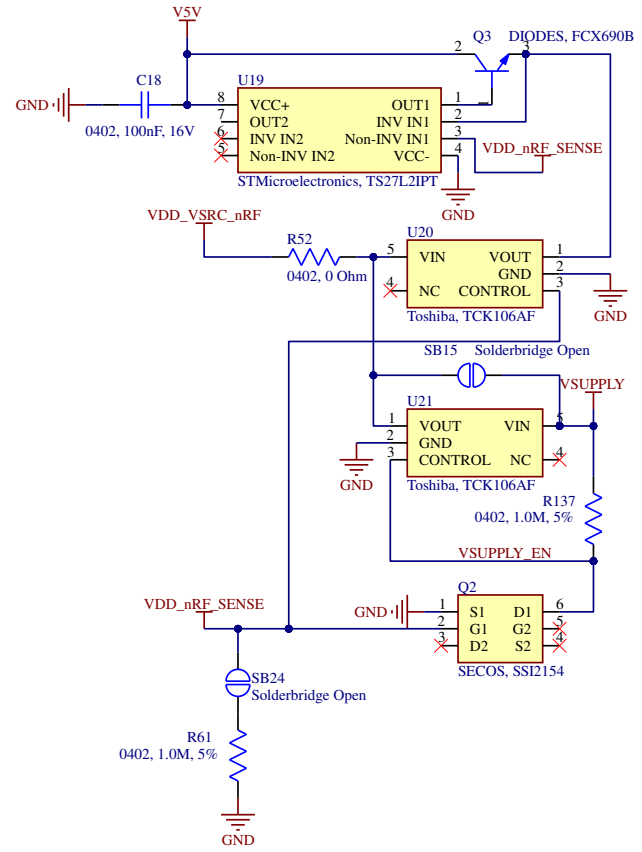

Figure 5: Schematic and PCB location of SB24

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6.1.1 Additional Power Option – Coin Cell (for BL653 module only – not the development board)

The coin cell powers *only* the BL653 module directly via SW6 (on the development board – power domain VDD_nRF_SW) and through R46 provides power to the I2C RTC chip (U16).

Refer to the Appendix for the correct method of coin cell insertion and removal.

6.2 Reset Button

The development board has a reset button (SW3) with the net name BOOT_RESET_BLE. The BOOT_RESET_BLE (is active low when SW3 pushed down) is routed to the BL653 module nRESET_BLE pin via an analog switch U25. The placement of the Reset button is shown in Figure 6.

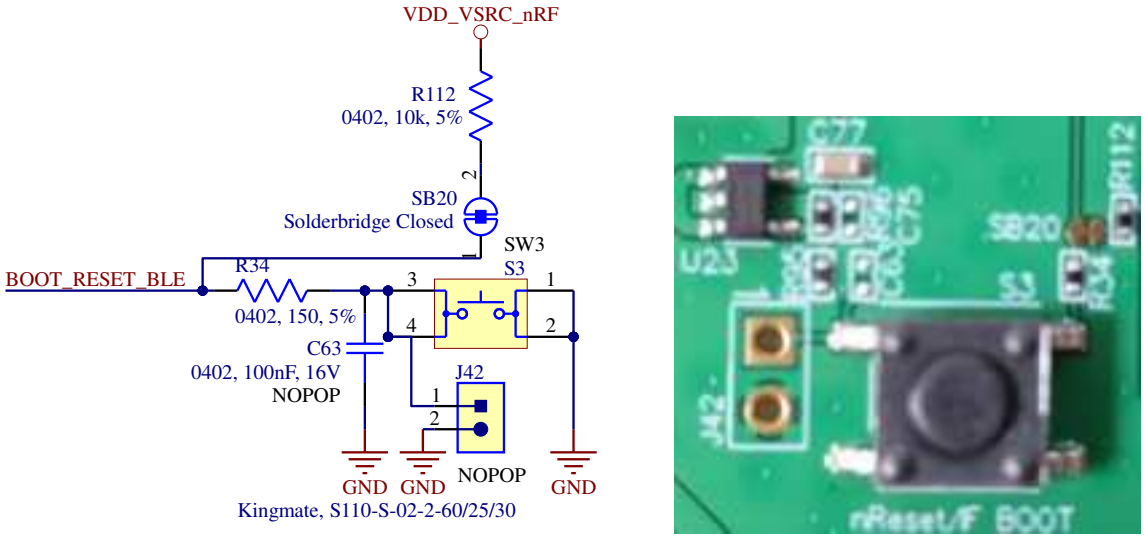

Figure 6: Reset button placement

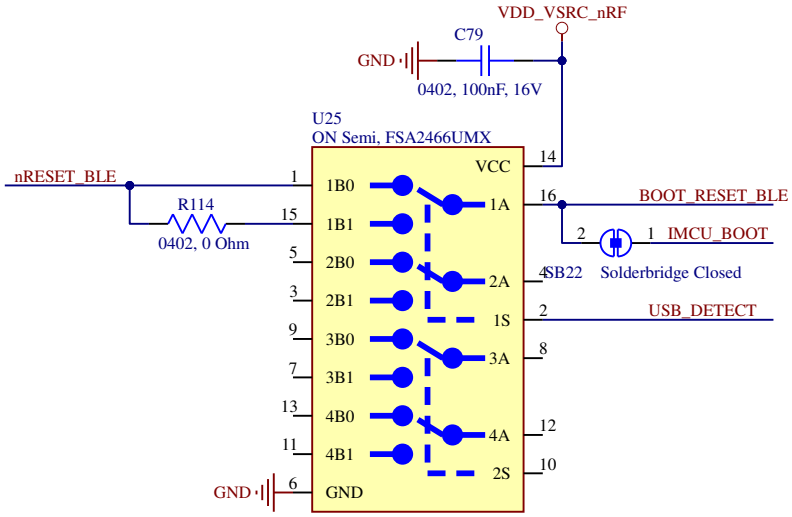

Figure 7: Reset button schematic and routing through analog switch and location diagram

By default, whether the analog switch (U25) control line (USB_DETECT) is low (USB2 cable not plugged in) or high (USB2 cable plugged in), the nReset button (SW3) is routed via the analog switch (U25) to BL653 nReset pin (nRESET_BLE).

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The development board has USB2 cable detection circuit that generates the USB_DETECT signal on its output, so if a USB cable is plugged into connector USB2, then USB2 cable detection circuit generates a HIGH on USB_DETECT or LOW if USB2 cable is not plugged in.

Table 2 displays the routing of SW3 reset button via analog switch U25 to the BL653 reset pin (regardless of whether the USB cable is plugged into USB2 or not).

Table 2: USB U4 USB-SWD to BL653 SWD signal routing connections

SW3 reset button into Analog switch U25 (net name)	USB cable plugged into USB2 (USB_DETECT HIGH)	No USB cable plugged into USB2 (USB_DETECT LOW)	Comments
	Route SW3 reset button to BL653 (U5) reset pin via analog switch U25 (net name)	Route SW3 reset button to BL653 (U5) reset pin via analog switch U25	
BOOT_RESET_BLE	nRESET_BLE	nRESET_BLE	R114 0R resistor if removed allows SW3 to be disconnected from BL653 reset pin when USB2 cable plugged in.

6.3 SWD (JTAG) Interface

The development board provides access to the BL653 module two-wire SWD interface on JP1 via analog switch U24. This is REQUIRED for customer use, since the BL653 module supports *smart*BASIC runtime engine firmware over JTAG (as well as over UART).

Note: We recommend that you use JTAG (two-wire interface) to handle future BL653 module firmware upgrades. You MUST wire out the JTAG (two-wire interface) on your host design (four lines should be wired out, namely SWDIO, SWDCLK, GND, and VCC). Firmware upgrades can still be performed over the BL653 UART interface, but this is slower (60 seconds using UART vs. 10 seconds when using JTAG) than using the BL653 JTAG (two-wire interface).

Upgrading *smart*BASIC runtime engine firmware or loading *smart*BASIC applications also can be done using the UART interface.

For those customers (using Nordic SDK) that require access to BL653 SWD (JTAG) interface, the BL653 development board (see Figure 1) has on-board circuitry to allow access to BL653 module SWD interface (via USB connector USB2).

When the USB cable is plugged into connector USB2 (the USB cable detection output generates a HIGH for USB_DETECT and USB_DETECTp when switch SW11 is in position 2-1 – the default) and Atmel MCU SWD (JTAG) signals are routed to the BL653 SWD interface. This is required to connect the two-wire SWD (JTAG) interface from U14 to the BL653 SWD (JTAG) interface.

When the USB cable is plugged into connector USB2 and the SW11 is in position 2-3 (Low), there is a LOW on U24 control line USB_DETECTp and the Atmel MCU SWD (JTAG) signals are routed to connector JP1 (which is not populated).

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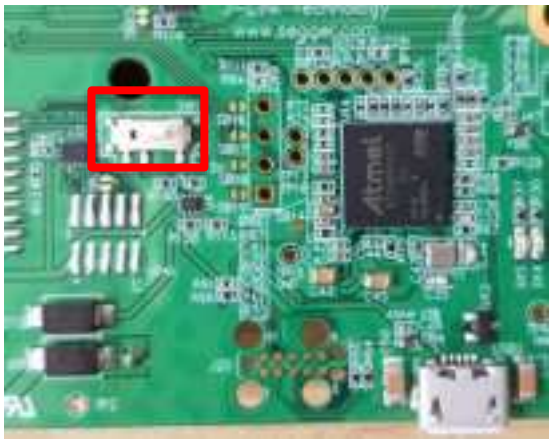

Figure 8: SW11 on development board (showing default position)

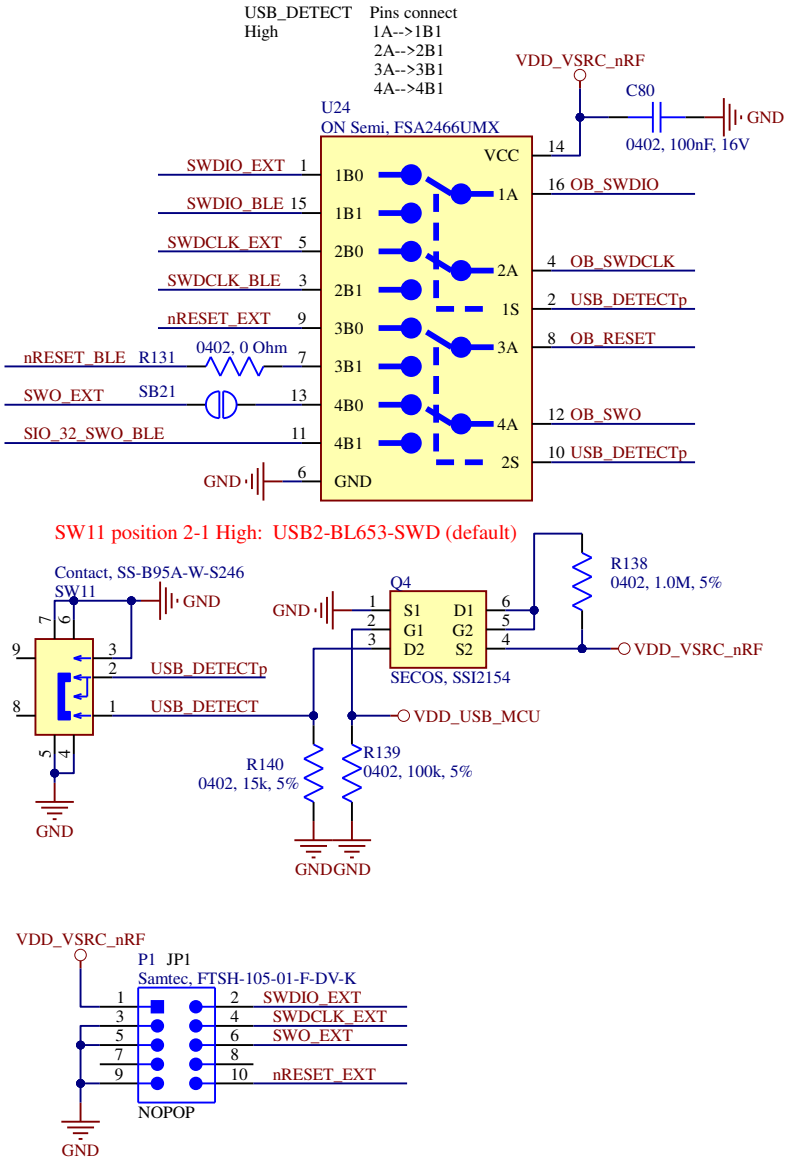

Figure 9: USB2 to SWD onboard circuitry routing via analog switch (U24)

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Table 3 displays the four signals running from Atmel MCU U14 (SWD interface plus SIO_32 and nReset_BLE) to the BL653 module (SWD interface plus SIO_32 and nReset_BLE).

Table 3: USB U4 USB-SWD to BL653 SWD signal routing connections

U4 (Atmel MCU) Net SWD Interface into Analog switch U24	USB cable plugged into USB2 (USB_DETECTp HIGH)	No USB cable plugged into USB2 (USB_DETECTp LOW)	Comments
	Route SWD Interface from Atmel MCU (U4) to BL653 Module Net Name	Route SWD Interface from Atmel MCU (U4) to JP1	
OB_SWDCLK	SWDCLK_BLE (pin 3)	SWDCLK_EXT (JP1 pin4)	
OB_SWDIO	SWDIO_BLE (pin 1)	SWDIO_EXT (JP1 pin2)	
OB_RESET	nRESET_BLE (pin 19) via R131 0R (Not populated)	nRESET_EXT (JP1 pin10)	
OB_SWO	SIO_32 (pin 7)	SWO_EXT (JP1 pin6) via SB21 open solderbridge	

SIO_32 is a trace output (called SWO, Serial Wire Output) and is not necessary for programming BL653 over the SWD interface.

nReset_BLE is not necessary for programming BL653 over the SWD interface.

6.4 Four-wire UART Serial Interface

The development board provides access to the BL653 module four-wire UART interface (TX, RX, CTS, RTS) either through USB (via UT10 FTDI USB-UART convertor chip) or through a breakout header connector J1.

Note: The BL653 module provides four-wire UART interface on the HW and the other four signals (DTR, DSR, DCD, RI), which are low bandwidth signals, can be implemented in a *smart*BASIC application using any spare digital SIO pins.

6.5 UART Mapping

The UART connection on the BL653 series module and the FTDI IC are shown in Table 4. Figure 10 explains how the BL653 series module UART is mapped to the breakout header connector J1. These connections are listed in Table 4.

Table 4: SIO/UART connections

BL653 (U5) SIO	BL653 Default Function	FTDI IC UART
SIO_06 (U5 pin35)	UART_TX (output)	USB_RX
SIO_08 (U5 pin29)	UART_RX (input)	USB_TX
SIO_05 (U5 pin39)	UART_RTS (output)	USB_CTS
SIO_07 (U5 pin37)	UART_CTS (input)	USB_RTS

Note: Additionally, SIO_35 (the nAutoRUN input pin on the module) can be driven by the USB_DTR output pin of the FTDI chip. This allows testing the $autorun$ application on boot without setting the autorun jumper on the development board. nAutorun can be controlled directly from Laird's UWTerminalX using the DTR tick box.

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6.5.1 UART Interface Driven by USB

- **USB Connector:** The development kit provides a USB Type Micro-B connector (USB1) which allows connection to any USB host device. The connector optionally supplies power to the development kit and the USB signals are connected to a USB-to-serial converter device (FT232R) when SW4 is set to the USB position.
- **USB – UART:** The development kit is fitted with a (U10) FTDI FT232R USB-to-UART converter which provides USB-to-Virtual COM port on any Windows PC (XP or later). Upon connection, Windows auto-installs the required drivers. For more details and driver downloads, visit the following website: http://www.ftdichip.com/Products/FT232R.htm.
- **UART Interface Driven by USB FTDI Chip:** In normal operation, the BL653 UART interface is driven by the FTDI FT232R USB-to-UART converter.

6.5.2 UART Interface Driven by External Source

- **UART Interface Driven by External UART Source:** The BL653 module UART interface (TX, RX, CTS, RTS) is presented at a 2.54 mm (0.1") pitch header (J1). To allow the BL653 UART interface to be driven from the breakout header connector (J1), the following must be configured:
  - The development board must be powered from a DC jack (CON1) or AAA batteries (J25) and with switch SW4 in DC position.
  - The FTDI device must be held in reset. This is achieved automatically by removal of the USB cable (from connector USB1), placing SW4 in the DC position or fitting a jumper on J27.
  - Fit a jumper on J35 (to switch the Analog switch U15 and route BL653 UART to J1) when connecting an external UART source (for example FTDI USB-UART TTL (3.3V) converter cable) using J1. This isolates the BL653 UART from the on-board USB-UART FTDI device. By default, the jumper on J35 is not fitted, so by default BL653 UART is routed to U10 FTDI FT232R USB –UART converter.

Note: The BL653 UART signal levels always need to match the supply voltage net VDD_VSRC_nRF, of the BL653.

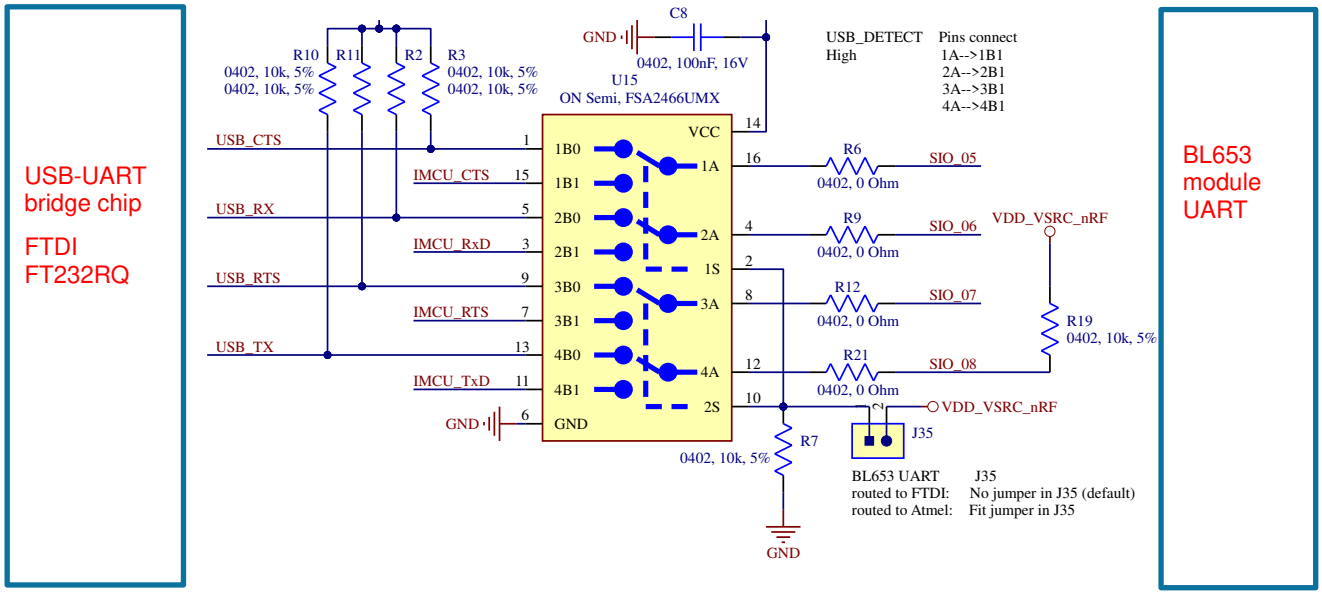

Figure 10: USB to UART (via FTDI chip on devboard) interface via analog switch U15

J1 pinout is designed to be used with FTDI USB-UART TTL (3.3V) converter cables (found at http://www.ftdichip.com/Products/Cables/USBTTLSerial.htm). One example is FTDI part TTL-232R-3V3.

If the BL653 on the development board is powered from 1.8V supply, then you must use the 1.8V version of the FTDI USB-UART cable. UART signal levels always need to match the supply voltage net VDD_nRF_SW of the BL653 development board.

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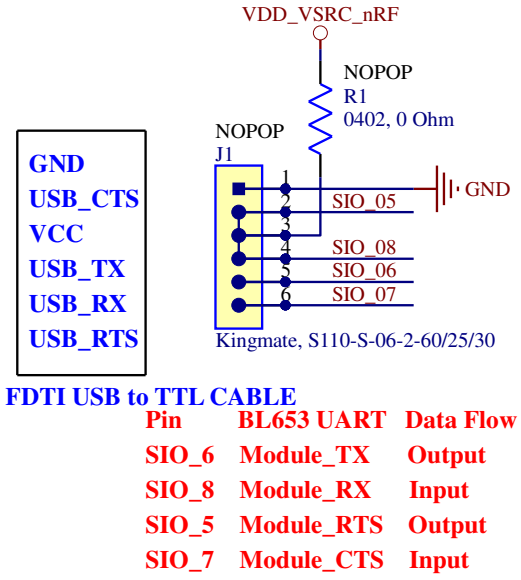

Figure 11: J1 wiring to match FTDI USB-UART cable (TTL-232R-3V3 cable)

Fit a jumper in J35 (to switch the Analog switch U15 and route BL653 UART to J1) when connecting an external FTDI USB-UART TTL (3.3V) converter cable using J1.

Fitting a jumper in J35 also allows the BL653 UART to be routed to Atmel MCU UART (signal also on J19 and net names beginning with IMCU_) via open solder bridges SB16 to SB19 shown in Figure 12. You must connect these bridges with solder. This may be useful for those customers wanting to work with the Nordic SDK.

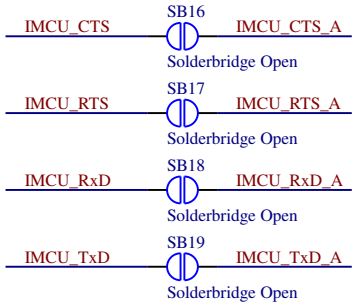

Figure 12: Open solder-bridges on the UART interface running from Atmel MCU (U4) to analog switch U15 (to BL653 ultimately)

6.6 nAutoRUN Pin and Operating Modes

On the development board, the USB_DTR output (FTDI chip U10) from the PC is wired to BL653 module pin SIO_35 (pin 5) which is the nAutoRUN pin.

Note: *smart*BASIC runtime engine FW checks for the status of nAutoRUN during power-up or reset. The nAutoRUN pin detects if the BL653 module should power up into Interactive/Development Mode (3.3 V) or Self-contained Run mode (0V). The module enters Self-contained Run mode if the nAutoRUN pin is at 0V and an application called $autorun$ exists in the module's file system, then the *smart*BASIC runtime engine FW executes the *smart*BASIC application script automatically; hence the name Self-contained Run mode.

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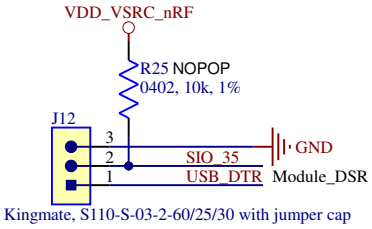
Tying nAutoRUN HIGH (to net name on devboard VDD_VSRC_nRF) inhibits the $autorun$ application from running. As an alternative to using USB_DTR, the J12 three-pin header allows a jumper to be fitted to select between the two operating modes.

Table 5: BL653 nAutoRUN header

nAutoRUN Pin	BL653 Operating Mode (pin28, nAutoRUN Mode/SIO_35)		
	Interactive/ Development Mode (SIO_35 (P1.01) set High Externally)	Self-contained Run Mode (nAutoRUN mode) (SIO_35 (P1.01) Low Internally)	Circuit
J12 Jumper Position			
	Develop Jumper on J12 pins 2-1	**nAutoRUN (default)** Jumper on J12 pins 2-3 BL653 has internal pull-down enabled, jumper in J12 in 2-3 can also be left off	Kingmate, S110-S-03-2-60/25/30 with jumper cap **Develop: jumper J12 pin2-1 (default)** **nAutoRUN: jumper J12 pin2-3**

The J12 header connector allows the USB_DTR signal from the FTDI chip to be disconnected from the BL653.

To connect the BL653 nAutoRUN pin SIO_35 (pin 5) to PC FTDI USB_DTR line via the J12 header connector, do the following:

- Fit the jumper into the J12 (pin 2-1) header connector to allow the PC (using UwTerminal) to control nAutoRUN pin (SIO_35).

To disconnect the BL653 nAutoRUN SIO_35 (pin 5) from the PC FTDI USB_DTR line, do the following:

- Remove the jumper on header connector J12 pin 2-1. Then nAutoRUN can be controlled by inserting the jumper onto J12 (pin 2-3) as shown in Table 5 (this is the default). The BL653 by default has pull-down enabled on the SIO_35 (nAutoRUN) pin, so the jumper into J12 (pin 2-3) is optional.

6.7 Virtual Serial Port Modes and Over-the-Air *smart*BASIC App Download

The Over-the-Air (OTA) feature makes it possible to download *smart*BASIC applications over the air to the BL653. To enable this feature, SIO_02 must be pulled high externally.

On the development board, header connector J5-pin1 brings out the BL653 SIO_02; J5-pin 2 brings out VCC_nRF_SW. To pull BL653 SIO_02 high (to net name VCC_nRF_SW on devboard), fit jumper into header J5.

Note: When SIO_02 is high, ensure that SIO_35 (nAutoRun) is NOT high at same time, otherwise you cannot load the *smart*BASIC application script.

This section discusses Virtual Serial Port (VSP) Command mode through pulling SIO_02 high and nAutoRUN (SIO_35) low. Refer to the documentation tab of the **BL653 product page:**
https://www.lairdconnect.com/wireless-modules/bluetooth-modules/bluetooth-5-modules/bl653-series-bluetooth-51-802154-nfc-module

Figure 13 shows the difference between VSP Bridge to UART mode and VSP Command mode and how SIO_02 and nAutoRUN (SIO_35) must be configured to select between these two modes.

- **VSP Bridge to UART mode** takes data sent from phone or tablet (over BLE) and sends to BL653 to be sent out of the BL653 UART (therefore data not stored on BL653).
- **VSP Command mode** takes data sent from phone or tablet and sends it to the BL653. This interprets as an AT command and the response is sent back. The OTA Android or iOS application can be used to download any *smart*BASIC application script over-the-air to the BL653, since a *smart*BASIC application is downloaded using AT commands.

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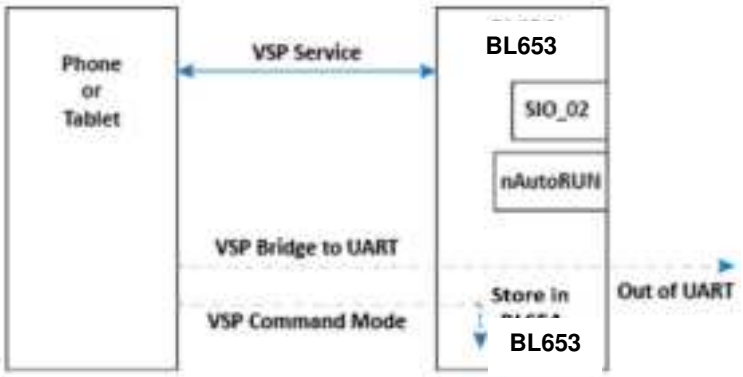

Figure 13: Differences between VSP bridge to UART mode and VSP Command mode

Table 6: vSP modes

Mode	SIO_02 and Jumper position J5	nAutoRUN (SIO_35) and Jumper position J12
VSP Bridge to UART mode	High by fitting jumper in J5	High by fitting jumper in J12 pin 2-1 and untick DTR box in UwTerminalX (the DTR box is ticked by default in UwTerminalX)
VSP Command mode	High by fitting jumper in J5	Low by fitting jumper in J12 pin 2-3

SIO_02 High (externally) selects the VSP service. When SIO_02 is High and nAutoRUN (SIO_35) is Low (externally), this selects VSP Command mode. When SIO_02 is High and nAutoRUN is High (externally), this selects VSP Bridge to UART mode.

When SIO_02 on module is set HIGH (externally), VSP is enabled and auto-bridged to UART when connected. However, for VSP Command mode, auto-bridge to UART is not required. With SIO_02 set to High and nAutoRUN (SIO_35) set to Low, the device enters VSP Command mode and you can then download the *smart*BASIC application onto the module over the air from the phone (or tablet).

7 SOFTWARE

The development board connects the BL653 module to a virtual COM port of a PC or other device. From a PC, you can communicate with the module using Laird's UwTerminalX (cross platform software available for Windows, Mac, and Linux). This utility allows connections to serial devices using any combination of the communications parameters listed in Table 7.

Table 7: UwTerminalX communication parameters for BL653

Port (Windows)	1 to 255
Port (Mac/Linux)	Any/dev/tty device
Baud Rate	1200 to 1000000 **Note:** Baud rate default is 115200 for BL653.
Parity	None
Data Bits	8
Stop Bits	1
Handshaking	None or CTS/RTS

Note: Baud rates higher than 115200 depend on the COM port capabilities of the host PC and may require an external USB – RS232 adapter or ExpressCard – RS232 card.

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The benefits of using UwTerminalX include the following:

- Continually displayed status of DSR, CTS, DCD, and RI
- Direct control of DTR on the host PC via a check box
- Direct control of RTS, if CTS / RTS Handshaking is disabled when UWTerminalX is launched
- Sending UART BREAK signals. Following provides explanation UART Break. (https://en.wikipedia.org/wiki/Universal_asynchronous_receiver/transmitter#Break_condition)
- Additional built-in features (right click in Terminal tab screen) to accelerate development including Automation and various XCompile/Load/Run options for downloading *smart*BASIC applications into the BL653.

Note: Full details on *smart*BASIC are available in the *smart*BASIC User Guide available at the Laird product page for BL653, along with a document giving a basic introduction to UwTerminalX. A help file is included with UwTerminalX that gives an overview of the program. Visit the BL653 product page at https://www.lairdconnect.com/wireless-modules/bluetooth-modules/bluetooth-5-modules/bl653-series-bluetooth-51-802154-nfc-module.

Tip: If the module returns a four-hex digit error code:
In UwTerminalX, select those four digits, right-click, and select **Lookup Selected Error-Code (Hex)**. A description of the error is then printed on screen.

8 Breakout Connector Pinouts

8.1 SIO (Special Input/Output Sockets) Breakout Connectors

Access to all 48 BL653 series module signal pins (SIO's = Signal Input /Output) is available on plated-through holes (for 2.54 mm pitch header connectors) on J44, J47, J48, J41, J29, J1, J12, J1, J5, J17, J21, J6, and J36.

Note: The BL653 module signal pins designation SIO (Signal Input /Output).

- DEFAULT type is DIO (Digital Input or Output) or UART (on fixed pins)
- ALTERNATE type is either AIN (Analog Input ADC), I2C, SPI, DIO (on fixed pins), PWM, FREQ, and NFC
- DIO or AIN functionality is selected using the GpioSetFunc() function in *smart*BASIC
- I2C, UART, SPI controlled by xxxOPEN() functions in *smart*BASIC
- SIO_05 to SIO_08 are DIO by default when $autorun$ app runs on power up
- SIO_09 and SIO_10 are NFC pins by default; they can be set to alternative function SIO using the GpioSetFunc() function in *smart*BASIC

These breakout connectors can interface to a wide array of sensors, the BL653 is user configurable through the *smart*BASIC application script to change each SIO pin from the default function (DIO, UART) to alternate functions (AIN (ADC), I2C, SPI, DIO), PWM, FREQ, and NFC. The BL653 development kit incorporates additional fly-lead cables inside the box to enable simple, hassle-free testing of these multiple interfaces.

Table 8 shows the BL653 module pins that are brought out to plated through Holes (suitable for 2.54 mm pitch headers).

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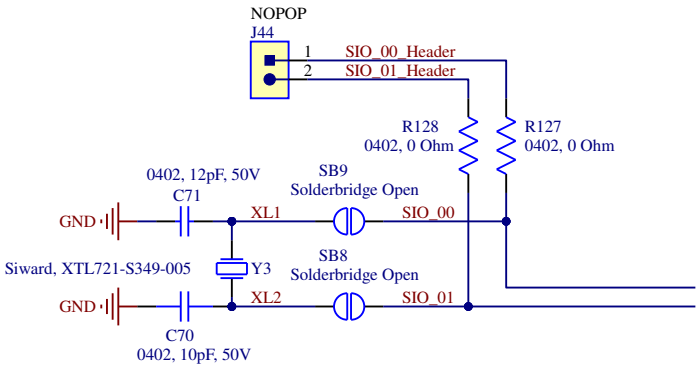
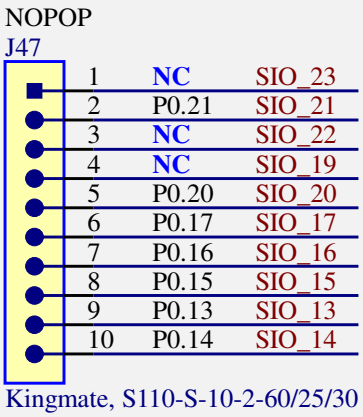
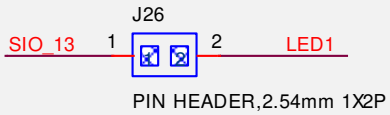
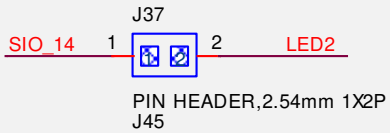
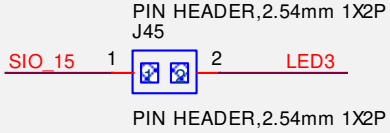
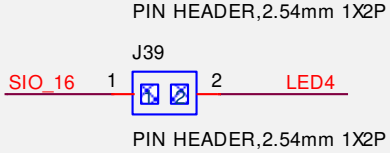
Table 8: Module pins exposed by plated through holes

Plated Through Holes or Header Connector	BL653 Module Signals Exposed
J44  	BL653 pin plated holes for access: ▪ SI0_ 00 ▪ SI0_ 01 J44 connects to SIO_00 and SIO_01 via 0R resistors R127 and R128. By default, the optional external 32.768 kHz crystal circuit is not connected to BL653 as SB8 and SB9 are open.
J47  	BL653 pin plated holes for access: ▪ SI0_ 23 NC ▪ SI0_ 21 P0.21 ▪ SI0_ 22 NC ▪ SI0_ 19 NC ▪ SI0_ 20 P0.20 ▪ SI0_ 17 P0.17 ▪ SI0_ 16 P0.16 ▪ SI0_ 15 P0.15 ▪ SI0_ 13 P0.13 ▪ SI0_ 14 P0.14 J47 header pins marked "NC" have no signal connected to them (wired to corresponding NC pin on BL653).
J26  	J26 Connects SIO_13 to LED1 J26 jumper fitted (default).
J37  	J37 Connects SIO_14 to LED2 J37 jumper fitted (default).
J45  	J45 Connects SIO_15 to LED3 J45 jumper fitted (default).
J39  	J39 Connects SIO_16 to LED4 J39 jumper fitted (default).

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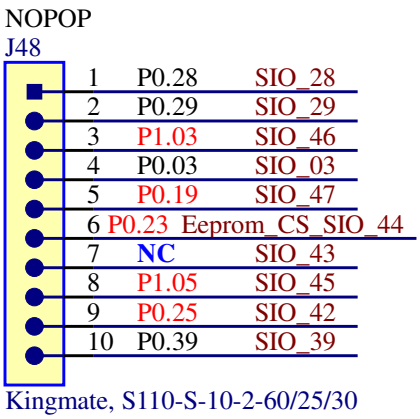
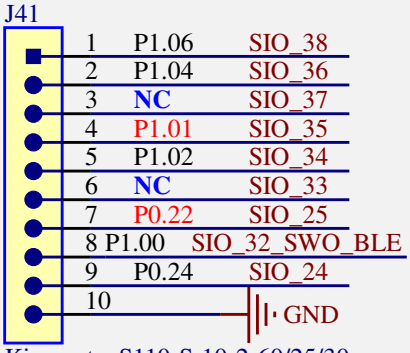
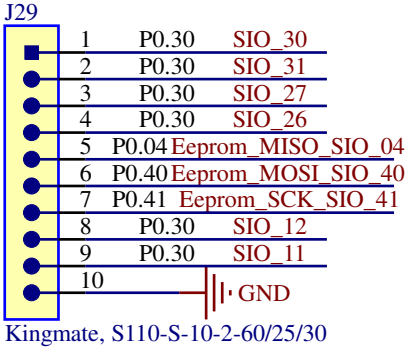
Plated Through Holes or Header Connector	BL653 Module Signals Exposed
J48  	BL653 pin plated holes for access: ▪ SI0_ 28 P0.28 ▪ SI0_ 29 P0.29 ▪ SI0_ 46 P1.03 ▪ SI0_ 03 P0.03 ▪ SI0_ 47 P0.19 ▪ SI0_ 44 (connects to Eeprom_CS) P0.23 ▪ SI0_ 43 NC ▪ SI0_ 45 P1.05 ▪ SI0_ 42 P0.25 ▪ SI0_ 39 P0.39 J48 header pins marked *NC* have no signal connected to them (wired to corresponding NC pin on BL653).
J41  	BL653 pin plated holes for access: ▪ SI0_ 38 P1.06 ▪ SI0_ 36 P1.04 ▪ SI0_ 37 NC ▪ SI0_ 35 P1.01 ▪ SI0_ 34 P1.02 ▪ SI0_ 33 NC ▪ SI0_ 25 P0.22 ▪ SI0_ 32 P1.00 ▪ SI0_ 24 P0.24 ▪ GND J41 header pins marked *NC* have no signal connected to them (wired to corresponding NC pin on BL653).
J29  	BL653 pin plated holes for access: ▪ SI0_ 30 ▪ SI0_ 31 ▪ SI0_ 27 ▪ SI0_ 26 ▪ SI0_ 04 (connects to Eeprom_MISO) ▪ SI0_ 40 (connects to Eeprom_MOSI) ▪ SI0_ 41 (connects to Eeprom_SCK) ▪ SI0_ 12 ▪ SI0_ 11 ▪ GND

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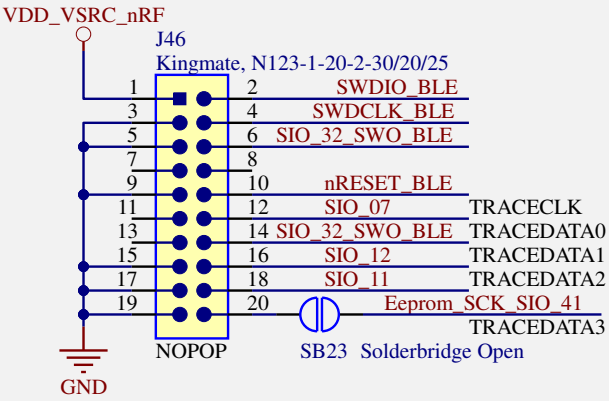
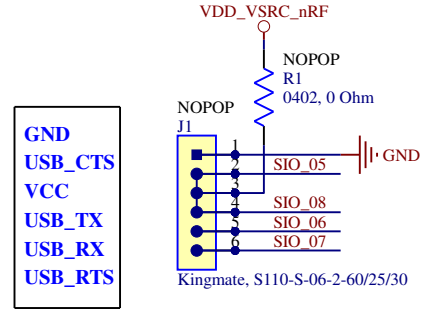
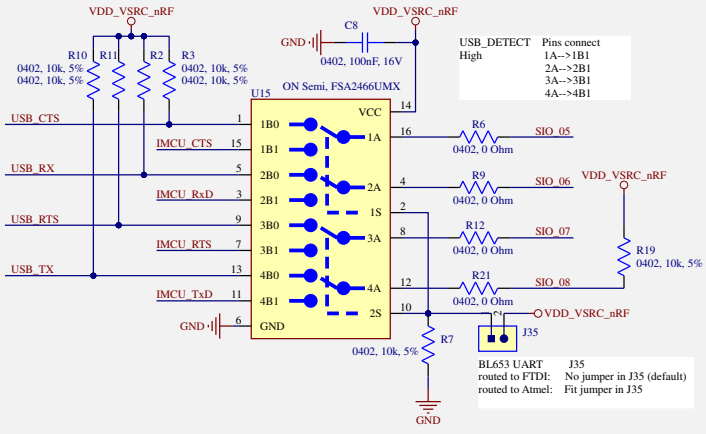
Plated Through Holes or Header Connector	BL653 Module Signals Exposed
J46  	J46 is NOPOP but is compatible to same connector on Nordic development board and brings out same signals. SIO_41 on BL653 is SPI_CLK (as an alternative function) is disconnected from J46 on devboard by open solderbridge SB23. SIO_41 on BL653 is directly connected to U2 (Eeprom) pin6 on devboard.
J1  **FDTI USB to TTL CABLE** **Pin BL653 UART Data Flow** **SIO_6 Module_TX Output** **SIO_8 Module_RX Input** **SIO_5 Module_RTS Output** **SIO_7 Module_CTS Input**	Serial Port plated holes for BL653 UART access. Refer to J1 schematic on the left.
J35 BL653 UART J35 routed to FTDI: No jumper in J35 (default) routed to Atmel: Fit jumper in J35  	Jumper in J35 selects between BL653 UART routed to FTDI Atmel MCU: **No Jumper on J35 (default)** Routes SIO_05 (RTS) to FTDI CTS Routes SIO_06 (TX) to FTDI RX Routes SIO_07 (CTS) to FTDI RTS Routes SIO_08 (RX) to FTDI TX **Jumper on J35 (Route to Atmel)** Routes SIO_05 (RTS) to IMCU_CTS Routes SIO_06 (TX) to IMCU_RxD Routes SIO_07 (CTS) to IMCU_RTS Routes SIO_08 (RX) to IMCU_TxD

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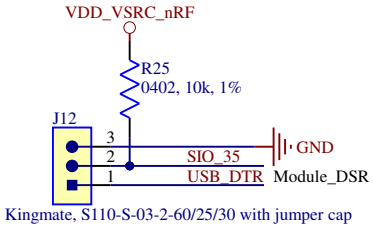
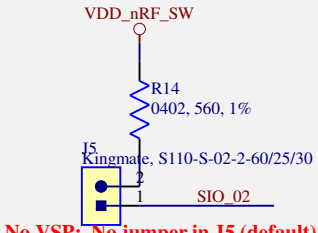
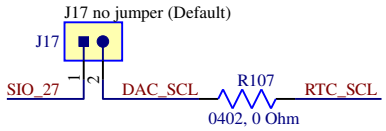
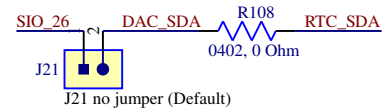
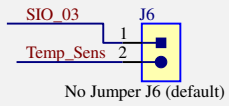
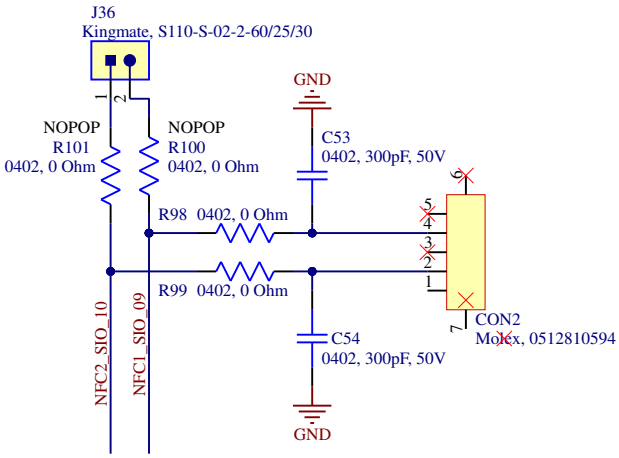
Plated Through Holes or Header Connector	BL653 Module Signals Exposed
J12  Kingmate, S110-S-03-2-60/25/30 with jumper cap **Develop: jumper J12 pin2-1 (default)** **nAutoRUN: jumper J12 pin2-3**	Connects SIO_35 (nAutoRUN) to FTDI DTR Default jumper fitted in J12 pin 2-1.
J5  **No VSP: No jumper in J5 (default)** **VSP: jumper in J5**	SIO_ 02 (for VSP capability) Can be used to pull-up SIO_02 to VDD_nRF_SW Default: No Jumper fitted on J5 SIO_02
J17  **J21**  	J17 Routes SIO_27 (I2C SCL) to RTC_SCL device J17 pin 2-1 jumper NOT fitted (default). J21 Routes SIO_26 (I2C_SDA) to RTC_SDA device J21 pin 2-1 jumper NOT fitted (default).
J6  No Jumper J6 (default)	J6 routes SIO_03 to Temp Sensor J6 pin 2-1 jumper NOT fitted (default)
J36  	BL653 pin plated holes for access: SI0_ 09 via R100 0R (default NOPOP) SI0_ 10 via R101 0R (default NOPOP) To use NFC1 pin as SIO_09 fit R100 0R and NOPOP R98. To use NFC1 pin as SIO_09 fit R101 0R and NOPOP R99.

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8.2 Additional Peripherals/Sensors

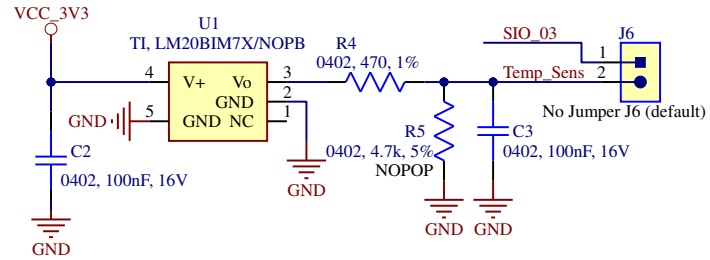
The BL653 development board provides for simple and hassle-free connectivity to a wide range of sensors, but also includes several on-board sensors and options to enable a developer to test functionality straight out of the box.

In the *smart*BASIC application code written to use sensors on the development board, including the Temperature sensor (U1) – analog output, SPI EEPROM (U2), I2C RTC chip (U16), LED1(D1), LED2(D2), LED3(D3), LED4(D4) Button1(SW1), Button2(SW2), Button3(SW9) and Button4(SW10) the SIO pins direction and type must be set in the *smart*BASIC application to override the defaults in the BL653 firmware.

For more information on these sample applications, see GitHub *smart*BASIC sample applications repository on the BL653 product page at https://github.com/LairdCP/BL653-Applications.

8.2.1 Temperature Sensor

The temperature sensor (U1) by default is connected to the BL653 module as jumper on J6 pin bridges TEMP_SENS and SIO_03.



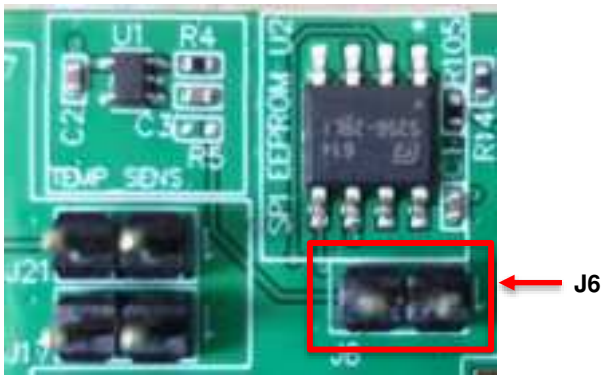


Figure 14: Temperature sensor schematic and PCB

The on-board temperature sensor (TI LM20BIM7 - www.ti.com/lit/ds/symlink/lm20.pdf) has an analogue output that can be connected to BL653 module pin SIO_03; but since the LM20BIM7 has an analogue output, the BL653 module SIO_03 digital pin (DIO) must be configured as AIN analogue input (ADC). To configure the SIO_03 pin from DIO pin to Alternate function AIN, see the example file "*ts.temperature.sensor.sb*" in the GitHub *smart*BASIC sample applications repository on the BL653 product page at https://github.com/LairdCP/BL653-Applications

Key specifications of the LM20BIM7 are as follows in

Table 9.

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Table 9: LM20BIM7 Specifications

Output type	Analogue output
Accuracy at 30ºC	±1.5ºC ±4ºC (max)
Accuracy at 40ºC to +85ºC	approx. ±2.5ºC ±5ºC (max)
Power supply voltage range	+2.4 V to 5.5 V
Current Drain	10 uA (max)
Output impedance	160 Ohms (max)

The LM20BIM7 datasheet states the relationship of Temperature (T) to Voltage output (Vo) can be approximated as a linear equation (for temperature range of -40ºC to +85ºC):

Vo(mV) = -11.67mV/ºC x T + 1858.3

gives the following calculated Vo versus temperature:

Table 10: LM20BIM7 Temperature to Voltage Output relationship

Temperature (T)	Typical Voltage
+80ºC	+924.7 mV
+70ºC	+1041.4 mV
+60ºC	+1158.1 mV
+50ºC	+1274.8 mV
+40ºC	+1391.5 mV
+30ºC	+1508.2 mV
+20ºC	+1624.9 mV
+10ºC	+1741.6 mV
+0ºC	+1858.2 mV
-10ºC	+1975.0 mV
-20ºC	+2091.7 mV
-30ºC	+2208.4 mV

8.2.2 I2C Sensor (RTC Chip)

The I2C RTC chip (U16) allows the BL653 I2C interface to be tested. The output of the RTC chip (U16) is on the I2C bus and is by default connected to the BL653 module via jumpers on J17 and J21.

Table 11: I2C RTC chip BL653 I2C signal mappings

I2C RTC EEPROM (U16)	BL653 module (U5) SIO	Comments
(U16 pin6) RTC_SCL	(U5 pin38) SIO_27	Fit jumper on J17 to route
(U16 pin5) RTC_SDA	(U5 pin36) SIO_26	Fit jumper on J21 to route

Fitting a jumper on J17 routes the RTC_SCL signal to BL653 SIO_27 and fitting a jumper on J21 routes the RTC_SDA to BL653 SIO_26.

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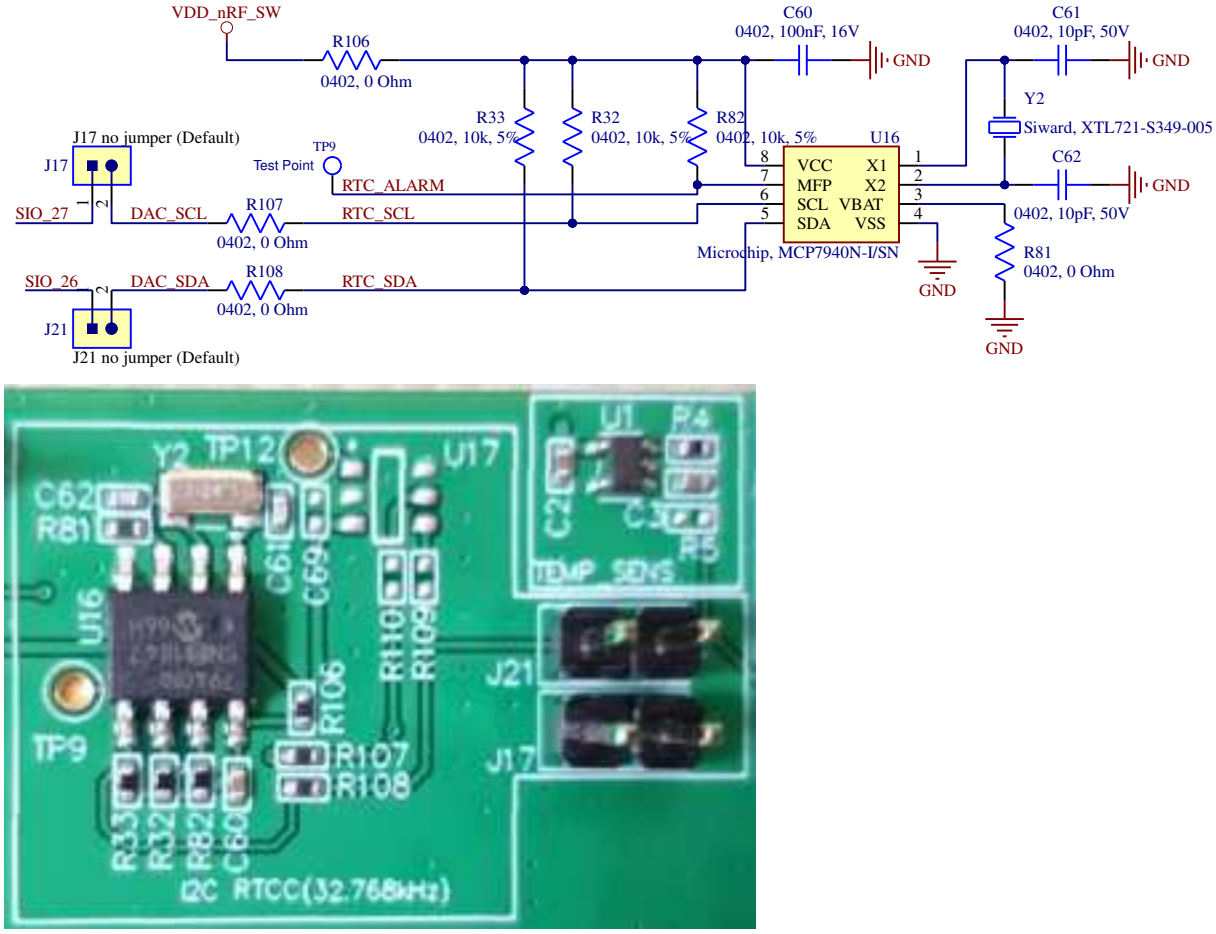

Figure 15: I2C device RTC chip schematic and PCB

To test the BL653 I2C interface, use *smart*BASIC application *rtcs.erver.sb* in the GitHub *smart*BASIC sample application repository on the BL653 product page at https://github.com/LairdCP/BL653-Applications. This application runs on the BL653 and can be used with an Android phone (requires an app such as nRF connect, https://play.google.com/store/apps/details?id=no.nordicsemi.android.mcp&hl=en_GB) or another BT900/BL620/BL652/BL653 loaded with "*rtcc.lient.sb*".

The *smart*BASIC application "*rtcs.erver.sb*" is a BLE RTC server, and it advertises the current time (which it gets from the I2C RTC chip (U4)).

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8.2.3 SPI Device EEPROM

The SPI EEPROM device (U2) is connected to the BL653 SPI pins **directly**. By default, the BL653 Module SIO_44 (used as the SPI_CS) is connected to EEPROM (U2) slave select line. Table 12 lists signal mappings of how the SPI EEPROM (U2) is wired to BL653 SIO pins.

Table 12: SPI EEPROM to BL653 SPI signal mappings

SPI EEPROM (U2)	BL653 (U5) SIO	Comments
(U2pin6) Eeprom_SCK_SIO_41	(U5pin30) SIO_41	
(U2pin2) Eeprom_MISO_SIO_04	(U5pin34) SIO_04	
(U2pin5) Eeprom_MOSI_SIO_40	(U5pin32) SIO_40	
(U2pin1) Eeprom_CS_SIO_44	(U5pin54) SIO_44	Configure SIO_44 as an output and drive output low in *smart*BASIC application to select SPI slave (SPI EEPROM U2). Remember SIO_44 on BL653 is connected to Nordic nRF52833 P0.23.

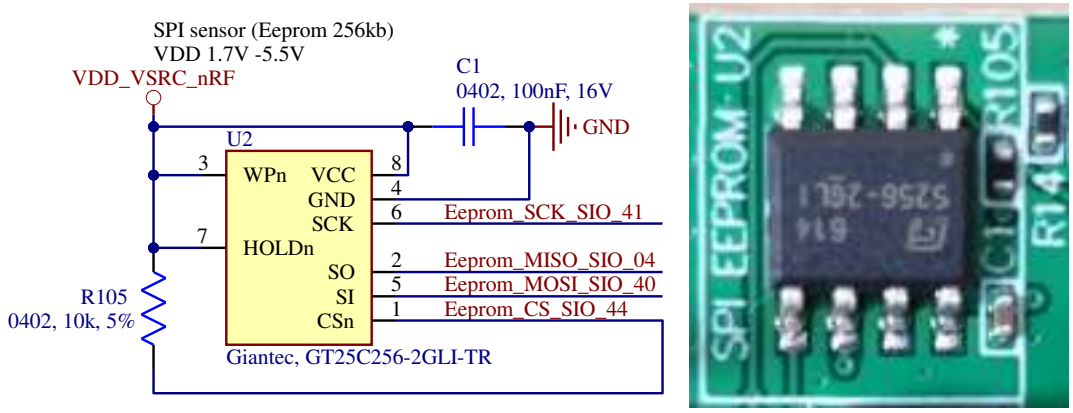

Figure 16: SPI EEPROM schematic and PCB

For a working example of the BL653 SPI interface using the SPI EEPROM (U2), a *smart*BASIC application for this will be available in the future in the GitHub *smart*BASIC sample application repository on the BL653 product page at https://github.com/LairdCP/BL653-Applications.

8.2.4 Push Button and LED Connected to BL653

The two push buttons and two LEDs on the BL653 are connected to dedicated SIOs of the BL653 module.

Table 13: LED's and Buttons to BL653 SIO signal mappings

Part	BL653 (U5) SIO	Comments
LED1 (D1)	Pin 20 SIO_13 (via header J26)	To connect LED1 to SIO_13, fit jumper in J26
LED2 (D2)	Pin 22 SIO_14 (via header J37)	To connect LED2 to SIO_14, fit jumper in J37
LED3 (D3)	Pin 18 SIO_15 (via header 45)	To connect LED3 to SIO_15, fit jumper in J45
LED4 (D4)	Pin 21 SIO_16 (via header J39)	To connect LED4 to SIO_16, fit jumper in J39
Button 1 (SW1)	Pin 27 SIO_11	
Button 2 (SW2)	Pin 28 SIO_12	
Button 3 (SW9)	Pin 10 SIO_24	
Button 4 (SW10)	Pin 8 SIO_25	Remember SIO_25 on BL653 is connected to Nordic nRF52833 P0.22.

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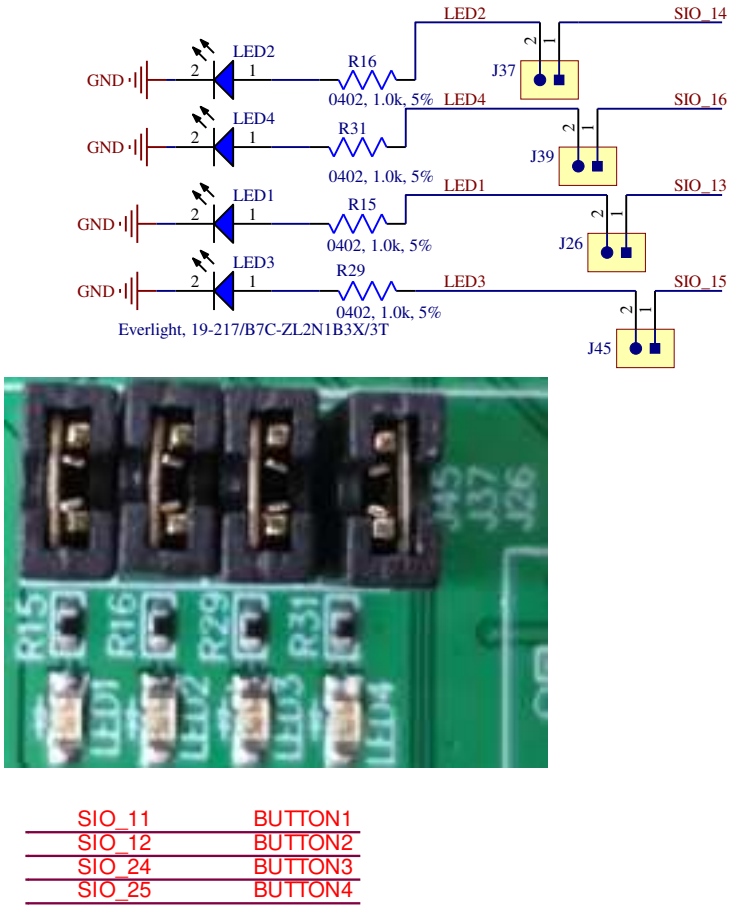

Figure 17: LEDs and Buttons schematic and PCB

The buttons (BUTTON1 and BUTTON2 for example) have no external pull-up resistor, so to use the buttons, the SIO_11 and SIO_12 pins must be configured as inputs with internal pull-up resistors (which is the default). The following *smart*BASIC lines configure the pull-ups:

```
rc = GPIOSETFUNC(11,1,4)     //sets SIO_11 (Button1) as a digital in, strong pull up
rc = GPIOSETFUNC(12,1,4)     //sets SIO_12 (Button2) as a digital in, strong pull up
```

Refer to the *smart*BASIC application script example "*btn.button.led.test.sb*" in the GitHub *smart*BASIC sample application repository on the BL653 product page at https://github.com/LairdCP/BL653-Applications.

The LEDs are active high, meaning that writing a logical one ("1") to the output pin illuminates the LED.

One example of when push buttons can be used is when a *smart*BASIC application is written to simulate a generic data profile. Push buttons can then be pressed to increment and decrement, such as a heart rate.

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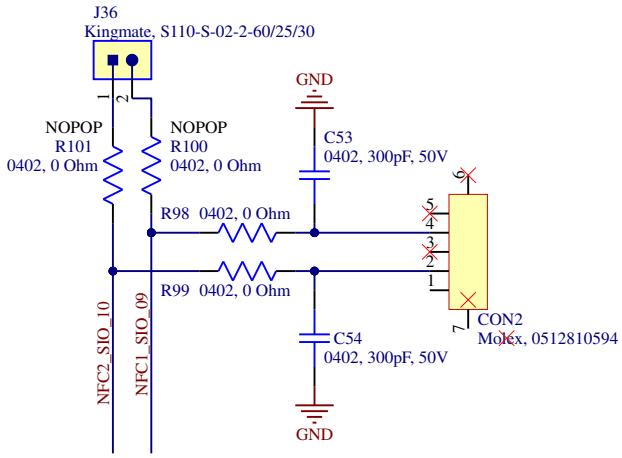
8.2.5 NFC External Antenna Connector and NFC Antenna RF Matching Circuit

The NFC antenna input connector (CON2) allows the Laird supplied flex-PCB NFC antenna to be plugged in. The BL653 module NFC circuit uses two pins, pin 59 (**NFC1/SIO_9**) and pin 57 (**NFC2/SIO_10**) to connect the antenna. These pins are shared with GPIOs (**SIO.09** and **SIO.10).** BL653 NFC pins are enabled by default. NFC can be disabled via *smart*BASIC application. Pin 59 (**NFC1/SIO_9**) and pin 57 (**NFC2/SIO_10**) are configured by default on the development board schematic to use NFC antenna, but if pin 59 (**NFC1/SIO_9**) and pin 57 (**NFC2/SIO_10**) are needed as normal GPIOs, R98 and R99 must be removed and R100 and R101 must be shorted by 0R.

C53 (300pF) and C54 (300pF) are RF tuning elements for the flexi-PCB NFC antenna.

Table 14: NFC input BL653 SIO signal mappings

BL653 (U5) SIO	Bring out SIO_9 and SIO_10 to NFC antenna connector (CON2)	Bring out SIO_9 and SIO_10 to Header connector (J36)
pin 59 (**NFC1/SIO_9**)	Fit R98 0R (default) Remove R100 0R (default)	Remove R98 0R Fit R100 0R
pin 57 (**NFC2/SIO_10**)	Fit R99 0R (default) Remove R101 0R (default)	Remove R99 0R Fit R101 with 0R



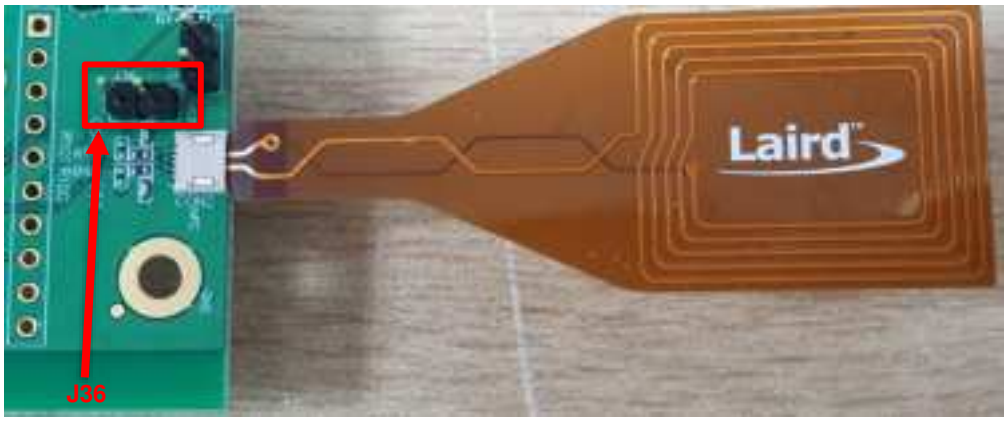


Figure 18: NFC antenna RF matching circuit, NFC antenna connector schematic and NFC plugged into connector CON2

The *smart*BASIC application *nfc.all.launch.sb* in the GitHub *smart*BASIC sample application repository on the BL653 product page at https://github.com/LairdCP/BL653-Applications exercises the following over the BL653 NFC: NFC:

- On Android NFC enabled devices – Opens Laird Toolkit or shows it in the Google Play store if not installed
- On Windows NFC enabled devices – Opens the calculator
- On other NFC enabled devices – Shows the Laird website or text saying ***this is a BL653***

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8.2.6 Optional 32.76 kHz Crystal

The BL653 on-chip 32.768kHz RC oscillator provides the standard accuracy of ±250 ppm, with calibration required every eight seconds (default) to stay within ±250 ppm.

The BL653 also allows, as an option, to connect an external higher accuracy (±20 ppm) 32.768 kHz crystal to the BL653-SX-xx pins SIO_01/XL2 (pin 41) and SIO_00/XL1 (pin 42). This provides improved protocol timing and helps with radio power consumption in the system standby doze/deep sleep modes by reducing the time that the Rx window must be open.

To connect the optional external 32.76kHz crystal oscillator circuit to the BL653 module, remove R127 and R128 and short SB8 and short SB9.

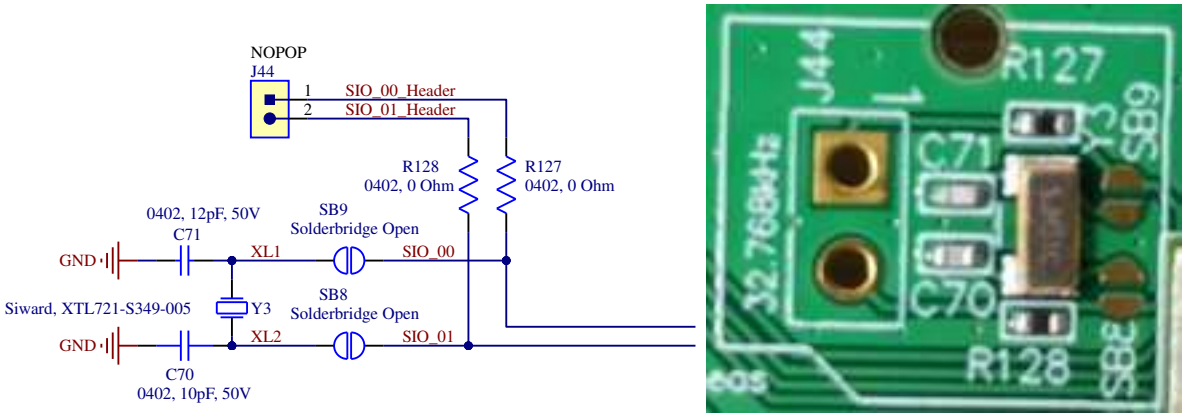

Figure 19: Optional external 32.768kHz crystal circuit schematic and PCB

A *smart*BASIC application will be available in the future in the GitHub *smart*BASIC sample application repository at: https://github.com/LairdCP/BL653-Applications.

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9 Other Features

9.1 Current Consumption Measurement

A removable jumper (on J7 and J9) is provided to break the power supply line directly to the module, allowing you to measure current consumption. For normal operation, the jumper on J7 (and J9) must be fitted (and is fitted by default).

IMPORTANT: To achieve the optimal power consumption of the BL653 series module on the development board, see the "*lp.low.power.deep.sleep.sb*" file in the GitHub *smart*BASIC sample application repository on the BL653 product page at https://github.com/LairdCP/BL653-Applications.

Note: This measures the current consumption of the **BL653** series module ONLY.

The current drawn by the BL653 series module can be monitored on the development board. Figure 20 shows the schematic and location of measuring points on the PCB related to current measurements.

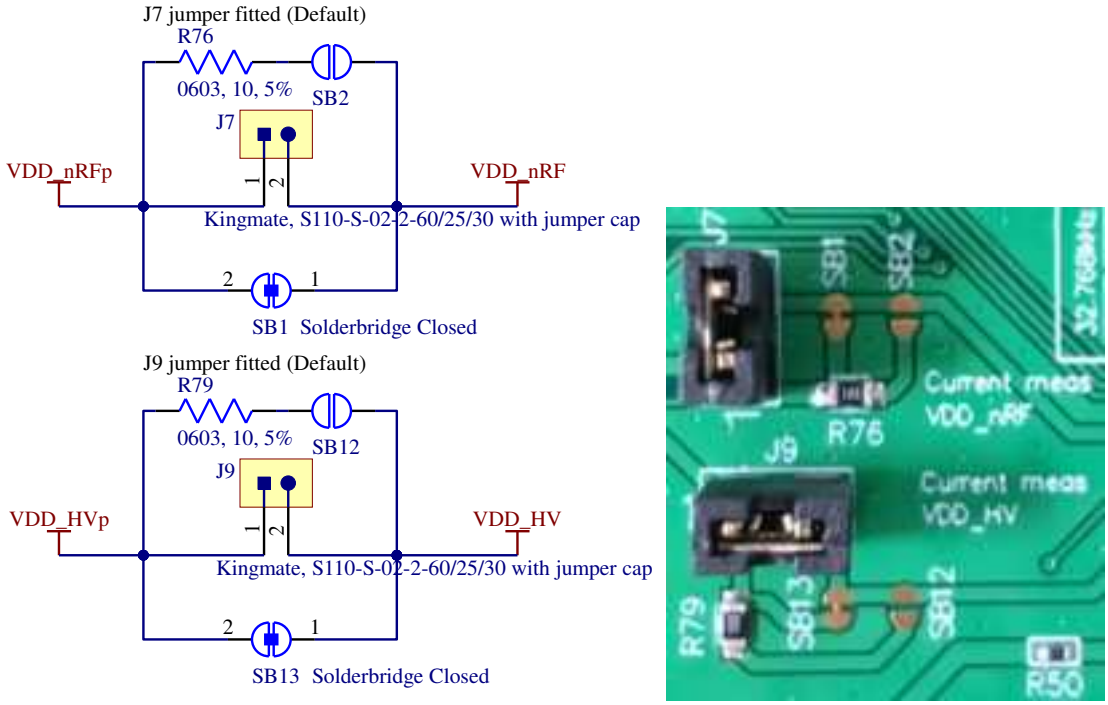

Figure 20: Current measurement schematic and PCB

There are two primary ways to measure the current consumption:

- **Using Ammeter –** Cut solder bridge SB1 and connect an ampere meter between the two pins of J7 pins 1-2. This monitors the current directly. This is when BL653 is powered using the normal voltage Mode (BL653 operated VDD pin). If the BL653 is powered using the high voltage Mode (BL653 operated VDD_HV pin), then only cut solder bridge SB13 and connect an ampere meter between the two pins of J9 (pins 1-2).
- **Using Oscilloscope –** The open solder bridge SB2 first needs to be shorted with solder, then the on-board 10 Ohm resistor R76 which is mounted across J7 pins 1-2 can be used as current sense resistor. Connect an oscilloscope or similar with two probes on the pins on the J7 connector and measure the differential voltage drop. The voltage drop is proportional with current consumption. If the 10 Ohm resistor is chosen, 10 mV equals 1mA.

  This method allows the dynamic current consumption waveforms to be shown on an oscilloscope as the BL653 radio operates. This can provide insight into power optimization.
- **Power Profiler Kit (PPK) from Nordic –** For more details, refer to http://www.nordicsemi.com/eng/Products/Power-Profiler-Kit/(language)/eng-GB

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10 APPENDIX

10.1 Coin Cell Insertion

To insert the coin cell, follow these steps:

1. Push the coin cell against positive contact spring of holder J34 (on the back side of the dev board).

Note: The coin cell sits below the positive contact spring (as shown with arrow).

Figure 21: Inserting the coin cell (step 1)

3. Push the coin cell down into the holder (J34).

Figure 22: Inserting the coin cell (step 2)

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10.2 Coin Cell Removal

To remove the coin cell, follow these steps:

1. Hold down the coin cell holder (J34) at the corners.
2. Use a screwdriver in the position shown in picture below, to gently remove the coin cell from the coin cell holder (J34). This is the correct method to remove coin-cell from holder (J34).

Note: Due to tight fit of coin cell in the coin-cell holder (J34), care should be taken prevent damage to the J34 land pads.

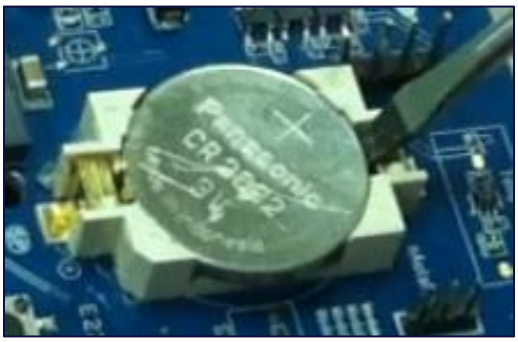

Figure 23: Removing the coin cell (step 2)

11 Additional Documentation

Laird offers a variety of documentation and ancillary information to support our customers through the initial evaluation process and ultimately into mass production. Additional documentation can be accessed from the Documentation tab of the Laird BL653 Product Page.

For any additional questions or queries, or to receive technical support for this Development Kit or for the BL653 module series, please contact Embedded Wireless Solutions Support: https://www.lairdconnect.com/resources/support