Device Migration Guidelines

Agilex™ 3 FPGAs and SoCs C-Series

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Contents

1. Introduction

This application note provides migration guidelines for Agilex™ 3 C-Series devices. The guidelines covers various device features to help you plan your Quartus® Prime software and board design up front to ensure seamless migration between devices within the same package.

Figure 1. Agilex 3 C-Series Device

	Product Line	A3C025[1]	A3C050	A3C065	A3C100	A3C135
Resources	Specification Options[2]	Y, Z	Y, Z	Y, Z	W, Y, Z	W, Y, Z
	Logic elements (LEs)	25,075	47,200	65,490	100,300	135,110
	Adaptive logic modules (ALMs)	8,500	16,000	22,200	34,000	45,800
	ALM registers	34,000	64,000	88,800	136,000	183,200
	M20K memory blocks	65	123	169	262	353
	M20K memory size (Mb)	1.27	2.40	3.30	5.12	6.89
	MLAB memory count	450	800	1,050	2,000	2,300
	MLAB memory size (Mb)	0.27	0.49	0.64	1.22	1.40
	I/O PLL	2	2	2	4	4
	Fabric-feeding IOPLL[3]	5	5	5	8	8
	Variable-precision digital signal processing (DSP) blocks	34	65	88	138	184
	18 x 19 multipliers	68	130	176	276	368
	Peak INT8 (TOPS)	0.47	0.90	1.21	1.90	2.54
Maximum Available Device Resources	LVDS pairs at 1.25 Gbps	48	48	48	96	96
	LPDDR4 interfaces (x32)	0	1	1	2	2
	MIPI D-PHY interface	0	7	7	14	14
	Differential (RX or TX) pairs at 12.5 Gbps	0	0	0	4	4
	PCIe* 3.0 x4 instance	0	0	0	1	1
	High-speed I/O (HSIO)	96	96	96	192	192
	High-voltage I/O (HVIO)	160	160	160	200	200
	Secure Device Manager (SDM)	Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, and physical anti-tamper support				
	Hard processor system (HPS)	NA			Multi-core with 32-bit/64-bit dual-core Arm Cortex*-A55 processor up to 800 MHz with 32 KB I/D cache and 128 KB L2 cache, and up to 1 MB L3 cache, multi-channels direct memory access (DMA), 512 KB on-chip RAM, USB 3.1 x1, USB 2.0 OTG x2, TSN MAC x3, UART x2, SPI M x2, SPI S x2, I3C x2, I2C x5, NAND x1, SDMMC x1, oscillator timer x2, SP timer x2, watchdog x5, and GPIO x2.	
	Transceiver	NA			PCIe hard IP up to PCIe 3.0 x4 endpoint (EP) and root port (RP) Transceiver channel count: up to 4 channels at 12.5 Gbps (NRZ) Ethernet IP: up to 4 x10 GbE hard IP (MAC, PCS, and FEC)	

Notes:
1. A3C025 does not support EMIF and MIPI.
2. Specification code definition:

Code	HPS	Crypto	EMIF, MIPI, PUF, SPDM Attestation
W	Yes	Yes	Yes
Y	No	No	Yes
Z	No	No	No

EMIF: External Memory Interface
MIPI: Mobile Industry Processor Interface
PUF: Physical Unclonable Function
SPDM: Security Protocol and Data Model

3. The fabric-feeding IOPLL count including system PLL at the transceiver bank. The system PLL can be repurposed for core fabric usage if not used for the transceiver.

Note: Refer to the *Agilex 3 FPGAs and SoCs Device Overview* for Ordering Part Number (OPN) Structure details.

Figure 2. Package Options, Migrations, and I/O Pins

- The arrows indicate the package migration paths. The shades represent the devices included in each path.
- Migration path shown includes both vertical and conditional migration scenario. Refer to *Migration Scope* for more details.
- To achieve full I/O(1) migration across devices in the same migration path, restrict I/Os and transceivers utilization to match the device with the lowest I/O and transceiver counts.

Series	Specification	Device	Package Key: HVIO / HSIO (LVDS) / HPSIO / Transceivers				
			Ball Pitch: 0.5 mm Grid Array Pattern: Standard MBGA: Micro Fineline BGA		Ball Pitch: Variable(1)(2) Grid Array Pattern: Variable Pitch BGA VPBGA: Variable Pitch BGA		
			M12A 484-pin MBGA 12 mm × 12 mm	**M16A** 896-pin MBGA 16 mm × 16 mm	**B18A** 474-pin VPBGA 18 mm × 18 mm	**B18B** 538-pin VPBGA 23 mm × 23 mm	**B23C** 931-pin VPBGA 23 mm × 23 mm
C-Series	Y; Z	A3C 025	160 / 72 (36) / 0 / 0		160 / 48 (24) / 0 / 0	160 / 96 (48) / 0 / 0	
		A3C 050	160 / 72 (36) / 0 / 0		160 / 48 (24) / 0 / 0	160 / 96 (48) / 0 / 0	
		A3C 065	160 / 72 (36) / 0 / 0		160 / 48 (24) / 0 / 0	160 / 96 (48) / 0 / 0	
	W; Y; Z	A3C 100		40 / 192 (96) / 48 / 4	160 / 48 (24) / 0 / 0		200 / 144 (72) / 48 / 4
		A3C 135		40 / 192 (96) / 48 / 4	160 / 48 (24) / 0 / 0		200 / 144 (72) / 48 / 4

Notes:
(1) The Variable Pitch BGA (VPBGA) packaging is compatible with Type III PCBs that use the design rules equivalent to 0.8 mm ball pitch and standard plated through hole (PTH) vias.
(2) The VPBGA ball pitch is variable and it helps to ease signal routing. For more information, contact your local sales representative.

Related Information

- Migration Scope on page 5
- Agilex™ 3 FPGAs and SoCs Device Overview

(1) — HSIO – High-speed I/O
— HVIO – High voltage I/O
— LVDS – Low voltage differential signaling channels

2. Migration Scope

2.1. Migration Supported Packages

Devices within package M12A, M16A, B18A, B18B, and B23C in the Agilex 3 C-Series family support migration between the same packages. Refer to Package Options, Migrations, and I/O Pins for details of device availability on each package.

2.2. Migration Scenarios

2.2.1. Vertical Migration

Vertical migration is a migration scenario which has no impact on board design requirements when migrating between different devices within the same package. For devices that you plan to migrate under this scenario, you can utilize the *Quartus Prime Software Design Migration* features to guide you on the design migration.

Table 1. Examples of Vertical Migration Scenarios for Each Package

Package	Migration From	Migration To	Note
M12A	A3CY050	A3CY065	Migrating between same device specification. No HPS is supported on either device. Both device support EMIF, MIPI, PUF, and Attestation.
M16A	A3CW100	A3CW135	Migrating between same device specification. Both devices support the same HPS core and number of transceiver channels. Both device support EMIF, MIPI, PUF, and Attestation.
B18A	A3CZ050	A3CZ065	Migrating between same device specification. No HPS is supported on either device. No EMIF, MIPI, PUF, and Attestation support on either device.
B18B	A3CZ025	A3CZ065	Migrating between same device specification. No HPS is supported on either device. No EMIF, MIPI, PUF, and Attestation support on either device
B23C	A3CW100	A3CW135	Migrating between same device specification. Both devices support the same HPS core and number of transceiver channels. Both devices support EMIF, MIPI, PUF, and Attestation.

Related Information

Quartus Prime Software Design Migration on page 24

2.2.2. Conditional Migration

You can migrate to utilize features offered in different devices within the same package using the same board by following certain board design guidelines. For devices you plan to migrate under the category of Conditional Migration, you must consider the board design upfront to support your future migration device.

Table 2. Examples of Conditional Migration Scenarios for Each Package

Package	Migration From	Migration To	Note
M12A	A3CY050	A3CZ065	Migrating from EMIF, MIPI, PUF, and Attestation supported to a not supported device.
M16A	A3CW100	A3CY135	Migrating from HPS supported device to non-HPS supported device.
B18A	A3CZ065	A3CW100	Migrating from non-HPS supported device to HPS supported device. Migrating from EMIF, MIPI, PUF, and Attestation not supported to a supported device.
B18B	A3CY050	A3CZ065	Migrating from EMIF, MIPI, PUF, and Attestation supported to a not supported device.
B23C	A3CW100	A3CZ135	Migrating from HPS supported device to non-HPS supported device. Migrating from EMIF, MIPI, PUF, and Attestation supported to a not supported device.

Note: Refer to the *Considerations for Migration Planning* section to understand the required considerations when planning migration to devices with conditional migration scenarios.

Note: Refer to the *Functional Area* section for the details of board design guidelines.

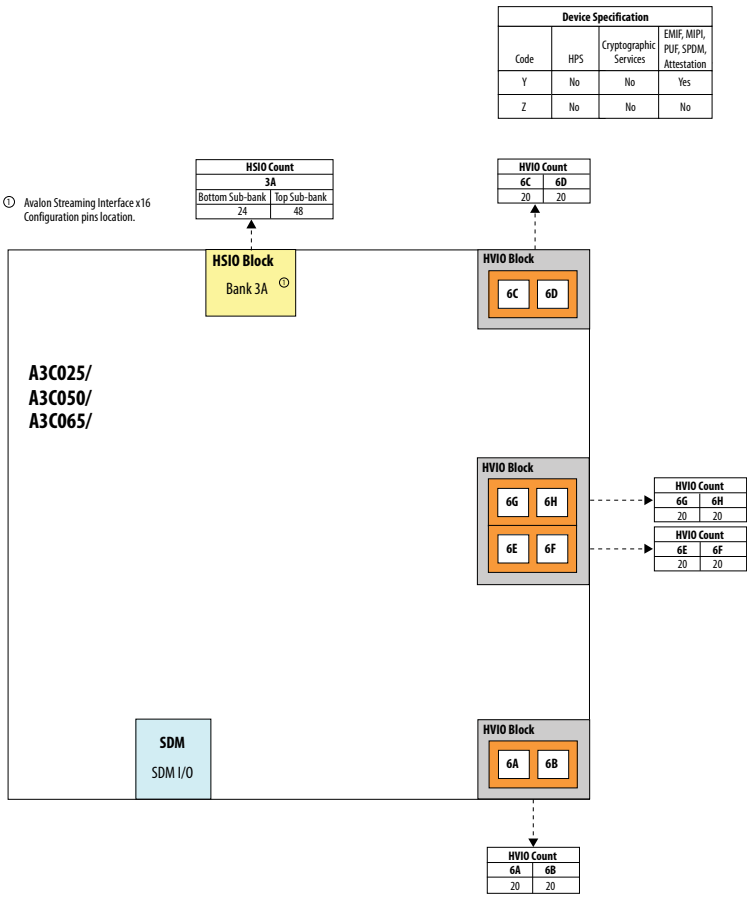
Related Information

- Considerations for Migration Planning on page 7
- Functional Area on page 17

2.3. Considerations for Migration Planning

2.3.1. Package M12A

Figure 3. Consideration Details



The M12A package is available in Device Specification of option Y and Z. Transceiver and HPS are not supported in this package. Support for EMIF and MIPI depends on the Device Specification of the selected device. All devices within the M12A package are available with the same HVIO and HSIO count. The considerations taken when migrating between this package depends on which device and Device Specification you are migrating to.

Refer to the following examples to understand the areas that require consideration when planning for migration within the M12A package.

Examples:

- If you are migrating within Device Specification Z of A3C025 to A3C065 devices, neither device supports HPS, EMIF, or MIPI. The resource count for HVIO and HSIO are the same, so this is categorized as Vertical Migration which has no impact on board design guidelines.
- If you are migrating from Device Specification Z of A3C065 to Device Specification Y of A3C065 devices, then you are migrating from devices with unsupported EMIF and MIPI features to a device that supports EMIF and MIPI.

The following table summarizes the areas that require consideration when planning migration within the M12A package. Refer to Functional Area on page 17 for more details on each area.

Table 3. M12A Package Consideration Requirement

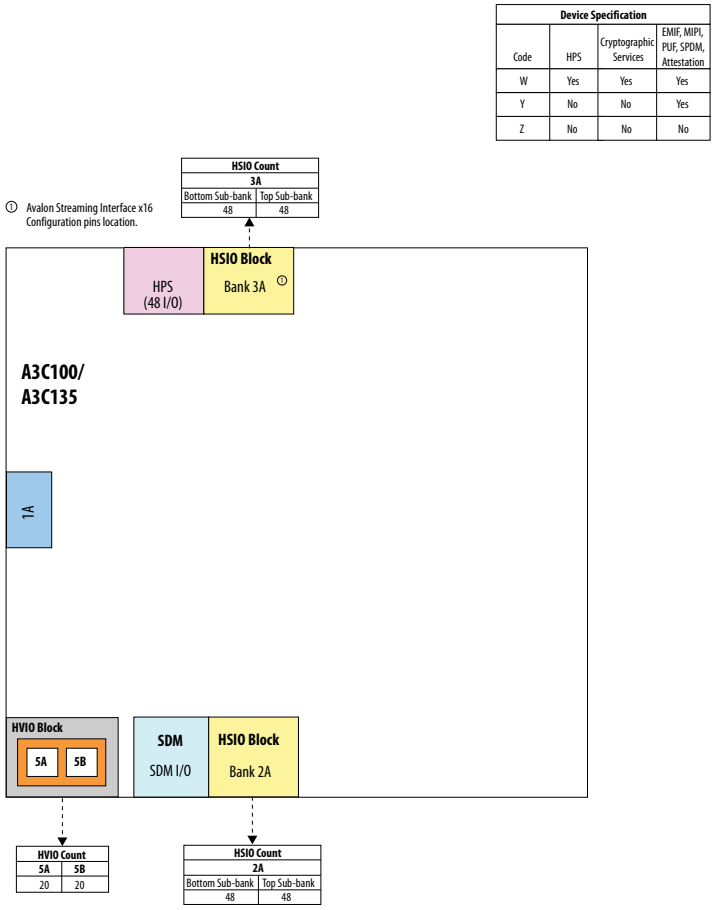
Area	Consideration Requirement
I/O	No
LVDS SERDES	Yes, refer to the *LVDS SERDES* section for more details.
Configuration	No
EMIF	Yes, refer to the *External Memory Interface* section for more details.
MIPI	Yes, refer to the *MIPI D-PHY* section for more details.
HPS	NA
Transceiver	NA
Power	No
Sensor	Yes, refer to the *Sensor* section for more details.

Related Information

- LVDS SERDES on page 18
- External Memory Interface on page 19
- Sensor on page 22
- MIPI D-PHY on page 20

2.3.2. Package M16A

Figure 4. Consideration Details



The M16A package is available with all Device Specification of W, Y, and Z. Support for HPS, EMIF, and MIPI depends on the Device Specification of the selected device. All devices within the M16A package are available with the same HVIO and HSIO resource count. The number of transceiver channels supported is the same across devices within this package. The considerations taken when migrating between this package depends on which device and Device Specification you are migrating to.

Refer to the following examples to understand the areas that require consideration when planning for migration within the M16A package.

Examples:

- If you are migrating from Device Specification Z of A3C135 to Device Specification Y of A3C100 devices, then you are migrating from devices with unsupported EMIF and MIPI features to a device that supports EMIF and MIPI.
- If you are migrating from Device Specification Y of A3C135 to Device Specification W of A3C100 devices, then you are migrating from non-HPS supported device to HPS supported device. EMIF and MIPI features are supported in both devices.
- If you are migrating from Device Specification Z of A3C135 to Device Specification W of A3C100 devices, then you are migrating from devices with unsupported EMIF and MIPI features to a device that supports EMIF and MIPI, as well as non-HPS supported device to HPS supported device.

The following table summarizes the areas that require consideration when planning migration within the M16A package. Refer to Functional Area on page 17 for more details on each area.

Table 4. M16A Package Consideration Requirement

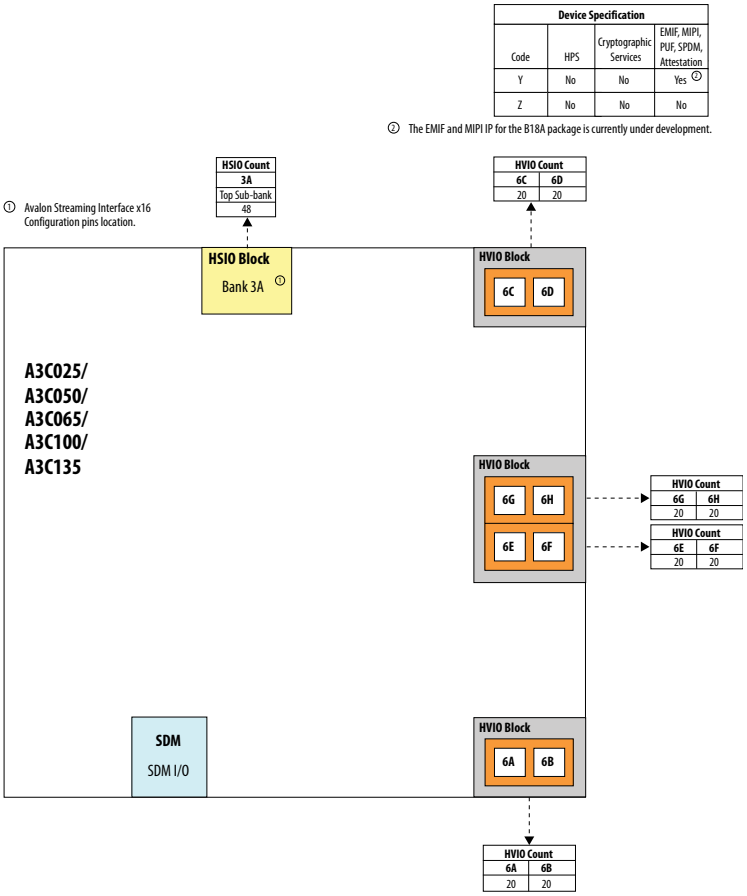
Area	Consideration Requirement
I/O	No
LVDS SERDES	Yes, refer to the *LVDS SERDES* section for more details.
Configuration	No
EMIF	Yes, refer to the *External Memory Interface* section for more details.
MIPI	Yes, refer to the *MIPI D-PHY* section for more details.
HPS	Yes, refer to the *HPS* section for more details.
Transceiver	No
Power	No
Sensor	Yes, refer to the *Sensor* section for more details.

Related Information

- LVDS SERDES on page 18
- HPS on page 21
- External Memory Interface on page 19
- Sensor on page 22
- MIPI D-PHY on page 20

2.3.3. Package B18A

Figure 5. Consideration Details



The B18A package is available with Device Specification of option Y and Z. Transceiver and HPS are not supported in this package. Support for EMIF and MIPI depends on the Device Specification of the selected device. The considerations taken when migrating between this package depends on which device and Device Specification you are migrating to. The B18A package is available with the same HVIO and HSIO count. There is an output pin utilization limit consideration required for HVIO pin.

Refer to the following examples to understand the areas that require consideration when planning for migration within the B18A package.

Examples:

- If you are migrating within Device Specification Z of A3C065 to A3C135 devices, neither device supports HPS, EMIF, or MIPI. The resource count for HVIO and HSIO are the same. This is categorized as Vertical Migration which has no impact on board design guidelines.
- If you are migrating from Device Specification Z of A3C065 to Device Specification Y of A3C135 devices, then you are migrating from devices with unsupported EMIF and MIPI features to supported devices.
- If you are migrating from A3C065 devices to A3C135 device, then you are migrating from devices that do not have any output pin utilization limit on the HVIO bank to devices that do have an output pin utilization limit. This requirement applicable for both Y and Z Device Specification of this package.

The following table summarizes the areas that require consideration when planning migration within the B18A package. Refer to Functional Area on page 17 for more details on each area.

Table 5. B18A Package Consideration Requirement

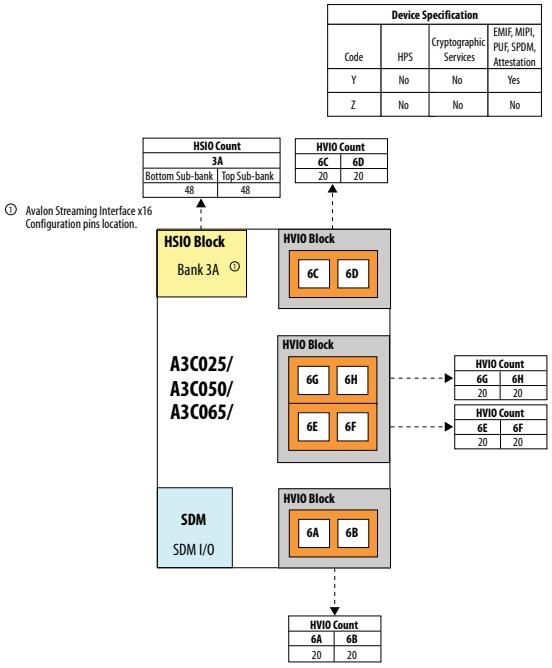
Area	Consideration Requirement
I/O	Yes, refer to the *I/O* section for more details.
LVDS SERDES	Yes, refer to the *LVDS SERDES* section for more details.
Configuration	No
EMIF	Yes, refer to the *External Memory Interface* section for more details.
MIPI	Yes, refer to the *MIPI D-PHY* section for more details.
HPS	NA
Transceiver	NA
Power	No
Sensor	Yes, refer to the *Sensor* section for more details.

Related Information

- LVDS SERDES on page 18
- I/O on page 17
- External Memory Interface on page 19
- Sensor on page 22
- MIPI D-PHY on page 20

2.3.4. Package B18B

Figure 6. Consideration Details



The B18B package is available with Device Specification of option Y and Z. Transceiver and HPS are not supported in this package. Support for EMIF and MIPI depends on the Device Specification of the selected device. The B18B package is available with the same HVIO and HSIO count. The considerations taken when migrating between this package depends on which device and Device Specification you are migrating to.

Refer to the following examples to understand the areas that require consideration when planning for migration within the B18B package.

Examples:

- If you are migrating within Device Specification Z of A3C025 to A3C065 devices, neither device supports HPS, EMIF, or MIPI. The resource count for HVIO and HSIO are the same, so this is categorized as Vertical Migration which has no impact on board design guidelines.
- If you are migrating from Device Specification Z of A3C065 to Device Specification Y of A3C065 devices, then you are migrating from devices with unsupported EMIF and MIPI features to a device that supports EMIF and MIPI.

The following table summarizes the areas that require consideration when planning migration within the B18B package. Refer to Functional Area on page 17 for more details on each area.

Table 6. B18B Package Consideration Requirement

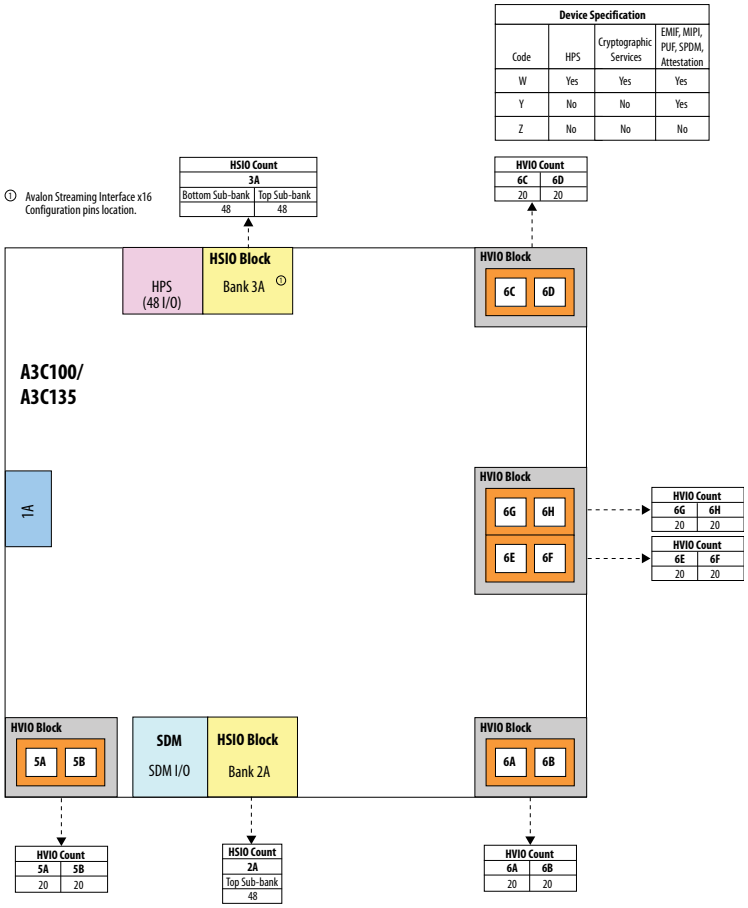
Area	Consideration Requirement
I/O	No
LVDS SERDES	Yes, refer to the *LVDS SERDES* section for more details.
Configuration	No
EMIF	Yes, refer to the *External Memory Interface* section for more details.
MIPI	Yes, refer to the *MIPI D-PHY* section for more details.
HPS	NA
Transceiver	NA
Power	No
Sensor	Yes, refer to the *Sensor* section for more details.

Related Information

- LVDS SERDES on page 18
- External Memory Interface on page 19
- Sensor on page 22
- MIPI D-PHY on page 20

2.3.5. Package B23C

Figure 7. Consideration Details



The B23C package is available with Device Specification of option W, Y, and Z. Support for HPS, EMIF, and MIPI depends on the Device Specification of the selected device. The B23C package is available with the same HVIO and HSIO count. The number of transceiver channels supported is the same across devices within this package. The considerations taken when migrating between this package depends on which device and Device Specification you are migrating to.

Refer to the following examples to understand the areas that require consideration when planning for migration within the B23C package.

Examples:

- If you are migrating from Device Specification Z of A3C135 to Device Specification Y of A3C100 devices, then you are migrating from devices with unsupported EMIF and MIPI features to a device that supports EMIF and MIPI.
- If you are migrating from Device Specification Y of A3C135 to Device Specification W of A3C100 devices, then you are migrating from non-HPS supported device to HPS supported device. EMIF and MIPI features are supported in both devices.
- If you are migrating from Device Specification Z of A3C135 to Device Specification W of A3C100 devices, then you are migrating from devices with unsupported EMIF and MIPI features to a device that supports EMIF and MIPI, as well as non-HPS supported device to HPS supported device.

The following table summarizes the areas that require consideration when planning migration within the B23C package. Refer to Functional Area on page 17 for more details on each area.

Table 7. B23C Package Consideration Requirement

Area	Consideration Requirement
I/O	No
LVDS SERDES	Yes, refer to the *LVDS SERDES* section for more details.
Configuration	No
EMIF	Yes, refer to the *External Memory Interface* section for more details.
MIPI	Yes, refer to the *MIPI D-PHY* section for more details.
HPS	Yes, refer to the *HPS* section for more details.
Transceiver	No
Power	No
Sensor	Yes, refer to the *Sensor* section for more details.

Related Information

- LVDS SERDES on page 18
- HPS on page 21
- External Memory Interface on page 19
- Sensor on page 22
- MIPI D-PHY on page 20

3. Functional Area

3.1. I/O

3.1.1. HSIO

Direct migration using identical pin planning and location is supported when migrating between devices within package M12A, M16A, B18B, B18A, and B23C because all devices within each of these packages have the same HSIO location availability. There is no change required to the VCCIO_PIO supply of these HSIO banks during migration.

3.1.2. HVIO

Direct migration using identical pin planning and location is supported when migrating between devices within package M12A, M16A, B18B, and B23C because all devices within each of these packages have the same HVIO location availability. There is no change required to the VCCIO_HVIO supply of these HVIO banks during migration.

For the B18A package, there is a HVIO output pin utilization limit on A3C100 and A3C135 devices. Migration between B18A package should consider the achievable amount of output pin utilization limit based on A3C100 and A3C135 devices.

If you are migrating from A3C100 and A3C135 devices to A3C025, A3C050, and A3C065 devices, you can reuse the same I/O planning and location.

Consideration must be taken when you are migrating from A3C025, A3C050, and A3C065 devices to A3C100 and A3C135 devices. Plan your design upfront in A3C025, A3C050, and A3C065 devices to ensure you only utilize the lesser output pins in the HVIO bank based on the achievable output pin count in A3C100 and A3C135 devices. There is no change required to the VCCIO_HVIO supply of these HVIO banks during migration.

Make use of the HVIO Overshoot Estimator to plan your HVIO pin utilization.

Refer to the *Agilex 3 Pin-Out Files* for more information regarding the VCCIO_HVIO pin location for Agilex 3 devices.

Refer to the *General Purpose I/O User Guide: Agilex 3 FPGAs and SoCs* for more information regarding HVIO bank feature, design guideline and HVIO Overshoot Estimator for Agilex 3 Device.

Related Information

- General-Purpose I/O User Guide: Agilex™ 3 FPGAs and SoCs
- Agilex™ 3 Device Pin-Out Files

3.2. LVDS SERDES

The LVDS SERDES IP supports different data rates across speed grades within Agilex 3 Device Specification W, Y and Z. If you are planning to migrate your design across device, you need to pre-plan your design by selecting the data rate range supported by both devices.

For example,

- -6 Speed Grade supported Fmax = 1250 Mbps
- -7 Speed Grade supported Fmax = 1000 Mbps

If you migrate your design from -6 speed grade to -7 speed grade devices, you need to limit the data rate by 1000 Mbps or lower than -7 speed grade supported Fmax.

The LVDS SERDES IP supports multiple I/O standards, features, and data rates in Agilex 3 devices. There is no change needed when Quartus Prime design migration happens between Agilex 3 devices if the supported I/O standards, features, and data rates within Agilex 3 devices are identical.

Refer to the *LVDS SERDES User Guide: Agilex 3 FPGAs and SoCs* for more information regarding the I/O standards and features for Agilex 3 devices.

Refer to the *Agilex 3 FPGAs and SoCs Device Data Sheet* for more information regarding supported data rate for Agilex 3 devices.

Related Information

- Agilex™ 3 FPGAs and SoCs Device Data Sheet
- LVDS SERDES User Guide: Agilex™ 3 FPGAs and SoCs

3.3. Configuration

All Agilex 3 devices include a Secure Device Manager (SDM) to manage FPGA configuration and security. The dedicated configuration pins in Agilex 3 devices support migration within the same package across different devices as shown in Agilex 3 C-Series Device and Package Options, Migrations, and I/O Pins.

All Agilex 3 devices that are designed with the PCIe HIP block located on the left side of the device support the Configuration via Protocol (CvP) application except for A3C025, A3C050, and A3C065 devices, which are not designed with PCIe HIP. The device that supports the CvP application supports migration within the same package across different devices. Refer to all the package diagram documented in Considerations for Migration Planning on page 7 for more details about the product line that supports CvP application.

Refer to the *Device Configuration User Guide: Agilex 3 FPGAs and SoCs* and the *Configuration via Protocol (CvP) Implementation User Guide: Agilex 3 FPGAs and SoCs* for more details on configuration solutions for Agilex 3 devices.

Related Information

- Device Configuration User Guide Agilex™ 3 FPGAs and SoCs
- Configuration via Protocol (CvP) Implementation User Guide: Agilex™ 3 FPGAs and SoCs

3.4. External Memory Interface

3.4.1. External Memory Protocol Supported in Agilex 3 C-Series Devices

Agilex 3 devices EMIF (External Memory Interface) is supported on Device Specification W and Y. The protocol supported is LPDDR4 component memory type.

Refer to the *Agilex 3 FPGAs and SoCs Device Data Sheet* for details.

The maximum number of External Memory Interface for each device depends on the number of HSIO banks and HSIO pin counts available in the device.

Refer to Package Options, Migrations, and I/O Pins for HSIO count availability for each device.

Note: The A3C025 device does not support EMIF.

Related Information

Agilex™ 3 FPGAs and SoCs Device Data Sheet

3.4.2. External Memory Interface Support

This section describes the maximum number of interfaces supported per device.

3.4.2.1. LPDDR4 Interfaces

The following table shows the maximum number of LPDDR4 interfaces per device.

Table 8. LPDDR4

Package	Number of HSIO Banks	HSIO Pins Count	Avalon® Streaming Interface x16 Support	LPDDR4 x32	LPDDR4 x16
B18A	1	48	No	–	1
			Yes	–	–
M12A	1	72	No	–	1
			Yes	–	–
B18B	1	96	No	1	1
			Yes	–	1
B23C	2	144	No	1	2
			Yes	–	2
M16A	2	192	No	2	2
			Yes	1	2

Note: These values correspond to Fabric EMIF instances.

3.4.3. External Memory Interface Migration Consideration

When planning for device migration, ensure the Device Specification selected supports EMIF.

Refer to the migration path for Agilex 3 devices in the *Considerations for Migration Planning* section.

The maximum number of EMIF interfaces supported when migrating to device within the package are the same because all devices within each of these packages have the same number of HSIO counts.

Consideration must be taken when you are migrating to/from devices with Device Specification Z since these devices do not support EMIF. Plan your board design upfront if you are planning to support EMIF with Device Specification W and Y devices in future migration.

Refer to the following documents for more information regarding External Memory Interface for Agilex 3 devices:

- *Agilex 3 Device Pin-Out Files*
- *Pin Connection Guidelines: Agilex 3 FPGAs and SoCs*
- *External Memory Interface Spec Estimator Tool*
- *External Memory Interfaces (EMIF) IP User Guide: Agilex 3 FPGA and SoCs*

Related Information

- Considerations for Migration Planning on page 7
- Pin Connection Guidelines: Agilex™ 3 FPGAs and SoCs
- External Memory Interfaces (EMIF) IP User Guide: Agilex™ 3 FPGAs and SoCs
- Agilex™ 3 Device Pin-Out Files

3.5. MIPI D-PHY

Altera MIPI D-PHY IP is supported in the Agilex 3 Device Specification W and Y. Altera MIPI D-PHY IP is not supported in Agilex 3 Device Specification Z, and also the A3C025 package of Agilex 3 Device Specification Y.

When planning for device migration, ensure the Device Specification selected supports MIPI.

Refer to the migration path for Agilex 3 devices in the Considerations for Migration Planning on page 7.

The maximum number of MIPI interfaces supported when migrating to a device within the package is the same because all devices within each of the packages have the same number of HSIO counts.

Related Information

- Considerations for Migration Planning on page 7
- MIPI D-PHY IP User Guide: Agilex™ 3 and Agilex™ 5 FPGAs
- Agilex™ 3 Device Pin-Out Files

3.6. HPS

Migrate From	Migrate To	Guidelines
Non-HPS supported device	HPS supported device	Provide power to all the HPS power rails and connect the HPS dedicated I/Os. Refer to the *Pin Connection Guidelines: Agilex 3 FPGAs and SoCs* for details.
HPS supported device	Non-HPS supported device	Connect all the HPS power rails to GND. HPS dedicated I/Os must be left floating no connect (NC).

Related Information

Pin Connection Guidelines: Agilex™ 3 FPGAs and SoCs

3.7. Transceiver

No migration guideline is needed when migrating from one Agilex 3 GTS transceiver device to another device, within the supported migration path.

The transceiver resources for the highspeed TX and RX serial data pins, TX PLLs, RX CDR, and System PLL count remain the same for all the device density supported within the same Agilex 3 packages, i.e M16A and B23C packages.

All the GTS transmitter and receiver pins, reference clock pins, CDR clockout pins, and RCOMP_GTS pins are directly migratable from one device density to another device density for the given device package.

Refer to the *GTS Transceiver PHY User Guide: Agilex 3 FPGAs and SOCs* for more information on the transceiver architecture and resources.

3.8. Power

3.8.1. Power Rails for Migration

During Agilex 3 device migration, ensure that power rail connections adhere to the required guidelines.

To ensure a smooth migration, prioritize understanding the key differences between the targeted package and the original package. Focus on reviewing the following areas:

Area	Notes
HPS	Some packages do not offer HPS. For migration of HPS to non-HPS and vice versa, the power rails connection will be different. Refer to the *HPS* section for the power rails connection guide.
I/O	Migration of HSIO and HVIO is possible within all packages as they have the same number of HSIO and HVIO count respectively. Refer to the *I/O* section for the power rails connection guide.
Transceiver	Migration of XCVR is possible within all packages as they have the same number of transceiver count. Refer to the *Pin Connection Guidelines: Agilex 3 FPGAs and SoCs* for more information.

Related Information

- Transceiver on page 21
- I/O on page 17
- HPS on page 21

- Pin Connection Guidelines: Agilex™ 3 FPGAs and SoCs

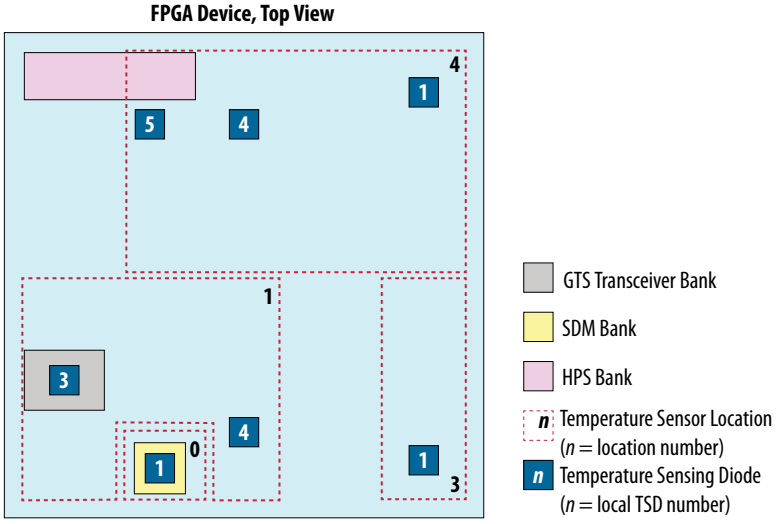
3.9. Sensor

The temperature sensor location support varies between the Agilex 3 devices. If the Quartus Prime design migrates between Agilex 3 devices of different temperature sensor and diode location, the RTL must be updated accordingly to avoid receiving error codes from SDM.

3.9.1. Temperature Sensor Location Support

The following diagram illustrate the temperature sensor and diode location for the Agilex 3 devices. The temperature sensor and diode location availability varies across device density support.

Figure 8. Temperature Sensor Location



The following table list out the temperature sensor and diode location availability across the Agilex 3 devices.

Table 9. Temperature Sensor and Diode Location Availability

The availability of the sensor locations and TSDs varies among Agilex 3 FPGAs. This table lists the availability of temperature sensor resources.

Sensor Location	TSD Location	Agilex 3 Devices	
		A3C 025 A3C 050 A3C 065	A3C 100 A3C 135
0	1	Yes	Yes
1	3	—	Yes
	4	—	Yes
3	1	Yes	Yes

continued...

Sensor Location	TSD Location	Agilex 3 Devices	
		A3C 025 A3C 050 A3C 065	A3C 100 A3C 135
4	1	Yes	—
	4	—	Yes
	5	—	Yes

For more information regarding voltage and temperature sensor for Agilex 3 devices, refer to the *Power Management User Guide: Agilex 3 FPGAs and SoCs*.

Related Information

Power Management User Guide: Agilex™ 3 FPGAs and SoCs

4. Quartus Prime Software Design Migration

This section describes the migration of the Quartus Prime design for Agilex 3 devices. This is achievable through the following methods:

- Changing the device OPN
  - In this method, you have the flexibility to change the location and pin assignments. From the pop-up window, as shown in the following figure, select **YES** and the Quartus Prime software will automatically assign the location assignments and ensure successful migration. If you intend to keep the existing assignments, select **NO** and you can do the assignments manually later.

Figure 9. Removing Location Assignments

- Using the Migration GUI
  - If the design is not flexible for assigned changes, using the Migration GUI helps in checking the compatibility of the devices listed. You can assign the best device listed from the **Compatible migration devices** list in the **Migration Devices** dialog box to the **Selected migration devices** list and compile the design until you can determine which device works best.

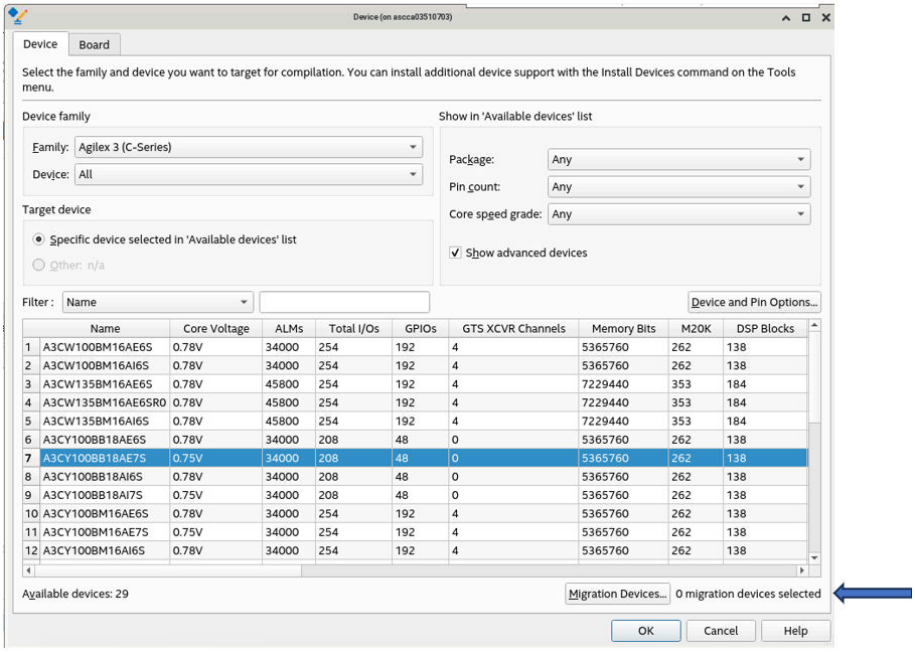
    You can also access the **Pin Migration View** window from the **Pin Planner**. Using this GUI, you can check the comparison table with the migration results between the devices chosen for migration which in return will provide ease in location assignments.

4.1. Migration via Migration GUI for Agilex 3 Devices

The example design used in this migration is a basic design to address the pin assignment and the I/O standard issues.

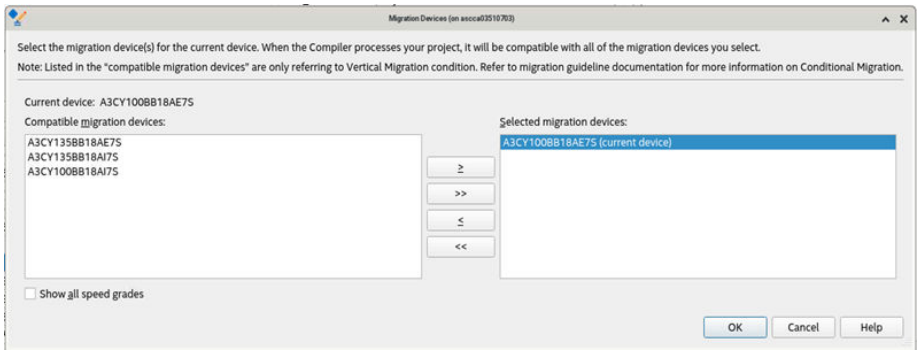
1. To start the device migration, right-click on the device tab in the **Project Navigator** window. This will navigate you to a pop-up window as shown in the following figure.

Figure 10. Device Page



2. Instead of changing the device directly (which will allow the Quartus Prime software to migrate to a new device by removing all the location assignments), select the **Migration Devices** tab located at the bottom right of the window as shown in Device Page. When you select the **Migration Devices** tab, a pop-up window will appear as shown in the following example figure.

Figure 11. Migration Devices



3. In the **Migration Devices** dialog box, click on the arrow buttons to move the migration devices between the **Compatible migration devices** list and the **Selected migration devices** list.

   Compatible devices are listed in the **Compatible migration devices** list. If you want the Quartus Prime software to display all compatible migration devices in the **Compatible migration devices** list regardless of a migration device's speed grade, turn on the **Show all speed grades** option. If you want the Quartus Prime software to display only the compatible migration devices that have the same speed grade as the target device in the **Compatible migration devices** list, uncheck the **Show all speed grades** option.

4. After choosing the device for migration, click **OK**. If you do not specify at least one migration device in the **Migration Devices** dialog box, the field next to **Migration Devices** tab in the **Device** window displays `0 migration devices selected`.
5. After specifying the device to use as a migration device, compile the design. However, the device migration may cause additional constraints. Compilation may fail due to the additional constraints, and the errors prompt you to check the pin assignments in the **Pin Planner** as shown in the following figure.

Figure 12. Pin Planner

Node Name	Direction	Location	I/O Bank	Fitter Location	I/O Standard
out pin_name5	Output	PIN_F27	6D	PIN_F27	1.8-V LVCMOS
in pin_name2	Input	PIN_D26	6D	PIN_D26	1.8-V LVCMOS
out pin_name4	Output	PIN_B14	6C	PIN_B29	2.5-V LVCMOS
out pin_name6	Output	PIN_H27	6D	PIN_H27	1.8-V LVCMOS
in pin_name1	Input	PIN_A14	6C	PIN_A29	2.5-V LVCMOS
in pin_name3	Input	PIN_F26	6D	PIN_F26	1.8-V LVCMOS

6. For the non-migratable I/O pins, leave them as NC. You can set the unused I/O pins as input tri-state in the Intel Quartus Prime software.

   Go to **Device** from the **Project Navigator** window and click on **Devices and Pin Options** as shown in the following figure. In the **Devices and Pin Options** window, under the **Reserve all unused pins** drop-down list, select **As input tri-stated**.

Figure 13. Device Page

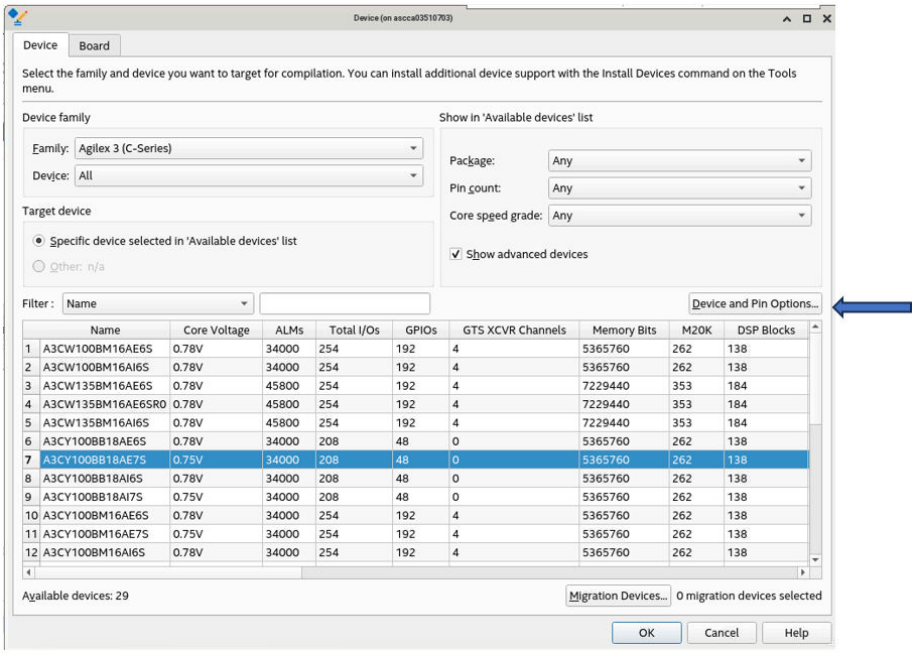
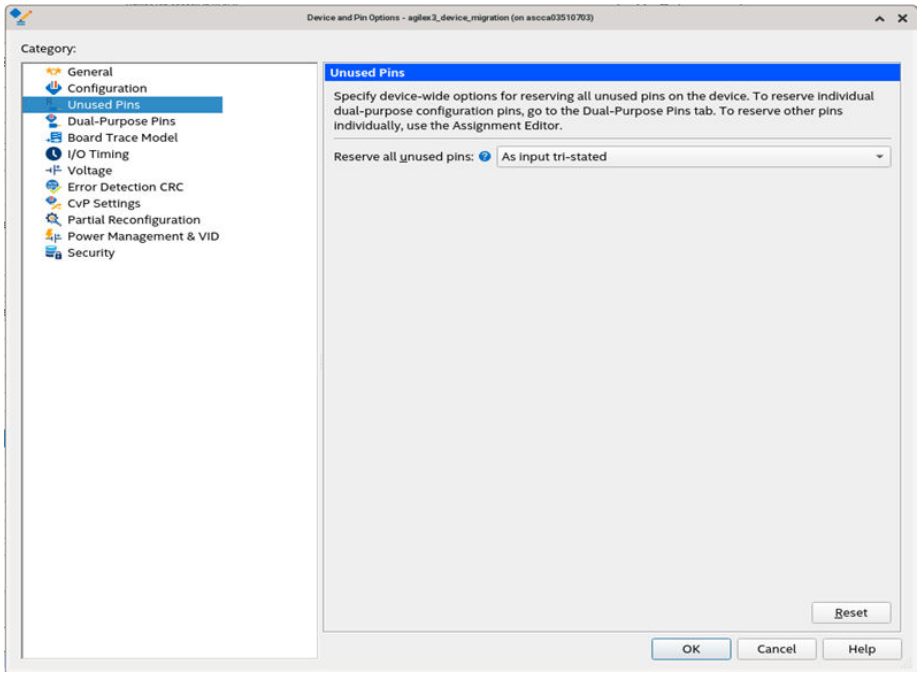


Figure 14. Devices and Pin Options

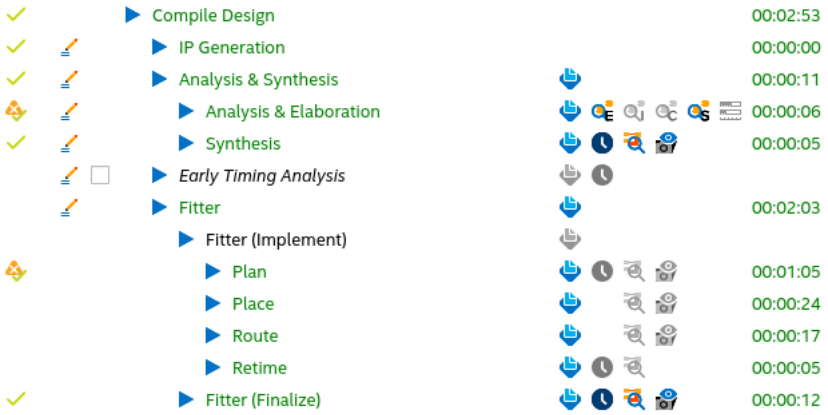


7. Remove the location assignment of the non-migratable pins as shown in the following figure and compile the design.

Figure 15. Location Assignment

Node Name	Direction	Location	I/O Bank	Fitter Location	I/O Standard
pin_name6	Output	PIN_H27	6D	PIN_H27	1.8-V LVCMOS
pin_name5	Output	PIN_F27	6D	PIN_F27	1.8-V LVCMOS
pin_name3	Input	PIN_F26	6D	PIN_F26	1.8-V LVCMOS
pin_name2	Input	PIN_D26	6D	PIN_D26	1.8-V LVCMOS
pin_name4	Output			PIN_B14	2.5-V LVCMOS
pin_name1	Input			PIN_A14	2.5-V LVCMOS

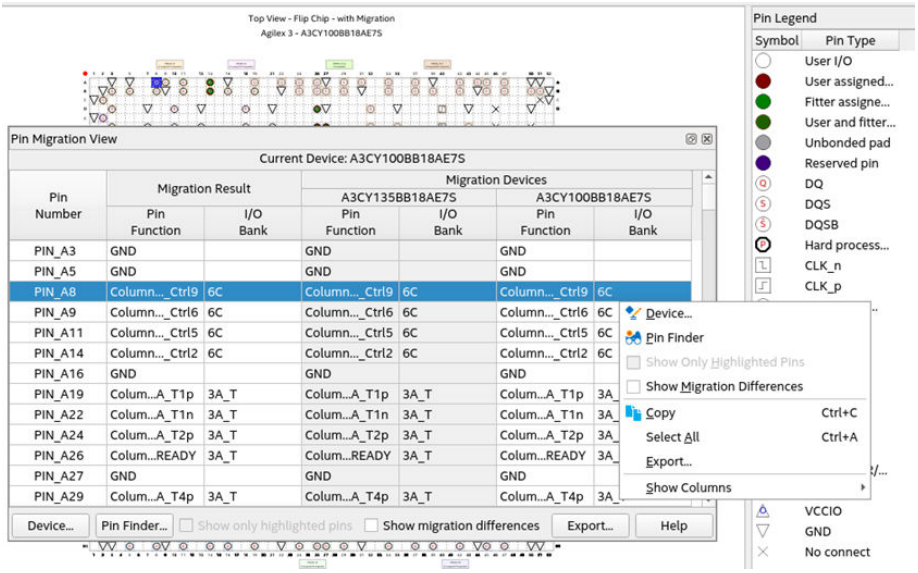
Figure 16. Design Compilation



8. If you have the flexibility of changing the non-migratable pins and their I/O standards, you can go the **Pin Migration View** window and check the pins compatibility and assign the pins accordingly.
9. The **Pin Migration View** window provides information about the suitability of the pins for device migration, as shown in the following figure. You can open this window in the **Pin Planner** by clicking **View ➤ Pin Migration View**. Select a pin in this view to display the following pin migration information:
   - Pin number
   - Migration result
   - Migration devices

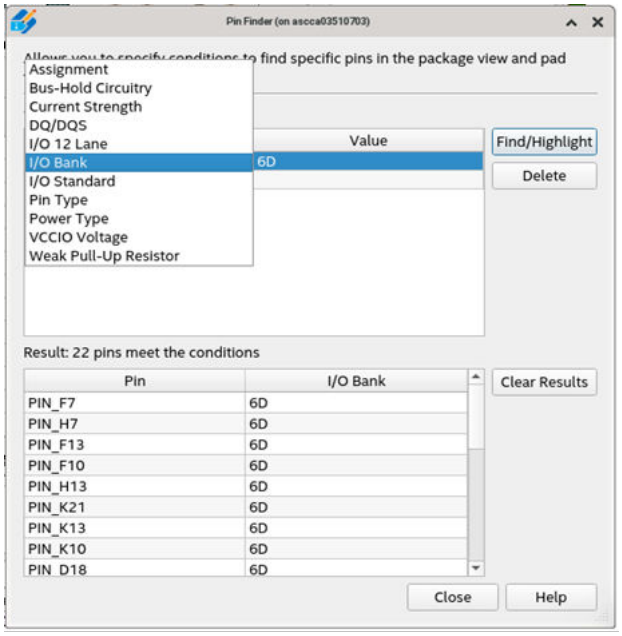
   You can access the following commands by right-clicking on the **Pin Migration View** window in the **Pin Planner**:
   - Device
   - Pin Finder
   - Show Only Highlighted Pins
   - Show Migration Differences
   - Export
   - Show Columns

Figure 17. Pin Migration View



You can look in the **Pin Finder** to find the pins according to the requirement as shown in the following figure.

Figure 18. Pin Finder



10. Change the pin assignment in the **Pin Planner** as shown in the following figure and compile the design to achieve a successful compilation.

Figure 19. Pin Assignments

Node Name	Direction	Location	I/O Bank	Fitter Location	I/O Standard
out pin_name5	Output	PIN_F27	6D	PIN_F27	1.8-V LVCMOS
in pin_name2	Input	PIN_D26	6D	PIN_D26	1.8-V LVCMOS
out pin_name4	Output	PIN_H21	6D	PIN_H21	1.8-V LVCMOS
out pin_name6	Output	PIN_H27	6D	PIN_H27	1.8-V LVCMOS
in pin_name1	Input	PIN_F21	6D	PIN_F21	1.8-V LVCMOS
in pin_name3	Input	PIN_F26	6D	PIN_F26	1.8-V LVCMOS

5. Document Revision History for Device Migration Guidelines: Agilex 3 FPGAs and SoCs C-Series

Document Version	Changes
2025.08.07	• Updated sections to remove outdated note: — *LPDDR4 Interfaces* — *MIPI D-PHY*
2025.06.06	Initial release.