PXI

NI PXI-6683 Series User Manual

NI PXI-6683 and NI PXI-6683H Timing and Synchronization Modules for PXI

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About This Manual

This manual describes the electrical and mechanical aspects of the NI PXI-6683 and NI PXI-6683H, and contains information concerning its operation and programming.

National Instruments Documentation

The *NI PXI-6683 Series User Manual* is one piece of the documentation set for your measurement system. You could have any of several other documents describing your hardware and software. Use the documentation you have as follows:

- Measurement hardware documentation—This documentation contains detailed information about the measurement hardware that plugs into or is connected to the computer. Use this documentation for hardware installation and configuration instructions, specifications about the measurement hardware, and application hints.
- Software documentation—Refer to the *NI-Sync User Manual*, available at `ni.com/manuals`.

You can download NI documentation from `ni.com/manuals`.

Related Documentation

The following documents contain information that you might find helpful as you read this manual:

- *PICMG 2.0 R3.0*, *CompactPCI Core Specification*, available from PICMG at `www.picmg.org`
- *PXI Specification*, Revision 2.1, available from `www.pxisa.org`
- *NI-Sync User Manual*, available from `ni.com/manuals`
- *NI PXI-6683(H) Calibration Procedure*, available from `ni.com/manuals`

1 Introduction

The NI PXI-6683 and NI PXI-6683H timing and synchronization modules synchronize PXI and PXI Express systems using GPS, IEEE 1588, IRIG-B, or PPS. The NI PXI-6683 Series boards also support synchronizing the system time of an RT system. The NI PXI-6683 Series boards can generate triggers and clock signals at programmable future times and timestamp input events with the synchronized system time. The NI PXI-6683 Series boards feature an on-board TCXO that can be disciplined to GPS, IEEE 1588, IRIG-B, or PPS for long term stability. The NI PXI-6683 Series boards also support routing of clock signals and triggers with low skew within a PXI chassis or between multiple chassis, providing you a method for synchronizing multiple devices in a PXI system.

The NI PXI-6683 has a full PXI connector, giving full PXI timing slot functionality. The NI PXI-6683H is designed to allow installation in a hybrid slot in a PXI Express system; this means some of the PXI Timing slot features are not available in the NI PXI-6683H. If synchronized low-skew triggers (Star triggers) or a disciplined 10 MHz clock are required in a PXI Express system, the NI PXI-6683H can be combined with an NI PXIe-667x timing module to provide this functionality.

What You Need to Get Started

To set up and use a NI PXI-6683 Series Timing and Synchronization Module, you need the following items:

- ☐ NI PXI-6683 Series Timing and Synchronization Module
- ☐ *NI PXI-6683 Series User Manual*
- ☐ *NI-Sync* CD
- ☐ One of the following software packages and documentation:
  - LabVIEW
  - LabWindows™/CVI™
  - Microsoft Visual C++ (MSVC)
- ☐ PXI or PXI Express chassis with an appropriate slot (full PXI slot for NI PXI-6683 and NI PXI-6683H, or PXIe hybrid slot for NI PXI-6683H)
- ☐ PXI or PXI Express embedded controller or a desktop computer connected to the PXI or PXI Express chassis using MXI hardware

Unpacking

The NI PXI-6683 Series is shipped in an antistatic package to prevent electrostatic damage to the module. Electrostatic discharge (ESD) can damage several components on the module.

Caution *Never* touch the exposed pins of connectors.

To avoid such damage in handling the module, take the following precautions:

- Ground yourself using a grounding strap or by touching a grounded object.
- Touch the antistatic package to a metal part of the computer chassis before removing the module from the package.

Remove the module from the package and inspect the module for loose components or any sign of damage. Notify NI if the module appears damaged in any way. Do *not* install a damaged module into the computer.

Store the NI PXI-6683 Series in the antistatic envelope when not in use.

Software Programming Choices

The NI PXI-6683 Series uses NI Sync software as its driver.

When programming the NI PXI-6683 Series, you can use NI application development environment (ADE) software such as LabVIEW or LabWindows/CVI, or you can use other ADEs such as Visual C/C++ to interface with the NI Sync software.

LabVIEW features interactive graphics, a state-of-the-art interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of virtual instruments for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

LabWindows/CVI is a complete ANSI C ADE that features an interactive user interface, code generation tools, and the LabWindows/CVI Data Acquisition and Easy I/O libraries.

Safety Information

The following section contains important safety information that you *must* follow when installing and using the product.

Do *not* operate the product in a manner not specified in this document. Misuse of the product can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to National Instruments for repair.

Do *not* substitute parts or modify the product except as described in this document. Use the product only with the chassis, modules, accessories, and cables specified in the installation instructions. You *must* have all covers and filler panels installed during operation of the product.

Do *not* operate the product in an explosive atmosphere or where there may be flammable gases or fumes. If you must operate the product in such an environment, it must be in a suitably rated enclosure.

If you need to clean the product, use a soft, nonmetallic brush. The product *must* be completely dry and free from contaminants before you return it to service.

Operate the product only at or below Pollution Degree 2. Pollution is foreign matter in a solid, liquid, or gaseous state that can reduce dielectric strength or surface resistivity. The following is a description of pollution degrees:

- Pollution Degree 1 means no pollution or only dry, nonconductive pollution occurs. The pollution has no influence.
- Pollution Degree 2 means that only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected.
- Pollution Degree 3 means that conductive pollution occurs, or dry, nonconductive pollution occurs that becomes conductive due to condensation.

You *must* insulate signal connections for the maximum voltage for which the product is rated. Do *not* exceed the maximum ratings for the product. Do not install wiring while the product is live with electrical signals. Do not remove or add connector blocks when power is connected to the system. Avoid contact between your body and the connector block signal when hot swapping modules. Remove power from signal lines before connecting them to or disconnecting them from the product.

Operate the product at or below the *installation category*[1] marked on the hardware label. Measurement circuits are subjected to *working voltages*[2] and transient stresses (overvoltage) from the circuit to which they are connected during measurement or test. Installation categories establish standard impulse withstand voltage levels that commonly occur in electrical distribution systems. The following is a description of installation categories:

- Installation Category I is for measurements performed on circuits not directly connected to the electrical distribution system referred to as MAINS[3] voltage. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special equipment, limited-energy parts of equipment, circuits powered by regulated low-voltage sources, and electronics.
- Installation Category II is for measurements performed on circuits directly connected to the electrical distribution system. This category refers to local-level electrical distribution, such as that provided by a standard wall outlet (for example, 115 V for U.S. or 230 V for Europe). Examples of Installation Category II are measurements performed on household appliances, portable tools, and similar products.
- Installation Category III is for measurements performed in the building installation at the distribution level. This category refers to measurements on hard-wired equipment such as equipment in fixed installations, distribution boards, and circuit breakers. Other examples are wiring, including cables, bus-bars, junction boxes, switches, socket-outlets in the fixed installation, and stationary motors with permanent connections to fixed installations.
- Installation Category IV is for measurements performed at the primary electrical supply installation (<1,000 V). Examples include electricity meters and measurements on primary overcurrent protection devices and on ripple control units.

[1] Installation categories, also referred to as *measurement categories*, are defined in electrical safety standard IEC 61010-1.

[2] Working voltage is the highest rms value of an AC or DC voltage that can occur across any particular insulation.

[3] MAINS is defined as a hazardous live electrical supply system that powers equipment. Suitably rated measuring circuits may be connected to the MAINS for measuring purposes.

2

Installing and Configuring

This chapter describes how to install the NI PXI-6683 Series hardware and software and how to configure the device.

Installing the Software

Refer to the `readme.htm` file that accompanies the *NI-Sync* CD for software installation directions.

Note Be sure to install the driver software *before* installing the NI PXI-6683 Series module.

Installing the Hardware

The following are general installation instructions. Consult the chassis user manual or technical reference manual for specific instructions and warnings about installing new modules.

1. Power off and unplug the chassis.

Caution Do not install the NI PXI-6683 Series module in the system controller slot (slot 1) of a chassis.

2. Choose an available slot in the chassis. Refer to Table 2-1 for more information about functionality.

   NI PXI-6683: Install the NI PXI-6683 in an available PXI slot.

   The NI PXI-6683 is a star trigger controller for PXI. It can replace PXI_CLK10 and control the PXI_STAR triggers. This functionality is only available when the NI PXI-6683 is installed in the system timing slot of a PXI chassis. The PXI triggers are accessible from any PXI slot.

   NI PXI-6683H: Install the NI PXI-6683H in an available PXI slot. If you are using a PXI Express (PXIe) system, install the NI PXI-6683H in an available PXI or PXIe/hybrid slot.

   The NI PXI-6683H is a special version of the NI PXI-6683, designed to also fit in hybrid slots on a PXI Express chassis. It does not have the ability to replace PXI_CLK10 or drive the PXI_STAR triggers.

Table 2-1. PXI/PXI Express Slot Type Compatibility

NI PXI Board	PXI System Timing Slot ◇	PXI Peripheral Slot ○	PXI Express Hybrid Slot ●H
NI PXI-6683	✓*	✓†	—
NI PXI-6683H	✓†	✓†	✓†

* Compatible; PXI_CLK10, PXI_CLKIN, PXI_STAR, PXI_TRIG functionality available.
† Compatible; PXI_TRIG functionality available.

3. Remove the filler panel for the PXI or PXI Express hybrid slot you chose in step 2.
4. Ground yourself using a grounding strap or by touching a grounded object. Follow the ESD protection precautions described in the *Unpacking* section of Chapter 1, *Introduction*.
5. Remove any packing material from the front panel screws and backplane connectors.
6. Insert the NI PXI-6683 Series module into the PXI or PXI Express hybrid slot. Use the injector/ejector handle to fully insert the module into the chassis.
7. Screw the front panel of the module to the front panel mounting rail of the chassis.
8. Visually verify the installation.
9. Plug in and power on the chassis.

The NI PXI-6683 Series module is now installed.

Verifying the Installation

During the first boot following the software and hardware installation of the NI PXI-6683 Series module, the OS detects the device and associates it with the NI-Sync driver software.

Configuring the Module

The NI PXI-6683 Series is completely software configurable. The system software automatically allocates all module resources.

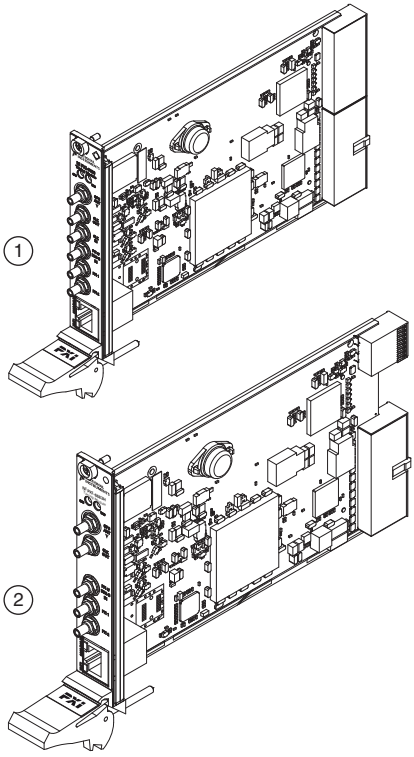
The two LEDs on the front panel provide information about module status. The front panel description sections of Chapter 3, *Hardware Overview*, describe the LEDs in greater detail.

3

Hardware Overview

This chapter presents an overview of the hardware functions of the NI PXI-6683 Series, shown in Figure 3-1.

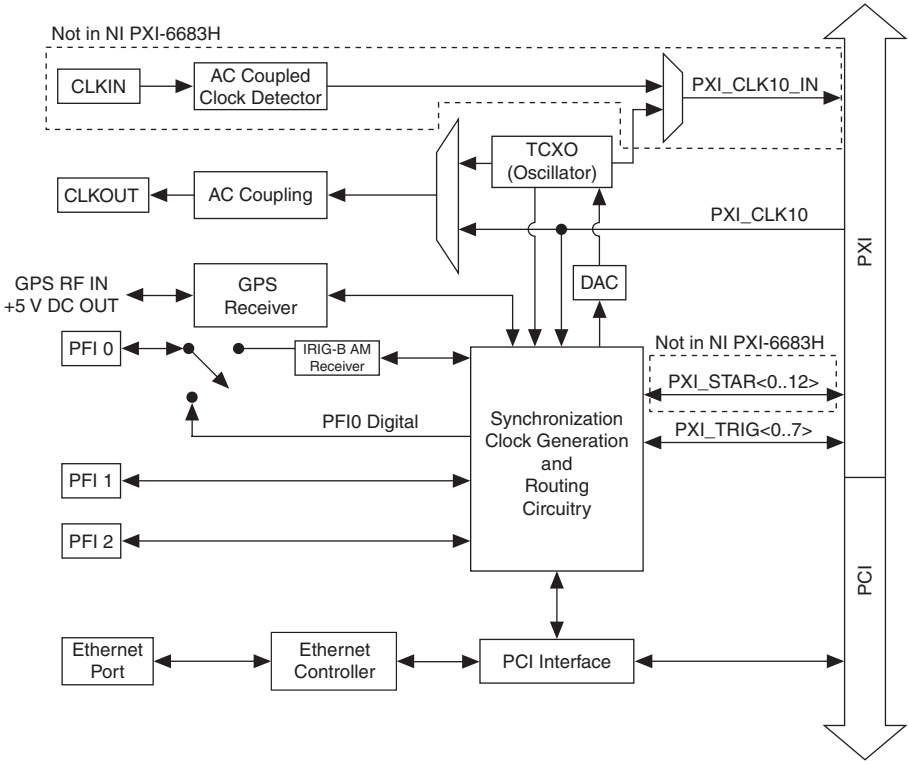
Figure 3-1. Isometric View of the NI PXI-6683 Series



1 NI PXI-6683 2 NI PXI-6683H

Figure 3-2 provides a functional overview of the NI PXI-6683 Series.

Figure 3-2. Functional Overview of the NI PXI-6683

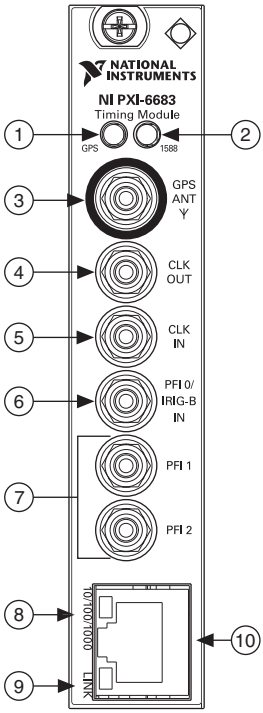


Note The NI PXI-6683H does not have PXI_STAR trigger lines, shown as *PXI_STAR<0..12>* in Figure 3-2. The NI PXI-6683H does not have the CLKIN circuitry, or the ability to drive PXI_CLK10_IN.

NI PXI-6683 Series Front Panel

Figure 3-3 shows the connectors and LEDs on the front panel of the NI PXI-6683 Series.

Figure 3-3. NI PXI-6683 Front Panel



1	GPS LED	6	PFI0/IRIG-B Input Connector
2	1588 LED	7	PFI<1..2> Connectors
3	GPS Antenna Connector	8	Ethernet Speed LED
4	CLKOUT Connector	9	Ethernet ACT/LINK LED
5	CLKIN Connector	10	RJ-45 Ethernet Connector

Note The NI PXI-6683H does not have the CLKIN connector, shown as item 5 in Figure 3-3.

GPS LED

The GPS LED indicates the status of the GPS hardware. Refer to Figure 3-3 for the GPS LED location.

Table 3-1 summarizes what the GPS LED indicates.

Table 3-1. GPS LED Color Description

Color	Status
Off	Not using GPS*
Amber	Attempting to start self survey
Blinking Amber	Self survey in progress
Blinking Green	Self survey complete (normal operation)
Red	Error†

* The GPS LED is turned off if GPS is not set as the time reference.
† An error is generated when the antenna is disconnected, when there is an antenna malfunction, or when there is a hardware malfunction.

1588 LED

The 1588 LED indicates the status of the IEEE 1588 synchronization protocol. Refer to Figure 3-3 for the 1588 LED location.

Table 3-2 summarizes what the 1588 LED indicates.

Table 3-2. 1588 LED Color Description

Color	Status
Off	Not using 1588*
Amber	Initializing
Blinking Amber (2 seconds)	Listening or Passive
Green	Uncalibrated or Slave
Blinking Green (2 seconds)	Master or Premaster
Red	Faulty

* 1588 has been disabled or stopped.

Ethernet Speed LED

The Ethernet Speed LED indicates the NI PXI-6683 Series Ethernet link speed. Refer to Figure 3-3 for the Ethernet Speed LED location.

Table 3-3 summarizes what the Ethernet Speed LED indicates.

Table 3-3. Ethernet Speed LED Description

Color	Status
Off	10 Mbps
Green	100 Mbps
Amber	1000 Mbps

Note When there is no Ethernet link the Ethernet Speed LED is off.

Ethernet ACT/LINK LED

The Ethernet ACT/LINK LED indicates the NI PXI-6683 Series Ethernet link condition. Refer to Figure 3-3 for the Ethernet ACT/LINK LED location.

Table 3-4 summarizes what the Ethernet ACT/LINK LED indicates.

Table 3-4. Ethernet ACT/LINK LED Color Description

Color	Status
Off	No Ethernet link
Green	Ethernet link established
Blink	Ethernet activity occurring

Connectors

This section describes the connectors on the front panel of the NI PXI-6683 Series. Refer to Figure 3-3 for the location of the connectors.

- **GPS ANT**—GPS antenna RF input and DC power output for active GPS antenna. This connector provides 5 VDC for an active antenna. This connector also serves as the input for the RF signal coming in from the GPS antenna.
- **CLKOUT**—Clock Output. This connector is used to source a 10 MHz clock that can be routed programmatically from the temperature-compensated crystal oscillator (TCXO) or backplane clock (PXI_CLK10).

- **CLKIN**—Clock Input. This connector supplies the module with a clock that can be programmatically routed to the PXI backplane (PXI_CLK10_IN) for distribution to the other modules in the chassis when the NI PXI-6683 is installed in the system timing slot.

Note The NI PXI-6683H does not have the CLKIN connector.

- **PFI<0..2>**—Programmable Function Interface <0..2>. These connectors can be used for either input or output. You can program the behavior of these PFI connections individually. Additionally, PFI0 can function as an input for IRIG-B DC or AM.

Caution Do not connect an AM signal to PFI0 when the PFI line is configured for digital operations. This could cause damage to the digital circuitry, the device driving the AM signal, or both. Always ensure the line is configured for IRIG-B AM operation before connecting an IRIG-B AM signal.

- **RJ-45 Ethernet**—10/100/1000 Mbit Ethernet connection. This connector allows the module to communicate via standard Ethernet cabling.

Caution Connections that exceed any of the maximum ratings of input or output signals on the NI PXI-6683 Series can damage the module, the computer, or other devices connected to the NI PXI-6683 Series. NI is *not* liable for any damage resulting from such signal connections.

Hardware Features

The NI PXI-6683 Series performs the following functions:

- Synchronization using GPS, IRIG-B, PPS, or IEEE 1588.
- Generation of future time events and clock signals, based on the synchronized time.
- Timestamping incoming signals with the synchronized time.
- Routing internally or externally generated signals from one location to another.
- Single-board clock disciplining capability.

Table 3-5 outlines the function and direction of the signals discussed in detail in the remainder of this chapter. These signals are also identified in Figure 3-2.

Table 3-5. NI PXI-6683 Series I/O Terminals

Signal Name	Direction	Description
PXI_CLK10_IN (System Timing Slot Only) (Not in NI PXI-6683H)	Out	This is a signal that can replace the native 10 MHz oscillator on the PXI backplane. PXI_CLK10_IN may originate from the onboard TCXO or from an external source connected to CLKIN.
PXI_CLK10	In	This signal is the PXI 10 MHz backplane clock. By default, this signal is the output of the native 10 MHz oscillator in the chassis. An NI PXI-6683 Series in the system timing slot can replace this signal with PXI_CLK10_IN.
Oscillator	N/A	This is the output of the 10 MHz TCXO. It is used by the FPGA for synchronization. An NI PXI-6683 in the system timing slot can be routed to CLKOUT or PXI_CLK10_IN. The TCXO is a very stable and accurate frequency source.
CLKIN (Not in NI PXI-6683H)	In	CLKIN is a signal connected to the SMB input pin of the same name. An NI PXI-6683 in the system timing slot can route CLKIN to PXI_CLK10_IN.
CLKOUT	Out	CLKOUT is the signal on the SMB output pin of the same name. Either the oscillator (TCXO) or PXI_CLK10 may be routed to this output.
PXI_STAR<0..12> (Not in NI PXI-6683H)	In/Out	The PXI star trigger bus connects the system timing slot to Slot <3..15> in a star configuration. The electrical paths of each star line are closely matched to minimize intermodule skew. An NI PXI-6683 in the system timing slot can route signals to Slots <3..15> using the star trigger bus.

Table 3-5. NI PXI-6683 Series I/O Terminals (Continued)

Signal Name	Direction	Description
PFI<0..2>	In/Out	The Programmable Function Interface pins on the NI PXI-6683 Series route timing and triggering signals between multiple PXI chassis. A wide variety of input and output signals can be routed to or from the PFI lines. PFI<0> also can function as an input for IRIG-B DC or AM.
PXI_TRIG<0..7>	In/Out	The PXI trigger bus consists of eight digital lines shared among all slots in the PXI chassis. The NI PXI-6683 Series can route a wide variety of signals to and from these lines.

The remainder of this chapter describes how these signals are used, acquired, and generated by the NI PXI-6683 Series hardware, and explains how you can use the signals between various locations to synchronize events in your system.

Clock and Event Generation

The NI PXI-6683 Series can generate two types of clock signals. The first type is generated with a precise 10 MHz oscillator, and the second is generated with the synchronized timebase. The following sections describe the two types of clock generation and explain the considerations for choosing either type. In addition to time-synchronized clock signals, the NI PXI-6683 Series is also capable of generating arbitrary digital events, to be used as triggers.

TCXO, PXI_CLK10, and Clock Disciplining

The NI PXI-6683 Series features a precision 10 MHz TCXO. The frequency accuracy and stability of this clock is greater than the frequency accuracy and stability of the native 10 MHz PXI backplane clock (PXI_CLK10).

The main source of error in most frequency reference oscillators is temperature variation. The TCXO contains circuitry to measure the temperature of the oscillator and adjust the oscillator's control voltage to compensate for temperature variations according to the crystal's known frequency variation across its operating temperature range.

An NI PXI-6683 module in the system timing slot of a PXI chassis can replace the native PXI 10 MHz backplane frequency reference clock (PXI_CLK10) with the more stable and accurate output of the TCXO. All other PXI modules in the chassis that reference the 10 MHz backplane clock benefit from this improved reference. The TCXO does not automatically replace the native 10 MHz clock; this feature must be explicitly enabled in software. The TCXO output also can be routed out to the CLKOUT connector.

The NI PXI-6683 has the capability to discipline its 10 MHz TCXO to an external time reference (such as GPS, IEEE 1588, or IRIG-B) by monitoring and adjusting the clock relative to the external time reference. The driver software automatically disciplines the TCXO to the selected time reference. TCXO disciplining can be disabled by setting the time reference to **Free Running**.

Note Some chassis (including the NI PXI-103*x* series) require toggling a hardware switch to enable the system timing module to override PXI_CLK10. Refer to your chassis user manual for more information.

Time-Synchronized Clock and Event Generation

The NI PXI-6683 Series is capable of generating clock signals and triggers based on the synchronized time base. The NI PXI-6683 Series keeps an internal time base with 10 ns resolution that can be free running or synchronized to GPS, IEEE 1588, IRIG-B, or PPS. The NI Sync API allows you to schedule triggers to occur at an arbitrary future time (future time events), or clocks with high and low times that are multiples of 10 ns (refer to Appendix A, *Specifications* for information about limitations). It is also possible to program the start and end time of a clock generated in this way.

Refer to Table 3-6 for a list of destinations for synchronized time clocks and future-time events.

PXI_CLK10 Synchronization Design Recommendations

- **Minimize Starting/Stopping of PXI_CLK10 Disciplining**—From startup, the PXI_CLK10 synchronization can take on the order of minutes to stabilize to the time reference. You should design your application such that PXI_CLK10 disciplining runs asynchronous to other programs that might start and stop more frequently. This minimizes the time spent letting the synchronization stabilize and lock.
- **Avoid Disrupting PXI_CLK10 Disciplining**—While you can use the devices used for PXI_CLK10 disciplining within other applications, you should avoid resetting them or changing the configured time reference. Doing so disrupts the PXI_CLK10 disciplining process.

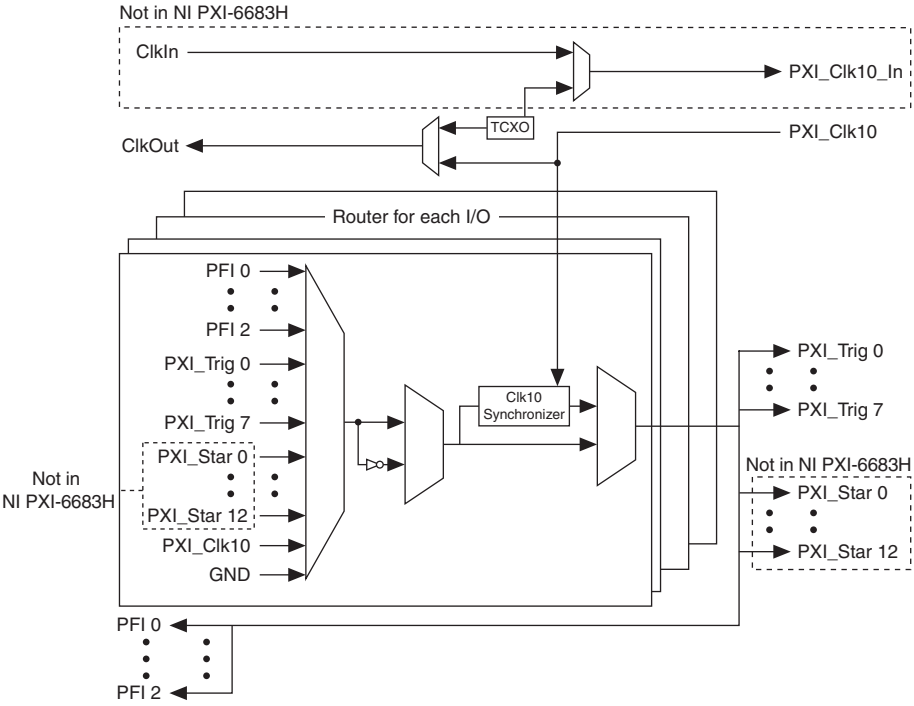
Routing Signals

The NI PXI-6683 Series has versatile trigger routing capabilities. It can route signals to and from the front panel, the PXI star triggers, and the PXI triggers. In addition, the polarity of the destination signal can be inverted, which is useful when handling active-low digital signals.

The NI PXI-6683 can replace the PXI backplane's native 10 MHz clock (PXI_CLK10) with its high-stability TCXO, or with a 10 MHz clock signal from the CLKIN connector (replacing PXI_CLK10 is not supported by the NI PXI-6683H). The NI PXI-6683 Series can route the TCXO, or PXI 10 MHz reference clock to CLKOUT.

Figure 3-4 summarizes the routing features of the NI PXI-6683 Series. The remainder of this chapter details the capabilities and constraints of the routing architecture.

Figure 3-4. High-Level Schematic of NI PXI-6683 Signal Routing Architecture



Note The NI PXI-6683H architecture is identical to the architecture described in Figure 3-4, except that it doesn't have the PXI_STAR trigger lines, CLKIN, or PXI_CLK10_IN.

Determining Sources and Destinations

All signal routing operations can be characterized by a *source* (input) and a *destination*. In addition, synchronous routing operations must also define a third signal known as the *synchronization clock*. Refer to the *Choosing the Type of Routing* section for more information on synchronous versus asynchronous routing.

Table 3-6 summarizes the sources and destinations of the NI PXI-6683 Series. The destinations are listed in the horizontal heading row, and the sources are listed in the column at the far left. A ✓ in a cell indicates that the source and destination combination defined by that cell is a valid routing combination.

Table 3-6. Sources and Destinations for NI PXI-6683 Series Signal Routing Operations

			Destinations				
			Front Panel		Backplane		
			CLKOUT	PFI<0..2>	PXI_ CLK10_IN*	PXI_Star Trigger <0..12>*	PXI TRIG <0..7>
Sources	Front Panel	CLKIN*	✓†	✓†	✓	✓†	✓†
		PFI<0..2>		✓		✓‡	✓
	Backplane	PXI_ CLK10	✓	✓		✓	✓
		PXI_STAR <0..12>*		✓‡		✓	✓
		PXI TRIG<0..7>		✓		✓	✓
	Onboard	TCXO	✓	✓†	✓	✓†	✓†
		Time-synchronized events and clocks		✓		✓	✓

* The NI PXI-6683H does not have a CLKIN connector, PXI_CLK10_IN, or PXI-STAR trigger lines.
† Can be accomplished in two stages by routing source to PXI_CLK10_IN, replacing PXI_CLK10 with PXI_CLK10_IN (occurs automatically in most chassis), and then routing PXI_CLK10 to the destination. The source must be 10 MHz.
‡ Asynchronous routes between a single source and multiple destinations are very low skew. See Appendix A, *Specifications*, for details.

I/O Considerations

Using the Ethernet Port

The NI PXI-6683 Series provides one standard RJ-45 connection for Ethernet communication. This port auto negotiates to the best possible speed—10 Mbps, 100 Mbps, or 1000 Mbps (auto-negotiation can be disabled by software). The Ethernet port is auto-MDI capable, which means crossover cabling is not necessary when connecting the NI PXI-6683 Series to another network card. The NI PXI-6683 Series senses whether a crossed connection is needed and performs the action internally. The Ethernet port also allows for full duplex operation, so traffic can be sent and received at the same time.

Using Front Panel PFI Terminals as Outputs

The front panel PFI output signals use +3.3 V signaling for high-impedance loads. You can use the PFI terminals to generate future time events and clock signals up to 1.5 MHz. PFI output

signals are suitable for driving most LEDs. To ensure proper signal integrity, use cables with 50 Ω impedance. PFI outputs can also drive 50 Ω loads, although logic-high voltage will be lower than 3.3 V. Refer to Appendix A, *Specifications*, for more information. Refer to the *NI-Sync User Manual* for information on how to set up the PFI lines for output.

Caution Do not attempt to drive signals into PFI terminals set up as outputs. Doing so can damage the NI PXI-6683 Series or the device driving the PFI terminal.

The signal source for each PFI trigger line configured as an output can be independently selected from one of the following options:

- Another PFI<0..2>
- PXI_TRIG<0..7>
- PXI_STAR<0..12> (NI PXI-6683 only)
- Future time events
- PXI_CLK10
- Ground

Tip Invert Ground to get a logic high.

The PFI trigger outputs may be synchronized to CLK10 except when routing future time events. Refer to the *Choosing the Type of Routing* section for more information about the synchronization clock.

Using Front Panel PFI Terminals as Inputs

The front panel PFI terminals can be configured by software to accept input signals. Refer to the *NI-Sync User Manual* for information on how to set up the PFI terminals to accept input signals. You can use these terminals to timestamp triggers with the synchronized system time or to route signals to other destinations (refer to Table 3-6). The input terminals accept native +3.3 V signaling, but are +5 V tolerant. Use 50 Ω source termination when driving signals into PFI terminals.

The voltage thresholds for the front-panel PFI input signals are fixed. Refer to Appendix A, *Specifications*, for the voltage thresholds. The front-panel PFI input signals can be timestamped on rising, falling, or both edges of an input signal.

Note Regarding PFI0

Since PFI0 is a dual-purpose terminal capable of performing digital I/O like the other PFI lines while also being capable of receiving IRIG-B AM and DC inputs, care is taken to protect the digital circuitry when PFI0 is being used as an IRIG-B AM input. This is achieved with a normally-open solid-state relay (SSR), which is closed only when digital operations for the line are enabled through the API. Digital operations include setting up routes in which PFI0 is the source or the destination, enabling timestamping for PFI0, scheduling future time events or clocks for PFI0, and setting IRIG-B DC as the time reference.

The SSR has a 5 ms open and close time. Therefore, care must be taken when using PFI0 to ensure correct operation when the SSR is switching.

To avoid issues due to the SSR switching, follow these guidelines:

- Whenever timestamping begins on PFI0, either ensure the input will remain at a logic low state for at least 5 ms or disregard timestamps for at least 5 ms.
- When setting up PFI0 as an output (future time events or clocks), ensure that PFI0 is driven low for at least 5 ms after the line is set up. Alternately, ensure that the external receiver can tolerate a slow rising edge.
- Before disabling PFI0 set up as an output, drive the output low to avoid a very slow ramp down.
- Any time a route is set up or changed where PFI0 is the source or the destination, allow for a 5 ms settling time.

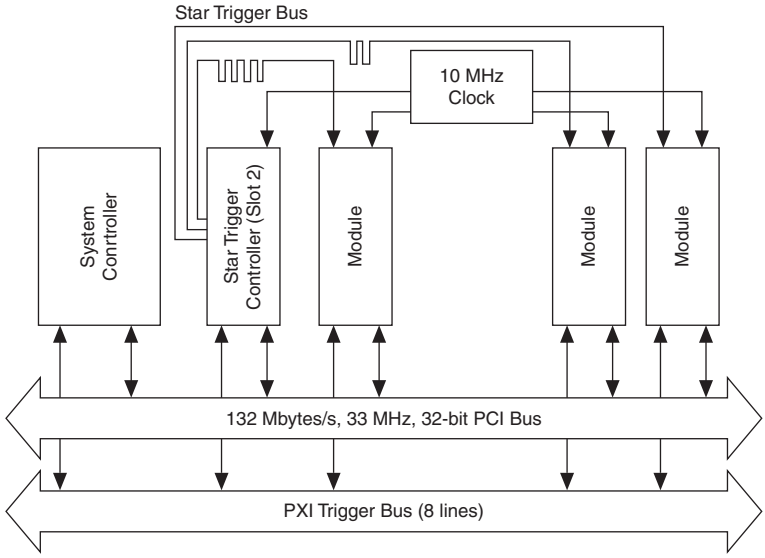
For more information, refer to KnowledgeBase **4E9BT88P** at `ni.com/support`.

Brief Overview of PXI Synchronization Features

PCI eXtensions for Instrumentation (PXI) is a rugged PC-based platform that offers a high-performance, low-cost deployment solution for measurement and automation systems. PXI combines the Peripheral Component Interconnect (PCI) electrical bus with the rugged, modular Eurocard mechanical packaging of CompactPCI and adds specialized synchronization buses and key software features.

Figure 3-5 provides an overview of the PXI synchronization architecture.

Figure 3-5. PXI Synchronization Architecture



The PXI trigger Bus, PXI star triggers, and PXI_CLK10 are PXI features that enhance synchronization. The PXI trigger bus is a multi-drop 8-line bus that goes to every slot. The PXI star trigger bus is a set of up to 13 point-to-point matched-length connections between the system timing slot and every slot starting with slot 3 and up to slot 15. The propagation delay between the system timing slot and each destination slot is matched to within 1ns to achieve low-skew triggering. PXI_CLK10 is a high quality 10 MHz clock that is distributed with low skew to each PXI slot. This 10 MHz signal can be sourced from the native PXI backplane oscillator or from the system timing slot Controller Module installed in the system timing slot (such as the NI PXI-6683).

The following sections describe in more detail the use of PXI triggers and PXI star triggers with the NI PXI-6683 series.

Using the PXI Triggers

The PXI trigger bus is a set of 8 electrical lines that go to every slot in a segment of a PXI chassis (multi-drop up to 8 slots). Only one PXI module should drive a particular PXI_Trigger line at a given time. The signal is then received by modules in all other PXI slots. This feature makes the PXI triggers convenient in situations where you want, for instance, to trigger several devices, because all modules will receive the same trigger.

Given the architecture of the PXI trigger bus, triggering signals do not reach each slot at precisely the same time. A difference of several nanoseconds can occur between slots, especially in larger PXI chassis (which can have buffers between segments). This delay is not a problem for many applications. However, if your application requires tighter synchronization, use the PXI_STAR triggers (see next section), or use the PXI trigger bus synchronous to PXI_CLK10.

The multi-drop nature of the PXI trigger bus can introduce signal integrity issues. Therefore, National Instruments does not recommend the use of PXI_Trigger lines for clock distribution. The preferred method for clock distribution is the use of the PXI_STAR triggers. However, the NI PXI-6683 Series does support routing of clocks to the PXI_Trigger lines, in case you must use them.

For each PXI_Trigger line configured as an output in the NI PXI-6683 Series, the signal source can be independently selected from the following options:

- PFI<0..2>
- Another PXI trigger line (PXI_TRIG<0..7>)
- PXI_STAR<0..12>
- Future time events
- PXI_CLK10
- Ground

Tip Invert Ground to get a logic high.

The PXI trigger outputs may be synchronized to CLK10 except when routing future time events. Refer to the *Choosing the Type of Routing* section for more information about the synchronization clock.

Using the PXI Star Triggers (NI PXI-6683 only)

There are up to 13 PXI star triggers per chassis. Each trigger line is a dedicated connection between the system timing slot and one other slot. The *PXI Specification*, Revision 2.1, requires that the propagation delay along each star trigger line be matched to within 1 ns. A typical upper limit for the skew in most NI PXI chassis is 500 ps. The low skew of the PXI star trigger bus is useful for applications that require triggers to arrive at several modules nearly simultaneously. The NI PXI-6683 is able to route low skew triggers to the PXI_Star lines from any PFI line.

The star trigger lines are bidirectional, so signals can be sent to the system timing slot from a module in another slot or from the system timing slot to the other module.

The signal source for each PXI star trigger line configured as an output can be independently selected from one of the following options:

- PFI<0..2> (low skew)
- PXI_TRIG<0..7>
- Another PXI star trigger line (PXI_STAR<0..12>)
- Synchronized time event
- PXI_CLK10
- Ground

Tip Invert Ground to get a logic high.

The PXI star trigger outputs may be synchronized to CLK10 except when routing future time events. Refer to the *Choosing the Type of Routing* section for more information about the synchronization clock.

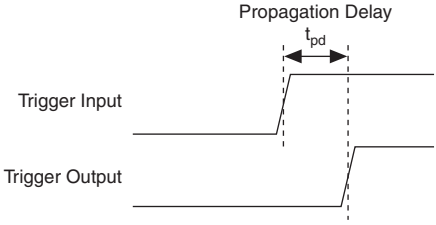
Choosing the Type of Routing

The NI PXI-6683 Series routes signals in one of two ways: asynchronously or synchronously. The following sections describe the two routing types and the considerations for choosing each type.

Asynchronous Routing

Asynchronous routing is the most straightforward method of routing signals. Any asynchronous route can be defined in terms of two signal locations: a source and a destination. A digital pulse or train comes in on the source and is propagated to the destination. When the source signal goes from low to high, this rising edge is transferred to the destination after a propagation delay through the module. Figure 3-6 illustrates an asynchronous routing operation.

Figure 3-6. Asynchronous Routing Operation



Some delay is always associated with an asynchronous route, and this delay varies among NI PXI-6683 Series modules, depending on variations in temperature and chassis voltage. Typical delay times in the NI PXI-6683 Series for asynchronous routes between various sources and destinations are given in Appendix A, *Specifications*.

Asynchronous routing works well if the total system delays are not too long for the application. Propagation delay could be caused by the following reasons:

- Output delay on the source
- Propagation delay of the signal across the backplane(s) and cable(s)
- Propagation delay of the signal through the NI PXI-6683 Series
- Time for the receiver to recognize the signal

The source of an asynchronous routing operation on the NI PXI-6683 Series can be any of the following lines:

- Any front panel PFI pin (PFI<0..2>)
- Any PXI Star trigger line (PXI_STAR<0..12>) (NI PXI-6683 only)
- Any PXI Trigger line (PXI_TRIG<0..7>)
- Synchronized time events
- PXI_CLK10
- Ground

Tip Invert Ground to get a logic high.

The destination of an asynchronous routing operation on the NI PXI-6683 Series can be any of the following lines:

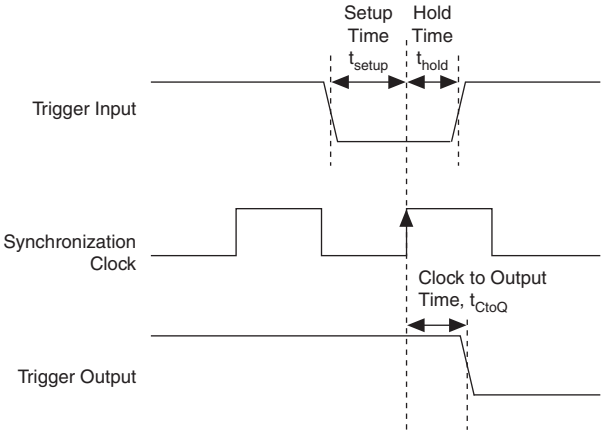
- Any front panel PFI pin (PFI<0..2>)
- Any PXI star trigger line (PXI_STAR<0..12>) (NI PXI-6683 only)
- Any PXI Trigger line (PXI_TRIG<0..7>)

Synchronous Routing

A synchronous routing operation is defined in terms of three signals: a source, destination, and a synchronization clock. Unlike asynchronous routing, the output of a synchronous routing operation does not directly follow the input after a propagation delay. Instead, the logic state of the input is sampled on each rising edge of the synchronization clock and the output is set to the logic state after a small delay, as shown in figure 3-7. Thus, the output is said to be *synchronous* with this clock.

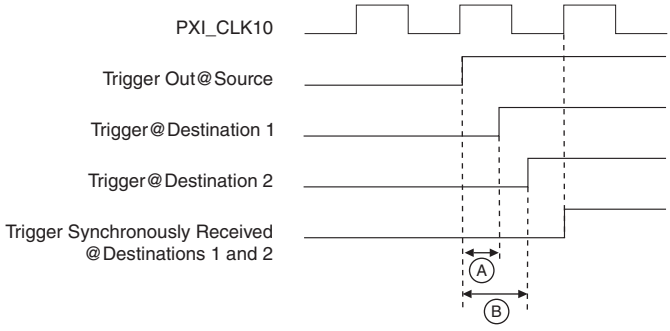
The PXI-6683 Series supports inverting the polarity of the routed signals; this can be useful when handling active-low digital signals.

Figure 3-7. Synchronous Routing Operation



Synchronous routing can be useful for eliminating skew when sending triggers to several destinations. For example, when sending triggers using the PXI Trigger lines, the trigger arrives at each slot at a slightly different time. However, if the trigger is sent and received synchronously using a low-skew synchronization clock, such as PXI_CLK10, all receiving devices can act on the trigger at the same time, as shown in Figure 3-8.

Figure 3-8. Synchronous Routing to Multiple Destinations



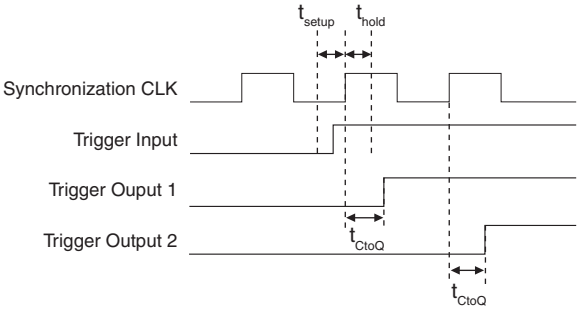
A: Propagation delay from source to destination 1.

B: Propagation delay from source to destination 2.

Synchronous routing requires the input to be stable at a logic low or logic high state within a window of time around the clock edge. This window of time around the clock edge is defined by the setup time (tsetup) and hold time (thold). If the input signal changes within this window of time, it is undetermined whether the output of the synchronous route will go to the old or new logic state. This is important, for example, if a source is being routed synchronously to several destinations. As shown in Figure 3-9, if the source signal changes within the setup-and-hold

window around the synchronization clock edge, one of the destinations might go to the new logic level while the other destination might remain at the old logic level and change when the next synchronization clock edge occurs.

Figure 3-9. Synchronous Routing Uncertainty with Setup-and-Hold Violation



Therefore, if your application requires that the trigger arrive at the multiple destinations simultaneously, you must ensure that the input is stable within the setup and hold window around the synchronization clock edge. For more information and possible methods to ensure this requirement is met, go to `ni.com/info` and enter Info Code `SyncTriggerRouting`.

Possible sources and destinations for synchronous routing include the following:

- Any front panel PFI pin (PFI<0..2>)
- Any PXI star trigger line (PXI_STAR<0..12>) (NI PXI-6683 only)
- Any PXI Trigger line (PXI_TRIG<0..7>)

In the NI PXI-6683 Series, the synchronization clock for synchronous routes is always PXI_CLK10.

The destination of a synchronous routing operation on the NI PXI-6683 Series can be any of the following lines:

- Any front panel PFI pin (PFI<0..2>)
- Any PXI star trigger line (PXI_STAR<0..12>) (NI PXI-6683 only)
- Any PXI Trigger line (PXI_TRIG<0..7>)

Note The possible destinations for a synchronous route are identical to those for an asynchronous route.

4

Synchronization

The NI PXI-6683 Series is capable of achieving tight synchronization with various other devices using GPS, IRIG-B, PPS, or IEEE 1588. When GPS or IRIG-B are selected as the synchronization source, the NI PXI-6683 Series module can also serve as an IEEE 1588 grandmaster. The following sections describe the synchronization capabilities of the NI PXI-6683 Series.

GPS

GPS stands for Global Positioning System, and it is a system of over 2 dozen satellites in medium Earth orbit that are constantly transmitting signals down to Earth. GPS receivers are able to detect these signals and determine location, speed, direction and time very precisely. GPS satellites are fitted with atomic clocks, and the signals they transmit to Earth contain timing information. This makes the GPS system a precise timing and synchronization source.

The NI PXI-6683 Series has a GPS receiver which powers an active GPS antenna and receives and processes the RF signals (1.575 GHz) from the satellites. The GPS receiver then generates a very precise pulse-per-second (PPS) that the NI PXI-6683 Series uses to achieve sub-microsecond synchronization.

GPS enables the NI PXI-6683 Series to synchronize PXI systems located far away from each other, as long as GPS satellites are visible to the antenna from each location. Furthermore, once the NI PXI-6683 Series is synchronized to GPS, it can function as an IEEE 1588 grandmaster to enable synchronization of external 1588 devices.

IRIG-B

IRIG is a standard used to transmit precise timing information between instruments to achieve synchronization. IRIG-B is a particular application of the IRIG standard, in which 100 bits of data are sent every second. Embedded in the data is a seconds' boundary marker that the receiving instrument uses to synchronize its timebase to the IRIG source. The rest of the data contains information such as the time of day, days since the beginning of the year, and optionally, control functions and the number of seconds since the start of the day, encoded as a straight binary number.

Refer to Appendix B, *IRIG Protocol Overview*, for more information about the IRIG standard.

The NI PXI-6683 Series can function as an IRIG-B receiver, supporting synchronization to sources outputting IRIG-B 12X (AM) and IRIG-B 00X (DC), compliant with IRIG 200-04 standard.

When configured to synchronize to an IRIG-B AM source, the NI PXI-6683 Series will be able to accept a 1 kHz AM modulated IRIG-B 12X signal on its PFI0 input. When configured to synchronize to an IRIG-B DC source, the NI PXI-6683 Series will be able to accept an IRIG-B 00X DC encoded signal on its PFI0 input.

Caution Do not connect an AM signal to PFI0 when the PFI line is configured for digital operations. This could cause damage to the digital circuitry, the device driving the AM signal, or both. Always ensure the line is configured for IRIG-B AM operation before connecting an IRIG-B AM signal.

Furthermore, once the NI PXI-6683 Series is synchronized to IRIG-B, it can function as an IEEE 1588 grandmaster to synchronize of external 1588 devices.

The following assumptions are made regarding the received IRIG-B signal. All conditions must be met for the NI PXI-6683 Series to be able to synchronize accurately:

- Seconds begin every minute at 0, increment to 59, and then roll over to 0.
- Minutes begin every hour at 0, increment to 59, and then roll over to 0.
- Hours begin every day at 0, increment to 23, and then roll over to 0.
- Days begin every year at 1. Days increment to 365 in non-leap years, or to 366 in leap years, and then roll-over to 1. Leap years must be supported. Valid values for year are 01 to 99, inclusive. Years are assumed to be in the XXI Century. For instance, year *09* represents 2009. If the year is not supplied (sent as *00*), the OS system time is read and the year is derived from it.

To achieve proper synchronization of the NI PXI-6683 Series, ensure that the IRIG-B source used conforms to the requirements listed above. Note that most IRIG-B sources conform to these requirements.

IEEE 1588

The NI PXI-6683 Series is capable of performing synchronization over Ethernet using IEEE 1588. It is possible to configure the NI PXI-6683 Series to synchronize to GPS or IRIG-B and then function as an IEEE 1588 grandmaster. It is also possible to configure the NI PXI-6683 Series to synchronize to IEEE 1588, in which case, the standard defines how the master will be selected. If the NI PXI-6683 Series is selected as IEEE 1588 master, and it is not configured to synchronize to GPS or IRIG-B, it will use its internal free-running timebase, which will be updated to the host computer’s system time during power up.

PPS

The NI PXI-6683 Series is capable of using a PPS (pulse per second) signal for synchronization. Any PFI, PXI_Trigger or PXI_Star line can be configured as the PPS input terminal. When synchronizing based on a PPS, the first pulse received will set the NI PXI-6683 Series internal timebase to either an arbitrary time supplied by the user, or the host computer's system time. Each subsequent pulse received will be interpreted as a second's boundary (the pulse occurring exactly 1 second after the previous pulse). As each pulse is received, the NI PXI-6683 Series will adjust its internal timebase to match the frequency of the PPS source.

For best results when using PPS Time Reference, ensure that the device supplying the PPS signal is capable of providing a stable, consistent 1Hz signal. Error can be induced into the system if the reference signal contains significant jitter, or if the reference frequency strays from 1 Hz.

Synchronization Best Practices

The NI PXI-6683 Series can achieve sub-microsecond synchronization. The following section describes some guidelines for achieving the best possible performance from your NI PXI-6683 Series module. While the NI PXI-6683 Series will function properly if you follow the specifications, the following guidelines may increase the synchronization performance.

Operating Environment

In order to achieve the best synchronization performance, refer to the following guidelines to provide a thermally stable environment. Also, ensure you remain within the specified operating temperature limits:

- Place the PXI or PXI Express chassis containing the NI PXI-6683 Series module in an environment free of rapid temperature transitions.
- Ensure that PXI filler panels are properly installed for unused PXI or PXI Express slots since inconsistent airflow and temperature transitions across thermally sensitive components can degrade the NI PXI-6683 Series module performance.
- Perform the same steps listed above for any other synchronization partners/systems.

Timing System Performance

The NI PXI-6683 Series can generate or receive a 1 Hz pulse per second signal on any PFI or PXI Trigger terminal. You can set up this signal to transition on the seconds boundary of the synchronized system time. You can then use this signal to analyze system performance by connecting two or more pulse per second signals to an oscilloscope and measuring the latency between them. Adjustments can be made to account for deterministic latency. Refer to the *NI-Sync API Reference Help* for more information. The NI PXI-6683 Series can also timestamp an incoming pulse per second signal. The NI PXI-6683 Series will timestamp the externally generated pulse per second with its internal timebase. By comparing this timestamp with the nearest seconds boundary, you can quickly determine the synchronization performance.

IEEE 1588 Synchronization Best Practices

Network Topology

To obtain the best NI PXI-6683 Series performance, follow these guidelines to set up the Ethernet network topology:

- Use short cabling when possible. Ethernet cabling is inherently asymmetric; the longer the cabling, the higher the asymmetry. This impacts synchronization performance, because the IEEE 1588 protocol assumes a symmetric network path.
- If several 1588 devices need to be synchronized on the same network, use a 1588-enabled switch. 1588-enabled switches are specifically designed to compensate for the varying latency of packets passing through them; thus enhancing synchronization performance.
- If a 1588-enabled switch is not available, use hubs when connecting to multiple IEEE 1588 devices. Unlike standard switches, hubs offer low latency and close to deterministic performance for Ethernet traffic. Standard Ethernet switches can have Ethernet packet latencies vary by hundreds of nanoseconds. This latency uncertainty degrades synchronization performance significantly.
- Ensure that the network is running at 1 Gbps by noting the Ethernet Speed LED status. Synchronization performance is degraded when running at 10 or 100 Mbps.

Note If it is impossible to use a 1000 or 100 Mbps network and you must run IEEE 1588 synchronization using a 10 Mbps network, ensure the network interface of the NI PXI-6683 Series is explicitly configured for 10 Mbps Full Duplex operation using the Windows configuration panels.

GPS Synchronization Best Practices

The NI PXI-6683 Series device has one SMB female connector on its front panel for a GPS active antenna. The connector provides a DC voltage to power the antenna and also serves as input for the GPS RF signal.

Antenna Installation

Caution National Instruments recommends using a lightning arrester in line with the GPS antenna installation to protect the NI PXI-6683 Series device and the PXI system from possible damage and operators from injury in the event of lightning.

The embedded GPS receiver in the NI PXI-6683 Series device requires signals from several satellites to compute accurate timing and location. The more satellites available to the receiver, the more accurately it can determine time and location. Therefore, the antenna location should be such that it receives signals from the greatest number of satellites possible. As the number of satellites visible to the antenna decreases, the synchronization performance may also decrease. Choose the antenna location so that the antenna has a clear view of the sky. There is no strict definition for a clear view of the sky, but a suitable guideline is that the GPS antenna should have a straight line of sight to the sky in all directions (360°) down to an imaginary line making a 30° angle with the ground. Locations far from trees and tall buildings that could block or reflect GPS satellite signals are best.

Maximum Cable Length

Maximum cable length depends on the GPS antenna gain and the cable's loss per unit of distance. National Instruments recommends a GPS signal strength of between -135 dBm and -120 dBm at the NI PXI-6683 Series device SMB input. GPS signal strength on the Earth's surface is typically -130 dBm. Targeting a signal strength of -125 dBm at the SMB input, you can compute the maximum cable length as:

Max_cable_loss = -130 dBm + antenna_gain - (-125 dBm)

Max_cable_length = Max_cable_loss / (loss_per_unit_of_distance)

For example, if you use an active antenna with gain of 28 dB and RG-58 cable, which has a rated loss at 1.5 GHz of about 0.8 dB/m (24.5 dB/100 ft), the maximum cable length you could use is:

Max_cable_loss = -130 dBm + 28 dB - (-125 dBm) = 23 dB

Max_cable_length = 23 dB / (0.8 dB/m) ≈ 29 m

Note The GPS antenna kit offered by National Instruments comes with a 30 m cable which has a loss of 15 dB/100 ft, making the total loss in the cable approximately 14.8 dB.

5

Calibration

This chapter discusses the calibration of the NI PXI-6683 and NI PXI-6683H.

Calibration consists of verifying the measurement accuracy of a device and correcting for any measurement error. The NI PXI-6683 and NI PXI-6683H are factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants—the corrections that were needed to meet specifications—are stored in the onboard nonvolatile memory (EEPROM). The driver software uses these stored values.

Factory Calibration

All NI PXI-6683 Series boards go through factory calibration. During that process the TCXO frequency is adjusted so that it matches a reference 10 MHz atomic clock. A calibration constant is then stored in on-board, non-volatile memory, along with other calibration metadata, such as calibration date and temperature.

The calibration constant is used at start-up when the board is configured for free running mode. When the NI PXI-6683 Series board is configured to use GPS, IEEE 1588, IRIG-B, or PPS as its time reference, the TCXO frequency is adjusted according to the time reference and the calibration constant is no longer used. If the board returns to free running mode, because it was so configured or the time reference is no longer present, then the last applied TCXO voltage is retained (it does not revert to the calibration constant).

Note If the board is configured to use IEEE 1588 as time reference, and selected as 1588 Master through 1588's Best Master Clock algorithm, the board will be free running and use its calibration constant.

Additional Information

Refer to `ni.com/calibration` for additional information on NI calibration services.

A

Specifications

CLKOUT Characteristics

Output frequency[1] ..... 10 MHz

Duty cycle distortion[1] ..... <1%, typical

Output impedance ..... 50 Ω, nominal

Output coupling ..... AC

PXI_CLK10 to CLKOUT delay ..... 8 ns, typical

Load	Square Wave
Open Load	5 V_{p-p}, typical
50 Ω Load	2.5 V_{p-p}, typical

Square wave rise/fall time
(10 to 90%) ..... <1 ns, typical

CLKIN Characteristics (NI PXI-6683 only)

CLKIN input frequency[2] ..... 10 MHz ±100 ppm, sine or square wave

Input impedance ..... 50 Ω, nominal

Input coupling ..... AC

Voltage range ..... 400 mV_{p-p} to 5 V_{p-p}

Absolute maximum input voltage[3] ..... 6 V_{p-p}

CLKIN to PXI_CLK10_IN delay ..... 11 ns, typical

Jitter added to CLKIN ..... 1.3 ps_{rms}, 10 Hz to 100 kHz, typical

Duty cycle distortion of CLKIN
to PXI_CLK10_IN ..... <1%, typical

Required input duty cycle[2] ..... 45 to 55%

---

[1] When configured to route the on-board oscillator (TCXO) or PXI_CLK10, otherwise CLKOUT will be disabled (default).

[2] This is a requirement of the PXI specification.

[3] Stresses beyond those listed can cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods of time can affect device reliability. Functional operation of the device outside the conditions indicated in the operational parts of the specification is not implied.

PFI<0..2>

Output Characteristics

Frequency range ..... DC to 50 MHz

Output impedance ..... 50 Ω, nominal

Output coupling ..... DC

Output voltage levels

- Output high ..... 1.2 V min, 1.6 V typical for 50 Ω load to ground
  2.6 V min, 3.3 V typical for 1 MΩ load
- Output low ..... 0.1 V max, 0 V typical for 50 Ω load to ground
  0.1 V max, 0 V typical for 1 MΩ load

Absolute maximum applied voltage[1] ..... 0 to 4.4 V

Output-to-output skew, asynchronous
PXI_STAR to PFI routes[2] ..... <400 ps, typical

Output-to-output skew,
other asynchronous routes ..... <1.5 ns, typical

Output-to-output skew, synchronous routes ..... <2 ns, typical

Synchronized trigger clock
to out time, t_{co} ..... 10 ns, max (relative to CLKOUT when configured to route PXI_CLK10)

Output current ..... ±48 mA, max

Square wave rise/fall time
(10 to 90%) for 50 Ω load ..... <1 ns, typical

Input Characteristics[3]

Frequency range ..... DC to 50 MHz

Input impedance ..... 1 kΩ, nominal

Input coupling ..... DC

Nominal voltage level ..... 0 to +3.3 V, +5 V tolerant

Absolute maximum input voltage [1] ..... -0.5 V to +6.0 V

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[1] Stresses beyond those listed can cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods of time can affect device reliability. Functional operation of the device outside the conditions indicated in the operational parts of the specifications is not implied.

[2] Applies to asynchronous routes from a single PXI_STAR input to multiple PFI outputs.

[3] For PFI 0 these characteristics apply when the line is configured as a digital input. They do not apply when configured as an IRIG-B AM input.

Input thresholds

Voltage threshold high ..... +2.3 V max

Voltage threshold low ..... +0.8 V min

Asynchronous delay, t_{pd}

PFI<0..2> to
PXI_TRIG<0..7> output..... 17 to 20 ns, typical

PFI<0..2> to
PXI_STAR<0..12> output[1]..... 12 ns, typical

Synchronized trigger
input setup time, t_{setup} ..... 25 ns, max (relative to CLKOUT when configured to route PXI_CLK10)

Synchronized trigger
input hold time, t_{hold}..... 0 ns (relative to CLKOUT when configured to route PXI_CLK10)

IRIG-B Input Characteristics (PFI0)

IRIG-B AM compatibility ..... IRIG-B 12X (200-04 standard)

Maximum Input voltage range ..... -5 V to +5 V

Input impedance ..... > 5 kΩ

Decode Input voltage range ..... 1.5 V to 10 V peak-peak mark (3:1 ratio mark:space)

Input carrier frequency ..... 1 kHz

Caution Do not connect an IRIG-B AM signal to PFI 0 when the input is configured for digital operation, as this can result in damage of the digital input circuitry.

IRIG-B DC compatibility ..... IRIG-B 00X (200-04 standard)

Input characteristics for IRIG-B DC ..... same as PFI digital input characteristics listed above

[1] The NI PXI-6683H does not have star trigger lines.

The following assumptions are made regarding the received IRIG-B signal. All conditions must be met for the NI PXI-6683 Series to be able to synchronize accurately:

- Seconds begin every minute at 0, increment to 59, and then roll over to 0.
- Minutes begin every hour at 0, increment to 59, and then roll over to 0.
- Hours begin every day at 0, increment to 23, and then roll over to 0.
- Days begin every year at 1. Days increment to 365 in non-leap years, or to 366 in leap years, and then roll-over to 1. Leap years must be supported. Valid values for year are 01 to 99, inclusive. Years are assumed to be in the XXI Century. For instance, year *09* represents 2009. If the year is not supplied (sent as *00*), the OS system time is read and the year is derived from it.

To achieve proper synchronization of the NI PXI-6683 Series ensure that the IRIG-B source used conforms to the requirements listed above. Note that most IRIG-B sources conform to these requirements.

PXI_STAR Trigger Characteristics (NI PXI-6683 only)

Output-to-output skew,
PFI to PXI_STAR routes[1,2] ..... <400 ps

Output-to-output skew, synchronous triggers ... <2 ns, typical

Asynchronous delays, t_{pd}

PXI_STAR<0..12> to
PFI<0..2> output ..... 8.5 ns, typical

PXI_STAR<0..12> to
PXI_TRIG<0..7> output ..... 10 to 18 ns, typical

PXI Trigger Characteristics

Output-to-output skew[1] ..... <5 ns, typical

Asynchronous delay, t_{pd}

PXI_TRIG<0..7> to
PFI<0..2> output ..... 13 to 23 ns, typical

[1] Measured at the NI PXI-6683 Series backplane connector.

[2] Applies to asynchronous routes from a single PFI input to multiple PXI_STAR outputs.

Timestamping and Time-Synchronized Clock Generation

Time-sychronized
clock period and duty cycle resolution ..... 10 ns

Note Clock signals generated on PFI, PXI_STAR (NI PXI-6683 only), or PXI Trigger lines must have a period and duty cycle that is a multiple of 10 ns.

Minimum pulse width for timestamping ..... 22 ns

TCXO Characteristics

Nominal frequency ..... 10 MHz

Accuracy within 1 year of calibration
adjustment within 0 °C to 55 °C
operating temperature range ..... ±3.5 ppm

Long-term stability ..... ±1 ppm/year

Stability vs temperature ..... <2 ppm peak-to-peak
within 0 °C to 55 °C operating temperature range

Tuning voltage range[1] ..... 0.6 V to 3.0 V

Tuning range ..... ±17.5 ppm minimum

Duty cycle ..... 45 to 55%

Recommended calibration interval ..... 1 year

[1] The TCXO will operate with a tuning voltage between 0 V and 0.6 V, but the frequency curve is flat below 0.6 V.

GPS Characteristics

DC voltage output for antenna ..... +5 V, ±5%
Maximum output current ..... 60 mA
Minimum current for antenna
Presence detection ..... 4.7 mA typical, 7.9 mA max
Input impedance ..... 50 Ω, nominal
GPS receiver type ..... 50 channels, GPS L1 frequency (1575.42 MHz), C/A Code
Recommended signal strength at
SMB connector ..... -130 dBm
Maximum RF power at input ..... +3 dBm
Accuracy
- PPS[1] ..... 15 ns
- Position[2],[3] ..... 2.5 m CEP, 3.5 m SEP
- Velocity[2] ..... 0.1 m/s

Maximum horizontal velocity ..... 310 m/s
Maximum vertical velocity ..... 50 m/s

[1] Compensating for quantization error

[2] All SV at -130 dBm

[3] 24 hours static

Physical

Chassis requirement

- NI PXI-6683 ..... One 3U CompactPCI or PXI slot (PXI system timing slot for full functionality)
- NI PXI-6683H ..... One 3U CompactPCI, PXI, or PXI Express hybrid slot

Weight

- NI PXI-6683 ..... 186 g
- NI PXI-6683H ..... 172 g

Front panel connectors

- NI PXI-6683 ..... Six SMB male, 50 Ω; one standard RJ-45 Ethernet connector
- NI PXI-6683H ..... Five SMB male, 50 Ω; one standard RJ-45 Ethernet connector

Front panel indicators ..... Two tricolor LEDs (green, red, and amber) for GPS and IEEE 1588 status, and two green/amber LEDs for Ethernet link status and speed

Recommended maximum cable lengths

- PFI, DC to 1.5 MHz..... 200 m
- CLKOUT to CLKIN[1] ..... 200 m
- Ethernet CAT5 ..... 100 m

Power Requirements

Voltage (V)	Typical	Maximum
+3.3 V	740 mA	1.86 A
+5 V	335 mA	1.14 A
+12 V	54 mA	175 mA
-12 V	24 mA	35 mA

[1] The NI PXI-6683H does not have a CLKIN connector.

Synchronization Accuracy

Test*	Synchronization Performance
GPS†	±40 ns, <8 ns standard deviation
IEEE 1588 3 m Ethernet direct connection‡	±25 ns, <4 ns standard deviation
IEEE 1588 through a 1588 switch‡,**	±40 ns, <8 ns standard deviation
IEEE 1588 through a hub‡,††	±60 ns, <12 ns standard deviation
IEEE 1588 through a switch‡,‡‡	±25 µs, <150 ns standard deviation
IRIG-B DC	±55 ns, <13 ns standard deviation
IRIG-B AM matching***,†††	±1.15 µs, <260 ns standard deviation
IRIG-B AM to source†††	±5 µs, <500 ns standard deviation
PPS	±40 ns, <8 ns standard deviation

*All synchronization performance figures are based on empirical results and represent typical behavior. All figures are obtained recording the offset between PPS signals generated by two NI PXI-6683 Series boards, inside a closed PXI chassis, configured to synchronize to the particular time reference, at ambient room temperature. Synchronization was performed for 15 minutes before PPS offset recording began. All test durations were at least 12 hours.

† For the GPS test, two NI PXI-6683 Series boards were independently synchronizing to GPS and configured to generate a PPS. The specification above represents typical empirical results. Please note that GPS satellites are only guaranteed to be within 100 ns of UTC. Therefore, the offset between any two devices synchronizing can be as high as 200 ns plus the offset of that device to GPS.

‡ Sync interval of 1 second was used for IEEE 1588 tests, and all Ethernet connections were 1 Gbps unless otherwise specified.

** Hirschmann MAR1040 Gb 1588 switch used.

†† Netgear DS104 Hub used with 100 Mbps links.

‡‡ Airlink 101 Gigabit over copper switch used. For this test, a moderate amount of non-1588 Ethernet traffic was present on the switch.

*** IRIG-B AM matching specification was obtained by setting two NI PXI-6683 Series boards to synchronize independently to the same IRIG-B AM source and generate a PPS. The offset between their PPS signals was then measured over a 12 hour period.

††† IRIG-B performance depends on IRIG-B source stability and quality.

Environmental

Operating Environment

Ambient temperature range ..... 0 to 55 °C
(Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)

Relative humidity range..... 10% to 90%, noncondensing
(Tested in accordance with IEC 60068-2-56.)

Maximum altitude..... 2,000 m (at 25 °C ambient temperature)

Pollution Degree 2

Indoor use only.

Storage Environment

Ambient temperature range ..... -40 to 70 °C
(Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)

Relative humidity range..... 5% to 95% noncondensing
(Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Operational Shock ..... 30 g peak, half-sine, 11 ms pulse
(Tested in accordance with IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)

Random Vibration

Operating ..... 5 to 500 Hz, 0.3 g_{rms}

Nonoperating ..... 5 to 500 Hz, 2.4 g_{rms}
(Tested in accordance with IEC 60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Note Specifications are subject to change without notice.

Safety

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product is designed to meet the requirements of the following standards of EMC for electrical equipment for measurement, control, and laboratory use:

- EN 61326 (IEC 61326): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note For the standards applied to assess the EMC of this product, refer to the *Online Product Certification* section.

Note For EMC compliance, operate this device with shielded cabling.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit `ni.com/environment/weee`.

电子信息产品污染控制管理办法 （中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 `ni.com/environment/rohs_china`。 (For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

B

IRIG Protocol Overview

IRIG (Inter Range Instrumentation Group) is a standard used to transmit precise timing information between instruments to achieve synchronization. There are 6 different IRIG standards defined (A,B,D,E,G and H). The main difference between the standards is the rate with which the synchronization pulses and the information bits are sent. The standards also differ slightly in the content of the information transmitted. Table B-1 summarizes the characteristics of each IRIG standard

Table B-1. IRIG Standard Definitions

IRIG Standard	Bit rate (bit duration)	Frame rate (frame duration)	Information sent
IRIG-A	1 Kbps (1 ms)	10 fps (100 ms)	TOY & Y (BCD) SOD (SBS)
IRIG-B	100 bps (10 ms)	1 fps (1 s)	TOY & Y (BCD) SOD (SBS)
IRIG-D	1 bpm (60 s)	1 fph (1 hour)	TOY (BCD) days and hours only
IRIG-E	10 bps (100 ms)	6 fpm (10s)	TOY & Y (BCD)
IRIG-G	10 kbps (0.1 ms)	100 fps (10 ms)	TOY & Y (BCD) Includes fractions of seconds
IRIG-H	1 bps (1 s)	1 fpm (60 s)	TOY (BCD) Days, hours and minutes only

bpm—bits per minute
bps—bits per second
fph—frames per hour
fpm—frames per minute
fps—frames per second

BCD—binary-coded decimal
SBS—straight binary seconds
SOD—seconds of day
TOY—time of year
Y—year

In addition to the characteristics of each standard described in the table above, each of those is subdivided further depending on the electrical characteristics of the signal used to transmit the data, and the actual data transmitted. This is usually specified by 3 digits that follow the IRIG standard name (for instance, IRIG-B 120). Table B-2 details the different characteristics of each IRIG option.

Table B-2. IRIG Option Characteristics

Modulation type		Carrier Signal Frequency		Information sent	
0	Pulse width modulated	0	DC	0	TOY (BCD), CB, SBS
1	Amplitude modulated (sine wave)	1	100 Hz	1	TOY (BCD), CB
2	Manchester modulated	2	1 kHz	2	TOY (BCD)
		3	10 kHz	3	TOY (BCD), SBS
		4	100 kHz	4	TOY (BCD), Year (BCD), CB, SBS
		5	1 MHz	5	TOY (BCD), Year (BCD), CB
				6	TOY (BCD), Year (BCD)
				7	TOY (BCD), Year (BCD), SBS
CB = control bits					

For example, IRIG-B 120 indicates that the information is sent once per second, 100 bits per second, on a 1kHz amplitude modulated sine wave, and that the information sent is the time of year in BCD, control bits, and the seconds of day in straight binary seconds.

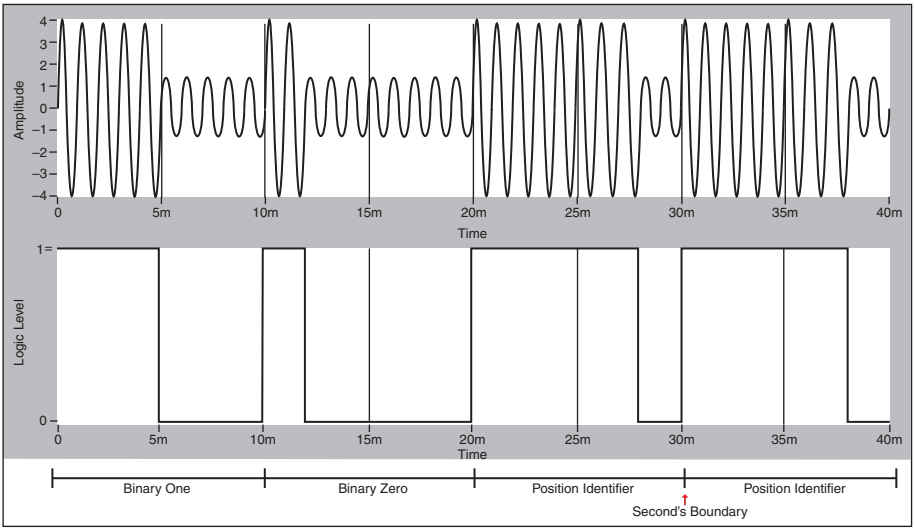
There are 3 types of “bits” sent in the IRIG standard: binary zeroes, binary ones and position identifiers. To transmit a binary zero, the source must keep the signal at mark for 20% of the bit duration and at space for the remaining 80%; to transmit a binary one the source must keep the signal at mark for 50% of the bit duration and at space for the remaining 50%; to transmit a position identifier, the source must keep the signal at mark for 80% of the bit duration, and at space for the remaining 20%. Binary bits are used to transmit information such as time of year, straight binary seconds, and so on, and position identifiers are used to separate the different pieces of data transmitted. The second’s boundary is embedded into the transmission by sending two consecutive position identifiers; the beginning of the second position identifier is the second’s boundary.

For pulse width modulated systems, conventional digital binary signaling is used, and mark is defined as the logic high state, while space is defined as the logic low state.

For amplitude modulated systems, the source must generate sinusoidal signaling modulating the amplitude such that it has a 10:3 mark:space amplitude ratio (the range of allowable mark to space ratios is 3:1 to 6:1). The source must phase align the generated sine wave such that the leading edges of bits are coincident with zero crossings of the sine wave.

Figure B-1 shows an example of transmission of a binary one, a binary zero, and two position identifiers (with the second's boundary at the leading edge of the second position identifier). The figure shows the information transmitted using an amplitude modulated signal, and a pulse width modulated signal.

Figure B-1. IRIG-B AM and DC Transmission Example



IRIG-B is one of the most common IRIG standards used. The following table describes how the information is transmitted when using IRIG-B each second.

Table B-3. IRIG-B Bit Assignments

Bit position	Information transmitted
0	Position identifier P_R (seconds' boundary marker)
1 to 4	Units of seconds
6 to 8	Tens of seconds
9	Position identifier P_I
10 to 13	Units of minutes
15 to 17	Tens of minutes

Table B-3. IRIG-B Bit Assignments (Continued)

Bit position	Information transmitted
19	Position identifier P_2
20 to 23	Units of hours
25 to 26	Tens of hours
29	Position identifier P_3
30 to 33	Units of days
35 to 38	Tens of days
39	Position identifier P_4
40 to 41	Hundreds of days
49	Position identifier P_5
50 to 53	Units of year or control function bits
55 to 58	Tens of year or control function bits
59	Position identifier P_6
60 to 68	Control function bits
69	Position identifier P_7
70 to 78	Control function bits
79	Position identifier P_8
80 to 88	Nine lowest significant bits of time of day in straight binary seconds (bit 80 -> 2^0 … bit 88 -> 2^8)
89	Position Identifier P_9
90 to 97	Eight most significant bits of time of day in straight binary seconds (bit 90 -> 2^9 … bit 97 -> 2^{16})
99	Position identifier P_0
Note: Bits not listed are index markers, and are sent as binary zeroes.	

The NI PXI-6683 Series uses the time of day information transmitted as BCD to synchronize its internal timebase. If the IRIG-B signal includes the year, then it also uses that information to synchronize its clock. Otherwise, it gets the year from the host computer. The NI PXI-6683 Series disregards the rest of the information contained in the IRIG-B signal. Therefore, when configured to synchronize to IRIG-B AM, the NI PXI-6683 Series supports IRIG-B 12X (200-04 standard) , and when configured to synchronize to IRIG-B DC, it supports IRIG-B 00X (200-04 standard).

The following assumptions are made regarding the received IRIG-B signal. All conditions must be met for the NI PXI-6683 Series to be able to synchronize accurately:

- Seconds begin every minute at 0, increment to 59, and then roll over to 0.
- Minutes begin every hour at 0, increment to 59, and then roll over to 0.
- Hours begin every day at 0, increment to 23, and then roll over to 0.
- Days begin every year at 1. Days increment to 365 in non-leap years, or to 366 in leap years, and then roll-over to 1. Leap years must be supported. Valid values for year are 01 to 99, inclusive. Years are assumed to be in the XXI Century. For instance, year *09* represents 2009. If the year is not supplied (sent as *00*), the OS system time is read and the year is derived from it.

To achieve proper synchronization of the NI PXI-6683 Series ensure that the IRIG-B source used conforms to the requirements listed above. Note that most IRIG-B sources conform to these requirements.

C

NI Services

NI provides global services and support as part of our commitment to your success. Take advantage of product services in addition to training and certification programs that meet your needs during each phase of the application life cycle; from planning and development through deployment and ongoing maintenance.

To get started, register your product at ni.com/myproducts.

As a registered NI product user, you are entitled to the following benefits:

- Access to applicable product services.
- Easier product management with an online account.
- Receive critical part notifications, software updates, and service expirations.

Log in to your MyNI user profile to get personalized access to your services.

Services and Resources

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- **Training and Certification**—The NI training and certification program is the most effective way to increase application development proficiency and productivity. Visit ni.com/training for more information.
  - The Skills Guide assists you in identifying the proficiency requirements of your current application and gives you options for obtaining those skills consistent with your time and budget constraints and personal learning preferences. Visit ni.com/skills-guide to see these custom paths.
  - NI offers courses in several languages and formats including instructor-led classes at facilities worldwide, courses on-site at your facility, and online courses to serve your individual needs.
- **Technical Support**—Support at ni.com/support includes the following resources:
  - **Self-Help Technical Resources**—Visit ni.com/support for software drivers and updates, a searchable KnowledgeBase, product manuals, step-by-step troubleshooting wizards, thousands of example programs, tutorials, application notes, instrument drivers, and so on. Registered users also receive access to the NI Discussion Forums at ni.com/forums. NI Applications Engineers make sure every question submitted online receives an answer.
  - **Software Support Service Membership**—The Standard Service Program (SSP) is a renewable one-year subscription included with almost every NI software product, including NI Developer Suite. This program entitles members to direct access to NI Applications Engineers through phone and email for one-to-one technical support, as well as exclusive access to online training modules at ni.com/self-paced-training. NI also offers flexible extended contract options that guarantee your SSP benefits are available without interruption for as long as you need them. Visit ni.com/ssp for more information.
- **Declaration of Conformity (DoC)**—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting ni.com/certification.

For information about other technical support options in your area, visit ni.com/services, or contact your local office at ni.com/contact.

You also can visit the Worldwide Offices section of ni.com/niglobal to access the branch office websites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

Glossary

Symbol	Prefix	Value
p	pico	10^{-12}
n	nano	10^{-9}
μ	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^{3}
M	mega	10^{6}

Symbols

%	percent
±	plus or minus
+	positive of, or plus
-	negative of, or minus
/	per
°	degree
Ω	ohm

A

AC	alternating current
ADE	application development environment
asynchronous	a property of an event that occurs at an arbitrary time, without synchronization to a reference clock

B

backplane	an assembly, typically a printed circuit board (PCB), with 96-pin connectors and signal paths that bus the connector pins. PXI systems have two connectors, called the J1 and J2 connectors.
bus	the group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. An example of a PC bus is the PCI bus.

C

C	Celsius
CLKIN	CLKIN is a signal connected to the SMB input pin of the same name. CLKIN also can serve as PXI_CLK10_IN.
CLKOUT	CLKOUT is the signal on the SMB output pin of the same name. PXI_CLK10 can be routed to CLKOUT.
clock	hardware component that controls timing for reading from or writing to groups
CompactPCI	an adaptation of the Peripheral Component Interconnect (PCI) Specification 2.1 or later for industrial and/or embedded applications requiring a more robust mechanical form factor than desktop PCI. It uses industry standard mechanical components and high-performance connector technologies to provide an optimized system intended for rugged applications. It is electrically compatible with the PCI Specification, which enables low-cost PCI components to be utilized in a mechanical form factor suited for rugged environments.

D

DAQ	data acquisition—(1) collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing; (2) collecting and measuring the same kinds of electrical signals with A/D and/or DIO devices plugged into a computer, and possibly generating control signals with D/A and/or DIO devices in the same computer
DC	direct current

E

ESD	electrostatic discharge

F

frequency	the basic unit of rate, measured in events or oscillations per second using a frequency counter or spectrum analyzer. Frequency is the reciprocal of the period of a signal.
front panel	the physical front panel of an instrument or other hardware

G

GPS	Global Positioning System; worldwide system that allows you to receive precise location and timing information.

H

Hz	hertz—the number of scans read or updates written per second

I

IEEE	Institute of Electrical and Electronics Engineers
IEEE 1588	an IEEE standard used to synchronize separate devices
in.	inch or inches

IRIG	Inter Range Instrumentation Group
IRIG-B	a standard used to transmit precise timing information

J

jitter	the rapid variation of a clock or sampling frequency from an ideal constant frequency

L

LabVIEW	a graphical programming language
LED	light-emitting diode—a semiconductor light source

M

master	the requesting or controlling device in a master/slave configuration
Measurement & Automation Explorer (MAX)	a controlled centralized configuration environment that allows you to configure all of your National Instruments DAQ, GPIB, IMAQ, IVI, Motion, VISA, and VXI devices

O

oscillator	a device that generates a fixed frequency signal. An oscillator most often generates signals by using oscillating crystals, but also may use tuned networks, lasers, or atomic clock sources. The most important specifications on oscillators are frequency accuracy, frequency stability, and phase noise.
output impedance	the measured resistance and capacitance between the output terminals of a circuit

P

PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 Mbytes/s.
PFI	Programmable Function Interface
PPS	Pulse Per Second
precision	the measure of the stability of an instrument and its capability to give the same measurement over and over again for the same input signal
propagation delay	the amount of time required for a signal to pass through a circuit
PXI	a rugged, open system for modular instrumentation based on CompactPCI, with special mechanical, electrical, and software features. The PXIbus standard was originally developed by National Instruments in 1997, and is now managed by the PXIbus Systems Alliance.
PXI star	a special set of trigger lines in the PXI backplane for high-accuracy device synchronization with minimal latencies on each PXI slot
PXI_Trig/PXI_Star synchronization clock	the clock signal that is used to synchronize the PXI Triggers or PXI_STAR triggers on an NI PXI-6683
PXI Trigger	the PXI timing bus that connects PXI devices directly, by means of connectors on top of the devices, for precise synchronization of functions

S

s	seconds
skew	the actual time difference between two events that would ideally occur simultaneously. Inter-channel skew is an example of the time differences introduced by different characteristics of multiple channels. Skew can occur between channels on one module, or between channels on separate modules (intermodule skew).
slave	a computer or peripheral device controlled by another computer
slot	the place in the computer or chassis in which a card or module can be installed
SMB	sub miniature type B—a small coaxial signal connector that features a snap coupling for fast connection
synchronous	a property of an event that is synchronized to a reference clock
system timing slot	the second slot in a PXI system which can house a master timing unit

T

t_{CtoQ}	clock to output time
t_{hold}	hold time
t_{pd}	propagation delay time
TRIG	trigger signal
trigger	a digital signal that starts or times a hardware event (for example, starting a data acquisition operation)
t_{setup}	setup time

V

V	volts
VI	virtual instrument

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