Solving TDC Challenges with Gowin FPGAs: Accurate, Scalable, and Cost-Effective Timing Solutions

White Paper

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1 Abstract

As time-domain applications continue to grow across sectors such as 3D sensing, quantum optics, medical imaging, and LiDAR, the demand for high-resolution, scalable, and reliable Time-to-Digital Converter (TDC) solutions has increased significantly. While FPGAs are a popular platform for TDC implementation, traditional approaches often suffer from inconsistent delay lines, environmental sensitivity, and limited channel scalability.

This white paper introduces GOWIN Semiconductor's innovative TDC architecture that leverages dedicated delay lines embedded in FPGA IO blocks. By circumventing the limitations of general-purpose logic fabric, GOWIN FPGAs offer superior timing precision, enhanced thermal and voltage stability, and support for high-density, multi-channel designs. The paper also explores real-world applications, including 3D Time-of-Flight cameras, digital oscilloscopes, and quantum photon counting systems, and demonstrates how GOWIN's solution reduces cost and power while improving performance.

Additionally, the paper presents a unique case study of a DIY Time-Based ADC, showcasing how GOWIN FPGAs enable creative, low-cost, high-resolution signal digitization. For engineers seeking accurate, efficient, and scalable TDC implementation, GOWIN's FPGA-based solution sets a new standard in time-domain signal processing.

2 Introduction to TOF and TDC technology

Time-of-Flight (ToF)

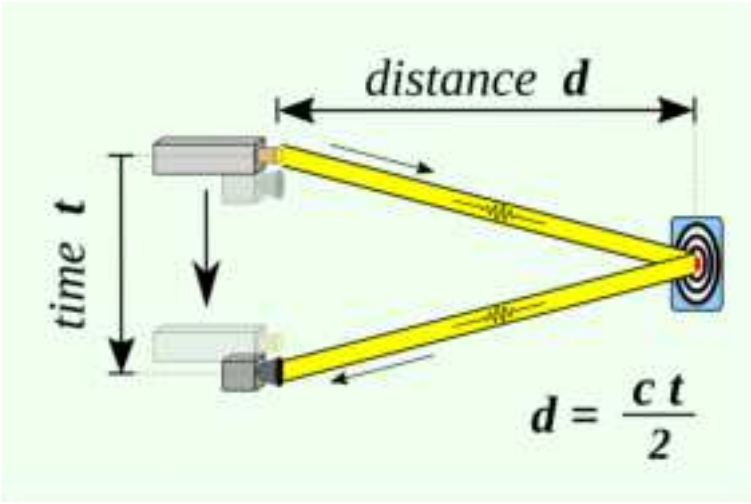
In the age of smart devices, autonomous systems, and immersive reality, the ability to perceive depth with speed and precision has become essential. At the heart of many advanced sensing solutions lies Time-of-Flight (ToF) technology—an optical distance measurement technique that is revolutionizing fields from mobile photography to robotics and industrial automation.

Time-of-Flight is a method for measuring distance by calculating the time it takes for a signal—typically a light pulse or modulated wave—to travel from a source to a target and back. By capturing this "flight time," the system can determine the exact distance to an object. The fundamental principle is simple, but its implementation relies on cutting-edge optoelectronics and timing technologies.

A typical ToF system consists of:

- Light Source: Often a VCSEL (Vertical-Cavity Surface-Emitting Laser) that emits near-infrared light.
- Sensor: Usually a SPAD (Single-Photon Avalanche Diode) or CMOS sensor that detects returning photons.

Timing Circuitry: Includes a Time-to-Digital Converter (TDC) that measures the time delay with extreme precision.



Concept of ToF from Wikipedia

There are two main types of ToF systems. One is Direct ToF (dToF). It measures the actual time delay between the emitted and received pulse. The other one is Indirect ToF (iToF). It measures the phase shift of a modulated light signal to estimate distance.

There are several Key Advantages of ToF.

- Real-time 3D Mapping: Generates depth maps at video frame rates.
- Compact & Low Power: Especially iToF, which is ideal for smartphones and AR glasses.
- High Accuracy & Range: Direct ToF can achieve centimeter to millimeter-level accuracy even over long distances.
- Versatile Integration: Easily embedded in consumer, automotive, and industrial systems.

As technology continues to evolve, ToF sensors are becoming smaller, faster, and more accurate. Future innovations will likely combine ToF with AI, edge computing, and multi-modal sensing (e.g., combining ToF with RGB or thermal imaging) to enable smarter, context-aware devices.

Time-to-Digital Converter (TDC)

A Time-to-Digital Converter (TDC) is an electronic circuit that measures the time interval between two events and converts it into a digital number. Unlike traditional ADCs (Analog-to-Digital Converters) that digitize voltage levels, TDCs focus on timing precision, offering exceptional performance for time-domain applications.

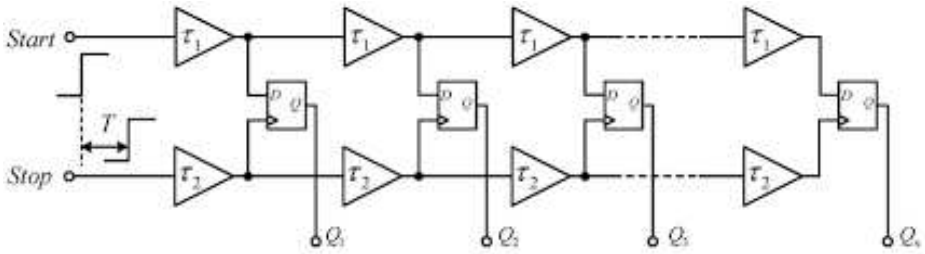
TDCs are essential in:

- Time-of-Flight (ToF) systems
- Particle detectors
- Optical communication
- LiDAR and 3D imaging
- Medical scanners (PET, CT)
- High-resolution oscilloscopes

TDCs measure the time between a start and stop signal. Depending on the architecture, they can achieve resolutions from nanoseconds down to tens of picoseconds or even lower.

Common Architectures:

1. Delay Line TDC:
   - Uses a chain of logic gates or buffers with known delay.
   - Captures which stage the signal reaches when stopped.
   - Simple and fast, but limited in resolution and sensitive to process/temperature.
2. Vernier TDC:
   - Uses two delay lines with slightly different delays.
   - The difference is used to interpolate timing more precisely.
   - Higher resolution but more complex.
3. Ring Oscillator or Counter-based TDC:
   - Measures coarse time with a counter and fine time with a delay chain.
   - Offers a wide dynamic range and scalable performance.
4. Time Interleaving or Multi-phase Clock:
   - Improves throughput by parallelizing the measurement process.
   - Ideal for high-frequency, high-event-rate applications.



Schematic of TDC based on Vernier Deley Line

Many TDCs are implemented on-chip FPGA or ASIC for flexibility and reduced cost.

3 Implementing TDC in FPGA

Why Use FPGAs for TDC?

FPGAs (Field-Programmable Gate Arrays) are ideal for implementing TDCs due to:

- High-speed internal logic and fine-grained delay elements
- Parallelism for multi-channel timing
- Customizability for application-specific requirements
- Lower cost and faster prototyping compared to ASICs

FPGAs enable rapid development of TDCs for applications such as:

- Time-of-Flight sensors (e.g., LiDAR)
- Scientific instrumentation (e.g., photon timing, nuclear detectors)
- Communication systems (e.g., jitter measurement, time synchronization)

Common TDC Implementation Techniques in FPGA

1. Tapped Delay Line (TDL) with LUTs and Carry Chains

- Uses the FPGA's carry-chain logic as a fine-grained delay line.
- A signal propagates through the chain; a fast sampling flip-flop array captures the position of the rising edge.
- The pattern of flip-flop outputs gives a "thermometer code" that's translated to fine time.

Pros: Simple, high resolution (20–50 ps typically)
Cons: Sensitive to temperature, voltage, and placement variability

2. Vernier Delay Line (VDL)

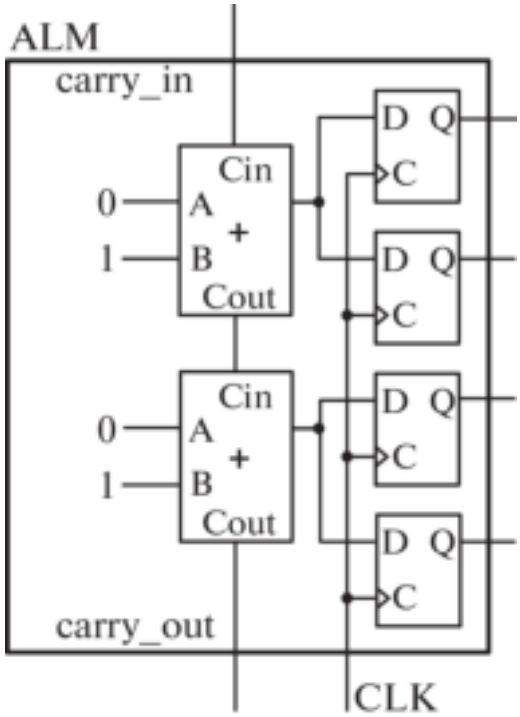
- Uses two delay chains with slightly different delays to create a "beat frequency" and interpolate time.
- Often implemented with carefully tuned LUTs or logic blocks.

Pros: Higher resolution than TDL (sub-10 ps achievable)
Cons: More complex, calibration-intensive

3. Multiphase Clocking

- Leverages a PLL to generate multiple clock phases.
- Uses these clocks to sample the timing signal more finely than the system clock.

Pros: Easy to implement, deterministic
Cons: Limited number of phases, coarse resolution (unless combined with other techniques)



One Example of Carry Chain based TDC

Limitations of FPGA-based TDC

Challenge	Description
Non-uniform delays	Delay lines vary due to routing, logic placement, process variation
Temperature/voltage drift	Delay elements are sensitive to environmental changes
Metastability	Occurs when sampling fast-changing signals asynchronously
Jitter	Internal and external clock noise can limit accuracy

4 GOWIN TDC Solution

While implementing TDCs in FPGAs offers tremendous flexibility and performance, designers often face a set of persistent challenges tied to the nature of traditional FPGA fabric. Gowin Semiconductor addresses these issues with a unique architectural innovation, offering a more robust and scalable TDC solution.

The Challenges of FPGA-Based TDCs

While FPGAs are widely used for implementing TDCs, several technical limitations can impact timing accuracy and reliability:

1. Routing and Placement Variability

Traditional TDC designs in FPGAs rely on a general-purpose logic fabric and internal routing.

As a result:

- Delay lines are non-uniform due to synthesis and routing differences.
- Fine-tuning the layout requires manual floorplanning and careful timing analysis.
- Achieving consistent results across devices and designs can be difficult.

2. Environmental Sensitivity

Standard FPGA delay elements are sensitive to:

- Temperature changes
- Voltage fluctuations
- Process variations

This leads to timing drift and requires active calibration or thermal compensation, increasing complexity and design time.

Gowin's Solution: Dedicated IO-Based Delay Architecture

To overcome these limitations, Gowin FPGAs integrate dedicated delay lines and registers directly into the IO blocks offering a new standard in accuracy and robustness for TDC design.

Key Advantages

1. Stable and Uniform Delay Lines

- Dedicated delay elements in the IOs are physically consistent and isolated from logic fabric.
- No dependency on random logic placement or FPGA routing.
- Ensures high linearity and repeatable measurements across multiple devices and temperature ranges.

2. Reduced Environmental Sensitivity

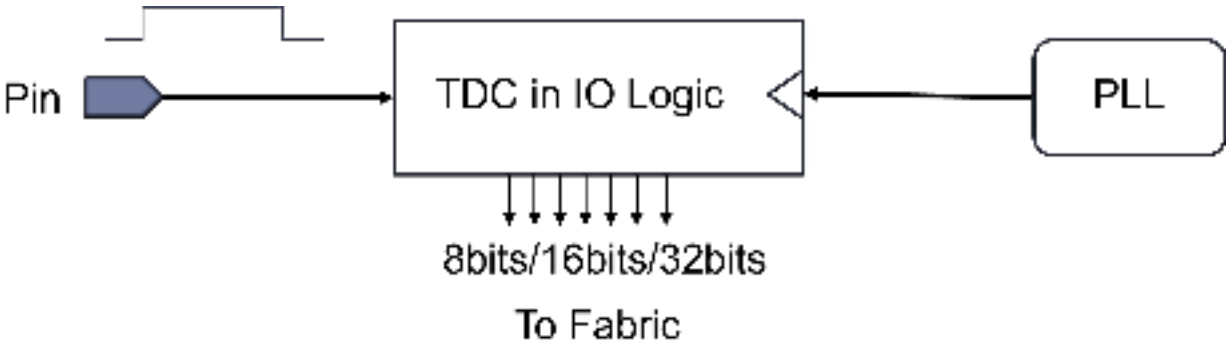
- IO block architecture minimizes the impact of process, voltage, and temperature (PVT) variations.
- Significantly improves timing stability without requiring external calibration or complex compensation logic.

3. High Channel Density

- Gowin FPGAs offer a high number of IOs per device, enabling the implementation of multi-channel TDCs at low cost.
- Ideal for applications such as LiDAR, SPAD arrays, and quantum experiments where many parallel timing channels are required.

4. Low-Cost and Power-Efficient

- By moving the TDC function to dedicated IO resources, Gowin avoids overloading core logic, allowing for smaller and more power-efficient FPGA configurations.
- Enables system designers to reduce BOM cost while maintaining high performance.



Gowin FPGA TDC architecture

Benchmarks

- 8 bits TDC in GW1N-1K, resolution can be 30ps or less
- 16 bits TDC in GW1N-2K works well @ 960MHz (7.8cm TDC)
- 32 bits in GW5A-138K tested @1650MHz (4.54cm TDC)
- 16 bits in GW5A-138K tested @1600MHz (4.69cm TDC)

Note, the clock frequency is the CLK in IOLogic driven by PLL.

The resolution X C = distance, where C is the speed of light

Summary

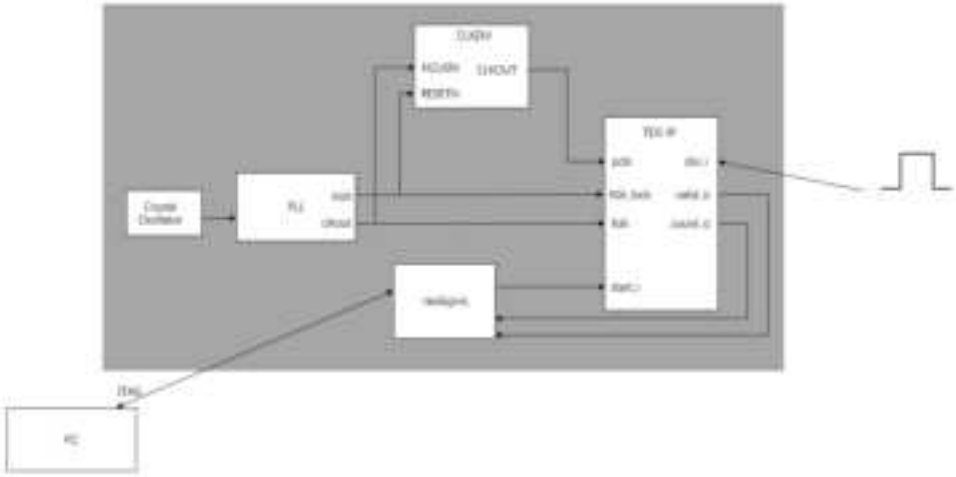
While traditional FPGA-based TDCs offer flexibility, they often fall short in terms of consistency, environmental stability, and scalability. Gowin's dedicated IO-based delay architecture directly addresses these challenges, delivering a stable, accurate, and scalable TDC platform.

By combining high IO count, reduced sensitivity to environmental variation, and low cost, Gowin FPGAs offer a differentiated solution for multi-channel TDC implementations—empowering designers to build faster, more reliable time-domain systems with confidence.

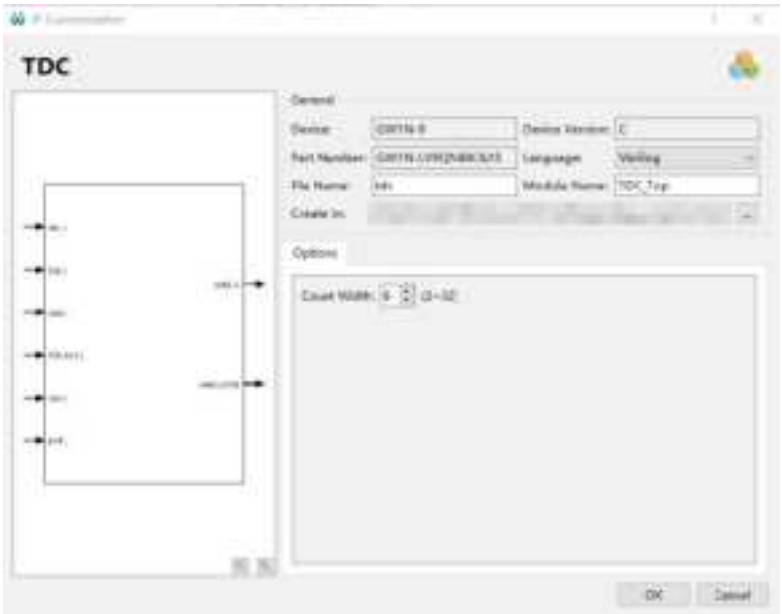
5 Device and IP Support

GOWIN TDC solution can be implemented in all Gowin FPGAs. The resolution will vary depending on the devices. Gowin EDA tools provide TDC IP and Guideline documents to help users to implement this solution. Please see IPUG1208-1.0E_Gowin TDC IP User Guide.

Here is the EDA software view of this IP.



Here is the IP core generator view:



6 Real World Applications

1. 3D Time-of-Flight (ToF) Cameras

▸ Use Case:

ToF cameras are used in mobile devices, industrial automation, gesture control, and augmented reality systems. They emit a short light pulse (typically from a VCSEL) and measure the time it takes for light to bounce off an object and return to the sensor.

▸ Role of FPGA TDC:

- Each SPAD (Single Photon Avalanche Diode) pixel in a ToF image sensor detects individual photons.
- A TDC in the FPGA measures the arrival time of the first photon per pulse.
- Timing precision of 20–100 ps enables accurate depth resolution (down to millimeter scale).
- Multiple TDCs may run in parallel (one per pixel or pixel group) to support high-resolution, real-time depth maps.

▸ Why FPGA:

- FPGAs provide massive parallelism, essential for capturing data from hundreds or thousands of SPADs simultaneously.
- They also allow real-time histogramming and digital filtering, minimizing external processing and improving accuracy.

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2. Quantum Optics & Time-Correlated Photon Counting (TCSPC)

▸ Use Case:

In quantum communication, quantum key distribution (QKD), and fluorescence lifetime imaging (FLIM), precise photon arrival time is critical. Researchers use these systems to study entanglement, photon correlations, and lifetimes at the single-photon level.

▸ Role of FPGA TDC:

- TDCs capture photon arrival timestamps with picosecond precision.
- Used in Time-Correlated Single Photon Counting (TCSPC) to build statistical histograms of photon events over time.
- Events are often random and sparse, requiring high-resolution, high-sensitivity, low-dead-time timing logic.

▸ Why FPGA:

- FPGA-based TDCs can be deeply customized for trigger logic, filtering, gating, and correlation algorithms.
- Researchers often use multi-channel TDCs to correlate events across different detectors.
- FPGA implementation offers real-time processing, eliminating the need for bulky post-processing steps.

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3. Digital Oscilloscopes and Signal Analysis

▸ Use Case:

Modern oscilloscopes (especially digital sampling scopes and time interval analyzers) rely on high-precision time capture to measure jitter, edge timing, and propagation delays in high-speed circuits and communication interfaces.

▸ Role of FPGA TDC:

- TDCs measure time intervals between fast rising/falling edges far more precisely than typical clocked sampling (which is limited to ~200ps at 5 GHz).
- TDCs can enable interpolation between sample points, enhancing effective timing resolution.
- Used for jitter analysis, eye diagram generation, and signal integrity testing.

▸ Why FPGA:

- FPGA fabric is ideal for implementing custom trigger logic, cross-domain synchronization, and time-tagging systems with minimal latency.
- In portable or embedded scopes, TDCs in FPGAs can reduce BOM cost while still achieving professional-grade accuracy.

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4. Precision LiDAR Systems

▸ Use Case:

In autonomous vehicles, drones, and surveying systems, LiDAR (Light Detection and Ranging) is used to build real-time 3D maps of the environment. Precision timing is key to converting photon return time into accurate distance.

▸ Role of FPGA TDC:

- Each laser pulse reflected off an object is captured by a detector (e.g., SPAD or APD).
- The TDC measures the time from laser emission to photon return.
- Timing resolution directly impacts ranging accuracy: e.g., 10 ps resolution ≈ 1.5 mm distance accuracy.

- Why FPGA:

  - LiDAR often requires multi-beam systems with multiple detectors firing rapidly (up to millions of events per second).
  - FPGA TDCs allow scalable parallelism and on-the-fly filtering to reject noise, ambient light, and invalid events.
  - TDCs implemented in IOs (as in Gowin FPGAs) reduce latency and power, critical for embedded mobile LiDAR.

A reconstructed 3D model by using 128-channel TDCs in the GW5A-138K device

7 A DIY Project example

You can indeed build an ADC (Analog-to-Digital Converter) using TDC (Time-to-Digital Converter) principles. This method is often called a Time-Based ADC or Time-Encoding ADC, and it leverages the conversion of an analog voltage into a time interval, which is then measured by a TDC.

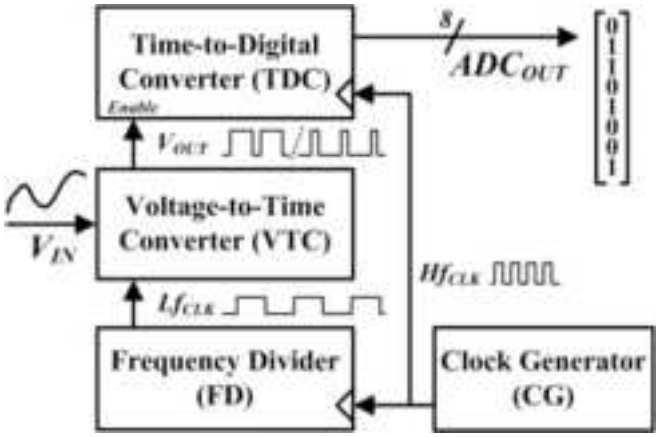
Here’s how it works, how it's constructed, and where it's useful:

Basic Idea:

Instead of directly digitizing voltage levels (as in a traditional ADC), you convert the analog voltage into a time delay, and then measure that delay using a Time-to-Digital Converter.

Voltage → Time → Digital

This approach takes advantage of the high timing resolution of modern TDCs, often enabling very fine quantization steps with lower power and simpler analog front ends.



How It Works: Core Components

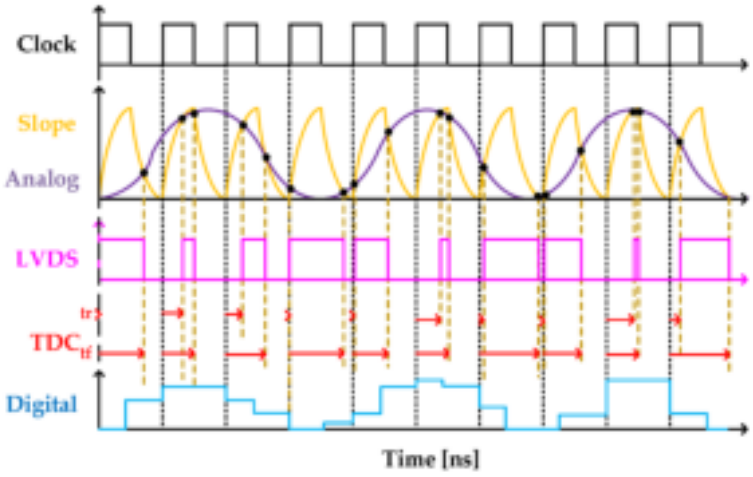
1. Voltage-to-Time Converter (VTC)

- This circuit converts the analog input voltage into a time delay.
- Common implementations:
  - Ramp Generator + Comparator:
    - A reference voltage ramps linearly.
    - When it crosses the input voltage, a comparator triggers the stop signal.
    - The time from start of ramp to trigger = analog voltage.
  - Current-Starved Delay Chain:
    - Delay elements modulated by analog voltage control current (and therefore delay).
    - Used in some VCO-based architecture.

2. Time-to-Digital Converter (TDC)

- Once the analog voltage is converted into a delay (a time interval), a high-resolution TDC digitizes that time.
- The output is a digital code corresponding to the original input voltage.

Timing Diagram (Conceptual)

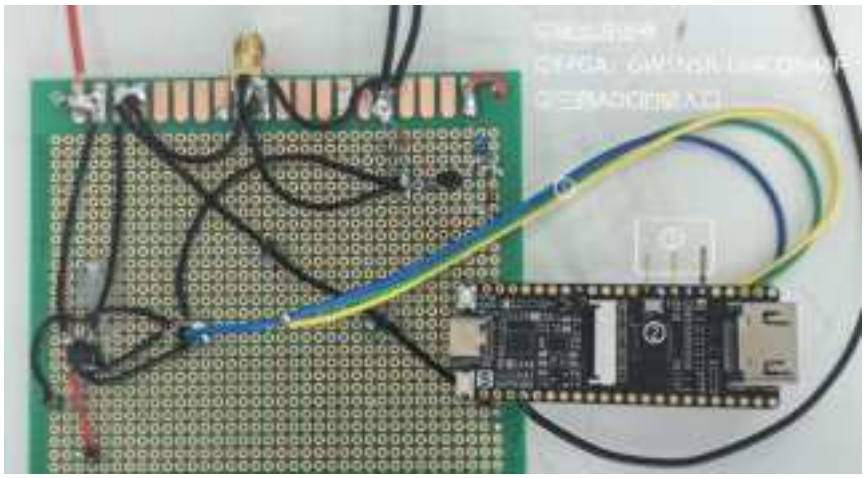


Timing Diagram of ADC based on TDC

ADC Performance Overview

Reference implementation and performance validation were conducted on the TANG Nano 4K development board (Chip: GW1NSR-LV4CQN48PC7/I6).

Testing Setup



Results

- Resolution: 7-bit
- Sample Rate: 60 kSPS to 1 MSPS
- Linearity (INL):
  - ±6 LSB @ 60 kSPS
  - ±10 LSB @ 1 MSPS
  - *(1 LSB = 10 mV)*
- Input Range: 0–0.8 V
- Effective Resolution: ~6.5 bits

FPGA Resource Utilization (Per ADC Channel)

- Logic Registers: 160
- Block SRAM (BSRAM): 1 block
- IDES8: 1 unit
- PLL: 1
- LVDS Differential Pair: 1
- Single-Ended I/O: 1

This makes the solution efficient for integration into small, cost-sensitive FPGAs while preserving sufficient logic and memory for additional system logic or control tasks

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Advantages

- High Resolution: TDCs can achieve ps-level resolution, translating to high-bit ADCs without expensive analog components.
- Low Power: Especially in applications that need low sampling rates (e.g., instrumentation).
- Digital-Friendly: Most of the system is digital, making it ideal for FPGA or ASIC implementation.

Challenges

- Nonlinearity: VTCs (especially ramp generators) often suffer from nonlinearity and temperature drift.
- Calibration: Requires runtime or startup calibration to maintain accuracy.
- Speed Limitations: Faster input conversion needs faster ramp/delay control, which becomes challenging.
- Noise Sensitivity: Analog front-end still needs a careful design to reduce jitter and drift.

Applications

- Low-speed, high-resolution sensors (e.g., temperature, pressure, bio-sensing)
- Time-domain signal processing
- FPGA-based instrumentation
- Neuromorphic or event-based processing
- Radiation-hardened or simplified ADC designs for harsh environments

8 Conclusion

Time-to-Digital Converters are at the heart of many emerging technologies, from high-resolution 3D imaging and LiDAR to quantum research and precision instrumentation. While FPGAs have long been a flexible platform for TDC design, traditional implementations often face limitations in timing accuracy, environmental stability, and scalability.

GOWIN Semiconductor addresses these challenges with a novel IO-based TDC architecture, delivering consistent and precise delay lines that are inherently less sensitive to temperature, voltage, and process variations. This architecture not only improves measurement linearity and timing resolution but also enables high channel density and efficient power utilization, critical for modern applications that demand real-time performance and compact form factors.

By integrating TDC functionality into dedicated IO resources, GOWIN FPGAs simplify design complexity, reduce calibration overhead, and lower total system cost. The result is a scalable, robust, and cost-effective timing solution ideal for engineers and system designers pushing the boundaries of time-domain performance.

As the need for precise timing grows across industries, GOWIN's FPGA-based TDC solution provides a reliable foundation for innovation, empowering next-generation systems with the accuracy, flexibility, and efficiency required to meet tomorrow's demands.

9 Reference

Trademark Acknowledgments:

Support and Feedback

GOWIN Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

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Revision History

Date	Version	Description
2025/07/08	1.0E	Initial draft

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