Evaluating the AD4080 Fast Precision 20-Bit, 40MSPS, Differential SAR ADC

FEATURES

- Full featured evaluation board for the AD4080 with power solution
- Single differential channel and common-mode input available through board SMA connectors
- The Analysis | Control | Evaluation (ACE) Software plugin is available for device configuration, data capture, and performance evaluation
- Flexible analog front end (two stages)
- Out-of-box evaluation experience with the SDP-K1 demonstration platform (EVAL-SDP-CK1Z)
- On-board low noise power solution and 3.0V precision reference
- On-board clock generation circuitry with sampling frequency selection via ACE software
- Compatible with Arduino Uno form factor (Rev3 form factor)

EVALUATION BOARD KIT CONTENTS

- EVAL-AD4080ARDZ evaluation board
- 12V AC/DC external wall mount adapter

EQUIPMENT NEEDED

- PC running Windows 10 operating system or higher
- EVAL-SDP-CK1Z digital host controller board and supporting USB cable (referred to in the text that follows as the SDP-K1)
- Differential precision signal source (the ADMX1001B precision signal source is preferred)
- 7V to 12V DC source (12V AC/DC external wall mount adapter supplied with evaluation kit)
- Two Subminiature Version A (SMA) to SMA cables to connect a differential signal source to the evaluation board

GENERAL DESCRIPTION

The EVAL-AD4080ARDZ evaluation board enables quick and easy evaluation of the performance and features of the AD4080. The EVAL-AD4080ARDZ is designed to demonstrate the performance of the AD4080 features in the ACE software environment. The EVAL-AD4080ARDZ evaluation kit supports the following AD4080 features:

- Serial peripheral interface (SPI) complementary metal-oxide semiconductor (CMOS) data output interface (read from first-in first out (FIFO))
- Analog-to-digital converter (ADC) configuration via SPI
- Internal or external generation of 1.1V regulated supply rails (external by default)
- Sampling rate capability 40/20/10MSPS (software selectable in ACE)

The EVAL-AD4080ARDZ evaluation board is designed for use with the system demonstration platform (SDP-K1) board to facilitate communication with the AD4080, enabling ADC configuration and data capture. The SDP-K1 controller board also provides the communication link to the host PC and the ACE software plugin. The primary controller board for the EVAL-AD4080ARDZ evaluation board is the SDP-K1. The EVAL-AD4080ARDZ evaluation board conforms to the Arduino Uno Shield mechanical and electrical standards to interface with the SDP-K1.

The EVAL-AD4080ARDZ evaluation solution includes the AD4080 industrial input and output (IIO) firmware application drivers for device configuration and ADC data capture. It also includes the AD4080 ACE plugin graphical interface (GUI) for performance evaluations.

For full details, see the AD4080 data sheet, which must be used in conjunction with this user guide when using the EVAL-AD4080ARDZ.

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REVISION HISTORY

4/2025—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPH

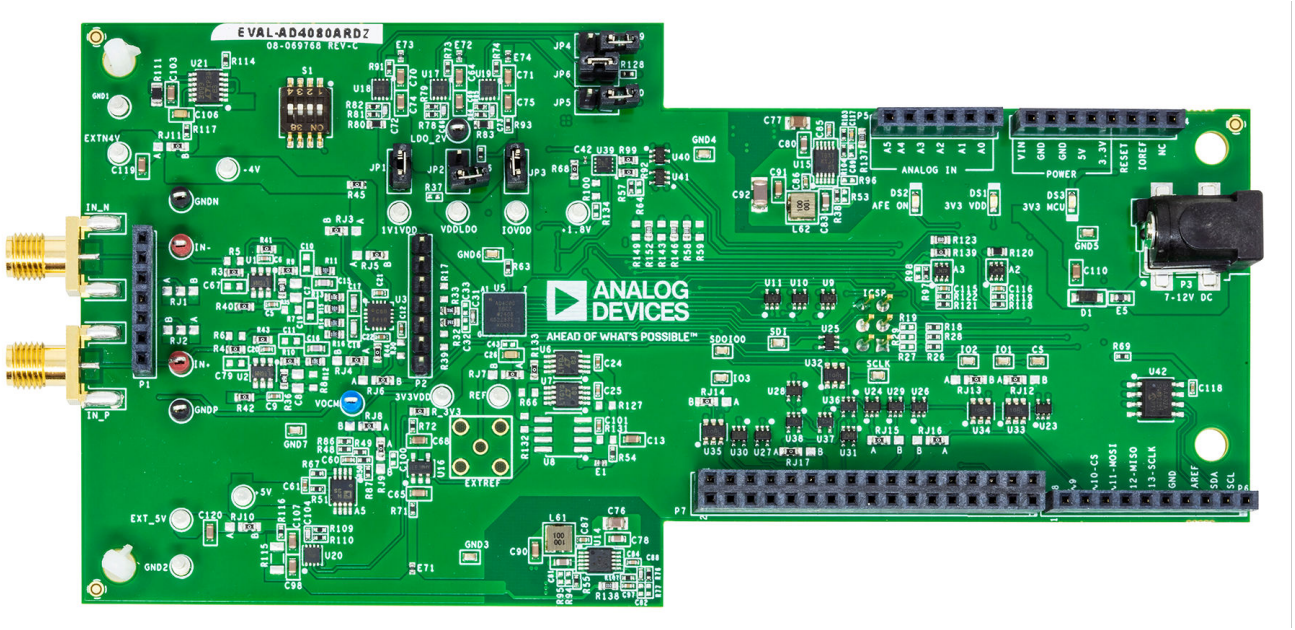


Figure 1. EVAL-AD4080ARDZ Evaluation Board Photograph—Top

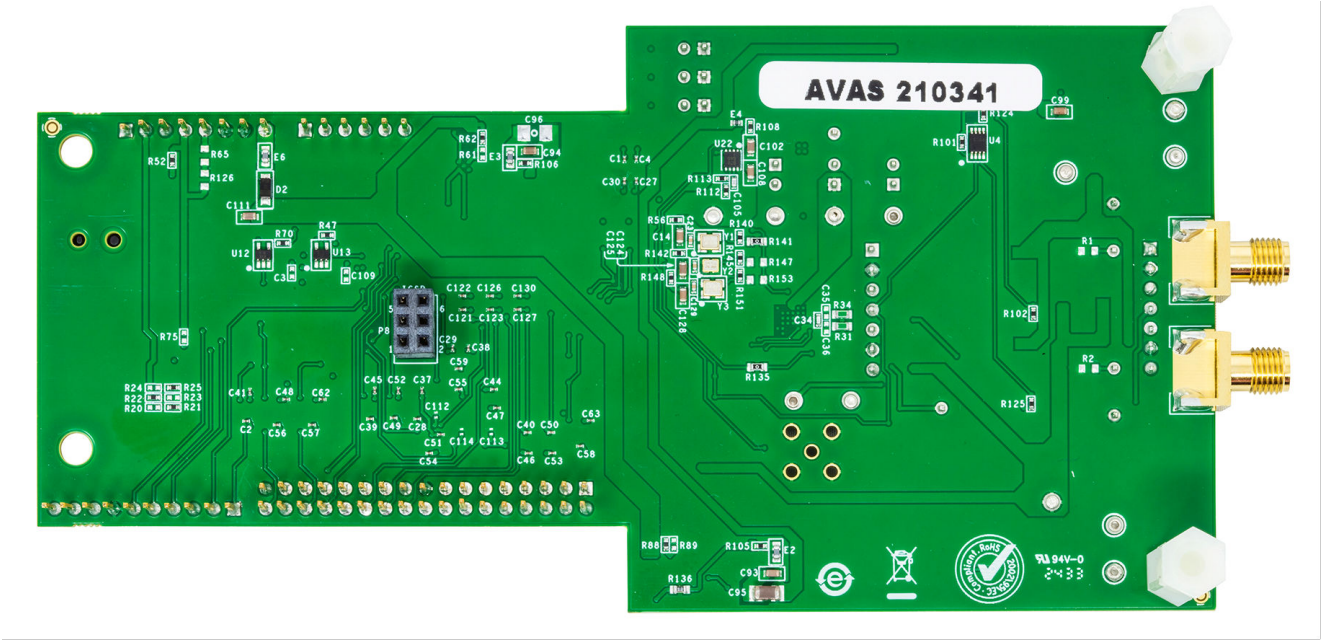


Figure 2. EVAL-AD4080ARDZ Evaluation Board Photograph—Bottom

EVALUATION BOARD HARDWARE GUIDE

HARDWARE OVERVIEW

A simplified block diagram of the EVAL-AD4080ARDZ hardware is shown in Figure 3. This evaluation board showcases the performance and features of the AD4080, and highlights the recommended companion components.

The EVAL-AD4080ARDZ enables effortless evaluation of the AD4080. All circuitry necessary to operate the AD4080 is included on the EVAL-AD4080ARDZ. See the Analog Input Circuit section, the Voltage Reference section, the Power Supplies Generation section, the Conversion and Data Clock Generation Circuit section, and the Digital Interface section for detailed specifics on each circuit block shown in Figure 3. For those blocks that can be modified to achieve different configurations, see the Supported Configurations section for additional details on how to implement these changes.

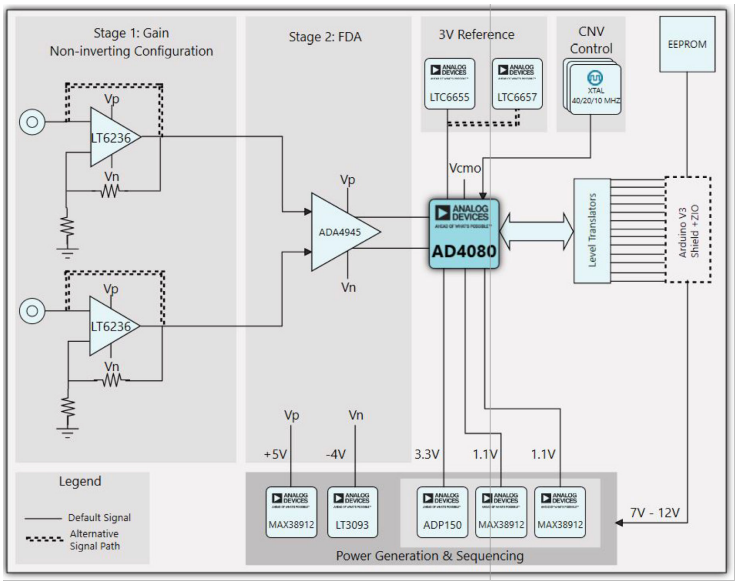


Figure 3. Simplified Block Diagram of the Evaluation Board

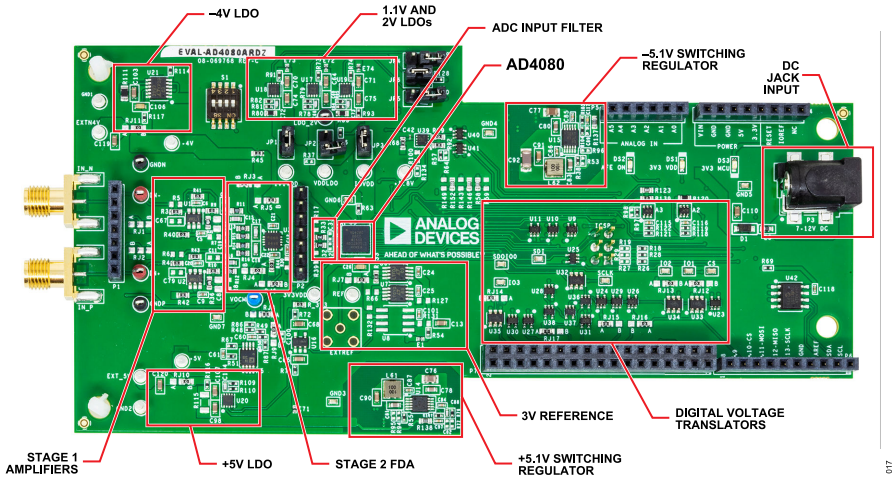


Figure 4. EVAL-AD4080ARDZ Evaluation Board Circuitry Locations—Top Side

EVALUATION BOARD HARDWARE GUIDE

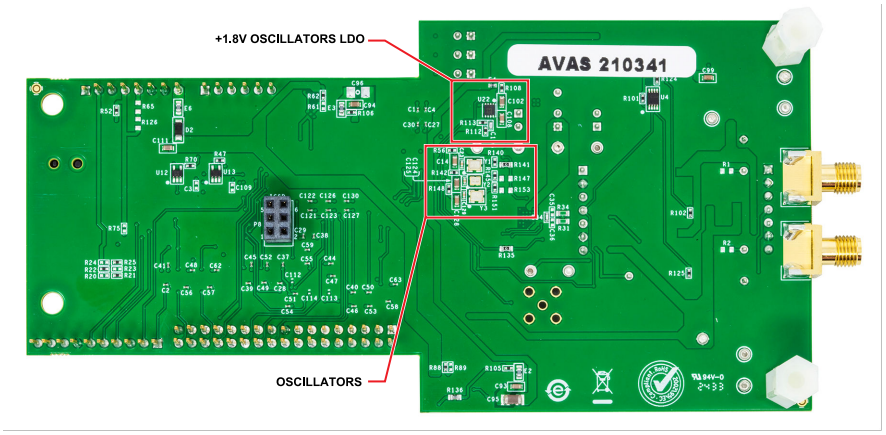


Figure 5. EVAL-AD4080ARDZ Evaluation Board Circuitry Locations—Bottom Side

ANALOG INPUT CIRCUIT

The EVAL-AD4080ARDZ includes a two-stage, precision signal conditioning circuit. The design is partitioned in this fashion to allow the greatest flexibility in optimizing signal chain performance for the targeted signal bandwidth for both evaluation and prototyping.

With the default configuration of the evaluation hardware, a differential 6V p-p input signal with the common-mode set to 1.5V results in a full-scale measurement from the ADC. The typical supported input frequency range is DC to 1MHz.

Recommendations regarding signal chain configuration for particular signal bandwidths of interest can be found in the Analog Front End (AFE) Considerations section.

INPUT STAGE (STAGE 1)

The input stage consists of a pair of LT6236 operational amplifiers (op amps) (U1 and U2). The LT6236 op amps are selected for their exceptional wideband (90MHz), low noise, favorable distortion performance, and low power consumption. The stage is configured for differential input, differential output, noninverting, unity-gain operation, ensuring that a preceding signal source or sensor is presented with a high impedance. With supply rail values of +5V and −4V, the valid range for the LT6236 inputs (INP and INM) is approximately −2V to +4V, which means that a common-mode voltage of 1.5V (available at V_{OCM}) for the inputs is close to ideal to allow maximum voltage range and minimize distortion.

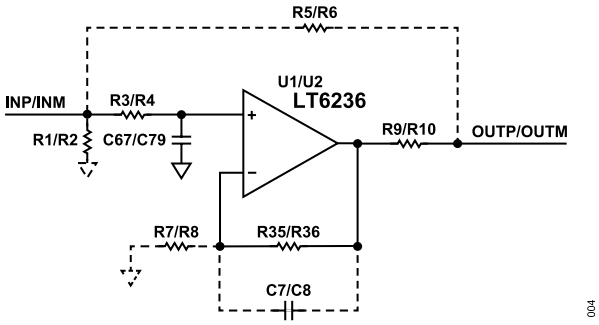


Figure 6. Stage 1 Simplified Schematic

The following can be configured in this stage:

- Stage bandwidth
  - No explicit bandwidth limiting (default)
  - Band limiting through RC input filter and/or capacitors across amplifier feedback
- Stage gain
  - Unity gain (default)
  - Noninverting gain setting
- Stage bypass
  - No bypass (default)
  - Bypass Stage 1
  - Bypass Stage 1 along with Stage 2 to use an amplifier mezzanine card (AMC) instead
- Input signal type
  - Differential (default)
  - Single-ended

EVALUATION BOARD HARDWARE GUIDE

FULLY DIFFERENTIAL AMPLIFIER STAGE (STAGE 2)

Stage 2 utilizes an ADA4945-1 (U3) fully differential amplifier configured for unity gain.

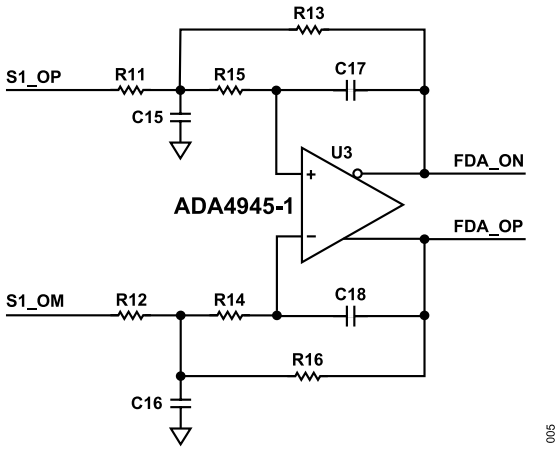


Figure 7. Stage 2 Simplified Schematic

The clamp pins of the ADA4945-1 ($-V_{CLAMP}$ and $+V_{CLAMP}$) are connected to the GND and VREF nodes respectively, which results in a limitation of the range at the output of the fully differential amplifier (FDA) of ~500mV beyond those nodes to protect the ADC from hard overdrive.

The common-mode input of the ADA4945-1 is floating by default, meaning that the output common-mode value is internally biased at a voltage equal to the midpoint between the output voltage clamps, that is, 1.5V.

With the default configuration, this stage presents a 3dB cutoff frequency of 1.1MHz at the output (measured at FDA_ON and FDA_OP nodes).

The following can be configured in this stage:

- Stage bypass
  - No bypass (default)
  - Bypass Stage 2
- ADA4945-1 power mode
  - Full power mode (default) achieves the maximum device bandwidth and best distortion performance.
  - Low-power mode minimizes power at the cost of distortion performance and reduces the amplifier bandwidth.
- Alternative amplifier installation
  - ADA4940-1
  - ADA4932-1
- Stage bypass
  - No bypass (default)
  - Bypass along with Stage 1 for using the AMC

VOLTAGE REFERENCE

The AD4080 requires an external 3V voltage reference. To achieve the specified performance, a suitable precision, low noise voltage reference must be used. AD4080 includes internal reference buffers and capacitors that make reference selection easier and eliminates the need for external buffers.

The following can be configured in this circuit:

- Reference selection
  - The LTC6655-3 is the default. The evaluation hardware includes LTC6655-3 (U6) as the primary recommended option, providing exceptional noise performance (0.1Hz to 10Hz noise specification of 0.25ppm p-p), combined with an initial accuracy of 0.025%, and a low temperature drift of 2ppm/°C.
  - The LT6657-3 (U7) is also mounted and provided as a second option. For that, a small configuration change is needed. R133 should be removed and placed into R66, and the R127 0Ω link should also be placed.
  - Alternatively, there is a footprint on the evaluation board for ADR4530B (U8) that can be mounted and provided as a third option for reference. See Table 1 for a comparison of recommended references. Similarly to the previously mentioned configuration, any 0Ω links from the LTC6655-3 and LT6657-3 should be removed and placed on R131 and R132.

Table 1. 3V Reference Comparison of the LT6657, LTC6655, and ADR4530B

Parameter	LT6657	LTC6655	ADR4530B
Accuracy (%)	0.10	0.025	0.02
Temperature Coefficient (ppm/°C)	1.5	2	2
0.1Hz to 10Hz Noise (ppm p-p)	0.5	0.25	0.53
Maximum Load (mA)	±10	±5	±10
Load Regulation (ppm/mA)	0.7	3	30
Maximum Supply (V)	40	13.2	15
Shutdown	Yes	Yes	No
Reverse Supply Protected	Yes	No	No
Reverse Output Protected	Yes	No	No
Current Limit	Yes	Yes	No
Thermal Protection	Yes	No	No
Shunt Mode	Yes	No	No
Supply Current, I_S (mA)	1.2	5	0.7
T_A (°C)	−40 to +125	−40 to +125	−40 to +125

COMMON-MODE CIRCUIT

The AD4080 includes a common-mode voltage generation feature. The common-mode voltage is equal to reference voltage (V_{REF})/2, and this voltage is provided through the CMO pin of the AD4080. The common-mode voltage generation feature is generally useful for biasing front-end stages, but it is optional to use this feature because the ADA4945-1 can use an internal biasing circuit to set the output common mode to the midpoint of the output clamping pins ($-V_{CLAMP}$ and $+V_{CLAMP}$).

The following can be configured in this circuit:

EVALUATION BOARD HARDWARE GUIDE

- FDA common-mode setting
  - Internal (default): The ADA4945-1 sets the output common-mode level to the output clamps midpoint.
  - External: Use the CMO voltage provided by the ADC to set the fully differential ADC driver amplifier (FDA) output common-mode level.
- Common-mode signal buffering
  - No buffering (default).
  - Buffering through the ADA4807-2 (A5) amplifier, which is only necessary if an additional load is placed on the AD4080 CMO output. Note that this output has an output impedance of 700Ω; consult the AD4080 data sheet for additional details.

POWER SUPPLIES GENERATION

The EVAL-AD4080ARDZ is designed to operate from a 7V to 12V supply provided by an AC/DC wall adapter. The 7V to 12V power supply is regulated down using a combination of switching regulators and linear dropout (LDO) regulators to generate the necessary power rails for the on-board circuitry.

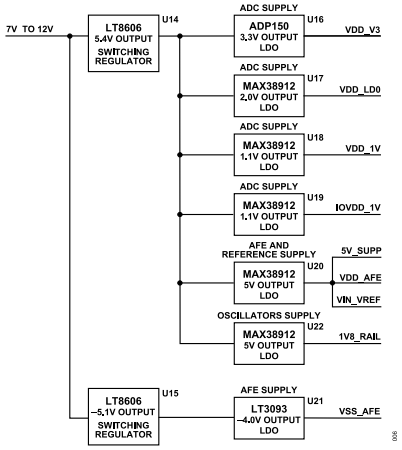


Figure 8. Power Circuitry Simplified Schematic

AD4080 POWER SUPPLY

The AD4080 requires the following three major power supplies:

- VDD33: 3.3V analog supply rail.
- VDD11: 1.1V ADC core supply.
- IOVDD: 1.1V digital interface supply.

The AD4080 includes integrated power supply decoupling; therefore, no external power supply decoupling is included on-board for the AD4080 power supply rails.

The following can be configured in this circuit:

- 1.1V rails (VDD11 and IOVDD) source
  - On-board generated rails (default): The rails are taken in from the MAX38912 regulators (U18 and U19), as shown in Figure 8.
  - Internal AD4080 LDO regulator: An LDO internal to the AD4080 can be enabled and used to power both 1.1V rails. Refer to the AD4080 data sheet for more details pertaining to the power supply rails and requirements.
  - Off-board external supply.
- 3.3V rail source
  - On-board generated rail (default): The rail is supplied by an ADP150 LDO regulator (U16), as shown in Figure 8.
  - Off-board external supply.

EVALUATION BOARD HARDWARE GUIDE

AMPLIFIER POWER SUPPLY

The signal conditioning circuitry of the EVAL-AD4080ARDZ is designed to operate from +5V and −4V rails. The positive and negative rails of the U1 and U2 amplifiers are supplied from the +5 V VDD_AFE rail and the −4V VSS_AFE rail.

The positive and negative rails of the fully differential U3 amplifier are supplied from the +5V VDD_AFR rail and −4V VSS_AFE rail. The common-mode buffer A5 amplifier is configured for a unipolar power supply; the positive supply rail of A5 is provided from the +5V 5V_SUPP rail, and the negative supply rail is connected to ground.

CONVERSION AND DATA CLOCK GENERATION CIRCUIT

The EVAL-AD4080ARDZ contains the necessary circuits to generate low jitter conversion (CNV+) clocks across the full operating range of the AD4080. This low jitter circuitry allows processing with fidelity full-scale input signals up to 1MHz.

The circuit consists of a 40MHz (Y1), 20MHz (Y2), and 10 MHz (Y3) CMOS reference oscillators, shown in Figure 9. That signal is fed directly to the CNV+ pin of the AD4080. Software sets the enable signal to select the conversion frequency by enabling the particular oscillator. In practice, to change the sample rate, the user changes the **Sampling Frequency (MHz)** field in the **Board Level** view of the **ACE Software**, as is detailed in Figure 13. The AD4080 can be evaluated by selecting a conversion frequency of 40MHz.

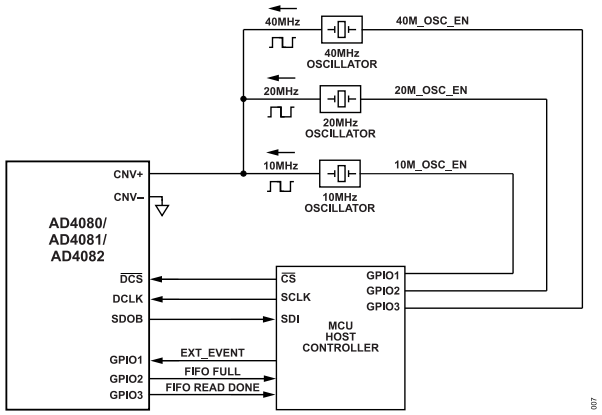


Figure 9. Simplified Diagram of the Clock Circuitry

DIGITAL INTERFACE

The EVAL-AD4080ARDZ utilizes the V3 Arduino connector (P4, P4, P6, and P7) from the SDP-K1 controller board to support ADC device configuration via the 4-wire SPI, conversion result access using the SPI data interface, and conversion control in SPI data interface mode. The SDP-K1 board acts as the medium for communication between the **ACE Software** plug-in and the EVAL-AD4080ARDZ hardware.

The AD4080 operates with a 1.1V digital interface supply voltage. To translate between this 1.1V level and the digital interface voltage level of the SDP-K1 (3.3V), SN74AUP1T34QDCKRQ1 unidirectional voltage level translators (U23, U24, U25, U26, U27, U28, U29, U30, and U31), and SN74AVC1T45DCKR bidirectional level translators (U32, U33, U34, and U35) are used on the EVAL-AD4080ARDZ hardware.

EVALUATION HARDWARE SETUP PROCEDURE

The following procedure must be observed to prepare the hardware for evaluation:

1. Ensure jumper P14 on the SDP-K1 board is set for VIO_ADJUST of 3.3V.
2. Connect the EVAL-AD4080ARDZ board to the SDP-K1 board as shown in Figure 10.
3. Connect the 12V DC power supply included in the evaluation kit, from the wall adapter to the SDP-K1 board barrel jack (P15). The green (DS1), blue (DS2), and blue (DS3) light-emitting diodes (LEDs) should light up upon connecting the DC voltage.
4. Connect the USB cable from the PC to the SDP-K1 board P2 USB-C connector. The orange DS1 connected light-emitting diode (LED) should light up on the SDP-K1 board upon this action.
5. Ensure that the EVAL-AD4080ARDZ configuration jumpers (JP1 to JP6) are set as shown in Figure 10, as follows: JP1, JP3, JP6: on; JP2, JP4, JP5: off.

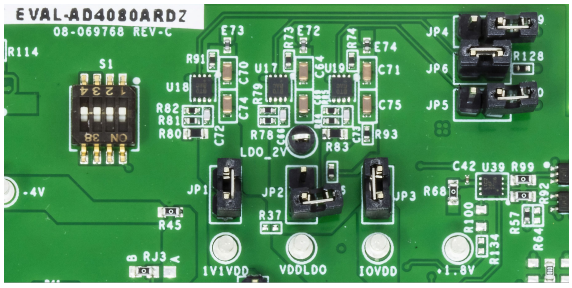


Figure 10. EVAL-AD4080ARDZ Jumpers JP1 to JP6 Setup

6. Ensure the switch (S1) Position 1 to Position 4 are all OFF.
7. The hardware is now ready to be used through the **ACE Software**.

EVALUATION SOFTWARE INSTALLATION

The **ACE Software** is a desktop software application that allows the evaluation and control of multiple evaluation systems from across the Analog Devices, Inc., product portfolio. The EVAL-AD4080ARDZ hardware is controlled and configured through the **ACE Software** with the required software plug-in that can be installed from within the ACE application.

Follow these steps to install the **ACE Software**:

1. Download the **ACE Software** package from the ACE Software web page on the Analog Devices website.
2. Click **'Download ACE Installer'** to download the installer file.
3. Run the installer and follow the instructions to complete the software installation process.

After ACE is successfully installed, the EVAL-AD4080ARDZ plug-in can be installed as follows:

1. Run the **ACE Software** and click on the **Plug-in Manager** in the ACE sidebar, then select **Available Packages**.
2. From the list of plug-ins available, select the **'Board.AD4080'** (note that you can use the **Search** field to help filter the list of boards to find the relevant one), then click **Install selected**.

EVALUATING THE AD4080 WITH THE ACE SOFTWARE

After the hardware setup is complete as per the Evaluation Hardware Setup Procedure section and the software is installed as specified in the Evaluation Software Installation section, the ACE software can be run for evaluation.

When ACE opens, the EVAL-AD4080ARDZ is automatically detected and displayed in the **Attached Hardware** panel, as highlighted in yellow in Figure 11.

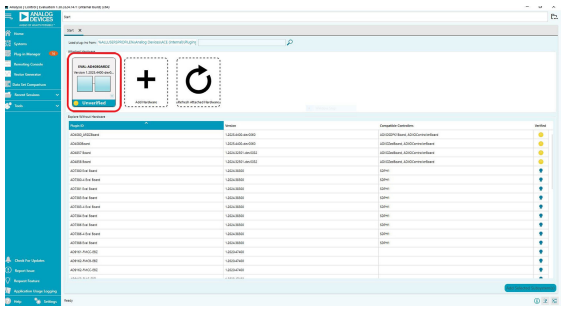


Figure 11. Auto-Detection of the Evaluation Board in the ACE Start Tab

When prompted with **ACE - Tinyiiod Firmware Required** pop up window, as shown below, Click **OK**. This will program the SDP-K1 board with the required firmware for the plug-in in ACE.

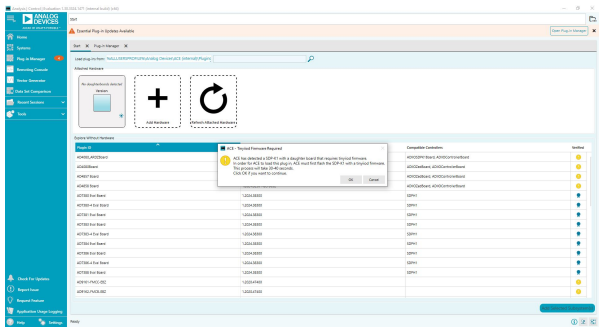


Figure 12. ACE - Tinyiiod Firmware Required Message

Double-click on the EVAL-AD4080ARDZ icon, and a new tab, **EVAL-AD4080ARDZ**, opens displaying a block diagram of the EVAL-AD4080ARDZ as shown in Figure 13.

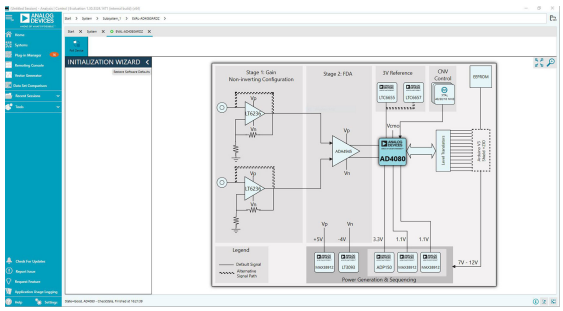


Figure 13. EVAL-AD4080ARDZ Tab Open in the ACE Software

This offers a **Board Level** view of the EVAL-AD4080ARDZ.

Double-clicking on the AD4080 from the block diagram now opens an AD4080 tab. This tab displays an **INITIAL CONFIGURATION** panel, a block diagram of the AD4080 chip, and two buttons in the lower-right corner (**Proceed to Memory Map** and **Proceed to Analysis**), which are highlighted in yellow in Figure 14.

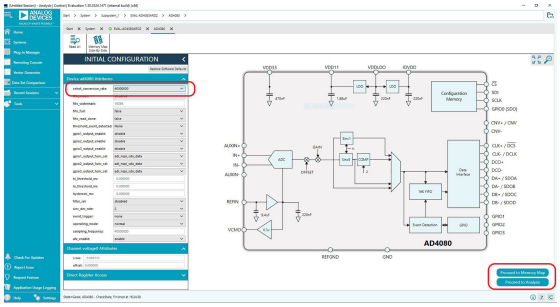


Figure 14. AD4080 Tab in the ACE Software

The tabs that are accessed through these two buttons provide the means to evaluate the AD4080 chip. See the AD4080 Memory Map section and the ANALYSIS Tab section for additional details. The sampling frequency can be configured within this window because it can control the required configuration of the supporting clocking components, as well as controlling the synchronization of the EVAL-AD4080ARDZ data with the SDP-K1 board. As a default, the **Sampling Frequency (MHz)** field is configured for 40MHz. Maximum sample size can be set to 16384 and the minimum sample size is 1.

AD4080 MEMORY MAP

Click **'Proceed to Memory Map'** within the AD4080 tab to open the **AD4080 Memory Map** tab, shown in Figure 15.

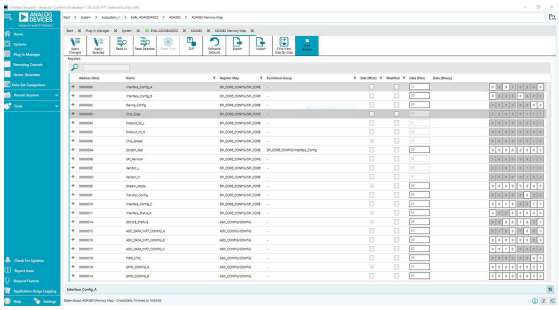


Figure 15. AD4080 Memory Map Tab in the ACE Software

This tab displays the registers from the AD4080 and can be used to read and write (if applicable) their content. For normal operation of the evaluation kit, no modifications are required to the ADC registers.

EVALUATING THE AD4080 WITH THE ACE SOFTWARE

ANALYSIS TAB

Click **'Proceed to Analysis'** within the AD4080 tab to open the **ANALYSIS** tab. This tab is used for capturing data through the evaluation board and analyzing the obtained data.

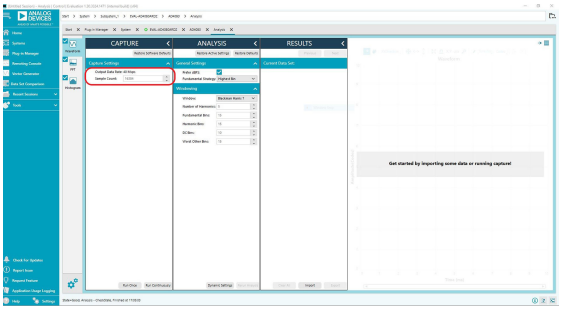


Figure 16. Analysis Tab in the ACE Software

The **ANALYSIS** tab contains three collapsible panels (**CAPTURE**, **ANALYSIS**, and **RESULTS**) and a data plot area to the right. Collapsing any of the three panels is done by clicking on the arrow located to the right of the panel name, which is useful to leave more space for the data plot area when needed.

- The **CAPTURE** panel allows setting the number of samples to be captured per dataset, triggering the acquisition of a single dataset, and initiating or stopping the continuous acquisition of a dataset.
- The **ANALYSIS** panel displays options related to the frequency domain analysis.
- The **RESULTS** panel provides metrics for the current dataset being displayed in the plot area. Different metrics are provided depending on the kind of plot that is selected (see the Time Domain (Waveform) Plot section, Frequency Domain (FFT) Plot section, and Histogram Plot section for additional details). This panel also allows navigating between the datasets acquired during the session and facilitates importing and exporting datasets in the internal format used by the **ACE Software**.

The user has the option to display the acquired datasets as a time domain waveform (default option), a frequency domain plot through a fast Fourier transform (FFT), or as a histogram, which is selected by clicking on any of the three corresponding buttons located to the left of the **CAPTURE** panel (see Figure 16).

TIME DOMAIN (WAVEFORM) PLOT

The active dataset can be displayed as a time domain waveform by clicking on the **Waveform** area highlighted in yellow in Figure 17, which is the default view. Note how the **CAPTURE** and **ANALYSIS** panels are collapsed for an improved display of the plot.

When the dataset is plotted as a time domain waveform, the **RESULTS** panel displays metrics relevant to time domain analysis: minimum, maximum, average, RMS, and so on.

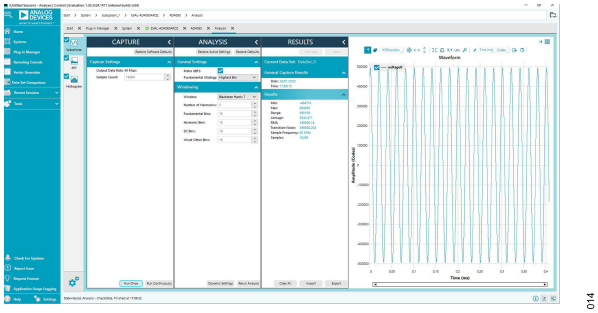


Figure 17. Dataset Plotted as Time Domain Waveform

FREQUENCY DOMAIN (FFT) PLOT

The active dataset can be displayed as a frequency domain plot by clicking on the **FFT** area highlighted in yellow in Figure 18. The plot then displays the FFT of the active dataset. In this case, the **Log Scale** is selected for the **Frequency (MHz)** axis above the graph.

When the dataset is plotted as a frequency domain plot, the **RESULTS** panel displays metrics relevant to frequency domain analysis: signal-to-noise ratio (SNR), dynamic range (DR), signal-to-noise and distortion ratio (SINAD), noise, and total harmonic distortion (THD).

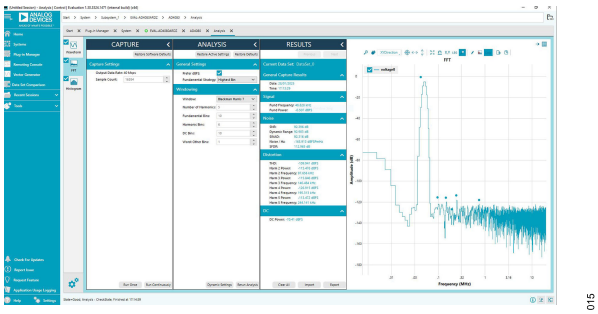


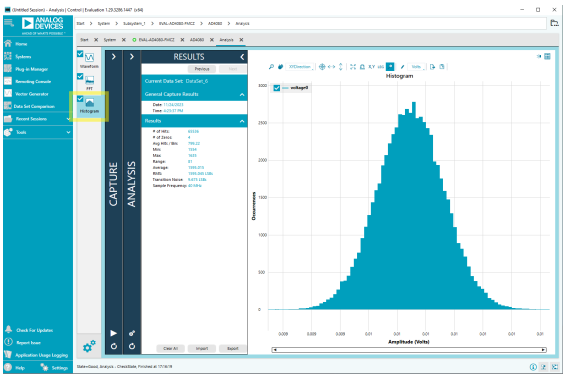
Figure 18. Dataset Plotted in the Frequency Domain

HISTOGRAM PLOT

The active dataset can be displayed as a histogram by clicking on the **Histogram** area highlighted in yellow in Figure 19. In this view, the vertical axis represents occurrences (bin hits) and the horizontal axis can be set to display either code or volt amplitude bins.

When the dataset is plotted as a histogram, the **RESULTS** panel displays metrics relevant to histogram analysis, such as minimum code, maximum code, RMS, and so forth.

EVALUATING THE AD4080 WITH THE ACE SOFTWARE



016

Figure 19. Dataset Plotted as a Histogram

SUPPORTED CONFIGURATIONS

The following sections describe the hardware and software configurations that the EVAL-AD4080ARDZ supports.

ANALOG FRONT-END

Stage 1 Bypass

Optionally, Stage 1 can be bypassed to allow direct drive of the second stage (FDA) from the SMA connectors.

To bypass Stage 1, do the following:

- Remove R3, R4, R9, and R10 to disconnect the Stage 1 amplifiers from the stage input and output.
- Populate R5 and R6 with 0Ω resistors to create the bypass path. Close Switch 1 and Switch 2 from the Switch Array S1 (see Table 2), to power down the now unused U1 and U2 amplifiers.

Stage 1 Gain

Stage 1 amplifiers are arranged for unity gain by default; however, this gain can be changed to a noninverting gain configuration.

To set the desired gain, choose a feedback resistance (R_{FB}) to gain resistance (R_G) ratio according to the following equation:

$$Gain = 1 + \frac{R_{FB}}{R_G} \quad (1)$$

The necessary changes follow:

- Change the R35 and R36 feedback resistors for a value of R_{FB}. See the LT6236 data sheet for more information on allowed values for R_{FB}.
- Populate R7 and R8 with a value of R_G. See the LT6236 data sheet for more information on allowed values for R_G.

Stage 1 Filtering

A differential, first-order, RC filter can be implemented at the input of Stage 1 to limit bandwidth and reduce noise.

To obtain the desired 3dB cutoff frequency, set values for the frequency capacitance (C_F) and frequency resistance (R_F) per the following equation:

$$f_{3dB} = \frac{1}{2\pi R_F C_F} \quad (2)$$

The following changes are necessary:

- Change R3 and R4 to a R_F value.
- Populate C67 and C79 with a C_F value.

In addition to (or instead of) the RC filter, the C7 and C8 capacitors across the feedback networks can be populated for further filtering.

Stage 1 Alternative Input Signal Sources

Differential Signal Source

In the default board configuration, the signal chain input (Stage 1) is designed to be driven by a fully differential signal source with 0V common mode applied at the SMA inputs (INP and INM). Because the default total gain of the signal chain is 1, an amplitude of 6V p-p in the differential signal results in a full-scale measurement at the ADC (−3V to +3V).

Note that the common-mode input requirement for the AD4080 (1.5V ± 50mV) does not apply to the signal at the input of the board because the ADA4945-1 driving the ADC sets its output common mode independently of the common mode at the input.

Single-Ended Input Source

A single-ended (ground-referenced) AC signal can be fed to one of the EVAL-AD4080ARDZ inputs (for example, INP), while the other input is grounded. An amplitude of 6V p-p results in a full-scale measurement at the ADC (−3V to +3V).

When a single-ended signal source is applied at IN_P, the U1 amplifier that buffers the other input (IN_N) can be optionally disabled and bypassed. The necessary changes to do this are as follows:

- Remove R3 and R9 to disconnect the amplifier input and output from the circuit.
- Populate R5 with a 0Ω resistor to enable the bypass path.
- Close Switch 1 (on position) from Switch Array S1 (see Table 2) to power down the now unused U1 amplifier. Note: the U2 amplifier is used, so Switch Position 2 of the switch should be off.

Stage 2 Alternative Amplifiers

By default, Stage 2 houses an ADA4945-1 low distortion, fully differential amplifier. Note that it is possible to use alternative amplifiers; however, these amplifiers are not included on the EVAL-AD4080ARDZ.

The ADA4940-1 can be used to achieve the lowest power consumption in this stage. When using the ADA4940-1, the noise and distortion performance are expected to degrade relative to the ADA4945-1.

The ADA4932-1 can be used for applications where distortion performance is critical or applications where distortion performance is required up to 10MHz. However, the improved distortion performance comes at the expense of higher power consumption.

Both the ADA4940-1 and ADA4932-1 are footprint compatible with ADA4945-1, although some pin connections must be changed. The necessary changes to use an alternative amplifier are as follows:

- Remove ADA4945-1 from the U3 footprint.
- Populate U3 with the ADA4940-1 or ADA4932-1.

SUPPORTED CONFIGURATIONS

- For the RJ3, RJ5, RJ6 solder links, remove the default linkage (Pad 2 to Pad 3 OR COM to B) and link Pad 1 to Pad 2 instead OR COM to A. For RJ4 remove the default linkage (Pad 2 to Pad 1 OR COM to A) and link Pad 3 to Pad 2 instead OR COM to B. (Refer to the EVAL-AD4080ARDZ schematic on the evaluation kit web page to see the position of the solder links.

COMMON-MODE CMO OUTPUT BUFFERING

By default, the common-mode voltage output from the ADC (CMO pin) is unbuffered and not connected to the V_{OCM} pin of the ADA4945-1. To make that connection, the following hardware modification is required:

- Populate R30 with a 0Ω resistor.

To buffer the CMO output of the AD4080 using an ADA4807-2 amplifier, the following hardware modifications are required:

- For the RJ8 and RJ9 solder links, remove the default linkage (Pad 1 to Pad 2) and link Pad 2 to Pad 3 instead.
- Remove R86.

VOLTAGE REFERENCE

Secondary Voltage Reference

The default reference is the LTC6655-3 (U6). To instead use the LT6657-3 (U7) secondary on-board reference, do the following:

- Remove the R133 resistor to disconnect the U6 output from the reference path.
- Populate R127 and R66 with a 0Ω resistor to connect U7 to the reference path.

There is an alternative third reference that could be used on the evaluation board. There is a footprint for ADR4530B, and this device could be soldered to the board as a third option. To do so, complete the following procedure:

1. Remove the R133 resistor to disconnect the U6 output from the reference path.
2. Remove R127 and R66 to disconnect the U7 output from the reference path.
3. Populate R131 and R132 with a 0Ω resistor to connect U8 to the reference path.
4. Solder the ADR4530B to the U8 footprint.

POWER SUPPLY RAILS

Internal AD4080 LDO Regulators for the 1.1V Rails

By default, the two 1.1V supply rails (VDD11 and IOVDD) required by the AD4080 are supplied by on-board LDO regulators (U18 and U19). The rails can be alternatively powered by two on-chip LDO regulators internal to the AD4080; however, this requires disconnecting the externally generated supplies from VDD11 and IOVDD and connecting a voltage source in the 1.5V to 2.75V range at the VDDLDO pin. The presence of this external voltage at the VDDLDO pin automatically triggers the startup of the internal regulators. A 2V, LDO regulator- (U17)generated rail on the EVAL-AD4080ARDZ is prepared for this function.

Therefore, to enable use of the on-chip LDO regulators, do the following:

- Remove the JP1, JP3, and JP6 jumpers to disconnect the AD4080 1.1V supply inputs from the on-board generated rails.
- Place a jumper across JP2, JP4, and JP5 to connect the 2V rail to the VDDLDO pin.

Off-Board Powering of Individual Power Rails

Any or all of the on-board power rails shown in the Power Supplies Generation section can be externally supplied to the evaluation hardware, which can be useful for evaluating the AD4080 with different power solutions or for measuring the supply currents with benchtop equipment. When providing power to power rails individually from an alternative source, the user must ensure that the source used can provide sufficient voltage and current to properly supply the rail. Failure to do so can result in damage to the on-board components.

LINK CONFIGURATION OPTIONS

The EVAL-AD4080ARDZ contains multiple solder links, jumpers, and a switch array to enable various configurations on the evaluation hardware. Table 2 through Table 7 summarize the functions and default settings of these components.

Table 2. Amplifier Power Mode and Power Down Switch Array (S1) Functionality

Switch	Function	S1 Closed (On)
S1-1	Stage 1 amplifier U1, enable or disable	U1 disabled
S1-2	Stage 1 amplifier U2, enable or disable	U2 disabled
S1-3	n/a	n/a
S1-4	n/a	n/a

SUPPORTED CONFIGURATIONS

Table 3. Solder Link Settings: Analog Front End

Link	Default Pads	Function	Comment
RJ3	Pad 2 to Pad 3	Selects the signal connected to Pin 16 (digital ground, D_{GND}) of the FDA (ADA4945-1, U3). This pin is the ground reference for the disable signal. By default, RJ3 is bridging Pad 2 to Pad 3; therefore, Pin 16 of U3 is connected to the AGND of the hardware.	Change the connection to Pad 1 to Pad 2 of RJ3 to connect Pin 16 to VSS_DRV. Apply this change when swapping the ADA4945-1 for ADA4932-1.
RJ4	Pad 1 to Pad 2	Selects the signal connected to Pin 5 (power mode selection, MODE) of the FDA (ADA4945-1, U3).By default, RJ4 is bridging Pad 1 to Pad 2 selecting high power mode of the ADA4945-1. Therefore FDA mode is connected to VDD_DRV pin by default.	Change the connection to Pad 2 to Pad 3 to connect Pin 5 to VSS_DRV. Apply this change when swapping ADA4945-1 for ADA4932-1.
RJ5	Pad 2 to Pad 3	Selects the signal connected to Pin 13 ($-V_{CLAMP}$) of the FDA. For the ADA4945-1 (U3), Pin 13 is used to select the negative clamp voltage. By default, RJ5 is bridging Pad 2 to Pad 3; therefore, Pin 13 of U3 is connected to AGND.	Change to Pad 1 to Pad2 to connect Pin 13 to VSS_DRV. Apply this change when swapping ADA4945-1 for ADA4932-1.
RJ6	Pad 2 to Pad 3	Selects the signal connected to Pin 8 ($+V_{CLAMP}$) of the FDA. For the ADA4945-1 (U3), Pin 8 selects the positive clamp voltage. By default, RJ6 bridges Pin 2 to Pin 3; therefore, Pin 13 of U3 is connected to REF_F.	Change to Pad 1 to Pad 2 to connect Pin 8 to VDD_DRV. Apply this change when swapping ADA4945-1 for ADA4932-1.

Table 4. Solder Link Settings: External Reference Selection

Link	Default	Function	Comment
RJ7	1-2	Selection of the on board voltage reference (LTC6655, LT6657, or ADR4530B) for the external voltage reference output signal, VREF vs. the external voltage reference through the SMA EXTREF socket. Note: the SMA is not soldered by default on the board.	Change RK7 link from Position 1/Position 2 to Position 2/Position 3 to enable the external reference path.

Table 5. Solder Link Settings: Common-Mode Buffering

Link	Default	Function	Comment
RJ8 and RJ9	1-2	Selection path for the AD4080 common-mode output signal between the buffered and unbuffered options. By default, the unbuffered path is selected.	Change both RJ8 and RJ9 links from Position 1/Position 2 to Position 2/Position 3 to select the buffered path. Remove R86 for buffered option.

Table 6. Solder Link Settings: Digital Interface

Link	Default	Function	Comment
RJ12, RJ13, and RJ14	2-3	For the SPI level translators (U33, U34, and U35), select the direction of the translator. Connecting the DIR pin of the translator high selects direction A to B, connecting the DIR pin of the translator low selects direction B to A. RJ12 (GPIO1) default configuration is A to B.	Do not change the connection in these solder links.

Table 7. Jumper Settings: Internal LDOs and Enable Signals Control

Jumper	Default	Function	Comment
JP2, JP4, and JP5	Disconnected	Select whether the 2V on-board supply rail is connected to the AD4080 internal LDO regulators supply pin or not.	Insert jumpers to supply the internal LDO regulators.
JP1, JP3, and JP6	Connected	Select whether the 1.1V supply rails are supplied by the on-board LDO regulators (U18 and U19) or the internal LDO regulators s from the AD4080.	Remove jumpers to stop using the on-board LDO regulators and use the internal LDO regulators instead.

ANALOG FRONT END (AFE) CONSIDERATIONS

The AFE of the EVAL-AD4080ARDZ can be modified to suit the needs of specific applications. Applying changes to the AFE usually involves trade-offs, and designing the right AFE for an application requires careful consideration. The following sections discuss some of the items that must be taken into consideration when designing or modifying the AFE for this hardware evaluation platform.

INPUT SIGNAL FILTERING

Limiting the bandwidth at the input of the signal chain to the region where the signal of interest lies helps reduce excess noise. This reduction of noise can be achieved by the provided mechanisms in the form of the RC filter at the board input, the addition of the do-not-install (DNI) capacitors in the amplifier feedback network bandwidth adjustment in Stage 1, or the increasing of the capacitance value for the existing capacitors in the FDA feedback loop. Note that the value of filter resistors may have an impact on the overall SNR.

The internal digital filters available inside the AD4080 are a useful feature when considering the filtering in the signal chain as a whole. The user can programmatically set a low-pass filter, choosing a simple Sinc1 filter or a higher order Sinc5 with a sharp roll-off to complement the AFE filter or to help relax its design requirements.

POWER VS. BANDWIDTH VS. NOISE

Choosing the lowest noise, lowest distortion, highest precision, wider bandwidth amplifiers may require more power to be consumed in the AFE to reach the required target performance. Therefore, power-constrained applications must carefully consider the choice of each amplifier.

GAIN

Care must be taken in the signal chain to consider where it is optimum to place gain to maximize the SNR. For example, it may be better to add the required signal gain in a preceding low noise amplifier stage rather than in the FDA that is tasked with driving the AD4080 because the FDA noise gain may have a bigger impact on the signal chain SNR than the gain set by the preceding lower noise stage.

ADC DRIVER STAGE

See the Easy Drive Analog Inputs section in the AD4080 data sheet for details about this topic.

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.