

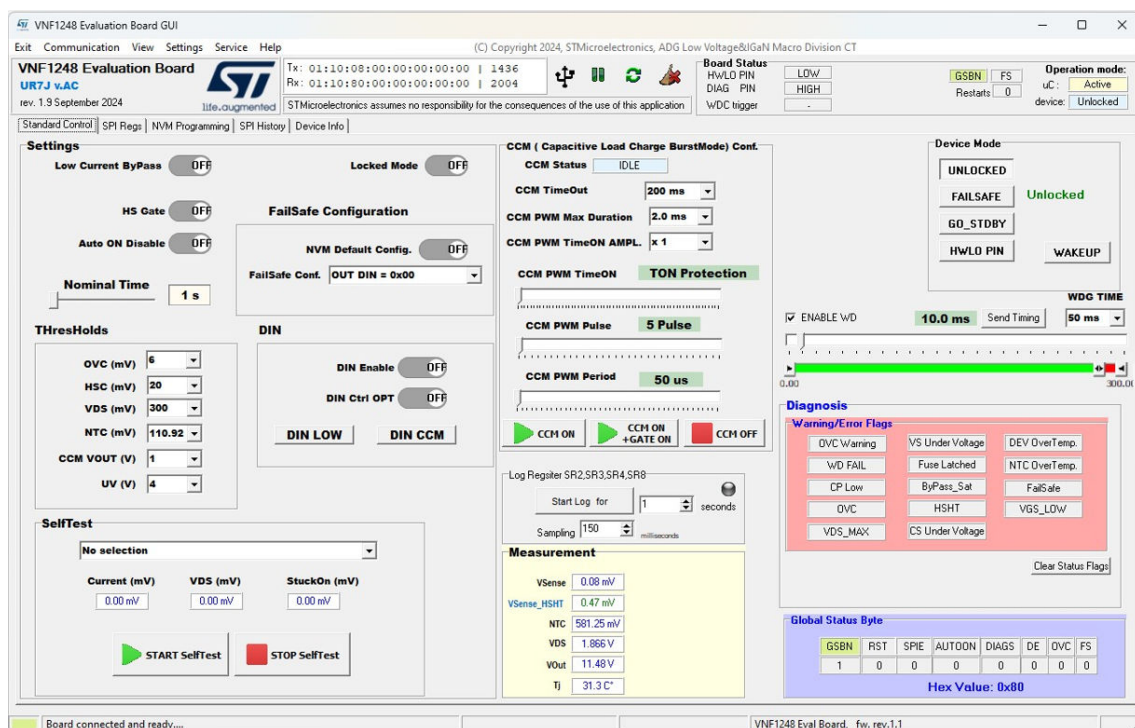
## Getting started with STSW-EV-VNF1248F software package for EV-VNF1248F

### Introduction

The **STSW-EV-VNF1248F** is the companion software package of the **EV-VNF1248F**. It contains the graphical user interface (GUI) and the firmware to be flashed onto the **EV-SPC582B** MCU board.

The combined system of **STSW-EV-VNF1248F** and **EV-VNF1248F** offers a simple evaluation system for the **VNF1248F** device, an advanced controller with eFuse algorithm driving high-side MOSFET in 12 V, 24 V and 48 V automotive applications.

**Figure 1. STSW-EV-VNF1248F Graphical User Interface**



## 1 Get software

To setup and control the [EV-VNF1248F](#) evaluation board through the dedicated Graphical User Interface, a software environment must be acquired, and specifically:

1. The [STSW-EV-VNF1248F](#) software package, which includes the GUI application and the related control firmware to flash onto the [EV-SPC582B](#) microcontroller board
2. The [SPC5-UDESTK Starterkit](#) software application to be used to flash the control firmware on the [EV-SPC582B](#) MCU board

### 1.1 Graphical User Interface and Control Firmware

Visit the dedicated page for [STSW-EV-VNF1248F](#): from the first tab **Overview**, a button is available to get the latest release of the software package in the form of a zip file. It includes the firmware package to control the [EV-VNF1248F](#) evaluation board and a folder with the GUI application to be launched on a desktop PC to communicate with the [VNF1248F](#) device.

Select the tab **Documentation** to retrieve the available documentation about the software package, and the tab **Tools & Software** to find the reference to the [EV-VNF1248F](#) ST web page.

### 1.2 Software ecosystem

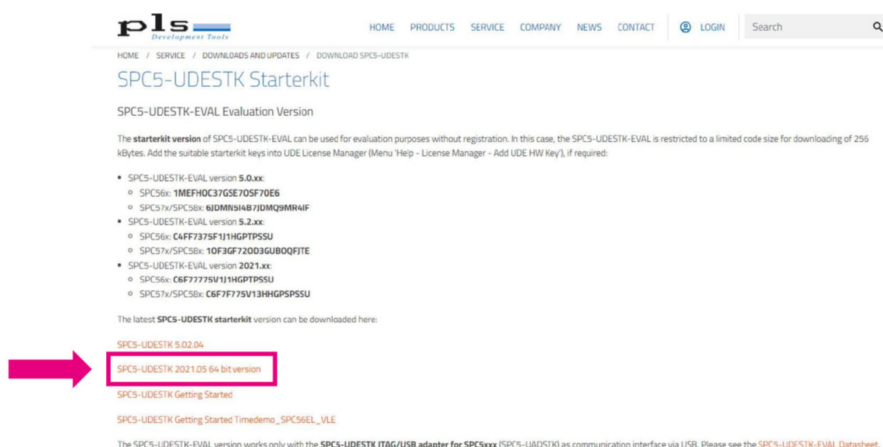
If you have a pre-flashed [EV-SPC582B](#) MCU board with the control firmware for [EV-VNF1248F](#) evaluation board, you can skip this section.

On the contrary, if you need to program the [EV-SPC582B](#) MCU board, a software package installed on your computer is required: [SPC5-UDESTK Starterkit](#).

#### UDE Starterkit 2021

The UDE tool **SPC5-UDESTK 2021.05 64-bit** version (file: **udestk-2021-05-spc5-stk.exe**) is available at: <https://www.pls-mc.com/support/downloads/download-spc5-udestk/>

**Figure 2. SPC5-UDESTK 2021.05 64-bit**



## 2 Software installation

The software ecosystem needed to setup a PC workstation to run the Graphical User Interface provided in [STSW-EV-VNF1248F](#) software package is now described.

### 2.1 Firmware programming tool installation

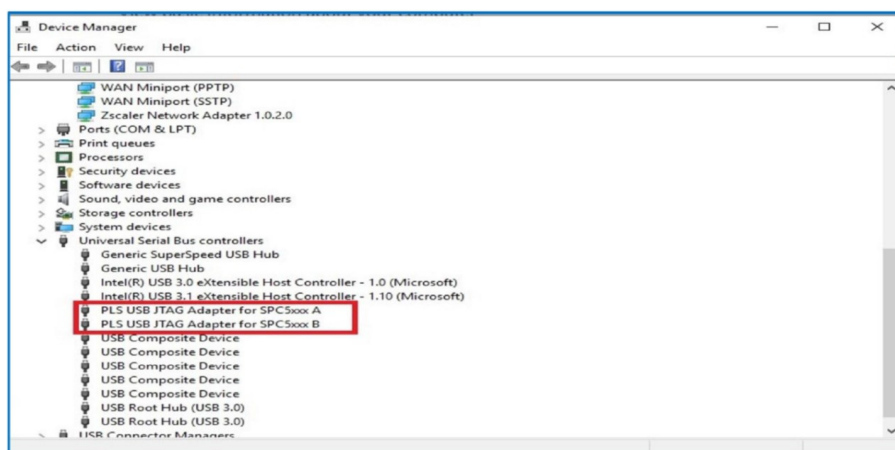
To program the control firmware in the [EV-SPC582B](#) MCU board, if needed, the **UDE Starterkit 2021** application must be installed on your PC workstation.

#### PLS UDE Starterkit 2021

Run the **udestk-2021-05-spc5-stk.exe** utility and follow the installation wizard. As a final step of the installation process, UDE STK driver is also installed.

After driver installation is finished, connect the USB cable to the [EV-SPC582B](#) and open the **Device Manager** in Windows OS: these two PLS controllers must have been recognized if everything went well.

Figure 3. Universal Serial Bus controllers

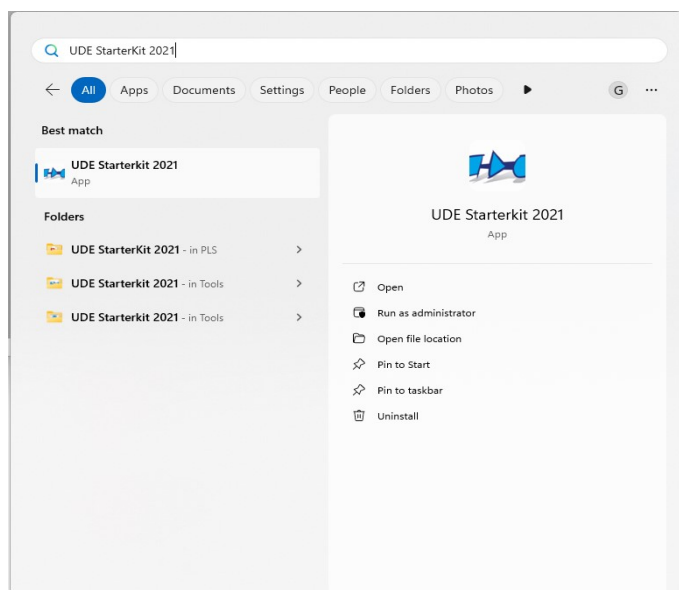


## 2.2 Firmware programming

The steps required to perform the firmware programming operation on the microcontroller board are detailed below.

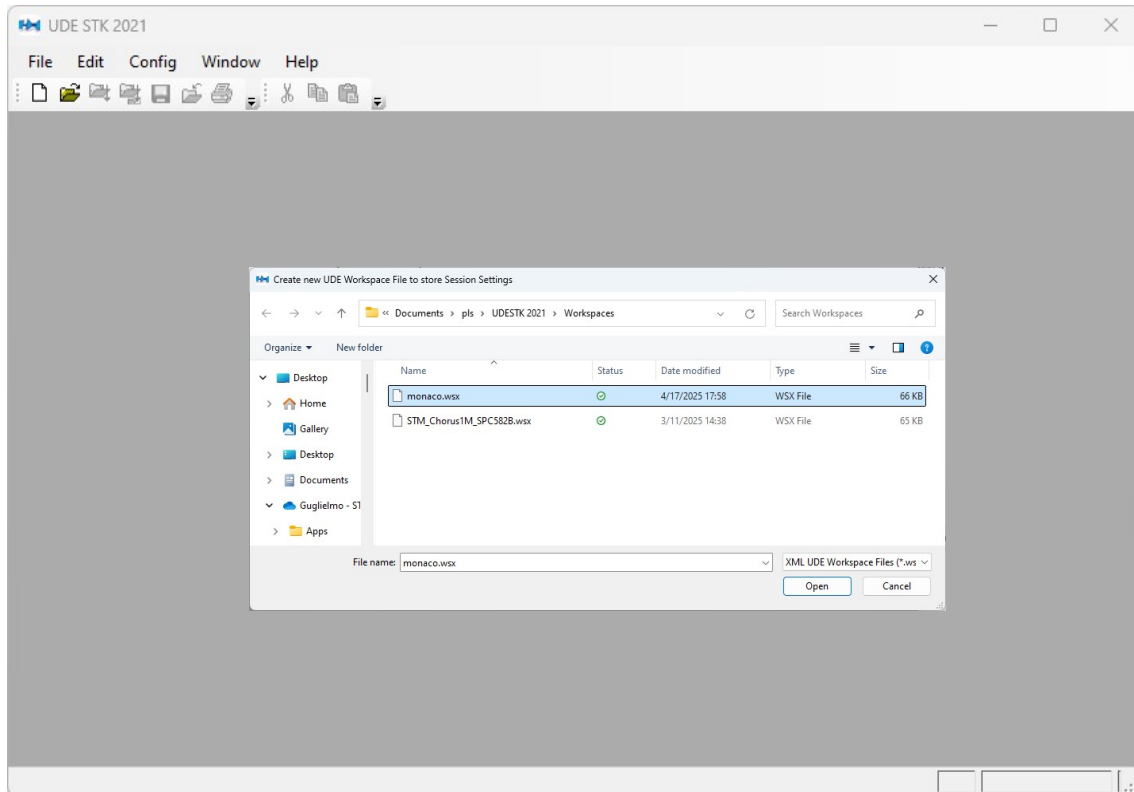
1. Setup the **EV-SPC582B** MCU board by putting jumpers on JP3 and JP4 on the right side (5 V) and connecting USB cable for board communication and programming.
2. Run **UDE Starterkit 2021** application on PC workstation

**Figure 4. UDE Starterkit 2021**



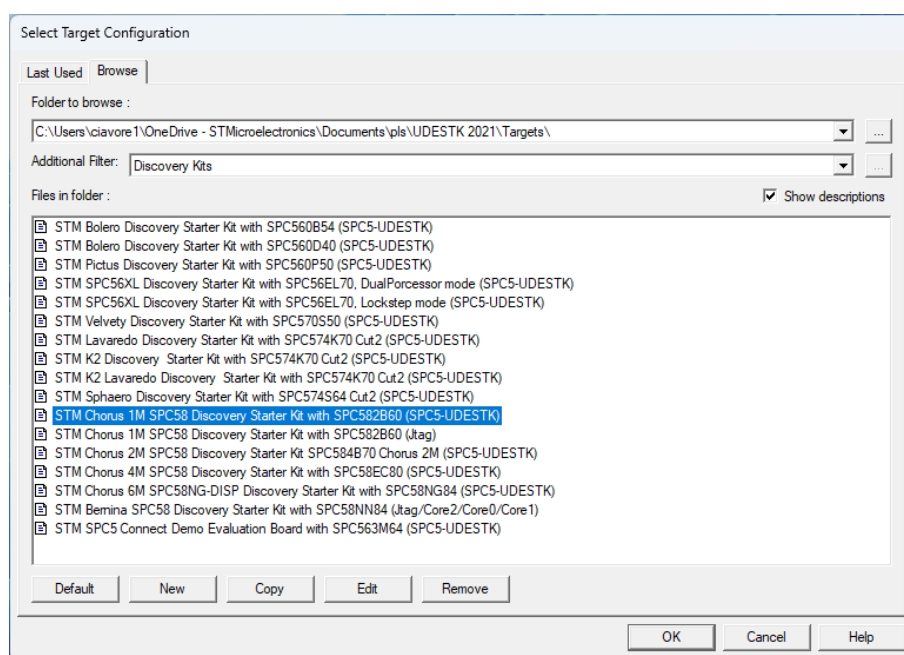
3. Select from **File** menu, the item **New Workspace**, and type a name for the workspace to be created, or overwritten if it already exists. In this example, the new workspace is named **monaco.wsx**

**Figure 5. New workspace creation**



4. **Select Target Configuration** window appears: set **Additional Filter: Discovery Kits**, and then click on **Default**.

**Figure 6. Select Target Configuration**



5. In the new dialog window, **Create or use default**, select **Use a default target configuration** and, in the Device tree dialog below, select in order:

**PowerPC**

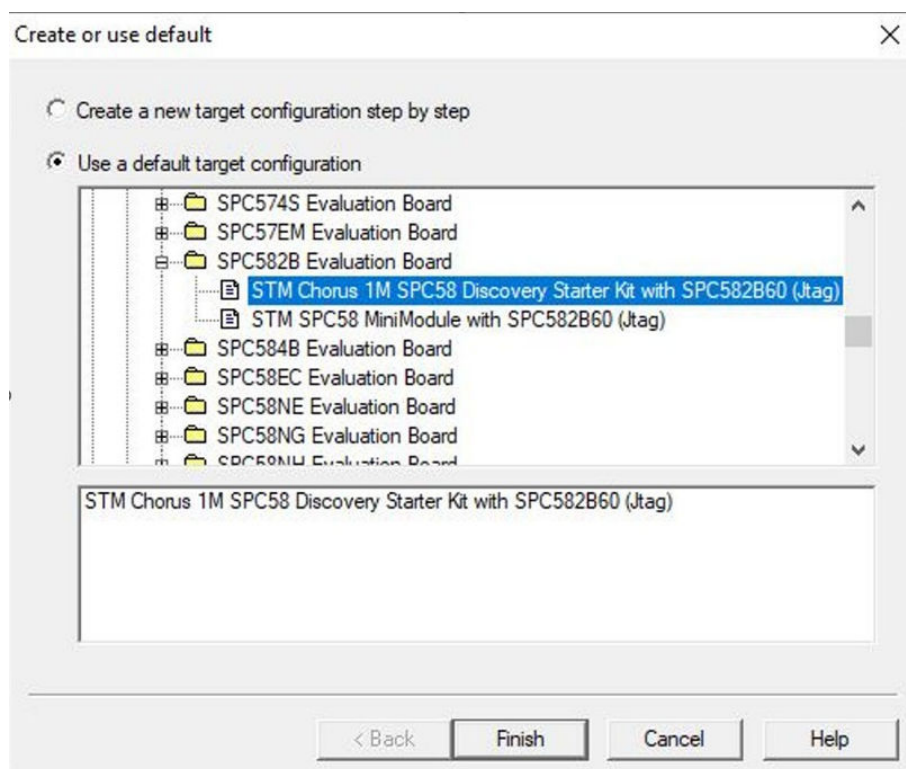
↳ **STM**

↳ **SPC582B Evaluation Board**

↳ **STM Chorus 1M SPC58 Discovery Starter Kit with SPC582B60 (Jtag)**

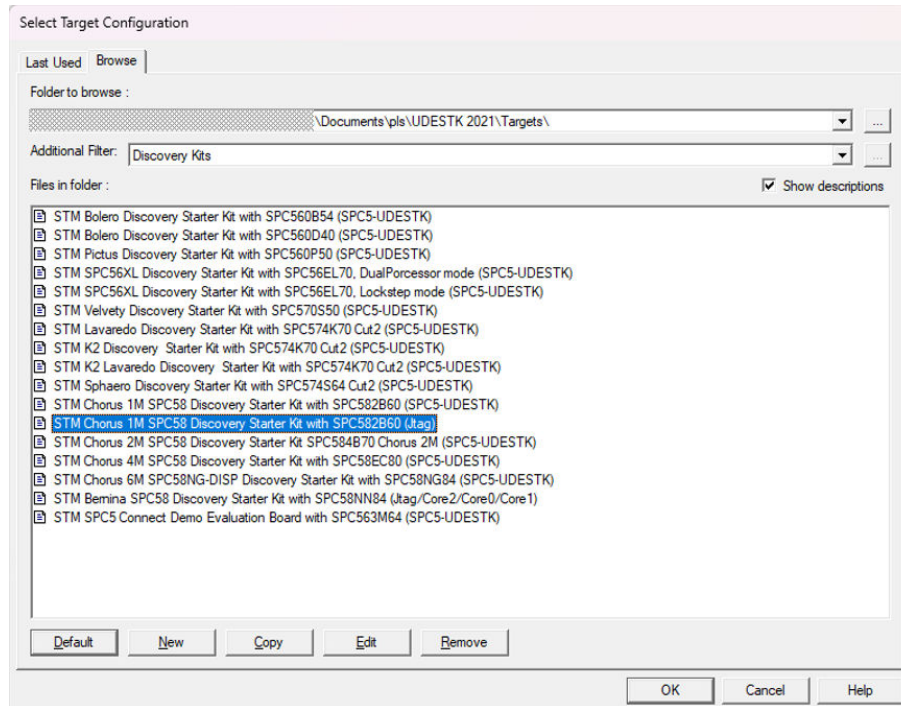
Press **Finish**: choose a name for this new configuration file

**Figure 7. Create or use default**



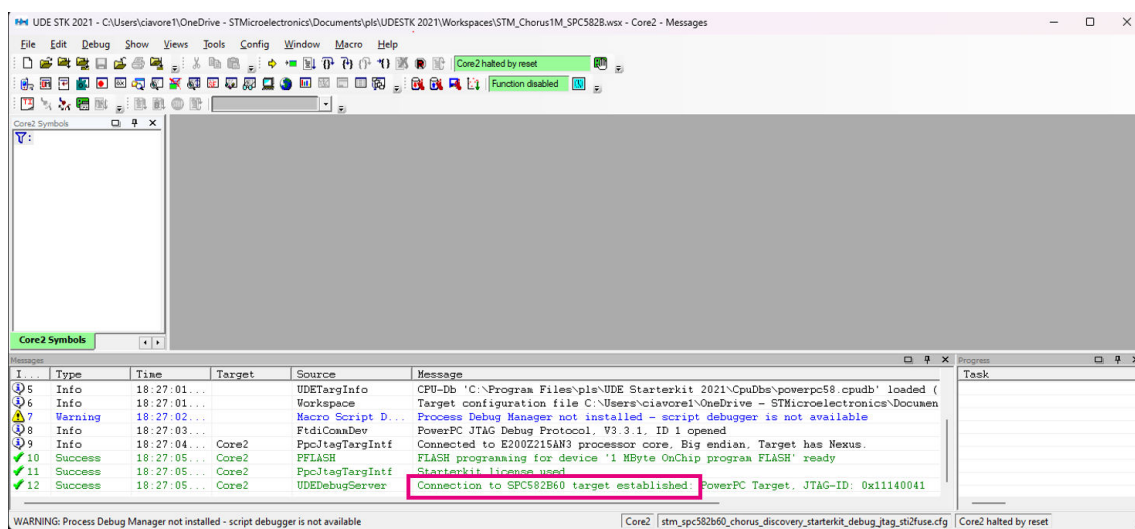
- Back in the **Select Target Configuration**, now select:  
**STM Chorus 1M SPC58 Discovery Starter Kit with SPC582B60 (Jtag)** and then press **OK**

Figure 8. Select Target Configuration dialog window



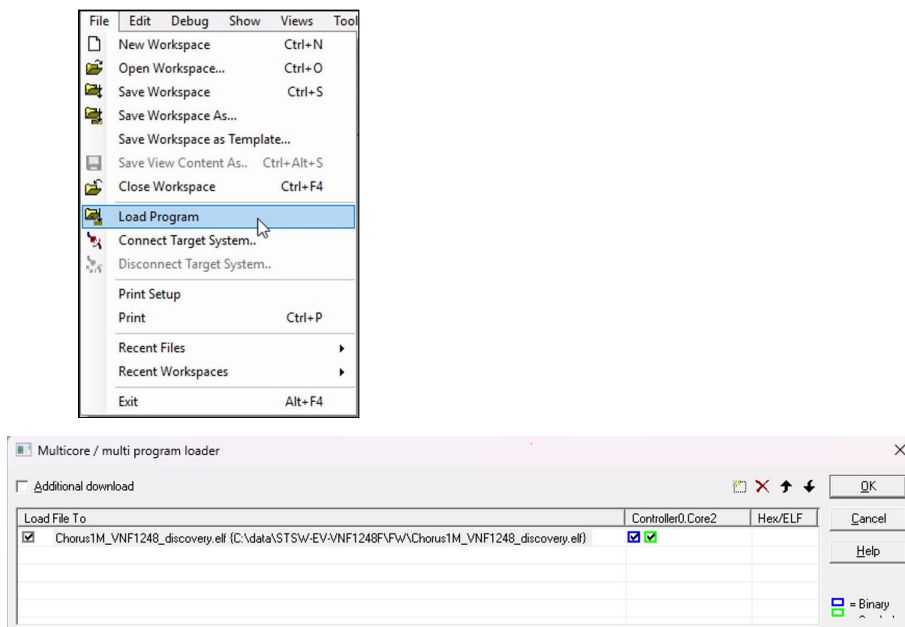
- In the **UDE STK 2021** window, verify that in the **Messages** window contains a line indicating that a successful connection to the target has been established:

Figure 9. Connection established



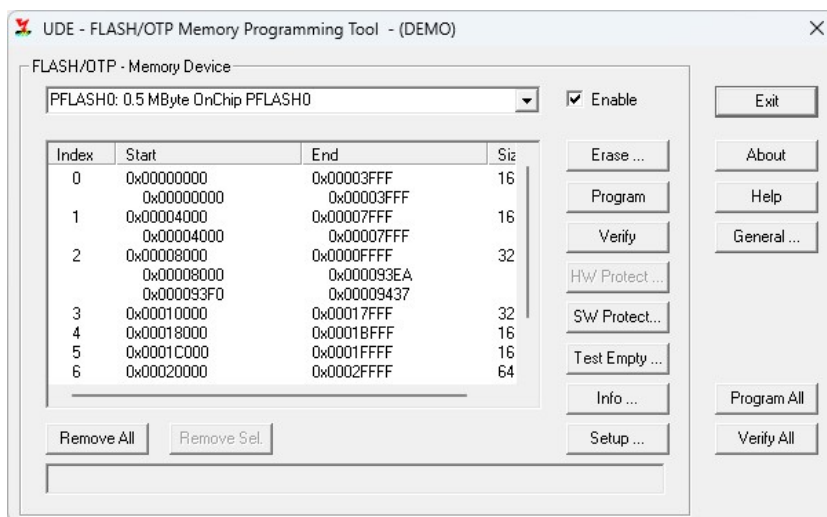
8. Select **Load Program** from **File** menu, browse your hard drive to select the provided control firmware (.elf file) and then press **OK** in the **Multicore / multi program loader** dialog window:

Figure 10. Load Program dialog windows



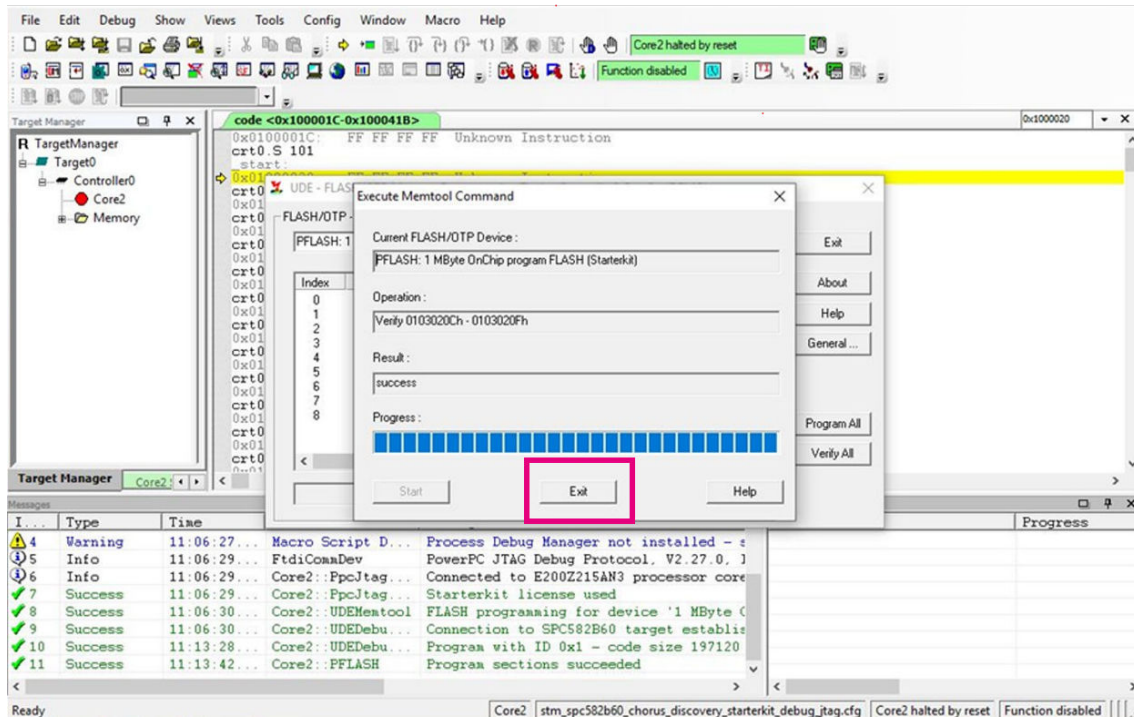
9. Press **Cancel** for any requests about Controller0.Core source files (.c or .h)
10. The **UDE - FLASH/OTP Memory Programming Tool - (DEMO)** window now appears. Press **Program All**:

Figure 11. FLASH/OTP Memory Programming Tool dialog window



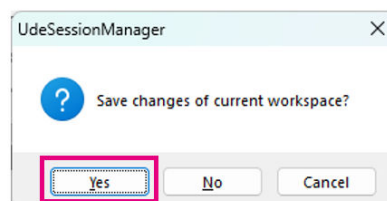
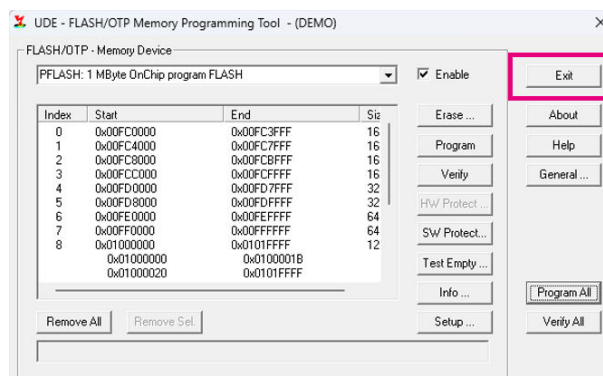
11. Follow the execution of programming operation through the **Execute Memtool Command** dialog window. At the end of the operation, check the **Result:** field reporting **success**, and then press **Exit**:

**Figure 12. FLASH/OTP Memory Programming**



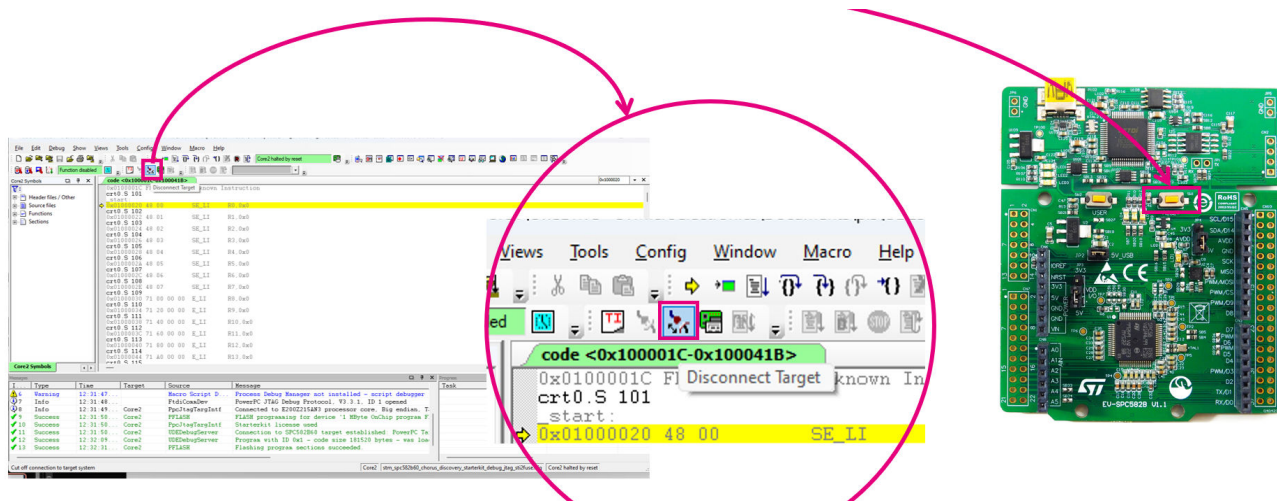
12. Press **Exit** also in the **UDE - FLASH/OTP Memory Programming Tool - (DEMO)** dialog window, and press **Yes**, if requested, to save workspace changes for future use:

**Figure 13. FLASH/OTP Memory Programming in progress**



13. To complete the firmware programming, simply disconnect the GUI from the target (see next figure) and reset it through the **RESET** push-button available on the **EV-SPC582B** microcontroller board:

**Figure 14. Target disconnected**



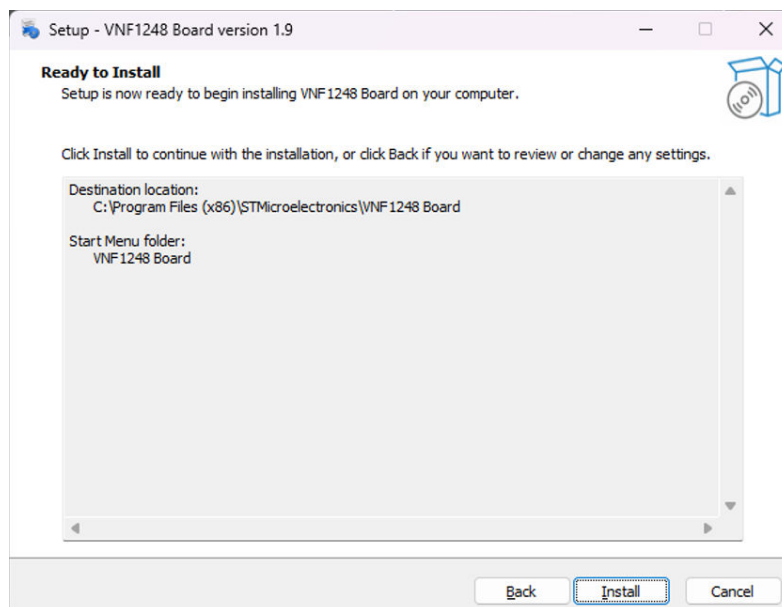
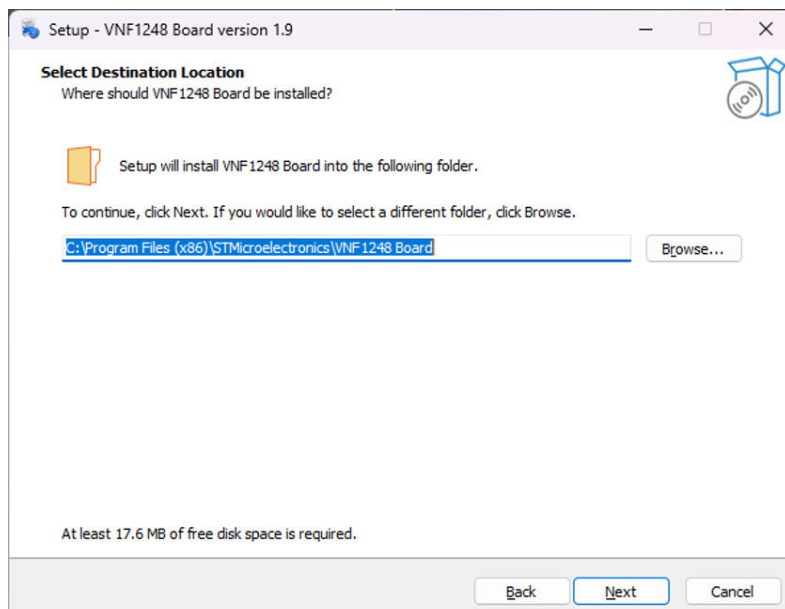
## 2.3 Graphical User Interface installation

To install the Graphical User Interface, the following steps must be executed.

1. Run the application provided in **STSW-EV-VNF1248F: Setup\_VNF1248\_vx.y.exe**

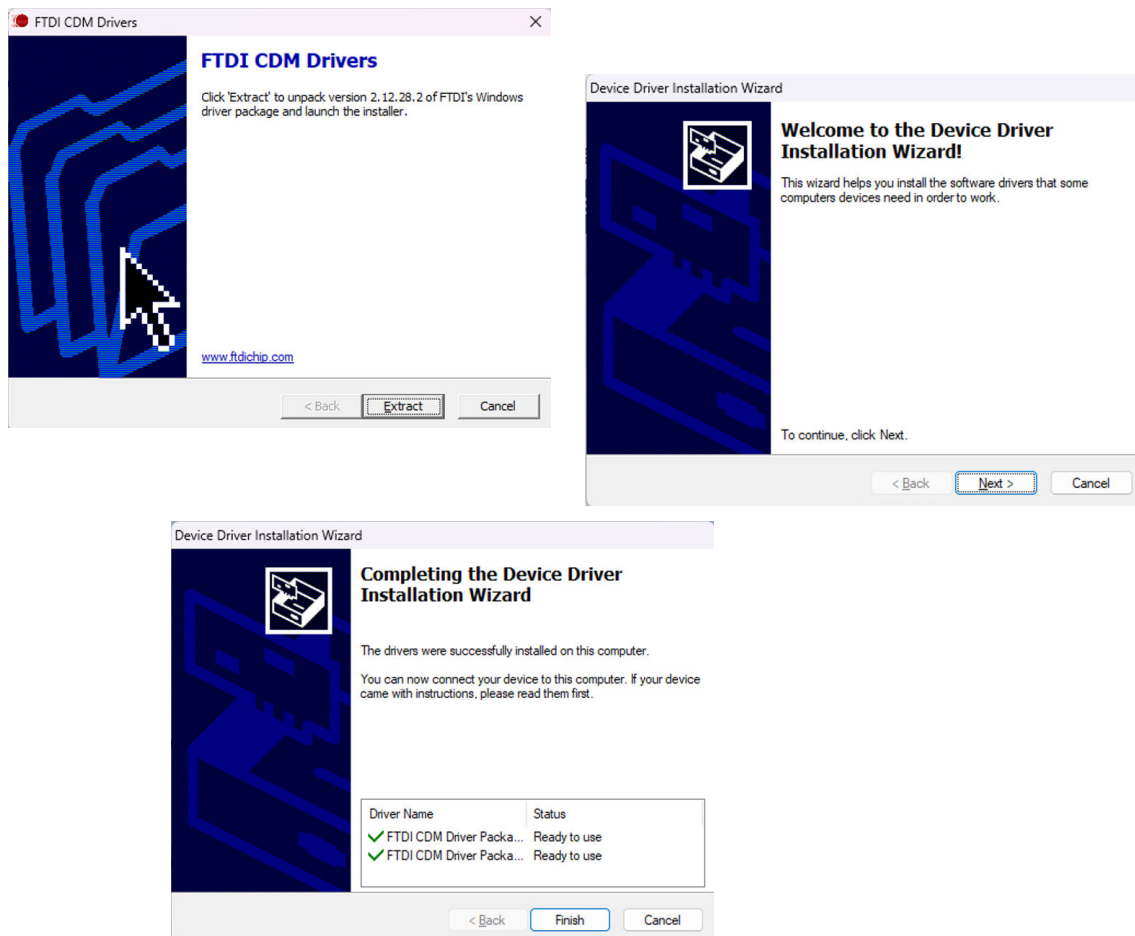
*Note: x.y is a generic version number, reported only as example*

Figure 15. Setup - VNF1248 Board



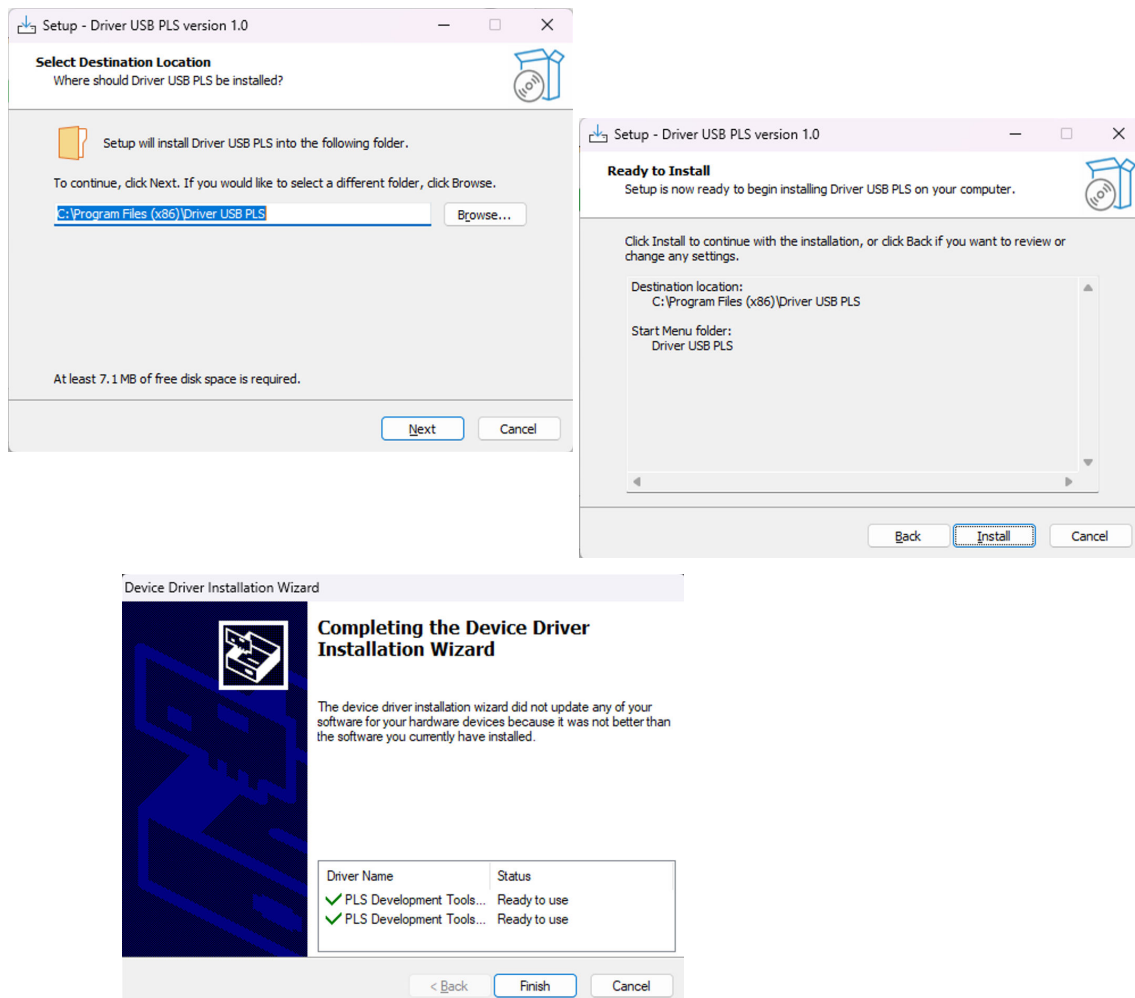
2. FTDI COM Drivers installation now starts:

Figure 16. FTDI COM Drivers



3. **USB PLS Drivers** will now be installed:

**Figure 17. Setup - USB PLS Drivers**



4. Press **Finish** to close the installation wizard, and launch **VNF1248 Evaluation board GUI** application.

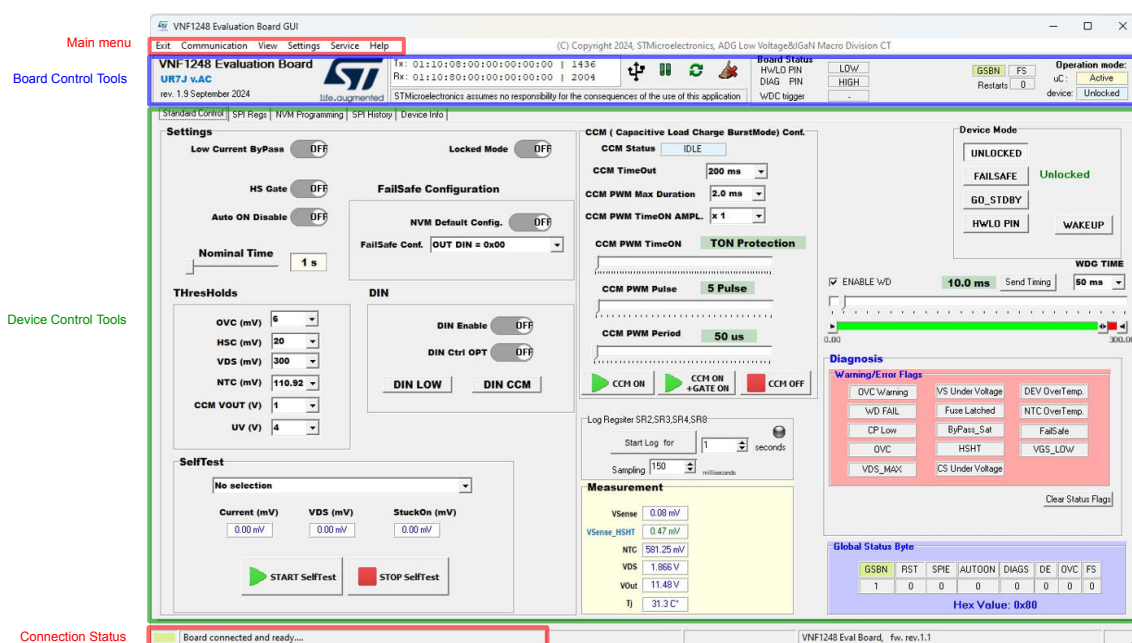
### 3 Graphical User Interface description

The Graphical User Interface included in the **STSW-EV-VNF1248F** software package is a powerful tool designed to setup and control the **VNF1248F** device embedded in the **EV-VNF1248F** evaluation board.

Launch the **VNF1248 Board** application, or run the **VNF1248\_EvalBoard.exe** related executable, to start the GUI.

The Graphical User Interface is composed by some sections that will be detailed in the next paragraphs. Below is an overview of the GUI graphic.

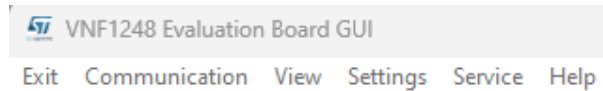
Figure 18. GUI sections



### 3.1 Main menu

The Graphical User Interface includes a command menu that allows you to perform some application settings, access support services, execute Windows OS operations, and visualize device data. Main menu items are described below in more details.

Figure 19. Main menu

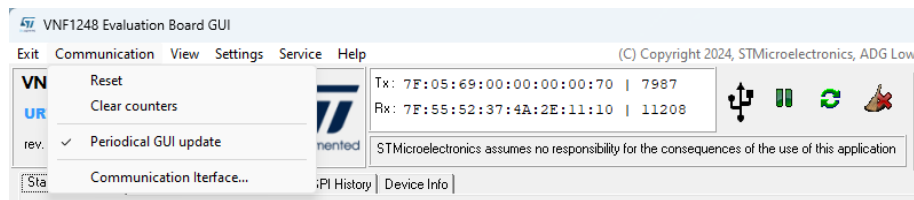


#### Exit

It simply closes the application

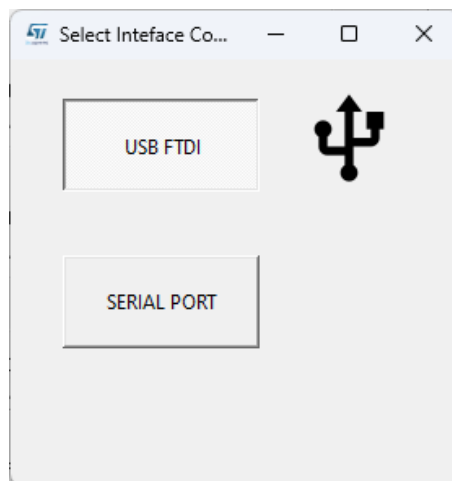
#### Communication

Figure 20. Communication



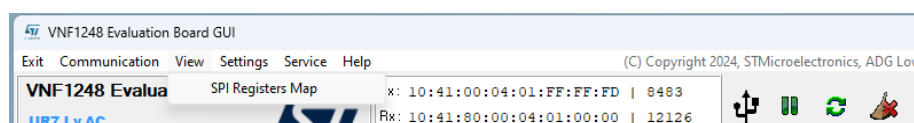
The proposed menu items allows you to reset communication traffic, clear all related counters, refresh the GUI periodically, and, most importantly, select the type of interface for the specific hardware connected. You can choose between a USB FTDI interface and a serial interface.

Figure 21. Communication Interface selection



#### View

Figure 22. View



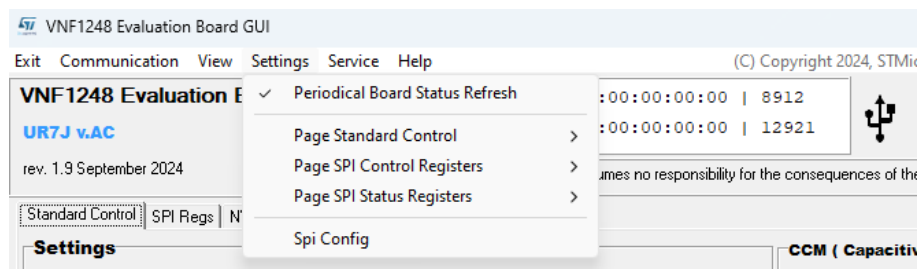
The SPI register map can be shown:

Figure 23. SPI Registers Overview

| SPI Registers Overview |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |
|------------------------|------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------|
| Adr: 0x01              | CR 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 04 01 |
| Adr: 0x02              | CR 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 00 00 |
| Adr: 0x03              | CR 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 00 00 |
| Adr: 0x04              | CR 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 00 00 |
| Adr: 0x05              | CR 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 00 00 |
| Adr: 0x11              | SR1  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 00 00 |
| Adr: 0x12              | SR2  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0x00 00 03 |
| Adr: 0x13              | SR3  | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0x2C 97 EE |
| Adr: 0x14              | SR4  | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0x7F B5 B2 |
| Adr: 0x15              | SR5  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 00 00 |
| Adr: 0x16              | SR6  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 00 00 |
| Adr: 0x17              | SR7  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 00 00 |
| Adr: 0x18              | SR8  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0x00 60 0A |

## Settings

Figure 24. Settings

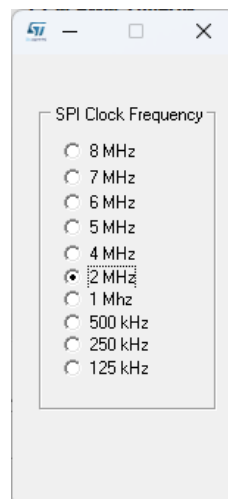


To configure periodical refresh of registers is allowed here.

Specific menu items are available to periodically:

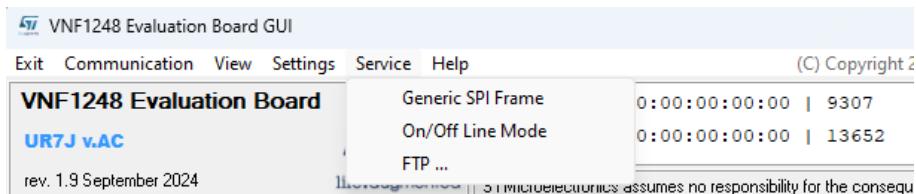
- refresh board status
- refresh and/or clear SPI Status Regs
- refresh SPI Control Regs
- config SPI Clock Frequency

Figure 25. SPI Clock Frequency



## Service

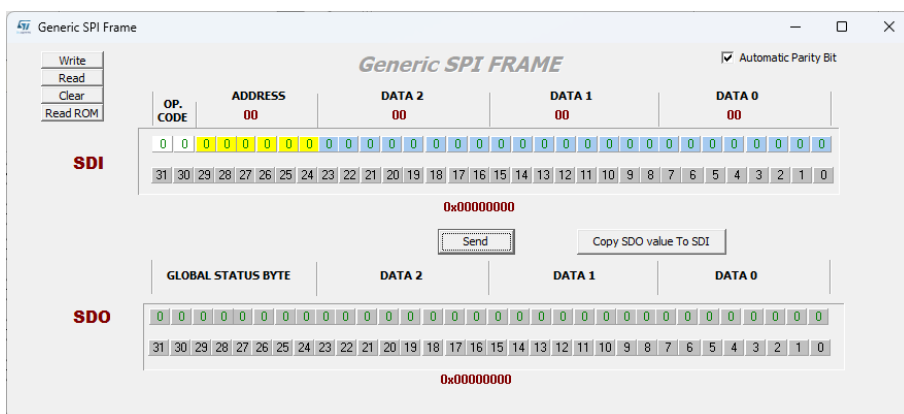
Figure 26. Service



Some services are available:

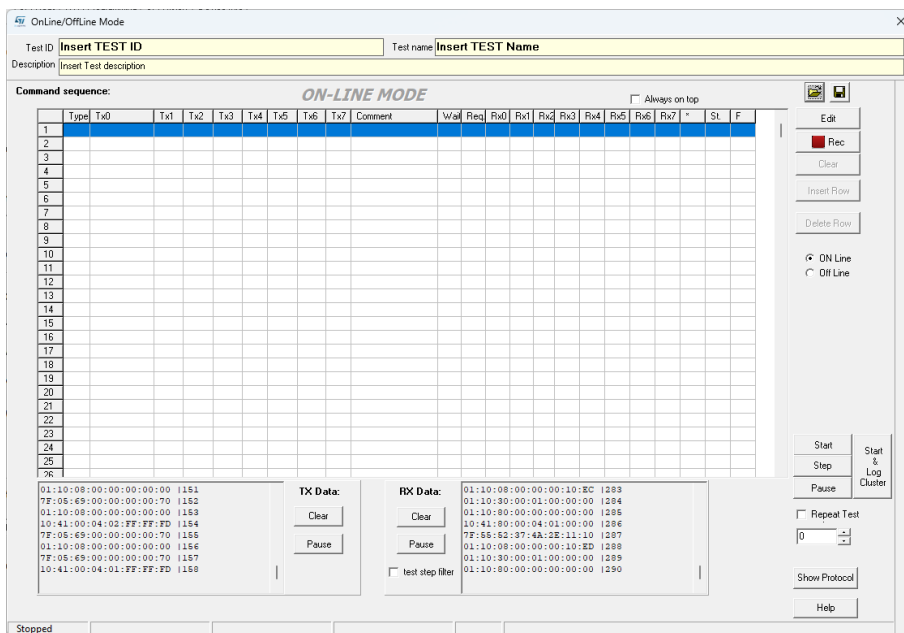
- **Generic SPI Frame** allows to send a customizable SPI frame to the VNF1248F device and to read its answer:

Figure 27. Generic SPI Frame



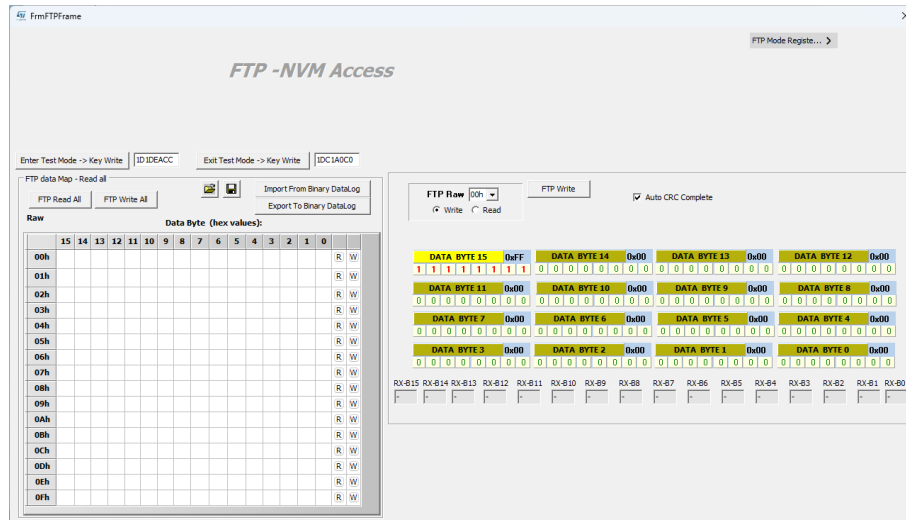
- **On/Off Line Mode** provides a powerful test and debug utility:

Figure 28. On/Off Line Mode



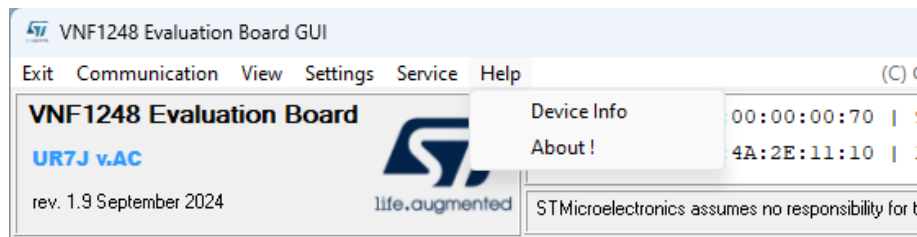
- **FTP** menu item is related to the Few Times Programmable feature of the embedded non-volatile memory, and specifically to customer sector program/erase/read operations:

Figure 29. FTP



Help

Figure 30. Help



## 3.2 Board control tools

The Graphical User Interface shows, under the main menu area, a graphical section that reports details about the GUI version, the [VNF1248F](#) device silicon cut, the communication traffic with the [EV-VNF1248F](#) evaluation board, some buttons with shortcuts to common actions, and the [EV-VNF1248F](#) board status.

Figure 31. Board Control Tools

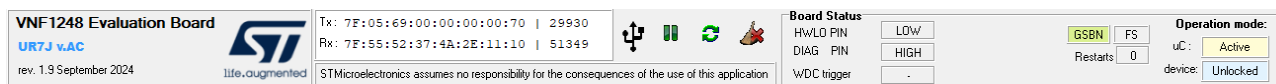
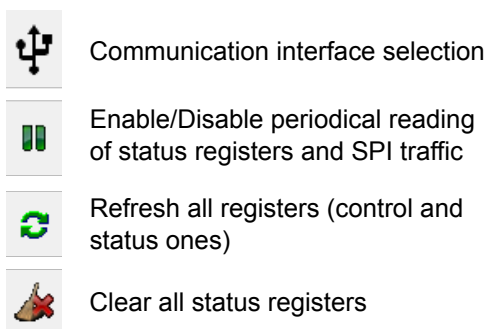


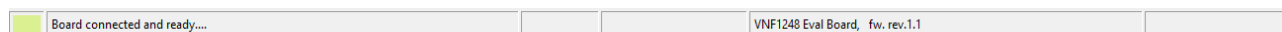
Figure 32. Common actions



### 3.3 Connection status

At the bottom of the Graphical User Interface, a Connection Status strip is presented. The normal application operation (communication between MCU board and GUI correctly established) is reported below. In case of missing communication, a red flag is shown in place of the green one here reported, and an error message is displayed.

**Figure 33. Connection status**



## 3.4 Device control tools

The most part of the Graphical User Interface is used for the pages dedicated to setup and control the [VNF1248F](#) device and its various features accessible through the [EV-VNF1248F](#) evaluation board. The pages are accessible from the tabs available on top of the section.

### 3.4.1 Standard Control

The main tab in the Graphical User Interface gives access to the main [VNF1248F](#) device features:

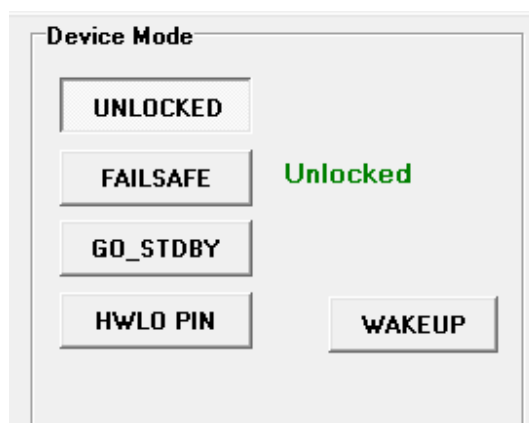
- Different device modes
- Device settings
- Different thresholds
- Perform self-test
- Log register data
- Perform measurements
- Configure CCM, DIN, Fail-safe features
- Retrieve diagnostic flags and Global Status data

#### Device Mode

All the device modes can be set by pressing the proper button.

**HWLO PIN** button enables/disables device HWLO pin.

Figure 34. Device Mode



#### Settings

General settings for [VNF1248F](#) device are available:

- **Low Current ByPass:** enables/disables the embedded P-channel Bypass, setting/resetting bit 3 of the Control Registers 1
- **HS Gate:** enables/disables the external MOSFET (and consequently turns ON/OFF the OUT line), setting/resetting bit 4 of Control Register 1
- **Auto ON Disable:** disables the automatic ON state of the external MOSFET in case of Low current bypass switch saturation fault, forced through HS\_GATE output, setting bit 23 of Control Register 1
- **Nominal Time:** Configures the fuse nominal time, setting bits from 23 to 16 of Control Register 2

Figure 35. Settings

### THresHolds

Several thresholds can be configured:

- **OVC (mV)**: Configures the value of Nominal Overcurrent Threshold, setting bits from 15 to 11 of Control Register 2
- **HSC (mV)**: Configures the threshold for Hard Short Circuit Latch-off, setting bits from 10 to 7 of Control Register 2
- **VDS (mV)**: Configures the threshold for External MOSFET desaturation shut-down, setting bits from 6 to 2 of Control Register 2
- **NTC (mV)**: Configures the threshold for External MOSFET overtemperature shutdown via NTC, setting bits from 8 to 5 of Control Register 3
- **CCM VOUT (V)**: Configures capacitive charge mode VOUT threshold, setting bits from 16 to 14 of Control Register 3
- **UV (V)**: Configures VS supply undervoltage threshold, setting bits from 11 to 10 of Control Register 3

### SelfTest

This section allows to select the Self-test to be executed (setting bits from 7 to 5 of Control Register 1) and to start and stop the test (setting bit 9 and bit 8 of Control Register 1).

A feedback on test result is also shown (value of Status register 5, 6, 7).

## FailSafe Configuration

This section allows to configure the Fail-safe state behavior (setting bits from 15 to 14 of Control Register 1).

### DIN

DIN can be used to enable capacitive charging mode functionality when device is in fail-safe state. DIN control enable can be accessed with setting bit 12 of Control Register 1 and its behavior configured setting bit 13 of Control Register 1.

## Capacitive Charging Mode

Digital logic implements a PWM-based control of high-side driver to allow charging a capacitive load through the off-chip Power MOSFET driven by the device.

The CCM section of the GUI allows to fully configure (some features are NVM mapped, other selectable through Control Register 5 bits), start (bit 18 Control Register 1) and stop (bit 19 Control Register 1) this feature.

Figure 36. CCM

**CCM (Capacitive Load Charge BurstMode) Conf.**

CCM Status: IDLE

CCM TimeOut: 200 ms

CCM PWM Max Duration: 2.0 ms

CCM PWM TimeON AMPL.: x 1

CCM PWM TimeON: TON Protection

CCM PWM Pulse: 5 Pulse

CCM PWM Period: 50 us

CCM ON CCM ON + GATE ON CCM OFF

## Log Register data

A set of Status Registers can be periodically read from device according to the duration and sampling rate selected.

Figure 37. Log Registers

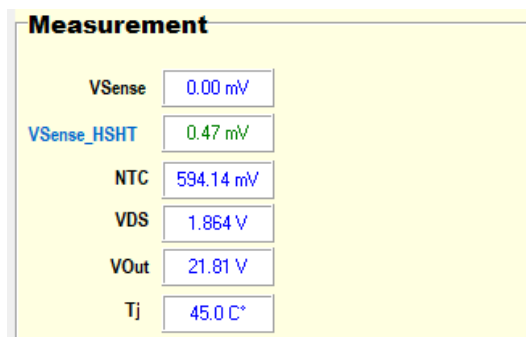
Log Register SR2,SR3,SR4,SR8

Start Log for: 1 seconds

Sampling: 150 milliseconds

## Measurement

Figure 38. Measurement

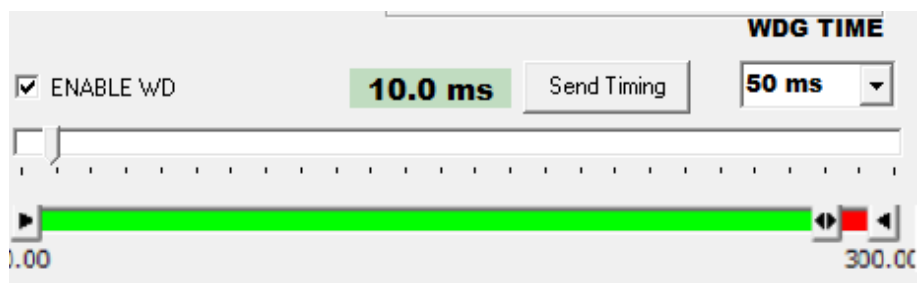


This section gives an overview about the following status registers:

- **VSense**: bits from 14 to 2 of Status Register 2
- **Vsense\_HSHT**: bits from 11 to 2 of Status Register 8
- **NTC**: bits from 11 to 2 of Status Register 3
- **VDS**: bits from 22 to 13 of Status Register 4
- **VOut**: bits from 11 to 2 of Status Register 4
- **Tj**: bits from 22 to 13 of Status Register 3

## Watchdog

Figure 39. Watchdog



WD serving is applied by refreshing the WD\_TRIG bit in one of the control registers.

**Enabled WD**: enables/disables WD serving by refreshing the WD\_TRIG bit

Period for Watchdog (WD) serving is adjustable by item **WDG TIME**.

There is also the possibility of setting the **WD refresh time** sent by MCU through a dedicated bar and button **Send Timing**. This allows to test the device WD timeout failure.

## Diagnostics

Diagnostic data is refreshed according to the device mode selected.

**Clear Status Flags** button allows to clear the error bits in the related status register.

The **Global Status Byte** is also presented.

Figure 40. Diagnostics

### Diagnosis

#### Warning/Error Flags

|             |                  |               |
|-------------|------------------|---------------|
| OVC Warning | VS Under Voltage | DEV OverTemp. |
| WD FAIL     | Fuse Latched     | NTC OverTemp. |
| CP Low      | ByPass_Sat       | FailSafe      |
| OVC         | HSHT             | VGS_LOW       |
| VDS_MAX     | CS Under Voltage |               |

Clear Status Flags

#### Global Status Byte

| GSRN | RST | SPIE | AUTOON | DIAGS | DE | OVC | FS |
|------|-----|------|--------|-------|----|-----|----|
| 1    | 0   | 0    | 0      | 0     | 0  | 0   | 0  |

Hex Value: 0x80

### 3.4.2 SPI Regs

The Graphical User Interface in this form shows the content of all SPI Registers: Control Registers 1-5 and Status Registers 1-8.

Each register has its own set of applicable actions.

The possible actions for the RAM registers are the following:

- Button **R**: read register content from the device
- Button **W**: store current content of the selected register to the device
- Button **C**: read and clear action on selected register

Register bits that can be modified are available for editing.

The Graphical User Interface provides side-by-side access to all the SPI Control Registers and SPI Status Registers of [VNF1248F](#) device in this form.

*Note: For Ctrl Reg4 both Function 1 and Function 2 register bits are shown. For more detailed description of all SPI registers refer to the device datasheet ([DS14109](#))*

Figure 41. SPI Control Registers

VNF1248 Evaluation Board GUI

Exit Communication View Settings Service Help (C) Copyright 2024, STMicroelectronics, ADG Low Voltage&I/GaN Macro Division CT

**VNF1248 Evaluation Board**  
UR7J v.AC  
rev. 1.9 September 2024

Tx: 10:58:00:00:00:00:00:00 | 21340  
Rx: 10:58:80:00:60:0A:00:00 | 34702

STMicroelectronics assumes no responsibility for the consequences of the use of this application

Standard Control **SPI Regs** NVM Programming SPI History Device Info

| Ctrl Reg1 |                |   |   | Ctrl Reg2 |            |   |   | Ctrl Reg3 |              |   |   | Ctrl Reg4 |              |   |   | Ctrl Reg4 |              |   |   | Ctrl Reg5 |              |   |   |
|-----------|----------------|---|---|-----------|------------|---|---|-----------|--------------|---|---|-----------|--------------|---|---|-----------|--------------|---|---|-----------|--------------|---|---|
| Addr.     | 0x01           | W | R | Addr.     | 0x02       | W | R | Addr.     | 0x03         | W | R | Addr.     | 0x04         | W | R | Addr.     | 0x04         | W | R | Addr.     | 0x05         | W | R |
| 23        | AUTO_ON_DIS    | 0 |   | 23        | T_NOM7     | 0 |   | 23        | -            | 0 |   | 23        | _CTM_ACCESS_ | 0 |   | 23        | -            | 0 |   | 23        | CCM_TIMEOUT1 | 0 |   |
| 22        | -              | 0 |   | 22        | T_NOM6     | 0 |   | 22        | -            | 0 |   | 22        | _CTM_ACCESS_ | 0 |   | 22        | -            | 0 |   | 22        | CCM_TIMEOUT0 | 0 |   |
| 21        | -              | 0 |   | 21        | T_NOM5     | 0 |   | 21        | -            | 0 |   | 21        | _CTM_ACCESS_ | 0 |   | 21        | -            | 0 |   | 21        | CM_PWM_SC_TN | 0 |   |
| 20        | LOCKED_MODE_EN | 0 |   | 20        | T_NOM4     | 0 |   | 20        | -            | 0 |   | 20        | _CTM_ACCESS_ | 0 |   | 20        | -            | 0 |   | 20        | CM_PWM_SC_TN | 0 |   |
| 19        | CCM_CTRL_OFF   | 0 |   | 19        | T_NOM3     | 0 |   | 19        | CCM_PWM_TON  | 0 |   | 19        | _CTM_ACCESS_ | 0 |   | 19        | -            | 0 |   | 19        | CM_PWM_SC_TN | 0 |   |
| 18        | CCM_CTRL_ON    | 0 |   | 18        | T_NOM2     | 0 |   | 18        | CCM_PWM_TON  | 0 |   | 18        | _CTM_ACCESS_ | 0 |   | 18        | -            | 0 |   | 18        | CM_PWM_SC_TN | 0 |   |
| 17        | NVM_DEF_UPLOAD | 0 |   | 17        | T_NOM1     | 0 |   | 17        | -            | 0 |   | 17        | _CTM_ACCESS_ | 0 |   | 17        | -            | 0 |   | 17        | CM_PWM_SC_TN | 0 |   |
| 16        | NVM_DEF_CFGEN  | 0 |   | 16        | T_NOM0     | 0 |   | 16        | CCM_VOUTTHR2 | 0 |   | 16        | _CTM_ACCESS_ | 0 |   | 16        | -            | 0 |   | 16        | CCM_PWM_SC_T | 0 |   |
| 15        | FS_MODE1       | 0 |   | 15        | OVC_THR4   | 0 |   | 15        | CCM_VOUTTHR  | 0 |   | 15        | _CTM_ACCESS_ | 0 |   | 15        | -            | 0 |   | 15        | CCM_PWM_SC_T | 0 |   |
| 14        | FS_MODE0       | 0 |   | 14        | OVC_THR3   | 0 |   | 14        | CCM_VOUTTHR  | 0 |   | 14        | _CTM_ACCESS_ | 0 |   | 14        | -            | 0 |   | 14        | CCM_PWM_SC_T | 0 |   |
| 13        | DIN_CTRL_OPT   | 0 |   | 13        | OVC_THR2   | 0 |   | 13        | -            | 0 |   | 13        | _CTM_ACCESS_ | 0 |   | 13        | -            | 0 |   | 13        | CCM_PWM_TON  | 0 |   |
| 12        | DIN_CTRL_EN    | 0 |   | 12        | OVC_THR1   | 0 |   | 12        | -            | 0 |   | 12        | _CTM_ACCESS_ | 0 |   | 12        | -            | 0 |   | 12        | CCM_PWM_TON  | 0 |   |
| 11        | GOSTBY         | 0 |   | 11        | OVC_THR0   | 0 |   | 11        | UV_THR1      | 0 |   | 11        | _CTM_ACCESS_ | 0 |   | 11        | NVM_ADDR3    | 0 |   | 11        | CCM_PWM_TON  | 0 |   |
| 10        | EN             | 1 |   | 10        | HSHT_THR3  | 0 |   | 10        | UV_THR0      | 0 |   | 10        | _CTM_ACCESS_ | 0 |   | 10        | NVM_ADDR2    | 0 |   | 10        | CCM_PWM_TON  | 0 |   |
| 9         | S_T_START      | 0 |   | 9         | HSHT_THR2  | 0 |   | 9         | UNLOCK       | 0 |   | 9         | _CTM_ACCESS_ | 0 |   | 9         | NVM_ADDR1    | 0 |   | 9         | CCM_PWM_TON  | 0 |   |
| 8         | S_T_STOP       | 0 |   | 8         | HSHT_THR1  | 0 |   | 8         | NTC_THR3     | 0 |   | 8         | _CTM_ACCESS_ | 0 |   | 8         | NVM_ADDR0    | 0 |   | 8         | CCM_PWM_TON  | 0 |   |
| 7         | S_T_CFG2       | 0 |   | 7         | HSHT_THR0  | 0 |   | 7         | NTC_THR2     | 0 |   | 7         | _CTM_ACCESS_ | 0 |   | 7         | -            | 0 |   | 7         | CCM_PWM_T5   | 0 |   |
| 6         | S_T_CFG1       | 0 |   | 6         | VDS_THR4   | 0 |   | 6         | NTC_THR1     | 0 |   | 6         | _CTM_ACCESS_ | 0 |   | 6         | -            | 0 |   | 6         | CCM_PWM_T4   | 0 |   |
| 5         | S_T_CFG0       | 0 |   | 5         | VDS_THR3   | 0 |   | 5         | NTC_THR0     | 0 |   | 5         | _CTM_ACCESS_ | 0 |   | 5         | -            | 0 |   | 5         | CCM_PWM_T3   | 0 |   |
| 4         | OUTCTL         | 0 |   | 4         | VDS_THR2   | 0 |   | 4         | WD_TIME1     | 0 |   | 4         | _CTM_ACCESS_ | 0 |   | 4         | -            | 0 |   | 4         | CCM_PWM_T2   | 0 |   |
| 3         | BYPASSCTL      | 0 |   | 3         | VDS_THR1   | 0 |   | 3         | WD_TIME0     | 0 |   | 3         | _CTM_ACCESS_ | 0 |   | 3         | NVM_WR_EN    | 0 |   | 3         | CCM_PWM_T1   | 0 |   |
| 2         | -              | 0 |   | 2         | VDS_THR0   | 0 |   | 2         | -            | 0 |   | 2         | _CTM_ACCESS_ | 0 |   | 2         | NVM_OP_START | 0 |   | 2         | CCM_PWM_T0   | 0 |   |
| 1         | WD_TRIG        | 0 |   | 1         | WD_TRIG    | 0 |   | 1         | WD_TRIG      | 0 |   | 1         | WD_TRIG      | 0 |   | 1         | WD_TRIG      | 0 |   | 1         | WD_TRIG      | 0 |   |
| 0         | PARITY BIT     | 1 |   | 0         | PARITY BIT | 0 |   | 0         | PARITY BIT   | 0 |   | 0         | PARITY BIT   | 0 |   | 0         | PARITY BIT   | 0 |   | 0         | PARITY BIT   | 0 |   |

0x000401 0x000000 0x000000 0x000000 0x000000 0x000000

Board connected and ready.... VNF1248 Eval Board, fw. rev.1.1

(United States) Accessibility: Investigate

Figure 42. SPI Status Registers

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Tx: 10:58:00:00:00:00:00 | 22989  
Rx: 10:58:80:00:60:0A:00:00 | 36855

Board Status  
HWLO PIN: LOW  
DIAG PIN: HIGH  
WDC trigger: -

Operation mode:  
uC: Active  
device: Unlocked

PI History | Device Info

| Status Reg1 |              |     | Status Reg2 |            |     | Status Reg3 |            |     | Status Reg4 |            |     | Status Reg5 |             |     | Status Reg6 |               |     | Status Reg7 |             |     | Status Reg8 |              |     |
|-------------|--------------|-----|-------------|------------|-----|-------------|------------|-----|-------------|------------|-----|-------------|-------------|-----|-------------|---------------|-----|-------------|-------------|-----|-------------|--------------|-----|
| Addr.       | 0x11         | C R | Addr.       | 0x12       | C R | Addr.       | 0x13       | C R | Addr.       | 0x14       | C R | Addr.       | 0x15        | C R | Addr.       | 0x16          | C R | Addr.       | 0x17        | C R | Addr.       | 0x18         | C R |
| 23          | CCM_STATUS1  | 0   | 23          | -          | 0   | 23          | -          | 0   | 23          | -          | 0   | 23          | -           | 0   | 23          | -             | 0   | 23          | -           | 0   | 23          | -            | 0   |
| 22          | CCM_STATUS0  | 0   | 22          | NVM_FAIL5  | 0   | 22          | TJ9        | 0   | 22          | VDS9       | 1   | 22          | -           | 0   | 22          | -             | 0   | 22          | -           | 0   | 22          | -            | 0   |
| 21          | CS_UV        | 0   | 21          | NVM_FAIL4  | 0   | 21          | TJ8        | 1   | 21          | VDS8       | 1   | 21          | -           | 0   | 21          | -             | 0   | 21          | -           | 0   | 21          | NVM_PROG_CNT | 0   |
| 20          | EXT_REG_ON   | 0   | 20          | NVM_FAIL3  | 0   | 20          | TJ7        | 0   | 20          | VDS7       | 1   | 20          | -           | 0   | 20          | -             | 0   | 20          | -           | 0   | 20          | NVM_PROG_CNT | 0   |
| 19          | DIN_ST       | 0   | 19          | NVM_FAIL2  | 0   | 19          | TJ6        | 1   | 19          | VDS6       | 1   | 19          | -           | 0   | 19          | -             | 0   | 19          | -           | 0   | 19          | NVM_PROG_CNT | 0   |
| 18          | DIS_OUT_FAIL | 0   | 18          | NVM_FAIL1  | 0   | 18          | TJ5        | 1   | 18          | VDS5       | 1   | 18          | -           | 0   | 18          | -             | 0   | 18          | -           | 0   | 18          | NVM_PROG_CNT | 0   |
| 17          | SELFTEST     | 0   | 17          | NVM_FAIL0  | 0   | 17          | TJ4        | 0   | 17          | VDS4       | 1   | 17          | -           | 0   | 17          | -             | 0   | 17          | -           | 0   | 17          | NVM_PROG_CNT | 0   |
| 16          | OUTST        | 0   | 16          | NVM_OP_ST1 | 0   | 16          | TJ3        | 0   | 16          | VDS3       | 1   | 16          | -           | 0   | 16          | -             | 0   | 16          | -           | 0   | 16          | NVM_PROG_CNT | 0   |
| 15          | BYPASSST     | 0   | 15          | NVM_OP_ST0 | 0   | 15          | TJ2        | 1   | 15          | VDS2       | 1   | 15          | -           | 0   | 15          | -             | 0   | 15          | -           | 0   | 15          | NVM_PROG_CNT | 0   |
| 14          | LOCKED_STATE | 0   | 14          | CURR_SNS12 | 0   | 14          | TJ1        | 1   | 14          | VDS1       | 0   | 14          | -           | 0   | 14          | JPDT_S_T_STUC | 0   | 14          | S_T_HSH     | 0   | 14          | NVM_PROG_CNT | 1   |
| 13          | FAILSAFE     | 0   | 13          | CURR_SNS11 | 0   | 13          | TJ0        | 1   | 13          | VDS0       | 1   | 13          | S_T_VDSMAX1 | 0   | 13          | S_T_VDSMAX2   | 0   | 13          | S_T_OVC     | 0   | 13          | NVM_PROG_CNT | 1   |
| 12          | HWLO_ST      | 0   | 12          | CURR_SNS10 | 0   | 12          | UPDT_TJ    | 1   | 12          | UPDT_VDS   | 1   | 12          | S_T_VDS9    | 0   | 12          | S_T_STUCK9    | 0   | 12          | S_T_CURR9   | 0   | 12          | NVM_PROG_CNT | 0   |
| 11          | VS_UV        | 0   | 11          | CURR_SNS9  | 0   | 11          | NTC9       | 0   | 11          | VOUT9      | 0   | 11          | S_T_VDS8    | 0   | 11          | S_T_STUCK8    | 0   | 11          | S_T_CURR8   | 0   | 11          | HSHT_SAR8    | 0   |
| 10          | HSHT         | 0   | 10          | CURR_SNS8  | 0   | 10          | NTC8       | 1   | 10          | VOUT8      | 1   | 10          | S_T_VDS7    | 0   | 10          | S_T_STUCK7    | 0   | 10          | S_T_CURR7   | 0   | 10          | HSHT_SAR7    | 0   |
| 9           | VDS_MAX      | 0   | 9           | CURR_SNS7  | 0   | 9           | NTC7       | 1   | 9           | VOUT7      | 0   | 9           | S_T_VDS6    | 0   | 9           | S_T_STUCK6    | 0   | 9           | S_T_CURR6   | 0   | 9           | HSHT_SAR6    | 0   |
| 8           | BYPASS_SAT   | 0   | 8           | CURR_SNS6  | 0   | 8           | NTC6       | 1   | 8           | VOUT6      | 1   | 8           | S_T_VDS5    | 0   | 8           | S_T_STUCK5    | 0   | 8           | S_T_CURR5   | 0   | 8           | HSHT_SAR5    | 0   |
| 7           | FUSE_LATCH   | 0   | 7           | CURR_SNS05 | 0   | 7           | NTC5       | 1   | 7           | VOUT5      | 1   | 7           | S_T_VDS4    | 0   | 7           | S_T_STUCK4    | 0   | 7           | S_T_CURR4   | 0   | 7           | HSHT_SAR4    | 0   |
| 6           | OVC          | 0   | 6           | CURR_SNS4  | 0   | 6           | NTC4       | 1   | 6           | VOUT4      | 0   | 6           | S_T_VDS3    | 0   | 6           | S_T_STUCK3    | 0   | 6           | S_T_CURR3   | 0   | 6           | HSHT_SAR3    | 0   |
| 5           | DEV_OVT      | 0   | 5           | CURR_SNS3  | 0   | 5           | NTC3       | 1   | 5           | VOUT3      | 1   | 5           | S_T_VDS2    | 0   | 5           | S_T_STUCK2    | 0   | 5           | S_T_CURR2   | 0   | 5           | HSHT_SAR2    | 0   |
| 4           | NTC_OVT      | 0   | 4           | CURR_SNS2  | 0   | 4           | NTC2       | 0   | 4           | VOUT2      | 1   | 4           | S_T_VDS1    | 0   | 4           | S_T_STUCK1    | 0   | 4           | S_T_CURR1   | 0   | 4           | HSHT_SAR1    | 1   |
| 3           | VGS_LOW      | 0   | 3           | CURR_SNS1  | 0   | 3           | NTC1       | 1   | 3           | VOUT1      | 0   | 3           | S_T_VDS0    | 0   | 3           | S_T_STUCK0    | 0   | 3           | S_T_CURR0   | 0   | 3           | HSHT_SAR0    | 0   |
| 2           | CP_LOW       | 0   | 2           | CURR_SNS0  | 0   | 2           | NTC0       | 1   | 2           | VOUT0      | 0   | 2           | S_T_VDSST1  | 0   | 2           | S_T_STUCKST1  | 0   | 2           | S_T_CURRST1 | 0   | 2           | HSHT_SAR0    | 0   |
| 1           | WID_FAIL     | 0   | 1           | UPDT_CURR  | 1   | 1           | UPDT_NTC   | 1   | 1           | UPDT_VOUT  | 1   | 1           | S_T_VDSST0  | 0   | 1           | S_T_STUCKST0  | 0   | 1           | S_T_CURRST0 | 0   | 1           | UPDT_HSHT    | 1   |
| 0           | PARITY BIT   | 0   | 0           | PARITY BIT | 1   | 0           | PARITY BIT | 0   | 0           | PARITY BIT | 0   | 0           | PARITY BIT  | 0   | 0           | PARITY BIT    | 0   | 0           | PARITY BIT  | 0   | 0           | PARITY BIT   | 0   |
| 0x000000    |              |     | 0x000003    |            |     | 0x2CF7EE    |            |     | 0x7FB5B2    |            |     | 0x000000    |             |     | 0x000000    |               |     | 0x000000    |             |     | 0x00600A    |              |     |

VNF1248 Eval Board - fw rev 1.1

### 3.4.3 NVM Programming

The control logic unit available in [VNF1248F](#) enables the user to program a portion of the embedded NVM memory. This allows testing and storing specific settings for key parameters to be used during operation. Specifically, one of the six available sectors (sector 5) can be written to or read by the customer after entering the proper command sequence. This sequence ensures a secure and safe access to the functionality, avoiding unexpected write operations that could corrupt NVM content.

More details about the non-volatile memory programming feature can be found in the device datasheet ([DS14109](#))

Below is the form provided in the Graphical User Interface to accomplish the NVM programming feature being reported.

Figure 43. NVM Programming

**VNF1248 Evaluation Board GUI**

Exit Communication View Settings Service Help

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**VNF1248 Evaluation Board**  
UR7J v.4C  
rev. 1.9 September 2024

Tx: 01:10:08:00:00:00:00 | 27748  
Rx: 01:10:80:00:00:00:00 | 43107

Board Status  
Hw/LD PIN: LOW  
DIAG PIN: HIGH  
WDC trigger: .

Operation mode:  
uC: Active  
device: Unlocked

Standard Control | SPI Regs | **NVM Programming** | SPI History | Device Info

### NVM Parameters

**Sect.** 5 **NVM Operation Status** IDLE **Program Counter** 6

**WRITE NVM** **Read NVM** **Reset**

**Low Current ByPass** OFF

**NVM Default Config.** OFF

**FailSafe Conf.** OUT DIN = 0x00

**DIN Enable** OFF

**DIN Ctrl OPT** OFF

**WDG TIME** 50 ms

**ThresHolds**

|              |        |
|--------------|--------|
| OVC (mV)     | 6      |
| HSC (mV)     | 20     |
| VDS (mV)     | 300    |
| NTC (mV)     | 110.92 |
| CCM VOUT (V) | 1      |
| UV (V)       | 4      |

**CCM (Capacitive Load Charge BurstMode) Conf.**

**CCM TimeOut** 200 ms

**CCM PWM Max Duration** 2.0 ms

**CCM PWM TimeON AMPL.** x 1

**CCM PWM TimeON** **TON Protection**

**CCM PWM Pulse** 5 Pulse

**CCM PWM Period** 50 us

**Device Mode**

UNLOCKED  
FAILSAFE  
GO\_STDBY  
HW/LD PIN

Unlocked

CR 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 0x00 04 01

CR 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0x00 00 00

CR 3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0x00 00 00

CR 5 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0x00 00 00

Board connected and ready... VNF1248 Eval Board, fw. rev.1.1

### 3.4.4

## SPI History

This form shows the SPI frames of the communication traffic between the Graphical User Interface and the VNF1248F device.

The **Clear List** button allows to erase the whole communication history from the log window.

It's also possible to select a Control Register and a Status Register for an easy access.

Figure 44. SPI History

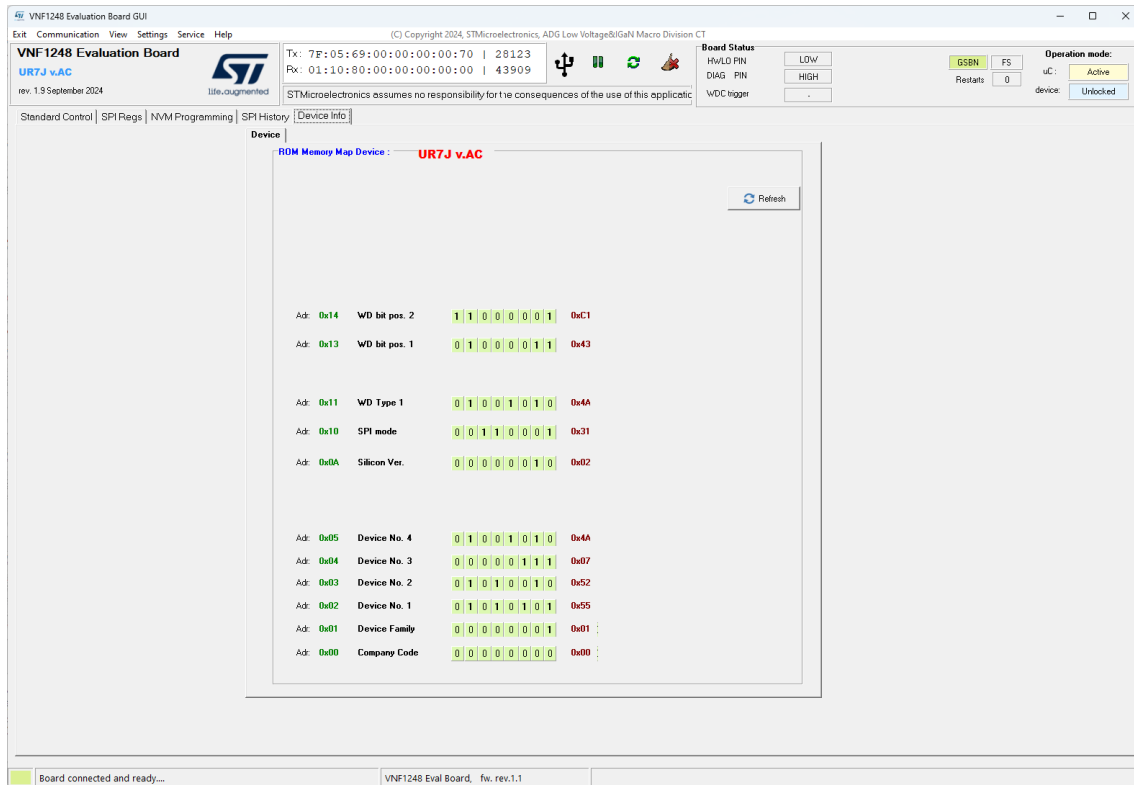
The screenshot shows the VNF1248 Evaluation Board GUI. The main window is titled 'VNF1248 Evaluation Board GUI' and contains several tabs: 'Standard Control', 'SPI Regs', 'NVM Programming', 'SPI History', and 'Device Info'. The 'SPI History' tab is selected, displaying a list of SPI transactions. Each transaction is represented by a line with a status (e.g., 'board status'), a data string (e.g., '0x00 00 00 10'), and an address (e.g., '27935'). A 'Clear List' button is located at the bottom of this list.

On the right side of the GUI, there are two sections: 'Status Register' and 'Control Register'. Each section contains a list of registers with their addresses and values. The 'Status Register' section has a 'Status Reg1' dropdown menu, and the 'Control Register' section has a 'Ctrl Reg1' dropdown menu. Below these dropdowns, there are buttons for '<< Status Register' and 'Control Register >>'. The status of the board is also displayed in the top right corner, including 'Board Status', 'H/WLD PIN', 'DAG PIN', 'WDC Error', 'Operation mode', 'uC', and 'device'.

### 3.4.5 Device Info

This form shows the ROM memory map of VNF1248F device. It can be refreshed manually with the dedicated button.

Figure 45. ROM Memory Map



## Revision history

**Table 1. Document revision history**

| Date        | Revision | Changes          |
|-------------|----------|------------------|
| 24-Jul-2025 | 1        | Initial release. |

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