AN14716

Migration guide from i.MX RT1170A to i.MX RT1170B

Rev. 1.0 — 11 June 2025 Application note

Document information

Information	Content
Keywords	AN14716, i.MX RT1170B, i.MX RT1170A, migration
Abstract	This document describes key differences in i.MX RT1170B when compared to i.MX RT1170A. This document is a migration reference.

1 Introduction

This document describes key differences in i.MX RT1170B when compared to i.MX RT1170A. This document is a migration reference.

This document is intended for the following audience:

- Engineers who developed projects based i.MX RT1170A and decided to migrate the project to i.MX RT1170B.
- Engineers familiar with i.MX RT1170A who want to start a new project based on previous knowledge of i.MX RT1170A.

2 Silicon changes

The silicon changes on i.MX RT1170B include:

1. "FSGPIO (GPIO_AD/GPIO_LPSR/GPIO_DISP_B2 bank)" change:
   This change fixes the issue reported in ERR052351 and ERR050643 in the i.MX RT1170A errata.
   a. ERR052351 FSGPIO: A parametric shift is observed over time on the FSGPIO output driver when it is powered by voltages above 1.98 V.
   b. ERR050643 GPIO: During the initial powerup, a brief pullup pulse can occur on the port.
2. ROM change:
   Cleaned the ROM patch. This change does not affect the open ROM API usage on i.MX RT1170B.
3. CHIPID change:
   The reset value of the "CHIPID" in the "MISC_DIFPROG" register is changed. For more details, see Section 4.

3 Data sheet changes

The i.MX RT1170B data sheet Rev.1 is based on the i.MX RT1170A data sheet Rev.5. As it is an initial version for i.MX RT1170B, there is no change list in the data sheet itself, and the changes based on the i.MX RT1170A data sheet Rev.5 are in this application note.

For all the common changes that should be applied to both i.MX RT1170B and i.MX RT1170A, see Section 8. These changes are regular DS update changes and they are not related to the migration.

This section lists only the changes applied on i.MX RT1170B that are related to the migration.

The table number listed below are from the i.MX RT1170B CEC. They may be different in IEC/AEC.

1. Part number changes:
   All the "MIMXRT117XXXXXA" occurrences are changed to "MIMXRT117XXXXXB". The "Silicon rev" list in "Figure 1. Part number nomenclature -i.MX RT11XX family" is also updated to support i.MX RT1170B.
2. In "Table 37. DC specification for GPIO_AD/GPIO_LPSR/GPIO_DISP_B2 bank":
   a. "IOH" is changed from -10 mA to -9 mA. (Output high, DSE = 1, High range mode).
   b. "IOH" is changed from -5 mA to -4.5 mA. (Output high, DSE = 0, High range mode).
3. In "Table 40. AC specifications for GPIO_AD/GPIO_LPSR/GPIO_DISP_B2 bank":
   Added new "Vpead" parameter on the pad.
4. In "Table 40. AC specifications for GPIO_AD/GPIO_LPSR/GPIO_DISP_B2 bank":
   "Pad rise/fall time (DSE=0, SRE=1)" in the continuous mode is changed from 6 ns to 7.5 ns.
5. In "Table 40. AC specifications for GPIO_AD/GPIO_LPSR/GPIO_DISP_B2 bank":
   A note is added:
   Note: *In the 3.3 V mode: If the IO toggling frequency is higher than or equal to 25 MHz, use the continuous range mode. If the IO toggling frequency is lower than 25 MHz, it is recommended to use the high range*

mode for better power consumption. In the 1.8 V mode: It is recommended to use the low range mode for better power consumption and better performance.

4 Reference manual changes

The i.MX RM1170 Reference Manual Rev. 4 is shared by i.MX RT1170A and i.MX RT1170B.

Only one change is related to the migration:

In the "CHIPID" in the "MISC_DIFPROG" register, the reset value of bit [7:4] is changed from "1011" to "uuuu".

A note is added:

Note: *For the i.MX RT1170A chip, bit [7:4] is "1011". For the i.MX RT1170B chip, bit [7:4] is "1100".*

For more changes that are not related to the migration, see the revision history in the reference manual.

5 Errata changes

Compared with Chip Errata for i.MX RT1170A, Rev. 1.6, the changes are as follows:

Removed:

1. ERR052351 FSGPIO: A parametric shift is observed over time on the "FSGPIO" output driver when it is powered by voltages above 1.98 V.
2. ERR050643 GPIO: During the initial powerup, a brief pullup pulse can occur on the port pins.

Added:

1. ERR052401 SEMC: "SEMC_CSX1/2/3" output timing degradation.

Description:

The "SEMC_CSX1/2/3" output delay is increased when compared to the Rev. A silicon. For the SYNC mode, it violates the maximum Tdvo by around 2.4 ns in the worst case. For the Async mode, configurations from the Rev. A silicon may be adjusted if using "SEMC_CSX1/2/3".

Workaround:

For the SYNC mode memory, use "SEMC_CSX0" or "SEMC_RDY" as a chip select. SDRAM can use "SEMC_CS0" as well. For the Async mode memory, if using "SEMC_CSX1/2/3", adjust the SEMC configuration (SRAMCR1[CES], NANDCR1[CES], NORCR1[CES]) to meet the device timing.

6 SDK code changes

The SDK version to support i.MX RT1170B will be SDK 25.06, which will be launched at the end of June 2025.

The code changes related to the migration in a previous SDK version include:

1. In "ROM_API_Init()", the previous code is not handling "CHIPID" correctly and leads to a wrong ROM API entry loaded.

```
void ROM_API_Init(void)
{
    if (ANADIG_MISC->MISC_DIFPROG == 0x001170a0U)
    {
        g_bootloaderTree = ((bootloader_api_entry_t *)*(uint32_t
 *)0x0020001cU);
    }
    else
```

```
    {
        g_bootloaderTree = ((bootloader_api_entry_t *)*(uint32_t
 *)0x0021001cU);
    }
}
```

2. In "ROM_FLEXSPI_NorFlash_ClearCache()", the "clearCacheFunctionAddress" is changed on i.MX RT1170B.

```
void ROM_FLEXSPI_NorFlash_ClearCache(uint32_t instance)
{
    uint32_t clearCacheFunctionAddress;
    if (ANADIG_MISC->MISC_DIFPROG == 0x001170a0U)
    {
        clearCacheFunctionAddress = 0x0020426bU;
    }
    else if (ANADIG_MISC->MISC_DIFPROG == 0x001170b0U)
    {
        clearCacheFunctionAddress = 0x0021a3b7U;
    }
    else
    {
        clearCacheFunctionAddress = 0x0021a3bfU;
    }
    …
}
```

7 Tool changes

1. J-Link version update: To support i.MX RT1170B well, J-Link v8.38 (or later) is needed.
2. For MCUXpresso v24.12 or earlier, the "RT1170_reset.scp" file in "C:\nxp\MCUXpressoIDE_24.12.148\ide\LinkServer\binaries\Scripts" must be updated to support i.MX RT1170B as follows:

```
550  REM IF a% & 0xFFFFFFFF != 0x00223104 Then GOTO 700
551  IF a% & 0xFFFFFFFF != 0x002231FC Then GOTO 700
```

8 Appendix A. Common changes in data sheets from i.MX RT1170A Rev.5 to i.MX RT1170B Rev.1

1. In "Table 8. Absolute maximum ratings":
   The storage temperature range is changed from -40 °C to -55 °C.
   Added a note below:
   Note: *The VDD_SOC_IN overshoot should be within 1.4 V and 20 ms.*
2. In "Table 89. SDR50/SDR104 interface timing specification":
   "SD6 (uSDHC Input Setup Time)" is changed from 2.5 to 2.0.
3. In "Table 38. AC specification for GPIO_EMC_B1/GPIO_EMC_B2/GPIO_SD_B1/GPIO_SD_B2/GPIO_DISP_B1":
   For the: Driver 3.3 V" application, "Rise/Fall time" is changed from 3 ns to 1.7 ns.
4. In "Table 61. FlexSPI output timing in SDR mode":
   "Max for TDVO" is changed from 4 to 1.
   "Min for TDHO" is changed from 2 to 0.
5. Removed "Table 105. Boot through SAI1".
6. In "Table 4. Special signal considerations", corrected the description for "JTAG_nnnn":

When JTAG_MOD is **low**, the JTAG interface is configured to a mode compliant with the IEEE 1149.1 standard.

7. In "Table 13. Typical power modes current and power consumption (Dual core)" and "Table 14. Typical power modes current and power consumption (Single core)":
   For the SNVS mode, added the following footnote:
   Note: *Please refer to section 4.7 and 4.11 in AN13104 for SNVS pin Leakage and how to enter SNVS mode.*
8. In "Figure 9. MCU-SDRAM circuit with overshoot/undershoot":
   Renamed "DIE" to "MCU", and put the arrow on the left.
9. In "Table 85. LPSPI Slave mode timing":
   For "twsck", use percentage as the "Unit".
10. In "Table 84. LPSPI Master mode":
    "tsu" is updated from 10 ns to 3 ns.
    "tv" is updated from 8 ns to 3.5 ns.
    The absolute maximum frequency of operation (fop) is updated from 30 MHz to 60 MHz.
    Added a note:
    Note: *Test with SAMPLE in CFGR1 being set.*
11. In "Table 11. Operating ranges":
    "NVCC_GPIO" is renamed to "NVCC_AD". This change will be reverted to "NVCC_GPIO" in the next version of release because it caused inconsistency in the document.
    The maximum for "NVCC_AD/DISP2/LPSR" is changed from 1.95 V to 1.98 V.
    Added notes:
    Note: *The operational ranges include both main DC component + AC ripple component.*
    Note: *NVCC for GPIO_AD/GPIO_LPSR/GPIO_DISP_B2 should not be floating to avoid leakage current of about 500 µA for each bank from VDDA_1P8_IN.*
12. In "Table 37. DC specification for GPIO_AD/GPIO_LPSR/GPIO_DISP_B2 bank":
    - Merged the normal voltage range/derated voltage range/derated2 voltage range to be the continuous range mode to align with the reference manual.
    - Renamed the low-voltage range to the low range mode to align with the reference manual.
    - Renamed the high-voltage range to the high range mode to align with the reference manual.
    - Min (VIH, Continuous range mode) is 0.7 * NVCC.
    - Max (VIL, Continuous range mode) is 0.25 * NVCC.
    - Max (VIL, Low range mode) is updated from "0.3 * NVCC" to "0.25 * NVCC".
    - Max (VIL, High range mode) is updated from "0.3 * NVCC" to "0.25 * NVCC".
    - Input Hysteresis (VHYSN) is changed to 120 mV.
    - IOH (Output high, DSE=1, Continuous range mode) is -10 mA.
    - IOH (Output high, DSE=0, Continuous range mode) is -5 mA.
    - IOL (Output low, DSE=1, Continuous range mode) is 10 mA.
    - IOL (Output low, DSE=0, Continuous range mode) is 5 mA.
    - NVCC for Continuous range mode is 3-3.6 V or 1.65-1.98 V.
    - NVCC MIN for Low range mode is updated from 1.71 V to 1.65 V.
    - Input leakage current is updated from 400 nA to 1 µA.

    Added a note:
    Note: *To select Continuous range mode/Low range mode/High range mode, please refer to IOMUXC GPR69[8:7], GPR69[5:4] and GPR69[2:1] in RM for AD/DISP2 bank and IOMUXC LPSR GPR34[2:1] in RM for LPSR bank.*
13. In "Table 40. AC specifications for GPIO_AD/GPIO_LPSR/GPIO_DISP_B2 bank":
    - Merged the normal voltage range/derated voltage range/derated2 voltage range to be the continuous range mode to align with the reference manual.
    - Renamed the low-voltage range to the low range mode to align with the reference manual.

- Renamed the high-voltage range to the high range mode to align with the reference manual.
- Pad rise/falling time(DSE=0, SRE=0, Continuous range mode) is 3 ns.
- Pad rise/falling time(DSE=0, SRE=0, High range mode) is updated from 3 ns to 6 ns.
- Pad rise/falling time(DSE=0, SRE=1, High range mode) is updated from 6 ns to 12 ns.
- Pad rise/falling time(DSE=1, SRE=0, Continuous range mode) is 2.5 ns.
- Pad rise/falling time(DSE=1, SRE=0, High range mode) is updated from 2.5 ns to 5 ns.
- Pad rise/falling time(DSE=1, SRE=1, Continuous range mode) is 5 ns.
- Pad rise/falling time(DSE=1, SRE=1, High range mode) is updated from 5 ns to 10 ns.
- Removed the "IPP_DO" to pad propagation delay parameter, which is not for customer usage.

Added notes:

Note: *In 3.3V mode: If the IO toggling frequency is higher than or equal to 25MHz, must use continuous range mode. If the IO toggling frequency is lower than 25MHz, it is recommended to use high range mode for better power consumption. In 1.8V mode: It is recommended to use low range mode for better power consumption and better performance.*

Note: *To select Continuous range mode/Low range mode/High range mode, please refer to IOMUXC GPR69[8:7], GPR69[5:4] and GPR69[2:1] in RM for AD/DISP2 bank and IOMUXC LPSR GPR34[2:1] in RM for LPSR bank.*

9 Note about the source code in the document

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10 Revision history

Table 1. Revision history

Document ID	Release date	Description
AN14716 v.1.0	11 June 2025	• Initial version

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