AN5293

Application note

Migration guide from STM32F7 Series to STMH74x/75x, STM32H72x/73x and STMH7A3/7Bx devices

Introduction

Designers of STM32 microcontroller applications must be able to replace easily one microcontroller type with another one from the same product family or from a different family. The reasons for migrating an application to a different microcontroller can be for example:

- To fulfill extended product requirements, extra demands on memory size, or an increased number of I/Os
- Meet cost reduction constraints that require a switch to smaller components and a shrunk PCB area

This application note analyzes the steps required to migrate applications from an existing STM32F7 Series device to one of the following STM32H7 lines below:

Table 1. Applicable products

Type(1)	Product lines
STM32H7A3/7Bx	STM32H7A3/7B3 and STM32H7B0 Value
STM32H72x/73x	STM32H723/733, STM32H725/735, and STM32H730 Value
STM32H74x/75x	STM32H742, STM32H743/753, STM32H745/755 and STM32H750(2)

1. *These generic names are sometimes used on this document to refer to the corresponding STM32H7 lines defined on the product lines column.*
2. *The dual core aspect of this line's devices is not considered for the purposes of this document.*

This application note provides a guideline on both hardware and peripheral migration. To understand fully all the information provided by this application note, the user must be familiar with the STM32 microcontroller family.

For additional information, refer to the following documents available on *www.st.com*:

- STM32F75xxx and STM32F74xxx advanced Arm®-based 32-bit MCUs reference manual (RM0385)
- STM32H745/755 and STM32H747/757 advanced Arm®-based 32-bit MCUs reference manual (RM0399)
- STM32F76xxx and STM32F77xxx advanced Arm®-based 32-bit MCUs reference manual (RM0410)
- STM32H742, STM32H743/753 and STM32H750 Value line advanced Arm®-based 32-bit MCUs" reference manual (RM0433)
- STM32H7A3/7B3 and STM32H7B0 Value line advanced Arm®-based 32-bit MCUs reference manual (RM0455)
- STM32H723/733, STM32H725/735, and STM32H730 Value line advanced Arm®-based 32-bit MCUs reference manual (RM0468)

1 General information

This document applies to all STM32F7 Series devices and to the STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx lines devices. All these products are Arm®-based microcontrollers.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 STM32H7 devices overview

STM32H7 devices offer extra performance compared to the STM32F7 Series devices without additional complexity. STM32H7 delivers its maximum theoretical performance by taking advantage of an L1-cache regardless of whether the code is executed from the embedded flash memory or the external memory.

STM32H7 devices, as Cortex®-M7 variants, are compatible with the STM32F7 Series devices (for the common packages). This compatibility allows customers to easily migrate from STM32F7 towards STM32H7 devices and to benefit from their significantly higher performance and their advanced peripherals.

STM32H7 devices include a larger set of peripherals with advanced features and optimized power consumption compared to the STM32F7 devices such as:

- Low-power universal asynchronous receiver transmitter (LPUART)
- Single wire protocol master interface (SWPMI)
- FD controller area network (FDCAN)
- Operational amplifiers (OPAMP)
- Comparator (COMP)
- Voltage reference buffer (VREFBUF)
- Switch mode power supply step down converter (SMPS)

This migration guide covers the migration from STM32F7 Series devices towards STM32H7A3/7Bx, STM32H72x/73x, and STM32H74x/75x devices.

The new features present on STM32H7 devices but not already present on STM32F7 Series devices or other STM32H7 devices are not covered in this document. Refer to the STM32H7 devices reference manual and datasheets for more details.

The following table presents the main differences between STM32H7A3/7Bx, STM32H72x/73x, and STM32H74x/75x devices at a glance. The following sections describe the differences in detail.

Table 2. **STM32H7 lines differences at a glance**

Feature		STH32H74x/75x	STH32H7Ax/7Bx	STH32H72x/73x
Core		Arm Cortex-M7, MPU, DP-FPU, L1 16KB-D/16KB-I ARM Cortex-M4, MPU, SP-FPU, ART	Arm Cortex-M7, MPU, DP-FPU, L1 16KB-D/16KB-I -	Arm Cortex-M7, MPU, DP-FPU, L1 32KB-D/32KB-I -
Operating range		1.62 to 3.6 V and Tj–40 to +125º C Up to +140º C with SMPS VOS1 limited to 125°C Vcore @VOS0: Tj limited to 105°C, VDD min 1.7 V No SMPS	1.62 to 3.6 V and Tj–40 to +130 º C Vcore @VOS0: Tj limited to 105°C VDD min 1.7 V	1.62 to 3.6 V and Tj–40 to +125º C Up to 140º C with SMPS VOS1 up to 140°C Vcore @VOS0: Tj limited to 105°C VDD min 1.7 V LDO VDD min 2.2 V SMPS
Cortex-M7 frequency/ DMIPS		480 MHz / 1027 DMIPS in VOS0 400 MHz / 856 DMIPS in VOS1	280 MHz / 599 DMIPS in VOS0 225 MHz / 481 DMIPS in VOS1	550 MHz / 1177 DMIPS in VOS0 400 MHz / 856 DMIPS in VOS1
AXI and AHB max frequency		240 MHz	280 MHz	275 MHz
APB max frequency		120 MHz	140 MHz	137.5 MHz
Debug	SWD/ JTAG/ETM	**I/I/4 Kbytes**	I/I/4 Kbytes	I /I/2 Kbytes
Low-power modes		Sleep, Stop, Standby, Vbat	Sleep, Stop, **Retention,** Standby, Vbat	Sleep, Stop, Standby, Vbat

2.1 STM32H74x/75x devices

The migration from STM32F7 Series devices towards STM32H743/753 devices is covered in detail in the application note *Migration of microcontroller applications from STM32F7 Series to STM32H743/753 Line* (AN4936).

The maximum theoretical performance of the STM32H74x/75x devices Cortex® -M7 core is 1414 CoreMark / 1027 DMIPS at 480 MHZ f_{CPU}.

When compared to other STM32H7 devices, STM32H74x/75x devices offer the following additional features:

- one Cortex®-M4 (STM32H745/755 only)
- one high-resolution timer
- one additional 16b ADC
- MIPI-DSI interface for driving the DSI display (STM32H747/757)
- two additional SAI
- one additional USB (FS)

When compared to STM32H72x/73x devices, STM32H74x/75x devices offer the following additional features:

- additional flash and RAM memory
- one additional passive tamper
- additional RAM for debug trace

When compared to STM32H7A3/7Bx devices, STM32H74x/75x devices offer the following additional features:

- two additional low-power timers.

2.2 STM32H72x/73x devices overview

The maximum theoretical performance of the STM32H72/73x devices Cortex® -M7 core is 2778CoreMark / 1177 DMIPS at 550 MHz f_{CPU}.

STM32H72x/73x devices are the fastest STM32H7 Series devices.

When compared to other STM32H7 devices, STM32H72x/73x devices offer the following additional features:

- more data and instruction cache
- possibility to increase instruction tightly coupled memory size
- FMAC (filtering) and Cordic (trigonometric) blocks for mathematical acceleration
- low pin-count package (UFQFPN68)
- more 32b timers, FDCAN, UART, USART, I2C
- one low-power 12b ADC in the low-power domain
- increased acceptable temperature at high frequency (400 MHz)

When compared to STM32H74x/75x devices, STM32H72/73x devices offer the following additional features:

- two OCTOSPI interfaces, instead of a single QUADSPI
- possibility to store encrypted code or data on external Octo-SPI memories (for STM32H73x devices)
- a parallel synchronous slave interface (PSSI)
- a digital temperature sensor

When compared to STM32H7A3/7Bx devices, STM32H72x/73x devices offer the following additional features:

- Ethernet
- two low-power timers added.

2.3 STM32H7A3/7Bx devices

The maximum theoretical performance of the STM32H7A3/7Bx devices Cortex® -M7 core is 1414 CoreMark / 599 DMIPS at 280-MHZ f_{CPU}.

STM32H7A3/7Bx devices are also the entry point of the wider STM32H7 Series devices, which can be seen as an easy stepladder to benefit from the high performance, the rich connectivity and the enhanced features of this advanced platform.

When compared to other STM32H7 devices, STM32H7A3/7Bx devices offer the following additional features:

- further optimized power consumption, significant in the low-power modes
- simplification of the power domains
- increased internal RAM size, very useful for graphics applications
- DFSDM increased to nine filters with dedicated DMA
- graphical oriented memory management unit (GFXXMMU)
- one DAC in low-power domain
- new tampers and active tamper which increases the security level

When compared to STM32H743/753 devices, STM32H7A3/7Bx devices offer the following additional features:

- two OCTOSPI interfaces, instead of a single QUADSPI
- possibility to store encrypted code or data on external Octo-SPI memories (for STM32H7B3 devices)
- a parallel synchronous slave interface (PSSI)
- a digital temperature sensor

When compared to STM32H72x/73x devices, STM32H7A3/7Bx devices offer the following additional features:

- increased flash memory size
- jpeg decoder
- DFSDM increased to nine filters with dedicated DMA
- graphical oriented memory management unit (GFXXMMU)
- additional RAM for debug trace.

3 System architecture differences between STM32F7 and STM32H7 Series

STM32F7 Series devices have one single available domain: an embedded AHB bus matrix.

In STM32H72x/73x and STM32H74x/75x devices there are three domains: an AXI bus matrix and two AHB bus matrices. Bus bridges permit the interconnection of the bus masters with the bus slaves:

- **D1 domain**: is the high bandwidth / high performance domain with the Cortex-M7 core and acceleration mechanisms. This domain encompasses the high-bandwidth features and the smart management thanks to the AXI bus matrix.
- **D2 domain**: is the "I/O processing" domain. It encompasses most peripherals that are less bandwidth demanding.
- **D3 domain**: it embeds up to 64-Kbyte RAM and has a subset of peripherals to run the basic functions while the domains 1 and 2 can be shut-off to save power (autonomous mode).

For the STM32H7A3/7Bx devices, the D1 and D2 domains are merged in a single domain called CD domain (or CPU domain) and the D3 domain evolved into a domain called SRD domain (or smart-run domain).

- **CD domain**: the CPU domain encompasses the Cortex-M7 core, the AXI bus matrix, an AHB bus matrix and most of the peripherals.
- **SRD domain**: it embeds a 32-Kbyte RAM and some peripherals to run basic functions while the CPU domain is in low-power mode (autonomous mode). For STM32H7A37Bx devices the power consumption in autonomous and Stop modes of this domain has been further optimized.

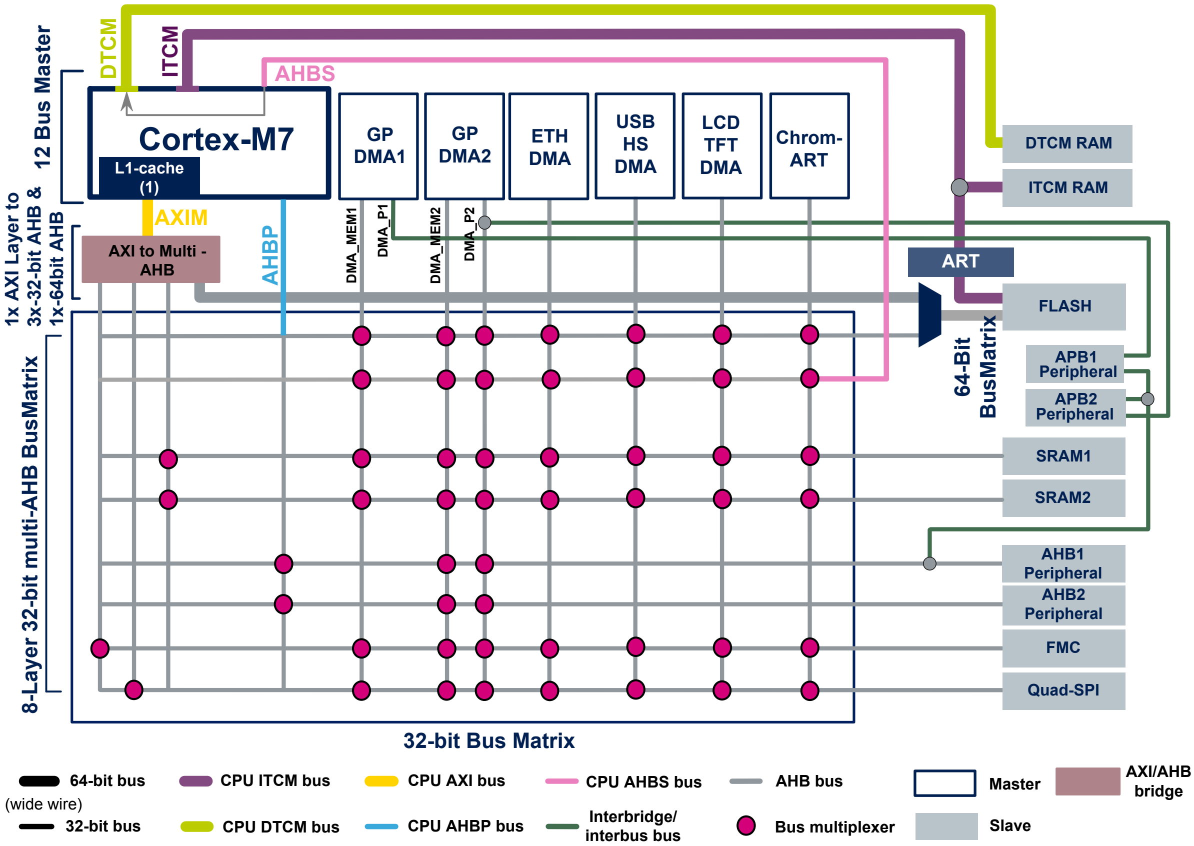
The differences in power modes are addressed on the Power (PWR) section of this application note.

The table below and the two subsequent figures illustrate the system architecture differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 3. Available bus matrix on STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

Device	AHB bus matrix	AXI bus matrix
STM32F7 Series	1	NA
STM32H74x/75x and STM32H72x/73x	2	1
STM32H7A3/7Bx	2	1

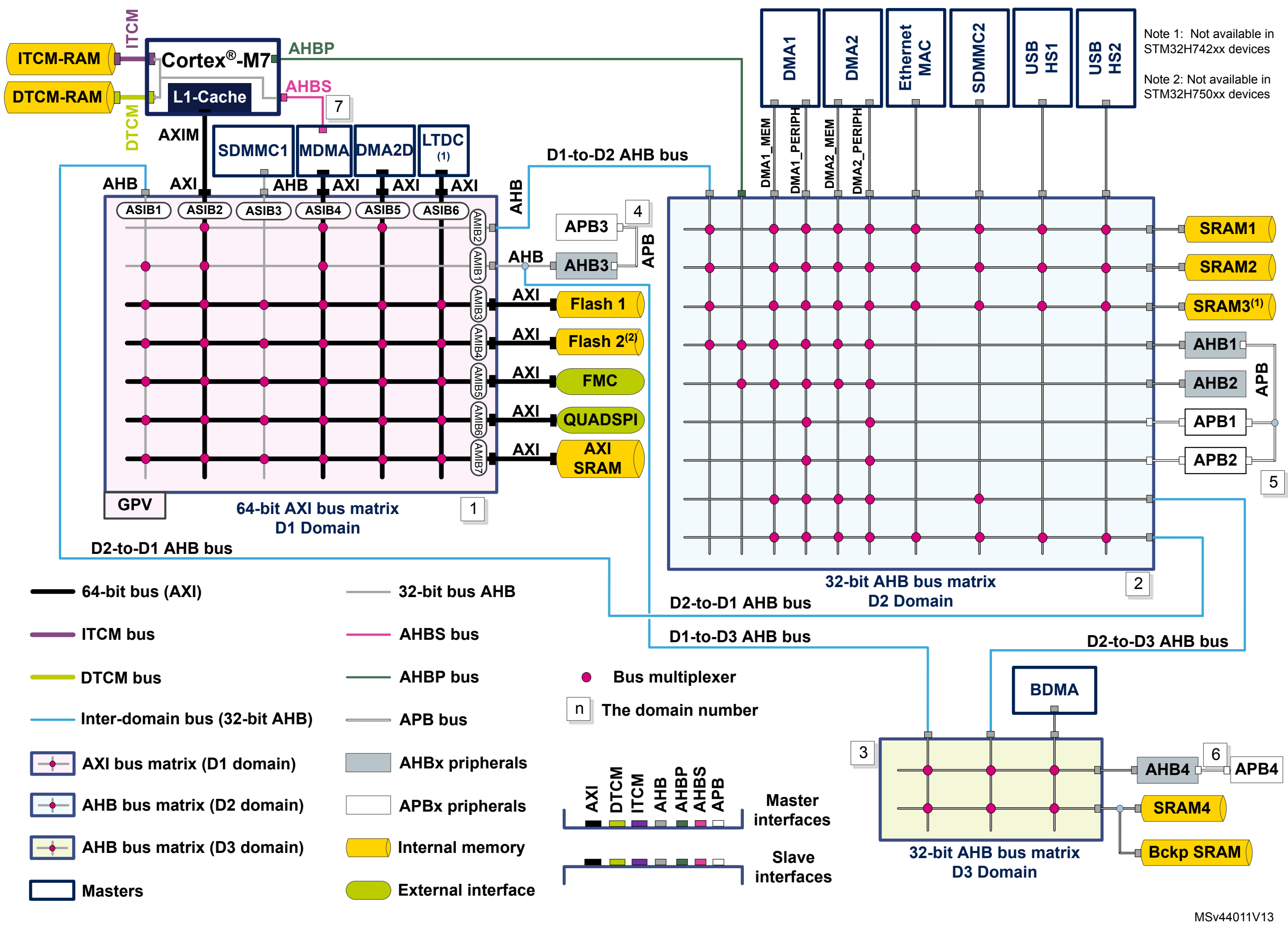
Figure 1. STM32F7 Series devices system architecture



Note: I/D cache size:

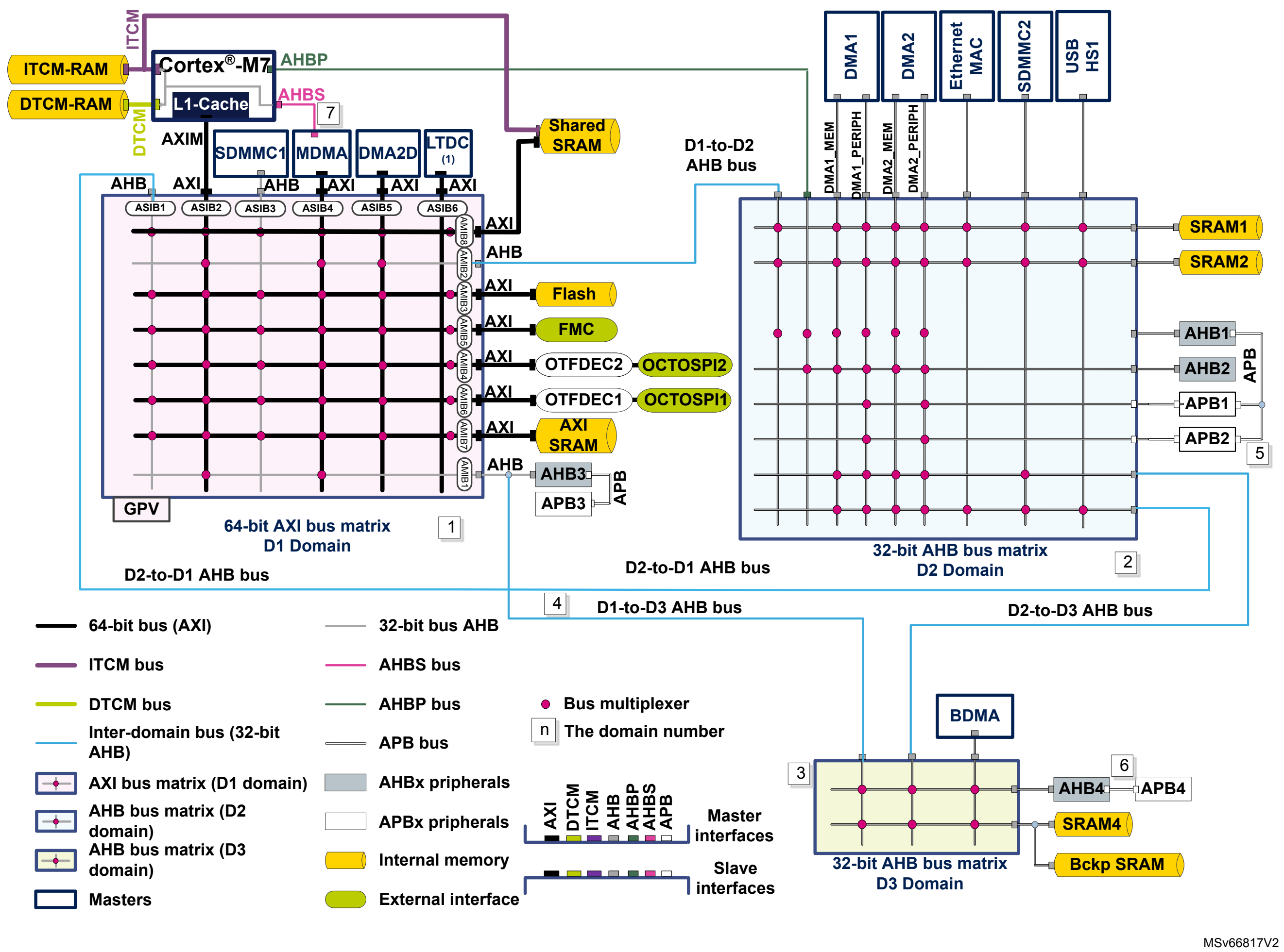
- *For STM32F74xxx and STM32F75xxx devices: 4 Kbytes.*
- *For STM32F72xxx and STM32F73xxx devices: 8 Kbytes.*
- *For STM32F76xxx and STM32F77xxx devices: 16 Kbytes.*

Figure 2. STM32H74x/75x devices system architecture



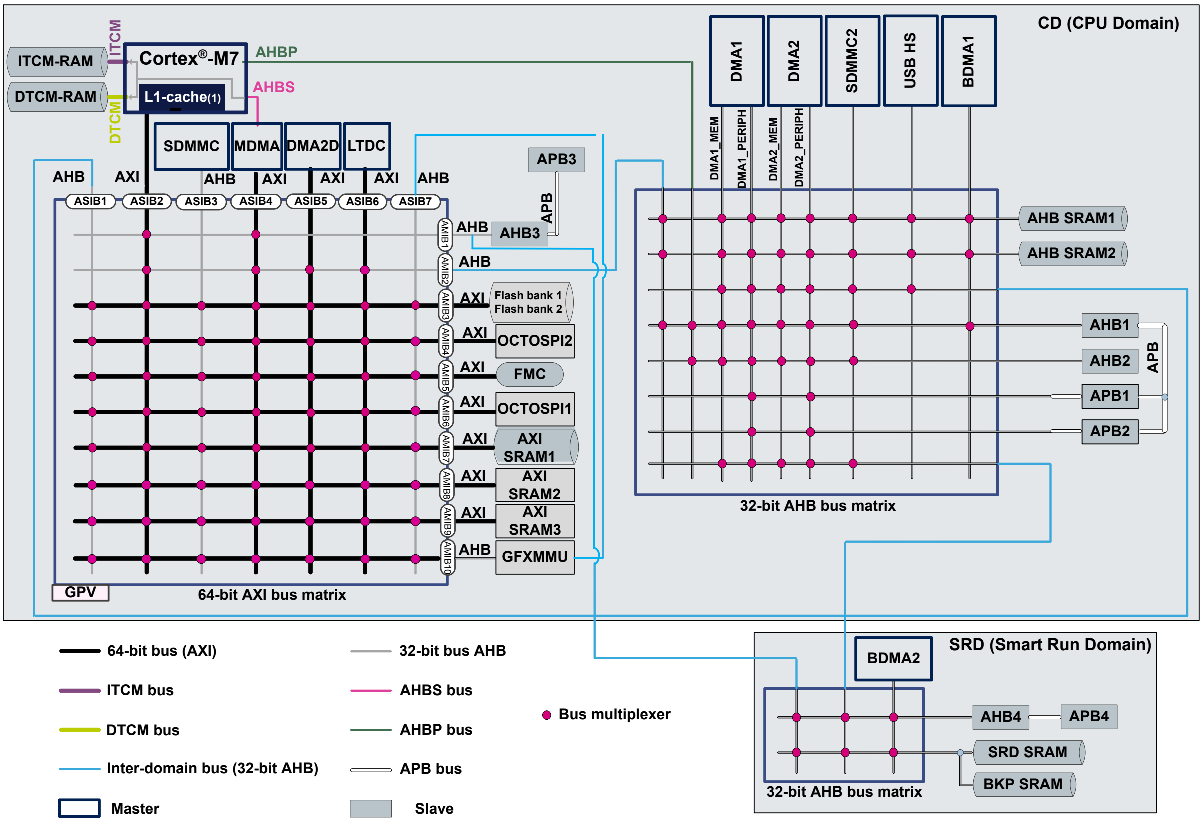
Note: STM32H74x/75x devices supports 16-Kbyte instruction cache and 16-Kbyte data cache.

Figure 3. STM32H72x/73x devices system architecture



Note: STM32H72x/73x devices supports 32-Kbyte instruction cache and 32-Kbyte data cache.

Figure 4. STM32H7A3/7Bx devices system architecture



Note: STM32H7B0x support a single bank (flash Bank1 only)

4 Hardware migration

4.1 Available packages

The available packages on STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices are listed in the table below.

STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices support the switched-mode power supply (SMPS) step-down converter available in some specific packages, which are not compatible with the legacy packages (see table below and refer to Figure 6).

Table 4. Available packages on STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

<table>
<tr><th>Package</th><th>STM32F7 Series</th><th>STM32H74x/75x</th><th>STM32H72x/73x</th><th>STM32H7A3/7Bx</th><th>Regulator</th></tr>
<tr><td>LQFP64</td><td rowspan="5">Available</td><td>NA</td><td>NA</td><td rowspan="4">Available</td><td rowspan="11">LDO(1)</td></tr>
<tr><td>LQFP100</td><td rowspan="3">Available</td><td rowspan="4">Available</td></tr>
<tr><td>TFBGA100</td></tr>
<tr><td>LQFP144</td></tr>
<tr><td>UFBGA144</td><td>NA</td><td rowspan="2">NA</td></tr>
<tr><td>UFBGA169</td><td>NA</td><td rowspan="4">Available</td><td rowspan="5">NA</td></tr>
<tr><td>UFBGA176+25</td><td rowspan="4">Available</td><td rowspan="2">Available</td></tr>
<tr><td>LQFP176</td></tr>
<tr><td>LQFP208</td><td>NA</td></tr>
<tr><td>TFBGA216</td><td>NA</td><td>Available</td></tr>
<tr><td>TFBGA240</td><td rowspan="10">NA</td><td>Available</td><td>NA</td><td rowspan="2">NA</td></tr>
<tr><td>VFQFPN68 SMPS</td><td rowspan="3">NA</td><td rowspan="6">Available</td><td rowspan="9">LDO/SMPS/
regulator bypass</td></tr>
<tr><td>LQFP100 SMPS</td><td rowspan="6">Available</td></tr>
<tr><td>TFBGA100 SMPS</td></tr>
<tr><td>LQFP144 SMPS</td><td>Available</td></tr>
<tr><td>UFBGA169 SMPS</td><td>NA</td></tr>
<tr><td>UFBGA176+25 SMPS</td><td rowspan="3">Available</td></tr>
<tr><td>LQFP176 SMPS</td><td rowspan="3">NA</td></tr>
<tr><td>LQFP208 SMPS</td><td>NA</td></tr>
<tr><td>TFBGA225 SMPS</td><td>NA</td><td>Available</td></tr>
<tr><td>WLCSPxxx</td><td colspan="5">Specific for each device</td></tr>
</table>

1. *STM32F7 Series and STM32H7A3/7Bx lnes devices can be used in Regulator bypass mode.*

4.2 Pinout compatibility

STM32F7 Series devices and STM32H74x/75x devices are pin to pin compatible with the STM32H7A3/7Bx devices (with some restrictions for the LQFP64, TFBGA100, LQFP176, UFBGA176 and TFBGA216 packages).

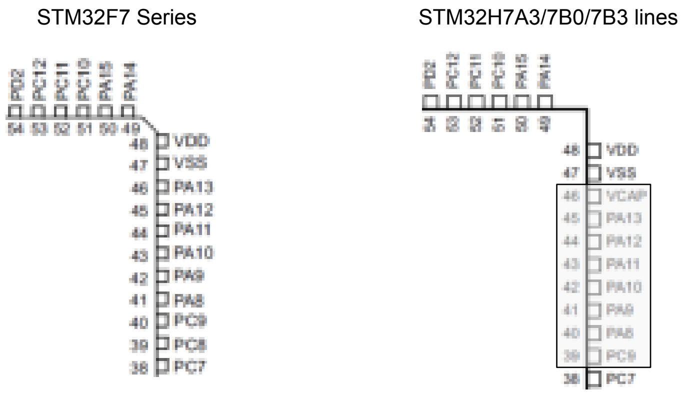
In STM32H72x/73x devices, LQFP100 SMPS pin 72 is VCAP whereas it is PE0 for STM32H7A3/7Bx.

In STM32H7A3/7Bx devices, a second VCAP pin is added for the LQFP64 package; in consequence, several GPIOs are no longer compatible with STM32F7 Series devices. See below table and figure for more details.

Table 5. LQFP64 package compatibility between STM32F7 Series and STM32H7A3/7Bx devices

Package	Pin	STM32F7 Series	STM32H7A3/7Bx
LQFP64	38	PC7	PC7
	39	PC8	PC9
	40	PC9	PA8
	41	PA8	PA9
	42	PA9	PA10
	43	PA10	PA11
	44	PA11	PA12
	45	PA12	PA13
	46	PA13	VCAP

Figure 5. LQFP64 package compatibility



For the TFBGA100, LQFP176, UFBGA176 and TFBGA216 packages, the BYPASS_REG pin is replaced in the STM32H7 Series with a VSS pin.

For the STM32F7 Series devices, the BYPASS_REG pin connected to VDD permits to select the mode where the internal regulator is switched off and the core supply is externally provided.

For the STM32H7 Series devices, there is no dedicated pin that defines if the regulator is in bypass mode or which regulator(s) is/are used. It is done through software at system startup. Both LDO and SMPS regulators are enabled by default during startup and the user software defines if the LDO or the SMPS or both are switched off (see Figure 6).

Note: Special care has to be taken if an STM32F7 Series device is replaced with an STM32H7 device on a PCB board where the BYPASS_REG pin is set to VDD (see the table below).

The following table and figure illustrate the BYPASS_REG pin incompatibility in TFBGA100, LQFP176, UFBGA176 and TFBGA216 packages and the system supply configuration on the STM32F7 Series devices and STM32H74x/75x devices.

Table 6. BYPASS_REG pin incompatibility between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

Package	Pin/ ball	STM32F7 Series	STM32H74x/ 75x	STM32H72x/ 73x	STM32H7A3/7Bx	Comment
TFGA100	Ball E6	BYPASS_REG	VSS	VSS	VSS	Impacts only the boards designed with STM32F7 Series devices in the regulator bypass mode (BYPASS_REG set to VDD)
LQFP176	Pin 48		VSS	NA		
UFBGA176+25	Ball L4		VSS	NA		
TFBGA216	Ball L5		NA	NA		

Figure 6. System supply configuration on STM32H74x/75x and STM32H7A3/7Bx devices with SMPS

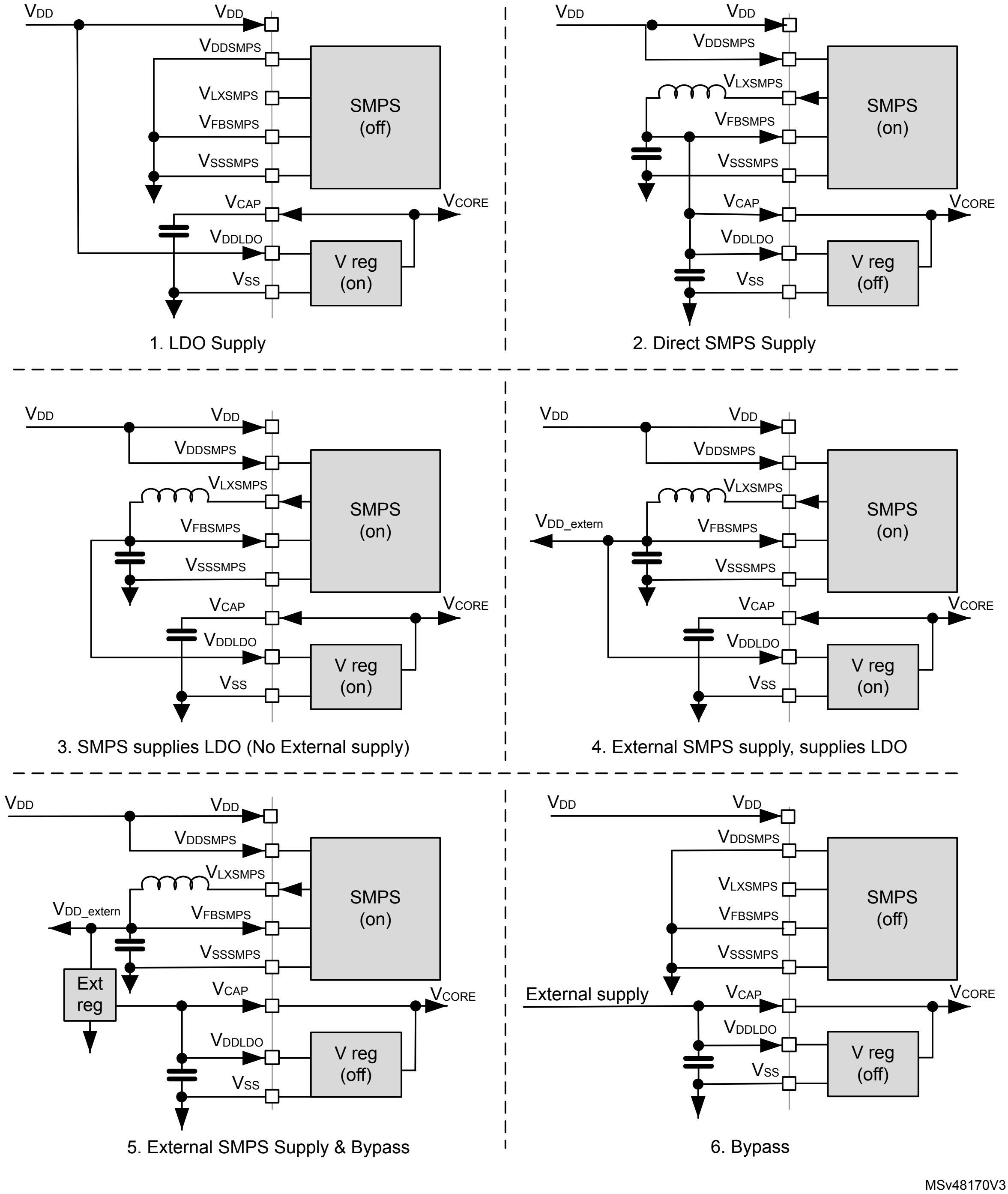
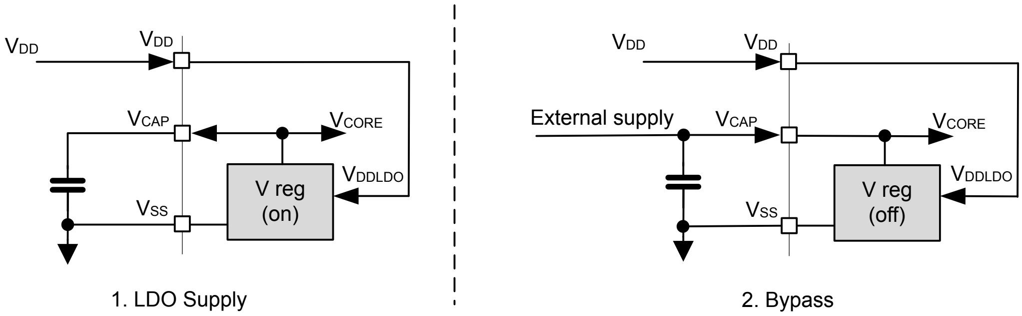


Figure 7. System supply configuration on STM32H74x/75x and STM32H7A3/7Bx devices without SMPS



4.3 System bootloader

The system bootloader is located in the system memory, programmed by ST during production. The system bootloader permits to reprogram the flash memory using one of the supported serial interfaces. More details are provided in the following table:

Table 7. STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices bootloader communication peripherals

System bootloader peripherals	STM32F7 Series I/O pin	STM32H74x/75x I/O pin	STM32H7A3/7Bx I/O pin	STM32H72x/73x I/O pin
DFU	USB OTG FS (PA11 / PA12) in device mode			
USART1	PA9 / PA10			
USART 2	NA	PA2 / PA3		
USART3	PB10 / PB11 PC10 / PC11	PB10 / PB11		PB10 / PB11 PD8 / PD9
I2C1	PB6 / PB9			
I2C2	PF0 / PF1			
I2C3	PA8 / PC9			
SPI1	PA7 / PA6 / PA5 / PA4			
SPI2	PI3 / PI2 / PI1 / PI0			NA
SPI3	NA	PC12 / PC11/ PC10 / PA15		
SPI4	PE14 / PE13 / PE12 / PE11			
FDCAN1	PB5 / PB13 [(1)] PD0 / PD1[(2)]	NA	PH13 / PH14 PD1 / PD0	PH13 / PH14 PD1 / PD0

1. *Available on the STM32F74xxx/75xxx and STM32F76xxx/77xxx devices.*
2. *Available on the STM32F72xxx/73xxx devices.*

5 Boot mode compatibility

The STM32F7 Series devices, the STM32H74x/75x, STM32H72x/73x, and the STM32H7A3/7Bx devices boot spaces are based on BOOT0 and boot address option bytes as described in the table below.

For the STM32F7 Series devices, the boot base address supports any address in the range from 0x0000 0000 to 0x3FFF FFFF while in STM32H74x/75x, STM32H72x/73x, and the STM32H7A3/7Bx, the boot base address supports any address in the range from 0x0000 0000 to 0x3FFF 0000.

Table 8. **Boot mode compatibility between STM32F7 Series, STM32H74x/75x, STM32H72x/73x, and STM32H7A3/7Bx devices**

Boot mode selection		STM32F7 Series	STM32H74x/75x, STM32H72x/73x, and STM32H7A3/7Bx
Boot	Boot address option bytes		
0	BOOT_ADD0[15:0]	Boot address defined by user option byte BOOT_ADD0[15:0] ST programmed value: flash on ITCM at 0x0020 0000	Boot address defined by user option byte BOOT_ADD0[15:0] ST programmed value: flash memory at 0x0800 0000
1	BOOT_ADD1[15:0]	Boot address defined by user option byte BOOT_ADD1[15:0] ST programmed value: System bootloader at 0x0010 0000	Boot address defined by user option byte BOOT_ADD1[15:0] ST programmed value: System bootloader at 0x1FF0 0000

6 Peripheral migration

6.1 STM32 product cross-compatibility

The STM32 microcontrollers embed a set of peripherals, which can be classed in three categories:

- The first category is for the peripherals that are by definition common to all products. Those peripherals are identical, so they have the same structure, registers, and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- The second category is for the peripherals that are shared by all STM32 products but have only minor differences (in general to support new features), so the migration from one product to another is very easy and does not need any significant new development effort.
- The third category is for peripherals that have been considerably changed from one product to another (new architecture, new features...). For this category of peripherals, the migration requires a new development at application level.

This table below shows the STM32 peripheral compatibility between the STM32F7 Series, STM32H74x/75x and STM32H7A3/7Bx devices. The software compatibility mentioned in this table refers only to the register description for *low-level* drivers. The Cube hardware abstraction layer (HAL) is compatible between STM32F7 Series devices, STM32H74x/75x and STM32H7A3/7Bx devices.

Table 9. Peripheral summary for STM32F7 Series, STM32H74x/75x, STM32H72x/73x, and STM32H7A3/7Bx devices

<table>
<tr><th colspan="2">Peripheral</th><th>STM32F7 Series</th><th>STM32H74x/75x</th><th>STM32H7A3/7Bx</th><th>STM32H72x/73x</th><th>Compatibility/ comments</th></tr>
<tr><td colspan="2">Power supply</td><td>• Power supply for I/Os: 1.71 to 3.6 V
• Internal regulator VDD = 1.7 to 3.6 V</td><td colspan="3">• Power supply for I/Os: 1.62 to 3.6 V
• Internal regulator VDDLDO = 1.62 to 3.6 V
• SMPS step down converter
• VDDSMPS = 1.62 to 3.6 V</td><td>-</td></tr>
<tr><td colspan="2">Maximum frequency</td><td>216 MHz</td><td>480 MHz</td><td>280 MHz</td><td>550 MHz</td><td>-</td></tr>
<tr><td colspan="2">MPU region number</td><td>8</td><td colspan="3">16</td><td>-</td></tr>
<tr><td colspan="2">Flash memory</td><td colspan="3">Up to 2 Mbytes single or dual bank</td><td>Up to 1Mbytes single bank</td><td>With ECC protection for STM32H7 Series devices</td></tr>
<tr><td rowspan="6">SRAM</td><td>System</td><td>512 Kbytes</td><td>~1 Mbyte
(992 Kbytes)</td><td>~1.3 Mbytes
(1312 Kbytes)</td><td>564 Kbytes</td><td>With ECC protection for STM32H72/72/724/75, ECC protection on TCM and cache only for STM32H7A/7B</td></tr>
<tr><td>ITCM</td><td>16 Kbytes</td><td colspan="2">64 Kbytes</td><td>64 Kbytes to
256 Kbytes</td><td>-</td></tr>
<tr><td>DTCM</td><td colspan="4">128 Kbytes</td><td>-</td></tr>
<tr><td>Data cache</td><td colspan="3">16 Kbytes</td><td>32 Kbytes</td><td>-</td></tr>
<tr><td>Instruction cache</td><td colspan="3">16 Kbytes</td><td>32 Kbytes</td><td>-</td></tr>
<tr><td>Backup</td><td colspan="4">4 Kbytes</td><td>-</td></tr>
<tr><td rowspan="2">Common peripherals</td><td>FMC</td><td colspan="4">1</td><td>-</td></tr>
<tr><td>QUADSPI</td><td colspan="2">1</td><td colspan="2">NA</td><td>-</td></tr>
</table>

<table>
<tr><th colspan="2">Peripheral</th><th>STM32F7 Series</th><th>STM32H74x/75x</th><th>STM32H7A3/7Bx</th><th>STM32H72x/73x</th><th>Compatibility/ comments</th></tr>
<tr><td rowspan="2">Common peripherals</td><td>OCTOSPI</td><td colspan="2">NA</td><td colspan="2">2</td><td>All QUADSPI features are covered by OCTOSPI</td></tr>
<tr><td>Ethernet</td><td colspan="2">1</td><td>NA</td><td>1</td><td>-</td></tr>
<tr><td rowspan="5">Timers</td><td>High resolution</td><td>NA</td><td>1</td><td colspan="2">NA</td><td>-</td></tr>
<tr><td>General purpose</td><td colspan="3">10</td><td>12</td><td>-</td></tr>
<tr><td>PWM</td><td colspan="4">2</td><td>-</td></tr>
<tr><td>Basic</td><td colspan="4">2</td><td>-</td></tr>
<tr><td>Low-power</td><td>1</td><td>5</td><td>3</td><td>5</td><td>-</td></tr>
<tr><td colspan="2">RNG</td><td colspan="4">Yes</td><td>-</td></tr>
<tr><td rowspan="16">Communication interfaces</td><td>SPI/I2S</td><td>4/3</td><td>6/3</td><td colspan="2">6/4</td><td>Wakeup from stop capability for STM32H7 Series</td></tr>
<tr><td>I2C</td><td colspan="3">4</td><td>5</td><td>-</td></tr>
<tr><td>USART</td><td colspan="2">4</td><td colspan="2">5</td><td>-</td></tr>
<tr><td>UART</td><td colspan="2">4</td><td colspan="2">5</td><td>-</td></tr>
<tr><td>LPUART</td><td>NA</td><td colspan="3">1</td><td>-</td></tr>
<tr><td>SAI</td><td>2</td><td>4</td><td colspan="2">2</td><td>-</td></tr>
<tr><td>SPDIFRX</td><td colspan="4">4 inputs</td><td>-</td></tr>
<tr><td>SWPMI</td><td>NA</td><td colspan="3">1</td><td>-</td></tr>
<tr><td>MDIO</td><td colspan="4">1</td><td>-</td></tr>
<tr><td>SDMMC</td><td colspan="4">2</td><td>-</td></tr>
<tr><td>CAN</td><td>x3 CANs (2.0B active)</td><td colspan="2">x2 CAN FD
(FDCAN1 supports TTCAN)</td><td>x3 CAN FD (FDCAN1 supports TTCAN)</td><td>-</td></tr>
<tr><td>USB OTG FS</td><td colspan="2">1</td><td colspan="2">NA</td><td>-</td></tr>
<tr><td>USB OTG HS</td><td colspan="4">1</td><td>Support FS and HS with ULPI</td></tr>
<tr><td>HDMI-CEC</td><td colspan="4">1</td><td>-</td></tr>
<tr><td rowspan="2">DFSDM number of filters</td><td colspan="2">1</td><td>2</td><td>1</td><td>-</td></tr>
<tr><td colspan="2">4</td><td>8/1</td><td>4</td><td>-</td></tr>
<tr><td rowspan="2">Digital camera interface</td><td>DCMI</td><td colspan="4">1</td><td>-</td></tr>
<tr><td>PSSI</td><td colspan="2">NA</td><td colspan="2">1</td><td>-</td></tr>
<tr><td colspan="2">MIPI-DSI host</td><td colspan="2">1</td><td colspan="2">NA</td><td>Available only on specific packages</td></tr>
<tr><td rowspan="3">Graphics</td><td>LCD-TFT</td><td colspan="4">1</td><td>-</td></tr>
<tr><td>Chrom-ART Accelerator™ (DMA2D)</td><td colspan="4">1</td><td>YCbCr to RGB color space conversion on STM32H7 Series</td></tr>
<tr><td>JPEG Codec</td><td colspan="3">1</td><td>NA</td><td></td></tr>
</table>

Peripheral		STM32F7 Series	STM32H74x/75x	STM32H7A3/7Bx	STM32H72x/73x	Compatibility/ comments
Graphics	GFXMMU	NA		1	NA	Graphical oriented memory management unit
GPIOs		Up to 159	Up to 168		Up to 128	-
Analog peripherals	ADC 12b	3	NA		1	Available down to 1.62 V for STM32H7 Series
	ADC 16b	NA	3	2		
	12-bit DAC	2 channels		3 channels	2 channels	-
	Operational amplifiers	NA	2			-
	Ultra-low-power comparator	NA	2			-
DMA		General-purpose DMA: 16-stream DMA controller with FIFOs and burst support	4 DMA controllers to unload the CPU • x1 high-speed general-purpose master direct memory access controller (MDMA) • x2 dual-port DMAs with FIFO and request router capabilities for optimal peripheral management • x1 basic DMA with request router capabilities	5 DMA controllers to unload the CPU • x1 high-speed general-purpose master direct memory access controller (MDMA) • x2 dual-port DMAs with FIFO and request router capabilities for optimal peripheral management • x1 basic DMA with request router capabilities • x1 basic DMA dedicated to the DFSDM	4 DMA controllers to unload the CPU • x1 high-speed general-purpose master direct memory access controller (MDMA) • x2 dual-port DMAs with FIFO and request router capabilities for optimal peripheral management • x1 basic DMA with request router capabilities	On STM32H7 Series: • No limitation for peripheral requests thanks to DMAMUX • DMA1 and DMA2 can access to peripherals in APB1/APB2 buses • Peripheral request mapping is no longer managed by the DMA controller but by the DMAMUX controller
Cryptographic acceleration		• AES 128, 192, 256, DES/TDES • HASH (MD5, SHA-1, SHA-2) • HMAC • True random number generator				-
Security	ROP	ROP	ROP, PC-ROP one secure-only areas per flash bank			-
	Tamper	Tamper	Tamper	Active tamper	Tamper	-

6.2 Memory organization

6.2.1 RAM size

The following table illustrates the difference of RAM size between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 10. Comparison of RAM size between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

<table>
<tr><th>Memory</th><th>STM32F7 Series</th><th>STM32H74x/75x</th><th>STM32H7A3/7Bx</th><th>STM32H72x/73x</th><th>Units</th></tr>
<tr><td>ITCM-RAM</td><td>16</td><td colspan="2">64</td><td>64(1)</td><td rowspan="9">Kbyte</td></tr>
<tr><td>DTCM-RAM</td><td>128(2)</td><td colspan="3">128</td></tr>
<tr><td>AXI-SRAM</td><td>-</td><td>512</td><td>1024
(split in 3 SRAMs)</td><td>128(1)</td></tr>
<tr><td>SRAM1</td><td>368</td><td>128</td><td>64</td><td>16</td></tr>
<tr><td>SRAM2</td><td>16</td><td>128</td><td>64</td><td>16</td></tr>
<tr><td>SRAM3</td><td>NA</td><td>32</td><td>NA</td><td>NA</td></tr>
<tr><td>SRAM4</td><td>NA</td><td>64</td><td>32</td><td>16</td></tr>
<tr><td>Backup SRAM</td><td colspan="4">4</td></tr>
<tr><td>Total</td><td>532</td><td>1060</td><td>1380</td><td>564</td></tr>
</table>

1. *Can be increased with ITCM / AXI hared memory.*
2. *64k bytes for STM32F74xxx/75xxx devices.*

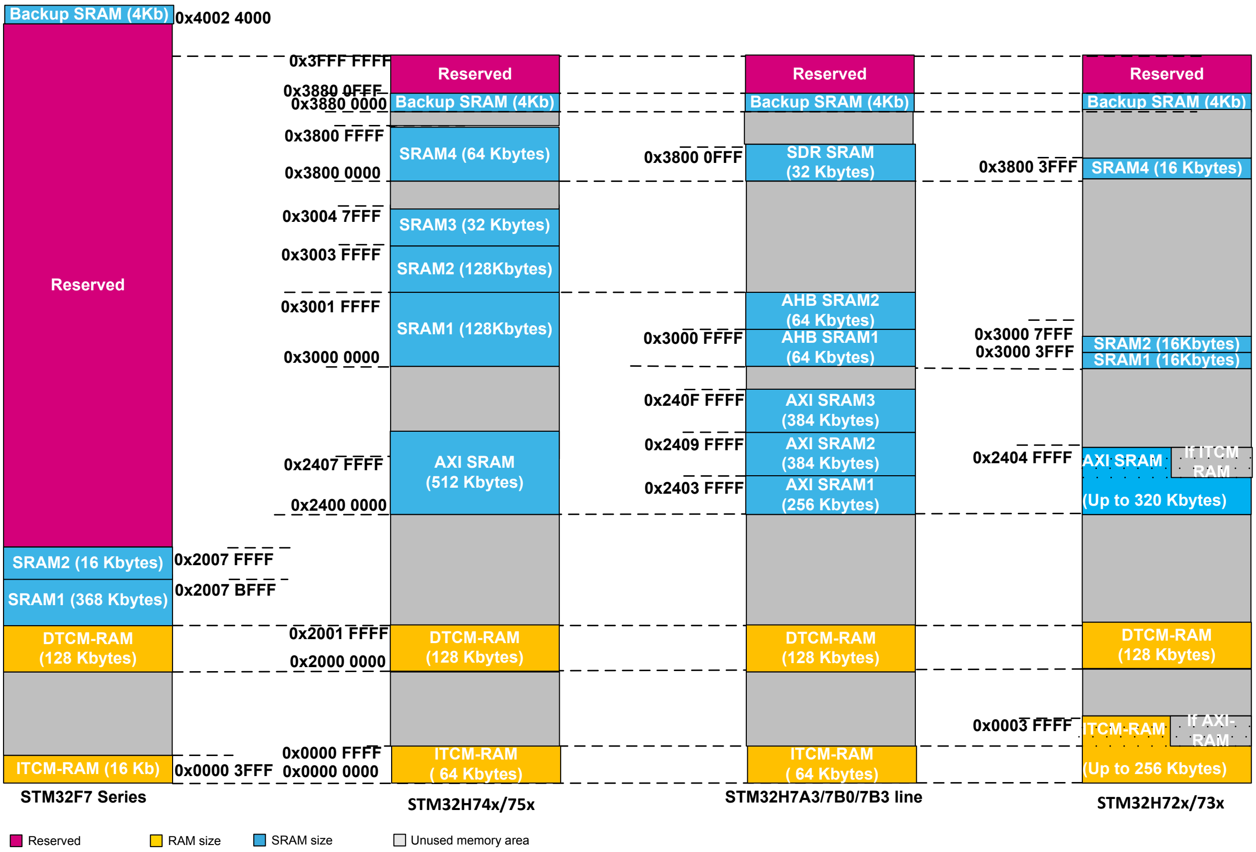
6.2.2 Memory map and peripherals register boundary addresses

The table and figure below illustrate the memory addresses between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 11. Memory organization and compatibility between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

<table>
<tr><th colspan="2">Memory</th><th>STM32F7</th><th>STM32H74/75</th><th>STM32H7A/7B</th><th>STM32H72/73</th><th>Comments</th></tr>
<tr><td colspan="2">ITCM-RAM</td><td>0x0000 0000 – 0x0000 3FFF</td><td colspan="2">0x0000 0000 – 0x0000 FFFF</td><td>0x0000 0000 – 0x0000 FFFF
0x0000 0000 – 0x0001 FFFF
0x0000 0000 – 0x0002 FFFF
0x0000 0000 – 0x0003 FFFF</td><td>STM32H72/73 size depends on shared memory assignment</td></tr>
<tr><td colspan="2">DTCM-RAM</td><td colspan="4">0x2000 0000 – 0x2001 FFFF</td><td>Some STM32F7 devices feature only 64 Kbytes</td></tr>
<tr><td rowspan="7">FLASH</td><td rowspan="3">Bank1</td><td rowspan="6">Flash bank 1
0x0800 0000 - 0x080F FFFF
Flash bank 2
0x0810 0000 - 0x081F FFFF</td><td colspan="3">0x0800 0000 - 0x080F FFFF</td><td>STM2H74/75xxI
STM32H7B3/H7A3xI
STM32H72/73xxG</td></tr>
<tr><td colspan="3">0x0800 0000 - 0x0807 FFFF</td><td>STM2H74/75xxG
STM32H7B3/ H7A3xG
STM32H72/73xxE</td></tr>
<tr><td colspan="3">0x0800 0000 - 0x0801 FFFF</td><td>Value line</td></tr>
<tr><td rowspan="3">Bank2</td><td colspan="2">0x0810 0000 - 0x081F FFFF</td><td>NA</td><td>STM2H74/75xxI
STM32H7B3/H7A3xI</td></tr>
<tr><td colspan="2">0x0810 0000 - 0x0817 FFFF</td><td>NA</td><td>STM2H74/75xxG
STM32H7B3/ H7A3xG</td></tr>
<tr><td colspan="3">NA</td><td>Value line</td></tr>
<tr><td>Flash - ITCM</td><td>0x0020 0000 – 0x003FF FFFF</td><td colspan="3">NA</td><td>NA</td></tr>
<tr><td rowspan="2">System memory</td><td>Bank1</td><td>0x1FF0 0000 – 0x1FF0 EDBF</td><td>0x1FF0 0000 – 0x1FF1 FFFF</td><td>0x1FF0 0000 – 0x1FF0 FFFF</td><td>0x1FF0 0000 – 0x1FF0 FFFF</td><td>NA</td></tr>
<tr><td>Bank2</td><td>NA</td><td>0x1FF4 0000 – 0x1FF5 FFFF</td><td>0x1FF1 0000 – 0x1FF1 FFFF</td><td colspan="2">NA</td></tr>
</table>

Figure 8. RAM memory organization of STM32F7 Series, STM32H743/753 and STM32H7A3/7Bx devices



Note: *DTCM-RAM size:*

- *128 Kbytes STM32F76xxx, STM32F77xxx and STM32H743/753 and STM32H7A3/7B0/7B3 devices*
- *64 Kbytes for the STM32F75xxx and STM32F74xxx devices*

6.2.3 Peripheral register boundary addresses

The peripheral address mapping has been changed for most of peripherals in the STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices versus the STM32F7 Series devices.

For more details about registers boundary addresses differences refer to Memory map and register boundary addresses section of RM0368, RM0385, RM0410, RM0433 and RM0455 reference manuals.

Section 6.2.2 Memory map and peripherals register boundary addresses shows the detail of all the peripherals address mapping differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 12. Examples of peripheral address mapping differences between STM32F7 Series,STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

Peripheral	STM32F7 Series devices	STM32H74/75 devices	STM32H72/73 devices	STM32H7A/7B devices	STM32F7 Series devices	STM32H74/75 devices	STM32H72/73 devices	STM32H7A/7B devices
	Bus				Base address			
QUADSPI control	AHB3		NA		0xA000 1000 - 0xA000 1FFF	0x5200 5000 - 0x5200 5FFF	NA	
GPIOA	AHB1	AHB4 (D3 or SRD)			0x4002 0000 - 0x4002 03FF	0x5802 0000 - 0x5802 03FF		
RCC					0x40023800 - 0x40023BFF	0x58024400 - 0x580247FF		
DFSDM2	NA			AHB4 (SRD)	NA			0x5800 6C00 - 0x5800 73FF
DTS	NA		AHB4 (D3 or SRD)		NA		0x5800 6800 - 0x5800 6BFF	
RTC2 and Backup reg	AHB1	AHB4 (D3)		NA	0x4000 2800 - 0x4000 2BFF	0x5800 4000 - 0x5800 43FF		NA
Tamp and Backup reg	NA			AHB4 (SRD)	NA			0x5800 4400 - 0x5800 47FF
RTC3	NA		NA		NA		NA	0x5800 4000 - 0x5800 43FF
DAC2								0x5800 3400 - 0x5800 37FF
GFXMMU				AHB3				0x5200 C000 - 0x5200 EFFF
OTFDEC2			AHB3				0x5200 BC00 - 0x5200 BFFF	
OTFDEC1							0x5200 B800 - 0x5200 BBFF	
OTCOSPI I/O manager							0x5200B400 - 0x5200B7FF	
Delay block OCTOSPI2							0x5200 B000 - 0x5200 B3FF	
OCTOSPI2							0x5200 A000 - 0x5200 AFFF	
Delay block OCTOSPI1							0x5200 6000 - 0x5200 63FF	
OCTOSPI1							0x5200 5000 - 0x5200 5FFF	
QUADSPI	AHB3		NA		0xA000 1000 - 0xA000 1FFF	0x5200 5000 - 0x5200 5FFF	NA	

Peripheral	STM32F7 Series devices	STM32H74/75 devices	STM32H72/73 devices	STM32H7A/7B devices	STM32F7 Series devices	STM32H74/75 devices	STM32H72/73 devices	STM32H7A/7B devices
	Bus				Base address			
BDMA1	NA			AHB2	NA			0x48022C00 - 0x48022FFF
HSEM	NA	AHB4			NA	0x58026400 - 0x580267FF		0x48020800 - 0x4802 0BFF
PSSI	NA		AHB2		NA		0x48020400 - 0x4802 07FF	
CRC	AHB1	AHB4 (D3)		AHB1	0x4002 3000 - 0x4002 33FF	0x5802 4C00 - 0x5802 4FFF		0x4002 3000 - 0x4002 33FF
DFSDM1	APB2				0x4001 7400 - 0x4001 77FF	0x4001 7000 - 0x4001 73FF		0x4001 7800 - 0x4001 7FFF
USART10	NA		APB2		NA		0x4001 1C00 - 0x4001 1FFF	
UART9							0x4001 1800 - 0x4001 1BFF	

6.3 Flash memory

Table 13 presents the differences of the flash memory interface between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx and devices.

The STM32H7 Series devices instantiate a different flash memory module both in terms of architecture and interface. For more information on programming, erasing and protection of STM32H7 Series devices refer to the corresponding product's reference manual.

Table 13. Flash memory differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

Flash	STM32F7 Series	STM32H74x/75x	STM32H72x/73x	STM32H7A3/7Bx
Mapping	AHB	AXI		
Flash address	• STM32F76xxx/ STM32F77xxx *Flash - AXI* 0x0800 0000 – 0x081F FFFF • STM32F746xx/ STM32F756xx *Flash - AXI* 0x0800 0000 – 0x080F FFFF	• Flash bank 1 0x0800 0000 – 0x080F FFFF • Flash bank 2 0x0810 0000 – 0x081F FFF	• Flash bank 1 0x0800 0000 – 0x080F FFFF	• Flash bank 1 0x0800 0000 – 0x080F FFFF • Flash bank 2 0x0810 0000 – 0x081F FFF
	• STM32F76xxx/ STM32F77xxx *Flash – ITCM* 0x0020 0000 – 0x003F FFFF • STM32F746xx/ STM32F756xx *Flash – ITCM* 0x0020 0000 – 0x002FF FFFF	NA		
Main / program memory	• STM32F76xxx/ STM32F77xxx – Up to 2 Mbytes (single/dual bank) – Single bank: up to 256-Kbyte sector size – Dual bank: up to 128-Kbyte sector size	Up to 2 Mbytes (dual bank) 128-Kbyte size sector	Up to 1 Mbyte (single bank) 128-Kbyte size sector	Up to 2 Mbytes (dual bank) 8-Kbyte size sector

<table>
<tr><th>Flash</th><th>STM32F7 Series</th><th>STM32H74x/75x</th><th>STM32H72x/73x</th><th>STM32H7A3/7Bx</th></tr>
<tr><td rowspan="2">Main / program memory</td><td>• STM32F746xx/ STM327F56xx
– Up to 1 Mbyte (single bank)
– Up to 256-Kbyte sector size</td><td></td><td></td><td></td></tr>
<tr><td>Programming granularity: 64 bits
Flash line width: 256 bits or 128 bits</td><td colspan="2">Programming granularity: 256 bits
Flash line width: 256 bits</td><td>Programming granularity: 128 bits
Flash line width: 128 bits</td></tr>
<tr><td>Wait state</td><td>Up to 9 (depending on the supply voltage and frequency)</td><td colspan="2">Up to 4 (depending on the core voltage and frequency)</td><td>Up to 6 (depending on the core voltage and frequency)</td></tr>
<tr><td>Option bytes</td><td>32 bytes</td><td colspan="3">2 Kbytes</td></tr>
<tr><td>OTP</td><td>1024 bytes</td><td colspan="2">NA</td><td>1024 bytes</td></tr>
<tr><td>Features</td><td>STM32F76xxx/STM32F77xxx
• Read while write (RWW)
• Supports dual boot mode
• Sector, mass erase and bank mass erase (only in Dual-bank mode)</td><td colspan="3">• Error code correction (ECC)
• Double-word, word, half-word and byte read / write operations
• Sector erase, bank erase and mass erase
• Dual-bank organization supporting simultaneous operations: two read/program/erase operations can be executed in parallel on the two banks
• Bank swapping: the address mapping of the user flash memory of each bank can be swapped.</td></tr>
<tr><td rowspan="3">Protection mechanisms</td><td colspan="4">Readout protection (RDP)</td></tr>
<tr><td rowspan="2">NA</td><td colspan="3">• 1 PCROP protection area per bank (execute-only memory)
• 1 secure area in user flash memory per bank</td></tr>
<tr><td colspan="2">Sector write protection
128-Kbyte sectors</td><td>Sector write protection
32-Kbyte sectors</td></tr>
</table>

6.4 Nested vectored interrupt controllers (NVIC)

The table below presents the interrupt vector differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 14. Interrupt vector differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

<table>
<tr><th>Position</th><th>STM32F7 Series</th><th>STM32H74x/75x</th><th>STM32H72x/73x</th><th>STM32H7A3/7Bx</th></tr>
<tr><td>2</td><td>NA</td><td colspan="3">RTC_TAMP_STAMP_CSS_LSE</td></tr>
<tr><td>18</td><td>ADC</td><td colspan="3">ADC1_2</td></tr>
<tr><td>19</td><td>CAN1_TX</td><td colspan="3">FDCAN1_IT0</td></tr>
<tr><td>20</td><td>CAN1_RX0</td><td colspan="3">FDCAN2_IT0</td></tr>
<tr><td>21</td><td>CAN1_RX1</td><td colspan="3">FDCAN1_IT1</td></tr>
<tr><td>22</td><td>CAN1_SCE</td><td colspan="3">FDCAN2_IT1</td></tr>
<tr><td>24</td><td>TIM1_BRK_TIM9</td><td colspan="3">TIM1_BRK</td></tr>
<tr><td>25</td><td>TIM1_UP_TIM10</td><td colspan="3">TIM1_UP</td></tr>
<tr><td>26</td><td>TIM1_TRG_COM_TIM11</td><td colspan="3">TIM1_TRG_COM</td></tr>
<tr><td>42</td><td>OTG_FS WKUP</td><td>OTG_FS WKUP</td><td>Reserved</td><td>DFSDM2</td></tr>
<tr><td>61</td><td>ETH</td><td colspan="2">ETH</td><td>Reserved</td></tr>
<tr><td>62</td><td>ETH_WKUP</td><td>ETH_WKUP</td><td>ETH_WKUP</td><td>Reserved</td></tr>
</table>

Position	STM32F7 Series	STM32H74x/75x	STM32H72x/73x	STM32H7A3/7Bx
63	CAN2_TX	FDCAN_CAL		
64	CAN2_TX	Reserved		DFSDM1_FLT4 (filter 4)
65	CAN2_RX1	Reserved		DFSDM1_FLT5 (filter 5)
66	CAN2_SCE	Reserved		DFSDM1_FLT6 (filter 6)
67	OTG_FS	Reserved		DFSDM1_FLT7 (filter 7)
81	-	FPU		
92	QUADSPI	QUADSPI	OCTOSPI	
97	Reserved	SPDIFRX		
98	DSIHOST	OTG_FS_EP1_OUT	Reserved	
99	DFSDM1_FLT1	OTG_FS_EP1_IN	Reserved	
100	DFSDM1_FLT2	OTG_FS_WKUP	Reserved	
101	DFSDM1_FLT3	OTG_FS	Reserved	
102	DFSDM1_FLT4	DMAMUX1_OV		
103	SDMMC2	HRTIM1_MST	Reserved	
104	CAN3_TX	HRTIM1_TIMA	Reserved	
105	CAN3_RX0	HRTIM_TIMB	Reserved	
106	CAN3_RX1	HRTIM1_TIMC	Reserved	
107	CAN3_SCE	HRTIM1_TIMD	Reserved	
108	JPEG	HRTIM_TIME	Reserved	
109	MDIOS	HRTIM1_FLT	Reserved	
110	NA	DFSDM1_FLT0 (filter 0)		
111		DFSDM1_FLT1 (filter 1)		
112		DFSDM1_FLT2 (filter 2)		
113		DFSDM1_FLT3 (filter 3)		
114	NA	SAI3	Reserved	
115	NA	SWPMI1		
116		TIM15		
117		TIM16		
118		TIM17		
119		MDIO_WKUP		
120		MDIO		
121		JPEG	NA	JPEG
122		MDMA		
123	NA	DSI/DSI_WKUP	Reserved	
124	NA	SDMMC2		
125		HSEM0		
127	NA	ADC3		DAC2
128	NA	DMAMUX2_OVR		
129		BDMA_CH1		
130		BDMA_CH2		
131		BDMA_CH3		

Position	STM32F7 Series	STM32H74x/75x	STM32H72x/73x	STM32H7A3/7Bx
132	NA	BDMA_CH4		
133		BDMA_CH5		
134		BDMA_CH6		
135		BDMA_CH7		
136		BDMA_CH8		
137		COMP		
138		LPTIM2		
139		LPTIM3		
140	NA	LPTIM4		UART9
141		LPTIM5		USART10
142	NA	LPUART1		
143	NA	WWDG1_RST	Reserved	
144	NA	CRS		
145		ECC		
146	NA	SAI4		Reserved
147		Reserved	TEMP_IT	
148		Reserved	Reserved	
149	NA	WKUP		
150	NA		OCTOSPI2	
151			OTFDEC1	
152			OTFDEC2	
153			FMAC	GFXMUX
154			CORDIC	BDMA1
155			UART9	NA
156			USART10	
157			I2C5_EV	
158			I2C5_ER	
159			FDCAN3_IT0	
160			FDCAN3_IT1	
161			TIM23	
162			TIM24	

6.5 Extended interrupt and event controller (EXTI)

6.5.1 EXTI main features in STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

The extended interrupt and event controller (EXTI) manages wakeup through configurable and direct event inputs. It provides wakeup requests to the power control, it generates interrupt requests to the CPU NVIC and to the D3/SRD domain DMAMUX2. It also generates events to the CPU event input.

The asynchronous event inputs are classified in two groups:

- Configurable events (active edge selection, dedicated pending flag, triggerable by software)

- Direct events (interrupt and wakeup sources from other peripherals, requiring to be cleared in the peripheral) with the following features:
  - Fixed rising edge active trigger
  - No interrupt pending status register bit in the EXTI (the interrupt pending status is provided by the peripheral generating the event)
  - Individual interrupt and event generation mask
  - No SW trigger possibility
  - Direct system SRD domain wakeup events, that have a SRD pending mask and status register and may have a SRD interrupt signal

The table below describes the difference of EXTI event input types between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

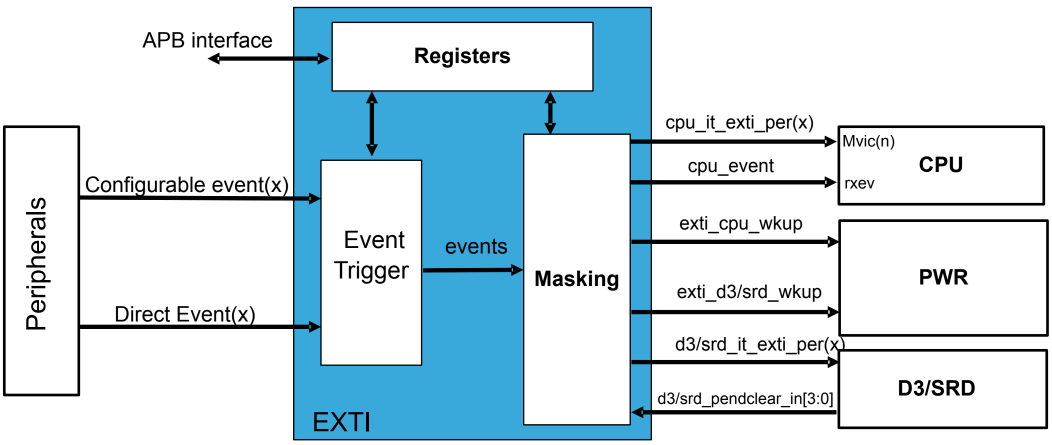
Table 15. EXTI event input types differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

Main features	STM32F7 Series	STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx
Configurable events	Available	Available
Direct events	-	Available

6.5.2 EXTI block diagram in STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

As shown in Figure 9, the EXTI consists of a register block accessed via an APB interface, an event input trigger block, and a masking block. The register block contains all the EXTI registers. The event input trigger block provides an event input edge triggering logic.

Figure 9. EXTI block diagram on STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices



Note: For more details about EXTI functional description and registers description, refer to RM0455.

The table below presents the EXTI line differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 16. EXTI line differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

EXTI line	STM32F7 Series	STM32H74x/75x	STM32H72x/73x	STM32H7A3/7Bx	Event input type
		Source	Source	Source	
0 - 15	EXTI[15:0]	EXTI[15:0]			Configurable
16	PVD output	PVD and AVD			Configurable
17	RTC alarm event	RTC alarms			Configurable

EXTI line	STM32F7 Series	STM32H74x/75x	STM32H72x/73x	STM32H7A3/7Bx	Event input type
		Source	Source	Source	
18	USB OTG FS wakeup event	RTC tamper, RTC timestamp, RCC LSECSS			Configurable
19	Ethernet wakeup event	RTC wakeup timer			Configurable
20	USB OTG HS (configured in FS) wakeup event	COMP1			Configurable
21	RTC tamper and time stamp events	COMP2			Configurable
22	RTC wakeup event	I2C1 wakeup			Direct
23	LPTIM1 asynchronous event	I2C2 wakeup			Direct
24	MDIO slave asynchronous interrupt	I2C3 wakeup			Direct
25	NA	I2C4 wakeup			Direct
26		USART1 wakeup			Direct
27		USART2 wakeup			Direct
28		USART3 wakeup			Direct
29		USART6 wakeup			Direct
30		UART4 wakeup			Direct
31		UART5 wakeup			Direct
32		UART7 wakeup			Direct
33		UART8 wakeup			Direct
34	NA	LPUART1 RX wakeup			Direct
35		LPUART1 TX wakeup			Direct
36	NA	SPI1 wakeup			Direct
37		SPI2 wakeup			Direct
38		SPI3 wakeup			Direct
39		SPI4 wakeup			Direct
40		SPI5 wakeup			Direct
41		SPI6 wakeup			Direct
42		MDIO wakeup			Direct
43		USB1 wakeup			Direct
44	NA	USB2 wakeup		Reserved	Direct
47	NA	LPTIM1 wakeup			Direct
48		LPTIM2 wakeup			Direct
49		LPTIM2 output			Configurable
50		LPTIM3 wakeup			Direct
51		LPTIM3 output			Configurable
52	NA	LPTIM4 wakeup		UART9 wakeup	Direct
53		LPTIM5 wakeup		USART10 wakeup	Direct
54	NA	SWPMI wakeup			Direct
55		WKUP1			Direct
56		WKUP2			Direct
57		WKUP3	Reserved	WKUP3	Direct

<table>
<tr><th rowspan="2">EXTI line</th><th rowspan="2">STM32F7 Series</th><th>STM32H74x/75x</th><th>STM32H72x/73x</th><th>STM32H7A3/7Bx</th><th rowspan="2">Event input type</th></tr>
<tr><th>Source</th><th>Source</th><th>Source</th></tr>
<tr><td>58</td><td rowspan="8">NA</td><td colspan="3">WKUP4</td><td>Direct</td></tr>
<tr><td>59</td><td>WKUP5</td><td>Reserved</td><td>WKUP5</td><td>Direct</td></tr>
<tr><td>60</td><td colspan="3">WKUP6</td><td>Direct</td></tr>
<tr><td>61</td><td colspan="3">RCC interrupt</td><td>Direct</td></tr>
<tr><td>62</td><td colspan="3">I2C4 Event interrupt</td><td>Direct</td></tr>
<tr><td>63</td><td colspan="3">I2C4 Error interrupt</td><td>Direct</td></tr>
<tr><td>64</td><td colspan="3">LPUART1 global Interrupt</td><td>Direct</td></tr>
<tr><td>65</td><td colspan="3">SPI6 interrupt</td><td>Direct</td></tr>
<tr><td>66</td><td rowspan="8">NA</td><td colspan="2">BDMA CH0 interrupt</td><td>BDMA2 CH0 interrupt</td><td>Direct</td></tr>
<tr><td>67</td><td colspan="2">BDMA CH1 interrupt</td><td>BDMA2 CH1 interrupt</td><td>Direct</td></tr>
<tr><td>68</td><td colspan="2">BDMA CH2 interrupt</td><td>BDMA2 CH2 interrupt</td><td>Direct</td></tr>
<tr><td>69</td><td colspan="2">BDMA CH3 interrupt</td><td>BDMA2 CH3 interrupt</td><td>Direct</td></tr>
<tr><td>70</td><td colspan="2">BDMA CH4 interrupt</td><td>BDMA2 CH4 interrupt</td><td>Direct</td></tr>
<tr><td>71</td><td colspan="2">BDMA CH5 interrupt</td><td>BDMA2 CH5 interrupt</td><td>Direct</td></tr>
<tr><td>72</td><td colspan="2">BDMA CH6 interrupt</td><td>BDMA2 CH6 interrupt</td><td>Direct</td></tr>
<tr><td>73</td><td colspan="2">BDMA CH7 interrupt</td><td>BDMA2 CH7 interrupt</td><td>Direct</td></tr>
<tr><td>74</td><td>NA</td><td colspan="3">DMAMUX2 interrupt</td><td>Direct</td></tr>
<tr><td>75</td><td rowspan="3">NA</td><td colspan="2">ADC3 interrupt</td><td>Reserved</td><td>Direct</td></tr>
<tr><td>76</td><td colspan="2">SAI4 interrupt</td><td>Reserved</td><td>Direct</td></tr>
<tr><td>77</td><td>NA</td><td>HSEM0</td><td>NA</td><td>-</td></tr>
<tr><td>85</td><td>NA</td><td colspan="3">HDMICEC wakeup</td><td>Configurable</td></tr>
<tr><td>86</td><td>NA</td><td>ETHERNET wakeup</td><td>ETH_ASYNC_IT</td><td>Reserved</td><td>Configurable</td></tr>
<tr><td>87</td><td>NA</td><td colspan="3">HSECSS interrupt</td><td>Direct</td></tr>
<tr><td>88</td><td>NA</td><td>Reserved</td><td colspan="2">TEMP wakeup</td><td>Direct</td></tr>
<tr><td>89</td><td colspan="2" rowspan="3">NA</td><td>UART9 wakeup</td><td>NA</td><td>-</td></tr>
<tr><td>90</td><td>USART10 wakeup</td><td>NA</td><td>-</td></tr>
<tr><td>91</td><td>I2C5 wakeup</td><td>NA</td><td>-</td></tr>
</table>

Note: For more details about EXTI events input mapping, refer to EXTI event input mapping section of RM0433, RM0468 and RM0455 reference manuals.

6.6 Reset and clock control (RCC)

6.6.1 Clock management

The table below presents the source clock differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 17. **Different source clock in STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices**

Source clock		STM32F7 Series	STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx
Internal oscillators	HSI	16 MHz	8/16/32/64 MHz
	HSI48	NA	48 MHz
	CSI	NA	4 MHz
	LSI	32 kHz	32 kHz
External oscillators	HSE	4-26 MHz	4-50 MHz
	LSE	32.768 kHz	
PLLs(1)		x3 without fractional mode	x3 with fractional mode (13-bit fractional multiplication factor)

1. *Special care to be taken for the PLL configuration:*
   - *STM32H72x/73x and STM32H74x/75x: the PLL VCO max frequency is 836 MHz*
   - *STM32H7A3/7Bx: the PLL VCO max frequency is 560 MHz*

6.6.2 Peripheral clock distribution

The peripheral clocks are the clocks provided by the RCC to the peripherals. Two kinds of clocks are available:

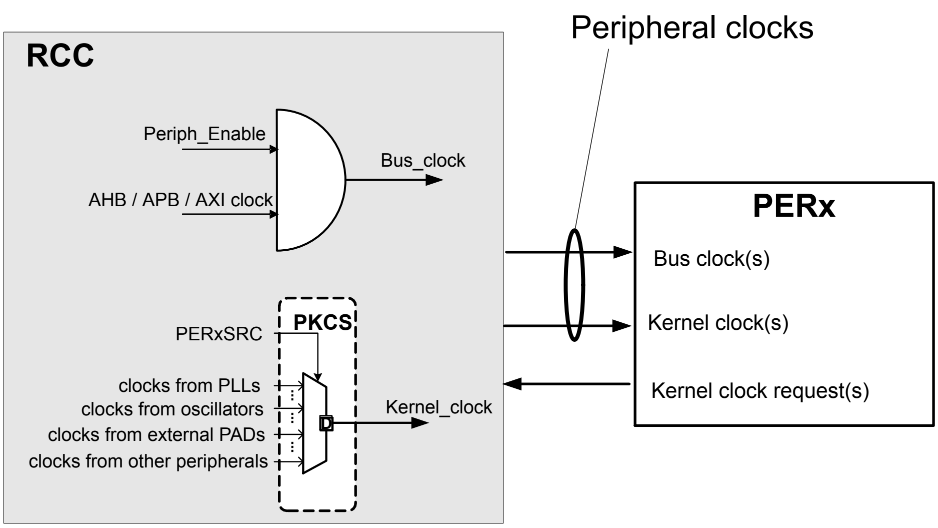
- The bus interface clocks
- The kernel clocks

On STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices, the peripherals generally receive:

- One or several bus clocks.
- One or several kernel clocks.

Figure 10 describes the peripheral clock distribution on STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Figure 10. **Peripheral clock distribution on STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices**



The following table describes an example of peripheral clock distribution for STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

For more details about the kernel peripheral clock distribution, refer to Kernel clock distribution overview table of RM0455, RM0468 and RM0433 reference manuals.

Table 18. Peripheral clock distribution example

Peripheral	STM32F7 Series	STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx
SPI1	**APB2_Clock**	• Bus clock APB2_Clock • Kernel clock Pll1_q_ck/Pll2_p_ck/Pll3_p_ck/I2S_CKIN/ Per_ck
USART1	• Bus clock APB2_Clock • Kernel clock – LSE – HSI – SYSCLK – PCLK2	• Bus clock APB2_Clock • Kernel clock Pll2_q_ck/pll3_q_ck/hsi_ker_ck/csi_ker_ck/lse_ck

6.7 Operating conditions

The table below illustrates the maximum operating frequency of STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 19. General operating conditions for STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

Scale	STM32F7 Series devices maximum frequency	STM32H74x/75x devices maximum frequency		STM32H72x/73x devices maximum frequency		STM32H7A3/7Bx devices maximum frequency		Unit
		Max CPU	Max D1/D2/D3	Max CPU	Max D1/D2/D3	Max CPU	Max CD/SRD	
Scale 0	NA	480	240	550	275	280	280	MHz
Scale 1	216	400	200	400	200	225	225	
Scale 2	180	300	160	300	150	160	160	
Scale 3	144	200	88	170	85	88	88	

7 Power (PWR)

The table below presents the PWR controller differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices. Both dynamic and static power-consumption had been optimized for the STM32H7A3/7Bx devices.

Table 20. PWR differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

PWR		STM32F7 Series	STM32H72x/73x and STM32H74x/75x	STM32H7A3/7Bx
Low-power modes	Autonomous mode (basic operation with inactive CPU domain(s) in low-power mode)	NA	D3 in Run mode	SRD in Run mode
			D1/D2 in DStop	CD in DStop
			NA	CD in DStop with RAM Shut-off[1]
			D1/D2 in DStandby	NA
			NA	CD in DStop2 (retention mode) with/without RAM Shuf-off[1]
	Stop	Stop	D3 in DStop	SRD in DStop
			D1/D2 in DStop	CD in DStop
		NA	NA	CD in DStop with RAM Shut-off[1]
			D1/D2 in DStandby	NA
			NA	CD in DStop2 (retention mode) with/without RAM Shuf-off[1]
Power supplies	External power supply for I/Os	VDD = 1.7 to 3.6 V	VDD = 1.62 to 3.6 V	
	Internal regulator (LDO) supplying VCORE	VDD = 1.7 to 3.6 V	VDDLDO = 1.62 to 3.6 V	
	Step-down converter (SMPS) supplying VCORE	NA	VDDSMPS = 1.62 to 3.6 V	
	External analog power supply	VDDA = 1.7 to 3.6 V VREF-	VDDA = 1.8 to 3.6 V VREF-	
		VREF+: a separate reference voltage, available on VREF+ pin for ADC and DAC	VREF+: a separate reference voltage, available on VREF+ pin for ADC and DAC When enabled by ENVR bit in the VREFBUF control status and status register[2], VREF+ is provided from the internal voltage reference buffer	
	USB power supply	VDD33USB = 3.0 to 3.6 V	VDD33USB = 3.0 to 3.6 V VDD50USB = 4.0 to 5.5 V	
	Backup domain	VBAT = 1.65 to 3.6 V	VBAT = 1.2 to 3.6 V	
	Independent power supply	VDDSDMMC = 1.7 to 3.6 V VDDDSI = 1.7 to 3.6 V	NA NA	VDDMMC = 1.62 to 3.6 V NA
	VCORE supplies	1.08 V ≤ VCAP_1 and VCAP_2 ≤ 1.40 V	0.7 V ≤ VCAP ≤ 1.35 V	1.0 V ≤ VCAP ≤ 1.3V

<table>
<tr><th colspan="3">PWR</th><th>STM32F7 Series</th><th>STM32H72x/73x and STM32H74x/75x</th><th>STM32H7A3/7Bx</th></tr>
<tr><td rowspan="4">Power supplies</td><td rowspan="4">Reg bypass: must be supplied from external regulator on VCAP pins</td><td>VOS0</td><td>NA</td><td>1.35 V</td><td>1.3 V</td></tr>
<tr><td>VOS1</td><td>1.32 V</td><td colspan="2">1.2 V</td></tr>
<tr><td>VOS2</td><td>1.26 V</td><td colspan="2">1.1 V</td></tr>
<tr><td>VOS3</td><td>1.14 V</td><td colspan="2">1.00 V</td></tr>
<tr><td colspan="3">Peripheral supply regulation</td><td>DSI voltage regulator</td><td colspan="2">USB regulator</td></tr>
<tr><td colspan="3" rowspan="2">Power supply supervision</td><td colspan="3">POR/PDR monitor
BOR monitor
PVD monitor</td></tr>
<tr><td>NA</td><td colspan="2">AVD monitor(3)
VBAT thresholds(4)
Temperature thresholds(5)</td></tr>
</table>

1. *To further optimize the power consumption, the unused RAMs can be Shut-off with the consequence of their content being lost (refer to RM0455).*
2. *For more details about VREFBUF see Voltage reference buffer (VREFBUF) section of RM0433, RM0468 and RM0455 reference manuals.*
3. *Analog voltage detector (AVD): to monitor the VDDA supply by comparing it to a threshold selected by the ALS[1:0] bits in the PWR_CR1 register. The AVD is enabled by setting the AVDEN bit in the PWR_CR1 register.*
4. *Battery voltage thresholds (VBAT thresholds): indicate if VBAT is higher or lower than the threshold. The VBAT supply monitoring (available only in VBAT mode) can be enabled/disabled via MONEN bit in the PWR_CR2 register.*
5. *Temperature thresholds: the temperature monitoring can be enabled/disabled via MONEN bit in the PWR_CR2 register. It indicates whether the device temperature is higher or lower than the threshold.*

8 System configuration controller (SYSCFG)

The table below illustrates the SYSCFG main differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 21. SYSCFG main features differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

<table>
<tr><th>-</th><th>STM32F7 Series</th><th>STM32H74x/75x</th><th>STM32H72x/73x</th><th>STM32H7A3/7Bx</th></tr>
<tr><td rowspan="6">SYSCFG</td><td>Remap the memory areas
Manage Class B feature</td><td colspan="3">NA</td></tr>
<tr><td colspan="3">Select the Ethernet PHY interface</td><td>NA</td></tr>
<tr><td colspan="4">Manage the external interrupt line connection to the GPIOs
Manage I/O compensation cell feature
I2C Fast mode + configuration</td></tr>
<tr><td>NA</td><td colspan="3">Analog switch configuration management</td></tr>
<tr><td>NA</td><td colspan="2">Get readout protection and flash memory bank swap informations
Management of boot sequences and boot addresses
Get BOR reset level
Get flash memory secured and protected sector status
Get flash memory write protections status
Get DTCM secured section status
Get independent watchdog behavior (hardware or software / freeze)
Reset generation in Stop and Standby mode
Get secure mode enabling/disabling</td><td>Not part of the system controller
Features are part of the flash memory registers</td></tr>
<tr><td colspan="2">NA</td><td>Management of timer break input lock
Control CPU frequency boost</td><td>NA</td></tr>
</table>

Note: For more details, refer to the SYSCFG register description section of RM0433, RM0468 and RM0455 reference manuals.

9 Secure digital input/output and MultiMediaCard interface (SDMMC)

The following table presents the differences between the SDMMC interface of STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 22. **SDMMC differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices**

SDMMC	STM32F7 Series	STM32H72x/73x and STM32H74x/75x	STM32H7A3/7Bx
Features	Full compliance with MultiMediaCard system specification version 4.2. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit	Full compliance with MultiMediaCard system specification version 4.51. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit	
	Full compliance with SD memory card specifications version 2.0	Full compliance with SD memory card specifications version 4.1.	
	Full compliance with SD I/O card specification version 2.0. Card support for two different databus modes: 1-bit (default) and 4-bit	Full compliance with SDIO card specification version 4.0. Card support for two different databus modes: 1-bit (default) and 4-bit.	
	Data transfer up to 200 Mbyte/s for the 8-bit mode.	Data transfer up to 208 Mbyte/s for the 8-bit mode.(1)	
	NA	SDMMC IDMA: is used to provide high speed transfer between the SDMMC FIFO and the memory. The AHB master optimizes the bandwidth of the system bus. The SDMMC internal DMA (IDMA) provides one channel to be used either for transmit or receive.	
	Independent power supply for SDMMC2	NA	Independent power supply for SDMMC2

1. *Depending of the maximum allowed IO speed. for more details refer to datasheets.*

10 Universal (synchronous) asynchronous receiver-transmitter (U(S)ART)

The STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices implement several new features on the U(S)ART compared to the STM32F7 Series devices. The following table shows the U(S)ART differences.

Table 23. U(S)ART differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

<table>
<tr><th>U(S)ART</th><th>STM32F7 Series</th><th>STM32H74x/75x3</th><th>STM32H72x/73x and STM32H7A3/7Bx</th></tr>
<tr><td>Instances</td><td>x4 USART
x4 UART</td><td>x4 USART
x4 UART
x1 LPUART</td><td>x5 USART
x5 UART
x1 LPUART</td></tr>
<tr><td>Clock</td><td colspan="3">Dual clock domain with dedicated kernel clock for peripherals independent from PCLK</td></tr>
<tr><td>Wakeup</td><td rowspan="2">NA</td><td colspan="2">Wakeup from low-power mode</td></tr>
<tr><td>Features</td><td colspan="2">SPI slave transmission, underrun flag
Two internal FIFOs for transmit and receive data
Each FIFO can be enabled/disabled by software and come with a status flag.</td></tr>
</table>

11 Serial peripheral interface (SPI)

The STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices implement some enhanced SPI compared to the STM32F7 Series devices. See the table below for the SPI differences.

Table 24. SPI differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

<table>
<tr><th>SPI</th><th>STM32F7 Series</th><th>STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx</th></tr>
<tr><td>Instances</td><td>x4</td><td>x6</td></tr>
<tr><td>Clock</td><td>Single clock domain</td><td>Dual clock domain with dedicated kernel and serial interface clock independent from PCLK with transmission and reception capability at low-power stop</td></tr>
<tr><td>Wakeup</td><td>NA</td><td>Wakeup from low-power mode</td></tr>
<tr><td rowspan="2">Features</td><td colspan="2">• Full-duplex synchronous transfers on three lines (with two separated data lines)
• Half-duplex synchronous transfer on two lines (with single bidirectional data line)
• Simplex synchronous transfers on two lines (with unidirectional data line)
• 8 master mode baud rate prescalers up to fPCLK/2
• Slave mode frequency up to fPCLK/2
• NSS management by hardware or software for both master and slave
• Master and slave capability, multi-master multi-slave support
• Programmable clock polarity and phase
• Programmable data order with MSB-first or LSB-first shifting
• Dedicated transmission, reception and error flags with interrupt capability
• SPI Motorola and TI formats support
• Hardware CRC feature for reliable communication (at the end of transaction):
– Configurable size and polynomial
– Autommatic CRC upend in Tx mode
– Automatic CRC check in Rx mode
– Configurable RxFIFO threshold, data packeting support
• Configurable data size (4-32 bit)</td></tr>
<tr><td>• Two 32-bit embedded Rx and Tx FIFOs with DMA capability
• CRC pattern size 8 or 16 bit
• RxFIFO threshold 8 or 16 bit</td><td>• Protection of configuration and setting
• Adjustable minimum delays between data and between SS and data flow at master
Configurable SS signal polarity and timing, MISO x MOSI swap capability
• Programmable number of data within a transaction to control SS and CRC
Two 16x or 8x 8-bit embedded Rx and TxFIFOs with DMA capability
• Programmable number of data in transaction
Configurable behavior at slave underrun condition (support of cascaded circular buffers)
• Master automatic suspend at receive mode
Master start/suspend control
• Alternate function control of associated GPIOs
Selected status and error flags with wake up capability
• CRC pattern size configurable from 4 to 32 bit
Configurable CRC polynomial length
• RxFIFO threshold from 1 to 16 data</td></tr>
</table>

12 Integrated interchip sound interface (I2S)

The table below presents the I2S differences between the STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 25. I2S differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

I2S	STM32F7 Series	STM32H74x/75x3	STM32H72x/73x and STM32H7A3/7Bx
Features	x3	x3	x4
	Full duplex only when the extension module is implemented	Full duplex native	
	Minimum allowed value = 4	More flexible clock generator (division by 1,2 are possible)	
	Sampling edge is not programmable	Programmable sampling edge for the bit clock	
	Frame sync polarity cannot be selected	Programmable frame sync polarity	
	Receive buffer accessible in half-word	Receive buffer accessible in half-word and words	
	Data are right aligned into the receive buffer	Various data arrangement available into the receive buffer	
	Error flags signaling for underrun, overrun and frame error	Error flags signaling for underrun, overrun and frame error	
	NA	Improved reliability: automatic resynchronization to the frame sync in case of frame error	
		Improved reliability: re-alignement of left and right samples in case of underrun or overrun situation	
		MSb/LSb possible in the serial data interface	
	16 or 32 bits channel length in master	16 or 32 bits channel length in master	
	16 or 32 bits channel length in slave	Any channel length in slave	
	NA	Embedded RX and TX FIFOs	
	DMA capabilities (16-bit wide)	DMA capabilities (16-bit and 32-bit wide)	

13 Flexible memory controller (FMC)

The table below presents the FMC differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 26. **FMC differences between STM32F7 Series devices, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices**

FMC	STM32F7 Series	STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx
Mapping	AHB	AXI
Clock	Single clock domain	Dual clock domain with dedicated kernel clock for peripherals independent from AXI clock
Bank remap	SYSCFG_MEMRMP register FMC bank mapping can be configured by software through the SWP_FMC[1:0] bits.	FMC_BCR1 register FMC bank mapping can be configured by software through the BMAP[1:0] bits. See Figure 11 and Figure 12.
Features	NA	FMCEN bit: FMC controller Enable bit added in the FMC_BCR1 register. To modify some parameters while FMC is enabled follow the below sequence: 1. First disable the FMC controller to prevent any further accesses to any memory controller during register modification. 2. Update all required configurations. 3. Enable the FMC controller again. When the SDRAM controller is used, if the SDCLK clock ratio or refresh rate has to be modified after initialization phase, the following procedure must be followed. 1. Put the SDRAM device in Self-refresh mode. 2. Disable the FMC controller by resetting the FMCEN bit in the FMC_BCR1 register. 3. Update the required parameters. 4. Enable the FMC controller once all parameters are updated. 5. Then, send the clock configuration enable command to exit Self-fresh mode.

Figure 11. **FMC bank address mapping on STM32H7A3/7Bx and STM32H72x/73x devices**

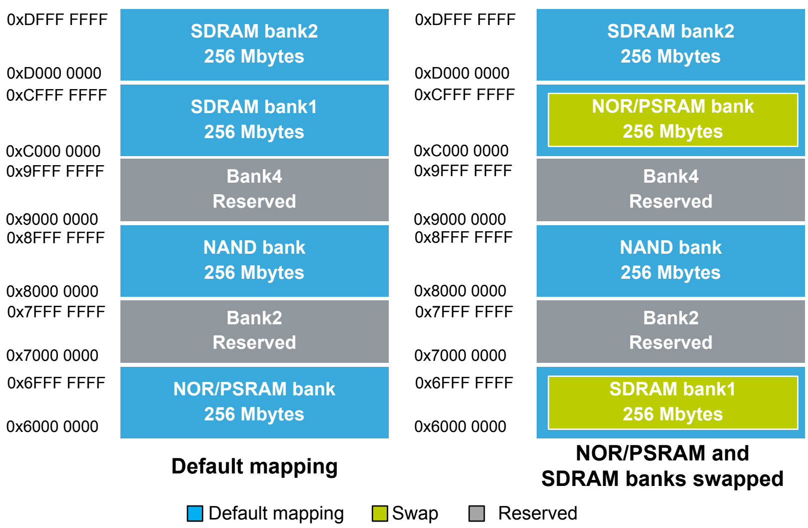
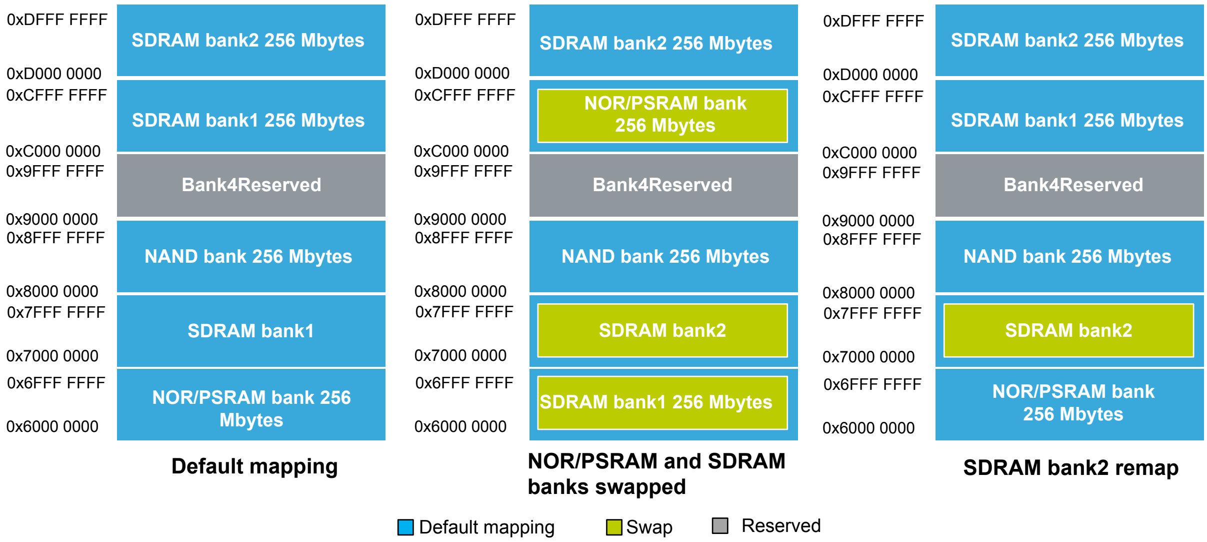


Figure 12. FMC bank address mapping on STM32H74x/75x devices



14 Analog-to-digital converters (ADC)

The following table presents the differences between the ADC peripheral of the STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 27. ADC differences between STM32F7 Series,STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

ADC	STM32F7 Series	STM32H74x/75x	STM32H72x/73x	STM32H7A3/7Bx
Instances	x3	x3		x2
Clock	Single clock domain	Dual clock domain with dedicated kernel clock for peripherals independent from CLK or HCLK		
Number of channels	Up to 24 channels	Up to 20 channels		
Resolution	12, 10, 8 or 6-bit	16, 14, 12, 10 or 8-bit	16, 14, 12, 10 or 8-bit for ADC1 and ADC2 12, 10, 8 or 6-bit for ADC3	16, 14, 12, 10 or 8-bit
Conversion modes	• Single • Continuous • Scan • Discontinuous • Dual and triple mode			
DMA	Yes			
New features	NA	Input voltage reference from VREF+ pin or internal VREFBUF reference ADC conversion time is independent from the AHB bus clock frequency Self-calibration (both offset and the linearity) Low-power features Three analog watchdogs per ADC Internal dedicated channels: the internal DAC1 channel 1 and channel 2 are connected to ADC2 Oversampler: • 32-bit data register • Oversampling ratio adjustable from 2 to 1024 • Programmable data right and left shift Data can be routed to DFSDM for post processing		
	NA	All the internal references (VBAT, VREFINT, VSENSE) are connected to ADC3	Internal references VBAT, VREFINT are connected to ADC3 and ADC2 VSENSE is connected to ADC3	All the internal references (VBAT, VREFINT, VSENSE) are connected to ADC2 The internal DAC2 channel 1 is connected to ADC2 One additional DAC for STM32H7A3/7B0/7B3 devices

The following two tables present the differences of external trigger for regular channels and injected channels between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 28. External trigger for regular channel differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

Type	EXTSEL[3:0] STM32F7 Series devices	EXTSEL[4:0] STM32H7 Series	ADC			
			STM32F7 Series	STM32H74x/75x	STM32H72x/73x	STM32H7A3/7Bx
Internal signal from on-chip timers	0000	00000	TIM1_CC1 event			
	0001	00001	TIM1_CC2 event			
	0010	00010	TIM1_CC3 event			
	0011	00011	TIM2_CC2 event			
	0100	00100	TIM5_TRGO event	TIM3_TRGO event		
	0101	00101	TIM4_CC4 event			
	0110	00110	TIM3_CC4	EXTI line 11		
	0111	00111	TIM8_TRGO event			
	1000	01000	TIM8_TRGO(2) event			
	1001	01001	TIM1_TRGO event			
	1010	01010	TIM1_TRGO(2) event			
	1011	01011	TIM2_TRGO event			
	1100	01100	TIM4_TRGO event			
	1101	01101	TIM6_TRGO event			
	NA	01110	EXTI line11	TIM15_TRGO event		
	1111	01111	NA	TIM3_CC4 event		
	NA	10000		HRTIM1_ADCTRG 1 event	Reserved	
		10001		HRTIM1_ADCTRG 3 event	Reserved	
		10010		LPTIM1_OUT event		
		10011		LPTIM2_OUT event		
		10100		LPTIM3_OUT event		
		10101		NA	TIM23_TRGO event	NA
		10110			TIM24_TRGO event	

Table 29. External trigger for injected channel differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

<table>
<tr><th rowspan="2">Type</th><th rowspan="2">JEXTSEL[3:0]
STM32F7 Series</th><th rowspan="2">JEXTSEL[4:0]
STM32H7 Series</th><th colspan="4">ADC</th></tr>
<tr><th>STM32F7 Series</th><th>STM32H74x/75x</th><th>STM32H72x/73x</th><th>STM32H7A3/7Bx</th></tr>
<tr><td rowspan="22">Internal signal from on-chip timers</td><td>0000</td><td>00000</td><td colspan="4">TIM1_TRGO event</td></tr>
<tr><td>0001</td><td>00001</td><td colspan="4">TIM1_CC4 event</td></tr>
<tr><td>0010</td><td>00010</td><td colspan="4">TIM2_TRGO event</td></tr>
<tr><td>0011</td><td>00011</td><td colspan="4">TIM2_CC1 event</td></tr>
<tr><td>0100</td><td>00100</td><td colspan="4">TIM3_CC4 event</td></tr>
<tr><td>0101</td><td>00101</td><td colspan="4">TIM4_TRGO event</td></tr>
<tr><td>NA</td><td>00110</td><td>NA</td><td colspan="3">EXTI line 15</td></tr>
<tr><td>0111</td><td>00111</td><td colspan="4">TIM8_CC4 event</td></tr>
<tr><td>1000</td><td>01000</td><td colspan="4">TIM1_TRGO(2) event</td></tr>
<tr><td>1001</td><td>01001</td><td colspan="4">TIM8_TRGO event</td></tr>
<tr><td>1010</td><td>01010</td><td colspan="4">TIM8_TRGO(2) event</td></tr>
<tr><td>1011</td><td>01011</td><td colspan="4">TIM3_CC3 event</td></tr>
<tr><td>1100</td><td>01100</td><td colspan="4">TIM3_TRGO event</td></tr>
<tr><td>1101</td><td>01101</td><td colspan="4">TIM3_CC1 event</td></tr>
<tr><td>1110</td><td>01110</td><td colspan="4">TIM6_TRGO event</td></tr>
<tr><td rowspan="8">NA</td><td>01111</td><td rowspan="8">NA</td><td colspan="3">TIM15_TRGO event</td></tr>
<tr><td>10000</td><td>HRTIM1_ADCTRG 2 event</td><td colspan="2">Reserved</td></tr>
<tr><td>10001</td><td>HRTIM1_ADCTRG 4 event</td><td colspan="2">Reserved</td></tr>
<tr><td>10010</td><td colspan="3">LPTIM1_OUT event</td></tr>
<tr><td>10011</td><td colspan="3">LPTIM2_OUT event</td></tr>
<tr><td>10100</td><td colspan="3">LPTIM3_OUT event</td></tr>
<tr><td>10101</td><td rowspan="2">NA</td><td>TIM23_TRGO event</td><td rowspan="2">NA</td></tr>
<tr><td>10110</td><td>TIM24_TRGO event</td></tr>
</table>

15 Digital-to-analog converter (DAC)

The STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices implement some enhanced DAC compared to the STM32F7 Series devices. Refer to the table below for the main DAC differences between them.

Table 30. DAC differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

DAC	STM32F7 Series	STM32H74x/75x	STM32H72x/73x	STM32H7A3/7Bx
Instance	1x One dual channel	1x One dual channel		2x One dual channel One single channel
Clock	Single clock domain	Single clock domain (APB) LSI is used for sample and hold mode		
Features	Input voltage reference, VREF+	Input voltage reference from VREF+ pin or internal VREFBUF reference		
	NA	Buffer offset calibration DAC output connection to on chip peripherals Sample and hold mode for low power operation in Stop mode		

Table 31. DAC1 trigger selection differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

Type	TSEL[2:0] STM32F7 Series	TSEL[3:0] STM32H7 Series	DAC1			
			STM32F7 Series	STM32H74x/75x	STM32H72x/73x	STM32H7A3/7Bx
Internal signal from on-chip timers	000	0000	TIM6_TRGO	SWTRIG		
	001	0001	TIM8_TRGO	TIM1_TRGO		
	010	0010	TIM7_TRGO	TIM2_TRGO		
	011	0011	TIM5_TRGO	TIM4_TRGO		
	100	0100	TIM2_TRGO	TIM5_TRGO		TIM3_TRGO event
	101	0101	TIM4_TRGO	TIM6_TRGO		
	110	0110	EXTI9	TIM7_TRGO		EXTI line 11
	111	0111	SWTRIG	TIM8_TRGO		
	NA	1000	NA	TIM15_TRGO		
		1001		HRTIM1_DACTRG1	Reserved	
		1010		HRTIM1_DACTRG2	Reserved	
		1011		LPTIM1_OUT		
		1100		LPTIM2_OUT		
		1101		EXTI9		
		1110		Reserved	TIM23_TRGO event	LPTIM2_OUT
		1111		Reserved	TIM24_TRGO event	Reserved

Table 32. DAC2 trigger selection new for STM32H7A3/7Bx devices

Type	TSEL[3:0]	DAC2
		STM32H7A3/7B0/7B3 devices
Internal signal from on-chip timers	0000	SWTRIG
	0001	TIM1_TRGO
	0010	TIM2_TRGO
	0011	TIM4_TRGO
	0100	TIM5_TRGO
	0101	TIM6_TRGO
	0110	TIM7_TRGO
	0111	TIM8_TRGO
	1000	TIM15_TRGO
	1001	Reserved
	1010	Reserved
	1011	LPTIM1_OUT
	1100	LPTIM2_OUT
	1101	EXTI9
	1110	LPTIM3_OUT
	1111	Reserved

16 USB on-the-go (USB OTG)

The STM32H72x/73x and STM32H7A3/7Bx devices embed one USB OTG HS/FS instance while the STM32H74x/75x devices and STM32F7 Series devices embed one USB OTG HS/FS instance and one USB OTG FS instance.

The table below summarizes the difference of USB OTG between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 33. USB OTG differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

USB OTG	STM32F7 Series		STM32H74x/75x	STM32H72x/73x and STM32H7A3/7Bx
Instance	FS	HS	x2 HS[(1)]	HS
Device bidirectional endpoints (including EP0)	6	9	9	
Host mode channels	12	16	16	
Size of dedicated SRAM	1.2 Kbytes	4 Kbytes	4 Kbytes	
USB 2.0 link power management (LPM) support	Yes			
OTG revision supported	1.3, 2.0		2.0	
Attach detection protocol (ADP) support	Not supported			
Battery Charging Detection (BCD) support	No		Yes	
ULPI available to primary IOs via, muxing	-	x1	x1	x1
Integrated PHY	x1 FS	x1 FS	x1 FS	x1 FS
DMA availability	Yes			

1. *Both OTG_HS1 and OTG_HS2 can potentially be programmed for HS operation, only one has an accessible ULPI interface which will allow a High Speed operation using an external HS transceiver.*

17 Ethernet (ETH)

The STM32H74x/75x and STM32H72x/73x devices implement several new features on the Ethernet compared to the STM32F7 Series devices.

There is no Ethernet embedded in STM32H7A3/7Bx devices.

Table 34. Ethernet differences between STM32F7 and STM32H7 devices

<table>
<tr><th>Ethernet</th><th>STM32F7 Series</th><th>STM32H74x/75x and STM32H72x/73x lines</th></tr>
<tr><td>Operation modes and PHY support</td><td colspan="2">10/100 Mbps data rate
Full-duplex and half-duplex operations
MII and RMII interface to external PHY</td></tr>
<tr><td>Processing control</td><td>NA</td><td>Multi-layer filtering (Layer 3 and 4, VLAN and MAC filtering)
Double VLAN support (C-VLAN+ S-VLAN)</td></tr>
<tr><td>Offload processing</td><td>NA</td><td>Automatic ARP response
TCP segmentation</td></tr>
<tr><td rowspan="2">Low-power mode</td><td colspan="2">Remote wakeup packet AMD Magic Packet detections</td></tr>
<tr><td>NA</td><td>Energy efficient Ethernet (EEE)</td></tr>
</table>

18 Digital filter for sigma delta modulators (DFSDM)

The STM32H7A3/7Bx devices implement several new features on DFSDM compared to STM32H74x/75x, STM32H72x/73x and STM32F7 Series devices with a DFSDM.

For STM32H7A3/7Bx devices, an additional single filter DFSDM has been included in the APB4 that can run in autonomous mode. The following table shows the DFSDM differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 35. DFSDM differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

DFSDM	STM32F7 Series	STM32H74x/75x and STM32H72x/73x	STM32H7A3/7Bx	
Instance	DFSDM1	DFSDM1	DFSDM1	DFSDM2
Number of channels	8		8	2
Number of filters	4		8	1
Input from ADC	NA	Yes	Yes	NA
Supported trigger sources	12	16		7

The table below presents the DFSDM internal signals differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 36. DFSDM internal signal differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

Name	STM32F7 Series	STM32H74x/75x and STM32H72x/73x	STM32H7A3/7Bx	
Instance	DFSDM1	DFSDM1	DFSDM1	DFSDM2
Internal/ external trigger signal	Refer to the following tables for DFSDM triggers signals connections			
break signal output	Refer to the following tables for DFSDM break signal connections			
DMA request signal	x4 DMA request from DFSDM_FLTx (x =0..3)		x8 DMA request from DFSDM_FLTx (x =0..7)	x1 DMA request
Interrupt request signal	x4 interrupt request from each DFSDM_FLTx (x=0..3)		x8 interrupt request from each DFSDM_FLTx (x=0..7)	x1 interrupt request
ADC input data	NA	dfsdm_dat_adc[15:0]		NA

This table describes the DFSDM triggers connection differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 37. DFSDM trigger connection differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

Trigger name	STM32F7 Series	STM32H74x/75x	STM32H72x/73x	STM32H7A3/7Bx	
Instance	DFSDM1	DFSDM1	DFSDM1	DFSDM1	DFSDM2
DFSDM_JTRG[0]	TIM1_TRGO				Reserved
DFSDM_JTRG[1]	TIM1_TRGO2				
DFSDM_JTRG[2]	TIM8_TRGO				
DFSDM_JTRG[3]	TIM8_TRGO2				
DFSDM_JTRG[4]	TIM3_TRGO				
DFSDM_JTRG[5]	TIM4_TRGO				
DFSDM_JTRG[6]	TIM10_OC1	TIM16_OC1			
DFSDM_JTRG[7]	TIM6_TRGO				
DFSDM_JTRG[8]	TIM7_TRGO				
DFSDM_JTRG[9]	Reserved	HRTIM1_ADCTRG1	Reserved		
DFSDM_JTRG[10]	Reserved	HRTIM1_ADCTRG3	Reserved		
DFSDM_JTRG[11]	Reserved		TIM23_TRGO	Reserved	
DFSDM_JTRG[12]	Reserved		TIM24_TRGO	Reserved	
DFSDM_JTRG[13:23]	Reserved				
DFSDM_JTRG[24]	EXTI11				
DFSDM_JTRG[25]	EXTI15				
DFSDM_JTRG[26]	LPTIMER1				
DFSDM_JTRG[27]	Reserved	LPTIMER2			
DFSDM_JTRG[28]	Reserved	LPTIMER3			
DFSDM_JTRG[29]	Reserved			COMP1_OUT	
DFSDM_JTRG[30]	Reserved			COMP2_OUT	
DFSDM_JTRG[31]	Reserved				

This table presents the DFSDM break connections differences between STM32F7 Series devices, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices.

Table 38. DFSDM break connection differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices

Break name	STM32F7 Series	STM32H74x/75x	STM32H72x/73x	STM32H7A3/7Bx	
Instance	DFSDM1	DFSDM1	DFSDM1	DFSDM1	DFSDM2
DFSDM_BREAK[0]	TIM1 break	TIM15 break	TIM1/TIM15 break		LPTIM3 ETR
DFSDM_BREAK[1]	TIM1 break2	TIM16 break2	TIM1_break2 /TIM16 break		-
DFSDM_BREAK[2]	TIM8 break	TIM1/TIM17/TIM8 break	TIM17/TIM8 break		-
DFSDM_BREAK[3]	TIM8 break2	TIM1/TIM8 break2	TIM8 break2		-

Revision history

Table 39. **Document revision history**

Date	Version	Changes
27-Feb-2019	1	Initial release.
15-Mar-2019	2	Updated: • Section 2.3 STM32H7A3/7Bx devices • Section 3 System architecture differences between STM32F7 and STM32H7 Series • Section 6.1 • Section 7 Power (PWR) • Section 6.2.2 • Table 27. ADC differences between STM32F7 Series,STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices
31-Jan-2020	3	Changed document classification to public.
25-May-2020	4	Updated: • Added support for the STM32H7B0 Value line devices • Section 2.3 STM32H7A3/7Bx devices • Section 3 • Figure 4. STM32H7A3/7Bx devices system architecture • Figure 6. System supply configuration on STM32H74x/75x and STM32H7A3/7Bx devices with SMPS • Section 6.1 • Section 6.2.2 • Table 13. Flash memory differences between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices • Table 17. Different source clock in STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices • Table 19. General operating conditions for STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices Added: • Section 1 General information • Figure 7. System supply configuration on STM32H74x/75x and STM32H7A3/7Bx devices without SMPS
12-Oct-2020	5	Updated Table 7. STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices bootloader communication peripherals
17-Aug-2022	6	Changed Flash into flash in the whole document. Updated: • Document title and scope to add STM32H723/733, STM32H725/735, STM32H730 Value, STM32H742, STM32H745/755, and STM32H750 lines • Cover page to align with new scope and to add Table 1, which indicates all the specific product lines covered in this document and the generic names that are used from this version on to refer to the identified three groups of STM32H7 lines. • All chapters in the document are impacted by the new document's scope and updated in consequence.

Date	Version	Changes
		Modified: • Figure 4. STM32H7A3/7Bx devices system architecture • STM32H7A3/B3 I/O pin corresponding to FDCAN1 in Table 7. STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices bootloader communication peripherals • Table 11. Memory organization and compatibility between STM32F7 Series, STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices • Table 12. Examples of peripheral address mapping differences between STM32F7 Series,STM32H74x/75x, STM32H72x/73x and STM32H7A3/7Bx devices Added: • Section 2 STM32H7 devices overview • Section 2.1 STM32H74x/75x devices • Section 2.2 STM32H72x/73x devices overview • Table 34. Ethernet differences between STM32F7 and STM32H7 devices Updated Section 12 title.

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