

# RL78/L12

User's Manual: Hardware

## 16-Bit Single-Chip Microcontrollers

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## NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

# How to Use This Manual

## Readers

This manual is intended for user engineers who wish to understand the functions of the RL78/L12 and design and develop application systems and programs for these devices. The target products are as follows.

- 32-pin: R5F10RBx (x = 8, A, C)
- 44-pin: R5F10RFx (x = 8, A, C)
- 48-pin: R5F10RGx (x = 8, A, C)
- 52-pin: R5F10RJx (x = 8, A, C)
- 64-pin: R5F10RLx (x = A, C)

## Purpose

This manual is intended to give users an understanding of the functions described in the **Organization** below.

## Organization

The RL78/L12 manual is separated into two parts: this manual and the software edition (common to the RL78 family).

|                                                     |                                                   |
|-----------------------------------------------------|---------------------------------------------------|
| <b>RL78/L12<br/>User's Manual<br/>(This Manual)</b> | <b>RL78 Family<br/>User's Manual<br/>Software</b> |
|-----------------------------------------------------|---------------------------------------------------|

- Pin functions
- Internal block functions
- Interrupts
- Other on-chip peripheral functions
- Electrical specifications
- CPU functions
- Instruction set
- Explanation of each instruction

## How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
  - Read this manual in the order of the **CONTENTS**. The mark "<R>" shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.
- How to interpret the register format:
  - For a bit number enclosed in angle brackets, the bit name is defined as a reserved word in the assembler, and is defined as an sfr variable using the #pragma sfr directive in the compiler.
- To know details of the RL78/L12 Microcontroller instructions:
  - Refer to the separate document **RL78 Family User's Manual: Software (R01US0015E)**.



**Conventions**

Data significance: Higher digits on the left and lower digits on the right

Active low representations:  $\overline{\text{xxx}}$  (overscore over pin and signal name)

**Note:** Footnote for item marked with **Note** in the text

**Caution:** Information requiring particular attention

**Remark:** Supplementary information

Numerical representations: Binary      ...xxxx or xxxxB  
Decimal      ...xxxx  
Hexadecimal      ...xxxxH

**Related Documents**

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

**Documents Related to Devices**

| Document Name                       | Document No. |
|-------------------------------------|--------------|
| RL78/L12 User's Manual Hardware     | This manual  |
| RL78 Family User's Manual: Software | R01US0015E   |

**Documents Related to Flash Memory Programming**

| Document Name                                | Document No. |
|----------------------------------------------|--------------|
| PG-FP5 Flash Memory Programmer User's Manual | R20UT0008E   |

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#### Other Documents

| Document Name                                                                      | Document No. |
|------------------------------------------------------------------------------------|--------------|
| RENESAS MICROCOMPUTER GENERAL CATALOG                                              | R01CS0001E   |
| Semiconductor Package Mount Manual                                                 | <b>Note</b>  |
| Quality Grades on NEC Semiconductor Devices                                        | C11531E      |
| NEC Semiconductor Device Reliability/Quality Control System                        | C10983E      |
| Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD) | C11892E      |

**Note** See the "Semiconductor Package Mount Manual" website (<http://www.renesas.com/products/package/manual/index.jsp>).

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## CHAPTER 1 OUTLINE

### 1.1 Features

- Minimum instruction execution time can be changed from high speed (0.04167  $\mu$ s: @ 24 MHz operation with high-speed on-chip oscillator clock) to ultra low-speed (30.5  $\mu$ s: @ 32.768 kHz operation with subsystem clock)
- General-purpose register: 8 bits  $\times$  32 registers (8 bits  $\times$  8 registers  $\times$  4 banks)
- ROM: 8 to 32 KB, RAM: 1 to 1.5 KB, Data flash memory: 2 KB
- On-chip high-speed on-chip oscillator clock
  - Select from 24 MHz (TYP.), 16 MHz (TYP.), 12 MHz (TYP.), 8 MHz (TYP.), 4 MHz (TYP.), and 1 MHz (TYP.)
- On-chip single-power-supply flash memory (with prohibition of block erase/writing function)
- Self-programming
- On-chip debug function
- On-chip power-on-reset (POR) circuit and voltage detector (LVD)
- On-chip watchdog timer (operable with the low-speed on-chip oscillator clock)
- On-chip multiplier and divider/multiply-accumulator
  - 16 bits  $\times$  16 bits = 32 bits (Unsigned or signed)
  - 32 bits  $\div$  32 bits = 32 bits (Unsigned)
  - 16 bits  $\times$  16 bits + 32 bits = 32 bits (Unsigned or signed)
- On-chip key interrupt function
- On-chip clock output/buzzer output controller
- On-chip BCD adjustment
- I/O ports: 20 to 47(N-ch open drain: 2)
- Timer
  - 16-bit timer: 8 channels  
(remote control output available only for 44-, 48-, 52-, and 64-pin products)
  - Watchdog timer: 1 channel
  - Real-time clock: 1 channel (Correction clock output)
  - 12-bit interval timer: 1 channel
- Serial interface
  - CSI: 2 channels
  - UART (LIN-bus supported): 1 channel
  - I<sup>2</sup>C: 1 channel
- Different potential interface: Can connect to a 1.8/2.5/3 V device
- 8/10-bit resolution A/D converter ( $V_{DD} = EV_{DD} = 1.6$  to 5.5 V): 4 to 10 channels
- LCD controller/driver (Internal voltage boosting method (44-, 48-, 52-, 64-pin products only), capacitor split method, and external resistance division method are switchable)
  - Segment signal output: 39 (35)<sup>Note</sup> to 13
  - Common signal output: 4 (8)<sup>Note</sup>
- Standby function: HALT, STOP, SNOOZE mode
- DMA controller: 2 channels
- Power supply voltage:  $V_{DD} = 1.6$  to 5.5 V
- Operating ambient temperature:  $T_A = -40$  to  $+85^{\circ}\text{C}$

**Note** The values in parentheses are the number of signal outputs when 8com is used.

**Remark** The functions mounted depend on the product. See **1.6 Outline of Functions**.

## O ROM, RAM capacities

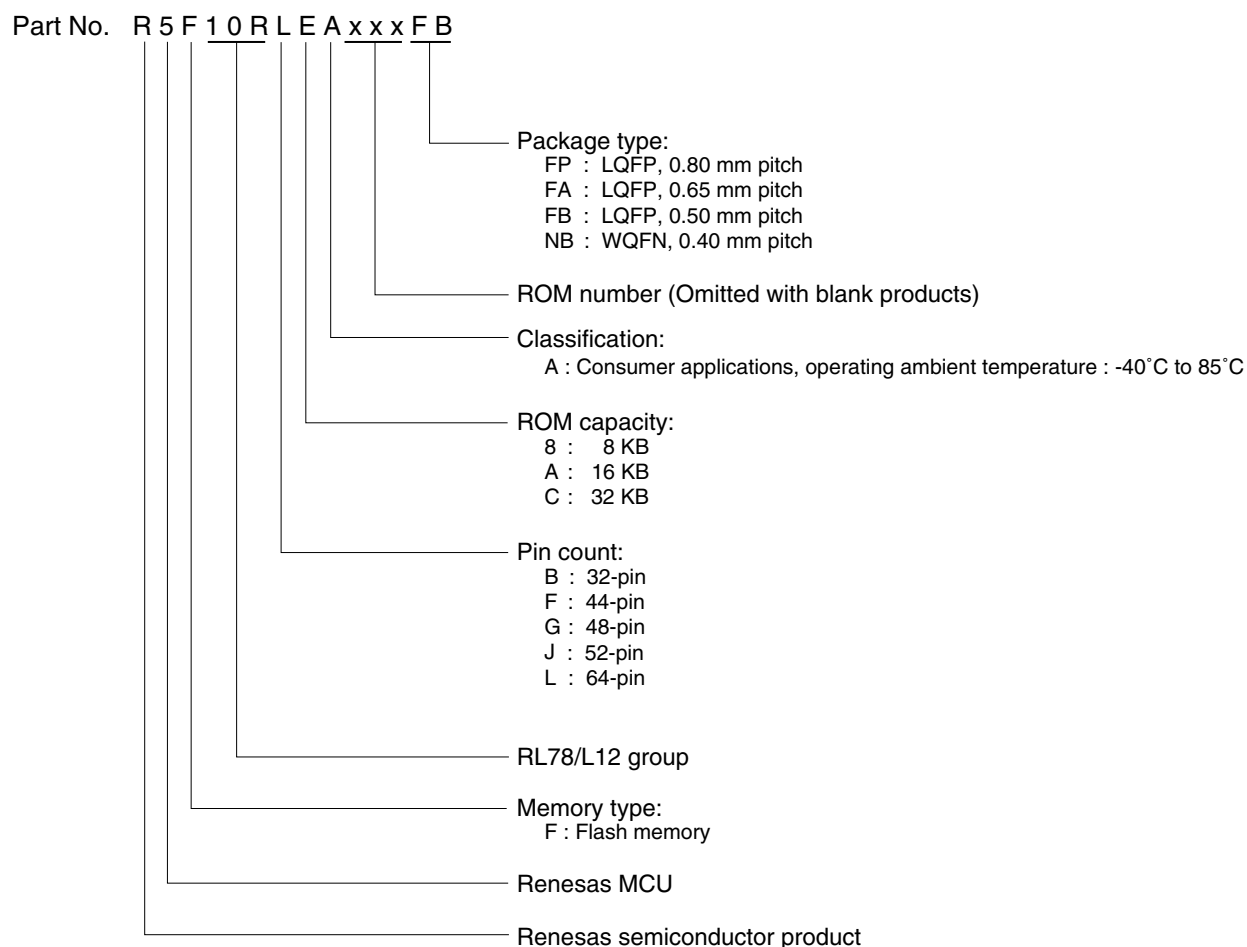
| Flash<br>ROM | Data<br>flash | RAM                       | RL78/L12 |          |          |          |          |
|--------------|---------------|---------------------------|----------|----------|----------|----------|----------|
|              |               |                           | 32 pins  | 44 pins  | 48 pins  | 52 pins  | 64 pins  |
| 32 KB        | 2 KB          | 1.5<br>KB <sup>Note</sup> | R5F10RBC | R5F10RFC | R5F10RGC | R5F10RJC | R5F10RLC |
| 16 KB        | 2 KB          | 1<br>KB <sup>Note</sup>   | R5F10RBA | R5F10RFA | R5F10RGA | R5F10RJA | R5F10RLA |
| 8KB          | 2 KB          | 1<br>KB <sup>Note</sup>   | R5F10RB8 | R5F10RF8 | R5F10RG8 | R5F10RJ8 | –        |

**Note** In the case of the 1 KB, and 1.5 KB, this is 630 bytes when the self-programming function and data flash function is used. (For details, see **CHAPTER 3 CPU ARCHITECTURE**)

**Remark** The functions mounted depend on the product. See **1.6 Outline of Functions**.

## &lt;R&gt; 1.2 List of Part Numbers

&lt;R&gt; Figure 1-1 Part Number, Memory Size, and Package of RL78/L12



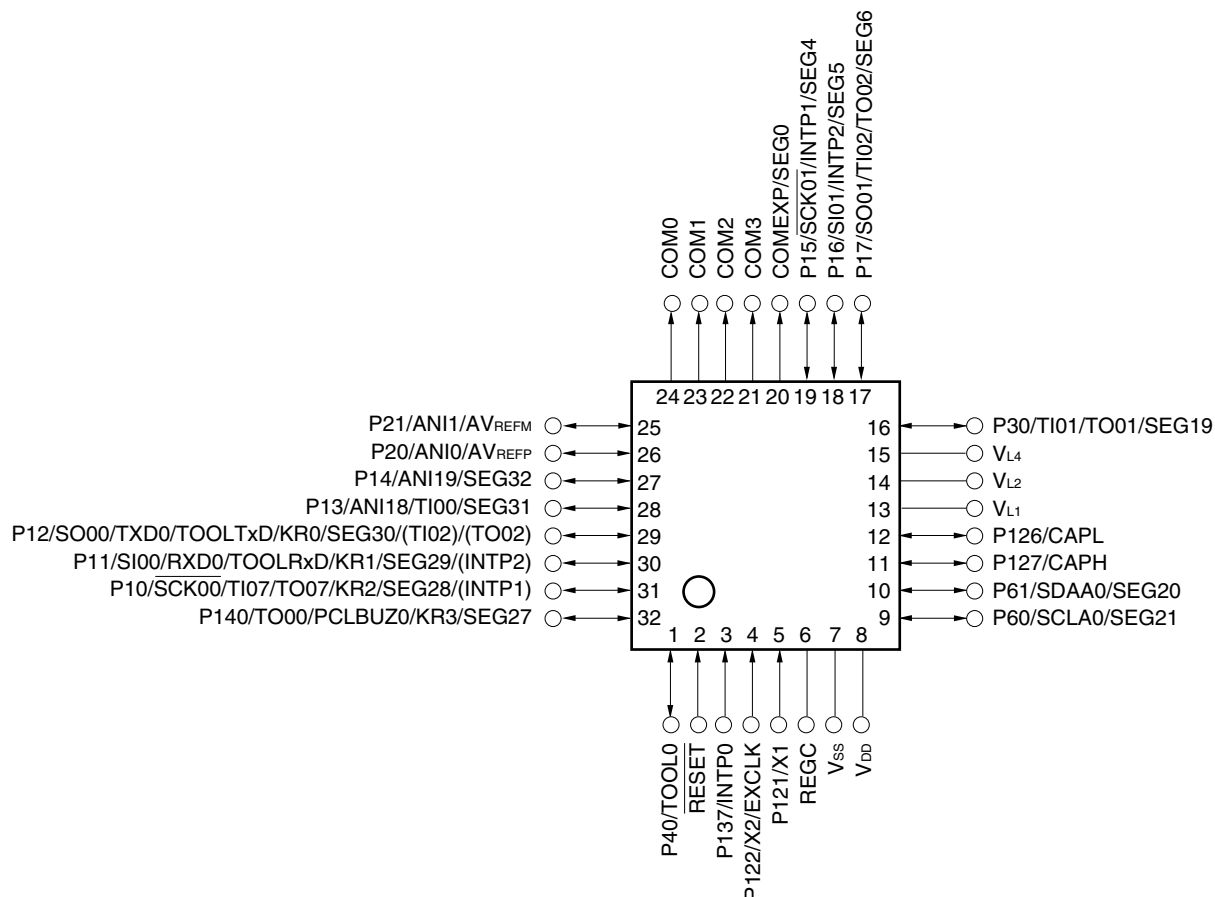
| Pin count | Package                                       | Part Number                           |
|-----------|-----------------------------------------------|---------------------------------------|
| 32 pins   | 32-pin plastic LQFP (7 × 7)                   | R5F10RB8AFP, R5F10RBAAFP, R5F10RBCAFP |
| 44 pins   | 44-pin plastic LQFP (10 × 10)                 | R5F10RF8AFP, R5F10RFAAFP, R5F10RFCAFP |
| 48 pins   | 48-pin plastic LQFP<br>(fine pitch) (7 × 7)   | R5F10RG8AFB, R5F10RGAAFB, R5F10RGCAFB |
| 52 pins   | 52-pin plastic LQFP (10 × 10)                 | R5F10RJ8AFA, R5F10RJAAFA, R5F10RJCAFA |
| 64 pins   | 64-pin plastic WQFN (8 × 8)                   | R5F10RLAANB, R5F10RLCANB              |
|           | 64-pin plastic LQFP (fine pitch)<br>(10 × 10) | R5F10RLAAFB, R5F10RLCAFB              |
|           | 64-pin plastic LQFP (12 × 12)                 | R5F10RLAAFA, R5F10RLCAFA              |

**Caution** The RL78/L12 has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

### 1.3 Pin Configuration (Top View)

#### 1.3.1 32-pin products

- 32-pin plastic LQFP (7 × 7)



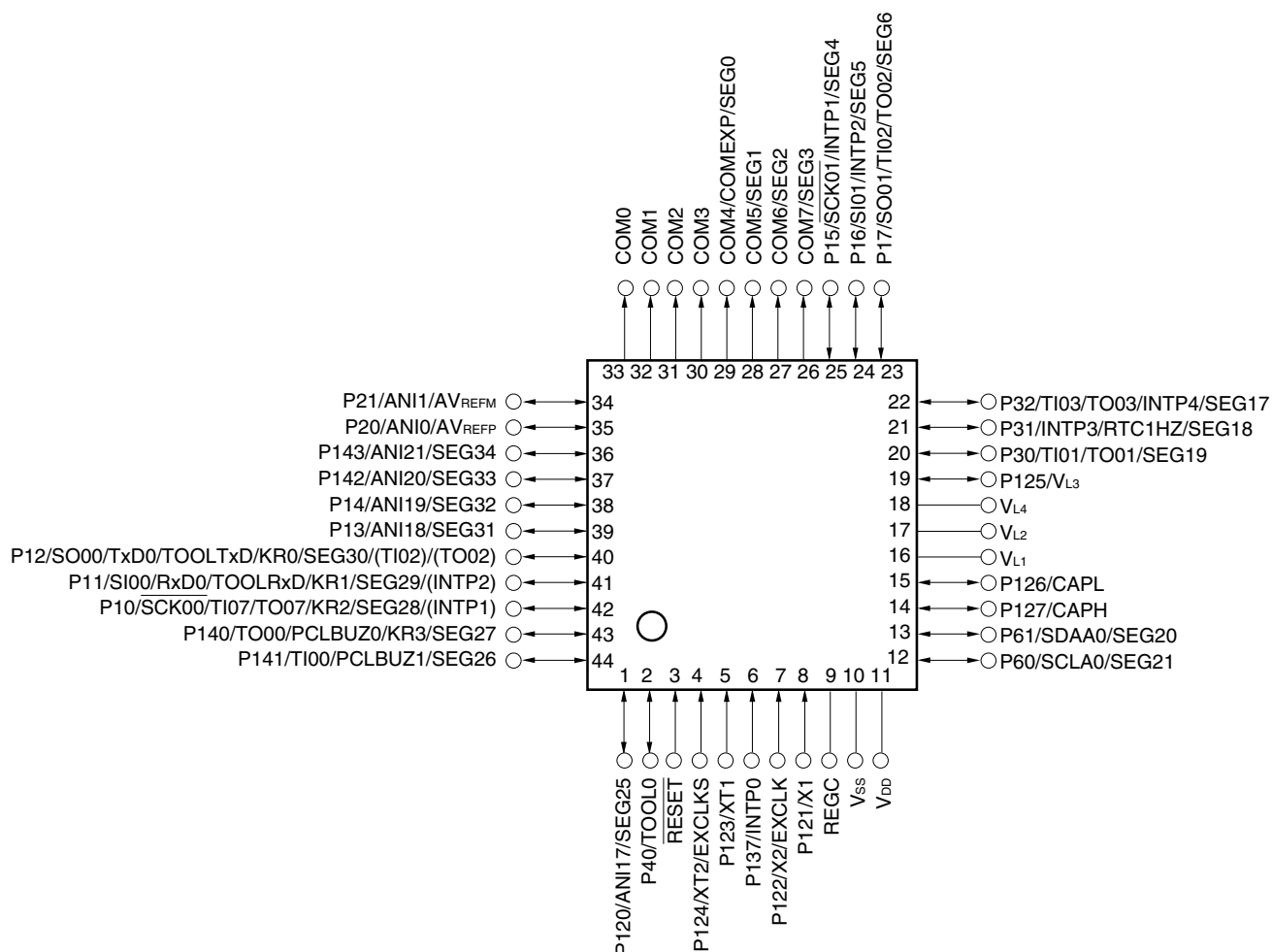
**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1  $\mu$ F).

**Remarks** 1. For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

### 1.3.2 44-pin products

- 44-pin plastic LQFP (10 × 10)



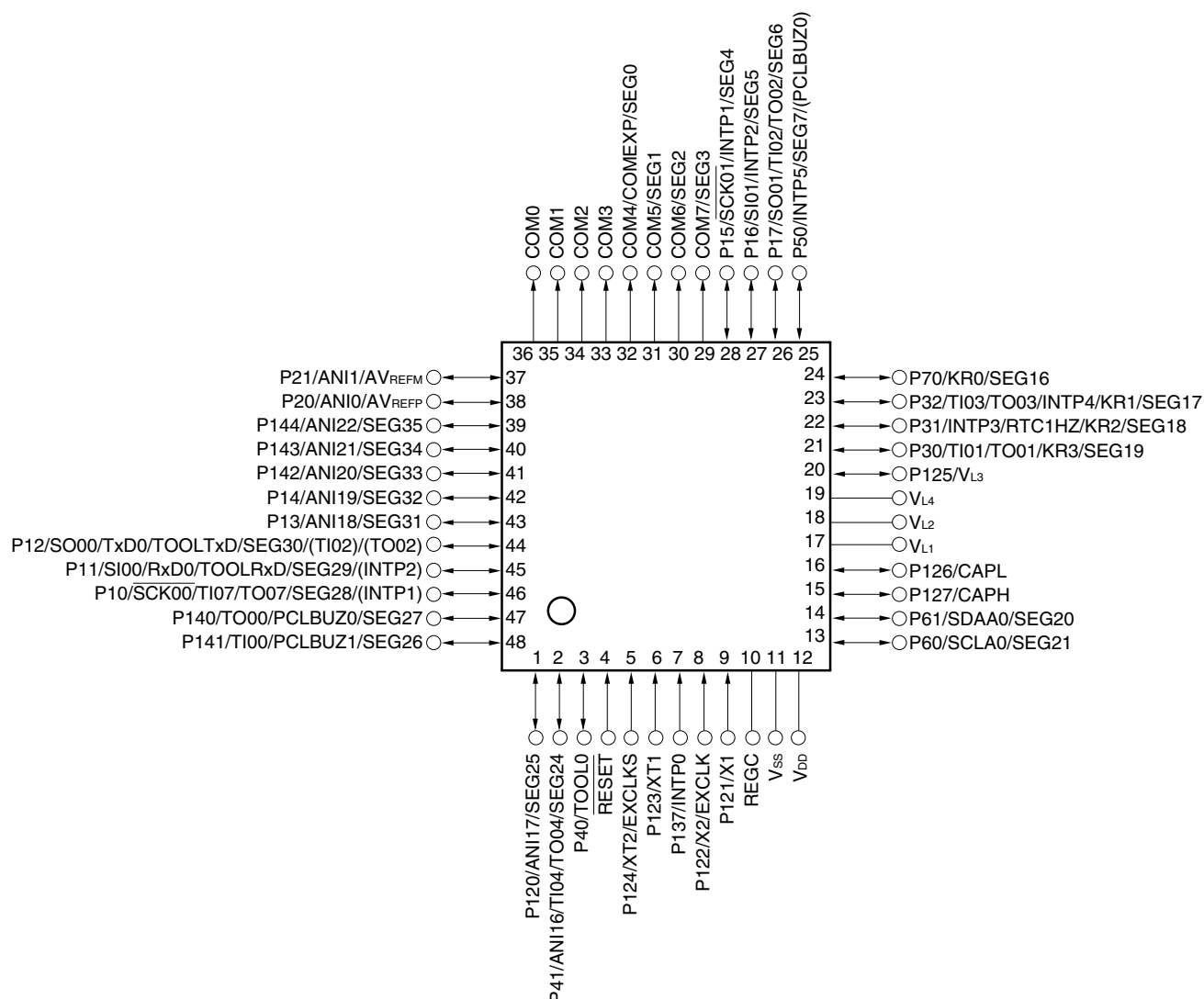
**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1  $\mu$ F).

**Remarks** 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8. Format of Peripheral I/O Redirection Register (PIOR)**.

### 1.3.3 48-pin products

- 48-pin plastic LQFP (fine pitch) (7 × 7)



**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

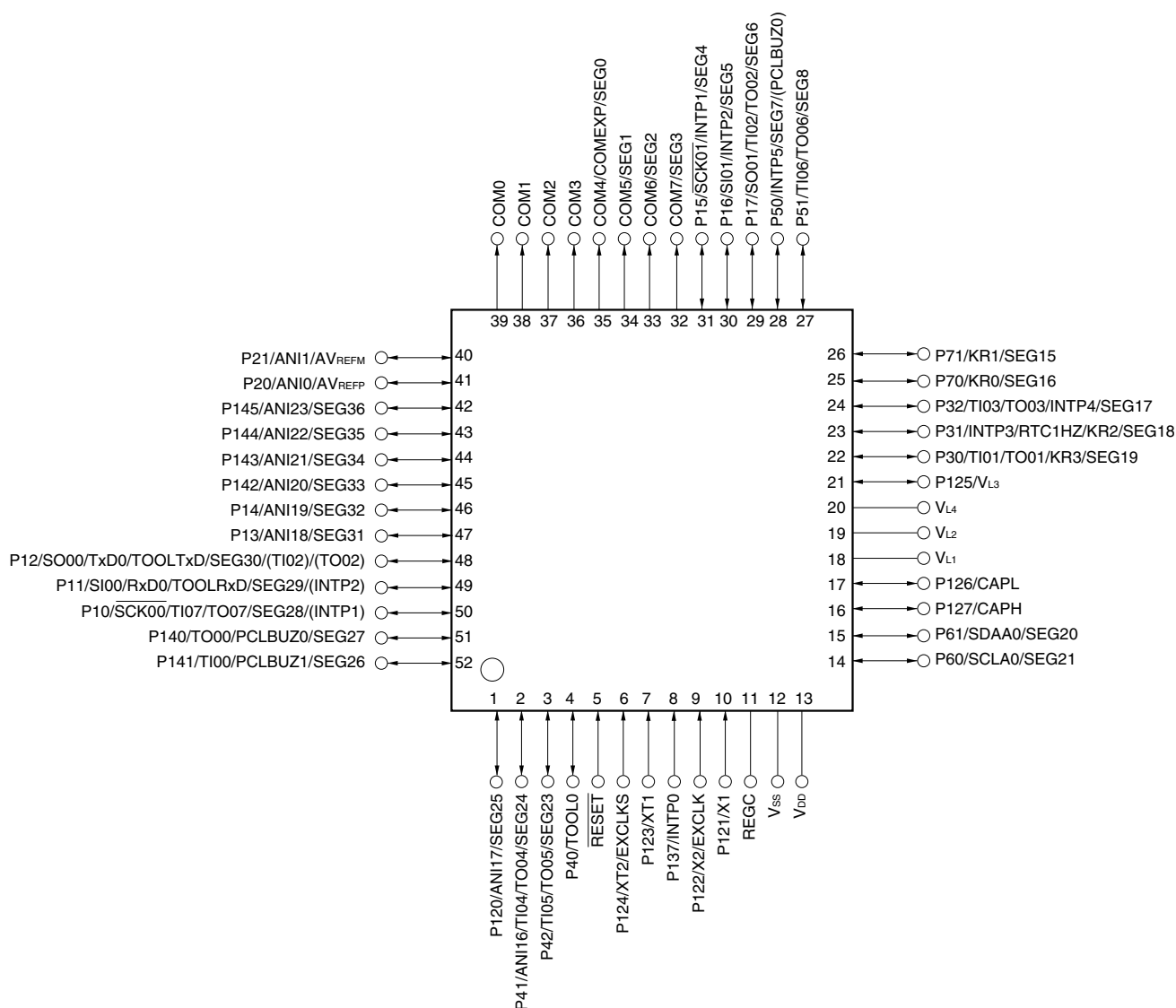
**Remarks** 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8. Format of Peripheral I/O Redirection Register (PIOR)**.



## 1.3.4 52-pin products

- 52-pin plastic LQFP (10 × 10)



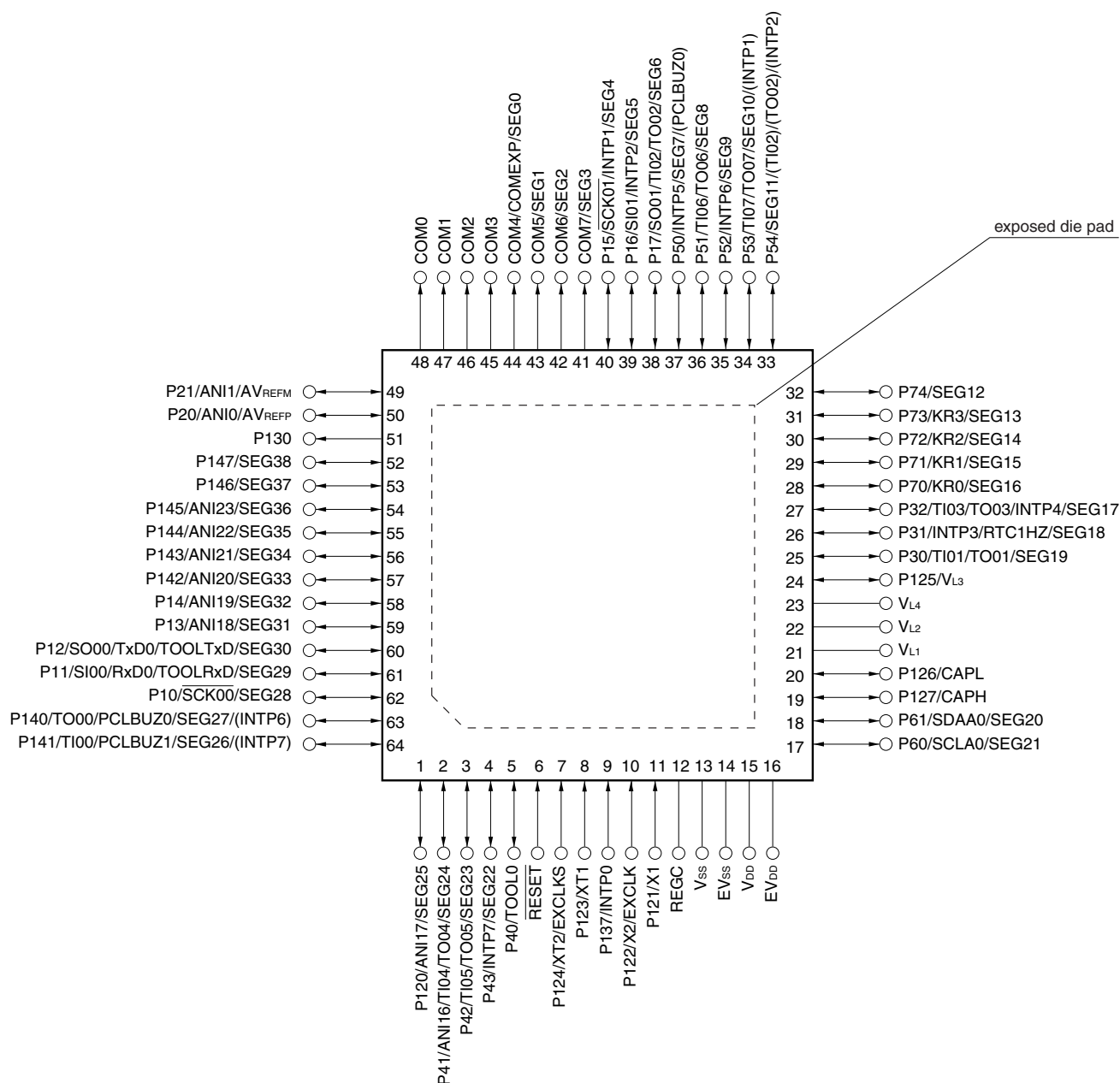
**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

- 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8. Format of Peripheral I/O Redirection Register (PIOR)**.

## 1.3.5 64-pin products

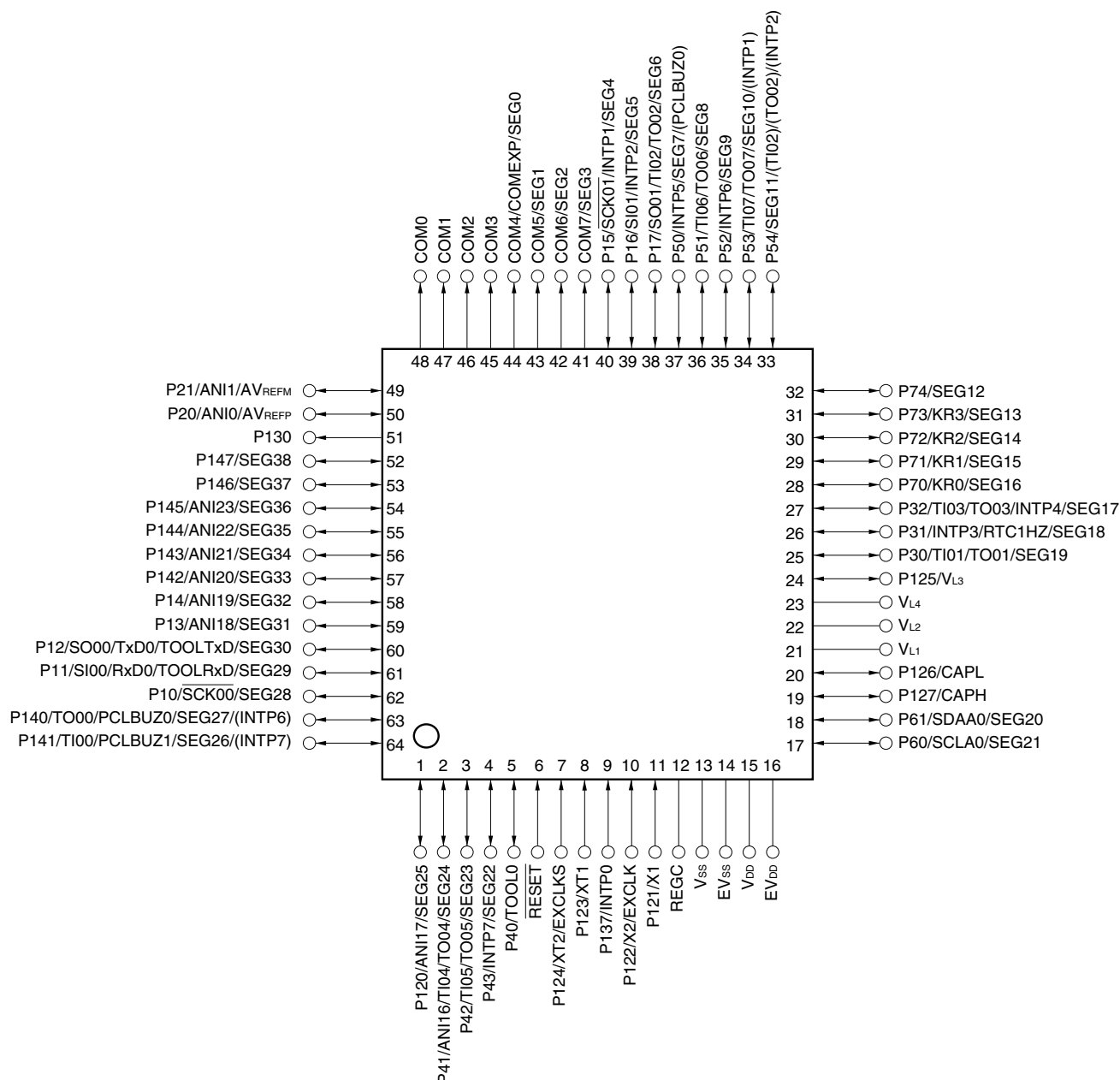
- 64-pin plastic WQFN (8 × 8)



- Cautions**
1. Make EV<sub>SS</sub> pin the same potential as V<sub>SS</sub> pin.
  2. Make V<sub>DD</sub> pin the same potential as EV<sub>DD</sub> pin.
  3. Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
  2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V<sub>DD</sub> and EV<sub>DD</sub> pins and connect the V<sub>SS</sub> and EV<sub>SS</sub> pins to separate ground lines.
  3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8. Format of Peripheral I/O Redirection Register (PIOR)**.

- 64-pin plastic LQFP (fine pitch) (10 × 10)
- 64-pin plastic LQFP (12 × 12)



- Cautions**
1. Make EV<sub>SS</sub> pin the same potential as V<sub>SS</sub> pin.
  2. Make V<sub>DD</sub> pin the same potential as EV<sub>DD</sub> pin.
  3. Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

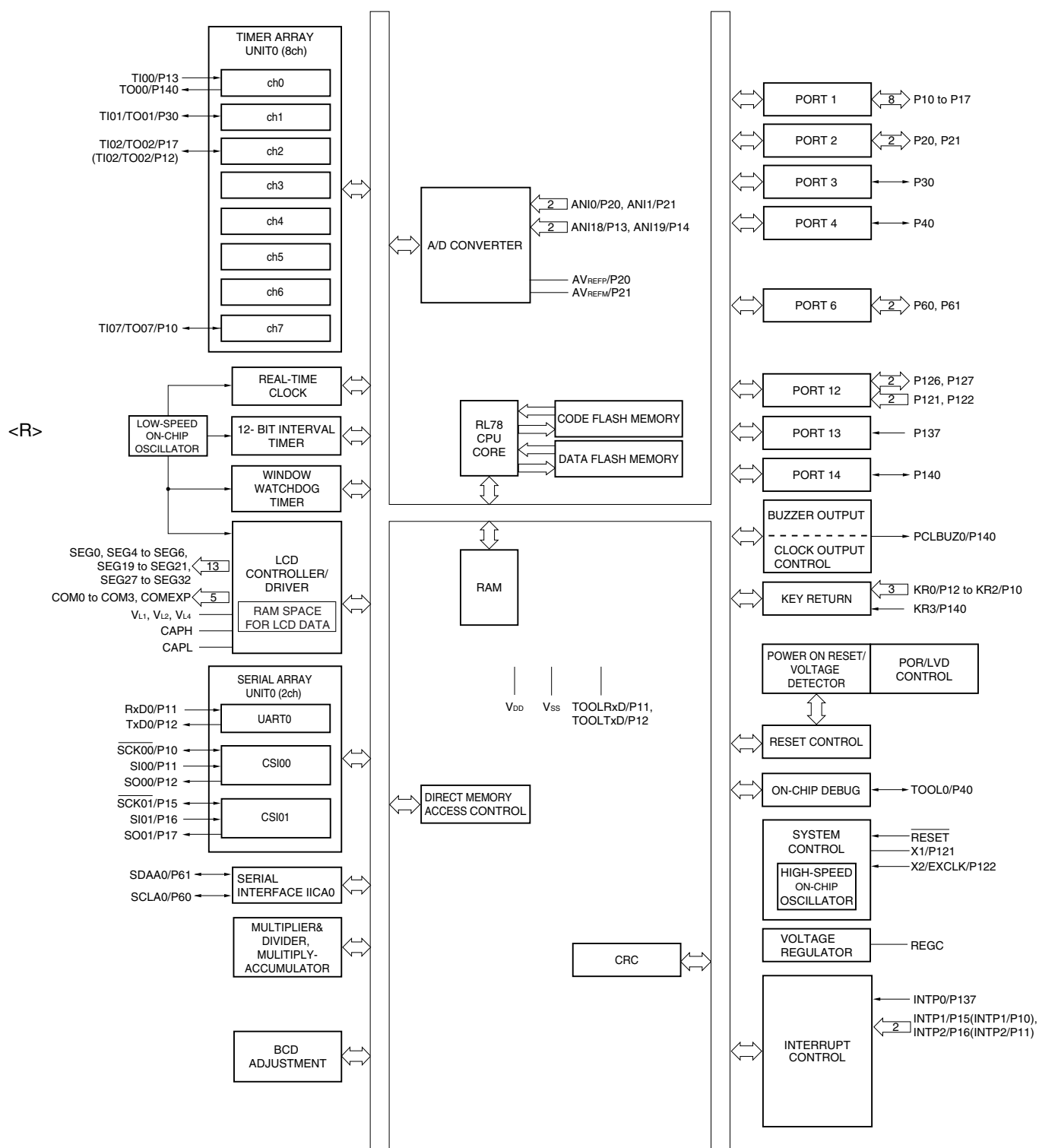
- Remarks**
1. For pin identification, see 1.4 Pin Identification.
  2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V<sub>DD</sub> and EV<sub>DD</sub> pins and connect the V<sub>SS</sub> and EV<sub>SS</sub> pins to separate ground lines.
  3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to Figure 4-8. Format of Peripheral I/O Redirection Register (PIOR).

## 1.4 Pin Identification

|                     |                                             |                   |                                                   |
|---------------------|---------------------------------------------|-------------------|---------------------------------------------------|
| ANIO, ANI1,         |                                             | P130, P137:       | Port 13                                           |
| ANI16 to ANI23:     | Analog Input                                | P140 to P147:     | Port 14                                           |
| AVREFM:             | Analog Reference<br>Voltage Minus           | PCLBUZ0, PCLBUZ1: | Programmable Clock<br>Output/Buzzer Output        |
| AVREFP:             | Analog Reference<br>Voltage Plus            | REGC:             | Regulator Capacitance                             |
| CAPH, CAPL:         | Capacitor for LCD                           | RESET:            | Reset                                             |
| COM0 to COM7,       |                                             | RTC1HZ:           | Real-time Clock Correction Clock<br>(1 Hz) Output |
| COMEXP:             | LCD Common Output                           | RxD0:             | Receive Data                                      |
| EVDD:               | Power Supply for Port                       | SCK00, SCK01:     | Serial Clock Input/Output                         |
| EVSS:               | Ground for Port                             | SCLA0:            | Serial Clock Input/Output                         |
| EXCLK:              | External Clock Input<br>(Main System Clock) | SDAA0:            | Serial Data Input/Output                          |
| EXCLKS:             | External Clock Input<br>(Subsystem Clock)   | SEG0 to SEG38:    | LCD Segment Output                                |
| <R> INTP0 to INTP7: | Interrupt Request From<br>Peripheral        | SI00, SI01:       | Serial Data Input                                 |
| KR0 to KR3:         | Key Return                                  | SO00, SO01:       | Serial Data Output                                |
| P10 to P17:         | Port 1                                      | TI00 to TI07:     | Timer Input                                       |
| P20, P21:           | Port 2                                      | TO00 to TO07:     | Timer Output                                      |
| P30 to P32:         | Port 3                                      | TOOL0:            | Data Input/Output for Tool                        |
| P40 to P43:         | Port 4                                      | TOOLRxD, TOOLTxD: | Data Input/Output for External Device             |
| P50 to P54:         | Port 5                                      | TxD0:             | Transmit Data                                     |
| P60, P61:           | Port 6                                      | VDD:              | Power Supply                                      |
| P70 to P74:         | Port 7                                      | VL1 to VL4:       | LCD Power Supply                                  |
| P120 to P127:       | Port 12                                     | VSS:              | Ground                                            |
|                     |                                             | X1, X2:           | Crystal Oscillator (Main System Clock)            |
|                     |                                             | XT1, XT2:         | Crystal Oscillator (Subsystem Clock)              |

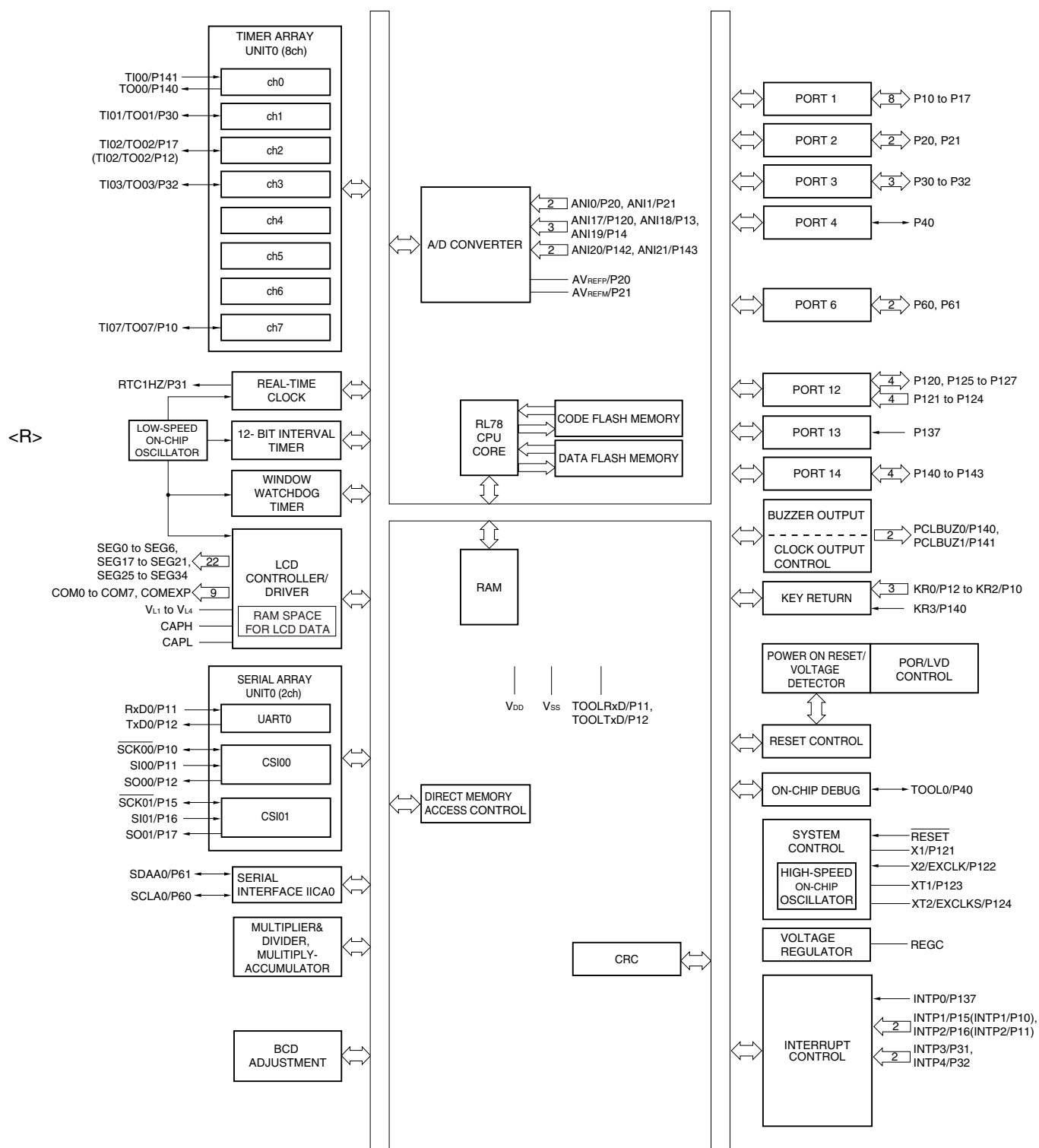
## 1.5 Block Diagram

### 1.5.1 32-pin products



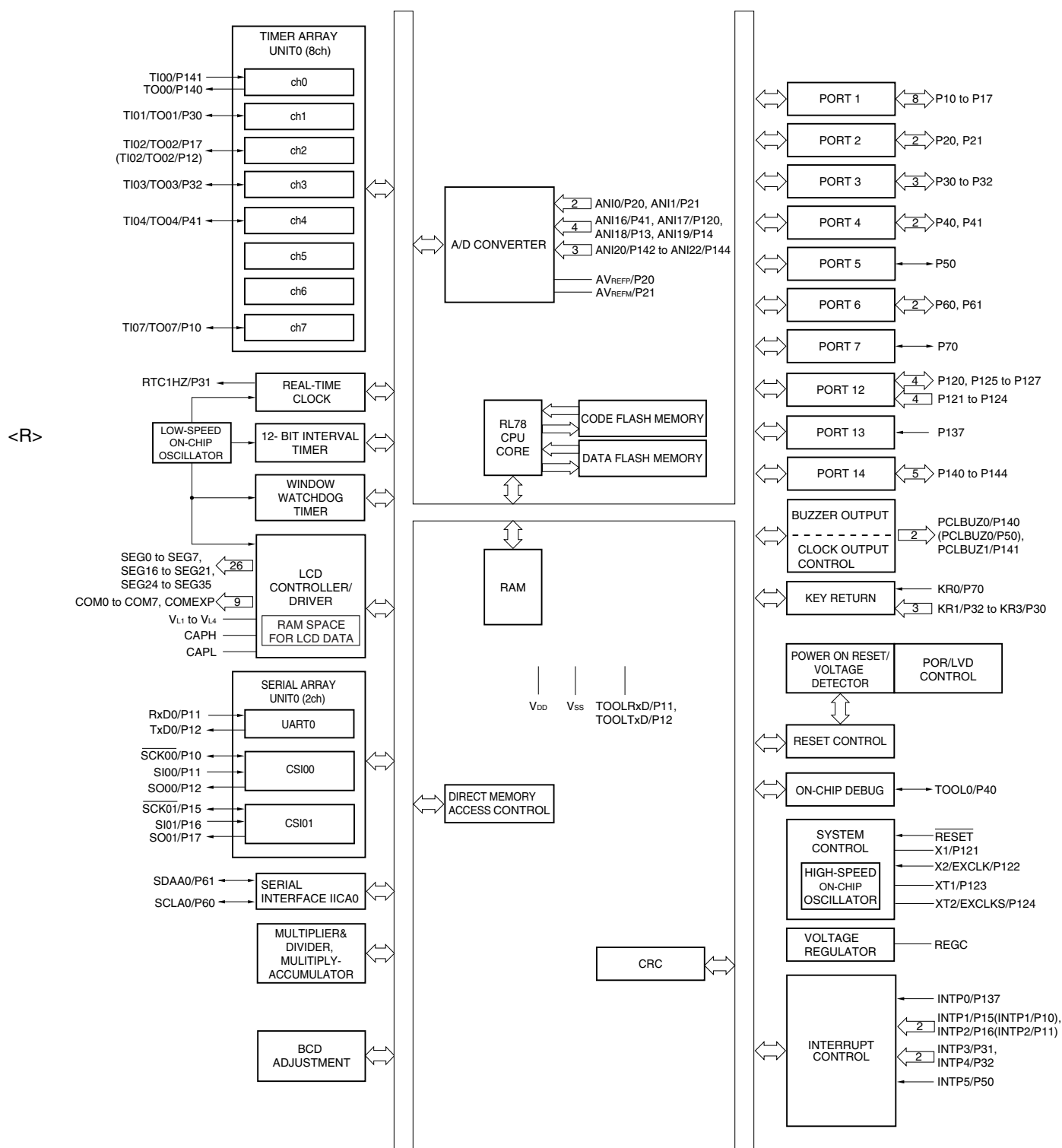
**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

## 1.5.2 44-pin products



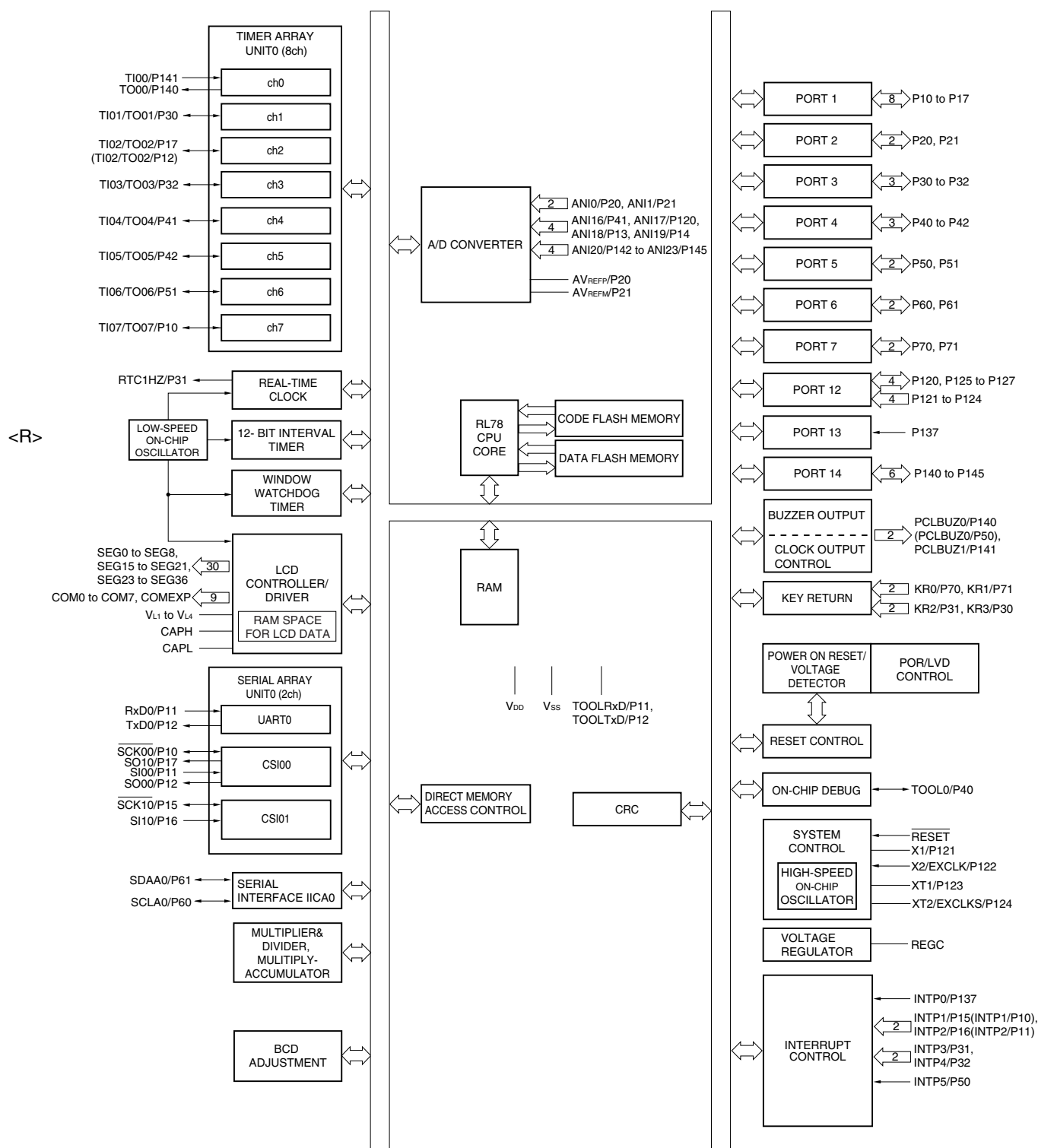
**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

## 1.5.3 48-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

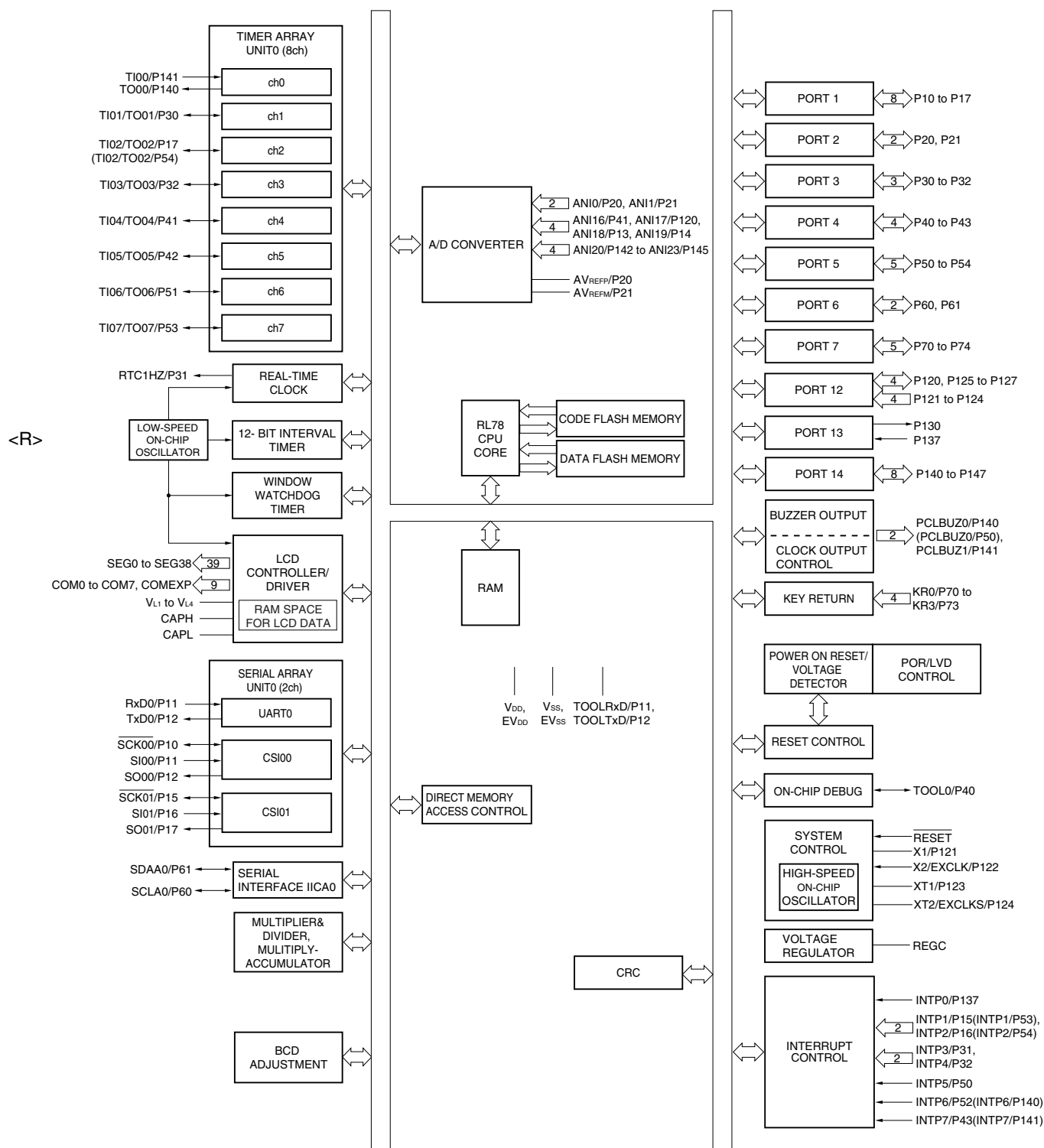
## 1.5.4 52-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)



## 1.5.5 64-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

## 1.6 Outline of Functions

**Caution** This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

| Item                               |                                                  | 32-pin                                                                                                                                                                                                                                                                                                                        | 44-pin                                                                                                                   | 48-pin                                               | 52-pin                                         | 64-pin                   |
|------------------------------------|--------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------|------------------------------------------------|--------------------------|
|                                    |                                                  | R5F10RBx                                                                                                                                                                                                                                                                                                                      | R5F10RFx                                                                                                                 | R5F10RGx                                             | R5F10RJx                                       | R5F10RLx                 |
| Code flash memory (KB)             |                                                  | 8 to 32                                                                                                                                                                                                                                                                                                                       | 8 to 32                                                                                                                  | 8 to 32                                              | 8 to 32                                        | 16, 32                   |
| Data flash memory (KB)             |                                                  | 2                                                                                                                                                                                                                                                                                                                             | 2                                                                                                                        | 2                                                    | 2                                              | 2                        |
| RAM (KB)                           |                                                  | 1, 1.5 <sup>Note 1</sup>                                                                                                                                                                                                                                                                                                      | 1, 1.5 <sup>Note 1</sup>                                                                                                 | 1, 1.5 <sup>Note 1</sup>                             | 1, 1.5 <sup>Note 1</sup>                       | 1, 1.5 <sup>Note 1</sup> |
| Memory space                       |                                                  | 1 MB                                                                                                                                                                                                                                                                                                                          |                                                                                                                          |                                                      |                                                |                          |
| Main system clock                  | High-speed system clock                          | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>1 to 20 MHz: V <sub>DD</sub> = 2.7 to 5.5 V, 1 to 8 MHz: V <sub>DD</sub> = 1.8 to 2.7 V, 1 to 4 MHz: V <sub>DD</sub> = 1.6 to 1.8 V                                                                                                             |                                                                                                                          |                                                      |                                                |                          |
|                                    | High-speed on-chip oscillator clock              | HS (high-speed main) operation: 1 to 24 MHz (V <sub>DD</sub> = 2.7 to 5.5 V),<br>HS (high-speed main) operation: 1 to 16 MHz (V <sub>DD</sub> = 2.4 to 5.5 V),<br>LS (low-speed main) operation: 1 to 8 MHz (V <sub>DD</sub> = 1.8 to 5.5 V),<br>LV (low-voltage main) operation: 1 to 4 MHz (V <sub>DD</sub> = 1.6 to 5.5 V) |                                                                                                                          |                                                      |                                                |                          |
| Subsystem clock                    |                                                  | –                                                                                                                                                                                                                                                                                                                             | XT1 (crystal) oscillation , external subsystem clock input (EXCLKS)<br>32.768 kHz (TYP.): V <sub>DD</sub> = 1.6 to 5.5 V |                                                      |                                                |                          |
| Low-speed on-chip oscillator clock |                                                  | Internal oscillation<br>15 kHz (TYP.): V <sub>DD</sub> = 1.6 to 5.5 V                                                                                                                                                                                                                                                         |                                                                                                                          |                                                      |                                                |                          |
| General-purpose register           |                                                  | 8 bits × 32 registers (8 bits × 8 registers × 4 banks)                                                                                                                                                                                                                                                                        |                                                                                                                          |                                                      |                                                |                          |
| Minimum instruction execution time |                                                  | 0.04167 μs (High-speed on-chip oscillator clock: f <sub>IH</sub> = 24 MHz operation)                                                                                                                                                                                                                                          |                                                                                                                          |                                                      |                                                |                          |
|                                    |                                                  | 0.05 μs (High-speed system clock: f <sub>MX</sub> = 20 MHz operation)                                                                                                                                                                                                                                                         |                                                                                                                          |                                                      |                                                |                          |
|                                    |                                                  | 30.5 μs (Subsystem clock: f <sub>SUB</sub> = 32.768 kHz operation)                                                                                                                                                                                                                                                            |                                                                                                                          |                                                      |                                                |                          |
| Instruction set                    |                                                  | <ul style="list-style-type: none"><li>• Data transfer (8/16 bits)</li><li>• Adder and subtractor/logical operation (8/16 bits)</li><li>• Multiplication (8 bits × 8 bits)</li><li>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.</li></ul>                                      |                                                                                                                          |                                                      |                                                |                          |
| I/O port                           | Total                                            | 20                                                                                                                                                                                                                                                                                                                            | 29                                                                                                                       | 33                                                   | 37                                             | 47                       |
|                                    | CMOS I/O                                         | 15                                                                                                                                                                                                                                                                                                                            | 22                                                                                                                       | 26                                                   | 30                                             | 39                       |
|                                    | CMOS input                                       | 3                                                                                                                                                                                                                                                                                                                             | 5                                                                                                                        | 5                                                    | 5                                              | 5                        |
|                                    | CMOS output                                      | –                                                                                                                                                                                                                                                                                                                             | –                                                                                                                        | –                                                    | –                                              | 1                        |
|                                    | N-ch open-drain I/O (EV <sub>DD</sub> tolerance) | 2                                                                                                                                                                                                                                                                                                                             | 2                                                                                                                        | 2                                                    | 2                                              | 2                        |
| Timer                              | 16-bit timer                                     | 8 channels                                                                                                                                                                                                                                                                                                                    | 8 channels (with 1 channel remote control output function)                                                               |                                                      |                                                |                          |
|                                    | Watchdog timer                                   | 1 channel                                                                                                                                                                                                                                                                                                                     |                                                                                                                          |                                                      |                                                |                          |
|                                    | Real-time clock (RTC)                            | 1 channel                                                                                                                                                                                                                                                                                                                     |                                                                                                                          |                                                      |                                                |                          |
|                                    | 12-bit interval timer (IT)                       | 1 channel                                                                                                                                                                                                                                                                                                                     |                                                                                                                          |                                                      |                                                |                          |
|                                    | Timer output                                     | 4 channels<br>(PWM outputs:<br>3 <sup>Note 2</sup> )                                                                                                                                                                                                                                                                          | 5 channels<br>(PWM outputs:<br>4 <sup>Note 2</sup> )                                                                     | 6 channels<br>(PWM outputs:<br>5 <sup>Note 2</sup> ) | 8 channels (PWM outputs: 7 <sup>Note 2</sup> ) |                          |
|                                    | RTC output                                       | –                                                                                                                                                                                                                                                                                                                             | 1<br>• 1 Hz (subsystem clock: f <sub>SUB</sub> = 32.768 kHz or )                                                         |                                                      |                                                |                          |

**Notes** 1. In the case of the 1 KB, and 1.5 KB, this is 630 bytes when the self-programming function and data flash function is used. (For details, see **CHAPTER 3 CPU ARCHITECTURE**)

2. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves). (**6.8.3 Operation as multiple PWM output function**)

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| Item                                        |                       | 32-pin                                                                                                                                                                                                                                                                                                                                                                                             | 44-pin                    | 48-pin                    | 52-pin                    | 64-pin                    |
|---------------------------------------------|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
|                                             |                       | R5F10RBx                                                                                                                                                                                                                                                                                                                                                                                           | R5F10RFx                  | R5F10RGx                  | R5F10RJx                  | R5F10RLx                  |
| Clock output/buzzer output                  |                       | 1                                                                                                                                                                                                                                                                                                                                                                                                  | 2                         |                           |                           |                           |
|                                             |                       | <ul style="list-style-type: none"><li>2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz<br/>(Main system clock: <math>f_{\text{MAIN}} = 20</math> MHz operation)</li><li>256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz<br/>(Subsystem clock: <math>f_{\text{SUB}} = 32.768</math> kHz operation)</li></ul>                                       |                           |                           |                           |                           |
| 8/10-bit resolution A/D converter           |                       | 4 channels                                                                                                                                                                                                                                                                                                                                                                                         | 7 channels                | 9 channels                | 10 channels               | 10 channels               |
| Serial interface                            |                       | • CSI: 2 channel/UART (LIN-bus supported): 1 channel                                                                                                                                                                                                                                                                                                                                               |                           |                           |                           |                           |
|                                             | I <sup>2</sup> C bus  | 1 channel                                                                                                                                                                                                                                                                                                                                                                                          | 1 channel                 | 1 channel                 | 1 channel                 | 1 channel                 |
| LCD controller/driver                       |                       | Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.                                                                                                                                                                                                                                                                                  |                           |                           |                           |                           |
|                                             | Segment signal output | 13                                                                                                                                                                                                                                                                                                                                                                                                 | 22 (18) <sup>Note 1</sup> | 26 (22) <sup>Note 1</sup> | 30 (26) <sup>Note 1</sup> | 39 (35) <sup>Note 1</sup> |
|                                             | Common signal output  | 4                                                                                                                                                                                                                                                                                                                                                                                                  | 4 (8) <sup>Note 1</sup>   |                           |                           |                           |
| Multiplier and divider/multiply-accumulator |                       | <ul style="list-style-type: none"><li>16 bits × 16 bits = 32 bits (Unsigned or signed)</li><li>32 bits ÷ 32 bits = 32 bits (Unsigned)</li><li>16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)</li></ul>                                                                                                                                                                                 |                           |                           |                           |                           |
| DMA controller                              |                       | 2 channels                                                                                                                                                                                                                                                                                                                                                                                         |                           |                           |                           |                           |
| Vectored interrupt sources                  | Internal              | 23                                                                                                                                                                                                                                                                                                                                                                                                 | 23                        | 23                        | 23                        | 23                        |
|                                             | External              | 4                                                                                                                                                                                                                                                                                                                                                                                                  | 6                         | 7                         | 7                         | 9                         |
| Key interrupt                               |                       | 4                                                                                                                                                                                                                                                                                                                                                                                                  |                           |                           |                           |                           |
| Reset                                       |                       | <ul style="list-style-type: none"><li>Reset by <math>\overline{\text{RESET}}</math> pin</li><li>Internal reset by watchdog timer</li><li>Internal reset by power-on-reset</li><li>Internal reset by voltage detector</li><li>Internal reset by illegal instruction execution<sup>Note 2</sup></li><li>Internal reset by RAM parity error</li><li>Internal reset by illegal-memory access</li></ul> |                           |                           |                           |                           |
| Power-on-reset circuit                      |                       | <ul style="list-style-type: none"><li>Power-on-reset: 1.51 ±0.04 V</li><li>Power-down-reset: 1.50 ±0.04 V</li></ul>                                                                                                                                                                                                                                                                                |                           |                           |                           |                           |
| Voltage detector                            |                       | <ul style="list-style-type: none"><li>Rising edge : 1.67 V to 4.06 V (14 stages)</li><li>Falling edge : 1.63 V to 3.98 V (14 stages)</li></ul>                                                                                                                                                                                                                                                     |                           |                           |                           |                           |
| On-chip debug function                      |                       | Provided                                                                                                                                                                                                                                                                                                                                                                                           |                           |                           |                           |                           |
| Power supply voltage                        |                       | V <sub>DD</sub> = 1.6 to 5.5 V                                                                                                                                                                                                                                                                                                                                                                     |                           |                           |                           |                           |
| Operating ambient temperature               |                       | T <sub>A</sub> = −40 to +85 °C                                                                                                                                                                                                                                                                                                                                                                     |                           |                           |                           |                           |

**Notes** 1. The values in parentheses are the number of signal outputs when 8 com is used.

2. The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

&lt;R&gt;

## CHAPTER 2 PIN FUNCTIONS

### 2.1 Port Function

Pin I/O buffer power supplies depend on the product. The relationship between these power supplies and the pins is shown below.

**Table 2-1. Pin I/O Buffer Power Supplies**

**(1) 32-pin, 44-pin, 48-pin, 52-pin products**

| Power Supply    | Corresponding Pins |
|-----------------|--------------------|
| V <sub>DD</sub> | All pins           |

**(2) 64-pin products**

| Power Supply     | Corresponding Pins                                      |
|------------------|---------------------------------------------------------|
| EV <sub>DD</sub> | • Port pins other than P20, P21, P121 to P124, and P137 |
| V <sub>DD</sub>  | • P20, P21, P121 to P124, and P137<br>• RESET, REGC pin |

Set in each port I/O, buffer, pull-up resistor is also valid for alternate functions.

### 2.1.1 32-pin products

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| Function Name | I/O | Function                                                                                                                                                                                                                                                                                                                                                                                                 | After Reset           | Alternate Function                        |
|---------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-------------------------------------------|
| P10           | I/O | Port 1.<br>8-bit I/O port.<br>P13 and P14 can be set to analog input <sup>Note 1</sup> .<br>Input of P10, P11, P15, and P16 can be set to TTL input buffer.<br>Output of P10, P12, P15, and P17 can be set to N-ch open-drain output ( $V_{DD}$ tolerance).<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port. | Digital input invalid | SCK00/TI07/TO07/KR2/SEG28/(INTP1)         |
| P11           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | SI00/RxD0/TOOLRxD/KR1/SEG29/(INTP2)       |
| P12           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | SO00/TxD0/TOOLTxD/KR0/SEG30/(TI02)/(TO02) |
| P13           |     |                                                                                                                                                                                                                                                                                                                                                                                                          | Analog input port     | ANI18/TI00/SEG31                          |
| P14           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | ANI19/SEG32                               |
| P15           |     |                                                                                                                                                                                                                                                                                                                                                                                                          | Digital input invalid | SCK01/INTP1/SEG4                          |
| P16           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | SI01/INTP2/SEG5                           |
| P17           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | SO01/TI02/TO02/SEG6                       |
| P20           | I/O | Port 2.<br>2-bit I/O port.<br>Can be set to analog input <sup>Note 2</sup> .<br>Input/output can be specified in 1-bit units.                                                                                                                                                                                                                                                                            | Analog input port     | ANI0/AV <sub>REFP</sub>                   |
| P21           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | ANI1/AV <sub>REFM</sub>                   |
| P30           | I/O | Port 3.<br>1-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                                                                                                                                                                                  | Digital input invalid | TI01/TO01/SEG19                           |
| P40           | I/O | Port 4.<br>1-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                                                                                                                                                                                  | Input port            | TOOL0                                     |

<R> **Notes 1.** When the each pin is used as input, specify them as either digital or analog in Port mode control register X (PMCX) (This register can be specified in 1-bit unit).

<R> **2.** Setting digital or analog to each pin can be done in A/D port configuration register (ADPC).

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8. Format of Peripheral I/O Redirection Register (PIOR)**.

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| Function Name | I/O   | Function                                                                                                                                                                 | After Reset              | Alternate Function         |
|---------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|----------------------------|
| P60           | I/O   | Port 6.<br>2-bit I/O port.<br>Input/output can be specified in 1-bit units.                                                                                              | Digital input<br>invalid | SCLA0/SEG21                |
| P61           |       |                                                                                                                                                                          |                          | SDAA0/SEG20                |
| P121          | Input | Port 12.<br>2-bit I/O port and 2-bit input port.<br>For only P126 and P127, input/output can be specified in 1-bit units.                                                | Input port               | X1                         |
| P122          |       |                                                                                                                                                                          |                          | X2/EXCLK                   |
| P126          | I/O   | For only P126 and P127, use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                         | Digital input<br>invalid | CAPL                       |
| P127          |       |                                                                                                                                                                          |                          | CAPH                       |
| P137          | Input | Port 13.<br>1-bit input port.                                                                                                                                            | Input port               | INTP0                      |
| P140          | I/O   | Port 14.<br>1-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port. | Digital input<br>invalid | TO00/PCLBUZ0/KR3/<br>SEG27 |

## 2.1.2 44-pin products

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| Function Name | I/O | Function                                                                                                                                                                                                                                                                                                                                                                                                 | After Reset           | Alternate Function                                |
|---------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|---------------------------------------------------|
| P10           | I/O | Port 1.<br>8-bit I/O port.<br>P13 and P14 can be set to analog input <sup>Note 1</sup> .<br>Input of P10, P11, P15, and P16 can be set to TTL input buffer.<br>Output of P10, P12, P15, and P17 can be set to N-ch open-drain output ( $V_{DD}$ tolerance).<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port. | Digital input invalid | SCK00/TI07/TO07/<br>KR2/SEG28/<br>(INTP1)         |
| P11           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | SI00/RxD0/TOOLRxD/<br>KR1/SEG29/<br>(INTP2)       |
| P12           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | SO00/TxD0/<br>TOOLTxD/KR0/SEG30/<br>(TI02)/(TO02) |
| P13           |     |                                                                                                                                                                                                                                                                                                                                                                                                          | Analog input port     | ANI18/SEG31                                       |
| P14           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | ANI19/SEG32                                       |
| P15           |     |                                                                                                                                                                                                                                                                                                                                                                                                          | Digital input invalid | SCK01/INTP1/SEG4                                  |
| P16           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | SI01/INTP2/SEG5                                   |
| P17           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | SO01/TI02/TO02/SEG6                               |
| P20           | I/O | Port 2.<br>2-bit I/O port.<br>Can be set to analog input <sup>Note 2</sup> .<br>Input/output can be specified in 1-bit units.                                                                                                                                                                                                                                                                            | Analog input port     | ANI0/AV <sub>REFP</sub>                           |
| P21           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | ANI1/AV <sub>REFM</sub>                           |
| P30           | I/O | Port 3.<br>3-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                                                                                                                                                                                  | Digital input invalid | TI01/TO01/SEG19                                   |
| P31           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | INTP3/RTC1HZ/<br>SEG18                            |
| P32           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | TI03/TO03/INTP4/<br>SEG17                         |
| P40           | I/O | Port 4.<br>1-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                                                                                                                                                                                  | Input port            | TOOL0                                             |

- <R> **Notes 1.** When the each pin is used as input, specify them as either digital or analog in Port mode control register X (PMCX) (This register can be specified in 1-bit unit).
- <R> **2.** Setting digital or analog to each pin can be done in A/D port configuration register (ADPC).

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8. Format of Peripheral I/O Redirection Register (PIOR)**.

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| Function Name | I/O   | Function                                                                                                                                                                                                                                                                                                             | After Reset              | Alternate Function         |
|---------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|----------------------------|
| P60           | I/O   | Port 6.<br>2-bit I/O port.<br>Input/output can be specified in 1-bit units.                                                                                                                                                                                                                                          | Digital input<br>invalid | SCLA0/SEG21                |
| P61           |       |                                                                                                                                                                                                                                                                                                                      |                          | SDAA0/SEG20                |
| P120          | I/O   | Port 12.<br>4-bit I/O port and 4-bit input port.<br>P120 can be set to analog input <sup>Note</sup> .<br>For only P120, and P125 to P127, input/output can be specified in 1-bit units.<br>For only P120, and P125 to P127, use of an on-chip pull-up resistor can be specified by a software setting at input port. | Analog input<br>port     | ANI17/SEG25                |
| P121          | Input |                                                                                                                                                                                                                                                                                                                      | Input port               | X1                         |
| P122          |       |                                                                                                                                                                                                                                                                                                                      |                          | X2/EXCLK                   |
| P123          |       |                                                                                                                                                                                                                                                                                                                      |                          | XT1                        |
| P124          |       |                                                                                                                                                                                                                                                                                                                      |                          | XT2/EXCLKS                 |
| P125          | I/O   |                                                                                                                                                                                                                                                                                                                      | Digital input<br>invalid | VL3                        |
| P126          |       |                                                                                                                                                                                                                                                                                                                      |                          | CAPL                       |
| P127          |       |                                                                                                                                                                                                                                                                                                                      |                          | CAPH                       |
| P137          | Input | Port 13.<br>1-bit input port.                                                                                                                                                                                                                                                                                        | Input port               | INTP0                      |
| P140          | I/O   | Port 14.<br>4-bit I/O port.<br>P142 and P143 can be set to analog input <sup>Note</sup> .<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                               | Digital input<br>invalid | TO00/PCLBUZ0/KR3/<br>SEG27 |
| P141          |       |                                                                                                                                                                                                                                                                                                                      |                          | TI00/PCLBUZ1/SEG26         |
| P142          |       |                                                                                                                                                                                                                                                                                                                      | Analog input<br>port     | ANI20/SEG33                |
| P143          |       |                                                                                                                                                                                                                                                                                                                      |                          | ANI21/SEG34                |

<R> **Note** When the each pin is used as input, specify them as either digital or analog in Port mode control register X (PMCX) (This register can be specified in 1-bit unit).



## 2.1.3 48-pin products

(1/2)

| Function Name | I/O | Function                                                                                                                                                                                                                                                                                                                                                                                                 | After Reset           | Alternate Function                    |
|---------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|---------------------------------------|
| P10           | I/O | Port 1.<br>8-bit I/O port.<br>P13 and P14 can be set to analog input <sup>Note 1</sup> .<br>Input of P10, P11, P15, and P16 can be set to TTL input buffer.<br>Output of P10, P12, P15, and P17 can be set to N-ch open-drain output ( $V_{DD}$ tolerance).<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port. | Digital input invalid | SCK00/TI07/TO07/SEG28/(INTP1)         |
| P11           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | SI00/RxD0/TOOLRxD/SEG29/(INTP2)       |
| P12           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | SO00/TxD0/TOOLTxD/SEG30/(TI02)/(TO02) |
| P13           |     |                                                                                                                                                                                                                                                                                                                                                                                                          | Analog input port     | ANI18/SEG31                           |
| P14           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | ANI19/SEG32                           |
| P15           |     |                                                                                                                                                                                                                                                                                                                                                                                                          | Digital input invalid | SCK01/INTP1/SEG4                      |
| P16           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | SI01/INTP2/SEG5                       |
| P17           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | SO01/TI02/TO02/SEG6                   |
| P20           | I/O | Port 2.<br>2-bit I/O port.<br>Can be set to analog input <sup>Note 2</sup> .<br>Input/output can be specified in 1-bit units.                                                                                                                                                                                                                                                                            | Analog input port     | ANI0/AV <sub>REFP</sub>               |
| P21           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | ANI1/AV <sub>REFM</sub>               |
| P30           | I/O | Port 3.<br>3-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                                                                                                                                                                                  | Digital input invalid | TI01/TO01/KR3/SEG19                   |
| P31           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | INTP3/RTC1HZ/KR2/SEG18                |
| P32           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | TI03/TO03/INTP4/KR1/SEG17             |
| P40           | I/O | Port 4.<br>2-bit I/O port.<br>P41 can be set to analog input <sup>Note 1</sup> .<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                                                                                                                            | Input port            | TOOL0                                 |
| P41           |     |                                                                                                                                                                                                                                                                                                                                                                                                          | Analog input port     | ANI16/TI04/TO04/SEG24                 |

<R> **Notes 1.** When the each pin is used as input, specify them as either digital or analog in Port mode control register X (PMCX) (This register can be specified in 1-bit unit).

<R> **2.** Setting digital or analog to each pin can be done in A/D port configuration register (ADPC).

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8. Format of Peripheral I/O Redirection Register (PIOR)**.

(2/2)

| Function Name | I/O   | Function                                                                                                                                                                                                                                                                                                         | After Reset           | Alternate Function       |
|---------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|--------------------------|
| P50           | I/O   | Port 5.<br>1-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                                                                                          | Digital input invalid | INTP5/SEG7/<br>(PCLBUZ0) |
| P60           | I/O   | Port 6.<br>2-bit I/O port.<br>Input/output can be specified in 1-bit units.                                                                                                                                                                                                                                      | Digital input invalid | SCLA0/SEG21              |
| P61           |       |                                                                                                                                                                                                                                                                                                                  |                       | SDAA0/SEG20              |
| P70           | I/O   | Port 7.<br>1-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                                                                                          | Digital input invalid | KR0/SEG16                |
| P120          | I/O   | Port 12.<br>4-bit I/O port and 4-bit input port.<br>P120 can be set to analog input <sup>Note</sup> .<br>For only P120, and P125 to P127, input/output can be specified in 1-bit units.<br>For only P120, P125 to P127, use of an on-chip pull-up resistor can be specified by a software setting at input port. | Analog input port     | ANI17/SEG25              |
| P121          | Input |                                                                                                                                                                                                                                                                                                                  | Input port            | X1                       |
| P122          |       |                                                                                                                                                                                                                                                                                                                  |                       | X2/EXCLK                 |
| P123          |       |                                                                                                                                                                                                                                                                                                                  |                       | XT1                      |
| P124          |       |                                                                                                                                                                                                                                                                                                                  |                       | XT2/EXCLKS               |
| P125          | I/O   |                                                                                                                                                                                                                                                                                                                  | Digital input invalid | V <sub>L3</sub>          |
| P126          |       |                                                                                                                                                                                                                                                                                                                  |                       | CAPL                     |
| P127          |       |                                                                                                                                                                                                                                                                                                                  |                       | CAPH                     |
| P137          | Input | Port 13.<br>1-bit input port.                                                                                                                                                                                                                                                                                    | Input port            | INTP0                    |
| P140          | I/O   | Port 14.<br>5-bit I/O port.<br>P142 to p144 can be set to analog input <sup>Note</sup> .<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                            | Digital input invalid | TO00/PCLBUZ0/<br>SEG27   |
| P141          |       |                                                                                                                                                                                                                                                                                                                  |                       | TI00/PCLBUZ1/SEG26       |
| P142          |       |                                                                                                                                                                                                                                                                                                                  | Analog input port     | ANI20/SEG33              |
| P143          |       |                                                                                                                                                                                                                                                                                                                  |                       | ANI21/SEG34              |
| P144          |       |                                                                                                                                                                                                                                                                                                                  |                       | ANI22/SEG35              |

<R> **Note** When the each pin is used as input, specify them as either digital or analog in Port mode control register X (PMCX) (This register can be specified in 1-bit unit).

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8. Format of Peripheral I/O Redirection Register (PIOR)**.

## 2.1.4 52-pin products

(1/2)

| Function Name | I/O | Function                                                                                                                                                                                                                                                                                                                                                                                                 | After Reset           | Alternate Function                            |
|---------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-----------------------------------------------|
| P10           | I/O | Port 1.<br>8-bit I/O port.<br>P13 and P14 can be set to analog input <sup>Note 1</sup> .<br>Input of P10, P11, P15, and P16 can be set to TTL input buffer.<br>Output of P10, P12, P15, and P17 can be set to N-ch open-drain output ( $V_{DD}$ tolerance).<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port. | Digital input invalid | SCK00/<br>TI07/TO07/SEG28/<br>(INTP1)         |
| P11           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | SI00/RxD0/<br>TOOLRxD/SEG29/<br>(INTP2)       |
| P12           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | SO00/TxD0/<br>TOOLTxD/SEG30/<br>(TI02)/(TO02) |
| P13           |     |                                                                                                                                                                                                                                                                                                                                                                                                          | Analog input port     | ANI18/SEG31                                   |
| P14           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | ANI19/SEG32                                   |
| P15           |     |                                                                                                                                                                                                                                                                                                                                                                                                          | Digital input invalid | SCK01/INTP1/SEG4                              |
| P16           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | SI01/INTP2/SEG5                               |
| P17           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | SO01/TI02/TO02/<br>SEG6                       |
| P20           | I/O | Port 2.<br>2-bit I/O port.<br>Can be set to analog input <sup>Note 2</sup> .<br>Input/output can be specified in 1-bit units.                                                                                                                                                                                                                                                                            | Analog input port     | ANI0/AV <sub>REFP</sub>                       |
| P21           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | ANI1/AV <sub>REFM</sub>                       |
| P30           | I/O | Port 3.<br>3-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                                                                                                                                                                                  | Digital input invalid | TI01/TO01/KR3/<br>SEG19                       |
| P31           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | INTP3/RTC1HZ/<br>KR2/SEG18                    |
| P32           |     |                                                                                                                                                                                                                                                                                                                                                                                                          |                       | TI03/TO03/INTP4/<br>SEG17                     |
| P40           | I/O | Port 4.<br>3-bit I/O port.<br>P41 can be set to analog input <sup>Note 1</sup> .<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                                                                                                                            | Input port            | TOOL0                                         |
| P41           |     |                                                                                                                                                                                                                                                                                                                                                                                                          | Analog input port     | ANI16/TI04/TO04/<br>SEG24                     |
| P42           |     |                                                                                                                                                                                                                                                                                                                                                                                                          | Digital input invalid | TI05/TO05/SEG23                               |

<R> **Notes 1.** When the each pin is used as input, specify them as either digital or analog in Port mode control register X (PMCX) (This register can be specified in 1-bit unit).

<R> **2.** Setting digital or analog to each pin can be done in A/D port configuration register (ADPC).

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8. Format of Peripheral I/O Redirection Register (PIOR)**.

(2/2)

| Function Name | I/O   | Function                                                                                                                                                                                                                                                                                                                                                                         | After Reset              | Alternate Function       |
|---------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|--------------------------|
| P50           | I/O   | Port 5.<br>2-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                                                                                                                                                          | Digital input<br>invalid | INTP5/SEG7/<br>(PCLBUZ0) |
| P51           |       |                                                                                                                                                                                                                                                                                                                                                                                  |                          | TI06/TO06/SEG8           |
| P60           | I/O   | Port 6.<br>2-bit I/O port.<br>Input/output can be specified in 1-bit units.                                                                                                                                                                                                                                                                                                      | Digital input<br>invalid | SCLA0/SEG21              |
| P61           |       |                                                                                                                                                                                                                                                                                                                                                                                  |                          | SDAA0/SEG20              |
| P70           | I/O   | Port 7.<br>2-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                                                                                                                                                          | Digital input<br>invalid | KR0/SEG16                |
| P71           |       |                                                                                                                                                                                                                                                                                                                                                                                  |                          | KR1/SEG15                |
| P120          | I/O   | Port 12.<br>4-bit I/O port and 4-bit input port.<br>P120 can be set to analog input <sup>Note</sup> .<br>For only P120, input/output can be specified in 1-bit units.<br>For only P120, and P125 to P127, input/output can be specified in 1-bit units.<br>For only P120, P125 to P127, use of an on-chip pull-up resistor can be specified by a software setting at input port. | Analog input<br>port     | ANI17/SEG25              |
| P121          | Input |                                                                                                                                                                                                                                                                                                                                                                                  | Input port               | X1                       |
| P122          |       |                                                                                                                                                                                                                                                                                                                                                                                  |                          | X2/EXCLK                 |
| P123          |       |                                                                                                                                                                                                                                                                                                                                                                                  |                          | XT1                      |
| P124          |       |                                                                                                                                                                                                                                                                                                                                                                                  |                          | XT2/EXCLKS               |
| P125          | I/O   |                                                                                                                                                                                                                                                                                                                                                                                  | Digital input<br>invalid | V <sub>L3</sub>          |
| P126          |       |                                                                                                                                                                                                                                                                                                                                                                                  |                          | CAPL                     |
| P127          |       |                                                                                                                                                                                                                                                                                                                                                                                  |                          | CAPH                     |
| P137          | Input | Port 13.<br>1-bit input port.                                                                                                                                                                                                                                                                                                                                                    | Input port               | INTP0                    |
| P140          | I/O   | Port 14.<br>6-bit I/O port.<br>P142 to P145 can be set to analog input <sup>Note</sup> .<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                                                                                            | Digital input<br>invalid | TO00/PCLBUZ0/<br>SEG27   |
| P141          |       |                                                                                                                                                                                                                                                                                                                                                                                  |                          | TI00/PCLBUZ1/SEG26       |
| P142          |       |                                                                                                                                                                                                                                                                                                                                                                                  | Analog input<br>port     | ANI20/SEG33              |
| P143          |       |                                                                                                                                                                                                                                                                                                                                                                                  |                          | ANI21/SEG34              |
| P144          |       |                                                                                                                                                                                                                                                                                                                                                                                  |                          | ANI22/SEG35              |
| P145          |       |                                                                                                                                                                                                                                                                                                                                                                                  |                          | ANI23/SEG36              |

<R> **Note** When the each pin is used as input, specify them as either digital or analog in Port mode control register X (PMCX) (This register can be specified in 1-bit unit).

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8. Format of Peripheral I/O Redirection Register (PIOR)**.

## 2.1.5 64-pin products

(1/2)

| Function Name | I/O | Function                                                                                                                                                                                                                                                                                                                                                                                                        | After Reset           | Alternate Function      |
|---------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-------------------------|
| P10           | I/O | Port 1.<br>8-bit I/O port.<br>P13 and P14 can be set to analog input <sup>Note 1</sup> .<br>Input of P10, P11, P15, and P16 can be set to TTL input buffer.<br>Output of P10, P12, P15, and P17 can be set to N-ch open-drain output (EV <sub>DD</sub> tolerance).<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port. | Digital input invalid | SCK00/SEG28             |
| P11           |     |                                                                                                                                                                                                                                                                                                                                                                                                                 |                       | SI00/RxD0/TOOLRxD/SEG29 |
| P12           |     |                                                                                                                                                                                                                                                                                                                                                                                                                 |                       | SO00/TxD0/TOOLTxD/SEG30 |
| P13           |     |                                                                                                                                                                                                                                                                                                                                                                                                                 | Analog input port     | ANI18/SEG31             |
| P14           |     |                                                                                                                                                                                                                                                                                                                                                                                                                 |                       | ANI19/SEG32             |
| P15           |     |                                                                                                                                                                                                                                                                                                                                                                                                                 | Digital input invalid | SCK01/INTP1/SEG4        |
| P16           |     |                                                                                                                                                                                                                                                                                                                                                                                                                 |                       | SI01/INTP2/SEG5         |
| P17           |     |                                                                                                                                                                                                                                                                                                                                                                                                                 |                       | SO01/TI02/TO02/SEG6     |
| P20           | I/O | Port 2.<br>2-bit I/O port.<br>Can be set to analog input <sup>Note 2</sup> .<br>Input/output can be specified in 1-bit units.                                                                                                                                                                                                                                                                                   | Analog input port     | ANI0/AV <sub>REFP</sub> |
| P21           |     |                                                                                                                                                                                                                                                                                                                                                                                                                 |                       | ANI1/AV <sub>REFM</sub> |
| P30           | I/O | Port 3.<br>3-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                                                                                                                                                                                         | Digital input invalid | TI01/TO01/SEG19         |
| P31           |     |                                                                                                                                                                                                                                                                                                                                                                                                                 |                       | INTP3/RTC1HZ/SEG18      |
| P32           |     |                                                                                                                                                                                                                                                                                                                                                                                                                 |                       | TI03/TO03/INTP4/SEG17   |
| P40           | I/O | Port 4.<br>4-bit I/O port.<br>P41 can be set to analog input <sup>Note 1</sup> .<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                                                                                                                                   | Input port            | TOOL0                   |
| P41           |     |                                                                                                                                                                                                                                                                                                                                                                                                                 | Analog input port     | ANI16/TI04/TO04/SEG24   |
| P42           |     |                                                                                                                                                                                                                                                                                                                                                                                                                 | Digital input invalid | TI05/TO05/SEG23         |
| P43           |     |                                                                                                                                                                                                                                                                                                                                                                                                                 |                       | INTP7/SEG22             |

- <R> **Notes 1.** When the each pin is used as input, specify them as either digital or analog in Port mode control register X (PMCX) (This register can be specified in 1-bit unit).
- <R> **2.** Setting digital or analog to each pin can be done in A/D port configuration register (ADPC).

(2/2)

| Function Name | I/O    | Function                                                                                                                                                                                                                                                                                                         | After Reset                                         | Alternate Function              |       |
|---------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------|---------------------------------|-------|
| P50           | I/O    | Port 5.<br>5-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                                                                                          | Digital input<br>invalid                            | INTP5/SEG7/<br>(PCLBUZ0)        |       |
| P51           |        |                                                                                                                                                                                                                                                                                                                  |                                                     | TI06/TO06/<br>SEG8              |       |
| P52           |        |                                                                                                                                                                                                                                                                                                                  |                                                     | INTP6/SEG9                      |       |
| P53           |        |                                                                                                                                                                                                                                                                                                                  |                                                     | TI07/TO07/SEG10/<br>(INTP1)     |       |
| P54           |        |                                                                                                                                                                                                                                                                                                                  |                                                     | SEG11/(TI02)/<br>(TO02)/(INTP2) |       |
| P60           | I/O    | Port 6.<br>2-bit I/O port.<br>Input/output can be specified in 1-bit units.                                                                                                                                                                                                                                      | Digital input<br>invalid                            | SCLA0/SEG21                     |       |
| P61           |        |                                                                                                                                                                                                                                                                                                                  |                                                     | SDAA0/SEG20                     |       |
| P70           | I/O    | Port 7.<br>5-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                                                                                          | Digital input<br>invalid                            | KR0/SEG16                       |       |
| P71           |        |                                                                                                                                                                                                                                                                                                                  |                                                     | KR1/SEG15                       |       |
| P72           |        |                                                                                                                                                                                                                                                                                                                  |                                                     | KR2/SEG14                       |       |
| P73           |        |                                                                                                                                                                                                                                                                                                                  |                                                     | KR3/SEG13                       |       |
| P74           |        |                                                                                                                                                                                                                                                                                                                  |                                                     | SEG12                           |       |
| P120          | I/O    | Port 12.<br>4-bit I/O port and 4-bit input port.<br>P120 can be set to analog input <sup>Note</sup> .<br>For only P120, and P125 to P127, input/output can be specified in 1-bit units.<br>For only P120, P125 to P127, use of an on-chip pull-up resistor can be specified by a software setting at input port. | Analog input<br>port                                | ANI17/SEG25                     |       |
| P121          | Input  |                                                                                                                                                                                                                                                                                                                  | Input port                                          | X1                              |       |
| P122          |        |                                                                                                                                                                                                                                                                                                                  |                                                     | X2/EXCLK                        |       |
| P123          |        |                                                                                                                                                                                                                                                                                                                  |                                                     | XT1                             |       |
| P124          |        |                                                                                                                                                                                                                                                                                                                  |                                                     | XT2/EXCLKS                      |       |
| P125          | I/O    |                                                                                                                                                                                                                                                                                                                  | Digital input<br>invalid                            | V <sub>L3</sub>                 |       |
| P126          |        |                                                                                                                                                                                                                                                                                                                  |                                                     | CAPL                            |       |
| P127          |        |                                                                                                                                                                                                                                                                                                                  |                                                     | CAPH                            |       |
| P130          | Output |                                                                                                                                                                                                                                                                                                                  | Port 13.<br>1-bit output port and 1-bit input port. | Output port                     | —     |
| P137          | Input  |                                                                                                                                                                                                                                                                                                                  |                                                     | Input port                      | INTP0 |
| P140          | I/O    | Port 14.<br>8-bit I/O port.<br>P142 to P145 can be set to analog input <sup>Note</sup> .<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting at input port.                                                                            | Digital input<br>invalid                            | TO00/PCLBUZ0/<br>SEG27/(INTP6)  |       |
| P141          |        |                                                                                                                                                                                                                                                                                                                  |                                                     | TI00/PCLBUZ1/<br>SEG26/(INTP7)  |       |
| P142          |        |                                                                                                                                                                                                                                                                                                                  | Analog input<br>port                                | ANI20/SEG33                     |       |
| P143          |        |                                                                                                                                                                                                                                                                                                                  |                                                     | ANI21/SEG34                     |       |
| P144          |        |                                                                                                                                                                                                                                                                                                                  |                                                     | ANI22/SEG35                     |       |
| P145          |        |                                                                                                                                                                                                                                                                                                                  |                                                     | ANI23/SEG36                     |       |
| P146          |        |                                                                                                                                                                                                                                                                                                                  | Digital input<br>invalid                            | SEG37                           |       |
| P147          |        |                                                                                                                                                                                                                                                                                                                  |                                                     | SEG38                           |       |

<R> **Note** When the each pin is used as input, specify them as either digital or analog in Port mode control register X (PMCX) (This register can be specified in 1-bit unit).

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8. Format of Peripheral I/O Redirection Register (PIOR)**.

## 2.1.6 Pins for each product (pins other than port pins)

(1/5)

| Function Name   | I/O    | Function                                                                         | 64-pin | 52-pin | 48-pin | 44-pin | 32-pin |
|-----------------|--------|----------------------------------------------------------------------------------|--------|--------|--------|--------|--------|
| ANI0            | Input  | A/D converter analog input                                                       | √      | √      | √      | √      | √      |
| ANI1            |        |                                                                                  | √      | √      | √      | √      | √      |
| ANI16           |        |                                                                                  | √      | √      | √      | –      | –      |
| ANI17           |        |                                                                                  | √      | √      | √      | √      | –      |
| ANI18           |        |                                                                                  | √      | √      | √      | √      | √      |
| ANI19           |        |                                                                                  | √      | √      | √      | √      | √      |
| ANI20           |        |                                                                                  | √      | √      | √      | √      | –      |
| ANI21           |        |                                                                                  | √      | √      | √      | √      | –      |
| ANI22           |        |                                                                                  | √      | √      | √      | –      | –      |
| ANI23           |        |                                                                                  | √      | √      | –      | –      | –      |
| CAPH            | –      | Connecting a capacitor for LCD controller/driver                                 | √      | √      | √      | √      | √      |
| CAPL            |        |                                                                                  | √      | √      | √      | √      | √      |
| COM0            | Output | LCD controller/driver common signal outputs                                      | √      | √      | √      | √      | √      |
| COM1            |        |                                                                                  | √      | √      | √      | √      | √      |
| COM2            |        |                                                                                  | √      | √      | √      | √      | √      |
| COM3            |        |                                                                                  | √      | √      | √      | √      | √      |
| COM4            |        |                                                                                  | √      | √      | √      | √      | –      |
| COM5            |        |                                                                                  | √      | √      | √      | √      | –      |
| COM6            |        |                                                                                  | √      | √      | √      | √      | –      |
| COM7            |        |                                                                                  | √      | √      | √      | √      | –      |
| COMEXP          | Output | LCD controller/driver common signal outputs for memory-type liquid crystal panel | √      | √      | √      | √      | √      |
| V <sub>L1</sub> | –      | LCD drive voltage                                                                | √      | √      | √      | √      | √      |
| V <sub>L2</sub> |        |                                                                                  | √      | √      | √      | √      | √      |
| V <sub>L3</sub> |        |                                                                                  | √      | √      | √      | √      | –      |
| V <sub>L4</sub> |        |                                                                                  | √      | √      | √      | √      | √      |
| SEG0            | Output | LCD controller/driver segment signal outputs                                     | √      | √      | √      | √      | √      |
| SEG1            |        |                                                                                  | √      | √      | √      | √      | –      |
| SEG2            |        |                                                                                  | √      | √      | √      | √      | –      |
| SEG3            |        |                                                                                  | √      | √      | √      | √      | –      |
| SEG4            |        |                                                                                  | √      | √      | √      | √      | √      |
| SEG5            |        |                                                                                  | √      | √      | √      | √      | √      |
| SEG6            |        |                                                                                  | √      | √      | √      | √      | √      |
| SEG7            |        |                                                                                  | √      | √      | √      | –      | –      |
| SEG8            |        |                                                                                  | √      | √      | –      | –      | –      |
| SEG9            |        |                                                                                  | √      | –      | –      | –      | –      |

**Remark** √: Mounted  
 –: Not mounted

(2/5)

| Function Name | I/O    | Function                                     | 64-pin | 52-pin | 48-pin | 44-pin | 32-pin |
|---------------|--------|----------------------------------------------|--------|--------|--------|--------|--------|
| SEG10         | Output | LCD controller/driver segment signal outputs | √      | –      | –      | –      | –      |
| SEG11         |        |                                              | √      | –      | –      | –      | –      |
| SEG12         |        |                                              | √      | –      | –      | –      | –      |
| SEG13         |        |                                              | √      | –      | –      | –      | –      |
| SEG14         |        |                                              | √      | –      | –      | –      | –      |
| SEG15         |        |                                              | √      | √      | –      | –      | –      |
| SEG16         |        |                                              | √      | √      | √      | –      | –      |
| SEG17         |        |                                              | √      | √      | √      | √      | –      |
| SEG18         |        |                                              | √      | √      | √      | √      | –      |
| SEG19         |        |                                              | √      | √      | √      | √      | √      |
| SEG20         |        |                                              | √      | √      | √      | √      | √      |
| SEG21         |        |                                              | √      | √      | √      | √      | √      |
| SEG22         |        |                                              | √      | –      | –      | –      | –      |
| SEG23         |        |                                              | √      | √      | –      | –      | –      |
| SEG24         |        |                                              | √      | √      | √      | –      | –      |
| SEG25         |        |                                              | √      | √      | √      | √      | –      |
| SEG26         |        |                                              | √      | √      | √      | √      | –      |
| SEG27         |        |                                              | √      | √      | √      | √      | √      |
| SEG28         |        |                                              | √      | √      | √      | √      | √      |
| SEG29         |        |                                              | √      | √      | √      | √      | √      |
| SEG30         |        |                                              | √      | √      | √      | √      | √      |
| SEG31         |        |                                              | √      | √      | √      | √      | √      |
| SEG32         |        |                                              | √      | √      | √      | √      | √      |
| SEG33         |        |                                              | √      | √      | √      | √      | –      |
| SEG34         |        |                                              | √      | √      | √      | √      | –      |
| SEG35         |        |                                              | √      | √      | √      | –      | –      |
| SEG36         |        |                                              | √      | √      | –      | –      | –      |
| SEG37         |        |                                              | √      | –      | –      | –      | –      |
| SEG38         |        |                                              | √      | –      | –      | –      | –      |

**Remark** √: Mounted  
 –: Not mounted



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| Function Name | I/O    | Function                                                                                                                                              | 64-pin | 52-pin | 48-pin | 44-pin | 32-pin |
|---------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|--------|--------|--------|
| INTP0         | Input  | External interrupt request input                                                                                                                      | √      | √      | √      | √      | √      |
| INTP1         |        |                                                                                                                                                       | √      | √      | √      | √      | √      |
| INTP2         |        |                                                                                                                                                       | √      | √      | √      | √      | √      |
| INTP3         |        |                                                                                                                                                       | √      | √      | √      | √      | –      |
| INTP4         |        |                                                                                                                                                       | √      | √      | √      | √      | –      |
| INTP5         |        |                                                                                                                                                       | √      | √      | √      | –      | –      |
| INTP6         |        |                                                                                                                                                       | √      | –      | –      | –      | –      |
| INTP7         |        |                                                                                                                                                       | √      | –      | –      | –      | –      |
| KR0           | Input  | Key interrupt input                                                                                                                                   | √      | √      | √      | √      | √      |
| KR1           |        |                                                                                                                                                       | √      | √      | √      | √      | √      |
| KR2           |        |                                                                                                                                                       | √      | √      | √      | √      | √      |
| KR3           |        |                                                                                                                                                       | √      | √      | √      | √      | √      |
| PCLBUZ0       | Output | Clock output/buzzer output                                                                                                                            | √      | √      | √      | √      | √      |
| PCLBUZ1       |        |                                                                                                                                                       | √      | √      | √      | √      | –      |
| REGC          | –      | Connecting regulator output stabilization capacitance for internal operation. Connect to V <sub>SS</sub> via a capacitor (0.47 to 1 $\mu$ F: target). | √      | √      | √      | √      | √      |
| RTC1HZ        | Output | Real-time clock correction clock (1 Hz) output                                                                                                        | √      | √      | √      | √      | –      |
| RESET         | Input  | System reset input                                                                                                                                    | √      | √      | √      | √      | √      |
| RxD0          | Input  | Serial data input to UART0                                                                                                                            | √      | √      | √      | √      | √      |
| SCK00         | I/O    | Clock input/output for CSI00 and CSI01                                                                                                                | √      | √      | √      | √      | √      |
| SCK01         |        |                                                                                                                                                       | √      | √      | √      | √      | √      |
| SCLA0         | I/O    | Clock input/output for I <sup>2</sup> C                                                                                                               | √      | √      | √      | √      | √      |
| SDAA0         | I/O    | Serial data I/O for I <sup>2</sup> C                                                                                                                  | √      | √      | √      | √      | √      |
| SI00          | Input  | Serial data input to CSI00 and CSI01                                                                                                                  | √      | √      | √      | √      | √      |
| SI01          |        |                                                                                                                                                       | √      | √      | √      | √      | √      |
| SO00          | Output | Serial data output from CSI00 and CSI01                                                                                                               | √      | √      | √      | √      | √      |
| SO01          |        |                                                                                                                                                       | √      | √      | √      | √      | √      |

**Remark** √: Mounted

–: Not mounted

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| Function Name | I/O    | Function                                      | 64-pin | 52-pin | 48-pin | 44-pin | 32-pin |
|---------------|--------|-----------------------------------------------|--------|--------|--------|--------|--------|
| TI00          | Input  | External count clock input to 16-bit timer 00 | √      | √      | √      | √      | √      |
| TI01          |        | External count clock input to 16-bit timer 01 | √      | √      | √      | √      | √      |
| TI02          |        | External count clock input to 16-bit timer 02 | √      | √      | √      | √      | √      |
| TI03          |        | External count clock input to 16-bit timer 03 | √      | √      | √      | √      | –      |
| TI04          |        | External count clock input to 16-bit timer 04 | √      | √      | √      | –      | –      |
| TI05          |        | External count clock input to 16-bit timer 05 | √      | √      | –      | –      | –      |
| TI06          |        | External count clock input to 16-bit timer 06 | √      | √      | –      | –      | –      |
| TI07          |        | External count clock input to 16-bit timer 07 | √      | √      | √      | √      | √      |
| TO00          | Output | 16-bit timer 00 output                        | √      | √      | √      | √      | √      |
| TO01          |        | 16-bit timer 01 output                        | √      | √      | √      | √      | √      |
| TO02          |        | 16-bit timer 02 output                        | √      | √      | √      | √      | √      |
| TO03          |        | 16-bit timer 03 output                        | √      | √      | √      | √      | –      |
| TO04          |        | 16-bit timer 04 output                        | √      | √      | √      | –      | –      |
| TO05          |        | 16-bit timer 05 output                        | √      | √      | –      | –      | –      |
| TO06          |        | 16-bit timer 06 output                        | √      | √      | –      | –      | –      |
| TO07          |        | 16-bit timer 07 output                        | √      | √      | √      | √      | √      |
| TxD0          | Output | Serial data output from UART0                 | √      | √      | √      | √      | √      |
| X1            | –      | Resonator connection for main system clock    | √      | √      | √      | √      | √      |
| X2            | –      |                                               | √      | √      | √      | √      | √      |
| EXCLK         | Input  | External clock input for main system clock    | √      | √      | √      | √      | √      |
| EXCLKS        | Input  | External clock input for subsystem clock      | √      | √      | √      | √      | –      |
| XT1           | –      | Resonator connection for subsystem clock      | √      | √      | √      | √      | –      |
| XT2           | –      |                                               | √      | √      | √      | √      | –      |

**Remark** √: Mounted  
 –: Not mounted

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| Function Name       | I/O    | Function                                                                                                                                                                        | 64-pin | 52-pin | 48-pin | 44-pin | 32-pin |
|---------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|--------|--------|--------|
| V <sub>DD</sub>     | –      | <32-pin, 44-pin, 48-pin, 52-pin><br>Positive power supply for all pins<br><64-pin ><br>Positive power supply for P20, P21, P121 to P124, P137 and $\overline{\text{RESET}}$ pin | √      | √      | √      | √      | √      |
| EV <sub>DD</sub>    | –      | <64-pin><br>Positive power supply for ports (other than P20, P21, P121 to P124, P137) and pins other ports (except for the $\overline{\text{RESET}}$ pin)                       | √      | –      | –      | –      | –      |
| AV <sub>REFP</sub>  | Input  | A/D converter reference potential (+ side) input                                                                                                                                | √      | √      | √      | √      | √      |
| AV <sub>REFM</sub>  | Input  | A/D converter reference potential (– side) input                                                                                                                                | √      | √      | √      | √      | √      |
| V <sub>SS</sub>     | –      | <32-pin, 44-pin, 48-pin, 52-pin><br>Ground potential for all pins<br><64-pin><br>Ground potential for P20, P21, P121 to P124, P137 and $\overline{\text{RESET}}$ pin            | √      | √      | √      | √      | √      |
| EV <sub>SS</sub>    | –      | <64-pin ><br>Ground potential for ports (other than P20, P21, P121 to P124, P137) and pins other ports (except for the $\overline{\text{RESET}}$ pin)                           | √      | –      | –      | –      | –      |
| TOOLRx <sub>D</sub> | Input  | UART reception pin for the external device connection used during flash memory programming                                                                                      | √      | √      | √      | √      | √      |
| TOOLTxD             | Output | UART transmission pin for the external device connection used during flash memory programming                                                                                   | √      | √      | √      | √      | √      |
| TOOL0               | I/O    | Data I/O for flash memory programmer/debugger                                                                                                                                   | √      | √      | √      | √      | √      |

**Remark** √: Mounted  
 –: Not mounted

## 2.2 Description of Pin Functions

**Remark** The pins mounted depend on the product. See **1.3 Pin Configuration (Top View)** and **2.1 Port Function**.

### 2.2.1 P10 to P17 (port 1)

P10 to P17 function as an I/O port. These pins also function as serial interface data I/O, serial interface clock I/O, programming UART I/O, timer I/O, segment output of LCD controller/driver, external interrupt request input and A/D converter analog input.

Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 1 (PU1).

Input to the P10, P11, P15 and P16 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units, using port input mode register 1 (PIM1).

Output from the P10, P12, P15, P17 pins can be specified as normal CMOS output or N-ch open-drain output ( $V_{DD}$  tolerance<sup>Note 1</sup>/EV $V_{DD}$  tolerance<sup>Note 2</sup>) in 1-bit units, using port output mode register 1 (POM1).

Input to the P13 and P14 pins can be specified as analog input or digital input in 1-bit units, using port mode control register 1 (PMC1). This register can be specified in 1-bit unit.

The following operation modes can be specified in 1-bit units.

- Notes**
1. 32, 44, 48, 52-pin products :  $V_{DD}$  tolerance
  2. 64-pin products : EV $V_{DD}$  tolerance

#### (1) Port mode

P10 to P17 function as an I/O port. P10 to P17 can be set to input or output port in 1-bit units using port mode register 1 (PM1).

#### (2) Control mode

P10 to P17 function as serial interface data I/O, serial interface clock I/O, programming UART I/O, timer I/O, segment output of LCD controller/driver, external interrupt request input and A/D converter analog input.

##### (a) INTP1, INTP2

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

##### (b) TxD0

This is a serial data output pin of serial interface UART0.

##### (c) RxD0

This is a serial data input pin of serial interface UART0.

##### (d) SCK00, SCK01

These are the serial clock I/O pins of serial interface CSI00 and CSI01.

##### (e) SI00, SI01

These are the serial data input pins of serial interface CSI00 and CSI01.

##### (f) SO00, SO01

These are the serial data output pins of serial interface CSI00 and CSI01.

##### (g) TI02

This is a pin for inputting an external count clock/capture trigger to 16-bit timer 02.

##### (h) TO02

This is a timer output pin from 16-bit timers 02.

**(i) TOOLTxD**

This UART serial data output pin for an external device connection is used during flash memory programming.

**(j) TOOLRxD**

This UART serial data input pin for an external device connection is used during flash memory programming.

**(k) SEG4 to SEG6, SEG28 to SEG32**

These are the segment output pins of LCD controller/driver.

**(l) ANI18, ANI19**

These are the analog input pins (ANI18, ANI19) of A/D converter.

When using this pin as analog input pin, see **Figure 11-41. Analog Input Pin Connection**.

### 2.2.2 P20 and P21 (port 2)

P20 and P21 function as an I/O port. These pins also function as A/D converter analog input and reference voltage input.

Setting digital or analog to each pin can be done in A/D port configuration register (ADPC).

The following operation modes can be specified in 1-bit units.

**(1) Port mode**

P20 and P21 function as an I/O port. P20 and P21 can be set to input or output port in 1-bit units using port mode register 2 (PM2).

**(2) Control mode**

P20 to P27 function as A/D converter analog input and reference voltage input.

**(a) ANI0, ANI1**

These are the analog input pins (ANI0, ANI1) of A/D converter.

When using this pin as analog input pin, see **Figure 11-41. Analog Input Pin Connection**.

**(b) AV<sub>REFP</sub>**

This is a pin that inputs the A/D converter reference potential (+ side).

**(c) AV<sub>REFM</sub>**

This is a pin that inputs the A/D converter reference potential (–side).

### 2.2.3 P30 to P32 (port 3)

P30 to P32 function as an I/O port. These pins also function as, external interrupt request input, real-time clock correction clock output, segment output of LCD controller/driver, and timer I/O.

Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 3 (PU3)

The following operation modes can be specified in 1-bit units.

**(1) Port mode**

P30 to P32 function as an I/O port. P30 to P33 can be set to input or output port in 1-bit units using port mode register 3 (PM3).

**(2) Control mode**

P30 to P32 function as external interrupt request input, real-time clock correction clock output, segment output of LCD controller/driver, and timer I/O.

**(a) INTP3, INTP4**

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

**(b) RTC1HZ**

This is a real-time clock correction clock (1 Hz) output pin.

**(c) TI01, TI03**

These are the pins for inputting an external count clock/capture trigger to 16-bit timers 01 and 03.

**(d) TO01, TO03**

These are the timer output pins from 16-bit timers 01 and 03.

**(e) SEG17 to SEG19**

These are the segment output pins of LCD controller/driver.

**2.2.4 P40 to P43 (port 4)**

P40 to P43 function as an I/O port. These pins also function as segment output of LCD controller/driver, external interrupt request input, data I/O for a flash memory programmer/debugger, timer I/O, and A/D converter analog input.

Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 4 (PU4).

Be sure to connect an external pull-up resistor to P40 when on-chip debugging is enabled (by using an option byte).

Input to the P41 pin can be specified as analog input or digital input in 1-bit units, using port mode control register 4 (PMC4). This register can be specified in 1-bit unit.

The following operation modes can be specified in 1-bit units.

**(1) Port mode**

P40 to P43 function as an I/O port. P40 to P43 can be set to input or output port in 1-bit units using port mode register 4 (PM4).

**(2) Control mode**

P40 to P43 function as segment output of LCD controller/driver, external interrupt request input, data I/O for a flash memory programmer/debugger, timer I/O, and A/D converter analog input.

**(a) TI04, TI05**

These are the pins for inputting an external count clock/capture trigger to 16-bit timers 04 and 05.

**(b) TO04, TO05**

These are the timer output pins from 16-bit timers 04 and 05.

**(c) TOOL0**

This is a data I/O pin for a flash memory programmer/debugger.

Be sure to pull up this pin externally when on-chip debugging is enabled (pulling it down is prohibited).

**(d) INTP7**

This is an external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

**(e) SEG22 to SEG24**

These are the segment output pins of LCD controller/driver.

**(f) ANI16**

This is an analog input pin (ANI16) of A/D converter.

When using this pin as analog input pin, see **Figure 11-41. Analog Input Pin Connection.**

**Caution** After reset release, the relationships between P40/TOOL0 and the operating mode are as follows.

**Table 2-2. Relationships Between P40/TOOL0 and Operation Mode After Reset Release**

| P40/TOOL0       | Operating mode                |
|-----------------|-------------------------------|
| V <sub>DD</sub> | Normal operation mode         |
| 0 V             | Flash memory programming mode |

For details, see 26. 5 Programming Method.

**2.2.5 P50 to P54 (port 5)**

P50 to P54 function as an I/O port. These pins also function as external interrupt request input, segment output of LCD controller/driver, and timer I/O.

Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 5 (PU5).

The following operation modes can be specified in 1-bit units.

**(1) Port mode**

P50 to P54 function as an I/O port. P50 to P54 can be set to input or output port in 1-bit units using port mode register 5 (PM5).

**(2) Control mode**

P50 to P54 function as external interrupt request input, segment output of LCD controller/driver, and timer I/O.

**(a) INTP5, INTP6**

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

**(b) TI06, TI07**

These are the pins for inputting an external count clock/capture trigger to 16-bit timers 06 and 07.

**(c) TO06, TO07**

These are the timer output pins from 16-bit timers 06 and 07.

**(d) SEG7 to SEG11**

These are the segment output pins of LCD controller/driver.

### 2.2.6 P60 and P61 (port 6)

P60 and P61 function as an I/O port. These pins also function as segment output of LCD controller/driver, serial interface data I/O, and clock I/O.

The following operation modes can be specified in 1-bit units.

#### (1) Port mode

P60 and P61 function as an I/O port. P60 to P67 can be set to input port or output port in 1-bit units using port mode register 6 (PM6).

Output of P60 and P61 is N-ch open-drain output ( $EV_{DD}$  tolerance).

#### (2) Control mode

P60 and P61 function as segment output of LCD controller/driver, serial interface data I/O, and clock I/O.

##### (a) SCLA0,

This is a serial clock I/O pin of serial interface IICA.

##### (b) SDAA0

This is a serial data I/O pins of serial interface IICA.

##### (c) SEG20, SEG21

These are the segment output pins of LCD controller/driver.

### 2.2.7 P70 to P74 (port 7)

P70 to P74 function as an I/O port. These pins also function as key interrupt input and segment output of LCD controller/driver.

Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 7 (PU7).

The following operation modes can be specified in 1-bit units.

#### (1) Port mode

P70 to P74 function as an I/O port. P70 to P74 can be set to input or output port in 1-bit units using port mode register 7 (PM7).

#### (2) Control mode

P70 to P74 function as key interrupt input and segment output of LCD controller/driver.

##### (a) KR0 to KR3

These are the key interrupt input pins.

##### (b) SEG12 to SEG16

These are the segment output pins of LCD controller/driver.



### 2.2.8 P120 to P127 (port 12)

P120 and P125 to P127 function as an I/O port. P121 to P124 functions as 4-bit input port. These pins also function as A/D converter analog input, connecting resonator for main system clock, connecting resonator for subsystem clock, external clock input for main system clock, external clock input for subsystem clock, segment output of LCD controller/driver, connecting a capacitor for LCD controller/driver, and power supply voltage pin for driving the LCD.

P120 and P125 to P127 use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

Input to the P120 pin can be specified as analog input or digital input in 1-bit units, using port mode control register 12 (PMC12). This register can be specified in 1-bit unit.

The following operation modes can be specified in 1-bit units.

#### (1) Port mode

P120 and P125 to P127 function as a 1-bit I/O port. P120 can be set to input or output port using port mode register 12 (PM12).

P121 to P124 functions as a 4-bit input port.

#### (2) Control mode

P120 to P127 function as A/D converter analog input, connecting resonator for main system clock, connecting resonator for subsystem clock, external clock input for main system clock, external clock input for subsystem clock, segment output of LCD controller/driver, connecting a capacitor for LCD controller/driver, and power supply voltage pin for driving the LCD.

##### (a) ANI17

This is an analog input pin (ANI17) of A/D converter.

When using this pin as analog input pin, see **Figure 11-41. Analog Input Pin Connection.**

##### (b) X1, X2

These are the pins for connecting a resonator for main system clock.

##### (c) EXCLK

This is an external clock input pin for main system clock.

##### (d) XT1, XT2

These are the pins for connecting a resonator for subsystem clock.

##### (e) EXCLKS

This is an external clock input pin for subsystem clock.

##### (f) SEG25

This is a segment output pin of LCD controller/driver.

##### (g) CAPH, CAPL

These are the pins for connecting a capacitor for LCD controller/driver.

##### (h) VL3

This is the pin for inputting a power supply voltage pin for driving the LCD.

- Cautions**
1. To use P125/V<sub>L3</sub> as a general-purpose port, set bit 1 (LBAS1) and bit 0 (LBAS0) of the LCD mode register (LCDM0) to 00B or 01B.
  2. To use P127/CAPH, and P126/CAPL as a general-purpose port, set bit 7 (MDSET1) and bit 6 (MDSET0) of LCD mode register (LCDM0) to “00B”, which is the same as their default status setting.

### 2.2.9 P130, P137 (port 13)

P130 functions as a 1-bit output-only port. P137 functions as a 1-bit input-only port. P137 pin also functions as external interrupt request input.

#### (1) Port mode

P130 functions as a 1-bit output-only port.

P137 functions as a 1-bit input-only port.

#### (2) Control mode

P137 functions as external interrupt request input.

##### (a) INTP0

This is an external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

### 2.2.10 P140 to P147 (port 14)

P140 to P147 function as an I/O port. These pins also function as clock/buzzer output, segment output of LCD controller/driver, A/D converter analog input, and timer I/O.

Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 14 (PU14).

When the P142 to P146 pins are used as input, specify them as either digital or analog in Port mode control register 14 (PMC14). This register can be specified in 1-bit unit.

The following operation modes can be specified in 1-bit units.

#### (1) Port mode

P140 to P147 function as an I/O port. P140 to P147 can be set to input or output port in 1-bit units using port mode register 14 (PM14).

#### (2) Control mode

P140 to P147 function as clock/buzzer output, segment output of LCD controller/driver, A/D converter analog input, and timer I/O.

##### (a) ANI20 to ANI23

These are the analog input pins (ANI20 to ANI23) of A/D converter.

When using this pin as analog input pin, see **Figure 11-41. Analog Input Pin Connection.**

##### (b) PCLBUZ0, PCLBUZ1

These are the clock/buzzer output pins.

##### (c) SEG26, SEG27, SEG33 to SEG38

These are the segment output pins of LCD controller/driver.

##### (d) TI00

This is a pin for inputting an external count clock/capture trigger to 16-bit timer 00.

**(e) T000**

This is a timer output pin from 16-bit timers 00.

**2.2.11 V<sub>DD</sub>, EV<sub>DD</sub>, V<sub>SS</sub>, EV<sub>SS</sub>****(1) V<sub>DD</sub>, EV<sub>DD</sub>****(a) 32, 44, 48, 52-pin products**

V<sub>DD</sub> is the positive power supply pin.

**(b) 64-pin products**

V<sub>DD</sub> is the positive power supply pin for P20, P21, P121 to P124, P137 and  $\overline{\text{RESET}}$  pin.

EV<sub>DD</sub> is the positive power supply pin for ports other than P20, P21, P121 to P124, P137, and pins other than ports (except for the  $\overline{\text{RESET}}$  pin) .

**(2) V<sub>SS</sub>, EV<sub>SS</sub>****(a) 32, 44, 48, 52-pin products**

V<sub>SS</sub> is the ground potential pin.

**(b) 64-pin products**

V<sub>SS</sub> is the ground potential pin for P20, P21, P121 to P124, P137 and  $\overline{\text{RESET}}$  pin.

EV<sub>SS</sub> is the ground potential pin for ports other than P20, P21, P121 to P124, P137, and pins other than ports (except for the  $\overline{\text{RESET}}$  pin) .

**Remark** Use bypass capacitors (about 0.1  $\mu$  F) as noise and latch up countermeasures with relatively thick wires at the shortest distance to V<sub>DD</sub> to V<sub>SS</sub>, and EV<sub>DD</sub> to EV<sub>SS</sub> lines.

**2.2.12 COM0 to COM7**

These are common outputs of LCD controller/driver.

**2.2.13 COMEXP**

These are common outputs for memory-type liquid crystal panel of LCD controller/driver.

**2.2.14 SEG0 to SEG3**

These are segment outputs of LCD controller/driver.

**2.2.15 VL1, VL2, VL4**

These are the pins for inputting a power supply voltage pin for driving the LCD.

**2.2.16  $\overline{\text{RESET}}$** 

This is the active-low system reset input pin.

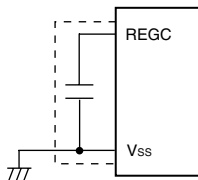
When the external reset pin is not used, connect this pin directly or via a resistor to V<sub>DD</sub>.

When the external reset pin is used, design the circuit based on V<sub>DD</sub>.

### 2.2.17 REGC

This is the pin for connecting regulator output stabilization capacitance for internal operation. Connect this pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.



**Caution** Keep the wiring length as short as possible for the broken-line part in the above figure.

### 2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-3 shows the types of pin I/O circuits and the recommended connections of unused pins.

<R> **Remark** The pins mounted depend on the product. See 1.3 Pin Configuration (Top View) and 2.1 Pin Function List.

**Table 2-3. Connection of Unused Pins (64-pin products) (1/3)**

| Pin Name                    | I/O Circuit Type | I/O | Recommended Connection of Unused Pins                                                                                                                                                                            |
|-----------------------------|------------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| P10/SCK00/SEG28             | 45-B             | I/O | <When setting to port I/O><br><br>Input:   Independently connect to EV <sub>DD</sub> or EV <sub>SS</sub> via a resistor.<br><br>Output:   Leave open.<br><br><When setting to segment output><br><br>Leave open. |
| P11/SI00/RxD0/TOOLRxD/SEG29 |                  |     |                                                                                                                                                                                                                  |
| P12/SO00/TxD0/TOOLTxD/SEG30 | 45-A             |     |                                                                                                                                                                                                                  |
| P13/ANI18/SEG31             | 45-D             |     |                                                                                                                                                                                                                  |
| P14/ANI19/SEG32             |                  |     |                                                                                                                                                                                                                  |
| P15/SCK01/INTP1/SEG4        | 45-B             |     |                                                                                                                                                                                                                  |
| P16/SI01/INTP2/SEG5         |                  |     |                                                                                                                                                                                                                  |
| P17/SO01/TI02/TO02/SEG6     | 45-A             |     |                                                                                                                                                                                                                  |
| P20/ANI0/AV <sub>REFP</sub> | 11-T             |     |                                                                                                                                                                                                                  |
| P21/ANI1/AV <sub>REFM</sub> |                  |     |                                                                                                                                                                                                                  |
| P30/TI01/TO01/SEG19         | 45-A             |     |                                                                                                                                                                                                                  |
| P31/INTP3/RTC1HZ/SEG18      |                  |     |                                                                                                                                                                                                                  |
| P32/TI03/TO03/INTP4/SEG17   |                  |     |                                                                                                                                                                                                                  |
| P40/TOOL0                   | 8-R              |     |                                                                                                                                                                                                                  |
| P41/ANI16/TI04/TO04/SEG24   | 45-D             |     |                                                                                                                                                                                                                  |
| P42/TI05/TO05/SEG23         | 45-A             |     |                                                                                                                                                                                                                  |
| P43/INTP7/SEG22             |                  |     |                                                                                                                                                                                                                  |
|                             |                  |     | Input:   Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor.<br>Output:   Leave open.                                                                                                    |
|                             |                  |     | <When setting to port I/O><br><br>Input:   Independently connect to EV <sub>DD</sub> or EV <sub>SS</sub> via a resistor.<br><br>Output:   Leave open.<br><br><When setting to segment output><br><br>Leave open. |
|                             |                  |     | Input:   Independently connect to EV <sub>DD</sub> via a resistor or leave open.<br><br>Output:   Leave open.                                                                                                    |
|                             |                  |     | <When setting to port I/O><br><br>Input:   Independently connect to EV <sub>DD</sub> or EV <sub>SS</sub> via a resistor.<br><br>Output:   Leave open.<br><br><When setting to segment output><br><br>Leave open. |

**Remark** With products not provided with an EV<sub>DD</sub> or EV<sub>SS</sub> pin, replace EV<sub>DD</sub> with V<sub>DD</sub>, or replace EV<sub>SS</sub> with V<sub>SS</sub>.

Table 2-3. Connection of Unused Pins (64-pin products) (2/3)

| Pin Name                            | I/O Circuit Type | I/O    | Recommended Connection of Unused Pins                                                                                                                                                                                                                                                              |                                                                                                                 |                                                                             |
|-------------------------------------|------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| P50/INTP5/SEG7/(PCLBUZ0)            | 45-A             | I/O    | <When setting to port I/O><br><br>Input: Independently connect to EV <sub>DD</sub> or EV <sub>SS</sub> via a resistor.<br><br>Output: Leave open.<br><br><When setting to segment output><br><br>Leave open.                                                                                       |                                                                                                                 |                                                                             |
| P51/TI06/TO06/SEG8                  |                  |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P52/INTP6/SEG9                      |                  |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P53/TI07/TO07/SEG10/<br>(INTP1)     |                  |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P54/SEG11/(TI02)/(TO02)/<br>(INTP2) |                  |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P60/SCLA0/SEG21                     | 45-C             |        | Input: Independently connect to EV <sub>DD</sub> or EV <sub>SS</sub> via a resistor.<br><br>Output: Set the port's output latch to 0 and leave the pins open,<br>or set the port's output latch to 1 and independently<br>connect the pins to EV <sub>DD</sub> or EV <sub>SS</sub> via a resistor. |                                                                                                                 |                                                                             |
| P61/SDAA0/SEG20                     |                  |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P70/KR0/SEG16                       | 45-A             |        | <When setting to port I/O><br><br>Input: Independently connect to EV <sub>DD</sub> or EV <sub>SS</sub> via a resistor.<br><br>Output: Leave open.<br><br><When setting to segment output><br><br>Leave open.                                                                                       |                                                                                                                 |                                                                             |
| P71/KR1/SEG15                       |                  |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P72/KR2/SEG14                       |                  |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P73/KR3/SEG13                       |                  |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P74/SEG12                           |                  |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P120/ANI17/SEG25                    | 45-D             |        |                                                                                                                                                                                                                                                                                                    | Input                                                                                                           | Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor. |
| P121/X1                             | 37-C             |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P122/X2/EXCLK                       |                  |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P123/XT1                            |                  |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P124/XT2/EXCLKS                     |                  |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P125/V <sub>L3</sub>                | 5-AO             | I/O    |                                                                                                                                                                                                                                                                                                    | Input: Independently connect to EV <sub>DD</sub> or EV <sub>SS</sub> via a resistor.<br><br>Output: Leave open. |                                                                             |
| P126/CAPL                           | 12-I             |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P127/CAPH                           |                  |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P130                                | 3-C              | Output | Leave open.                                                                                                                                                                                                                                                                                        |                                                                                                                 |                                                                             |
| P137/INTP0                          | 2                | Input  | Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor.                                                                                                                                                                                                                        |                                                                                                                 |                                                                             |
| P140/TO00/PCLBUZ0/<br>SEG27/(INTP6) | 45-A             | I/O    | <When setting to port I/O><br><br>Input: Independently connect to EV <sub>DD</sub> or EV <sub>SS</sub> via a resistor.<br><br>Output: Leave open.<br><br><When setting to segment output><br><br>Leave open.                                                                                       |                                                                                                                 |                                                                             |
| P141/TI00/PCLBUZ1/SEG26/<br>(INTP7) |                  |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P142/ANI20/SEG33                    | 45-D             |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P143/ANI21/SEG34                    |                  |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P144/ANI22/SEG35                    |                  |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P145/ANI23/SEG36                    |                  |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P146/SEG37                          | 45-A             |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| P147/SEG38                          |                  |        |                                                                                                                                                                                                                                                                                                    |                                                                                                                 |                                                                             |
| RESET                               | 2                |        |                                                                                                                                                                                                                                                                                                    | Input                                                                                                           | Connect directly or via a resistor to V <sub>DD</sub> .                     |
| REGC                                | —                |        |                                                                                                                                                                                                                                                                                                    | —                                                                                                               | Connect to V <sub>SS</sub> via capacitor (0.47 to 1 μF).                    |

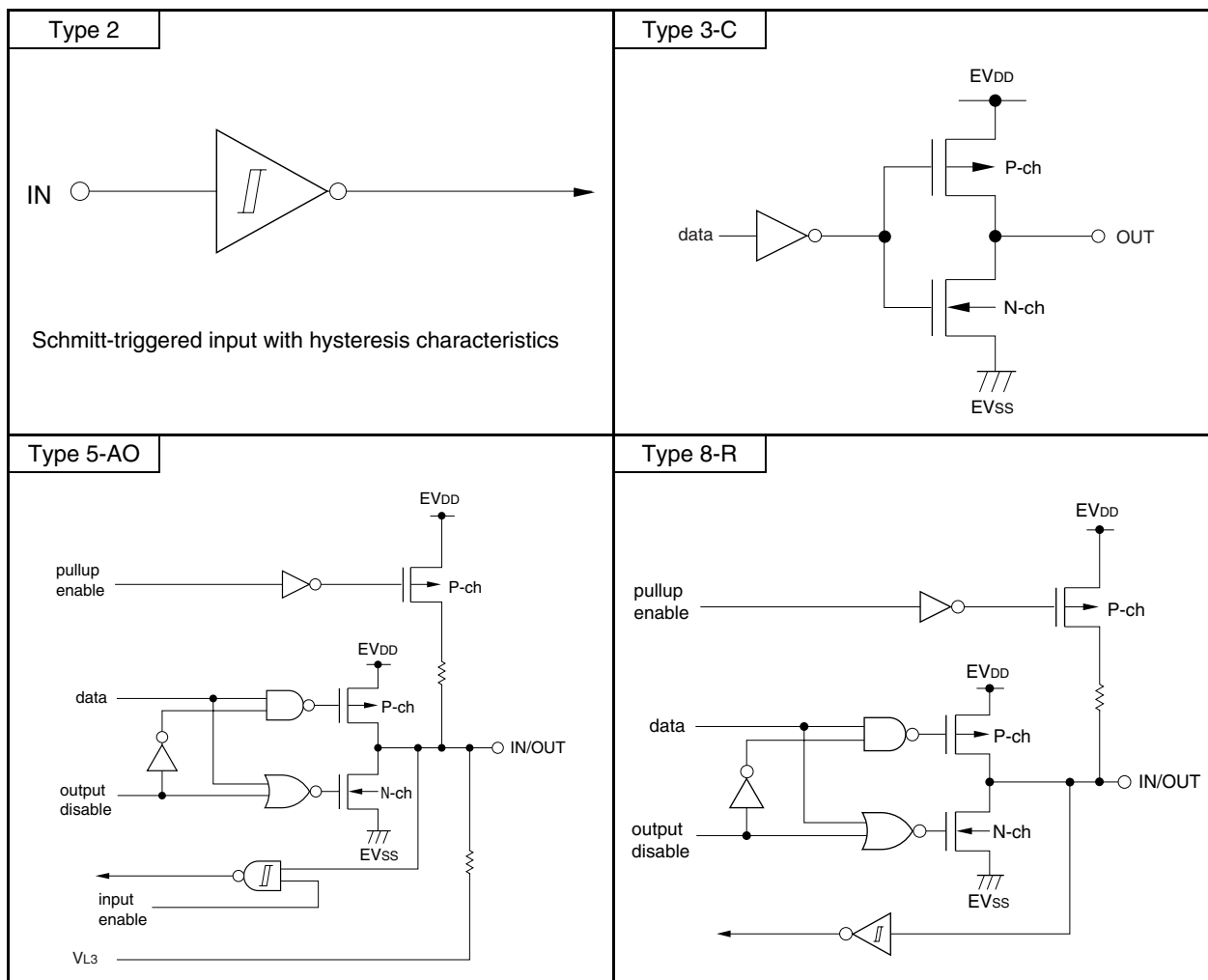
- Remarks 1.** With products not provided with an EV<sub>DD</sub> or EV<sub>SS</sub> pin, replace EV<sub>DD</sub> with V<sub>DD</sub>, or replace EV<sub>SS</sub> with V<sub>SS</sub>.
- 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

**Table 2-3. Connection of Unused Pins (64-pin products) (3/3)**

| Pin Name                                            | I/O Circuit Type | I/O    | Recommended Connection of Unused Pins |
|-----------------------------------------------------|------------------|--------|---------------------------------------|
| COM0 to COM3                                        | 45               | Output | Leave open.                           |
| COM4/COMEXP/SEG0                                    | 45               |        |                                       |
| COM5/SEG1                                           |                  |        |                                       |
| COM6/SEG2                                           |                  |        |                                       |
| COM7/SEG3                                           |                  |        |                                       |
| V <sub>L1</sub> , V <sub>L2</sub> , V <sub>L4</sub> | —                | —      |                                       |

&lt;R&gt;

Figure 2-1. Pin I/O Circuit List (1/4)

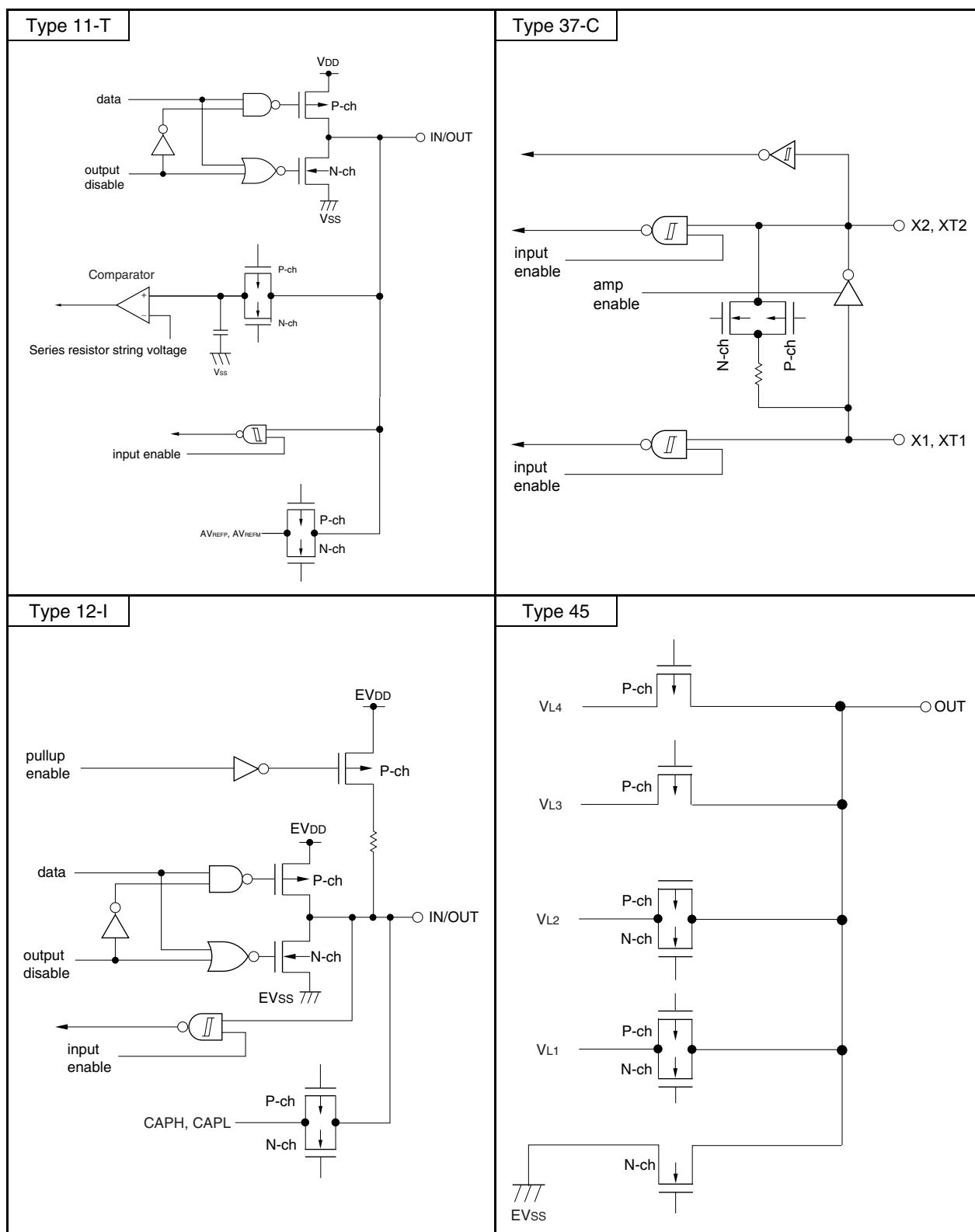


**Remark** With products not provided with an EV<sub>DD</sub> or EV<sub>SS</sub> pin, replace EV<sub>DD</sub> with V<sub>DD</sub>, or replace EV<sub>SS</sub> with V<sub>SS</sub>.



&lt;R&gt;

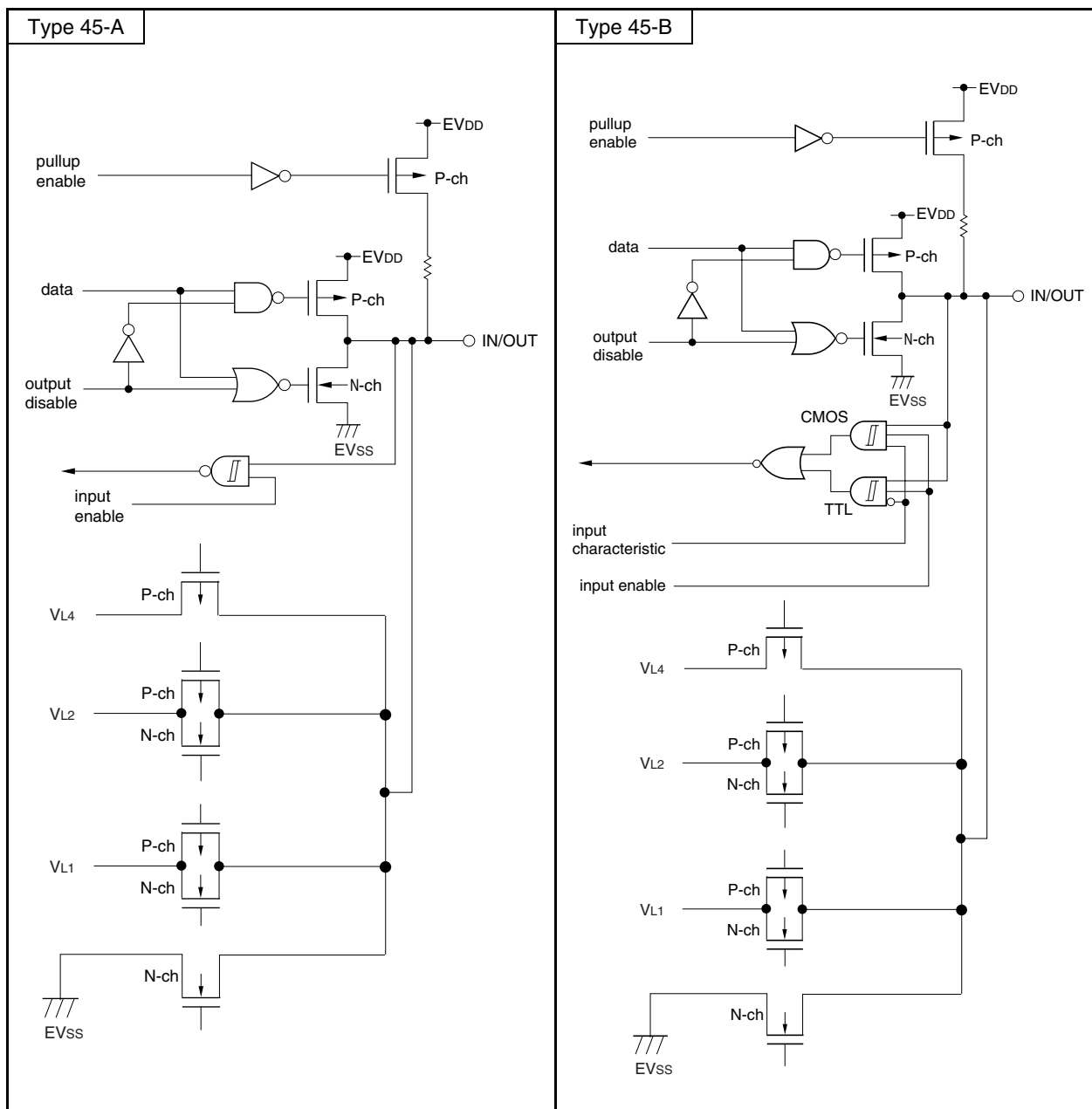
Figure 2-1. Pin I/O Circuit List (2/4)



**Remark** With products not provided with an EV<sub>DD</sub> or EV<sub>SS</sub> pin, replace EV<sub>DD</sub> with V<sub>DD</sub>, or replace EV<sub>SS</sub> with V<sub>SS</sub>.

&lt;R&gt;

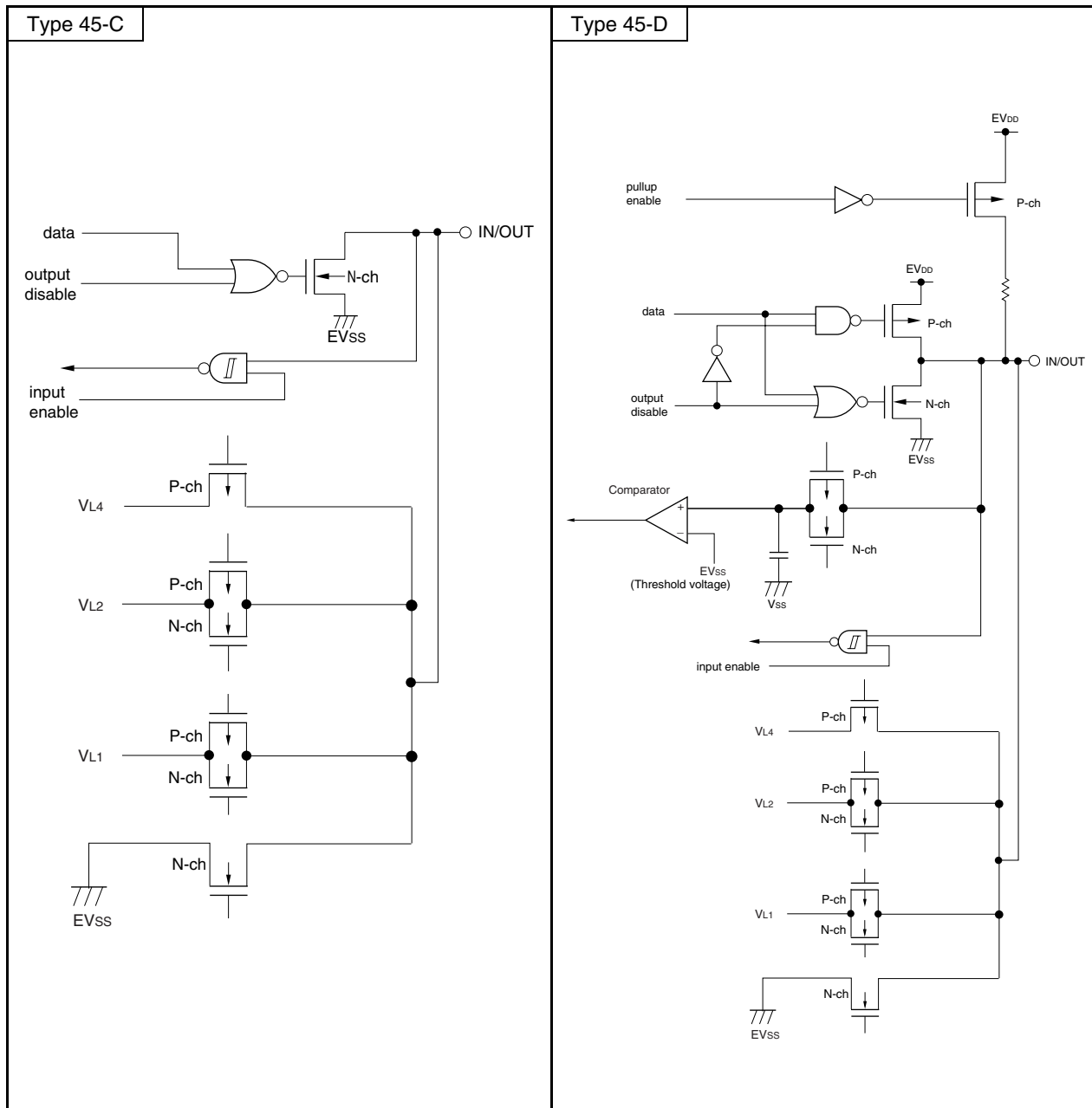
Figure 2-1. Pin I/O Circuit List (3/4)



**Remark** With products not provided with an EV<sub>DD</sub> or EV<sub>SS</sub> pin, replace EV<sub>DD</sub> with V<sub>DD</sub>, or replace EV<sub>SS</sub> with V<sub>SS</sub>.

$\langle R \rangle$

### Figure 2-1. Pin I/O Circuit List (4/4)



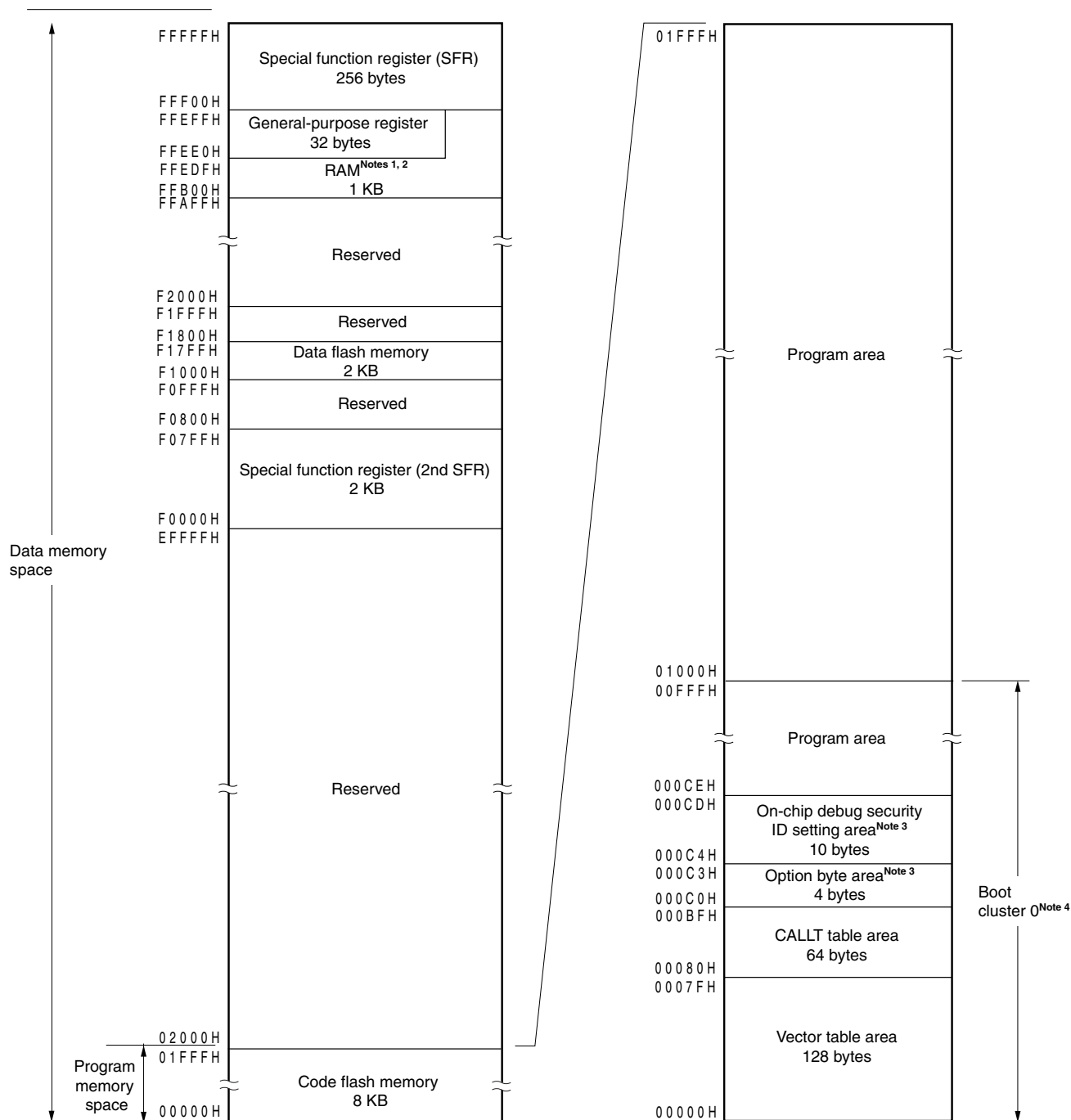
**Remark** With products not provided with an EV<sub>DD</sub> or EV<sub>SS</sub> pin, replace EV<sub>DD</sub> with V<sub>DD</sub>, or replace EV<sub>SS</sub> with V<sub>SS</sub>.

## CHAPTER 3 CPU ARCHITECTURE

### 3.1 Memory Space

<R> Products in the RL78/L12 can access a 1 MB address space. Figures 3-1 to 3-3 show the memory maps.

&lt;R&gt;

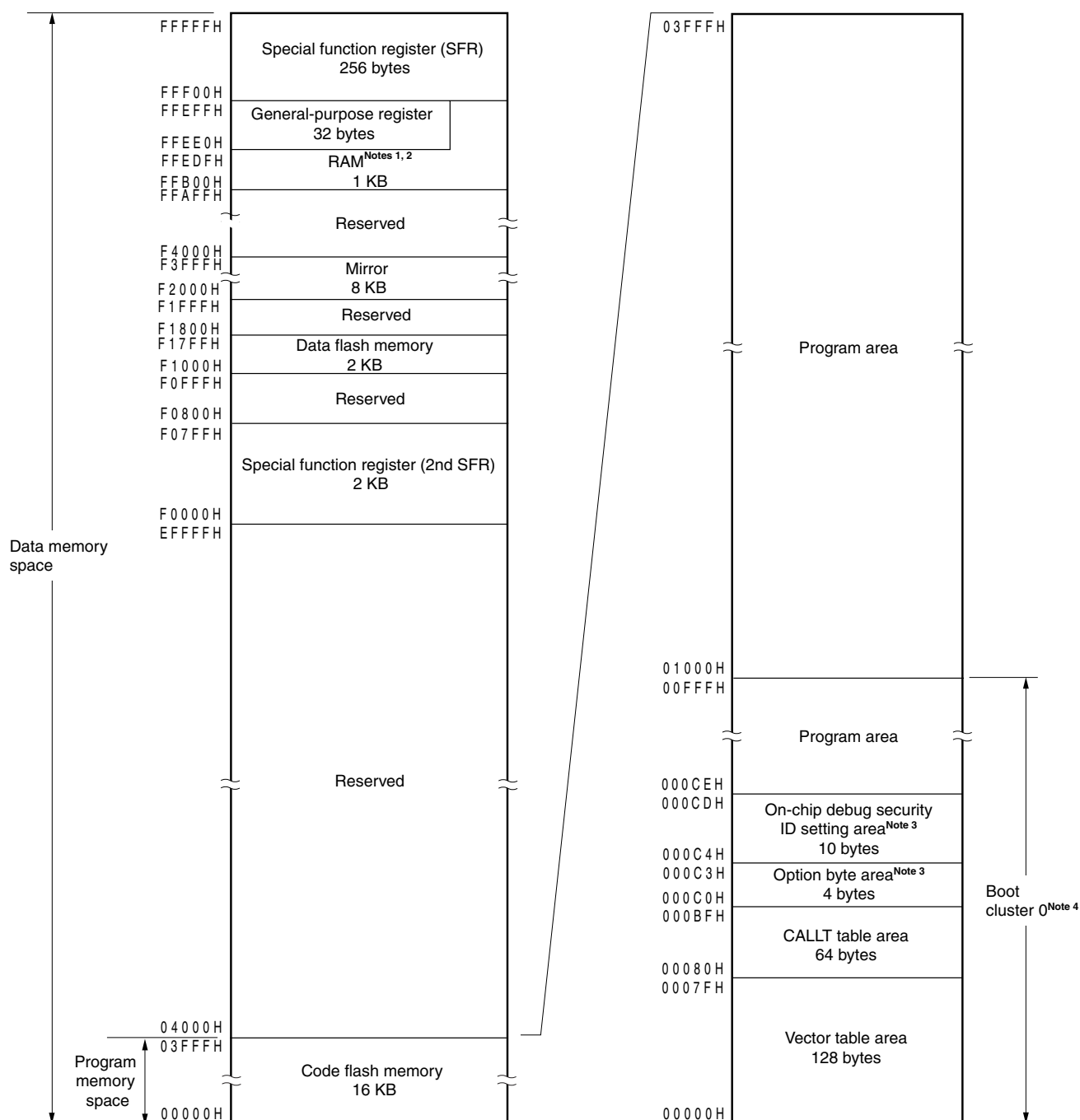
**Figure 3-1. Memory Map (R5F10Rx8 (x = B, F, G, J))**

- <R> **Notes**
1. Use of the area FFE20H to FFEDFH and FFB00H to FFC89H is prohibited when using the self-programming function and data flash function, because this area is used for self-programming library.
  2. Instructions can be executed from the RAM area excluding the general-purpose register area.
  3. Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
  4. Writing boot cluster 0 can be prohibited depending on the setting of security (see 26.6 Security Setting).

<R> **Caution** While RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize RAM areas where data access is to proceed and the RAM area + 10 bytes when instructions are fetched from RAM areas, respectively.

Reset signal generation sets RAM parity error resets to enabled (RPERDIS = 0). For details, see 23.3.3 RAM parity error detection function.

&lt;R&gt;

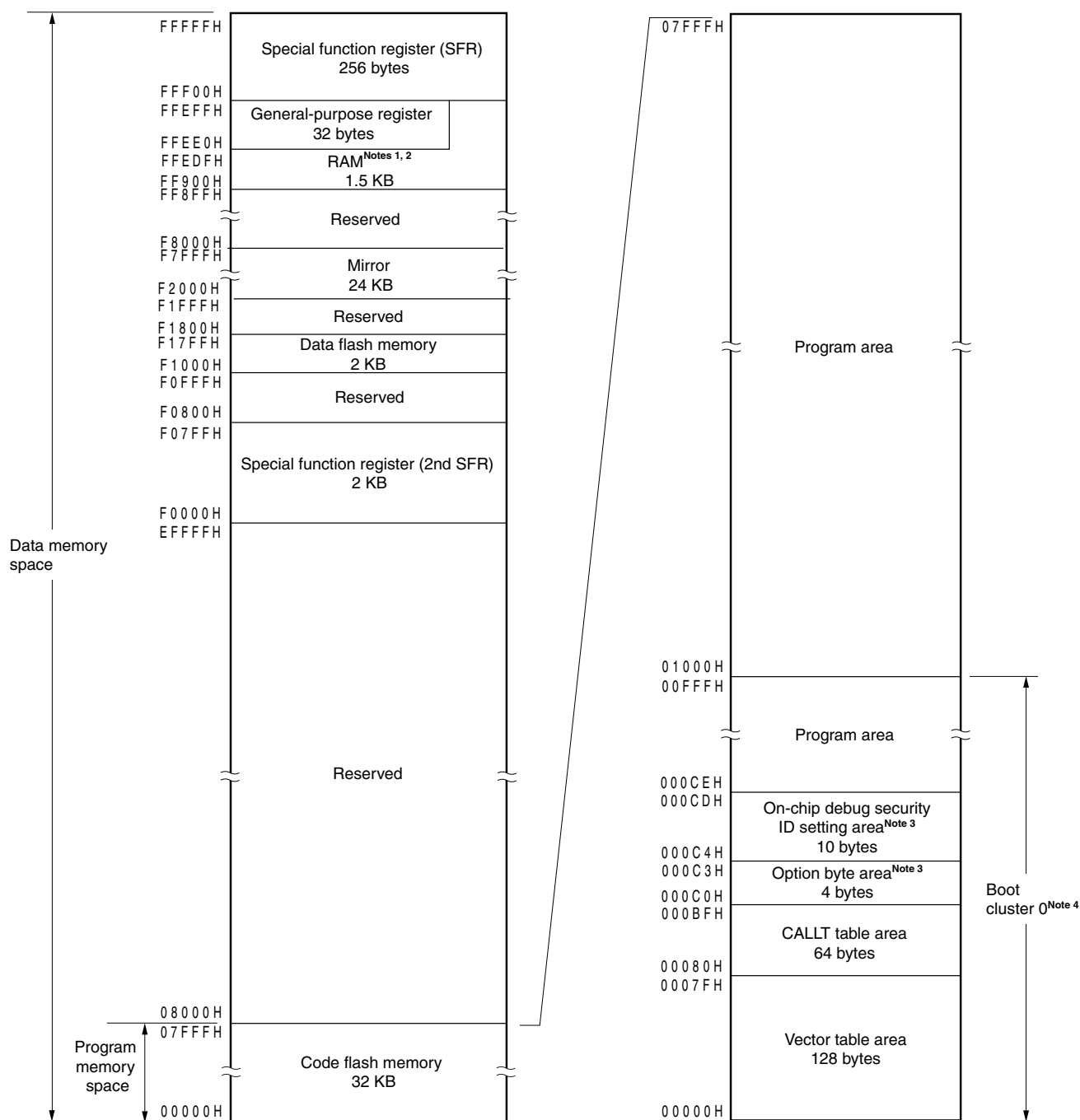
**Figure 3-2. Memory Map (R5F10RxA (x = B, F, G, J, L))**

- <R> **Notes**
1. Use of the area FFE20H to FFEDFH and FFB00H to FFC89H is prohibited when using the self-programming function and data flash function, because this area is used for self-programming library.
  2. Instructions can be executed from the RAM area excluding the general-purpose register area.
  3. Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
  4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **26.6 Security Setting**).

<R> **Caution** While RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize RAM areas where data access is to proceed and the RAM area + 10 bytes when instructions are fetched from RAM areas, respectively.

Reset signal generation sets RAM parity error resets to enabled (RPERDIS = 0). For details, see **23.3.3 RAM parity error detection function**.

&lt;R&gt;

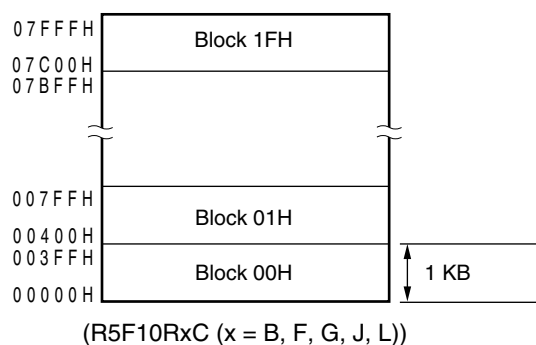
**Figure 3-3. Memory Map (R5F10RxC (x = B, F, G, J, L))**

- <R> **Notes**
1. Use of the area FFE20H to FFEDFH and FF900H to FFC89H is prohibited when using the self-programming function and data flash function, because this area is used for self-programming library.
  2. Instructions can be executed from the RAM area excluding the general-purpose register area.
  3. Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
  4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **26.6 Security Setting**).

<R> **Caution** While RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize RAM areas where data access is to proceed and the RAM area + 10 bytes when instructions are fetched from RAM areas, respectively.

Reset signal generation sets RAM parity error resets to enabled (RPERDIS = 0). For details, see **23.3.3 RAM parity error detection function**.

**Remark** The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, see **Table 3-1 Correspondence Between Address Values and Block Numbers in Flash Memory.**



Correspondence between the address values and block numbers in the flash memory are shown below.

**Table 3-1. Correspondence Between Address Values and Block Numbers in Flash Memory**

| Address Value    | Block Number | Address Value    | Block Number | Address Value    | Block Number | Address Value    | Block Number |
|------------------|--------------|------------------|--------------|------------------|--------------|------------------|--------------|
| 00000H to 003FFH | 00H          | 02000H to 023FFH | 08H          | 04000H to 043FFH | 10H          | 06000H to 063FFH | 18H          |
| 00400H to 007FFH | 01H          | 02400H to 027FFH | 09H          | 04400H to 047FFH | 11H          | 06400H to 067FFH | 19H          |
| 00800H to 00BFFH | 02H          | 02800H to 02BFFH | 0AH          | 04800H to 04BFFH | 12H          | 06800H to 06BFFH | 1AH          |
| 00C00H to 00FFFH | 03H          | 02C00H to 02FFFH | 0BH          | 04C00H to 04FFFH | 13H          | 06C00H to 06FFFH | 1BH          |
| 01000H to 013FFH | 04H          | 03000H to 033FFH | 0CH          | 05000H to 053FFH | 14H          | 07000H to 073FFH | 1CH          |
| 01400H to 017FFH | 05H          | 03400H to 037FFH | 0DH          | 05400H to 057FFH | 15H          | 07400H to 077FFH | 1DH          |
| 01800H to 01BFFH | 06H          | 03800H to 03BFFH | 0EH          | 05800H to 05BFFH | 16H          | 07800H to 07BFFH | 1EH          |
| 01C00H to 01FFFH | 07H          | 03C00H to 03FFFH | 0FH          | 05C00H to 05FFFH | 17H          | 07C00H to 07FFFH | 1FH          |

<R> **Remark** R5F10Rx8 (x = B, F, G, J): Block numbers 00H to 07H

R5F10RxA (x = B, F, G, J, L): Block numbers 00H to 0FH

R5F10RxC (x = B, F, G, J, L): Block numbers 00H to 1FH



### 3.1.1 Internal program memory space

The internal program memory space stores the program and table data.

The RL78/L12 products incorporate internal ROM (flash memory), as shown below.

**Table 3-2. Internal ROM Capacity**

| Part Number                  | Internal ROM |                                    |
|------------------------------|--------------|------------------------------------|
|                              | Structure    | Capacity                           |
| R5F10Rx8 (x = B, F, G, J)    | Flash memory | 8192 × 8 bits (00000H to 01FFFFH)  |
| R5F10RxA (x = B, F, G, J, L) |              | 16384 × 8 bits (00000H to 03FFFFH) |
| R5F10RxC (x = B, F, G, J, L) |              | 32768 × 8 bits (00000H to 07FFFFH) |

The internal program memory space is divided into the following areas.

#### (1) Vector table area

The 128-byte area 00000H to 0007FH is reserved as a vector table area. The program start addresses for branch upon reset or generation of each interrupt request are stored in the vector table area. Furthermore, the interrupt jump address is a 64 K address of 00000H to 0FFFFH, because the vector code is assumed to be 2 bytes.

Of the 16-bit address, the lower 8 bits are stored at even addresses and the higher 8 bits are stored at odd addresses.

Table 3-3. Vector Table (1/2)

| Vector Table Address | Interrupt Source                     | 64-pin | 52-pin | 48-pin | 44-pin | 32-pin |
|----------------------|--------------------------------------|--------|--------|--------|--------|--------|
| 0000H                | RESET, POR, LVD, WDT, TRAP, IAW, RPE | √      | √      | √      | √      | √      |
| 0004H                | INTWDTI                              | √      | √      | √      | √      | √      |
| 0006H                | INTLVI                               | √      | √      | √      | √      | √      |
| 0008H                | INTP0                                | √      | √      | √      | √      | √      |
| 000AH                | INTP1                                | √      | √      | √      | √      | √      |
| 000CH                | INTP2                                | √      | √      | √      | √      | √      |
| 000EH                | INTP3                                | √      | √      | √      | √      | —      |
| 0010H                | INTP4                                | √      | √      | √      | √      | —      |
| 0012H                | INTP5                                | √      | √      | √      | —      | —      |
| 0014H                | INTDMA0                              | √      | √      | √      | √      | √      |
| 0016H                | INTDMA1                              | √      | √      | √      | √      | √      |
| 0018H                | INTST0                               | √      | √      | √      | √      | √      |
|                      | INTCSI00                             | √      | √      | √      | √      | √      |
| 001AH                | INTSR0                               | √      | √      | √      | √      | √      |
|                      | INTCSI01                             | √      | √      | √      | √      | √      |
| 001CH                | INTSRE0                              | √      | √      | √      | √      | √      |
|                      | INTTM01H                             | √      | √      | √      | √      | √      |
| 0020H                | INTTM00                              | √      | √      | √      | √      | √      |
| 0024H                | INTTM03H                             | √      | √      | √      | √      | √      |
| 0026H                | INTIICA0                             | √      | √      | √      | √      | √      |
| 0028H                | INTTM01                              | √      | √      | √      | √      | √      |
| 002AH                | INTTM02                              | √      | √      | √      | √      | √      |
| 002CH                | INTTM03                              | √      | √      | √      | √      | √      |
| 002EH                | INTAD                                | √      | √      | √      | √      | √      |

**Remark**   √/: Mounted  
 —: Not mounted

Table 3-3. Vector Table (2/2)

| Vector Table Address | Interrupt Source | 64-pin | 52-pin | 48-pin | 44-pin | 32-pin |
|----------------------|------------------|--------|--------|--------|--------|--------|
| 0030H                | INTRTC           | √      | √      | √      | √      | √      |
| 0032H                | INTIT            | √      | √      | √      | √      | √      |
| 0034H                | INTKR            | √      | √      | √      | √      | √      |
| 003CH                | INTTM04          | √      | √      | √      | √      | √      |
| 003EH                | INTTM05          | √      | √      | √      | √      | √      |
| 0040H                | INTTM06          | √      | √      | √      | √      | √      |
| 0042H                | INTTM07          | √      | √      | √      | √      | √      |
| 0044H                | INTLCD0          | √      | √      | √      | √      | √      |
| 0046H                | INTP6            | √      | –      | –      | –      | –      |
| 0048H                | INTP7            | √      | –      | –      | –      | –      |
| 004AH                | INTMD            | √      | √      | √      | √      | √      |
| 004CH                | INTFL            | √      | √      | √      | √      | √      |
| 007EH                | BRK              | √      | √      | √      | √      | √      |

**Remark**    √: Mounted  
                  –: Not mounted

## (2) CALLT instruction table area

The 64-byte area 00080H to 000BFH can store the subroutine entry address of a 2-byte call instruction (CALLT). Set the subroutine entry address to a value in a range of 00000H to 0FFFFH (because an address code is of 2 bytes).

## (3) Option byte area

A 4-byte area of 000C0H to 000C3H can be used as an option byte area. For details, see **CHAPTER 25 OPTION BYTE**.

## (4) On-chip debug security ID setting area

<R> A 10-byte area of 000C4H to 000CDH can be used as an on-chip debug security ID setting area. For details, see **CHAPTER 27 ON-CHIP DEBUG FUNCTION**.

### 3.1.2 Mirror area

<R> The RL78/L12 mirrors the code flash area of 02000H to 07FFFFH, to F2000H to F7FFFFH (the code flash area to be mirrored is set by the processor mode control register (PMC)).

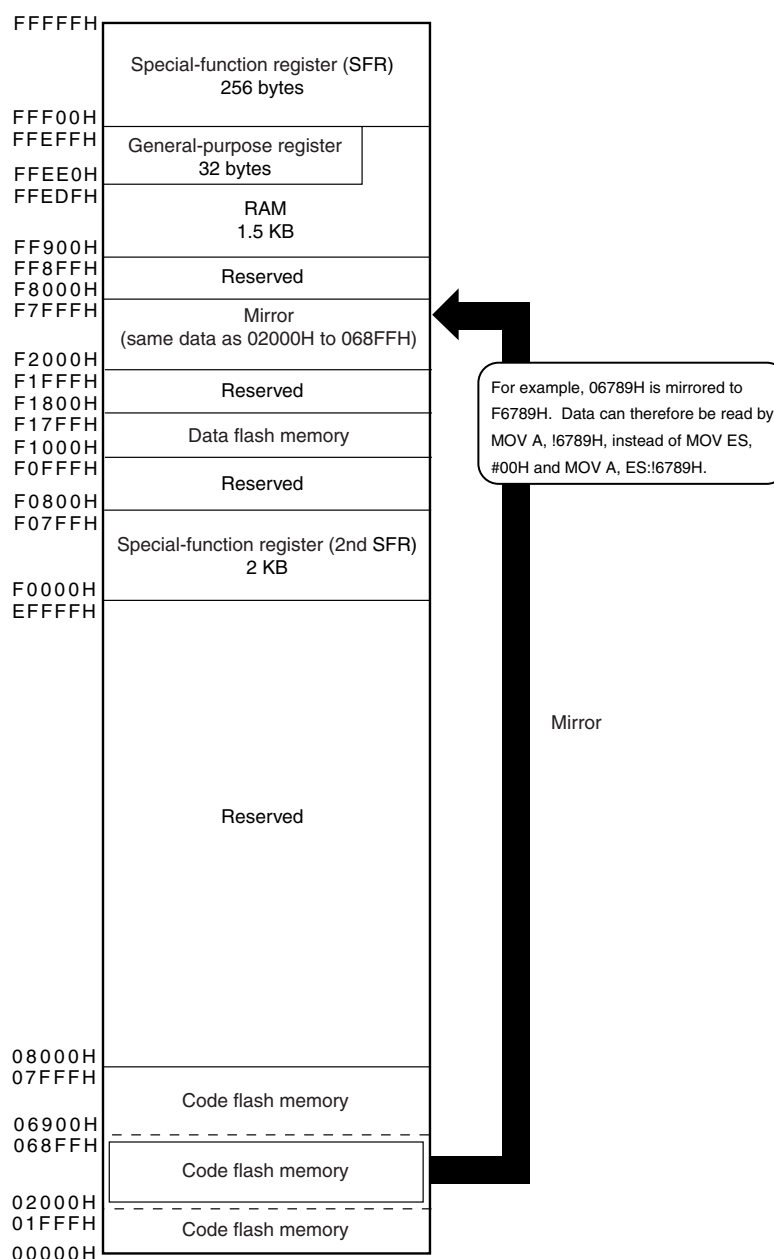
By reading data from F2000H to F7FFFFH, an instruction that does not have the ES register as an operand can be used, and thus the contents of the code flash can be read with the shorter code. However, the code flash area is not mirrored to the SFR, extended SFR, RAM, and use prohibited areas.

See **3.1 Memory Space** for the mirror area of each product.

The mirror area can only be read and no instruction can be fetched from this area.

The following show examples.

#### Example R5F10RxC (x = B, F, G, J, L) (Flash memory: 32 KB, RAM: 1.5 KB)



The PMC register is described below.

- **Processor mode control register (PMC)**

This register sets the flash memory space for mirroring to area from F0000H to FFFFFH.

The PMC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

**Figure 3-4. Format of Configuration of Processor Mode Control Register (PMC)**

Address: FFFFEH After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | <0> |
|--------|---|---|---|---|---|---|---|-----|
| PMC    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MAA |

| MAA | Selection of flash memory space for mirroring to area from F0000H to FFFFFH |
|-----|-----------------------------------------------------------------------------|
| 0   | 00000H to 0FFFFH is mirrored to F0000H to FFFFFH                            |
| 1   | Setting prohibited                                                          |

- <R> **Cautions**
1. Be sure to clear bit 0 (MAA) of this register to 0 (default value).
  2. After setting the PMC register, wait for at least one instruction and access the mirror area.

### 3.1.3 Internal data memory space

The RL78/L12 products incorporate the following RAMs.

**Table 3-4. Internal RAM Capacity**

| Part Number                  | Internal RAM                     |
|------------------------------|----------------------------------|
| R5F10Rx8 (x = B, F, G, J)    | 1024 × 8 bits (FFB00H to FFEFFH) |
| R5F10RxA (x = B, F, G, J, L) |                                  |
| R5F10RxC (x = B, F, G, J, L) | 1536 × 8 bits (FF900H to FFEFFH) |

<R> The internal RAM can be used as a data area and a program area where instructions are fetched (it is prohibited to use the general-purpose register area for fetching instructions). Four general-purpose register banks consisting of eight 8-bit registers per bank are assigned to the 32-byte area of FFEE0H to FFEFFH of the internal RAM area.

The internal RAM is used as stack memory.

<R> **Cautions** 1. It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space for fetching instructions or as a stack area.

<R> 2. The internal RAM in the following products cannot be used as stack area when using the self-programming function and data flash function.

R5F10Rx8 (x = B, F, G, J) : FFE20H to FFEDFH, FFB00H to FFC89H

R5F10RxA (x = B, F, G, J, L) : FFE20H to FFEDFH, FFB00H to FFC89H

R5F10RxC (x = B, F, G, J, L) : FFE20H to FFEDFH, FF900H to FFC89H

### 3.1.4 Special function register (SFR) area

On-chip peripheral hardware special function registers (SFRs) are allocated in the area FFF00H to FFFFFH (see **Table 3-5** in **3.2.4 Special function registers (SFRs)**).

**Caution** Do not access addresses to which SFRs are not assigned.

### 3.1.5 Extended special function register (2nd SFR: 2nd Special Function Register) area

On-chip peripheral hardware special function registers (2nd SFRs) are allocated in the area F0000H to F07FFH (see **Table 3-6** in **3.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**).

SFRs other than those in the SFR area (FFF00H to FFFFFH) are allocated to this area. An instruction that accesses the extended SFR area, however, is 1 byte longer than an instruction that accesses the SFR area.

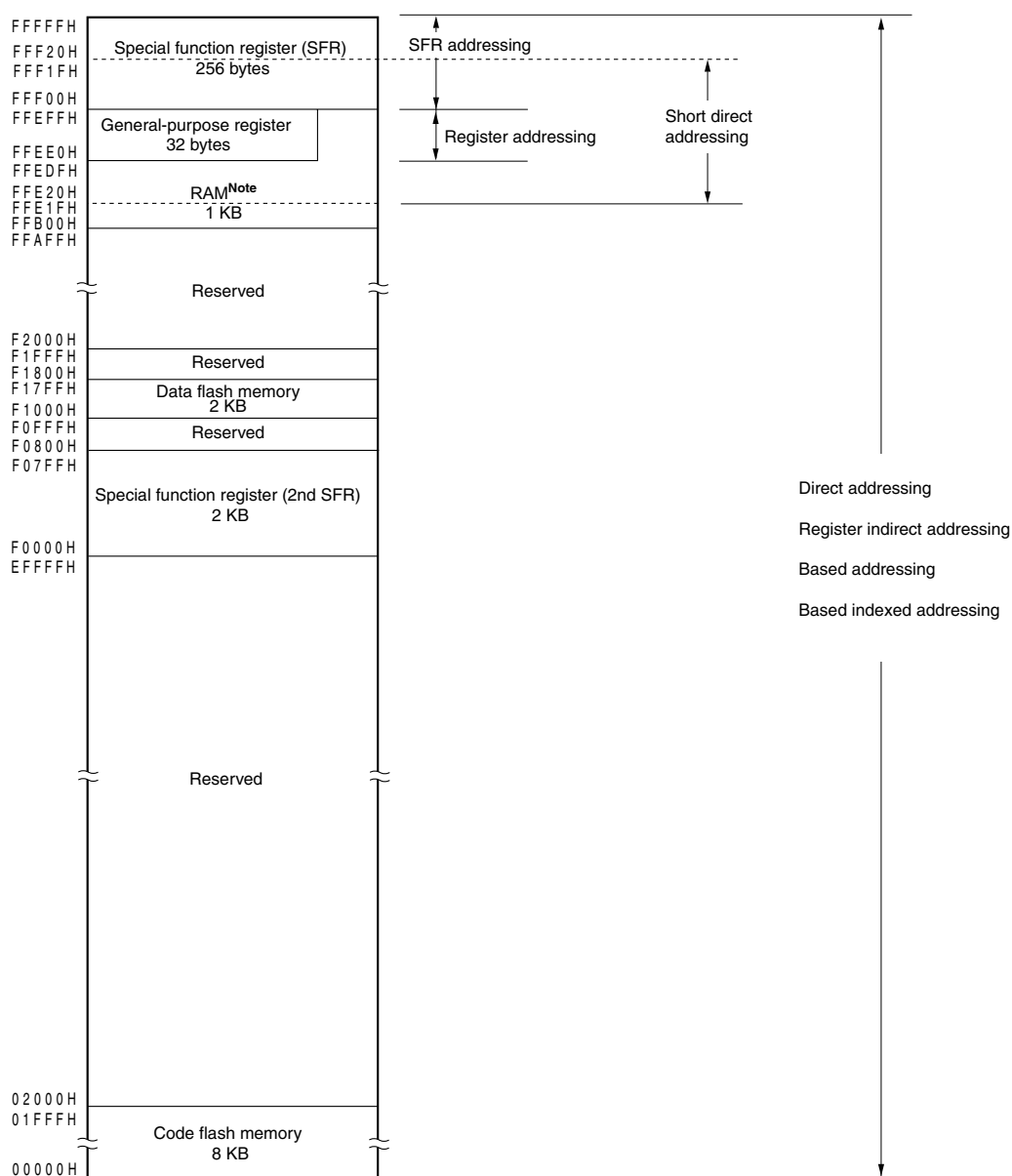
**Caution** Do not access addresses to which extended SFRs are not assigned.

### 3.1.6 Data memory addressing

Addressing refers to the method of specifying the address of the instruction to be executed next or the address of the register or memory relevant to the execution of instructions.

<R> Several addressing modes are provided for addressing the memory relevant to the execution of instructions for the RL78/L12, based on operability and other considerations. In particular, special addressing methods designed for the functions of the special function registers (SFR) and general-purpose registers are available for use. Figures 3-5 to 3-7 show correspondence between data memory and addressing. For details of each addressing, see **3.4 Addressing for Processing Data Addresses**.

Figure 3-5. Correspondence Between Data Memory and Addressing (R5F10Rx8 (x = B, F, G, J))

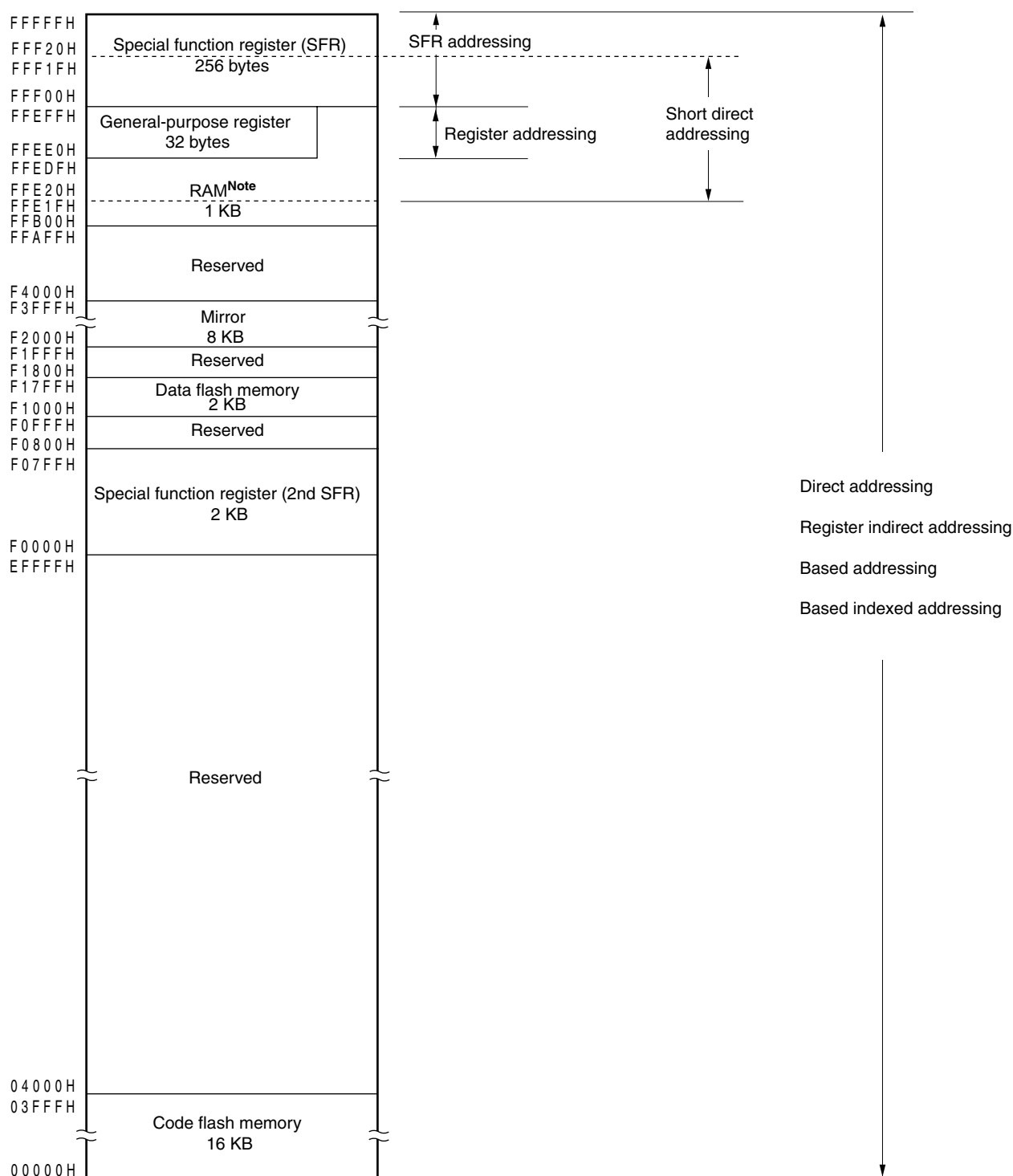


<R> **Note** Use of the area FFE20H to FFEDFH and FFB00H to FFC89H is prohibited when using the self-programming function and data flash function, because this area is used for self-programming library.

<R> **Caution** While RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize RAM areas where data access is to proceed and the RAM area + 10 bytes when instructions are fetched from RAM areas, respectively.

Reset signal generation sets RAM parity error resets to enabled (RPERDIS = 0). For details, see **23.3.3 RAM parity error detection function**.

Figure 3-6. Correspondence Between Data Memory and Addressing (R5F10RxA (x = B, F, G, J, L))



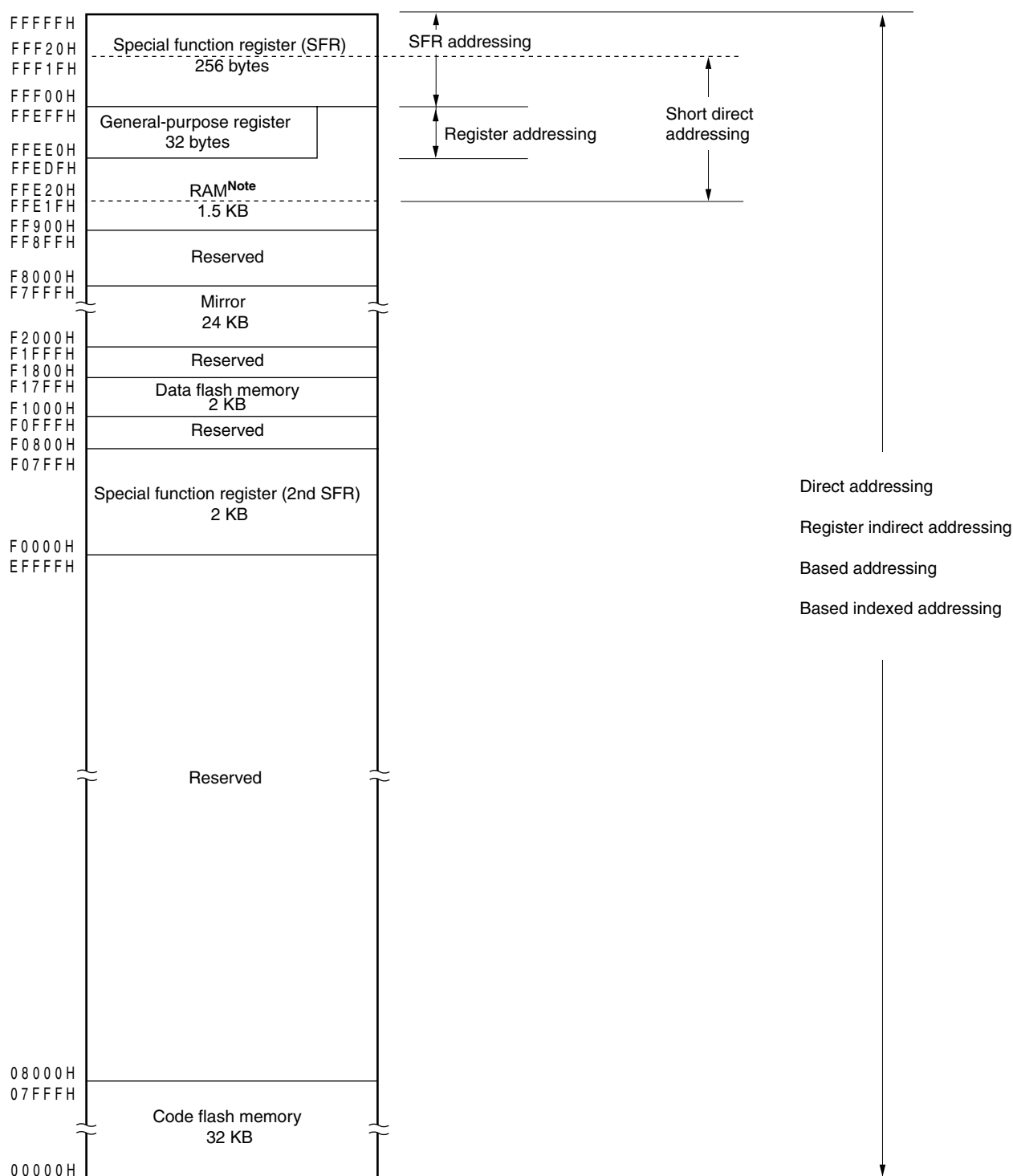
<R> **Note** Use of the area FFE20H to FFEDFH and FFB00H to FFC89H is prohibited when using the self-programming function and data flash function, because this area is used for self-programming library.

<R> **Caution** While RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize RAM areas where data access is to proceed and the RAM area + 10 bytes when instructions are fetched from RAM areas, respectively.

Reset signal generation sets RAM parity error resets to enabled (RPERDIS = 0). For details, see 23.3.3 RAM parity error detection function.



Figure 3-7. Correspondence Between Data Memory and Addressing (R5F10Rx C (x = B, F, G, J, L))



<R> **Note** Use of the area FFE20H to FFEDFH and FF900H to FFC89H is prohibited when using the self-programming function and data flash function, because this area is used for self-programming library.

<R> **Caution** While RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize RAM areas where data access is to proceed and the RAM area + 10 bytes when instructions are fetched from RAM areas, respectively.

Reset signal generation sets RAM parity error resets to enabled (RPERDIS = 0). For details, see 23.3.3 RAM parity error detection function.

## 3.2 Processor Registers

The RL78/L12 products incorporate the following processor registers.

### 3.2.1 Control registers

The control registers control the program sequence, statuses and stack memory. The control registers consist of a program counter (PC), a program status word (PSW) and a stack pointer (SP).

#### (1) Program counter (PC)

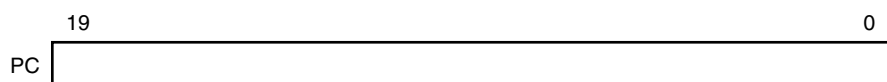
The program counter is a 20-bit register that holds the address information of the next program to be executed.

In normal operation, PC is automatically incremented according to the number of bytes of the instruction to be fetched.

<R> When a branch instruction is executed, immediate data and register contents are set.

Reset signal generation sets the reset vector table values at addresses 0000H and 0001H to the 16 lower-order bits of the program counter. The four higher-order bits of the program counter are cleared to 0000.

**Figure 3-8. Format of Program Counter**

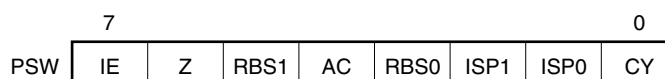


#### (2) Program status word (PSW)

The program status word is an 8-bit register consisting of various flags set/reset by instruction execution.

Program status word contents are stored in the stack area upon vectored interrupt request is acknowledged or PUSH PSW instruction execution and are restored upon execution of the RETB, RETI and POP PSW instructions. Reset signal generation sets the PSW register to 06H.

**Figure 3-9. Format of Program Status Word**



##### (a) Interrupt enable flag (IE)

<R> This flag controls the interrupt request acknowledge operations of the CPU.

When 0, the IE flag is set to the interrupt disabled (DI) state, and all maskable interrupt requests are disabled.

When 1, the IE flag is set to the interrupt enabled (EI) state and maskable interrupt request acknowledgment is controlled with an in-service priority flag (ISP1, ISP0), an interrupt mask flag for various interrupt sources, and a priority specification flag.

The IE flag is reset (0) upon DI instruction execution or interrupt acknowledgment and is set (1) upon EI instruction execution.

##### (b) Zero flag (Z)

<R> When the operation or comparison result is zero or equal, this flag is set (1). It is reset (0) in all other cases.

##### (c) Register bank select flags (RBS0, RBS1)

These are 2-bit flags to select one of the four register banks.

In these flags, the 2-bit information that indicates the register bank selected by SEL RBn instruction execution is stored.

**(d) Auxiliary carry flag (AC)**

If the operation result has a carry from bit 3 or a borrow at bit 3, this flag is set (1). It is reset (0) in all other cases.

**(e) In-service priority flags (ISP1, ISP0)**

This flag manages the priority of acknowledgeable maskable vectored interrupts. Vectored interrupt requests specified lower than the value of ISP0 and ISP1 flags by the priority specification flag registers (PRn0L, PRn0H, PRn1L, PRn1H, PRn2L) (see 17.3.3) can not be acknowledged. Actual vectored interrupt request acknowledgment is controlled by the interrupt enable flag (IE).

**Remark** n = 0, 1

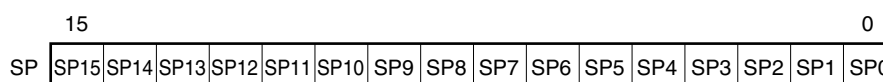
**(f) Carry flag (CY)**

This flag stores overflow and underflow upon add/subtract instruction execution. It stores the shift-out value upon rotate instruction execution and functions as a bit accumulator during bit operation instruction execution.

**(3) Stack pointer (SP)**

This is a 16-bit register to hold the start address of the memory stack area. Only the internal RAM area can be set as the stack area.

**Figure 3-10. Format of Stack Pointer**



<R> In stack addressing through a stack pointer, the SP is decremented ahead of write (save) to the stack memory and is incremented after read (restore) from the stack memory.

- Cautions**
1. Since reset signal generation makes the SP contents undefined, be sure to initialize the SP before using the stack.
  2. It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space as a stack area.
  3. The internal RAM in the following products cannot be used as stack area when using the self-programming function and data flash function.

R5F10Rx8 (x = B, F, G, J): FFB00H to FFC89H

R5F10RxA (x = B, F, G, J, L): FFB00H to FFC89H

R5F10RxC (x = B, F, G, J, L): FF900H to FFC89H

### 3.2.2 General-purpose registers

General-purpose registers are mapped at particular addresses (FFEE0H to FFEFFH) of the data memory. The general-purpose registers consists of 4 banks, each bank consisting of eight 8-bit registers (X, A, C, B, E, D, L, and H).

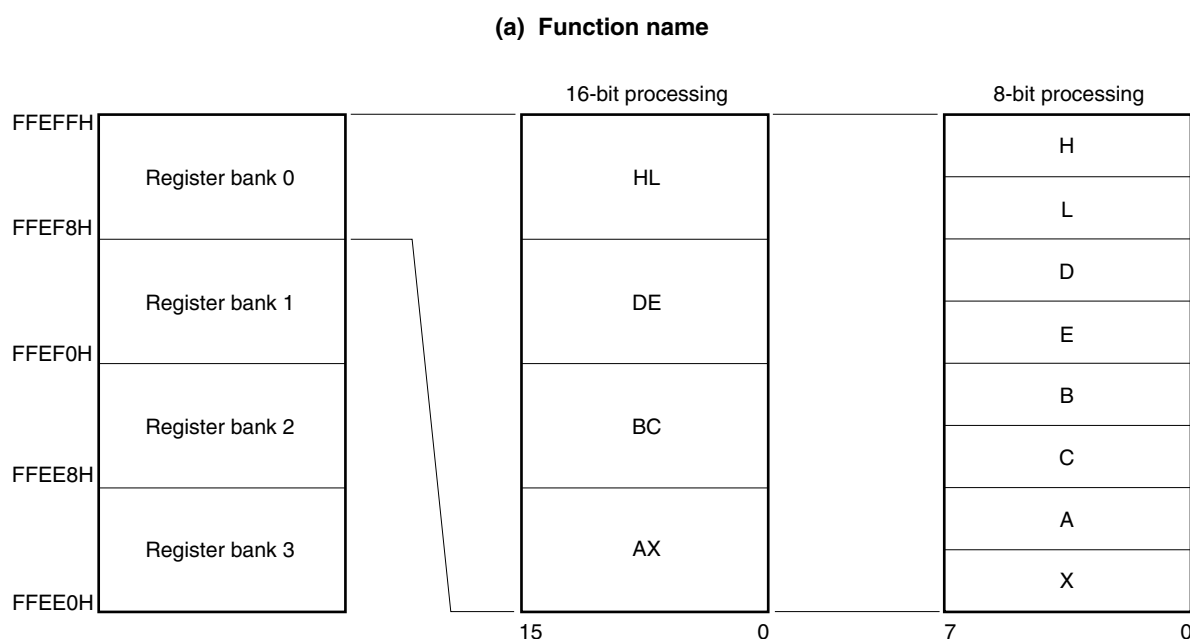
Each register can be used as an 8-bit register, and two 8-bit registers can also be used in a pair as a 16-bit register (AX, BC, DE, and HL).

Register banks to be used for instruction execution are set by the CPU control instruction (SEL RBn). Because of the 4-register bank configuration, an efficient program can be created by switching between a register for normal processing and a register for interrupt processing for each bank.

**Caution** It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space for fetching instructions or as a stack area.

<R>

**Figure 3-11. Configuration of General-Purpose Registers**



### 3.2.3 ES and CS registers

<R> The ES register and CS register are used to specify the higher address for data access and when a branch instruction is executed (register direct addressing), respectively.

The default value of the ES register after reset is 0FH, and that of the CS register is 00H.

**Figure 3-12. Configuration of ES and CS Registers**

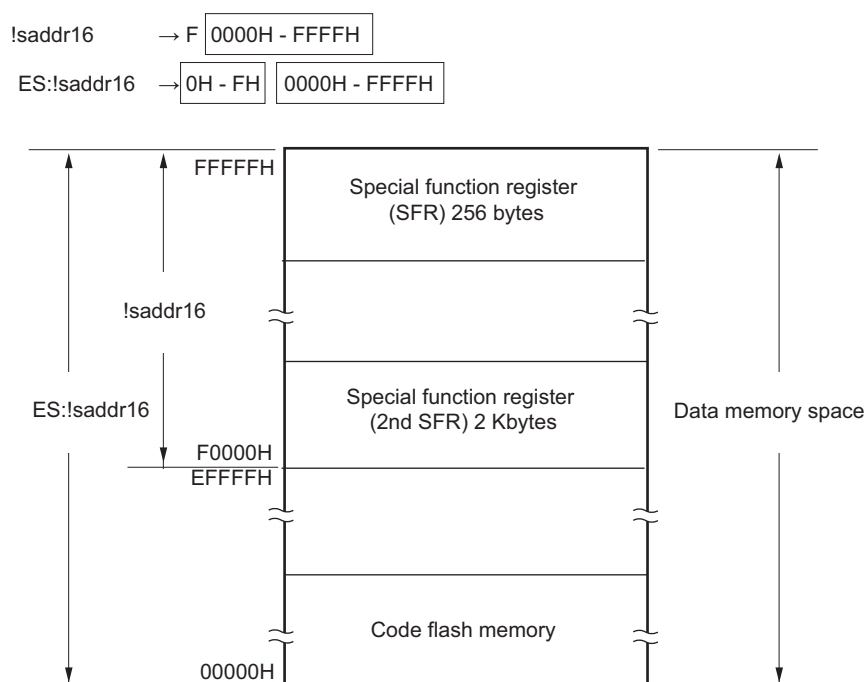
|    |   |   |   |   |     |     |     |     |
|----|---|---|---|---|-----|-----|-----|-----|
|    | 7 | 6 | 5 | 4 | 3   | 2   | 1   | 0   |
| ES | 0 | 0 | 0 | 0 | ES3 | ES2 | ES1 | ES0 |

|    |   |   |   |   |     |     |     |     |
|----|---|---|---|---|-----|-----|-----|-----|
|    | 7 | 6 | 5 | 4 | 3   | 2   | 1   | 0   |
| CS | 0 | 0 | 0 | 0 | CS3 | CP2 | CP1 | CP0 |

<R> Though the data area which can be accessed with 16-bit addresses is the 64 Kbytes from F0000H to FFFFFH, using the ES register as well extends this to the 1 Mbyte from 00000H to FFFFFH.

**Figure 3-13 Extension of Data Area Which Can Be Accessed**



### 3.2.4 Special function registers (SFRs)

Unlike a general-purpose register, each SFR has a special function.

SFRs are allocated to the FFF00H to FFFFFH area.

SFRs can be manipulated like general-purpose registers, using operation, transfer, and bit manipulation instructions. The manipulable bit units, 1, 8, and 16, depend on the SFR type.

Each manipulation bit unit can be specified as follows.

- 1-bit manipulation  
<R> Describe as follows for the 1-bit manipulation instruction operand (sfr.bit).  
When the bit name is defined: <Bit name>  
When the bit name is not defined: <Register name>.<Bit number> or <Address>.<Bit number>
- 8-bit manipulation  
<R> Describe the symbol defined by the assembler for the 8-bit manipulation instruction operand (sfr). This manipulation can also be specified with an address.
- 16-bit manipulation  
<R> Describe the symbol defined by the assembler for the 16-bit manipulation instruction operand (sfrp). When specifying an address, describe an even address.

Table 3-5 gives a list of the SFRs. The meanings of items in the table are as follows.

- Symbol  
Symbol indicating the address of a special function register. It is a reserved word in the assembler, and is defined as an sfr variable using the #pragma sfr directive in the compiler. When using the assembler, debugger, and simulator, symbols can be written as an instruction operand.
- R/W  
Indicates whether the corresponding SFR can be read or written.  
R/W: Read/write enable  
R: Read only  
W: Write only
- Manipulable bit units  
“√” indicates the manipulable bit unit (1, 8, or 16). “—” indicates a bit unit for which manipulation is not possible.
- After reset  
Indicates each register status upon reset signal generation.

**Caution** Do not access addresses to which extended SFRs are not assigned.

**Remark** For extended SFRs (2nd SFRs), see 3.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers).

Table 3-5. SFR List (1/5)

| Address | Special Function Register (SFR) Name        | Symbol         | R/W | Manipulable Bit Range |       |        | After Reset |
|---------|---------------------------------------------|----------------|-----|-----------------------|-------|--------|-------------|
|         |                                             |                |     | 1-bit                 | 8-bit | 16-bit |             |
| FFF01H  | Port register 1                             | P1             | R/W | √                     | √     | –      | 00H         |
| FFF02H  | Port register 2                             | P2             | R/W | √                     | √     | –      | 00H         |
| FFF03H  | Port register 3                             | P3             | R/W | √                     | √     | –      | 00H         |
| FFF04H  | Port register 4                             | P4             | R/W | √                     | √     | –      | 00H         |
| FFF05H  | Port register 5                             | P5             | R/W | √                     | √     | –      | 00H         |
| FFF06H  | Port register 6                             | P6             | R/W | √                     | √     | –      | 00H         |
| FFF07H  | Port register 7                             | P7             | R/W | √                     | √     | –      | 00H         |
| FFF0CH  | Port register 12                            | P12            | R/W | √                     | √     | –      | Undefined   |
| FFF0DH  | Port register 13                            | P13            | R/W | √                     | √     | –      | Undefined   |
| FFF0EH  | Port register 14                            | P14            | R/W | √                     | √     | –      | 00H         |
| FFF10H  | Serial data register 00                     | TXD0/<br>SIO00 | R/W | –                     | √     | √      | 0000H       |
| FFF11H  |                                             | –              |     | –                     | –     | –      |             |
| FFF12H  | Serial data register 01                     | RXD0/<br>SIO01 | R/W | –                     | √     | √      | 0000H       |
| FFF13H  |                                             | –              |     | –                     | –     | –      |             |
| FFF18H  | Timer data register 00                      | TDR00          | R/W | –                     | –     | √      | 0000H       |
| FFF19H  |                                             |                |     | –                     | –     | –      |             |
| FFF1AH  | Timer data register 01                      | TDR01L         | R/W | –                     | √     | √      | 00H         |
| FFF1BH  |                                             | TDR01H         |     | –                     | √     | –      | 00H         |
| FFF1EH  | 10-bit A/D conversion result register       | ADCR           | R   | –                     | –     | √      | 0000H       |
| FFF1FH  | 8-bit A/D conversion result register        | ADCRH          | R   | –                     | √     | –      | 00H         |
| FFF21H  | Port mode register 1                        | PM1            | R/W | √                     | √     | –      | FFH         |
| FFF22H  | Port mode register 2                        | PM2            | R/W | √                     | √     | –      | FFH         |
| FFF23H  | Port mode register 3                        | PM3            | R/W | √                     | √     | –      | FFH         |
| FFF24H  | Port mode register 4                        | PM4            | R/W | √                     | √     | –      | FFH         |
| FFF25H  | Port mode register 5                        | PM5            | R/W | √                     | √     | –      | FFH         |
| FFF26H  | Port mode register 6                        | PM6            | R/W | √                     | √     | –      | FFH         |
| FFF27H  | Port mode register 7                        | PM7            | R/W | √                     | √     | –      | FFH         |
| FFF2CH  | Port mode register 12                       | PM12           | R/W | √                     | √     | –      | FFH         |
| FFF2EH  | Port mode register 14                       | PM14           | R/W | √                     | √     | –      | FFH         |
| FFF30H  | A/D converter mode register 0               | ADM0           | R/W | √                     | √     | –      | 00H         |
| FFF31H  | Analog input channel specification register | ADS            | R/W | √                     | √     | –      | 00H         |
| FFF32H  | A/D converter mode register 1               | ADM1           | R/W | √                     | √     | –      | 00H         |
| FFF34H  | Key return control register                 | KRCTL          | R/W | √                     | √     | –      | 00H         |
| FFF35H  | Key return flag register                    | KRF            | R/W | –                     | √     | –      | 00H         |
| FFF37H  | Key return mode register 0                  | KRM0           | R/W | √                     | √     | –      | 00H         |

Table 3-5. SFR List (2/5)

| Address | Special Function Register (SFR) Name              | Symbol                 | R/W | Manipulable Bit Range |       |        | After Reset           |
|---------|---------------------------------------------------|------------------------|-----|-----------------------|-------|--------|-----------------------|
|         |                                                   |                        |     | 1-bit                 | 8-bit | 16-bit |                       |
| FFF38H  | External interrupt rising edge enable register 0  | EGP0                   | R/W | √                     | √     | –      | 00H                   |
| FFF39H  | External interrupt falling edge enable register 0 | EGN0                   | R/W | √                     | √     | –      | 00H                   |
| FFF40H  | LCD mode register 0                               | LCDM0                  | R/W | –                     | √     | –      | 00H                   |
| FFF41H  | LCD mode register 1                               | LCDM1                  | R/W | Note 1                | √     | –      | 00H                   |
| FFF42H  | LCD clock control register                        | LCDC0                  | R/W | –                     | √     | –      | 00H                   |
| FFF43H  | LCD boost level control register                  | VLCD                   | R/W | –                     | √     | –      | 04H                   |
| FFF4CH  | Memory-type liquid crystal control register       | MLCD                   | R/W | √                     | √     | –      | 00H                   |
| FFF50H  | IICA shift register 0                             | IICA0                  | R/W | –                     | √     | –      | 00H                   |
| FFF51H  | IICA status register 0                            | IICS0                  | R   | √                     | √     | –      | 00H                   |
| FFF52H  | IICA flag register 0                              | IICF0                  | R/W | √                     | √     | –      | 00H                   |
| FFF64H  | Timer data register 02                            | TDR02                  | R/W | –                     | –     | √      | 0000H                 |
| FFF65H  |                                                   |                        |     |                       |       |        |                       |
| FFF66H  | Timer data register 03                            | TDR03L                 | R/W | –                     | √     | √      | 00H                   |
| FFF67H  |                                                   | TDR03H                 |     | –                     | √     |        | 00H                   |
| FFF68H  | Timer data register 04                            | TDR04                  | R/W | –                     | –     | √      | 0000H                 |
| FFF69H  |                                                   |                        |     |                       |       |        |                       |
| FFF6AH  | Timer data register 05                            | TDR05                  | R/W | –                     | –     | √      | 0000H                 |
| FFF6BH  |                                                   |                        |     |                       |       |        |                       |
| FFF6CH  | Timer data register 06                            | TDR06                  | R/W | –                     | –     | √      | 0000H                 |
| FFF6DH  |                                                   |                        |     |                       |       |        |                       |
| FFF6EH  | Timer data register 07                            | TDR07                  | R/W | –                     | –     | √      | 0000H                 |
| FFF6FH  |                                                   |                        |     |                       |       |        |                       |
| FFF90H  | Interval timer control register                   | ITMC                   | R/W | –                     | –     | √      | 0FFFH                 |
| FFF91H  |                                                   |                        |     |                       |       |        |                       |
| FFF92H  | Second count register                             | SEC <sup>Note 3</sup>  | R/W | –                     | √     | –      | 00H                   |
| FFF93H  | Minute count register                             | MIN <sup>Note 3</sup>  | R/W | –                     | √     | –      | 00H                   |
| FFF94H  | Hour count register                               | HOUR <sup>Note 3</sup> | R/W | –                     | √     | –      | 12H <sup>Note 2</sup> |
| FFF95H  | Week count register                               | WEEK <sup>Note 3</sup> | R/W | –                     | √     | –      | 00H                   |
| FFF96H  | Day count register                                | DAY <sup>Note 3</sup>  | R/W | –                     | √     | –      | 01H                   |

**Notes** 1. When a memory-type liquid crystal waveform is used : –

When other than a memory-type liquid crystal waveform is used : √

- The value of this register is 00H if the AMPM bit (bit 3 of real-time clock control register 0 (RTCC0)) is set to 1 after reset.
- 44-, 48-, 52-, and 64-pin product only



Table 3-5. SFR List (3/5)

| Address | Special Function Register (SFR) Name                   | Symbol                    | R/W  | Manipulable Bit Range |       |        | After Reset                   |
|---------|--------------------------------------------------------|---------------------------|------|-----------------------|-------|--------|-------------------------------|
|         |                                                        |                           |      | 1-bit                 | 8-bit | 16-bit |                               |
| FFF97H  | Month count register                                   | MONTH <sup>Note 5</sup>   | R/W  | –                     | √     | –      | 01H                           |
| FFF98H  | Year count register                                    | YEAR <sup>Note 5</sup>    | R/W  | –                     | √     | –      | 00H                           |
| FFF99H  | Watch error correction register                        | SUBCUD <sup>Note 5</sup>  | R/W  | –                     | √     | –      | 00H                           |
| FFF9AH  | Alarm minute register                                  | ALARMWM <sup>Note 5</sup> | R/W  | –                     | √     | –      | 00H                           |
| FFF9BH  | Alarm hour register                                    | ALARMWH <sup>Note 5</sup> | R/W  | –                     | √     | –      | 12H                           |
| FFF9CH  | Alarm week register                                    | ALARMWW <sup>Note 5</sup> | R/W  | –                     | √     | –      | 00H                           |
| FFF9DH  | Real-time clock control register 0                     | RTCC0                     | R/W  | √                     | √     | –      | 00H                           |
| FFF9EH  | Real-time clock control register 1                     | RTCC1 <sup>Note 5</sup>   | R/W  | √                     | √     | –      | 00H                           |
| FFFA0H  | Clock operation mode control register                  | CMC                       | R/W  | –                     | √     | –      | 00H                           |
| FFFA1H  | Clock operation status control register                | CSC                       | R/W  | √                     | √     | –      | C0H                           |
| FFFA2H  | Oscillation stabilization time counter status register | OSTC                      | R    | √                     | √     | –      | 00H                           |
| FFFA3H  | Oscillation stabilization time select register         | OSTS                      | R/W  | –                     | √     | –      | 07H                           |
| FFFA4H  | System clock control register                          | CKC                       | R/W  | √                     | √     | –      | 00H                           |
| FFFA5H  | Clock output select register 0                         | CKS0                      | R/W  | √                     | √     | –      | 00H                           |
| FFFA6H  | Clock output select register 1                         | CKS1 <sup>Note 5</sup>    | R/W  | √                     | √     | –      | 00H                           |
| FFFA8H  | Reset control flag register                            | RESF                      | R    | –                     | √     | –      | Undefined <sup>Note 1</sup>   |
| FFFA9H  | Voltage detection register                             | LVIM                      | R/W  | √                     | √     | –      | 00H <sup>Note 2</sup>         |
| FFFAAH  | Voltage detection level register                       | LVIS                      | R/W  | √                     | √     | –      | 00H/01H/81H <sup>Note 3</sup> |
| FFFABH  | Watchdog timer enable register                         | WDTE                      | R/W  | –                     | √     | –      | 1AH/9AH <sup>Note 4</sup>     |
| FFFACH  | CRC input register                                     | CRCIN                     | R/W  | –                     | √     | –      | 00H                           |
| FFFB0H  | DMA SFR address register 0                             | DSA0                      | R/W  | –                     | √     | –      | 00H                           |
| FFFB1H  | DMA SFR address register 1                             | DSA1                      | R/W  | –                     | √     | –      | 00H                           |
| FFFB2H  | DMA RAM address register 0L                            | DRA0L                     | DRA0 | R/W                   | –     | √      | 00H                           |
| FFFB3H  | DMA RAM address register 0H                            | DRA0H                     |      | R/W                   | –     | √      | 00H                           |
| FFFB4H  | DMA RAM address register 1L                            | DRA1L                     | DRA1 | R/W                   | –     | √      | 00H                           |
| FFFB5H  | DMA RAM address register 1H                            | DRA1H                     |      | R/W                   | –     | √      | 00H                           |
| FFFB6H  | DMA byte count register 0L                             | DBC0L                     | DBC0 | R/W                   | –     | √      | 00H                           |
| FFFB7H  | DMA byte count register 0H                             | DBC0H                     |      | R/W                   | –     | √      | 00H                           |
| FFFB8H  | DMA byte count register 1L                             | DBC1L                     | DBC1 | R/W                   | –     | √      | 00H                           |
| FFFB9H  | DMA byte count register 1H                             | DBC1H                     |      | R/W                   | –     | √      | 00H                           |
| FFFBABH | DMA mode control register 0                            | DMC0                      | R/W  | √                     | √     | –      | 00H                           |
| FFFBABH | DMA mode control register 1                            | DMC1                      | R/W  | √                     | √     | –      | 00H                           |
| FFFBCH  | DMA operation control register 0                       | DRC0                      | R/W  | √                     | √     | –      | 00H                           |
| FFFBCH  | DMA operation control register 1                       | DRC1                      | R/W  | √                     | √     | –      | 00H                           |

- Notes**
1. The reset value of the RESF register varies depending on the reset source.
  2. The reset value of the LVIM register varies depending on the reset source.
  3. The reset value of the LVIS register varies depending on the reset source and the setting of the option byte.
  4. The reset value of the WDTE register is determined by the setting of the option byte.

&lt;R&gt;

5. 44-, 48-, 52-, and 64-pin product only

Table 3-5. SFR List (4/5)

| Address | Special Function Register (SFR) Name     | Symbol |      | R/W | Manipulable Bit Range |       |        | After Reset |
|---------|------------------------------------------|--------|------|-----|-----------------------|-------|--------|-------------|
|         |                                          |        |      |     | 1-bit                 | 8-bit | 16-bit |             |
| FFFD0H  | Interrupt request flag register 2L       | IF2L   | IF2  | R/W | √                     | √     | √      | 00H         |
| FFFD4H  | Interrupt mask flag register 2L          | MK2L   | MK2  | R/W | √                     | √     | √      | FFH         |
| FFFD8H  | Priority specification flag register 02L | PR02L  | PR02 | R/W | √                     | √     | √      | FFH         |
| FFFDCH  | Priority specification flag register 12L | PR12L  | PR12 | R/W | √                     | √     | √      | FFH         |
| FFFE0H  | Interrupt request flag register 0L       | IF0L   | IF0  | R/W | √                     | √     | √      | 00H         |
| FFFE1H  | Interrupt request flag register 0H       | IF0H   |      | R/W | √                     | √     |        | 00H         |
| FFFE2H  | Interrupt request flag register 1L       | IF1L   | IF1  | R/W | √                     | √     | √      | 00H         |
| FFFE3H  | Interrupt request flag register 1H       | IF1H   |      | R/W | √                     | √     |        | 00H         |
| FFFE4H  | Interrupt mask flag register 0L          | MK0L   | MK0  | R/W | √                     | √     | √      | FFH         |
| FFFE5H  | Interrupt mask flag register 0H          | MK0H   |      | R/W | √                     | √     |        | FFH         |
| FFFE6H  | Interrupt mask flag register 1L          | MK1L   | MK1  | R/W | √                     | √     | √      | FFH         |
| FFFE7H  | Interrupt mask flag register 1H          | MK1H   |      | R/W | √                     | √     |        | FFH         |
| FFFE8H  | Priority specification flag register 00L | PR00L  | PR00 | R/W | √                     | √     | √      | FFH         |
| FFFE9H  | Priority specification flag register 00H | PR00H  |      | R/W | √                     | √     |        | FFH         |
| FFFEAH  | Priority specification flag register 01L | PR01L  | PR01 | R/W | √                     | √     | √      | FFH         |
| FFFEBH  | Priority specification flag register 01H | PR01H  |      | R/W | √                     | √     |        | FFH         |
| FFFECH  | Priority specification flag register 10L | PR10L  | PR10 | R/W | √                     | √     | √      | FFH         |
| FFFEDH  | Priority specification flag register 10H | PR10H  |      | R/W | √                     | √     |        | FFH         |
| FFFEEH  | Priority specification flag register 11L | PR11L  | PR11 | R/W | √                     | √     | √      | FFH         |
| FFFEFH  | Priority specification flag register 11H | PR11H  |      | R/W | √                     | √     |        | FFH         |

**Table 3-5. SFR List (5/5)**

| Address | Special Function Register (SFR) Name        | Symbol | R/W | Manipulable Bit Range |       |        | After Reset |
|---------|---------------------------------------------|--------|-----|-----------------------|-------|--------|-------------|
|         |                                             |        |     | 1-bit                 | 8-bit | 16-bit |             |
| FFFF0H  | Multiplication/division data register A (L) | MDAL   | R/W | –                     | –     | √      | 0000H       |
| FFFF1H  |                                             |        |     |                       |       |        |             |
| FFFF2H  | Multiplication/division data register A (H) | MDAH   | R/W | –                     | –     | √      | 0000H       |
| FFFF3H  |                                             |        |     |                       |       |        |             |
| FFFF4H  | Multiplication/division data register B (H) | MDBH   | R/W | –                     | –     | √      | 0000H       |
| FFFF5H  |                                             |        |     |                       |       |        |             |
| FFFF6H  | Multiplication/division data register B (L) | MDBL   | R/W | –                     | –     | √      | 0000H       |
| FFFF7H  |                                             |        |     |                       |       |        |             |
| FFFFEH  | Processor mode control register             | PMC    | R/W | √                     | √     | –      | 00H         |

**Remark** For extended SFRs (2nd SFRs), see **Table 3-6 Extended SFR (2nd SFR) List**.

### 3.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)

Unlike a general-purpose register, each extended SFR (2<sup>nd</sup> SFR) has a special function.

Extended SFRs are allocated to the F0000H to F07FFH area. SFRs other than those in the SFR area (FFF00H to FFFFFH) are allocated to this area. An instruction that accesses the extended SFR area, however, is 1 byte longer than an instruction that accesses the SFR area.

Extended SFRs can be manipulated like general-purpose registers, using operation, transfer, and bit manipulation instructions. The manipulable bit units, 1, 8, and 16, depend on the SFR type.

Each manipulation bit unit can be specified as follows.

- 1-bit manipulation  
<R> Describe as follows for the 1-bit manipulation instruction operand (!addr16.bit)  
When the bit name is defined: <Bit name>  
When the bit name is not defined: <Register name>.<Bit number> or <Address>.<Bit number>
- 8-bit manipulation  
Describe the symbol defined by the assembler for the 8-bit manipulation instruction operand (!addr16). This manipulation can also be specified with an address.
- 16-bit manipulation  
Describe the symbol defined by the assembler for the 16-bit manipulation instruction operand (!addr16). When specifying an address, describe an even address.

Table 3-6 gives a list of the extended SFRs. The meanings of items in the table are as follows.

- Symbol  
Symbol indicating the address of an extended SFR. It is a reserved word in the assembler, and is defined as an sfr variable using the #pragma sfr directive in the compiler. When using the assembler, debugger, and simulator, symbols can be written as an instruction operand.
- R/W  
Indicates whether the corresponding extended SFR can be read or written.  
R/W: Read/write enable  
R: Read only  
W: Write only
- Manipulable bit units  
“√” indicates the manipulable bit unit (1, 8, or 16). “–” indicates a bit unit for which manipulation is not possible.
- After reset  
Indicates each register status upon reset signal generation.

**Caution** Do not access addresses to which extended SFRs (2nd SFRs) are not assigned.

**Remark** For SFRs in the SFR area, see 3.2.4 Special function registers (SFRs).

Table 3-6. Extended SFR (2nd SFR) List (1/6)

| Address | Special Function Register (SFR) Name                      | Symbol  | R/W | Manipulable Bit Range |       |        | After Reset                 |
|---------|-----------------------------------------------------------|---------|-----|-----------------------|-------|--------|-----------------------------|
|         |                                                           |         |     | 1-bit                 | 8-bit | 16-bit |                             |
| F0010H  | A/D converter mode register 2                             | ADM2    | R/W | √                     | √     | –      | 00H                         |
| F0011H  | Conversion result comparison upper limit setting register | ADUL    | R/W | –                     | √     | –      | FFH                         |
| F0012H  | Conversion result comparison lower limit setting register | ADLL    | R/W | –                     | √     | –      | 00H                         |
| F0013H  | A/D test register                                         | ADTES   | R/W | –                     | √     | –      | 00H                         |
| F0031H  | Pull-up resistor option register 1                        | PU1     | R/W | √                     | √     | –      | 00H                         |
| F0033H  | Pull-up resistor option register 3                        | PU3     | R/W | √                     | √     | –      | 00H                         |
| F0034H  | Pull-up resistor option register 4                        | PU4     | R/W | √                     | √     | –      | 01H                         |
| F0035H  | Pull-up resistor option register 5                        | PU5     | R/W | √                     | √     | –      | 00H                         |
| F0037H  | Pull-up resistor option register 7                        | PU7     | R/W | √                     | √     | –      | 00H                         |
| F003CH  | Pull-up resistor option register 12                       | PU12    | R/W | √                     | √     | –      | 00H                         |
| F003EH  | Pull-up resistor option register 14                       | PU14    | R/W | √                     | √     | –      | 00H                         |
| F0041H  | Port input mode register 1                                | PIM1    | R/W | √                     | √     | –      | 00H                         |
| F0051H  | Port output mode register 1                               | POM1    | R/W | √                     | √     | –      | 00H                         |
| F0061H  | Port mode control register 1                              | PMC1    | R/W | √                     | √     | –      | FFH                         |
| F0064H  | Port mode control register 4                              | PMC4    | R/W | √                     | √     | –      | FFH                         |
| F006CH  | Port mode control register 12                             | PMC12   | R/W | √                     | √     | –      | FFH                         |
| F006EH  | Port mode control register 14                             | PMC14   | R/W | √                     | √     | –      | FFH                         |
| F0070H  | Noise filter enable register 0                            | NFEN0   | R/W | √                     | √     | –      | 00H                         |
| F0071H  | Noise filter enable register 1                            | NFEN1   | R/W | √                     | √     | –      | 00H                         |
| F0073H  | Input switch control register                             | ISC     | R/W | √                     | √     | –      | 00H                         |
| F0074H  | Timer input select register 0                             | TIS0    | R/W | –                     | √     | –      | 00H                         |
| F0076H  | A/D port configuration register                           | ADPC    | R/W | –                     | √     | –      | 00H                         |
| F0077H  | Peripheral I/O redirection register                       | PIOR    | R/W | –                     | √     | –      | 00H                         |
| F0078H  | Invalid memory access detection control register          | IAWCTL  | R/W | –                     | √     | –      | 00H                         |
| F0079H  | Timer output select register <sup>Note 2</sup>            | TOS     | R/W | √                     | √     | –      | 00H                         |
| F0090H  | Data flash control register                               | DFLCTL  | R/W | √                     | √     | –      | 00H                         |
| F00A0H  | High-speed on-chip oscillator trimming register           | HIOTRM  | R/W | –                     | √     | –      | Undefined <sup>Note 1</sup> |
| F00A8H  | High-speed on-chip oscillator frequency select register   | HOCODIV | R/W | –                     | √     | –      | Undefined                   |

**Notes** 1. The value after a reset is adjusted at the time of shipment.

2. 44-, 48-, 52-, and 64-pin product only

Table 3-6. Extended SFR (2nd SFR) List (2/6)

| Address | Special Function Register (SFR) Name               | Symbol | R/W   | Manipulable Bit Range |       |        | After Reset |
|---------|----------------------------------------------------|--------|-------|-----------------------|-------|--------|-------------|
|         |                                                    |        |       | 1-bit                 | 8-bit | 16-bit |             |
| F00E0H  | Multiplication/division data register C (L)        | MDCL   | R/W   | –                     | –     | √      | 0000H       |
| F00E2H  | Multiplication/division data register C (H)        | MDCH   | R/W   | –                     | –     | √      | 0000H       |
| F00E8H  | Multiplication/division control register           | MDUC   | R/W   | √                     | √     | –      | 00H         |
| F00F0H  | Peripheral enable register 0                       | PER0   | R/W   | √                     | √     | –      | 00H         |
| F00F3H  | Operation speed mode control register              | OSMC   | R/W   | –                     | √     | –      | 00H         |
| F00F5H  | RAM parity error control register                  | RPECTL | R/W   | √                     | √     | –      | 00H         |
| F00FEH  | BCD adjust result register                         | BCDADJ | R     | –                     | √     | –      | Undefined   |
| F0100H  | Serial status register 00                          | SSR00L | SSR00 | R                     | –     | √      | 0000H       |
| F0101H  |                                                    | –      |       |                       | –     | –      |             |
| F0102H  | Serial status register 01                          | SSR01L | SSR01 | R                     | –     | √      | 0000H       |
| F0103H  |                                                    | –      |       |                       | –     | –      |             |
| F0108H  | Serial flag clear trigger register 00              | SIR00L | SIR00 | R/W                   | –     | √      | 0000H       |
| F0109H  |                                                    | –      |       |                       | –     | –      |             |
| F010AH  | Serial flag clear trigger register 01              | SIR01L | SIR01 | R/W                   | –     | √      | 0000H       |
| F010BH  |                                                    | –      |       |                       | –     | –      |             |
| F0110H  | Serial mode register 00                            | SMR00  | R/W   | –                     | –     | √      | 0020H       |
| F0111H  |                                                    |        |       | –                     | –     | –      |             |
| F0112H  | Serial mode register 01                            | SMR01  | R/W   | –                     | –     | √      | 0020H       |
| F0113H  |                                                    |        |       | –                     | –     | –      |             |
| F0118H  | Serial communication operation setting register 00 | SCR00  | R/W   | –                     | –     | √      | 0087H       |
| F0119H  |                                                    |        |       | –                     | –     | –      |             |
| F011AH  | Serial communication operation setting register 01 | SCR01  | R/W   | –                     | –     | √      | 0087H       |
| F011BH  |                                                    |        |       | –                     | –     | –      |             |
| F0120H  | Serial channel enable status register 0            | SE0L   | SE0   | R                     | √     | √      | 0000H       |
| F0121H  |                                                    | –      |       |                       | –     | –      |             |
| F0122H  | Serial channel start register 0                    | SS0L   | SS0   | R/W                   | √     | √      | 0000H       |
| F0123H  |                                                    | –      |       |                       | –     | –      |             |
| F0124H  | Serial channel stop register 0                     | ST0L   | ST0   | R/W                   | √     | √      | 0000H       |
| F0125H  |                                                    | –      |       |                       | –     | –      |             |
| F0126H  | Serial clock select register 0                     | SPS0L  | SPS0  | R/W                   | –     | √      | 0000H       |
| F0127H  |                                                    | –      |       |                       | –     | –      |             |
| F0128H  | Serial output register 0                           | SO0    | R/W   | –                     | –     | √      | 0303H       |
| F0129H  |                                                    |        |       | –                     | –     | –      |             |
| F012AH  | Serial output enable register 0                    | SOE0L  | SOE0  | R/W                   | √     | √      | 0000H       |
| F012BH  |                                                    | –      |       |                       | –     | –      |             |
| F0134H  | Serial output level register 0                     | SOL0L  | SOL0  | R/W                   | –     | √      | 0000H       |
| F0135H  |                                                    | –      |       |                       | –     | –      |             |
| F0138H  | Serial standby control register 0                  | SSC0L  | SSC0  | R/W                   | –     | √      | 0000H       |
| F0139H  |                                                    | –      |       |                       | –     | –      |             |

Table 3-6. Extended SFR (2nd SFR) List (3/6)

| Address | Special Function Register (SFR) Name | Symbol | R/W | Manipulable Bit Range |       |        | After Reset |
|---------|--------------------------------------|--------|-----|-----------------------|-------|--------|-------------|
|         |                                      |        |     | 1-bit                 | 8-bit | 16-bit |             |
| F0180H  | Timer counter register 00            | TCR00  | R   | –                     | –     | √      | FFFFH       |
| F0181H  |                                      |        |     |                       |       |        |             |
| F0182H  | Timer counter register 01            | TCR01  | R   | –                     | –     | √      | FFFFH       |
| F0183H  |                                      |        |     |                       |       |        |             |
| F0184H  | Timer counter register 02            | TCR02  | R   | –                     | –     | √      | FFFFH       |
| F0185H  |                                      |        |     |                       |       |        |             |
| F0186H  | Timer counter register 03            | TCR03  | R   | –                     | –     | √      | FFFFH       |
| F0187H  |                                      |        |     |                       |       |        |             |
| F0188H  | Timer counter register 04            | TCR04  | R   | –                     | –     | √      | FFFFH       |
| F0189H  |                                      |        |     |                       |       |        |             |
| F018AH  | Timer counter register 05            | TCR05  | R   | –                     | –     | √      | FFFFH       |
| F018BH  |                                      |        |     |                       |       |        |             |
| F018CH  | Timer counter register 06            | TCR06  | R   | –                     | –     | √      | FFFFH       |
| F018DH  |                                      |        |     |                       |       |        |             |
| F018EH  | Timer counter register 07            | TCR07  | R   | –                     | –     | √      | FFFFH       |
| F018FH  |                                      |        |     |                       |       |        |             |
| F0190H  | Timer mode register 00               | TMR00  | R/W | –                     | –     | √      | 0000H       |
| F0191H  |                                      |        |     |                       |       |        |             |
| F0192H  | Timer mode register 01               | TMR01  | R/W | –                     | –     | √      | 0000H       |
| F0193H  |                                      |        |     |                       |       |        |             |
| F0194H  | Timer mode register 02               | TMR02  | R/W | –                     | –     | √      | 0000H       |
| F0195H  |                                      |        |     |                       |       |        |             |
| F0196H  | Timer mode register 03               | TMR03  | R/W | –                     | –     | √      | 0000H       |
| F0197H  |                                      |        |     |                       |       |        |             |
| F0198H  | Timer mode register 04               | TMR04  | R/W | –                     | –     | √      | 0000H       |
| F0199H  |                                      |        |     |                       |       |        |             |
| F019AH  | Timer mode register 05               | TMR05  | R/W | –                     | –     | √      | 0000H       |
| F019BH  |                                      |        |     |                       |       |        |             |
| F019CH  | Timer mode register 06               | TMR06  | R/W | –                     | –     | √      | 0000H       |
| F019DH  |                                      |        |     |                       |       |        |             |
| F019EH  | Timer mode register 07               | TMR07  | R/W | –                     | –     | √      | 0000H       |
| F019FH  |                                      |        |     |                       |       |        |             |

Table 3-6. Extended SFR (2nd SFR) List (4/6)

| Address | Special Function Register (SFR) Name       | Symbol   |       | R/W | Manipulable Bit Range |       |        | After Reset |
|---------|--------------------------------------------|----------|-------|-----|-----------------------|-------|--------|-------------|
|         |                                            |          |       |     | 1-bit                 | 8-bit | 16-bit |             |
| F01A0H  | Timer status register 00                   | TSR00L   | TSR00 | R   | –                     | √     | √      | 0000H       |
| F01A1H  |                                            | –        |       |     | –                     |       |        |             |
| F01A2H  | Timer status register 01                   | TSR01L   | TSR01 | R   | –                     | √     | √      | 0000H       |
| F01A3H  |                                            | –        |       |     | –                     |       |        |             |
| F01A4H  | Timer status register 02                   | TSR02L   | TSR02 | R   | –                     | √     | √      | 0000H       |
| F01A5H  |                                            | –        |       |     | –                     |       |        |             |
| F01A6H  | Timer status register 03                   | TSR03L   | TSR03 | R   | –                     | √     | √      | 0000H       |
| F01A7H  |                                            | –        |       |     | –                     |       |        |             |
| F01A8H  | Timer status register 04                   | TSR04L   | TSR04 | R   | –                     | √     | √      | 0000H       |
| F01A9H  |                                            | –        |       |     | –                     |       |        |             |
| F01AAH  | Timer status register 05                   | TSR05L   | TSR05 | R   | –                     | √     | √      | 0000H       |
| F01ABH  |                                            | –        |       |     | –                     |       |        |             |
| F01ACH  | Timer status register 06                   | TSR06L   | TSR06 | R   | –                     | √     | √      | 0000H       |
| F01ADH  |                                            | –        |       |     | –                     |       |        |             |
| F01AEH  | Timer status register 07                   | TSR07L   | TSR07 | R   | –                     | √     | √      | 0000H       |
| F01AFH  |                                            | –        |       |     | –                     |       |        |             |
| F01B0H  | Timer channel enable status register 0     | TE0L     | TE0   | R   | √                     | √     | √      | 0000H       |
| F01B1H  |                                            | –        |       |     | –                     |       |        |             |
| F01B2H  | Timer channel start register 0             | TS0L     | TS0   | R/W | √                     | √     | √      | 0000H       |
| F01B3H  |                                            | –        |       |     | –                     |       |        |             |
| F01B4H  | Timer channel stop register 0              | TT0L     | TT0   | R/W | √                     | √     | √      | 0000H       |
| F01B5H  |                                            | –        |       |     | –                     |       |        |             |
| F01B6H  | Timer clock select register 0              | TPS0     |       | R/W | –                     | –     | √      | 0000H       |
| F01B7H  |                                            |          |       |     |                       |       |        |             |
| F01B8H  | Timer output register 0                    | TO0L     | TO0   | R/W | –                     | √     | √      | 0000H       |
| F01B9H  |                                            | –        |       |     | –                     |       |        |             |
| F01BAH  | Timer output enable register 0             | TOE0L    | TOE0  | R/W | √                     | √     | √      | 0000H       |
| F01BBH  |                                            | –        |       |     | –                     |       |        |             |
| F01BCH  | Timer output level register 0              | TOL0L    | TOL0  | R/W | –                     | √     | √      | 0000H       |
| F01BDH  |                                            | –        |       |     | –                     |       |        |             |
| F01BEH  | Timer output mode register 0               | TOM0L    | TOM0  | R/W | –                     | √     | √      | 0000H       |
| F01BFH  |                                            | –        |       |     | –                     |       |        |             |
| F0230H  | IICA control register 00                   | IICCTL00 |       | R/W | √                     | √     | –      | 00H         |
| F0231H  | IICA control register 01                   | IICCTL01 |       | R/W | √                     | √     | –      | 00H         |
| F0232H  | IICA low-level width setting register 0    | IICWL0   |       | R/W | –                     | √     | –      | FFH         |
| F0233H  | IICA high-level width setting register 0   | IICWH0   |       | R/W | –                     | √     | –      | FFH         |
| F0234H  | Slave address register 0                   | SVA0     |       | R/W | –                     | √     | –      | 00H         |
| F02F0H  | Flash memory CRC control register          | CRC0CTL  |       | R/W | √                     | √     | –      | 00H         |
| F02F2H  | Flash memory CRC operation result register | PGCRCL   |       | R/W | –                     | –     | √      | 0000H       |
| F02FAH  | CRC data register                          | CRCD     |       | R/W | –                     | –     | √      | 0000H       |



Table 3-6. Extended SFR (2nd SFR) List (5/6)

| Address | Special Function Register (SFR) Name | Symbol | R/W | Manipulable Bit Range |       |        | After Reset |
|---------|--------------------------------------|--------|-----|-----------------------|-------|--------|-------------|
|         |                                      |        |     | 1-bit                 | 8-bit | 16-bit |             |
| F0300H  | LCD port function register 0         | PFSEG0 | R/W | √                     | √     | –      | F0H         |
| F0301H  | LCD port function register 1         | PFSEG1 | R/W | √                     | √     | –      | FFH         |
| F0302H  | LCD port function register 2         | PFSEG2 | R/W | √                     | √     | –      | FFH         |
| F0303H  | LCD port function register 3         | PFSEG3 | R/W | √                     | √     | –      | FFH         |
| F0304H  | LCD port function register 4         | PFSEG4 | R/W | √                     | √     | –      | 7FH         |
| F0308H  | LCD Input switch control register    | ISCLCD | R/W | √                     | √     | –      | 00H         |
| F0400H  | LCD display data memory 0            | SEG0   | R/W | –                     | √     | –      | 00H         |
| F0401H  | LCD display data memory 1            | SEG1   | R/W | –                     | √     | –      | 00H         |
| F0402H  | LCD display data memory 2            | SEG2   | R/W | –                     | √     | –      | 00H         |
| F0403H  | LCD display data memory 3            | SEG3   | R/W | –                     | √     | –      | 00H         |
| F0404H  | LCD display data memory 4            | SEG4   | R/W | –                     | √     | –      | 00H         |
| F0405H  | LCD display data memory 5            | SEG5   | R/W | –                     | √     | –      | 00H         |
| F0406H  | LCD display data memory 6            | SEG6   | R/W | –                     | √     | –      | 00H         |
| F0407H  | LCD display data memory 7            | SEG7   | R/W | –                     | √     | –      | 00H         |
| F0408H  | LCD display data memory 8            | SEG8   | R/W | –                     | √     | –      | 00H         |
| F0409H  | LCD display data memory 9            | SEG9   | R/W | –                     | √     | –      | 00H         |
| F040AH  | LCD display data memory 10           | SEG10  | R/W | –                     | √     | –      | 00H         |
| F040BH  | LCD display data memory 11           | SEG11  | R/W | –                     | √     | –      | 00H         |
| F040CH  | LCD display data memory 12           | SEG12  | R/W | –                     | √     | –      | 00H         |
| F040DH  | LCD display data memory 13           | SEG13  | R/W | –                     | √     | –      | 00H         |
| F040EH  | LCD display data memory 14           | SEG14  | R/W | –                     | √     | –      | 00H         |
| F040FH  | LCD display data memory 15           | SEG15  | R/W | –                     | √     | –      | 00H         |
| F0410H  | LCD display data memory 16           | SEG16  | R/W | –                     | √     | –      | 00H         |
| F0411H  | LCD display data memory 17           | SEG17  | R/W | –                     | √     | –      | 00H         |
| F0412H  | LCD display data memory 18           | SEG18  | R/W | –                     | √     | –      | 00H         |
| F0413H  | LCD display data memory 19           | SEG19  | R/W | –                     | √     | –      | 00H         |
| F0414H  | LCD display data memory 20           | SEG20  | R/W | –                     | √     | –      | 00H         |
| F0415H  | LCD display data memory 21           | SEG21  | R/W | –                     | √     | –      | 00H         |
| F0416H  | LCD display data memory 22           | SEG22  | R/W | –                     | √     | –      | 00H         |
| F0417H  | LCD display data memory 23           | SEG23  | R/W | –                     | √     | –      | 00H         |
| F0418H  | LCD display data memory 24           | SEG24  | R/W | –                     | √     | –      | 00H         |
| F0419H  | LCD display data memory 25           | SEG25  | R/W | –                     | √     | –      | 00H         |

**Table 3-6. Extended SFR (2nd SFR) List (6/6)**

| Address | Special Function Register (SFR) Name | Symbol | R/W | Manipulable Bit Range |       |        | After Reset |
|---------|--------------------------------------|--------|-----|-----------------------|-------|--------|-------------|
|         |                                      |        |     | 1-bit                 | 8-bit | 16-bit |             |
| F041AH  | LCD display data memory 26           | SEG26  | R/W | –                     | √     | –      | 00H         |
| F041BH  | LCD display data memory 27           | SEG27  | R/W | –                     | √     | –      | 00H         |
| F041CH  | LCD display data memory 28           | SEG28  | R/W | –                     | √     | –      | 00H         |
| F041DH  | LCD display data memory 29           | SEG29  | R/W | –                     | √     | –      | 00H         |
| F041EH  | LCD display data memory 30           | SEG30  | R/W | –                     | √     | –      | 00H         |
| F041FH  | LCD display data memory 31           | SEG31  | R/W | –                     | √     | –      | 00H         |
| F0420H  | LCD display data memory 32           | SEG32  | R/W | –                     | √     | –      | 00H         |
| F0421H  | LCD display data memory 33           | SEG33  | R/W | –                     | √     | –      | 00H         |
| F0422H  | LCD display data memory 34           | SEG34  | R/W | –                     | √     | –      | 00H         |
| F0423H  | LCD display data memory 35           | SEG35  | R/W | –                     | √     | –      | 00H         |
| F0424H  | LCD display data memory 36           | SEG36  | R/W | –                     | √     | –      | 00H         |
| F0425H  | LCD display data memory 37           | SEG37  | R/W | –                     | √     | –      | 00H         |
| F0426H  | LCD display data memory 38           | SEG38  | R/W | –                     | √     | –      | 00H         |

**Remark** For SFRs in the SFR area, see **Table 3-5 SFR List**.

### 3.3 Instruction Address Addressing

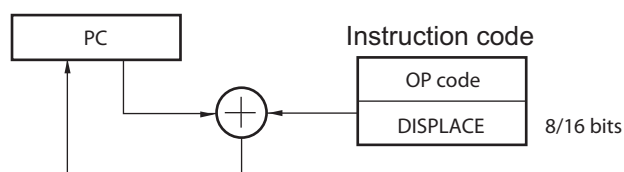
#### 3.3.1 Relative addressing

##### [Function]

Relative addressing stores in the program counter (PC) the result of adding a displacement value included in the instruction word (signed complement data:  $-128$  to  $+127$  or  $-32768$  to  $+32767$ ) to the program counter (PC)'s value (the start address of the next instruction), and specifies the program address to be used as the branch destination. Relative addressing is applied only to branch instructions.

&lt;R&gt;

Figure 3-14. Outline of Relative Addressing



#### 3.3.2 Immediate addressing

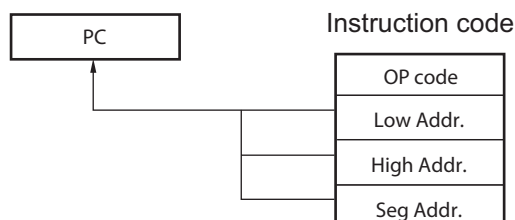
##### [Function]

Immediate addressing stores immediate data of the instruction word in the program counter, and specifies the program address to be used as the branch destination.

For immediate addressing, CALL !!addr20 or BR !!addr20 is used to specify 20-bit addresses and CALL !addr16 or BR !addr16 is used to specify 16-bit addresses. 0000 is set to the higher 4 bits when specifying 16-bit addresses.

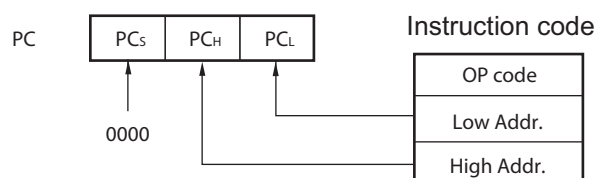
&lt;R&gt;

Figure 3-15. Example of CALL !!addr20/BR !!addr20



&lt;R&gt;

Figure 3-16. Example of CALL !addr16/BR !addr16



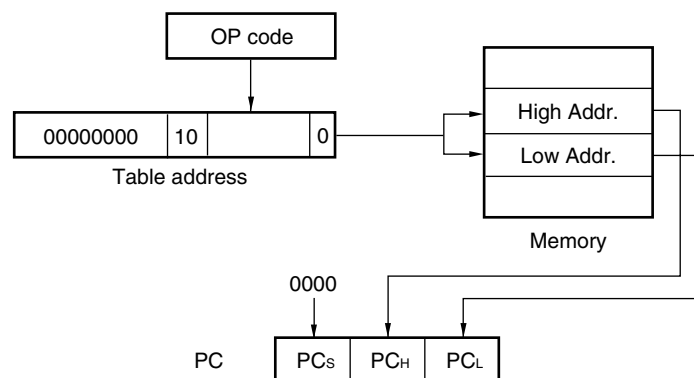
### 3.3.3 Table indirect addressing

#### [Function]

Table indirect addressing specifies a table address in the CALLT table area (0080H to 00BFH) with the 5-bit immediate data in the instruction word, stores the contents at that table address and the next address in the program counter (PC) as 16-bit data, and specifies the program address. Table indirect addressing is applied only for CALLT instructions.

In the RL78 microcontrollers, branching is enabled only to the 64 KB space from 00000H to 0FFFFH.

**Figure 3-17. Outline of Table Indirect Addressing**

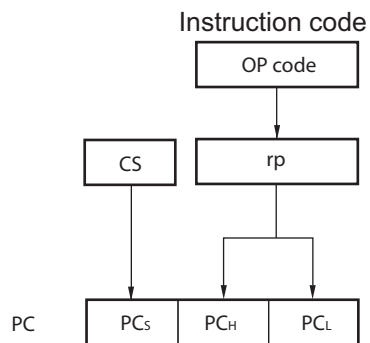


### 3.3.4 Register direct addressing

**[Function]**

Register direct addressing stores in the program counter (PC) the contents of a general-purpose register pair (AX/BC/DE/HL) and CS register of the current register bank specified with the instruction word as 20-bit data, and specifies the program address. Register direct addressing can be applied only to the CALL AX, BC, DE, HL, and BR AX instructions.

&lt;R&gt;

**Figure 3-18. Outline of Register Direct Addressing**

### 3.4 Addressing for Processing Data Addresses

#### 3.4.1 Implied addressing

##### [Function]

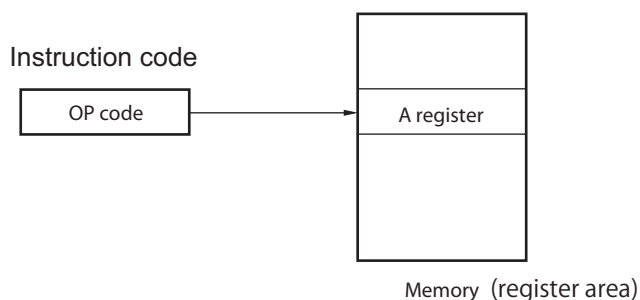
Instructions for accessing registers (such as accumulators) that have special functions are directly specified with the instruction word, without using any register specification field in the instruction word.

##### [Operand format]

<R> Implied addressing can be applied only to MULU X.

<R>

**Figure 3-19. Outline of Implied Addressing**



#### 3.4.2 Register addressing

##### [Function]

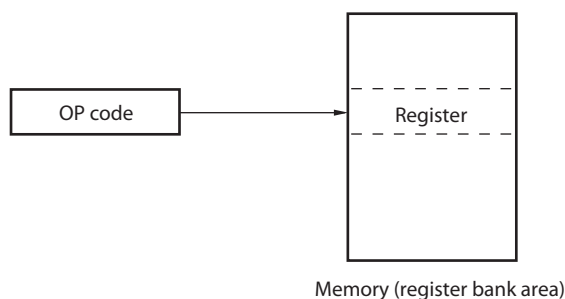
Register addressing accesses a general-purpose register as an operand. The instruction word of 3-bit long is used to select an 8-bit register and the instruction word of 2-bit long is used to select a 16-bit register.

##### [Operand format]

| Identifier | Description            |
|------------|------------------------|
| r          | X, A, C, B, E, D, L, H |
| rp         | AX, BC, DE, HL         |

<R>

**Figure 3-20. Outline of Register Addressing**



### 3.4.3 Direct addressing

#### [Function]

Direct addressing uses immediate data in the instruction word as an operand address to directly specify the target address.

#### [Operand format]

| Identifier     | Description                                                                              |
|----------------|------------------------------------------------------------------------------------------|
| <R> !addr16    | Label or 16-bit immediate data (only the space from F0000H to FFFFFH is specifiable)     |
| <R> ES:!addr16 | Label or 16-bit immediate data (higher 4-bit addresses are specified by the ES register) |

Figure 3-21. Example of ADDR16

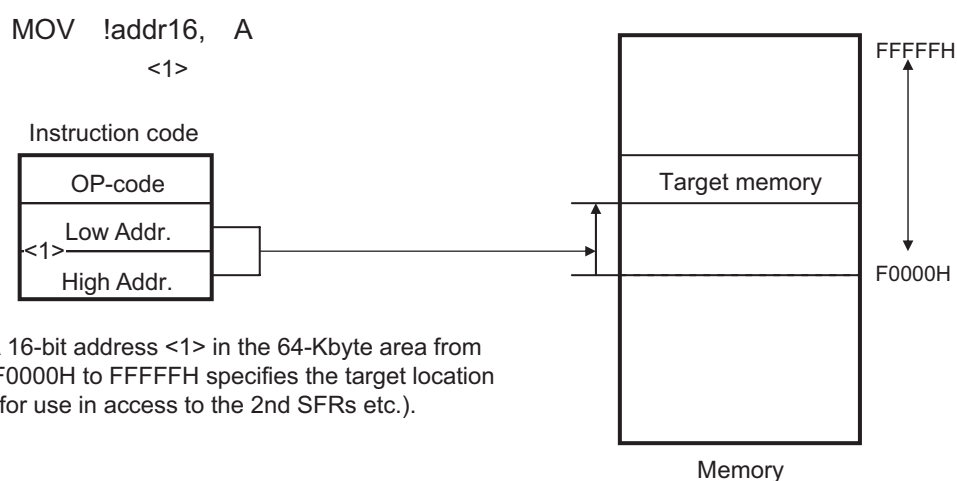
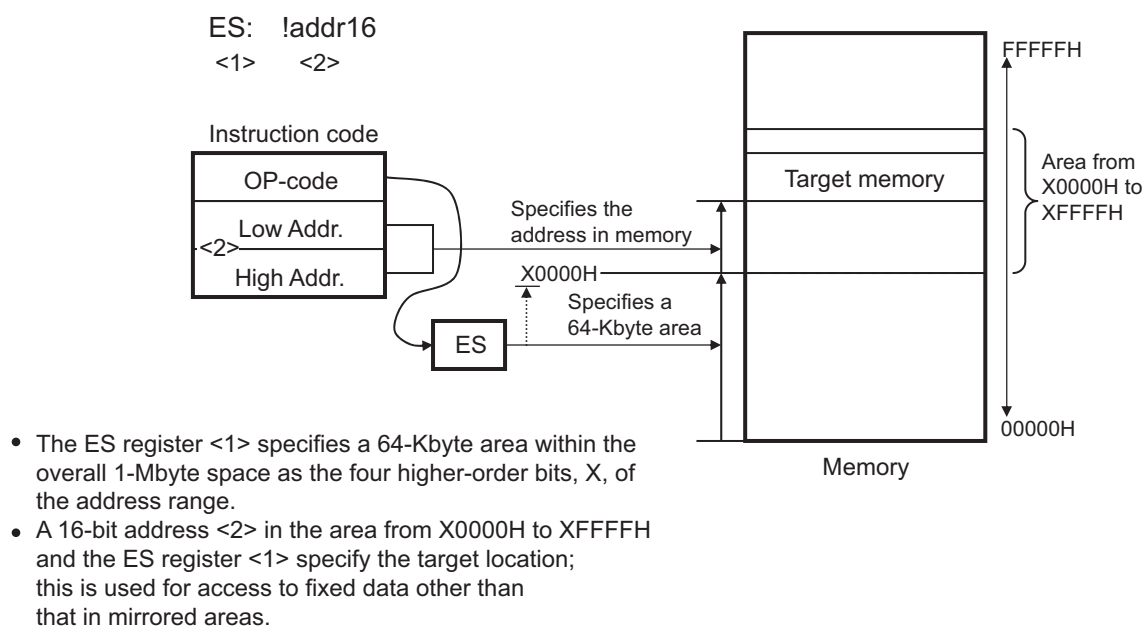


Figure 3-22. Example of ES:ADDR16



### 3.4.4 Short direct addressing

#### [Function]

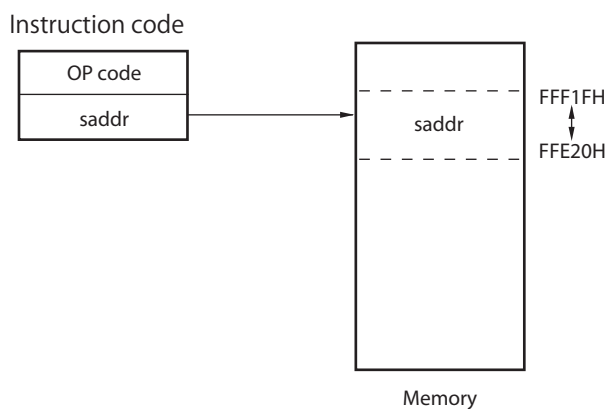
Short direct addressing directly specifies the target addresses using 8-bit data in the instruction word. This type of addressing is applied only to the space from FFE20H to FFF1FH.

#### [Operand format]

| Identifier | Description                                                                                                                                             |
|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| SADDR      | Label, FFE20H to FFF1FH immediate data, or 0FE20H to 0FF1FH immediate data<br>(only the space from FFE20H to FFF1FH is specifiable)                     |
| SADDRP     | Label, FFE20H to FFF1FH immediate data, or 0FE20H to 0FF1FH immediate data (even address only)<br>(only the space from FFE20H to FFF1FH is specifiable) |

<R>

**Figure 3-23. Outline of Short Direct Addressing**



**Remark** SADDR and SADDRP are used to describe the values of addresses FE20H to FF1FH with 16-bit immediate data (higher 4 bits of actual address are omitted), and the values of addresses FFE20H to FFF1FH with 20-bit immediate data.

Regardless of whether SADDR or SADDRP is used, addresses within the space from FFE20H to FFF1FH are specified for the memory.



### 3.4.5 SFR addressing

#### [Function]

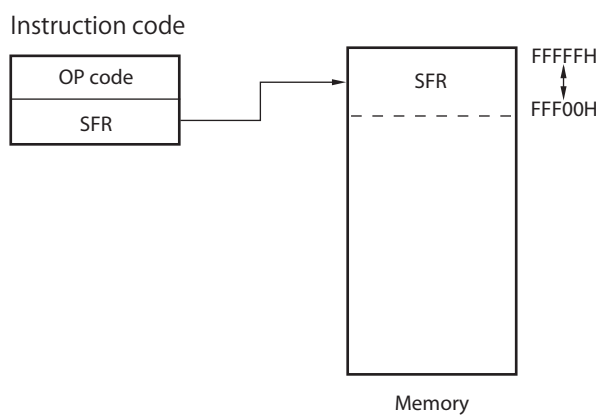
SFR addressing directly specifies the target SFR addresses using 8-bit data in the instruction word. This type of addressing is applied only to the space from FFF00H to FFFFFH.

#### [Operand format]

| Identifier | Description                                  |
|------------|----------------------------------------------|
| SFR        | SFR name                                     |
| SFRP       | 16-bit-manipulatable SFR name (even address) |

<R>

**Figure 3-24. Outline of SFR Addressing**



### 3.4.6 Register indirect addressing

#### [Function]

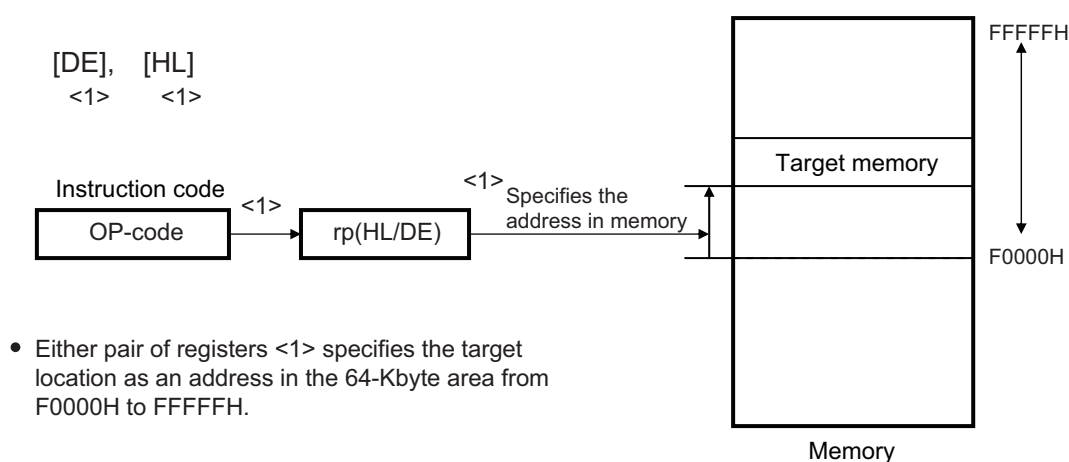
Register indirect addressing directly specifies the target addresses using the contents of the register pair specified with the instruction word as an operand address.

#### [Operand format]

| Identifier | Description                                                                |
|------------|----------------------------------------------------------------------------|
| –          | [DE], [HL] (only the space from F0000H to FFFFFH is specifiable)           |
| –          | ES:[DE], ES:[HL] (higher 4-bit addresses are specified by the ES register) |

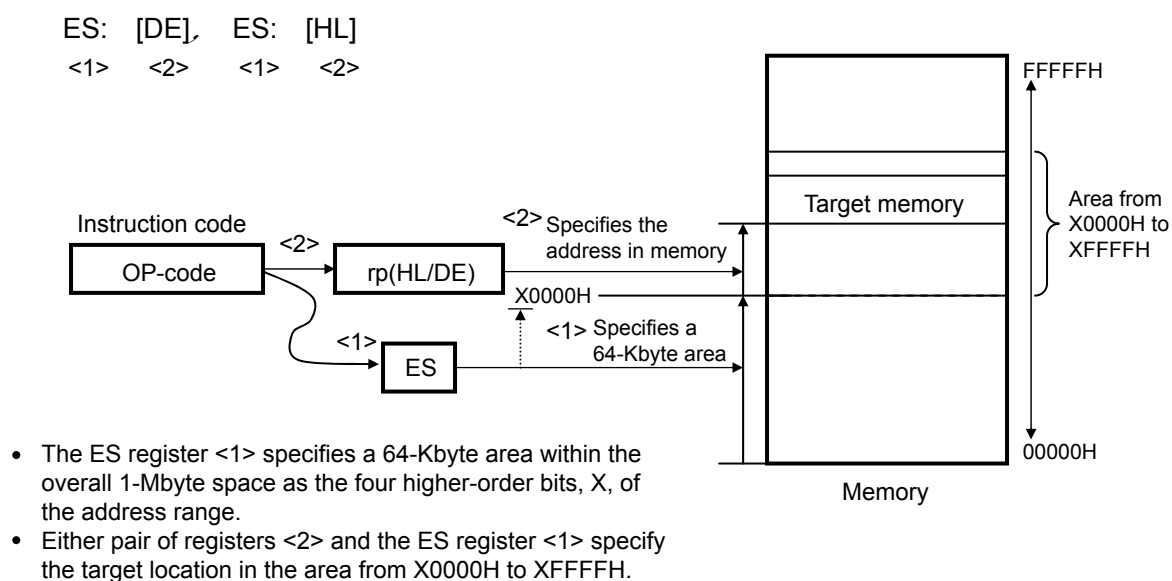
&lt;R&gt;

Figure 3-25. Example of [DE], [HL]



&lt;R&gt;

Figure 3-26. Example of ES:[DE], ES:[HL]



### 3.4.7 Based addressing

#### [Function]

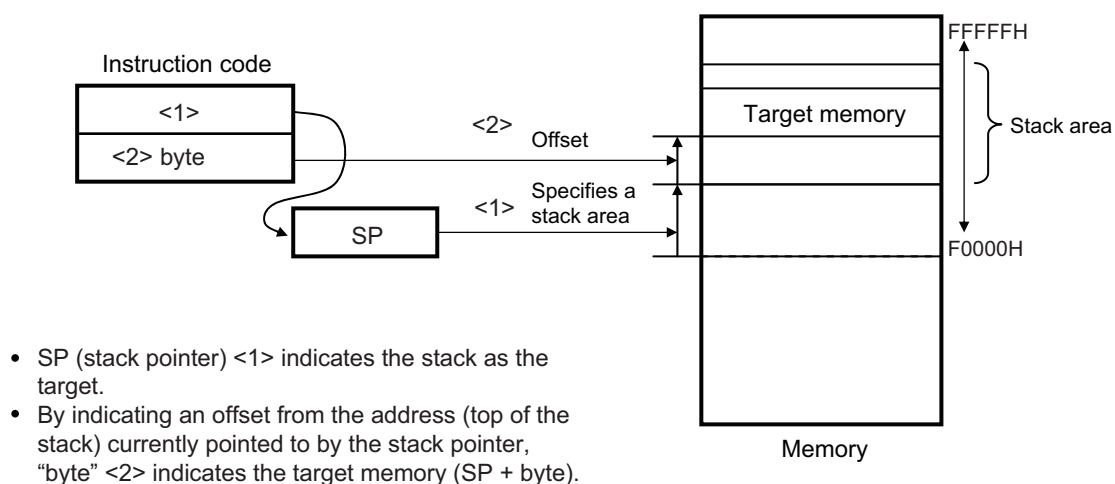
<R> Based addressing uses the contents of a register pair specified with the instruction word or 16-bit immediate data as a base address, and 8-bit immediate data or 16-bit immediate data as offset data. The sum of these values is used to specify the target address.

#### [Operand format]

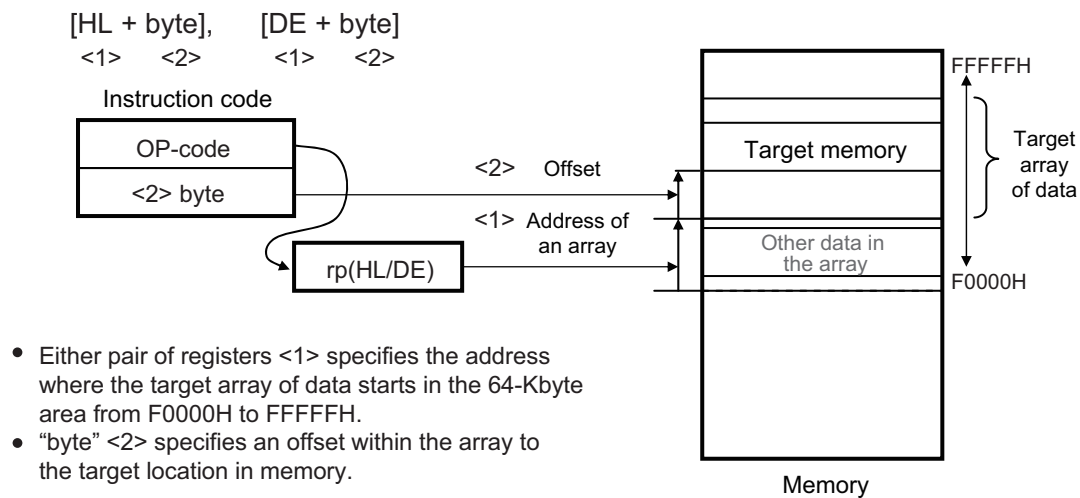
| Identifier | Description                                                                                 |
|------------|---------------------------------------------------------------------------------------------|
| –          | [HL + byte], [DE + byte], [SP + byte] (only the space from F0000H to FFFFFH is specifiable) |
| –          | word[B], word[C] (only the space from F0000H to FFFFFH is specifiable)                      |
| –          | word[BC] (only the space from F0000H to FFFFFH is specifiable)                              |
| –          | ES:[HL + byte], ES:[DE + byte] (higher 4-bit addresses are specified by the ES register)    |
| –          | ES:word[B], ES:word[C] (higher 4-bit addresses are specified by the ES register)            |
| –          | ES:word[BC] (higher 4-bit addresses are specified by the ES register)                       |

<R>

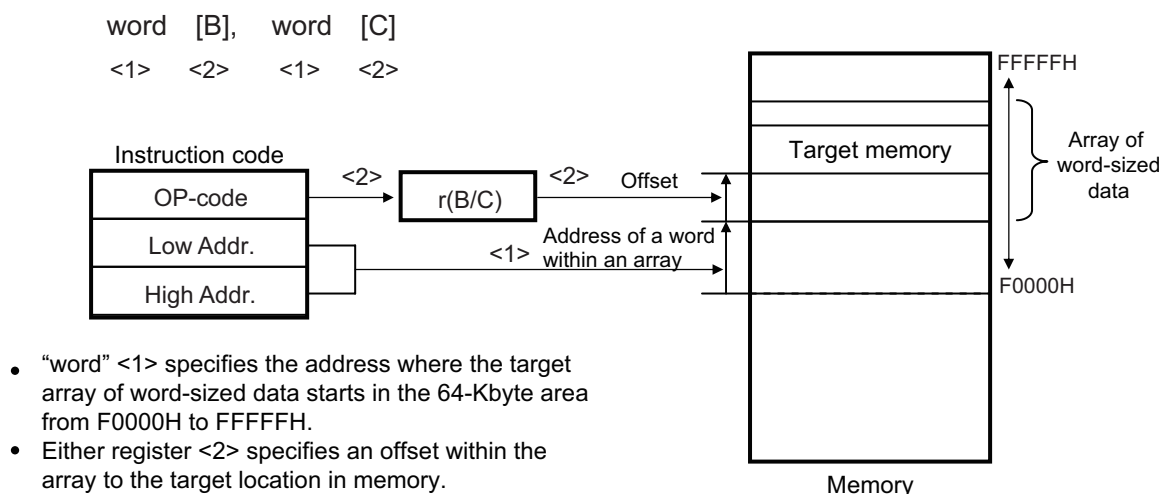
**Figure 3-27. Example of [SP+byte]**



&lt;R&gt;

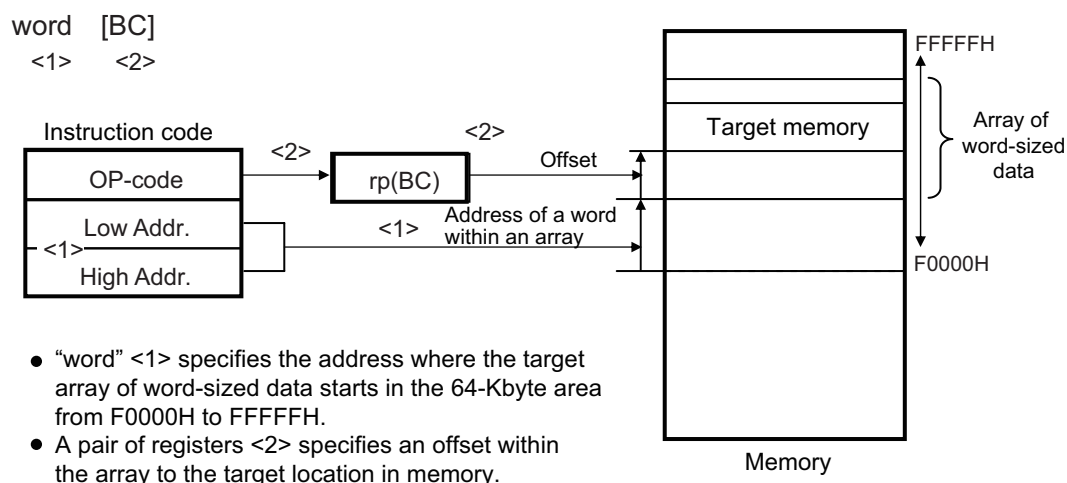
**Figure 3-28. Example of [HL + byte], [DE + byte]**

&lt;R&gt;

**Figure 3-29. Example of word[B], word[C]**

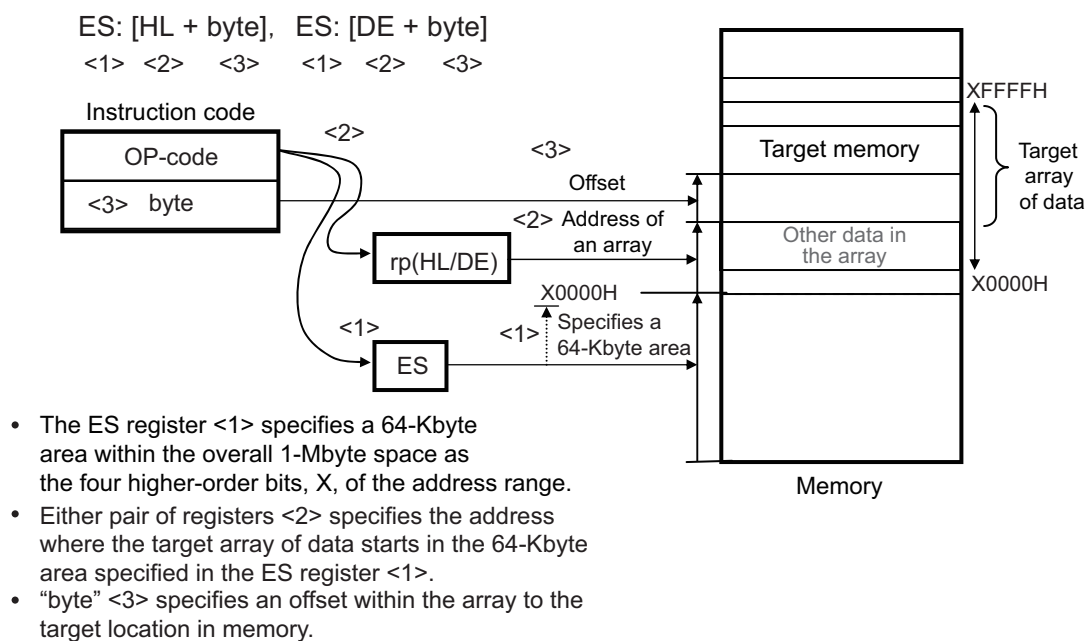
&lt;R&gt;

Figure 3-30. Example of word[BC]

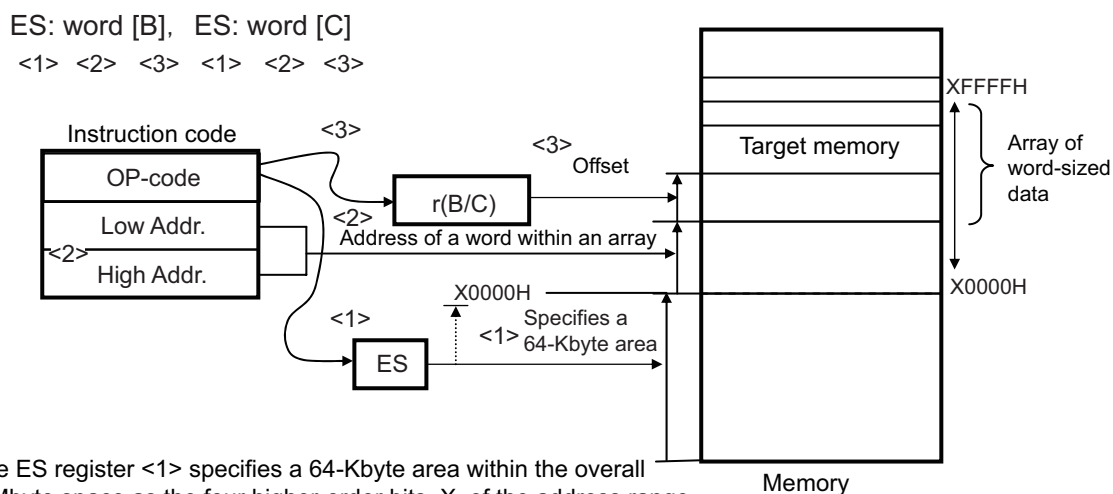


&lt;R&gt;

Figure 3-31. Example of ES:[HL + byte], ES:[DE + byte]

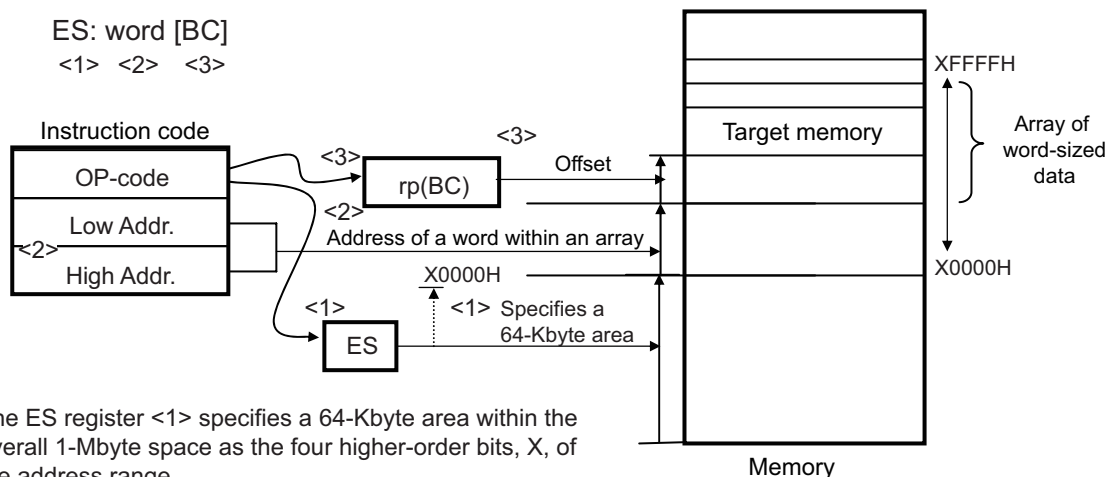


&lt;R&gt;

**Figure 3-32. Example of ES:word[B], ES:word[C]**

- The ES register <1> specifies a 64-Kbyte area within the overall 1-Mbyte space as the four higher-order bits, X, of the address range.
- “word” <2> specifies the address where the target array of word-sized data starts in the 64-Kbyte area specified in the ES register <1>.
- Either register <3> specifies an offset within the array to the target location in memory.

&lt;R&gt;

**Figure 3-33. Example of ES:word[BC]**

- The ES register <1> specifies a 64-Kbyte area within the overall 1-Mbyte space as the four higher-order bits, X, of the address range.
- “word” <2> specifies the address where the target array of word-sized data starts in the 64-Kbyte area specified in the ES register <1>.
- A pair of registers <3> specifies an offset within the array to the target location in memory.

### 3.4.8 Based indexed addressing

#### [Function]

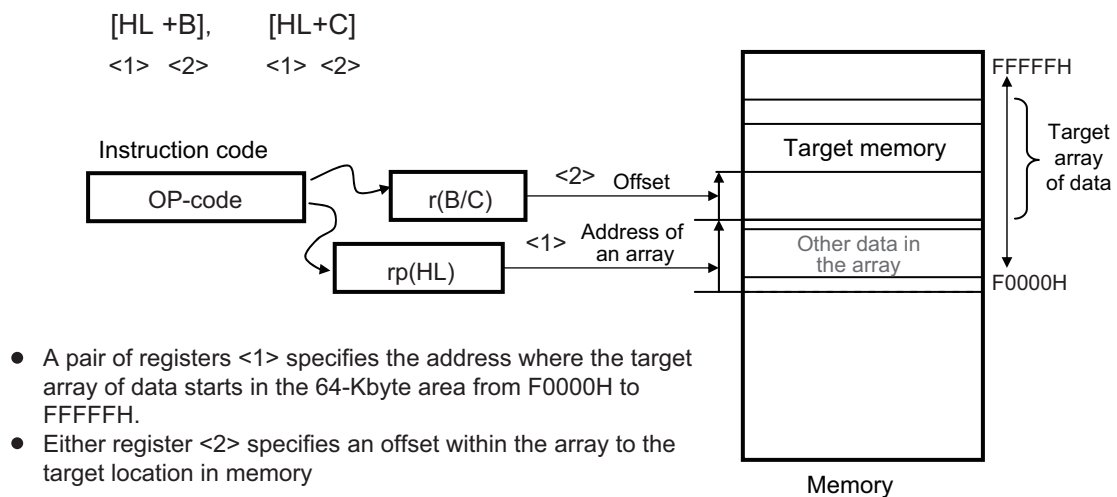
Based indexed addressing uses the contents of a register pair specified with the instruction word as the base address, and the content of the B register or C register similarly specified with the instruction word as offset address. The sum of these values is used to specify the target address.

#### [Operand format]

| Identifier | Description                                                                    |
|------------|--------------------------------------------------------------------------------|
| –          | [HL+B], [HL+C] (only the space from F0000H to FFFFFH is specifiable)           |
| –          | ES:[HL+B], ES:[HL+C] (higher 4-bit addresses are specified by the ES register) |

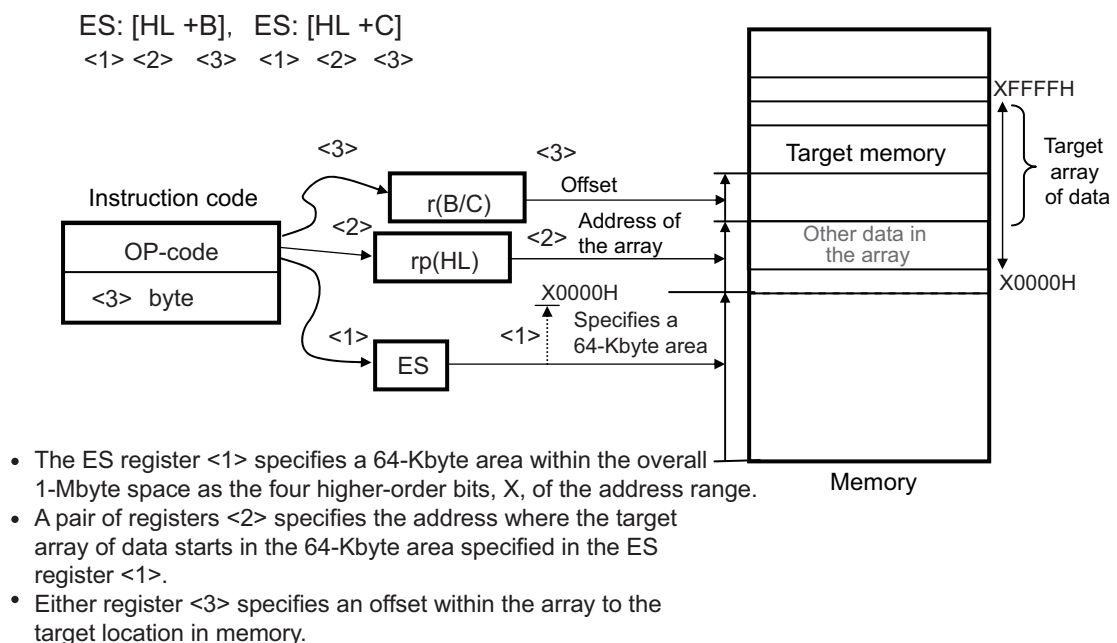
&lt;R&gt;

Figure 3-34. Example of [HL+B], [HL+C]



&lt;R&gt;

Figure 3-35. Example of ES:[HL+B], ES:[HL+C]



### 3.4.9 Stack addressing

#### [Function]

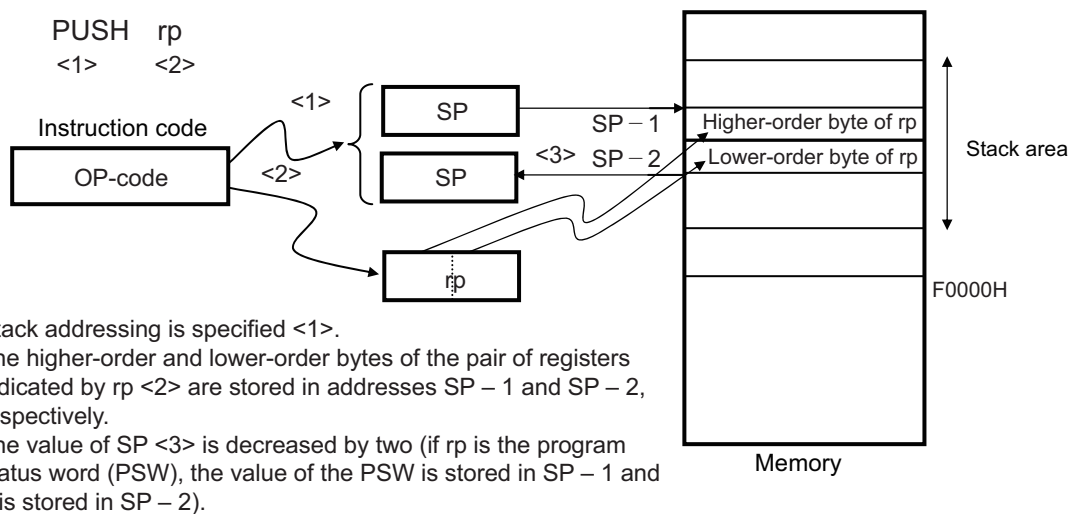
<R> The stack area is indirectly addressed with the stack pointer (SP) contents. This addressing is automatically employed when the PUSH, POP, subroutine call, and return instructions are executed or the register is saved/restored upon generation of an interrupt request.

Stack addressing is applied only to the internal RAM area.

#### <R> [Description format]

| Identifier | Description                                                                                                              |
|------------|--------------------------------------------------------------------------------------------------------------------------|
| –          | PUSH PSW AX/BC/DE/HL<br>POP PSW AX/BC/DE/HL<br>CALL/CALLT<br>RET<br>BRK<br>RETB<br>(Interrupt request generated)<br>RETI |

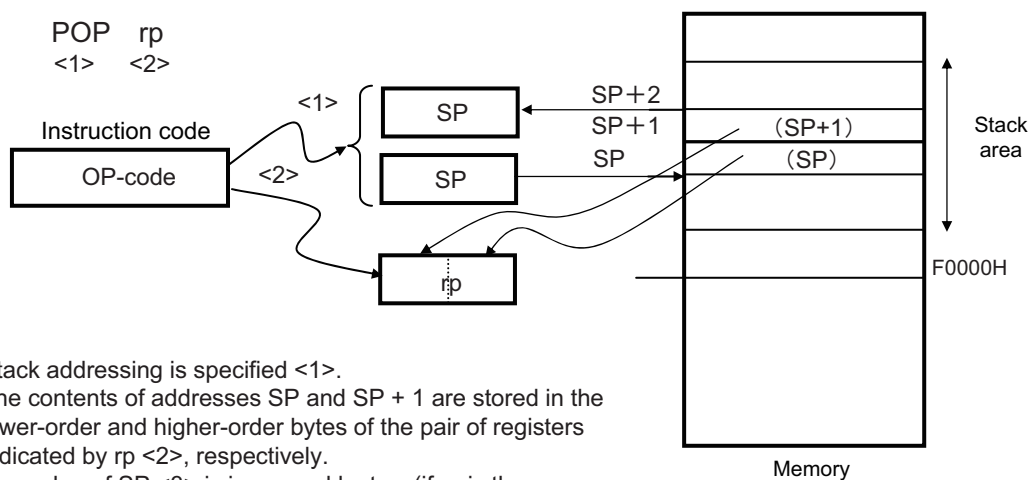
<R> **Figure 3-36. Example of PUSH rp**





&lt;R&gt;

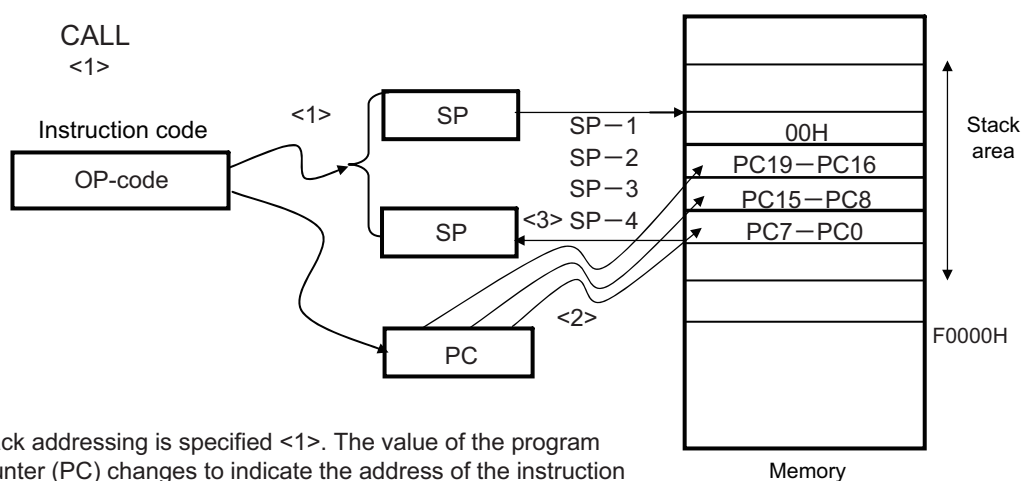
Figure 3-37. Example of POP



- Stack addressing is specified <1>.
- The contents of addresses SP and SP + 1 are stored in the lower-order and higher-order bytes of the pair of registers indicated by rp <2>, respectively.
- The value of SP <3> is increased by two (if rp is the program status word (PSW), the content of address SP + 1 is stored in the PSW).

&lt;R&gt;

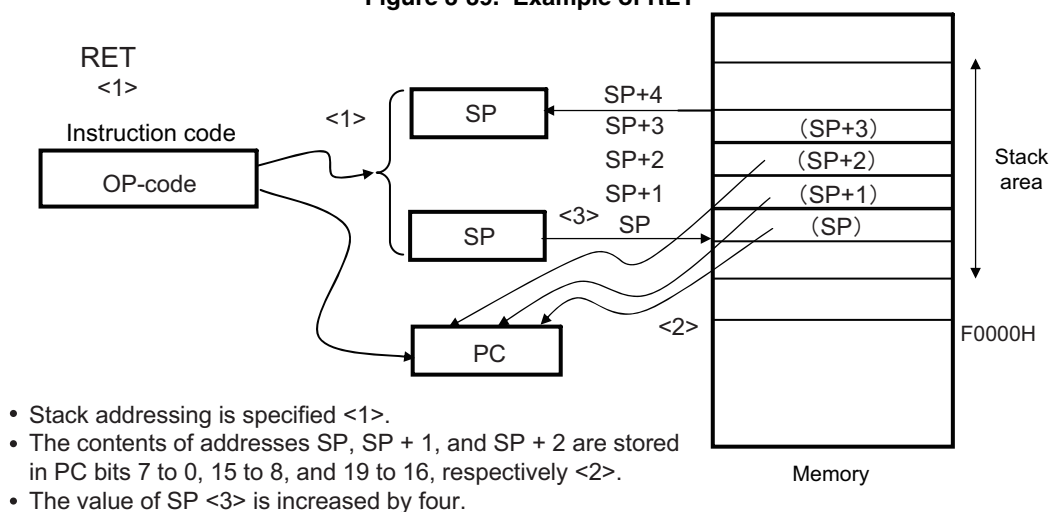
Figure 3-38. Example of CALL, CALLT



- Stack addressing is specified <1>. The value of the program counter (PC) changes to indicate the address of the instruction following the CALL instruction.
- 00H, the values of PC bits 19 to 16, 15 to 8, and 7 to 0 are stored in addresses SP - 1, SP - 2, SP - 3, and SP - 4, respectively <2>.
- The value of the SP <3> is decreased by 4.

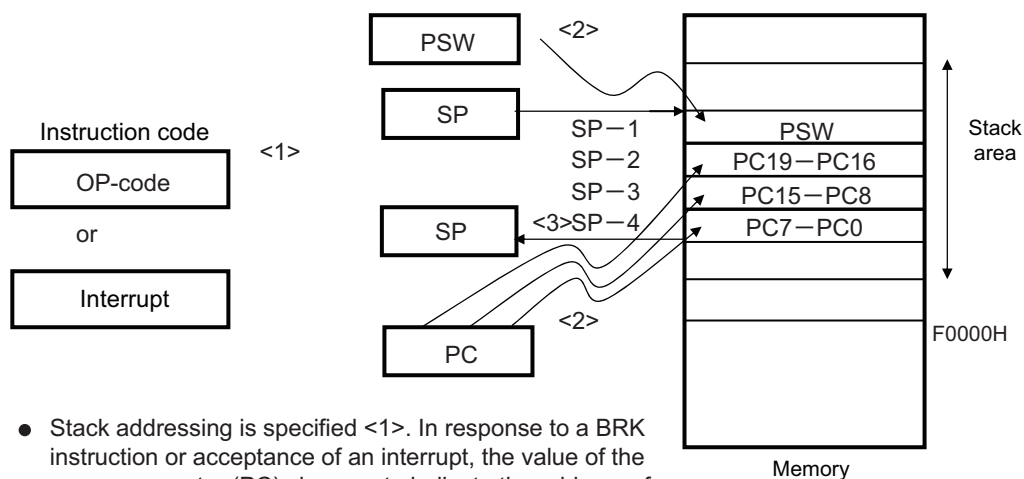
&lt;R&gt;

Figure 3-39. Example of RET



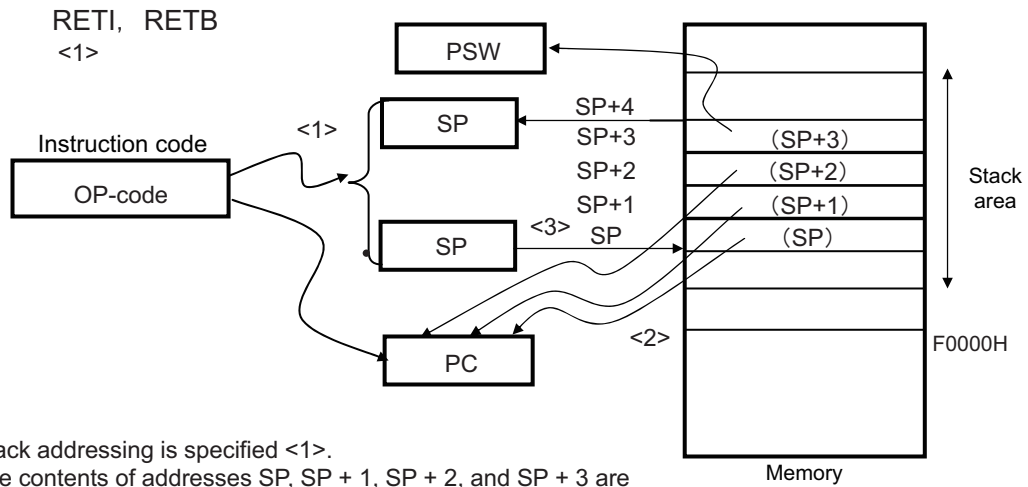
&lt;R&gt;

Figure 3-40. Example of Interrupt, BRK



<R>

**Figure 3-41. Example of RETI, RETB**



- Stack addressing is specified <1>.
- The contents of addresses SP, SP + 1, SP + 2, and SP + 3 are stored in PC bits 7 to 0, 15 to 8, 19 to 16, and the PSW, respectively <2>.
- The value of SP <3> is increased by four.

## CHAPTER 4 PORT FUNCTIONS

### 4.1 Port Functions

<R> The RL78/L12 microcontrollers are provided with digital I/O ports, which enable variety of control operations.

In addition to the function as digital I/O ports, these ports have several alternate functions. For details of the alternate functions, see **CHAPTER 2 PIN FUNCTIONS**.

## 4.2 Port Configuration

Ports include the following hardware.

**Table 4-1. Port Configuration**

| Item              | Configuration                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Control registers | Port mode registers (PM1 to PM7, PM12, PM14)<br>Port registers (P1 to P7, P12-P14)<br>Pull-up resistor option registers (PU1, PU3 to PU5, PU7, PU12, PU14)<br>Port input mode register (PIM1)<br>Port output mode register (POM1)<br>Port mode control registers (PMC1, PMC4, PMC12, PMC14)<br>A/D port configuration register (ADPC)<br>Peripheral I/O redirection register (PIOR)<br>LCD port function registers (PFSEG0 PFSEG4)<br>LCD input switch control register (ISCLCD)                                                                    |
| Port              | <ul style="list-style-type: none"> <li>• 32-pin products<br/>Total: 20 (CMOS I/O: 15, CMOS input: 3, N-ch open drain I/O: 2)</li> <li>• 44-pin products<br/>Total: 29 (CMOS I/O: 22, CMOS input: 5, N-ch open drain I/O: 2)</li> <li>• 48-pin products<br/>Total: 33 (CMOS I/O: 26, CMOS input: 5, N-ch open drain I/O: 2)</li> <li>• 52-pin products<br/>Total: 37 (CMOS I/O: 30, CMOS input: 5, N-ch open drain I/O: 2)</li> <li>• 64-pin products<br/>Total: 47 (CMOS I/O: 39, CMOS input: 5, CMOS output: 1, N-ch open drain I/O: 2)</li> </ul> |
| Pull-up resistor  | <ul style="list-style-type: none"> <li>• 32-pin products Total: 13</li> <li>• 44-pin products Total: 20</li> <li>• 48-pin products Total: 24</li> <li>• 52-pin products Total: 28</li> <li>• 64-pin products Total: 37</li> </ul>                                                                                                                                                                                                                                                                                                                   |

### 4.3 Registers Controlling Port Function

Port functions are controlled by the following registers.

- Port mode registers (PMxx)
- Port registers (Pxx)
- Pull-up resistor option registers (PUxx)
- Port input mode registers (PIMxx)
- Port output mode registers (POMxx)
- Port mode control registers (PMCxx)
- A/D port configuration register (ADPC)
- Peripheral I/O redirection register (PIOR)
- LCD port function registers (PFSEG0 to PFSEG4)
- LCD input switch control register (ISCLCD)

<R> **Caution** The undefined bits in each register vary by product and must be used with their initial value.

**Table 4-2. PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits mounted on each product (1/3)**

| Port   |   | Bit name         |                 |                  |                   |                   |                   | 64  | 52  | 48  | 44  | 32  |
|--------|---|------------------|-----------------|------------------|-------------------|-------------------|-------------------|-----|-----|-----|-----|-----|
|        |   | PMxx<br>register | Pxx<br>register | PUxx<br>register | PIMxx<br>register | POMxx<br>register | PMCxx<br>register | pin | pin | pin | pin | pin |
| Port 0 | – | –                | –               | –                | –                 | –                 | –                 | –   | –   | –   | –   | –   |
| Port 1 | 0 | PM10             | P10             | PU10             | PIM10             | POM10             | –                 | √   | √   | √   | √   | √   |
|        | 1 | PM11             | P11             | PU11             | PIM11             | –                 | –                 | √   | √   | √   | √   | √   |
|        | 2 | PM12             | P12             | PU12             | –                 | POM12             | –                 | √   | √   | √   | √   | √   |
|        | 3 | PM13             | P13             | PU13             | –                 | –                 | PMC13             | √   | √   | √   | √   | √   |
|        | 4 | PM14             | P14             | PU14             | –                 | –                 | PMC14             | √   | √   | √   | √   | √   |
|        | 5 | PM15             | P15             | PU15             | PIM15             | POM15             | –                 | √   | √   | √   | √   | √   |
|        | 6 | PM16             | P16             | PU16             | PIM16             | –                 | –                 | √   | √   | √   | √   | √   |
|        | 7 | PM17             | P17             | PU17             | –                 | POM17             | –                 | √   | √   | √   | √   | √   |
| Port 2 | 0 | PM20             | P20             | –                | –                 | –                 | –                 | √   | √   | √   | √   | √   |
|        | 1 | PM21             | P21             | –                | –                 | –                 | –                 | √   | √   | √   | √   | √   |
|        | 2 | –                | –               | –                | –                 | –                 | –                 | –   | –   | –   | –   | –   |
|        | 3 | –                | –               | –                | –                 | –                 | –                 | –   | –   | –   | –   | –   |
|        | 4 | –                | –               | –                | –                 | –                 | –                 | –   | –   | –   | –   | –   |
|        | 5 | –                | –               | –                | –                 | –                 | –                 | –   | –   | –   | –   | –   |
|        | 6 | –                | –               | –                | –                 | –                 | –                 | –   | –   | –   | –   | –   |
|        | 7 | –                | –               | –                | –                 | –                 | –                 | –   | –   | –   | –   | –   |

Table 4-2. PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits mounted on each product (2/3)

| Port   |   | Bit name      |              |               |                |                |                | 64 pin | 52 pin | 48 pin | 44 pin | 32 pin |
|--------|---|---------------|--------------|---------------|----------------|----------------|----------------|--------|--------|--------|--------|--------|
|        |   | PMxx register | Pxx register | PUxx register | PIMxx register | POMxx register | PMCxx register |        |        |        |        |        |
| Port 3 | 0 | PM30          | P30          | PU30          | —              | —              | —              | √      | √      | √      | √      | √      |
|        | 1 | PM31          | P31          | PU31          | —              | —              | —              | √      | √      | √      | √      | —      |
|        | 2 | PM32          | P32          | PU32          | —              | —              | —              | √      | √      | √      | √      | —      |
|        | 3 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
|        | 4 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
|        | 5 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
|        | 6 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
|        | 7 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
| Port 4 | 0 | PM40          | P40          | PU40          | —              | —              | —              | √      | √      | √      | √      | √      |
|        | 1 | PM41          | P41          | PU41          | —              | —              | PMC41          | √      | √      | √      | —      | —      |
|        | 2 | PM42          | P42          | PU42          | —              | —              | —              | √      | √      | —      | —      | —      |
|        | 3 | PM43          | P43          | PU43          | —              | —              | —              | √      | —      | —      | —      | —      |
|        | 4 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
|        | 5 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
|        | 6 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
|        | 7 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
| Port 5 | 0 | PM50          | P50          | PU50          | —              | —              | —              | √      | √      | √      | —      | —      |
|        | 1 | PM51          | P51          | PU51          | —              | —              | —              | √      | √      | —      | —      | —      |
|        | 2 | PM52          | P52          | PU52          | —              | —              | —              | √      | —      | —      | —      | —      |
|        | 3 | PM53          | P53          | PU53          | —              | —              | —              | √      | —      | —      | —      | —      |
|        | 4 | PM54          | P54          | PU54          | —              | —              | —              | √      | —      | —      | —      | —      |
|        | 5 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
|        | 6 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
|        | 7 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
| Port 6 | 0 | PM60          | P60          | —             | —              | —              | —              | √      | √      | √      | √      | √      |
|        | 1 | PM61          | P61          | —             | —              | —              | —              | √      | √      | √      | √      | √      |
|        | 2 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
|        | 3 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
|        | 4 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
|        | 5 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
|        | 6 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
|        | 7 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
| Port 7 | 0 | PM70          | P70          | PU70          | —              | —              | —              | √      | √      | √      | —      | —      |
|        | 1 | PM71          | P71          | PU71          | —              | —              | —              | √      | √      | —      | —      | —      |
|        | 2 | PM72          | P72          | PU72          | —              | —              | —              | √      | —      | —      | —      | —      |
|        | 3 | PM73          | P73          | PU73          | —              | —              | —              | √      | —      | —      | —      | —      |
|        | 4 | PM74          | P74          | PU74          | —              | —              | —              | √      | —      | —      | —      | —      |
|        | 5 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
|        | 6 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |
|        | 7 | —             | —            | —             | —              | —              | —              | —      | —      | —      | —      | —      |

Table 4-2. PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits mounted on each product (3/3)

| Port    |   | Bit name         |                 |                  |                   |                   |                   | 64<br>pin | 52<br>pin | 48<br>pin | 44<br>pin | 32<br>pin |
|---------|---|------------------|-----------------|------------------|-------------------|-------------------|-------------------|-----------|-----------|-----------|-----------|-----------|
|         |   | PMxx<br>register | Pxx<br>register | PUxx<br>register | PIMxx<br>register | POMxx<br>register | PMCxx<br>register |           |           |           |           |           |
| Port 8  | – | –                | –               | –                | –                 | –                 | –                 | –         | –         | –         | –         | –         |
| Port 9  | – | –                | –               | –                | –                 | –                 | –                 | –         | –         | –         | –         | –         |
| Port 10 | – | –                | –               | –                | –                 | –                 | –                 | –         | –         | –         | –         | –         |
| Port 11 | – | –                | –               | –                | –                 | –                 | –                 | –         | –         | –         | –         | –         |
| Port 12 | 0 | PM120            | P120            | PU120            | –                 | –                 | PMC120            | √         | √         | √         | √         | –         |
|         | 1 | –                | P121            | –                | –                 | –                 | –                 | √         | √         | √         | √         | √         |
|         | 2 | –                | P122            | –                | –                 | –                 | –                 | √         | √         | √         | √         | √         |
|         | 3 | –                | P123            | –                | –                 | –                 | –                 | √         | √         | √         | √         | –         |
|         | 4 | –                | P124            | –                | –                 | –                 | –                 | √         | √         | √         | √         | –         |
|         | 5 | PM125            | P125            | PU125            | –                 | –                 | –                 | √         | √         | √         | √         | –         |
|         | 6 | PM126            | P126            | PU126            | –                 | –                 | –                 | √         | √         | √         | √         | √         |
|         | 7 | PM127            | P127            | PU127            | –                 | –                 | –                 | √         | √         | √         | √         | √         |
| Port 13 | 0 | –                | P130            | –                | –                 | –                 | –                 | √         | –         | –         | –         | –         |
|         | 1 | –                | –               | –                | –                 | –                 | –                 | –         | –         | –         | –         | –         |
|         | 2 | –                | –               | –                | –                 | –                 | –                 | –         | –         | –         | –         | –         |
|         | 3 | –                | –               | –                | –                 | –                 | –                 | –         | –         | –         | –         | –         |
|         | 4 | –                | –               | –                | –                 | –                 | –                 | –         | –         | –         | –         | –         |
|         | 5 | –                | –               | –                | –                 | –                 | –                 | –         | –         | –         | –         | –         |
|         | 6 | –                | –               | –                | –                 | –                 | –                 | –         | –         | –         | –         | –         |
|         | 7 | –                | P137            | –                | –                 | –                 | –                 | √         | √         | √         | √         | √         |
| Port 14 | 0 | PM140            | P140            | PU140            | –                 | –                 | –                 | √         | √         | √         | √         | √         |
|         | 1 | PM141            | P141            | PU141            | –                 | –                 | –                 | √         | √         | √         | √         | –         |
|         | 2 | PM142            | P142            | PU142            | –                 | –                 | PMC142            | √         | √         | √         | √         | –         |
|         | 3 | PM143            | P143            | PU143            | –                 | –                 | PMC143            | √         | √         | √         | √         | –         |
|         | 4 | PM144            | P144            | PU144            | –                 | –                 | PMC144            | √         | √         | √         | –         | –         |
|         | 5 | PM145            | P145            | PU145            | –                 | –                 | PMC145            | √         | √         | –         | –         | –         |
|         | 6 | PM146            | P146            | PU146            | –                 | –                 | –                 | √         | –         | –         | –         | –         |
|         | 7 | PM147            | P147            | PU147            | –                 | –                 | –                 | √         | –         | –         | –         | –         |
| Port 15 | – | –                | –               | –                | –                 | –                 | –                 | –         | –         | –         | –         | –         |

The format of each register is described below. The description here uses the 64-pin products as an example.



For the registers mounted on others than 64-pin products, refer to **table 4-2**.

#### 4.3.1 Port mode registers (PMxx)

These registers specify input or output mode for the port in 1-bit units.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

When port pins are used as alternate-function pins, set the port mode register by referencing **4.5 Settings of Port Related Register When Using Alternate Function**.

Figure 4-1. Format of Port Mode Register (64-pin products)

| Symbol | 7                                                              | 6     | 5     | 4     | 3     | 2     | 1     | 0     | Address | After reset | R/W |
|--------|----------------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|---------|-------------|-----|
| PM1    | PM17                                                           | PM16  | PM15  | PM14  | PM13  | PM12  | PM11  | PM10  | FFF21H  | FFH         | R/W |
| PM2    | 1                                                              | 1     | 1     | 1     | 1     | 1     | PM21  | PM20  | FFF22H  | FFH         | R/W |
| PM3    | 1                                                              | 1     | 1     | 1     | 1     | PM32  | PM31  | PM30  | FFF23H  | FFH         | R/W |
| PM4    | 1                                                              | 1     | 1     | 1     | PM43  | PM42  | PM41  | PM40  | FFF24H  | FFH         | R/W |
| PM5    | 1                                                              | 1     | 1     | PM54  | PM53  | PM52  | PM51  | PM50  | FFF25H  | FFH         | R/W |
| PM6    | 1                                                              | 1     | 1     | 1     | 1     | 1     | PM61  | PM60  | FFF26H  | FFH         | R/W |
| PM7    | 1                                                              | 1     | 1     | PM74  | PM73  | PM72  | PM71  | PM70  | FFF27H  | FFH         | R/W |
| PM12   | PM127                                                          | PM126 | PM125 | 1     | 1     | 1     | 1     | PM120 | FFF2CH  | FFH         | R/W |
| PM14   | PM147                                                          | PM146 | PM145 | PM144 | PM143 | PM142 | PM141 | PM140 | FFF2EH  | FFH         | R/W |
| PMmn   | Pmn pin I/O mode selection<br>(m = 1 to 7, 12, 14; n = 0 to 7) |       |       |       |       |       |       |       |         |             |     |
| 0      | Output mode (output buffer on)                                 |       |       |       |       |       |       |       |         |             |     |
| 1      | Input mode (output buffer off)                                 |       |       |       |       |       |       |       |         |             |     |

**Caution** Be sure to set bits 2 to 7 of the PM2 register, bits 3 to 7 of the PM3 register, bits 4 to 7 of the PM4 register, bits 5 to 7 of the PM5 register, bits 2 to 7 of the PM6 register, bits 5 to 7 of the PM7 register, and bits 1 to 4 of the PM12 register to “1”.

### 4.3.2 Port registers (Pxx)

These registers set the output latch value of a port.

If the data is read in the input mode, the pin level is read. If it is read in the output mode, the output latch value is read<sup>Note</sup>.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

**Note** If P13, P14, P20, P21, P41, P120, and P142 to P145 are set up as analog inputs of the A/D converter, when a port is read while in the input mode, 0 is always returned, not the pin level.

**Figure 4-2. Format of Port Register (64-pin products)**

| Symbol | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    | Address | After reset        | R/W                   |
|--------|------|------|------|------|------|------|------|------|---------|--------------------|-----------------------|
| P1     | P17  | P16  | P15  | P14  | P13  | P12  | P11  | P10  | FFF01H  | 00H (output latch) | R/W                   |
| P2     | 0    | 0    | 0    | 0    | 0    | 0    | P21  | P20  | FFF02H  | 00H (output latch) | R/W                   |
| P3     | 0    | 0    | 0    | 0    | 0    | P32  | P31  | P30  | FFF03H  | 00H (output latch) | R/W                   |
| P4     | 0    | 0    | 0    | 0    | P43  | P42  | P41  | P40  | FFF04H  | 00H (output latch) | R/W                   |
| P5     | 0    | 0    | 0    | P54  | P53  | P52  | P51  | P50  | FFF05H  | 00H (output latch) | R/W                   |
| P6     | 0    | 0    | 0    | 0    | 0    | 0    | P61  | P60  | FFF06H  | 00H (output latch) | R/W                   |
| P7     | 0    | 0    | 0    | P74  | P73  | P72  | P71  | P70  | FFF07H  | 00H (output latch) | R/W                   |
| P12    | P127 | P126 | P125 | P124 | P123 | P122 | P121 | P120 | FFF0CH  | Undefined          | R/W <sup>Note 1</sup> |
| P13    | P137 | 0    | 0    | 0    | 0    | 0    | 0    | P130 | FFF0DH  | Note 2             | R/W <sup>Note 1</sup> |
| P14    | P147 | P146 | P145 | P144 | P143 | P142 | P141 | P140 | FFF0EH  | 00H (output latch) | R/W                   |

| Pmn | Output data control (in output mode) | Input data read (in input mode) |
|-----|--------------------------------------|---------------------------------|
| 0   | Output 0                             | Input low level                 |
| 1   | Output 1                             | Input high level                |

**Notes 1.** P121 to P124, and P137 are read-only.

**2.** P137 : Undefined

P130: 0 (output latch)

**Remark** m = 1 to 7, 12 to 14; n = 0 to 7

### 4.3.3 Pull-up resistor option registers (PUxx)

These registers specify whether the on-chip pull-up resistors are to be used or not. On-chip pull-up resistors can be used in 1-bit units only for the bits set to input mode ( $PM_{mn} = 1$  and  $POM_{mn} = 0$ ) for the pins to which the use of an on-chip pull-up resistor has been specified in these registers. On-chip pull-up resistors cannot be connected to bits set to <R> output mode and bits used as alternate-function output pins and analog setting ( $PMC = 1$ ,  $ADPC = 1$ ), regardless of the settings of these registers.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H (Only PU4 is set to 01H).

<R> **Caution** When a port with the  $PIM_n$  register is input from different potential device to TTL buffer, pull up to the power supply of the different potential device via a external pull-up resistor by setting  $PUM_n = 0$ .

Figure 4-3. Format of Pull-up Resistor Option Register (64-pin products)

| Symbol | 7                                                                                    | 6     | 5     | 4     | 3     | 2     | 1     | 0     | Address | After reset | R/W |
|--------|--------------------------------------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|---------|-------------|-----|
| PU1    | PU17                                                                                 | PU16  | PU15  | PU14  | PU13  | PU12  | PU11  | PU10  | F0031H  | 00H         | R/W |
| PU3    | 0                                                                                    | 0     | 0     | 0     | 0     | PU32  | PU31  | PU30  | F0033H  | 00H         | R/W |
| PU4    | 0                                                                                    | 0     | 0     | 0     | PU43  | PU42  | PU41  | PU40  | F0034H  | 01H         | R/W |
| PU5    | 0                                                                                    | 0     | 0     | PU54  | PU53  | PU52  | PU51  | PU50  | F0035H  | 00H         | R/W |
| PU7    | 0                                                                                    | 0     | 0     | PU74  | PU73  | PU72  | PU71  | PU70  | F0037H  | 00H         | R/W |
| PU12   | PU127                                                                                | PU126 | PU125 | 0     | 0     | 0     | 0     | PU120 | F003CH  | 00H         | R/W |
| PU14   | PU147                                                                                | PU146 | PU145 | PU144 | PU143 | PU142 | PU141 | PU140 | F003EH  | 00H         | R/W |
| PUMn   | Pmn pin on-chip pull-up resistor selection<br>(m = 1, 3 to 5, 7, 12, 14; n = 0 to 7) |       |       |       |       |       |       |       |         |             |     |
| 0      | On-chip pull-up resistor not connected                                               |       |       |       |       |       |       |       |         |             |     |
| 1      | On-chip pull-up resistor connected                                                   |       |       |       |       |       |       |       |         |             |     |

**Caution** For the pins used as LCD function pins ( $SEG_{xx}$ ,  $CAPL$ ,  $CAPH$ , and  $V_{L3}$ ), be sure to clear the corresponding  $PUM_n$  bit of the  $PUM$  register to 0.

#### 4.3.4 Port input mode register (PIM1)

These registers set the input buffer in 1-bit units.

TTL input buffer can be selected during serial communication, etc with an external device of the different potential.

Port input mode registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

**Figure 4-4. Format of Port Input Mode Register (64-pin products)**

| Symbol | 7 | 6     | 5     | 4 | 3 | 2 | 1     | 0     | Address | After reset | R/W |
|--------|---|-------|-------|---|---|---|-------|-------|---------|-------------|-----|
| PIM1   | 0 | PIM16 | PIM15 | 0 | 0 | 0 | PIM11 | PIM10 | F0041H  | 00H         | R/W |

| PIM1n | P1n pin input buffer selection<br>(n = 0, 1, 5, 6) |
|-------|----------------------------------------------------|
| 0     | Normal input buffer                                |
| 1     | TTL input buffer                                   |

**Caution** When using P10/SCK00/SEG28, P11/SI00/RxD0/TOOLRxD/SEG29, P15/SCK01/INTP1/SEG4, and P16/SI01/INTP2/SEG5 as LCD controller/driver function pins (segment output pins), setting the PIM1n bit to 1 is prohibited.

#### 4.3.5 Port output mode register (POM1)

This register set the output mode of P10, P12, P15, P17 in 1-bit units.

N-ch open drain output ( $V_{DD}$  tolerance<sup>Note 1</sup>/EV<sub>DD</sub> tolerance<sup>Note 2</sup>) mode can be selected during serial communication with an external device of the different potential.

In addition, POMxx register is set with PUxx register, whether or not to use the on-chip pull-up resistor.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 4-5. Format of Port Input Mode Register (64-pin products)**

| Symbol | 7     | 6 | 5     | 4 | 3 | 2     | 1 | 0     | Address | After reset | R/W |
|--------|-------|---|-------|---|---|-------|---|-------|---------|-------------|-----|
| POM1   | POM17 | 0 | POM15 | 0 | 0 | POM12 | 0 | POM10 | F0051H  | 00H         | R/W |

| POM1n | Pmn pin output mode selection (n = 0, 2, 5, 7)                                                                                                                 |
|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | Normal output mode<br>When input mode, enable to the PUMn bit                                                                                                  |
| 1     | N-ch open-drain output ( $V_{DD}$ tolerance <sup>Note 1</sup> /EV <sub>DD</sub> tolerance <sup>Note 2</sup> ) mode<br>When input mode, disable to the PUMn bit |

**Notes 1.** 32, 44, 48, 52-pin products :  $V_{DD}$  tolerance

**2.** 64-pin products : EV<sub>DD</sub> tolerance

#### 4.3.6 Port mode control registers (PMC1, PMC4, PMC12, PMC14)

These registers set the P13, P14, P41, P120, and P142 to P145 digital I/O/analog input in 1-bit units.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to FFH.

**Figure 4-6. Format of Port Mode Control Register (64-pin products)**

| Symbol | 7                                                                            | 6 | 5      | 4      | 3      | 2      | 1     | 0      | Address | After reset | R/W |
|--------|------------------------------------------------------------------------------|---|--------|--------|--------|--------|-------|--------|---------|-------------|-----|
| PMC1   | 1                                                                            | 1 | 1      | PMC14  | PMC13  | 1      | 1     | 1      | F0061H  | FFH         | R/W |
| PMC4   | 1                                                                            | 1 | 1      | 1      | 1      | 1      | PMC41 | 1      | F0064H  | FFH         | R/W |
| PMC12  | 1                                                                            | 1 | 1      | 1      | 1      | 1      | 1     | PMC120 | F006CH  | FFH         | R/W |
| PMC14  | 1                                                                            | 1 | PMC145 | PMC144 | PMC143 | PMC142 | 1     | 1      | F006EH  | FFH         | R/W |
| PMCMn  | Pmn pin digital I/O/analog input selection<br>(m = 1, 4, 12, 14; n = 0 to 5) |   |        |        |        |        |       |        |         |             |     |
| 0      | Digital I/O (alternate function other than analog input)                     |   |        |        |        |        |       |        |         |             |     |
| 1      | Analog input                                                                 |   |        |        |        |        |       |        |         |             |     |

- <R> **Cautions 1. Set the channel used for A/D conversion to the input mode by using port mode registers 1, 4, 12, 14 (PM1, PM4, PM12, PM14).**
- <R> **2. Do not set the pin set by the PMC register as digital I/O by the analog input channel specification register (ADS).**

### 4.3.7 A/D port configuration register (ADPC)

This register switches the P20/ANI0, P21/AN21 pins to digital I/O of port or analog input of A/D converter.

The ADPC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

**Figure 4-7. Format of A/D Port Configuration Register (ADPC)**

Address: F0076H After reset: 00H R/W

|        |   |   |   |   |   |   |       |       |
|--------|---|---|---|---|---|---|-------|-------|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0     |
| ADPC   | 0 | 0 | 0 | 0 | 0 | 0 | ADPC1 | ADPC0 |

| ADPC1 | ADPC0 | Analog input (A)/digital I/O (D) switching |          |
|-------|-------|--------------------------------------------|----------|
|       |       | ANI1/P21                                   | ANI0/P20 |
| 0     | 0     | A                                          | A        |
| 0     | 1     | D                                          | D        |
| 1     | 0     | D                                          | A        |
| 1     | 1     | A                                          | A        |

- Cautions**
1. Set the port to analog input by ADPC register to the input mode by using port mode registers 2 (PM2).
  2. Do not set the pin set by the ADPC register as digital I/O by the analog input channel specification register (ADS).

### 4.3.8 Peripheral I/O redirection register (PIOR)

This register is used to specify whether to enable or disable the peripheral I/O redirect function.

This function is used to switch ports to which alternate functions are assigned.

<R> Use the PIOR register to assign a port to the function to redirect and enable the function.

In addition, can be changed the settings for redirection until its function enable operation.

The PIOR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

**Figure 4-8. Format of Peripheral I/O Redirection Register (PIOR)**

Address: F0077H After reset: 00H R/W

|        |   |   |   |   |   |   |       |       |
|--------|---|---|---|---|---|---|-------|-------|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0     |
| PIOR   | 0 | 0 | 0 | 0 | 0 | 0 | PIOR1 | PIOR0 |

| Bit   | Function  | 64-pin        |      | 52-pin        |     | 48-pin        |     | 44-pin                                                    |     | 32-pin        |     |
|-------|-----------|---------------|------|---------------|-----|---------------|-----|-----------------------------------------------------------|-----|---------------|-----|
|       |           | Setting value |      | Setting value |     | Setting value |     | Setting value                                             |     | Setting value |     |
|       |           | 0             | 1    | 0             | 1   | 0             | 1   | 0                                                         | 1   | 0             | 1   |
| PIOR1 | PCLBUZ0   | P140          | P50  | P140          | P50 | P140          | P50 | This area cannot be used.<br>Be set to 0 (default value). |     |               |     |
| PIOR0 | INTP1     | P15           | P53  | P15           | P10 | P15           | P10 | P15                                                       | P10 | P15           | P10 |
|       | INTP2     | P16           | P54  | P16           | P11 | P16           | P11 | P16                                                       | P11 | P16           | P11 |
|       | INTP6     | P52           | P140 | —             | —   | —             | —   | —                                                         | —   | —             | —   |
|       | INTP7     | P43           | P141 | —             | —   | —             | —   | —                                                         | —   | —             | —   |
|       | TI02/TO02 | P17           | P54  | P17           | P12 | P17           | P12 | P17                                                       | P12 | P17           | P12 |



### 4.3.9 LCD port function registers 0 to 4 (PFSEG0 to PFSEG4)

These registers set whether to use pins P10 to P17, P30 to P32, P41 to P43, P50 to P54, P60, P61, P70 to P74, P120, and P140 to P147 as port pins (other than segment output pins) or segment output pins.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH (PFSEG0 is set to F0H, and PFSEG4 is set to 7FH).

**Remark** The correspondence between the segment output pins (SEGxx) and the PFSEG register (PFSEGxx bits) and the existence of SEGxx pins in each product are shown in Table 4-3 Segment Output Pins in Each Product and Correspondence with PFSEG Register (PFSEG Bits).

**Figure 4-9. Format of LCD port function registers 0 to 4 (PFSEG0 to PFSEG4) (64-pin products)**

Address: F0300H After reset: F0H R/W

|        |         |         |         |         |   |   |   |   |
|--------|---------|---------|---------|---------|---|---|---|---|
| Symbol | 7       | 6       | 5       | 4       | 3 | 2 | 1 | 0 |
| PFSEG0 | PFSEG07 | PFSEG06 | PFSEG05 | PFSEG04 | 0 | 0 | 0 | 0 |

Address: F0301H After reset: FFH R/W

|        |         |         |         |         |         |         |         |         |
|--------|---------|---------|---------|---------|---------|---------|---------|---------|
| Symbol | 7       | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
| PFSEG1 | PFSEG15 | PFSEG14 | PFSEG13 | PFSEG12 | PFSEG11 | PFSEG10 | PFSEG09 | PFSEG08 |

Address: F0302H After reset: FFH R/W

|        |         |         |         |         |         |         |         |         |
|--------|---------|---------|---------|---------|---------|---------|---------|---------|
| Symbol | 7       | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
| PFSEG2 | PFSEG23 | PFSEG22 | PFSEG21 | PFSEG20 | PFSEG19 | PFSEG18 | PFSEG17 | PFSEG16 |

Address: F0303H After reset: FFH R/W

|        |         |         |         |         |         |         |         |         |
|--------|---------|---------|---------|---------|---------|---------|---------|---------|
| Symbol | 7       | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
| PFSEG3 | PFSEG31 | PFSEG30 | PFSEG29 | PFSEG28 | PFSEG27 | PFSEG26 | PFSEG25 | PFSEG24 |

Address: F0304H After reset: 7FH R/W

|        |   |         |         |         |         |         |         |         |
|--------|---|---------|---------|---------|---------|---------|---------|---------|
| Symbol | 7 | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
| PFSEG4 | 0 | PFSEG38 | PFSEG37 | PFSEG36 | PFSEG35 | PFSEG34 | PFSEG33 | PFSEG32 |

|                               |                                                                                                                                                             |
|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PFSEGxx<br>(xx = 04<br>to 38) | Port (other than segment output)/segment outputs specification of Pmn pins<br>(mn = 10 to 17, 30 to 32, 41 to 43, 50 to 54, 60, 61, 70-74, 120, 140 to 147) |
| 0                             | Used the Pmn pin as port (other than segment output)                                                                                                        |
| 1                             | Used the Pmn pin as segment output                                                                                                                          |

**Table 4-3. Segment Output Pins in Each Product and Correspondence with PFSEG Register (PFSEG Bits)**

| Bit name of PFSEG register | Corresponding SEGxx pins | Alternate port | 64-pin | 52-pin | 48-pin | 44-pin | 32-pin |
|----------------------------|--------------------------|----------------|--------|--------|--------|--------|--------|
| PFSEG04                    | SEG4                     | P15            | √      | √      | √      | √      | √      |
| PFSEG05                    | SEG5                     | P16            | √      | √      | √      | √      | √      |
| PFSEG06                    | SEG6                     | P17            | √      | √      | √      | √      | √      |
| PFSEG07                    | SEG7                     | P50            | √      | √      | √      | –      | –      |
| PFSEG08                    | SEG8                     | P51            | √      | √      | –      | –      | –      |
| PFSEG09                    | SEG9                     | P52            | √      | –      | –      | –      | –      |
| PFSEG10                    | SEG10                    | P53            | √      | –      | –      | –      | –      |
| PFSEG11                    | SEG11                    | P54            | √      | –      | –      | –      | –      |
| PFSEG12                    | SEG12                    | P74            | √      | –      | –      | –      | –      |
| PFSEG13                    | SEG13                    | P73            | √      | –      | –      | –      | –      |
| PFSEG14                    | SEG14                    | P72            | √      | –      | –      | –      | –      |
| PFSEG15                    | SEG15                    | P71            | √      | √      | –      | –      | –      |
| PFSEG16                    | SEG16                    | P70            | √      | √      | √      | –      | –      |
| PFSEG17                    | SEG17                    | P32            | √      | √      | √      | √      | –      |
| PFSEG18                    | SEG18                    | P31            | √      | √      | √      | √      | –      |
| PFSEG19                    | SEG19                    | P30            | √      | √      | √      | √      | √      |
| PFSEG20                    | SEG20                    | P61            | √      | √      | √      | √      | √      |
| PFSEG21                    | SEG21                    | P60            | √      | √      | √      | √      | √      |
| PFSEG22                    | SEG22                    | P43            | √      | –      | –      | –      | –      |
| PFSEG23                    | SEG23                    | P42            | √      | √      | –      | –      | –      |
| PFSEG24                    | SEG24                    | P41            | √      | √      | √      | –      | –      |
| PFSEG25                    | SEG25                    | P120           | √      | √      | √      | √      | –      |
| PFSEG26                    | SEG26                    | P141           | √      | √      | √      | √      | –      |
| PFSEG27                    | SEG27                    | P140           | √      | √      | √      | √      | √      |
| PFSEG28                    | SEG28                    | P10            | √      | √      | √      | √      | √      |
| PFSEG29                    | SEG29                    | P11            | √      | √      | √      | √      | √      |
| PFSEG30                    | SEG30                    | P12            | √      | √      | √      | √      | √      |
| PFSEG31                    | SEG31                    | P13            | √      | √      | √      | √      | √      |
| PFSEG32                    | SEG32                    | P14            | √      | √      | √      | √      | √      |
| PFSEG33                    | SEG33                    | P142           | √      | √      | √      | √      | –      |
| PFSEG34                    | SEG34                    | P143           | √      | √      | √      | √      | –      |
| PFSEG35                    | SEG35                    | P144           | √      | √      | √      | –      | –      |
| PFSEG36                    | SEG36                    | P145           | √      | √      | –      | –      | –      |
| PFSEG37                    | SEG37                    | P146           | √      | –      | –      | –      | –      |
| PFSEG38                    | SEG38                    | P147           | √      | –      | –      | –      | –      |

**Remark** √: Supported, –: Not supported

#### 4.3.10 LCD input switch control register (ISCLCD)

The CAPL/P126, CAPH/P127, and VL3/P125 pins are internally connected with a Schmitt trigger buffer. To use these pins as LCD function, input to the Schmitt trigger buffer must be disabled, in order to prevent through-currents from entering.

The ISCLCD register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to 00H.

**Figure 4-10. Format of LCD input switch control register (ISCLCD)**

Address: F0308H After reset: 00H R/W

|        |   |   |   |   |   |   |        |        |
|--------|---|---|---|---|---|---|--------|--------|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1      | 0      |
| ISCLCD | 0 | 0 | 0 | 0 | 0 | 0 | ISCVL3 | ISCCAP |

|        |                                                   |
|--------|---------------------------------------------------|
| ISCVL3 | Control of schmitt trigger buffer of VL3/P125 pin |
| 0      | Makes digital input ineffective                   |
| 1      | Makes digital input effective                     |

|        |                                                                    |
|--------|--------------------------------------------------------------------|
| ISCCAP | Control of schmitt trigger buffer of CAPL/ P126 and CAPH/P127 pins |
| 0      | Makes digital input ineffective                                    |
| 1      | Makes digital input effective                                      |

- Cautions**
1. If ISCVL3 bit = 0, set the corresponding port control registers as follows:  
 PU125 bit of PU12 register = 0, P125 bit of P12 register = 0
  2. If ISCCAP bit = 0, set the corresponding port control registers as follows:  
 PU127 bit of PU12 register = 0, P127 bit of P12 register = 0  
 PU126 bit of PU12 register = 0, P126 bit of P12 register = 0

## 4.4 Port Function Operations

Port operations differ depending on whether the input or output mode is set, as shown below.

### 4.4.1 Writing to I/O port

#### (1) Output mode

A value is written to the output latch by a transfer instruction, and the output latch contents are output from the pin.

Once data is written to the output latch, it is retained until data is written to the output latch again.

The data of the output latch is cleared when a reset signal is generated.

#### (2) Input mode

<R> A value is written to the output latch by a transfer instruction, but since the output buffer is off, the pin status does not change. Therefore, byte data can be written to the ports used for both input and output.

Once data is written to the output latch, it is retained until data is written to the output latch again.

The data of the output latch is cleared when a reset signal is generated.

### 4.4.2 Reading from I/O port

#### (1) Output mode

The output latch contents are read by a transfer instruction. The output latch contents do not change.

#### (2) Input mode

The pin status is read by a transfer instruction. The output latch contents do not change.

### 4.4.3 Operations on I/O port

#### (1) Output mode

An operation is performed on the output latch contents, and the result is written to the output latch. The output latch contents are output from the pins.

Once data is written to the output latch, it is retained until data is written to the output latch again.

The data of the output latch is cleared when a reset signal is generated.

#### (2) Input mode

<R> The pin level is read and an operation is performed on its contents. The result of the operation is written to the output latch, but since the output buffer is off, the pin status does not change. Therefore, byte data can be written to the ports used for both input and output.

The data of the output latch is cleared when a reset signal is generated.

#### 4.4.4 Connecting to external device with different potential (1.8 V, 2.5 V, 3 V)

<R> It is possible to connect to an external device with a different potential (1.8 V, 2.5 V or 3 V) by changing EV<sub>DD</sub> to accord with the power supply of the connected device. In products in which EV<sub>DD</sub> cannot be specified independently, I/O connection with an external device operating on 1.8 V, 2.5 V or 3 V is still possible via the serial interface and general-purpose port by using port 1.

| External Device | EV <sub>DD</sub>                                                                   | No EV <sub>DD</sub>                                        |
|-----------------|------------------------------------------------------------------------------------|------------------------------------------------------------|
| 3 V             | $4.0\text{ V} \leq \text{EV}_{\text{DD}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ | $4.0\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ |
| 2.5 V           | $3.3\text{ V} \leq \text{EV}_{\text{DD}} = \text{V}_{\text{DD}} < 4.0\text{ V}$    | $3.3\text{ V} \leq \text{V}_{\text{DD}} \leq 4.0\text{ V}$ |
| 1.8 V           | $1.8\text{ V} \leq \text{EV}_{\text{DD}} = \text{V}_{\text{DD}} < 3.3\text{ V}$    | $1.8\text{ V} \leq \text{V}_{\text{DD}} \leq 3.3\text{ V}$ |

Regarding inputs, Normal (CMOS)/TTL input buffer switching is possible on a bit-by-bit basis by the port input mode register (PIM1).

Moreover, regarding outputs, different potentials can be supported by switching the output buffer to the N-ch open drain ( $\text{V}_{\text{DD}}$  tolerance<sup>Note 1</sup>/EV<sub>DD</sub> tolerance<sup>Note 2</sup>) by the port output mode register (POM1).

Following, describes the connection of a serial interface.

- Notes**
- 32, 44, 48, 52-pin products : V<sub>DD</sub> tolerance
  - 64-pin products : EV<sub>DD</sub> tolerance

#### (1) Setting procedure when using I/O pins of UART0, CSI00, and CSI01 functions

##### (a) Use as 1.8 V, 2.5 V, 3 V input port

<1> If pull-up is needed, externally pull up the pin to be used up to the power supply of the target device (on-chip pull-up resistor cannot be used).

In case of UART0: P11

In case of CSI00: P10, P11

In case of CSI01: P15, P16

<2> After reset release, the port mode is the input mode (Hi-Z).

<3> Set the corresponding bit of the PIM1 register to 1 to switch to the TTL input buffer.

<4> V<sub>IH</sub>/V<sub>IL</sub> operates on 1.8 V, 2.5 V, 3 V operating voltage.

**(b) Use as 1.8 V, 2.5 V, 3 V output port**

<1> Pull up externally the pin to be used to the power supply of the target device (on-chip pull-up resistor cannot be used).

In case of UART0: P12

In case of CSI00: P10, P12

In case of CSI01: P15, P17

<2> After reset release, the port mode changes to the input mode (Hi-Z).

<3> Set the output latch of the corresponding port to 1.

<4> Set the corresponding bit of the POM1 register to 1 to set the N-ch open drain output ( $V_{DD}$  tolerance<sup>Note 1</sup>/EV<sub>DD</sub> tolerance<sup>Note 2</sup>) mode.

<5> Set the output mode by manipulating the PM1 register.

At this time, the output data is high level, so the pin is in the Hi-Z state.

<6> Can be communication by setting the serial array unit.

**Notes** 1. 32, 44, 48, 52-pin products :  $V_{DD}$  tolerance

2. 64-pin products : EV<sub>DD</sub> tolerance

## 4.5 Settings of Port Related Register When Using Alternate Function

To use the alternate function of a port pin, set the port mode register, and output latch as shown in Table 4-4.

<R> **Caution** If the output function of an alternate function is assigned to a pin that is also used as an output pin, the output of the unused alternate function must be set to its initial state. See 4.6.2 for details about the applicable units and how to handle such pins.

**Table 4-4. Settings of Port Related Register When Using Alternate Function (1/4)**

| Pin Name | Alternate Function      |        | PIORx | PFSEGxx     | POMxx | PMCxx | PMxx | Pxx |
|----------|-------------------------|--------|-------|-------------|-------|-------|------|-----|
|          | Function Name           | I/O    |       |             |       |       |      |     |
| P10      | SCK00                   | Input  | ×     | PFSEG28 = 0 | ×     | –     | 1    | ×   |
|          |                         | Output | ×     | PFSEG28 = 0 | 0/1   | –     | 0    | 1   |
|          | SEG28                   | Output | ×     | PFSEG28 = 1 | 0     | –     | 0    | 0   |
| P11      | SI00                    | Input  | ×     | PFSEG29 = 0 | –     | –     | 1    | ×   |
|          | RxD0                    | Input  | ×     | PFSEG29 = 0 | –     | –     | 1    | ×   |
|          | TOOLRxD                 | Input  | ×     | PFSEG29 = 0 | –     | –     | 1    | ×   |
|          | SEG29                   | Output | ×     | PFSEG29 = 1 | –     | –     | 0    | 0   |
| P12      | SO00                    | Output | ×     | PFSEG30 = 0 | 0/1   | –     | 0    | 1   |
|          | TxD0                    | Output | ×     | PFSEG30 = 0 | 0/1   | –     | 0    | 1   |
|          | TOOLTxD                 | Output | ×     | PFSEG30 = 0 | 0/1   | –     | 0    | 1   |
|          | SEG30                   | Output | ×     | PFSEG30 = 1 | 0     | –     | 0    | 0   |
| P13      | ANI18 <sup>Note 1</sup> | Input  | ×     | PFSEG31 = 1 | –     | 1     | 1    | ×   |
|          | SEG31                   | Output | ×     | PFSEG31 = 1 | –     | 0     | 0    | 0   |
| P14      | ANI19 <sup>Note 1</sup> | Input  | ×     | PFSEG32 = 1 | –     | 1     | 1    | ×   |
|          | SEG32                   | Output | ×     | PFSEG32 = 1 | –     | 0     | 0    | 0   |
| P15      | SCK01                   | Input  | ×     | PFSEG04 = 0 | ×     | –     | 1    | ×   |
|          |                         | Output | ×     | PFSEG04 = 0 | 0/1   | –     | 0    | 1   |
|          | INTP1                   | Input  | 0     | PFSEG04 = 0 | ×     | –     | 1    | ×   |
|          | SEG4                    | Output | ×     | PFSEG04 = 1 | 0     | –     | 0    | 0   |
| P16      | SI01                    | Input  | ×     | PFSEG05 = 0 | –     | –     | 1    | ×   |
|          | INTP2                   | Input  | 0     | PFSEG05 = 0 | –     | –     | 1    | ×   |
|          | SEG5                    | Output | ×     | PFSEG05 = 1 | –     | –     | 0    | 0   |

**Remarks 1.** ×: don't care

PIORx: Peripheral I/O redirection register

PFSEG: LCD port function register

POMxx: Port output mode register

PMCxx: Port mode control register

PMxx: Port mode register

Pxx: Port output latch

- The relationship between pins and their alternate functions shown in this table indicates the relationship when a 64-pin product is used. In other products, alternate functions might be assigned to different pins, but even in this case, the PIORx, PFSEGx, POMxx, PMCxx, PMxx, and Pxx settings remain the same.
- For details about ports that also serve as segment output pins (SEGxx) (P10 to P16), see **4.5.1 Operation of Ports That Alternately Function as SEGxx Pins.**

Table 4-4. Settings of Port Related Register When Using Alternate Function (2/4)

| Pin Name              | Alternate Function                   |        | PIORx | PFSEGxx     | POMxx | PMCxx | PMxx | Pxx |
|-----------------------|--------------------------------------|--------|-------|-------------|-------|-------|------|-----|
|                       | Function Name                        | I/O    |       |             |       |       |      |     |
| P17                   | SO01                                 | Output | ×     | PFSEG06 = 0 | 0/1   | –     | 0    | 1   |
|                       | TI02                                 | Input  | 0     | PFSEG06 = 0 | ×     | –     | 1    | ×   |
|                       | TO02                                 | Output | 0     | PFSEG06 = 0 | 0/1   | –     | 0    | 0   |
|                       | SEG6                                 | Output | ×     | PFSEG06 = 1 | 0     | –     | 0    | 0   |
| P20 <sup>Note 2</sup> | ANI0 <sup>Note 2</sup>               | Input  | ×     | –           | –     | –     | 1    | ×   |
|                       | AV <sub>REFP</sub> <sup>Note 2</sup> | Input  | ×     | –           | –     | –     | 1    | ×   |
| P21 <sup>Note 2</sup> | ANI1 <sup>Note 2</sup>               | Input  | ×     | –           | –     | –     | 1    | ×   |
|                       | AV <sub>REFM</sub> <sup>Note 2</sup> | Input  | ×     | –           | –     | –     | 1    | ×   |
| P30                   | TI01                                 | Input  | ×     | PFSEG19 = 0 | –     | –     | 1    | ×   |
|                       | TO01                                 | Output | ×     | PFSEG19 = 0 | –     | –     | 0    | 0   |
|                       | SEG19                                | Output | ×     | PFSEG19 = 1 | –     | –     | 0    | 0   |
| P31                   | INTP3                                | Input  | ×     | PFSEG18 = 0 | –     | –     | 1    | ×   |
|                       | RTC1HZ                               | Output | ×     | PFSEG18 = 0 | –     | –     | 0    | 0   |
|                       | SEG18                                | Output | ×     | PFSEG18 = 1 | –     | –     | 0    | 0   |
| P32                   | TI03                                 | Input  | ×     | PFSEG17 = 0 | –     | –     | 1    | ×   |
|                       | TO03                                 | Output | ×     | PFSEG17 = 0 | –     | –     | 0    | 0   |
|                       | INTP4                                | Input  | ×     | PFSEG17 = 0 | –     | –     | 1    | ×   |
|                       | SEG17                                | Output | ×     | PFSEG17 = 1 | –     | –     | 0    | 0   |
| P40                   | TOOL0                                | I/O    | ×     | –           | –     | –     | ×    | ×   |
| P41                   | ANI16 <sup>Note 1</sup>              | Input  | ×     | PFSEG24 = 1 | –     | 1     | 1    | ×   |
|                       | TI04                                 | Input  | ×     | PFSEG24 = 0 | –     | 0     | 1    | ×   |
|                       | TO04                                 | Output | ×     | PFSEG24 = 0 | –     | 0     | 0    | 0   |
|                       | SEG24                                | Output | ×     | PFSEG24 = 1 | –     | 0     | 0    | 0   |
| P42                   | TI05                                 | Input  | ×     | PFSEG23 = 0 | –     | –     | 1    | ×   |
|                       | TO05                                 | Output | ×     | PFSEG23 = 0 | –     | –     | 0    | 0   |
|                       | SEG23                                | Output | ×     | PFSEG23 = 1 | –     | –     | 0    | 0   |
| P43                   | INTP7                                | Input  | 0     | PFSEG22 = 0 | –     | –     | 1    | ×   |
|                       | SEG22                                | Output | ×     | PFSEG22 = 1 | –     | –     | 0    | 0   |

Remarks 1. ×: don't care

PIORx: Peripheral I/O redirection register

PFSEG: LCD port function register

POMxx: Port output mode register

PMCxx: Port mode control register

PMxx: Port mode register

Pxx: Port output latch

- The relationship between pins and their alternate functions shown in this table indicates the relationship when a 64-pin product is used. In other products, alternate functions might be assigned to different pins, but even in this case, the PIORx, PFSEGx, POMxx, PMCxx, PMxx, and Pxx settings remain the same.
- For details about ports that also serve as segment output pins (SEGxx) (P17, P30 to P32, P41 to P43), see 4.5.1 Operation of Ports That Alternately Function as SEGxx Pins.

(The notes are described after the last table.)



Table 4-4. Settings of Port Related Register When Using Alternate Function (3/4)

| Pin Name | Alternate Function |        | PIORx | PFSEGxx     | POMxx | PMCxx | PMxx | Pxx |
|----------|--------------------|--------|-------|-------------|-------|-------|------|-----|
|          | Function Name      | I/O    |       |             |       |       |      |     |
| P50      | INTP5              | Input  | ×     | PFSEG07 = 0 | –     | –     | 1    | ×   |
|          | SEG7               | Output | ×     | PFSEG07 = 1 | –     | –     | 0    | 0   |
|          | (PCLBUZ0)          | Output | 1     | PFSEG07 = 0 | –     | –     | 0    | 0   |
| P51      | TI06               | Input  | ×     | PFSEG08 = 0 | –     | –     | 1    | ×   |
|          | TO06               | Output | ×     | PFSEG08 = 0 | –     | –     | 0    | 0   |
|          | SEG8               | Output | ×     | PFSEG08 = 1 | –     | –     | 0    | 0   |
| P52      | INTP6              | Input  | 0     | PFSEG09 = 0 | –     | –     | 1    | ×   |
|          | SEG9               | Output | ×     | PFSEG09 = 1 | –     | –     | 0    | 0   |
| P53      | TI07               | Input  | ×     | PFSEG10 = 0 | –     | –     | 1    | ×   |
|          | TO07               | Output | ×     | PFSEG10 = 0 | –     | –     | 0    | 0   |
|          | SEG10              | Output | ×     | PFSEG10 = 1 | –     | –     | 0    | 0   |
|          | (INTP1)            | Input  | 1     | PFSEG10 = 0 | –     | –     | 1    | ×   |
| P54      | SEG11              | Output | ×     | PFSEG11 = 1 | –     | –     | 0    | 0   |
|          | (TI02)             | Input  | 1     | PFSEG11 = 0 | –     | –     | 1    | ×   |
|          | (TO02)             | Output | 1     | PFSEG11 = 0 | –     | –     | 0    | 0   |
|          | (INTP2)            | Input  | 1     | PFSEG11 = 0 | –     | –     | 1    | ×   |
| P60      | SCLA0              | I/O    | ×     | PFSEG21 = 0 | –     | –     | 0    | 0   |
|          | SEG21              | Output | ×     | PFSEG21 = 1 | –     | –     | 0    | 0   |
| P61      | SDAA0              | I/O    | ×     | PFSEG20 = 0 | –     | –     | 0    | 0   |
|          | SEG20              | Output | ×     | PFSEG20 = 1 | –     | –     | 0    | 0   |
| P70      | KR0                | Input  | ×     | PFSEG16 = 0 | –     | –     | 1    | ×   |
|          | SEG16              | Output | ×     | PFSEG16 = 1 | –     | –     | 0    | 0   |
| P71      | KR1                | Input  | ×     | PFSEG15 = 0 | –     | –     | 1    | ×   |
|          | SEG15              | Output | ×     | PFSEG15 = 1 | –     | –     | 0    | 0   |
| P72      | KR2                | Input  | ×     | PFSEG14 = 0 | –     | –     | 1    | ×   |
|          | SEG14              | Output | ×     | PFSEG14 = 1 | –     | –     | 0    | 0   |
| P73      | KR3                | Input  | ×     | PFSEG13 = 0 | –     | –     | 1    | ×   |
|          | SEG13              | Output | ×     | PFSEG13 = 1 | –     | –     | 0    | 0   |
| P74      | SEG12              | Output | ×     | PFSEG12 = 1 | –     | –     | 0    | 0   |

Remarks 1. ×: don't care

PIORx: Peripheral I/O redirection register

PFSEG: LCD port function register

POMxx: Port output mode register

PMCxx: Port mode control register

PMxx: Port mode register

Pxx: Port output latch

- The relationship between pins and their alternate functions shown in this table indicates the relationship when a 64-pin product is used. In other products, alternate functions might be assigned to different pins, but even in this case, the PIORx, PFSEGx, POMxx, PMCxx, PMxx, and Pxx settings remain the same.
- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).
- For details about ports that also serve as segment output pins (SEGxx) (P50 to P54, P60, P61, P70 to P74), see 4.5.1 **Operation of Ports That Alternately Function as SEGxx Pins**.

(The notes are described after the last table.)

**Table 4-4. Settings of Port Related Register When Using Alternate Function (4/4)**

| Pin Name | Alternate Function      |        | PIORx | PFSEGxx     | POMxx | PMCxx | PMxx | Pxx | ISCLCD |
|----------|-------------------------|--------|-------|-------------|-------|-------|------|-----|--------|
|          | Function Name           | I/O    |       |             |       |       |      |     |        |
| P120     | ANI17 <sup>Note 1</sup> | Input  | ×     | PFSEG25 = 1 | –     | 1     | 1    | ×   | –      |
|          | SEG25                   | Output | ×     | PFSEG25 = 1 | –     | 0     | 0    | 0   | –      |
| P125     | V <sub>L3</sub>         | I/O    | ×     | –           | –     | –     | 1    | 0   | 0      |
| P126     | CAPL                    | Output | ×     | –           | –     | –     | 1    | 0   | 0      |
| P127     | CAPH                    | Output | ×     | –           | –     | –     | 1    | 0   | 0      |
| P137     | INTP0                   | Input  | ×     | –           | –     | –     | –    | –   | –      |
| P140     | TO00                    | Output | ×     | PFSEG27 = 0 | –     | –     | 0    | 0   | –      |
|          | PCLBUZ0                 | Output | 0     | PFSEG27 = 0 | –     | –     | 0    | 0   | –      |
|          | SEG27                   | Output | ×     | PFSEG27 = 1 | –     | –     | 0    | 0   | –      |
|          | (INTP6)                 | Input  | 1     | PFSEG27 = 0 | –     | –     | 1    | ×   | –      |
| P141     | TI00                    | Input  | ×     | PFSEG26 = 0 | –     | –     | 1    | ×   | –      |
|          | PCLBUZ1                 | Output | ×     | PFSEG26 = 0 | –     | –     | 0    | 0   | –      |
|          | SEG26                   | Output | ×     | PFSEG26 = 1 | –     | –     | 0    | 0   | –      |
|          | (INTP7)                 | Input  | 1     | PFSEG26 = 0 | –     | –     | 1    | ×   | –      |
| P142     | ANI20 <sup>Note 1</sup> | Input  | ×     | PFSEG33 = 1 | –     | 1     | 1    | ×   | –      |
|          | SEG33                   | Output | ×     | PFSEG33 = 1 | –     | 0     | 0    | 0   | –      |
| P143     | ANI21 <sup>Note 1</sup> | Input  | ×     | PFSEG34 = 1 | –     | 1     | 1    | ×   | –      |
|          | SEG34                   | Output | ×     | PFSEG34 = 1 | –     | 0     | 0    | 0   | –      |
| P144     | ANI22 <sup>Note 1</sup> | Input  | ×     | PFSEG35 = 1 | –     | 1     | 1    | ×   | –      |
|          | SEG35                   | Output | ×     | PFSEG35 = 1 | –     | 0     | 0    | 0   | –      |
| P145     | ANI23 <sup>Note 1</sup> | Input  | ×     | PFSEG36 = 1 | –     | 1     | 1    | ×   | –      |
|          | SEG36                   | Output | ×     | PFSEG36 = 1 | –     | 0     | 0    | 0   | –      |
| P146     | SEG37                   | Output | ×     | PFSEG37 = 1 | –     | –     | 0    | 0   | –      |
| P147     | SEG38                   | Output | ×     | PFSEG38 = 1 | –     | –     | 0    | 0   | –      |

**Remarks 1.** ×: don't care

PIORx: Peripheral I/O redirection register

PFSEG: LCD port function register

POMxx: Port output mode register

PMCxx: Port mode control register

PMxx: Port mode register

Pxx: Port output latch

ISCLCD: LCD Input switch control register

- The relationship between pins and their alternate functions shown in this table indicates the relationship when a 64-pin product is used. In other products, alternate functions might be assigned to different pins, but even in this case, the PIORx, PFSEGx, POMxx, PMCxx, PMxx, and Pxx settings remain the same.
- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).
- For details about ports that also serve as segment output pins (SEGxx) (P120, P140 to P147), see **4.5.1 Operation of Ports That Alternately Function as SEGxx Pins.**
- For details about ports that also serve as V<sub>L3</sub>, CAPL, and CAPH pins (P125 to P127), see **4.5.2 Operation of Ports That Alternately Function as V<sub>L3</sub>, CAPL, CAPH Pins.**

(The notes are described after the last table.)

- Notes** 1. The functions of the ANI16/P41, ANI17/P120, ANI18/P13, ANI19/P14, and ANI20/P142 to ANI23/P145 pins can be selected by using the port mode control registers 1, 4, 12, 14 (PMC1, PMC4, PMC12, PMC14), analog input channel specification register (ADS), and port mode registers 1, 4, 12, 14 (PM1, PM4, PM12, PM14).

**Table 4-5. Settings of ANI16/P41, ANI17/P120, ANI18/P13, ANI19/P14, and ANI20/P142 to ANI23/P145 Pins Function**

| PMC1, PMC4, PMC12, PMC14 Registers | PM1, PM4, PM12, PM14 Registers | ADS Register         | ANI16/P41, ANI17/P120, ANI18/P13, ANI19/P14, and ANI20/P142 to ANI23/P145 Pins |
|------------------------------------|--------------------------------|----------------------|--------------------------------------------------------------------------------|
| Digital I/O selection              | Input mode                     | ×                    | Digital input                                                                  |
|                                    | Output mode                    | ×                    | Digital output                                                                 |
| Analog input selection             | Input mode                     | Selects ANI.         | Analog input (to be converted)                                                 |
|                                    |                                | Does not select ANI. | Analog input (not to be converted)                                             |
|                                    | Output mode                    | Selects ANI.         | Setting prohibited                                                             |
|                                    |                                | Does not select ANI. |                                                                                |

2. The functions of the ANI0/P20 and ANI1/P21 pins can be selected by using the A/D port configuration register (ADPC), analog input channel specification register (ADS), and port mode register 2 (PM2).

**Table 4-6. Settings of ANI0/P20 and ANI1/P21 Pins Function**

| ADPC Register          | PM2 Register | ADS Register         | ANI0/P20 and ANI1/P21 Pins         |
|------------------------|--------------|----------------------|------------------------------------|
| Digital I/O selection  | Input mode   | ×                    | Digital input                      |
|                        | Output mode  | ×                    | Digital output                     |
| Analog input selection | Input mode   | Selects ANI.         | Analog input (to be converted)     |
|                        |              | Does not select ANI. | Analog input (not to be converted) |
|                        | Output mode  | Selects ANI.         | Setting prohibited                 |
|                        |              | Does not select ANI. |                                    |

#### 4.5.1 Operation of Ports That Alternately Function as SEGxx Pins

The functions of ports that also serve as segment output pins (SEGxx) can be selected by using the port mode control register (PMCxx), port mode register (PMxx), and LCD port function registers 0 to 4 (PFSEG0 to PFSEG4).

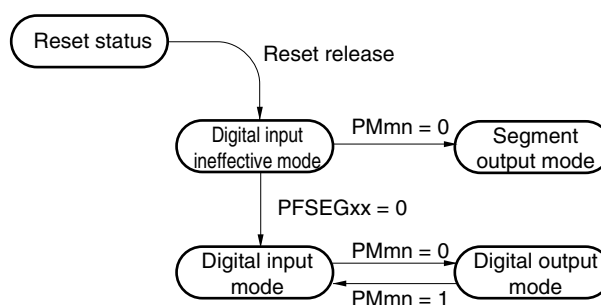
- (1) P10 to P12, P15 to P17, P30 to P32, P42, P43, P50 to P54, P60, P61, P70 to P74, P140, P141 (ports that do not serve as analog input pins (ANLxx))

**Table 4-7. Settings of SEGxx/Port Pin Function**

| PFSEGxx bit of<br>PFSEG0 to PFSEG4 registers | PMxx bit of<br>PMxx Register | Pin Function                   | Initial status |
|----------------------------------------------|------------------------------|--------------------------------|----------------|
| 1                                            | 1                            | Digital input ineffective mode | √              |
| 0                                            | 0                            | Digital output mode            | —              |
| 0                                            | 1                            | Digital input mode             | —              |
| 1                                            | 0                            | Segment output mode            | —              |

The following shows the SEGxx/port pin function status transitions.

**Figure 4-11. SEGxx/Port Pin Function Status Transition Diagram**



**Caution** Be sure to set the segment output mode before segment output starts (while SCOC of LCD mode register 1 (LCDM1) is 0).

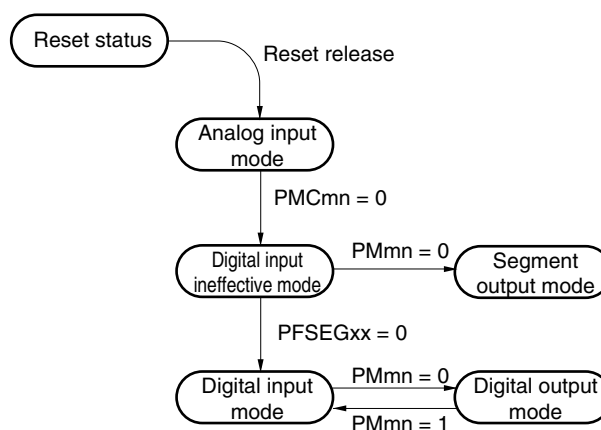
## (2) P13, P14, P41, P120, P142 to P147 (ports that serve as analog input pins (ANLxx))

Table 4-8. Settings of ANLxx/SEGxx/Port Pin Function

| PMCxx bit of<br>PMCxx register | PFSEGxx bit<br>PFSEG0 to PFSEG4 registers | PMxx bit of<br>PMxx Register | Pin Function                   | Initial status |
|--------------------------------|-------------------------------------------|------------------------------|--------------------------------|----------------|
| 1                              | 1                                         | 1                            | Analog input mode              | √              |
| 0                              | 0                                         | 0                            | Digital output mode            | —              |
| 0                              | 0                                         | 1                            | Digital input mode             | —              |
| 0                              | 1                                         | 0                            | Segment output mode            | —              |
| 0                              | 1                                         | 1                            | Digital input ineffective mode | —              |
| Other than above               |                                           |                              | Setting prohibited             |                |

The following shows the ANLxx/SEGxx/port pin function status transitions.

Figure 4-12. ANLxx/SEGxx/Port Pin Function Status Transition Diagram



**Caution** Be sure to set the segment output mode before segment output starts (while SCOC of LCD mode register 1 (LCDM1) is 0).

### 4.5.2 Operation of Ports That Alternately Function as $V_{L3}$ , CAPL, CAPH Pins

The functions of the  $V_{L3}$ /P125, CAPL/P126, CAPH/P127 pins can be selected by using the LCD input switch control register (ISCLCD), LCD mode register 0 (LCDM0), and port mode register 12 (PM12).

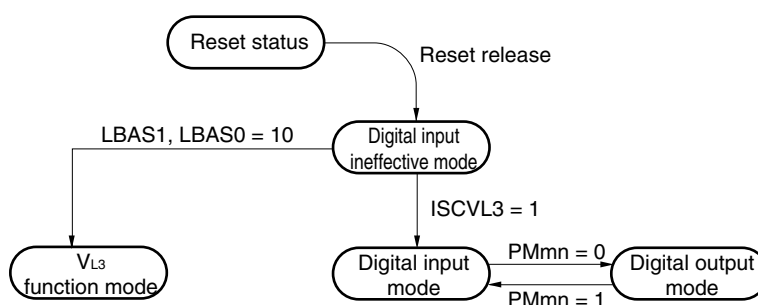
#### (1) $V_{L3}$ /P125

**Table 4-9. Settings of  $V_{L3}$ /P125 Pin Function**

| Bias Setting<br>(LBAS1 and LBAS0 bits of<br>LCDM0 Register ) | ISCVL3 bit of<br>ISCLCD Register | PM125 bit of<br>PM12 Register | Pin Function                   | Initial status |
|--------------------------------------------------------------|----------------------------------|-------------------------------|--------------------------------|----------------|
| other than 1/4 bias method<br>(LBAS1, LBAS0 = 00 or 01)      | 0                                | 1                             | Digital input ineffective mode | √              |
|                                                              | 1                                | 0                             | Digital output mode            | —              |
|                                                              | 1                                | 1                             | Digital input mode             | —              |
| 1/4 bias method<br>(LBAS1, LBAS0 = 10)                       | 0                                | 1                             | $V_{L3}$ function mode         | —              |
| Other than above                                             |                                  |                               | Setting prohibited             |                |

The following shows the  $V_{L3}$ /P125 pin function status transitions.

**Figure 4-13.  $V_{L3}$ /P125 Pin Function Status Transition Diagram**



**Caution** Be sure to set the  $V_{L3}$  function mode before segment output starts (while SCOC of LCD mode register 1 (LCDM1) is 0).

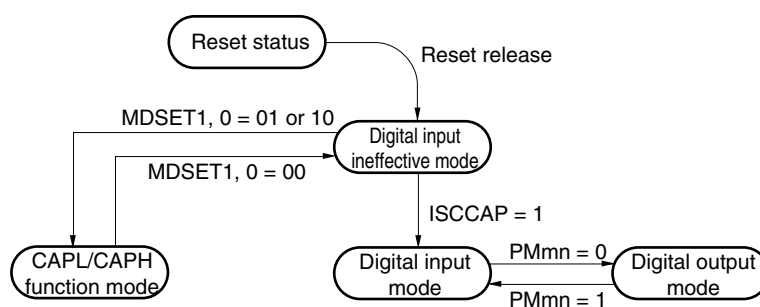
## (2) CAPL/P126, CAPH/P127

Table 4-10. Settings of CAPL/P126, CAPH/P127 Pins Function

| LCD drive voltage generator<br>(MDSET1 and MDSET0 bits<br>of LCDM0 Register )     | ISCCAP bit of<br>ISCLCD Register | PM126, PM127 bits<br>of PM12 Register | Pin Function                   | Initial status |
|-----------------------------------------------------------------------------------|----------------------------------|---------------------------------------|--------------------------------|----------------|
| External resistance division<br>(MDSET1, MDSET0 = 00)                             | 0                                | 1                                     | Digital input ineffective mode | √              |
|                                                                                   | 1                                | 0                                     | Digital output mode            | —              |
|                                                                                   | 1                                | 1                                     | Digital input mode             | —              |
| Internal voltage boosting or<br>capacitor split<br>(MDSET1, MDSET0 = 01 or<br>10) | 0                                | 1                                     | CAPL/CAPH function mode        | —              |
| Other than above                                                                  |                                  |                                       | Setting prohibited             |                |

The following shows the CAPL/P126 and CAPH/P127 pins function status transitions.

Figure 4-14. CAPL/P126 and CAPH/P127 Pins Function Status Transition Diagram



**Caution** Be sure to set the CAPL/CAPH function mode before segment output starts (while SCOC of LCD mode register 1 (LCDM1) is 0).

## 4.6 Cautions When Using Port Function

### 4.6.1 Cautions on 1-Bit Manipulation Instruction for Port Register n (Pn)

When a 1-bit manipulation instruction is executed on a port that provides both input and output functions, the output latch value of an input port that is not subject to manipulation may be written in addition to the targeted bit.

Therefore, it is recommended to rewrite the output latch when switching a port from input mode to output mode.

**<Example>** When P10 is an output port, P11 to P17 are input ports (all pin statuses are high level), and the port latch value of port 1 is 00H, if the output of output port P10 is changed from low level to high level via a 1-bit manipulation instruction, the output latch value of port 1 is FFH.

**Explanation:** The targets of writing to and reading from the Pn register of a port whose PMnm bit is 1 are the output latch and pin status, respectively.

A 1-bit manipulation instruction is executed in the following order in the RL78/L12.

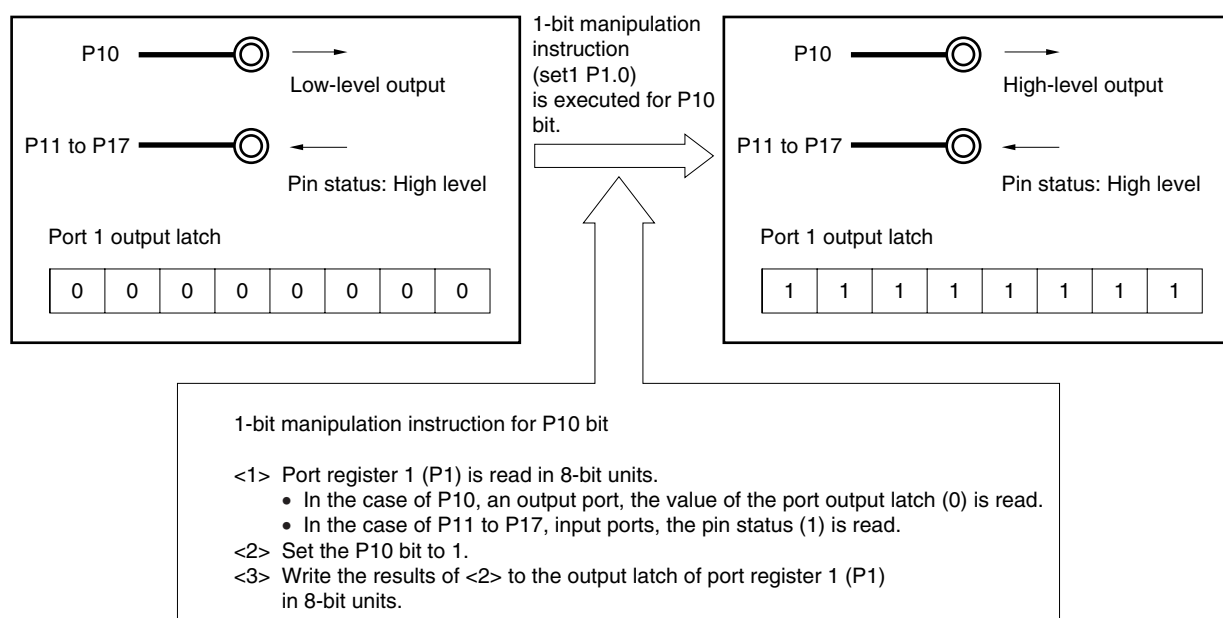
- <1> The Pn register is read in 8-bit units.
- <2> The targeted one bit is manipulated.
- <3> The Pn register is written in 8-bit units.

In step <1>, the output latch value (0) of P10, which is an output port, is read, while the pin statuses of P11 to P17, which are input ports, are read. If the pin statuses of P11 to P17 are high level at this time, the read value is FEH.

The value is changed to FFH by the manipulation in <2>.

FFH is written to the output latch by the manipulation in <3>.

**Figure 4-15. Bit Manipulation Instruction (P10)**





**<R> 4.6.2 Notes on specifying the pin settings**

If the output function of an alternate function is assigned to a pin that is also used as an output pin, the output of the unused alternate function must be set to its initial state so as to prevent conflicting outputs. This also applies to the functions assigned by using the peripheral I/O redirection register (PIOR). For details about the alternate output function, see **4.5 Settings of Port Related Register When Using Alternate Function**.

No specific setting is required for input pins because the output function of their alternate functions is disabled (the buffer output is Hi-Z).

**Table 4-11. Handling of Unused Alternate Functions**

| Affected Unit               | Output or I/O Pins of Unused Alternate Functions | Handling of Unused Alternate Functions                                                                                                                                                                                                                                                                                                                                |
|-----------------------------|--------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Timer array units           | TOmn                                             | Make sure that bit m (TOmn) of timer output register m (TOm) and bit n (TOEmn) of timer output enable register m (TOEm) are set to their initial value (0).                                                                                                                                                                                                           |
| Clock/buzzer output circuit | PCLBUZn                                          | Make sure that bit 7 (PCLOEn) of clock output select register n (CKSn) is set to its initial value (0).                                                                                                                                                                                                                                                               |
| Serial array units          | SOMn, TxDn                                       | Make sure that bit n (SEmn) of serial channel enable status register m (SEm), bit n (SOMn) of serial output register m (SOM), and bit n (SOEmn) of serial output enable register m (SOEm) are set to their initial value (1 for SOMn and 0 for others).                                                                                                               |
| LCD controller/driver       | SEGmn                                            | Make sure that LCD port function registers n (PFSEGN) are set to 0                                                                                                                                                                                                                                                                                                    |
|                             | CAPL, CAPH                                       | Make sure that bit 0 (ISCCAP) of LCD input switch control register (ISCLCD) is set to 1 and make sure that bits 7, 6 (MDSET1, MDSET0) of LCD mode register 0 (LCDM0) are set to 00.                                                                                                                                                                                   |
|                             | VL3                                              | Make sure that bit 1 (ISCVL3) of LCD input switch control register (ISCLCD) is set to 1 and make sure that bits 1, 0 (LBAS1, LBAS0) of LCD mode register 0 (LCDM0) are set to 00 or make sure that bit 1 (ISCVL3) of LCD input switch control register (ISCLCD) is set to 1 and make sure that bits 1, 0 (LBAS1, LBAS0) of LCD mode register 0 (LCDM0) are set to 01. |

Example: P17/SO01/TI02/TO02/SEG6 pin of 64-pin products

**(1) When the pin is used as SO01 output**

- P17: Specify the output mode by setting PM17 of port mode register 1 to 0.  
 TI02: This is input pins, so this note does not apply.  
 TO02: This is an output pin, so set TO02 and TOE02 of timer array unit 0 to 0.  
 SEG6: This is an output pin, so set PFSEG06 of LCD controller/driver to 0.

**(2) When the pin is used as TO02 output**

- P17: Specify the output mode by setting PM17 of port mode register 1 to 0.  
 SO01: This is an output pin, so set SE11, SO11, and SOE11 of serial array unit 1 to 0, 1, and 0, respectively.  
 TI02: This is input pins, so this note does not apply.  
 SEG6: This is an output pin, so set PFSEG06 of LCD controller/driver to 0.

Like TxD0 when using the P12/SO00/TxD0/TOOLTxD/SEG30 pin as the SO00 output pin, changing the operation mode does not enable alternate functions assigned to pins on the same serial channel, and this note does not apply to such pins. (If the CSI function is specified (MD001 = 0), the pin does not function as a UART pin, and therefore TxD0 output is invalid.)

Disabling the unused functions, including blocks that are only used for input or do not have I/O, is recommended to lower power consumption.

## CHAPTER 5 CLOCK GENERATOR

The presence or absence of connecting resonator pin for main system clock, connecting resonator pin for subsystem clock, external clock input pin for main system clock, and external clock input pin for subsystem clock, depends on the product.

| Output pin    | 32-pin | 44, 48, 52, 64-pin |
|---------------|--------|--------------------|
| X1, X2 pins   | √      | √                  |
| EXCLK pin     | √      | √                  |
| XT1, XT2 pins | –      | √                  |
| EXCLKS pin    | –      | √                  |

**Caution** The 32-pin products don't have the subsystem clock.

### 5.1 Functions of Clock Generator

The clock generator generates the clock to be supplied to the CPU and peripheral hardware.

The following three kinds of system clocks and clock oscillators are selectable.

#### (1) Main system clock

##### <1> X1 oscillator

This circuit oscillates a clock of  $f_x = 1$  to 20 MHz by connecting a resonator to X1 and X2.

Oscillation can be stopped by executing the STOP instruction or setting of the MSTOP bit (bit 7 of the clock operation status control register (CSC)).

##### <2> High-speed on-chip oscillator

The frequency at which to oscillate can be selected from among  $f_{IH} = 24, 16, 12, 8, 4$ , or 1 MHz (typ.) by using the option byte (000C2H). After a reset release, the CPU always starts operating with this high-speed on-chip oscillator clock. Oscillation can be stopped by executing the STOP instruction or setting the HIOSTOP bit (bit 0 of the CSC register).

<R> The frequency specified by using an option byte can be changed by using the high-speed on-chip oscillator frequency select register (HOCODIV). For details about the frequency, see Figure 5-9 Format of High-speed On-chip Oscillator Frequency Select Register (HOCODIV).

The frequencies that can be specified for the high-speed on-chip oscillator by using the option byte and the high-speed on-chip oscillator frequency select register (HOCODIV) are shown below.

| Power Supply Voltage                         | Oscillation Frequency (MHz) |   |   |   |   |   |    |    |    |
|----------------------------------------------|-----------------------------|---|---|---|---|---|----|----|----|
|                                              | 1                           | 2 | 3 | 4 | 6 | 8 | 12 | 16 | 24 |
| $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | √                           | √ | √ | √ | √ | √ | √  | √  | √  |
| $2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$    | √                           | √ | √ | √ | √ | √ | √  | √  | –  |
| $1.8\text{ V} \leq V_{DD} < 2.4\text{ V}$    | √                           | √ | √ | √ | √ | √ | –  | –  | –  |
| $1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$    | √                           | √ | – | √ | – | – | –  | –  | –  |

An external main system clock ( $f_{EX} = 1$  to 20 MHz) can also be supplied from the EXCLK/X2/P122 pin. An external main system clock input can be disabled by executing the STOP instruction or setting of the MSTOP bit.

As the main system clock, a high-speed system clock (X1 clock or external main system clock) or high-speed on-chip oscillator clock can be selected by setting of the MCM0 bit (bit 4 of the system clock control register (CKC)).

## (2) Subsystem clock

### • XT1 clock oscillator

This circuit oscillates a clock of  $f_{XT} = 32.768$  kHz by connecting a 32.768 kHz resonator to XT1 and XT2. Oscillation can be stopped by setting the XTSTOP bit (bit 6 of the clock operation status control register (CSC)).

An external subsystem clock ( $f_{EXS} = 32.768$  KHz) can also be supplied from the EXCLKS/XT2/P124 pin. An external subsystem clock input can be disabled by setting the XTSTOP bit.

## (3) Low-speed on-chip oscillator clock

This circuit oscillates a clock of  $f_{IL} = 15$  kHz (TYP.).

The low-speed on-chip oscillator clock cannot be used as the CPU clock.

Only the following peripheral hardware runs on the low-speed on-chip oscillator clock.

- Watchdog timer
- Real-time clock
- 12-bit interval timer
- LCD driver/controller

This clock operates when bit 4 (WDTON) of the option byte (000C0H), bit 4 (WUTMMCK0) of the operation speed mode control register (OSMC), or both are set to 1.

However, when WDTON = 1, WUTMMCK0 = 0, and bit 0 (WDSTBYON) of the option byte (000C0H) is 0, oscillation of the low-speed on-chip oscillator stops if the HALT or STOP instruction is executed.

**Caution** The low-speed on-chip oscillator clock ( $f_{IL}$ ) can only be selected as the real-time clock operation clock when the fixed-cycle interrupt function is used.

**Remark**

|             |                                               |
|-------------|-----------------------------------------------|
| $f_X$ :     | X1 clock oscillation frequency                |
| $f_{IH}$ :  | High-speed on-chip oscillator clock frequency |
| $f_{EX}$ :  | External main system clock frequency          |
| $f_{XT}$ :  | XT1 clock oscillation frequency               |
| $f_{EXS}$ : | External subsystem clock frequency            |
| $f_{IL}$ :  | Low-speed on-chip oscillator clock frequency  |

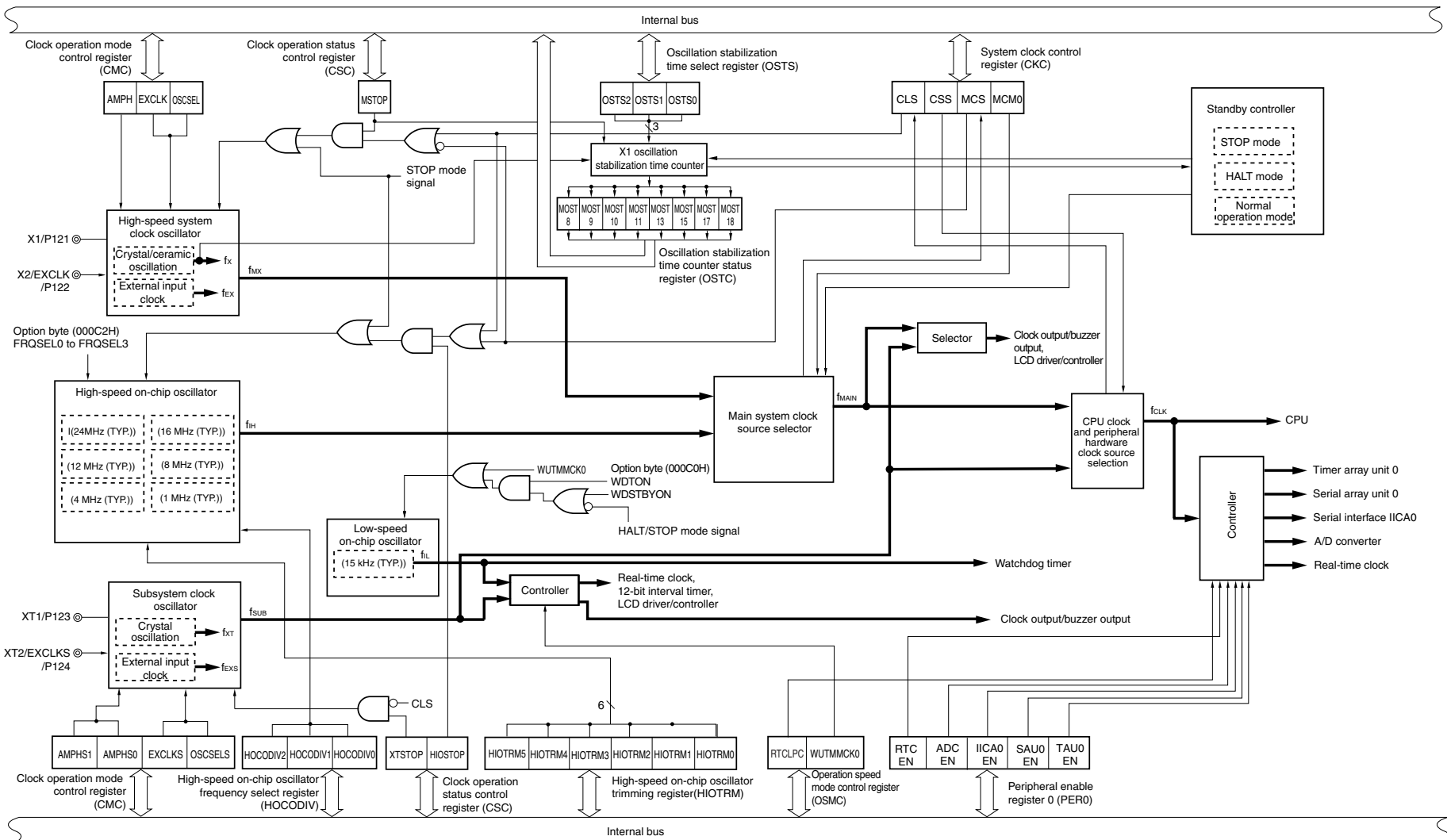
## 5.2 Configuration of Clock Generator

The clock generator includes the following hardware.

**Table 5-1. Configuration of Clock Generator**

| Item              | Configuration                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Control registers | Clock operation mode control register (CMC)<br>System clock control register (CKC)<br>Clock operation status control register (CSC)<br>Oscillation stabilization time counter status register (OSTC)<br>Oscillation stabilization time select register (OSTS)<br>Peripheral enable register 0 (PER0)<br>Operation speed mode control register (OSMC)<br>High-speed on-chip oscillator frequency select register (HOCODIV)<br>High-speed on-chip oscillator trimming register (HIOTRM) |
| Oscillators       | X1 oscillator<br>XT1 oscillator<br>High-speed on-chip oscillator<br>Low-speed on-chip oscillator                                                                                                                                                                                                                                                                                                                                                                                      |

Figure 5-1. Block Diagram of Clock Generator



(Remark is listed on the next page after next.)

&lt;R&gt;

|               |                          |                                               |
|---------------|--------------------------|-----------------------------------------------|
| <b>Remark</b> | <b>fx:</b>               | X1 clock oscillation frequency                |
|               | <b>f<sub>IH</sub>:</b>   | High-speed on-chip oscillator clock frequency |
|               | <b>f<sub>EX</sub>:</b>   | External main system clock frequency          |
|               | <b>f<sub>MX</sub>:</b>   | High-speed system clock frequency             |
|               | <b>f<sub>MAIN</sub>:</b> | Main system clock frequency                   |
|               | <b>f<sub>XT</sub>:</b>   | XT1 clock oscillation frequency               |
|               | <b>f<sub>EXS</sub>:</b>  | External subsystem clock frequency            |
|               | <b>f<sub>SUB</sub>:</b>  | Subsystem clock frequency                     |
|               | <b>f<sub>CLK</sub>:</b>  | CPU/peripheral hardware clock frequency       |
|               | <b>f<sub>IL</sub>:</b>   | Low-speed on-chip oscillator clock frequency  |

### 5.3 Registers Controlling Clock Generator

The following nine registers are used to control the clock generator.

- Clock operation mode control register (CMC)
- System clock control register (CKC)
- Clock operation status control register (CSC)
- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)
- Peripheral enable register 0 (PER0)
- Operation speed mode control register (OSMC)
- High-speed on-chip oscillator frequency select register (HOCODIV)
- High-speed on-chip oscillator trimming register (HIOTRM)

#### 5.3.1 Clock operation mode control register (CMC)

This register is used to set the operation mode of the X1/P121, X2/EXCLK/P122, XT1/P123, and XT2/EXCLKS/P124 pins, and to select a gain of the oscillator.

The CMC register can be written only once by an 8-bit memory manipulation instruction after reset release. This register can be read by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 5-2. Format of Clock Operation Mode Control Register (CMC)**

Address: FFFA0H After reset: 00H R/W

|        |        |                                           |                                             |         |                                      |        |                      |      |
|--------|--------|-------------------------------------------|---------------------------------------------|---------|--------------------------------------|--------|----------------------|------|
| Symbol | 7      | 6                                         | 5                                           | 4       | 3                                    | 2      | 1                    | 0    |
| CMC    | EXCLK  | OSCSEL                                    | EXCLKS                                      | OSCSELS | 0                                    | AMPHS1 | AMPHS0               | AMPH |
|        |        |                                           |                                             |         |                                      |        |                      |      |
|        | EXCLK  | OSCSEL                                    | High-speed system clock pin operation mode  |         | X1/P121 pin                          |        | X2/EXCLK/P122 pin    |      |
|        | 0      | 0                                         | Input port mode                             |         | Input port                           |        |                      |      |
|        | 0      | 1                                         | X1 oscillation mode                         |         | Crystal/ceramic resonator connection |        |                      |      |
|        | 1      | 0                                         | Input port mode                             |         | Input port                           |        |                      |      |
|        | 1      | 1                                         | External clock input mode                   |         | Input port                           |        | External clock input |      |
|        |        |                                           |                                             |         |                                      |        |                      |      |
|        | EXCLKS | OSCSELS                                   | Subsystem clock pin operation mode          |         | XT1/P123 pin                         |        | XT2/EXCLKS/P124 pin  |      |
|        | 0      | 0                                         | Input port mode                             |         | Input port                           |        |                      |      |
|        | 0      | 1                                         | XT1 oscillation mode                        |         | Crystal resonator connection         |        |                      |      |
|        | 1      | 0                                         | Input port mode                             |         | Input port                           |        |                      |      |
|        | 1      | 1                                         | External clock input mode                   |         | Input port                           |        | External clock input |      |
|        |        |                                           |                                             |         |                                      |        |                      |      |
|        | AMPHS1 | AMPHS0                                    | XT1 oscillator oscillation mode selection   |         |                                      |        |                      |      |
|        | 0      | 0                                         | Low power consumption oscillation (default) |         |                                      |        |                      |      |
|        | 0      | 1                                         | Normal oscillation                          |         |                                      |        |                      |      |
|        | 1      | 0                                         | Ultra-low power consumption oscillation     |         |                                      |        |                      |      |
|        | 1      | 1                                         | Setting prohibited                          |         |                                      |        |                      |      |
|        |        |                                           |                                             |         |                                      |        |                      |      |
|        | AMPH   | Control of X1 clock oscillation frequency |                                             |         |                                      |        |                      |      |
|        | 0      | 1 MHz ≤ f <sub>x</sub> ≤ 10 MHz           |                                             |         |                                      |        |                      |      |
|        | 1      | 10 MHz < f <sub>x</sub> ≤ 20 MHz          |                                             |         |                                      |        |                      |      |

- Cautions 1.** The CMC register can be written only once after reset release, by an 8-bit memory manipulation instruction. When using the CMC register with its initial value (00H), be sure to set the register to 00H after a reset ends in order to prevent malfunction due to a program loop. Such a malfunction becomes unrecoverable when a value other than 00H is mistakenly written.
- After reset release, set the CMC register before X1 or XT1 oscillation is started as set by the clock operation status control register (CSC).
  - Be sure to set the AMPH bit to 1 if the X1 clock oscillation frequency exceeds 10 MHz.
  - Specify the settings for the AMPH, AMPHS1, and AMPHS0 bits while  $f_{IH}$  is selected as  $f_{CLK}$  after a reset ends (before  $f_{CLK}$  is switched to  $f_{MX}$ ).
  - Oscillation stabilization time of  $f_{XT}$ , counting on the software.
  - Although the maximum system clock frequency is 24 MHz, the maximum frequency of the X1 oscillator is 20 MHz.

(Cautions and Remark are given on the next page.)

**Cautions 7.** The XT1 oscillator is a circuit with low amplification in order to achieve low-power consumption. Note the following points when designing the circuit.

- Pins and circuit boards include parasitic capacitance. Therefore, perform oscillation evaluation using a circuit board to be actually used and confirm that there are no problems.
- Before using the ultra-low power consumption oscillation (AMPHS1, AMPHS0 = 1, 0) as the mode of the XT1 oscillator, evaluate the resonators.
- Make the wiring between the XT1 and XT2 pins and the resonators as short as possible, and minimize the parasitic capacitance and wiring resistance. Note this particularly when the ultra-low power consumption oscillation (AMPHS1, AMPHS0 = 1, 0) is selected.
- Configure the circuit of the circuit board, using material with little wiring resistance.
- Place a ground pattern that has the same potential as V<sub>SS</sub> as much as possible near the XT1 oscillator.
- Be sure that the signal lines between the XT1 and XT2 pins, and the resonators do not cross with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.
- The impedance between the XT1 and XT2 pins may drop and oscillation may be disturbed due to moisture absorption of the circuit board in a high-humidity environment or dew condensation on the board. When using the circuit board in such an environment, take measures to damp-proof the circuit board, such as by coating.
- When coating the circuit board, use material that does not cause capacitance or leakage between the XT1 and XT2 pins.

**Remark** fx: X1 clock frequency



### 5.3.2 System clock control register (CKC)

This register is used to select a CPU/peripheral hardware clock and main system clock.

The CKC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

**Figure 5-3. Format of System Clock Control Register (CKC)**

Address: FFFA4H After reset: 00H R/W<sup>Note 1</sup>

| Symbol | <7> | <6> | <5> | <4>  | 3 | 2 | 1 | 0 |
|--------|-----|-----|-----|------|---|---|---|---|
| CKC    | CLS | CSS | MCS | MCM0 | 0 | 0 | 0 | 0 |

|     |                                                       |
|-----|-------------------------------------------------------|
| CLS | Status of CPU/peripheral hardware clock ( $f_{CLK}$ ) |
| 0   | Main system clock ( $f_{MAIN}$ )                      |
| 1   | Subsystem clock ( $f_{SUB}$ )                         |

|                     |                                                          |
|---------------------|----------------------------------------------------------|
| CSS                 | Selection of CPU/peripheral hardware clock ( $f_{CLK}$ ) |
| 0                   | Main system clock ( $f_{MAIN}$ )                         |
| 1 <sup>Note 2</sup> | Subsystem clock ( $f_{SUB}$ )                            |

|     |                                                  |
|-----|--------------------------------------------------|
| MCS | Status of Main system clock ( $f_{MAIN}$ )       |
| 0   | High-speed on-chip oscillator clock ( $f_{IH}$ ) |
| 1   | High-speed system clock ( $f_{MX}$ )             |

|                        |                                                                                                      |
|------------------------|------------------------------------------------------------------------------------------------------|
| MCM0 <sup>Note 2</sup> | Main system clock ( $f_{MAIN}$ ) operation control                                                   |
| 0                      | Selects the high-speed on-chip oscillator clock ( $f_{IH}$ ) as the main system clock ( $f_{MAIN}$ ) |
| 1                      | Selects the high-speed system clock ( $f_{MX}$ ) as the main system clock ( $f_{MAIN}$ )             |

**Notes** 1. Bits 7 and 5 are read-only.

2. Changing the value of the MCM0 bit is prohibited while the CSS bit is set to 1.

**Remarks** 1.  $f_{IH}$ : High-speed on-chip oscillator clock frequency

$f_{MX}$ : High-speed system clock frequency

$f_{MAIN}$ : Main system clock frequency

$f_{SUB}$ : Subsystem clock frequency

2.  $\times$ : don't care

**Cautions** 1. Be sure to set bit 3 to 0.

2. The clock set by the CSS bit is supplied to the CPU and peripheral hardware. If the CPU clock is changed, therefore, the clock supplied to peripheral hardware (except the real-time clock, 12-bit interval timer, clock output/buzzer output, LCD driver/controller, and watchdog timer) is also changed at the same time. Consequently, stop each peripheral function when changing the CPU/peripheral hardware clock.

3. If the subsystem clock is used as the peripheral hardware clock, the operations of the A/D converter and IICA are not guaranteed. For the operating characteristics of the peripheral hardware, refer to the chapters describing the various peripheral hardware as well as CHAPTER 30 ELECTRICAL SPECIFICATIONS.

### 5.3.3 Clock operation status control register (CSC)

This register is used to control the operations of the high-speed system clock, high-speed on-chip oscillator clock, and subsystem clock (except the low-speed on-chip oscillator clock).

The CSC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to C0H.

**Figure 5-4. Format of Clock Operation Status Control Register (CSC)**

Address: FFFA1H After reset: C0H R/W

| Symbol | <7>   | <6>    | 5 | 4 | 3 | 2 | 1 | <0>     |
|--------|-------|--------|---|---|---|---|---|---------|
| CSC    | MSTOP | XTSTOP | 0 | 0 | 0 | 0 | 0 | HIOSTOP |

|       |                                           |                                          |                 |
|-------|-------------------------------------------|------------------------------------------|-----------------|
| MSTOP | High-speed system clock operation control |                                          |                 |
|       | X1 oscillation mode                       | External clock input mode                | Input port mode |
| 0     | X1 oscillator operating                   | External clock from EXCLK pin is valid   | Input port      |
| 1     | X1 oscillator stopped                     | External clock from EXCLK pin is invalid |                 |

|        |                                   |                                           |                 |
|--------|-----------------------------------|-------------------------------------------|-----------------|
| XTSTOP | Subsystem clock operation control |                                           |                 |
|        | XT1 oscillation mode              | External clock input mode                 | Input port mode |
| 0      | XT1 oscillator operating          | External clock from EXCLKS pin is valid   | Input port      |
| 1      | XT1 oscillator stopped            | External clock from EXCLKS pin is invalid |                 |

|         |                                                       |  |  |
|---------|-------------------------------------------------------|--|--|
| HIOSTOP | High-speed on-chip oscillator clock operation control |  |  |
| 0       | High-speed on-chip oscillator operating               |  |  |
| 1       | High-speed on-chip oscillator stopped                 |  |  |

- Cautions**
1. After reset release, set the clock operation mode control register (CMC) before setting the CSC register.
  2. Set the oscillation stabilization time select register (OSTS) before setting the MSTOP bit to 0 after releasing reset. Note that if the OSTS register is being used with its default settings, the OSTS register is not required to be set here.
  3. To start X1 oscillation as set by the MSTOP bit, check the oscillation stabilization time of the X1 clock by using the oscillation stabilization time counter status register (OSTC).
  4. When starting XT1 oscillation by setting the XSTOP bit, wait for oscillation of the subsystem clock to stabilize by setting a wait time using software.
  5. Do not stop the clock selected for the CPU peripheral hardware clock (f<sub>CLK</sub>) with the OSC register.
  6. The setting of the flags of the register to stop clock oscillation (invalidate the external clock input) and the condition before clock oscillation is to be stopped are as Table 5-2.

**Table 5-2. Stopping Clock Method**

| Clock                               | Condition Before Stopping Clock<br>(Invalidating External Clock Input)                                                                           | Setting of CSC<br>Register Flags |
|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|
| X1 clock                            | CPU and peripheral hardware clocks operate with a clock other than the high-speed system clock.<br>(CLS = 0 and MCS = 0, or CLS = 1)             | MSTOP = 1                        |
| External main system clock          |                                                                                                                                                  |                                  |
| XT1 clock                           | CPU and peripheral hardware clocks operate with a clock other than the subsystem clock.<br>(CLS = 0)                                             | XTSTOP = 1                       |
| External subsystem clock            |                                                                                                                                                  |                                  |
| High-speed on-chip oscillator clock | CPU and peripheral hardware clocks operate with a clock other than the high-speed on-chip oscillator clock.<br>(CLS = 0 and MCS = 1, or CLS = 1) | HIOSTOP = 1                      |

### 5.3.4 Oscillation stabilization time counter status register (OSTC)

This is the register that indicates the count status of the X1 clock oscillation stabilization time counter.

The X1 clock oscillation stabilization time can be checked in the following case,

- If the X1 clock starts oscillation while the high-speed on-chip oscillator clock or subsystem clock is being used as the CPU clock.
- If the STOP mode is entered and then released while the high-speed on-chip oscillator clock is being used as the CPU clock with the X1 clock oscillating.

The OSTC register can be read by a 1-bit or 8-bit memory manipulation instruction.

When reset signal is generated, the STOP instruction and MSTOP (bit 7 of clock operation status control register (CSC)) = 1 clear the OSTC register to 00H.

**Remark** The oscillation stabilization time counter starts counting in the following cases.

- When oscillation of the X1 clock starts (EXCLK, OSCSEL = 0, 1 → MSTOP = 0)
- When the STOP mode is released

**Figure 5-5. Format of Oscillation Stabilization Time Counter Status Register (OSTC)**

Address: FFFA2H After reset: 00H R

|        |           |           |            |            |            |            |            |            |
|--------|-----------|-----------|------------|------------|------------|------------|------------|------------|
| Symbol | 7         | 6         | 5          | 4          | 3          | 2          | 1          | 0          |
| OSTC   | MOST<br>8 | MOST<br>9 | MOST<br>10 | MOST<br>11 | MOST<br>13 | MOST<br>15 | MOST<br>17 | MOST<br>18 |

| MOST<br>8 | MOST<br>9 | MOST<br>10 | MOST<br>11 | MOST<br>13 | MOST<br>15 | MOST<br>17 | MOST<br>18 | Oscillation stabilization time status |                          |                          |
|-----------|-----------|------------|------------|------------|------------|------------|------------|---------------------------------------|--------------------------|--------------------------|
|           |           |            |            |            |            |            |            |                                       | $f_x = 10 \text{ MHz}$   | $f_x = 20 \text{ MHz}$   |
| 0         | 0         | 0          | 0          | 0          | 0          | 0          | 0          | $2^8/f_x \text{ max.}$                | $25.6 \mu\text{s max.}$  | $12.8 \mu\text{s max.}$  |
| 1         | 0         | 0          | 0          | 0          | 0          | 0          | 0          | $2^9/f_x \text{ min.}$                | $25.6 \mu\text{s min.}$  | $12.8 \mu\text{s min.}$  |
| 1         | 1         | 0          | 0          | 0          | 0          | 0          | 0          | $2^9/f_x \text{ min.}$                | $51.2 \mu\text{s min.}$  | $25.6 \mu\text{s min.}$  |
| 1         | 1         | 1          | 0          | 0          | 0          | 0          | 0          | $2^{10}/f_x \text{ min.}$             | $102.4 \mu\text{s min.}$ | $51.2 \mu\text{s min.}$  |
| 1         | 1         | 1          | 1          | 0          | 0          | 0          | 0          | $2^{11}/f_x \text{ min.}$             | $204.8 \mu\text{s min.}$ | $102.4 \mu\text{s min.}$ |
| 1         | 1         | 1          | 1          | 1          | 0          | 0          | 0          | $2^{13}/f_x \text{ min.}$             | $819.2 \mu\text{s min.}$ | $409.6 \mu\text{s min.}$ |
| 1         | 1         | 1          | 1          | 1          | 1          | 0          | 0          | $2^{15}/f_x \text{ min.}$             | $3.27 \text{ ms min.}$   | $1.64 \text{ ms min.}$   |
| 1         | 1         | 1          | 1          | 1          | 1          | 1          | 0          | $2^{17}/f_x \text{ min.}$             | $13.11 \text{ ms min.}$  | $6.55 \text{ ms min.}$   |
| 1         | 1         | 1          | 1          | 1          | 1          | 1          | 1          | $2^{18}/f_x \text{ min.}$             | $26.21 \text{ ms min.}$  | $13.11 \text{ ms min.}$  |

**Cautions** 1. After the above time has elapsed, the bits are set to 1 in order from the MOST8 bit and remain 1.

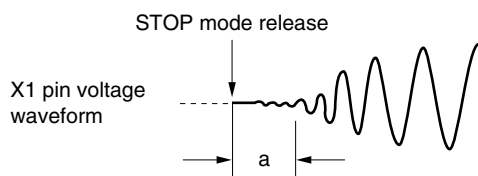
2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by the oscillation stabilization time select register (OSTS).

In the following cases, set the oscillation stabilization time of the OSTS register to the value greater than the count value which is to be checked by the OSTC register.

- If the X1 clock starts oscillation while the high-speed on-chip oscillator clock or subsystem clock is being used as the CPU clock.
- If the STOP mode is entered and then released while the high-speed on-chip oscillator clock is being used as the CPU clock with the X1 clock oscillating.

(Note, therefore, that only the status up to the oscillation stabilization time set by the OSTS register is set to the OSTC register after the STOP mode is released.)

3. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



**Remark**  $f_x$ : X1 clock oscillation frequency

### 5.3.5 Oscillation stabilization time select register (OSTS)

This register is used to select the X1 clock oscillation stabilization wait time when the STOP mode is released.

When the X1 clock is selected as the CPU clock, the operation automatically waits for the time set using the OSTS register after the STOP mode is released.

When the high-speed on-chip oscillator clock is selected as the CPU clock, confirm with the oscillation stabilization time counter status register (OSTC) that the desired oscillation stabilization time has elapsed after the STOP mode is released. The oscillation stabilization time can be checked up to the time set using the OSTC register.

The OSTS register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets the OSTS register to 07H.

**Figure 5-6. Format of Oscillation Stabilization Time Select Register (OSTS)**

Address: FFFA3H After reset: 07H R/W

|        |   |   |   |   |   |       |       |       |
|--------|---|---|---|---|---|-------|-------|-------|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2     | 1     | 0     |
| OSTS   | 0 | 0 | 0 | 0 | 0 | OSTS2 | OSTS1 | OSTS0 |

| OSTS2 | OSTS1 | OSTS0 | Oscillation stabilization time selection | $f_x = 10 \text{ MHz}$ | $f_x = 20 \text{ MHz}$ |
|-------|-------|-------|------------------------------------------|------------------------|------------------------|
| 0     | 0     | 0     | $2^8/f_x$                                | 25.6 $\mu\text{s}$     | 12.8 $\mu\text{s}$     |
| 0     | 0     | 1     | $2^9/f_x$                                | 51.2 $\mu\text{s}$     | 25.6 $\mu\text{s}$     |
| 0     | 1     | 0     | $2^{10}/f_x$                             | 102.4 $\mu\text{s}$    | 51.2 $\mu\text{s}$     |
| 0     | 1     | 1     | $2^{11}/f_x$                             | 204.8 $\mu\text{s}$    | 102.4 $\mu\text{s}$    |
| 1     | 0     | 0     | $2^{13}/f_x$                             | 819.2 $\mu\text{s}$    | 409.6 $\mu\text{s}$    |
| 1     | 0     | 1     | $2^{15}/f_x$                             | 3.27 ms                | 1.64 ms                |
| 1     | 1     | 0     | $2^{17}/f_x$                             | 13.11 ms               | 6.55 ms                |
| 1     | 1     | 1     | $2^{18}/f_x$                             | 26.21 ms               | 13.11 ms               |

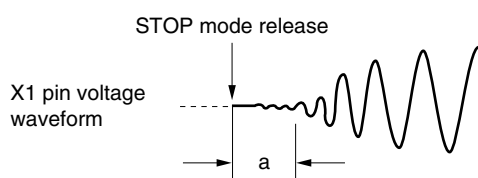
**Cautions** 1. To set the STOP mode when the X1 clock is used as the CPU clock, set the OSTS register before executing the STOP instruction.

2. Change the setting of the OSTS register before setting the MSTOP bit of the clock operation status control register (CSC) to 0.
3. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.
4. The oscillation stabilization time counter counts up to the oscillation stabilization time set by the OSTS register.

In the following cases, set the oscillation stabilization time of the OSTS register to the value greater than the count value which is to be checked by the OSTC register after the oscillation starts.

- If the X1 clock starts oscillation while the high-speed on-chip oscillator clock or subsystem clock is being used as the CPU clock.
- If the STOP mode is entered and then released while the high-speed on-chip oscillator clock is being used as the CPU clock with the X1 clock oscillating. (Note, therefore, that only the status up to the oscillation stabilization time set by the OSTS register is set to the OSTC register after the STOP mode is released.)

5. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



**Remark**  $f_x$ : X1 clock oscillation frequency

### 5.3.6 Peripheral enable register 0 (PER0)

These registers are used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

To use the peripheral functions below, which are controlled by this register, set (1) the bit corresponding to each function before specifying the initial settings of the peripheral functions.

- Real-time clock, 12-bit interval timer
- A/D converter
- Serial interface IICA0
- Serial array unit 0
- Timer array unit 0
- LCD driver/controller

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

**Figure 5-7. Format of Peripheral Enable Register 0 (PER0) (1/2)**

Address: F00F0H After reset: 00H R/W

| Symbol | <7>   | 6 | <5>   | <4>     | 3 | <2>    | 1 | <0>    |
|--------|-------|---|-------|---------|---|--------|---|--------|
| PER0   | RTCEN | 0 | ADCEN | IICA0EN | 0 | SAU0EN | 0 | TAU0EN |

| RTCEN | Real-time clock (RTC) and 12-bit interval timer                                                                                                                                                     | LCD driver/controller and clock output/buzzer output controller                                                                                    |                                                                                                                                                      |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |                                                                                                                                                                                                     | When subsystem clock ( $f_{SUB}$ ) is selected.                                                                                                    | When subsystem clock ( $f_{SUB}$ ) is not selected.                                                                                                  |
| 0     | Stops input clock supply.<br>• SFR used by the real-time clock (RTC) and 12-bit interval timer cannot be written.<br>• The real-time clock (RTC) and 12-bit interval timer are in the reset status. | Stops input clock and subsystem clock supply.<br>• SFR used by the LCD driver/controller and clock output/buzzer output can be read and written.   | Enables input clock and main system clock supply.<br>• SFR used by the LCD driver/controller and clock output/buzzer output can be read and written. |
| 1     | Enables input clock supply.<br>• SFR used by the real-time clock (RTC) and 12-bit interval timer can be read and written.                                                                           | Enables input clock and subsystem clock supply.<br>• SFR used by the LCD driver/controller and clock output/buzzer output can be read and written. |                                                                                                                                                      |

| ADCEN | Control of A/D converter input clock supply                                                                                    |
|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 0     | Stops input clock supply.<br>• SFR used by the A/D converter cannot be written.<br>• The A/D converter is in the reset status. |
| 1     | Enables input clock supply.<br>• SFR used by the A/D converter can be read and written.                                        |

**Caution** Be sure to clear the following bits 1, 3, and 6 to 0.

**Figure 5-7. Format of Peripheral Enable Register 0 (PER0) (2/2)**

Address: F00F0H After reset: 00H R/W

|        |       |   |       |         |   |        |   |        |
|--------|-------|---|-------|---------|---|--------|---|--------|
| Symbol | <7>   | 6 | <5>   | <4>     | 3 | <2>    | 1 | <0>    |
| PER0   | RTCEN | 0 | ADCEN | IICA0EN | 0 | SAU0EN | 0 | TAU0EN |

| IICA0EN | Control of serial interface IICA0 input clock supply                                                                                                                                                 |
|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0       | Stops input clock supply.<br><ul style="list-style-type: none"> <li>SFR used by the serial interface IICA0 cannot be written.</li> <li>The serial interface IICA0 is in the reset status.</li> </ul> |
| 1       | Enables input clock supply.<br><ul style="list-style-type: none"> <li>SFR used by the serial interface IICA0 can be read and written.</li> </ul>                                                     |

| SAU0EN | Control of serial array unit 0 input clock supply                                                                                                                                              |
|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0      | Stops input clock supply.<br><ul style="list-style-type: none"> <li>SFR used by the serial array unit 0 cannot be written.</li> <li>The serial array unit 0 is in the reset status.</li> </ul> |
| 1      | Enables input clock supply.<br><ul style="list-style-type: none"> <li>SFR used by the serial array unit 0 can be read and written.</li> </ul>                                                  |

| TAU0EN | Control of timer array unit 0 input clock supply                                                                                                                                     |
|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0      | Stops input clock supply.<br><ul style="list-style-type: none"> <li>SFR used by timer array unit 0 cannot be written.</li> <li>Timer array unit 0 is in the reset status.</li> </ul> |
| 1      | Enables input clock supply.<br><ul style="list-style-type: none"> <li>SFR used by timer array unit 0 can be read and written.</li> </ul>                                             |

**Caution** Be sure to clear the following bits 1, 3, and 6 to 0.



### 5.3.7 Operation speed mode control register (OSMC)

This register is used to reduce power consumption by stopping as many unnecessary clock functions.

If the RTCLPC bit is set to 1, power consumption can be reduced, because clock supply to the peripheral functions, except the real-time clock, 12-bit interval timer, and LCD driver/controller, is stopped in HALT mode while subsystem clock is selected as CPU clock. Set bit 7 (RTCEN) of peripheral enable registers 0 (PER0) to 1 before this setting.

In addition, the OSMC register can be used to select the operation clock of the real-time clock, 12-bit interval timer, and LCD driver/controller.

The OSMC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 5-8. Format of Operation Speed Mode Control Register (OSMC)**

Address: F00F3H After reset: 00H R/W

| Symbol | 7      | 6 | 5 | 4        | 3 | 2 | 1 | 0 |
|--------|--------|---|---|----------|---|---|---|---|
| OSMC   | RTCLPC | 0 | 0 | WUTMMCK0 | 0 | 0 | 0 | 0 |

| RTCLPC | Setting in HALT mode while subsystem clock is selected as CPU clock                                                                   |
|--------|---------------------------------------------------------------------------------------------------------------------------------------|
| 0      | Enables supply of subsystem clock to peripheral functions<br>(See Table 19-1 for peripheral functions whose operations are enabled.)  |
| 1      | Stops supply of subsystem clock to peripheral functions other than real-time clock, 12-bit interval timer, and LCD driver/controller. |

| WUTMMCK0<br><small>Note</small> | Selection of operation clock for real-time clock, 12-bit interval timer, and LCD driver/controller | Selection of clock output from PCLBUZn pin of clock output/buzzer output |
|---------------------------------|----------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|
| 0                               | Subsystem clock ( $f_{SUB}$ )                                                                      | Selecting the subsystem clock ( $f_{SUB}$ ) is enabled.                  |
| 1                               | Low-speed on-chip oscillator clock ( $f_{IL}$ )                                                    | Selecting the subsystem clock ( $f_{SUB}$ ) is disabled.                 |

**Note** Be sure to select the subsystem clock (WUTMMCK0 bit = 0) if the subsystem clock is oscillating.

**Cautions** 1. The subsystem clock and low-speed on-chip oscillator clock can only be switched by using the WUTMMCK0 bit if the real-time clock, 12-bit interval timer, and LCD driver/controller are all stopped.

These are stopped as follows:

Real-time clock: Set the RTCE bit to 0.

12-bit interval timer: Set the RINTE bit to 0.

LCD driver/controller: Set the SCOC and VLCON bits to 0.

2. Do not select  $f_{SUB}$  as the clock output or buzzer output clock when the WUTMMCK0 bit is set to 1.

**Remark** RTCE: Bit 7 of real-time clock control register 0 (RTCC0)  
 RINTE: Bit 15 of the interval timer control register (ITMC)  
 SCOC: Bit 6 of LCD mode register 1 (LCDM1)  
 VLCON: Bit 5 of LCD mode register 1 (LCDM1)

### 5.3.8 High-speed on-chip oscillator frequency select register (HOCODIV)

The frequency of the high-speed on-chip oscillator which is set by an option byte (000C2H) can be changed by using high-speed on-chip oscillator frequency select register (HOCODIV). However, the selectable frequency depends on the FRQSEL3 bit of the option byte (000C2H).

The HOCODIV register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to default value (undefined).

**Figure 5-9. Format of High-speed On-chip Oscillator frequency select register (HOCODIV)**

Address: F00A8H After reset: undefined R/W

|         |   |   |   |   |   |          |          |          |
|---------|---|---|---|---|---|----------|----------|----------|
| Symbol  | 7 | 6 | 5 | 4 | 3 | 2        | 1        | 0        |
| HOCODIV | 0 | 0 | 0 | 0 | 0 | HOCODIV2 | HOCODIV1 | HOCODIV0 |

| HOCODIV2          | HOCODIV1 | HOCODIV0 | High-Speed On-Chip Oscillator Clock Frequency |                    |
|-------------------|----------|----------|-----------------------------------------------|--------------------|
|                   |          |          | FRQSEL3 Bit is 0                              | FRQSEL3 Bit is 1   |
| 0                 | 0        | 0        | 24 MHz                                        | Setting prohibited |
| 0                 | 0        | 1        | 12 MHz                                        | 16 MHz             |
| 0                 | 1        | 0        | 6 MHz                                         | 8 MHz              |
| 0                 | 1        | 1        | 3 MHz                                         | 4 MHz              |
| 1                 | 0        | 0        | Setting prohibited                            | 2 MHz              |
| 1                 | 0        | 1        | Setting prohibited                            | 1 MHz              |
| Other than aboves |          |          | Setting prohibited                            |                    |

<R>

**Cautions** 1. Set the HOCODIV register within the operable voltage range of the flash operation mode set in the option byte (000C2H) before and after the frequency change.

| Option Byte (000C2H)<br>Value |        | Flash Operation Mode       | Operating<br>Frequency Range | Operating Voltage<br>Range |
|-------------------------------|--------|----------------------------|------------------------------|----------------------------|
| CMODE1                        | CMODE2 |                            |                              |                            |
| 0                             | 0      | LV (low-voltage main) mode | 1 to 4 MHz                   | 1.6 to 5.5 V               |
| 1                             | 0      | LS (low-speed main) mode   | 1 to 8 MHz                   | 1.8 to 5.5 V               |
| 1                             | 1      | HS (high-speed main) mode  | 1 to 16 MHz                  | 2.4 to 5.5 V               |
|                               |        |                            | 1 to 32 MHz                  | 2.7 to 5.5 V               |

<R>

2. Set the HOCODIV register with the high-speed on-chip oscillator clock ( $f_{IH}$ ) selected as the CPU/peripheral hardware clock ( $f_{CLK}$ ).

<R>

3. After the frequency is changed with the HOCODIV register, the frequency is switched after the following transition time has elapsed.

- Operation for three clocks at the pre-change frequency
- CPU/peripheral hardware clock wait at the post-change frequency for up to three clocks

### 5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)

This register is used to adjust the accuracy of the high-speed on-chip oscillator.

With self-measurement of the high-speed on-chip oscillator frequency via a timer using high-accuracy external clock input (timer array unit), and so on, the accuracy can be adjusted.

The HIOTRM register can be set by an 8-bit memory manipulation instruction.

**Caution** The frequency will vary if the temperature and V<sub>DD</sub> pin voltage change after accuracy adjustment. When the temperature and V<sub>DD</sub> voltage change, accuracy adjustment must be executed regularly or before the frequency accuracy is required.

Figure 5-10. Format of High-Speed On-Chip Oscillator Trimming Register (HIOTRM)

Address: F00A0H After reset: **Note** R/W

|        |   |   |         |         |         |         |         |         |
|--------|---|---|---------|---------|---------|---------|---------|---------|
| Symbol | 7 | 6 | 5       | 4       | 3       | 2       | 1       | 0       |
| HIOTRM | 0 | 0 | HIOTRM5 | HIOTRM4 | HIOTRM3 | HIOTRM2 | HIOTRM1 | HIOTRM0 |

| HIOTRM5     | HIOTRM4 | HIOTRM3 | HIOTRM2 | HIOTRM1 | HIOTRM0 | High-speed on-chip oscillator |
|-------------|---------|---------|---------|---------|---------|-------------------------------|
| 0           | 0       | 0       | 0       | 0       | 0       | Minimum speed                 |
| 0           | 0       | 0       | 0       | 0       | 1       | ↑                             |
| 0           | 0       | 0       | 0       | 1       | 0       |                               |
| 0           | 0       | 0       | 0       | 1       | 1       |                               |
| 0           | 0       | 0       | 1       | 0       | 0       |                               |
| •<br>•<br>• |         |         |         |         |         |                               |
| 1           | 1       | 1       | 1       | 1       | 0       | ↓                             |
| 1           | 1       | 1       | 1       | 1       | 1       |                               |
|             |         |         |         |         |         | Maximum speed                 |

**Note** The reset value differs for each chip.

## 5.4 System Clock Oscillator

### 5.4.1 X1 oscillator

The X1 oscillator oscillates with a crystal resonator or ceramic resonator (1 to 20 MHz) connected to the X1 and X2 pins.

An external clock can also be input. In this case, input the clock signal to the EXCLK pin.

To use the X1 oscillator, set bits 7 and 6 (EXCLK, OSCSEL) of the clock operation mode control register (CMC) as follows.

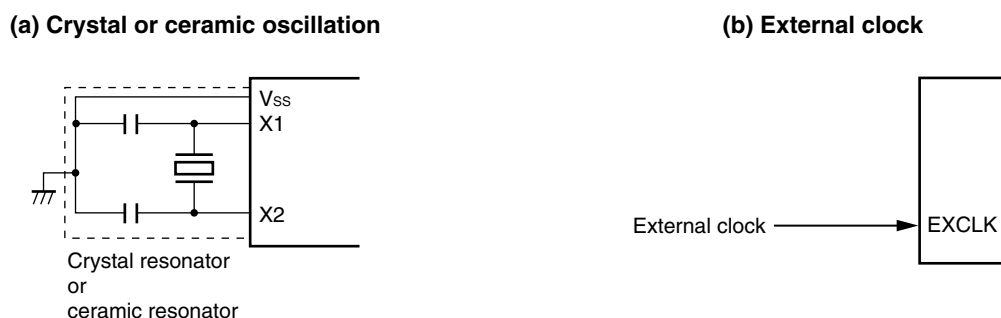
- Crystal or ceramic oscillation: EXCLK, OSCSEL = 0, 1
- External clock input: EXCLK, OSCSEL = 1, 1

When the X1 oscillator is not used, set the input port mode (EXCLK, OSCSEL = 0, 0).

When the pins are not used as input port pins, either, see **Table 2-3 Connection of Unused Pins (64-pin products)**.

Figure 5-11 shows an example of the external circuit of the X1 oscillator.

**Figure 5-11. Example of External Circuit of X1 Oscillator**



Cautions are listed on the next page.

### 5.4.2 XT1 oscillator

The XT1 oscillator oscillates with a crystal resonator (32.768 kHz (TYP.)) connected to the XT1 and XT2 pins.

To use the XT1 oscillator, set bit 4 (OSCSELS) of the clock operation mode control register (CMC) to 1.

An external clock can also be input. In this case, input the clock signal to the EXCLKS pin.

To use the XT1 oscillator, set bits 5 and 4 (EXCLKS, OSCSELS) of the clock operation mode control register (CMC) as follows.

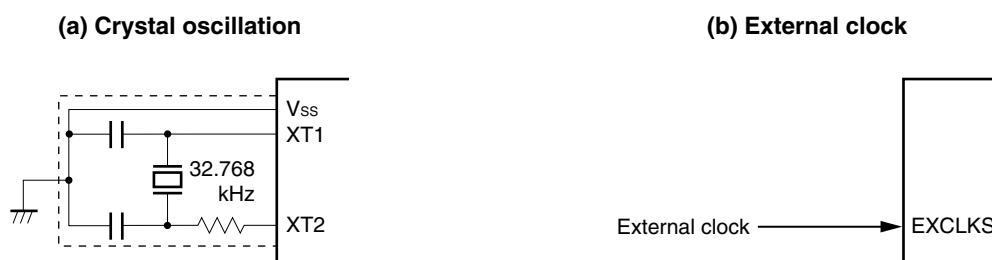
- Crystal oscillation: EXCLKS, OSCSELS = 0, 1
- External clock input: EXCLKS, OSCSELS = 1, 1

When the XT1 oscillator is not used, set the input port mode (EXCLKS, OSCSELS = 0, 0).

When the pins are not used as input port pins, either, see **Table 2-3. Connection of Unused Pins (64-pin products)**.

Figure 5-12 shows an example of the external circuit of the XT1 oscillator.

Figure 5-12. Example of External Circuit of XT1 Oscillator



**Caution** When using the X1 oscillator and XT1 oscillator, wire as follows in the area enclosed by the broken lines in the Figures 5-10 and 5-11 to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as V<sub>SS</sub>. Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

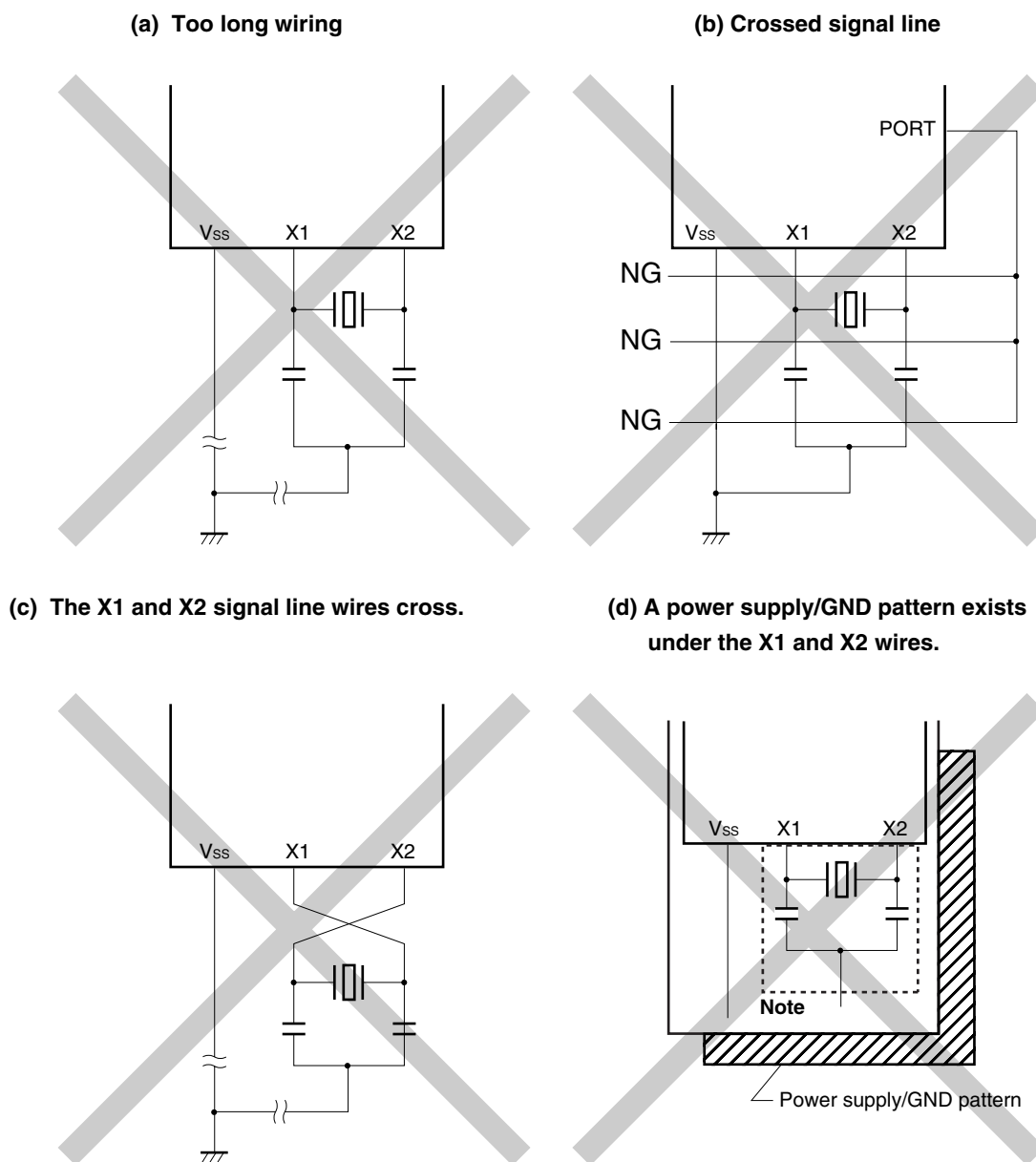
The XT1 oscillator is a circuit with low amplification in order to achieve low-power consumption. Note the following points when designing the circuit.

- Pins and circuit boards include parasitic capacitance. Therefore, perform oscillation evaluation using a circuit board to be actually used and confirm that there are no problems.
- Before using the ultra-low power consumption oscillation (AMP<sub>HS1</sub>, AMP<sub>HS0</sub> = 1, 0) as the mode of the XT1 oscillator, evaluate the resonators.
- Make the wiring between the XT1 and XT2 pins and the resonators as short as possible, and minimize the parasitic capacitance and wiring resistance. Note this particularly when the ultra-low power consumption oscillation (AMP<sub>HS1</sub>, AMP<sub>HS0</sub> = 1, 0) is selected.
- Configure the circuit of the circuit board, using material with little wiring resistance.
- Place a ground pattern that has the same potential as V<sub>SS</sub> as much as possible near the XT1 oscillator.
- Be sure that the signal lines between the XT1 and XT2 pins, and the resonators do not cross with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.
- The impedance between the XT1 and XT2 pins may drop and oscillation may be disturbed due to moisture absorption of the circuit board in a high-humidity environment or dew condensation on the board. When using the circuit board in such an environment, take measures to damp-proof the circuit board, such as by coating.
- When coating the circuit board, use material that does not cause capacitance or leakage between the XT1 and XT2 pins.

&lt;R&gt;

Figure 5-13 shows examples of incorrect resonator connection.

**Figure 5-13. Examples of Incorrect Resonator Connection (1/2)**



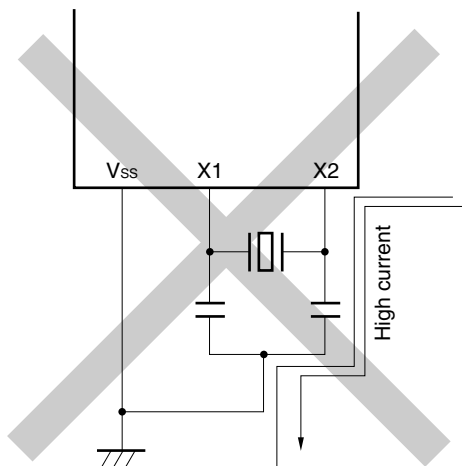
**Note** Do not place a power supply/GND pattern under the wiring section (section indicated by a broken line in the figure) of the X1 and X2 pins and the resonators in a multi-layer board or double-sided board.

Do not configure a layout that will cause capacitance elements and affect the oscillation characteristics.

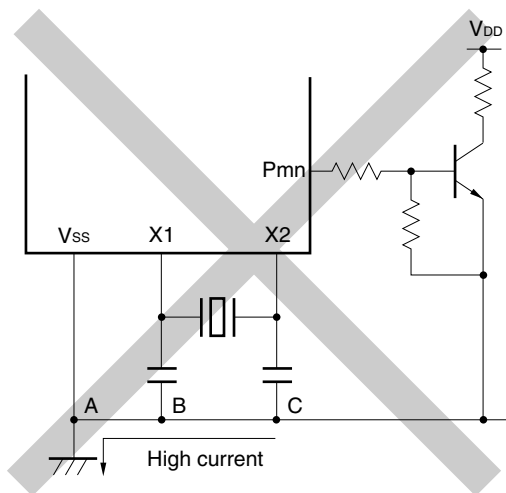
**Remark** When using the subsystem clock, replace X1 and X2 with XT1 and XT2, respectively. Also, insert resistors in series on the XT2 side.

Figure 5-13. Examples of Incorrect Resonator Connection (2/2)

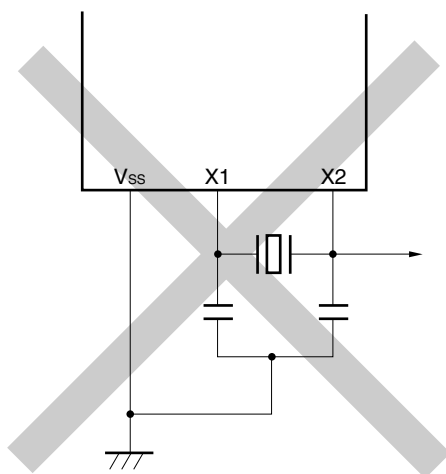
(e) Wiring near high alternating current



(f) Current flowing through ground line of oscillator (potential at points A, B, and C fluctuates)



(g) Signals are fetched



**Caution** When X2 and XT1 are wired in parallel, the crosstalk noise of X2 may increase with XT1, resulting in malfunctioning.

**Remark** When using the subsystem clock, replace X1 and X2 with XT1 and XT2, respectively. Also, insert resistors in series on the XT2 side.

### 5.4.3 High-speed on-chip oscillator

The high-speed on-chip oscillator is incorporated in the RL78/L12. The frequency can be selected from among 24, 16, 12, 8, 4, or 1 MHz by using the option byte (000C2H). Oscillation can be controlled by bit 0 (HIOSTOP) of the clock operation status control register (CSC). The high-speed on-chip oscillator automatically starts oscillating after reset release.

### 5.4.4 Low-speed on-chip oscillator

The low-speed on-chip oscillator is incorporated in the RL78/L12.

The low-speed on-chip oscillator clock is used only as a clock of the watchdog timer, real-time clock, 12-bit interval timer, and LCD driver/controller. The low-speed on-chip oscillation clock cannot be used as the CPU clock.

This clock operates when bit 4 (WDTON) of the option byte (000C0H), bit 4 (WUTMMCK0) of the operation speed mode control register (OSMC), or both are set to 1.

Unless the watchdog timer is stopped and WUTMMCK0 is a value other than zero, oscillation of the low-speed on-chip oscillator continues. While the watchdog timer operates, the low-speed on-chip oscillator does not stop even if the program freezes.



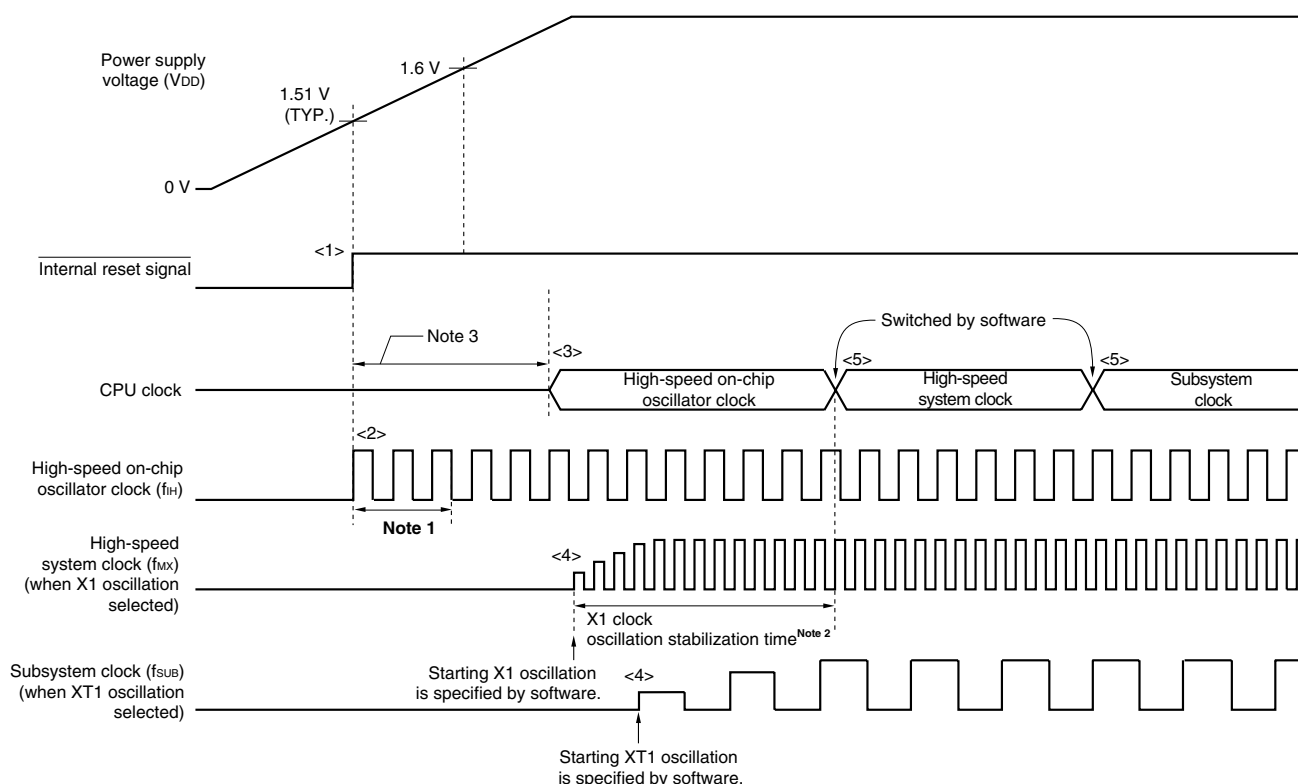
## 5.5 Clock Generator Operation

The clock generator generates the following clocks and controls the operation modes of the CPU, such as standby mode (see **Figure 5-1**).

- Main system clock  $f_{\text{MAIN}}$ 
  - High-speed system clock  $f_{\text{MX}}$ 
    - X1 clock  $f_{\text{X}}$
    - External main system clock  $f_{\text{EX}}$
  - High-speed on-chip oscillator  $f_{\text{IH}}$
- Subsystem clock  $f_{\text{SUB}}$ 
  - XT1 clock  $f_{\text{XT}}$
  - External subsystem clock  $f_{\text{XS}}$
- Low-speed on-chip oscillator clock  $f_{\text{IL}}$
- CPU/peripheral hardware clock  $f_{\text{CLK}}$

The CPU starts operation when the high-speed on-chip oscillator starts outputting after a reset release in the RL78/L12. When the power supply voltage is turned on, the clock generator operation is shown in Figure 5-14.

Figure 5-14. Clock Generator Operation When Power Supply Voltage Is Turned On



- <1> When the power is turned on, an internal reset signal is generated by the power-on-reset (POR) circuit.
- <2> When the power supply voltage exceeds 1.51 V (TYP.), the reset is released and the high-speed on-chip oscillator automatically starts oscillation.
- <3> The CPU starts operation on the high-speed on-chip oscillator clock after a reset processing such as waiting for the voltage of the power supply or regulator to stabilize has been performed after reset release.
- <4> Set the start of oscillation of the X1 or XT1 clock via software (see 5.6.2 Example of setting X1 oscillation clock and 5.6.3 Example of setting XT1 oscillation clock).
- <5> When switching the CPU clock to the X1 or XT1 clock, wait for the clock oscillation to stabilize, and then set switching via software (see 5.6.2 Example of setting X1 oscillation clock and 5.6.3 Example of setting XT1 oscillation clock).

**Notes** 1. The internal reset processing time includes the oscillation accuracy stabilization time of the high-speed on-chip oscillator clock.

2. When releasing a reset, confirm the oscillation stabilization time for the X1 clock using the oscillation stabilization time counter status register (OSTC).

<R> 3. For the reset processing time, see **CHAPTER 21 POWER-ON-RESET CIRCUIT**.

**Caution** It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK pin is used.

## 5.6 Controlling Clock

### 5.6.1 Example of setting high-speed on-chip oscillator

After a reset release, the CPU/peripheral hardware clock ( $f_{CLK}$ ) always starts operating with the high-speed on-chip oscillator clock. The frequency of the high-speed on-chip oscillator can be selected from 24, 16, 12, 8, 4, and 1 MHz by using FRQSEL0 to FRQSEL3 of the option byte (000C2H).

[Option byte setting]

Address: 000C2H

| Option<br>byte<br>(000C2H) | 7      | 6      | 5 | 4 | 3       | 2       | 1       | 0       |
|----------------------------|--------|--------|---|---|---------|---------|---------|---------|
|                            | CMODE1 | CMODE0 |   |   | FRQSEL3 | FRQSEL2 | FRQSEL1 | FRQSEL0 |
|                            | 0/1    | 0/1    | 1 | 0 | 0/1     | 0/1     | 0/1     | 0/1     |

| CMODE1           | CMODE0 | Setting of flash operation mode |                                                                                                                    |
|------------------|--------|---------------------------------|--------------------------------------------------------------------------------------------------------------------|
| 0                | 0      | LV (low voltage main) mode      | $V_{DD} = 1.6\text{ V to }5.5\text{ V@1 MHz to 4 MHz}$                                                             |
| 1                | 0      | LS (low speed main) mode        | $V_{DD} = 1.8\text{ V to }5.5\text{ V@1 MHz to 8 MHz}$                                                             |
| 1                | 1      | HS (high speed main) mode       | $V_{DD} = 2.4\text{ V to }5.5\text{ V@1 MHz to 16 MHz}$<br>$V_{DD} = 2.7\text{ V to }5.5\text{ V@1 MHz to 24 MHz}$ |
| Other than above |        | Setting prohibited              |                                                                                                                    |

| FRQSEL3          | FRQSEL2 | FRQSEL1 | FRQSEL0 | Frequency of the high-speed on-chip oscillator |
|------------------|---------|---------|---------|------------------------------------------------|
| 0                | 0       | 0       | 0       | 24 MHz                                         |
| 1                | 0       | 0       | 1       | 16 MHz                                         |
| 0                | 0       | 0       | 1       | 12 MHz                                         |
| 1                | 0       | 1       | 0       | 8 MHz                                          |
| 1                | 0       | 1       | 1       | 4 MHz                                          |
| 1                | 1       | 0       | 1       | 1 MHz                                          |
| Other than above |         |         |         | Setting prohibited                             |

[High-speed on-chip oscillator frequency select register (HOCODIV) setting]

Address: F00A8H

|         | 7 | 6 | 5 | 4 | 3 | 2        | 1        | 0        |
|---------|---|---|---|---|---|----------|----------|----------|
| HOCODIV | 0 | 0 | 0 | 0 | 0 | HOCODIV2 | HOCODIV1 | HOCODIV0 |

| HOCODIV2         | HOCODIV1 | HOCODIV0 | Selection of high-speed on-chip oscillator clock frequency |                    |
|------------------|----------|----------|------------------------------------------------------------|--------------------|
|                  |          |          | FRQSEL3 Bit is 0                                           | FRQSEL3 Bit is 1   |
| 0                | 0        | 0        | 24 MHz                                                     | Setting prohibited |
| 0                | 0        | 1        | 12 MHz                                                     | 16 MHz             |
| 0                | 1        | 0        | 6 MHz                                                      | 8 MHz              |
| 0                | 1        | 1        | 3 MHz                                                      | 4 MHz              |
| 1                | 0        | 0        | Setting prohibited                                         | 2 MHz              |
| 1                | 0        | 1        | Setting prohibited                                         | 1 MHz              |
| Other than above |          |          | Setting prohibited                                         |                    |

### 5.6.2 Example of setting X1 oscillation clock

After a reset release, the CPU/peripheral hardware clock ( $f_{CLK}$ ) always starts operating with the high-speed on-chip oscillator clock. To subsequently change the clock to the X1 oscillation clock, set the oscillator and start oscillation by using the oscillation stabilization time select register (OSTS), clock operation mode control register (CMC) and clock operation status control register (CSC) and wait for oscillation to stabilize by using the oscillation stabilization time counter status register (OSTC). After the oscillation stabilizes, set the X1 oscillation clock to  $f_{CLK}$  by using the system clock control register (CKC).

[Register settings] Set the register in the order of <1> to <5> below.

- <R> <1> Set (1) the OSCSEL bit of the CMC register, except for the cases where  $f_x > 10$  MHz, in such cases set (1) the AMPH bit, to operate the X1 oscillator.

|     | 7     | 6      | 5      | 4       | 3 | 2      | 1      | 0    |
|-----|-------|--------|--------|---------|---|--------|--------|------|
| CMC | EXCLK | OSCSEL | EXCLKS | OSCSELS |   | AMPHS1 | AMPHS0 | AMPH |
|     | 0     | 1      | 0      | 0       | 0 | 0      | 0      | 0/1  |

AMPH bit: Set this bit to 0 if the X1 oscillation clock is 10 MHz or less.

- <2> Using the OSTS register, select the oscillation stabilization time of the X1 oscillator at releasing of the STOP mode.  
Example: Setting values when a wait of at least 102.4  $\mu$ s is set based on a 10 MHz resonator.

|      | 7 | 6 | 5 | 4 | 3 | 2     | 1     | 0     |
|------|---|---|---|---|---|-------|-------|-------|
| OSTS |   |   |   |   |   | OSTS2 | OSTS1 | OSTS0 |
|      | 0 | 0 | 0 | 0 | 0 | 0     | 1     | 0     |

- <3> Clear (0) the MSTOP bit of the CSC register to start oscillating the X1 oscillator.

|     | 7     | 6      | 5 | 4 | 3 | 2 | 1 | 0       |
|-----|-------|--------|---|---|---|---|---|---------|
| CSC | MSTOP | XTSTOP |   |   |   |   |   | HIOSTOP |
|     | 0     | 1      | 0 | 0 | 0 | 0 | 0 | 0       |

- <4> Use the OSTC register to wait for oscillation of the X1 oscillator to stabilize.

Example: Wait until the bits reach the following values when a wait of at least 102.4  $\mu$ s is set based on a 10 MHz resonator.

|      | 7     | 6     | 5      | 4      | 3      | 2      | 1      | 0      |
|------|-------|-------|--------|--------|--------|--------|--------|--------|
| OSTC | MOST8 | MOST9 | MOST10 | MOST11 | MOST13 | MOST15 | MOST17 | MOST18 |
|      | 1     | 1     | 1      | 0      | 0      | 0      | 0      | 0      |

- <5> Use the MCM0 bit of the CKC register to specify the X1 oscillation clock as the CPU/peripheral hardware clock.

|     | 7   | 6   | 5   | 4    | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|------|---|---|---|---|
| CKC | CLS | CSS | MCS | MCM0 |   |   |   |   |
|     | 0   | 0   | 0   | 1    | 0 | 0 | 0 | 0 |

### 5.6.3 Example of setting XT1 oscillation clock

After a reset release, the CPU/peripheral hardware clock ( $f_{CLK}$ ) always starts operating with the high-speed on-chip oscillator clock. To subsequently change the clock to the XT1 oscillation clock, set the oscillator and start oscillation by using the operation speed mode control register (OSMC), clock operation mode control register (CMC), and clock operation status control register (CSC), set the XT1 oscillation clock to  $f_{CLK}$  by using the system clock control register (CKC).

[Register settings] Set the register in the order of <1> to <5> below.

<1> To run only the real-time clock, 12-bit interval timer, and LCD driver/controller on the subsystem clock (ultra-low current consumption) when in the sub-HALT mode, set the RTCLPC bit to 1.

|      | 7             | 6 | 5 | 4             | 3 | 2 | 1 | 0 |
|------|---------------|---|---|---------------|---|---|---|---|
| OSMC | RTCLPC<br>0/1 | 0 | 0 | WUTMMCK0<br>0 | 0 | 0 | 0 | 0 |

<2> Set (1) the OSCSELS bit of the CMC register to operate the XT1 oscillator.

|     | 7          | 6           | 5           | 4            | 3 | 2             | 1             | 0         |
|-----|------------|-------------|-------------|--------------|---|---------------|---------------|-----------|
| CMC | EXCLK<br>0 | OSCSEL<br>0 | EXCLKS<br>0 | OSCSELS<br>1 | 0 | AMPHS1<br>0/1 | AMPHS0<br>0/1 | AMPH<br>0 |

AMPHS0 and AMPHS1 bits: These bits are used to specify the oscillation mode of the XT1 oscillator.

<3> Clear (0) the XTSTOP bit of the CSC register to start oscillating the XT1 oscillator.

|     | 7          | 6           | 5 | 4 | 3 | 2 | 1 | 0            |
|-----|------------|-------------|---|---|---|---|---|--------------|
| CSC | MSTOP<br>1 | XTSTOP<br>0 | 0 | 0 | 0 | 0 | 0 | HIOSTOP<br>0 |

<4> Use the timer function or another function to wait for oscillation of the subsystem clock to stabilize by using software.

<5> Use the CSS bit of the CKC register to specify the XT1 oscillation clock as the CPU/peripheral hardware clock.

|     | 7        | 6        | 5        | 4         | 3 | 2 | 1 | 0 |
|-----|----------|----------|----------|-----------|---|---|---|---|
| CKC | CLS<br>0 | CSS<br>1 | MCS<br>0 | MCM0<br>0 | 0 | 0 | 0 | 0 |

## 5.6.4 CPU clock status transition diagram

Figure 5-15 shows the CPU clock status transition diagram of this product.

<R>

Figure 5-15. CPU Clock Status Transition Diagram

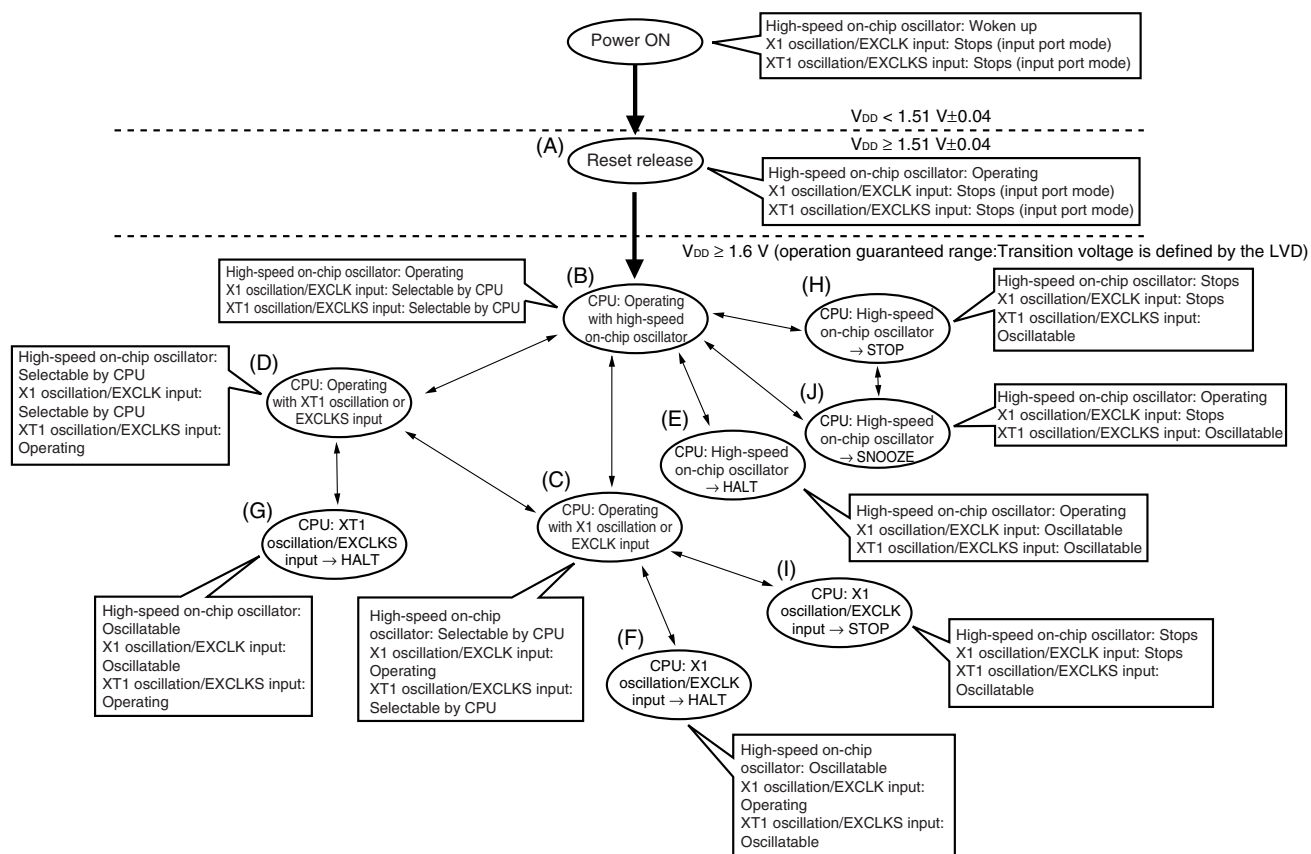


Table 5-3 shows transition of the CPU clock and examples of setting the SFR registers.

**Table 5-3. CPU Clock Transition and SFR Register Setting Examples (1/5)**

**(1) CPU operating with high-speed on-chip oscillator clock (B) after reset release (A)**

| Status Transition | SFR Register Setting                                                      |
|-------------------|---------------------------------------------------------------------------|
| (A) → (B)         | SFR registers do not have to be set (default status after reset release). |

**<R> (2) CPU operating with high-speed system clock (C) after reset release (A)**

(The CPU operates with the high-speed on-chip oscillator clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

| Setting Flag of SFR Register<br>Status Transition               | CMC Register <sup>Note</sup> |        |      | OSTS Register | CSC Register | OSTC Register       | CKC Register |
|-----------------------------------------------------------------|------------------------------|--------|------|---------------|--------------|---------------------|--------------|
|                                                                 | EXCLK                        | OSCSEL | AMPH |               | MSTOP        |                     | MCM0         |
| (A) → (B) → (C)<br>(X1 clock: 1 MHz ≤ f <sub>x</sub> ≤ 10 MHz)  | 0                            | 1      | 0    | <b>Note 2</b> | 0            | Must be checked     | 1            |
| (A) → (B) → (C)<br>(X1 clock: 10 MHz < f <sub>x</sub> ≤ 20 MHz) | 0                            | 1      | 1    | <b>Note 2</b> | 0            | Must be checked     | 1            |
| (A) → (B) → (C)<br>(external main clock)                        | 1                            | 1      | ×    | <b>Note 2</b> | 0            | Must not be checked | 1            |

**Notes 1.** The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release.

**2.** Set the oscillation stabilization time as follows.

- Desired the oscillation stabilization time counter status register (OSTC) oscillation stabilization time ≤ Oscillation stabilization time set by the oscillation stabilization time select register (OSTS)

**Caution** Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 30 ELECTRICAL SPECIFICATIONS).

**(3) CPU operating with subsystem clock (D) after reset release (A)**

(The CPU operates with the high-speed on-chip oscillator clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

| Setting Flag of SFR Register<br>Status Transition | CMC Register <sup>Note</sup> |         |        |        | CSC Register | Waiting for Oscillation Stabilization | CKC Register |
|---------------------------------------------------|------------------------------|---------|--------|--------|--------------|---------------------------------------|--------------|
|                                                   | EXCLKS                       | OSCSELS | AMPHS1 | AMPHS0 | XTSTOP       |                                       | CSS          |
| (A) → (B) → (D)<br>(XT1 clock)                    | 0                            | 1       | 0/1    | 0/1    | 0            | Necessary                             | 1            |
| (A) → (B) → (D)<br>(external sub clock)           | 1                            | 1       | ×      | ×      | 0            | Necessary                             | 1            |

**Note** The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release.

**Remarks 1.** ×: don't care

**2.** (A) to (J) in Table 5-3 correspond to (A) to (J) in Figure 5-15.

Table 5-3. CPU Clock Transition and SFR Register Setting Examples (2/5)

## (4) CPU clock changing from high-speed on-chip oscillator clock (B) to high-speed system clock (C)

(Setting sequence of SFR registers) →

| Setting Flag of SFR Register<br>Status Transition | CMC Register <sup>Note 1</sup> |        |      | OSTS Register | CSC Register | OSTC Register       | CKC Register |
|---------------------------------------------------|--------------------------------|--------|------|---------------|--------------|---------------------|--------------|
|                                                   | EXCLK                          | OSCSEL | AMPH |               | MSTOP        |                     |              |
| (B) → (C)<br>(X1 clock: 1 MHz ≤ fX ≤ 10 MHz)      | 0                              | 1      | 0    | <b>Note 2</b> | 0            | Must be checked     | 1            |
| (B) → (C)<br>(X1 clock: 10 MHz < fX ≤ 20 MHz)     | 0                              | 1      | 1    | <b>Note 2</b> | 0            | Must be checked     | 1            |
| (B) → (C)<br>(external main clock)                | 1                              | 1      | ×    | <b>Note 2</b> | 0            | Must not be checked | 1            |

Unnecessary if these registers are already set      Unnecessary if the CPU is operating with the high-speed system clock

**Notes** 1. The clock operation mode control register (CMC) can be changed only once after reset release. This setting is not necessary if it has already been set.

2. Set the oscillation stabilization time as follows.

- Desired the oscillation stabilization time counter status register (OSTC) oscillation stabilization time ≤ Oscillation stabilization time set by the oscillation stabilization time select register (OSTS)

**Caution** Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 30 ELECTRICAL SPECIFICATIONS).

## (5) CPU clock changing from high-speed on-chip oscillator clock (B) to subsystem clock (D)

(Setting sequence of SFR registers) →

| Setting Flag of SFR Register<br>Status Transition | CMC Register <sup>Note</sup> |         | CSC Register | Waiting for Oscillation Stabilization | CKC Register |
|---------------------------------------------------|------------------------------|---------|--------------|---------------------------------------|--------------|
|                                                   | EXCLKS                       | OSCSELS | XTSTOP       |                                       | CSS          |
| (B) → (D)<br>(XT1 clock)                          | 0                            | 1       | 0            | Necessary                             | 1            |
| (B) → (D)<br>(external sub clock)                 | 1                            | 1       | 0            | Necessary                             | 1            |

Unnecessary if the CPU is operating with the subsystem clock

**Note** The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release.

**Remarks** 1. ×: don't care

2. (A) to (J) in Table 5-3 correspond to (A) to (J) in Figure 5-15.



Table 5-3. CPU Clock Transition and SFR Register Setting Examples (3/5)

## (6) CPU clock changing from high-speed system clock (C) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFR registers) →

| Setting Flag of SFR Register<br>Status Transition | CSC Register | Oscillation accuracy<br>stabilization time | CKC Register |
|---------------------------------------------------|--------------|--------------------------------------------|--------------|
|                                                   | HIOSTOP      |                                            | MCM0         |
| (C) → (B)                                         | 0            | 30 $\mu$ s                                 | 0            |

Unnecessary if the CPU is operating with the  
high-speed on-chip oscillator clock

## (7) CPU clock changing from high-speed system clock (C) to subsystem clock (D)

(Setting sequence of SFR registers) →

| Setting Flag of SFR Register<br>Status Transition | CSC Register | Waiting for Oscillation<br>Stabilization | CKC Register |
|---------------------------------------------------|--------------|------------------------------------------|--------------|
|                                                   | XTSTOP       |                                          | CSS          |
| (C) → (D)                                         | 0            | Necessary                                | 1            |

Unnecessary if the CPU is operating with the  
subsystem clock

## (8) CPU clock changing from subsystem clock (D) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFR registers) →

| Setting Flag of SFR Register<br>Status Transition | CSC Register | CKC Register |      |
|---------------------------------------------------|--------------|--------------|------|
|                                                   | HIOSTOP      | CSS          | MCM0 |
| (D) → (B)                                         | 0            | 0            | 0    |

Unnecessary if the CPU  
is operating with the  
high-speed on-chip  
oscillator clock

Unnecessary if this  
register is already set

**Remark** (A) to (J) in Table 5-3 correspond to (A) to (J) in Figure 5-15.

Table 5-3. CPU Clock Transition and SFR Register Setting Examples (4/5)

## (9) CPU clock changing from subsystem clock (D) to high-speed system clock (C)

(Setting sequence of SFR registers) 

| Setting Flag of SFR Register<br>Status Transition      | OSTS Register | CSC Register | OSTC Register       | CKC Register |      |
|--------------------------------------------------------|---------------|--------------|---------------------|--------------|------|
|                                                        |               | MSTOP        |                     | CSS          | MCM0 |
| (D) → (C) (X1 clock: 1 MHz ≤ f <sub>x</sub> ≤ 10 MHz)  | <b>Note</b>   | 0            | Must be checked     | 0            | 1    |
| (D) → (C) (X1 clock: 10 MHz < f <sub>x</sub> ≤ 20 MHz) | <b>Note</b>   | 0            | Must be checked     | 0            | 1    |
| (D) → (C) (external main clock)                        | <b>Note</b>   | 0            | Must not be checked | 0            | 1    |


 Unnecessary if the CPU is operating with the high-speed system clock
 
 Unnecessary if these registers are already set

**Note** Set the oscillation stabilization time as follows.

- Desired the oscillation stabilization time counter status register (OSTC) oscillation stabilization time ≤ Oscillation stabilization time set by the oscillation stabilization time select register (OSTS)

**Caution** Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 30 ELECTRICAL SPECIFICATIONS).

## (10) • HALT mode (E) set while CPU is operating with high-speed on-chip oscillator clock (B)

- HALT mode (F) set while CPU is operating with high-speed system clock (C)
- HALT mode (G) set while CPU is operating with subsystem clock (D)

| Status Transition                   | Setting                    |
|-------------------------------------|----------------------------|
| (B) → (E)<br>(C) → (F)<br>(D) → (G) | Executing HALT instruction |

**Remark** (A) to (J) in Table 5-3 correspond to (A) to (J) in Figure 5-15.

Table 5-3. CPU Clock Transition and SFR Register Setting Examples (5/5)

- (11) • STOP mode (H) set while CPU is operating with high-speed on-chip oscillator clock (B)  
 • STOP mode (I) set while CPU is operating with high-speed system clock (C)

(Setting sequence) →

| Status Transition |                            | Setting                                                        |                        |                            |
|-------------------|----------------------------|----------------------------------------------------------------|------------------------|----------------------------|
| (B) → (H)         |                            | Stopping peripheral functions that cannot operate in STOP mode | –                      | Executing STOP instruction |
| (C) → (I)         | In X1 oscillation          |                                                                | Sets the OSTS register |                            |
|                   | External main system clock |                                                                | –                      |                            |

(12) CPU changing from STOP mode (H) to SNOOZE mode (J)

For details about the setting for switching from the STOP mode to the SNOOZE mode, see **11.8 SNOOZE Mode Function**, **12.5.7 SNOOZE mode function** and **12.6.3 SNOOZE mode function**.

**Remark** (A) to (J) in Table 5-3 correspond to (A) to (J) in Figure 5-15.

### 5.6.5 Condition before changing CPU clock and processing after changing CPU clock

Condition before changing the CPU clock and processing after changing the CPU clock are shown below.

**Table 5-4. Changing CPU Clock (1/2)**

| CPU Clock                           |                                     | Condition Before Change                                                                                                       | Processing After Change                                                                   |
|-------------------------------------|-------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|
| Before Change                       | After Change                        |                                                                                                                               |                                                                                           |
| High-speed on-chip oscillator clock | X1 clock                            | Stabilization of X1 oscillation<br>• OSCSEL = 1, EXCLK = 0, MSTOP = 0<br>• After elapse of oscillation stabilization time     | Operating current can be reduced by stopping high-speed on-chip oscillator (HIOSTOP = 1). |
|                                     | External main system clock          | Enabling input of external clock from the EXCLK pin<br>• OSCSEL = 1, EXCLK = 1, MSTOP = 0                                     |                                                                                           |
|                                     | XT1 clock                           | Stabilization of XT1 oscillation<br>• OSCSELS = 1, EXCLKS = 0, XTSTOP = 0<br>• After elapse of oscillation stabilization time |                                                                                           |
|                                     | External subsystem clock            | Enabling input of external clock from the EXCLKS pin<br>• OSCSELS = 1, EXCLKS = 1, XTSTOP = 0                                 |                                                                                           |
| <R> X1 clock                        | High-speed on-chip oscillator clock | Oscillation of high-speed on-chip oscillator<br>• HIOSTOP = 0<br>• After elapse of oscillation accuracy stabilization time    | X1 oscillation can be stopped (MSTOP = 1).                                                |
|                                     | External main system clock          | Transition not possible<br>(To change the clock, set it again after executing reset once.)                                    | —                                                                                         |
|                                     | XT1 clock                           | Stabilization of XT1 oscillation<br>• OSCSELS = 1, EXCLKS = 0, XTSTOP = 0<br>• After elapse of oscillation stabilization time | X1 oscillation can be stopped (MSTOP = 1).                                                |
|                                     | External subsystem clock            | Enabling input of external clock from the EXCLKS pin<br>• OSCSELS = 1, EXCLKS = 1, XTSTOP = 0                                 | X1 oscillation can be stopped (MSTOP = 1).                                                |
| <R> External main system clock      | High-speed on-chip oscillator clock | Oscillation of high-speed on-chip oscillator<br>• HIOSTOP = 0<br>• After elapse of oscillation accuracy stabilization time    | External main system clock input can be disabled (MSTOP = 1).                             |
|                                     | X1 clock                            | Transition not possible<br>(To change the clock, set it again after executing reset once.)                                    | —                                                                                         |
|                                     | XT1 clock                           | Stabilization of XT1 oscillation<br>• OSCSELS = 1, EXCLKS = 0, XTSTOP = 0<br>• After elapse of oscillation stabilization time | External main system clock input can be disabled (MSTOP = 1).                             |
|                                     | External subsystem clock            | Enabling input of external clock from the EXCLKS pin<br>• OSCSELS = 1, EXCLKS = 1, XTSTOP = 0                                 | External main system clock input can be disabled (MSTOP = 1).                             |

Table 5-4. Changing CPU Clock (2/2)

| CPU Clock                    |                                     | Condition Before Change                                                                                                                                                                              | Processing After Change                                      |
|------------------------------|-------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|
| Before Change                | After Change                        |                                                                                                                                                                                                      |                                                              |
| <R> XT1 clock                | High-speed on-chip oscillator clock | Oscillation of high-speed on-chip oscillator and selection of high-speed on-chip oscillator clock as main system clock<br>• HIOSTOP = 0, MCS = 0                                                     | XT1 oscillation can be stopped (XTSTOP = 1)                  |
|                              | X1 clock                            | Stabilization of X1 oscillation and selection of high-speed system clock as main system clock<br>• OSCSEL = 1, EXCLK = 0, MSTOP = 0<br>• After elapse of oscillation stabilization time<br>• MCS = 1 |                                                              |
|                              | External main system clock          | Enabling input of external clock from the EXCLK pin and selection of high-speed system clock as main system clock<br>• OSCSEL = 1, EXCLK = 1, MSTOP = 0<br>• MCS = 1                                 |                                                              |
|                              | High-speed on-chip oscillator clock | Transition not possible                                                                                                                                                                              | —                                                            |
| <R> External subsystem clock | High-speed on-chip oscillator clock | Oscillation of high-speed on-chip oscillator and selection of high-speed on-chip oscillator clock as main system clock<br>• HIOSTOP = 0, MCS = 0                                                     | External subsystem clock input can be disabled (XTSTOP = 1). |
|                              | X1 clock                            | Stabilization of X1 oscillation and selection of high-speed system clock as main system clock<br>• OSCSEL = 1, EXCLK = 0, MSTOP = 0<br>• After elapse of oscillation stabilization time<br>• MCS = 1 |                                                              |
|                              | External main system clock          | Enabling input of external clock from the EXCLK pin and selection of high-speed system clock as main system clock<br>• OSCSEL = 1, EXCLK = 1, MSTOP = 0<br>• MCS = 1                                 |                                                              |
|                              | XT1 clock                           | Transition not possible                                                                                                                                                                              | —                                                            |

### 5.6.6 Time required for switchover of CPU clock and system clock

By setting bits 4 and 6 (MCM0, CSS) of the system clock control register (CKC), the CPU clock can be switched (between the main system clock and the subsystem clock), and main system clock can be switched (between the high-speed on-chip oscillator clock and the high-speed system clock).

The actual switchover operation is not performed immediately after rewriting to the CKC register; operation continues on the pre-switchover clock for several clocks (see Table 5-5 to Table 5-7).

Whether the CPU is operating on the main system clock or the subsystem clock can be ascertained using bit 7 (CLS) of the CKC register. Whether the main system clock is operating on the high-speed system clock or high-speed on-chip oscillator clock can be ascertained using bit 5 (MCS) of the CKC register.

When the CPU clock is switched, the peripheral hardware clock is also switched.

**Table 5-5. Maximum Time Required for System Clock Switchover**

| Clock A    | Switching directions  | Clock B   | Remark        |
|------------|-----------------------|-----------|---------------|
| $f_{IH}$   | $\longleftrightarrow$ | $f_{MX}$  | See Table 5-6 |
| $f_{MAIN}$ | $\longleftrightarrow$ | $f_{SUB}$ | See Table 5-7 |

**Table 5-6. Maximum Number of Clocks Required for  $f_{IH} \leftrightarrow f_{MX}$**

| Set Value Before Switchover  |                      | Set Value After Switchover   |                              |
|------------------------------|----------------------|------------------------------|------------------------------|
| MCM0                         |                      | MCM0                         |                              |
|                              |                      | 0<br>( $f_{MAIN} = f_{IH}$ ) | 1<br>( $f_{MAIN} = f_{MX}$ ) |
| 0<br>( $f_{MAIN} = f_{IH}$ ) | $f_{MX} \geq f_{IH}$ |                              | 2 clock                      |
|                              | $f_{MX} < f_{IH}$    |                              | $2f_{IH}/f_{MX}$ clock       |
| 1<br>( $f_{MAIN} = f_{MX}$ ) | $f_{MX} \geq f_{IH}$ | $2f_{MX}/f_{IH}$ clock       |                              |
|                              | $f_{MX} < f_{IH}$    | 2 clock                      |                              |

**Table 5-7. Maximum Number of Clocks Required for  $f_{MAIN} \leftrightarrow f_{SUB}$**

| Set Value Before Switchover   |  | Set Value After Switchover    |                               |
|-------------------------------|--|-------------------------------|-------------------------------|
| CSS                           |  | CSS                           |                               |
|                               |  | 0<br>( $f_{CLK} = f_{MAIN}$ ) | 1<br>( $f_{CLK} = f_{SUB}$ )  |
| 0<br>( $f_{CLK} = f_{MAIN}$ ) |  |                               | $1 + 2f_{MAIN}/f_{SUB}$ clock |
| 1<br>( $f_{CLK} = f_{SUB}$ )  |  | 3 clock                       |                               |

- Remarks**
1. The number of clocks listed in Table 5-6 to Table 5-7 is the number of CPU clocks before switchover.
  2. Calculate the number of clocks in Table 5-6 to Table 5-7 by removing the decimal portion.

**Example** When switching the main system clock from the high-speed system clock to the high-speed on-chip oscillator clock (@ oscillation with  $f_{IH} = 8$  MHz,  $f_{MX} = 10$  MHz)

<R>  $2f_{MX}/f_{IH} = 2 (10/8) = 2.5 \rightarrow 3$  clocks

### 5.6.7 Conditions before clock oscillation is stopped

The following lists the register flag settings for stopping the clock oscillation (disabling external clock input) and conditions before the clock oscillation is stopped.

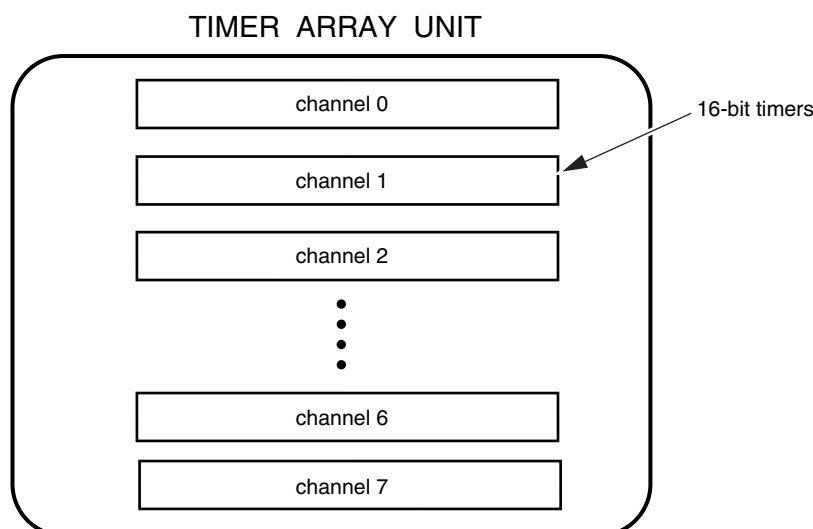
**Table 5-8. Conditions Before the Clock Oscillation Is Stopped and Flag Settings**

| Clock                               | Conditions Before Clock Oscillation Is Stopped<br>(External Clock Input Disabled)                           | Flag Settings of SFR<br>Register |
|-------------------------------------|-------------------------------------------------------------------------------------------------------------|----------------------------------|
| High-speed on-chip oscillator clock | MCS = 1 or CLS = 1<br>(The CPU is operating on a clock other than the high-speed on-chip oscillator clock.) | HIOSTOP = 1                      |
| X1 clock                            | MCS = 0 or CLS = 1<br>(The CPU is operating on a clock other than the high-speed system clock.)             | MSTOP = 1                        |
| External main system clock          |                                                                                                             |                                  |
| XT1 clock                           | CLS = 0<br>(The CPU is operating on a clock other than the subsystem clock.)                                | XTSTOP = 1                       |
| External subsystem clock            |                                                                                                             |                                  |

## CHAPTER 6 TIMER ARRAY UNIT

The timer array unit has eight 16-bit timers.

Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more “channels” can be used to create a high-accuracy timer.



- Cautions**
1. The presence or absence of timer I/O pins depends on the product. See Table 6-2 Timer I/O Pins Provided in Each Product for details.
  2. Most of the following descriptions in this chapter use the 64-pin products as an example.

For details about each function, see the table below.

| Independent channel operation function                                                                                                                                                                                                                                                                                                                                                                                                            | Simultaneous channel operation function                                                                                                                                                                                                                             |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <ul style="list-style-type: none"> <li>• Interval timer (→ refer to 6.7.1)</li> <li>• Square wave output (→ refer to 6.7.1)</li> <li>• External event counter (→ refer to 6.7.2)</li> <li>• Divider <sup>Note 1</sup> (→ refer to 6.7.3)</li> <li>• Input pulse interval measurement (→ refer to 6.7.4)</li> <li>• Measurement of high-/low-level width of input signal (→ refer to 6.7.5)</li> <li>• Delay counter (→ refer to 6.7.6)</li> </ul> | <ul style="list-style-type: none"> <li>• One-shot pulse output(→ refer to 6.8.1)</li> <li>• PWM output(→ refer to 6.8.2)</li> <li>• Multiple PWM output(→ refer to 6.8.3)</li> <li>• Remote control output function <sup>Note 2</sup> (→ refer to 6.8.4)</li> </ul> |

- Notes**
1. Only channel 0.
  2. 44, 48, 52, 64-pin products only.

It is possible to use the 16-bit timer of channels 1 and 3 as two 8-bit timers (higher and lower). The functions that can use channels 1 and 3 as 8-bit timers are as follows:

- Interval timer/square wave output
- External event counter (lower 8-bit timer only)
- Delay counter (lower 8-bit timer only)

Channel 5 can be used to realize LIN-bus communication operating in combination with UART0 of the serial array unit.



## 6.1 Functions of Timer Array Unit

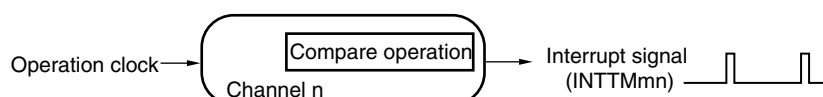
Timer array unit has the following functions.

### 6.1.1 Independent channel operation function

By operating a channel independently, it can be used for the following purposes without being affected by the operation mode of other channels.

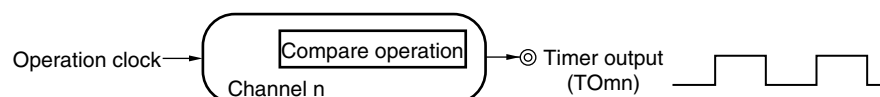
#### (1) Interval timer

Each timer of a unit can be used as a reference timer that generates an interrupt (INTTMmn) at fixed intervals.



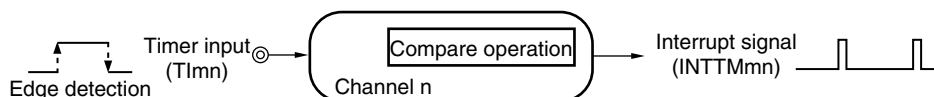
#### (2) Square wave output

A toggle operation is performed each time INTTMmn interrupt is generated and a square wave with a duty factor of 50% is output from a timer output pin (TOMn).



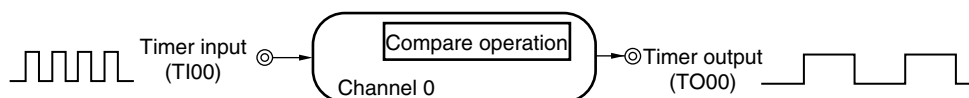
#### (3) External event counter

Each timer of a unit can be used as an event counter that generates an interrupt when the number of the valid edges of a signal input to the timer input pin (TIMn) has reached a specific value.



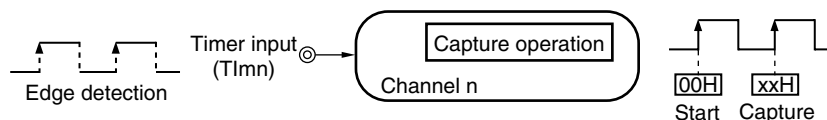
#### (4) Divider function (channel 0 only)

A clock input from a timer input pin (TI00) is divided and output from an output pin (TO00).



#### (5) Input pulse interval measurement

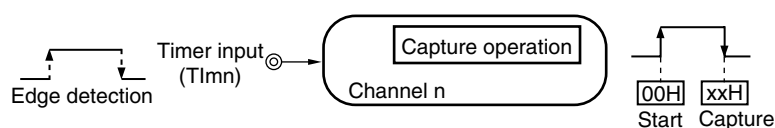
Counting is started by the valid edge of a pulse signal input to a timer input pin (TIMn). The count value of the timer is captured at the valid edge of the next pulse. In this way, the interval of the input pulse can be measured.



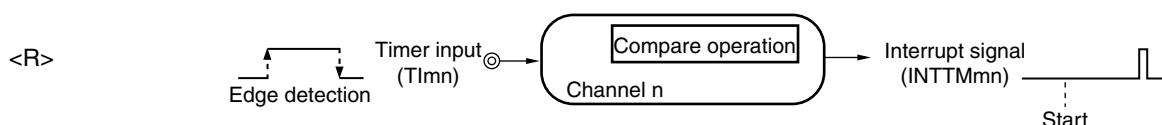
(Note, Caution, and Remark are listed on the next page.)

**(6) Measurement of high-/low-level width of input signal**

Counting is started by a single edge of the signal input to the timer input pin (TImn), and the count value is captured at the other edge. In this way, the high-level or low-level width of the input signal can be measured.

**(7) Delay counter**

Counting is started at the valid edge of the signal input to the timer input pin (TImn), and an interrupt is generated after any delay period.



**Remarks 1** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

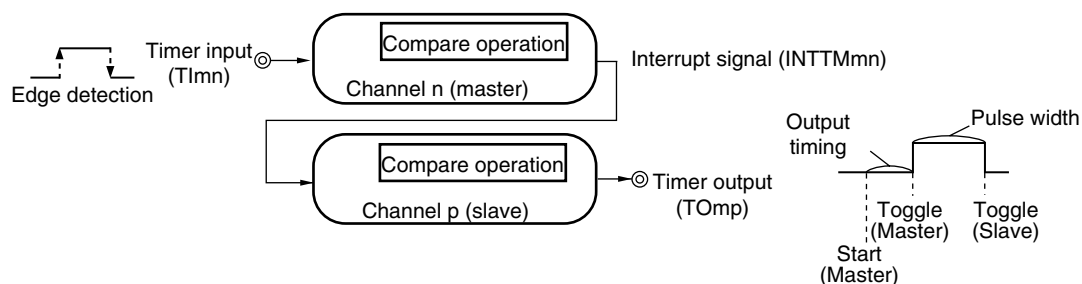
**2.** The presence or absence of timer I/O pins of channel 0 to 7 depends on the product. See **Table 6-2 Timer I/O Pins provided in Each Product** for details.

**6.1.2 Simultaneous channel operation function**

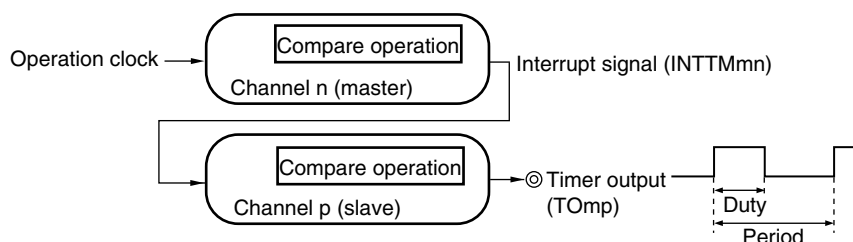
By using the combination of a master channel (a reference timer mainly controlling the cycle) and slave channels (timers operating according to the master channel), channels can be used for the following purposes.

**(1) One-shot pulse output**

Two channels are used as a set to generate a one-shot pulse with a specified output timing and a specified pulse width.

**(2) PWM (Pulse Width Modulation) output**

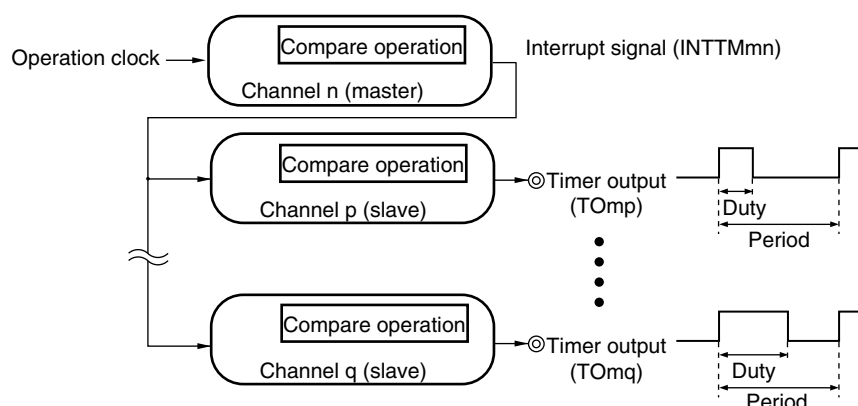
Two channels are used as a set to generate a pulse with a specified period and a specified duty factor.



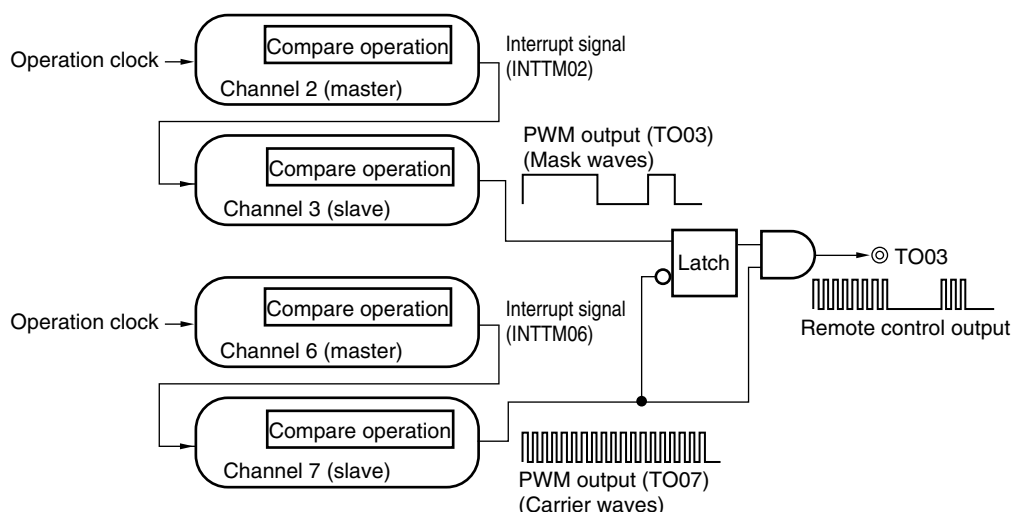
(Caution is listed on the next page.)

**(3) Multiple PWM (Pulse Width Modulation) output**

By extending the PWM function and using one master channel and two or more slave channels, up to seven types of PWM signals that have a specific period and a specified duty factor can be generated.

**(4) Remote control output function**

The pairings of channels 2 and 3 and channels 6 and 7 are used to output the PWM signal. The PWM signal output from channel 3 is used as a mask waves, the PWM signal output from channel 7 is used as a carrier waves, and the logical products of these signals are output as remote control output.



<R> **Caution** For details about the rules of simultaneous channel operation function, see 6.4.1 Basic rules of simultaneous channel operation function.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7),  
p, q: Slave channel number (n < p < q ≤ 7)

### 6.1.3 8-bit timer operation function (channels 1 and 3 only)

The 8-bit timer operation function makes it possible to use a 16-bit timer channel in a configuration consisting of two 8-bit timer channels. This function can only be used for channels 1 and 3.

**Caution** There are several rules for using 8-bit timer operation function.

For details, see 6.4.2 Basic rules of 8-bit timer operation function (channels 1 and 3 only).

### 6.1.4 LIN-bus supporting function (channel 5 only)

Timer array unit is used to check whether signals received in LIN-bus communication match the LIN-bus communication format.

#### (1) Detection of wakeup signal

The timer starts counting at the falling edge of a signal input to the serial data input pin (RxD0) of UART0 and the count value of the timer is captured at the rising edge. In this way, a low-level width can be measured. If the low-level width is greater than a specific value, it is recognized as a wakeup signal.

#### (2) Detection of break field

The timer starts counting at the falling edge of a signal input to the serial data input pin (RxD0) of UART0 after a wakeup signal is detected, and the count value of the timer is captured at the rising edge. In this way, a low-level width is measured. If the low-level width is greater than a specific value, it is recognized as a break field.

#### (3) Measurement of pulse width of sync field

After a break field is detected, the low-level width and high-level width of the signal input to the serial data input pin (RxD0) of UART0 are measured. From the bit interval of the sync field measured in this way, a baud rate is calculated.

**Remark** For details about setting up the operations used to implement the LIN-bus, see 6.3.14 Input switch control register (ISC) and 6.7.5 Operation as input signal high-/low-level width measurement.

## 6.2 Configuration of Timer Array Unit

Timer array unit includes the following hardware.

**Table 6-1. Configuration of Timer Array Unit**

| Item              | Configuration                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Timer/counter     | Timer count register mn (TCRmn)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Register          | Timer data register mn (TDRmn)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| Timer input       | TI00 to TI07 <sup>Note 1</sup> , RxD0 pin (for LIN-bus)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| Timer output      | TO00 to TO07 <sup>Note 1</sup> , output controller                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| Control registers | <div> &lt;Registers of unit setting block&gt; <ul style="list-style-type: none"> <li>• Peripheral enable register 0 (PER0)</li> <li>• Timer clock select register m (TPSm)</li> <li>• Timer channel enable status register m (TEm)</li> <li>• Timer channel start register m (TSM)</li> <li>• Timer channel stop register m (TTm)</li> <li>• Timer input select register 0 (TIS0)</li> <li>• Timer output select register (TOS)</li> <li>• Timer output enable register m (TOEm)</li> <li>• Timer output register m (TOM)</li> <li>• Timer output level register m (TOLm)</li> <li>• Timer output mode register m (TOMm)</li> </ul> </div> <div> &lt;Registers of each channel&gt; <ul style="list-style-type: none"> <li>• Timer mode register mn (TMRmn)</li> <li>• Timer status register mn (TSRmn)</li> <li>• Input switch control register (ISC)</li> <li>• Noise filter enable register 1 (NFEN1)</li> <li>• Port mode control register (PMCxx)<sup>Note 2</sup></li> <li>• Port mode register (PMxx)<sup>Note 2</sup></li> <li>• Port register (Pxx)<sup>Note 2</sup></li> </ul> </div> |

**Notes** 1. The presence or absence of timer I/O pins of channel 0 to 7 depends on the product. See **Table 6-2 Timer I/O Pins provided in Each Product** for details.

2. The Port mode control register (PMCxx), port mode registers (PMxx) and port registers (Pxx) to be set differ depending on the product. For details, see **6.3.16 Port mode registers 1, 3 to 5, 14 (PM1, PM3 to PM5, PM14)**.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

The presence or absence of timer I/O pins in each timer array unit channel depends on the product.

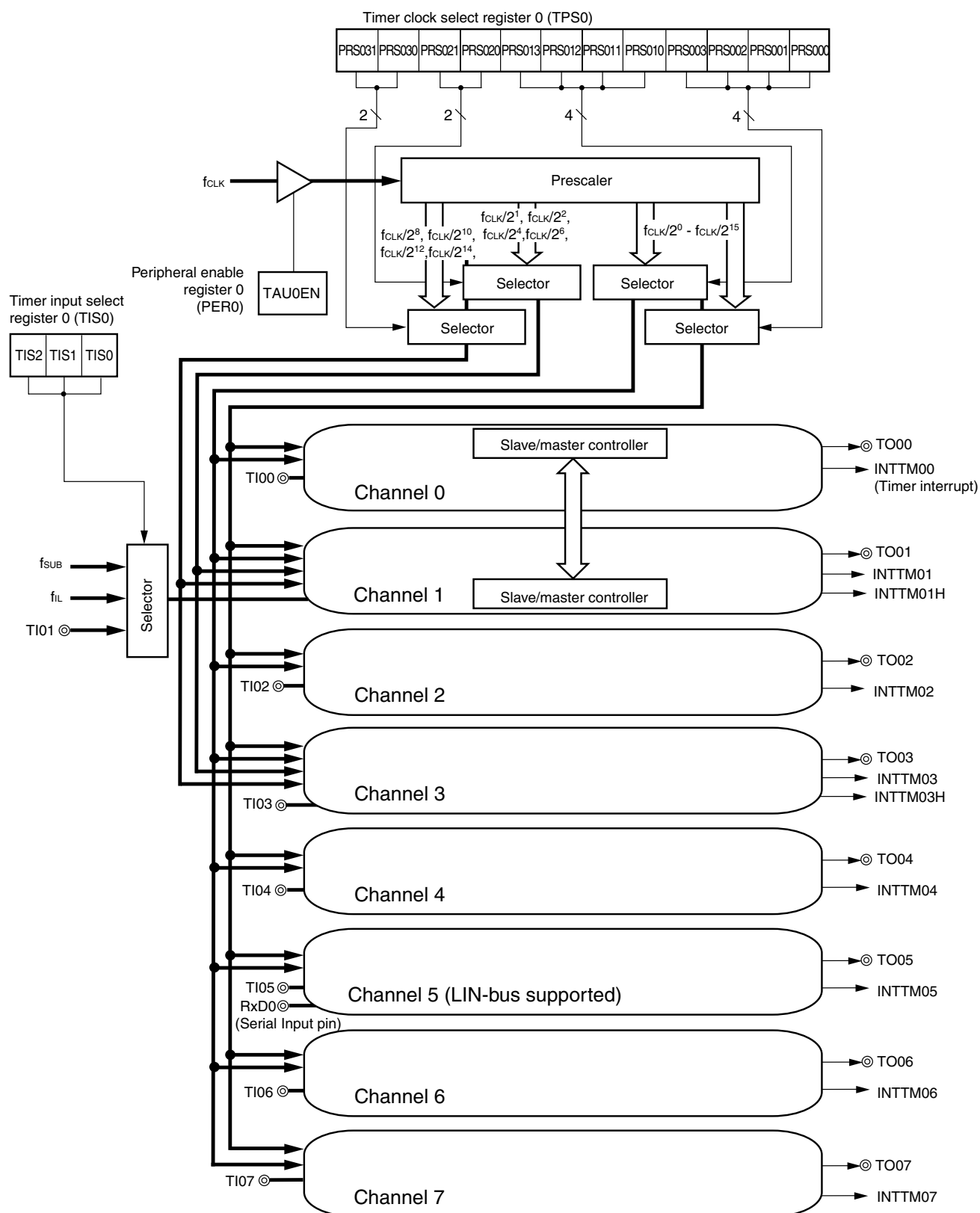
**Table 6-2. Timer I/O Pins Provided in Each Product**

| Timer array unit<br>channels | I/O Pins of Each Product |                      |               |               |                        |
|------------------------------|--------------------------|----------------------|---------------|---------------|------------------------|
|                              | 32-pin                   | 44-pin               | 48-pin        | 52-pin        | 64-pin                 |
| Channel 0                    | P13/TI00,<br>P140/TO00   | P141/TI00, P140/TO00 |               |               |                        |
| Channel 1                    | P30/TI01/TO01            |                      |               |               |                        |
| Channel 2                    | P17/TI02/TO02<br>(P12)   |                      |               |               | P17/TI02/TO02<br>(P54) |
| Channel 3                    | –                        | P32/TI03/TO03        |               |               |                        |
| Channel 4                    | –                        | –                    | P41/TI04/TO04 |               |                        |
| Channel 5                    | –                        | –                    | –             | P42/TI05/TO05 |                        |
| Channel 6                    | –                        | –                    | –             | P51/TI06/TO06 |                        |
| Channel 7                    | P10/TI07/TO07            |                      |               |               | P53/TI07/TO07          |

- Remarks**
1. When timer input and timer output are shared by the same pin, either only timer input or only timer output can be used.
  2. –: There is no timer I/O pin, but the channel is available. (However, the channel can only be used as an interval timer.)
  3. “(P12), (P54)” indicates an alternate port when the bit 0 of the peripheral I/O redirection register (PIOR) is set to “1”.

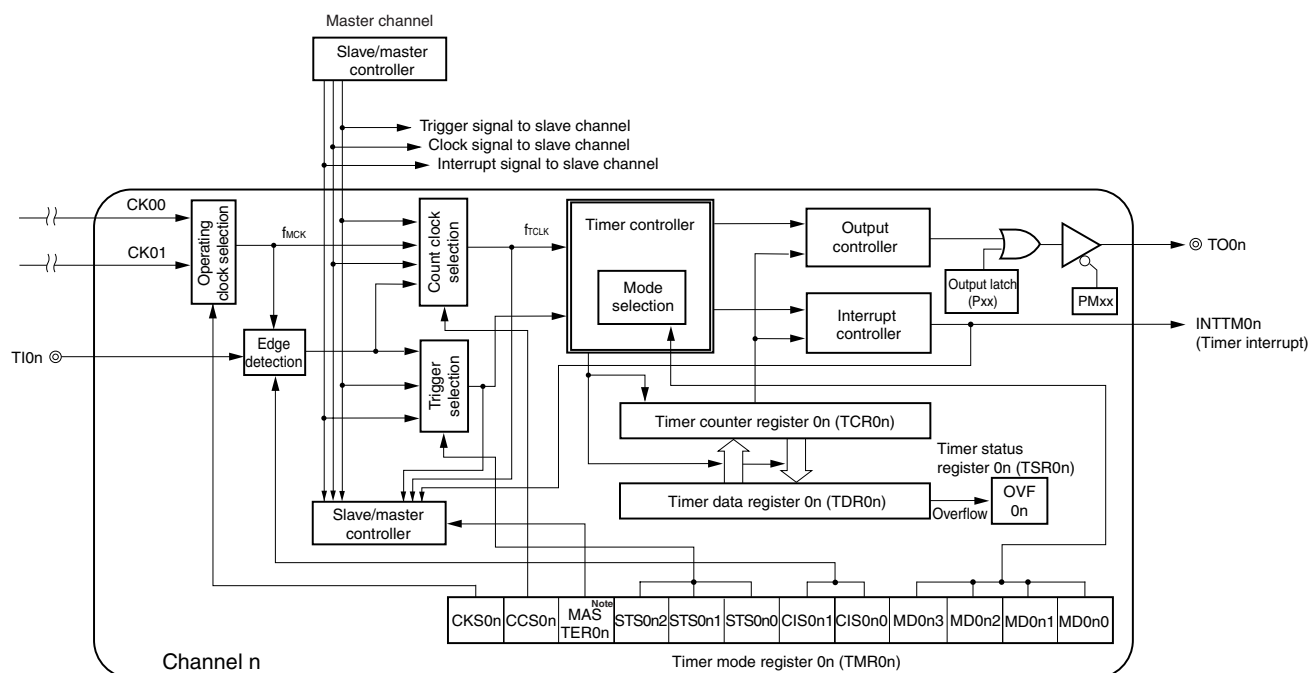
Figure 6-1 shows the block diagrams of the timer array unit.

Figure 6-1. Entire Configuration of Timer Array Unit (Example: 64-pin products)

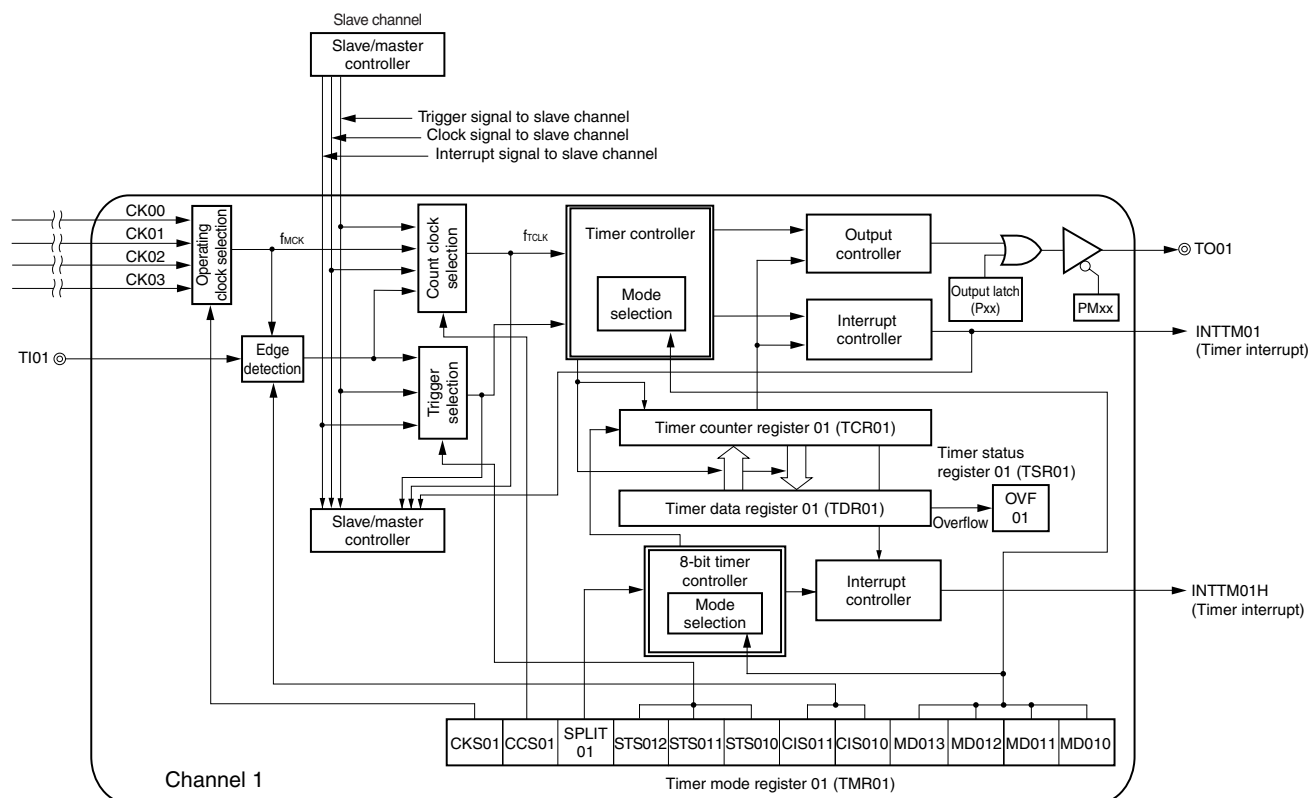


**Remark** f<sub>SUB</sub>: Subsystem clock frequency  
 f<sub>IL</sub>: Low-speed on-chip oscillator clock frequency

&lt;R&gt;

**Figure 6-2. Internal Block Diagram of Channels 0, 2, 4, 6 of Timer Array Unit 0****Note** n = 2, 4, 6 only**Remark** n = 0, 2, 4, 6

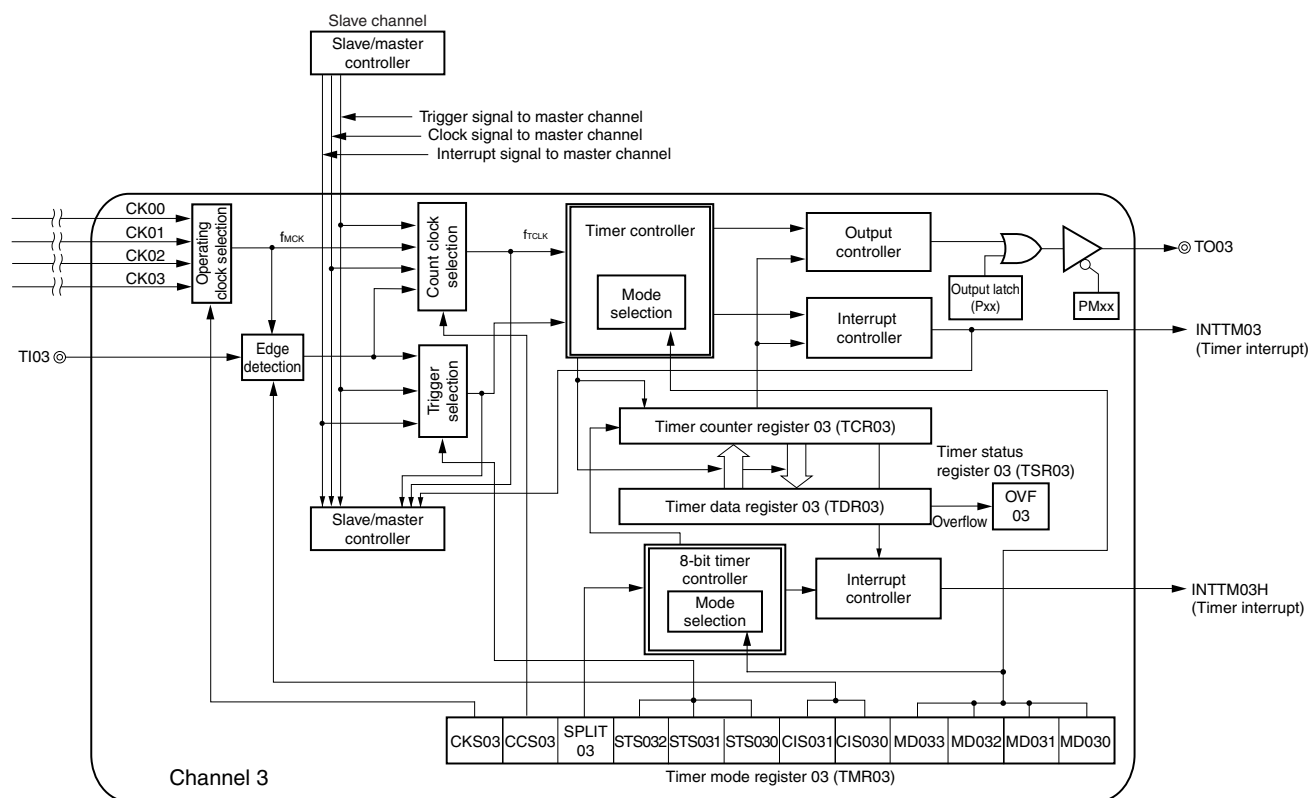
&lt;R&gt;

**Figure 6-3. Internal Block Diagram of Channel 1 of Timer Array Unit 0**



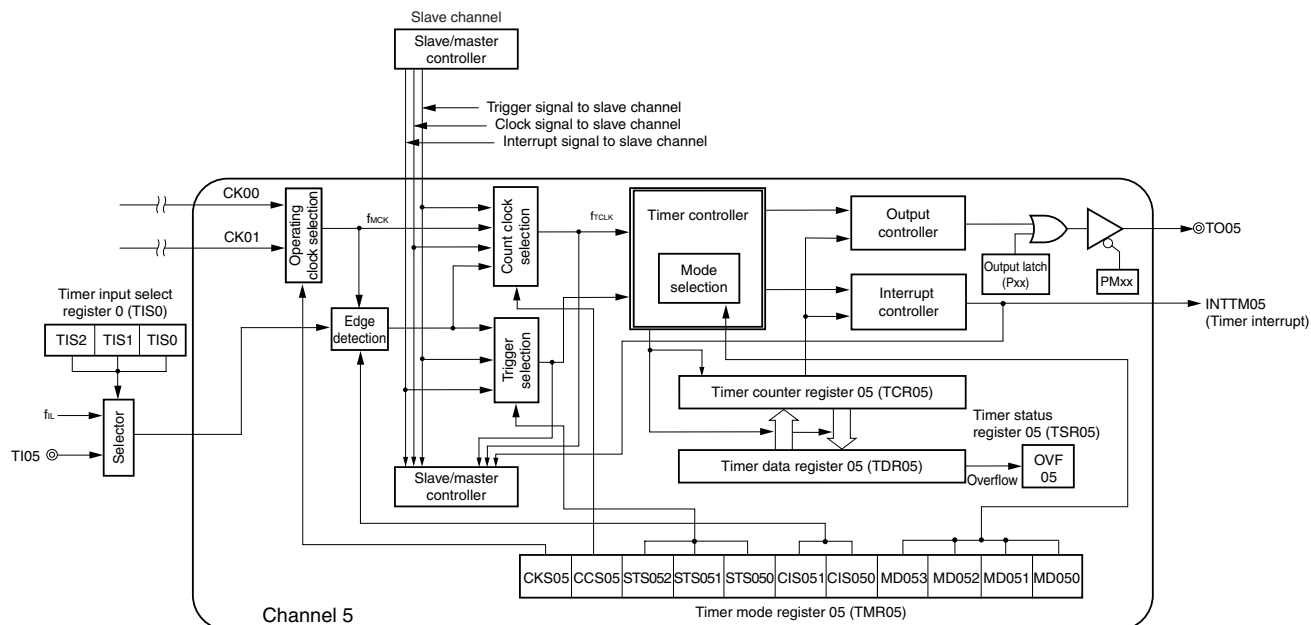
&lt;R&gt;

Figure 6-4. Internal Block Diagram of Channel 3 of Timer Array Unit 0

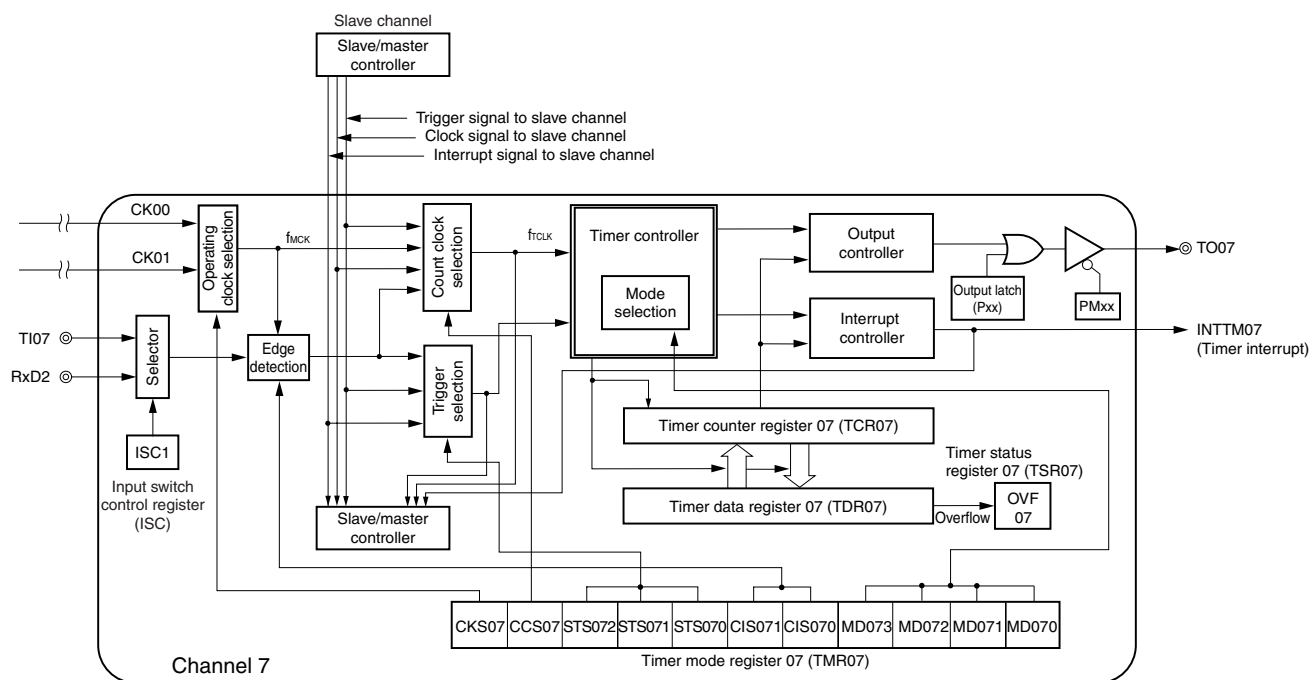


&lt;R&gt;

Figure 6-5. Internal Block Diagram of Channel 5 of Timer Array Unit 0



&lt;R&gt;

**Figure 6-6. Internal Block Diagram of Channel 7 of Timer Array Unit 0**

### 6.2.1 Timer count register mn (TCRmn)

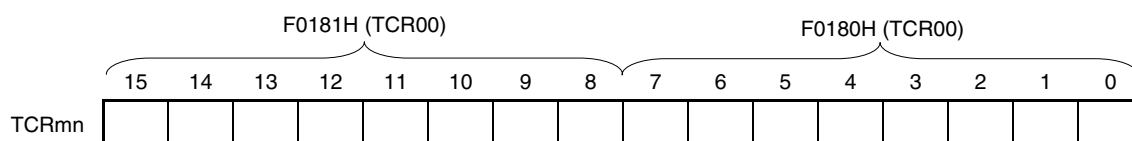
The TCRmn register is a 16-bit read-only register and is used to count clocks.

The value of this counter is incremented or decremented in synchronization with the rising edge of a count clock.

Whether the counter is incremented or decremented depends on the operation mode that is selected by the MDmn3 to MDmn0 bits of timer mode register mn (TMRmn) (refer to **6.3.3 Timer mode register mn (TMRmn)**).

**Figure 6-7. Format of Timer Count Register mn (TCRmn)**

Address: F0180H, F0181H (TCR00) to F018EH, F018FH (TCR07) After reset: FFFFH R



**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

The count value can be read by reading timer count register mn (TCRmn).

The count value is set to FFFFH in the following cases.

- When the reset signal is generated
- When the TAU0EN bit of peripheral enable register 0 (PER0) is cleared
- When counting of the slave channel has been completed in the PWM output mode
- When counting of the slave channel has been completed in the delay count mode
- When counting of the master/slave channel has been completed in the one-shot pulse output mode
- When counting of the slave channel has been completed in the multiple PWM output mode

The count value is cleared to 0000H in the following cases.

- When the start trigger is input in the capture mode
- When capturing has been completed in the capture mode

**Caution** The count value is not captured to timer data register mn (TDRmn) even when the TCRmn register is read.

The TCRmn register read value differs as follows according to operation mode changes and the operating status.

<R>

**Table 6-3. Timer Count Register mn (TCRmn) Read Value in Various Operation Modes**

| Operation Mode           | Count Mode | Timer count register mn (TCRmn) Read Value <sup>Note</sup>    |                                                                              |                                                                                 |                                                        |
|--------------------------|------------|---------------------------------------------------------------|------------------------------------------------------------------------------|---------------------------------------------------------------------------------|--------------------------------------------------------|
|                          |            | Value if the operation mode was changed after releasing reset | Value if the Operation was restarted after count operation paused (TTmn = 1) | Value if the operation mode was changed after count operation paused (TTmn = 1) | Value when waiting for a start trigger after one count |
| Interval timer mode      | Count down | FFFFH                                                         | Value if stop                                                                | Undefined                                                                       | –                                                      |
| Capture mode             | Count up   | 0000H                                                         | Value if stop                                                                | Undefined                                                                       | –                                                      |
| Event counter mode       | Count down | FFFFH                                                         | Value if stop                                                                | Undefined                                                                       | –                                                      |
| One-count mode           | Count down | FFFFH                                                         | Value if stop                                                                | Undefined                                                                       | FFFFH                                                  |
| Capture & one-count mode | Count up   | 0000H                                                         | Value if stop                                                                | Undefined                                                                       | Capture value of TDRmn register + 1                    |

**Note** This indicates the value read from the TCRmn register when channel n has stopped operating as a timer (TEmn = 0) and has been enabled to operate as a counter (TSmn = 1). The read value is held in the TCRmn register until the count operation starts.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

### 6.2.2 Timer data register mn (TDRmn)

This is a 16-bit register from which a capture function and a compare function can be selected.

The capture or compare function can be switched by selecting an operation mode by using the MDmn3 to MDmn0 bits of timer mode register mn (TMRmn).

The value of the TDRmn register can be changed at any time.

This register can be read or written in 16-bit units.

<R> In addition, for the TDRm1 and TDRm3 registers, while in the 8-bit timer mode (when the SPLIT bits of timer mode registers m1 and m3 (TMRm1, TMRm3) are 1), it is possible to read and write the data in 8-bit units, with TDRm1H and TDRm3H used as the higher 8 bits, and TDRm1L and TDRm3L used as the lower 8 bits.

Reset signal generation clears this register to 0000H.

**Figure 6-8. Format of Timer Data Register mn (TDRmn) (n = 0, 2, 4 to 7)**

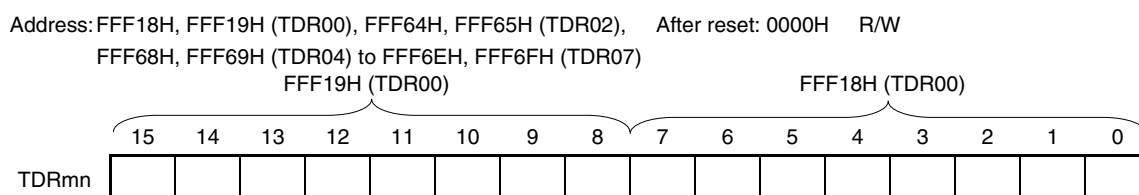
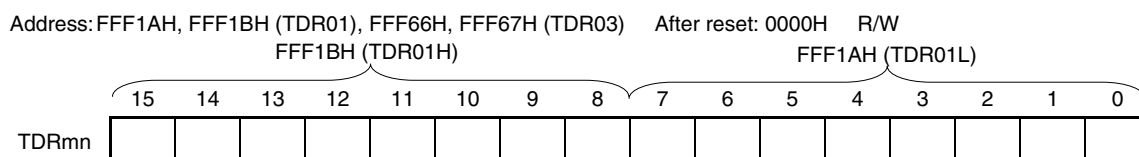


**Figure 6-9. Format of Timer Data Register mn (TDRmn) (n = 1, 3)**



#### (i) When timer data register mn (TDRmn) is used as compare register

Counting down is started from the value set to the TDRmn register. When the count value reaches 0000H, an interrupt signal (INTTMmn) is generated. The TDRmn register holds its value until it is rewritten.

**Caution** The TDRmn register does not perform a capture operation even if a capture trigger is input, when it is set to the compare function.

#### (ii) When timer data register mn (TDRmn) is used as capture register

The count value of timer count register mn (TCRmn) is captured to the TDRmn register when the capture trigger is input.

A valid edge of the TImn pin can be selected as the capture trigger. This selection is made by timer mode register mn (TMRmn).

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

### 6.3 Registers Controlling Timer Array Unit

Timer array unit is controlled by the following registers.

- Peripheral enable register 0 (PER0)
- Timer clock select register m (TPSm)
- Timer mode register mn (TMRmn)
- Timer status register mn (TSRmn)
- Timer channel enable status register m (TEm)
- Timer channel start register m (TSm)
- Timer channel stop register m (TTm)
- Timer input select register 0 (TIS0)
- Timer output select register (TOS)
- Timer output enable register m (TOEm)
- Timer output register m (TOM)
- Timer output level register m (TOLm)
- Timer output mode register m (TOMm)
- Input switch control register (ISC)
- Noise filter enable registers 1 (NFEN1)
- Port mode control register (PMCxx)<sup>Note</sup>
- Port mode register (PMxx)<sup>Note</sup>
- Port register (Pxx)<sup>Note</sup>

**Note** The port mode registers (PMxx) and port registers (Pxx) to be set differ depending on the product. For details, see 6.3.16 Port mode registers 1, 3 to 5, 14 (PM1, PM3 to PM5, PM14).

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

### 6.3.1 Peripheral enable register 0 (PER0)

This registers is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When the timer array unit is used, be sure to set bit 0 (TAU0EN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 6-10. Format of Peripheral Enable Register 0 (PER0)**

Address: F00F0H After reset: 00H R/W

| Symbol | <7>   | 6 | <5>   | <4>     | 3 | <2>    | 1 | <0>    |
|--------|-------|---|-------|---------|---|--------|---|--------|
| PER0   | RTCEN | 0 | ADCEN | IICA0EN | 0 | SAU0EN | 0 | TAU0EN |

| TAU0EN | Control of timer array unit input clock                                                                                                                                                     |
|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0      | Stops supply of input clock.<br><ul style="list-style-type: none"> <li>SFR used by the timer array unit cannot be written.</li> <li>The timer array unit is in the reset status.</li> </ul> |
| 1      | Supplies input clock.<br><ul style="list-style-type: none"> <li>SFR used by the timer array unit can be read/written.</li> </ul>                                                            |

- Cautions**
- When setting the timer array unit, be sure to set the TAU0EN bit to 1 first. If TAU0EN = 0, writing to a control register of timer array unit is ignored, and all read values are default values (except for the timer input select register 0 (TIS0), timer output select register (TOS), input switch control register (ISC), noise filter enable register 1 (NFEN1), port mode control registers 1, 4, 14 (PMC1, PMC4, PMC14), port mode registers 1, 3 to 5, 14 (PM1, PM3 to PM5, PM14), and port registers 1, 3 to 5, 14 (P1, P3 to P5, P14)).
  - Be sure to clear bits 1, 3, and 6 to "0".

<R>

### 6.3.2 Timer clock select register m (TPSm)

The TPSm register is a 16-bit register that is used to select two types or four types of operation clocks (CKm0, CKm1) that are commonly supplied to each channel from external prescaler. CKm1 is selected by using bits 7 to 4 of the TPSm register, and CKm0 is selected by using bits 3 to 0. In addition, for channel 1 and 3, CKm2 is selected by using bits 9 and 8 of the TPSm register, and CKm3 is selected by using bits 13 and 12.

Rewriting of the TPSm register during timer operation is possible only in the following cases.

If the PRSm00 to PRSm03 bits can be rewritten ( $n = 0$  to  $7$ ):

All channels for which CKm0 is selected as the operation clock (CKSmn1, CKSmn0 = 0, 0) are stopped (TEmn = 0).

If the PRSm10 to PRSm13 bits can be rewritten ( $n = 0$  to  $7$ ):

All channels for which CKm1 is selected as the operation clock (CKSmn1, CKSmn0 = 0, 1) are stopped (TEmn = 0).

If the PRSm20 and PRSm21 bits can be rewritten ( $n = 1, 3$ ):

All channels for which CKm2 is selected as the operation clock (CKSmn1, CKSmn0 = 1, 0) are stopped (TEmn = 0).

If the PRSm30 and PRSm31 bits can be rewritten ( $n = 1, 3$ ):

All channels for which CKm3 is selected as the operation clock (CKSmn1, CKSmn0 = 1, 1) are stopped (TEmn = 0).

The TPSm register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 6-11. Format of Timer Clock Select register m (TPSm) (1/2)

Address: F01B6H, F01B7H After reset: 0000H R/W

| Symbol | 15 | 14 | 13         | 12         | 11 | 10 | 9          | 8          | 7          | 6          | 5          | 4          | 3          | 2          | 1          | 0          |
|--------|----|----|------------|------------|----|----|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|
| TPSm   | 0  | 0  | PRS<br>m31 | PRS<br>m30 | 0  | 0  | PRS<br>m21 | PRS<br>m20 | PRS<br>m13 | PRS<br>m12 | PRS<br>m11 | PRS<br>m10 | PRS<br>m03 | PRS<br>m02 | PRS<br>m01 | PRS<br>m00 |

| PRS<br>mk3 | PRS<br>mk2 | PRS<br>mk1 | PRS<br>mk0 |                                   | Selection of operation clock (CKmk) <sup>Note</sup> (k = 0, 1) |                          |                           |                           |                           |
|------------|------------|------------|------------|-----------------------------------|----------------------------------------------------------------|--------------------------|---------------------------|---------------------------|---------------------------|
|            |            |            |            |                                   | f <sub>CLK</sub> = 2 MHz                                       | f <sub>CLK</sub> = 5 MHz | f <sub>CLK</sub> = 10 MHz | f <sub>CLK</sub> = 20 MHz | f <sub>CLK</sub> = 24 MHz |
| 0          | 0          | 0          | 0          | f <sub>CLK</sub>                  | 2 MHz                                                          | 5 MHz                    | 10 MHz                    | 20 MHz                    | 24 MHz                    |
| 0          | 0          | 0          | 1          | f <sub>CLK</sub> /2               | 1 MHz                                                          | 2.5 MHz                  | 5 MHz                     | 10 MHz                    | 12 MHz                    |
| 0          | 0          | 1          | 0          | f <sub>CLK</sub> /2 <sup>2</sup>  | 500 kHz                                                        | 1.25 MHz                 | 2.5 MHz                   | 5 MHz                     | 6 MHz                     |
| 0          | 0          | 1          | 1          | f <sub>CLK</sub> /2 <sup>3</sup>  | 250 kHz                                                        | 625 kHz                  | 1.25 MHz                  | 2.5 MHz                   | 3 MHz                     |
| 0          | 1          | 0          | 0          | f <sub>CLK</sub> /2 <sup>4</sup>  | 125 kHz                                                        | 312.5 kHz                | 625 kHz                   | 1.25 MHz                  | 1.5 MHz                   |
| 0          | 1          | 0          | 1          | f <sub>CLK</sub> /2 <sup>5</sup>  | 62.5 kHz                                                       | 156.2 kHz                | 312.5 kHz                 | 625 kHz                   | 750 kHz                   |
| 0          | 1          | 1          | 0          | f <sub>CLK</sub> /2 <sup>6</sup>  | 31.25 kHz                                                      | 78.1 kHz                 | 156.2 kHz                 | 312.5 kHz                 | 375 kHz                   |
| 0          | 1          | 1          | 1          | f <sub>CLK</sub> /2 <sup>7</sup>  | 15.62 kHz                                                      | 39.1 kHz                 | 78.1 kHz                  | 156.2 kHz                 | 187.5 kHz                 |
| 1          | 0          | 0          | 0          | f <sub>CLK</sub> /2 <sup>8</sup>  | 7.81 kHz                                                       | 19.5 kHz                 | 39.1 kHz                  | 78.1 kHz                  | 93.8 kHz                  |
| 1          | 0          | 0          | 1          | f <sub>CLK</sub> /2 <sup>9</sup>  | 3.91 kHz                                                       | 9.76 kHz                 | 19.5 kHz                  | 39.1 kHz                  | 46.9 kHz                  |
| 1          | 0          | 1          | 0          | f <sub>CLK</sub> /2 <sup>10</sup> | 1.95 kHz                                                       | 4.88 kHz                 | 9.76 kHz                  | 19.5 kHz                  | 23.4 kHz                  |
| 1          | 0          | 1          | 1          | f <sub>CLK</sub> /2 <sup>11</sup> | 976 Hz                                                         | 2.44 kHz                 | 4.88 kHz                  | 9.76 kHz                  | 11.7 kHz                  |
| 1          | 1          | 0          | 0          | f <sub>CLK</sub> /2 <sup>12</sup> | 488 Hz                                                         | 1.22 kHz                 | 2.44 kHz                  | 4.88 kHz                  | 5.86 kHz                  |
| 1          | 1          | 0          | 1          | f <sub>CLK</sub> /2 <sup>13</sup> | 244 Hz                                                         | 610 Hz                   | 1.22 kHz                  | 2.44 kHz                  | 2.93 kHz                  |
| 1          | 1          | 1          | 0          | f <sub>CLK</sub> /2 <sup>14</sup> | 122 Hz                                                         | 305 Hz                   | 610 Hz                    | 1.22 kHz                  | 1.46 kHz                  |
| 1          | 1          | 1          | 1          | f <sub>CLK</sub> /2 <sup>15</sup> | 61 Hz                                                          | 153 Hz                   | 305 Hz                    | 610 Hz                    | 732 Hz                    |

<R> **Note** When changing the clock selected for f<sub>CLK</sub> (by changing the system clock control register (CKC) value), stop timer array unit (TTm = 00FFH).

**Cautions 1.** Be sure to clear bits 15, 14, 11, 10 to “0”.

<R> **2.** If f<sub>CLK</sub> (undivided) is selected as the operation clock (CKmk) and TDRnm is set to 0000H (n = 0 or 1, m = 0 to 7), interrupt requests output from timer array units are not detected.

**Remarks 1.** f<sub>CLK</sub>: CPU/peripheral hardware clock frequency

<R> **2.** Waveform of the clock to be selected in the TPSm register which becomes high level for one period of f<sub>CLK</sub> from its rising edge (m = 1 to 15). For details, see 6.5.1 Count clock (f<sub>CLK</sub>).



**Figure 6-11. Format of Timer Clock Select register m (TPSm) (2/2)**

Address: F01B6H, F01B7H    After reset: 0000H    R/W

| Symbol | 15 | 14 | 13         | 12         | 11 | 10 | 9          | 8          | 7          | 6          | 5          | 4          | 3          | 2          | 1          | 0          |
|--------|----|----|------------|------------|----|----|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|
| TPSm   | 0  | 0  | PRS<br>m31 | PRS<br>m30 | 0  | 0  | PRS<br>m21 | PRS<br>m20 | PRS<br>m13 | PRS<br>m12 | PRS<br>m11 | PRS<br>m10 | PRS<br>m03 | PRS<br>m02 | PRS<br>m01 | PRS<br>m00 |

| PRS<br>m21 | PRS<br>m20 |                                  | Selection of operation clock (CKm2) <sup>Note</sup> |                          |                           |                           |                           |
|------------|------------|----------------------------------|-----------------------------------------------------|--------------------------|---------------------------|---------------------------|---------------------------|
|            |            |                                  | f <sub>CLK</sub> = 2 MHz                            | f <sub>CLK</sub> = 5 MHz | f <sub>CLK</sub> = 10 MHz | f <sub>CLK</sub> = 20 MHz | f <sub>CLK</sub> = 24 MHz |
| 0          | 0          | f <sub>CLK</sub> /2              | 1 MHz                                               | 2.5 MHz                  | 5 MHz                     | 10 MHz                    | 12 MHz                    |
| 0          | 1          | f <sub>CLK</sub> /2 <sup>2</sup> | 500 kHz                                             | 1.25 MHz                 | 2.5 MHz                   | 5 MHz                     | 6 MHz                     |
| 1          | 0          | f <sub>CLK</sub> /2 <sup>4</sup> | 125 kHz                                             | 312.5 kHz                | 625 MHz                   | 1.25 MHz                  | 1.5 MHz                   |
| 1          | 1          | f <sub>CLK</sub> /2 <sup>6</sup> | 31.25 kHz                                           | 78.1 kHz                 | 156.2 kHz                 | 312.5 kHz                 | 375 MHz                   |

| PRS<br>m31 | PRS<br>m30 | Selection of operation clock (CKm3) <sup>Note</sup> |                          |                           |                           |                           |          |
|------------|------------|-----------------------------------------------------|--------------------------|---------------------------|---------------------------|---------------------------|----------|
|            |            | f <sub>CLK</sub> = 2 MHz                            | f <sub>CLK</sub> = 5 MHz | f <sub>CLK</sub> = 10 MHz | f <sub>CLK</sub> = 20 MHz | f <sub>CLK</sub> = 24 MHz |          |
| 0          | 0          | f <sub>CLK</sub> /2 <sup>8</sup>                    | 7.81 kHz                 | 19.5 kHz                  | 39.1 kHz                  | 78.1 kHz                  | 93.8 kHz |
| 0          | 1          | f <sub>CLK</sub> /2 <sup>10</sup>                   | 1.95 kHz                 | 4.88 kHz                  | 9.76 kHz                  | 19.5 kHz                  | 23.4 kHz |
| 1          | 0          | f <sub>CLK</sub> /2 <sup>12</sup>                   | 488 Hz                   | 1.22 kHz                  | 2.44 kHz                  | 4.88 kHz                  | 5.86 kHz |
| 1          | 1          | f <sub>CLK</sub> /2 <sup>14</sup>                   | 122 HZ                   | 305 Hz                    | 610 Hz                    | 1.22 kHz                  | 1.46 kHz |

**Note** When changing the clock selected for f<sub>CLK</sub> (by changing the system clock control register (CKC) value), stop timer array unit (TTm = 00FFH).

The timer array unit must also be stopped if the operating clock (f<sub>MCK</sub>) specified by using the CKSmn0, and CKSmn1 bits or the valid edge of the signal input from the TImn pin is selected as the count clock (f<sub>CLK</sub>).

**Caution** Be sure to clear bits 15, 14, 11, 10 to “0”.

By using channels 1 and 3 in the 8-bit timer mode and specifying CKm2 or CKm3 as the operation clock, the interval times shown in Table 6-4 can be achieved by using the interval timer function.

**Table 6-4. Interval Times Available for Operation Clock CKSm2 or CKSm3**

| Clock |                                   | Interval time (f <sub>CLK</sub> = 24 MHz) |                        |                      |                       |
|-------|-----------------------------------|-------------------------------------------|------------------------|----------------------|-----------------------|
|       |                                   | 10 μs <sup>Note</sup>                     | 100 μs <sup>Note</sup> | 1 ms <sup>Note</sup> | 10 ms <sup>Note</sup> |
| CKm2  | f <sub>CLK</sub> /2               | √                                         | —                      | —                    | —                     |
|       | f <sub>CLK</sub> /2 <sup>2</sup>  | √                                         | —                      | —                    | —                     |
|       | f <sub>CLK</sub> /2 <sup>4</sup>  | √                                         | √                      | —                    | —                     |
|       | f <sub>CLK</sub> /2 <sup>6</sup>  | √                                         | √                      | —                    | —                     |
| CKm3  | f <sub>CLK</sub> /2 <sup>8</sup>  | —                                         | √                      | √                    | —                     |
|       | f <sub>CLK</sub> /2 <sup>10</sup> | —                                         | √                      | √                    | —                     |
|       | f <sub>CLK</sub> /2 <sup>12</sup> | —                                         | —                      | √                    | √                     |
|       | f <sub>CLK</sub> /2 <sup>14</sup> | —                                         | —                      | √                    | √                     |

**Note** The margin is within 5 %.

**Remarks 1.** f<sub>CLK</sub>: CPU/peripheral hardware clock frequency

**2.** For details of asignal of f<sub>CLK</sub>/2<sup>i</sup> selected with the TPSm register, see **6.5.1 Count clock (f<sub>CLK</sub>)**.

### 6.3.3 Timer mode register mn (TMRmn)

The TMRmn register sets an operation mode of channel n. This register is used to select the operation clock (f<sub>MCK</sub>), select the count clock, select the master/slave, select the 16 or 8-bit timer (only for channels 1 and 3), specify the start trigger and capture trigger, select the valid edge of the timer input, and specify the operation mode (interval, capture, event counter, one-count, or capture and one-count).

Rewriting the TMRmn register is prohibited when the register is in operation (when TEMn = 1). However, bits 7 and 6 (CISmn1, CISmn0) can be rewritten even while the register is operating with some functions (when TEMn = 1) (for details, see **6.7 Independent Channel Operation Function of Timer Array Unit** and **6.8 Simultaneous Channel Operation Function of Timer Array Unit**).

The TMRmn register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

**Caution** The bits mounted depend on the channels in the bit 11 of TMRmn register.

**TMRm2, TMRm4, TMRm6: MASTERmn bit (n = 2, 4, 6)**

**TMRm1, TMRm3: SPLITmn bit (n = 1, 3)**

**TMRm0, TMRm5, TMRm7: Fixed to 0**

**Figure 6-12. Format of Timer Mode Register mn (TMRmn) (1/4)**

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W

|                        |            |            |    |           |              |            |            |            |            |            |   |   |           |           |           |           |
|------------------------|------------|------------|----|-----------|--------------|------------|------------|------------|------------|------------|---|---|-----------|-----------|-----------|-----------|
| Symbol                 | 15         | 14         | 13 | 12        | 11           | 10         | 9          | 8          | 7          | 6          | 5 | 4 | 3         | 2         | 1         | 0         |
| TMRmn<br>(n = 2, 4, 6) | CKS<br>mn1 | CKS<br>mn0 | 0  | CCS<br>mn | MAST<br>ERmn | STS<br>mn2 | STS<br>mn1 | STS<br>mn0 | CIS<br>mn1 | CIS<br>mn0 | 0 | 0 | MD<br>mn3 | MD<br>mn2 | MD<br>mn1 | MD<br>mn0 |

|                     |            |            |    |           |             |            |            |            |            |            |   |   |           |           |           |           |
|---------------------|------------|------------|----|-----------|-------------|------------|------------|------------|------------|------------|---|---|-----------|-----------|-----------|-----------|
| Symbol              | 15         | 14         | 13 | 12        | 11          | 10         | 9          | 8          | 7          | 6          | 5 | 4 | 3         | 2         | 1         | 0         |
| TMRmn<br>(n = 1, 3) | CKS<br>mn1 | CKS<br>mn0 | 0  | CCS<br>mn | SPLIT<br>mn | STS<br>mn2 | STS<br>mn1 | STS<br>mn0 | CIS<br>mn1 | CIS<br>mn0 | 0 | 0 | MD<br>mn3 | MD<br>mn2 | MD<br>mn1 | MD<br>mn0 |

|                        |            |            |    |           |                   |            |            |            |            |            |   |   |           |           |           |           |
|------------------------|------------|------------|----|-----------|-------------------|------------|------------|------------|------------|------------|---|---|-----------|-----------|-----------|-----------|
| Symbol                 | 15         | 14         | 13 | 12        | 11                | 10         | 9          | 8          | 7          | 6          | 5 | 4 | 3         | 2         | 1         | 0         |
| TMRmn<br>(n = 0, 5, 7) | CKS<br>mn1 | CKS<br>mn0 | 0  | CCS<br>mn | 0 <sup>Note</sup> | STS<br>mn2 | STS<br>mn1 | STS<br>mn0 | CIS<br>mn1 | CIS<br>mn0 | 0 | 0 | MD<br>mn3 | MD<br>mn2 | MD<br>mn1 | MD<br>mn0 |

| CKS<br>mn1                                                                                                                                                            | CKS<br>mn0 | Selection of operation clock ( $f_{MCK}$ ) of channel n          |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|------------------------------------------------------------------|
| 0                                                                                                                                                                     | 0          | Operation clock CKm0 set by timer clock select register m (TPSm) |
| 0                                                                                                                                                                     | 1          | Operation clock CKm2 set by timer clock select register m (TPSm) |
| 1                                                                                                                                                                     | 0          | Operation clock CKm1 set by timer clock select register m (TPSm) |
| 1                                                                                                                                                                     | 1          | Operation clock CKm3 set by timer clock select register m (TPSm) |
| Operation clock ( $f_{MCK}$ ) is used by the edge detector. A count clock ( $f_{CLK}$ ) and a sampling clock are generated depending on the setting of the CCSmn bit. |            |                                                                  |
| The operation clocks CKm2 and CKm3 can only be selected for channels 1 and 3.                                                                                         |            |                                                                  |

| CCS<br>mn                                                                                             | Selection of count clock ( $f_{CLK}$ ) of channel n                                                             |
|-------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|
| 0                                                                                                     | Operation clock ( $f_{MCK}$ ) specified by the CKSmn0 and CKSmn1 bits                                           |
| 1                                                                                                     | Valid edge of input signal input from the TImn pin<br>In channel 5, Valid edge of input signal selected by TIS0 |
| Count clock ( $f_{CLK}$ ) is used for the timer/counter, output controller, and interrupt controller. |                                                                                                                 |

<R> **Note** Bit 11 is fixed at 0 of read only, write is ignored.**Cautions 1.** Be sure to clear bits 13, 5, and 4 to "0".

**2.** The timer array unit must be stopped (TTm = 00FFH) if the clock selected for  $f_{CLK}$  is changed (by changing the value of the system clock control register (CKC)), even if the operating clock specified by using the CKSmn0 and CKSmn1 bits ( $f_{MCK}$ ) or the valid edge of the signal input from the TImn pin is selected as the count clock ( $f_{CLK}$ ).

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

**Figure 6-12. Format of Timer Mode Register mn (TMRmn) (2/4)**

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W

|                        |            |            |    |           |              |            |            |            |            |            |   |   |           |           |           |           |
|------------------------|------------|------------|----|-----------|--------------|------------|------------|------------|------------|------------|---|---|-----------|-----------|-----------|-----------|
| Symbol                 | 15         | 14         | 13 | 12        | 11           | 10         | 9          | 8          | 7          | 6          | 5 | 4 | 3         | 2         | 1         | 0         |
| TMRmn<br>(n = 2, 4, 6) | CKS<br>mn1 | CKS<br>mn0 | 0  | CCS<br>mn | MAST<br>ERmn | STS<br>mn2 | STS<br>mn1 | STS<br>mn0 | CIS<br>mn1 | CIS<br>mn0 | 0 | 0 | MD<br>mn3 | MD<br>mn2 | MD<br>mn1 | MD<br>mn0 |

|                     |            |            |    |           |             |            |            |            |            |            |   |   |           |           |           |           |
|---------------------|------------|------------|----|-----------|-------------|------------|------------|------------|------------|------------|---|---|-----------|-----------|-----------|-----------|
| Symbol              | 15         | 14         | 13 | 12        | 11          | 10         | 9          | 8          | 7          | 6          | 5 | 4 | 3         | 2         | 1         | 0         |
| TMRmn<br>(n = 1, 3) | CKS<br>mn1 | CKS<br>mn0 | 0  | CCS<br>mn | SPLIT<br>mn | STS<br>mn2 | STS<br>mn1 | STS<br>mn0 | CIS<br>mn1 | CIS<br>mn0 | 0 | 0 | MD<br>mn3 | MD<br>mn2 | MD<br>mn1 | MD<br>mn0 |

|                        |            |            |    |           |                   |            |            |            |            |            |   |   |           |           |           |           |
|------------------------|------------|------------|----|-----------|-------------------|------------|------------|------------|------------|------------|---|---|-----------|-----------|-----------|-----------|
| Symbol                 | 15         | 14         | 13 | 12        | 11                | 10         | 9          | 8          | 7          | 6          | 5 | 4 | 3         | 2         | 1         | 0         |
| TMRmn<br>(n = 0, 5, 7) | CKS<br>mn1 | CKS<br>mn0 | 0  | CCS<br>mn | 0 <sup>Note</sup> | STS<br>mn2 | STS<br>mn1 | STS<br>mn0 | CIS<br>mn1 | CIS<br>mn0 | 0 | 0 | MD<br>mn3 | MD<br>mn2 | MD<br>mn1 | MD<br>mn0 |

(Bit 11 of TMRmn (n = 2, 4, 6))

Set 1: 0, 1, 2, 3, 4, 5, 6, 7

|                  |                                                                                                                    |
|------------------|--------------------------------------------------------------------------------------------------------------------|
| MAS<br>TER<br>mn | Selection between using channel n independently or simultaneously with another channel(as a slave or master)       |
| 0                | Operates in independent channel operation function or as slave channel in simultaneous channel operation function. |
| 1                | Operates as master channel in simultaneous channel operation function.                                             |

Only the channel 2, 4, 6 can be set as a master channel (MASTERmn = 1).  
Be sure to use channel 0, 5, 7 are fixed to 0 (Regardless of the bit setting, channel 0 operates as master, because it is the highest channel).  
Clear the MASTERmn bit to 0 for a channel that is used with the independent channel operation function.

(Bit 11 of TMRmn (n = 1, 3))

|             |                                                                                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| SPLI<br>Tmn | Selection of 8 or 16-bit timer operation for channels 1 and 3                                                                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0           | Operates as 16-bit timer.<br>(Operates in independent channel operation function or as slave channel in simultaneous channel operation function.) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 1           | Operates as 8-bit timer.                                                                                                                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

|                  |            |            |                                                                                                                                                |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------|------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|
| STS<br>mn2       | STS<br>mn1 | STS<br>mn0 | Setting of start trigger or capture trigger of channel n                                                                                       |  |  |  |  |  |  |  |  |  |  |  |  |
| 0                | 0          | 0          | Only software trigger start is valid (other trigger sources are unselected).                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |
| 0                | 0          | 1          | Valid edge of the TImn pin input is used as both the start trigger and capture trigger.                                                        |  |  |  |  |  |  |  |  |  |  |  |  |
| 0                | 1          | 0          | Both the edges of the TImn pin input are used as a start trigger and a capture trigger.                                                        |  |  |  |  |  |  |  |  |  |  |  |  |
| 1                | 0          | 0          | Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function). |  |  |  |  |  |  |  |  |  |  |  |  |
| Other than above |            |            | Setting prohibited                                                                                                                             |  |  |  |  |  |  |  |  |  |  |  |  |

<R> **Note** Bit 11 is fixed at 0 of read only, write is ignored.**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

**Figure 6-12. Format of Timer Mode Register mn (TMRmn) (3/4)**

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W

|                        |            |            |    |           |              |            |            |            |            |            |   |   |           |           |           |           |
|------------------------|------------|------------|----|-----------|--------------|------------|------------|------------|------------|------------|---|---|-----------|-----------|-----------|-----------|
| Symbol                 | 15         | 14         | 13 | 12        | 11           | 10         | 9          | 8          | 7          | 6          | 5 | 4 | 3         | 2         | 1         | 0         |
| TMRmn<br>(n = 2, 4, 6) | CKS<br>mn1 | CKS<br>mn0 | 0  | CCS<br>mn | MAST<br>ERmn | STS<br>mn2 | STS<br>mn1 | STS<br>mn0 | CIS<br>mn1 | CIS<br>mn0 | 0 | 0 | MD<br>mn3 | MD<br>mn2 | MD<br>mn1 | MD<br>mn0 |

|                     |            |            |    |           |             |            |            |            |            |            |   |   |           |           |           |           |
|---------------------|------------|------------|----|-----------|-------------|------------|------------|------------|------------|------------|---|---|-----------|-----------|-----------|-----------|
| Symbol              | 15         | 14         | 13 | 12        | 11          | 10         | 9          | 8          | 7          | 6          | 5 | 4 | 3         | 2         | 1         | 0         |
| TMRmn<br>(n = 1, 3) | CKS<br>mn1 | CKS<br>mn0 | 0  | CCS<br>mn | SPLIT<br>mn | STS<br>mn2 | STS<br>mn1 | STS<br>mn0 | CIS<br>mn1 | CIS<br>mn0 | 0 | 0 | MD<br>mn3 | MD<br>mn2 | MD<br>mn1 | MD<br>mn0 |

|                        |            |            |    |           |                   |            |            |            |            |            |   |   |           |           |           |           |
|------------------------|------------|------------|----|-----------|-------------------|------------|------------|------------|------------|------------|---|---|-----------|-----------|-----------|-----------|
| Symbol                 | 15         | 14         | 13 | 12        | 11                | 10         | 9          | 8          | 7          | 6          | 5 | 4 | 3         | 2         | 1         | 0         |
| TMRmn<br>(n = 0, 5, 7) | CKS<br>mn1 | CKS<br>mn0 | 0  | CCS<br>mn | 0 <sup>Note</sup> | STS<br>mn2 | STS<br>mn1 | STS<br>mn0 | CIS<br>mn1 | CIS<br>mn0 | 0 | 0 | MD<br>mn3 | MD<br>mn2 | MD<br>mn1 | MD<br>mn0 |

| CIS<br>mn1                                                                                                                            | CIS<br>mn0 | Selection of TImn pin input valid edge                                                                      |
|---------------------------------------------------------------------------------------------------------------------------------------|------------|-------------------------------------------------------------------------------------------------------------|
| 0                                                                                                                                     | 0          | Falling edge                                                                                                |
| 0                                                                                                                                     | 1          | Rising edge                                                                                                 |
| 1                                                                                                                                     | 0          | Both edges (when low-level width is measured)<br>Start trigger: Falling edge, Capture trigger: Rising edge  |
| 1                                                                                                                                     | 1          | Both edges (when high-level width is measured)<br>Start trigger: Rising edge, Capture trigger: Falling edge |
| If both the edges are specified when the value of the STSmn2 to STSmn0 bits is other than 010B, set the CISmn1 to CISmn0 bits to 10B. |            |                                                                                                             |

| MD<br>mn3                                                                                 | MD<br>mn2 | MD<br>mn1 | MD<br>mn0 | Operation mode of channel n | Corresponding function                                                             | Count operation of<br>TCR |
|-------------------------------------------------------------------------------------------|-----------|-----------|-----------|-----------------------------|------------------------------------------------------------------------------------|---------------------------|
| 0                                                                                         | 0         | 0         | 1/0       | Interval timer mode         | Interval timer / Square wave<br>output / Divider function / PWM<br>output (master) | Counting down             |
| 0                                                                                         | 1         | 0         | 1/0       | Capture mode                | Input pulse interval<br>measurement                                                | Counting up               |
| 0                                                                                         | 1         | 1         | 0         | Event counter mode          | External event counter                                                             | Counting down             |
| 1                                                                                         | 0         | 0         | 1/0       | One-count mode              | Delay counter / One-shot pulse<br>output / PWM output (slave)                      | Counting down             |
| 1                                                                                         | 1         | 0         | 0         | Capture & one-count mode    | Measurement of high-/low-level<br>width of input signal                            | Counting up               |
| Other than above                                                                          |           |           |           | Setting prohibited          |                                                                                    |                           |
| The operation of the MDmn0 bit varies depending on each operation mode (see table below). |           |           |           |                             |                                                                                    |                           |

<R> **Note** Bit 11 is fixed at 0 of read only, write is ignored.**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

**Figure 6-12. Format of Timer Mode Register mn (TMRmn) (4/4)**

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W

|                        |            |            |    |           |              |            |            |            |            |            |   |   |           |           |           |           |
|------------------------|------------|------------|----|-----------|--------------|------------|------------|------------|------------|------------|---|---|-----------|-----------|-----------|-----------|
| Symbol                 | 15         | 14         | 13 | 12        | 11           | 10         | 9          | 8          | 7          | 6          | 5 | 4 | 3         | 2         | 1         | 0         |
| TMRmn<br>(n = 2, 4, 6) | CKS<br>mn1 | CKS<br>mn0 | 0  | CCS<br>mn | MAST<br>ERmn | STS<br>mn2 | STS<br>mn1 | STS<br>mn0 | CIS<br>mn1 | CIS<br>mn0 | 0 | 0 | MD<br>mn3 | MD<br>mn2 | MD<br>mn1 | MD<br>mn0 |

|                     |            |            |    |           |             |            |            |            |            |            |   |   |           |           |           |           |
|---------------------|------------|------------|----|-----------|-------------|------------|------------|------------|------------|------------|---|---|-----------|-----------|-----------|-----------|
| Symbol              | 15         | 14         | 13 | 12        | 11          | 10         | 9          | 8          | 7          | 6          | 5 | 4 | 3         | 2         | 1         | 0         |
| TMRmn<br>(n = 1, 3) | CKS<br>mn1 | CKS<br>mn0 | 0  | CCS<br>mn | SPLIT<br>mn | STS<br>mn2 | STS<br>mn1 | STS<br>mn0 | CIS<br>mn1 | CIS<br>mn0 | 0 | 0 | MD<br>mn3 | MD<br>mn2 | MD<br>mn1 | MD<br>mn0 |

|                        |            |            |    |           |                     |            |            |            |            |            |   |   |           |           |           |           |
|------------------------|------------|------------|----|-----------|---------------------|------------|------------|------------|------------|------------|---|---|-----------|-----------|-----------|-----------|
| Symbol                 | 15         | 14         | 13 | 12        | 11                  | 10         | 9          | 8          | 7          | 6          | 5 | 4 | 3         | 2         | 1         | 0         |
| TMRmn<br>(n = 0, 5, 7) | CKS<br>mn1 | CKS<br>mn0 | 0  | CCS<br>mn | 0 <sup>Note 1</sup> | STS<br>mn2 | STS<br>mn1 | STS<br>mn0 | CIS<br>mn1 | CIS<br>mn0 | 0 | 0 | MD<br>mn3 | MD<br>mn2 | MD<br>mn1 | MD<br>mn0 |

| Operation mode<br>(Value set by the MDmn3 to MDmn1 bits<br>(see table above)) | MD<br>mn0 | Setting of starting counting and interrupt                                                                                                                                                              |
|-------------------------------------------------------------------------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| • Interval timer mode<br>(0, 0, 0)                                            | 0         | Timer interrupt is not generated when counting is started<br>(timer output does not change, either).                                                                                                    |
| • Capture mode<br>(0, 1, 0)                                                   | 1         | Timer interrupt is generated when counting is started<br>(timer output also changes).                                                                                                                   |
| • Event counter mode<br>(0, 1, 1)                                             | 0         | Timer interrupt is not generated when counting is started<br>(timer output does not change, either).                                                                                                    |
| • One-count mode <sup>Note 2</sup><br>(1, 0, 0)                               | 0         | Start trigger is invalid during counting operation.<br>At that time, interrupt is not generated.                                                                                                        |
|                                                                               | 1         | Start trigger is valid during counting operation <sup>Note 3</sup> .<br>At that time, interrupt is not generated.                                                                                       |
| • Capture & one-count mode<br>(1, 1, 0)                                       | 0         | Timer interrupt is not generated when counting is started<br>(timer output does not change, either).<br>Start trigger is invalid during counting operation.<br>At that time interrupt is not generated. |
| Other than above                                                              |           | Setting prohibited                                                                                                                                                                                      |

&lt;R&gt;

&lt;R&gt;

&lt;R&gt;

**Notes 1.** Bit 11 is fixed at 0 of read only, write is ignored.**2.** In one-count mode, interrupt output (INTTmn) when starting a count operation and Tmn output are not controlled.**3.** If the start trigger (TSmn = 1) is issued during operation, the counter is initialized, an interrupt is generated, and recounting is started (does not occur the interrupt request).**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

### 6.3.4 Timer status register mn (TSRmn)

The TSRmn register indicates the overflow status of the counter of channel n.

The TSRmn register is valid only in the capture mode (MDmn3 to MDmn1 = 010B) and capture & one-count mode (MDmn3 to MDmn1 = 110B). See Table 6-5 for the operation of the OVF bit in each operation mode and set/clear conditions.

The TSRmn register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the TSRmn register can be set with an 8-bit memory manipulation instruction with TSRmnL.

Reset signal generation clears this register to 0000H.

**Figure 6-13. Format of Timer Status Register mn (TSRmn)**

Address: F01A0H, F01A1H (TSR00) to F01AEH, F01AFH (TSR07)    After reset: 0000H    R

|        |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |     |
|--------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-----|
| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0   |
| TSRmn  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OVF |

|                                                                                                |                                      |
|------------------------------------------------------------------------------------------------|--------------------------------------|
| OVF                                                                                            | Counter overflow status of channel n |
| 0                                                                                              | Overflow does not occur.             |
| 1                                                                                              | Overflow occurs.                     |
| When OVF = 1, this flag is cleared (OVF = 0) when the next value is captured without overflow. |                                      |

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

**Table 6-5. OVF Bit Operation and Set/Clear Conditions in Each Operation Mode**

| Timer operation mode       | OVF bit | Set/clear conditions                         |
|----------------------------|---------|----------------------------------------------|
| • Capture mode             | clear   | When no overflow has occurred upon capturing |
| • Capture & one-count mode | set     | When an overflow has occurred upon capturing |
| • Interval timer mode      | clear   | —<br><br>(Use prohibited)                    |
| • Event counter mode       | set     |                                              |
| • One-count mode           |         |                                              |

**Remark** The OVF bit does not change immediately after the counter has overflowed, but changes upon the subsequent capture.

### 6.3.5 Timer channel enable status register m (TE<sub>m</sub>)

The TE<sub>m</sub> register is used to enable or stop the timer operation of each channel.

Each bit of the TE<sub>m</sub> register corresponds to each bit of the timer channel start register m (T<sub>Sm</sub>) and the timer channel stop register m (T<sub>Tm</sub>). When a bit of the T<sub>Sm</sub> register is set to 1, the corresponding bit of this register is set to 1. When a bit of the T<sub>Tm</sub> register is set to 1, the corresponding bit of this register is cleared to 0.

The TE<sub>m</sub> register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the TE<sub>m</sub> register can be set with a 1-bit or 8-bit memory manipulation instruction with TE<sub>m</sub>L.

Reset signal generation clears this register to 0000H.

**Figure 6-14. Format of Timer Channel Enable Status register m (TE<sub>m</sub>)**

Address: F01B0H, F01B1H    After reset: 0000H    R

| Symbol          | 15 | 14 | 13 | 12 | 11                    | 10 | 9                     | 8 | 7                    | 6                    | 5                    | 4                    | 3                    | 2                    | 1                    | 0                    |
|-----------------|----|----|----|----|-----------------------|----|-----------------------|---|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| TE <sub>m</sub> | 0  | 0  | 0  | 0  | TEH <sub>m</sub><br>3 | 0  | TEH <sub>m</sub><br>1 | 0 | TE <sub>m</sub><br>7 | TE <sub>m</sub><br>6 | TE <sub>m</sub><br>5 | TE <sub>m</sub><br>4 | TE <sub>m</sub><br>3 | TE <sub>m</sub><br>2 | TE <sub>m</sub><br>1 | TE <sub>m</sub><br>0 |

|           |                                                                                                                           |
|-----------|---------------------------------------------------------------------------------------------------------------------------|
| TEH<br>03 | Indication of whether operation of the higher 8-bit timer is enabled or stopped when channel 3 is in the 8-bit timer mode |
| 0         | Operation is stopped.                                                                                                     |
| 1         | Operation is enabled.                                                                                                     |

|           |                                                                                                                           |
|-----------|---------------------------------------------------------------------------------------------------------------------------|
| TEH<br>01 | Indication of whether operation of the higher 8-bit timer is enabled or stopped when channel 1 is in the 8-bit timer mode |
| 0         | Operation is stopped.                                                                                                     |
| 1         | Operation is enabled.                                                                                                     |

|                                                                                                                                                                                |                                                         |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------|
| TE <sub>m</sub> n                                                                                                                                                              | Indication of operation enable/stop status of channel n |
| 0                                                                                                                                                                              | Operation is stopped.                                   |
| 1                                                                                                                                                                              | Operation is enabled.                                   |
| This bit displays whether operation of the lower 8-bit timer for TE <sub>m</sub> 1 and TE <sub>m</sub> 3 is enabled or stopped when channel 1 or 3 is in the 8-bit timer mode. |                                                         |

**Remark**    m: Unit number (m = 0), n: Channel number (n = 0 to 7)



### 6.3.6 Timer channel start register m (TSm)

The TSm register is a trigger register that is used to initialize timer count register mn (TCRmn) and start the counting operation of each channel.

When a bit of this register is set to 1, the corresponding bit of timer channel enable status register m (TEm) is set to 1. The TSmn, TSHm1, TSHm3 bits are immediately cleared when operation is enabled (TEmn, TEHm1, TEHm3 = 1), because they are trigger bits.

The TSm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TSm register can be set with a 1-bit or 8-bit memory manipulation instruction with TSmL.

Reset signal generation clears this register to 0000H.

**Figure 6-15. Format of Timer Channel Start register m (TSm)**

Address: F01B2H, F01B3H After reset: 0000H R/W

| Symbol | 15 | 14 | 13 | 12 | 11    | 10 | 9     | 8 | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|--------|----|----|----|----|-------|----|-------|---|------|------|------|------|------|------|------|------|
| TSm    | 0  | 0  | 0  | 0  | TSHm3 | 0  | TSHm1 | 0 | TSm7 | TSm6 | TSm5 | TSm4 | TSm3 | TSm2 | TSm1 | TSm0 |

|       |                                                                                                                                                                                                                                          |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TSHm3 | Trigger to enable operation (start operation) of the higher 8-bit timer when channel 3 is in the 8-bit timer mode                                                                                                                        |
| 0     | No trigger operation                                                                                                                                                                                                                     |
| 1     | The TEHm3 bit is set to 1 and the count operation becomes enabled.<br>The TCRm3 register count operation start in the interval timer mode in the count operation enabled state (see Table 6-6 in <b>6.5.2 Start timing of counter</b> ). |

|       |                                                                                                                                                                                                                                          |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TSHm1 | Trigger to enable operation (start operation) of the higher 8-bit timer when channel 1 is in the 8-bit timer mode                                                                                                                        |
| 0     | No trigger operation                                                                                                                                                                                                                     |
| 1     | The TEHm1 bit is set to 1 and the count operation becomes enabled.<br>The TCRm1 register count operation start in the interval timer mode in the count operation enabled state (see Table 6-6 in <b>6.5.2 Start timing of counter</b> ). |

|      |                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TSmn | Operation enable (start) trigger of channel n                                                                                                                                                                                                                                                                                                                                                                    |
| 0    | No trigger operation                                                                                                                                                                                                                                                                                                                                                                                             |
| 1    | The TEmn bit is set to 1 and the count operation becomes enabled.<br>The TCRmn register count operation start in the count operation enabled state varies depending on each operation mode (see Table 6-6 in <b>6.5.2 Start timing of counter</b> ).<br>This bit is the trigger to enable operation (start operation) of the lower 8-bit timer for TSm1 and TSm3 when channel 1 or 3 is in the 8-bit timer mode. |

**Cautions** 1. Be sure to clear bits 15 to 12, 10, 8 to “0”

2. When switching from a function that does not use TImn pin input to one that does, the following wait period is required from when timer mode register mn (TMRmn) is set until the TSmn (TSHm1, TSHm3) bit is set to 1.

When the TImn pin noise filter is enabled (TNFENmn = 1): Four cycles of the operation clock (f<sub>MCK</sub>)

When the TImn pin noise filter is disabled (TNFENmn = 0): Two cycles of the operation clock (f<sub>MCK</sub>)

**Remarks** 1. When the TSm register is read, 0 is always read.

2. m: Unit number (m = 0), n: Channel number (n = 0 to 7)

### 6.3.7 Timer channel stop register m (TTm)

The TTm register is a trigger register that is used to stop the counting operation of each channel.

When a bit of this register is set to 1, the corresponding bit of timer channel enable status register m (TEm) is cleared to 0. The TTmn, TTHm1, TTHm3 bits are immediately cleared when operation is stopped (TEmn, TTHm1, TTHm3 = 0), because they are trigger bits.

The TTm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TTm register can be set with a 1-bit or 8-bit memory manipulation instruction with TTmL.

Reset signal generation clears this register to 0000H.

**Figure 6-16. Format of Timer Channel Stop register m (TTm)**

Address: F01B4H, F01B5H    After reset: 0000H    R/W

| Symbol | 15 | 14 | 13 | 12 | 11        | 10 | 9         | 8 | 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|--------|----|----|----|----|-----------|----|-----------|---|----------|----------|----------|----------|----------|----------|----------|----------|
| TTm    | 0  | 0  | 0  | 0  | TTHm<br>3 | 0  | TTHm<br>1 | 0 | TTm<br>7 | TTm<br>6 | TTm<br>5 | TTm<br>4 | TTm<br>3 | TTm<br>2 | TTm<br>1 | TTm<br>0 |

|           |                                                                                               |
|-----------|-----------------------------------------------------------------------------------------------|
| TTH<br>m3 | Trigger to stop operation of the higher 8-bit timer when channel 3 is in the 8-bit timer mode |
| 0         | No trigger operation                                                                          |
| 1         | Operation is stopped (stop trigger is generated).                                             |

|           |                                                                                               |
|-----------|-----------------------------------------------------------------------------------------------|
| TTH<br>m1 | Trigger to stop operation of the higher 8-bit timer when channel 1 is in the 8-bit timer mode |
| 0         | No trigger operation                                                                          |
| 1         | Operation is stopped (stop trigger is generated).                                             |

|          |                                                                                                                                                                                                        |
|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TTm<br>n | Operation stop trigger of channel n                                                                                                                                                                    |
| 0        | No trigger operation                                                                                                                                                                                   |
| 1        | TEmn bit clear to 0, to be count operation stop enable status.<br>This bit is the trigger to stop operation of the lower 8-bit timer for TTm1 and TTm3 when channel 1 or 3 is in the 8-bit timer mode. |

<R>

**Caution** Be sure to clear bits 15 to 12, 10, 8 of the TTm register to “0”.

**Remarks 1.** When the TTm register is read, 0 is always read.

2. m: Unit number (m = 0), n: Channel number (n = 0 to 7)

### 6.3.8 Timer input select register 0 (TIS0)

The TIS0 register is used to select the channel 1 timer input.

The TIS0 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 6-17. Format of Timer Input Select register 0 (TIS0)**

Address: F0074H After reset: 00H R/W

|        |   |   |   |   |   |       |       |       |
|--------|---|---|---|---|---|-------|-------|-------|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2     | 1     | 0     |
| TIS0   | 0 | 0 | 0 | 0 | 0 | TIS02 | TIS01 | TIS00 |

| TIS02            | TIS01 | TIS00 | Selection of timer input used with channel 1          |
|------------------|-------|-------|-------------------------------------------------------|
| 0                | 0     | 0     | Input signal of timer input pin (TI01)                |
| 1                | 0     | 0     | Low-speed on-chip oscillator clock (f <sub>IL</sub> ) |
| 1                | 0     | 1     | Subsystem clock (f <sub>SUB</sub> )                   |
| Other than above |       |       | Setting prohibited                                    |

<R> **Caution** High-level width, low-level width of timer input is selected, will require more than  $1/f_{MCK} + 10$  ns. Therefore, when selecting f<sub>SUB</sub> to f<sub>CLK</sub> (CSS bit of CKS register = 1), can not TIS02 bit set to 1.

### 6.3.9 Timer output select register (TOS)

The TOS register is used to enable the remote control output function.

Remote control output are generated by using the PWM output signal generated by channels 2 and 3 (mask wave) to mask the PWM output signal generated by channels 6 and 7 (carrier wave).

Rewriting the TOS register is only possible before counting starts (TE02, TE03, TE06, TE07 = 0).

The TOS register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 6-18. Format of Timer Output Select register (TOS)**

Address: F0079H After reset: 00H R/W

|        |   |   |   |   |   |   |   |      |
|--------|---|---|---|---|---|---|---|------|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0    |
| TOS    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TOS0 |

| TOS0 | Remote control output setting                              |
|------|------------------------------------------------------------|
| 0    | Disable (channels 2, 3, 6, and 7 is used for timer output) |
| 1    | Enable (remote control output to the TO03 pin)             |

- Cautions**
1. Channels 2, 3, 6, and 7 cannot be used for any other function when remote control output is enabled (TOS0 = 1).
  2. Do not set the TOS0 bit to 1 in 32-pin products.

### 6.3.10 Timer output enable register m (TOEm)

The TOEm register is used to enable or disable timer output of each channel.

Channel n for which timer output has been enabled becomes unable to rewrite the value of the TOmn bit of timer output register m (TOM) described later by software, and the value reflecting the setting of the timer output function through the count operation is output from the timer output pin (TOMn).

The TOEm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TOEm register can be set with a 1-bit or 8-bit memory manipulation instruction with TOEmL.

Reset signal generation clears this register to 0000H.

**Figure 6-19. Format of Timer Output Enable register m (TOEm)**

Address: F01BAH, F01BBH    After reset: 0000H    R/W

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7         | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|--------|----|----|----|----|----|----|---|---|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| TOEm   | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | TOE<br>m7 | TOE<br>m6 | TOE<br>m5 | TOE<br>m4 | TOE<br>m3 | TOE<br>m2 | TOE<br>m1 | TOE<br>m0 |

| <R> | TOE<br>mn | Timer output enable/disable of channel n                                                                                                                            |
|-----|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     | 0         | Disable output of timer.<br>Without reflecting on TOMn bit timer operation, to fixed the output.<br>Writing to the TOMn bit is enabled.                             |
|     | 1         | Enable output of timer.<br>Reflected in the TOMn bit timer operation, to generate the output waveform.<br>Writing to the TOMn bit is disabled (writing is ignored). |

**Caution** Be sure to clear bits 15 to 8 to “0”.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

### 6.3.11 Timer output register m (TOM)

The TOM register is a buffer register of timer output of each channel.

The value of each bit in this register is output from the timer output pin (TOMn) of each channel.

The TOMn bit of this register can be rewritten by software only when timer output is disabled (TOEmn = 0). When timer output is enabled (TOEmn = 1), rewriting this register by software is ignored, and the value is changed only by the timer operation.

To use the P140/TO00, P30/TI01/TO01, P17/TI02/TO02, P32/TI03/TO03, P41/TI04/TO04, P42/TI05/TO05, P51/TI06/TO06, or P53/TI07/TO07 pin as a port function pin, set the corresponding TOMn bit to "0".

The TOM register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TOM register can be set with an 8-bit memory manipulation instruction with TOML.

Reset signal generation clears this register to 0000H.

**Figure 6-20. Format of Timer Output register m (TOM)**

Address: F01B8H, F01B9H After reset: 0000H R/W

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|--------|----|----|----|----|----|----|---|---|------|------|------|------|------|------|------|------|
| TOM    | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | TOM7 | TOM6 | TOM5 | TOM4 | TOM3 | TOM2 | TOM1 | TOM0 |

| TOMn | Timer output of channel n  |
|------|----------------------------|
| 0    | Timer output value is "0". |
| 1    | Timer output value is "1". |

**Caution** Be sure to clear bits 15 to 8 to "0".

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

### 6.3.12 Timer output level register m (TOLm)

The TOLm register is a register that controls the timer output level of each channel.

The setting of the inverted output of channel n by this register is reflected at the timing of set or reset of the timer output signal while the timer output is enabled (TOEmn = 1) in the Slave channel output mode (TOMmn = 1). In the master channel output mode (TOMmn = 0), this register setting is invalid.

The TOLm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TOLm register can be set with an 8-bit memory manipulation instruction with TOLmL.

Reset signal generation clears this register to 0000H.

**Figure 6-21. Format of Timer Output Level register m (TOLm)**

Address: F01BCH, F01BDH After reset: 0000H R/W

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7         | 6         | 5         | 4         | 3         | 2         | 1         | 0 |
|--------|----|----|----|----|----|----|---|---|-----------|-----------|-----------|-----------|-----------|-----------|-----------|---|
| TOLm   | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | TOL<br>m7 | TOL<br>m6 | TOL<br>m5 | TOL<br>m4 | TOL<br>m3 | TOL<br>m2 | TOL<br>m1 | 0 |

| TOL<br>mn | Control of timer output level of channel n |
|-----------|--------------------------------------------|
| 0         | Positive logic output (active-high)        |
| 1         | Negative logic output (active-low)         |

**Caution** Be sure to clear bits 15 to 8, and 0 to “0”.

- Remarks**
1. If the value of this register is rewritten during timer operation, the timer output logic is inverted when the timer output signal changes next, instead of immediately after the register value is rewritten.
  2. m: Unit number (m = 0), n: Channel number (n = 0 to 7)

### 6.3.13 Timer output mode register m (TOMm)

The TOMm register is used to control the timer output mode of each channel.

When a channel is used for the independent channel operation function, set the corresponding bit of the channel to be used to 0.

When a channel is used for the simultaneous channel operation function (PWM output, one-shot pulse output, or multiple PWM output), set the corresponding bit of the master channel to 0 and the corresponding bit of the slave channel to 1.

The setting of each channel n by this register is reflected at the timing when the timer output signal is set or reset while the timer output is enabled ( $TOEmn = 1$ ).

The TOMm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TOMm register can be set with an 8-bit memory manipulation instruction with TOMmL.

Reset signal generation clears this register to 0000H.

**Figure 6-22. Format of Timer Output Mode register m (TOMm)**

Address: F01BEH, F01BFH After reset: 0000H R/W

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7         | 6         | 5         | 4         | 3         | 2         | 1         | 0 |
|--------|----|----|----|----|----|----|---|---|-----------|-----------|-----------|-----------|-----------|-----------|-----------|---|
| TOMm   | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | TOM<br>m7 | TOM<br>m6 | TOM<br>m5 | TOM<br>m4 | TOM<br>m3 | TOM<br>m2 | TOM<br>m1 | 0 |

| TOM<br>mn | Control of timer output mode of channel n                                                                                                                                                       |
|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0         | Master channel output mode (to produce toggle output by timer interrupt request signal (INTTMmn))                                                                                               |
| 1         | Slave channel output mode (output is set by the timer interrupt request signal (INTTMmn) of the master channel, and reset by the timer interrupt request signal (INTTM0p) of the slave channel) |

**Caution** Be sure to clear bits 15 to 8, and 0 to “0”.

**Remark** m: Unit number (m = 0)

n: Channel number

n = 0 to 7 (n = 0, 2, 4, 6 for master channel)

p: Slave channel number

$n < p \leq 7$

(For details of the relation between the master channel and slave channel, refer to **6.4.1 Basic rules of simultaneous channel operation function**.)

### 6.3.14 Input switch control register (ISC)

The ISC1 and ISC0 bits of the ISC register are used to implement LIN-bus communication operation by using channel 5 in association with the serial array unit. When the ISC1 bit is set to 1, the input signal of the serial data input pin (RxD0) is selected as a timer input signal.

The ISC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 6-23. Format of Input Switch Control Register (ISC)**

Address: F0073H    After reset: 00H    R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0    |
|--------|---|---|---|---|---|---|------|------|
| ISC    | 0 | 0 | 0 | 0 | 0 | 0 | ISC1 | ISC0 |

|      |                                                                                                                                                                                     |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ISC1 | Switching channel 5 input of timer array unit                                                                                                                                       |
| 0    | 52 and 64-pin products:<br>Uses the input signal of the TI05 pin as a timer input (normal operation).<br>32, 44, 48-pin products:<br>Do not use a timer input signal for channel 5. |
| 1    | Input signal of the RxD0 pin is used as timer input (detects the wakeup signal and measures the low width of the break field and the pulse width of the sync field).                |

|      |                                                                                           |
|------|-------------------------------------------------------------------------------------------|
| ISC0 | Switching external interrupt (INTP0) input                                                |
| 0    | Uses the input signal of the INTP0 pin as an external interrupt (normal operation).       |
| 1    | Uses the input signal of the RxD0 pin as an external interrupt (wakeup signal detection). |

**Caution** Be sure to clear bits 7 to 2 to “0”.

**Remark** When the LIN-bus communication function is used, select the input signal of the RxD0 pin by setting ISC1 to 1.



### 6.3.15 Noise filter enable register 1 (NFEN1)

The NFEN1 register is used to set whether the noise filter can be used for the timer input signal to each channel.

Enable the noise filter by setting the corresponding bits to 1 on the pins in need of noise removal.

When the noise filter is ON, match detection and synchronization of the 2 clocks is performed with the CPU/peripheral hardware clock ( $f_{MCK}$ ). When the noise filter is OFF, only synchronization is performed with the CPU/peripheral hardware clock ( $f_{MCK}$ ) <sup>Note</sup>.

The NFEN1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Note** For details, see **6.5.1 (2) When valid edge of input signal input from the TImn pin is selected (CCSmn = 1)** and **6.5.2 Start timing of counter**.

**Figure 6-24. Format of Noise Filter Enable Register 1 (NFEN1)**

Address: F0071H    After reset: 00H    R/W

| Symbol | 7       | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
|--------|---------|---------|---------|---------|---------|---------|---------|---------|
| NFEN1  | TNFEN07 | TNFEN06 | TNFEN05 | TNFEN04 | TNFEN03 | TNFEN02 | TNFEN01 | TNFEN00 |

| TNFEN07 | Enable/disable using noise filter of TI07TO07P53 pin signal |
|---------|-------------------------------------------------------------|
| 0       | Noise filter OFF                                            |
| 1       | Noise filter ON                                             |

| TNFEN06 | Enable/disable using noise filter of TI06/TO06/P51 pin input signal |
|---------|---------------------------------------------------------------------|
| 0       | Noise filter OFF                                                    |
| 1       | Noise filter ON                                                     |

| TNFEN05 | Enable/disable using noise filter of TI05/TO05/P42 pin or RxD0/P11 pin input signal <sup>Note</sup> |
|---------|-----------------------------------------------------------------------------------------------------|
| 0       | Noise filter OFF                                                                                    |
| 1       | Noise filter ON                                                                                     |

| TNFEN04 | Enable/disable using noise filter of TI04/TO04/P41 pin input signal |
|---------|---------------------------------------------------------------------|
| 0       | Noise filter OFF                                                    |
| 1       | Noise filter ON                                                     |

| TNFEN03 | Enable/disable using noise filter of TI03/TO03/P32 pin input signal |
|---------|---------------------------------------------------------------------|
| 0       | Noise filter OFF                                                    |
| 1       | Noise filter ON                                                     |

| TNFEN02 | Enable/disable using noise filter of TI02/TO02/P17 pin input signal |
|---------|---------------------------------------------------------------------|
| 0       | Noise filter OFF                                                    |
| 1       | Noise filter ON                                                     |

| TNFEN01 | Enable/disable using noise filter of TI01/TO01/P30 pin input signal |
|---------|---------------------------------------------------------------------|
| 0       | Noise filter OFF                                                    |
| 1       | Noise filter ON                                                     |

| TNFEN00 | Enable/disable using noise filter of TI00/P141 pin input signal |
|---------|-----------------------------------------------------------------|
| 0       | Noise filter OFF                                                |
| 1       | Noise filter ON                                                 |

**Note** The applicable pin can be switched by setting the ISC1 bit of the ISC register.

ISC1 = 0: Whether or not to use the noise filter of the TI05 pin can be selected.

ISC1 = 1: Whether or not to use the noise filter of the RxD0 pin can be selected.

**Remark** The presence or absence of timer I/O pins of channel 0 to 7 depends on the product. See **Table 6-2 Timer I/O Pins provided in Each Product** for details.

### 6.3.16 Port mode registers 1, 3 to 5, 14 (PM1, PM3 to PM5, PM14)

These registers set input/output of ports 1, 3 to 5, 14 in 1-bit units.

The presence or absence of timer I/O pins depends on the product. When using the timer array unit, set the following port mode registers according to the product used.

32, and 44-pin products: PM1, PM3, PM14

48-pin products: PM1, PM3, PM4, PM14

52, and 64-pin products: PM1, PM3 to PM5, PM14

When using the ports (such as P140/TO00 and P41/TO04/TI04) to be shared with the timer output pin for timer output, set the port mode control register (PMCxx) bit, port mode register (PMxx) bit and port register (Pxx) bit corresponding to each port to 0.

Example: When using P41/TO04/TI04 for timer output

Set the PMC41 bit of port mode control register 4 to 0.

Set the PM41 bit of port mode register 4 to 0.

Set the P41 bit of port register 4 to 0.

When using the ports (such as P141/TI00 and P41/TO04/TI04) to be shared with the timer input pin for timer input, set the port mode register (PMxx) bit corresponding to each port to 1. And set the port mode control register (PMCxx) bit corresponding to each port to 0. At this time, the port register (Pxx) bit may be 0 or 1.

Example: When using P41/TO04/TI04 for timer input

Set the PMC41 bit of port mode control register 4 to 0.

Set the PM41 bit of port mode register 4 to 1.

Set the P41 bit of port register 4 to 0 or 1.

The PM1, PM3 to PM5, PM14 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

**Figure 6-25. Format of Port Mode Registers 1, 3 to 5, 14 (PM1, PM3 to PM5, PM14) (64-pin products)**

Address: FFF21H After reset: FFH R/W

| Symbol | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|--------|------|------|------|------|------|------|------|------|
| PM1    | PM17 | PM16 | PM15 | PM14 | PM13 | PM12 | PM11 | PM10 |

Address: FFF23H After reset: FFH R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2    | 1    | 0    |
|--------|---|---|---|---|---|------|------|------|
| PM3    | 1 | 1 | 1 | 1 | 1 | PM32 | PM31 | PM30 |

Address: FFF24H After reset: FFH R/W

| Symbol | 7 | 6 | 5 | 4 | 3    | 2    | 1    | 0    |
|--------|---|---|---|---|------|------|------|------|
| PM4    | 1 | 1 | 1 | 1 | PM43 | PM42 | PM41 | PM40 |

Address: FFF25H After reset: FFH R/W

| Symbol | 7 | 6 | 5 | 4    | 3    | 2    | 1    | 0    |
|--------|---|---|---|------|------|------|------|------|
| PM5    | 1 | 1 | 1 | PM54 | PM53 | PM52 | PM51 | PM50 |

Address: FFF2EH After reset: FFH R/W

| Symbol | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| PM14   | PM147 | PM146 | PM145 | PM144 | PM143 | PM142 | PM141 | PM140 |

| PMmn | Pmn pin I/O mode selection (m = 1, 3 to 5, 14; n = 0 to 7) |
|------|------------------------------------------------------------|
| 0    | Output mode (output buffer on)                             |
| 1    | Input mode (output buffer off)                             |

**Remark** The figure shown above presents the format of port mode registers 1, 3 to 5, 14 of the 64-pin products. The format of the port mode register of other products, see **Table 4-3. PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits mounted on each product.**

## 6.4 Basic Rules of Timer Array Unit

### 6.4.1 Basic rules of simultaneous channel operation function

When simultaneously using multiple channels, namely, a combination of a master channel (a reference timer mainly counting the cycle) and slave channels (timers operating according to the master channel), the following rules apply.

- (1) Only an even channel (channel 0, 2, 4, etc.) can be set as a master channel.
- (2) Any channel, except channel 0, can be set as a slave channel.
- (3) The slave channel must be lower than the master channel.

Example: If channel 2 is set as a master channel, channel 3 or those that follow (channels 3, 4, 5, etc.) can be set as a slave channel.

- (4) Two or more slave channels can be set for one master channel.
- (5) When two or more master channels are to be used, slave channels with a master channel between them may not be set.

Example: If channels 0 and 4 are set as master channels, channels 1 to 3 can be set as the slave channels of master channel 0. Channels 5 to 7 cannot be set as the slave channels of master channel 0.

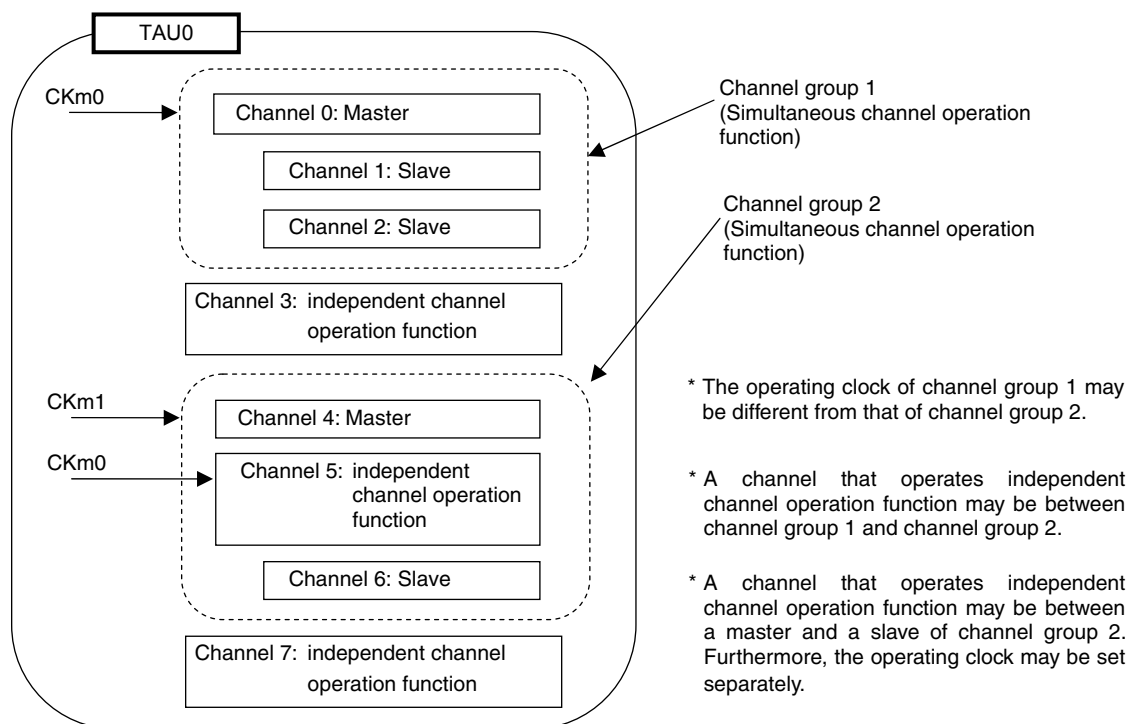
- (6) The operating clock for a slave channel in combination with a master channel must be the same as that of the master channel. The CKSmn0, CKSmn1 bits (bit 15, 14 of timer mode register mn (TMRmn)) of the slave channel that operates in combination with the master channel must be the same value as that of the master channel.
- (7) A master channel can transmit INTTMmn (interrupt), start software trigger, and count clock to the lower channels.
- (8) A slave channel can use INTTMmn (interrupt), a start software trigger, or the count clock of the master channel as a source clock, but cannot transmit its own INTTMmn (interrupt), start software trigger, or count clock to channels with lower channel numbers.
- (9) A master channel cannot use INTTMmn (interrupt), a start software trigger, or the count clock from the other higher master channel as a source clock.
- (10) To simultaneously start channels that operate in combination, the channel start trigger bit (TSmn) of the channels in combination must be set at the same time.
- (11) During the counting operation, a TSmn bit of a master channel or TSmn bits of all channels which are operating simultaneously can be set. It cannot be applied to TSmn bits of slave channels alone.
- (12) To stop the channels in combination simultaneously, the channel stop trigger bit (TTmn) of the channels in combination must be set at the same time.
- (13) CKm2/CKm3 cannot be selected while channels are operating simultaneously, because the operating clocks of master channels and slave channels have to be synchronized.
- (14) Timer mode register m0 (TMRm0) has no master bit (it is fixed as "0"). However, as channel 0 is the highest channel, it can be used as a master channel during simultaneous operation.

The rules of the simultaneous channel operation function are applied in a channel group (a master channel and slave channels forming one simultaneous channel operation function).

If two or more channel groups that do not operate in combination are specified, the basic rules of the simultaneous channel operation function in **6.4.1 Basic rules of simultaneous channel operation function** do not apply to the channel groups.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

## Example



### 6.4.2 Basic rules of 8-bit timer operation function (channels 1 and 3 only)

The 8-bit timer operation function makes it possible to use a 16-bit timer channel in a configuration consisting of two 8-bit timer channels.

This function can only be used for channels 1 and 3, and there are several rules for using it.

The basic rules for this function are as follows:

- (1) The 8-bit timer operation function applies only to channels 1 and 3.
- (2) When using 8-bit timers, set the SPLIT bit of timer mode register mn (TMRmn) to 1.
- (3) The higher 8 bits can be operated as the interval timer function.
- (4) At the start of operation, the higher 8 bits output INTTMm1H/INTTMm3H (an interrupt) (which is the same operation performed when MDmn0 is set to 1).
- (5) The operation clock of the higher 8 bits is selected according to the CKSmn1 and CKSmn0 bits of the lower-bit TMRmn register.
- (6) For the higher 8 bits, the TSHm1/TSHm3 bit is manipulated to start channel operation and the TTHm1/TTHm3 bit is manipulated to stop channel operation. The channel status can be checked using the TEHm1/TEHm3 bit.
- (7) The lower 8 bits operate according to the TMRmn register settings. The following three functions support operation of the lower 8 bits:
  - Interval timer function
  - External event counter function
  - Delay count function
- (8) For the lower 8 bits, the TSm1/TSm3 bit is manipulated to start channel operation and the TTm1/TTm3 bit is manipulated to stop channel operation. The channel status can be checked using the TEM1/TEM3 bit.
- (9) During 16-bit operation, manipulating the TSHm1, TSHm3, TTHm1, and TTHm3 bits is invalid. The TSm1, TSm3, TTm1, and TTm3 bits are manipulated to operate channels 1 and 3. The TEHm3 and TEHm1 bits are not changed.
- (10) For the 8-bit timer function, the simultaneous operation functions (one-shot pulse, PWM, and multiple PWM) cannot be used.

**Remark** m: Unit number (m = 0), n: Channel number (n = 1, 3)

## 6.5 Operation of Counter

### 6.5.1 Count clock ( $f_{\text{TCLK}}$ )

The count clock ( $f_{\text{TCLK}}$ ) of the timer array unit can be selected between following by CCSmn bit of timer mode register mn (TMRmn).

- Operation clock ( $f_{\text{MCK}}$ ) specified by the CKSmn0 and CKSmn1 bits
- Valid edge of input signal input from the TImn pin

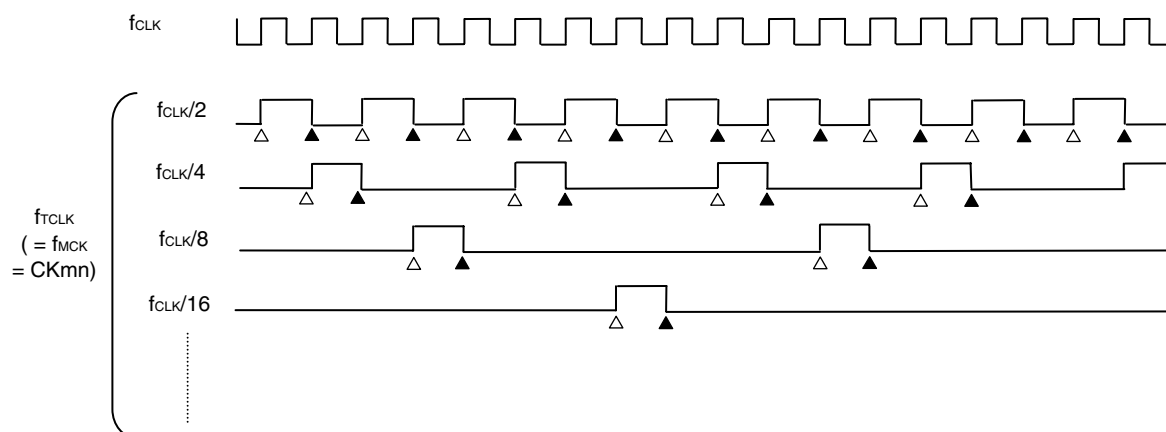
Because the timer array unit is designed to operate in synchronization with  $f_{\text{CLK}}$ , the timings of the count clock ( $f_{\text{TCLK}}$ ) are shown below.

#### (1) When operation clock ( $f_{\text{MCK}}$ ) specified by the CKSmn0 and CKSmn1 bits is selected (CCSmn = 0)

The count clock ( $f_{\text{TCLK}}$ ) is between  $f_{\text{CLK}}$  to  $f_{\text{CLK}}/2^{15}$  by setting of timer clock select register m (TPSm). When a divided  $f_{\text{CLK}}$  is selected, however, the clock selected in TPSm register, but a signal which becomes high level for one period of  $f_{\text{CLK}}$  from its rising edge. When a  $f_{\text{CLK}}$  is selected, fixed to high level

Counting of timer count register mn (TCRmn) delayed by one period of  $f_{\text{CLK}}$  from rising edge of the count clock, because of synchronization with  $f_{\text{CLK}}$ . But, this is described as “counting at rising edge of the count clock”, as a matter of convenience.

Figure 6-26. Timing of  $f_{\text{CLK}}$  and count clock ( $f_{\text{TCLK}}$ ) (When CCSmn = 0)



- Remarks 1.  $\Delta$  : Rising edge of the count clock  
 $\blacktriangle$  : Synchronization, increment/decrement of counter  
 2.  $f_{\text{CLK}}$ : CPU/peripheral hardware clock

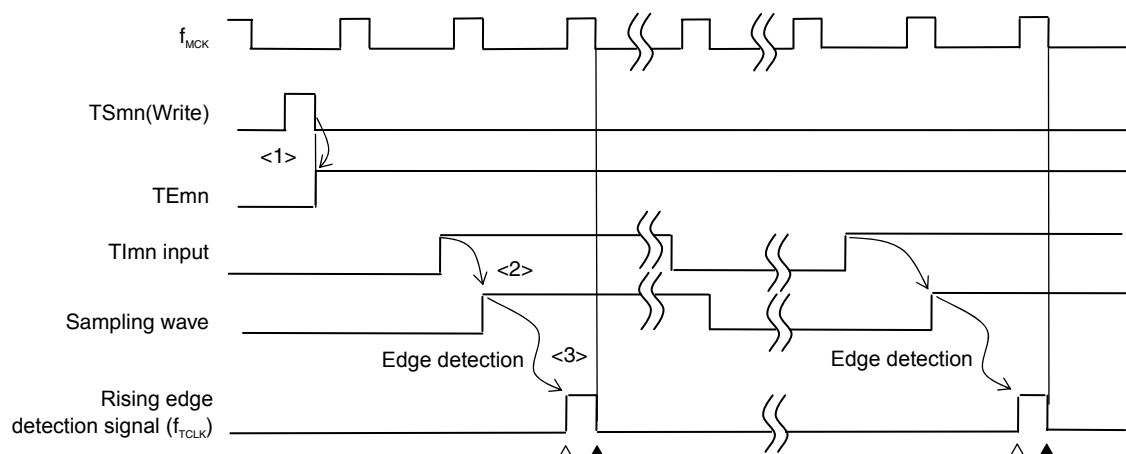


**(2) When valid edge of input signal input from the TImn pin is selected (CCSmn = 1)**

The count clock ( $f_{TCLK}$ ) is between  $f_{CLK}$  to  $f_{CLK} / 2^{15}$  by setting of timer clock select register m (TPSm). When a divided  $f_{CLK}$  is selected, however, the count clock is not a signal which is simply divided  $f_{CLK}$  by  $2^m$ , but a signal which becomes high level for one period of  $f_{CLK}$  from its rising edge ( $m = 1$  to 15).

Counting of timer count register mn (TCRmn) delayed by one period of  $f_{CLK}$  from rising edge of the count clock, because of synchronization with  $f_{CLK}$ . But, this is described as “counting at rising edge of the count clock”, as a matter of convenience.

**Figure 6-27. Timing of  $f_{CLK}$  and count clock ( $f_{TCLK}$ ) (When CCSmn = 1, noise filter unused)**



<1> Setting TSmn bit to 1 enables the timer to be started and to become wait state for valid edge of input signal via the TImn pin.

<2> The rise of input signal via the TImn pin is sampled by  $f_{MCK}$ .

<3> The edge is detected by the rising of the sampled signal and the detection signal (count clock) is output.

**Remarks 1.**  $\Delta$  : Rising edge of the count clock

$\blacktriangle$  : Synchronization, increment/decrement of counter

**2.**  $f_{MCK}$ : Operation clock of channel n

**3.** The waveform of the input signal to TImn pin of the input pulse interval measurement, the measurement of high/low width of input signal, the delay counter, the one-shot pulse output is the same as that shown in **Figure 6-27**.

### 6.5.2 Start timing of counter

Timer count register mn (TCRmn) becomes enabled to operation by setting of TSmn bit of timer channel start register m (TSM).

Operations from count operation enabled state to timer count Register mn (TCRmn) count start is shown in Table 6-6.

<R> **Table 6-6. Operations from Count Operation Enabled State to Timer count Register mn (TCRmn) Count Start**

| Timer operation mode                                                           | Operation when TSmn = 1 is set                                                                                                                                                                                                                                                                                                                                                                                                                        |
|--------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <ul style="list-style-type: none"> <li>Interval timer mode</li> </ul>          | <p>No operation is carried out from start trigger detection (TSmn=1) until count clock generation.</p> <p>The first count clock loads the value of the TDRmn register to the TCRmn register and the subsequent count clock performs count down operation (see <b>6.5.3 (1) Operation of interval timer mode</b>).</p>                                                                                                                                 |
| <ul style="list-style-type: none"> <li>Event counter mode</li> </ul>           | <p>Writing 1 to the TSmn bit loads the value of the TDRmn register to the TCRmn register.</p> <p>If detect edge of TImn input. The subsequent count clock performs count down operation (see <b>6.5.3 (2) Operation of event counter mode</b>).</p>                                                                                                                                                                                                   |
| <ul style="list-style-type: none"> <li>Capture mode</li> </ul>                 | <p>No operation is carried out from start trigger detection (TSmn = 1) until count clock generation.</p> <p>The first count clock loads 0000H to the TCRmn register and the subsequent count clock performs count up operation (see <b>6.5.3 (3) Operation of capture mode (input pulse interval measurement)</b>).</p>                                                                                                                               |
| <ul style="list-style-type: none"> <li>One-count mode</li> </ul>               | <p>The waiting-for-start-trigger state is entered by writing 1 to the TSmn bit while the timer is stopped (TEmn = 0).</p> <p>No operation is carried out from start trigger detection until count clock generation.</p> <p>The first count clock loads the value of the TDRmn register to the TCRmn register and the subsequent count clock performs count down operation (see <b>6.5.3 (4) Operation of one-count mode</b>).</p>                     |
| <ul style="list-style-type: none"> <li>Capture &amp; one-count mode</li> </ul> | <p>The waiting-for-start-trigger state is entered by writing 1 to the TSmn bit while the timer is stopped (TEmn = 0).</p> <p>No operation is carried out from start trigger detection until count clock generation.</p> <p>The first count clock loads 0000H to the TCRmn register and the subsequent count clock performs count up operation (see <b>6.5.3 (5) Operation of capture &amp; one-count mode (high-level interval measurement)</b>).</p> |

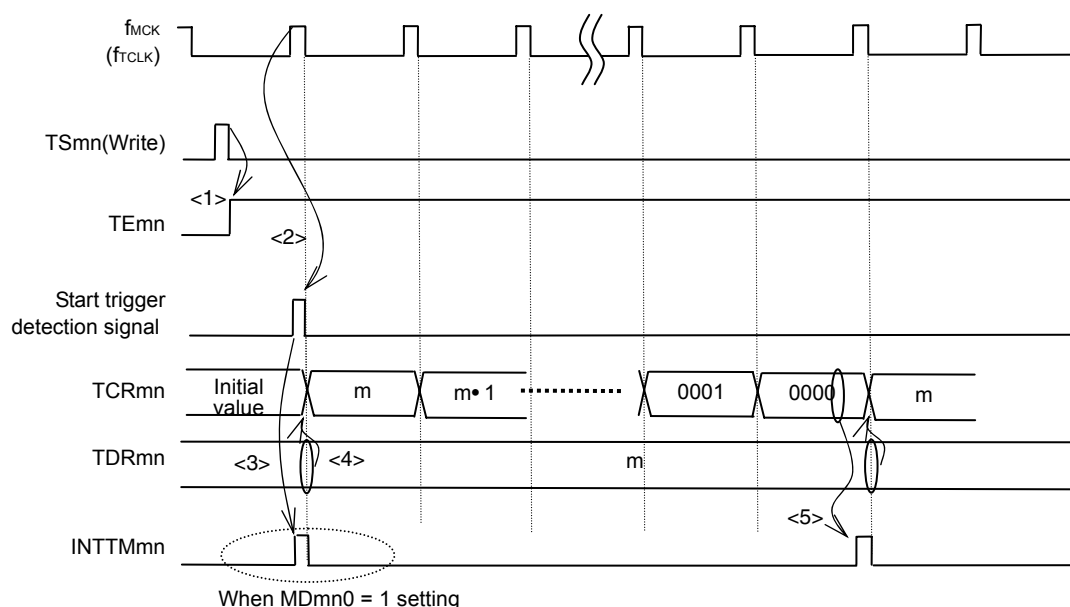
### <R> 6.5.3 Operation of counter

Here, the counter operation in each mode is explained.

#### (1) Operation of interval timer mode

- <1> Operation is enabled ( $TE_{mn} = 1$ ) by writing 1 to the  $TS_{mn}$  bit. Timer count register  $mn$  ( $TCR_{mn}$ ) holds the initial value until count clock generation.
- <2> A start trigger is generated at the first count clock after operation is enabled.
- <3> When the  $MD_{mn0}$  bit is set to 1,  $INTT_{Mmn}$  is generated by the start trigger.
- <4> By the first count clock after the operation enable, the value of timer data register  $mn$  ( $TDR_{mn}$ ) is loaded to the  $TCR_{mn}$  register and counting starts in the interval timer mode.
- <5> When the  $TCR_{mn}$  register counts down and its count value is 0000H,  $INTT_{Mmn}$  is generated and the value of timer data register  $mn$  ( $TDR_{mn}$ ) is loaded to the  $TCR_{mn}$  register and counting keeps on.

Figure 6-28. Operation Timing (In Interval Timer Mode)

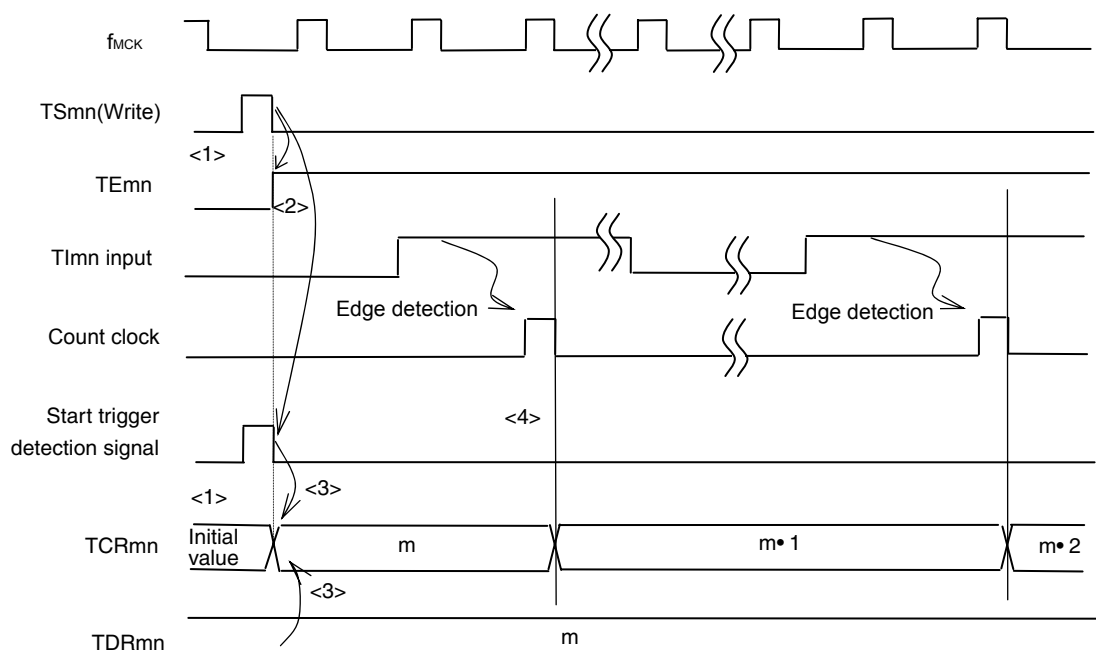


**Caution** In the first cycle operation of count clock after writing the  $TS_{mn}$  bit, an error at a maximum of one clock is generated since count start delays until count clock has been generated. When the information on count start timing is necessary, an interrupt can be generated at count start by setting  $MD_{mn0} = 1$ .

**Remark**  $f_{MCK}$ , the start trigger detection signal, and  $INTT_{Mmn}$  become active between one clock in synchronization with  $f_{CLK}$ .

**(2) Operation of event counter mode**

- <1> Timer count register mn (TCRmn) holds its initial value while operation is stopped ( $TE_{mn} = 0$ ).
- <2> Operation is enabled ( $TE_{mn} = 1$ ) by writing 1 to the TSmn bit.
- <3> As soon as 1 has been written to the TSmn bit and 1 has been set to the  $TE_{mn}$  bit, the value of timer data register mn (TDRmn) is loaded to the TCRmn register to start counting.
- <4> After that, the TCRmn register value is counted down according to the count clock of the valid edge of the TImn input.

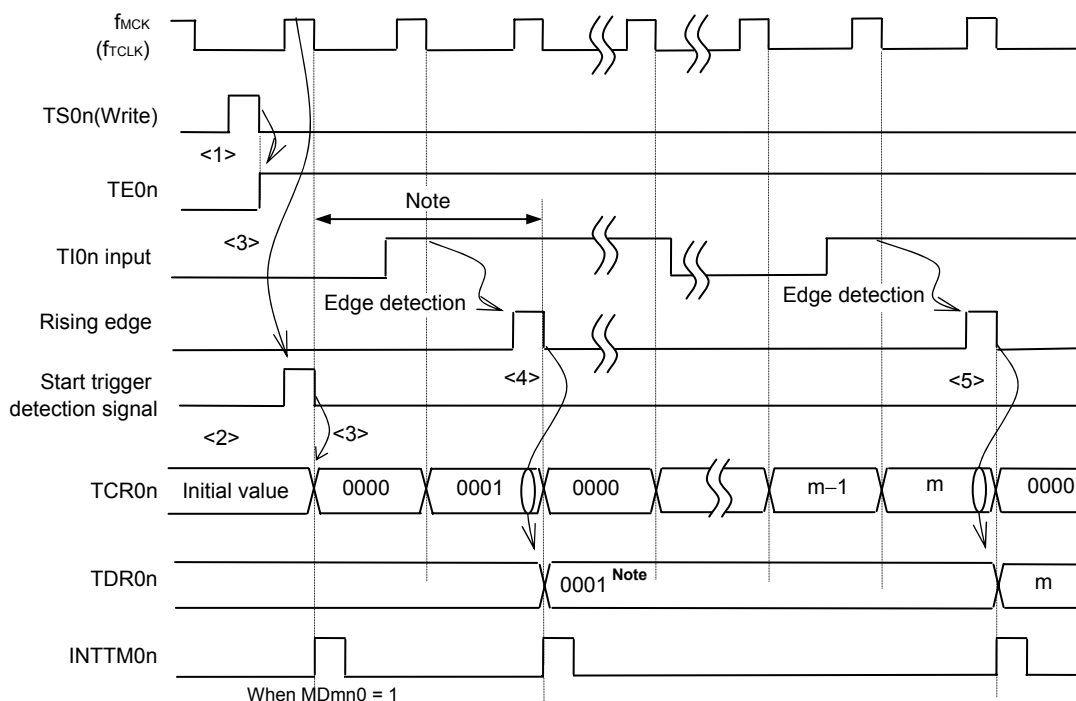
**Figure 6-29. Operation Timing (In Event Counter Mode)**

**Remark** The timing is shown in Figure 6-25 indicates while the noise filter is not used. By making the noise filter on-state, the edge detection becomes 2  $f_{MCK}$  cycles (it sums up to 3 to 4 cycles) later than the normal cycle of TImn input.

**(3) Operation of capture mode (input pulse interval measurement)**

- <1> Operation is enabled ( $TE_{mn} = 1$ ) by writing 1 to the  $TS_{mn}$  bit.
- <2> Timer count register  $mn$  ( $TCR_{mn}$ ) holds the initial value until count clock generation.
- <3> A start trigger is generated at the first count clock after operation is enabled. And the value of 0000H is loaded to the  $TCR_{mn}$  register and counting starts in the capture mode. (When the  $MD_{mn0}$  bit is set to 1,  $INTTM_{mn}$  is generated by the start trigger.)
- <4> On detection of the valid edge of the  $TI_{mn}$  input, the value of the  $TCR_{mn}$  register is captured to timer data register  $mn$  ( $TDR_{mn}$ ) and  $INTTM_{mn}$  is generated. However, this capture value is meaningless. The  $TCR_{mn}$  register keeps on counting from 0000H.
- <5> On next detection of the valid edge of the  $TI_{mn}$  input, the value of the  $TCR_{mn}$  register is captured to timer data register  $mn$  ( $TDR_{mn}$ ) and  $INTTM_{mn}$  is generated.

<R> **Figure 6-30. Operation Timing (In Capture Mode : Input Pulse Interval Measurement)**



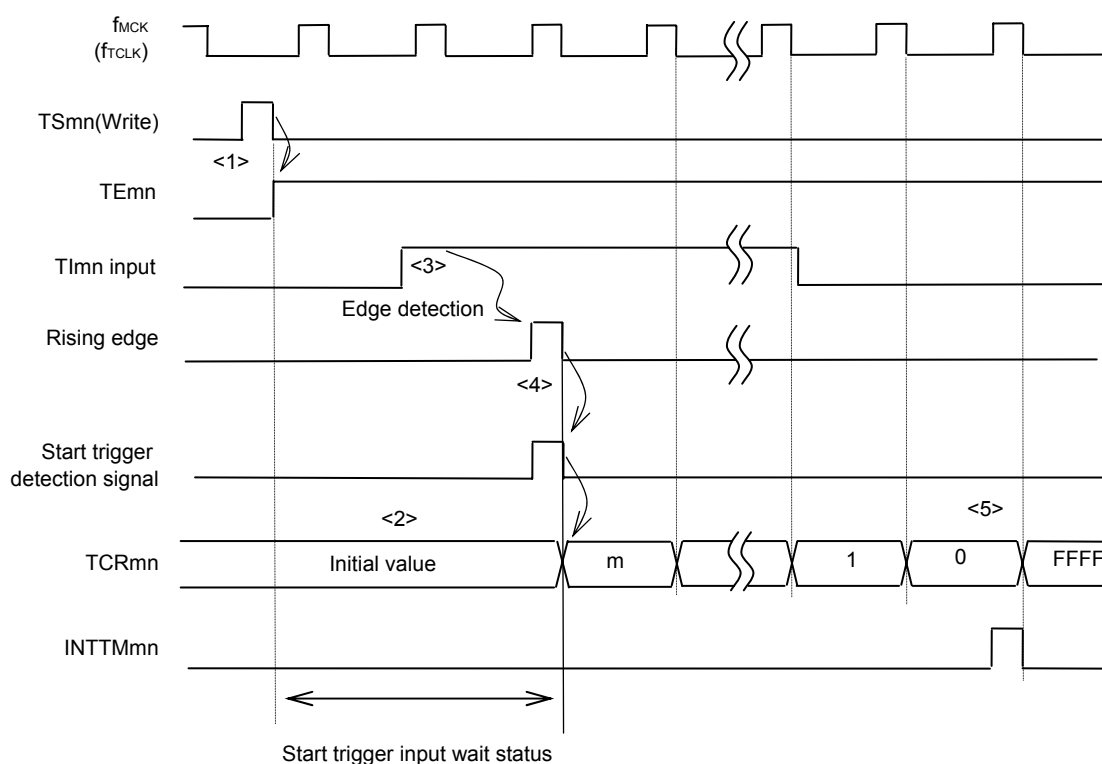
**Note** If a clock has been input to  $TI_{mn}$  (the trigger exists) when capturing starts, counting starts when a trigger is detected, even if no edge is detected. Therefore, the first captured value (<4>) does not determine a pulse interval (in the above figure, 0001 just indicates two clock cycles but does not determine the pulse interval) and so the user can ignore it.

**Caution** In the first cycle operation of count clock after writing the  $TS_{mn}$  bit, an error at a maximum of one clock is generated since count start delays until count clock has been generated. When the information on count start timing is necessary, an interrupt can be generated at count start by setting  $MD_{mn0} = 1$ .

**Remark** The timing is shown in Figure 6-25 indicates while the noise filter is not used. By making the noise filter on-state, the edge detection becomes  $2 f_{MCK}$  cycles (it sums up to 3 to 4 cycles) later than the normal cycle of  $TI_{mn}$  input.

**(4) Operation of one-count mode**

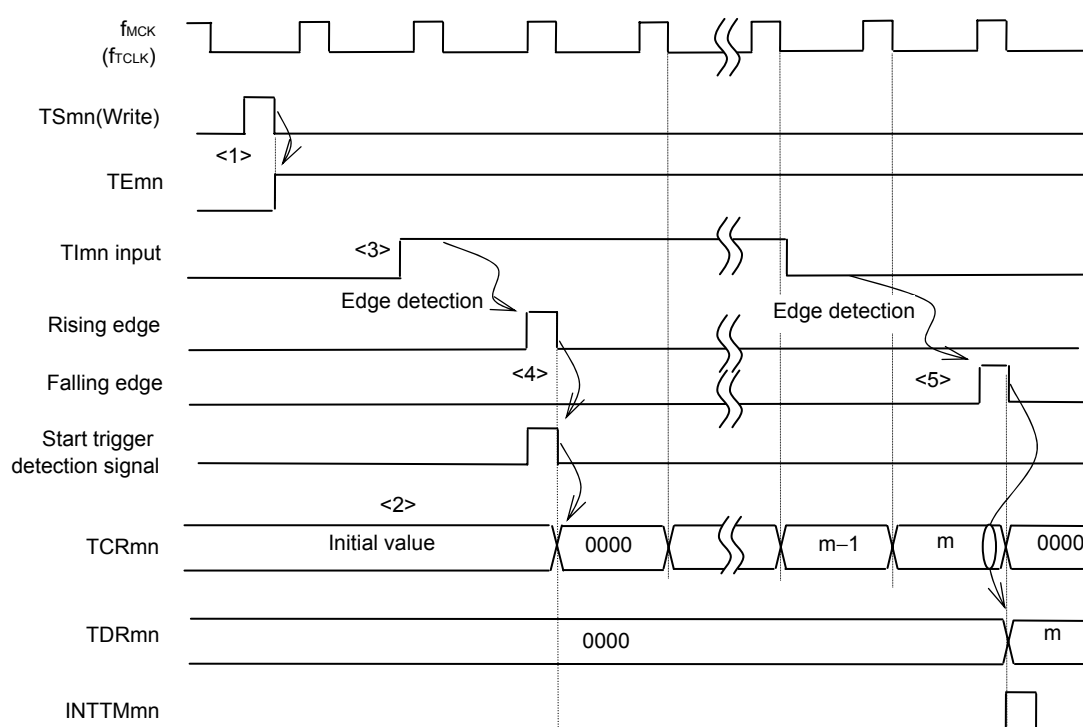
- <1> Operation is enabled ( $TE_{mn} = 1$ ) by writing 1 to the  $TS_{mn}$  bit.
- <2> Timer count register  $mn$  ( $TCR_{mn}$ ) holds the initial value until start trigger generation.
- <3> Rising edge of the  $TI_{mn}$  input is detected.
- <4> On start trigger detection, the value of timer data register  $mn$  ( $TDR_{mn}$ ) is loaded to the  $TCR_{mn}$  register and count starts.
- <5> When the  $TCR_{mn}$  register counts down and its count value is 0000H,  $INTTM_{mn}$  is generated and the value of the  $TCR_{mn}$  register becomes FFFFH and counting stops

**Figure 6-31. Operation Timing (In One-count Mode)**

**Remark** The timing is shown in Figure 6-27 indicates while the noise filter is not used. By making the noise filter on-state, the edge detection becomes 2  $f_{MCK}$  cycles (it sums up to 3 to 4 cycles) later than the normal cycle of  $TI_{mn}$  input. The error per one period occurs be the asynchronous between the period of the  $TI_{mn}$  input and that of the count clock ( $f_{MCK}$ ).

**(5) Operation of capture & one-count mode (high-level width measurement)**

- <1> Operation is enabled ( $TE_{mn} = 1$ ) by writing 1 to the  $TS_{mn}$  bit of timer channel start register  $m$  ( $TS_m$ ).
- <2> Timer count register  $mn$  ( $TCR_{mn}$ ) holds the initial value until start trigger generation.
- <3> Rising edge of the  $TI_{mn}$  input is detected.
- <4> On start trigger detection, the value of 0000H is loaded to the  $TCR_{mn}$  register and count starts.
- <5> On detection of the falling edge of the  $TI_{mn}$  input, the value of the  $TCR_{mn}$  register is captured to timer data register  $mn$  ( $TDR_{mn}$ ) and  $INTTM_{mn}$  is generated.

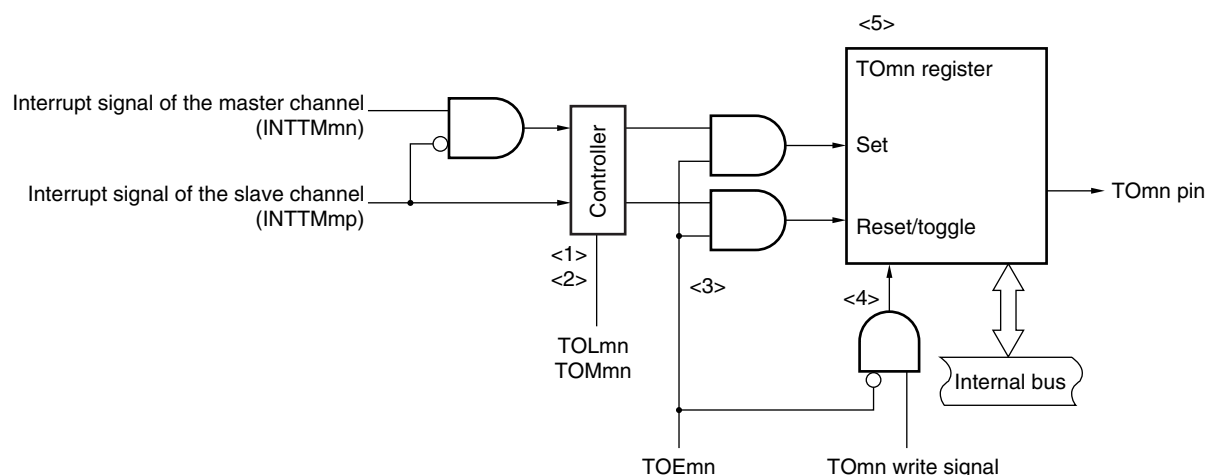
**Figure 6-32. Operation Timing (In Capture & One-count Mode : High-level Width Measurement)**

**Remark** The timing is shown in Figure 6-28 indicates while the noise filter is not used. By making the noise filter on-state, the edge detection becomes 2  $f_{MCK}$  cycles (it sums up to 3 to 4 cycles) later than the normal cycle of  $TI_{mn}$  input. The error per one period occurs be the asynchronous between the period of the  $TI_{mn}$  input and that of the count clock ( $f_{MCK}$ ).

## 6.6 Channel Output (TOMn pin) Control

### 6.6.1 TOMn pin output circuit configuration

Figure 6-33. Output Circuit Configuration



The following describes the TOMn pin output circuit.

- <1> When TOMmn = 0 (master channel output mode), the set value of timer output level register m (TOLm) is ignored and only INTTM0p (slave channel timer interrupt) is transmitted to timer output register m (TOM).
- <2> When TOMmn = 1 (slave channel output mode), both INTTMmn (master channel timer interrupt) and INTTM0p (slave channel timer interrupt) are transmitted to the TOM register.  
At this time, the TOLm register becomes valid and the signals are controlled as follows:

When TOLmn = 0: Positive logic output (INTTMmn → set, INTTM0p → reset)

When TOLmn = 1: Negative logic output (INTTMmn → reset, INTTM0p → set)

When INTTMmn and INTTM0p are simultaneously generated, (0% output of PWM), INTTM0p (reset signal) takes priority, and INTTMmn (set signal) is masked.

- <3> While timer output is enabled (TOEmn = 1), INTTMmn (master channel timer interrupt) and INTTM0p (slave channel timer interrupt) are transmitted to the TOM register. Writing to the TOM register (TOMn write signal) becomes invalid.

When TOEmn = 1, the TOMn pin output never changes with signals other than interrupt signals.

To initialize the TOMn pin output level, it is necessary to set timer operation is stoped (TOEmn = 0) and to write a value to the TOM register.

- <4> While timer output is disabled (TOEmn = 0), writing to the TOMn bit to the target channel (TOMn write signal) becomes valid. When timer output is disabled (TOEmn = 0), neither INTTMmn (master channel timer interrupt) nor INTTM0p (slave channel timer interrupt) is transmitted to the TOM register.
- <5> The TOM register can always be read, and the TOMn pin output level can be checked.

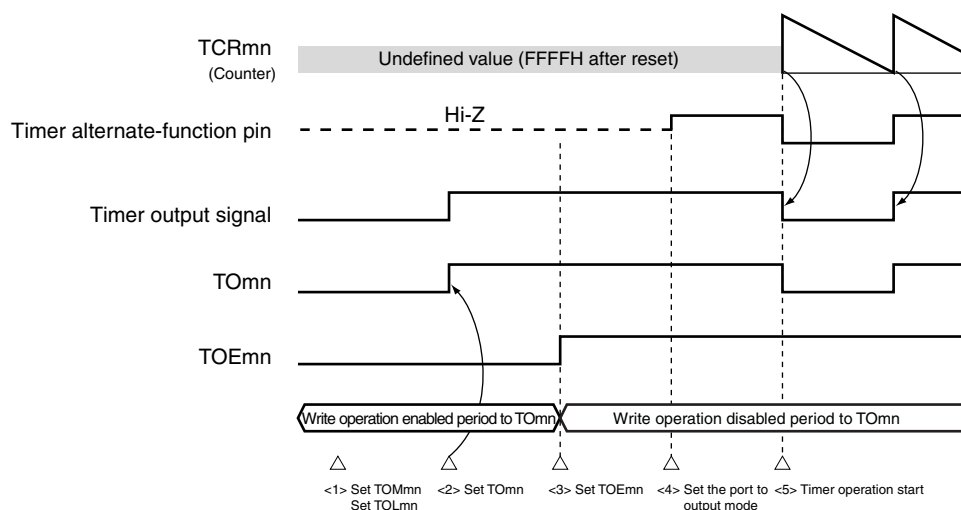
**Remark** m: Unit number (m = 0)  
 n: Channel number  
 n = 0 to 7 (n = 0, 2, 4, 6 for master channel)  
 p: Slave channel number  
 n < p ≤ 7



### 6.6.2 TOMn Pin Output Setting

The following figure shows the procedure and status transition of the TOMn output pin from initial setting to timer operation start.

**Figure 6-34. Status Transition from Timer Output Setting to Operation Start**



<1> The operation mode of timer output is set.

- TOMmn bit (0: Master channel output mode, 1: Slave channel output mode)
- TOLmn bit (0: Positive logic output, 1: Negative logic output)

<2> The timer output signal is set to the initial status by setting timer output register m (TOM).

<3> The timer output operation is enabled by writing 1 to the TOEmn bit (writing to the TOM register is disabled).

<R> <4> The port is set to digital I/O by port mode control register (PMCxx) (see **6.3.16 Port mode registers 1, 3 to 5, 14 (PM1, PM3 to PM5, PM14)**).

<5> The port I/O setting is set to output (see **6.3.16 Port mode registers 1, 3 to 5, 14 (PM1, PM3 to PM5, PM14)**).

<6> The timer operation is enabled (TSMn = 1).

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

### 6.6.3 Cautions on Channel Output Operation

#### (1) Changing values set in the registers T<sub>Om</sub>, T<sub>OEm</sub>, and T<sub>OLm</sub> during timer operation

Since the timer operations (operations of timer count register mn (TCR<sub>mn</sub>) and timer data register mn (TDR<sub>mn</sub>)) are independent of the T<sub>Om</sub>n output circuit and changing the values set in timer output register m (T<sub>Om</sub>), timer output enable register m (T<sub>OEm</sub>), and timer output level register m (T<sub>OLm</sub>), does not affect the timer operation, the values can be changed during timer operation. To output an expected waveform from the T<sub>Om</sub>n pin by timer operation, however, set the T<sub>Om</sub>, T<sub>OEm</sub>, and T<sub>OLm</sub> registers to the values stated in the register setting example of each operation shown by **6.7** and **6.8**.

When the values set to the T<sub>OEm</sub>, and T<sub>OLm</sub> registers (but not the T<sub>Om</sub> register) are changed close to the occurrence of the timer interrupt (INTT<sub>Mmn</sub>) of each channel, the waveform output to the T<sub>Om</sub>n pin might differ, depending on whether the values are changed immediately before or immediately after the timer interrupt (INTT<sub>Mmn</sub>) occurs.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

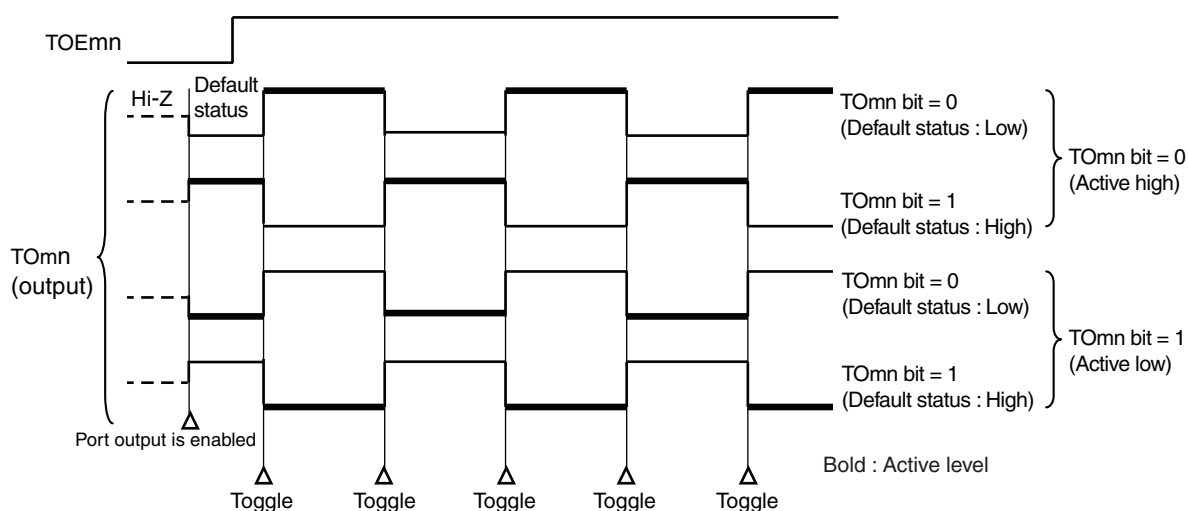
**(2) Default level of TOMn pin and output level after timer operation start**

The change in the output level of the TOMn pin when timer output register m (TOM) is written while timer output is disabled (TOEmn = 0), the initial level is changed, and then timer output is enabled (TOEmn = 1) before port output is enabled, is shown below.

**(a) When operation starts with master channel output mode (TOMmn = 0) setting**

The setting of timer output level register m (TOLm) is invalid when master channel output mode (TOMmn = 0). When the timer operation starts after setting the default level, the toggle signal is generated and the output level of the TOMn pin is reversed.

&lt;R&gt;

**Figure 6-35. TOMn Pin Output Status at Toggle Output (TOMmn = 0)**

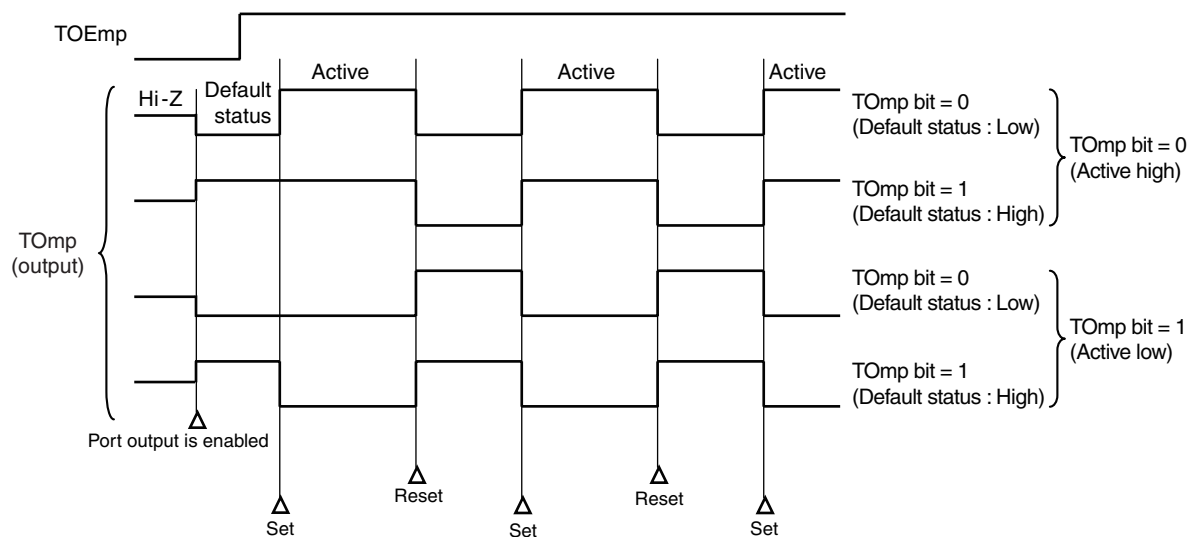
**Remarks 1.** Toggle: Reverse TOMn pin output status

**2.** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

**(b) When operation starts with slave channel output mode (TOMmp = 1) setting (PWM output)**

When slave channel output mode (TOMmp = 1), the active level is determined by timer output level register m (TOLm) setting.

&lt;R&gt;

**Figure 6-36. TOmn Pin Output Status at PWM Output (TOMmp = 1)**

**Remarks 1.** Set: The output signal of the TOmp pin changes from inactive level to active level.

Reset: The output signal of the TOmp pin changes from active level to inactive level.

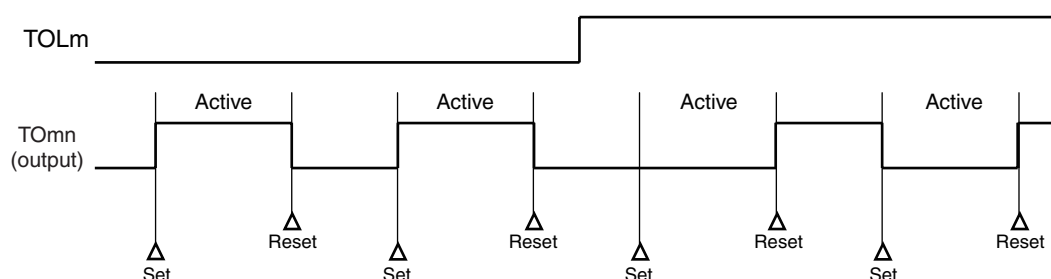
2. m: Unit number (m = 0), n: Channel number (p = 1 to 7)

**(3) Operation of TOMn pin in slave channel output mode (TOMmn = 1)****(a) When timer output level register m (TOLm) setting has been changed during timer operation**

When the TOLm register setting has been changed during timer operation, the setting becomes valid at the generation timing of the TOMn pin change condition. Rewriting the TOLm register does not change the output level of the TOMn pin.

The operation when TOMmn is set to 1 and the value of the TOLm register is changed while the timer is operating (TEMn = 1) is shown below.

&lt;R&gt;

**Figure 6-37. Operation when TOLm Register Has Been Changed during Timer Operation**

**Remarks 1.** Set: The output signal of the TOMn pin changes from inactive level to active level.

Reset: The output signal of the TOMn pin changes from active level to inactive level.

2. m: Unit number (m = 0), n: Channel number (n = 0 to 7)

**(b) Set/reset timing**

To realize 0%/100% output at PWM output, the TOMn pin/TOMn bit set timing at master channel timer interrupt (INTTMmn) generation is delayed by 1 count clock by the slave channel.

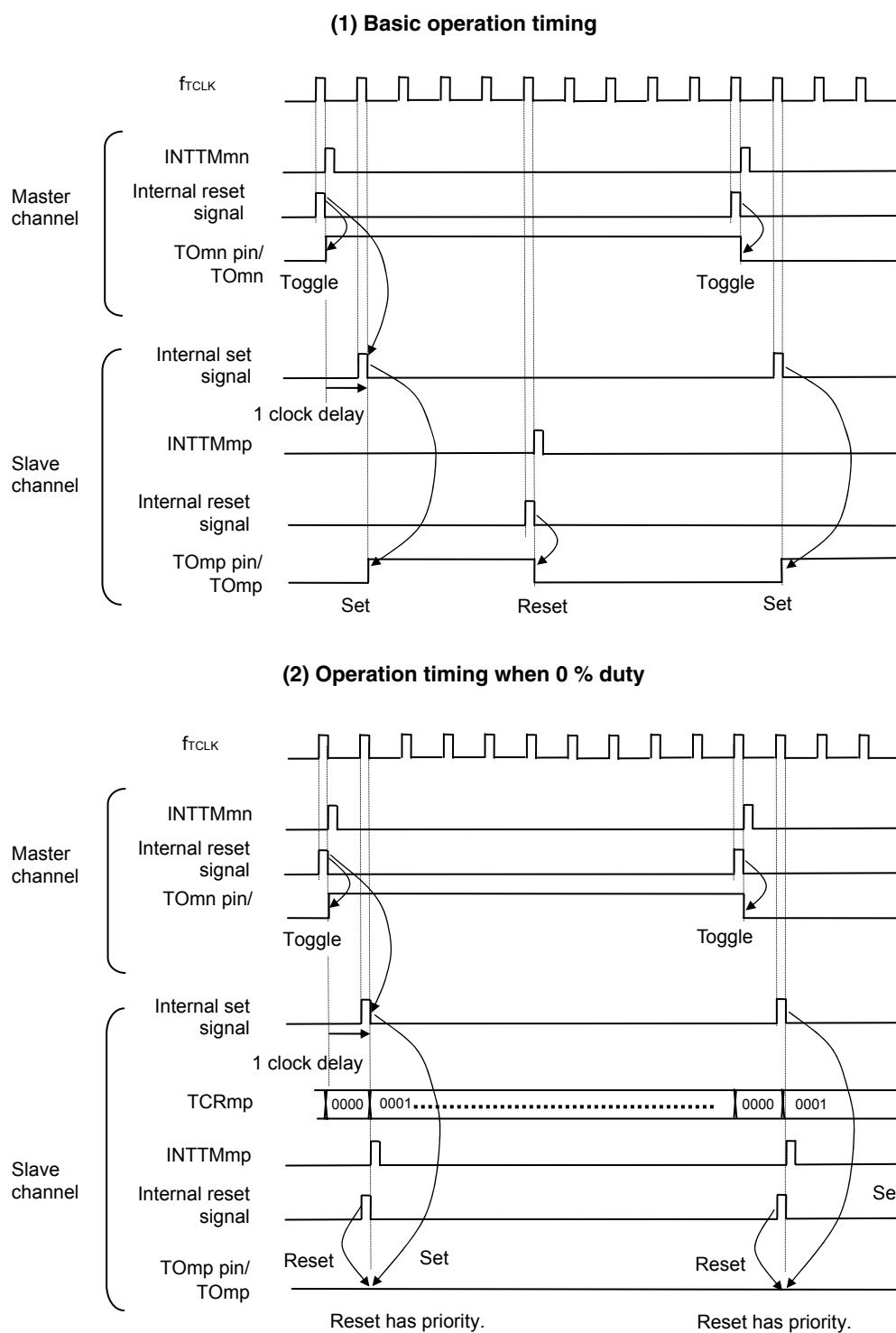
If the set condition and reset condition are generated at the same time, a higher priority is given to the latter.

Figure 6-38 shows the set/reset operating statuses where the master/slave channels are set as follows.

Master channel: TOEmn = 1, TOMmn = 0, TOLmn = 0

Slave channel: TOEmp = 1, TOMmp = 1, TOLmp = 0

Figure 6-38. Set/Reset Timing Operating Statuses



**Remarks 1.** Internal reset signal: TOn pin reset/toggle signal

Internal set signal: TOn pin set signal

**2.** m: Unit number (m = 0)

n: Channel number (n = 0 to 7)

n = 0 to 7 (n = 0, 2, 4, 6 for master channel)

p: Slave channel number

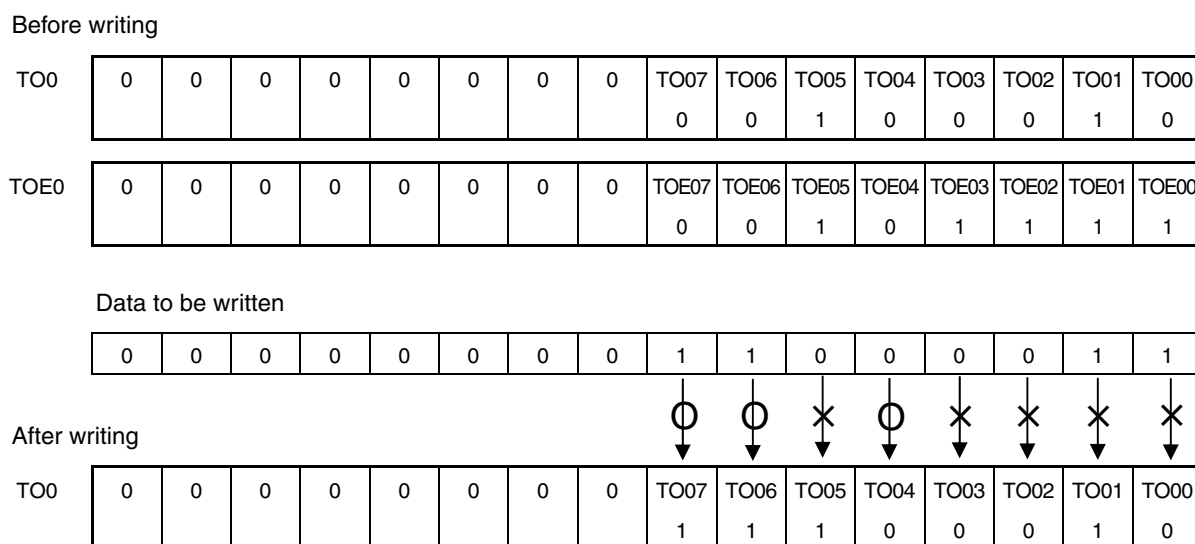
$n < p \leq 7$

### 6.6.4 Collective manipulation of TOMn bit

In timer output register m (TOM), the setting bits for all the channels are located in one register in the same way as timer channel start register m (TSM). Therefore, the TOMn bit of all the channels can be manipulated collectively.

Only the desired bits can also be manipulated by enabling writing only to the TOMn bits (TOEmn = 0) that correspond to the relevant bits of the channel used to perform output (TOMn).

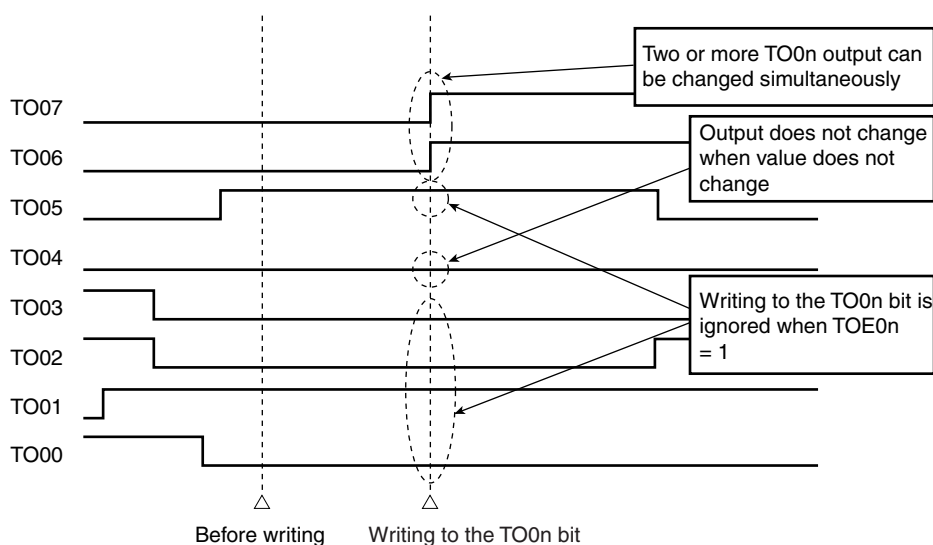
**Figure 6-39 Example of TO0n Bit Collective Manipulation**



Writing is done only to the TOMn bit with TOEmn = 0, and writing to the TOMn bit with TOEmn = 1 is ignored.

TOMn (channel output) to which TOEmn = 1 is set is not affected by the write operation. Even if the write operation is done to the TOMn bit, it is ignored and the output change by timer operation is normally done.

**Figure 6-40. TO0n Pin Statuses by Collective Manipulation of TO0n Bit**



(Caution and Remark are given on the next page.)

**Caution** While timer output is enabled ( $TOEmn = 1$ ), even if the output by timer interrupt of each timer ( $INTTMmn$ ) contends with writing to the  $TOmn$  bit, output is normally done to the  $TOmn$  pin.

**Remark** m: Unit number ( $m = 0$ ), n: Channel number ( $n = 0$  to 7)

### 6.6.5 Timer Interrupt and $TOmn$ Pin Output at Operation Start

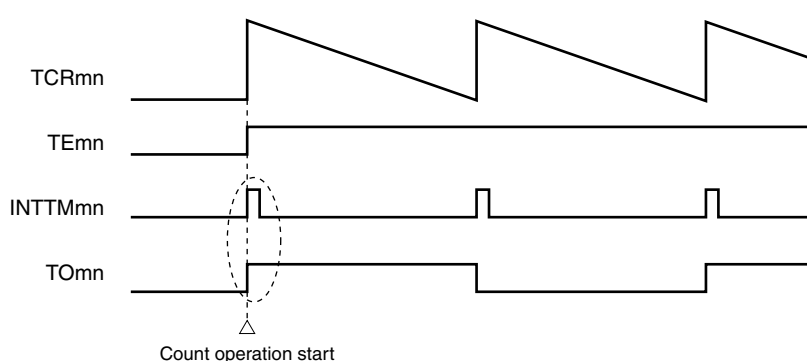
In the interval timer mode or capture mode, the  $MDmn0$  bit in timer mode register mn ( $TMRmn$ ) sets whether or not to generate a timer interrupt at count start.

When  $MDmn0$  is set to 1, the count operation start timing can be known by the timer interrupt ( $INTTMmn$ ) generation.

In the other modes, neither timer interrupt at count operation start nor  $TOmn$  output is controlled.

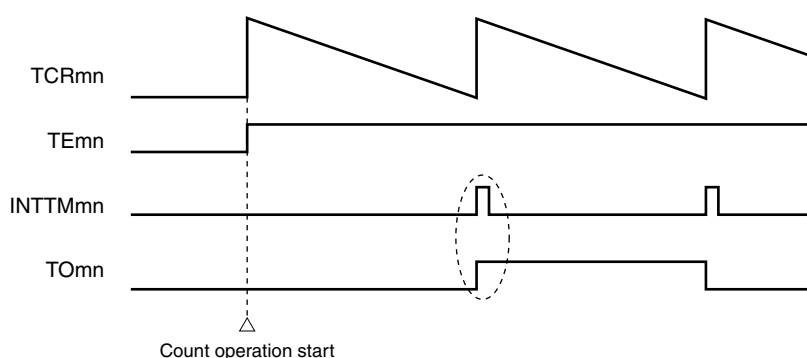
Figures 6-41 and 6-42 show operation examples when the interval timer mode ( $TOEmn = 1$ ,  $TOMmn = 0$ ) is set.

**Figure 6-41. When  $MDmn0$  is set to 1**



When  $MDmn0$  is set to 1, a timer interrupt ( $INTTMmn$ ) is output at count operation start, and  $TOmn$  performs a toggle operation.

**Figure 6-42. When  $MDmn0$  is set to 0**



When  $MDmn0$  is set to 1, a timer interrupt ( $INTTMmn$ ) is output at count operation start, and  $TOmn$  performs a toggle operation.

When  $MDmn0$  is set to 0, a timer interrupt ( $INTTMmn$ ) is not output at count operation start, and  $TOmn$  does not change either. After counting one cycle,  $INTTMmn$  is output and  $TOmn$  performs a toggle operation.

**Remark** m: Unit number ( $m = 0$ ), n: Channel number ( $n = 0$  to 7)



## 6.7 Independent Channel Operation Function of Timer Array Unit

### 6.7.1 Operation as interval timer/square wave output

#### (1) Interval timer

The timer array unit can be used as a reference timer that generates INTTMmn (timer interrupt) at fixed intervals. The interrupt generation period can be calculated by the following expression.

|                                                                                                                               |
|-------------------------------------------------------------------------------------------------------------------------------|
| $\text{Generation period of INTTMmn (timer interrupt)} = \text{Period of count clock} \times (\text{Set value of TDRmn} + 1)$ |
|-------------------------------------------------------------------------------------------------------------------------------|

#### (2) Operation as square wave output

TOMn performs a toggle operation as soon as INTTMmn has been generated, and outputs a square wave with a duty factor of 50%.

The period and frequency for outputting a square wave from TOMn can be calculated by the following expressions.

|                                                                                                                                                                                       |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <ul style="list-style-type: none"> <li>• Period of square wave output from TOMn = Period of count clock <math>\times</math> (Set value of TDRmn + 1) <math>\times</math> 2</li> </ul> |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

|                                                                                                                                                                             |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <ul style="list-style-type: none"> <li>• Frequency of square wave output from TOMn = Frequency of count clock / {(Set value of TDRmn + 1) <math>\times</math> 2}</li> </ul> |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

Timer count register mn (TCRmn) operates as a down counter in the interval timer mode.

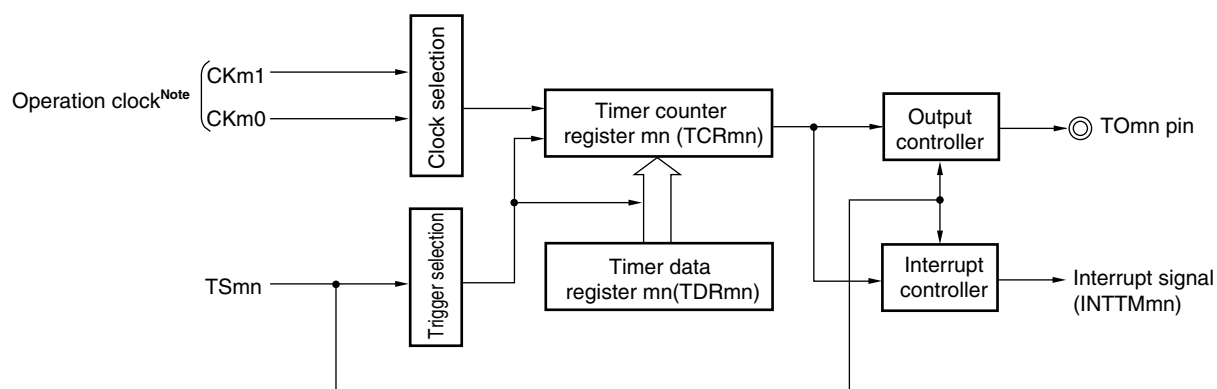
The TCRmn register loads the value of timer data register mn (TDRmn) at the first count clock after the channel start trigger bit (TSmn, TSHm1, TSHm3) of timer channel start register m (TSM) is set to 1. If the MDmn0 bit of timer mode register mn (TMRmn) is 0 at this time, INTTMmn is not output and TOMn is not toggled. If the MDmn0 bit of the TMRmn register is 1, INTTMmn is output and TOMn is toggled.

After that, the TCRmn register count down in synchronization with the count clock.

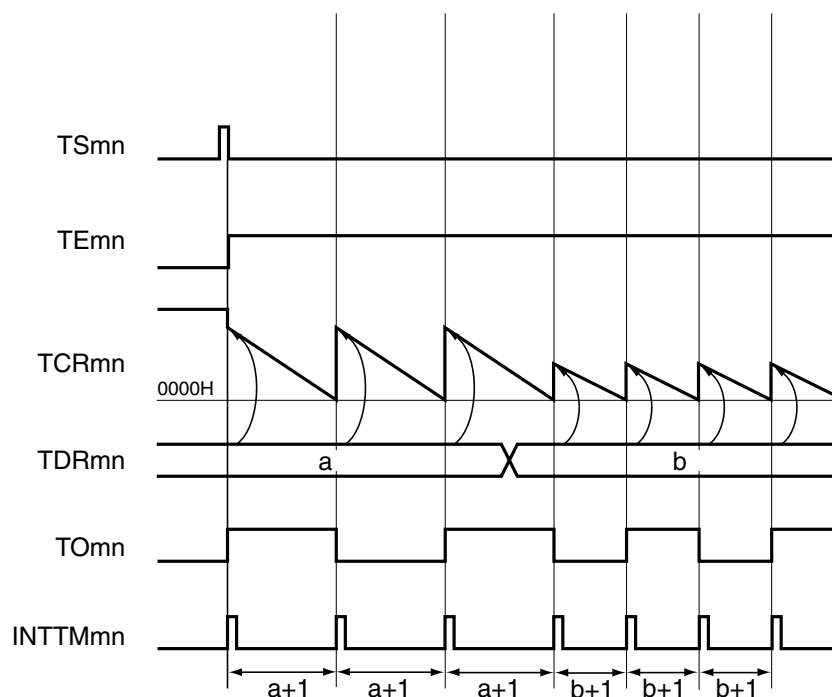
When TCRmn = 0000H, INTTMmn is output and TOMn is toggled at the next count clock. At the same time, the TCRmn register loads the value of the TDRmn register again. After that, the same operation is repeated.

The TDRmn register can be rewritten at any time. The new value of the TDRmn register becomes valid from the next period.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

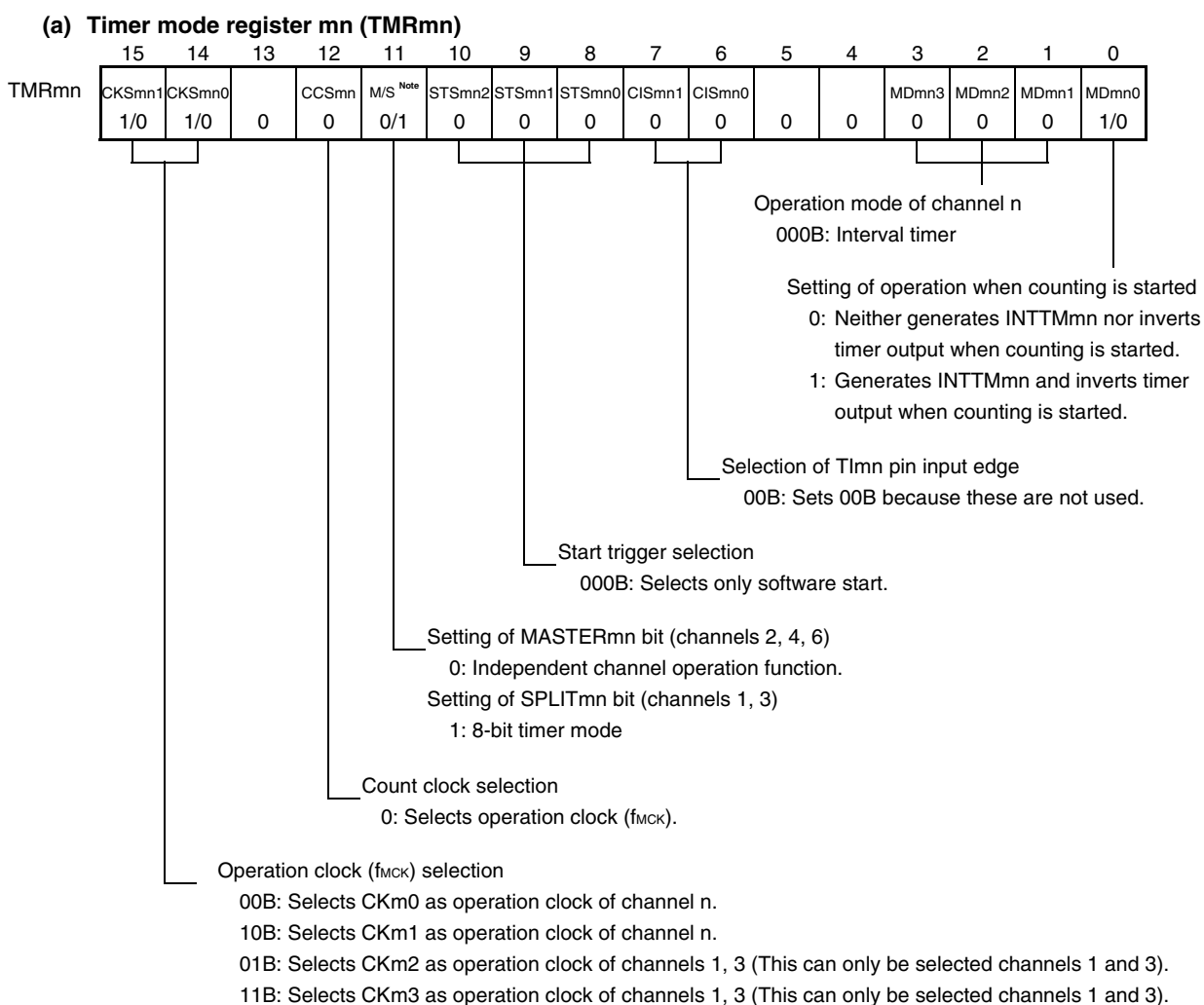
**Figure 6-43. Block Diagram of Operation as Interval Timer/Square Wave Output**

**Note** When channels 1 and 3, the clock can be selected from CKm0, CKm1, CKm2 and CKm3.

**Figure 6-44. Example of Basic Timing of Operation as Interval Timer/Square Wave Output (MDmn0 = 1)**

- Remarks**
1. m: Unit number (m = 0), n: Channel number (n = 0 to 7)
  2. TSmn: Bit n of timer channel start register m (TSm)  
 TEmn: Bit n of timer channel enable status register m (TEm)  
 TCRmn: Timer count register mn (TCRmn)  
 TDRmn: Timer data register mn (TDRmn)  
 TOMn: TOMn pin output signal

Figure 6-45. Example of Set Contents of Registers During Operation as Interval Timer/Square Wave Output (1/2)



## (b) Timer output register m (TOM)

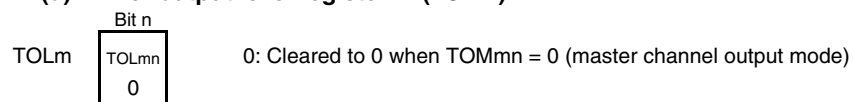
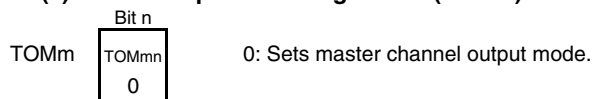
|     |       |                         |
|-----|-------|-------------------------|
| TOM | Bit n |                         |
|     | TOMn  | 0: Outputs 0 from TOMn. |
|     | 1/0   | 1: Outputs 1 from TOMn. |

## (c) Timer output enable register m (TOEm)

|      |       |                                                             |
|------|-------|-------------------------------------------------------------|
| TOEm | Bit n |                                                             |
|      | TOEmn | 0: Stops the TOMn output operation by counting operation.   |
|      | 1/0   | 1: Enables the TOMn output operation by counting operation. |

**Note** TMRm2, TMRm4, TMRm6: MASTERmn bit  
 TMRm1, TMRm3: SPLITmn bit  
 TMRm0, TMRm5, TMRm7: Fixed to 0

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

**Figure 6-45. Example of Set Contents of Registers During Operation as Interval Timer/Square Wave Output (2/2)****(d) Timer output level register m (TOLm)****(e) Timer output mode register m (TOMm)**

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Figure 6-46. Operation Procedure of Interval Timer/Square Wave Output Function (1/2)

|                         | Software Operation                                                                                                                                                                                                                                                     | Hardware Status                                                                                                                                                                                                                                                                                                  |
|-------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TAU default setting     |                                                                                                                                                                                                                                                                        | Power-off status<br>(Clock supply is stopped and writing to each register is disabled.)                                                                                                                                                                                                                          |
|                         | Sets the TAU0EN bit of peripheral enable register 0 (PER0) to 1.                                                                                                                                                                                                       | Power-on status. Each channel stops operating.<br>(Clock supply is started and writing to each register is enabled.)                                                                                                                                                                                             |
|                         | Sets timer clock select register m (TPSm).<br>Determines clock frequencies of CKm0 to CKm3.                                                                                                                                                                            |                                                                                                                                                                                                                                                                                                                  |
| Channel default setting | Sets timer mode register mn (TMRmn) (determines operation mode of channel).<br>Sets interval (period) value to timer data register mn (TDRmn).                                                                                                                         | Channel stops operating.<br>(Clock is supplied and some power is consumed.)                                                                                                                                                                                                                                      |
|                         | To use the TOMn output<br>Clears the TOMmn bit of timer output mode register m (TOMm) to 0 (master channel output mode).<br>Clears the TOLmn bit to 0.<br>Sets the TOMn bit and determines default level of the TOMn output.                                           | The TOMn pin goes into Hi-Z output state.                                                                                                                                                                                                                                                                        |
|                         | Sets the TOEmn bit to 1 and enables operation of TOMn.<br>Clears the port register and port mode register to 0.                                                                                                                                                        | The TOMn default setting level is output when the port mode register is in the output mode and the port register is 0.<br>TOMn does not change because channel stops operating.<br>The TOMn pin outputs the TOMn set level.                                                                                      |
| Operation start         | (Sets the TOEmn bit to 1 only if using TOMn output and resuming operation.).<br>Sets the TSmn (TSHm1, TSHm3) bit to 1.<br>The TSmn (TSHm1, TSHm3) bit automatically returns to 0 because it is a trigger bit.                                                          | TEmn (TEHm1, TEHm3) = 1, and count operation starts.<br>Value of the TDRmn register is loaded to timer count register mn (TCRmn) at the count clock input. INTTMmn is generated and TOMn performs toggle operation if the MDmn0 bit of the TMRmn register is 1.                                                  |
| During operation        | Set values of the TMRmn register, TOMmn, and TOLmn bits cannot be changed.<br>Set value of the TDRmn register can be changed.<br>The TCRmn register can always be read.<br>The TSRmn register is not used.<br>Set values of the TOM and TOEm registers can be changed. | Counter (TCRmn) counts down. When count value reaches 0000H, the value of the TDRmn register is loaded to the TCRmn register again and the count operation is continued.<br>By detecting TCRmn = 0000H, INTTMmn is generated and TOMn performs toggle operation.<br>After that, the above operation is repeated. |
| Operation stop          | The TTmn (TTHm1, TTHm3) bit is set to 1.<br>The TTmn (TTHm1, TTHm3) bit automatically returns to 0 because it is a trigger bit.                                                                                                                                        | TEmn (TEHm1, TEHm3), and count operation stops.<br>The TCRmn register holds count value and stops.<br>The TOMn output is not initialized but holds current status.                                                                                                                                               |
|                         | The TOEmn bit is cleared to 0 and value is set to the TOMn bit.                                                                                                                                                                                                        | The TOMn pin outputs the TOMn bit set level.                                                                                                                                                                                                                                                                     |

Operation is resumed.

(Remark is listed on the next page.)

**Figure 6-46. Operation Procedure of Interval Timer/Square Wave Output Function (2/2)**

|             | Software Operation                                                                                                                                                                                                                   | Hardware Status                                                                                                                                                                        |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TAU<br>stop | <p>To hold the TOMn pin output level<br/>Clears the TOMn bit to 0 after the value to<br/>be held is set to the port register. —————&gt;</p> <p>When holding the TOMn pin output level is not necessary<br/>Setting not required.</p> | <p>The TOMn pin output level is held by port function.</p>                                                                                                                             |
|             | <p>The TAU0EN bit of the PER0 register is cleared to 0. —————&gt;</p>                                                                                                                                                                | <p>Power-off status<br/>All circuits are initialized and SFR of each channel is also<br/>initialized.<br/>(The TOMn bit is cleared to 0 and the TOMn pin is set to<br/>port mode.)</p> |

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

### 6.7.2 Operation as external event counter

The timer array unit can be used as an external event counter that counts the number of times the valid input edge (external event) is detected in the TImn pin. When a specified count value is reached, the event counter generates an interrupt. The specified number of counts can be calculated by the following expression.

$$\text{Specified number of counts} = \text{Set value of TDRmn} + 1$$

Timer count register mn (TCRmn) operates as a down counter in the event counter mode.

The TCRmn register loads the value of timer data register mn (TDRmn) by setting any channel start trigger bit (TSmn, TSHm1, TSHm3) of timer channel start register m (TSM) to 1.

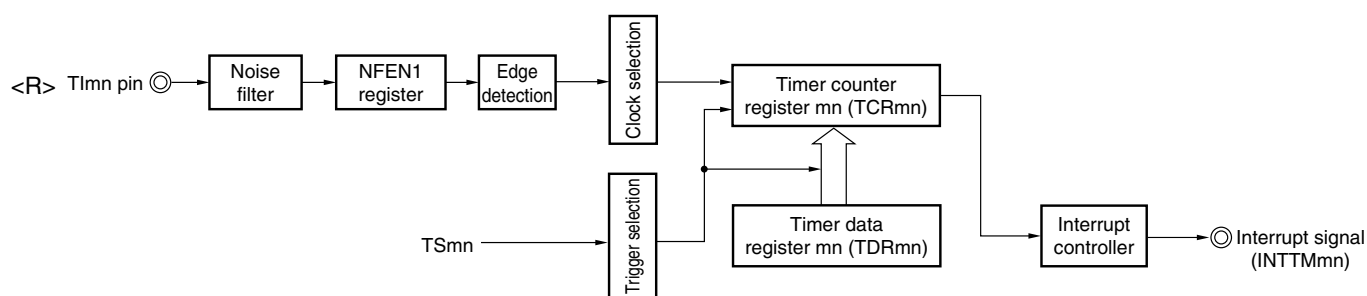
The TCRmn register counts down each time the valid input edge of the TImn pin has been detected. When TCRmn = 0000H, the TCRmn register loads the value of the TDRmn register again, and outputs INTTMmn.

After that, the above operation is repeated.

An irregular waveform that depends on external events is output from the TOMn pin. Stop the output by setting the TOEmn bit of timer output enable register m (TOEm) to 0.

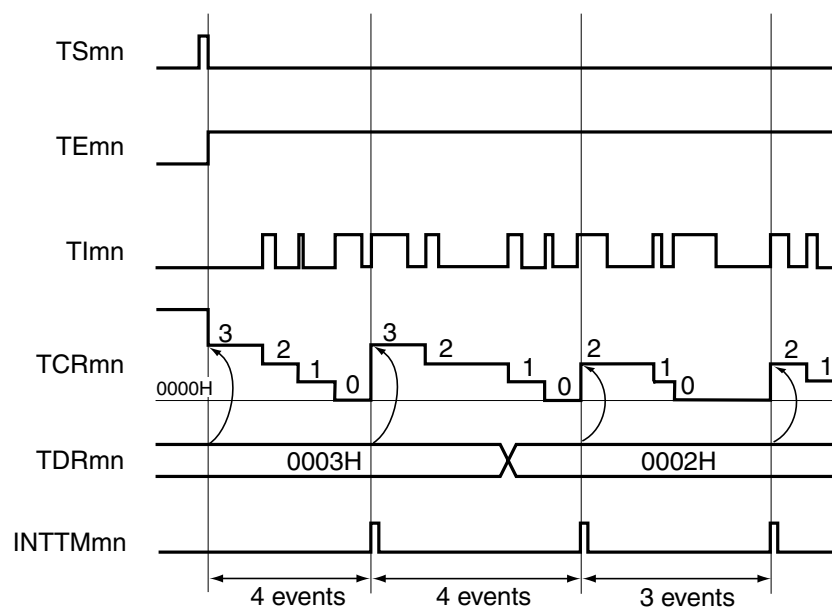
The TDRmn register can be rewritten at any time. The new value of the TDRmn register becomes valid during the next count period.

**Figure 6-47. Block Diagram of Operation as External Event Counter**



**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

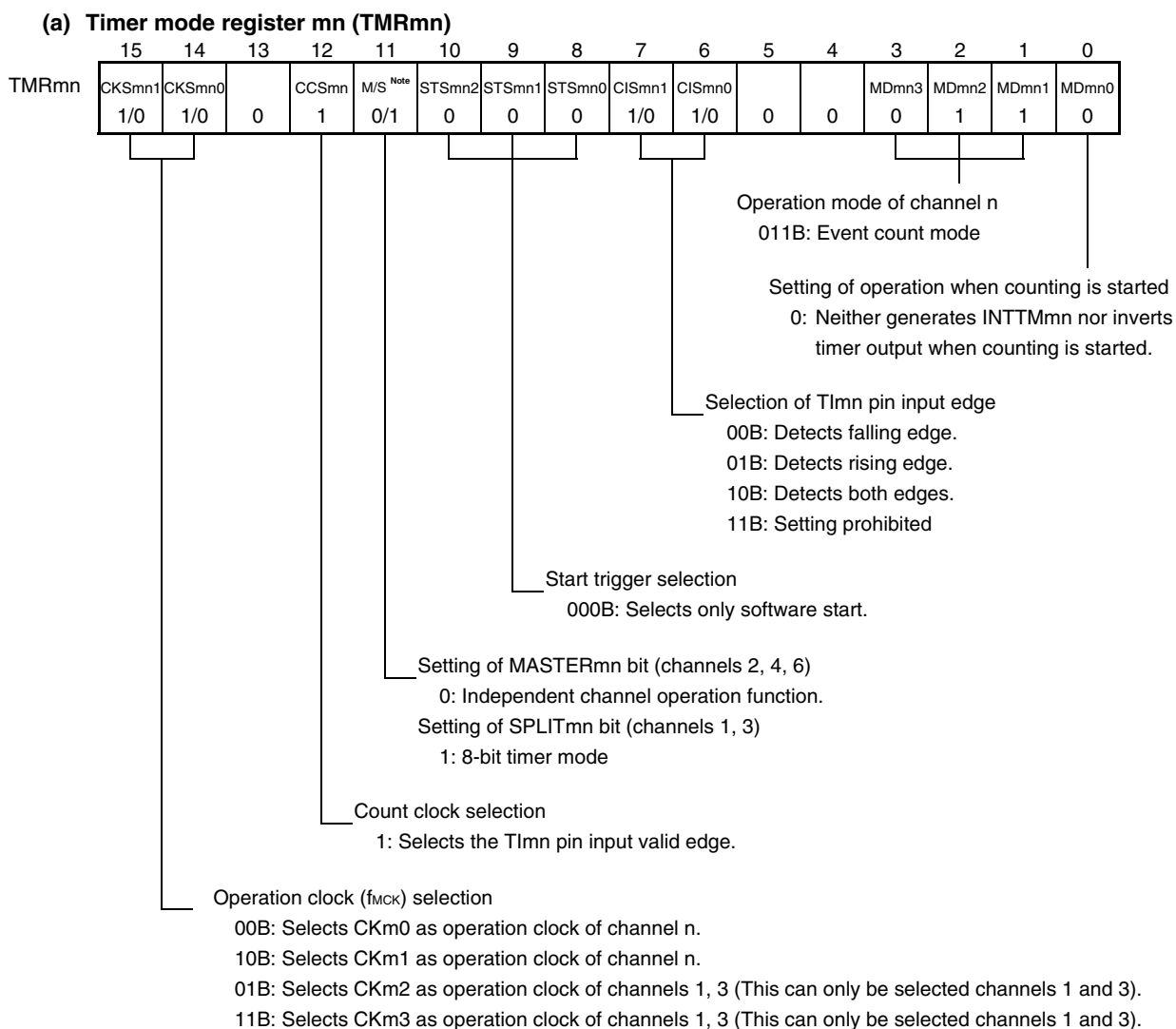
Figure 6-48. Example of Basic Timing of Operation as External Event Counter



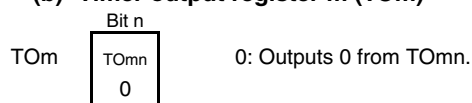
- Remarks**
1. m: Unit number (m = 0), n: Channel number (n = 0 to 7)
  2. TSmn: Bit n of timer channel start register m (TSm)  
 TEmn: Bit n of timer channel enable status register m (TEm)  
 TImn: TImn pin input signal  
 TCRmn: Timer count register mn (TCRmn)  
 TDRmn: Timer data register mn (TDRmn)



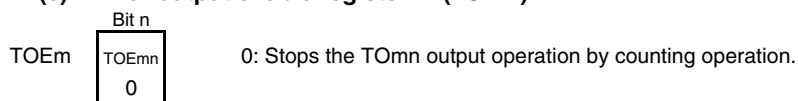
Figure 6-49. Example of Set Contents of Registers in External Event Counter Mode (1/2)



## (b) Timer output register m (TOM)



## (c) Timer output enable register m (TOEm)



**Note** TMRm2, TMRm4, TMRm6: MASTERmn bit  
 TMRm1, TMRm3: SPLITmn bit  
 TMRm0, TMRm5, TMRm7: Fixed to 0

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

**Figure 6-49. Example of Set Contents of Registers in External Event Counter Mode (2/2)****(d) Timer output level register m (TOLm)**

TOLm
 

|       |
|-------|
| Bit n |
| TOLmn |
| 0     |

 0: Cleared to 0 when TOMmn = 0 (master channel output mode).

**(e) Timer output mode register m (TOMm)**

TOMm
 

|       |
|-------|
| Bit n |
| TOMmn |
| 0     |

 0: Sets master channel output mode.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

**Figure 6-50. Operation Procedure When External Event Counter Function Is Used**

|                         | Software Operation                                                                                                                                                                                                                                                                                          | Hardware Status                                                                                                                                                                                                                                                                                                                               |
|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TAU default setting     |                                                                                                                                                                                                                                                                                                             | Power-off status<br>(Clock supply is stopped and writing to each register is disabled.)                                                                                                                                                                                                                                                       |
|                         | Sets the TAU0EN bit of peripheral enable register 0 (PER0) to 1.                                                                                                                                                                                                                                            | Power-on status. Each channel stops operating.<br>(Clock supply is started and writing to each register is enabled.)                                                                                                                                                                                                                          |
|                         | Sets timer clock select register m (TPSm).<br>Determines clock frequencies of CKm0 to CKm3.                                                                                                                                                                                                                 |                                                                                                                                                                                                                                                                                                                                               |
| Channel default setting | Sets timer mode register mn (TMRmn) (determines operation mode of channel).<br>Sets number of counts to timer data register mn (TDRmn).<br>Clears the TOEmn bit of timer output enable register m (TOEm) to 0.                                                                                              | Channel stops operating.<br>(Clock is supplied and some power is consumed.)                                                                                                                                                                                                                                                                   |
| Operation start         | Sets the TSMn bit to 1.<br>The TSMn bit automatically returns to 0 because it is a trigger bit.                                                                                                                                                                                                             | TEmn = 1, and count operation starts.<br>Value of the TDRmn register is loaded to timer count register mn (TCRmn) and detection of the TImn pin input edge is awaited.                                                                                                                                                                        |
| During operation        | Set value of the TDRmn register can be changed.<br>Sets corresponding bit of noise filter enable register 1, 2 (NFEN1, NFEN2) to 1.<br>The TCRmn register can always be read.<br>The TSRmn register is not used.<br>Set values of the TMRmn register, TOMmn, TOLmn, TOMn, and TOEmn bits cannot be changed. | Counter (TCRmn) counts down each time input edge of the TImn pin has been detected. When count value reaches 0000H, the value of the TDRmn register is loaded to the TCRmn register again, and the count operation is continued. By detecting TCRmn = 0000H, the INTTMmn output is generated.<br>After that, the above operation is repeated. |
| Operation stop          | The TTmn bit is set to 1.<br>The TTmn bit automatically returns to 0 because it is a trigger bit.                                                                                                                                                                                                           | TEmn = 0, and count operation stops.<br>The TCRmn register holds count value and stops.                                                                                                                                                                                                                                                       |
| TAU stop                | The TAU0EN bit of the PER0 register is cleared to 0.                                                                                                                                                                                                                                                        | Power-off status<br>All circuits are initialized and SFR of each channel is also initialized.                                                                                                                                                                                                                                                 |

Operation is resumed.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

### 6.7.3 Operation as frequency divider (channel 0 only)

The timer array unit can be used as a frequency divider that divides a clock input to the TI00 pin and outputs the result from the TO00 pin.

The divided clock frequency output from TO00 can be calculated by the following expression.

- When rising edge/falling edge is selected:  

$$\text{Divided clock frequency} = \text{Input clock frequency} / \{(\text{Set value of TDR00} + 1) \times 2\}$$
- When both edges are selected:  

$$\text{Divided clock frequency} \equiv \text{Input clock frequency} / (\text{Set value of TDR00} + 1)$$

Timer count register 00 (TCR00) operates as a down counter in the interval timer mode.

After the channel start trigger bit (TS00) of timer channel start register 0 (TS0) is set to 1, the TCR00 register loads the value of timer data register 00 (TDR00) when the TI00 valid edge is detected.

If the MD000 bit of timer mode register 00 (TMR00) is 0 at this time, INTTM00 is not output and TO00 is not toggled. If the MD000 bit of timer mode register 00 (TMR00) is 1, INTTM00 is output and TO00 is toggled.

After that, the TCR00 register counts down at the valid edge of the TI00 pin. When TCR00 = 0000H, it toggles TO00. At the same time, the TCR00 register loads the value of the TDR00 register again, and continues counting.

If detection of both the edges of the TI00 pin is selected, the duty factor error of the input clock affects the divided clock period of the TO00 output.

The period of the TO00 output clock includes a sampling error of one period of the operation clock.

$$\text{Clock period of TO00 output} = \text{Ideal TO00 output clock period} \pm \text{Operation clock period (error)}$$

The TDR00 register can be rewritten at any time. The new value of the TDR00 register becomes valid during the next count period.

**Figure 6-51. Block Diagram of Operation as Frequency Divider**

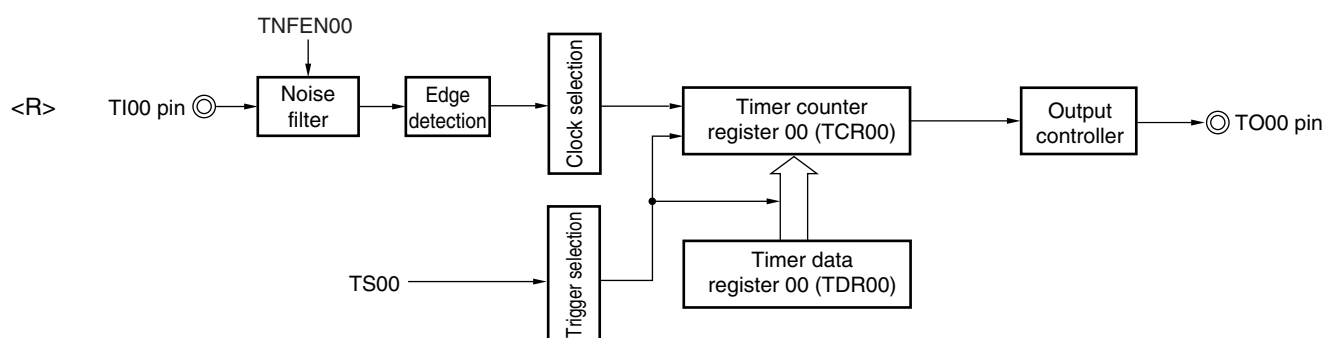
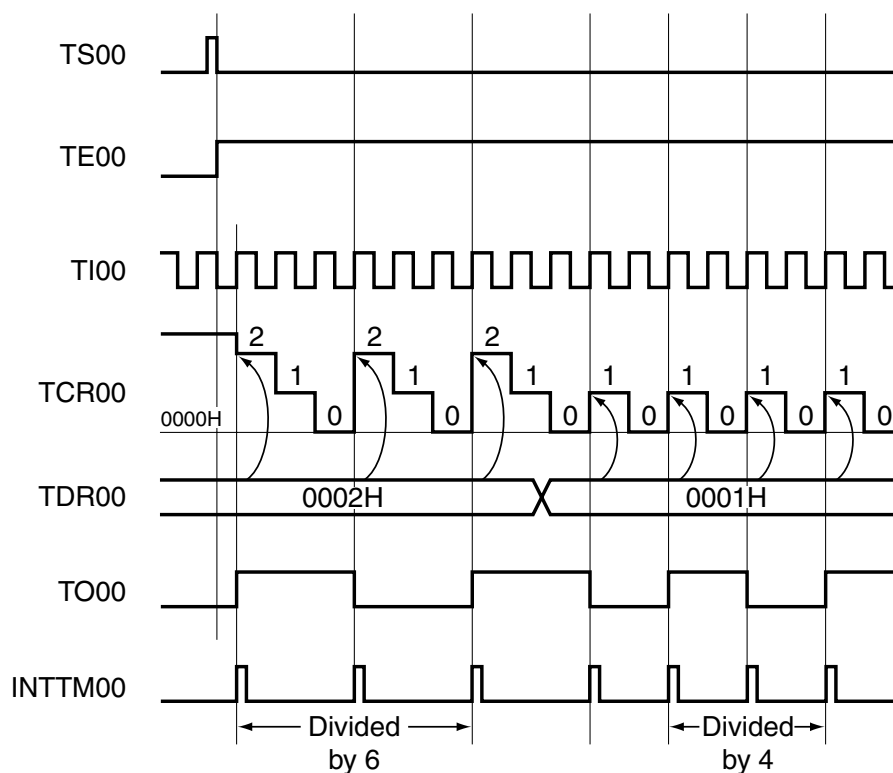
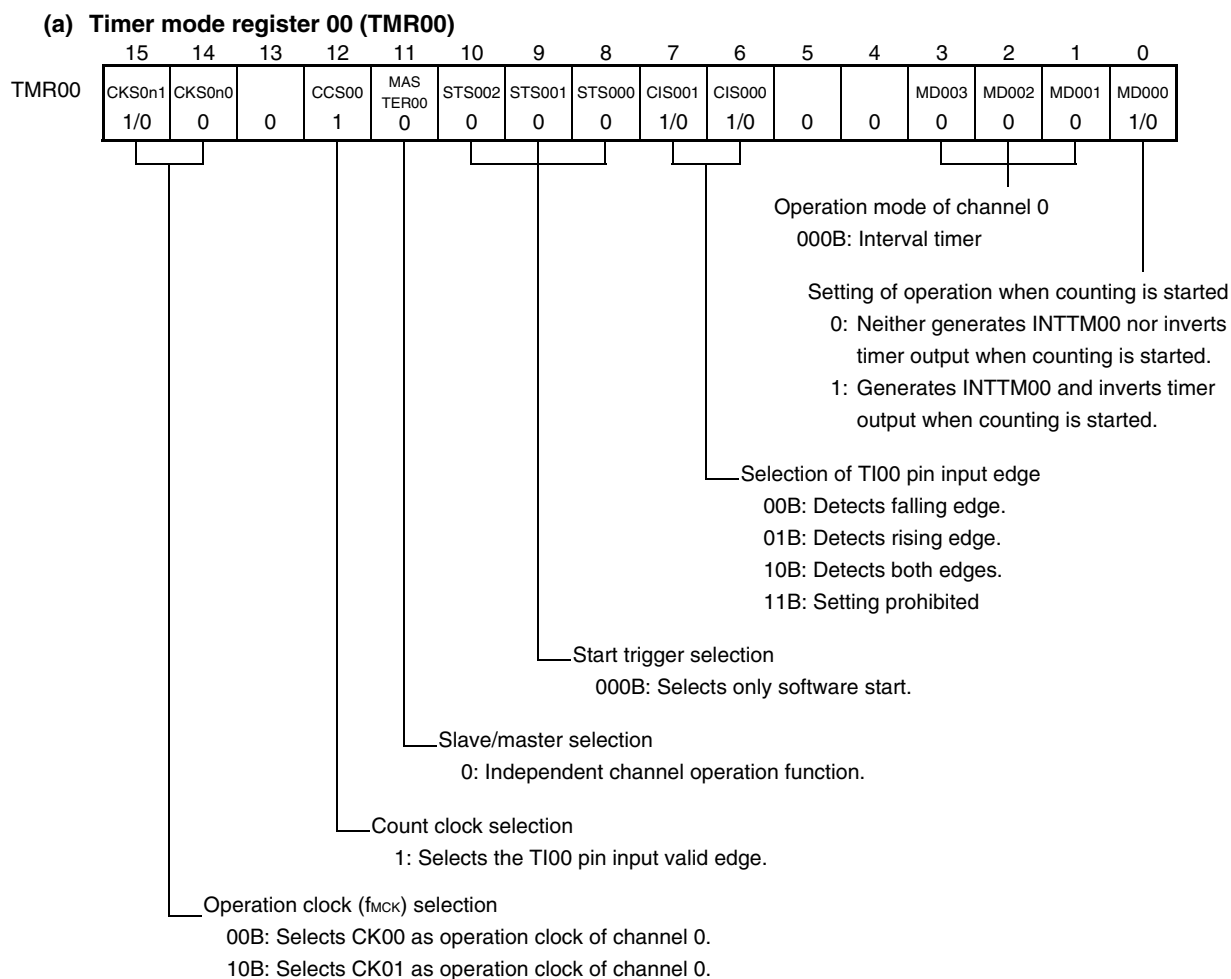


**Figure 6-52. Example of Basic Timing of Operation as Frequency Divider (MD000 = 1)**

**Remark** TS00: Bit n of timer channel start register 0 (TS0)  
 TE00: Bit n of timer channel enable status register 0 (TE0)  
 TI00: TI00 pin input signal  
 TCR00: Timer count register 00 (TCR00)  
 TDR00: Timer data register 00 (TDR00)  
 TO00: TO00 pin output signal

Figure 6-53. Example of Set Contents of Registers During Operation as Frequency Divider

**(b) Timer output register 0 (TO0)**

|       |                         |
|-------|-------------------------|
| Bit 0 |                         |
| TO0   | TO00                    |
|       | 1/0                     |
|       | 0: Outputs 0 from TO00. |
|       | 1: Outputs 1 from TO00. |

**(c) Timer output enable register 0 (TOE0)**

|       |                                                             |
|-------|-------------------------------------------------------------|
| Bit 0 |                                                             |
| TOE0  | TOE00                                                       |
|       | 1/0                                                         |
|       | 0: Stops the TO00 output operation by counting operation.   |
|       | 1: Enables the TO00 output operation by counting operation. |

**(d) Timer output level register 0 (TOL0)**

|       |                                                             |
|-------|-------------------------------------------------------------|
| Bit 0 |                                                             |
| TOL0  | TOL00                                                       |
|       | 0                                                           |
|       | 0: Cleared to 0 when master channel output mode (TOM00 = 0) |

**(e) Timer output mode register 0 (TOM0)**

|       |                                     |
|-------|-------------------------------------|
| Bit 0 |                                     |
| TOM0  | TOM00                               |
|       | 0                                   |
|       | 0: Sets master channel output mode. |

Figure 6-54. Operation Procedure When Frequency Divider Function Is Used

|                         | Software Operation                                                                                                                                                                                                                                                                                                                                         | Hardware Status                                                                                                                                                                                                                                                                                             |
|-------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TAU default setting     |                                                                                                                                                                                                                                                                                                                                                            | Power-off status<br>(Clock supply is stopped and writing to each register is disabled.)                                                                                                                                                                                                                     |
|                         | Sets the TAU0EN bit of peripheral enable register 0 (PER0) to 1.                                                                                                                                                                                                                                                                                           | Power-on status. Each channel stops operating.<br>(Clock supply is started and writing to each register is enabled.)                                                                                                                                                                                        |
|                         | Sets timer clock select register 0 (TPS0).<br>Determines clock frequencies of CK00 to CK03.                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                             |
| Channel default setting | Sets timer mode register 0n (TMR0n) (determines operation mode of channel and selects the detection edge).<br>Sets interval (period) value to timer data register 00 (TDR00).                                                                                                                                                                              | Channel stops operating.<br>(Clock is supplied and some power is consumed.)                                                                                                                                                                                                                                 |
|                         | Clears the TOM00 bit of timer output mode register 0 (TOM0) to 0 (master channel output mode).<br>Clears the TOL00 bit to 0.<br>Sets the TO00 bit and determines default level of the TO00 output.                                                                                                                                                         | The TO00 pin goes into Hi-Z output state.                                                                                                                                                                                                                                                                   |
|                         | Sets the TOE00 bit to 1 and enables operation of TO00.                                                                                                                                                                                                                                                                                                     | The TO00 default setting level is output when the port mode register is in output mode and the port register is 0.                                                                                                                                                                                          |
|                         | Clears the port register and port mode register to 0.                                                                                                                                                                                                                                                                                                      | TO00 does not change because channel stops operating.<br>The TO00 pin outputs the TO00 set level.                                                                                                                                                                                                           |
| Operation start         | Sets the TOE00 bit to 1 (only when operation is resumed).<br>Sets the TS00 bit to 1.<br>The TS00 bit automatically returns to 0 because it is a trigger bit.                                                                                                                                                                                               | TE00 = 1, and count operation starts.<br>Value of the TDR00 register is loaded to timer count register 00 (TCR00) at the count clock input. INTTM00 is generated and TO00 performs toggle operation if the MD000 bit of the TMR00 register is 1.                                                            |
| During operation        | Set value of the TDR00 register can be changed.<br>Sets corresponding bit of noise filter enable register 1, 2 (NFEN1, NFEN2) to 1.<br>The TCR00 register can always be read.<br>The TSR00 register is not used.<br>Set values of the TO0 and TOE0 registers can be changed.<br>Set values of the TMR00 register, TOM00, and TOL00 bits cannot be changed. | Counter (TCR00) counts down. When count value reaches 0000H, the value of the TDR00 register is loaded to the TCR00 register again, and the count operation is continued. By detecting TCR00 = 0000H, INTTM00 is generated and TO00 performs toggle operation. After that, the above operation is repeated. |
| Operation stop          | The TT00 bit is set to 1.<br>The TT00 bit automatically returns to 0 because it is a trigger bit.                                                                                                                                                                                                                                                          | TE00 = 0, and count operation stops.<br>The TCR00 register holds count value and stops.<br>The TO00 output is not initialized but holds current status.                                                                                                                                                     |
|                         | The TOE00 bit is cleared to 0 and value is set to the TO00 bit.                                                                                                                                                                                                                                                                                            | The TO00 pin outputs the TO00 set level.                                                                                                                                                                                                                                                                    |
| TAU stop                | To hold the TO00 pin output level<br>Clears the TO00 bit to 0 after the value to be held is set to the port register.<br>When holding the TO00 pin output level is not necessary<br>Setting not required.                                                                                                                                                  | The TO00 pin output level is held by port function.                                                                                                                                                                                                                                                         |
|                         | The TAU0EN bit of the PER0 register is cleared to 0.                                                                                                                                                                                                                                                                                                       | Power-off status<br>All circuits are initialized and SFR of each channel is also initialized.<br>(The TO00 bit is cleared to 0 and the TO00 pin is set to port mode).                                                                                                                                       |

Operation is resumed.

#### 6.7.4 Operation as input pulse interval measurement

The count value can be captured at the TImn valid edge and the interval of the pulse input to TImn can be measured. The pulse interval can be calculated by the following expression.

$$\text{TImn input pulse interval} = \text{Period of count clock} \times ((10000\text{H} \times \text{TSRmn: OVF}) + (\text{Capture value of TDRmn} + 1))$$

**Caution** The TImn pin input is sampled using the operating clock selected with the CKSmn bit of timer mode register mn (TMRmn), so an error of up to one operating clock cycle occurs.

Timer count register mn (TCRmn) operates as an up counter in the capture mode.

When the channel start trigger bit (TSmn) of timer channel start register m (TSM) is set to 1, the TCRmn register counts up from 0000H in synchronization with the count clock.

When the TImn pin input valid edge is detected, the count value of the TCRmn register is transferred (captured) to timer data register mn (TDRmn) and, at the same time, the TCRmn register is cleared to 0000H, and the INTTMmn is output. If the counter overflows at this time, the OVF bit of timer status register mn (TSRmn) is set to 1. If the counter does not overflow, the OVF bit is cleared. After that, the above operation is repeated.

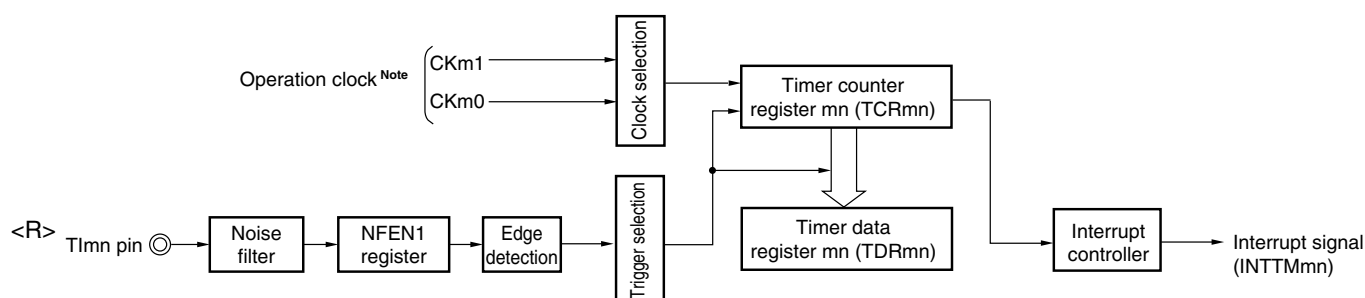
As soon as the count value has been captured to the TDRmn register, the OVF bit of the TSRmn register is updated depending on whether the counter overflows during the measurement period. Therefore, the overflow status of the captured value can be checked.

If the counter reaches a full count for two or more periods, it is judged to be an overflow occurrence, and the OVF bit of the TSRmn register is set to 1. However, a normal interval value cannot be measured for the OVF bit, if two or more overflows occur.

Set the STSmn2 to STSmn0 bits of the TMRmn register to 001B to use the valid edges of TImn as a start trigger and a capture trigger.

When TEmn = 1, a software operation (TSmn = 1) can be used as a capture trigger, instead of using the TImn pin input.

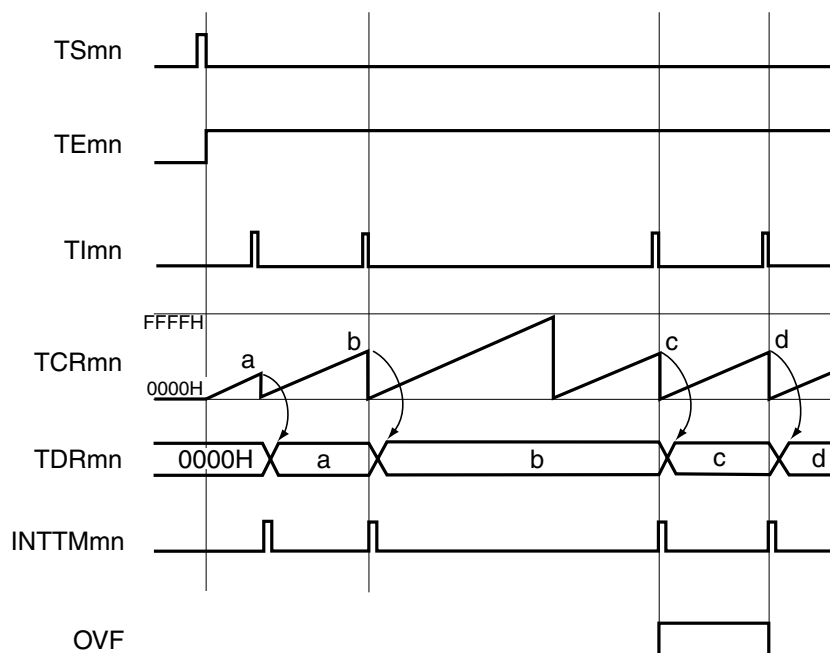
**Figure 6-55. Block Diagram of Operation as Input Pulse Interval Measurement**



**Note** When channels 1 and 3, the clock can be selected from CKm0, CKm1, CKm2 and CKm3.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

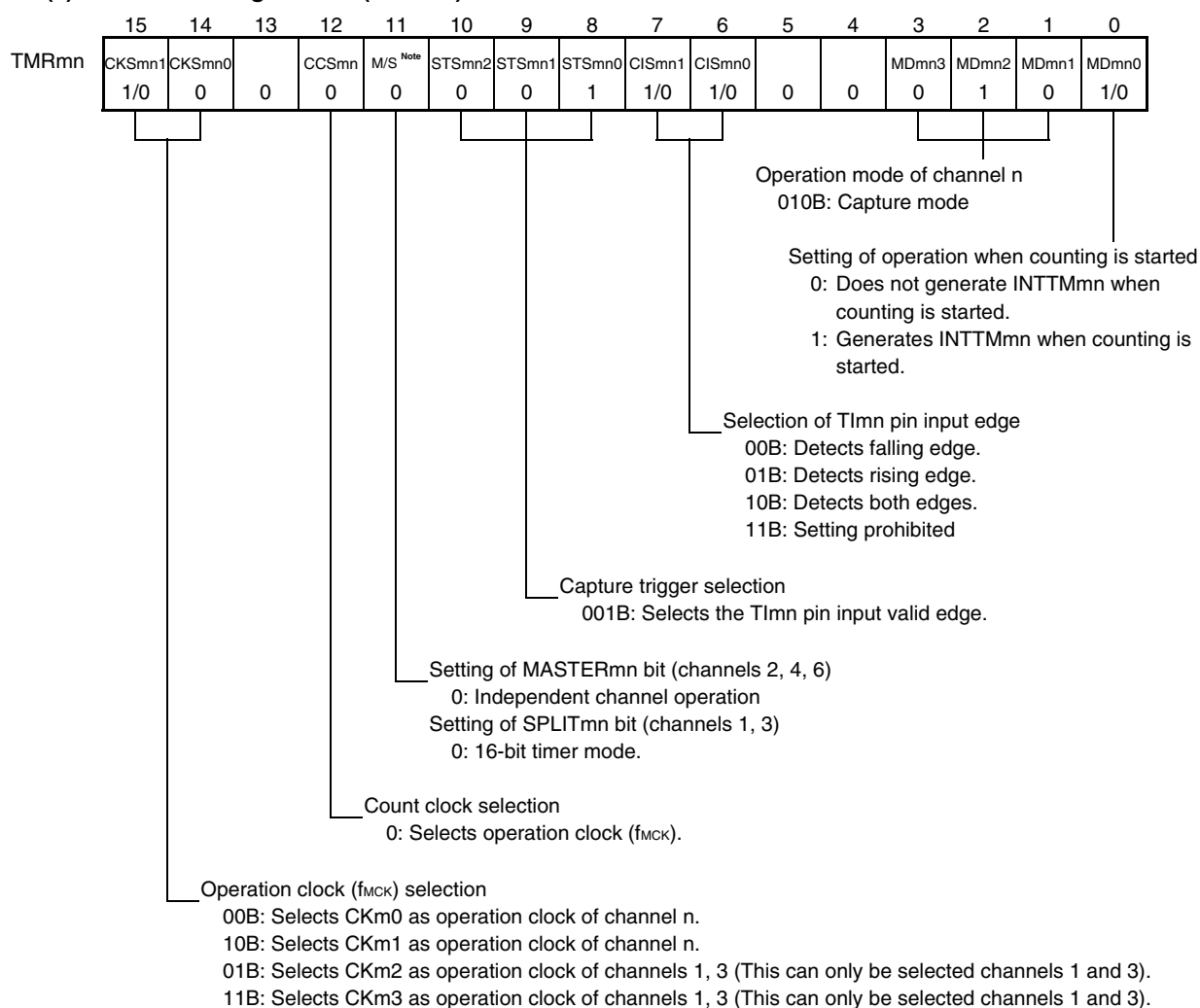


**Figure 6-56. Example of Basic Timing of Operation as Input Pulse Interval Measurement (MDmn0 = 0)**

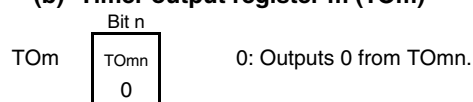
- Remarks**
1. m: Unit number (m = 0), n: Channel number (n = 0 to 7)
  2. TSmn: Bit n of timer channel start register m (TSM)
  - TE mn: Bit n of timer channel enable status register m (TEM)
  - TImn: TImn pin input signal
  - TCRmn: Timer count register mn (TCRmn)
  - TDRmn: Timer data register mn (TDRmn)
  - OVF: Bit 0 of timer status register mn (TSRmn)

Figure 6-57. Example of Set Contents of Registers to Measure Input Pulse Interval

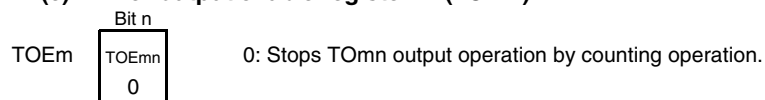
## (a) Timer mode register mn (TMRmn)



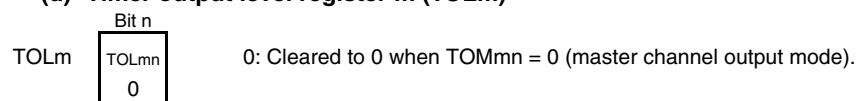
## (b) Timer output register m (TOM)



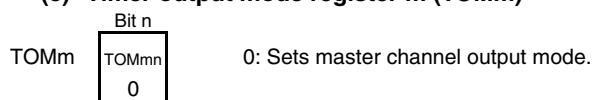
## (c) Timer output enable register m (TOEm)



## (d) Timer output level register m (TOLm)



## (e) Timer output mode register m (TOMm)



**Note** TMRm2, TMRm4, TMRm6: MASTERmn bit  
 TMRm1, TMRm3: SPLITmn bit  
 TMRm0, TMRm5, TMRm7: Fixed to 0

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Figure 6-58. Operation Procedure When Input Pulse Interval Measurement Function Is Used

|                         | Software Operation                                                                                                                                                                                                                                                                                                                                                              | Hardware Status                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TAU default setting     |                                                                                                                                                                                                                                                                                                                                                                                 | Power-off status<br>(Clock supply is stopped and writing to each register is disabled.)                                                                                                                                                                                                                                                                                                                                                                                 |
|                         | Sets the TAU0EN bit of peripheral enable register 0 (PER0) to 1.                                                                                                                                                                                                                                                                                                                | Power-on status. Each channel stops operating.<br>(Clock supply is started and writing to each register is enabled.)                                                                                                                                                                                                                                                                                                                                                    |
|                         | Sets timer clock select register m (TPSm).<br>Determines clock frequencies of CKm0 to CKm3.                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| Channel default setting | Sets timer mode register mn (TMRmn) (determines operation mode of channel).                                                                                                                                                                                                                                                                                                     | Channel stops operating.<br>(Clock is supplied and some power is consumed.)                                                                                                                                                                                                                                                                                                                                                                                             |
| Operation start         | Sets TSMn bit to 1.<br>The TSMn bit automatically returns to 0 because it is a trigger bit.                                                                                                                                                                                                                                                                                     | TEmn = 1, and count operation starts.<br>Timer count register mn (TCRmn) is cleared to 0000H at the count clock input.<br>When the MDmn0 bit of the TMRmn register is 1, INTTMmn is generated.                                                                                                                                                                                                                                                                          |
| During operation        | Set values of only the CISmn1 and CISmn0 bits of the TMRmn register can be changed.<br>Sets corepointing bit of noise filter enable register 1, 2 (NFEN1, NFEN2) to 1.<br>The TDRmn register can always be read.<br>The TCRmn register can always be read.<br>The TSRmn register can always be read.<br>Set values of the TOMmn, TOLmn, TOMn, and TOEmn bits cannot be changed. | Counter (TCRmn) counts up from 0000H. When the TImn pin input valid edge is detected, the count value is transferred (captured) to timer data register mn (TDRmn). At the same time, the TCRmn register is cleared to 0000H, and the INTTMmn signal is generated.<br>If an overflow occurs at this time, the OVF bit of timer status register mn (TSRmn) is set; if an overflow does not occur, the OVF bit is cleared.<br>After that, the above operation is repeated. |
| Operation stop          | The TTmn bit is set to 1.<br>The TTmn bit automatically returns to 0 because it is a trigger bit.                                                                                                                                                                                                                                                                               | TEmn = 0, and count operation stops.<br>The TCRmn register holds count value and stops.<br>The OVF bit of the TSRmn register is also held.                                                                                                                                                                                                                                                                                                                              |
| TAU stop                | The TAU0EN bit of the PER0 register is cleared to 0.                                                                                                                                                                                                                                                                                                                            | Power-off status<br>All circuits are initialized and SFR of each channel is also initialized.                                                                                                                                                                                                                                                                                                                                                                           |

Operation is resumed.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

### 6.7.5 Operation as input signal high-/low-level width measurement

**Caution** When using a channel to implement the LIN-bus, set bit 1 (ISC1) of the input switch control register (ISC) to 1. In the following descriptions, read TImn as RxD0.

By starting counting at one edge of the TImn pin input and capturing the number of counts at another edge, the signal width (high-level width/low-level width) of TImn can be measured. The signal width of TImn can be calculated by the following expression.

$$\text{Signal width of TImn input} = \text{Period of count clock} \times ((10000\text{H} \times \text{TSRmn: OVF}) + (\text{Capture value of TDRmn} + 1))$$

**Caution** The TImn pin input is sampled using the operating clock selected with the CKSmn bit of timer mode register mn (TMRmn), so an error equivalent to one operation clock occurs.

Timer count register mn (TCRmn) operates as an up counter in the capture & one-count mode.

When the channel start trigger bit (TSmn) of timer channel start register m (TSm) is set to 1, the TEmn bit is set to 1 and the TImn pin start edge detection wait status is set.

When the TImn pin input start edge (rising edge of the TImn pin input when the high-level width is to be measured) is detected, the counter counts up from 0000H in synchronization with the count clock. When the valid capture edge (falling edge of the TImn pin input when the high-level width is to be measured) is detected later, the count value is transferred to timer data register mn (TDRmn) and, at the same time, INTTMmn is output. If the counter overflows at this time, the OVF bit of timer status register mn (TSRmn) is set to 1. If the counter does not overflow, the OVF bit is cleared. The TCRmn register stops at the value "value transferred to the TDRmn register + 1", and the TImn pin start edge detection wait status is set. After that, the above operation is repeated.

As soon as the count value has been captured to the TDRmn register, the OVF bit of the TSRmn register is updated depending on whether the counter overflows during the measurement period. Therefore, the overflow status of the captured value can be checked.

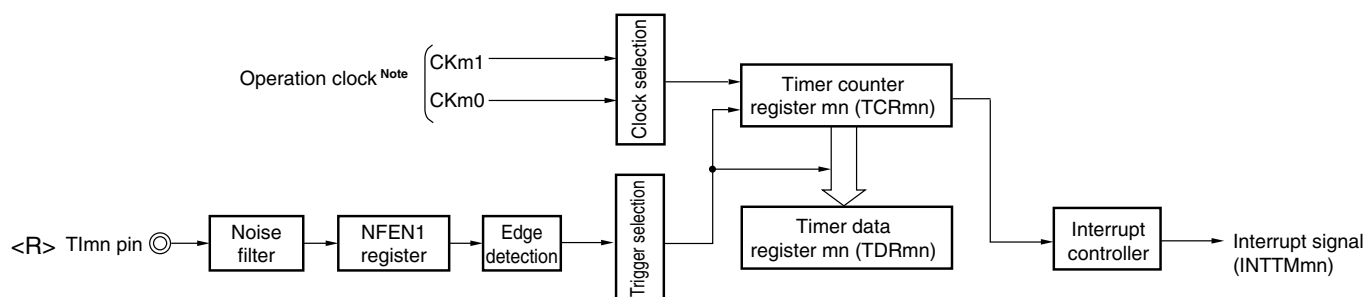
If the counter reaches a full count for two or more periods, it is judged to be an overflow occurrence, and the OVF bit of the TSRmn register is set to 1. However, a normal interval value cannot be measured for the OVF bit, if two or more overflows occur.

Whether the high-level width or low-level width of the TImn pin is to be measured can be selected by using the CISmn1 and CISmn0 bits of the TMRmn register.

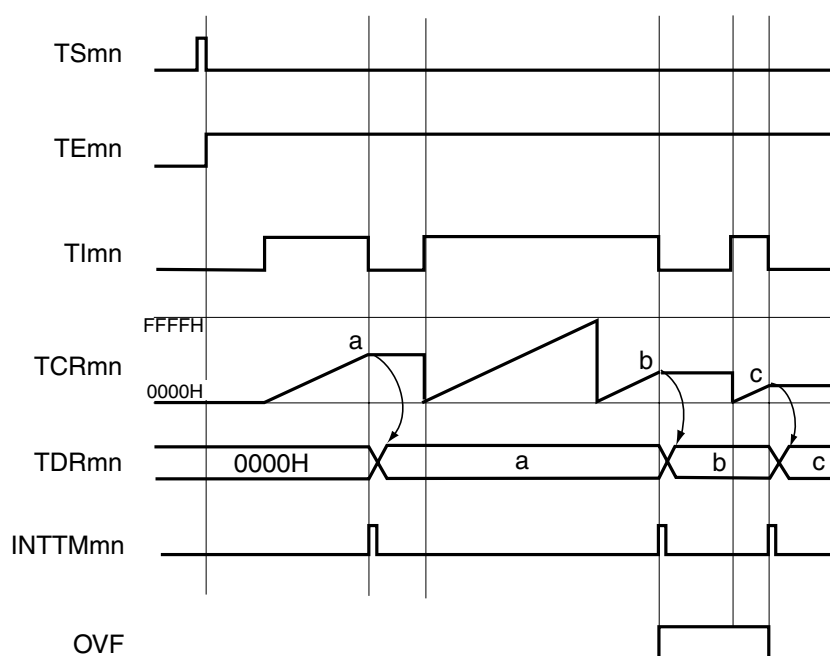
Because this function is used to measure the signal width of the TImn pin input, the TSmn bit cannot be set to 1 while the TEmn bit is 1.

CISmn1, CISmn0 of TMRmn register = 10B: Low-level width is measured.

CISmn1, CISmn0 of TMRmn register = 11B: High-level width is measured.

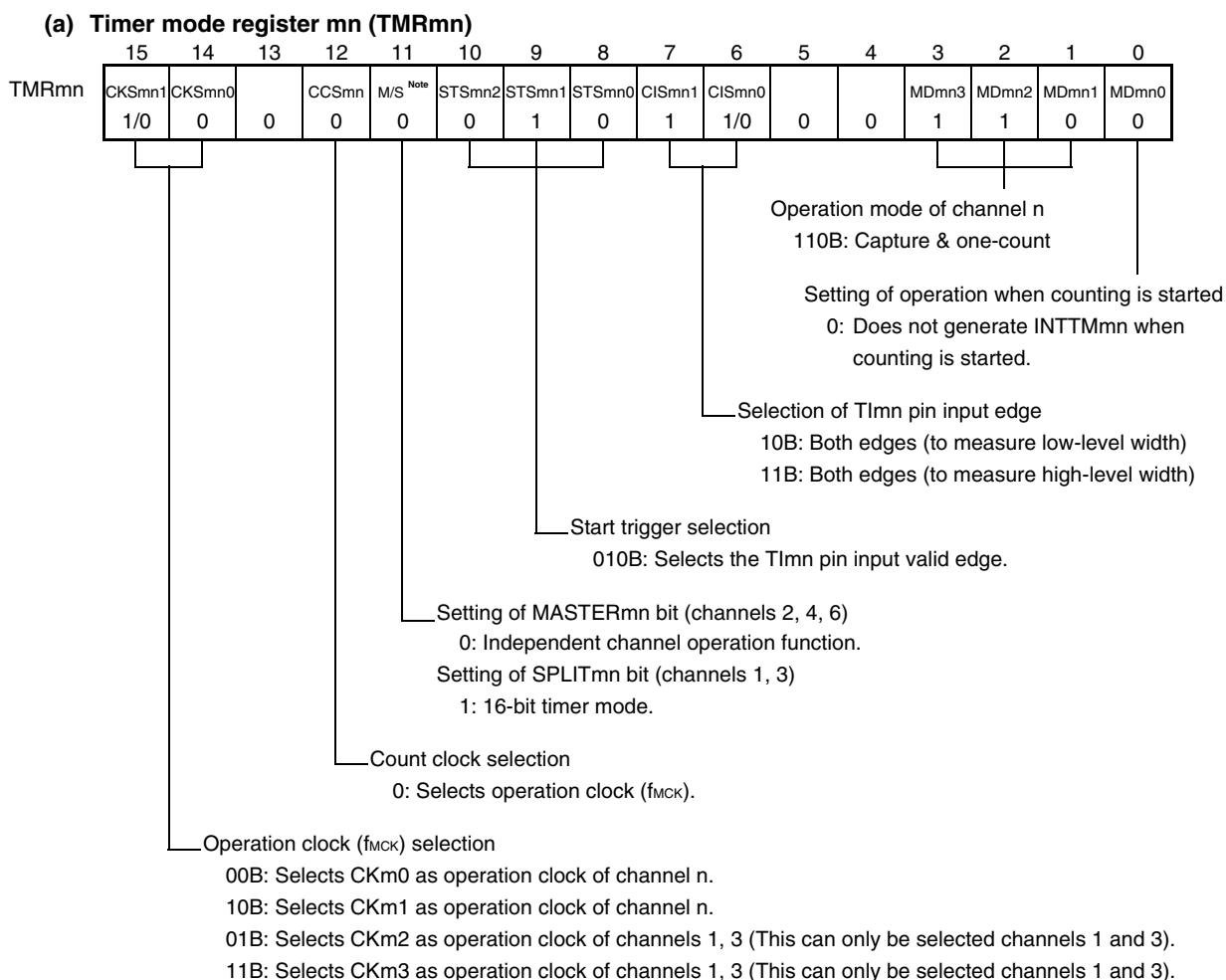
**Figure 6-59. Block Diagram of Operation as Input Signal High-/Low-Level Width Measurement**

**Note** For channels 1 and 3, the clock can be selected from CKm0, CKm1, CKm2 and CKm3.

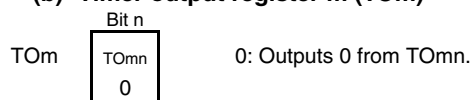
**Figure 6-60. Example of Basic Timing of Operation as Input Signal High-/Low-Level Width Measurement**

- Remarks**
1. m: Unit number (m = 0), n: Channel number (n = 0 to 7)
  2. TSmn: Bit n of timer channel start register m (TSm)  
 TEmn: Bit n of timer channel enable status register m (TEm)  
 TImn: TImn pin input signal  
 TCRmn: Timer count register mn (TCRmn)  
 TDRmn: Timer data register mn (TDRmn)  
 OVF: Bit 0 of timer status register mn (TSRmn)

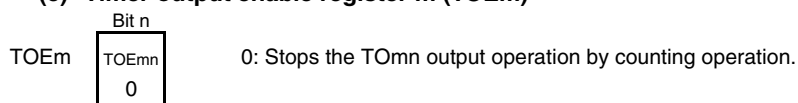
Figure 6-61. Example of Set Contents of Registers to Measure Input Signal High-/Low-Level Width



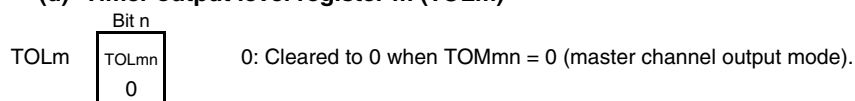
## (b) Timer output register m (TOM)



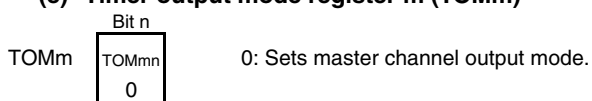
## (c) Timer output enable register m (TOEm)



## (d) Timer output level register m (TOLm)



## (e) Timer output mode register m (TOMm)



**Note** TMRm2, TMRm4, TMRm6: MASTERmn bit  
 TMRm1, TMRm3: SPLITmn bit  
 TMRm0, TMRm5, TMRm7: Fixed to 0

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

**Figure 6-62. Operation Procedure When Input Signal High-/Low-Level Width Measurement Function Is Used**

|                         | Software Operation                                                                                                                                                                                                                                                                                         | Hardware Status                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TAU default setting     |                                                                                                                                                                                                                                                                                                            | Power-off status<br>(Clock supply is stopped and writing to each register is disabled.)                                                                                                                                                                                                                                                                                                                                                                                          |
|                         | Sets the TAU0EN bit of peripheral enable register 0 (PER0) to 1.                                                                                                                                                                                                                                           | Power-on status. Each channel stops operating.<br>(Clock supply is started and writing to each register is enabled.)                                                                                                                                                                                                                                                                                                                                                             |
|                         | Sets timer clock select register m (TPSm).<br>Determines clock frequencies of CKm0 to CKm3.                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| Channel default setting | Sets timer mode register mn (TMRmn) (determines operation mode of channel).<br>Clears the TOEmn bit to 0 and stops operation of TOMn.                                                                                                                                                                      | Channel stops operating.<br>(Clock is supplied and some power is consumed.)                                                                                                                                                                                                                                                                                                                                                                                                      |
| Operation start         | Sets the TSmn bit to 1.<br>The TSmn bit automatically returns to 0 because it is a trigger bit.                                                                                                                                                                                                            | TEmn = 1, and the TImn pin start edge detection wait status is set.                                                                                                                                                                                                                                                                                                                                                                                                              |
|                         | Detects the TImn pin input count start valid edge.                                                                                                                                                                                                                                                         | Clears timer count register mn (TCRmn) to 0000H and starts counting up.                                                                                                                                                                                                                                                                                                                                                                                                          |
| During operation        | Set value of the TDRmn register can be changed.<br>Sets corresponding bit of noise filter enable register 1, 2 (NFEN1, NFEN2) to 1<br>The TCRmn register can always be read.<br>The TSRmn register is not used.<br>Set values of the TMRmn register, TOMmn, TOLmn, TOMn, and TOEmn bits cannot be changed. | When the TImn pin start edge is detected, the counter (TCRmn) counts up from 0000H. If a capture edge of the TImn pin is detected, the count value is transferred to timer data register mn (TDRmn) and INTTMmn is generated.<br>If an overflow occurs at this time, the OVF bit of timer status register mn (TSRmn) is set; if an overflow does not occur, the OVF bit is cleared. The TCRmn register stops the count operation until the next TImn pin start edge is detected. |
| Operation stop          | The TTmn bit is set to 1.<br>The TTmn bit automatically returns to 0 because it is a trigger bit.                                                                                                                                                                                                          | TEmn = 0, and count operation stops.<br>The TCRmn register holds count value and stops.<br>The OVF bit of the TSRmn register is also held.                                                                                                                                                                                                                                                                                                                                       |
| TAU stop                | The TAU0EN bit of the PER0 register is cleared to 0.                                                                                                                                                                                                                                                       | Power-off status<br>All circuits are initialized and SFR of each channel is also initialized.                                                                                                                                                                                                                                                                                                                                                                                    |

Operation is resumed.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

### 6.7.6 Operation as delay counter

It is possible to start counting down when the valid edge of the Tl<sub>mn</sub> pin input is detected (an external event), and then generate INTTM<sub>mn</sub> (a timer interrupt) after any specified interval.

It can also generate INTTM<sub>mn</sub> (timer interrupt) at any interval by making a software set TS<sub>mn</sub> = 1 and the count down start during the period of TE<sub>mn</sub> = 1.

The interrupt generation period can be calculated by the following expression.

$$\text{Generation period of INTTM}_{mn} \text{ (timer interrupt)} = \text{Period of count clock} \times (\text{Set value of TDR}_{mn} + 1)$$

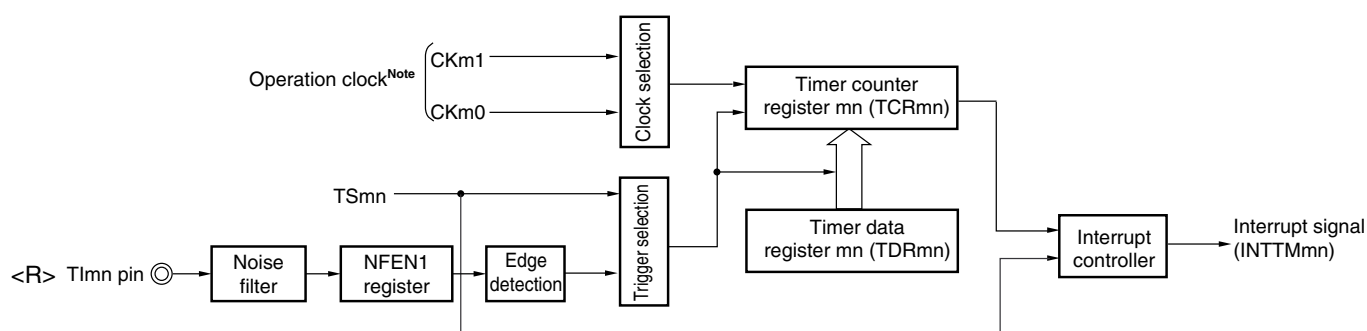
Timer count register *mn* (TCR<sub>mn</sub>) operates as a down counter in the one-count mode.

When the channel start trigger bit (TS<sub>mn</sub>, TSH<sub>m1</sub>, TSH<sub>m3</sub>) of timer channel start register *m* (TS<sub>m</sub>) is set to 1, the TE<sub>mn</sub>, TEH<sub>m1</sub>, TEH<sub>m3</sub> bits are set to 1 and the Tl<sub>mn</sub> pin input valid edge detection wait status is set.

Timer count register *mn* (TCR<sub>mn</sub>) starts operating upon Tl<sub>mn</sub> pin input valid edge detection and loads the value of timer data register *mn* (TDR<sub>mn</sub>). The TCR<sub>mn</sub> register counts down from the value of the TDR<sub>mn</sub> register it has loaded, in synchronization with the count clock. When TCR<sub>mn</sub> = 0000H, it outputs INTTM<sub>mn</sub> and stops counting until the next Tl<sub>mn</sub> pin input valid edge is detected.

The TDR<sub>mn</sub> register can be rewritten at any time. The new value of the TDR<sub>mn</sub> register becomes valid from the next period.

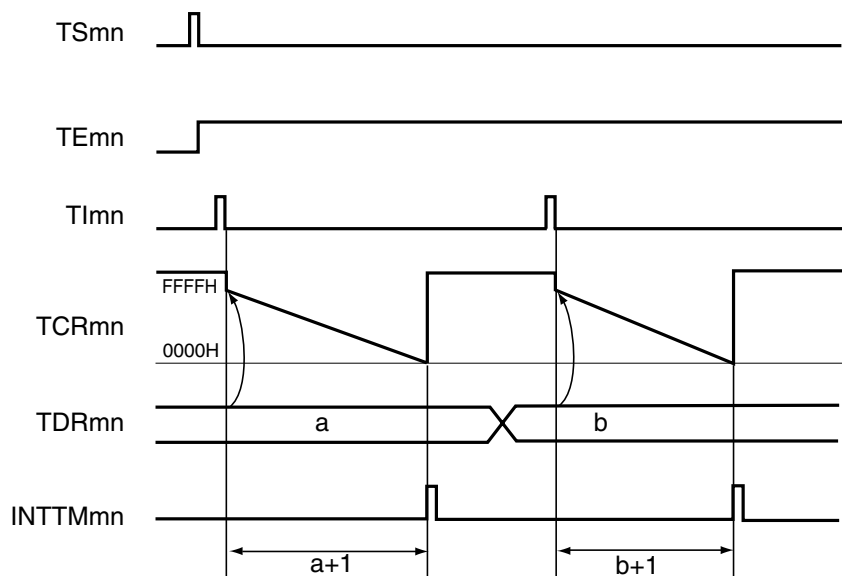
**Figure 6-63. Block Diagram of Operation as Delay Counter**



**Note** For using channels 1 and 3, the clock can be selected from CK<sub>m0</sub>, CK<sub>m1</sub>, CK<sub>m2</sub> and CK<sub>m3</sub>.

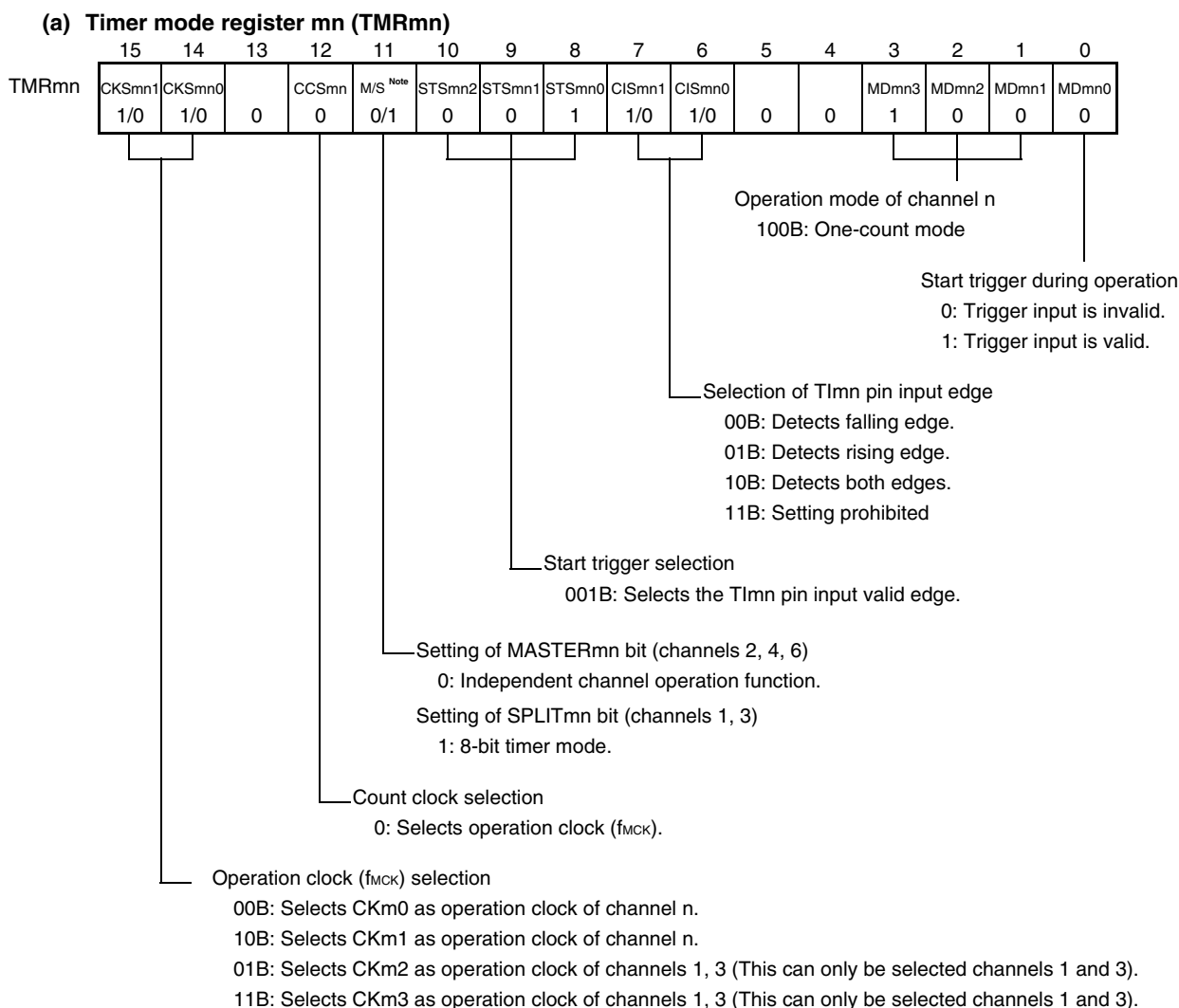
**Remark** *m*: Unit number (*m* = 0), *n*: Channel number (*n* = 0 to 7)



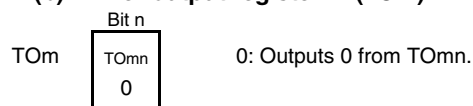
**Figure 6-64. Example of Basic Timing of Operation as Delay Counter**

- Remarks**
1. m: Unit number (m = 0), n: Channel number (n = 0 to 7)
  2. TSmn: Bit n of timer channel start register m (TSM)  
 TE mn: Bit n of timer channel enable status register m (TEM)  
 TImn: TImn pin input signal  
 TCRmn: Timer count register mn (TCRmn)  
 TDRmn: Timer data register mn (TDRmn)

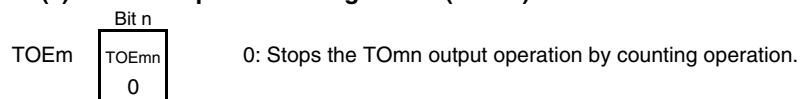
Figure 6-65. Example of Set Contents of Registers to Delay Counter (1/2)



## (b) Timer output register m (TOM)



## (c) Timer output enable register m (TOEm)



**Note** TMRm2, TMRm4, TMRm6: MASTERmn bit  
 TMRm1, TMRm3: SPLITmn bit  
 TMRm0, TMRm5, TMRm7: Fixed to 0

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

**Figure 6-65. Example of Set Contents of Registers to Delay Counter (2/2)****(d) Timer output level register m (TOLm)**

TOLm 

|       |
|-------|
| Bit n |
| TOLmn |
| 0     |

 0: Cleared to 0 when TOMmn = 0 (master channel output mode).

**(e) Timer output mode register m (TOMm)**

TOMm 

|       |
|-------|
| Bit n |
| TOMmn |
| 0     |

 0: Sets master channel output mode.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Figure 6-66. Operation Procedure When Delay Counter Function Is Used

|                         | Software Operation                                                                                                                                                                                              | Hardware Status                                                                                                                                                      |
|-------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TAU default setting     |                                                                                                                                                                                                                 | Power-off status<br>(Clock supply is stopped and writing to each register is disabled.)                                                                              |
|                         | Sets the TAU0EN bit of peripheral enable register 0 (PER0) to 1.                                                                                                                                                | Power-on status. Each channel stops operating.<br>(Clock supply is started and writing to each register is enabled.)                                                 |
|                         | Sets timer clock select register m (TPSm).<br>Determines clock frequencies of CKm0 to CKm3.                                                                                                                     |                                                                                                                                                                      |
| Channel default setting | Sets timer mode register mn (TMRmn) (determines operation mode of channel).<br>INTTMmn output delay is set to timer data register mn (TDRmn).<br>Clears the TOEmn bit to 0 and stops operation of TOMn.         | Channel stops operating.<br>(Clock is supplied and some power is consumed.)                                                                                          |
| Operation start         | Sets the TSmn bit to 1.<br>The TSmn bit automatically returns to 0 because it is a trigger bit.                                                                                                                 | TEmn = 1, and the TImn pin input valid edge detection wait status is set.                                                                                            |
|                         | Detects the TImn pin input valid edge.                                                                                                                                                                          | Value of the TDRmn register is loaded to the timer count register mn (TCRmn).                                                                                        |
| During operation        | Set value of the TDRmn register can be changed.<br>Sets corresponding bit of noise filter enable register 1, 2 (NFEN1, NFEN2) to 1<br>The TCRmn register can always be read.<br>The TSRmn register is not used. | The counter (TCRmn) counts down. When TCRmn counts down to 0000H, INTTMmn is output, and counting stops (which leaves TCRmn at 0000H) until the next TImn pin input. |
| Operation stop          | The TTmn bit is set to 1.<br>The TTmn bit automatically returns to 0 because it is a trigger bit.                                                                                                               | TEmn = 0, and count operation stops.<br>The TCRmn register holds count value and stops.                                                                              |
| TAU stop                | The TAU0EN bit of the PER0 register is cleared to 0.                                                                                                                                                            | Power-off status<br>All circuits are initialized and SFR of each channel is also initialized.                                                                        |

Operation is resumed.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0 to 7)

## 6.8 Simultaneous Channel Operation Function of Timer Array Unit

### 6.8.1 Operation as one-shot pulse output function

By using two channels as a set, a one-shot pulse having any delay pulse width can be generated from the signal input to the TImn pin.

The delay time and pulse width can be calculated by the following expressions.

$$\begin{aligned}\text{Delay time} &= \{\text{Set value of TDRmn (master)} + 2\} \times \text{Count clock period} \\ \text{Pulse width} &= \{\text{Set value of TDRmp (slave)}\} \times \text{Count clock period}\end{aligned}$$

The master channel operates in the one-count mode and counts the delays. Timer count register mn (TCRmn) of the master channel starts operating upon start trigger detection and loads the value of timer data register mn (TDRmn).

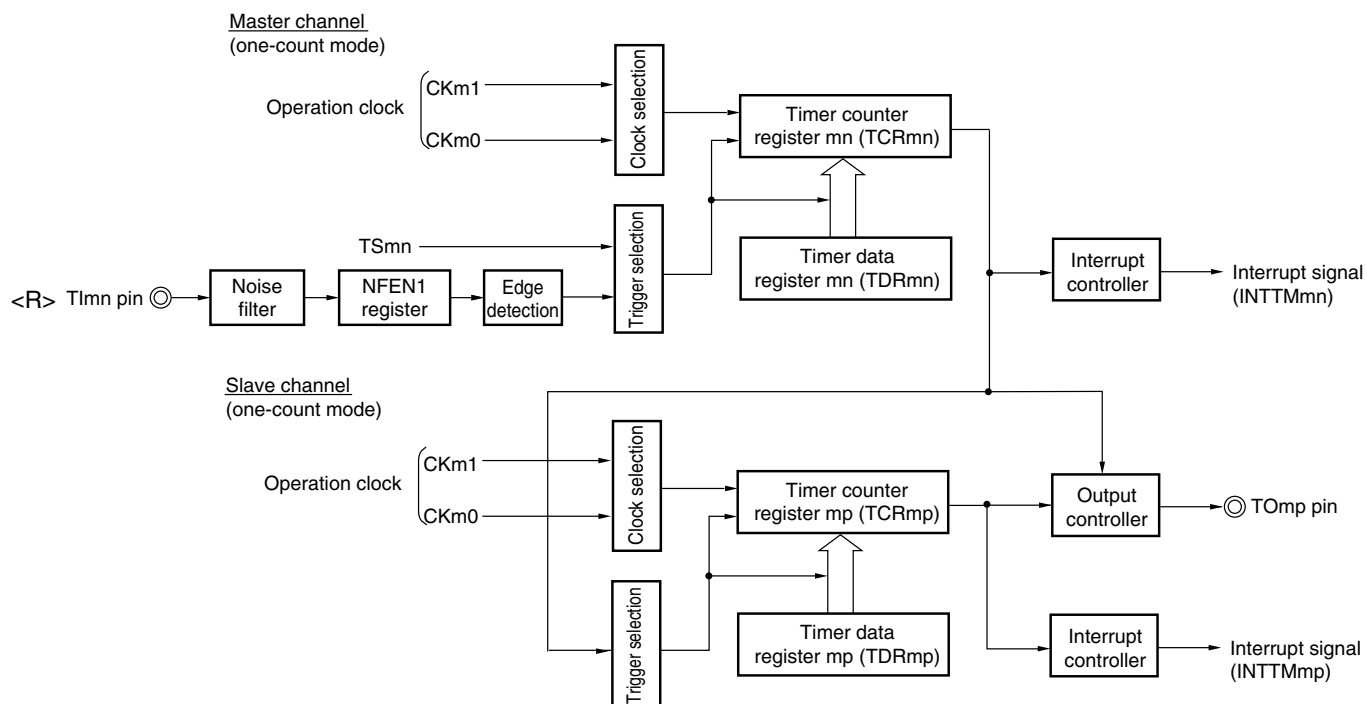
The TCRmn register counts down from the value of the TDRmn register it has loaded, in synchronization with the count clock. When TCRmn = 0000H, it outputs INTTMmn and stops counting until the next start trigger is detected.

The slave channel operates in the one-count mode and counts the pulse width. The TCRmp register of the slave channel starts operation using INTTMmn of the master channel as a start trigger, and loads the value of the TDRmp register. The TCRmp register counts down from the value of the TDRmp register it has loaded, in synchronization with the count value. When count value = 0000H, it outputs INTTMmp and stops counting until the next start trigger (INTTMmn of the master channel) is detected. The output level of TOmp becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmp = 0000H.

Instead of using the TImn pin input, a one-shot pulse can also be output using the software operation (TSmn = 1) as a start trigger.

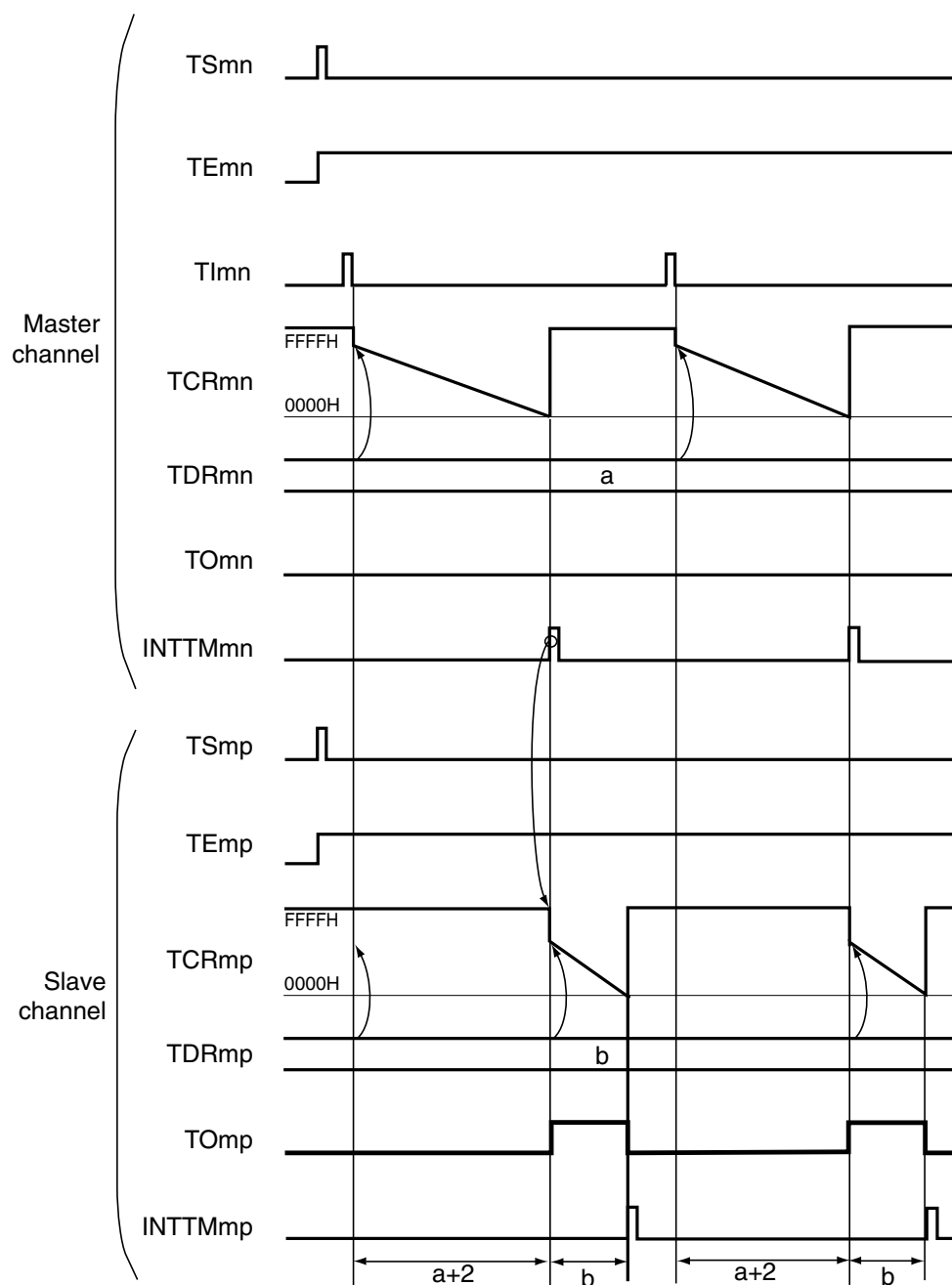
**Caution** The timing of loading of timer data register mn (TDRmn) of the master channel is different from that of the TDRmp register of the slave channel. If the TDRmn and TDRmp registers are rewritten during operation, therefore, an illegal waveform is output. Rewrite the TDRmn register after INTTMmn is generated and the TDRmp register after INTTMmp is generated.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)  
p: Slave channel number (n < p ≤ 7)

**Figure 6-67. Block Diagram of Operation as One-Shot Pulse Output Function**

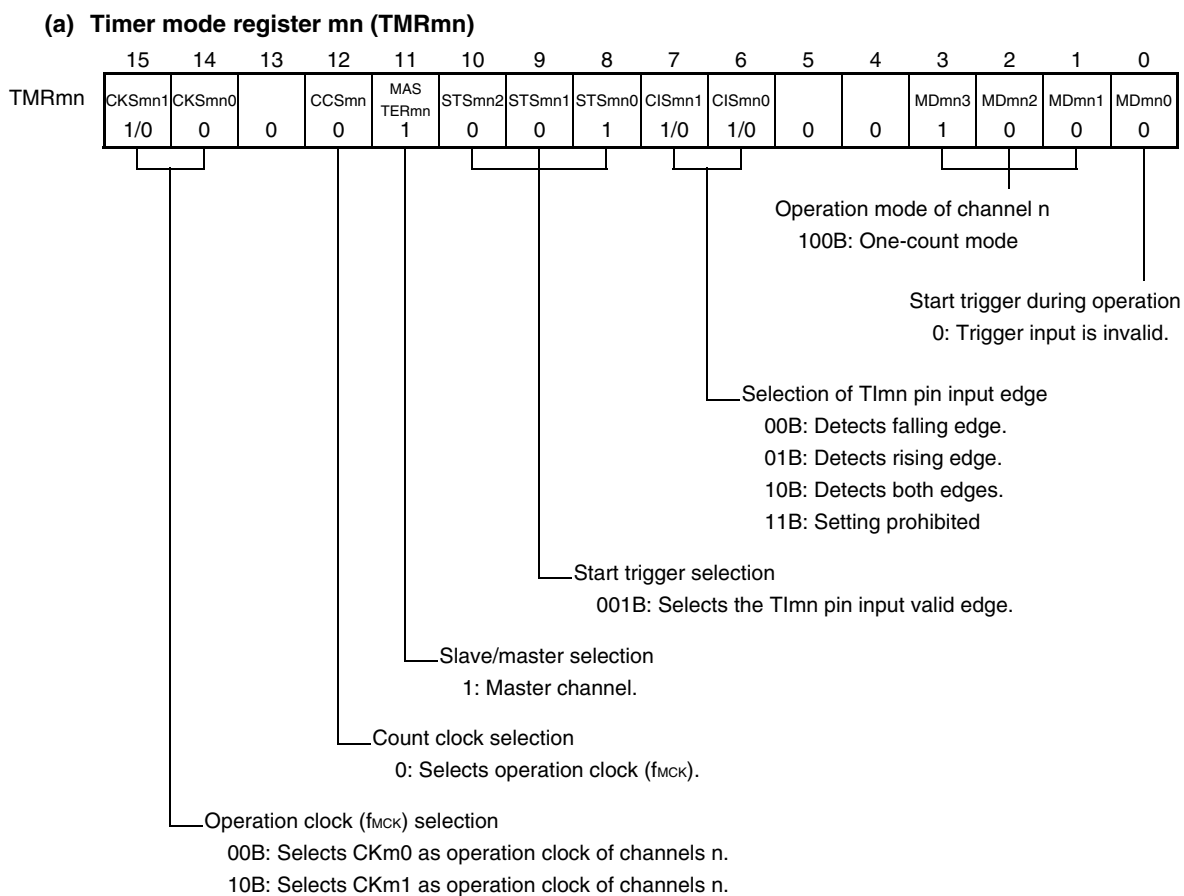
**Remark** m: Unit number ( $m = 0$ ), n: Channel number ( $n = 0, 2, 4, 6$ )  
 p: Slave channel number ( $n < p \leq 7$ )

Figure 6-68. Example of Basic Timing of Operation as One-Shot Pulse Output Function

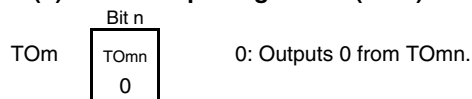


- Remarks**
1. m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)  
p: Slave channel number (n < p ≤ 7)
  2. TSmn, TSmp: Bit n, p of timer channel start register m (TSm)  
TEmn, TEm: Bit n, p of timer channel enable status register m (TEm)  
TI mn, TI mp: TI mn and TI mp pins input signal  
TCRmn, TCRmp: Timer count registers mn, mp (TCRmn, TCRmp)  
TDRmn, TDRmp: Timer data registers mn, mp (TDRmn, TDRmp)  
TOmn, TOmp: TOmn and TOmp pins output signal

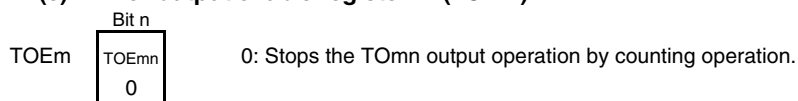
Figure 6-69. Example of Set Contents of Registers When One-Shot Pulse Output Function Is Used (Master Channel)



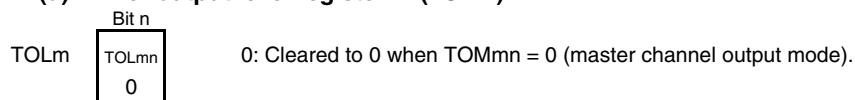
## (b) Timer output register m (TOM)



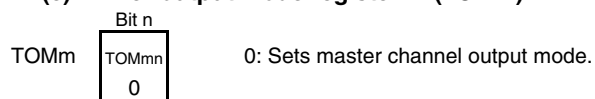
## (c) Timer output enable register m (TOEm)



## (d) Timer output level register m (TOLm)

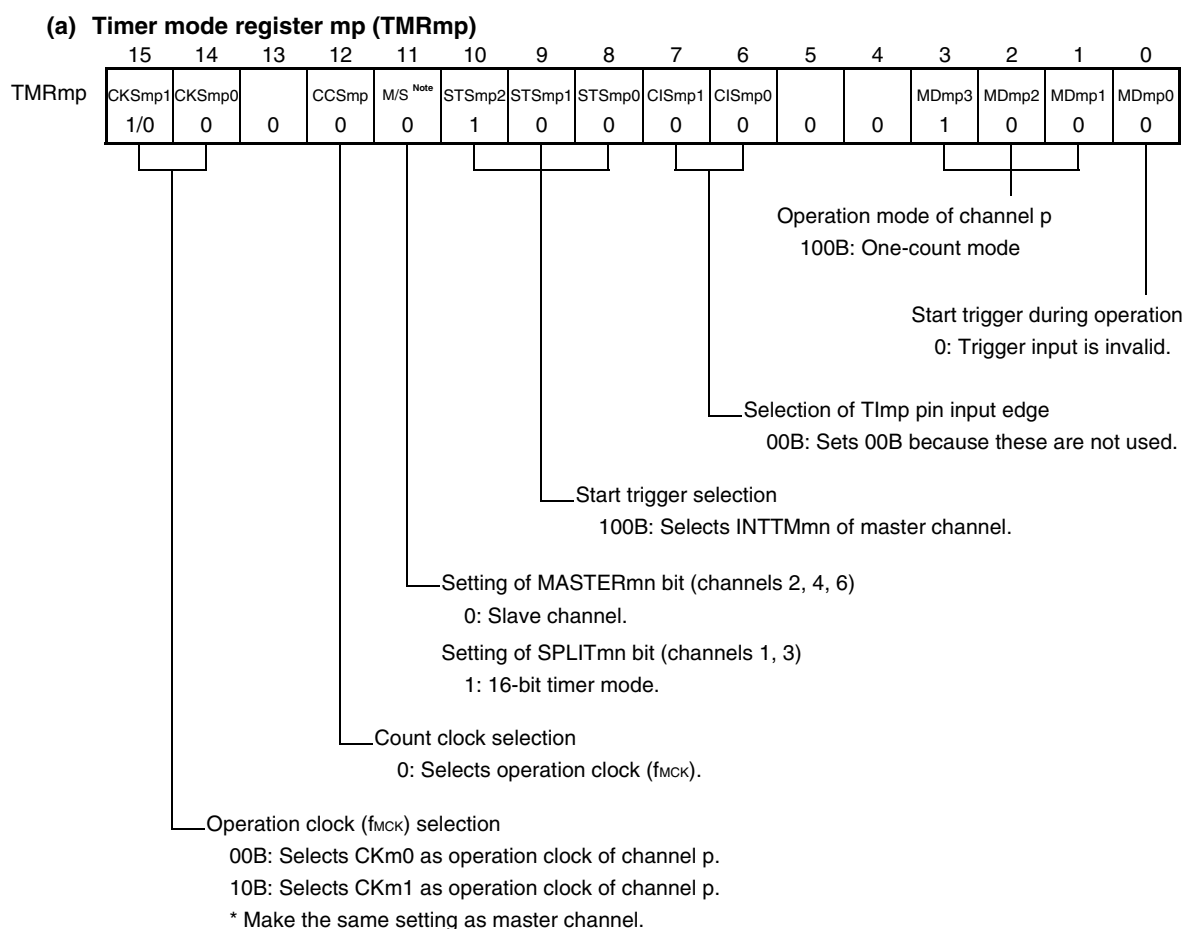


## (e) Timer output mode register m (TOMm)



**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)



**Figure 6-70. Example of Set Contents of Registers When One-Shot Pulse Output Function Is Used (Slave Channel)****(b) Timer output register m (TOM)**

|     |       |                                                    |
|-----|-------|----------------------------------------------------|
| TOM | Bit p |                                                    |
|     | TOMp  | 0: Outputs 0 from TOMp.<br>1: Outputs 1 from TOMp. |
|     | 1/0   |                                                    |

**(c) Timer output enable register m (TOEm)**

|      |       |                                                                                                                          |
|------|-------|--------------------------------------------------------------------------------------------------------------------------|
| TOEm | Bit p |                                                                                                                          |
|      | TOEmp | 0: Stops the TOMp output operation by counting operation.<br>1: Enables the TOMp output operation by counting operation. |
|      | 1/0   |                                                                                                                          |

**(d) Timer output level register m (TOLm)**

|      |       |                                                                                 |
|------|-------|---------------------------------------------------------------------------------|
| TOLm | Bit p |                                                                                 |
|      | TOLmp | 0: Positive logic output (active-high)<br>1: Negative logic output (active-low) |
|      | 1/0   |                                                                                 |

**(e) Timer output mode register m (TOMm)**

|      |       |                                        |
|------|-------|----------------------------------------|
| TOMm | Bit p |                                        |
|      | TOMmp | 1: Sets the slave channel output mode. |
|      | 1     |                                        |

**Note** TMRm2, TMRm4, TMRm6: MASTERmn bit

TMRm1, TMRm3: SPLITmp bit

TMRm5, TMRm7: Fixed to 0

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)

p: Slave channel number (n < p ≤ 7)

Figure 6-71. Operation Procedure of One-Shot Pulse Output Function (1/2)

|                         | Software Operation                                                                                                                                                                                                                                                         | Hardware Status                                                                                                                                                                                                         |
|-------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TAU default setting     |                                                                                                                                                                                                                                                                            | Power-off status<br>(Clock supply is stopped and writing to each register is disabled.)                                                                                                                                 |
|                         | Sets the TAU0EN bit of peripheral enable registers 0 (PER0) to 1. →                                                                                                                                                                                                        | Power-on status. Each channel stops operating.<br>(Clock supply is started and writing to each register is enabled.)                                                                                                    |
|                         | Sets timer clock select register m (TPSm).<br>Determines clock frequencies of CKm0 and CKm1.                                                                                                                                                                               |                                                                                                                                                                                                                         |
| Channel default setting | Sets timer mode register mn, mp (TMRmn, TMRmp) of two channels to be used (determines operation mode of channels).<br>An output delay is set to timer data register mn (TDRmn) of the master channel, and a pulse width is set to the TDRmp register of the slave channel. | Channel stops operating.<br>(Clock is supplied and some power is consumed.)                                                                                                                                             |
|                         | Sets slave channel.<br>The TOMmp bit of timer output mode register m (TOMm) is set to 1 (slave channel output mode).<br>Sets the TOLmp bit.<br>Sets the TOmp bit and determines default level of the TOmp output. →                                                        | The TOmp pin goes into Hi-Z output state.                                                                                                                                                                               |
|                         | Sets the TOEmp bit to 1 and enables operation of TOmp. →<br>Clears the port register and port mode register to 0. →                                                                                                                                                        | The TOmp default setting level is output when the port mode register is in output mode and the port register is 0.<br>TOmp does not change because channel stops operating.<br>The TOmp pin outputs the TOmp set level. |

(Remark is listed on the next page.)

Figure 6-71. Operation Procedure of One-Shot Pulse Output Function (2/2)

|                  | Software Operation                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Hardware Status                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Operation start  | Sets the TOEmp bit (slave) to 1 (only when operation is resumed).                                                                                                                                                                                                                                                                                                                                                                                                   | The TEMn and TEm bits are set to 1 and the master channel enters the TImn input edge detection wait status. Counter stops operating.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|                  | The TSmn (master) and TSmp (slave) bits of timer channel start register m (TSM) are set to 1 at the same time.                                                                                                                                                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|                  | The TSmn and TSmp bits automatically return to 0 because they are trigger bits.                                                                                                                                                                                                                                                                                                                                                                                     | Master channel starts counting.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| During operation | Detects the TImn pin input valid edge of master channel.                                                                                                                                                                                                                                                                                                                                                                                                            | Master channel loads the value of the TDRmn register to timer count register mn (TCRmn) when the TImn pin valid input edge is detected, and the counter starts counting down. When the count value reaches TCRmn = 0000H, the INTTMmn output is generated, and the counter stops until the next valid edge is input to the TImn pin. The slave channel, triggered by INTTMmn of the master channel, loads the value of the TDRmp register to the TCRmp register, and the counter starts counting down. The output level of TOmp becomes active one count clock after generation of INTTMmn from the master channel. It becomes inactive when TCRmp = 0000H, and the counting operation is stopped. After that, the above operation is repeated. |
|                  | Set values of only the CISmn1 and CISmn0 bits of the TMRmn register can be changed.<br>Sets corresponding bit of noise filter enable register 1, 2 (NFEN1, NFEN2) to 1.<br>Set values of the TMRmp, TDRmn, TDRmp registers, TOMmn, TOMmp, TOLmn, and TOLmp bits cannot be changed.<br>The TCRmn and TCRmp registers can always be read.<br>The TSRmn and TSRmp registers are not used.<br>Set values of the TOM and TOEm registers by slave channel can be changed. |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| Operation stop   | The TTmn (master) and TTmp (slave) bits are set to 1 at the same time.                                                                                                                                                                                                                                                                                                                                                                                              | TEMn, TEm = 0, and count operation stops.<br>The TCRmn and TCRmp registers hold count value and stop.<br>The TOmp output is not initialized but holds current status.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|                  | The TTmn and TTmp bits automatically return to 0 because they are trigger bits.                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| TAU stop         | The TOEmp bit of slave channel is cleared to 0 and value is set to the TOmp bit.                                                                                                                                                                                                                                                                                                                                                                                    | The TOmp pin outputs the TOmp set level.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|                  | To hold the TOmp pin output level<br>Clears the TOmp bit to 0 after the value to be held is set to the port register.<br>When holding the TOmp pin output level is not necessary<br>Setting not required.                                                                                                                                                                                                                                                           | The TOmp pin output level is held by port function.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| TAU stop         | The TAU0EN bit of the PER0 register is cleared to 0.                                                                                                                                                                                                                                                                                                                                                                                                                | Power-off status<br>All circuits are initialized and SFR of each channel is also initialized.<br>(The TOmp bit is cleared to 0 and the TOmp pin is set to port mode.)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)  
p: Slave channel number (n < p ≤ 7)

### 6.8.2 Operation as PWM function

Two channels can be used as a set to generate a pulse of any period and duty factor.

The period and duty factor of the output pulse can be calculated by the following expressions.

Pulse period = {Set value of TDRmn (master) + 1} × Count clock period  
 Duty factor [%] = {Set value of TDRmp (slave)} / {Set value of TDRmn (master) + 1} × 100  
 0% output: Set value of TDRmp (slave) = 0000H  
 100% output: Set value of TDRmp (slave) ≥ {Set value of TDRmn (master) + 1}

**Remark** The duty factor exceeds 100% if the set value of TDRmp (slave) > (set value of TDRmn (master) + 1), it summarizes to 100% output.

The master channel operates in the interval timer mode. If the channel start trigger bit (TSmn) of timer channel start register m (TSM) is set to 1, an interrupt (INTTMmn) is output, the value set to timer data register mn (TDRmn) is loaded to timer count register mn (TCRmn), and the counter counts down in synchronization with the count clock. When the counter reaches 0000H, INTTMmn is output, the value of the TDRmn register is loaded again to the TCRmn register, and the counter counts down. This operation is repeated until the channel stop trigger bit (TTmn) of timer channel stop register m (TTM) is set to 1.

If two channels are used to output a PWM waveform, the period until the master channel counts down to 0000H is the PWM output (TOmp) cycle.

The slave channel operates in one-count mode. By using INTTMmn from the master channel as a start trigger, the TCRmp register loads the value of the TDRmp register and the counter counts down to 0000H. When the counter reaches 0000H, it outputs INTTMmp and waits until the next start trigger (INTTMmn from the master channel) is generated.

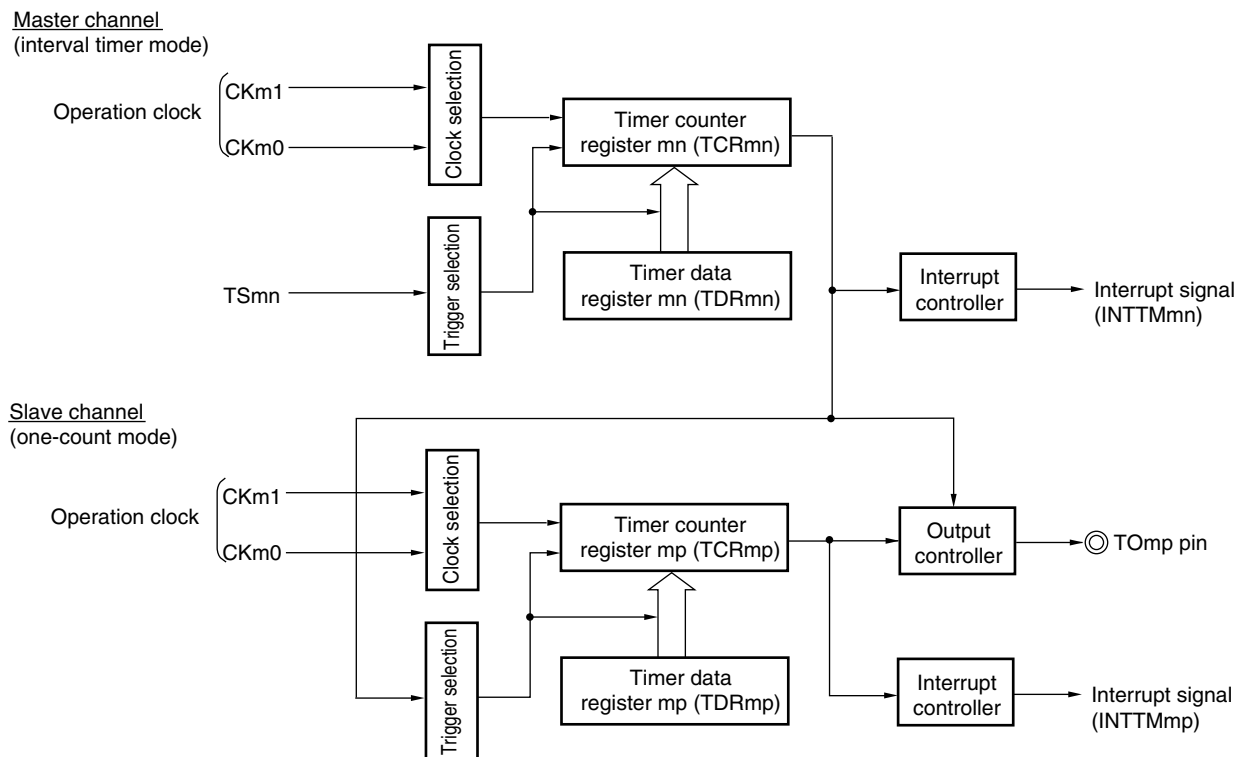
If two channels are used to output a PWM waveform, the period until the slave channel counts down to 0000H is the PWM output (TOmp) duty.

PWM output (TOmp) goes to the active level one clock after the master channel generates INTTMmn and goes to the inactive level when the TCRmp register of the slave channel becomes 0000H.

**Caution** To rewrite both timer data register mn (TDRmn) of the master channel and the TDRmp register of the slave channel, a write access is necessary two times. The timing at which the values of the TDRmn and TDRmp registers are loaded to the TCRmn and TCRmp registers is upon occurrence of INTTMmn of the master channel. Thus, when rewriting is performed split before and after occurrence of INTTMmn of the master channel, the TOmp pin cannot output the expected waveform. To rewrite both the TDRmn register of the master and the TDRmp register of the slave, therefore, be sure to rewrite both the registers immediately after INTTMmn is generated from the master channel.

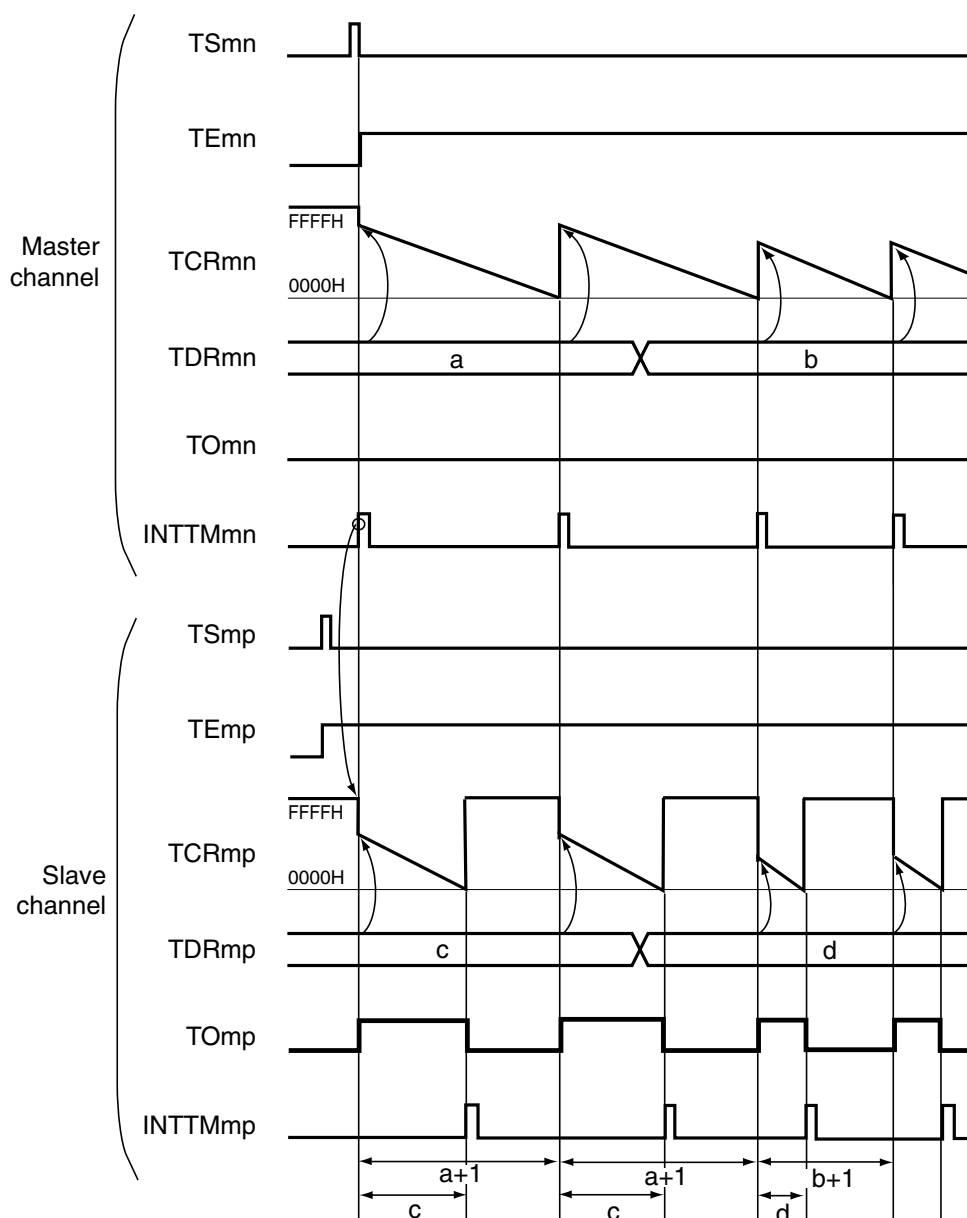
**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)  
 p: Slave channel number (n < p ≤ 7)

Figure 6-72. Block Diagram of Operation as PWM Function



**Remark** m: Unit number ( $m = 0$ ), n: Channel number ( $n = 0, 2, 4, 6$ )  
 p: Slave channel number ( $n < p \leq 7$ )

Figure 6-73. Example of Basic Timing of Operation as PWM Function



**Remark 1.** m: Unit number ( $m = 0$ ), n: Channel number ( $n = 0, 2, 4, 6$ )

p: Slave channel number ( $n < p \leq 7$ )

- 2.** TSmn, TSmp: Bit n, p of timer channel start register m (TSm)

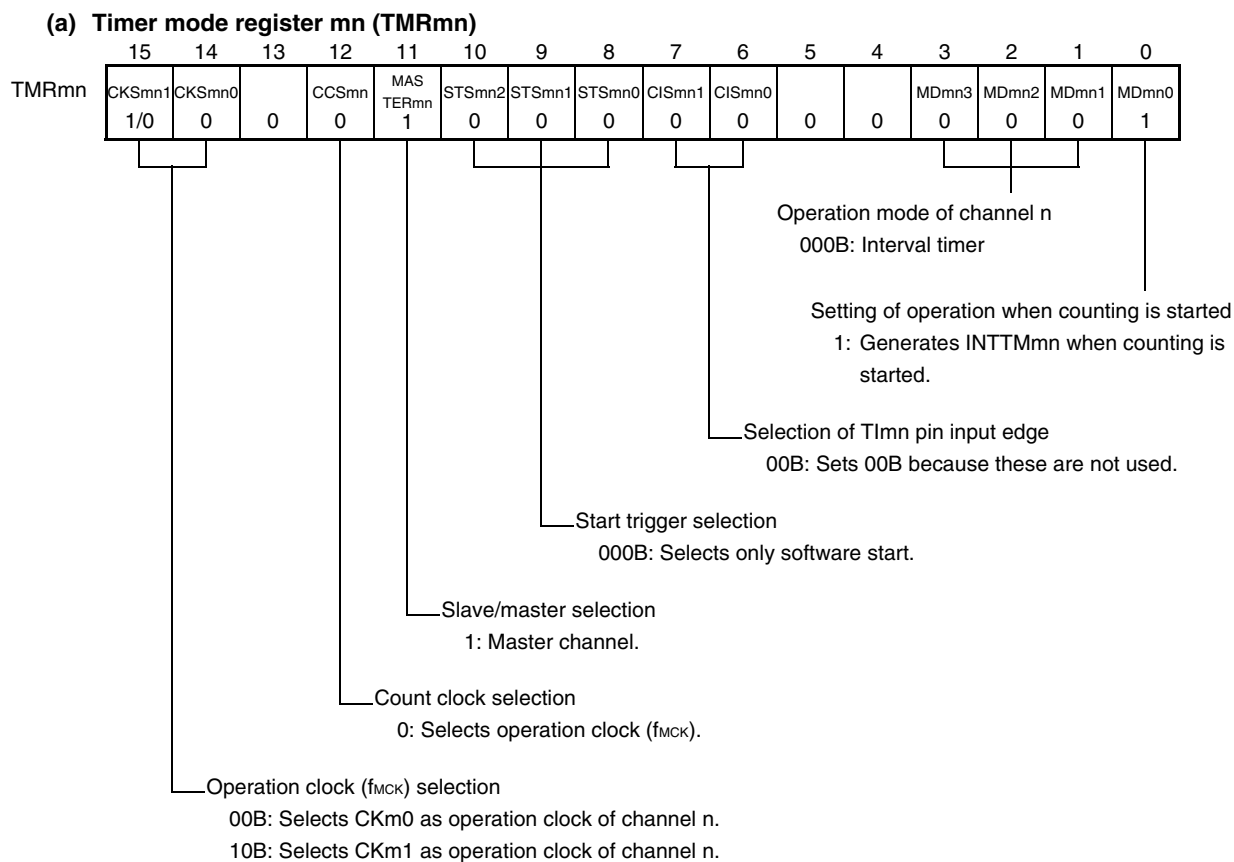
TEmn, TEmp: Bit n, p of timer channel enable status register m (TEm)

TCRmn, TCRmp: Timer count registers mn, mp (TCRmn, TCRmp)

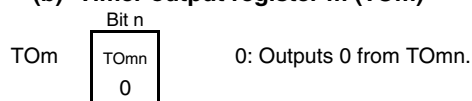
TDRmn, TDRmp: Timer data registers mn, mp (TDRmn, TDRmp)

TOmn, TOmp: TOmn and TOmp pins output signal

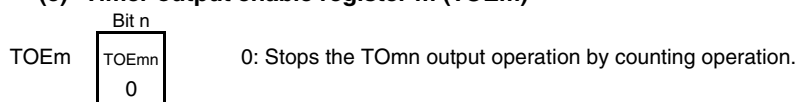
Figure 6-74. Example of Set Contents of Registers When PWM Function (Master Channel) Is Used



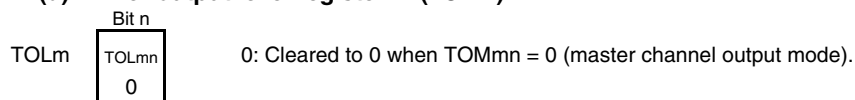
## (b) Timer output register m (TOM)



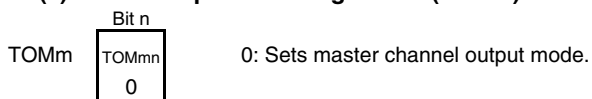
## (c) Timer output enable register m (TOEm)



## (d) Timer output level register m (TOLm)

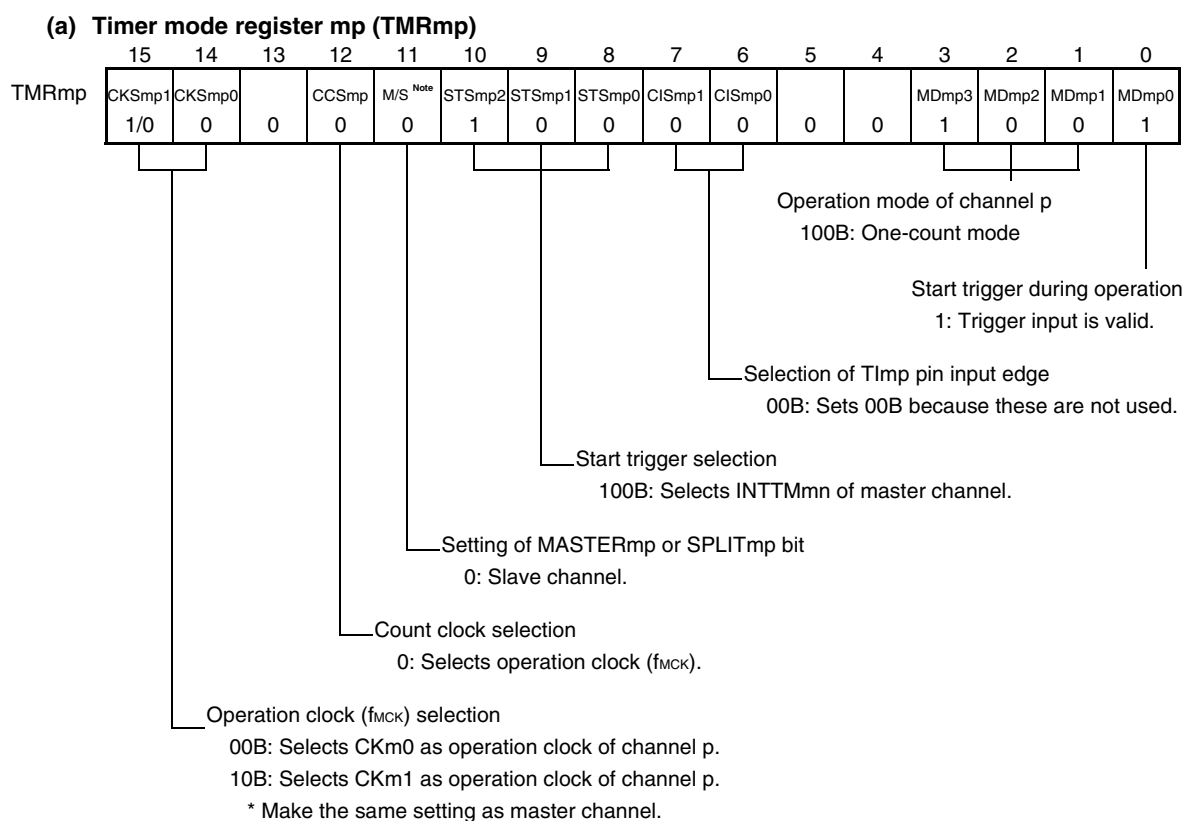


## (e) Timer output mode register m (TOMm)



**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)

Figure 6-75. Example of Set Contents of Registers When PWM Function (Slave Channel) Is Used



## (b) Timer output register m (TOM)

|     |       |                                                    |
|-----|-------|----------------------------------------------------|
| TOM | Bit p |                                                    |
|     | TOMp  | 0: Outputs 0 from TOMp.<br>1: Outputs 1 from TOMp. |
|     |       | 1/0                                                |

## (c) Timer output enable register m (TOEm)

|      |       |                                                                                                                          |
|------|-------|--------------------------------------------------------------------------------------------------------------------------|
| TOEm | Bit p |                                                                                                                          |
|      | TOEmp | 0: Stops the TOMp output operation by counting operation.<br>1: Enables the TOMp output operation by counting operation. |
|      |       | 1/0                                                                                                                      |

## (d) Timer output level register m (TOLm)

|      |       |                                                                                 |
|------|-------|---------------------------------------------------------------------------------|
| TOLm | Bit p |                                                                                 |
|      | TOLmp | 0: Positive logic output (active-high)<br>1: Negative logic output (active-low) |
|      |       | 1/0                                                                             |

## (e) Timer output mode register m (TOMm)

|      |       |                                        |
|------|-------|----------------------------------------|
| TOMm | Bit p |                                        |
|      | TOMmp | 1: Sets the slave channel output mode. |
|      |       | 1                                      |

**Note** TMRm5, TMRm7: Fixed to 0  
 TMRm1, TMRm3: SPLITmp bit

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)  
 p: Slave channel number (n < p ≤ 7)



Figure 6-76. Operation Procedure When PWM Function Is Used (1/2)

|                         | Software Operation                                                                                                                                                                                                                                                                     | Hardware Status                                                                                                                                                                                                         |
|-------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TAU default setting     |                                                                                                                                                                                                                                                                                        | Power-off status<br>(Clock supply is stopped and writing to each register is disabled.)                                                                                                                                 |
|                         | Sets the TAU0EN bit of peripheral enable register 0 (PER0) to 1.                                                                                                                                                                                                                       | Power-on status. Each channel stops operating.<br>(Clock supply is started and writing to each register is enabled.)                                                                                                    |
|                         | Sets timer clock select register m (TPSm).<br>Determines clock frequencies of CKm0 and CKm1.                                                                                                                                                                                           |                                                                                                                                                                                                                         |
| Channel default setting | Sets timer mode registers mn, mp (TMRmn, TMRmp) of two channels to be used (determines operation mode of channels).<br>An interval (period) value is set to timer data register mn (TDRmn) of the master channel, and a duty factor is set to the TDRmp register of the slave channel. | Channel stops operating.<br>(Clock is supplied and some power is consumed.)                                                                                                                                             |
|                         | Sets slave channel.<br>The TOMmp bit of timer output mode register m (TOMm) is set to 1 (slave channel output mode).<br>Sets the TOLmp bit.<br>Sets the TOmp bit and determines default level of the TOmp output.                                                                      | The TOmp pin goes into Hi-Z output state.                                                                                                                                                                               |
|                         | Sets the TOEmp bit to 1 and enables operation of TOmp.<br>Clears the port register and port mode register to 0.                                                                                                                                                                        | The TOmp default setting level is output when the port mode register is in output mode and the port register is 0.<br>TOmp does not change because channel stops operating.<br>The TOmp pin outputs the TOmp set level. |

(Remark is listed on the next page.)

Figure 6-76. Operation Procedure When PWM Function Is Used (2/2)

|                  | Software Operation                                                                                                                                                                                                                                                                                                                         | Hardware Status                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Operation start  | <p>Sets the TOEmp bit (slave) to 1 (only when operation is resumed).</p> <p>The TSmn (master) and TSmp (slave) bits of timer channel start register m (TSM) are set to 1 at the same time.</p> <p>The TSmn and TSmp bits automatically return to 0 because they are trigger bits.</p>                                                      | <p>TEmn = 1, TEm = 1</p> <p>► When the master channel starts counting, INTTMmn is generated. Triggered by this interrupt, the slave channel also starts counting.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| During operation | <p>Set values of the TMRmn and TMRmp registers, TOMmn, TOMmp, TOLmn, and TOLmp bits cannot be changed.</p> <p>Set values of the TDRmn and TDRmp registers can be changed after INTTMmn of the master channel is generated.</p> <p>The TCRmn and TCRmp registers can always be read.</p> <p>The TSRmn and TSRmp registers are not used.</p> | <p>The counter of the master channel loads the TDRmn register value to timer count register mn (TCRmn), and counts down. When the count value reaches TCRmn = 0000H, INTTMmn output is generated. At the same time, the value of the TDRmn register is loaded to the TCRmn register, and the counter starts counting down again.</p> <p>At the slave channel, the value of the TDRmp register is loaded to the TCRmp register, triggered by INTTMmn of the master channel, and the counter starts counting down. The output level of TOmp becomes active one count clock after generation of the INTTMmn output from the master channel. It becomes inactive when TCRmp = 0000H, and the counting operation is stopped.</p> <p>After that, the above operation is repeated.</p> |
| Operation stop   | <p>The TTmn (master) and TTmp (slave) bits are set to 1 at the same time.</p> <p>The TTmn and TTmp bits automatically return to 0 because they are trigger bits.</p> <p>The TOEmp bit of slave channel is cleared to 0 and value is set to the TOmp bit.</p>                                                                               | <p>TEmn, TEm = 0, and count operation stops.</p> <p>The TCRmn and TCRmp registers hold count value and stop.</p> <p>The TOmp output is not initialized but holds current status.</p> <p>-----</p> <p>► The TOmp pin outputs the TOmp set level.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| TAU stop         | <p>To hold the TOmp pin output level</p> <p>Clears the TOmp bit to 0 after the value to be held is set to the port register.</p> <p>When holding the TOmp pin output level is not necessary</p> <p>Setting not required.</p> <p>The TAU0EN bit of the PER0 register is cleared to 0.</p>                                                   | <p>► The TOmp pin output level is held by port function.</p> <p>-----</p> <p>► Power-off status</p> <p>All circuits are initialized and SFR of each channel is also initialized.</p> <p>(The TOmp bit is cleared to 0 and the TOmp pin is set to port mode.)</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)

p: Slave channel number (n < p ≤ 7)

### 6.8.3 Operation as multiple PWM output function

By extending the PWM function and using multiple slave channels, many PWM waveforms with different duty values can be output.

For example, when using two slave channels, the period and duty factor of an output pulse can be calculated by the following expressions.

$$\begin{aligned}\text{Pulse period} &= \{\text{Set value of TDRmn (master)} + 1\} \times \text{Count clock period} \\ \text{Duty factor 1 [\%]} &= \{\text{Set value of TDRmp (slave 1)}\} / \{\text{Set value of TDRmn (master)} + 1\} \times 100 \\ \text{Duty factor 2 [\%]} &= \{\text{Set value of TDRmq (slave 2)}\} / \{\text{Set value of TDRmn (master)} + 1\} \times 100\end{aligned}$$

**Remark** Although the duty factor exceeds 100% if the set value of TDRmp (slave 1) > {set value of TDRmn (master) + 1} or if the {set value of TDRmq (slave 2)} > {set value of TDRmn (master) + 1}, it is summarized into 100% output.

Timer count register mn (TCRmn) of the master channel operates in the interval timer mode and counts the periods.

The TCRmp register of the slave channel 1 operates in one-count mode, counts the duty factor, and outputs a PWM waveform from the TOmp pin. The TCRmp register loads the value of timer data register mp (TDRmp), using INTTMmn of the master channel as a start trigger, and starts counting down. When TCRmp = 0000H, TCRmp outputs INTTMmp and stops counting until the next start trigger (INTTMmn of the master channel) has been input. The output level of TOmp becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmp = 0000H.

In the same way as the TCRmp register of the slave channel 1, the TCRmq register of the slave channel 2 operates in one-count mode, counts the duty factor, and outputs a PWM waveform from the TOMq pin. The TCRmq register loads the value of the TDRmq register, using INTTMmn of the master channel as a start trigger, and starts counting down. When TCRmq = 0000H, the TCRmq register outputs INTTMmq and stops counting until the next start trigger (INTTMmn of the master channel) has been input. The output level of TOMq becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmq = 0000H.

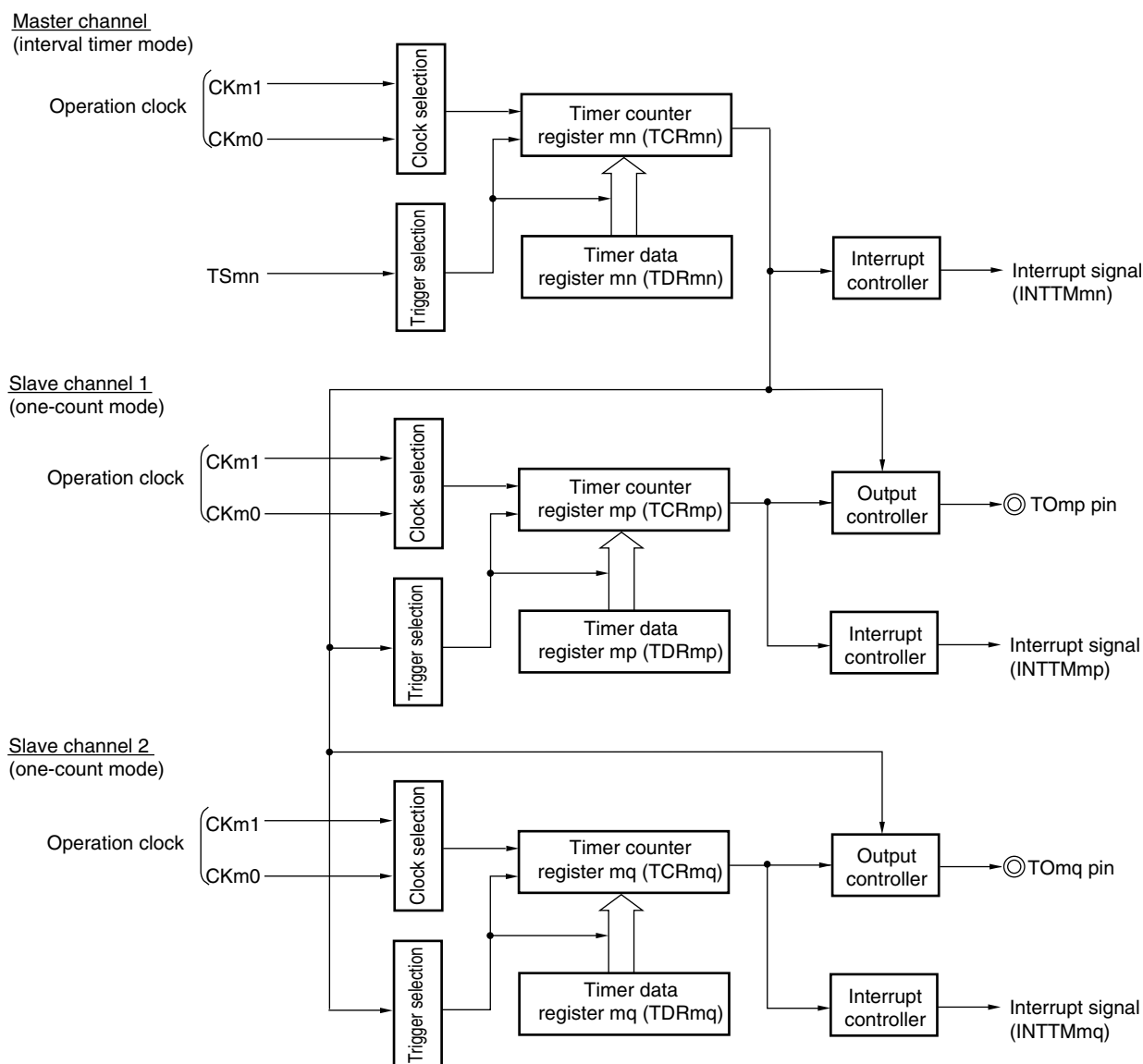
When channel 0 is used as the master channel as above, up to seven types of PWM signals can be output at the same time.

**Caution** To rewrite both timer data register mn (TDRmn) of the master channel and the TDRmp register of the slave channel 1, write access is necessary at least twice. Since the values of the TDRmn and TDRmp registers are loaded to the TCRmn and TCRmp registers after INTTMmn is generated from the master channel, if rewriting is performed separately before and after generation of INTTMmn from the master channel, the TOmp pin cannot output the expected waveform. To rewrite both the TDRmn register of the master and the TDRmp register of the slave, be sure to rewrite both the registers immediately after INTTMmn is generated from the master channel (This applies also to the TDRmq register of the slave channel 2).

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 2, 4)

p: Slave channel number 1, q: Slave channel number 2

<R> n < p < q ≤ 7 (Where p and q are integers greater than n)

**Figure 6-77. Block Diagram of Operation as Multiple PWM Output Function (output two types of PWMs)**

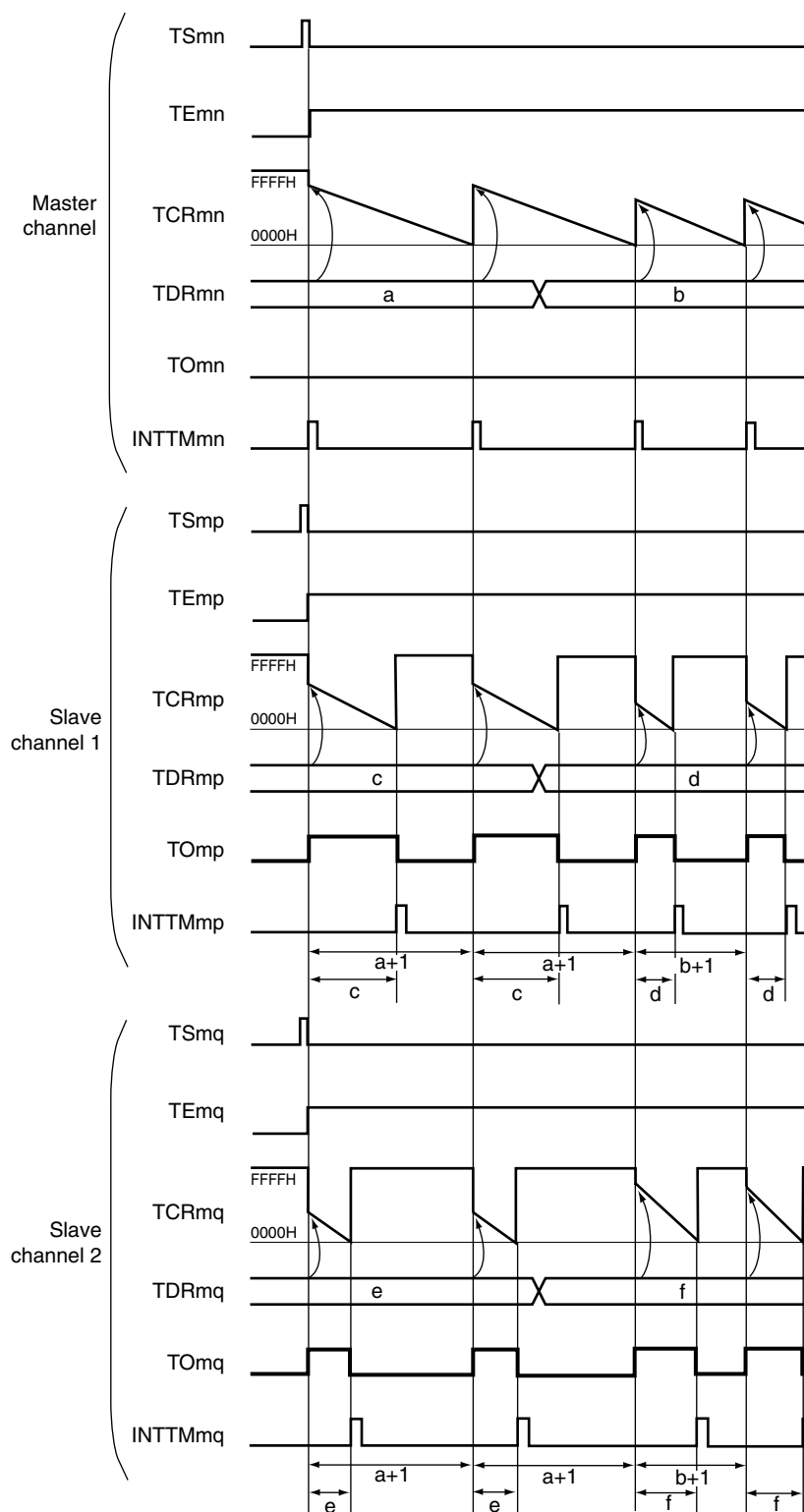
**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 2, 4)

p: Slave channel number 1, q: Slave channel number 2

n < p < q ≤ 7 (Where p and q are integers greater than n)

<R>

**Figure 6-78. Example of Basic Timing of Operation as Multiple PWM Output Function  
(Output two types of PWMs) (1/2)**



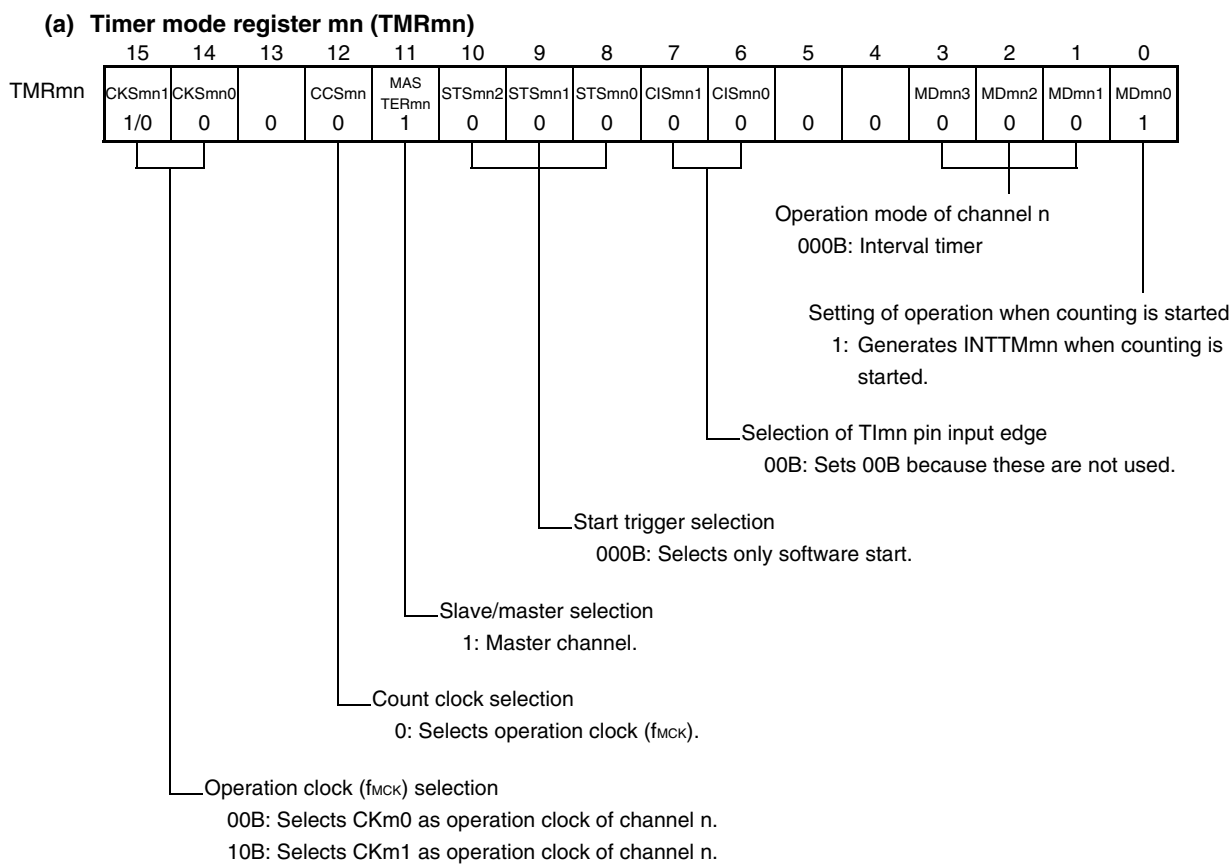
(Remark is listed on the next page.)

**Figure 6-78. Example of Basic Timing of Operation as Multiple PWM Output Function  
(Output two types of PWMs) (2/2)**

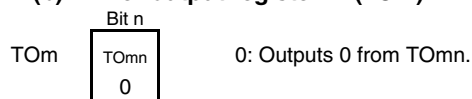
- Remark 1.** m: Unit number (m = 0), n: Channel number (n = 0, 2, 4)  
 p: Slave channel number 1, q: Slave channel number 2  
 n < p < q ≤ 7 (Where p and q are integers greater than n)
- 2.** TSmn, TSmp, TSmq: Bit n, p, q of timer channel start register m (TSM)  
 TEMn, TEmq, TEmq: Bit n, p, q of timer channel enable status register m (TEM)  
 TCRmn, TCRmp, TCRmq: Timer count registers mn, mp, mq (TCRmn, TCRmp, TCRmq)  
 TDRmn, TDRmp, TDRmq: Timer data registers mn, mp, mq (TDRmn, TDRmp, TDRmq)  
 TOMn, TOMp, TOMq: TOMn, TOMp, and TOMq pins output signal

<R>

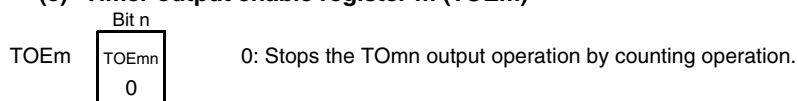
**Figure 6-79. Example of Set Contents of Registers  
When Multiple PWM Output Function (Master Channel) Is Used**



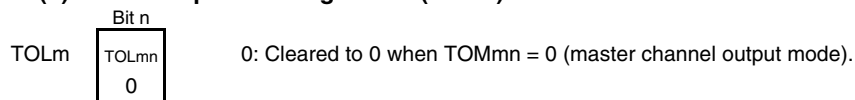
**(b) Timer output register m (TOM)**



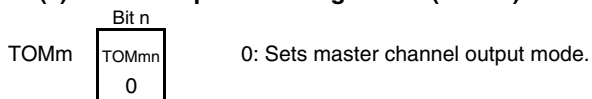
**(c) Timer output enable register m (TOEm)**



**(d) Timer output level register m (TOLm)**



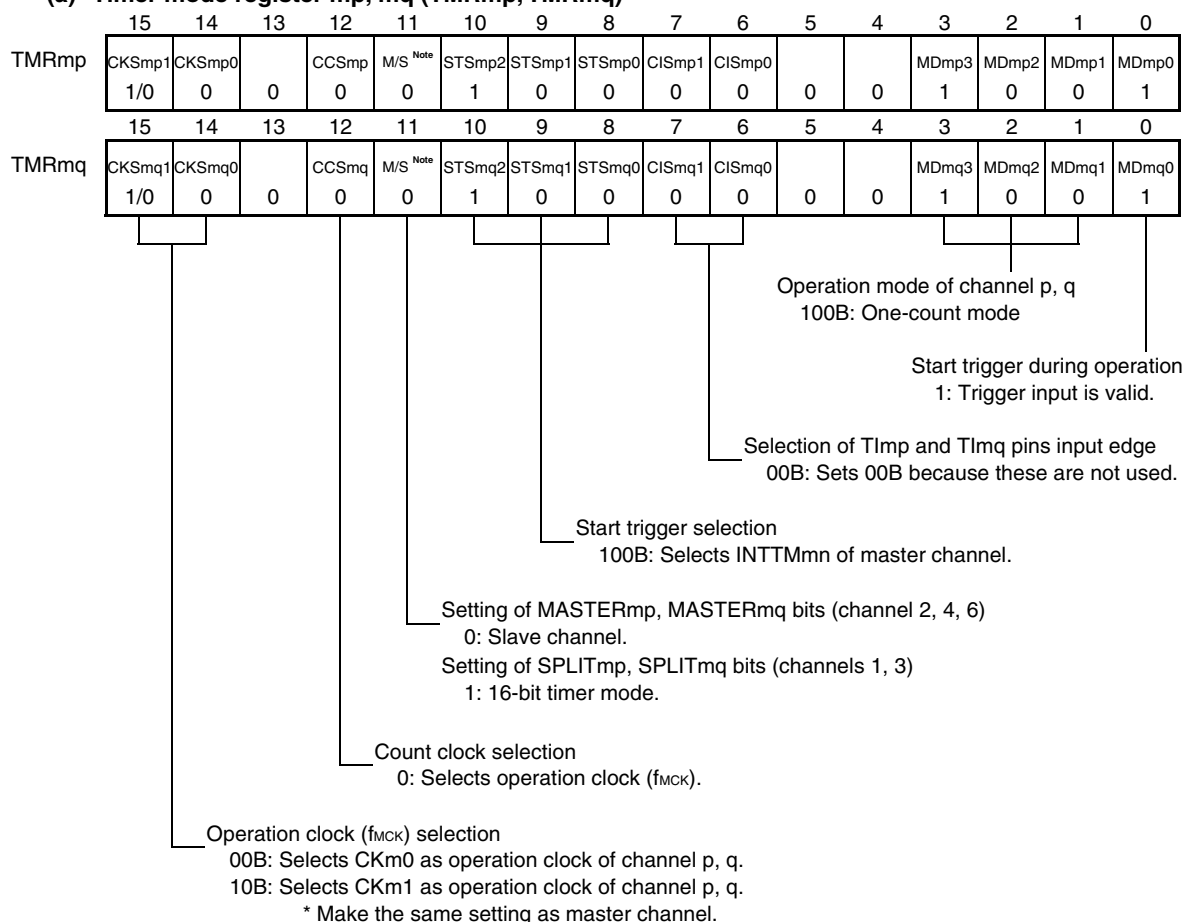
**(e) Timer output mode register m (TOMm)**



**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 2, 4)

**Figure 6-80. Example of Set Contents of Registers**  
**When Multiple PWM Output Function (Slave Channel) Is Used (output two types of PWMs)**

**(a) Timer mode register mp, mq (TMRmp, TMRmq)**



**(b) Timer output register m (TOM)**

|     | Bit q | Bit p |                                 |
|-----|-------|-------|---------------------------------|
| TOM | TOmq  | TOmp  | 0: Outputs 0 from TOmp or TOmq. |
|     | 1/0   | 1/0   | 1: Outputs 1 from TOmp or TOmq. |

**(c) Timer output enable register m (TOEm)**

|      | Bit q | Bit p |                                                                     |
|------|-------|-------|---------------------------------------------------------------------|
| TOEm | TOEmq | TOEmp | 0: Stops the TOmp or TOmq output operation by counting operation.   |
|      | 1/0   | 1/0   | 1: Enables the TOmp or TOmq output operation by counting operation. |

**(d) Timer output level register m (TOLm)**

|      | Bit q | Bit p |                                        |
|------|-------|-------|----------------------------------------|
| TOLm | TOLmq | TOLmp | 0: Positive logic output (active-high) |
|      | 1/0   | 1/0   | 1: Negative logic output (active-low)  |

**(e) Timer output mode register m (TOMm)**

|      | Bit q | Bit p |                                        |
|------|-------|-------|----------------------------------------|
| TOMm | TOMmq | TOMmp | 1: Sets the slave channel output mode. |
|      | 1     | 1     |                                        |

**Note** TMRm5, TMRm7: Fixed to 0

TMRm1, TMRm3: SPLITmp, SPLIT0q bit

TMRm2, TMRm4, TMRm6: MASTERmp, MASTERmq bit

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 2, 4)

p: Slave channel number 1, q: Slave channel number 2

n < p < q ≤ 7 (Where p and q are integers greater than n)

<R>



**Figure 6-81. Operation Procedure When Multiple PWM Output Function Is Used (1/2)**

|                         | Software Operation                                                                                                                                                                                                                                                                                            | Hardware Status                                                                                                               |
|-------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|
| TAU default setting     |                                                                                                                                                                                                                                                                                                               | Power-off status<br>(Clock supply is stopped and writing to each register is disabled.)                                       |
|                         | Sets the TAU0EN bit of peripheral enable register 0 (PER0) to 1. →                                                                                                                                                                                                                                            | Power-on status. Each channel stops operating.<br>(Clock supply is started and writing to each register is enabled.)          |
|                         | Sets timer clock select register m (TPSm).<br>Determines clock frequencies of CKm0 and CKm1.                                                                                                                                                                                                                  |                                                                                                                               |
| Channel default setting | Sets timer mode registers mn, mp, 0q (TMRmn, TMRmp, TMRmq) of each channel to be used (determines operation mode of channels).<br>An interval (period) value is set to timer data register mn (TDRmn) of the master channel, and a duty factor is set to the TDRmp and TDRmq registers of the slave channels. | Channel stops operating.<br>(Clock is supplied and some power is consumed.)                                                   |
|                         | Sets slave channels.<br>The TOMmp and TOMmq bits of timer output mode register m (TOMm) are set to 1 (slave channel output mode).<br>Sets the TOLmp and TOLmq bits.<br>Sets the TOmp and TOMq bits and determines default level of the TOmp and TOMq outputs. →                                               | The TOmp and TOMq pins go into Hi-Z output state.                                                                             |
|                         | Sets the TOEmp and TOEmq bits to 1 and enables operation of TOmp and TOMq. →                                                                                                                                                                                                                                  | The TOmp and TOMq default setting levels are output when the port mode register is in output mode and the port register is 0. |
|                         | Clears the port register and port mode register to 0. →                                                                                                                                                                                                                                                       | TOmp and TOMq do not change because channels stop operating.                                                                  |
|                         |                                                                                                                                                                                                                                                                                                               | The TOmp and TOMq pins output the TOmp and TOMq set levels.                                                                   |

(Note and Remark are listed on the next page.)

Figure 6-81. Operation Procedure When Multiple PWM Output Function Is Used (2/2)

|                  | Software Operation                                                                                                                                                                                                                                                                                                                                                | Hardware Status                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Operation start  | (Sets the TOEmp and TOEmq (slave) bits to 1 only when resuming operation.)<br>The TSmn bit (master), and TSmp and TSmq (slave) bits of timer channel start register m (TSM) are set to 1 at the same time.<br>The TSmn, TSmp, and TSmq bits automatically return to 0 because they are trigger bits.                                                              | TEmn = 1, TEmq = 1<br>When the master channel starts counting, INTTMmn is generated. Triggered by this interrupt, the slave channel also starts counting.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| During operation | Set values of the TMRmn, TMRmp, TMRmq registers, TOMmn, TOMmp, TOMmq, TOLmn, TOLmp, and TOLmq bits cannot be changed.<br>Set values of the TDRmn, TDRmp, and TDRmq registers can be changed after INTTMmn of the master channel is generated.<br>The TCRmn, TCRmp, and TCRmq registers can always be read.<br>The TSRmn, TSRmp, and TSR0q registers are not used. | The counter of the master channel loads the TDRmn register value to timer count register mn (TCRmn) and counts down. When the count value reaches TCRmn = 0000H, INTTMmn output is generated. At the same time, the value of the TDRmn register is loaded to the TCRmn register, and the counter starts counting down again.<br>At the slave channel 1, the values of the TDRmp register are transferred to the TCRmp register, triggered by INTTMmn of the master channel, and the counter starts counting down. The output levels of TOmp become active one count clock after generation of the INTTMmn output from the master channel. It becomes inactive when TCRmp = 0000H, and the counting operation is stopped.<br>At the slave channel 2, the values of the TDRmq register are transferred to TCRmq register, triggered by INTTMmn of the master channel, and the counter starts counting down. The output levels of TOMq become active one count clock after generation of the INTTMmn output from the master channel. It becomes inactive when TCRmq = 0000H, and the counting operation is stopped. After that, the above operation is repeated. |
| Operation stop   | The TTmn bit (master), TTmp, and TTmq (slave) bits are set to 1 at the same time.<br>The TTmn, TTmp, and TTmq bits automatically return to 0 because they are trigger bits.                                                                                                                                                                                       | TEmn, TEmq = 0, and count operation stops.<br>The TCRmn, TCRmp, and TCRmq registers hold count value and stop.<br>The TOmp and TOMq output are not initialized but hold current status.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|                  | The TOEmp and TOEmq bits of slave channels are cleared to 0 and value is set to the TOmp and TOMq bits.                                                                                                                                                                                                                                                           | The TOmp and TOMq pins output the TOmp and TOMq set levels.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| TAU stop         | To hold the TOmp and TOMq pin output levels<br>Clears the TOmp and TOMq bits to 0 after the value to be held is set to the port register.<br>When holding the TOmp and TOMq pin output levels are not necessary<br>Setting not required                                                                                                                           | The TOmp and TOMq pin output levels are held by port function.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                  | The TAU0EN bit of the PER0 register is cleared to 0.                                                                                                                                                                                                                                                                                                              | Power-off status<br>All circuits are initialized and SFR of each channel is also initialized.<br>(The TOmp and TOMq bits are cleared to 0 and the TOmp and TOMq pins are set to port mode.)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 2, 4)  
p: Slave channel number 1, q: Slave channel number 2  
n < p < q ≤ 7 (Where p and q are a integer greater than n)

#### 6.8.4 Remote control output function

The PWM output function is applied to the remote control output function.

The pairings of channels 2 and 3 and channels 6 and 7 are used to output the PWM signal (See **6.8.2 Operation as PWM function** for how to set up each channel.). The PWM signal output from channel 3 is used as a mask wave, the PWM signal output from channel 7 is used as a carrier waves, and the logical products of these signals are output as remote control output.

The high level width output part of the remote control output is composed of a 20 to 60 kHz carrier signal.

**Figure 6-82. Remote Control Output**

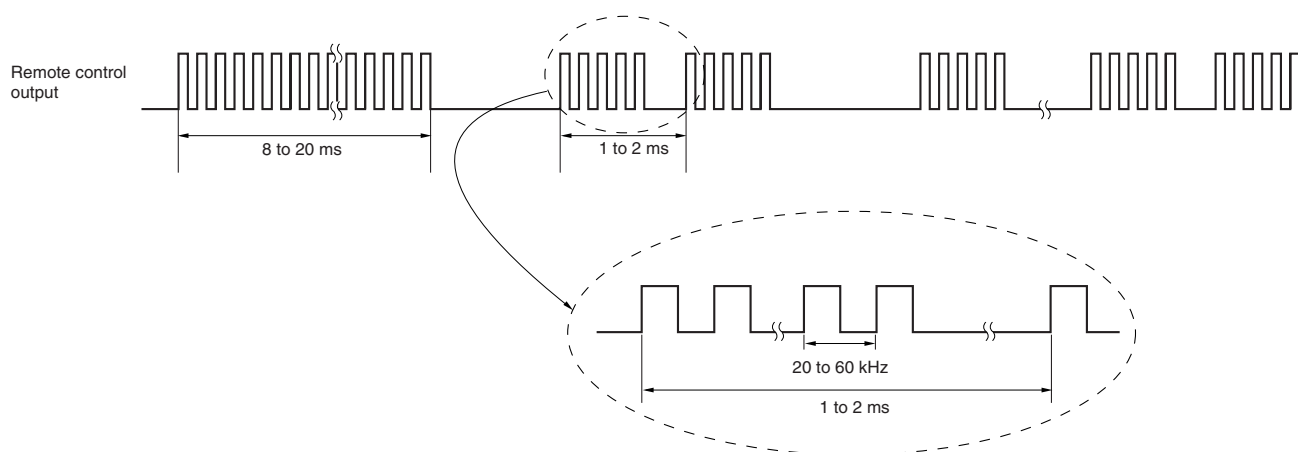


Figure 6-79 shows the steps for setting the remote control output.

&lt;R&gt;

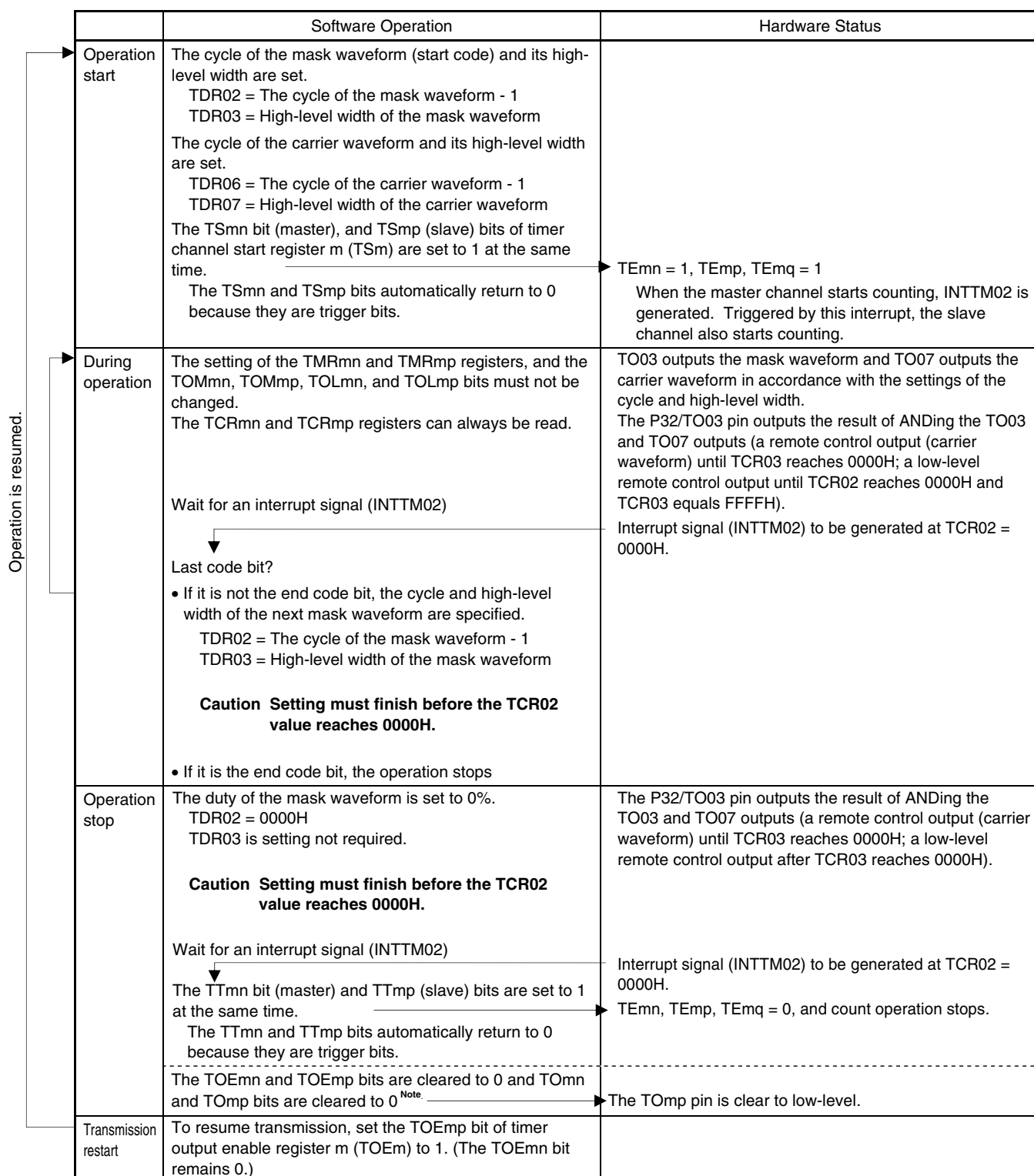
**Figure 6-83. Procedure for Setting Remote Control Output (1/2)**

|                               | Software Operation                                                                                                                                                                                                   | Hardware Status                                                                                                                                                                                                                                                 |
|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Pin mode setting              | Sets the PFSEG17 bit of PFSEG2 register, PM32 bit of PM3 register, PU3 bit of PFSEG2 register and P32 bit of P3 register to 1                                                                                        | Remote control output is invalid<br>P32/TO03 pin is low-level output                                                                                                                                                                                            |
| TAU default setting           |                                                                                                                                                                                                                      | Power-off status<br>(Clock supply is stopped and writing to each register is disabled.)                                                                                                                                                                         |
|                               | Sets the TAU0EN bit of peripheral enable register 0 (PER0) to 1.                                                                                                                                                     | Power-on status. Each channel stops operating.<br>(Clock supply is started and writing to each register is enabled.)                                                                                                                                            |
|                               | Sets timer clock select register 0 (TPS0).<br>Determines clock frequencies of CK00 and CK01.                                                                                                                         |                                                                                                                                                                                                                                                                 |
| Remote control output setting | The TOS0 bit of the Timer output select register (TOS) is set to 1.                                                                                                                                                  | Remote control output is valid<br>The P32/TO03 pin outputs the result (Low) of ANDING TO03 (Low) and TO07 (Low).<br>P32/TO03 pin can only be used as a remote control output<br>P53/TO07 pin can only be used as a alternative function other than timer output |
| Channel default setting       | Sets timer mode register mn (TMRmn) to 0801H and sets timer mode register mp (TMRmp) to 0409H determines operation mode of channels)..                                                                               | Channel stops operating.<br>(Clock is supplied and some power is consumed.)                                                                                                                                                                                     |
|                               | Sets master channels.<br>The TOMmn bit of timer output mode register m (TOMm) is set to 0 (master channel output mode).<br>Sets the TOLmn bit.<br>Sets the TOMn bit and determines default level of the TOMn output. | The TOMn pin goes into Hi-Z output state.                                                                                                                                                                                                                       |
|                               |                                                                                                                                                                                                                      | The TOMn default setting level is output when the port mode register is in output mode and the port register is 0.                                                                                                                                              |
|                               | Sets the TOEmn bit to 1 and enables operation of TOMn.                                                                                                                                                               | TOMn does not change because channels stop operating.                                                                                                                                                                                                           |
|                               | Clears the port register and port mode register to 0.                                                                                                                                                                | The TOMn pin outputs the TOMn set level.                                                                                                                                                                                                                        |
|                               | Sets slave channels.<br>The TOMmp bit of timer output mode register m (TOMm) is set to 1 (slave channel output mode).<br>Sets the TOLmp bit.<br>Sets the TOMp bit and determines default level of the TOMp output.   | The TOMp pin goes into Hi-Z output state.                                                                                                                                                                                                                       |
|                               |                                                                                                                                                                                                                      | The TOMp default setting level is output when the port mode register is in output mode and the port register is 0.                                                                                                                                              |
|                               | Sets the TOEmp bit to 1 and enables operation of TOMp.                                                                                                                                                               | TOMP does not change because channels stop operating.                                                                                                                                                                                                           |
|                               | Clears the port register and port mode register to 0.                                                                                                                                                                | The TOMp pin outputs the TOMp set level.                                                                                                                                                                                                                        |

(Remark is listed on the next page.)

&lt;R&gt;

Figure 6-83. Procedure for Setting Remote Control Output (2/2)



**Note** If these bits are not used by any TAU channel, clock supply may be stopped by clearing the TAU0EN bit of peripheral enable register 0 (PER0) to 0. In this case, to resume transmission, the settings for transmission must be re-specified after the power is turned on.

**Remark** m: Unit number (m = 0), n: Master channel number (n = 2, 6)  
 p: Slave channel number (p = 3, 7)  
 (When mask waveform: n = 2, n = 3 ; When carrier waveform: n = 6, p = 7)

## CHAPTER 7 REAL-TIME CLOCK

### 7.1 Functions of Real-time Clock

The real-time clock has the following features.

- Having counters of year, month, week, day, hour, minute, and second, and can count up to 99 years.
- Constant-period interrupt function (period: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month)
- Alarm interrupt function (alarm: week, hour, minute)
- Pin output function of 1 Hz (44, 48, 52, and 64-pin products only)

**Caution** The count of year, month, week, day, hour, minutes and second can only be performed when a subsystem clock ( $f_{SUB} = 32.768 \text{ kHz}$ ) is selected as the operation clock of the real-time clock. When the low-speed on-chip oscillator clock ( $f_{IL} = 15 \text{ kHz}$ ) is selected, only the constant-period interrupt function is available. The 32-pin products have the constant-period interrupt function only, because these products have no subsystem clock. However, the constant-period interrupt interval when  $f_{IL}$  is selected will be calculated with the constant-period (the value selected with RTCC0 register)  $\times f_{SUB}/f_{IL}$ .

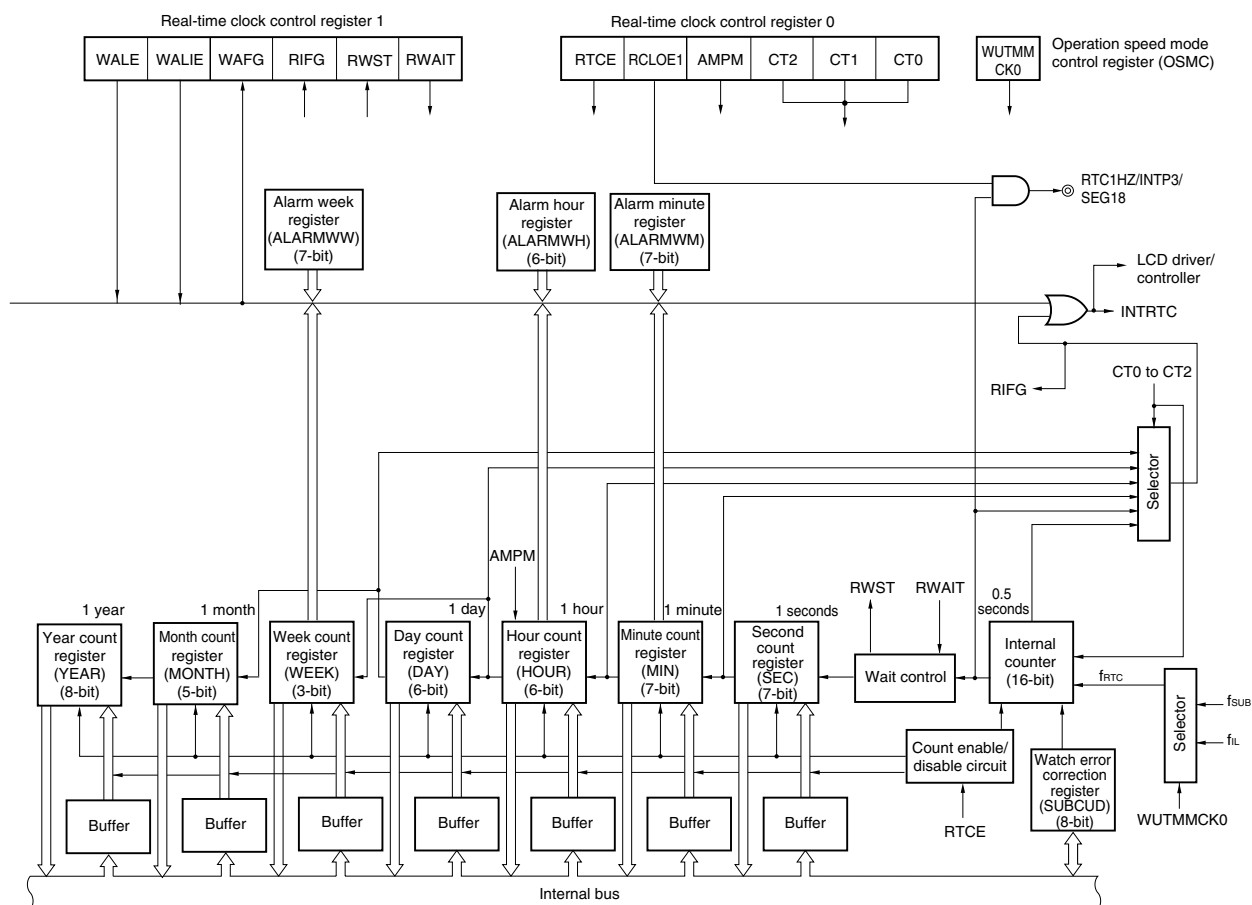
### 7.2 Configuration of Real-time Clock

The real-time clock includes the following hardware.

**Table 7-1. Configuration of Real-time Clock**

| Item              | Configuration                                |
|-------------------|----------------------------------------------|
| Counter           | Counter (16-bit)                             |
| Control registers | Peripheral enable register 0 (PER0)          |
|                   | Operation speed mode control register (OSMC) |
|                   | Real-time clock control register 0 (RTCC0)   |
|                   | Real-time clock control register 1 (RTCC1)   |
|                   | Second count register (SEC)                  |
|                   | Minute count register (MIN)                  |
|                   | Hour count register (HOUR)                   |
|                   | Day count register (DAY)                     |
|                   | Week count register (WEEK)                   |
|                   | Month count register (MONTH)                 |
|                   | Year count register (YEAR)                   |
|                   | Watch error correction register (SUBCUD)     |
|                   | Alarm minute register (ALARMWM)              |
|                   | Alarm hour register (ALARMWH)                |
|                   | Alarm week register (ALARMWW)                |

**Figure 7-1. Block Diagram of Real-time Clock**



**Caution** The count of year, month, week, day, hour, minutes and second can only be performed when a subsystem clock ( $f_{\text{SUB}} = 32.768 \text{ kHz}$ ) is selected as the operation clock of the real-time clock. When the low-speed on-chip oscillator clock ( $f_{\text{IL}} = 15 \text{ kHz}$ ) is selected, only the constant-period interrupt function is available. The 32-pin products have the constant-period interrupt function only, because these products have no subsystem clock. However, the constant-period interrupt interval when  $f_{\text{IL}}$  is selected will be calculated with the constant-period (the value selected with RTCC0 register)  $\times f_{\text{SUB}}/f_{\text{IL}}$ .

### 7.3 Registers Controlling Real-time Clock

The real-time clock is controlled by the following registers.

- Peripheral enable register 0 (PER0)
- Operation speed mode control register (OSMC)
- Real-time clock control register 0 (RTCC0)
- Real-time clock control register 1 (RTCC1)
- Second count register (SEC)
- Minute count register (MIN)
- Hour count register (HOUR)
- Day count register (DAY)
- Week count register (WEEK)
- Month count register (MONTH)
- Year count register (YEAR)
- Watch error correction register (SUBCUD)
- Alarm minute register (ALARMWM)
- Alarm hour register (ALARMWH)
- Alarm week register (ALARMWW)



### 7.3.1 Peripheral enable register 0 (PER0)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When the real-time clock is used, be sure to set bit 7 (RTCEN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 7-2. Format of Peripheral Enable Register 0 (PER0)**

Address: F00F0H After reset: 00H R/W

| Symbol | <7>   | 6 | <5>   | <4>     | 3 | <2>    | 1 | <0>    |
|--------|-------|---|-------|---------|---|--------|---|--------|
| PER0   | RTCEN | 0 | ADCEN | IICA0EN | 0 | SAU0EN | 0 | TAU0EN |

| RTCEN | Real-time clock (RTC) and 12-bit interval timer                                                                                                                                                                                                         | LCD driver/controller and clock output/buzzer output controller                                                                                                                                    |                                                                                                                                                                                                      |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |                                                                                                                                                                                                                                                         | When subsystem clock ( $f_{SUB}$ ) is selected                                                                                                                                                     | When subsystem clock ( $f_{SUB}$ ) is not selected                                                                                                                                                   |
| 0     | Stops input clock supply.<br><ul style="list-style-type: none"> <li>SFR used by the real-time clock (RTC) and 12-bit interval timer cannot be written.</li> <li>The real-time clock (RTC) and 12-bit interval timer are in the reset status.</li> </ul> | Stops input clock and subsystem clock supply.<br><ul style="list-style-type: none"> <li>SFR used by the LCD driver/controller and clock output/buzzer output can be read and written.</li> </ul>   | Enables input clock and main system clock supply.<br><ul style="list-style-type: none"> <li>SFR used by the LCD driver/controller and clock output/buzzer output can be read and written.</li> </ul> |
| 1     | Enables input clock supply.<br><ul style="list-style-type: none"> <li>SFR used by the real-time clock (RTC) and 12-bit interval timer can be read and written.</li> </ul>                                                                               | Enables input clock and subsystem clock supply.<br><ul style="list-style-type: none"> <li>SFR used by the LCD driver/controller and clock output/buzzer output can be read and written.</li> </ul> |                                                                                                                                                                                                      |

- Cautions**
1. When using the real-time clock, first set the RTCEN bit to 1, while oscillation of the input clock ( $f_{RTC}$ ) is stable. If RTCEN = 0, writing to a control register of the real-time clock, or 12-bit interval timer is ignored, and, even if the register is read, only the default value is read.
  2. The subsystem clock supply to peripheral functions other than the real-time clock, 12-bit interval timer, and LCD driver/controller can be stopped in HALT mode when the subsystem clock is used, by setting the RTCLPC bit of the operation speed mode control register (OSMC) to 1. In this case, set the RTCEN bit of the PER0 register to 1 and the other bits (bits 0 to 6) to 0.
  3. Be sure to clear the bits 1, 3, and 6 to 0.

### 7.3.2 Operation speed mode control register (OSMC)

The WUTMMCK0 bit can be used to select the real-time clock operation clock ( $f_{RTC}$ ).

In addition, by stopping clock functions that are unnecessary, the RTCLPC bit can be used to reduce power consumption. For details about setting the RTCLPC bit, see **CHAPTER 5 CLOCK GENERATOR**.

The OSMC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 7-3. Format of Operation Speed Mode Control Register (OSMC)**

Address: F00F3H After reset: 00H R/W

|        |        |   |   |          |   |   |   |   |
|--------|--------|---|---|----------|---|---|---|---|
| Symbol | 7      | 6 | 5 | 4        | 3 | 2 | 1 | 0 |
| OSMC   | RTCLPC | 0 | 0 | WUTMMCK0 | 0 | 0 | 0 | 0 |

|                                 |                                                                                                     |                                                                          |
|---------------------------------|-----------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|
| WUTMMCK0<br><small>Note</small> | Selection of operation clock for real-time clock, 12-bit interval timer, and LCD driver/controller. | Selection of clock output from PCLBUZn pin of clock output/buzzer output |
| 0                               | Subsystem clock ( $f_{SUB}$ )                                                                       | Selecting the subsystem clock ( $f_{SUB}$ ) is enabled.                  |
| 1                               | Low-speed on-chip oscillator clock ( $f_{IL}$ )                                                     | Selecting the subsystem clock ( $f_{SUB}$ ) is disabled.                 |

**Note** Be sure to select the subsystem clock (WUTMMCK0 bit = 0) if the subsystem clock is oscillating.

- Cautions**
1. The count of year, month, week, day, hour, minutes and second can only be performed when a subsystem clock ( $f_{SUB} = 32.768$  kHz) is selected as the operation clock of the real-time clock. When the low-speed on-chip oscillator clock ( $f_{IL} = 15$  kHz) is selected, only the constant-period interrupt function is available. The 32-pin products have the constant-period interrupt function only, because these products have no subsystem clock. However, the constant-period interrupt interval when  $f_{IL}$  is selected will be calculated with the constant-period (the value selected with RTCC0 register)  $\times f_{SUB}/f_{IL}$ .
  2. The subsystem clock and low-speed on-chip oscillator clock can only be switched by using the WUTMMCK0 bit if the real-time clock, 12-bit interval timer, and LCD driver/controller are all stopped.

These are stopped as follows:

Real-time clock: Set the RTCE bit to 0.

12-bit interval timer: Set the RINTE bit to 0.

LCD driver/controller: Set the SCOC and VLCON bits to 0.

**Remark**

RTCE: Bit 7 of real-time clock control register 0 (RTCC0)

RINTE: Bit 15 of the interval timer control register (ITMC)

SCOC: Bit 6 of LCD mode register 1 (LCDM1)

VLCON: Bit 5 of LCD mode register 1 (LCDM1)

### 7.3.3 Real-time clock control register 0 (RTCC0)

The RTCC0 register is an 8-bit register that is used to start or stop the real-time clock operation, control the RTC1HZ pin, and set a 12- or 24-hour system and the constant-period interrupt function.

The RTCC0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 7-4. Format of Real-time Clock Control Register 0 (RTCC0)**

Address: FFF9DH After reset: 00H R/W

|        |      |   |        |   |      |     |     |     |
|--------|------|---|--------|---|------|-----|-----|-----|
| Symbol | <7>  | 6 | <5>    | 4 | 3    | 2   | 1   | 0   |
| RTCC0  | RTCE | 0 | RCLOE1 | 0 | AMPM | CT2 | CT1 | CT0 |

|      |                                   |
|------|-----------------------------------|
| RTCE | Real-time clock operation control |
| 0    | Stops counter operation.          |
| 1    | Starts counter operation.         |

|        |                                           |
|--------|-------------------------------------------|
| RCLOE1 | RTC1HZ pin output control                 |
| 0      | Disables output of the RTC1HZ pin (1 Hz). |
| 1      | Enables output of the RTC1HZ pin (1 Hz).  |

|                                                                                                                                                                                                                                                                                                                                                                           |                                               |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|
| AMPM                                                                                                                                                                                                                                                                                                                                                                      | Selection of 12-/24-hour system               |
| 0                                                                                                                                                                                                                                                                                                                                                                         | 12-hour system (a.m. and p.m. are displayed.) |
| 1                                                                                                                                                                                                                                                                                                                                                                         | 24-hour system                                |
| <ul style="list-style-type: none"> <li>Rewrite the AMPM bit value after setting the RWAIT bit (bit 0 of real-time clock control register 1 (RTCC1)) to 1. If the AMPM bit value is changed, the values of the hour count register (HOUR) change according to the specified time system.</li> <li>Table 7-2 shows the displayed time digits that are displayed.</li> </ul> |                                               |

|                                                                                                                                                                                                                                                                                                                                                            |     |     |                                                                                 |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|---------------------------------------------------------------------------------|
| CT2                                                                                                                                                                                                                                                                                                                                                        | CT1 | CT0 | Constant-period interrupt (INTRTC) selection                                    |
| 0                                                                                                                                                                                                                                                                                                                                                          | 0   | 0   | Does not use constant-period interrupt function.                                |
| 0                                                                                                                                                                                                                                                                                                                                                          | 0   | 1   | Once per 0.5 s (synchronized with second count up)                              |
| 0                                                                                                                                                                                                                                                                                                                                                          | 1   | 0   | Once per 1 s (same time as second count up)                                     |
| 0                                                                                                                                                                                                                                                                                                                                                          | 1   | 1   | Once per 1 m (second 00 of every minute)                                        |
| 1                                                                                                                                                                                                                                                                                                                                                          | 0   | 0   | Once per 1 hour (minute 00 and second 00 of every hour)                         |
| 1                                                                                                                                                                                                                                                                                                                                                          | 0   | 1   | Once per 1 day (hour 00, minute 00, and second 00 of every day)                 |
| 1                                                                                                                                                                                                                                                                                                                                                          | 1   | ×   | Once per 1 month (Day 1, hour 00 a.m., minute 00, and second 00 of every month) |
| When changing the values of the CT2 to CT0 bits while the counter operates (RTCE = 1), rewrite the values of the CT2 to CT0 bits after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, after rewriting the values of the CT2 to CT0 bits, enable interrupt servicing after clearing the RIFG and RTCIF flags. |     |     |                                                                                 |

**Caution** Do not change the value of the RTCLOE1 bit when RTCE = 1.

**Remark** ×: don't care

### 7.3.4 Real-time clock control register 1 (RTCC1)

The RTCC1 register is an 8-bit register that is used to control the alarm interrupt function and the wait time of the counter.

The RTCC1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 7-5. Format of Real-time Clock Control Register 1 (RTCC1) (1/2)**

Address: FFF9EH After reset: 00H R/W

| Symbol | <7>  | <6>   | 5 | <4>  | <3>  | 2 | <1>  | <0>   |
|--------|------|-------|---|------|------|---|------|-------|
| RTCC1  | WALE | WALIE | 0 | WAFG | RIFG | 0 | RWST | RWAIT |

| WALE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Alarm operation control     |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|
| 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Match operation is invalid. |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Match operation is valid.   |
| When setting a value to the WALE bit while the counter operates (RTCE = 1) and WALIE = 1, rewrite the WALE bit after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG and RTCIF flags after rewriting the WALE bit. When setting each alarm register (WALIE flag of real-time clock control register 1 (RTCC1), the alarm minute register (ALARMWM), the alarm hour register (ALARMWH), and the alarm week register (ALARMWW)), set match operation to be invalid ("0") for the WALE bit. |                             |

| WALIE | Control of alarm interrupt (INTRTC) function operation |
|-------|--------------------------------------------------------|
| 0     | Does not generate interrupt on matching of alarm.      |
| 1     | Generates interrupt on matching of alarm.              |

| WAFG                                                                                                                                                                                                                                                                      | Alarm detection status flag    |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|
| 0                                                                                                                                                                                                                                                                         | Alarm mismatch                 |
| 1                                                                                                                                                                                                                                                                         | Detection of matching of alarm |
| This is a status flag that indicates detection of matching with the alarm. It is valid only when WALE = 1 and is set to "1" one clock (32.768 kHz) after matching of the alarm is detected. This flag is cleared when "0" is written to it. Writing "1" to it is invalid. |                                |

**Figure 7-5. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)**

|                                                                                                                                                                                                                                               |                                             |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|
| RIFG                                                                                                                                                                                                                                          | Constant-period interrupt status flag       |
| 0                                                                                                                                                                                                                                             | Constant-period interrupt is not generated. |
| 1                                                                                                                                                                                                                                             | Constant-period interrupt is generated.     |
| <p>This flag indicates the status of generation of the constant-period interrupt. When the constant-period interrupt is generated, it is set to "1".</p> <p>This flag is cleared when "0" is written to it. Writing "1" to it is invalid.</p> |                                             |

|                                                                                                                                                                                |                                     |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------|
| RWST                                                                                                                                                                           | Wait status flag of real-time clock |
| 0                                                                                                                                                                              | Counter is operating.               |
| 1                                                                                                                                                                              | Mode to read or write counter value |
| <p>This status flag indicates whether the setting of the RWAIT bit is valid.</p> <p>Before reading or writing the counter value, confirm that the value of this flag is 1.</p> |                                     |

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                                                                 |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------|
| RWAIT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Wait control of real-time clock                                 |
| 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Sets counter operation.                                         |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Stops SEC to YEAR counters. Mode to read or write counter value |
| <p>This bit controls the operation of the counter.</p> <p>Be sure to write "1" to it to read or write the counter value.</p> <p>As the counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0.</p> <p>When RWAIT = 1, it takes up to 1 clock (<math>f_{RTC}</math>) until the counter value can be read or written (RWST = 1).</p> <p>When the counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.</p> <p>However, when it wrote a value to second count register, it will not keep the overflow event.</p> |                                                                 |

**Caution** If writing is performed to the RTCC1 register with a 1-bit manipulation instruction, the RIFG flag and WAFG flag may be cleared. Therefore, to perform writing to the RTCC1 register, be sure to use an 8-bit manipulation instruction. To prevent the RIFG flag and WAFG flag from being cleared during writing, disable writing by setting 1 to the corresponding bit. If the RIFG flag and WAFG flag are not used and the value may be changed, the RTCC1 register may be written by using a 1-bit manipulation instruction.

**Remark** Fixed-cycle interrupts and alarm match interrupts use the same interrupt source (INTRTC). When using these two types of interrupts at the same time, which interrupt occurred can be judged by checking the fixed-cycle interrupt status flag (RIFG) and the alarm detection status flag (WAFG) upon INTRTC occurrence.

### 7.3.5 Second count register (SEC)

The SEC register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of seconds. It counts up when the counter (16-bit) overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks ( $f_{RTC}$ ) later. Set a decimal value of 00 to 59 to this register in BCD code.

The SEC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 7-6. Format of Second Count Register (SEC)**

Address: FFF92H    After reset: 00H    R/W

| Symbol | 7 | 6     | 5     | 4     | 3    | 2    | 1    | 0    |
|--------|---|-------|-------|-------|------|------|------|------|
| SEC    | 0 | SEC40 | SEC20 | SEC10 | SEC8 | SEC4 | SEC2 | SEC1 |

**Caution** When it reads or writes from/to the register while the counter is in operation ( $RTCE = 1$ ), follow the procedures described in the section 7.4.3 Reading/writing real-time clock.

### 7.3.6 Minute count register (MIN)

The MIN register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of minutes. It counts up when the second counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks ( $f_{RTC}$ ) later. Even if the second count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 59 to this register in BCD code.

The MIN register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 7-7. Format of Minute Count Register (MIN)**

Address: FFF93H    After reset: 00H    R/W

| Symbol | 7 | 6     | 5     | 4     | 3    | 2    | 1    | 0    |
|--------|---|-------|-------|-------|------|------|------|------|
| MIN    | 0 | MIN40 | MIN20 | MIN10 | MIN8 | MIN4 | MIN2 | MIN1 |

**Caution** When it reads or writes from/to the register while the counter is in operation ( $RTCE = 1$ ), follow the procedures described in the section 7.4.3 Reading/writing real-time clock.

### 7.3.7 Hour count register (HOUR)

The HOUR register is an 8-bit register that takes a value of 00 to 23 or 01 to 12 and 21 to 32 (decimal) and indicates the count value of hours.

It counts up when the minute counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks ( $f_{RTC}$ ) later. Even if the minute count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Specify a decimal value of 00 to 23, 01 to 12, or 21 to 32 by using BCD code according to the time system specified using bit 3 (AMPM) of real-time clock control register 0 (RTCC0).

If the AMPM bit value is changed, the values of the HOUR register change according to the specified time system.

The HOUR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 12H.

However, the value of this register is 00H if the AMPM bit (bit 3 of the RTCC0 register) is set to 1 after reset.

**Figure 7-8. Format of Hour Count Register (HOUR)**

Address: FFF94H    After reset: 12H    R/W

| Symbol | 7 | 6 | 5      | 4      | 3     | 2     | 1     | 0     |
|--------|---|---|--------|--------|-------|-------|-------|-------|
| HOUR   | 0 | 0 | HOUR20 | HOUR10 | HOUR8 | HOUR4 | HOUR2 | HOUR1 |

- Cautions**
1. Bit 5 (HOUR20) of the HOUR register indicates AM(0)/PM(1) if AMPM = 0 (if the 12-hour system is selected).
  2. When it reads or writes from/to the register while the counter is in operation (RTCE = 1), follow the procedures described in the section 7.4.3 Reading/writing real-time clock.

Table 7-2 shows the relationship between the setting value of the AMPM bit, the hour count register (HOUR) value, and time.

**Table 7-2. Displayed Time Digits**

| 24-Hour Display (AMPM = 1) |               | 12-Hour Display (AMPM = 1) |               |
|----------------------------|---------------|----------------------------|---------------|
| Time                       | HOUR Register | Time                       | HOUR Register |
| 0                          | 00H           | 12 a.m.                    | 12H           |
| 1                          | 01H           | 1 a.m.                     | 01H           |
| 2                          | 02H           | 2 a.m.                     | 02H           |
| 3                          | 03H           | 3 a.m.                     | 03H           |
| 4                          | 04H           | 4 a.m.                     | 04H           |
| 5                          | 05H           | 5 a.m.                     | 05H           |
| 6                          | 06H           | 6 a.m.                     | 06H           |
| 7                          | 07H           | 7 a.m.                     | 07H           |
| 8                          | 08H           | 8 a.m.                     | 08H           |
| 9                          | 09H           | 9 a.m.                     | 09H           |
| 10                         | 10H           | 10 a.m.                    | 10H           |
| 11                         | 11H           | 11 a.m.                    | 11H           |
| 12                         | 12H           | 12 p.m.                    | 32H           |
| 13                         | 13H           | 1 p.m.                     | 21H           |
| 14                         | 14H           | 2 p.m.                     | 22H           |
| 15                         | 15H           | 3 p.m.                     | 23H           |
| 16                         | 16H           | 4 p.m.                     | 24H           |
| 17                         | 17H           | 5 p.m.                     | 25H           |
| 18                         | 18H           | 6 p.m.                     | 26H           |
| 19                         | 19H           | 7 p.m.                     | 27H           |
| 20                         | 20H           | 8 p.m.                     | 28H           |
| 21                         | 21H           | 9 p.m.                     | 29H           |
| 22                         | 22H           | 10 p.m.                    | 30H           |
| 23                         | 23H           | 11 p.m.                    | 31H           |

The HOUR register value is set to 12-hour display when the AMPM bit is “0” and to 24-hour display when the AMPM bit is “1”.

In 12-hour display, the fifth bit of the HOUR register displays 0 for AM and 1 for PM.



### 7.3.8 Day count register (DAY)

The DAY register is an 8-bit register that takes a value of 1 to 31 (decimal) and indicates the count value of days. It counts up when the hour counter overflows.

This counter counts as follows.

- 01 to 31 (January, March, May, July, August, October, December)
- 01 to 30 (April, June, September, November)
- 01 to 29 (February, leap year)
- 01 to 28 (February, normal year)

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks ( $f_{RTC}$ ) later. Even if the hour count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 31 to this register in BCD code.

The DAY register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 01H.

**Figure 7-9. Format of Day Count Register (DAY)**

Address: FFF96H    After reset: 01H    R/W

| Symbol | 7 | 6 | 5     | 4     | 3    | 2    | 1    | 0    |
|--------|---|---|-------|-------|------|------|------|------|
| DAY    | 0 | 0 | DAY20 | DAY10 | DAY8 | DAY4 | DAY2 | DAY1 |

**Caution** When it reads or writes from/to the register while the counter is in operation ( $RTCE = 1$ ), follow the procedures described in the section 7.4.3 Reading/writing real-time clock.

### 7.3.9 Week count register (WEEK)

The WEEK register is an 8-bit register that takes a value of 0 to 6 (decimal) and indicates the count value of weekdays. It counts up in synchronization with the day counter.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f<sub>RTC</sub>) later. Set a decimal value of 00 to 06 to this register in BCD code.

The WEEK register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 7-10. Format of Week Count Register (WEEK)**

Address: FFF95H    After reset: 00H    R/W

|        |   |   |   |   |   |       |       |       |
|--------|---|---|---|---|---|-------|-------|-------|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2     | 1     | 0     |
| WEEK   | 0 | 0 | 0 | 0 | 0 | WEEK4 | WEEK2 | WEEK1 |

**Cautions** 1. The value corresponding to the month count register (MONTH) or the day count register (DAY) is not stored in the week count register (WEEK) automatically. After reset release, set the week count register as follow.

| Day       | WEEK |
|-----------|------|
| Sunday    | 00H  |
| Monday    | 01H  |
| Tuesday   | 02H  |
| Wednesday | 03H  |
| Thursday  | 04H  |
| Friday    | 05H  |
| Saturday  | 06H  |

2. When it reads or writes from/to the register while the counter is in operation (RTCE = 1), follow the procedures described in the section 7.4.3 Reading/writing real-time clock.

### 7.3.10 Month count register (MONTH)

The MONTH register is an 8-bit register that takes a value of 1 to 12 (decimal) and indicates the count value of months. It counts up when the day counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f<sub>RTC</sub>) later. Even if the day count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 12 to this register in BCD code.

The MONTH register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 01H.

**Figure 7-11. Format of Month Count Register (MONTH)**

Address: FFF97H After reset: 01H R/W

| Symbol | 7 | 6 | 5 | 4       | 3      | 2      | 1      | 0      |
|--------|---|---|---|---------|--------|--------|--------|--------|
| MONTH  | 0 | 0 | 0 | MONTH10 | MONTH8 | MONTH4 | MONTH2 | MONTH1 |

**Caution** When it reads or writes from/to the register while the counter is in operation (RTCE = 1), follow the procedures described in the section 7.4.3 Reading/writing real-time clock.

### 7.3.11 Year count register (YEAR)

The YEAR register is an 8-bit register that takes a value of 0 to 99 (decimal) and indicates the count value of years. It counts up when the month count register (MONTH) overflows.

Values 00, 04, 08, ..., 92, and 96 indicate a leap year.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f<sub>RTC</sub>) later. Even if the MONTH register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 99 to this register in BCD code.

The YEAR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 7-12. Format of Year Count Register (YEAR)**

Address: FFF98H After reset: 00H R/W

| Symbol | 7      | 6      | 5      | 4      | 3     | 2     | 1     | 0     |
|--------|--------|--------|--------|--------|-------|-------|-------|-------|
| YEAR   | YEAR80 | YEAR40 | YEAR20 | YEAR10 | YEAR8 | YEAR4 | YEAR2 | YEAR1 |

**Caution** When it reads or writes from/to the register while the counter is in operation (RTCE = 1), follow the procedures described in the section 7.4.3 Reading/writing real-time clock.

### 7.3.12 Watch error correction register (SUBCUD)

This register is used to correct the watch with high accuracy when it is slow or fast by changing the value that overflows from the counter (16-bit) to the second count register (SEC) (reference value: 7FFFH).

The SUBCUD register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 7-13. Format of Watch Error Correction Register (SUBCUD)**

Address: FFF99H After reset: 00H R/W

| Symbol | 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|--------|-----|----|----|----|----|----|----|----|
| SUBCUD | DEV | F6 | F5 | F4 | F3 | F2 | F1 | F0 |

| DEV                                                                                                                                                                | Setting of watch error correction timing                                             |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| 0                                                                                                                                                                  | Corrects watch error when the second digits are at 00, 20, or 40 (every 20 seconds). |
| 1                                                                                                                                                                  | Corrects watch error only when the second digits are at 00 (every 60 seconds).       |
| Writing to the SUBCUD register at the following timing is prohibited.                                                                                              |                                                                                      |
| <ul style="list-style-type: none"> <li>When DEV = 0 is set: For a period of SEC = 00H, 20H, 40H</li> <li>When DEV = 1 is set: For a period of SEC = 00H</li> </ul> |                                                                                      |

| F6                                                                                                        | Setting of watch error correction value                      |
|-----------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|
| 0                                                                                                         | Increases by $\{(F5, F4, F3, F2, F1, F0) - 1\} \times 2$ .   |
| 1                                                                                                         | Decreases by $\{((F5, F4, F3, F2, F1, F0) + 1) \times 2\}$ . |
| When (F6, F5, F4, F3, F2, F1, F0) = (*, 0, 0, 0, 0, 0, *), the watch error is not corrected. * is 0 or 1. |                                                              |
| /F5 to /F0 are the inverted values of the corresponding bits (000011 when 111100).                        |                                                              |
| Range of correction value: (when F6 = 0) 2, 4, 6, 8, ..., 120, 122, 124                                   |                                                              |
| (when F6 = 1) -2, -4, -6, -8, ..., -120, -122, -124                                                       |                                                              |

The range of value that can be corrected by using the watch error correction register (SUBCUD) is shown below.

|                                     | DEV = 0 (correction every 20 seconds) | DEV = 1 (correction every 60 seconds) |
|-------------------------------------|---------------------------------------|---------------------------------------|
| Correctable range                   | -189.2 ppm to 189.2 ppm               | -63.1 ppm to 63.1 ppm                 |
| Maximum excludes quantization error | ± 1.53 ppm                            | ± 0.51 ppm                            |
| Minimum resolution                  | ± 3.05 ppm                            | ± 1.02 ppm                            |

**Remark** If a correctable range is • 63.1 ppm or lower and 63.1 ppm or higher, set 0 to DEV.

### 7.3.13 Alarm minute register (ALARMWM)

This register is used to set minutes of alarm.

The ALARMWM register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Caution** Set a decimal value of 00 to 59 to this register in BCD code. If a value outside the range is set, the alarm is not detected.

Figure 7-14. Format of Alarm Minute Register (ALARMWM)

Address: FFF9AH After reset: 00H R/W

| Symbol  | 7 | 6    | 5    | 4    | 3   | 2   | 1   | 0   |
|---------|---|------|------|------|-----|-----|-----|-----|
| ALARMWM | 0 | WM40 | WM20 | WM10 | WM8 | WM4 | WM2 | WM1 |

### 7.3.14 Alarm hour register (ALARMWH)

This register is used to set hours of alarm.

The ALARMWH register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 12H.

However, the value of this register is 00H if the AMPM bit (bit 3 of the RTCC0 register) is set to 1 after reset.

**Caution** Set a decimal value of 00 to 23, 01 to 12, or 21 to 32 to this register in BCD code. If a value outside the range is set, the alarm is not detected.

Figure 7-15. Format of Alarm Hour Register (ALARMWH)

Address: FFF9BH After reset: 12H R/W

| Symbol  | 7 | 6 | 5    | 4    | 3   | 2   | 1   | 0   |
|---------|---|---|------|------|-----|-----|-----|-----|
| ALARMWH | 0 | 0 | WH20 | WH10 | WH8 | WH4 | WH2 | WH1 |

**Caution** Bit 5 (WH20) of the ALARMWH register indicates AM(0)/PM(1) if AMPM = 0 (if the 12-hour system is selected).

### 7.3.15 Alarm week register (ALARMWW)

This register is used to set date of alarm.

The ALARMWW register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7-16. Format of Alarm Week Register (ALARMWW)

Address: FFF9CH After reset: 00H R/W

| Symbol  | 7 | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|---------|---|-----|-----|-----|-----|-----|-----|-----|
| ALARMWW | 0 | WW6 | WW5 | WW4 | WW3 | WW2 | WW1 | WW0 |

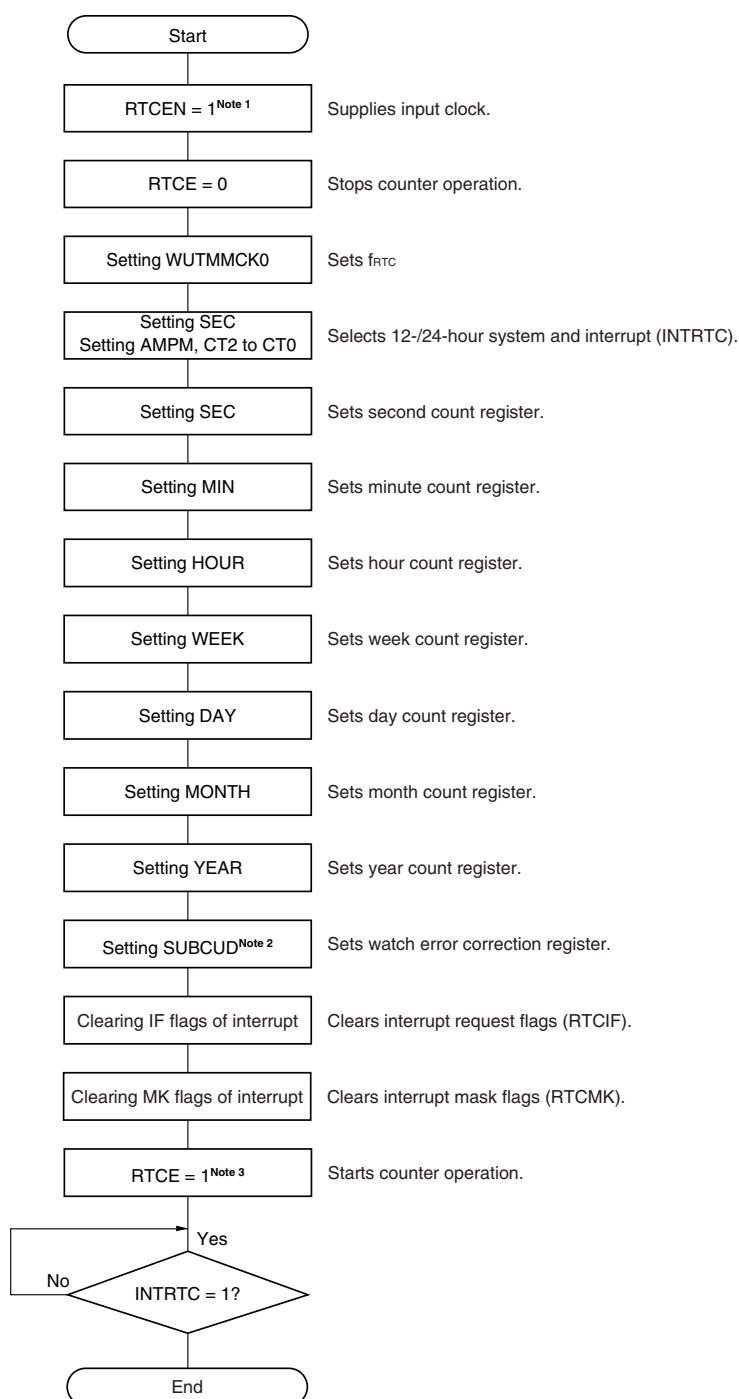
Here is an example of setting the alarm.

| Time of Alarm                            | Day         |             |             |             |             |             |             | 12-Hour Display |           |              |             | 24-Hour Display |           |              |             |
|------------------------------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----------------|-----------|--------------|-------------|-----------------|-----------|--------------|-------------|
|                                          | Sunday      | Monday      | Tuesday     | Wednesday   | Thursday    | Friday      | Saturday    | Hour<br>10      | Hour<br>1 | Minute<br>10 | Minute<br>1 | Hour<br>10      | Hour<br>1 | Minute<br>10 | Minute<br>1 |
|                                          | W<br>W<br>0 | W<br>W<br>1 | W<br>W<br>2 | W<br>W<br>3 | W<br>W<br>4 | W<br>W<br>5 | W<br>W<br>6 |                 |           |              |             |                 |           |              |             |
| Every day, 0:00 a.m.                     | 1           | 1           | 1           | 1           | 1           | 1           | 1           | 1               | 2         | 0            | 0           | 0               | 0         | 0            | 0           |
| Every day, 1:30 a.m.                     | 1           | 1           | 1           | 1           | 1           | 1           | 1           | 0               | 1         | 3            | 0           | 0               | 1         | 3            | 0           |
| Every day, 11:59 a.m.                    | 1           | 1           | 1           | 1           | 1           | 1           | 1           | 1               | 1         | 5            | 9           | 1               | 1         | 5            | 9           |
| Monday through<br>Friday, 0:00 p.m.      | 0           | 1           | 1           | 1           | 1           | 1           | 0           | 3               | 2         | 0            | 0           | 1               | 2         | 0            | 0           |
| Sunday, 1:30 p.m.                        | 1           | 0           | 0           | 0           | 0           | 0           | 0           | 2               | 1         | 3            | 0           | 1               | 3         | 3            | 0           |
| Monday, Wednesday,<br>Friday, 11:59 p.m. | 0           | 1           | 0           | 1           | 0           | 1           | 0           | 3               | 1         | 5            | 9           | 2               | 3         | 5            | 9           |

## 7.4 Real-time Clock Operation

### 7.4.1 Starting operation of real-time clock

**Figure 7-17. Procedure for Starting Operation of Real-time Clock**



- Notes**
1. First set the `RTCEN` bit to 1, while oscillation of the input clock (`fRTC`) is stable.
  2. Set up the `SUBCUD` register only if the watch error must be corrected. For details about how to calculate the correction value, see **7.4.6 Example of watch error correction of real-time clock**.
  3. Confirm the procedure described in **7.4.2 Shifting to HALT/STOP mode after starting operation** when shifting to HALT/STOP mode without waiting for `INTRTC = 1` after `RTCE = 1`.

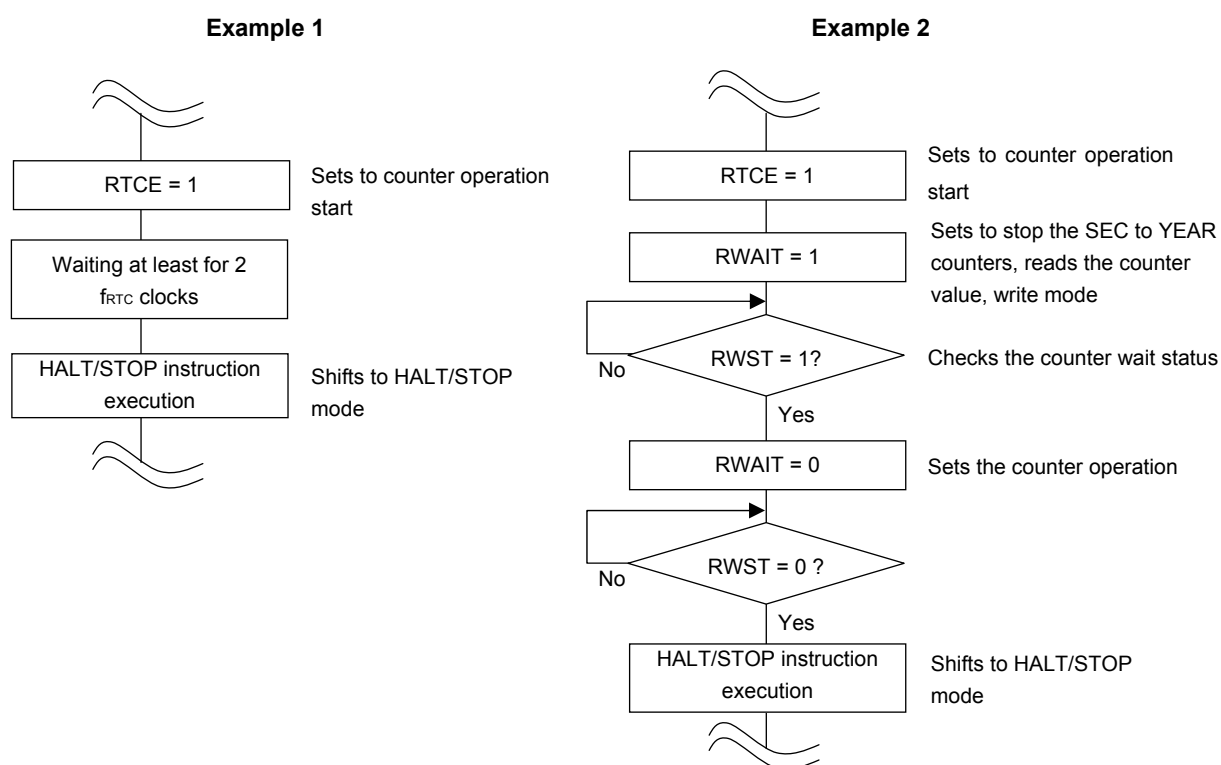
### <R> 7.4.2 Shifting to HALT/STOP mode after starting operation

Perform one of the following processing when shifting to HALT/STOP mode immediately after setting the RTCE bit to 1.

However, after setting the RTCE bit to 1, this processing is not required when shifting to HALT/STOP mode after the first INTRTC interrupt has occurred.

- Shifting to HALT/STOP mode when at least two input clocks ( $f_{RTC}$ ) have elapsed after setting the RTCE bit to 1 (see **Figure 7-18, Example 1**).
- Checking by polling the RWST bit to become 1, after setting the RTCE bit to 1 and then setting the RWAIT bit to 1. Afterward, setting the RWAIT bit to 0 and shifting to HALT/STOP mode after checking again by polling that the RWST bit has become 0 (see **Figure 7-18, Example 2**).

**Figure 7-18. Procedure for Shifting to HALT/STOP Mode After Setting RTCE bit to 1**



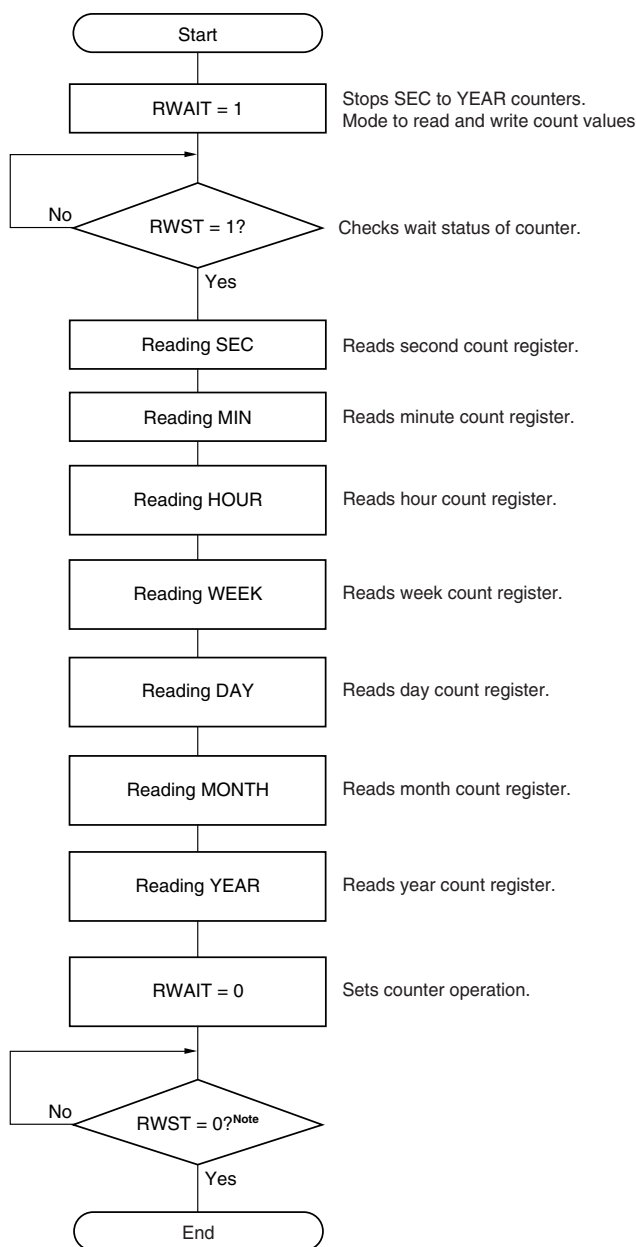


### 7.4.3 Reading/writing real-time clock

Read or write the counter after setting 1 to RWAIT first.

Set RWAIT to 0 after completion of reading or writing the counter.

**Figure 7-19. Procedure for Reading Real-time Clock**



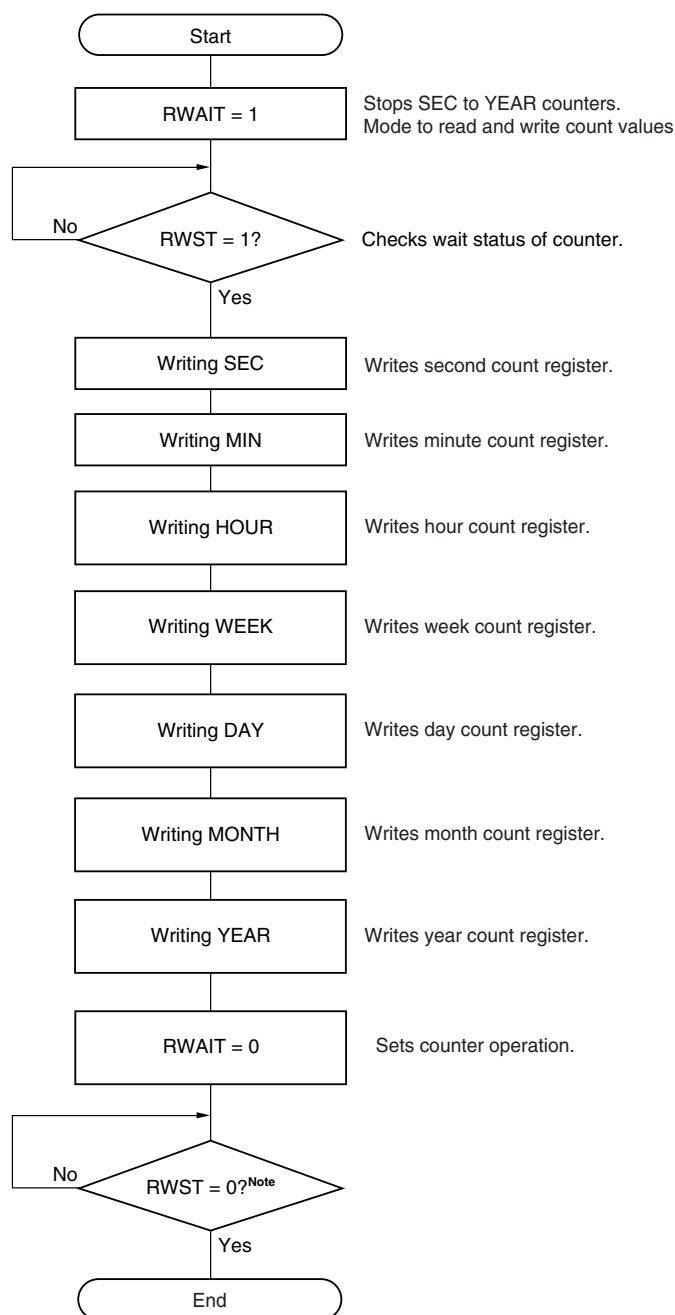
**Note** Be sure to confirm that RWST = 0 before setting STOP mode.

**Caution** Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.

**Remark** The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be read in any sequence.

All the registers do not have to read and only some registers may be read.

Figure 7-20. Procedure for Writing Real-time Clock



**Note** Be sure to confirm that RWST = 0 before setting STOP mode.

**Cautions** 1. Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.

2. When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counter operates (RTCE = 1), rewrite the values of the MIN register after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.

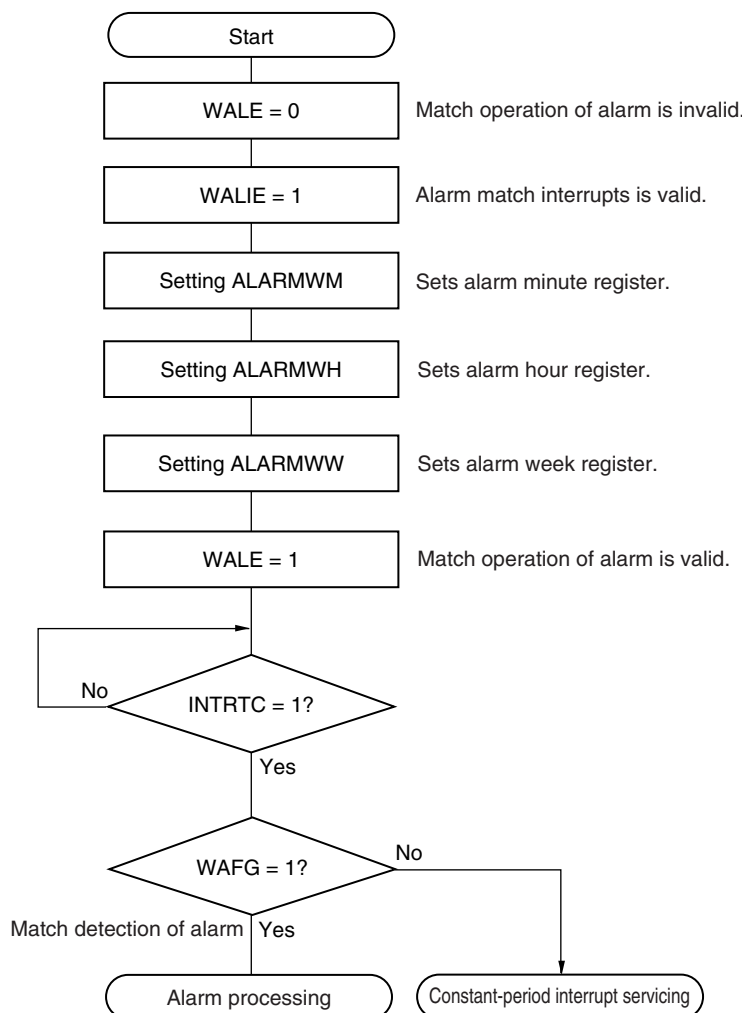
**Remark** The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be written in any sequence.

All the registers do not have to be set and only some registers may be written.

#### 7.4.4 Setting alarm of real-time clock

Set time of alarm after setting 0 to WALE (alarm operation invalid.) first.

**Figure 7-21. Alarm processing Procedure**

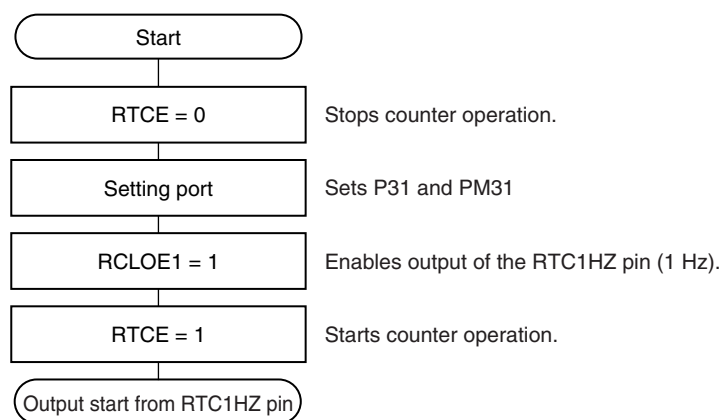


**Remarks 1.** The alarm week register (ALARMWW), alarm hour register (ALARMWH), and alarm week register (ALARMWW) may be written in any sequence.

- Fixed-cycle interrupts and alarm match interrupts use the same interrupt source (INTRTC). When using these two types of interrupts at the same time, which interrupt occurred can be judged by checking the fixed-cycle interrupt status flag (RIFG) and the alarm detection status flag (WAFG) upon INTRTC occurrence.

## 7.4.5 1 Hz output of real-time clock

Figure 7-22. 1 Hz Output Setting Procedure



**Caution** First set the RTCEN bit to 1, while oscillation of the input clock ( $f_{SUB}$ ) is stable.

#### 7.4.6 Example of watch error correction of real-time clock

The watch can be corrected with high accuracy when it is slow or fast, by setting a value to the watch error correction register.

##### Example of calculating the correction value

The correction value used when correcting the count value of the counter (16-bit) is calculated by using the following expression.

Set the DEV bit to 0 when the correction range is -63.1 ppm or less, or 63.1 ppm or more.

(When DEV = 0)

$$\text{Correction value}^{\text{Note}} = \text{Number of correction counts in 1 minute} \div 3 = (\text{Oscillation frequency} \div \text{Target frequency} - 1) \times 32768 \times 60 \div 3$$

(When DEV = 1)

$$\text{Correction value}^{\text{Note}} = \text{Number of correction counts in 1 minute} = (\text{Oscillation frequency} \div \text{Target frequency} - 1) \times 32768 \times 60$$

**Note** The correction value is the watch error correction value calculated by using bits 6 to 0 of the watch error correction register (SUBCUD).

(When F6 = 0) Correction value =  $\{(F5, F4, F3, F2, F1, F0) - 1\} \times 2$

(When F6 = 1) Correction value =  $-\{(/F5, /F4, /F3, /F2, /F1, /F0) + 1\} \times 2$

When (F6, F5, F4, F3, F2, F1, F0) is (\*, 0, 0, 0, 0, 0, \*), watch error correction is not performed. "\*" is 0 or 1. /F5 to /F0 are bit-inverted values (000011 when 111100).

- Remarks**
1. The correction value is 2, 4, 6, 8, ... 120, 122, 124 or -2, -4, -6, -8, ... -120, -122, -124.
  2. The oscillation frequency is the input clock (f<sub>RTC</sub>).  
It can be calculated from the output frequency of the RTC1HZ pin  $\times$  32768 when the watch error correction register is set to its initial value (00H).
  3. The target frequency is the frequency resulting after correction performed by using the watch error correction register.

**Correction example**

Example of correcting from 32767.4 Hz to 32768 Hz (32767.4 Hz + 18.3 ppm)

[Measuring the oscillation frequency]

The oscillation frequency<sup>Note</sup> of each product is measured by outputting about 1 Hz from the RTC1HZ pin when the watch error correction register (SUBCUD) is set to its initial value (00H).

**Note** See 7.4.5 1 Hz output of real-time clock for the setting procedure of outputting about 1 Hz from the RTC1HZ pin.

[Calculating the correction value]

(When the output frequency from the RTCCL pin is 0.9999817 Hz)

Oscillation frequency =  $32768 \times 0.9999817 \approx 32767.4$  Hz

Assume the target frequency to be 32768 Hz (32767.4 Hz + 18.3 ppm) and DEV to be 1.

The expression for calculating the correction value when DEV is 1 is applied.

$$\begin{aligned} \text{Correction value} &= \text{Number of correction counts in 1 minute} \\ &= (\text{Oscillation frequency} \div \text{Target frequency} - 1) \times 32768 \times 60 \\ &= (32767.4 \div 32768 - 1) \times 32768 \times 60 \\ &= -36 \end{aligned}$$

[Calculating the values to be set to (F6 to F0)]

(When the correction value is -36)

If the correction value is 0 or less (when quickening), assume F6 to be 1.

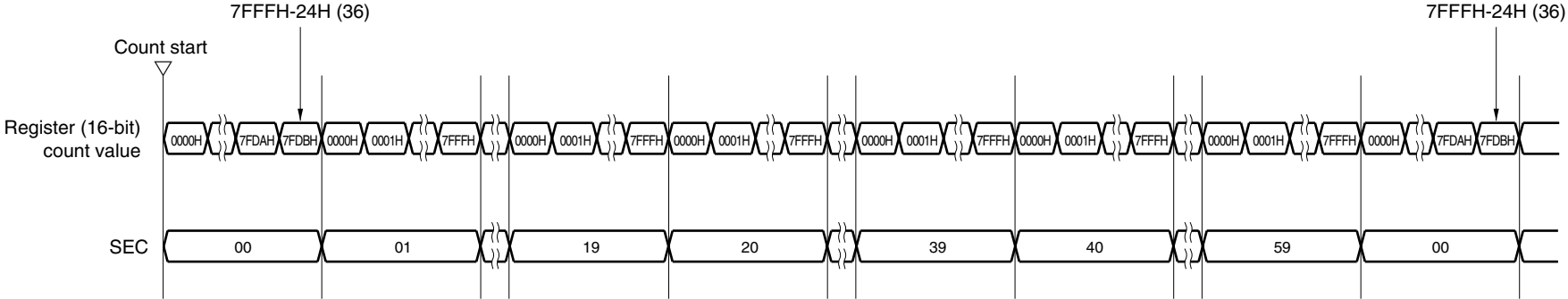
Calculate (F5, F4, F3, F2, F1, F0) from the correction value.

$$\begin{aligned} -\{(\text{F5}, \text{F4}, \text{F3}, \text{F2}, \text{F1}, \text{F0}) - 1\} \times 2 &= -36 \\ (\text{F5}, \text{F4}, \text{F3}, \text{F2}, \text{F1}, \text{F0}) &= 17 \\ (\text{F5}, \text{F4}, \text{F3}, \text{F2}, \text{F1}, \text{F0}) &= (0, 1, 0, 0, 0, 1) \\ (\text{F5}, \text{F4}, \text{F3}, \text{F2}, \text{F1}, \text{F0}) &= (1, 0, 1, 1, 1, 0) \end{aligned}$$

Consequently, when correcting from 32767.4 Hz to 32768 Hz (32767.4 Hz + 18.3 ppm), setting the correction register such that DEV is 1 and the correction value is -36 (bits 6 to 0 of the SUBCUD register: 1101110) results in 32768 Hz (0 ppm).

Figure 7-23 shows the operation when (DEV, F6, F5, F4, F3, F2, F1, F0) is (1, 1, 1, 0, 1, 1, 1, 0).

Figure 7-23. Correcting Operation when (DEV, F6, F5, F4, F3, F2, F1, F0) = (1, 1, 1, 0, 1, 1, 1, 0)



<R>

## CHAPTER 8 12-BIT INTERVAL TIMER

### 8.1 Functions of 12-bit Interval Timer

An interrupt (INTIT) is generated at any previously specified time interval. It can be utilized for wakeup from STOP mode and triggering an A/D converter's SNOOZE mode.

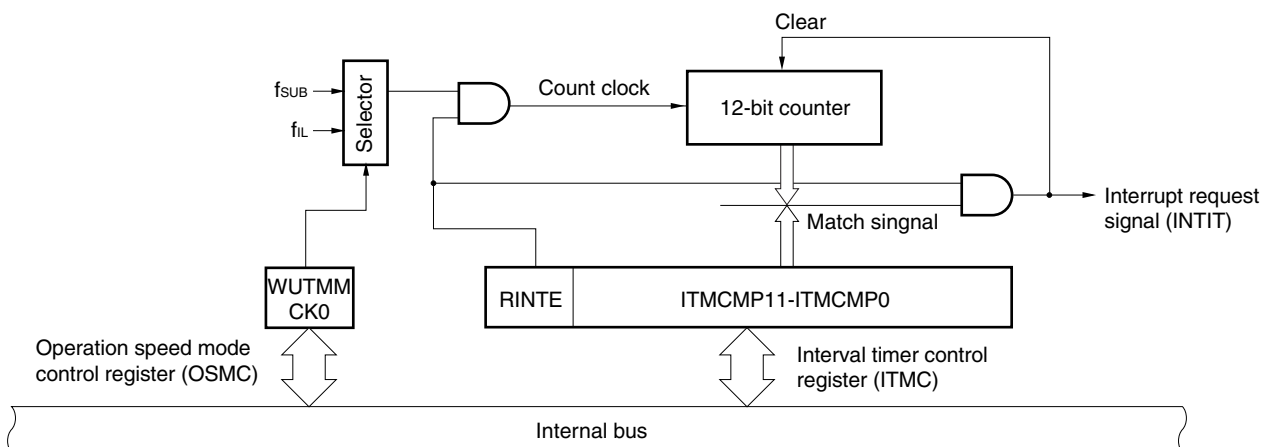
### 8.2 Configuration of 12-bit Interval Timer

The 12-bit interval timer includes the following hardware.

**Table 8-1. Configuration of 12-bit Interval Timer**

| Item              | Configuration                                |
|-------------------|----------------------------------------------|
| Counter           | 12-bit counter                               |
| Control registers | Peripheral enable register 0 (PER0)          |
|                   | Operation speed mode control register (OSMC) |
|                   | Interval timer control register (ITMC)       |

**Figure 8-1. Block Diagram of 12-bit Interval Timer**





### 8.3 Registers Controlling 12-bit Interval Timer

The 12-bit interval timer is controlled by the following registers.

- Peripheral enable register 0 (PER0)
- Operation speed mode control register (OSMC)
- Interval timer control register (ITMC)

### 8.3.1 Peripheral enable register 0 (PER0)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When the 12-bit interval timer is used, be sure to set bit 7 (RTCEN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 8-2. Format of Peripheral Enable Register 0 (PER0)**

Address: F00F0H After reset: 00H R/W

| Symbol | <7>   | 6 | <5>   | <4>     | 3 | <2>    | 1 | <0>    |
|--------|-------|---|-------|---------|---|--------|---|--------|
| PER0   | RTCEN | 0 | ADCEN | IICA0EN | 0 | SAU0EN | 0 | TAU0EN |

| RTCEN | Control of clock supply to real-time clock (RTC) and 12-bit interval timer                                                                                                                          | LCD driver/controller and clock output/buzzer output controller                                                                                    |                                                                                                                                                      |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |                                                                                                                                                                                                     | When subsystem clock ( $f_{SUB}$ ) is selected                                                                                                     | When subsystem clock ( $f_{SUB}$ ) is not selected                                                                                                   |
| 0     | Stops input clock supply.<br>• SFR used by the real-time clock (RTC) and 12-bit interval timer cannot be written.<br>• The real-time clock (RTC) and 12-bit interval timer are in the reset status. | Stops input clock and subsystem clock supply.<br>• SFR used by the LCD driver/controller and clock output/buzzer output can be read and written.   | Enables input clock and main system clock supply.<br>• SFR used by the LCD driver/controller and clock output/buzzer output can be read and written. |
| 1     | Enables input clock supply.<br>• SFR used by the real-time clock (RTC) and 12-bit interval timer can be read and written.                                                                           | Enables input clock and subsystem clock supply.<br>• SFR used by the LCD driver/controller and clock output/buzzer output can be read and written. |                                                                                                                                                      |

- Cautions**
1. When using the 12-bit interval timer, first set the RTCEN bit to 1, while oscillation of the input clock ( $f_{RTC}$ ) is stable. If RTCEN = 0, writing to a control register of the real-time clock, 12-bit interval timer, or LCD driver/controller is ignored, and, even if the register is read, only the default value is read.
  2. Clock supply to peripheral functions other than the real-time clock, 12-bit interval timer, and LCD driver/controller can be stopped in HALT mode when the subsystem clock is used, by setting the RTCLPC bit of the operation speed mode control register (OSMC) to 1. In this case, set the RTCEN bit of the PER0 register to 1 and the other bits (bits 0 to 6) to 0.
  3. Be sure to clear the bits 1, 3 and 6 to 0.

### 8.3.2 Operation speed mode control register (OSMC)

The WUTMMCK0 bit can be used to select the 12-bit interval timer operation clock.

In addition, by stopping clock functions that are unnecessary, the RTCLPC bit can be used to reduce power consumption. For details about setting the RTCLPC bit, see **CHAPTER 5 CLOCK GENERATOR**.

The OSMC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 8-3. Format of Operation Speed Mode Control Register (OSMC)**

Address: F00F3H After reset: 00H R/W

|        |        |   |   |          |   |   |   |   |
|--------|--------|---|---|----------|---|---|---|---|
| Symbol | 7      | 6 | 5 | 4        | 3 | 2 | 1 | 0 |
| OSMC   | RTCLPC | 0 | 0 | WUTMMCK0 | 0 | 0 | 0 | 0 |

|                                 |                                                                                                     |                                                                          |
|---------------------------------|-----------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|
| WUTMMCK0<br><small>Note</small> | Selection of operation clock for real-time clock, 12-bit interval timer, and LCD driver/controller. | Selection of clock output from PCLBUZn pin of clock output/buzzer output |
| 0                               | Subsystem clock ( $f_{SUB}$ )                                                                       | Selecting the subsystem clock ( $f_{SUB}$ ) is enabled.                  |
| 1                               | Low-speed on-chip oscillator clock ( $f_{IL}$ )                                                     | Selecting the subsystem clock ( $f_{SUB}$ ) is disabled.                 |

**Note** Be sure to select the subsystem clock (WUTMMCK0 bit = 0) if the subsystem clock is oscillating.

**Caution** The subsystem clock and low-speed on-chip oscillator clock can only be switched by using the WUTMMCK0 bit if the real-time clock, 12-bit interval timer, and LCD driver/controller are all stopped.

These are stopped as follows:

Real-time clock: Set the RTCE bit to 0.

Interval timer: Set the RINTE bit to 0.

LCD driver/controller: Set the SCOC and VLCON bits to 0.

**Remark** RTCE: Bit 7 of real-time clock control register 0 (RTCC0)  
 RINTE: Bit 15 of the interval timer control register (ITMC)  
 SCOC: Bit 6 of LCD mode register 1 (LCDM1)  
 VLCON: Bit 5 of LCD mode register 1 (LCDM1)

### 8.3.3 Interval timer control register (ITMC)

This register is used to set up the starting and stopping of the 12-bit interval timer operation and to specify the timer compare value.

The ITMC register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0FFFH.

**Figure 8-4. Format of Interval Timer Control Register (ITMC)**

Address: FFF90H    After reset: 0FFFH    R/W

| Symbol | 15    | 14 | 13 | 12 | 11 to 0           |
|--------|-------|----|----|----|-------------------|
| ITMC   | RINTE | 0  | 0  | 0  | ITCMP11 to ITCMP0 |

|       |                                         |
|-------|-----------------------------------------|
| RINTE | 12-bit interval timer operation control |
| 0     | Count operation stopped (count clear)   |
| 1     | Count operation started                 |

|                   |                                                                                                 |
|-------------------|-------------------------------------------------------------------------------------------------|
| ITCMP11 to ITCMP0 | Specification of the 12-bit interval timer compare value                                        |
| 001H              | These bits generate an interrupt at the fixed cycle (count clock cycles x (ITCMP setting + 1)). |
| •                 |                                                                                                 |
| •                 |                                                                                                 |
| •                 |                                                                                                 |
| FFFH              | Setting prohibit                                                                                |
| 000H              |                                                                                                 |

Example interrupt cycles when 001H or FFFH is specified for ITCMP11 to ITCMP0

- ITCMP11 to ITCMP0 = 001H, count clock: when  $f_{SUB} = 32.768 \text{ kHz}$   
 $1/32.768 \text{ [kHz]} \times (1 + 1) = 0.06103515625 \text{ [ms]} \cong 61.03 \text{ [}\mu\text{s]}$
- ITCMP11 to ITCMP0 = FFFH, count clock: when  $f_{SUB} = 32.768 \text{ kHz}$   
 $1/32.768 \text{ [kHz]} \times (4095 + 1) = 125 \text{ [ms]}$

- Cautions**
- Before changing the RINTE bit from 1 to 0, use the interrupt mask flag register to disable the INTIT interrupt servicing. When the operation starts (from 0 to 1) again, clear the ITIF flag, and then enable the interrupt servicing.
  - The value read from the RINTE bit is applied one count clock cycle after setting the RINTE bit.
  - When setting the RINTE bit to start operation of the counter after returning from a standby mode and then shifting to a standby mode again, either confirm that the value written to the RINTE bit has been applied, or make sure that at least one count clock cycle elapses between returning from a standby mode and shifting to a standby mode again.
  - Only change the setting of the ITCMP11 to ITCMP0 bits when RINTE = 0.  
However, it is possible to change the settings of the ITCMP11 to ITCMP0 bits at the same time as when changing RINTE from 0 to 1 or 1 to 0.

## 8.4 12-bit Interval Timer Operation

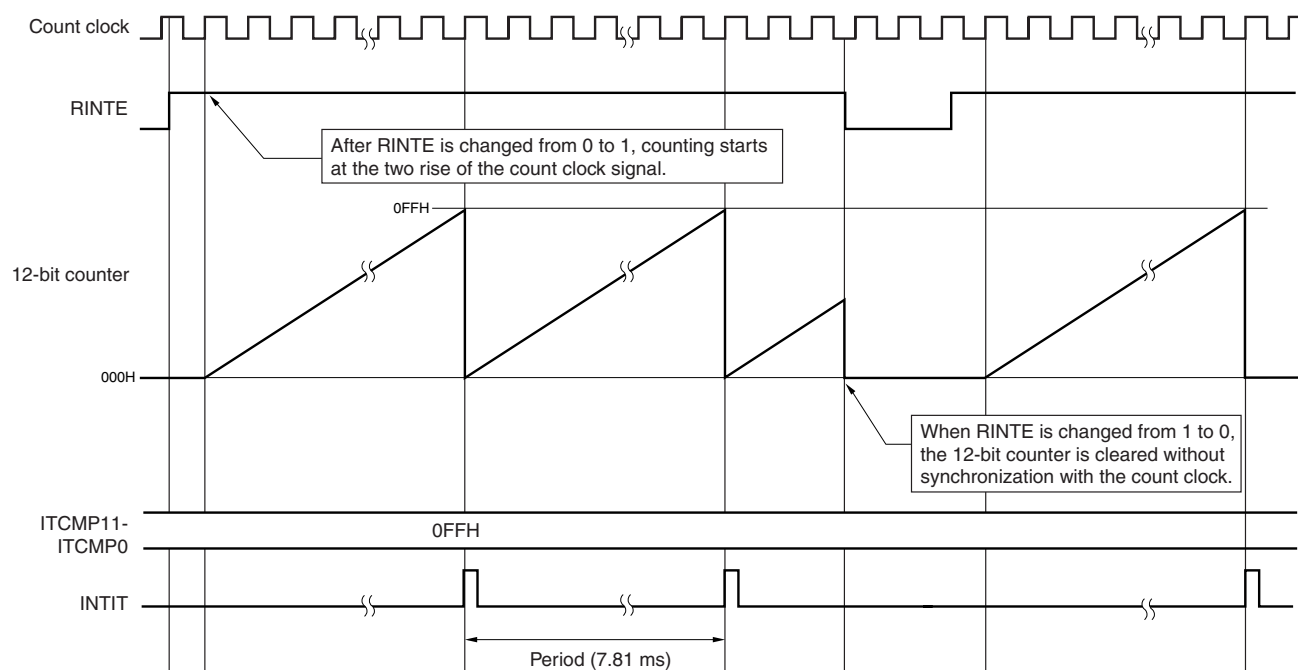
The count value specified for the ITCMP11 to ITCMP0 bits is used as an interval to operate an 12-bit interval timer that repeatedly generates interrupt requests (INTIT).

When the RINTE bit is set to 1, the 12-bit counter starts counting.

When the 12-bit counter value matches the value specified for the ITCMP11 to ITCMP0 bits, the 12-bit counter value is cleared to 0, counting continues, and an interrupt request signal (INTIT) is generated at the same time.

The basic operation of the 12-bit interval timer is as follows.

<R> **Figure 8-5. 12-bit Interval Timer Operation Timing (ITCMP11 to ITCMP0 = 0FFH, count clock:  $f_{SUB} = 32.768$  kHz)**



## CHAPTER 9 CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER

The number of output pins of the clock output and buzzer output controllers differs, depending on the product.

| Output pin | 32-pin | 44, 48, 52, 64-pin |
|------------|--------|--------------------|
| PCLBUZ0    | √      | √                  |
| PCLBUZ1    | —      | √                  |

**Caution** Most of the following descriptions in this chapter use the 64-pin as an example.

### 9.1 Functions of Clock Output/Buzzer Output Controller

The clock output controller is intended for carrier output during remote controlled transmission and clock output for supply to peripheral ICs.

Buzzer output is a function to output a square wave of buzzer frequency.

One pin can be used to output a clock or buzzer sound.

Two output pins, PCLBUZ0 and PCLBUZ1, are available.

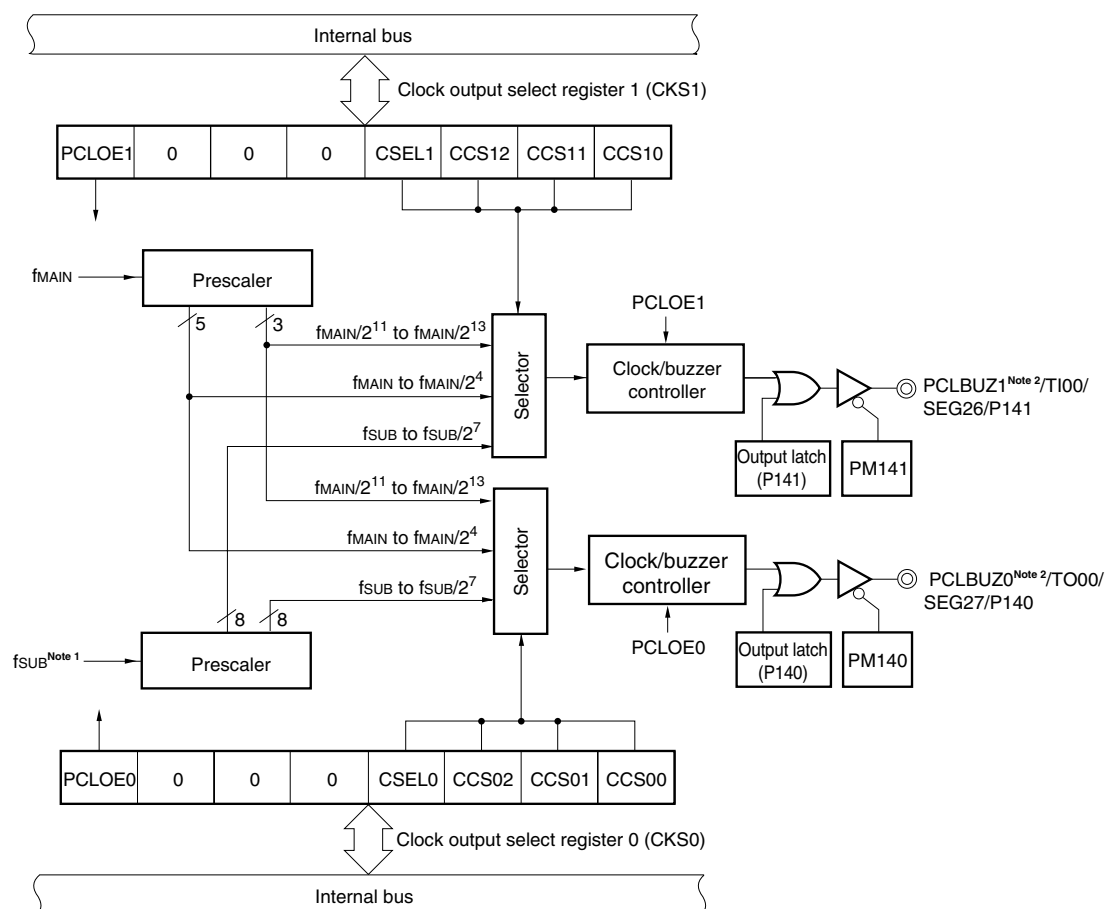
The PCLBUZn pin outputs a clock selected by clock output select register n (CKSn).

Figure 9-1 shows the block diagram of clock output/buzzer output controller.

**Caution** In the low-consumption RTC mode (when the RTCLPC bit of the operation speed mode control register (OSMC) = 1), it is not possible to output the subsystem clock ( $f_{SUB}$ ) from the PCLBUZn pin.

**Remark** n = 0, 1

Figure 9-1. Block Diagram of Clock Output/Buzzer Output Controller



- Notes**
1. Do not select  $f_{SUB}$  as the clock output from the clock output/buzzer output controller when the WUTMMCK0 bit of the OSMC register is set to 1.
  2. For output frequencies available from PCLBUZ0 and PCLBUZ1, refer **30.4 AC Characteristics**.

**Remark** PCLBUZ0 pin in above diagram shows the information of 48- to 64-pins products with PIOR1 = 0. In other cases, the name of pins, output latches (Pxx) and PMxx should be read differently (xx = 50).

## 9.2 Configuration of Clock Output/Buzzer Output Controller

The clock output/buzzer output controller includes the following hardware.

**Table 9-1. Configuration of Clock Output/Buzzer Output Controller**

| Item              | Configuration                                                                                                                                            |
|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| Control registers | Peripheral enable register 0 (PER0)<br>Clock output select registers n (CKSn)<br>Port mode registers 5, 14 (PM5, PM14)<br>Port registers 5, 14 (P5, P14) |

## 9.3 Registers Controlling Clock Output/Buzzer Output Controller

The following three registers are used to control the clock output/buzzer output controller.

- Peripheral enable register 0 (PER0)
- Clock output select registers n (CKSn)
- Port mode registers 5, 14 (PM5, PM14)



### 9.3.1 Peripheral enable register 0 (PER0)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When the clock output/buzzer output controller is used in subsystem clock ( $f_{SUB}$ ), be sure to set bit 7 (RTCEN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 9-2. Format of Peripheral Enable Register 0 (PER0)**

Address: F00F0H After reset: 00H R/W

| Symbol | <7>   | 6 | <5>   | <4>     | 3 | <2>    | 1 | <0>    |
|--------|-------|---|-------|---------|---|--------|---|--------|
| PER0   | RTCEN | 0 | ADCEN | IICA0EN | 0 | SAU0EN | 0 | TAU0EN |

| RTCEN | Real-time clock (RTC) and 12-bit interval timer                                                                                                                                                                                                         | LCD driver/controller and clock output/buzzer output controller                                                                                                                                    |                                                                                                                                                                                                      |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |                                                                                                                                                                                                                                                         | When subsystem clock ( $f_{SUB}$ ) is selected                                                                                                                                                     | When subsystem clock ( $f_{SUB}$ ) is not selected                                                                                                                                                   |
| 0     | Stops input clock supply.<br><ul style="list-style-type: none"> <li>SFR used by the real-time clock (RTC) and 12-bit interval timer cannot be written.</li> <li>The real-time clock (RTC) and 12-bit interval timer are in the reset status.</li> </ul> | Stops input clock and subsystem clock supply.<br><ul style="list-style-type: none"> <li>SFR used by the LCD driver/controller and clock output/buzzer output can be read and written.</li> </ul>   | Enables input clock and main system clock supply.<br><ul style="list-style-type: none"> <li>SFR used by the LCD driver/controller and clock output/buzzer output can be read and written.</li> </ul> |
| 1     | Enables input clock supply.<br><ul style="list-style-type: none"> <li>SFR used by the real-time clock (RTC) and 12-bit interval timer can be read and written.</li> </ul>                                                                               | Enables input clock and subsystem clock supply.<br><ul style="list-style-type: none"> <li>SFR used by the LCD driver/controller and clock output/buzzer output can be read and written.</li> </ul> |                                                                                                                                                                                                      |

**Caution** Be sure to clear the bits 1, 3 and 6 to 0.

### 9.3.2 Clock output select registers n (CKSn)

These registers set output enable/disable for clock output or for the buzzer frequency output pin (PCLBUZn), and set the output clock.

Select the clock to be output from the PCLBUZn pin by using the CKSn register.

The CKSn register are set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

**Figure 9-3. Format of Clock Output Select Register n (CKSn)**

Address: FFFA5H (CKS0), FFFA6H (CKS1) After reset: 00H R/W

|        |        |   |   |   |       |       |       |       |
|--------|--------|---|---|---|-------|-------|-------|-------|
| Symbol | <7>    | 6 | 5 | 4 | 3     | 2     | 1     | 0     |
| CKSn   | PCLOEn | 0 | 0 | 0 | CSELn | CCSn2 | CCSn1 | CCSn0 |

|        |                                                 |
|--------|-------------------------------------------------|
| PCLOEn | PCLBUZn pin output enable/disable specification |
| 0      | Output disable (default)                        |
| 1      | Output enable                                   |

| CSELn | CCSn2 | CCSn1 | CCSn0 |                                         | PCLBUZn pin output clock selection |                               |                                      |                                      |
|-------|-------|-------|-------|-----------------------------------------|------------------------------------|-------------------------------|--------------------------------------|--------------------------------------|
|       |       |       |       |                                         | f <sub>MAIN</sub> =<br>5 MHz       | f <sub>MAIN</sub> =<br>10 MHz | f <sub>MAIN</sub> =<br>20 MHz        | f <sub>MAIN</sub> =<br>24 MHz        |
| 0     | 0     | 0     | 0     | f <sub>MAIN</sub>                       | 5 MHz                              | 10 MHz <sup>Note 1</sup>      | Setting prohibited <sup>Note 1</sup> | Setting prohibited <sup>Note 1</sup> |
| 0     | 0     | 0     | 1     | f <sub>MAIN</sub> /2                    | 2.5 MHz                            | 5 MHz                         | 10 MHz <sup>Note 1</sup>             | 12 MHz <sup>Note 1</sup>             |
| 0     | 0     | 1     | 0     | f <sub>MAIN</sub> /2 <sup>2</sup>       | 1.25 MHz                           | 2.5 MHz                       | 5 MHz                                | 6 MHz                                |
| 0     | 0     | 1     | 1     | f <sub>MAIN</sub> /2 <sup>3</sup>       | 625 kHz                            | 1.25 MHz                      | 2.5 MHz                              | 3 MHz                                |
| 0     | 1     | 0     | 0     | f <sub>MAIN</sub> /2 <sup>4</sup>       | 312.5 kHz                          | 625 kHz                       | 1.25 MHz                             | 1.5 MHz                              |
| 0     | 1     | 0     | 1     | f <sub>MAIN</sub> /2 <sup>11</sup>      | 2.44 kHz                           | 4.88 kHz                      | 9.76 kHz                             | 11.7 kHz                             |
| 0     | 1     | 1     | 0     | f <sub>MAIN</sub> /2 <sup>12</sup>      | 1.22 kHz                           | 2.44 kHz                      | 4.88 kHz                             | 5.86 kHz                             |
| 0     | 1     | 1     | 1     | f <sub>MAIN</sub> /2 <sup>13</sup>      | 610 Hz                             | 1.22 kHz                      | 2.44 kHz                             | 2.93 kHz                             |
| 1     | 0     | 0     | 0     | f <sub>SUB</sub> <sup>Note 2</sup>      | 32.768 kHz                         |                               |                                      |                                      |
| 1     | 0     | 0     | 1     | f <sub>SUB</sub> /2 <sup>Note 2</sup>   | 16.384 kHz                         |                               |                                      |                                      |
| 1     | 0     | 1     | 0     | f <sub>SUB</sub> /2 <sup>2 Note 2</sup> | 8.192 kHz                          |                               |                                      |                                      |
| 1     | 0     | 1     | 1     | f <sub>SUB</sub> /2 <sup>3 Note 2</sup> | 4.096 kHz                          |                               |                                      |                                      |
| 1     | 1     | 0     | 0     | f <sub>SUB</sub> /2 <sup>4 Note 2</sup> | 2.048 kHz                          |                               |                                      |                                      |
| 1     | 1     | 0     | 1     | f <sub>SUB</sub> /2 <sup>5 Note 2</sup> | 1.024 kHz                          |                               |                                      |                                      |
| 1     | 1     | 1     | 0     | f <sub>SUB</sub> /2 <sup>6 Note 2</sup> | 512 Hz                             |                               |                                      |                                      |
| 1     | 1     | 1     | 1     | f <sub>SUB</sub> /2 <sup>7 Note 2</sup> | 256 Hz                             |                               |                                      |                                      |

**Notes** 1. Use the output clock within a range of 16 MHz. Furthermore, when using the output clock at 2.7 V ≤ V<sub>DD</sub> < 4.0 V, can be use it within 8 MHz only. See **30.4 AC Characteristics** for details.

2. Do not select f<sub>SUB</sub> as the clock output from the clock output/buzzer output controller when the WUTMMCK0 bit of the OSMC register is set to 1.

**Cautions** 1. Change the output clock after disabling clock output (PCLOEn = 0).

2. To shift to STOP mode when the main system clock is selected (CSELn = 0), set PCLOEn = 0 before executing the STOP instruction. When the subsystem clock is selected (CSELn = 1), PCLOEn = 1 can be set because the clock can be output in STOP mode.

**Cautions** 3. In the low-consumption RTC mode (when the RTCLPC bit of the operation speed mode control register (OSMC) = 1), it is not possible to output the subsystem clock ( $f_{SUB}$ ) from the PCLBUZn pin.

**Remarks** 1.  $n = 0, 1$   
2.  $f_{MAIN}$ : Main system clock frequency  
 $f_{SUB}$ : Subsystem clock frequency

**<R> 9.3.3 Port mode registers 5, 14 (PM5, PM14)**

These registers set input/output of port 5, 14 in 1-bit units.

When using the P50/INTP5/SEG7/(PCLBUZ0), P140/PCLBUZ0/TO00/SEG27 and P141/PCLBUZ1/TI00/SEG26 pins for clock output and buzzer output, clear PM50, PM140 and PM141 bits and the output latches of P50, P140 and P141 to 0.

The PM5 and PM14 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

**Figure 9-4. Format of Port Mode Registers 5, 14 (PM5, PM14)**

Address: FFF25H After reset: FFH R/W

|        |   |   |   |      |      |      |      |      |
|--------|---|---|---|------|------|------|------|------|
| Symbol | 7 | 6 | 5 | 4    | 3    | 2    | 1    | 0    |
| PM5    | 1 | 1 | 1 | PM54 | PM53 | PM52 | PM51 | PM50 |

Address: FFF2EH After reset: FFH R/W

|        |       |       |       |       |       |       |       |       |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| Symbol | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
| PM14   | PM147 | PM146 | PM145 | PM144 | PM143 | PM142 | PM141 | PM140 |

| PMmn | Pmn pin I/O mode selection (mn = 50 to 54, 140 to 147) |
|------|--------------------------------------------------------|
| 0    | Output mode (output buffer on)                         |
| 1    | Input mode (output buffer off)                         |

## 9.4 Operations of Clock Output/Buzzer Output Controller

One pin can be used to output a clock or buzzer sound.

The PCLBUZ0 pin outputs a clock/buzzer selected by the clock output select register 0 (CKS0).

The PCLBUZ1 pin outputs a clock/buzzer selected by the clock output select register 1 (CKS1).

### 9.4.1 Operation as output pin

The PCLBUZn pin is output as the following procedure.

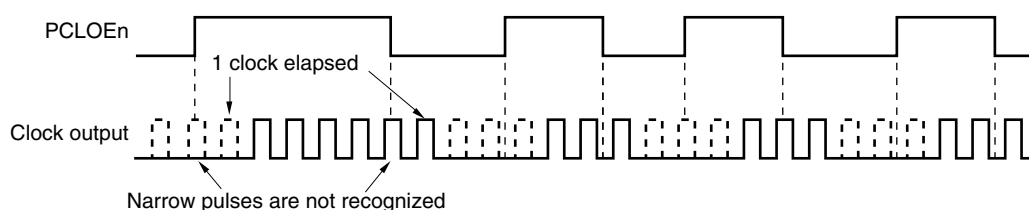
- <1> Select the output frequency with bits 0 to 3 (CCSn0 to CCSn2, CSELn) of the clock output select register (CKSn) of the PCLBUZn pin (output in disabled status).
- <2> Set bit 7 (PCLOEn) of the CKSn register to 1 to enable clock/buzzer output.

**Remarks 1.** The controller used for outputting the clock starts or stops outputting the clock one clock after enabling or disabling clock output (PCLOEn bit) is switched. At this time, pulses with a narrow width are not output.

Figure 9-5 shows enabling or stopping output using the PCLOEn bit and the timing of outputting the clock.

2.  $n = 0, 1$

**Figure 9-5. Remote Control Output Application Example**



## <R> 9.5 Cautions of clock output/buzzer output controller

When the main system clock is selected for the PCLBUZn output (CSELn = 0), if STOP or HALT mode is entered within 1.5 main system clock cycles after the output is disabled (PCLOEn = 0), the PCLBUZn output width becomes shorter.

## CHAPTER 10 WATCHDOG TIMER

### 10.1 Functions of Watchdog Timer

The watchdog timer operates on the low-speed on-chip oscillator clock.

The watchdog timer is used to detect an inadvertent program loop. If a program loop is detected, an internal reset signal is generated.

Program loop is detected in the following cases.

- If the watchdog timer counter overflows
- If a 1-bit manipulation instruction is executed on the watchdog timer enable register (WDTE)
- If data other than "ACH" is written to the WDTE register
- If data is written to the WDTE register during a window close period

When a reset occurs due to the watchdog timer, bit 4 (WDTRF) of the reset control flag register (RESF) is set to 1. For details of the RESF register, see **CHAPTER 20 RESET FUNCTION**.

<R> When  $75\% + 1/2t_{IL}$  of the overflow time is reached, an interval interrupt can be generated.

## 10.2 Configuration of Watchdog Timer

The watchdog timer includes the following hardware.

**Table 10-1. Configuration of Watchdog Timer**

| Item             | Configuration                         |
|------------------|---------------------------------------|
| Control register | Watchdog timer enable register (WDTE) |

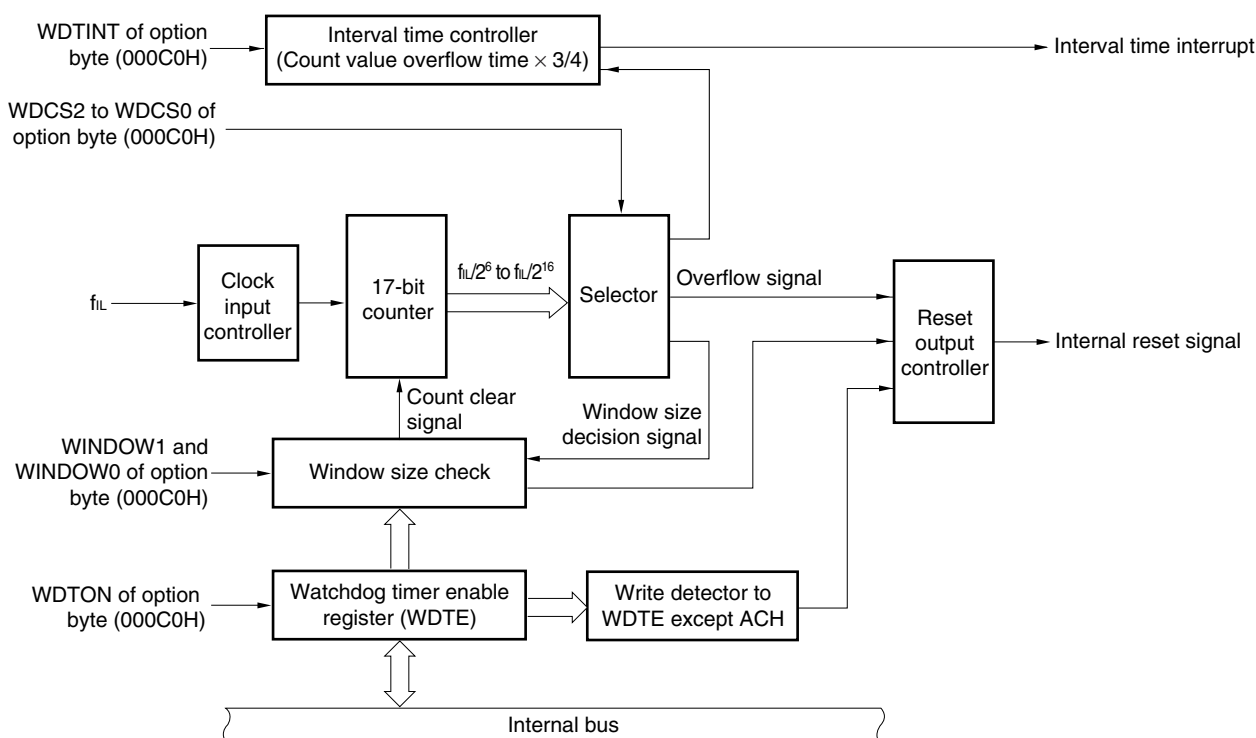
How the counter operation is controlled, overflow time, window open period, and interval interrupt are set by the option byte.

**Table 10-2. Setting of Option Bytes and Watchdog Timer**

| Setting of Watchdog Timer                                           | Option Byte (000C0H)            |
|---------------------------------------------------------------------|---------------------------------|
| Watchdog timer interval interrupt                                   | Bit 7 (WDTINT)                  |
| Window open period                                                  | Bits 6 and 5 (WINDOW1, WINDOW0) |
| Controlling counter operation of watchdog timer                     | Bit 4 (WDTON)                   |
| Overflow time of watchdog timer                                     | Bits 3 to 1 (WDCS2 to WDCS0)    |
| Controlling counter operation of watchdog timer (in HALT/STOP mode) | Bit 0 (WDSTBYON)                |

**Remark** For the option byte, see **CHAPTER 25 OPTION BYTE**.

**Figure 10-1. Block Diagram of Watchdog Timer**



### 10.3 Register Controlling Watchdog Timer

The watchdog timer is controlled by the watchdog timer enable register (WDTE).

#### (1) Watchdog timer enable register (WDTE)

Writing “ACH” to the WDTE register clears the watchdog timer counter and starts counting again.

This register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 9AH or 1AH<sup>Note</sup>.

**Figure 10-2. Format of Watchdog Timer Enable Register (WDTE)**

|                 |                                      |     |   |   |   |   |   |   |
|-----------------|--------------------------------------|-----|---|---|---|---|---|---|
| Address: FFFABH | After reset: 9AH/1AH <sup>Note</sup> | R/W |   |   |   |   |   |   |
| Symbol          | 7                                    | 6   | 5 | 4 | 3 | 2 | 1 | 0 |
| WDTE            |                                      |     |   |   |   |   |   |   |

**Note** The WDTE register reset value differs depending on the WDTON bit setting value of the option byte (000C0H). To operate watchdog timer, set the WDTON bit to 1.

| WDTON Bit Setting Value                     | WDTE Register Reset Value |
|---------------------------------------------|---------------------------|
| 0 (watchdog timer count operation disabled) | 1AH                       |
| 1 (watchdog timer count operation enabled)  | 9AH                       |

- Cautions**
1. If a value other than “ACH” is written to the WDTE register, an internal reset signal is generated.
  2. If a 1-bit memory manipulation instruction is executed for the WDTE register, an internal reset signal is generated.
  3. The value read from the WDTE register is 9AH/1AH (this differs from the written value (ACH)).



## 10.4 Operation of Watchdog Timer

### 10.4.1 Controlling operation of watchdog timer

1. When the watchdog timer is used, its operation is specified by the option byte (000C0H).
  - Enable counting operation of the watchdog timer by setting bit 4 (WDTON) of the option byte (000C0H) to 1 (the counter starts operating after a reset release) (for details, see **CHAPTER 25**).

| WDTON | Watchdog Timer Counter                                    |
|-------|-----------------------------------------------------------|
| 0     | Counter operation disabled (counting stopped after reset) |
| 1     | Counter operation enabled (counting started after reset)  |

- Set an overflow time by using bits 3 to 1 (WDCS2 to WDCS0) of the option byte (000C0H) (for details, see **10.4.2** and **CHAPTER 25**).
  - Set a window open period by using bits 6 and 5 (WINDOW1 and WINDOW0) of the option byte (000C0H) (for details, see **10.4.3** and **CHAPTER 25**).
2. After a reset release, the watchdog timer starts counting.
  3. By writing “ACH” to the watchdog timer enable register (WDTE) after the watchdog timer starts counting and before the overflow time set by the option byte, the watchdog timer is cleared and starts counting again.
  4. After that, write the WDTE register the second time or later after a reset release during the window open period. If the WDTE register is written during a window close period, an internal reset signal is generated.
  5. If the overflow time expires without “ACH” written to the WDTE register, an internal reset signal is generated. An internal reset signal is generated in the following cases.
    - If a 1-bit manipulation instruction is executed on the WDTE register
    - If data other than “ACH” is written to the WDTE register

- Cautions**
1. When data is written to the watchdog timer enable register (WDTE) for the first time after reset release, the watchdog timer is cleared in any timing regardless of the window open time, as long as the register is written before the overflow time, and the watchdog timer starts counting again.
  2. If the watchdog timer is cleared by writing “ACH” to the WDTE register, the actual overflow time may be different from the overflow time set by the option byte by up to 2/f<sub>IL</sub> seconds.
  3. The watchdog timer can be cleared immediately before the count value overflows.

**Cautions** 4. The operation of the watchdog timer in the HALT, STOP, and SNOOZE modes differs as follows depending on the set value of bit 0 (WDSTBYON) of the option byte (000C0H).

|                | WDSTBYON = 0                    | WDSTBYON = 1                        |
|----------------|---------------------------------|-------------------------------------|
| In HALT mode   | Watchdog timer operation stops. | Watchdog timer operation continues. |
| In STOP mode   |                                 |                                     |
| In SNOOZE mode |                                 |                                     |

If WDSTBYON = 0, the watchdog timer resumes counting after the HALT or STOP mode is released. At this time, the counter is cleared to 0 and counting starts.

When operating with the X1 oscillation clock after releasing the STOP mode, the CPU starts operating after the oscillation stabilization time has elapsed.

Therefore, if the period between the STOP mode release and the watchdog timer overflow is short, an overflow occurs during the oscillation stabilization time, causing a reset.

Consequently, set the overflow time in consideration of the oscillation stabilization time when operating with the X1 oscillation clock and when the watchdog timer is to be cleared after the STOP mode release by an interval interrupt.

#### 10.4.2 Setting overflow time of watchdog timer

Set the overflow time of the watchdog timer by using bits 3 to 1 (WDCS2 to WDCS0) of the option byte (000C0H).

If an overflow occurs, an internal reset signal is generated. The present count is cleared and the watchdog timer starts counting again by writing "ACH" to the watchdog timer enable register (WDTE) during the window open period before the overflow time.

The following overflow times can be set.

**Table 10-3. Setting of Overflow Time of Watchdog Timer**

| WDCS2 | WDCS1 | WDCS0 | Overflow Time of Watchdog Timer<br>(f <sub>IL</sub> = 17.25 kHz (MAX.)) |
|-------|-------|-------|-------------------------------------------------------------------------|
| 0     | 0     | 0     | 2 <sup>6</sup> /f <sub>IL</sub> (3.71 ms)                               |
| 0     | 0     | 1     | 2 <sup>7</sup> /f <sub>IL</sub> (7.42 ms)                               |
| 0     | 1     | 0     | 2 <sup>8</sup> /f <sub>IL</sub> (14.84 ms)                              |
| 0     | 1     | 1     | 2 <sup>9</sup> /f <sub>IL</sub> (29.68 ms)                              |
| 1     | 0     | 0     | 2 <sup>11</sup> /f <sub>IL</sub> (118.72 ms)                            |
| 1     | 0     | 1     | 2 <sup>13</sup> /f <sub>IL</sub> (474.90 ms)                            |
| 1     | 1     | 0     | 2 <sup>14</sup> /f <sub>IL</sub> (949.80 ms)                            |
| 1     | 1     | 1     | 2 <sup>16</sup> /f <sub>IL</sub> (3799.19 ms)                           |

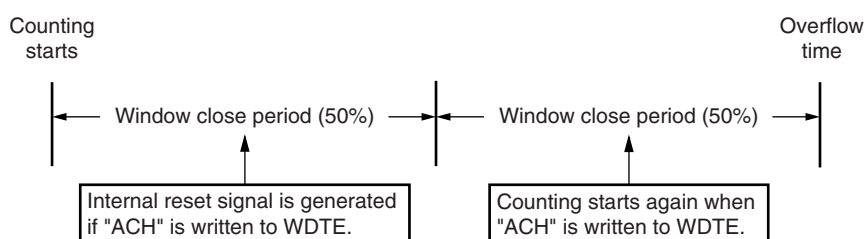
**Remark** f<sub>IL</sub>: Low-speed on-chip oscillator clock frequency

### 10.4.3 Setting window open period of watchdog timer

Set the window open period of the watchdog timer by using bits 6 and 5 (WINDOW1, WINDOW0) of the option byte (000C0H). The outline of the window is as follows.

- If "ACH" is written to the watchdog timer enable register (WDTE) during the window open period, the watchdog timer is cleared and starts counting again.
- Even if "ACH" is written to the WDTE register during the window close period, an abnormality is detected and an internal reset signal is generated.

**Example:** If the window open period is 50%



**Caution** When data is written to the WDTE register for the first time after reset release, the watchdog timer is cleared in any timing regardless of the window open time, as long as the register is written before the overflow time, and the watchdog timer starts counting again.

The window open period can be set as follows.

**Table 10-4. Setting Window Open Period of Watchdog Timer**

| WINDOW1 | WINDOW0 | Window Open Period of Watchdog Timer |
|---------|---------|--------------------------------------|
| 0       | 0       | Setting prohibited                   |
| 0       | 1       | 50%                                  |
| 1       | 0       | 75%                                  |
| 1       | 1       | 100%                                 |

**Caution** When bit 0 (WDSTBYON) of the option byte (000C0H) = 0, the window open period is 100% regardless of the values of the WINDOW1 and WINDOW0 bits.

**Remark** If the overflow time is set to  $2^9/f_{IL}$ , the window close time and open time are as follows.

|                   | Setting of Window Open Period |                   |               |
|-------------------|-------------------------------|-------------------|---------------|
|                   | 50%                           | 75%               | 100%          |
| Window close time | 0 to 20.08 ms                 | 0 to 10.04 ms     | None          |
| Window open time  | 20.08 to 29.68 ms             | 10.04 to 29.68 ms | 0 to 29.68 ms |

<When window open period is 50%>

- Overflow time:  
 $2^9/f_{IL} \text{ (MAX.)} = 2^9/17.25 \text{ kHz} = 29.68 \text{ ms}$
- Window close time:  
 $0 \text{ to } 2^9/f_{IL} \text{ (MIN.)} \times (1 - 0.5) = 0 \text{ to } 2^9/12.75 \text{ kHz} \times 0.5 = 0 \text{ to } 20.08 \text{ ms}$
- Window open time:  
 $2^9/f_{IL} \text{ (MIN.)} \times (1 - 0.5) \text{ to } 2^9/f_{IL} \text{ (MAX.)} = 2^9/12.75 \text{ kHz} \times 0.5 \text{ to } 2^9/17.25 \text{ kHz} = 20.08 \text{ to } 29.68 \text{ ms}$

#### 10.4.4 Setting watchdog timer interval interrupt

Depending on the setting of bit 7 (WDTINT) of an option byte (000C0H), an interval interrupt (INTWDTI) can be <R> generated when  $75\% + 1/2f_{IL}$  of the overflow time is reached.

**Table 10-5. Setting of Watchdog Timer Interval Interrupt**

| WDTINT | Use of Watchdog Timer Interval Interrupt                                             |
|--------|--------------------------------------------------------------------------------------|
| 0      | Interval interrupt is used.                                                          |
| 1      | Interval interrupt is generated when $75\% + 1/2f_{IL}$ of overflow time is reached. |

<R>

**Caution** When operating with the X1 oscillation clock after releasing the STOP mode, the CPU starts operating after the oscillation stabilization time has elapsed.

Therefore, if the period between the STOP mode release and the watchdog timer overflow is short, an overflow occurs during the oscillation stabilization time, causing a reset.

Consequently, set the overflow time in consideration of the oscillation stabilization time when operating with the X1 oscillation clock and when the watchdog timer is to be cleared after the STOP mode release by an interval interrupt.

**Remark** The watchdog timer continues counting even after INTWDTI is generated (until ACH is written to the watchdog timer enable register (WDTE)). If ACH is not written to the WDTE register before the overflow time, an internal reset signal is generated.

## CHAPTER 11 A/D CONVERTER

The number of analog input channels of the A/D converter differs, depending on the product.

|                       | 32-pin                             | 44-pin                               | 48-pin                               | 52, 64-pin                            |
|-----------------------|------------------------------------|--------------------------------------|--------------------------------------|---------------------------------------|
| Analog input channels | 4 ch<br>(ANI0, ANI1, ANI18, ANI19) | 7 ch<br>(ANI0, ANI1, ANI17 to ANI21) | 9 ch<br>(ANI0, ANI1, ANI16 to ANI22) | 10 ch<br>(ANI0, ANI1, ANI16 to ANI23) |

**Caution** Most of the following descriptions in this chapter use the 64-pin as an example.

### 11.1 Function of A/D Converter

The A/D converter is a 10-bit resolution<sup>Note</sup> converter that converts analog input signals into digital values, and is configured to control analog inputs, including up to 10 channels of A/D converter analog inputs (ANI0, ANI1 and ANI16 to ANI23).

The A/D converter has the following function.

- **10-bit resolution A/D conversion**<sup>Note</sup>

10-bit resolution A/D conversion is carried out repeatedly for one analog input channel selected from ANI0, ANI1 and ANI16 to ANI23. Each time an A/D conversion operation ends, an interrupt request (INTAD) is generated.

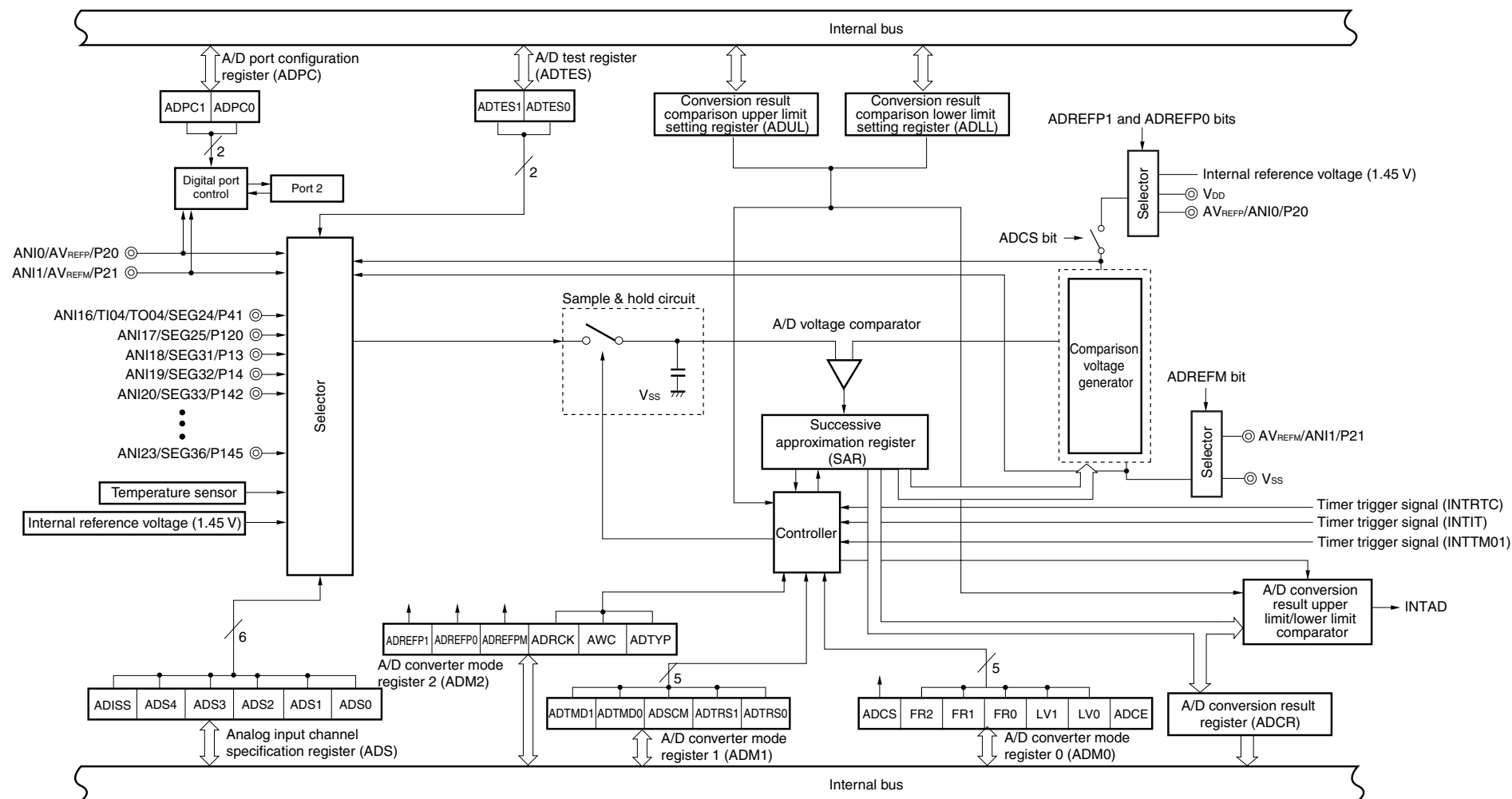
**Note** 8-bit resolution can also be selected by using the ADTYP bit of A/D converter mode register 2 (ADM2).

Various A/D conversion modes can be specified by using the mode combinations below.

| Trigger Mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Conversion Operation Mode                                                                                                                                                                                                                                                               |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <ul style="list-style-type: none"> <li>• Software trigger<br/>Conversion is started by specifying a software trigger.</li> <li>• Hardware trigger no-wait mode<br/>Conversion is started by detecting a hardware trigger.</li> <li>• Hardware trigger wait mode<br/>The power is turned on by detecting a hardware trigger while the system is off and in the conversion standby state, and conversion is then started automatically after the stabilization wait time passes.</li> </ul> | <ul style="list-style-type: none"> <li>• One-shot conversion mode<br/>A/D conversion is performed on the selected channel once.</li> <li>• Sequential conversion mode<br/>A/D conversion is sequentially performed on the selected channels until it is stopped by software.</li> </ul> |

$\langle R \rangle$

**Figure 11-1. Block Diagram of A/D Converter**



**Remark** Analog input pin for figure 11-1 when a 64-pin product is used.

## 11.2 Configuration of A/D Converter

The A/D converter includes the following hardware.

### (1) ANI0, ANI1 and ANI16 to ANI23 pins

These are the analog input pins of the 10 channels of the A/D converter. They input analog signals to be converted into digital signals. Pins other than the one selected as the analog input pin can be used as I/O port pins.

### (2) Sample & hold circuit

The sample & hold circuit samples each of the analog input voltages sequentially sent from the input circuit, and sends them to the A/D voltage comparator. This circuit also holds the sampled analog input voltage during A/D conversion.

### (3) A/D voltage comparator

This A/D voltage comparator compares the voltage generated from the voltage tap of the comparison voltage generator with the analog input voltage. If the analog input voltage is found to be greater than the reference voltage ( $1/2 AV_{REF}$ ) as a result of the comparison, the most significant bit (MSB) of the successive approximation register (SAR) is set. If the analog input voltage is less than the reference voltage ( $1/2 AV_{REF}$ ), the MSB bit of the SAR is reset.

After that, bit 8 of the SAR register is automatically set, and the next comparison is made. The voltage tap of the comparison voltage generator is selected by the value of bit 9, to which the result has been already set.

Bit 9 = 0: ( $1/4 AV_{REF}$ )

Bit 9 = 1: ( $3/4 AV_{REF}$ )

The voltage tap of the comparison voltage generator and the analog input voltage are compared and bit 8 of the SAR register is manipulated according to the result of the comparison.

Analog input voltage  $\geq$  Voltage tap of comparison voltage generator: Bit 8 = 1

Analog input voltage  $\leq$  Voltage tap of comparison voltage generator: Bit 8 = 0

Comparison is continued like this to bit 0 of the SAR register.

When performing A/D conversion at a resolution of 8 bits, the comparison continues until bit 2 of the SAR register.

**Remark**  $AV_{REF}$ : The + side reference voltage of the A/D converter. This can be selected from  $AV_{REFP}$ , the internal reference voltage (1.45 V), and  $V_{DD}$ .

### (4) Comparison voltage generator

The comparison voltage generator generates the comparison voltage input from an analog input pin.

**(5) Successive approximation register (SAR)**

The SAR register is a register that sets voltage tap data whose values from the comparison voltage generator match the voltage values of the analog input pins, 1 bit at a time starting from the most significant bit (MSB).

If data is set in the SAR register all the way to the least significant bit (LSB) (end of A/D conversion), the contents of the SAR register (conversion results) are held in the A/D conversion result register (ADCR). When all the specified A/D conversion operations have ended, an A/D conversion end interrupt request signal (INTAD) is generated.

**(6) 10-bit A/D conversion result register (ADCR)**

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCR register holds the A/D conversion result in its higher 10 bits (the lower 6 bits are fixed to 0).

**(7) 8-bit A/D conversion result register (ADCRH)**

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCRH register stores the higher 8 bits of the A/D conversion result.

**(8) Controller**

This circuit controls the conversion time of an input analog signal that is to be converted into a digital signal, as well as starting and stopping of the conversion operation. When A/D conversion has been completed, this controller generates INTAD.

**(9) AV<sub>REFP</sub> pin**

This pin inputs an external reference voltage (AV<sub>REFP</sub>).

If using AV<sub>REFP</sub> as the + side reference voltage of the A/D converter, set the ADREFP1 and ADREFP0 bits of A/D converter mode register 2 (ADM2) to 0 and 1, respectively.

<R> The analog signals input to ANI16 to ANI23 are converted to digital signals based on the voltage applied between AV<sub>REFP</sub> and the – side reference voltage (AV<sub>REFM</sub>/V<sub>SS</sub>).

In addition to AV<sub>REFP</sub>, it is possible to select V<sub>DD</sub> or the internal reference voltage (1.45 V) as the + side reference voltage of the A/D converter.

**(10) AV<sub>REFM</sub> pin**

This pin inputs an external reference voltage (AV<sub>REFM</sub>). If using AV<sub>REFM</sub> as the – side reference voltage of the A/D converter, set the ADREFM bit of the ADM2 register to 1.

In addition to AV<sub>REFM</sub>, it is possible to select V<sub>SS</sub> as the – side reference voltage of the A/D converter.



### 11.3 Registers Used in A/D Converter

The A/D converter uses the following registers.

- Peripheral enable register 0 (PER0)
- A/D converter mode register 0 (ADM0)
- A/D converter mode register 1 (ADM1)
- A/D converter mode register 2 (ADM2)
- 10-bit A/D conversion result register (ADCR)
- 8-bit A/D conversion result register (ADCRH)
- Analog input channel specification register (ADS)
- Conversion result comparison upper limit setting register (ADUL)
- Conversion result comparison lower limit setting register (ADLL)
- A/D test register (ADTES)
- A/D port configuration register (ADPC)
- Port mode control registers 1, 4, 12, and 14 (PMC1, PMC4, PMC12, PMC14)
- Port mode registers 1, 2, 4, 12, and 14 (PM1, PM2, PM4, PM12, PM14)

### 11.3.1 Peripheral enable register 0 (PER0)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When the A/D converter is used, be sure to set bit 5 (ADCEN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 11-2. Format of Peripheral Enable Register 0 (PER0)**

Address: F00F0H After reset: 00H R/W

| Symbol | <7>   | 6 | <5>   | <4>     | 3 | <2>    | 1 | <0>    |
|--------|-------|---|-------|---------|---|--------|---|--------|
| PER0   | RTCEN | 0 | ADCEN | IICA0EN | 0 | SAU0EN | 0 | TAU0EN |

| ADCEN | Control of A/D converter input clock supply                                                                                                                                        |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | Stops input clock supply.<br><ul style="list-style-type: none"> <li>SFR used by the A/D converter cannot be written.</li> <li>The A/D converter is in the reset status.</li> </ul> |
| 1     | Enables input clock supply.<br><ul style="list-style-type: none"> <li>SFR used by the A/D converter can be read/written.</li> </ul>                                                |

<R>

**Cautions 1.** When setting the A/D converter, be sure to set the following registers first while the ADCEN bit is set to 1. If ADCEN = 0, writing to a control register of the A/D converter is ignored, and, even if the register is read, only the default value is read (except for port mode registers 1, 2, 4, 12, and 14 (PM1, PM2, PM4, PM12, and PM14), port mode registers 1, 2, 4, 12, and 14 (PM1, PM2, PM4, PM12, and PM14), port mode control registers 1, 4, 12, and 14 (PMC1, PMC4, PMC12, PMC14), and A/D port configuration register (ADPC)).

- A/D converter mode register 0 (ADM0)
- A/D converter mode register 1 (ADM1)
- A/D converter mode register 2 (ADM2)
- 10-bit A/D conversion result register (ADCR)
- 8-bit A/D conversion result register (ADCRH)
- Analog input channel specification register (ADS)
- Conversion result comparison upper limit setting register (ADUL)
- Conversion result comparison lower limit setting register (ADLL)
- A/D test register (ADTES).

2. Be sure to clear bits 1, 3, and 6 to 0.

### 11.3.2 A/D converter mode register 0 (ADM0)

This register sets the conversion time for analog input to be A/D converted, and starts/stops conversion.

The ADM0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 11-3. Format of A/D Converter Mode Register 0 (ADM0)**

Address: FFF30H After reset: 00H R/W

|        |      |   |                       |                       |                       |                       |                       |      |
|--------|------|---|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|------|
| Symbol | <7>  | 6 | 5                     | 4                     | 3                     | 2                     | 1                     | <0>  |
| ADM0   | ADCS | 0 | FR2 <sup>Note 1</sup> | FR1 <sup>Note 1</sup> | FR0 <sup>Note 1</sup> | LV1 <sup>Note 1</sup> | LV0 <sup>Note 1</sup> | ADCE |

|      |                                                                                                                                                                                                                    |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ADCS | A/D conversion operation control                                                                                                                                                                                   |
| 0    | Stops conversion operation<br>[When read]<br>Conversion stopped/standby status                                                                                                                                     |
| 1    | Enables conversion operation<br>[When read]<br>While in the software trigger mode: Conversion operation status<br>While in the hardware trigger wait mode: Stabilization wait status + conversion operation status |

|      |                                                            |
|------|------------------------------------------------------------|
| ADCE | A/D voltage comparator operation control <sup>Note 2</sup> |
| 0    | Stops A/D voltage comparator operation                     |
| 1    | Enables A/D voltage comparator operation                   |

**Notes** 1. For details of the FR2 to FR0, LV1, LV0 bits, and A/D conversion, see **Table 11-3 A/D Conversion Time Selection**.

2. In software trigger mode and hardware trigger no-wait mode, the operation of the A/D voltage comparator is controlled by the ADCS and ADCE bits, and time is required for the conversion value to stabilize after the A/D converter starts operating (1.0  $\mu$ s). Valid conversion results can therefore be obtained from the first conversion by setting the ADCE bit to 1 and then waiting for the stabilization time (1.0  $\mu$ s) to elapse before setting the ADCS bit to 1. If the ADCS bit is set to 1 before the stabilization time (1.0  $\mu$ s) elapses, the first conversion data must be ignored.

- <R> **Cautions** 1. Change the FR2 to FR0, LV1, and LV0 bits while conversion is stopped (ADCS = 0, ADCE = 0).
- <R> 2. Do not set the ADCS bit to 1 and the ADCE bit to 0 at the same time.
- <R> 3. Do not change the ADCS and ADCE bits from 0 to 1 at the same time by using an 8-bit manipulation instruction. Be sure to set these bits in the order described in 11.7 A/D Converter Setup Flowchart.
4. Be sure to clear bit 6 to 0.

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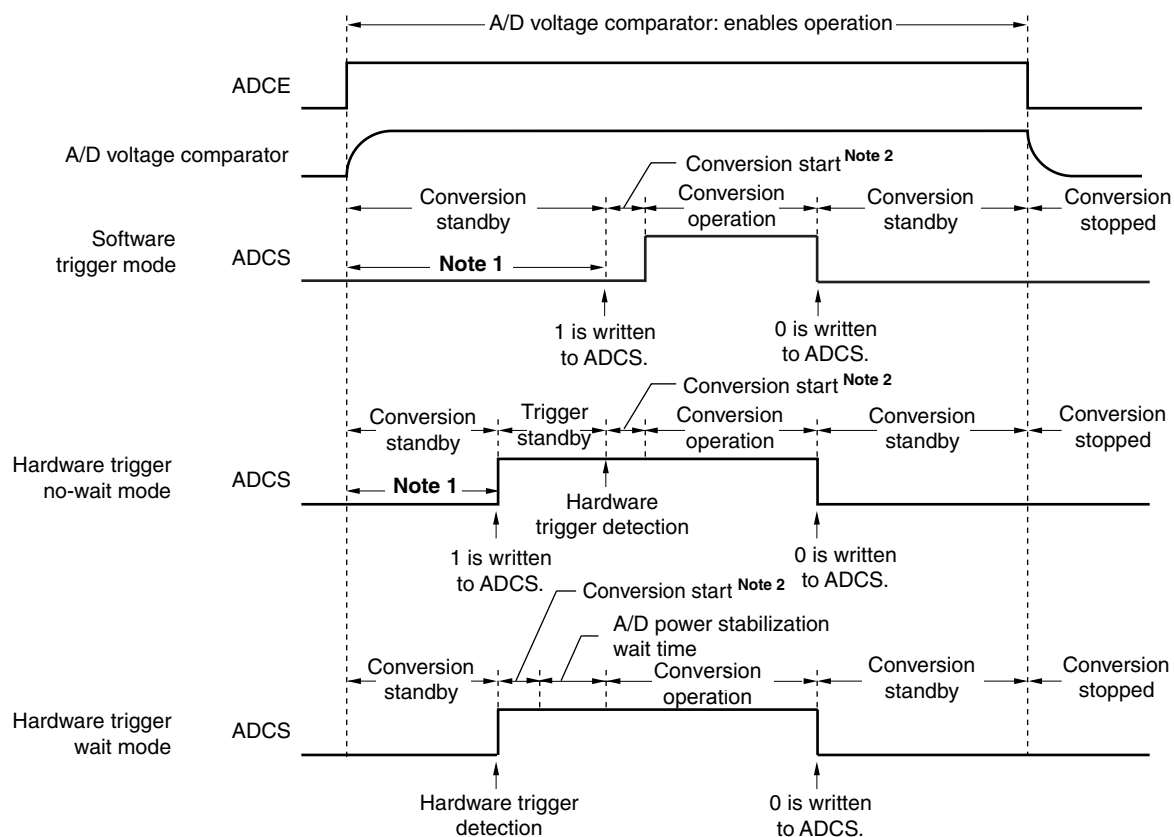
**Table 11-1. Settings of ADCS and ADCE Bits**

| ADCS | ADCE | A/D Conversion Operation |
|------|------|--------------------------|
| 0    | 0    | Stop status              |
| 0    | 1    | Conversion standby mode  |
| 1    | 0    | Setting prohibited       |
| 1    | 1    | Conversion mode          |

**Table 11-2. Setting and Clearing Conditions for ADCS Bit**

| A/D Conversion Mode           |                            | Set Conditions                   | Clear Conditions                                                                                                                                     |
|-------------------------------|----------------------------|----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| Software trigger mode         | Sequential conversion mode | When 1 is written to ADCS        | When 0 is written to ADCS                                                                                                                            |
|                               | One-shot conversion mode   |                                  | <ul style="list-style-type: none"> <li>When 0 is written to ADCS</li> <li>The bit is automatically cleared to 0 when A/D conversion ends.</li> </ul> |
| Hardware trigger no-wait mode | Sequential conversion mode |                                  | When 0 is written to ADCS                                                                                                                            |
|                               | One-shot conversion mode   |                                  | When 0 is written to ADCS                                                                                                                            |
| Hardware trigger wait mode    | Sequential conversion mode | When a hardware trigger is input | When 0 is written to ADCS                                                                                                                            |
|                               | One-shot conversion mode   |                                  | <ul style="list-style-type: none"> <li>When 0 is written to ADCS</li> <li>The bit is automatically cleared to 0 when A/D conversion ends.</li> </ul> |

Figure 11-4. Timing Chart When A/D Voltage Comparator Is Used



**Notes 1.** While in the software trigger mode or hardware trigger no-wait mode, the time from the rising of the ADCE bit to the falling of the ADCS bit must be 1  $\mu$ s or longer to stabilize the internal circuit.

**2.** The following time is the maximum amount of time necessary to start conversion.

| ADM0 |     |     | Conversion<br>Clock<br>( $f_{AD}$ ) | Conversion Start Time (Number of $f_{CLK}$ Clocks)      |                            |
|------|-----|-----|-------------------------------------|---------------------------------------------------------|----------------------------|
| FR2  | FR1 | FR0 |                                     | Software trigger mode/<br>Hardware trigger no wait mode | Hardware trigger wait mode |
| 0    | 0   | 0   | $f_{CLK}/64$                        | 63                                                      | 1                          |
| 0    | 0   | 1   | $f_{CLK}/32$                        | 31                                                      |                            |
| 0    | 1   | 0   | $f_{CLK}/16$                        | 15                                                      |                            |
| 0    | 1   | 1   | $f_{CLK}/8$                         | 7                                                       |                            |
| 1    | 0   | 0   | $f_{CLK}/6$                         | 5                                                       |                            |
| 1    | 0   | 1   | $f_{CLK}/5$                         | 4                                                       |                            |
| 1    | 1   | 0   | $f_{CLK}/4$                         | 3                                                       |                            |
| 1    | 1   | 1   | $f_{CLK}/2$                         | 1                                                       |                            |

<R>

However, for the second and subsequent conversion in sequential conversion mode, the conversion start time and stabilization wait time for A/D power supply do not occur after a hardware trigger is detected.

**Remark**  $f_{CLK}$ : CPU/peripheral hardware clock frequency

- Cautions**
1. If using the hardware trigger wait mode, setting the ADCS bit to 1 is prohibited (but the bit is automatically switched to 1 when the hardware trigger signal is detected). However, it is possible to clear the ADCS bit to 0 to specify the A/D conversion standby status.
  2. While in the one-shot conversion mode of the hardware trigger no-wait mode, the ADCS flag is not automatically cleared to 0 when A/D conversion ends. Instead, 1 is retained.
  - 3 Only rewrite the value of the ADCE bit when ADCS = 0 (while in the conversion stopped/conversion standby status).
  4. To complete A/D conversion, specify at least the following time as the hardware trigger interval:  
Hardware trigger no wait mode:  $2 f_{CLK} \text{ clock} + \text{A/D conversion time}$   
Hardware trigger wait mode:  $2 f_{CLK} \text{ clock} + \text{stabilization wait time} + \text{A/D conversion time}$

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**Table 11-3. A/D Conversion Time Selection (1/4)**

(1) When there is no stabilization wait time

Normal mode 1, 2 (software trigger mode/hardware trigger no-wait mode)

| A/D Converter Mode Register 0<br>(ADM0) |     |     |     |     | Mode     | Conversion<br>Clock (f <sub>AD</sub> ) | Number of<br>Conversion<br>Clock<br>Cycles                                                 | Conversion<br>Time    | Conversion Time Selection       |                             |                             |                              |                              |            |            |
|-----------------------------------------|-----|-----|-----|-----|----------|----------------------------------------|--------------------------------------------------------------------------------------------|-----------------------|---------------------------------|-----------------------------|-----------------------------|------------------------------|------------------------------|------------|------------|
| FR2                                     | FR1 | FR0 | LV1 | LV0 |          |                                        |                                                                                            |                       | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V |                             |                             |                              |                              |            |            |
|                                         |     |     |     |     |          |                                        |                                                                                            |                       | f <sub>CLK</sub> =<br>1 MHz     | f <sub>CLK</sub> =<br>4 MHz | f <sub>CLK</sub> =<br>8 MHz | f <sub>CLK</sub> =<br>16 MHz | f <sub>CLK</sub> =<br>24 MHz |            |            |
| 0                                       | 0   | 0   | 0   | 0   | Normal 1 | f <sub>CLK</sub> /64                   | 19 f <sub>AD</sub><br>(number<br>of<br>sampling<br>clock<br>cycles:<br>7 f <sub>AD</sub> ) | 1216/f <sub>CLK</sub> | Setting<br>prohibited           | Setting<br>prohibited       | Setting<br>prohibited       | 76 μs                        | 50.6667 μs                   |            |            |
| 0                                       | 0   | 1   |     |     |          | f <sub>CLK</sub> /32                   | 608/f <sub>CLK</sub>                                                                       |                       |                                 |                             |                             | 76 μs                        | 38 μs                        | 25.3333 μs |            |
| 0                                       | 1   | 0   |     |     |          | f <sub>CLK</sub> /16                   | 304/f <sub>CLK</sub>                                                                       |                       |                                 |                             |                             | 76 μs                        | 38 μs                        | 19 μs      | 12.6667 μs |
| 0                                       | 1   | 1   |     |     |          | f <sub>CLK</sub> /8                    | 152/f <sub>CLK</sub>                                                                       |                       |                                 |                             |                             | 38 μs                        | 19 μs                        | 9.5 μs     | 6.3333 μs  |
| 1                                       | 0   | 0   |     |     |          | f <sub>CLK</sub> /6                    | 114/f <sub>CLK</sub>                                                                       |                       |                                 |                             |                             | 28.5 μs                      | 14.25 μs                     | 7.125 μs   | 4.75 μs    |
| 1                                       | 0   | 1   |     |     |          | f <sub>CLK</sub> /5                    | 95/f <sub>CLK</sub>                                                                        | 95 μs                 |                                 |                             |                             | 23.75 μs                     | 11.875 μs                    | 5.938 μs   | 3.9583 μs  |
| 1                                       | 1   | 0   |     |     |          | f <sub>CLK</sub> /4                    | 76/f <sub>CLK</sub>                                                                        | 76 μs                 | 19 μs                           | 9.5 μs                      | 4.75 μs                     | 3.1667 μs                    | Note 1                       |            |            |
| 1                                       | 1   | 1   |     |     |          | f <sub>CLK</sub> /2                    | 38/f <sub>CLK</sub>                                                                        | 38 μs                 | 9.5 μs                          | 4.75 μs                     | 2.375 μs                    | Notes 1, 2                   | Setting<br>prohibited        |            |            |
| 0                                       | 0   | 0   | 0   | 1   | Normal 2 | f <sub>CLK</sub> /64                   | 17 f <sub>AD</sub><br>(number<br>of<br>sampling<br>clock<br>cycles:<br>5 f <sub>AD</sub> ) | 1088/f <sub>CLK</sub> | Setting<br>prohibited           | Setting<br>prohibited       | Setting<br>prohibited       | 68 μs                        | 45.3333 μs                   |            |            |
| 0                                       | 0   | 1   |     |     |          | f <sub>CLK</sub> /32                   | 544/f <sub>CLK</sub>                                                                       |                       |                                 |                             |                             | 68 μs                        | 34 μs                        | 22.6667 μs |            |
| 0                                       | 1   | 0   |     |     |          | f <sub>CLK</sub> /16                   | 272/f <sub>CLK</sub>                                                                       |                       |                                 |                             |                             | 68 μs                        | 34 μs                        | 17 μs      | 11.3333 μs |
| 0                                       | 1   | 1   |     |     |          | f <sub>CLK</sub> /8                    | 136/f <sub>CLK</sub>                                                                       |                       |                                 |                             |                             | 34 μs                        | 17 μs                        | 8.5 μs     | 5.6667 μs  |
| 1                                       | 0   | 0   |     |     |          | f <sub>CLK</sub> /6                    | 102/f <sub>CLK</sub>                                                                       |                       |                                 |                             |                             | 25.5 μs                      | 12.75 μs                     | 6.375 μs   | 4.25 μs    |
| 1                                       | 0   | 1   |     |     |          | f <sub>CLK</sub> /5                    | 85/f <sub>CLK</sub>                                                                        | 85 μs                 |                                 |                             |                             | 21.25 μs                     | 10.625 μs                    | 5.3125 μs  | 3.5417 μs  |
| 1                                       | 1   | 0   |     |     |          | f <sub>CLK</sub> /4                    | 68/f <sub>CLK</sub>                                                                        | 68 μs                 | 17 μs                           | 8.5 μs                      | 4.25 μs                     | Notes 1, 2                   | 2.8333 μs                    |            |            |
| 1                                       | 1   | 1   |     |     |          | f <sub>CLK</sub> /2                    | 34/f <sub>CLK</sub>                                                                        | 34 μs                 | 8.5 μs                          | 4.25 μs                     | 2.125 μs                    | Notes 1, 2                   | Setting<br>prohibited        |            |            |

**Notes 1.** Setting prohibited when V<sub>DD</sub> < 3.6 V.**2.** This value is prohibited when using the temperature sensor.**Cautions 1.** When rewriting the FR2 to FR0, LV1, and LV0 bits to other than the same data, make sure that conversion has stopped (ADCS = 0, ADCE = 0).**2.** The above conversion time does not include conversion state time. Conversion state time add in the first conversion. Select conversion time, taking clock frequency errors into consideration.**Remark** f<sub>CLK</sub>: CPU/peripheral hardware clock frequency

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**Table 11-3. A/D Conversion Time Selection (2/4)**(2) When there is no stabilization wait time<sup>Note 1</sup>

Low-voltage mode 1, 2 (software trigger mode/hardware trigger no-wait mode)

| A/D Converter Mode Register 0<br>(ADM0) |     |     |     |     | Mode             | Conversion<br>Clock (f <sub>AD</sub> ) | Number of<br>Conversion<br>Clock<br>Cycles                                                 | Conversion<br>Time    | Conversion Time Selection       |                             |                             |                              |                              |                             |                             |                             |
|-----------------------------------------|-----|-----|-----|-----|------------------|----------------------------------------|--------------------------------------------------------------------------------------------|-----------------------|---------------------------------|-----------------------------|-----------------------------|------------------------------|------------------------------|-----------------------------|-----------------------------|-----------------------------|
| FR2                                     | FR1 | FR0 | LV1 | LV0 |                  |                                        |                                                                                            |                       | 1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V |                             | Note 2                      | Note 3                       | Note 4                       |                             |                             |                             |
|                                         |     |     |     |     |                  |                                        |                                                                                            |                       | f <sub>CLK</sub> =<br>1 MHz     | f <sub>CLK</sub> =<br>4 MHz | f <sub>CLK</sub> =<br>8 MHz | f <sub>CLK</sub> =<br>16 MHz | f <sub>CLK</sub> =<br>24 MHz |                             |                             |                             |
| 0                                       | 0   | 0   | 1   | 0   | Low-voltage<br>1 | f <sub>CLK</sub> /64                   | 19 f <sub>AD</sub><br>(number<br>of<br>sampling<br>clock<br>cycles:<br>7 f <sub>AD</sub> ) | 1216/f <sub>CLK</sub> | Setting<br>prohibited           | Setting<br>prohibited       | Setting<br>prohibited       | 76 μs                        | 50.6667 μs                   |                             |                             |                             |
| 0                                       | 0   | 1   |     |     |                  | f <sub>CLK</sub> /32                   |                                                                                            | 608/f <sub>CLK</sub>  |                                 |                             |                             | 76 μs                        | 38 μs                        | 25.3333 μs                  |                             |                             |
| 0                                       | 1   | 0   |     |     |                  | f <sub>CLK</sub> /16                   |                                                                                            | 304/f <sub>CLK</sub>  |                                 |                             |                             | 76 μs                        | 38 μs                        | 19 μs                       | 12.6667 μs                  |                             |
| 0                                       | 1   | 1   |     |     |                  | f <sub>CLK</sub> /8                    |                                                                                            | 152/f <sub>CLK</sub>  |                                 |                             |                             | 38 μs <sup>Note 7</sup>      | 19 μs                        | 9.5 μs <sup>Note 6</sup>    | 6.3333 μs                   |                             |
| 1                                       | 0   | 0   |     |     |                  | f <sub>CLK</sub> /6                    |                                                                                            | 114/f <sub>CLK</sub>  |                                 |                             |                             | 28.5 μs <sup>Note 7</sup>    | 14.25 μs <sup>Note 6</sup>   | 7.125 μs <sup>Note 6</sup>  | 4.75 μs                     |                             |
| 1                                       | 0   | 1   |     |     |                  | f <sub>CLK</sub> /5                    |                                                                                            | 95/f <sub>CLK</sub>   |                                 |                             |                             | 95 μs <sup>Note 7</sup>      | 23.75 μs <sup>Note 6</sup>   | 11.875 μs <sup>Note 6</sup> | 5.938 μs <sup>Note 6</sup>  | 3.9587 μs                   |
| 1                                       | 1   | 0   |     |     |                  | f <sub>CLK</sub> /4                    |                                                                                            | 76/f <sub>CLK</sub>   |                                 |                             |                             | 76 μs <sup>Note 7</sup>      | 19 μs <sup>Note 6</sup>      | 9.5 μs <sup>Note 6</sup>    | 4.75 μs <sup>Note 6</sup>   | 3.1667 μs <sup>Note 5</sup> |
| 1                                       | 1   | 1   |     |     |                  | f <sub>CLK</sub> /2                    |                                                                                            | 38/f <sub>CLK</sub>   |                                 |                             |                             | 38 μs <sup>Note 7</sup>      | 9.5 μs <sup>Note 6</sup>     | 4.75 μs <sup>Note 6</sup>   | 2.375 μs <sup>Note 5</sup>  | Setting<br>prohibited       |
| 0                                       | 0   | 0   | 1   | 1   | Low-voltage<br>2 | f <sub>CLK</sub> /64                   | 17 f <sub>AD</sub><br>(number<br>of<br>sampling<br>clock<br>cycles:<br>5 f <sub>AD</sub> ) | 1088/f <sub>CLK</sub> | Setting<br>prohibited           | Setting<br>prohibited       | Setting<br>prohibited       | 68 μs                        | 45.3333 μs                   |                             |                             |                             |
| 0                                       | 0   | 1   |     |     |                  | f <sub>CLK</sub> /32                   |                                                                                            | 544/f <sub>CLK</sub>  |                                 |                             |                             | 68 μs                        | 34 μs                        | 22.6667 μs                  |                             |                             |
| 0                                       | 1   | 0   |     |     |                  | f <sub>CLK</sub> /16                   |                                                                                            | 272/f <sub>CLK</sub>  |                                 |                             |                             | 68 μs                        | 34 μs                        | 17 μs                       | 11.3333 μs                  |                             |
| 0                                       | 1   | 1   |     |     |                  | f <sub>CLK</sub> /8                    |                                                                                            | 136/f <sub>CLK</sub>  |                                 |                             |                             | 34 μs <sup>Note 7</sup>      | 17 μs                        | 8.5 μs <sup>Note 6</sup>    | 5.6667 μs                   |                             |
| 1                                       | 0   | 0   |     |     |                  | f <sub>CLK</sub> /6                    |                                                                                            | 102/f <sub>CLK</sub>  |                                 |                             |                             | 25.5 μs <sup>Note 7</sup>    | 12.75 μs <sup>Note 6</sup>   | 6.375 μs <sup>Note 6</sup>  | 4.25 μs                     |                             |
| 1                                       | 0   | 1   |     |     |                  | f <sub>CLK</sub> /5                    |                                                                                            | 85/f <sub>CLK</sub>   |                                 |                             |                             | 85 μs <sup>Note 7</sup>      | 21.25 μs <sup>Note 6</sup>   | 10.625 μs <sup>Note 6</sup> | 5.3125 μs <sup>Note 6</sup> | 3.5417 μs                   |
| 1                                       | 1   | 0   |     |     |                  | f <sub>CLK</sub> /4                    |                                                                                            | 68/f <sub>CLK</sub>   |                                 |                             |                             | 68 μs <sup>Note 7</sup>      | 17 μs <sup>Note 6</sup>      | 8.5 μs <sup>Note 6</sup>    | 4.25 μs <sup>Note 6</sup>   | 2.8333 μs <sup>Note 5</sup> |
| 1                                       | 1   | 1   |     |     |                  | f <sub>CLK</sub> /2                    |                                                                                            | 34/f <sub>CLK</sub>   |                                 |                             |                             | 34 μs <sup>Note 7</sup>      | 8.5 μs <sup>Note 6</sup>     | 4.25 μs <sup>Note 6</sup>   | 2.125 μs <sup>Note 5</sup>  | Setting<br>prohibited       |

**Notes 1.** This mode is prohibited when using the temperature sensors.**2.** 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V**3.** 2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V**4.** 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V**5.** Setting prohibited when V<sub>DD</sub> < 3.6 V.**6.** Setting prohibited when V<sub>DD</sub> < 2.7 V.**7.** Setting prohibited when V<sub>DD</sub> < 1.8 V.**Cautions 1.** When rewriting the FR2 to FR0, LV1, and LV0 bits to other than the same data, make sure that conversion has stopped (ADCS = 0, ADCE = 0).**2.** The above conversion time does not include conversion state time. Conversion state time add in the first conversion. Select conversion time, taking clock frequency errors into consideration.**Remark** f<sub>CLK</sub>: CPU/peripheral hardware clock frequency



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**Table 11-3. A/D Conversion Time Selection (3/4)**

(3) When there is stabilization wait time  
 Normal mode 1, 2 (hardware trigger wait mode<sup>Note 1)</sup>)

| A/D Converter Mode<br>Register 0 (ADM0) |         |         |         |         | Mode        | Conversion<br>Clock (f <sub>AD</sub> ) | Number of<br>Stabilization<br>Wait Cycles | Number of<br>Conversion<br>Clock<br>Cycles                                                 | Stabilization<br>Wait Cycles +<br>Conversion<br>Time | Conversion Time Selection       |                             |                             |                              |                              |
|-----------------------------------------|---------|---------|---------|---------|-------------|----------------------------------------|-------------------------------------------|--------------------------------------------------------------------------------------------|------------------------------------------------------|---------------------------------|-----------------------------|-----------------------------|------------------------------|------------------------------|
| FR<br>2                                 | FR<br>1 | FR<br>0 | LV<br>1 | LV<br>0 |             |                                        |                                           |                                                                                            |                                                      | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V |                             |                             |                              |                              |
|                                         |         |         |         |         |             |                                        |                                           |                                                                                            |                                                      | f <sub>CLK</sub> =<br>1 MHz     | f <sub>CLK</sub> =<br>4 MHz | f <sub>CLK</sub> =<br>8 MHz | f <sub>CLK</sub> =<br>16 MHz | f <sub>CLK</sub> =<br>24 MHz |
| 0                                       | 0       | 0       | 0       | 0       | Normal<br>1 | f <sub>CLK</sub> /64                   | 8 f <sub>AD</sub>                         | 19 f <sub>AD</sub><br>(number<br>of<br>sampling<br>clock<br>cycles:<br>7 f <sub>AD</sub> ) | 1728/f <sub>CLK</sub>                                | Setting<br>prohibited           | Setting<br>prohibited       | Setting<br>prohibited       | 108 μs                       | 72 μs                        |
| 0                                       | 0       | 1       |         |         |             | f <sub>CLK</sub> /32                   |                                           |                                                                                            | 864/f <sub>CLK</sub>                                 |                                 |                             | 108 μs                      | 54 μs                        | 36 μs                        |
| 0                                       | 1       | 0       |         |         |             | f <sub>CLK</sub> /16                   |                                           |                                                                                            | 432/f <sub>CLK</sub>                                 |                                 | 108 μs                      | 54 μs                       | 27 μs                        | 18 μs                        |
| 0                                       | 1       | 1       |         |         |             | f <sub>CLK</sub> /8                    |                                           |                                                                                            | 216/f <sub>CLK</sub>                                 |                                 | 54 μs                       | 27 μs                       | 13.5 μs                      | 9 μs                         |
| 1                                       | 0       | 0       |         |         |             | f <sub>CLK</sub> /6                    |                                           |                                                                                            | 162/f <sub>CLK</sub>                                 |                                 | 40.5 μs                     | 20.25 μs                    | 10.125 μs                    | 6.75 μs                      |
| 1                                       | 0       | 1       |         |         |             | f <sub>CLK</sub> /5                    |                                           |                                                                                            | 135/f <sub>CLK</sub>                                 | 135 μs                          | 33.75 μs                    | 16.875 μs                   | 8.4375 μs                    | 5.625 μs                     |
| 1                                       | 1       | 0       |         |         |             | f <sub>CLK</sub> /4                    |                                           |                                                                                            | 108/f <sub>CLK</sub>                                 | 108 μs                          | 27 μs                       | 13.5 μs                     | 6.75 μs                      | 4.5 μs                       |
| 1                                       | 1       | 1       |         |         |             | f <sub>CLK</sub> /2                    |                                           |                                                                                            | 54/f <sub>CLK</sub>                                  | 54 μs                           | 13.5 μs                     | 6.75 μs                     | 3.375 μs<br>Notes 3          | Setting<br>prohibited        |
| 0                                       | 0       | 0       | 0       | 1       | Normal<br>2 | f <sub>CLK</sub> /64                   | 8 f <sub>AD</sub>                         | 17 f <sub>AD</sub><br>(number<br>of<br>sampling<br>clock<br>cycles:<br>5 f <sub>AD</sub> ) | 1600/f <sub>CLK</sub>                                | Setting<br>prohibited           | Setting<br>prohibited       | Setting<br>prohibited       | 100 μs                       | 66.6667 μs                   |
| 0                                       | 0       | 1       |         |         |             | f <sub>CLK</sub> /32                   |                                           |                                                                                            | 800/f <sub>CLK</sub>                                 |                                 |                             | 100 μs                      | 50 μs                        | 33.3333 μs                   |
| 0                                       | 1       | 0       |         |         |             | f <sub>CLK</sub> /16                   |                                           |                                                                                            | 400/f <sub>CLK</sub>                                 |                                 | 100 μs                      | 50 μs                       | 25 μs                        | 16.6667 μs                   |
| 0                                       | 1       | 1       |         |         |             | f <sub>CLK</sub> /8                    |                                           |                                                                                            | 200/f <sub>CLK</sub>                                 |                                 | 50 μs                       | 25 μs                       | 12.5 μs                      | 8.3333 μs                    |
| 1                                       | 0       | 0       |         |         |             | f <sub>CLK</sub> /6                    |                                           |                                                                                            | 150/f <sub>CLK</sub>                                 |                                 | 37.5 μs                     | 18.75 μs                    | 9.375 μs                     | 6.25 μs                      |
| 1                                       | 0       | 1       |         |         |             | f <sub>CLK</sub> /5                    |                                           |                                                                                            | 125/f <sub>CLK</sub>                                 | 125 μs                          | 31.25 μs                    | 15.625 μs                   | 7.8125 μs                    | 5.2083 μs                    |
| 1                                       | 1       | 0       |         |         |             | f <sub>CLK</sub> /4                    |                                           |                                                                                            | 100/f <sub>CLK</sub>                                 | 100 μs                          | 25 μs                       | 12.5 μs                     | 6.25 μs                      | 4.1667 μs<br>Notes 2, 3      |
| 1                                       | 1       | 1       |         |         |             | f <sub>CLK</sub> /2                    |                                           |                                                                                            | 50/f <sub>CLK</sub>                                  | 50 μs                           | 12.5 μs                     | 6.25 μs                     | 3.125 μs<br>Notes 2, 3       | Setting<br>prohibited        |

**Notes 1.** For the second and subsequent conversion in sequential conversion mode, the conversion start time and stabilization wait time for A/D power supply do not occur after a hardware trigger is detected (see **table 12-3 (1/4)**).

- Setting prohibited when V<sub>DD</sub> < 3.6 V.
- This value is prohibited when using the temperature sensors.

**Cautions 1.** When rewriting the FR2 to FR0, LV1, and LV0 bits to other than the same data, make sure that conversion has stopped (ADCS = 0, ADCE = 0).

- The above conversion time does not include conversion state time. Conversion state time add in the first conversion. Select conversion time, taking clock frequency errors into consideration.
- When hardware trigger wait mode, specify the conversion time, including the stabilization wait time from the hardware trigger detection.

**Remark** f<sub>CLK</sub>: CPU/peripheral hardware clock frequency

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**Table 11-3. A/D Conversion Time Selection (4/4)**

(4) When there is no stabilization wait time  
 Low-voltage mode 1, 2<sup>Note 1</sup> (hardware trigger wait mode<sup>Note 2</sup>)

| A/D Converter Mode<br>Register 0 (ADM0) |         |         |         |         | Mode                | Conversion<br>Clock (f <sub>AD</sub> ) | Number of<br>Stabilization<br>Wait Cycles | Number of<br>Conversion<br>Clock<br>Cycles                                                 | Stabilization<br>Wait Cycles +<br>Conversion<br>Time | Conversion Time Selection       |                             |                             |                              |                              |
|-----------------------------------------|---------|---------|---------|---------|---------------------|----------------------------------------|-------------------------------------------|--------------------------------------------------------------------------------------------|------------------------------------------------------|---------------------------------|-----------------------------|-----------------------------|------------------------------|------------------------------|
| FR<br>2                                 | FR<br>1 | FR<br>0 | LV<br>1 | LV<br>0 |                     |                                        |                                           |                                                                                            |                                                      | 1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V | Note 3                      | Note 4                      | Note 5                       |                              |
|                                         |         |         |         |         |                     |                                        |                                           |                                                                                            |                                                      | f <sub>CLK</sub> =<br>1 MHz     | f <sub>CLK</sub> =<br>4 MHz | f <sub>CLK</sub> =<br>8 MHz | f <sub>CLK</sub> =<br>16 MHz | f <sub>CLK</sub> =<br>24 MHz |
| 0                                       | 0       | 0       | 0       | 0       | Low<br>voltage<br>1 | f <sub>CLK</sub> /64                   | 2 f <sub>AD</sub>                         | 19 f <sub>AD</sub><br>(number<br>of<br>sampling<br>clock<br>cycles:<br>7 f <sub>AD</sub> ) | 1344/f <sub>CLK</sub>                                | Setting<br>prohibited           | Setting<br>prohibited       | Setting<br>prohibited       | 84 μs                        | 56 μs                        |
| 0                                       | 0       | 1       |         |         |                     | f <sub>CLK</sub> /32                   |                                           |                                                                                            | 672/f <sub>CLK</sub>                                 |                                 |                             | 84 μs                       | 42 μs                        | 28 μs                        |
| 0                                       | 1       | 0       |         |         |                     | f <sub>CLK</sub> /16                   |                                           |                                                                                            | 336/f <sub>CLK</sub>                                 |                                 | 84 μs                       | 42 μs                       | 21 μs                        | 14 μs                        |
| 0                                       | 1       | 1       |         |         |                     | f <sub>CLK</sub> /8                    |                                           |                                                                                            | 168/f <sub>CLK</sub>                                 |                                 | 42 μs <sup>Note 8</sup>     | 21 μs                       | 10.5 μs <sup>Note 7</sup>    | 7 μs                         |
| 1                                       | 0       | 0       |         |         |                     | f <sub>CLK</sub> /6                    |                                           |                                                                                            | 126/f <sub>CLK</sub>                                 |                                 | 31.25 μs <sup>Note 8</sup>  | 15.75 μs <sup>Note 7</sup>  | 7.875 μs <sup>Note 7</sup>   | 5.25 μs                      |
| 1                                       | 0       | 1       |         |         |                     | f <sub>CLK</sub> /5                    |                                           |                                                                                            | 105/f <sub>CLK</sub>                                 | 105 μs                          | 26.25 μs <sup>Note 8</sup>  | 13.125 μs <sup>Note 7</sup> | 6.5625 μs <sup>Note 7</sup>  | 4.375 μs                     |
| 1                                       | 1       | 0       |         |         |                     | f <sub>CLK</sub> /4                    |                                           |                                                                                            | 84/f <sub>CLK</sub>                                  | 84 μs                           | 21 μs <sup>Note 8</sup>     | 10.5 μs <sup>Note 7</sup>   | 5.25 μs <sup>Note 7</sup>    | 3.5 μs <sup>Note 6</sup>     |
| 1                                       | 1       | 1       |         |         |                     | f <sub>CLK</sub> /2                    |                                           |                                                                                            | 42/f <sub>CLK</sub>                                  | 42 μs <sup>Note 8</sup>         | 10.5 μs <sup>Note 7</sup>   | 5.25 μs <sup>Note 7</sup>   | 2.625 μs <sup>Note 6</sup>   | Setting<br>prohibited        |
| 0                                       | 0       | 0       | 0       | 1       | Low<br>voltage<br>2 | f <sub>CLK</sub> /64                   | 2 f <sub>AD</sub>                         | 17 f <sub>AD</sub><br>(number<br>of<br>sampling<br>clock<br>cycles:<br>5 f <sub>AD</sub> ) | 1216/f <sub>CLK</sub>                                | Setting<br>prohibited           | Setting<br>prohibited       | Setting<br>prohibited       | 76 μs                        | 50.6667 μs                   |
| 0                                       | 0       | 1       |         |         |                     | f <sub>CLK</sub> /32                   |                                           |                                                                                            | 608/f <sub>CLK</sub>                                 |                                 |                             | 76 μs                       | 38 μs                        | 25.3333 μs                   |
| 0                                       | 1       | 0       |         |         |                     | f <sub>CLK</sub> /16                   |                                           |                                                                                            | 304/f <sub>CLK</sub>                                 |                                 | 76 μs                       | 38 μs                       | 19 μs                        | 12.6667 μs                   |
| 0                                       | 1       | 1       |         |         |                     | f <sub>CLK</sub> /8                    |                                           |                                                                                            | 152/f <sub>CLK</sub>                                 |                                 | 38 μs <sup>Note 8</sup>     | 19 μs                       | 9.5 μs <sup>Note 7</sup>     | 6.3333 μs                    |
| 1                                       | 0       | 0       |         |         |                     | f <sub>CLK</sub> /6                    |                                           |                                                                                            | 114/f <sub>CLK</sub>                                 |                                 | 28.5 μs <sup>Note 8</sup>   | 14.25 μs <sup>Note 7</sup>  | 7.125 μs <sup>Note 7</sup>   | 4.75 μs                      |
| 1                                       | 0       | 1       |         |         |                     | f <sub>CLK</sub> /5                    |                                           |                                                                                            | 96/f <sub>CLK</sub>                                  | 96 μs                           | 23.75 μs <sup>Note 8</sup>  | 12 μs <sup>Note 7</sup>     | 5.938 μs <sup>Note 7</sup>   | 4.0 μs                       |
| 1                                       | 1       | 0       |         |         |                     | f <sub>CLK</sub> /4                    |                                           |                                                                                            | 76/f <sub>CLK</sub>                                  | 76 μs                           | 19 μs <sup>Note 8</sup>     | 9.5 μs <sup>Note 7</sup>    | 4.75 μs <sup>Note 7</sup>    | 3.1667 μs <sup>Note 6</sup>  |
| 1                                       | 1       | 1       |         |         |                     | f <sub>CLK</sub> /2                    |                                           |                                                                                            | 38/f <sub>CLK</sub>                                  | 38 μs <sup>Note 8</sup>         | 9.5 μs <sup>Note 7</sup>    | 4.75 μs <sup>Note 7</sup>   | 2.375 μs <sup>Note 6</sup>   | Setting<br>prohibited        |

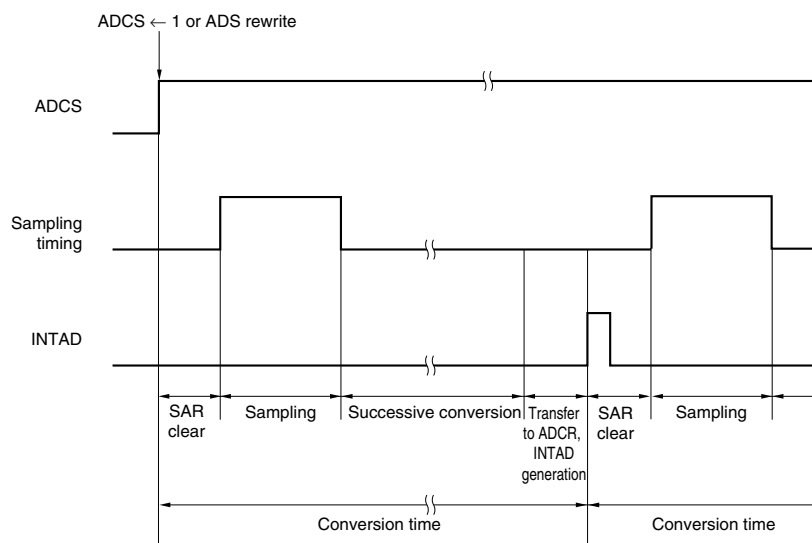
**Notes 1.** This mode is prohibited when using the temperature sensor

- For the second and subsequent conversion in sequential conversion mode, the conversion start time and stabilization wait time for A/D power supply do not occur after a hardware trigger is detected (see **table 12-3 (2/4)**).
- 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V
- 2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V
- 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V
- Setting prohibited when V<sub>DD</sub> < 3.6 V.
- Setting prohibited when V<sub>DD</sub> < 2.7 V.
- Setting prohibited when V<sub>DD</sub> < 1.8 V.

**Cautions 1.** When rewriting the FR2 to FR0, LV1, and LV0 bits to other than the same data, make sure that conversion has stopped (ADCS = 0, ADCE = 0).

- The above conversion time does not include conversion state time. Conversion state time add in the first conversion. Select conversion time, taking clock frequency errors into consideration.
- When hardware trigger wait mode, specify the conversion time, including the stabilization wait time from the hardware trigger detection.

**Remark** f<sub>CLK</sub>: CPU/peripheral hardware clock frequency

**Figure 11-5. A/D Converter Sampling and A/D Conversion Timing (Example for Software Trigger Mode)**

### 11.3.3 A/D converter mode register 1 (ADM1)

This register is used to specify the A/D conversion trigger, conversion mode, and hardware trigger signal.

The ADM1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 11-6. Format of A/D Converter Mode Register 1 (ADM1)**

Address: FFF32H After reset: 00H R/W

| Symbol | 7      | 6      | 5     | 4 | 3 | 2 | 1      | 0      |
|--------|--------|--------|-------|---|---|---|--------|--------|
| ADM1   | ADTMD1 | ADTMD0 | ADSCM | 0 | 0 | 0 | ADTRS1 | ADTRS0 |

| ADTMD1 | ADTMD0 | Selection of the A/D conversion trigger mode |
|--------|--------|----------------------------------------------|
| 0      | ×      | Software trigger mode                        |
| 1      | 0      | Hardware trigger no-wait mode                |
| 1      | 1      | Hardware trigger wait mode                   |

| ADSCM | Specification of the A/D conversion mode |
|-------|------------------------------------------|
| 0     | Sequential conversion mode               |
| 1     | One-shot conversion mode                 |

| ADTRS1 | ADTRS0 | Selection of the hardware trigger signal                           |
|--------|--------|--------------------------------------------------------------------|
| 0      | 0      | End of timer channel 1 count or capture interrupt signal (INTTM01) |
| 0      | 1      | Setting prohibited                                                 |
| 1      | 0      | Real-time clock interrupt signal (INTRTC)                          |
| 1      | 1      | 12-bit interval timer interrupt signal (INTIT)                     |

<R>

**Cautions** 1. Rewrite the value of the ADM1 register while conversion is stopped (ADCS = 0, ADCE = 0).

<R>

2. To complete A/D conversion, specify at least the following time as the hardware trigger interval:

Hardware trigger no wait mode:  $2 f_{CLK} \text{ clock} + \text{A/D conversion time}$

Hardware trigger wait mode:  $2 f_{CLK} \text{ clock} + \text{stabilization wait time} + \text{A/D conversion time}$

3. In modes other than SNOOZE mode, input of the next INTRTC or INTIT will not be recognized as a valid hardware trigger for up to four  $f_{CLK}$  cycles after the first INTRTC or INTIT is input.

**Remarks** 1. ×: don't care

2.  $f_{CLK}$ : CPU/peripheral hardware clock frequency

### 11.3.4 A/D converter mode register 2 (ADM2)

This register is used to select the A/D converter reference voltage, check the upper limit and lower limit A/D conversion result values, select the resolution, and specify whether to use the SNOOZE mode.

The ADM2 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 11-7. Format of A/D Converter Mode Register 2 (ADM2) (1/2)**

Address: F0010H After reset: 00H R/W

| Symbol | 7       | 6       | 5      | 4 | <3>   | <2> | 1 | <0>   |
|--------|---------|---------|--------|---|-------|-----|---|-------|
| ADM2   | ADREFP1 | ADREFP0 | ADREFM | 0 | ADRCK | AWC | 0 | ADTYP |

| ADREFP1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | ADREFP0 | Selection of the + side reference voltage source of the A/D converter |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----------------------------------------------------------------------|
| 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 0       | Supplied from V <sub>DD</sub>                                         |
| 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 1       | Supplied from P20/AV <sub>REFP</sub> /ANI0                            |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 0       | Supplied from the internal reference voltage (1.45 V)                 |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 1       | Setting prohibited                                                    |
| <ul style="list-style-type: none"> <li>When ADREFP1 or ADREFP0 bit is rewritten, this must be configured in accordance with the following procedures.               <ol style="list-style-type: none"> <li>Set ADCE = 0</li> <li>Change the values of ADREFP1 and ADREFP0</li> <li>Stabilization wait time (A)</li> <li>Set ADCE = 1</li> <li>Stabilization wait time (B)</li> </ol>               When ADREFP1 and ADREFP0 are set to 1 and 0, the setting is changed to A = 5 <math>\mu</math>s, B = 1 <math>\mu</math>s.<br/>               When ADREFP1 and ADREFP0 are set to 0 and 0 or 0 and 1, A needs no wait and B = 1 <math>\mu</math>s.             </li> <li>When ADREFP1 and ADREFP0 are set to 1 and 0, respectively, A/D conversion cannot be performed on the temperature sensor output and internal reference voltage.<br/>Be sure to perform A/D conversion while ADISS = 0.</li> </ul> |         |                                                                       |

| ADREFM | Selection of the – side reference voltage source of the A/D converter |
|--------|-----------------------------------------------------------------------|
| 0      | Supplied from V <sub>SS</sub>                                         |
| 1      | Supplied from P21/AV <sub>REFM</sub> /ANI1                            |

| ADRCK                                                                                  | Checking the upper limit and lower limit conversion result values                                                                       |
|----------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 0                                                                                      | The interrupt signal (INTAD) is output when the ADLL register $\leq$ the ADCR register $\leq$ the ADUL register (<1>).                  |
| 1                                                                                      | The interrupt signal (INTAD) is output when the ADCR register < the ADLL register (<2>) or the ADUL register < the ADCR register (<3>). |
| Figure 11-8 shows the generation range of the interrupt signal (INTAD) for <1> to <3>. |                                                                                                                                         |

<R> **Note** This setting can be used only in HS (high-speed main) mode.

<R> **Cautions 1.** Rewrite the value of the ADM2 register while conversion is stopped (ADCS = 0, ADCE = 0).

<R> **2.** Do not set the ADREFP1 bit to 1 when shifting to STOP mode, or to HALT mode while the CPU is operating on the subsystem clock. Also, if the ADREFP1 bit is set to 1, the temperature sensor operating current indicated in 30.3.2 Supply current characteristics (I<sub>TMPS</sub>) will be added to the current consumption when shifting to HALT mode while the CPU is operating on the main system clock.

<R> **3.** When using AV<sub>REFP</sub> and AV<sub>REFM</sub>, specify ANI0 and ANI1 as the analog input channels and specify input mode by using the port mode register.

Figure 11-7. Format of A/D Converter Mode Register 2 (ADM2) (2/2)

Address: F0010H After reset: 00H R/W

|        |         |         |        |   |       |     |   |       |
|--------|---------|---------|--------|---|-------|-----|---|-------|
| Symbol | 7       | 6       | 5      | 4 | <3>   | <2> | 1 | <0>   |
| ADM2   | ADREFP1 | ADREFP0 | ADREFM | 0 | ADRCK | AWC | 0 | ADTYP |

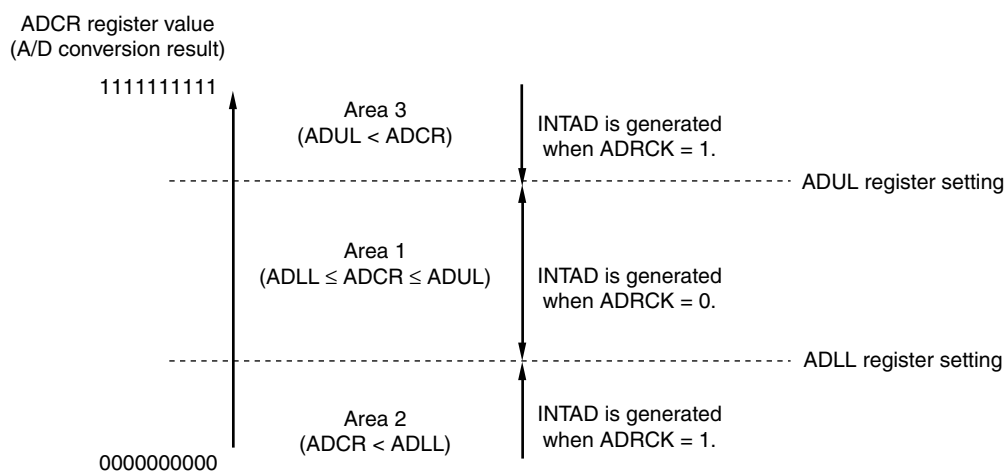
| AWC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Specification of the SNOOZE mode     |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|
| 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Do not use the SNOOZE mode function. |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Use the SNOOZE mode function.        |
| <p>When there is a hardware trigger signal in the STOP mode, the STOP mode is exited, and A/D conversion is performed without operating the CPU (the SNOOZE mode).</p> <ul style="list-style-type: none"> <li>The SNOOZE mode function can only be specified when the high-speed on-chip oscillator clock is selected for the CPU/peripheral hardware clock (<math>f_{CLK}</math>). If any other clock is selected, specifying this mode is prohibited.</li> <li>Using the SNOOZE mode function in the software trigger mode or hardware trigger no-wait mode is prohibited.</li> <li>Using the SNOOZE mode function in the sequential conversion mode is prohibited.</li> <li>When using the SNOOZE mode function, specify a hardware trigger interval of at least “shift time to SNOOZE mode<sup>Note</sup> + A/D power supply stabilization wait time + A/D conversion time + 2 <math>f_{CLK}</math> clock”</li> <li>Even when using SNOOZE mode, be sure to set the AWC bit to 0 in normal operation mode and change it to 1 just before shifting to STOP mode.</li> </ul> <p>Also, be sure to change the AWC bit to 0 after returning from STOP mode to normal operation mode.</p> <p>If the AWC bit is left set to 1, A/D conversion will not start normally in spite of the subsequent SNOOZE or normal operation mode.</p> |                                      |

| ADTYP | Selection of the A/D conversion resolution |
|-------|--------------------------------------------|
| 0     | 10-bit resolution                          |
| 1     | 8-bit resolution                           |

**Note** Refer to “From STOP to SNOOZE” in 19.3.3 SNOOZE mode

**Caution** Only rewrite the value of the ADM2 register while conversion operation is stopped (which is indicated by the ADCS bit of A/D converter mode register 0 (ADM0) being 0).

Figure 11-8. ADRCK Bit Interrupt Signal Generation Range



**Remark** If INTAD does not occur, the A/D conversion result is not stored in the ADCR or ADCRH register.

### 11.3.5 10-bit A/D conversion result register (ADCR)

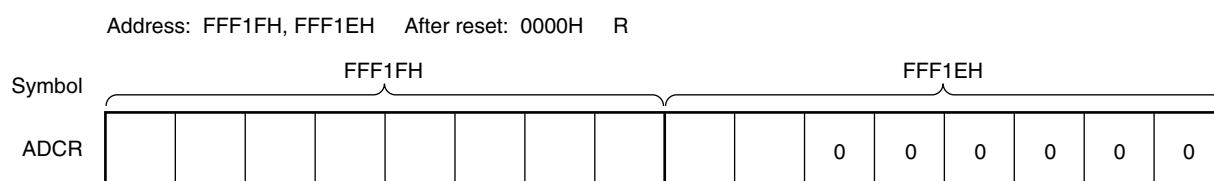
This register is a 16-bit register that stores the A/D conversion result. The lower 6 bits are fixed to 0. Each time A/D conversion ends, the conversion result is loaded from the successive approximation register (SAR). The higher 8 bits of the conversion result are stored in FFF1FH and the lower 2 bits are stored in the higher 2 bits of FFF1EH<sup>Note</sup>.

The ADCR register can be read by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

<R> **Note** If the A/D conversion result is outside the range specified by using the A/D conversion comparison function (the value specified by the ADRCK bit of the ADM2 register and ADUL/ADLL registers; see Figure 11-8), the result is not stored.

**Figure 11-9. Format of 10-bit A/D Conversion Result Register (ADCR)**



- Cautions**
1. When writing to the A/D converter mode register 0 (ADM0), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of the ADCR register may become undefined. Read the conversion result following conversion completion before writing to the ADM0, ADS, and ADPC registers. Using timing other than the above may cause an incorrect conversion result to be read.
  2. When 8-bit resolution A/D conversion is selected (when the ADTYP bit of A/D converter mode register 2 (ADM2) is 1) and the ADCR register is read, 0 is read from the lower two bits (ADCR1 and ADCR0).
  3. When the ADCR register is accessed in 16-bit units, the higher 10 bits of the conversion result are read in order starting at bit 15.

### 11.3.6 8-bit A/D conversion result register (ADCRH)

This register is an 8-bit register that stores the A/D conversion result. The higher 8 bits of 10-bit resolution are stored <sup>Note</sup>.

The ADCRH register can be read by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

<R> **Note** If the A/D conversion result is outside the range specified by using the A/D conversion comparison function (the value specified by the ADRCK bit of the ADM2 register and ADUL/ADLL registers; see Figure 11-8), the result is not stored.

**Figure 11-10. Format of 8-bit A/D Conversion Result Register (ADCRH)**

Address: FFF1FH    After reset: 00H    R

|        |   |   |   |   |   |   |   |   |
|--------|---|---|---|---|---|---|---|---|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADCRH  |   |   |   |   |   |   |   |   |

**Caution** When writing to the A/D converter mode register 0 (ADM0), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of the ADCRH register may become undefined. Read the conversion result following conversion completion before writing to the ADM0, ADS, and ADPC registers. Using timing other than the above may cause an incorrect conversion result to be read.



### 11.3.7 Analog input channel specification register (ADS)

This register specifies the input channel of the analog voltage to be A/D converted.

The ADS register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 11-11. Format of Analog Input Channel Specification Register (ADS)**

Address: FFF31H After reset: 00H R/W

| Symbol | 7     | 6 | 5 | 4    | 3    | 2    | 1    | 0    |
|--------|-------|---|---|------|------|------|------|------|
| ADS    | ADISS | 0 | 0 | ADS4 | ADS3 | ADS2 | ADS1 | ADS0 |

| ADISS                | ADS4 | ADS3 | ADS2 | ADS1 | ADS0 | Analog input channel | Input source                                             |
|----------------------|------|------|------|------|------|----------------------|----------------------------------------------------------|
| 0                    | 0    | 0    | 0    | 0    | 0    | ANI0                 | P20/ANI0/AV <sub>REFP</sub> pin                          |
| 0                    | 0    | 0    | 0    | 0    | 1    | ANI1                 | P21/ANI1/AV <sub>REFM</sub> pin                          |
| 0                    | 1    | 0    | 0    | 0    | 0    | ANI16                | P41/ANI16 pin                                            |
| 0                    | 1    | 0    | 0    | 0    | 1    | ANI17                | P120/ANI17 pin                                           |
| 0                    | 1    | 0    | 0    | 1    | 0    | ANI18                | P13/ANI18 pin                                            |
| 0                    | 1    | 0    | 0    | 1    | 1    | ANI19                | P14/ANI19 pin                                            |
| 0                    | 1    | 0    | 1    | 0    | 0    | ANI20                | P142/ANI20 pin                                           |
| 0                    | 1    | 0    | 1    | 0    | 1    | ANI21                | P143/ANI21 pin                                           |
| 0                    | 1    | 0    | 1    | 1    | 0    | ANI22                | P144/ANI22 pin                                           |
| 0                    | 1    | 0    | 1    | 1    | 1    | ANI23                | P145/ANI23 pin                                           |
| 1                    | 0    | 0    | 0    | 0    | 0    | –                    | Temperature sensor output<br>Notes 1, 2                  |
| 1                    | 0    | 0    | 0    | 0    | 1    | –                    | Internal reference voltage<br>output (1.45 V) Notes 1, 2 |
| Other than the above |      |      |      |      |      | Setting prohibited   |                                                          |

- Notes**
1. Do not select when shifting to STOP mode, or to HALT mode while the CPU is operating on the subsystem clock.
  2. Can only be used in HS (high-speed main) mode.

- Cautions**
1. Be sure to clear bits 5 and 6 to 0.
  2. Set a channel to be set the analog input by ADPC and PMC registers in the input mode by using port mode registers 1, 2, 4, 12, and 14 (PM1, PM2, PM4, PM12, PM14).
  3. Do not set the pin that is set by the A/D port configuration register (ADPC) as digital I/O by the ADS register.
  4. Do not set the pin that is set by port mode control register 1, 4, 12, or 14 (PMC1, PMC4, PMC12, PMC14) as digital I/O by the ADS register.
  5. Rewrite the value of the ADISS bit while conversion is stopped (ADCS = 0, ADCE = 0).
  6. If using AV<sub>REFP</sub> as the + side reference voltage source of the A/D converter, do not select ANI0 as an A/D conversion channel.
  7. If using AV<sub>REFM</sub> as the – side reference voltage source of the A/D converter, do not select ANI1 as an A/D conversion channel.
  8. If ADISS is set to 1, the internal reference voltage (1.45 V) cannot be used for the + side reference voltage source.

<R>

- <R> **Cautions 9.** Do not set the ADISS bit to 1 when shifting to STOP mode, or to HALT mode while the CPU is operating on the subsystem clock. Also, if the ADREFP1 bit is set to 1, the A/D converter reference voltage current (I<sub>ADREF</sub>) indicated in 30.3.2 Supply current characteristics will be added to the current consumption when shifting to HALT mode while the CPU is operating on the main system clock.
- <R> **10.** Ignore the conversion result if the corresponding ANI pin does not exist in the product used.

### 11.3.8 Conversion result comparison upper limit setting register (ADUL)

This register is used to specify the setting for checking the upper limit of the A/D conversion results.

The A/D conversion results and ADUL register value are compared, and interrupt signal (INTAD) generation is controlled in the range specified for the ADRCK bit of A/D converter mode register 2 (ADM2) (shown in **Figure 11-8**).

The ADUL register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

**Caution** When 10-bit resolution A/D conversion is selected, the higher eight bits of the 10-bit A/D conversion result register (ADCR) are compared with the ADUL register.

**Figure 11-12. Format of Conversion Result Comparison Upper Limit Setting Register (ADUL)**

Address: F0011H After reset: FFH R/W

| Symbol | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| ADUL   | ADUL7 | ADUL6 | ADUL5 | ADUL4 | ADUL3 | ADUL2 | ADUL1 | ADUL0 |

### 11.3.9 Conversion result comparison lower limit setting register (ADLL)

This register is used to specify the setting for checking the lower limit of the A/D conversion results.

The A/D conversion results and ADLL register value are compared, and interrupt signal (INTAD) generation is controlled in the range specified for the ADRCK bit of A/D converter mode register 2 (ADM2) (shown in **Figure 11-8**).

The ADLL register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 11-13. Format of Conversion Result Comparison Lower Limit Setting Register (ADLL)**

Address: F0012H After reset: 00H R/W

| Symbol | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| ADLL   | ADLL7 | ADLL6 | ADLL5 | ADLL4 | ADLL3 | ADLL2 | ADLL1 | ADLL0 |

**Caution** When 10-bit resolution A/D conversion is selected, the higher eight bits of the 10-bit A/D conversion result register (ADCR) are compared with the ADLL register.

### 11.3.10 A/D test register (ADTES)

This register is used to select the + side reference voltage ( $AV_{REFP}$ ) or - side reference voltage ( $AV_{REFM}$ ) of the A/D converter, or the analog input channel (ANLxx) as the A/D conversion target for the A/D test function.

The ADTES register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 11-14. Format of A/D Test Register (ADTES)**

Address: F0013H After reset: 00H R/W

|        |   |   |   |   |   |   |        |        |
|--------|---|---|---|---|---|---|--------|--------|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1      | 0      |
| ADTES  | 0 | 0 | 0 | 0 | 0 | 0 | ADTES1 | ADTES0 |

| ADTES1               | ADTES0 | A/D conversion target                                                                                  |
|----------------------|--------|--------------------------------------------------------------------------------------------------------|
| 0                    | 0      | ANLxx (This is specified using the analog input channel specification register (ADS).) <sup>Note</sup> |
| 1                    | 0      | $AV_{REFM}$                                                                                            |
| 1                    | 1      | $AV_{REFP}$                                                                                            |
| Other than the above |        | Setting prohibited                                                                                     |

**Note** Temperature sensor output/internal reference voltage (1.45 V) can be used only in HS (high-speed main) mode.

<R>

**Caution** For details of the A/D test function, see CHAPTER 23 SAFETY FUNCTIONS.

### 11.3.11 A/D port configuration register (ADPC)

This register switches the ANI0/P20 and ANI1/P21 pins to analog input of A/D converter or digital I/O of port.

The ADPC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 11-15. Format of A/D Port Configuration Register (ADPC)**

Address: F0076H After reset: 00H R/W

|        |   |   |   |   |   |   |       |       |
|--------|---|---|---|---|---|---|-------|-------|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0     |
| ADPC   | 0 | 0 | 0 | 0 | 0 | 0 | ADPC1 | ADPC0 |

| ADPC1 | ADPC0 | Analog input (A)/digital I/O (D) switching |          |
|-------|-------|--------------------------------------------|----------|
|       |       | ANI1/P21                                   | ANI0/P20 |
| 0     | 0     | A                                          | A        |
| 0     | 1     | D                                          | D        |
| 1     | 0     | D                                          | A        |
| 1     | 1     | A                                          | A        |

- Cautions**
1. Set the port to analog input by ADPC register to the input mode by using port mode register 2 (PM2).
  2. Do not set the pin set by the ADPC register as digital I/O by the analog input channel specification register (ADS).
  3. When using  $AV_{REFP}$  and  $AV_{REFM}$ , specify ANI0 and ANI1 as the analog input channels and specify input mode by using the port mode register.

<R>

### 11.3.12 Port mode control registers 1, 4, 12, and 14 (PMC1, PMC4, PMC12, PMC14)

This register switches the ANI16 to ANI23 pins to digital I/O of port or analog input of A/D converter.

The PMC1, PMC4, PMC12, and PMC14 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

**Figure 11-16. Formats of Port Mode Control Registers 1, 4, 12, and 14 (PMC1, PMC4, PMC12, PMC14)**

Address: F0061H    After reset: FFH    R/W

|        |   |   |   |       |       |   |   |   |
|--------|---|---|---|-------|-------|---|---|---|
| Symbol | 7 | 6 | 5 | 4     | 3     | 2 | 1 | 0 |
| PMC1   | 1 | 1 | 1 | PMC14 | PMC13 | 1 | 1 | 1 |

Address: F0064H    After reset: FFH    R/W

|        |   |   |   |   |   |   |       |   |
|--------|---|---|---|---|---|---|-------|---|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0 |
| PMC4   | 1 | 1 | 1 | 1 | 1 | 1 | PMC41 | 1 |

Address: F006CH    After reset: FFH    R/W

|        |   |   |   |   |   |   |   |        |
|--------|---|---|---|---|---|---|---|--------|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0      |
| PMC12  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | PMC120 |

Address: F006EH    After reset: FFH    R/W

|        |   |   |        |        |        |        |   |   |
|--------|---|---|--------|--------|--------|--------|---|---|
| Symbol | 7 | 6 | 5      | 4      | 3      | 2      | 1 | 0 |
| PMC14  | 1 | 1 | PMC145 | PMC144 | PMC143 | PMC142 | 1 | 1 |

|       |                                                                           |
|-------|---------------------------------------------------------------------------|
| PMCMn | Pmn pin digital I/O/analog input selection (m = 1, 4, 12, 14; n = 0 to 5) |
| 0     | Digital I/O (dual-use function other than analog input)                   |
| 1     | Analog input                                                              |

<R> **Caution** Set the port to analog input by PMC register to the input mode by using port mode registers x (PMx).

**11.3.13 Port mode registers 1, 2, 4, 12, and 14 (PM1, PM2, PM4, PM12, PM14)**

When using the ANI0/AV<sub>REFP</sub>/P20, ANI1/AV<sub>REFM</sub>/P21, ANI16/TI04/TO04/SEG24/P41, ANI17/SEG25/P120, ANI18/SEG31/P13, ANI19/SEG32/P14, or ANI20/SEG33/P142 to ANI23/SEG36/P145 pin for an analog input port, set the PM20, PM21, PM41, PM120, PM13, PM14, or PM142 to PM145 bit to 1. The output latches of P20, P21, P41, P120, P13, P14, and P142 to P145 at this time may be 0 or 1.

If the PM20, PM21, PM41, PM120, PM13, PM14, and PM142 to PM145 bits are set to 0, they cannot be used as analog input port pins.

The PM1, PM2, PM4, PM12, and PM14 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

**Caution** If a pin is set as an analog input port, not the pin level but “0” is always read.

**Figure 11-17. Formats of Port Mode Registers 1, 2, 4, 12, and 14 (PM1, PM2, PM4, PM12, PM14) (64-pin products)**

Address: FFF21H After reset: FFH R/W

| Symbol | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|--------|------|------|------|------|------|------|------|------|
| PM1    | PM17 | PM16 | PM15 | PM14 | PM13 | PM12 | PM11 | PM10 |

Address: FFF22H After reset: FFH R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0    |
|--------|---|---|---|---|---|---|------|------|
| PM2    | 1 | 1 | 1 | 1 | 1 | 1 | PM21 | PM20 |

Address: FFF24H After reset: FFH R/W

| Symbol | 7 | 6 | 5 | 4 | 3    | 2    | 1    | 0    |
|--------|---|---|---|---|------|------|------|------|
| PM4    | 1 | 1 | 1 | 1 | PM43 | PM42 | PM41 | PM40 |

Address: FFF2CH After reset: FFH R/W

| Symbol | 7     | 6     | 5     | 4 | 3 | 2 | 1 | 0     |
|--------|-------|-------|-------|---|---|---|---|-------|
| PM12   | PM127 | PM126 | PM125 | 1 | 1 | 1 | 1 | PM120 |

Address: FFF2EH After reset: FFH R/W

| Symbol | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| PM14   | PM147 | PM146 | PM145 | PM144 | PM143 | PM142 | PM141 | PM140 |

| PMmn | Pmn pin I/O mode selection (m = 1, 2, 4, 12, 14, n = 0 to 7) |
|------|--------------------------------------------------------------|
| 0    | Output mode (output buffer on)                               |
| 1    | Input mode (output buffer off)                               |

<R> **Caution** When using AV<sub>REFP</sub> and AV<sub>REFM</sub>, specify ANI0 and ANI1 as the analog input channels and specify input mode by using the port mode register.

**Remark** The figure shown above presents the format of port mode registers 1, 2, 4, 12, and 14 of the 64-pin products. The format of the port mode register of other products, see **Table 4-2. PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits mounted on each product.**

The ANI0/P20 and ANI1/P21 pins are as shown below depending on the settings of the A/D port configuration register (ADPC), analog input channel specification register (ADS), and PM2 registers.

**Table 11-4. Setting Functions of ANI0/P20 and ANI1/P21 Pins**

| ADPC                   | PM2         | ADS                  | ANI0/P20 and ANI1/P21 Pins         |
|------------------------|-------------|----------------------|------------------------------------|
| Digital I/O selection  | Input mode  | –                    | Digital input                      |
|                        | Output mode | –                    | Digital output                     |
| Analog input selection | Input mode  | Selects ANI.         | Analog input (to be converted)     |
|                        |             | Does not select ANI. | Analog input (not to be converted) |
|                        | Output mode | Selects ANI.         | Setting prohibited                 |
|                        |             | Does not select ANI. |                                    |

The ANI16/P41, ANI17/P120, ANI18/P13, ANI19/P14, and ANI20/P142 to ANI23/P145 pins are as shown below depending on the settings of port mode control registers 1, 4, 12, and 14 (PMC1, PMC4, PMC12, PMC14), analog input channel specification register (ADS), PM1, PM4, PM12, and PM14 registers.

**Table 11-5. Setting Functions of ANI16/P41, ANI17/P120, ANI18/P13, ANI19/P14, and ANI20/P142 to ANI23/P145 Pins**

| PMC1, PMC4, PMC12, PMC14 Registers | PM1, PM4, PM12, PM14 Registers | ADS Register         | ANI16/P41, ANI17/P120, ANI18/P13, ANI19/P14, and ANI20/P142 to ANI23/P145 Pins |
|------------------------------------|--------------------------------|----------------------|--------------------------------------------------------------------------------|
| Digital I/O selection              | Input mode                     | –                    | Digital input                                                                  |
|                                    | Output mode                    | –                    | Digital output                                                                 |
| Analog input selection             | Input mode                     | Selects ANI.         | Analog input (to be converted)                                                 |
|                                    |                                | Does not select ANI. | Analog input (not to be converted)                                             |
|                                    | Output mode                    | Selects ANI.         | Setting prohibited                                                             |
|                                    |                                | Does not select ANI. |                                                                                |

## 11.4 A/D Converter Conversion Operations

The A/D converter conversion operations are described below.

- <1> The voltage input to the selected analog input channel is sampled by the sample & hold circuit.
- <2> When sampling has been done for a certain time, the sample & hold circuit is placed in the hold state and the sampled voltage is held until the A/D conversion operation has ended.
- <3> Bit 9 of the successive approximation register (SAR) is set. The series resistor string voltage tap is set to (1/2)  $AV_{REF}$  by the tap selector.
- <4> The voltage difference between the series resistor string voltage tap and sampled voltage is compared by the voltage comparator. If the analog input is greater than (1/2)  $AV_{REF}$ , the MSB bit of the SAR register remains set to 1. If the analog input is smaller than (1/2)  $AV_{REF}$ , the MSB bit is reset to 0.
- <5> Next, bit 8 of the SAR register is automatically set to 1, and the operation proceeds to the next comparison. The series resistor string voltage tap is selected according to the preset value of bit 9, as described below.
  - Bit 9 = 1: (3/4)  $AV_{REF}$
  - Bit 9 = 0: (1/4)  $AV_{REF}$

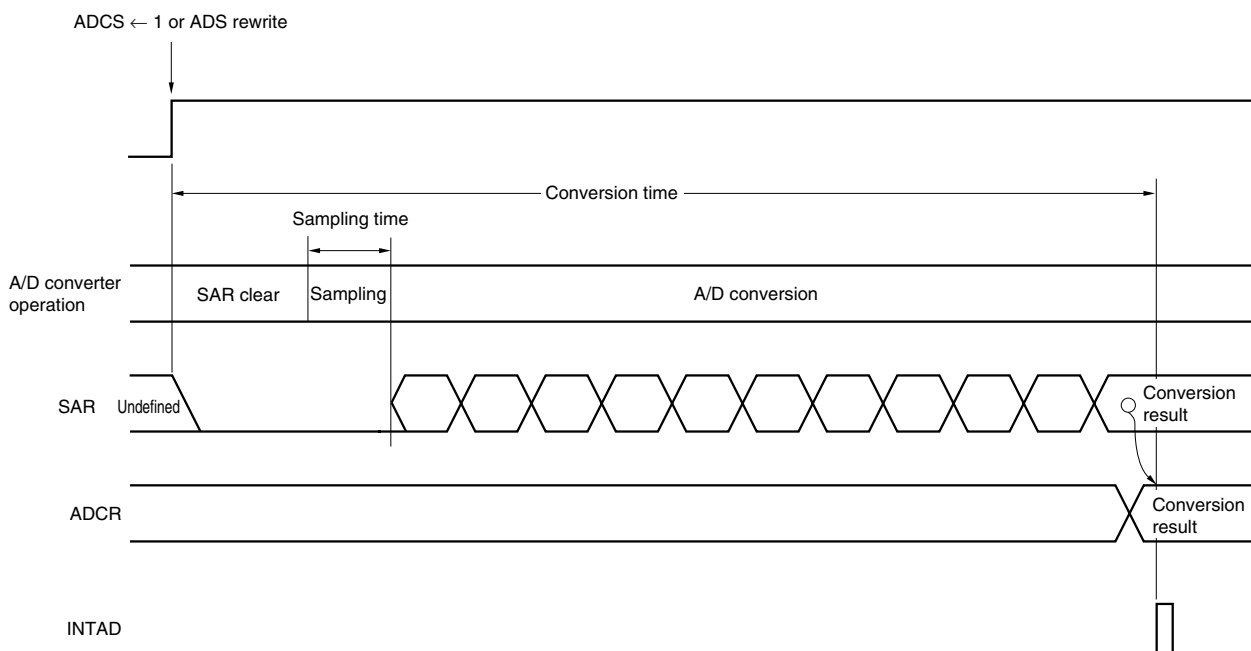
The voltage tap and sampled voltage are compared and bit 8 of the SAR register is manipulated as follows.

- Sampled voltage  $\geq$  Voltage tap: Bit 8 = 1
- Sampled voltage < Voltage tap: Bit 8 = 0
- <6> Comparison is continued in this way up to bit 0 of the SAR register.
- <7> Upon completion of the comparison of 10 bits, an effective digital result value remains in the SAR register, and the result value is transferred to the A/D conversion result register (ADCR, ADCRH) and then latched<sup>Note 1</sup>.  
At the same time, the A/D conversion end interrupt request (INTAD) can also be generated<sup>Note 1</sup>.
- <8> Repeat steps <1> to <7>, until the ADCS bit is cleared to 0<sup>Note 2</sup>.  
To stop the A/D converter, clear the ADCS bit to 0.

- <R> **Notes**
1. If the A/D conversion result is outside the A/D conversion result range specified by the ADRCK bit and the ADUL and ADLL registers (see Figure 11-8), the A/D conversion result interrupt request signal is not generated and no A/D conversion results are stored in the ADCR and ADCRH registers.
  2. While in the sequential conversion mode, the ADCS flag is not automatically cleared to 0. This flag is not automatically cleared to 0 while in the one-shot conversion mode of the hardware trigger no-wait mode, either. Instead, 1 is retained.

**Remarks** 1. Two types of the A/D conversion result registers are available.

- ADCR register (16 bits): Store 10-bit A/D conversion value
  - ADCRH register (8 bits): Store 8-bit A/D conversion value
2.  $AV_{REF}$ : The + side reference voltage of the A/D converter. This can be selected from  $AV_{REFP}$ , the internal reference voltage (1.45 V), and  $V_{DD}$ .

**Figure 11-18. Conversion Operation of A/D Converter (Software Trigger Mode)**

A/D conversion operations are performed continuously until bit 7 (ADCS) of the A/D converter mode register (ADM) is reset (0) by software.

If a write operation is performed to the analog input channel specification register (ADS) during an A/D conversion operation, the conversion operation is initialized, and if the ADCS bit is set (1), conversion starts again from the beginning.

Reset signal generation clears the A/D conversion result register (ADCR, ADCRH) to 0000H or 00H.



## 11.5 Input Voltage and Conversion Results

The relationship between the analog input voltage input to the analog input pins (ANI0, ANI1, ANI16 to ANI23) and the theoretical A/D conversion result (stored in the 10-bit A/D conversion result register (ADCR)) is shown by the following expression.

$$\text{SAR} = \text{INT} \left( \frac{V_{\text{AIN}}}{V_{\text{REF}}} \times 1024 + 0.5 \right)$$

$$\text{ADCR} = \text{SAR} \times 64$$

or

$$\left( \frac{\text{ADCR}}{64} - 0.5 \right) \times \frac{V_{\text{REF}}}{1024} \leq V_{\text{AIN}} < \left( \frac{\text{ADCR}}{64} + 0.5 \right) \times \frac{V_{\text{REF}}}{1024}$$

where, INT( ): Function which returns integer part of value in parentheses

$V_{\text{AIN}}$ : Analog input voltage

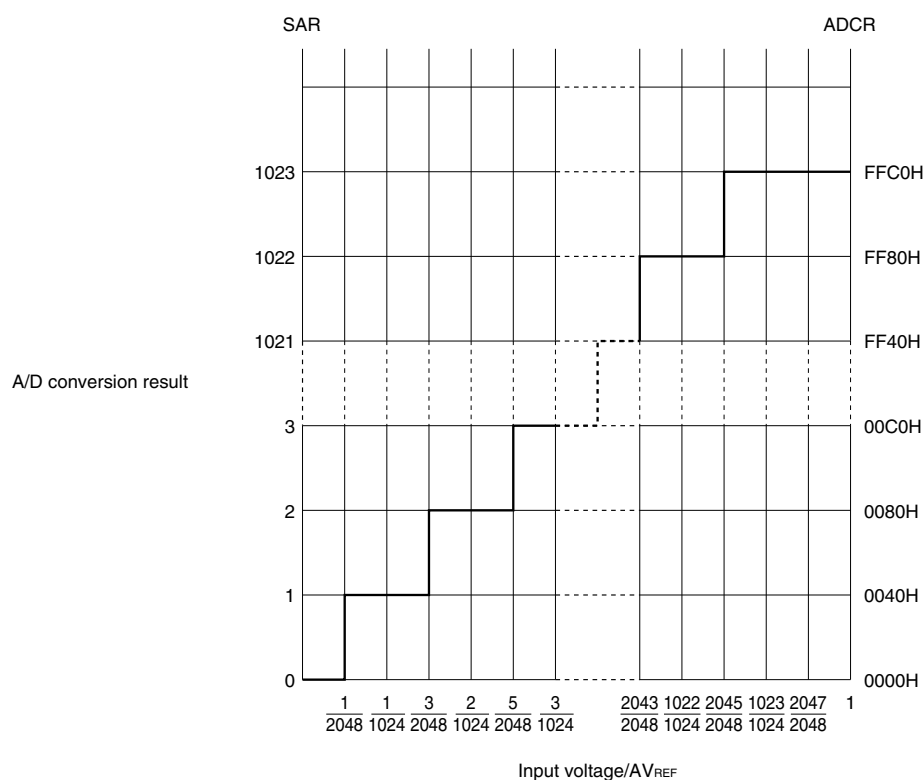
$V_{\text{REF}}$ :  $V_{\text{REF}}$  pin voltage

ADCR: A/D conversion result register (ADCR) value

SAR: Successive approximation register

Figure 11-19 shows the relationship between the analog input voltage and the A/D conversion result.

**Figure 11-19. Relationship Between Analog Input Voltage and A/D Conversion Result**



**Remark**  $V_{\text{REF}}$ : The + side reference voltage of the A/D converter. This can be selected from  $V_{\text{REFP}}$ , the internal reference voltage (1.45 V), and  $V_{\text{DD}}$ .

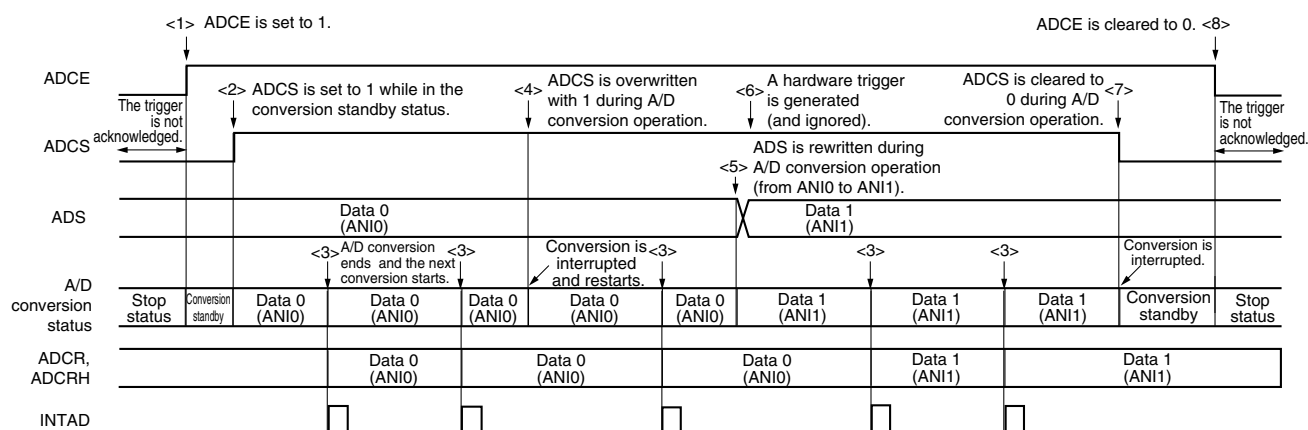
## 11.6 A/D Converter Operation Modes

The operation of each A/D converter mode is described below. In addition, the procedure for specifying each mode is described in **11.7 A/D Converter Setup Flowchart**.

### 11.6.1 Software trigger mode (sequential conversion mode)

- <1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.
- <2> After the software counts up to the stabilization wait time (1.0  $\mu$ s), the ADCS bit of the ADM0 register is set to 1 to perform the A/D conversion of the analog input specified by the analog input channel specification register (ADS).
- <3> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated. After A/D conversion ends, the next A/D conversion immediately starts.
- <4> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.
- <5> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.
- <6> Even if a hardware trigger is input during conversion operation, A/D conversion does not start.
- <7> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status.
- <8> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCE = 0, specifying 1 for ADCS is ignored and A/D conversion does not start.

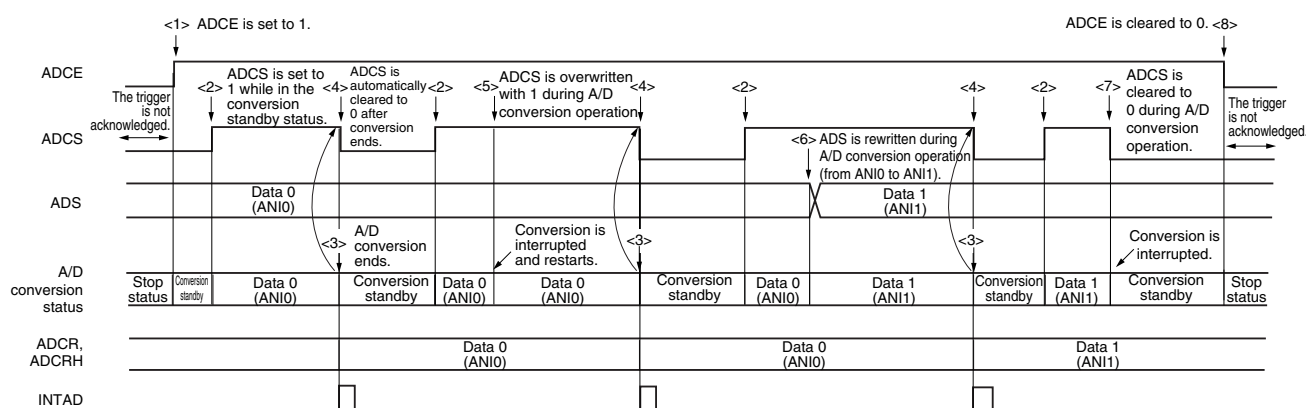
**Figure 11-20. Example of Software Trigger Mode (Sequential Conversion Mode) Operation Timing**



### 11.6.2 Software trigger mode (one-shot conversion mode)

- <1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.
- <2> After the software counts up to the stabilization wait time ( $1.0 \mu\text{s}$ ), the ADCS bit of the ADM0 register is set to 1 to perform the A/D conversion of the analog input specified by the analog input channel specification register (ADS).
- <3> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated.
- <4> After A/D conversion ends, the ADCS bit is automatically cleared to 0, and the system enters the A/D conversion standby status.
- <5> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.
- <6> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.
- <7> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status.
- <8> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When  $\text{ADCE} = 0$ , specifying 1 for ADCS is ignored and A/D conversion does not start. In addition, A/D conversion does not start even if a hardware trigger is input while in the A/D conversion standby status.

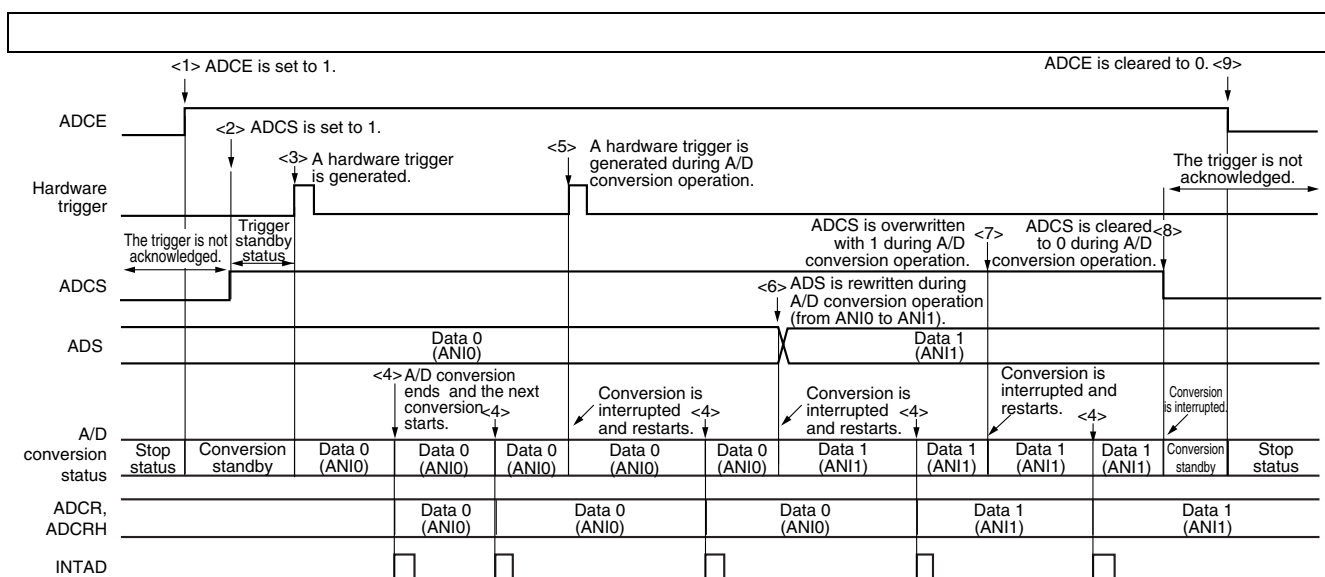
**Figure 11-21. Example of Software Trigger Mode (One-Shot Conversion Mode) Operation Timing**



### 11.6.3 Hardware trigger no-wait mode (sequential conversion mode)

- <1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.
- <2> After the software counts up to the stabilization wait time (1.0  $\mu$ s), the ADCS bit of the ADM0 register is set to 1 to place the system in the hardware trigger standby status (and conversion does not start at this stage). Note that, while in this status, A/D conversion does not start even if ADCS is set to 1.
- <3> If a hardware trigger is input while ADCS = 1, A/D conversion is performed on the analog input specified by the analog input channel specification register (ADS).
- <4> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated. After A/D conversion ends, the next A/D conversion immediately starts.
- <5> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.
- <6> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.
- <7> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.
- <8> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status. However, the A/D converter does not stop in this status.
- <9> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCS = 0, inputting a hardware trigger is ignored and A/D conversion does not start.

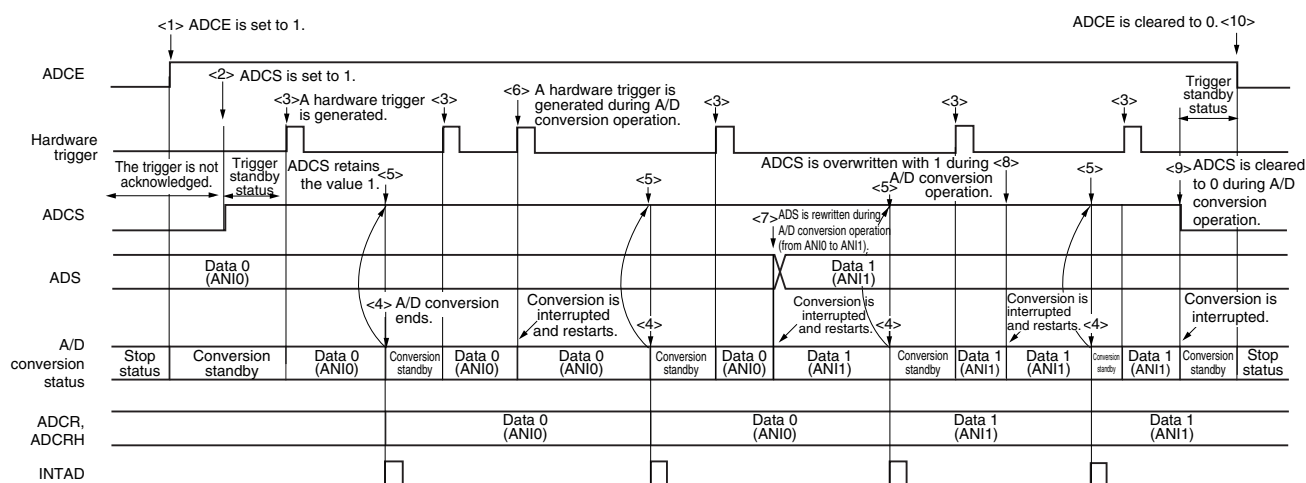
**Figure 11-22. Example of Hardware Trigger No-Wait Mode (Sequential Conversion Mode) Operation Timing**



### 11.6.4 Hardware trigger no-wait mode (one-shot conversion mode)

- <1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.
- <2> After the software counts up to the stabilization wait time (1.0  $\mu$ s), the ADCS bit of the ADM0 register is set to 1 to place the system in the hardware trigger standby status (and conversion does not start at this stage). Note that, while in this status, A/D conversion does not start even if ADCS is set to 1.
- <3> If a hardware trigger is input while ADCS = 1, A/D conversion is performed on the analog input specified by the analog input channel specification register (ADS).
- <4> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated.
- <5> After A/D conversion ends, the ADCS bit remains set to 1, and the system enters the A/D conversion standby status.
- <6> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.
- <7> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.
- <8> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.
- <9> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status. However, the A/D converter does not stop in this status.
- <10> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCS = 0, inputting a hardware trigger is ignored and A/D conversion does not start.

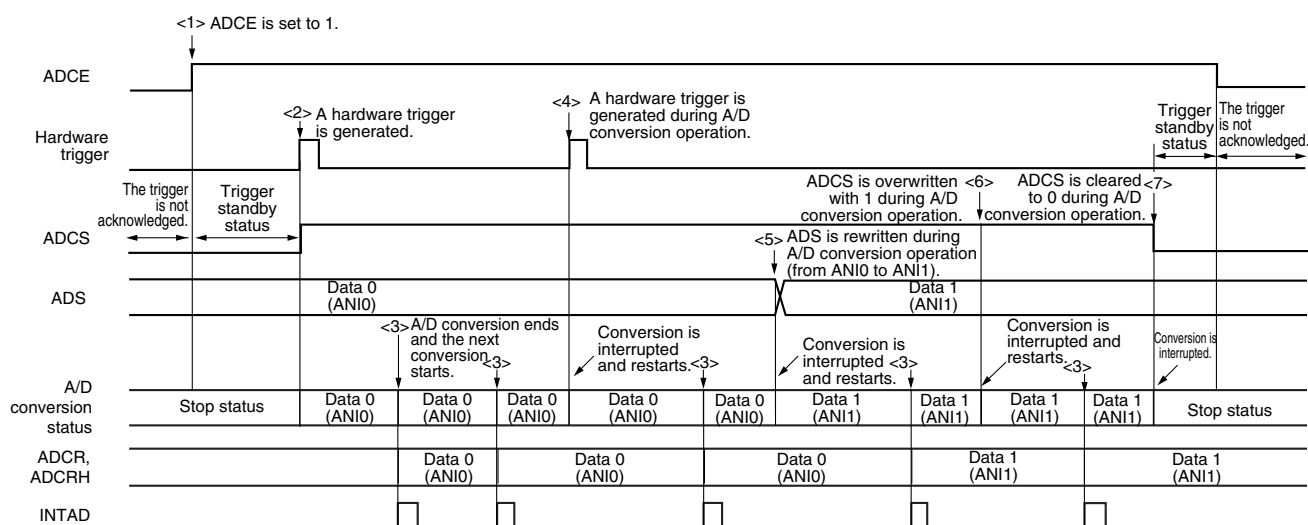
**Figure 11-23. Example of Hardware Trigger No-Wait Mode (One-Shot Conversion Mode) Operation Timing**



### 11.6.5 Hardware trigger wait mode (sequential conversion mode)

- <1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the hardware trigger standby status.
- <2> If a hardware trigger is input while in the hardware trigger standby status, A/D conversion is performed on the analog input specified by the analog input channel specification register (ADS). The ADCS bit of the ADM0 register is automatically set to 1 according to the hardware trigger input.
- <3> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated. After A/D conversion ends, the next A/D conversion immediately starts. (At this time, no hardware trigger is necessary.)
- <4> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.
- <5> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.
- <6> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.
- <7> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, the system enters the hardware trigger standby status, and the A/D converter enters the stop status. When ADCE = 0, inputting a hardware trigger is ignored and A/D conversion does not start.

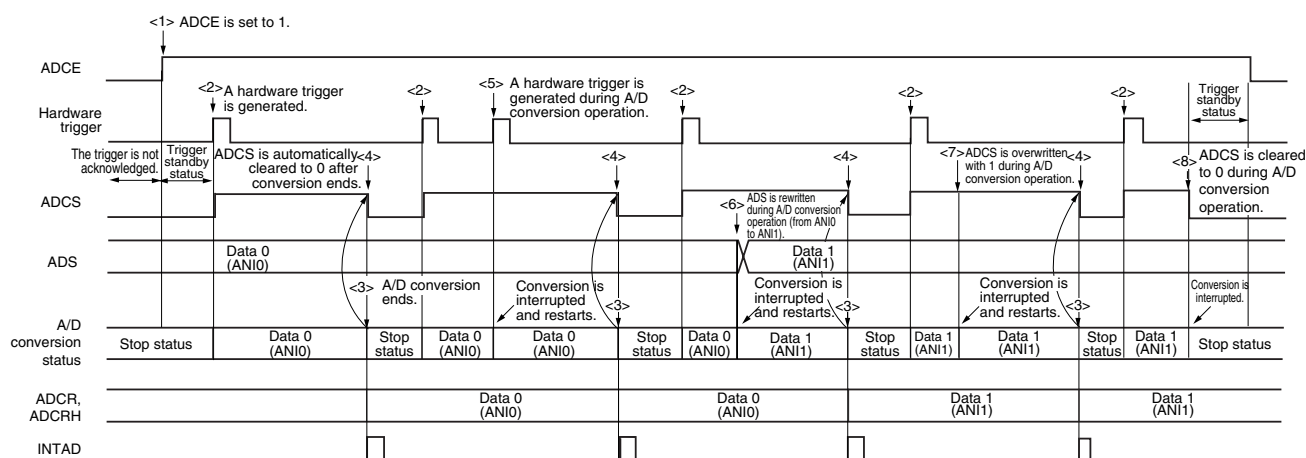
**Figure 11-24. Example of Hardware Trigger Wait Mode (Sequential Conversion Mode) Operation Timing**



### 11.6.6 Hardware trigger wait mode (one-shot conversion mode)

- <1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the hardware trigger standby status.
- <2> If a hardware trigger is input while in the hardware trigger standby status, A/D conversion is performed on the analog input specified by the analog input channel specification register (ADS). The ADCS bit of the ADM0 register is automatically set to 1 according to the hardware trigger input.
- <3> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated.
- <4> After A/D conversion ends, the ADCS bit is automatically cleared to 0, and the A/D converter enters the stop status.
- <5> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.
- <6> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.
- <7> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is initialized.
- <8> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, the system enters the hardware trigger standby status, and the A/D converter enters the stop status. When ADCE = 0, inputting a hardware trigger is ignored and A/D conversion does not start.

**Figure 11-25. Example of Hardware Trigger Wait Mode (One-Shot Conversion Mode) Operation Timing**



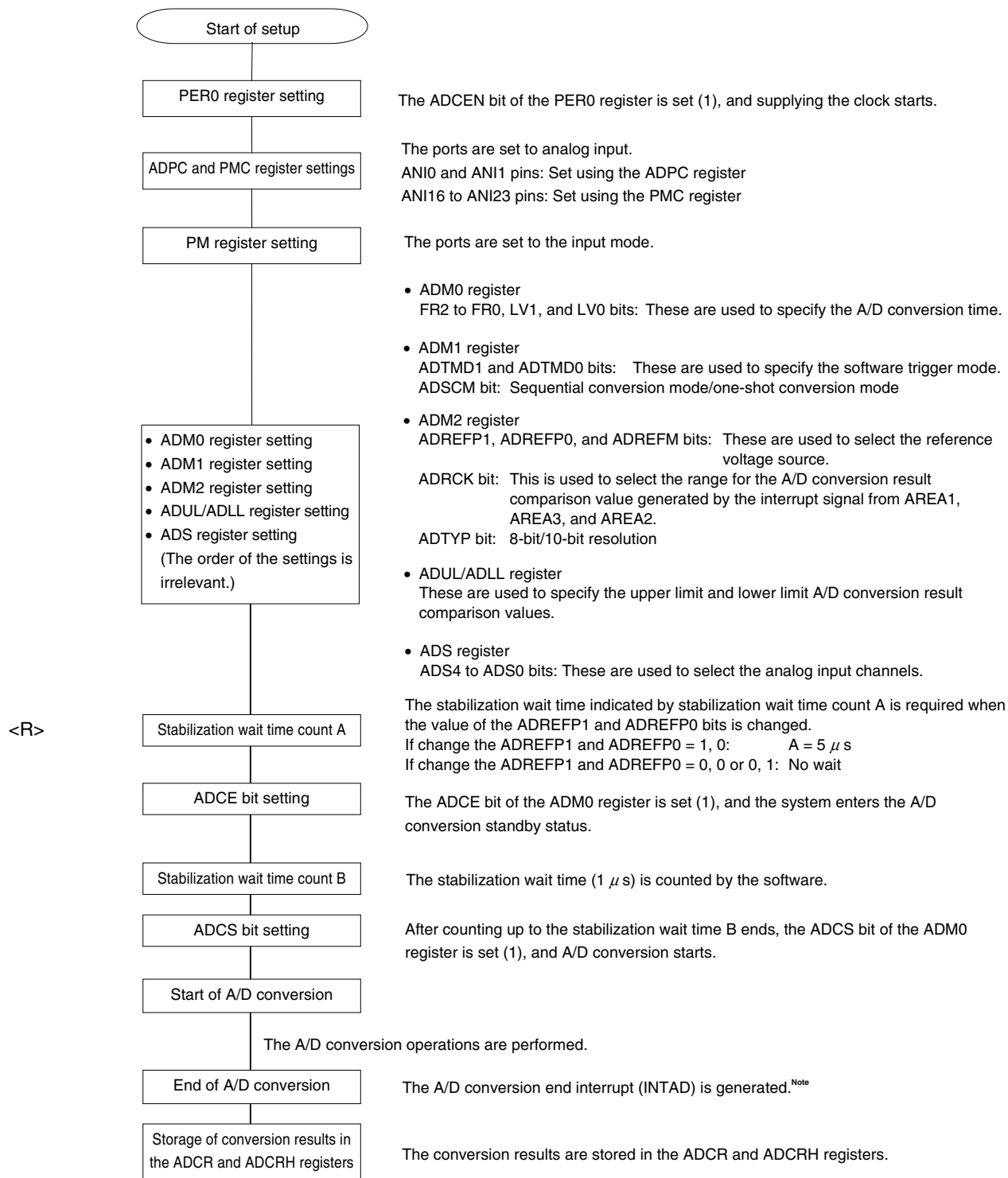
### 11.7 A/D Converter Setup Flowchart

The A/D converter setup flowchart in each operation mode is described below.



## 11.7.1 Setting up software trigger mode

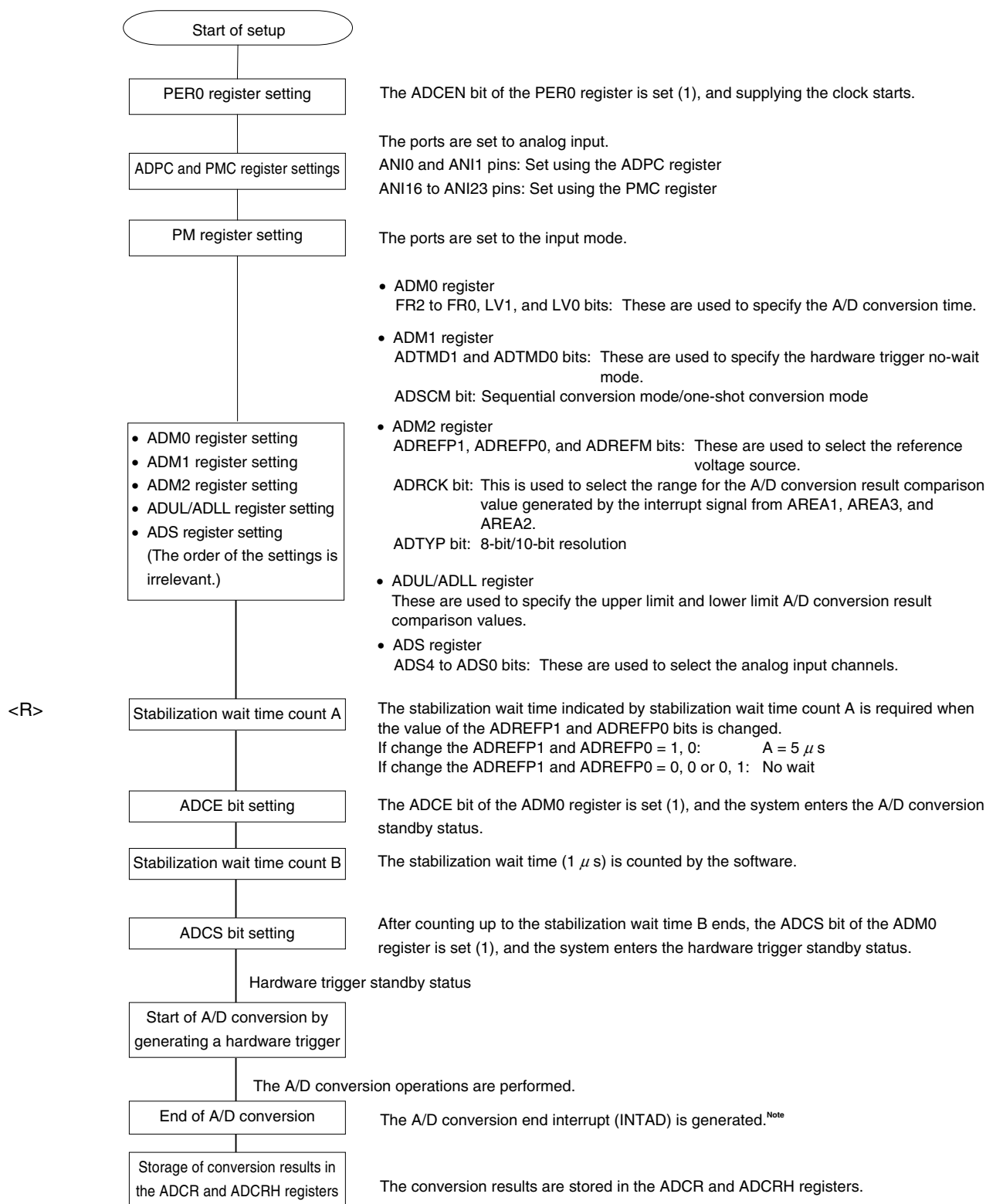
Figure 11-26. Setting up Software Trigger Mode



**Note** Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH registers.

## 11.7.2 Setting up hardware trigger no-wait mode

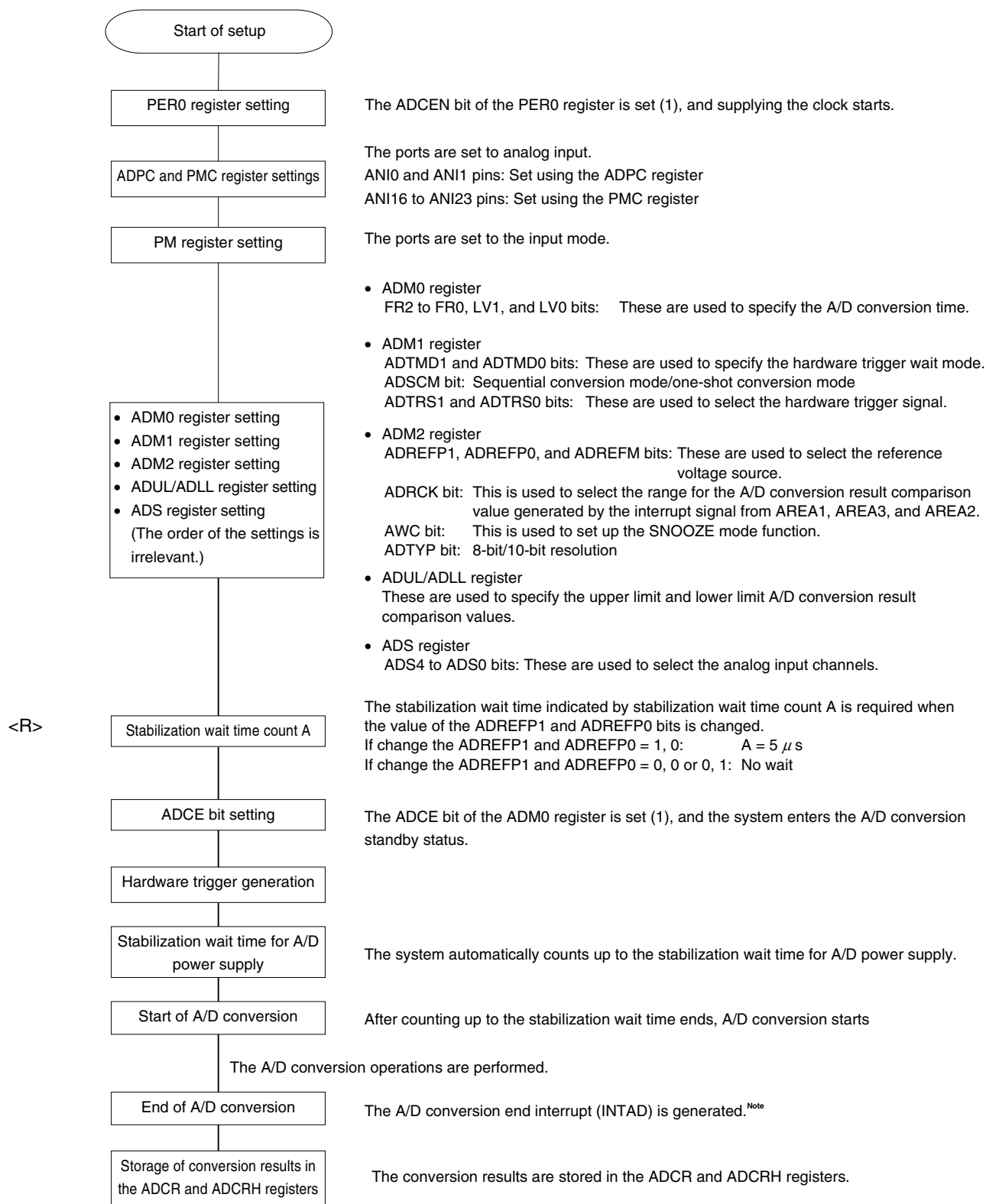
Figure 11-27. Setting up Hardware Trigger No-Wait Mode



**Note** Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH registers.

## 11.7.3 Setting up hardware trigger wait mode

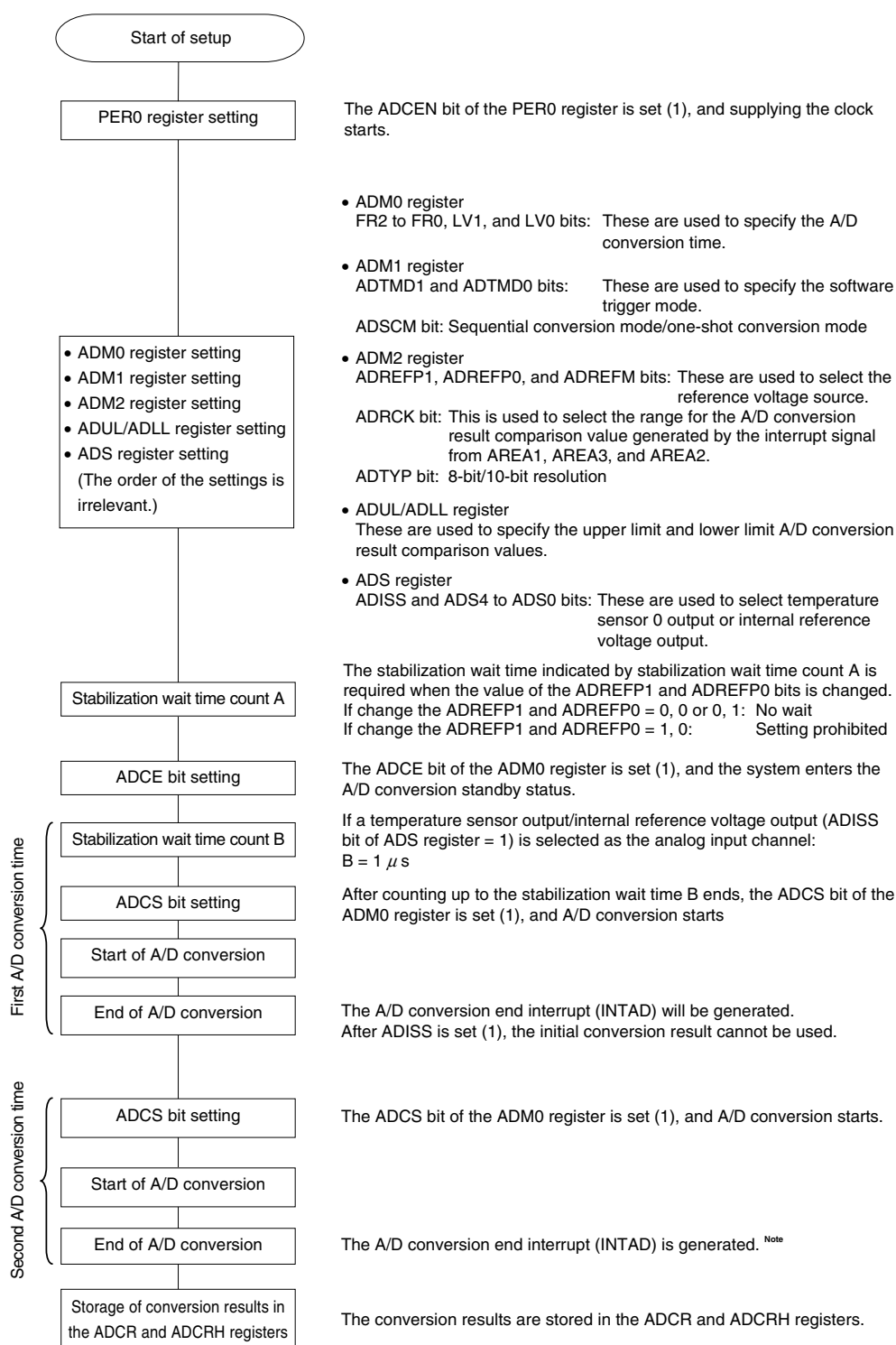
Figure 11-28. Setting up Hardware Trigger Wait Mode



**Note** Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH registers.

### 11.7.4 Setup when temperature sensor output/internal reference voltage output is selected (example for software trigger mode and one-shot conversion mode)

<R> **Figure 11-29. Setup when temperature sensor output/internal reference voltage output is selected**

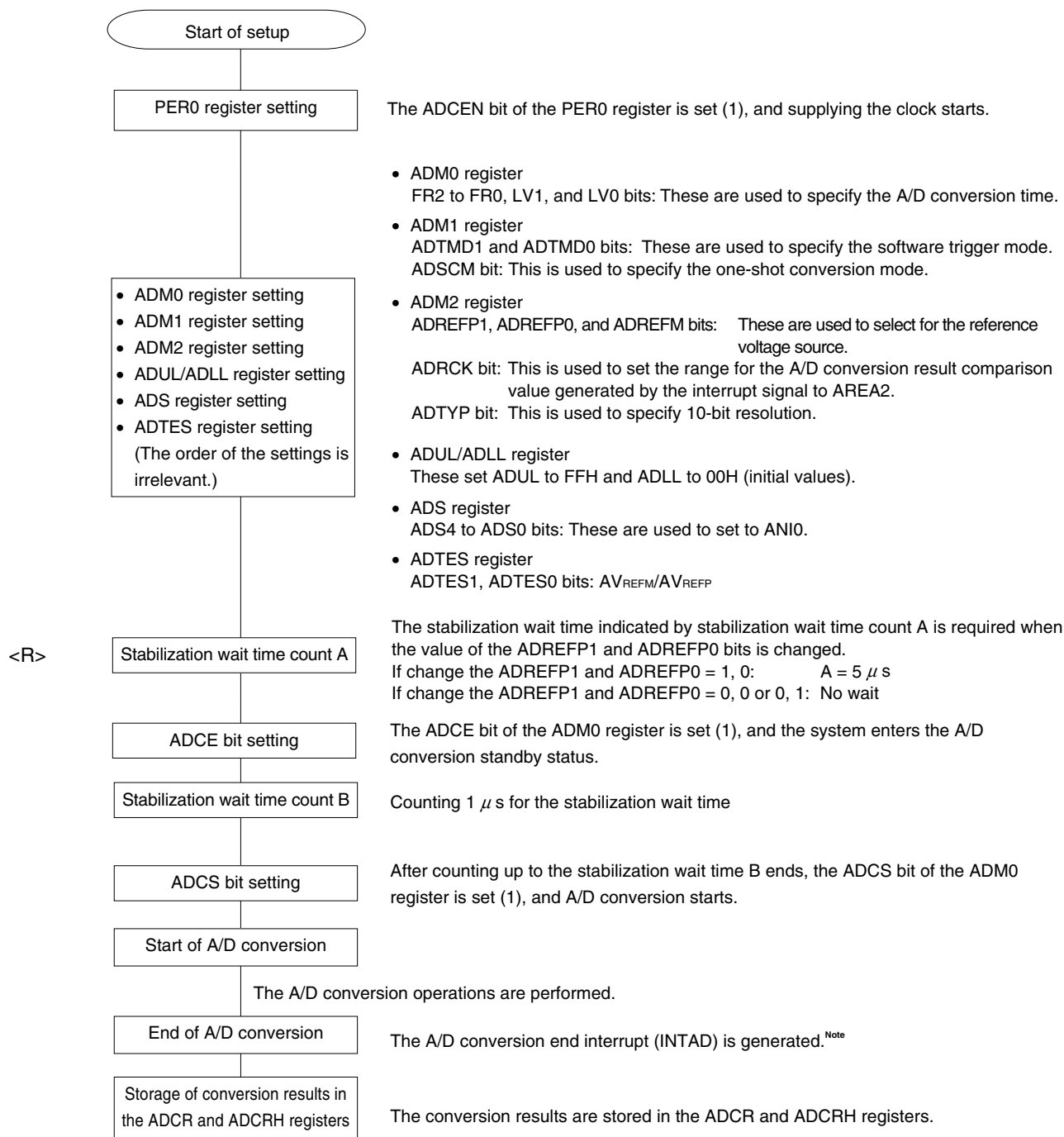


**Note** Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH registers.

**Caution** This setting can be used only in HS (high-speed main) mode.

## 11.7.5 Setting up test mode

Figure 11-30. Setting up Test Trigger Mode



**Note** Depending on the settings of the ADRCCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH registers.

## 11.8 SNOOZE Mode Function

In the SNOOZE mode, A/D conversion is triggered by inputting a hardware trigger in the STOP mode. Normally, A/D conversion is stopped while in the STOP mode, but, by using the SNOOZE mode, A/D conversion can be performed without operating the CPU by inputting a hardware trigger. This is effective for reducing the operation current.

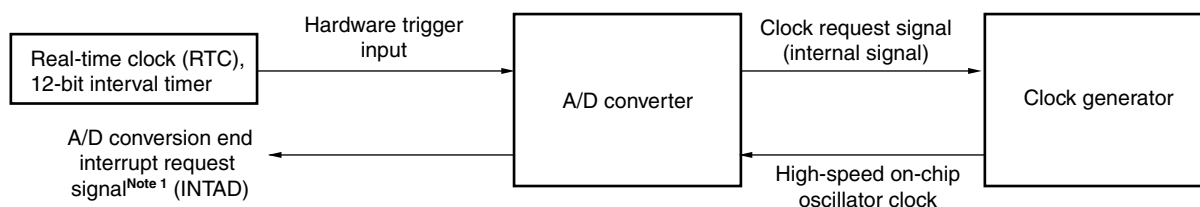
<R> If the A/D conversion result range is specified using the ADUL and ADLL registers, A/D conversion results can be judged at a certain interval of time in SNOOZE mode. Using this function enables power supply voltage monitoring and input key judgment based on A/D inputs.

In the SNOOZE mode, only the following two conversion modes can be used:

- Hardware trigger wait mode (one-shot conversion mode)

**Caution** That the SNOOZE mode can only be specified when the high-speed on-chip oscillator clock is selected for  $f_{CLK}$ .

Figure 11-31. Block Diagram When Using SNOOZE Mode Function



When using the SNOOZE mode function, the initial setting of each register is specified before switching to the STOP mode. (For details about these settings, see 11.7.3 **Setting up hardware trigger wait mode**<sup>Note 2</sup>.) Just before move to STOP mode, bit 2 (AWC) of A/D converter mode register 2 (ADM2) is set to 1. After the initial settings are specified, bit 0 (ADCE) of A/D converter mode register 0 (ADM0) is set to 1.

If a hardware trigger is input after switching to the STOP mode, the high-speed on-chip oscillator clock is supplied to the A/D converter. After supplying this clock, the system automatically counts up to the stabilization wait time, and then A/D conversion starts.

The SNOOZE mode operation after A/D conversion ends differs depending on whether an interrupt signal is generated<sup>Note 1</sup>.

- Notes**
1. Depending on the setting of the A/D conversion result comparison function (ADRCK bit, ADUL/ADLL register), there is a possibility of no interrupt signal being generated.
  2. Be sure to set the ADM1 register to E2H or E3H.

**Caution** The A/D converter's internal voltage cannot be used in SNOOZE mode.

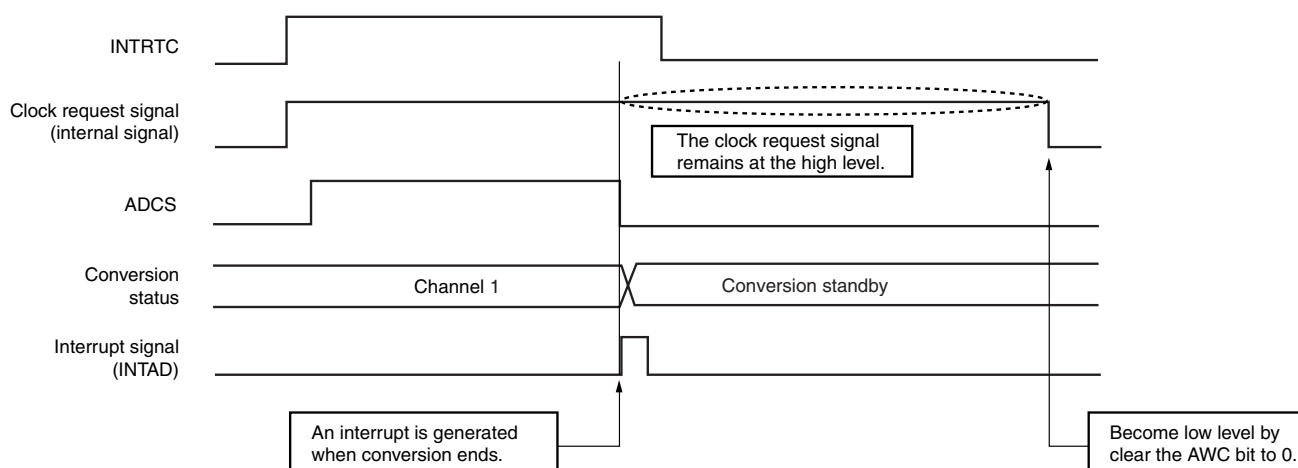
**Remark** The hardware trigger is INTRTC and INTIT.  
Specify the hardware trigger by using the A/D Converter Mode Register 1 (ADM1).

**(1) If an interrupt is generated after A/D conversion ends**

If the A/D conversion result value is inside the range of values specified by the A/D conversion result comparison function (which is set up by using the ADRCK bit and ADUL/ADLL register), the A/D conversion end interrupt request signal (INTAD) is generated.

<R> When A/D conversion ends and an A/D conversion end interrupt request signal (INTAD) is generated, the A/D converter returns to normal operation mode from SNOOZE mode. At this time, be sure to clear bit 2 (AWC = 0: SNOOZE mode release) of the A/D converter mode register 2 (ADM2). If the AWC bit is left set to 1, A/D conversion will not start normally in the subsequent SNOOZE or normal operation mode.

**Figure 11-32. Operation Example When Interrupt Is Generated After A/D Conversion Ends**

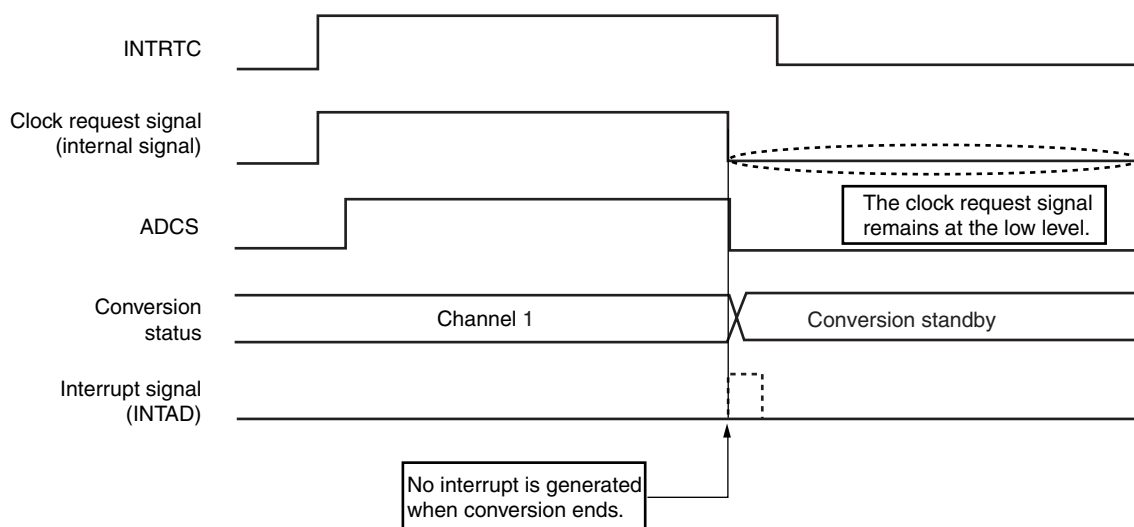


**(2) If no interrupt is generated after A/D conversion ends**

If the A/D conversion result value is outside the range of values specified by the A/D conversion result comparison function (which is set up by using the ADRCK bit and ADUL/ADLL register), the A/D conversion end interrupt request signal (INTAD) is not generated.

If the A/D conversion end interrupt request signal (INTAD) is not generated after A/D conversion ends, the clock request signal (an internal signal) is automatically set to the low level, and supplying the high-speed on-chip oscillator clock stops. If a hardware trigger is input later, A/D conversion work is again performed in the SNOOZE mode.

**Figure 11-33. Operation Example When No Interrupt Is Generated After A/D Conversion Ends**

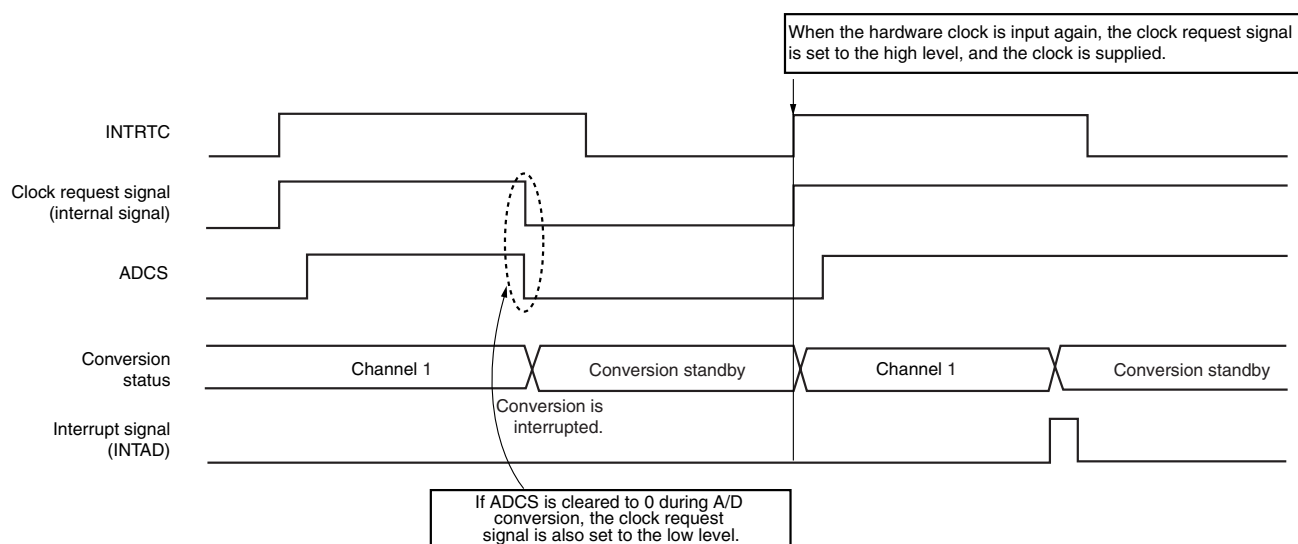




**(3) Operation when A/D conversion is interrupted or resumed**

If A/D conversion is interrupted (by clearing bit 7 (ADCS) of A/D converter mode register 0 (ADM0) to 0), the clock request signal (an internal signal) is set to the low level, and supplying the high-speed on-chip oscillator clock stops. When another hardware trigger is input, the clock request signal is set to the high level, supplying the high-speed on-chip oscillator clock resumes, and A/D conversion starts in the SNOOZE mode.

**Figure 11-34. Example of Operation When A/D Conversion Is Interrupted or Resumed**



## 11.9 How to Read A/D Converter Characteristics Table

Here, special terms unique to the A/D converter are explained.

### (1) Resolution

This is the minimum analog input voltage that can be identified. That is, the percentage of the analog input voltage per bit of digital output is called 1LSB (Least Significant Bit). The percentage of 1LSB with respect to the full scale is expressed by %FSR (Full Scale Range).

1LSB is as follows when the resolution is 10 bits.

$$\begin{aligned} 1\text{LSB} &= 1/2^{10} = 1/1024 \\ &= 0.098\%\text{FSR} \end{aligned}$$

Accuracy has no relation to resolution, but is determined by overall error.

### (2) Overall error

This shows the maximum error value between the actual measured value and the theoretical value.

Zero-scale error, full-scale error, integral linearity error, and differential linearity errors that are combinations of these express the overall error.

Note that the quantization error is not included in the overall error in the characteristics table.

### (3) Quantization error

When analog values are converted to digital values, a  $\pm 1/2\text{LSB}$  error naturally occurs. In an A/D converter, an analog input voltage in a range of  $\pm 1/2\text{LSB}$  is converted to the same digital code, so a quantization error cannot be avoided.

Note that the quantization error is not included in the overall error, zero-scale error, full-scale error, integral linearity error, and differential linearity error in the characteristics table.

Figure 11-35. Overall Error

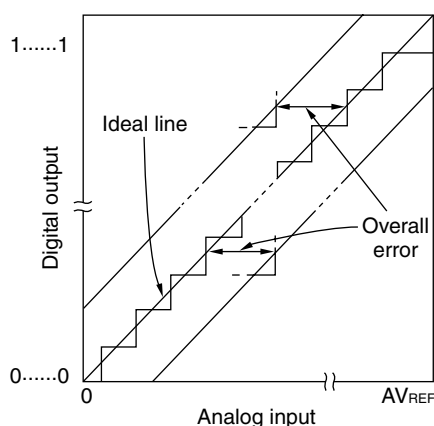
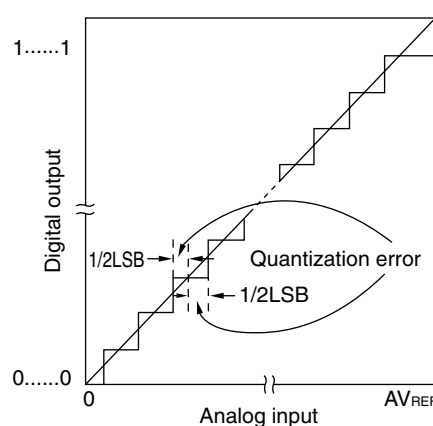


Figure 11-36. Quantization Error



### (4) Zero-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value ( $1/2\text{LSB}$ ) when the digital output changes from 0.....000 to 0.....001.

If the actual measurement value is greater than the theoretical value, it shows the difference between the actual measurement value of the analog input voltage and the theoretical value ( $3/2\text{LSB}$ ) when the digital output changes from 0.....001 to 0.....010.

**(5) Full-scale error**

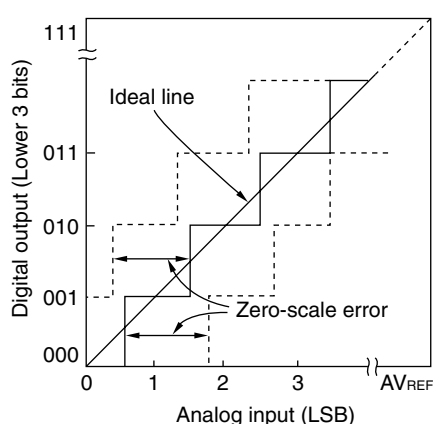
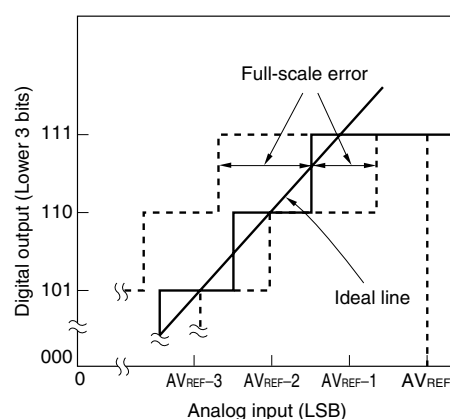
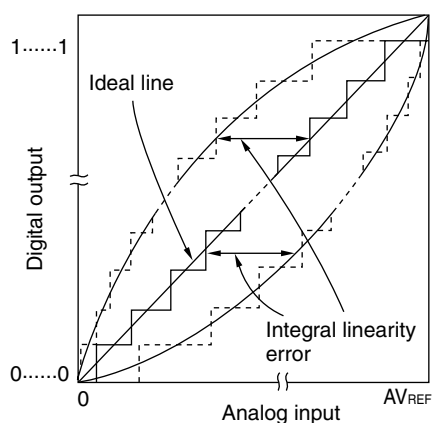
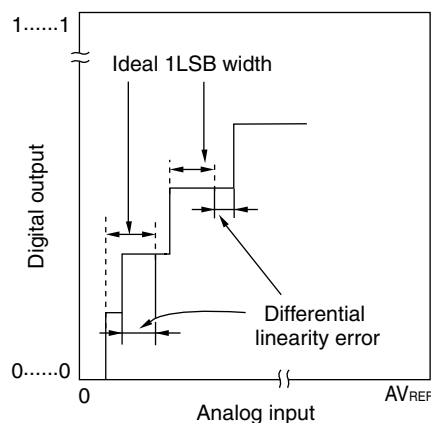
This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (Full-scale – 3/2LSB) when the digital output changes from 1.....110 to 1.....111.

**(6) Integral linearity error**

This shows the degree to which the conversion characteristics deviate from the ideal linear relationship. It expresses the maximum value of the difference between the actual measurement value and the ideal straight line when the zero-scale error and full-scale error are 0.

**(7) Differential linearity error**

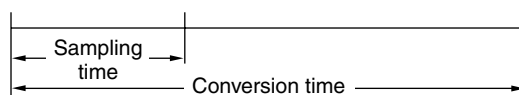
While the ideal width of code output is 1LSB, this indicates the difference between the actual measurement value and the ideal value.

**Figure 11-37. Zero-Scale Error****Figure 11-38. Full-Scale Error****Figure 11-39. Integral Linearity Error****Figure 11-40. Differential Linearity Error****(8) Conversion time**

This expresses the time from the start of sampling to when the digital output is obtained. The sampling time is included in the conversion time in the characteristics table.

**(9) Sampling time**

This is the time the analog switch is turned on for the analog voltage to be sampled by the sample & hold circuit.



## 11.10 Cautions for A/D Converter

### (1) Operating current in STOP mode

Shift to STOP mode after stopping the A/D converter (by setting bit 7 (ADCS) of A/D converter mode register 0 (ADM0) to 0). The operating current can be reduced by setting bit 0 (ADCE) of the ADM0 register to 0 at the same time.

To restart from the standby status, clear bit 0 (ADIF) of interrupt request flag register 1H (IF1H) to 0 and start operation.

### (2) Input range of ANI0, ANI1 and ANI16 to ANI23 pins

Observe the rated range of the ANI0, ANI1 and ANI16 to ANI23 pins input voltage. If a voltage of  $V_{DD}$  and  $AV_{REFP}$  or higher and  $V_{SS}$  and  $AV_{REFM}$  or lower (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

When internal reference voltage (1.45 V) is selected reference voltage source for the + side of the A/D converter, do not input internal reference voltage or higher voltage to a pin selected by the ADS register. However, it is no problem that a pin not selected by the ADS register is inputted voltage greater than the internal reference voltage.

<R> **Caution Internal reference voltage (1.45 V) can be used only in HS (high-speed main) mode.**

### (3) Conflicting operations

<1> Conflict between the A/D conversion result register (ADCR, ADCRH) write and the ADCR or ADCRH register read by instruction upon the end of conversion

The ADCR or ADCRH register read has priority. After the read operation, the new conversion result is written to the ADCR or ADCRH registers.

<2> Conflict between the ADCR or ADCRH register write and the A/D converter mode register 0 (ADM0) write, the analog input channel specification register (ADS), or A/D port configuration register (ADPC) write upon the end of conversion

The ADM0, ADS, or ADPC registers write has priority. The ADCR or ADCRH register write is not performed, nor is the conversion end interrupt signal (INTAD) generated.

### (4) Noise countermeasures

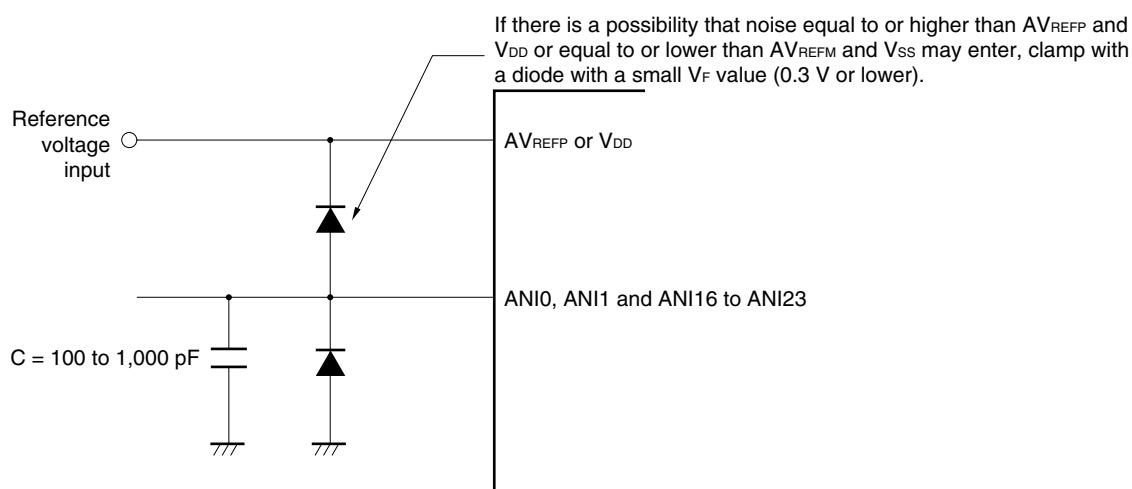
To maintain the 10-bit resolution, attention must be paid to noise input to the  $AV_{REFP}$ ,  $V_{DD}$ , ANI0, ANI1 and ANI16 to ANI23 pins.

<1> Connect a capacitor with a low equivalent resistance and a good frequency response to the power supply.

<2> The higher the output impedance of the analog input source, the greater the influence. To reduce the noise, connecting external C as shown in Figure 11-41 is recommended.

<3> Do not switch these pins with other pins during conversion.

<4> The accuracy is improved if the HALT mode is set immediately after the start of conversion.

**Figure 11-41. Analog Input Pin Connection****(5) Analog input (ANIn) pins**

- <1> The analog input pins (ANI0 and ANI1) are also used as input port pins (P20 and P21). When A/D conversion is performed with any of the ANI0 and ANI1 pins selected, do not change to output value P20 and P21 while conversion is in progress; otherwise the conversion resolution may be degraded.
- <2> If a pin adjacent to a pin that is being A/D converted is used as a digital I/O port pin, the A/D conversion result might differ from the expected value due to a coupling noise. Be sure to prevent such a pulse from being input or output.

**(6) Input impedance of analog input (ANIn) pins**

This A/D converter charges a sampling capacitor for sampling during sampling time.

Therefore, only a leakage current flows when sampling is not in progress, and a current that charges the capacitor flows during sampling. Consequently, the input impedance fluctuates depending on whether sampling is in progress, and on the other states.

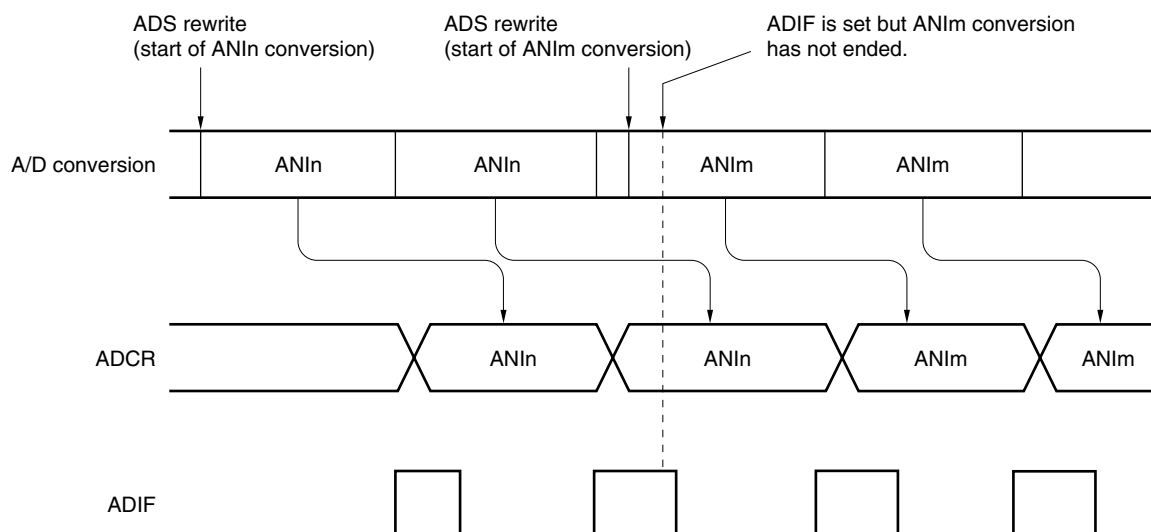
To make sure that sampling is effective, however, it is recommended to keep the output impedance of the analog input source to within 1 kΩ, and to connect a capacitor of about 100 pF to the ANI0, ANI1 and ANI16 to ANI23 pins (see **Figure 11-41**).

**(7) Interrupt request flag (ADIF)**

The interrupt request flag (ADIF) is not cleared even if the analog input channel specification register (ADS) is changed.

Therefore, if an analog input pin is changed during A/D conversion, the A/D conversion result and ADIF flag for the pre-change analog input may be set just before the ADS register rewrite. Caution is therefore required since, at this time, when ADIF flag is read immediately after the ADS register rewrite, ADIF flag is set despite the fact A/D conversion for the post-change analog input has not ended.

When A/D conversion is stopped and then resumed, clear ADIF flag before the A/D conversion operation is resumed.

**Figure 11-42. Timing of A/D Conversion End Interrupt Request Generation****(8) Conversion results just after A/D conversion start**

In software trigger mode and hardware trigger no-wait mode, if the ADCE bit is set to 1 and then the ADCS bit is set to 1 before the stabilization time (1.0  $\mu$ s) elapses, the A/D conversion value immediately after A/D conversion starts might not satisfy the ratings. In this case, take measures such as polling the A/D conversion end interrupt request signal (INTAD) and discarding the first conversion result.

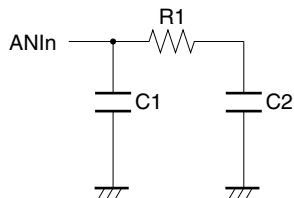
**(9) A/D conversion result register (ADCR, ADCRH) read operation**

When a write operation is performed to A/D converter mode register 0 (ADM0), analog input channel specification register (ADS), A/D port configuration register (ADPC), and port mode control register (PMC), the contents of the ADCR and ADCRH registers may become undefined. Read the conversion result following conversion completion before writing to the ADM0, ADS, ADPC, or PMC register. Using a timing other than the above may cause an incorrect conversion result to be read.

**(10) Internal equivalent circuit**

The equivalent circuit of the analog input block is shown below.

**Figure 11-43. Internal Equivalent Circuit of ANIn Pin**



<R>

**Table 11-6. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)**

| $AV_{REFP}, V_{DD}$                          | ANIn Pins      | R1 [kΩ] | C1 [pF] | C2 [pF] |
|----------------------------------------------|----------------|---------|---------|---------|
| $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | ANI0 and ANI1  | 14      | 8       | 2.5     |
|                                              | ANI16 to ANI23 | 18      | 8       | 7.0     |
| $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | ANI0 and ANI1  | 39      | 8       | 2.5     |
|                                              | ANI16 to ANI23 | 53      | 8       | 7.0     |
| $1.8\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ | ANI0 and ANI1  | 231     | 8       | 2.5     |
|                                              | ANI16 to ANI23 | 321     | 8       | 7.0     |
| $1.6\text{ V} \leq V_{DD} < 2.7\text{ V}$    | ANI0 and ANI1  | 632     | 8       | 2.5     |
|                                              | ANI16 to ANI23 | 902     | 8       | 7.0     |

**Caution** The A/D converter's internal voltage cannot be used in SNOOZE mode.

**Remark** The resistance and capacitance values shown in Table 11-6 are not guaranteed values.

**(11) Starting the A/D converter**

Start the A/D converter after the  $AV_{REFP}$  and  $V_{DD}$  voltages stabilize.

## CHAPTER 12 SERIAL ARRAY UNIT

Serial array unit has two serial channels. Each channel can achieve 3-wire serial (CSI), and UART. Function assignment of each channel supported by the RL78/L12 is as shown below.

| Channel | Used as CSI | Used as UART               |
|---------|-------------|----------------------------|
| 0       | CSI00       | UART0 (supporting LIN-bus) |
| 1       | CSI01       |                            |

### 12.1 Functions of Serial Array Unit

Each serial interface supported by the RL78/L12 has the following features.

#### 12.1.1 3-wire serial I/O (CSI00, CSI01)

Data is transmitted or received in synchronization with the serial clock ( $\overline{\text{SCK}}$ ) output from the master channel.

3-wire serial communication is clocked communication performed by using three communication lines: one for the serial clock ( $\overline{\text{SCK}}$ ), one for transmitting serial data (SO), one for receiving serial data (SI).

For details about the settings, see **12.5 Operation of 3-Wire Serial I/O (CSI00, CSI01) Communication**.

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

[Clock control]

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate

<R> During master communication (CSI00): Max.  $f_{\text{MCK}}/2$  <sup>Notes 1, 2</sup>  
 During master communication (other than CSI00): Max.  $f_{\text{MCK}}/4$  <sup>Note 2</sup>  
 During slave communication: Max.  $f_{\text{MCK}}/6$  <sup>Note 2</sup>

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

In addition, CSI00 supports the SNOOZE mode. When  $\overline{\text{SCK}}$  input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible.

- <R> **Notes 1.** In master communication (CSI00), maximum transfer rate become  $f_{\text{MCK}}/2$  when the following conditions.
- $2.7\text{ V} \leq \text{EV}_{\text{DD}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$
  - $f_{\text{MCK}} \leq 12\text{ MHz}$
- Other cases, maximum transfer rate become  $f_{\text{MCK}}/4$ .
- 2.** Use the clocks within a range satisfying the  $\overline{\text{SCK}}$  cycle time ( $t_{\text{CKCY}}$ ) characteristics (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS**).



### 12.1.2 UART (UART0)

This is a start-stop synchronization function using two lines: serial data transmission (TxD) and serial data reception (RxD) lines. By using these two communication lines, each data frame, which consist of a start bit, data, parity bit, and stop bit, is transferred asynchronously (using the internal baud rate) between the microcontroller and the other communication party. Full-duplex UART communication can be performed by using a channel dedicated to transmission (even-numbered channel) and a channel dedicated to reception (odd-numbered channel). The LIN-bus can be implemented by using timer array unit with an external interrupt (INTP0).

For details about the settings, see **12.6 Operation of UART (UART0) Communication**.

[Data transmission/reception]

- Data length of 7, 8, or 9 bits
- Select the MSB/LSB first
- Level setting of transmit/receive data and select of reverse
- Parity bit appending and parity check functions
- Stop bit appending

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt
- Error interrupt in case of framing error, parity error, or overrun error

[Error detection flag]

- Framing error, parity error, or overrun error

In addition, UART0 supports the SNOOZE mode. When RxD input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible.

The LIN-bus is accepted in UART0 (0 and 1 channels).

[LIN-bus functions]

- Wakeup signal detection
- Break field (BF) detection
- Sync field measurement, baud rate calculation

} Using the external interrupt (INTP0) and timer array unit

## 12.2 Configuration of Serial Array Unit

The serial array unit includes the following hardware.

**Table 12-1. Configuration of Serial Array Unit**

| Item               | Configuration                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Shift register     | 9 bits                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| Buffer register    | Lower 9 bits of serial data register mn (SDRmn) <sup>Note</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| Serial clock I/O   | SCK00, SCK01 pins (for 3-wire serial I/O)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| Serial data input  | SI00, SI01 pins (for 3-wire serial I/O), RxD0 pin (for UART supporting LIN-bus)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| Serial data output | SO00, SO01 pins (for 3-wire serial I/O), TxD0 pin (for UART supporting LIN-bus), output controller                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Control registers  | <div> <div>&lt;Registers of unit setting block&gt;</div> <ul style="list-style-type: none"> <li>• Peripheral enable register 0 (PER0)</li> <li>• Serial clock select register m (SPSm)</li> <li>• Serial channel enable status register m (SEm)</li> <li>• Serial channel start register m (SSm)</li> <li>• Serial channel stop register m (STm)</li> <li>• Serial output enable register m (SOEm)</li> <li>• Serial output register m (SOM)</li> <li>• Serial output level register m (SOLm)</li> <li>• Serial standby control register m (SSCm)</li> <li>• Input switch control register (ISC)</li> <li>• Noise filter enable register 0 (NFEN0)</li> </ul> </div> <div> <div>&lt;Registers of each channel&gt;</div> <ul style="list-style-type: none"> <li>• Serial data register mn (SDRmn)</li> <li>• Serial mode register mn (SMRmn)</li> <li>• Serial communication operation setting register mn (SCRmn)</li> <li>• Serial status register mn (SSRmn)</li> <li>• Serial flag clear trigger register mn (SIRmn)</li> </ul> </div> <div> <ul style="list-style-type: none"> <li>• Port input mode register 1 (PIM1)</li> <li>• Port output mode register 1 (POM1)</li> <li>• LCD port function registers 0, 3 (PFSEG0, PFSEG3)</li> <li>• Port mode register 1 (PM1)</li> <li>• Port register 1 (P1)</li> </ul> </div> |

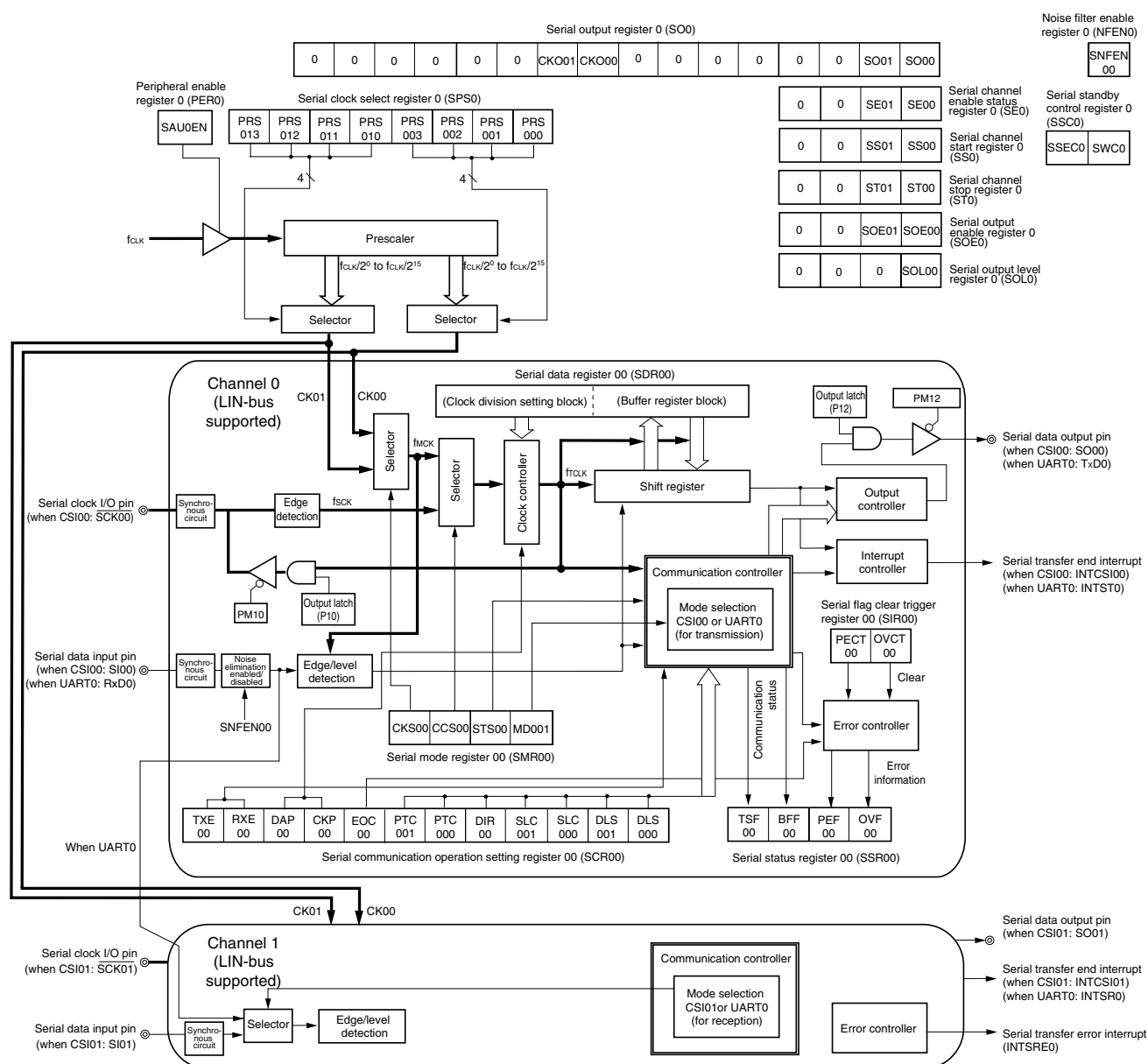
**Note** The lower 8 bits of serial data register mn (SDRmn) can be read or written as the following SFR, depending on the communication mode.

- CSIp communication ... SIOp (CSIp data register)
- UARTq reception ... RXDq (UARTq receive data register)
- UARTq transmission ... TXDq (UARTq transmit data register)

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01),  
q: UART number (q = 0)

Figure 12-1 shows the block diagram of the serial array unit.

**Figure 12-1. Block Diagram of Serial Array Unit**



### 12.2.1 Shift register

This is a 9-bit register that converts parallel data into serial data or vice versa.

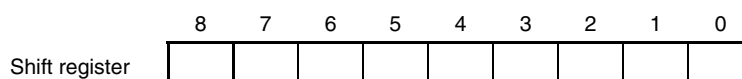
In case of the UART communication of nine bits of data, nine bits (bits 0 to 8) are used.

During reception, it converts data input to the serial pin into parallel data.

When data is transmitted, the value set to this register is output as serial data from the serial output pin.

The shift register cannot be directly manipulated by program.

To read or write the shift register, use the lower 9 bits of serial data register mn (SDRmn).



### 12.2.2 Lower 9 bits of the serial data register mn (SDRmn)

The SDRmn register is the transmit/receive data register (16 bits) of channel n. Bits 8 to 0 (lower 9 bits) function as a transmit/receive buffer register, and bits 15 to 9 are used as a register that sets the division ratio of the operation clock ( $f_{MCK}$ ).

When data is received, parallel data converted by the shift register is stored in the lower 9 bits. When data is to be transmitted, set transmit to be transferred to the shift register to the lower 9 bits.

The data stored in the lower 9 bits of this register is as follows, depending on the setting of bits 0 and 1 (DLSmn0, DLSmn1) of serial communication operation setting register mn (SCRmn), regardless of the output sequence of the data.

- 7-bit data length (stored in bits 0 to 6 of SDRmn register)
- 8-bit data length (stored in bits 0 to 7 of SDRmn register)
- 9-bit data length (stored in bits 0 to 8 of SDRmn register) (settable in UART0 mode only)

The SDRmn register can be read or written in 16-bit units.

The lower 8 bits of the SDRmn register can be read or written <sup>Note</sup> as the following SFR, depending on the communication mode.

- CSIp communication ... SIOp (CSIp data register)
- UARTq reception ... RXDq (UARTq receive data register)
- UARTq transmission ... TXDq (UARTq transmit data register)

Reset signal generation clears the SDRmn register to 0000H.

**Note** Writing in 8-bit units is prohibited when the operation is stopped (SEmn = 0).

**Remarks 1.** After data is received, "0" is stored in bits 0 to 8 in bit portions that exceed the data length.

- 2.** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01),  
q: UART number (q = 0)

**Figure 12-2. Format of Serial Data Register mn (SDRmn) (mn = 00, 01)**

Address: FFF10H, FFF11H (SDR00), FFF12H, FFF13H (SDR01)

After reset: 0000H R/W



**Remark** For the function of the higher 7 bits of the SDRmn register, see **12.3 Registers Controlling Serial Array Unit**.

### 12.3 Registers Controlling Serial Array Unit

Serial array unit is controlled by the following registers.

- Peripheral enable register 0 (PER0)
- Serial clock select register m (SPSm)
- Serial mode register mn (SMRmn)
- Serial communication operation setting register mn (SCRmn)
- Serial data register mn (SDRmn)
- Serial flag clear trigger register mn (SIRmn)
- Serial status register mn (SSRmn)
- Serial channel start register m (SSm)
- Serial channel stop register m (STm)
- Serial channel enable status register m (SEm)
- Serial output enable register m (SOEm)
- Serial output level register m (SOLm)
- Serial output register m (SOM)
- Serial standby control register m (SSCm)
- Input switch control register (ISC)
- Noise filter enable register 0 (NFEN0)
- Port input mode register 1 (PIM1)
- Port output mode register 1 (POM1)
- LCD port function registers 0, 3 (PFSEG0, PFSEG3)
- Port mode register 1 (PM1)
- Port registers 1 (P1)

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1)

### 12.3.1 Peripheral enable register 0 (PER0)

PER0 is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When serial array unit is used, be sure to set bit 2 (SAU0EN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the PER0 register to 00H.

**Figure 12-3. Format of Peripheral Enable Register 0 (PER0)**

Address: F00F0H After reset: 00H R/W

| Symbol | <7>   | 6 | <5>   | <4>     | 3 | <2>    | 1 | <0>    |
|--------|-------|---|-------|---------|---|--------|---|--------|
| PER0   | RTCEN | 0 | ADCEN | IICA0EN | 0 | SAU0EN | 0 | TAU0EN |

| SAU0EN | Control of serial array unit input clock supply                                                                                                                                       |
|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0      | Stops supply of input clock.<br><ul style="list-style-type: none"> <li>SFR used by serial array unit cannot be written.</li> <li>Serial array unit is in the reset status.</li> </ul> |
| 1      | Enables input clock supply.<br><ul style="list-style-type: none"> <li>SFR used by serial array unit can be read/written.</li> </ul>                                                   |

- Cautions**
- When setting serial array unit, be sure to set the SAU0EN bit to 1 first. If SAU0EN = 0, writing to a control register of serial array unit is ignored, and, even if the register is read, only the default value is read (except for the input switch control register (ISC), noise filter enable register 0 (NFEN0), port input mode register 1 (PIM1), port output mode register 1 (POM1), LCD port function registers 0, 3 (PFSEG0, PFSEG3), port mode register 1 (PM1), and port register 1 (P1)).
  - Be sure to clear bits 1, 3, 6 to "0".

### 12.3.2 Serial clock select register m (SPSm)

The SPSm register is a 16-bit register that is used to select two types of operation clocks (CKm0, CKm1) that are commonly supplied to each channel. CKm1 is selected by bits 7 to 4 of the SPSm register, and CKm0 is selected by bits 3 to 0.

Rewriting the SPSm register is prohibited when the register is in operation (when SEMn = 1).

The SPSm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SPSm register can be set with an 8-bit memory manipulation instruction with SPSmL.

Reset signal generation clears the SPSm register to 0000H.



Figure 12-4. Format of Serial Clock Select Register m (SPSm)

Address: F0126H, F0127H After reset: 0000H R/W

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7          | 6          | 5          | 4          | 3          | 2          | 1          | 0          |
|--------|----|----|----|----|----|----|---|---|------------|------------|------------|------------|------------|------------|------------|------------|
| SPSm   | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | PRS<br>m13 | PRS<br>m12 | PRS<br>m11 | PRS<br>m10 | PRS<br>m03 | PRS<br>m02 | PRS<br>m01 | PRS<br>m00 |

| PRS<br>mk3 | PRS<br>mk2 | PRS<br>mk1 | PRS<br>mk0 |                                   | Section of operation clock (CKmk) <sup>Note 1</sup> |                          |                           |                           |                           |
|------------|------------|------------|------------|-----------------------------------|-----------------------------------------------------|--------------------------|---------------------------|---------------------------|---------------------------|
|            |            |            |            |                                   | f <sub>CLK</sub> = 2 MHz                            | f <sub>CLK</sub> = 5 MHz | f <sub>CLK</sub> = 10 MHz | f <sub>CLK</sub> = 20 MHz | f <sub>CLK</sub> = 24 MHz |
| 0          | 0          | 0          | 0          | f <sub>CLK</sub>                  | 2 MHz                                               | 5 MHz                    | 10 MHz                    | 20 MHz                    | 24 MHz                    |
| 0          | 0          | 0          | 1          | f <sub>CLK</sub> /2               | 1 MHz                                               | 2.5 MHz                  | 5 MHz                     | 10 MHz                    | 12 MHz                    |
| 0          | 0          | 1          | 0          | f <sub>CLK</sub> /2 <sup>2</sup>  | 500 kHz                                             | 1.25 MHz                 | 2.5 MHz                   | 5 MHz                     | 6 MHz                     |
| 0          | 0          | 1          | 1          | f <sub>CLK</sub> /2 <sup>3</sup>  | 250 kHz                                             | 625 kHz                  | 1.25 MHz                  | 2.5 MHz                   | 3 MHz                     |
| 0          | 1          | 0          | 0          | f <sub>CLK</sub> /2 <sup>4</sup>  | 125 kHz                                             | 313 kHz                  | 625 kHz                   | 1.25 MHz                  | 1.5 MHz                   |
| 0          | 1          | 0          | 1          | f <sub>CLK</sub> /2 <sup>5</sup>  | 62.5 kHz                                            | 156 kHz                  | 313 kHz                   | 625 kHz                   | 750 kHz                   |
| 0          | 1          | 1          | 0          | f <sub>CLK</sub> /2 <sup>6</sup>  | 31.3 kHz                                            | 78.1 kHz                 | 156 kHz                   | 313 kHz                   | 375 kHz                   |
| 0          | 1          | 1          | 1          | f <sub>CLK</sub> /2 <sup>7</sup>  | 15.6 kHz                                            | 39.1 kHz                 | 78.1 kHz                  | 156 kHz                   | 187.5 kHz                 |
| 1          | 0          | 0          | 0          | f <sub>CLK</sub> /2 <sup>8</sup>  | 7.81 kHz                                            | 19.5 kHz                 | 39.1 kHz                  | 78.1 kHz                  | 93.8 kHz                  |
| 1          | 0          | 0          | 1          | f <sub>CLK</sub> /2 <sup>9</sup>  | 3.91 kHz                                            | 9.77 kHz                 | 19.5 kHz                  | 39.1 kHz                  | 46.9 kHz                  |
| 1          | 0          | 1          | 0          | f <sub>CLK</sub> /2 <sup>10</sup> | 1.95 kHz                                            | 4.88 kHz                 | 9.77 kHz                  | 19.5 kHz                  | 23.4 kHz                  |
| 1          | 0          | 1          | 1          | f <sub>CLK</sub> /2 <sup>11</sup> | 977 Hz                                              | 2.44 kHz                 | 4.88 kHz                  | 9.77 kHz                  | 11.7 kHz                  |
| 1          | 1          | 0          | 0          | f <sub>CLK</sub> /2 <sup>12</sup> | 488 Hz                                              | 1.22 kHz                 | 2.44 kHz                  | 4.88 kHz                  | 5.86 kHz                  |
| 1          | 1          | 0          | 1          | f <sub>CLK</sub> /2 <sup>13</sup> | 244 Hz                                              | 610 Hz                   | 1.22 kHz                  | 2.44 kHz                  | 2.93 kHz                  |
| 1          | 1          | 1          | 0          | f <sub>CLK</sub> /2 <sup>14</sup> | 122 Hz                                              | 305 Hz                   | 610 Hz                    | 1.22 kHz                  | 1.46 kHz                  |
| 1          | 1          | 1          | 1          | f <sub>CLK</sub> /2 <sup>15</sup> | 61 Hz                                               | 153 kHz                  | 305 Hz                    | 610 Hz                    | 732 Hz                    |

**Note** When changing the clock selected for f<sub>CLK</sub> (by changing the system clock control register (CKC) value), do so after having stopped (serial channel stop register m (STm) = 000FH) the operation of the serial array unit (SAU).

**Caution** Be sure to clear bits 15 to 8 to “0”.

- Remarks**
1. f<sub>CLK</sub>: CPU/peripheral hardware clock frequency  
f<sub>SUB</sub>: Subsystem clock frequency
  2. m: Unit number (m = 0)
  3. k = 0, 1

### 12.3.3 Serial mode register mn (SMRmn)

The SMRmn register is a register that sets an operation mode of channel n. It is also used to select an operation clock ( $f_{MCK}$ ), specify whether the serial clock ( $f_{SCK}$ ) may be input or not, set a start trigger, an operation mode (CSI, or UART), and an interrupt source. This register is also used to invert the level of the receive data only in the UART mode.

Rewriting the SMRmn register is prohibited when the register is in operation (when  $SE_{mn} = 1$ ). However, the MDmn0 bit can be rewritten during operation.

The SMRmn register can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets the SMRmn register to 0020H.

**Figure 12-5. Format of Serial Mode Register mn (SMRmn) (1/2)**

Address: F0110H, F0111H (SMR00), F0112H, F0113H (SMR01) After reset: 0020H R/W

| Symbol | 15        | 14        | 13 | 12 | 11 | 10 | 9 | 8                         | 7 | 6                          | 5 | 4 | 3 | 2 | 1         | 0         |
|--------|-----------|-----------|----|----|----|----|---|---------------------------|---|----------------------------|---|---|---|---|-----------|-----------|
| SMRmn  | CKS<br>mn | CCS<br>mn | 0  | 0  | 0  | 0  | 0 | STS<br>mn <sup>Note</sup> | 0 | SIS<br>mn0 <sup>Note</sup> | 1 | 0 | 0 | 0 | MD<br>mn1 | MD<br>mn0 |

|                                                                                                                                                                                                               |                                                         |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------|
| CKS<br>mn                                                                                                                                                                                                     | Selection of operation clock ( $f_{MCK}$ ) of channel n |
| 0                                                                                                                                                                                                             | Operation clock CKm0 set by the SPSm register           |
| 1                                                                                                                                                                                                             | Operation clock CKm1 set by the SPSm register           |
| Operation clock ( $f_{MCK}$ ) is used by the edge detector. In addition, depending on the setting of the CCSmn bit and the higher 7 bits of the SDRmn register, a transfer clock ( $f_{TCLK}$ ) is generated. |                                                         |

|                                                                                                                                                                                                                                                                                 |                                                                                   |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|
| CCS<br>mn                                                                                                                                                                                                                                                                       | Selection of transfer clock ( $f_{TCLK}$ ) of channel n                           |
| 0                                                                                                                                                                                                                                                                               | Divided operation clock $f_{MCK}$ specified by the CKSmn bit                      |
| 1                                                                                                                                                                                                                                                                               | Clock input $f_{SCK}$ from the $\overline{SCKp}$ pin (slave transfer in CSI mode) |
| Transfer clock $f_{TCLK}$ is used for the shift register, communication controller, output controller, interrupt controller, and error controller. When $CCS_{mn} = 0$ , the division ratio of operation clock ( $f_{MCK}$ ) is set by the higher 7 bits of the SDRmn register. |                                                                                   |

|                                                                                            |                                                                          |
|--------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|
| STS<br>mn                                                                                  | Selection of start trigger source                                        |
| 0                                                                                          | Only software trigger is valid (selected for CSI and UART transmission). |
| 1                                                                                          | Valid edge of the RxDq pin (selected for UART reception)                 |
| Transfer is started when the above source is satisfied after 1 is set to the SSm register. |                                                                          |

**Note** The SMR01 register only.

**Caution** Be sure to clear bits 13 to 6, and 4 to 2 for the SMR00 register, or bits 13 to 9, 7, 4 to 2 for the SMR01 register to “0”. And be sure to set bit 5 to “1”.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01),  
q: UART number (q = 0)

**Figure 12-5. Format of Serial Mode Register mn (SMRmn) (2/2)**

Address: F0110H, F0111H (SMR00), F0112H, F0113H (SMR01) After reset: 0020H R/W

| Symbol | 15        | 14        | 13 | 12 | 11 | 10 | 9 | 8                         | 7 | 6                          | 5 | 4 | 3 | 2 | 1         | 0         |
|--------|-----------|-----------|----|----|----|----|---|---------------------------|---|----------------------------|---|---|---|---|-----------|-----------|
| SMRmn  | CKS<br>mn | CCS<br>mn | 0  | 0  | 0  | 0  | 0 | STS<br>mn <sup>Note</sup> | 0 | SIS<br>mn0 <sup>Note</sup> | 1 | 0 | 0 | 0 | MD<br>mn1 | MD<br>mn0 |

|            |                                                                                                     |
|------------|-----------------------------------------------------------------------------------------------------|
| SIS<br>mn0 | Controls inversion of level of receive data of channel n in UART mode                               |
| 0          | Falling edge is detected as the start bit.<br>The input communication data is captured as is.       |
| 1          | Rising edge is detected as the start bit.<br>The input communication data is inverted and captured. |

|           |                                        |
|-----------|----------------------------------------|
| MD<br>mn1 | Setting of operation mode of channel n |
| 0         | CSI mode                               |
| 1         | UART mode                              |

|                                                                                                                           |                                                                                                            |
|---------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|
| MD<br>mn0                                                                                                                 | Selection of interrupt source of channel n                                                                 |
| 0                                                                                                                         | Transfer end interrupt                                                                                     |
| 1                                                                                                                         | Buffer empty interrupt<br>(Occurs when data is transferred from the SDRmn register to the shift register.) |
| For successive transmission, the next transmit data is written by setting the MDmn0 bit to 1 when SDRmn data has run out. |                                                                                                            |

**Note** The SMR01 register only.**Caution** Be sure to clear bits 13 to 6, and 4 to 2 for the SMR00 register, or bits 13 to 9, 7, 4 to 2 for the SMR01 register to “0”. And be sure to set bit 5 to “1”.**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01),  
q: UART number (q = 0)

### 12.3.4 Serial communication operation setting register mn (SCRmn)

The SCRmn register is a communication operation setting register of channel n. It is used to set a data transmission/reception mode, phase of data and clock, whether an error signal is to be masked or not, parity bit, start bit, stop bit, and data length.

Rewriting the SCRmn register is prohibited when the register is in operation (when SEMn = 1).

The SCRmn register can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets the SCRmn register to 0087H.

**Figure 12-6. Format of Serial Communication Operation Setting Register mn (SCRmn) (1/2)**

Address: F0118H, F0119H (SCR00), F011AH, F011BH (SCR01) After reset: 0087H R/W

| Symbol | 15        | 14        | 13        | 12        | 11 | 10        | 9          | 8          | 7         | 6 | 5                            | 4          | 3 | 2 | 1          | 0          |
|--------|-----------|-----------|-----------|-----------|----|-----------|------------|------------|-----------|---|------------------------------|------------|---|---|------------|------------|
| SCRmn  | TXE<br>mn | RXE<br>mn | DAP<br>mn | CKP<br>mn | 0  | EOC<br>mn | PTC<br>mn1 | PTC<br>mn0 | DIR<br>mn | 0 | SLCm<br>n1 <sup>Note 1</sup> | SLC<br>mn0 | 0 | 1 | DLSm<br>n1 | DLS<br>mn0 |

| TXE<br>mn | RXE<br>mn | Setting of operation mode of channel n |
|-----------|-----------|----------------------------------------|
| 0         | 0         | Disable communication.                 |
| 0         | 1         | Reception only                         |
| 1         | 0         | Transmission only                      |
| 1         | 1         | Transmission/reception                 |

| DAP<br>mn | CKP<br>mn | Selection of data and clock phase in CSI mode | Type |
|-----------|-----------|-----------------------------------------------|------|
| 0         | 0         |                                               | 1    |
| 0         | 1         |                                               | 2    |
| 1         | 0         |                                               | 3    |
| 1         | 1         |                                               | 4    |

Be sure to set DAPmn, CKPmn = 0, 0 in the UART mode.

| EOC<br>mn | Selection of masking of error interrupt signal (INTSREx (x = 0 to 3))                |
|-----------|--------------------------------------------------------------------------------------|
| 0         | Masks error interrupt INTSREx (INTSRx is not masked).                                |
| 1         | Enables generation of error interrupt INTSREx (INTSRx is masked if an error occurs). |

Set EOCmn = 0 in the CSI mode, and during UART transmission<sup>Note 2</sup>.

&lt;R&gt;

- Notes**
1. The SCR00 register only.
  2. When using CSIp not with EOCmn = 0, error interrupt INTSREn may be generated.

**Caution** Be sure to clear the following bits to “0”.

SCR00: bits 11, 6, 3

SCR01: bits 11, 6, 5, 3

Be sure to set bit 2 to “1”.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01)

**Figure 12-6. Format of Serial Communication Operation Setting Register mn (SCRmn) (2/2)**

Address: F0118H, F0119H (SCR00), F011AH, F011BH (SCR01) After reset: 0087H R/W

|        |           |           |           |           |    |           |            |            |           |   |                              |            |   |   |            |            |
|--------|-----------|-----------|-----------|-----------|----|-----------|------------|------------|-----------|---|------------------------------|------------|---|---|------------|------------|
| Symbol | 15        | 14        | 13        | 12        | 11 | 10        | 9          | 8          | 7         | 6 | 5                            | 4          | 3 | 2 | 1          | 0          |
| SCRmn  | TXE<br>mn | RXE<br>mn | DAP<br>mn | CKP<br>mn | 0  | EOC<br>mn | PTC<br>mn1 | PTC<br>mn0 | DIR<br>mn | 0 | SLCm<br>n1 <sup>Note 1</sup> | SLC<br>mn0 | 0 | 1 | DLSm<br>n1 | DLS<br>mn0 |

| PTC<br>mn1 | PTC<br>mn0 | Setting of parity bit in UART mode   |                         |
|------------|------------|--------------------------------------|-------------------------|
|            |            | Transmission                         | Reception               |
| 0          | 0          | Does not output the parity bit.      | Receives without parity |
| 0          | 1          | Outputs 0 parity <sup>Note 2</sup> . | No parity judgment      |
| 1          | 0          | Outputs even parity.                 | Judged as even parity.  |
| 1          | 1          | Outputs odd parity.                  | Judges as odd parity.   |

Be sure to set PTCmn1, PTCmn0 = 0, 0 in the CSI mode.

| DIR<br>mn | Selection of data transfer sequence in CSI and UART modes |
|-----------|-----------------------------------------------------------|
| 0         | Inputs/outputs data with MSB first.                       |
| 1         | Inputs/outputs data with LSB first.                       |

| SLCm<br>n1 <sup>Note 1</sup> | SLC<br>mn0 | Setting of stop bit in UART mode                    |
|------------------------------|------------|-----------------------------------------------------|
| 0                            | 0          | No stop bit                                         |
| 0                            | 1          | Stop bit length = 1 bit                             |
| 1                            | 0          | Stop bit length = 2 bits (mn = 00, 02, 10, 12 only) |
| 1                            | 1          | Setting prohibited                                  |

When the transfer end interrupt is selected, the interrupt is generated when all stop bits have been completely transferred.  
Set 1 bit (SLCmn1, SLCmn0 = 0, 1) during UART reception.  
Set no stop bit (SLCmn1, SLCmn0 = 0, 0) in the CSI mode.

| DLS<br>mn1       | DLS<br>mn0 | Setting of data length in CSI and UART modes                                                  |
|------------------|------------|-----------------------------------------------------------------------------------------------|
| 0                | 1          | 9-bit data length (stored in bits 0 to 8 of the SDRmn register) (settable in UART0 mode only) |
| 1                | 0          | 7-bit data length (stored in bits 0 to 6 of the SDRmn register)                               |
| 1                | 1          | 8-bit data length (stored in bits 0 to 7 of the SDRmn register)                               |
| Other than above |            | Setting prohibited                                                                            |

**Notes 1.** The SCR00 register only.**2.** 0 is always added regardless of the data contents.**Caution** Be sure to clear the following bits to “0”.**SCR00: bits 11, 6, 3****SCR01: bits 11, 6, 5, 3****Be sure to set bit 2 to “1”.****Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01)

### 12.3.5 Higher 7 bits of the serial data register mn (SDRmn)

The SDRmn register is the transmit/receive data register (16 bits) of channel n. Bits 8 to 0 (lower 9 bits) function as a transmit/receive buffer register, and bits 15 to 9 are used as a register that sets the division ratio of the operation clock ( $f_{MCK}$ ).

If the CCSmn bit of serial mode register mn (SMRmn) is cleared to 0, the clock set by dividing the operating clock by the higher 7 bits of the SDRmn register is used as the transfer clock.

The lower 9 bits of the SDRmn register function as a transmit/receive buffer register. During reception, the parallel data converted by the shift register is stored in the lower 9 bits, and during transmission, the data to be transmitted to the shift register is set to the lower 9 bits.

The SDRmn register can be read or written in 16-bit units.

However, the higher 7 bits can be written or read only when the operation is stopped ( $SE_{mn} = 0$ ). During operation ( $SE_{mn} = 1$ ), a value is written only to the lower 9 bits of the  $SDR_{mn}$  register. When the  $SDR_{mn}$  register is read during operation, 0 is always read.

Reset signal generation clears the SDRmn register to 0000H.

**Figure 12-7. Format of Serial Data Register mn (SDRmn)**

[illegible]

- Cautions**
1. Setting SDRmn[15:9] = (0000000B, 0000001B) is prohibited when UART0 is used.
  2. Do not write eight bits to the lower eight bits if operation is stopped (SEmn = 0). (If these bits are written to, the higher seven bits are cleared to 0.)

- Remarks**
1. For the function of the lower 9 bits of the SDRmn register, see **12.2 Configuration of Serial Array Unit**.
  2. m: Unit number (m = 0), n: Channel number (n = 0, 1)

### 12.3.6 Serial flag clear trigger register mn (SIRmn)

The SIRmn register is a trigger register that is used to clear each error flag of channel n.

When each bit (FECTmn, PECTmn, OVCTmn) of this register is set to 1, the corresponding bit (FEFmn, PEFmn, OVFMn) of serial status register mn is cleared to 0. Because the SIRmn register is a trigger register, it is cleared immediately when the corresponding bit of the SSRmn register is cleared.

The SIRmn register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SIRmn register can be set with an 8-bit memory manipulation instruction with SIRmnL.

Reset signal generation clears the SIRmn register to 0000H.

**Figure 12-8. Format of Serial Flag Clear Trigger Register mn (SIRmn)**

Address: F0108H, F0109H (SIR00), F010AH, F010BH (SIR01)    After reset: 0000H    R/W

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2                          | 1          | 0          |
|--------|----|----|----|----|----|----|---|---|---|---|---|---|---|----------------------------|------------|------------|
| SIRmn  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FECT<br>mn <sup>Note</sup> | PEC<br>Tmn | OVC<br>Tmn |

|            |                                                  |
|------------|--------------------------------------------------|
| FEC<br>Tmn | Clear trigger of framing error of channel n      |
| 0          | Not cleared                                      |
| 1          | Clears the FEFmn bit of the SSRmn register to 0. |

|            |                                                  |
|------------|--------------------------------------------------|
| PEC<br>Tmn | Clear trigger of parity error flag of channel n  |
| 0          | Not cleared                                      |
| 1          | Clears the PEFmn bit of the SSRmn register to 0. |

|            |                                                  |
|------------|--------------------------------------------------|
| OVC<br>Tmn | Clear trigger of overrun error flag of channel n |
| 0          | Not cleared                                      |
| 1          | Clears the OVFMn bit of the SSRmn register to 0. |

**Note** The SIR01 register only.

**Caution** Be sure to clear bits 15 to 3 (or bits 15 to 2 for the SIR00 register) to “0”.

**Remarks**

1. m: Unit number (m = 0), n: Channel number (n = 0, 1)
2. When the SIRmn register is read, 0000H is always read.

### 12.3.7 Serial status register mn (SSRmn)

The SSRmn register is a register that indicates the communication status and error occurrence status of channel n. The errors indicated by this register are a framing error, parity error, and overrun error.

The SSRmn register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the SSRmn register can be set with an 8-bit memory manipulation instruction with SSRmnL.

Reset signal generation clears the SSRmn register to 0000H.

**Figure 12-9. Format of Serial Status Register mn (SSRmn) (1/2)**

Address: F0100H, F0101H (SSR00), F0102H, F0103H (SSR01)    After reset: 0000H    R

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6         | 5         | 4 | 3 | 2                         | 1         | 0         |
|--------|----|----|----|----|----|----|---|---|---|-----------|-----------|---|---|---------------------------|-----------|-----------|
| SSRmn  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | TSF<br>mn | BFF<br>mn | 0 | 0 | FEFm<br>n <sup>Note</sup> | PEF<br>mn | OVF<br>mn |

| TSF<br>mn                                                                                                                                                                                                                                                                                                                                             | Communication status indication flag of channel n |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------|
| 0                                                                                                                                                                                                                                                                                                                                                     | Communication is stopped or suspended.            |
| 1                                                                                                                                                                                                                                                                                                                                                     | Communication is in progress.                     |
| <Clear conditions> <ul style="list-style-type: none"> <li>• The STmn bit of the STm register is set to 1 (communication is stopped) or the SSmn bit of the SSm register is set to 1 (communication is suspended).</li> <li>• Communication ends.</li> </ul> <Set condition> <ul style="list-style-type: none"> <li>• Communication starts.</li> </ul> |                                                   |

| BFF<br>mn                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Buffer register status indication flag of channel n |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------|
| 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Valid data is not stored in the SDRmn register.     |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Valid data is stored in the SDRmn register.         |
| <Clear conditions> <ul style="list-style-type: none"> <li>• Transferring transmit data from the SDRmn register to the shift register ends during transmission.</li> <li>• Reading receive data from the SDRmn register ends during reception.</li> <li>• The STmn bit of the STm register is set to 1 (communication is stopped) or the SSmn bit of the SSm register is set to 1 (communication is enabled).</li> </ul> <Set conditions> <ul style="list-style-type: none"> <li>• Transmit data is written to the SDRmn register while the TXEmn bit of the SCRmn register is set to 1 (transmission or transmission and reception mode in each communication mode).</li> <li>• Receive data is stored in the SDRmn register while the RXEmn bit of the SCRmn register is set to 1 (reception or transmission and reception mode in each communication mode).</li> <li>• A reception error occurs.</li> </ul> |                                                     |

**Note** The SSR01 register only.

**Caution** If data is written to the SDRmn register when BFFmn = 1, the transmit/receive data stored in the register is discarded and an overrun error (OVEmn = 1) is detected.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1)



Figure 12-9. Format of Serial Status Register mn (SSRmn) (2/2)

Address: F0100H, F0101H (SSR00), F0102H, F0103H (SSR01) After reset: 0000H R

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6         | 5         | 4 | 3 | 2                         | 1         | 0         |
|--------|----|----|----|----|----|----|---|---|---|-----------|-----------|---|---|---------------------------|-----------|-----------|
| SSRmn  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | TSF<br>mn | BFF<br>mn | 0 | 0 | FEFm<br>n <sup>Note</sup> | PEF<br>mn | OVF<br>mn |

| FEFm<br>n <sup>Note</sup>                                                                                                                                                                                                                            | Framing error detection flag of channel n |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|
| 0                                                                                                                                                                                                                                                    | No error occurs.                          |
| 1                                                                                                                                                                                                                                                    | An error occurs (during UART reception).  |
| <Clear condition> <ul style="list-style-type: none"> <li>• 1 is written to the FECTmn bit of the SIRmn register.</li> </ul> <Set condition> <ul style="list-style-type: none"> <li>• A stop bit is not detected when UART reception ends.</li> </ul> |                                           |

| PEF<br>mn                                                                                                                                                                                                                                                                                                | Parity error detection flag of channel n     |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------|
| 0                                                                                                                                                                                                                                                                                                        | No error occurs.                             |
| 1                                                                                                                                                                                                                                                                                                        | Parity error occurs (during UART reception). |
| <Clear condition> <ul style="list-style-type: none"> <li>• 1 is written to the PECTmn bit of the SIRmn register.</li> </ul> <Set condition> <ul style="list-style-type: none"> <li>• The parity of the transmit data and the parity bit do not match when UART reception ends (parity error).</li> </ul> |                                              |

| OVF<br>mn                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Overrun error detection flag of channel n |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|
| 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | No error occurs.                          |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | An error occurs                           |
| <Clear condition> <ul style="list-style-type: none"> <li>• 1 is written to the OVCTmn bit of the SIRmn register.</li> </ul> <Set condition> <ul style="list-style-type: none"> <li>• Even though receive data is stored in the SDRmn register, that data is not read and transmit data or the next receive data is written while the RXEmn bit of the SCRmn register is set to 1 (reception or transmission and reception mode in each communication mode).</li> <li>• Transmit data is not ready for slave transmission or transmission and reception in CSI mode.</li> </ul> |                                           |

**Note** The SSR01 register only.**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1)

### 12.3.8 Serial channel start register m (SSm)

The SSm register is a trigger register that is used to enable starting communication/count by each channel.

When 1 is written a bit of this register (SSmn), the corresponding bit (SEmn) of serial channel enable status register m (SEm) is set to 1 (Operation is enabled). Because the SSmn bit is a trigger bit, it is cleared immediately when SEMn = 1.

The SSm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SSm register can be set with an 1-bit or 8-bit memory manipulation instruction with SSmL.

Reset signal generation clears the SSm register to 0000H.

**Figure 12-10. Format of Serial Channel Start Register m (SSm)**

Address: F0122H, F0123H    After reset: 0000H    R/W

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0    |
|--------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|------|------|
| SS0    | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SS01 | SS00 |

|      |                                                                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------|-----------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| SSmn | Operation start trigger of channel n                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0    | No trigger operation                                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 1    | Sets the SEMn bit to 1 and enters the communication wait status <sup>Note</sup> . |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

<R> **Note** If set the SSmn = 1 to during a communication operation, will wait status to stop the communication. At this time, holding status value of control register and shift register, SCKmn and SOMn pins, and FEFmn, PEFmn, OVFmn flags.

- Cautions**
1. Be sure to clear bits 15 to 2 to "0".
  2. For the UART reception, set the RXEmn bit of SCRmn register to 1, and then be sure to set SSmn to 1 after 4 or more f<sub>MCK</sub> clocks have elapsed.

- Remarks**
1. m: Unit number (m = 0), n: Channel number (n = 0, 1)
  2. When the SSm register is read, 0000H is always read.

### 12.3.9 Serial channel stop register m (STm)

The STm register is a trigger register that is used to enable stopping communication/count by each channel.

When 1 is written a bit of this register (STmn), the corresponding bit (SEmn) of serial channel enable status register m (SEm) is cleared to 0 (operation is stopped). Because the STmn bit is a trigger bit, it is cleared immediately when SEmn = 0.

The STm register can set written by a 16-bit memory manipulation instruction.

The lower 8 bits of the STm register can be set with a 1-bit or 8-bit memory manipulation instruction with STmL.

Reset signal generation clears the STm register to 0000H.

**Figure 12-11. Format of Serial Channel Stop Register m (STm)**

Address: F0124H, F0125H    After reset: 0000H    W

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0    |
|--------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|------|------|
| ST0    | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ST01 | ST00 |

|          |                                                                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|----------|----------------------------------------------------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| STm<br>n | Operation stop trigger of channel n                                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0        | No trigger operation                                                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 1        | Clears the SEmn bit to 0 and stops the communication operation <sup>Note</sup> . |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

<R> **Note** Holding status value of the control register and shift register, the  $\overline{\text{SCKmn}}$  and SOMn pins, and FEFmn, PEFmn, OVFmn flags.

**Caution** Be sure to clear bits 15 to 2 to “0”.

**Remarks** 1. m: Unit number (m = 0), n: Channel number (n = 0, 1)  
2. When the STm register is read, 0000H is always read.

### 12.3.10 Serial channel enable status register m (SEm)

The SEm register indicates whether data transmission/reception operation of each channel is enabled or stopped.

When 1 is written a bit of serial channel start register m (SSm), the corresponding bit of this register is set to 1. When 1 is written a bit of serial channel stop register m (STm), the corresponding bit is cleared to 0.

Channel n that is enabled to operate cannot rewrite by software the value of the CKOm<sub>n</sub> bit (serial clock output of channel n) of serial output register m (SOM) to be described below, and a value reflected by a communication operation is output from the serial clock pin.

Channel n that stops operation can set the value of the CKOm<sub>n</sub> bit of the SOM register by software and output its value from the serial clock pin. In this way, any waveform, such as that of a start condition/stop condition, can be created by software.

The SEm register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the SEm register can be set with a 1-bit or 8-bit memory manipulation instruction with SEmL.

Reset signal generation clears the SEm register to 0000H.

**Figure 12-12. Format of Serial Channel Enable Status Register m (SEm)**

Address: F0120H, F0121H    After reset: 0000H    R

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0    |
|--------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|------|------|
| SE0    | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SE01 | SE00 |

| SEm <sub>n</sub> | Indication of operation enable/stop status of channel n |
|------------------|---------------------------------------------------------|
| 0                | Operation stops                                         |
| 1                | Operation is enabled.                                   |

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1)

### 12.3.11 Serial output enable register m (SOEm)

The SOEm register is a register that is used to enable or stop output of the serial communication operation of each channel.

Channel n that enables serial output cannot rewrite by software the value of the SOMn bit of serial output register m (SOM) to be described below, and a value reflected by a communication operation is output from the serial data output pin.

For channel n, whose serial output is stopped, the SOMn bit value of the SOM register can be set by software, and that value can be output from the serial data output pin. In this way, any waveform of the start condition and stop condition can be created by software.

The SOEm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SOEm register can be set with a 1-bit or 8-bit memory manipulation instruction with SOEmL.

Reset signal generation clears the SOEm register to 0000H.

**Figure 12-13. Format of Serial Output Enable Register m (SOEm)**

Address: F012AH, F012BH    After reset: 0000H    R/W

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1         | 0         |
|--------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-----------|-----------|
| SOE0   | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SOE<br>01 | SOE<br>00 |

| SOE<br>mn | Serial output enable/stop of channel n            |
|-----------|---------------------------------------------------|
| 0         | Stops output by serial communication operation.   |
| 1         | Enables output by serial communication operation. |

**Caution** Be sure to clear bits 15 to 2 to “0”.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1)

### 12.3.12 Serial output register m (SOM)

The SOM register is a buffer register for serial output of each channel.

The value of the SOMn bit of this register is output from the serial data output pin of channel n.

The value of the CKOMn bit of this register is output from the serial clock output pin of channel n.

The SOMn bit of this register can be rewritten by software only when serial output is disabled (SOEmn = 0). When serial output is enabled (SOEmn = 1), rewriting by software is ignored, and the value of the register can be changed only by a serial communication operation.

The CKOMn bit of this register can be rewritten by software only when the channel operation is stopped (SEmn = 0). While channel operation is enabled (SEmn = 1), rewriting by software is ignored, and the value of the CKOMn bit can be changed only by a serial communication operation.

To use the pin for serial interface as a port function pin, set the corresponding CKOMn and SOMn bits to "1".

The SOM register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears the SOM register to 0F0FH.

<R>

**Figure 12-14. Format of Serial Output Register m (SOM)**

Address: F0128H, F0129H    After reset: 0303H    R/W

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9         | 8         | 7 | 6 | 5 | 4 | 3 | 2 | 1        | 0        |
|--------|----|----|----|----|----|----|-----------|-----------|---|---|---|---|---|---|----------|----------|
| SO0    | 0  | 0  | 0  | 0  | 0  | 0  | CKO<br>01 | CKO<br>00 | 0 | 0 | 0 | 0 | 0 | 0 | SO<br>01 | SO<br>00 |

|           |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|-----------|-----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| CKO<br>mn | Serial clock output of channel n  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0         | Serial clock output value is "0". |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 1         | Serial clock output value is "1". |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

|          |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|----------|----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| SO<br>mn | Serial data output of channel n  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0        | Serial data output value is "0". |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 1        | Serial data output value is "1". |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**Caution** Be sure to clear bits 15 to 10 and 7 to 2 to "0".

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1)

### 12.3.13 Serial output level register m (SOLm)

The SOLm register is a register that is used to set inversion of the data output level of each channel.

This register can be set only in the UART mode. Be sure to set 0 for corresponding bit in the CSI mode.

Inverting channel n by using this register is reflected on pin output only when serial output is enabled (SOEmn = 1). When serial output is disabled (SOEmn = 0), the value of the SOMn bit is output as is.

Rewriting the SOLm register is prohibited when the register is in operation (when SEMn = 1).

The SOLm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SOLm register can be set with an 8-bit memory manipulation instruction with SOLmL.

Reset signal generation clears the SOLm register to 0000H.

**Figure 12-15. Format of Serial Output Level Register m (SOLm)**

Address: F0134H, F0135H    After reset: 0000H    R/W

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0     |
|--------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|
| SOL0   | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SOL00 |

|       |                                                                               |
|-------|-------------------------------------------------------------------------------|
| SOLmn | Selects inversion of the level of the transmit data of channel n in UART mode |
| 0     | Communication data is output as is.                                           |
| 1     | Communication data is inverted and output.                                    |

**Caution** Be sure to clear bits 15 to 1 to “0”.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0)

### 12.3.14 Serial standby control register m (SSCm)

The SSCm register is used to control the startup of reception (the SNOOZE mode) while in the STOP mode when receiving CSI00 or UART0 serial data.

The SSCm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SSCm register can be set with an 8-bit memory manipulation instruction with SSCmL.

Reset signal generation clears the SSCm register to 0000H.

**Caution** The maximum transfer rate in the SNOOZE mode is as follows.

- When using CSI00 : 1 Mbps
- When using UART0 : 9600 bps

Figure 12-16. Format of Serial Standby Control Register m (SSCm)

Address: F0138H After reset: 0000H R/W

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1         | 0        |
|--------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-----------|----------|
| SSCm   | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SS<br>ECm | SWC<br>m |

| SS<br>ECm | Selection of whether to enable or stop the generation of transfer end interrupt                                                                                                                                                                                                                                                                                                                                                       |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0         | Enable the generation of error interrupt (INTSRE0).<br>In the following cases, the clock request signal (an internal signal) to the clock generator is also cleared: <ul style="list-style-type: none"> <li>• When the SWC bit is cleared to 0</li> <li>• When the UART reception start bit is mistakenly detected</li> </ul>                                                                                                         |
| 1         | Stop the generation of error interrupt (INTSRE0).<br>In the following cases, the clock request signal (an internal signal) to the clock generator is also cleared: <ul style="list-style-type: none"> <li>• When the SWCm bit is cleared to 0</li> <li>• When the UART reception start bit is mistakenly detected</li> <li>• When the transfer end interrupt generation timing is based on a parity error or framing error</li> </ul> |

<R>

| SWC<br>m | Setting of the SNOOZE mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0        | Do not use the SNOOZE mode function.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 1        | Use the SNOOZE mode function.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|          | <ul style="list-style-type: none"> <li>• When there is a hardware trigger signal in the STOP mode, the STOP mode is exited, and A/D conversion is performed without operating the CPU (the SNOOZE mode).</li> <li>• The SNOOZE mode function can only be specified when the high-speed on-chip oscillator clock is selected for the CPU/peripheral hardware clock (<math>f_{CLK}</math>). If any other clock is selected, specifying this mode is prohibited.</li> <li>• Even when using SNOOZE mode, be sure to set the SWCm bit to 0 in normal operation mode and change it to 1 just before shifting to STOP mode.<br/>Also, be sure to change the SWCm bit to 0 after returning from STOP mode to normal operation mode.</li> </ul> |

**Caution** Setting SSECm, SWCm = 1, 0 is prohibited.

**Remark** m: Unit number (m = 0)



### 12.3.15 Input switch control register (ISC)

The ISC1 and ISC0 bits of the ISC register are used to realize a LIN-bus communication operation by UART0 in coordination with an external interrupt and the timer array unit.

When bit 0 is set to 1, the input signal of the serial data input (RxD0) pin is selected as an external interrupt (INTP0) that can be used to detect a wakeup signal.

When bit 1 is set to 1, the input signal of the serial data input (RxD0) pin is selected as a timer input, so that wake up signal can be detected, the low width of the break field, and the pulse width of the sync field can be measured by the timer.

The ISC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the ISC register to 00H.

**Figure 12-17. Format of Input Switch Control Register (ISC)**

Address: F0073H After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0    |
|--------|---|---|---|---|---|---|------|------|
| ISC    | 0 | 0 | 0 | 0 | 0 | 0 | ISC1 | ISC0 |

| ISC1 | Switching channel 5 input of timer array unit                                                                                                                                       |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0    | 52 and 64-pin products:<br>Uses the input signal of the TI05 pin as a timer input (normal operation).<br>32, 44, 48-pin products:<br>Do not use a timer input signal for channel 5. |
| 1    | Input signal of the RxD0 pin is used as timer input (detects the wakeup signal and measures the low width of the break field and the pulse width of the sync field).                |

| ISC0 | Switching external interrupt (INTP0) input                                                |
|------|-------------------------------------------------------------------------------------------|
| 0    | Uses the input signal of the INTP0 pin as an external interrupt (normal operation).       |
| 1    | Uses the input signal of the RxD0 pin as an external interrupt (wakeup signal detection). |

**Caution** Be sure to clear bits 7 to 2 to “0”.

### 12.3.16 Noise filter enable register 0 (NFEN0)

The NFEN0 register is used to set whether the noise filter can be used for the input signal from the serial data input pin to each channel.

Disable the noise filter of the pin used for CSI communication, by clearing the corresponding bit of this register to 0.

Enable the noise filter of the pin used for UART communication, by setting the corresponding bit of this register to 1.

When the noise filter is enabled, CPU/peripheral hardware clock ( $f_{CLK}$ ) is synchronized with 2-clock match detection.

When the noise filter is OFF, only synchronization is performed with the CPU/peripheral hardware clock ( $f_{MCK}$ ).

The NFEN0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the NFEN0 register to 00H.

**Figure 12-18. Format of Noise Filter Enable Register 0 (NFEN0)**

Address: F0070H    After reset: 00H    R/W

|        |   |   |   |   |   |   |   |         |
|--------|---|---|---|---|---|---|---|---------|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0       |
| NFEN0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SNFEN00 |

|         |                                 |
|---------|---------------------------------|
| SNFEN00 | Use of noise filter of RxD0 pin |
| 0       | Noise filter OFF                |
| 1       | Noise filter ON                 |

Set the SNFEN00 bit to 1 to use the RxD0 pin.

Clear the SNFEN00 bit to 0 to use the other than RxD0 pin.

**Caution** Be sure to clear bits 7 to 1 to “0”.

**12.3.17 Port input mode register 1 (PIM1)**

This register set the input buffer of port 1 in 1-bit units.

The PIM1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the PIM1 register to 00H.

**Figure 12-19. Format of Port Input Mode Register 1 (PIM1)**

Address F0041H    After reset: 00H    R/W

| Symbol | 7 | 6     | 5     | 4 | 3 | 2 | 1     | 0     |
|--------|---|-------|-------|---|---|---|-------|-------|
| PIM1   | 0 | PIM16 | PIM15 | 0 | 0 | 0 | PIM11 | PIM10 |

| PIM1n | P1n pin input buffer selection (n = 0, 1, 5, 6) |
|-------|-------------------------------------------------|
| 0     | Normal input buffer                             |
| 1     | TTL input buffer                                |

**12.3.18 Port output mode register 1 (POM1)**

This register set the output mode of port 1 in 1-bit units.

The POM1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

<R> In addition, POM1 register is set with PUxx register, whether or not to use the on-chip pull-up resistor.

Reset signal generation clears the POM1 register to 00H.

Refer to Table 4-2 to see which POMxx registers are provided for each product.

**Figure 12-20. Format of Port Output Mode Register 1 (POM1)**

Address F0051H    After reset: 00H    R/W

| Symbol | 7     | 6 | 5     | 4 | 3 | 2     | 1 | 0     |
|--------|-------|---|-------|---|---|-------|---|-------|
| POM1   | POM17 | 0 | POM15 | 0 | 0 | POM12 | 0 | POM10 |

| POM1n | P1n pin output buffer selection (n = 0, 2, 5, 7)                                                                                                        |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | Normal output mode<br>When the input, enable to the PUMn bit                                                                                            |
| 1     | N-ch open-drain output ( $V_{DD}$ tolerance <sup>Note 1</sup> / $EV_{DD}$ tolerance <sup>Note 2</sup> ) mode<br>When the input, disable to the PUMn bit |

**Notes** 1. 32, 44, 48, 52-pin products :  $V_{DD}$  tolerance

2. 64-pin products :  $EV_{DD}$  tolerance

### 12.3.19 Port mode register 1 (PM1)

This register sets input/output of port 1 in 1-bit units.

When using the ports (such as P10/ $\overline{\text{SCK00}}$ /SEG28, P17/SO01/TI02/TO02/SEG6) to be shared with the serial data output pin or serial clock output pin for serial data output or serial clock output, set the port mode register (PM1) bit and <R> LCD port function registers 0, 3 (PFSEG0, PFSEG3) bits corresponding to each port to 0. And set the port register (P1) bit corresponding to each port to 1

Example: When using P17/SO01/TI02/TO02/SEG6 for serial data output

<R> Set the PFSEG06 bit of the LCD port function register 0 to 0  
Set the PM17 bit of the port mode register 1 to 0.  
Set the P17 bit of the port register 1 to 1.

When using the ports (such as P10/ $\overline{\text{SCK00}}$ /SEG28, P11/SI00/RxD0/TOOLRxD/SEG29) to be shared with the serial data input pin or serial clock input pin for serial data input or serial clock input, set the port mode register (PM1) bit <R> corresponding to each port to 1. And set the LCD port function registers 0, 3 (PFSEG0, PFSEG3) bit to 0. At this time, the port register (P1) bit may be 0 or 1.

Example: When using P11/SI00/RxD0/TOOLRxD/SEG29 for serial data input

<R> Set the PFSEG29 bit of the LCD port function register 3 to 0  
Set the PM11 bit of port mode register 1 to 1.  
Set the P11 bit of port register 1 to 0 or 1.

The PM1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets the PM1 register to FFH.

**Figure 12-21. Format of Port Mode Register 1 (PM1)**

Address: FFF21H After reset: FFH R/W

| Symbol | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|--------|------|------|------|------|------|------|------|------|
| PM1    | PM17 | PM16 | PM15 | PM14 | PM13 | PM12 | PM11 | PM10 |

| PM1n | P1n pin I/O mode selection (n = 0 to 7) |
|------|-----------------------------------------|
| 0    | Output mode (output buffer on)          |
| 1    | Input mode (output buffer off)          |

## 12.4 Operation stop mode

Each serial interface of serial array unit has the operation stop mode.

In this mode, serial communication cannot be executed, thus reducing the power consumption.

In addition, the pin for serial interface can be used as port function pins in this mode.

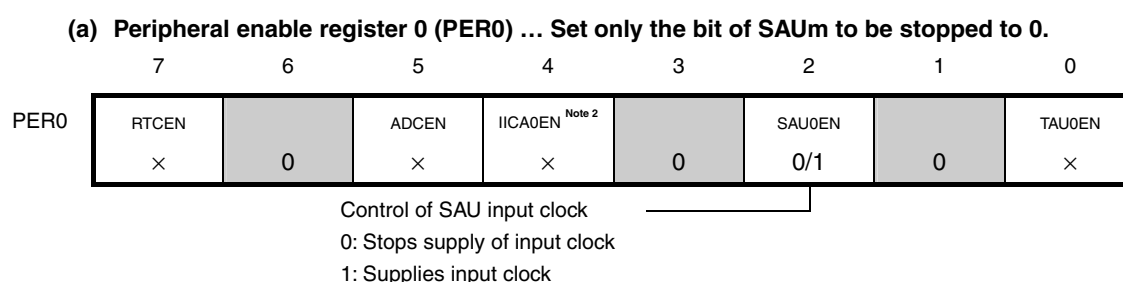
### 12.4.1 Stopping the operation by units

The stopping of the operation by units is set by using peripheral enable register 0 (PER0).

The PER0 register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

To stop the operation of serial array unit, set bit 2 (SAU0EN) to 0.

**Figure 12-22. Peripheral Enable Register 0 (PER0) Setting When Stopping the Operation by Units**



**Cautions 1.** If SAU0EN = 0, writing to a control register of serial array unit m is ignored, and, even if the register is read, only the default value is read

Note that this does not apply to the following registers.

- Input switch control register (ISC)
- Noise filter enable register 0 (NFEN0)
- Serial standby control register 0 (SSC0)
- Port input mode register 1 (PIM1)
- Port output mode register 1 (POM1)
- LCD port function registers 0, 3 (PFSEG0, PFSEG3)
- Port mode register 1 (PM1)
- Port register 1 (P1)

**2.** Be sure to clear bits to 6, 3, 1 to “0”.

**Remark**  : Setting disabled (set to the initial value)

×: Bits not used with serial array units (depending on the settings of other peripheral functions)

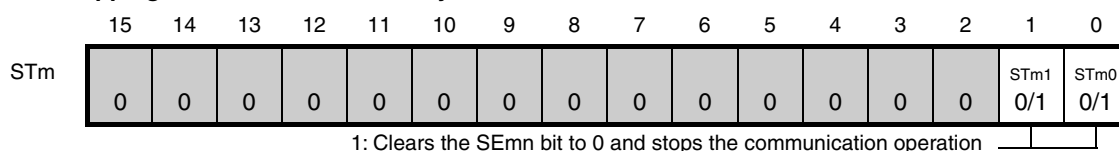
0/1: Set to 0 or 1 depending on the usage of the user

### 12.4.2 Stopping the operation by channels

The stopping of the operation by channels is set using each of the following registers.

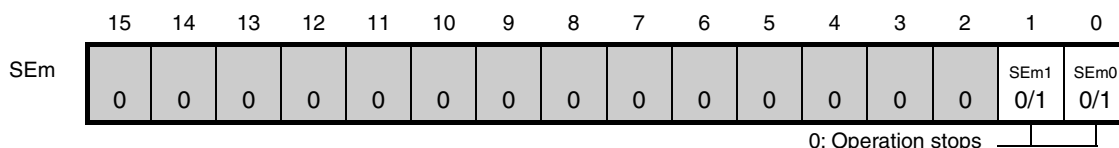
**Figure 12-23. Each Register Setting When Stopping the Operation by Channels**

- (a) **Serial channel stop register m (STm) ... This register is a trigger register that is used to enable stopping communication/count by each channel.**



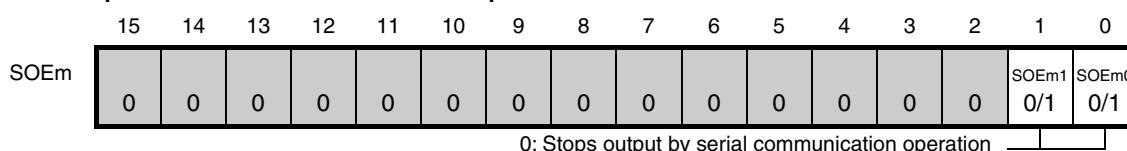
\* Because the ST<sub>m</sub>n bit is a trigger bit, it is cleared immediately when SE<sub>m</sub>n = 0.

- (b) **Serial Channel Enable Status Register m (SEm) ... This register indicates whether data transmission/reception operation of each channel is enabled or stopped.**



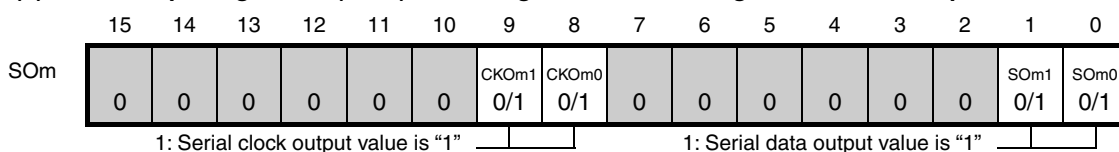
\* The SEm register is a read-only status register, whose operation is stopped by using the STm register. With a channel whose operation is stopped, the value of the CKOm<sub>n</sub> bit of the SOm register can be set by software.

- (c) **Serial output enable register m (SOEm) ... This register is a register that is used to enable or stop output of the serial communication operation of each channel.**



\* For channel n, whose serial output is stopped, the SOm<sub>n</sub> bit value of the SOm register can be set by software.

- (d) **Serial output register m (SOm) ... This register is a buffer register for serial output of each channel.**



\* When using pins corresponding to each channel as port function pins, set the corresponding CKOm<sub>n</sub>, SOm<sub>n</sub> bits to "1".

**Remarks 1.** m: Unit number (m = 0), n: Channel number (n = 0, 1)

**2.** : Setting disabled (set to the initial value), 0/1: Set to 0 or 1 depending on the usage of the user

## 12.5 Operation of 3-Wire Serial I/O (CSI00, CSI01) Communication

This is a clocked communication function that uses three lines: serial clock ( $\overline{\text{SCK}}$ ) and serial data (SI and SO) lines.

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

[Clock control]

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate

During master communication (CSI00): Max.  $f_{\text{MCK}}/2$  <sup>Notes 1, 2</sup>

During master communication (CSI01): Max.  $f_{\text{MCK}}/4$  <sup>Note 2</sup>

During slave communication: Max.  $f_{\text{MCK}}/6$  <sup>Note 2</sup>

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

In addition, CSI00 supports the SNOOZE mode. When  $\overline{\text{SCK}}$  input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible.

- <R>      **Notes 1.** In master communication (CSI00), maximum transfer rate become  $f_{\text{MCK}}/2$  when the following conditions.
- $2.7 \text{ V} \leq \text{EV}_{\text{DD}} = \text{V}_{\text{DD}} \leq 5.5 \text{ V}$
  - $f_{\text{MCK}} \leq 12 \text{ MHz}$
- Other cases, maximum transfer rate become  $f_{\text{MCK}}/4$ .
- 2.** Use the clocks within a range satisfying the  $\overline{\text{SCK}}$  cycle time ( $t_{\text{KCY}}$ ) characteristics (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS**).



The channels supporting 3-wire serial I/O (CSI00, CSI01) are channels 0 and 1.

| Channel | Used as CSI | Used as UART               |
|---------|-------------|----------------------------|
| 0       | CSI00       | UART0 (supporting LIN-bus) |
| 1       | CSI01       |                            |

3-wire serial I/O (CSI00, CSI01) performs the following seven types of communication operations.

- Master transmission (See 12.5.1.)
- Master reception (See 12.5.2.)
- Master transmission/reception (See 12.5.3.)
- Slave transmission (See 12.5.4.)
- Slave reception (See 12.5.5.)
- Slave transmission/reception (See 12.5.6.)
- SNOOZE mode function (See 12.5.7.)

### 12.5.1 Master transmission

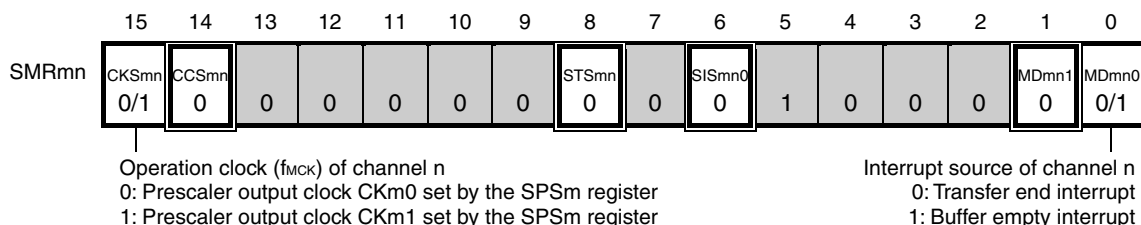
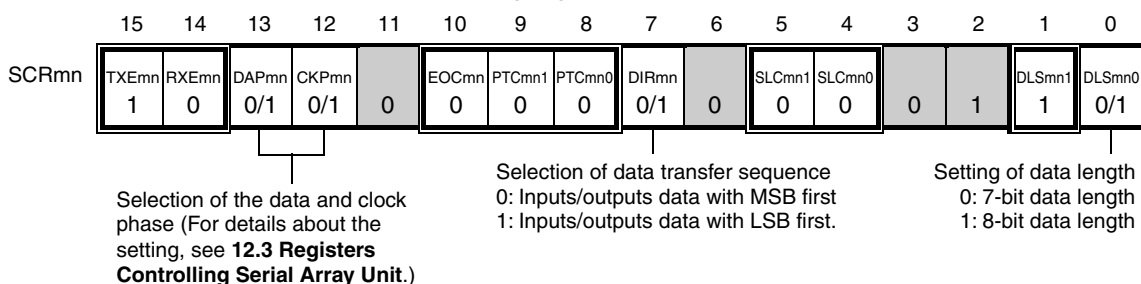
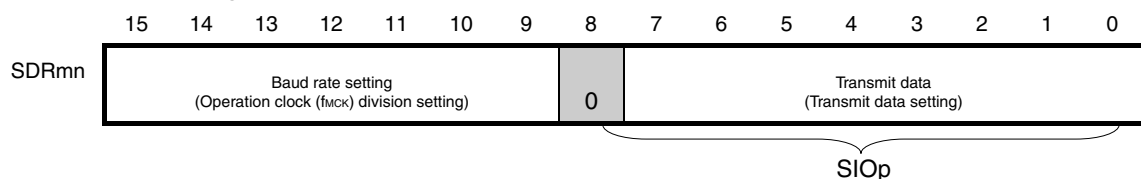
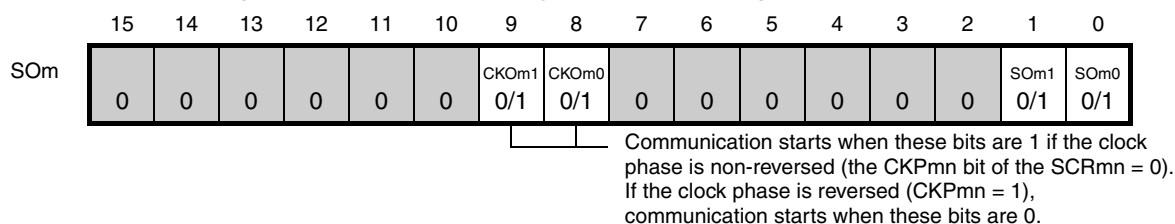
Master transmission is that the RL78/L12 outputs a transfer clock and transmits data to another device.

| 3-Wire Serial I/O    | CSI00                                                                                                                                                                                                                                                                                                                                                                          | CSI01                            |
|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|
| Target channel       | Channel 0                                                                                                                                                                                                                                                                                                                                                                      | Channel 1                        |
| Pins used            | $\overline{\text{SCK00}}$ , SO00                                                                                                                                                                                                                                                                                                                                               | $\overline{\text{SCK01}}$ , SO01 |
| Interrupt            | INTCSI00                                                                                                                                                                                                                                                                                                                                                                       | INTCSI01                         |
|                      | Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.                                                                                                                                                                                                                                                      |                                  |
| Error detection flag | None                                                                                                                                                                                                                                                                                                                                                                           |                                  |
| Transfer data length | 7 or 8 bits                                                                                                                                                                                                                                                                                                                                                                    |                                  |
| Transfer rate        | Max. $f_{\text{MCK}}/2$ [Hz] (CSI00), $f_{\text{MCK}}/4$ [Hz] (CSI01)<br>Min. $f_{\text{CLK}}/(2 \times 2^{15} \times 128)$ [Hz] <sup>Note</sup> $f_{\text{CLK}}$ : System clock frequency                                                                                                                                                                                     |                                  |
| Data phase           | Selectable by the DAPmn bit of the SCRmn register <ul style="list-style-type: none"> <li>• DAPmn = 0: Data output starts from the start of the operation of the serial clock.</li> <li>• DAPmn = 1: Data output starts half a clock before the start of the serial clock operation.</li> </ul>                                                                                 |                                  |
| Clock phase          | Selectable by the CKPmn bit of the SCRmn register <ul style="list-style-type: none"> <li>• CKPmn = 0: Non-reverse (data output at the falling edge and data input at the rising edge of <math>\overline{\text{SCK}}</math>)</li> <li>• CKPmn = 1: Reverse (data output at the rising edge and data input at the falling edge of <math>\overline{\text{SCK}}</math>)</li> </ul> |                                  |
| Data direction       | MSB or LSB first                                                                                                                                                                                                                                                                                                                                                               |                                  |

**Note** Use this operation within a range that satisfies the conditions above and the Peripheral functions characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS**).

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01

## (1) Register setting

**Figure 12-24. Example of Contents of Registers for Master Transmission of 3-Wire Serial I/O (CSI00, CSI01) (1/2)****(a) Serial mode register mn (SMRmn)****(b) Serial communication operation setting register mn (SCRmn)****(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)****(d) Serial output register m (SOM) ... Sets only the bits of the target channel.**

- Remarks** 1. m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01
2.   : Setting is fixed in the CSI master transmission mode,   : Setting disabled (set to the initial value)  
 0/1: Set to 0 or 1 depending on the usage of the user

**Figure 12-24. Example of Contents of Registers for Master Transmission of 3-Wire Serial I/O (CSI00, CSI01) (2/2)**

**(e) Serial output enable register m (SOEm) ... Sets only the bits of the target channel to 1.**

|      |    |    |    |    |    |    |   |   |   |   |   |   |   |   |       |       |
|------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-------|-------|
|      | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0     |
| SOEm |    |    |    |    |    |    |   |   |   |   |   |   |   |   | SOEm1 | SOEm0 |
|      | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0/1   | 0/1   |

**(f) Serial channel start register m (SSm) ... Sets only the bits of the target channel to 1.**

|     |    |    |    |    |    |    |   |   |   |   |   |   |   |   |      |      |
|-----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|------|------|
|     | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0    |
| SSm |    |    |    |    |    |    |   |   |   |   |   |   |   |   | SSm1 | SSm0 |
|     | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0/1  | 0/1  |

**Remarks 1.** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01

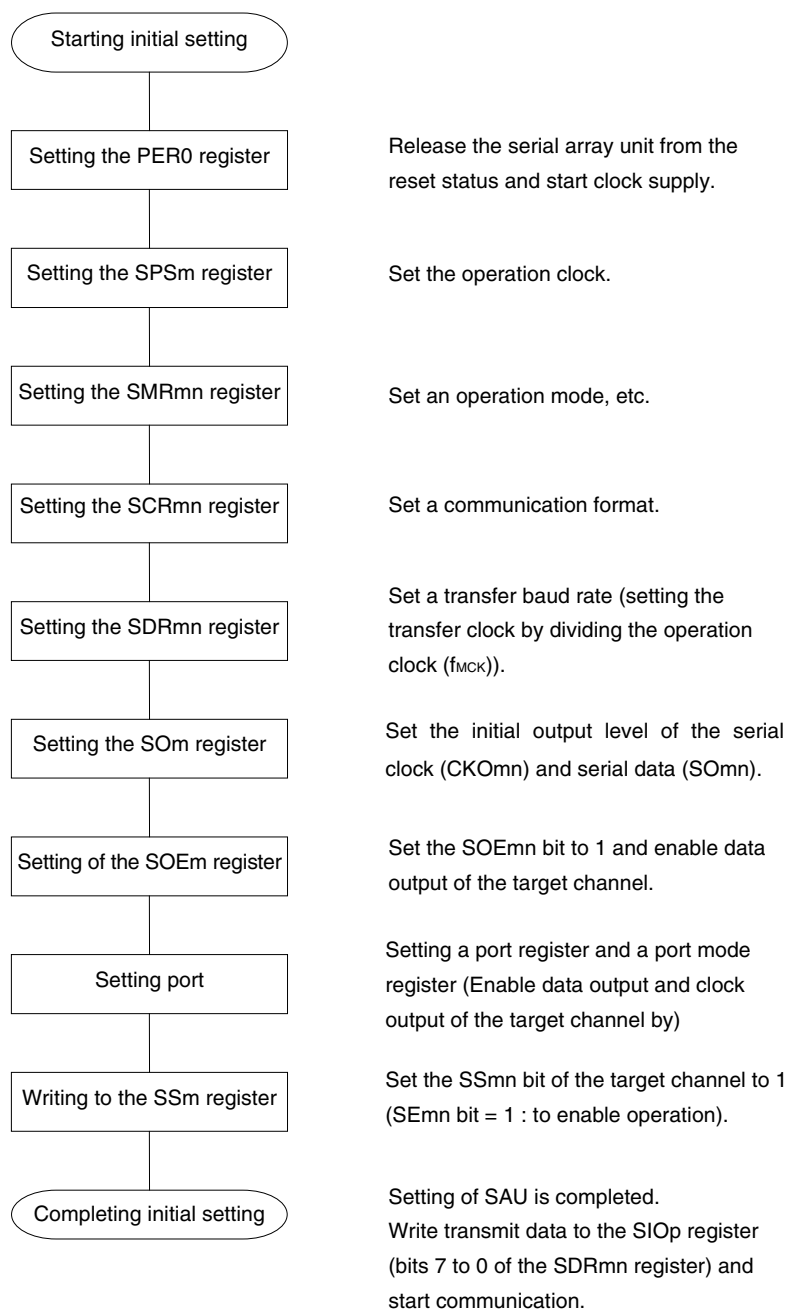
**2.** : Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

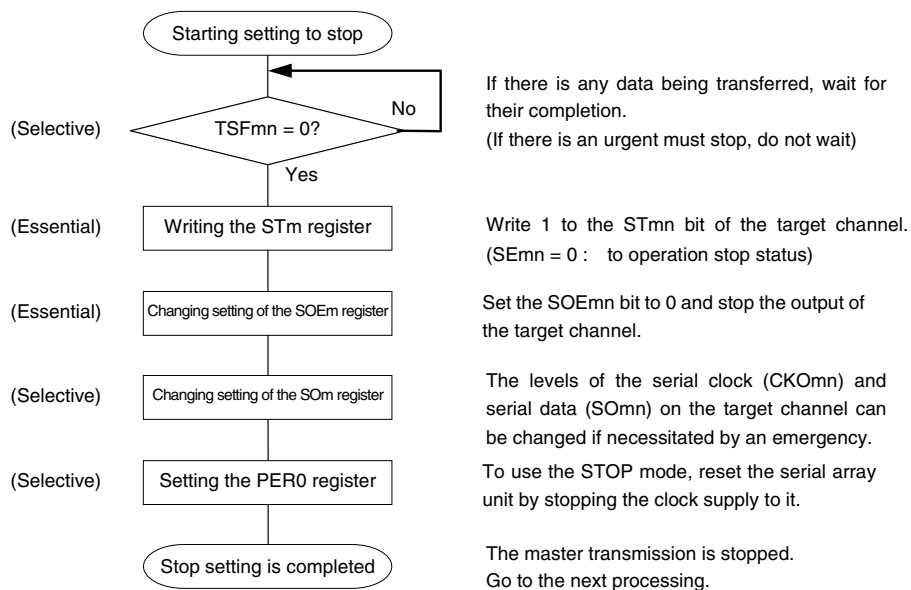
0/1: Set to 0 or 1 depending on the usage of the user

## (2) Operation procedure

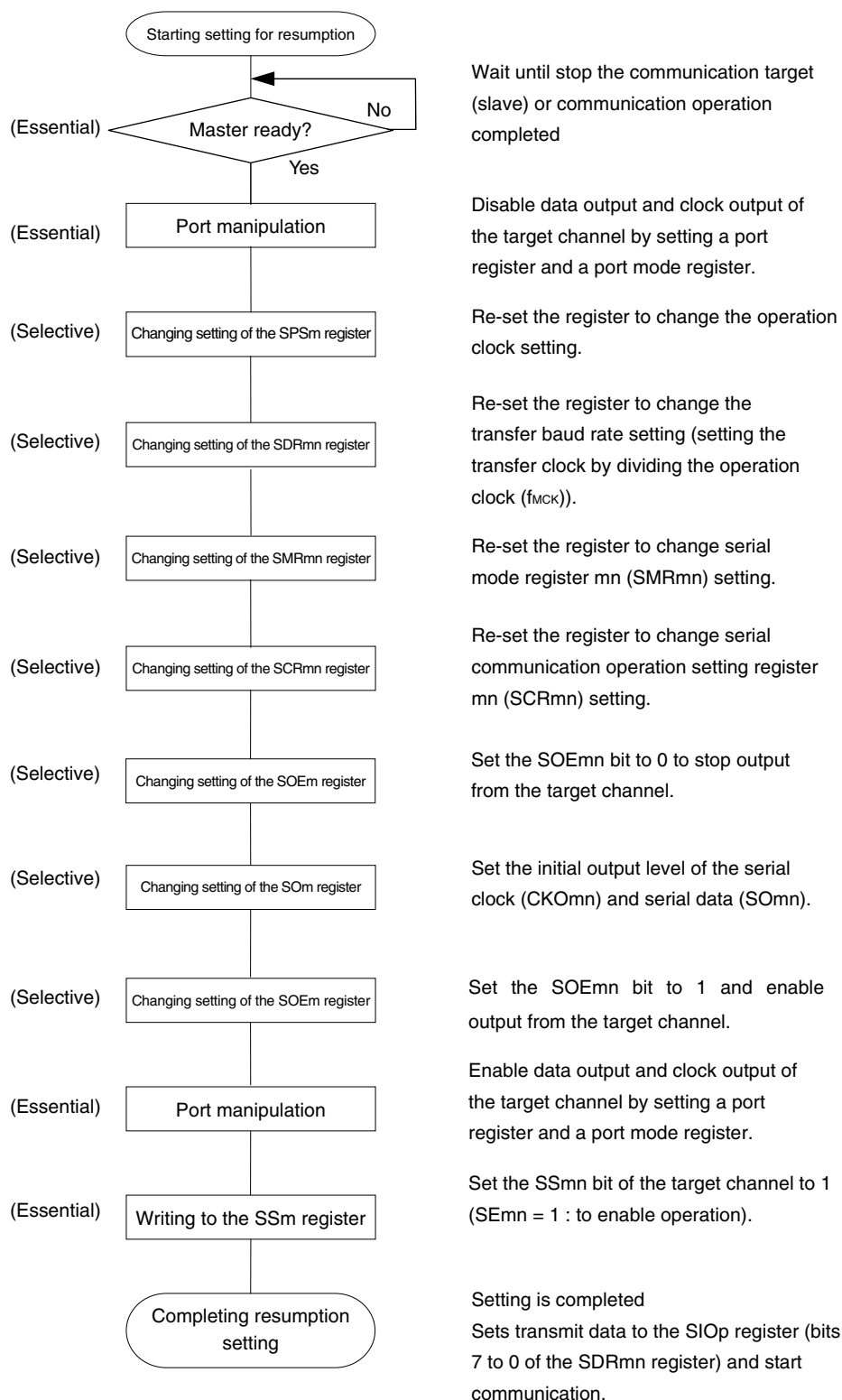
&lt;R&gt;

**Figure 12-25. Initial Setting Procedure for Master Transmission**

&lt;R&gt;

**Figure 12-26. Procedure for Stopping Master Transmission**

&lt;R&gt;

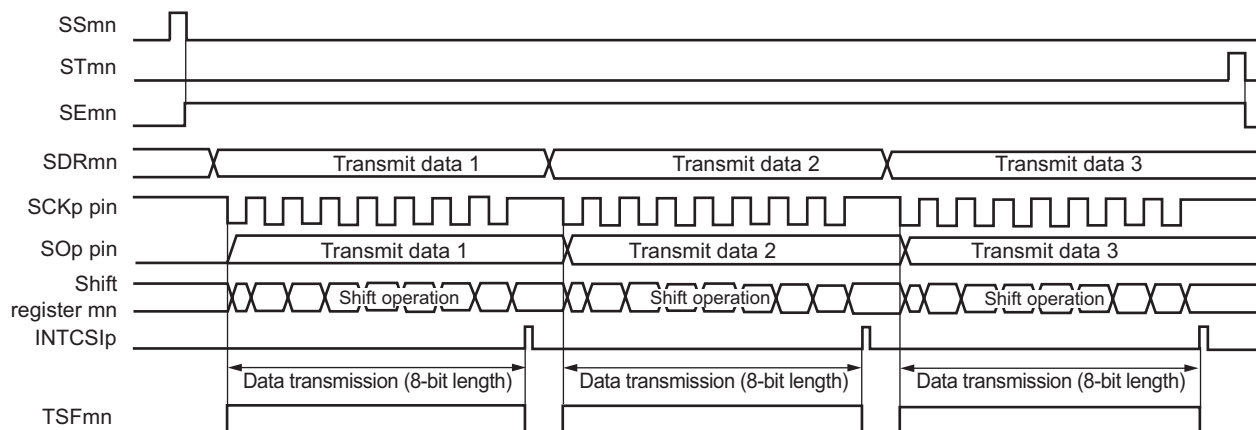
**Figure 12-27. Procedure for Resuming Master Transmission**

**Remark** If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (slave) stops or transmission finishes, and then perform initialization instead of restarting the transmission.

## (3) Processing flow (in single-transmission mode)

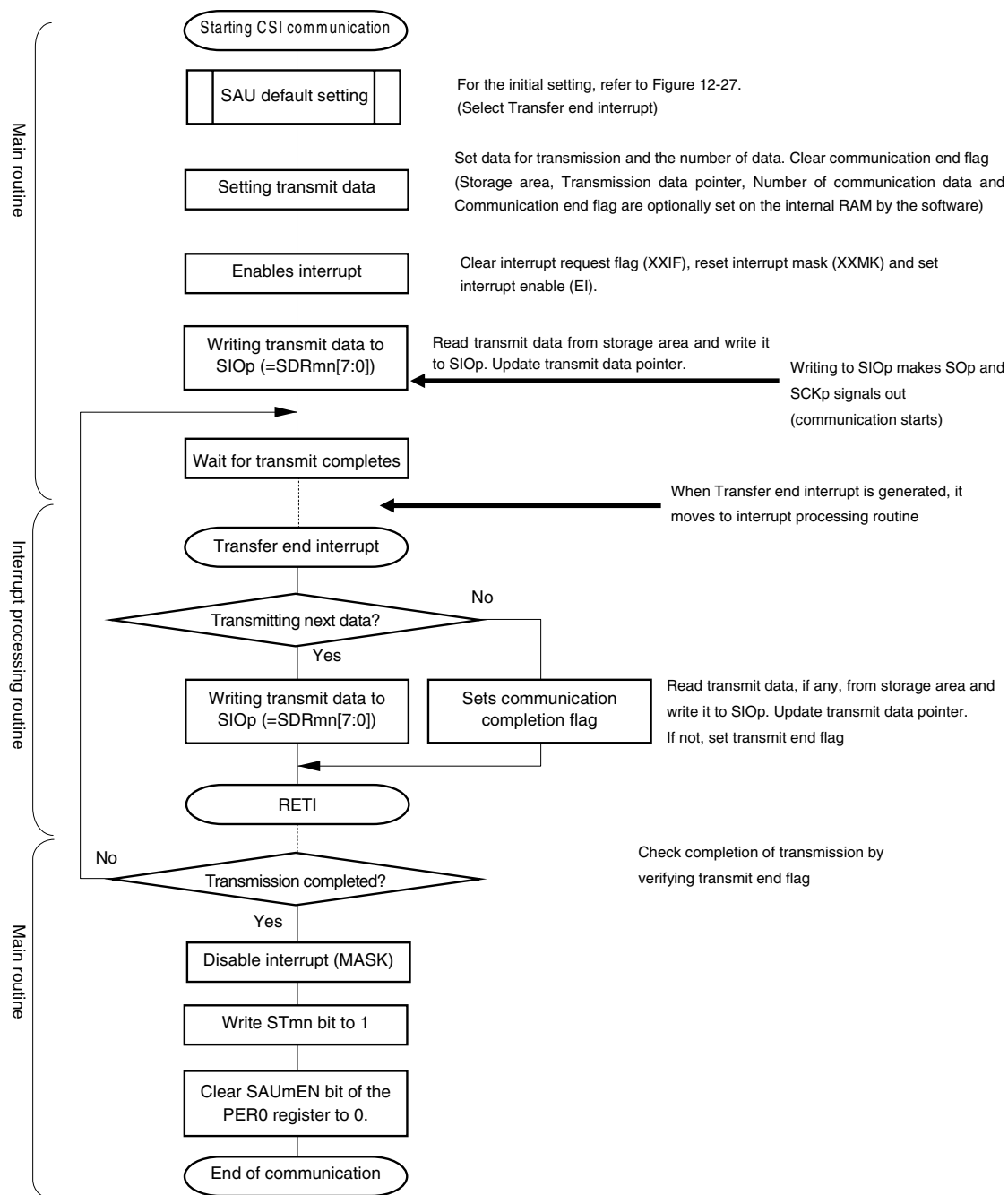
&lt;R&gt;

**Figure 12-28. Timing Chart of Master Transmission (in Single-Transmission Mode)**  
 (Type 1: DAPmn = 0, CKPmn = 0)



**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01

Figure 12-29. Flowchart of Master Transmission (in Single-Transmission Mode)

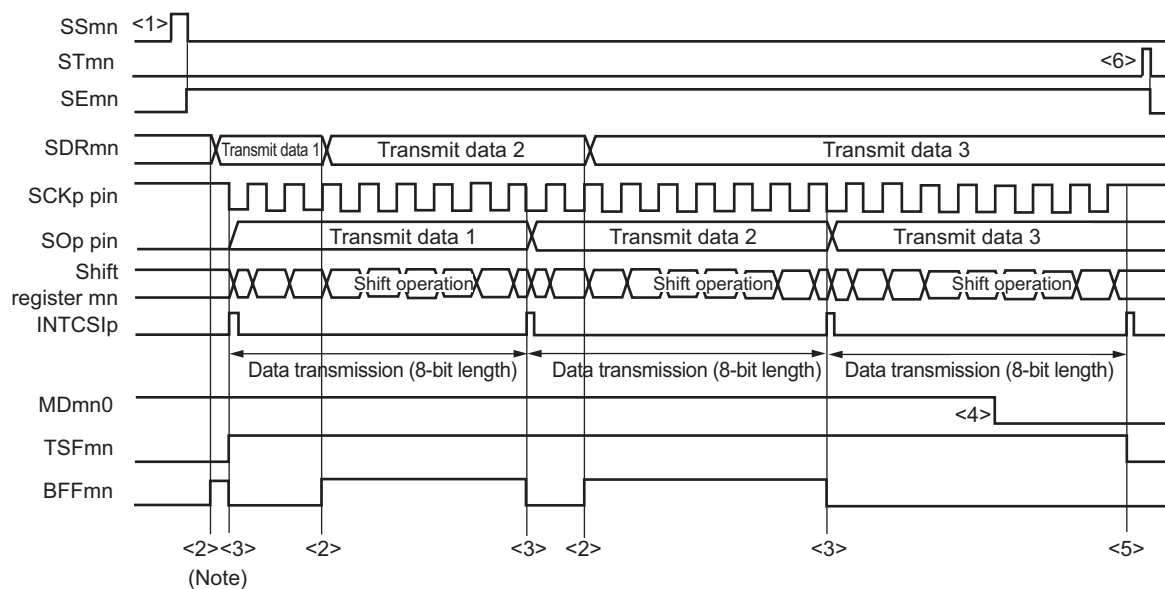




## (4) Processing flow (in continuous transmission mode)

&lt;R&gt;

**Figure 12-30. Timing Chart of Master Transmission (in Continuous Transmission Mode)**  
 (Type 1: DAPmn = 0, CKPmn = 0)

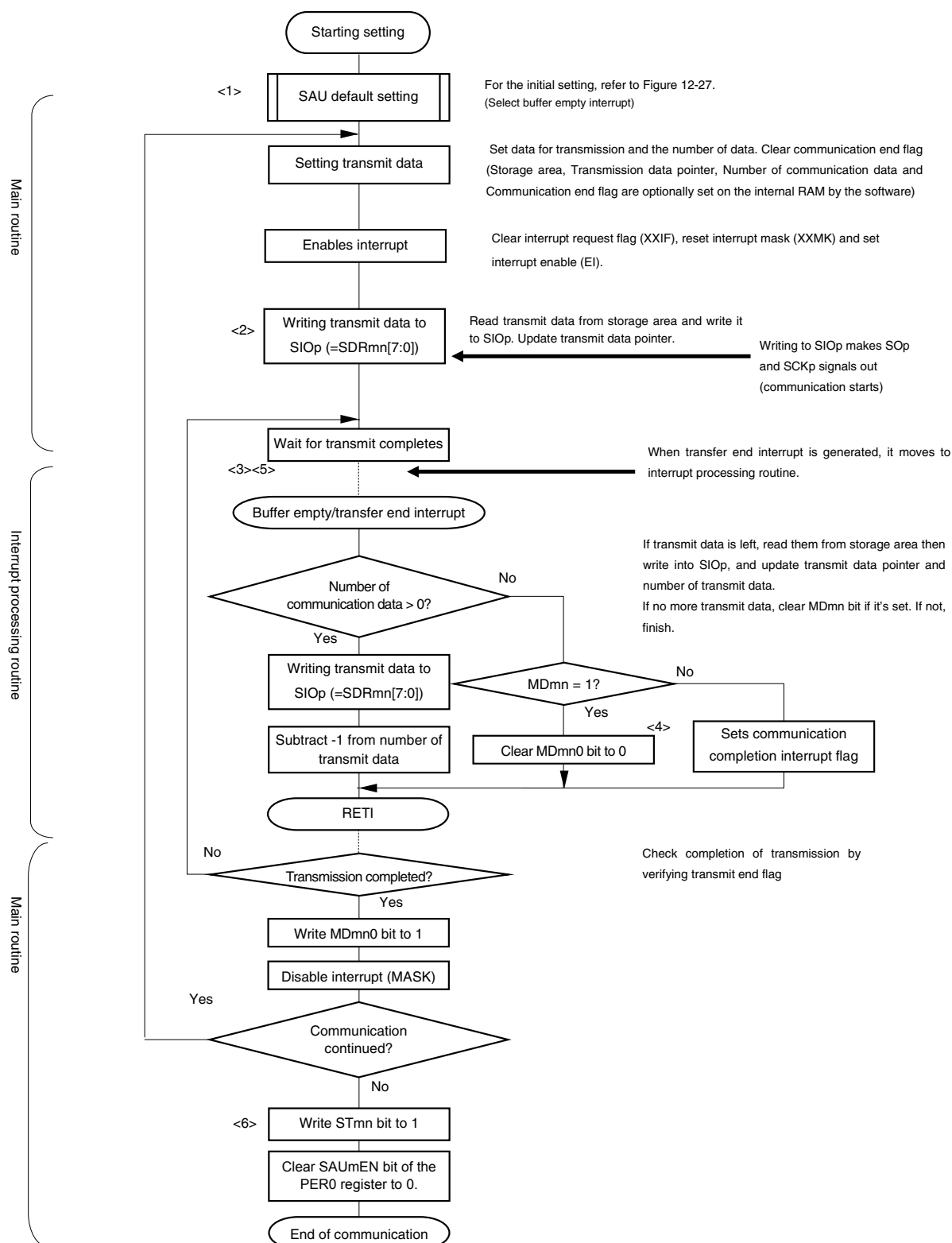


**Note** If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

**Caution** The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it will be rewritten before the transfer end interrupt of the last transmit data.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01

Figure 12-31. Flowchart of Master Transmission (in Continuous Transmission Mode)



**Remark** <1> to <6> in the figure correspond to <1> to <6> in **Figure 12-30 Timing Chart of Master Transmission (in Continuous Transmission Mode)**.

### 12.5.2 Master reception

Master reception is that the RL78/L12 outputs a transfer clock and receives data from other device.

<R>

| 3-Wire Serial I/O    | CSI00                                                                                                                                                                                                                                                                                        | CSI01                            |
|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|
| Target channel       | Channel 0                                                                                                                                                                                                                                                                                    | Channel 1                        |
| Pins used            | $\overline{\text{SCK00}}$ , SI00                                                                                                                                                                                                                                                             | $\overline{\text{SCK01}}$ , SI01 |
| Interrupt            | INTCSI00                                                                                                                                                                                                                                                                                     | INTCSI01                         |
|                      | Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.                                                                                                                                                                    |                                  |
| Error detection flag | Overflow error detection flag (OVFmn) only                                                                                                                                                                                                                                                   |                                  |
| Transfer data length | 7 or 8 bits                                                                                                                                                                                                                                                                                  |                                  |
| Transfer rate        | Max. $f_{\text{MCK}}/2$ [Hz] (CSI00), $f_{\text{MCK}}/4$ [Hz] (CSI01)<br>Min. $f_{\text{CLK}}/(2 \times 2^{15} \times 128)$ [Hz] <sup>Note</sup> $f_{\text{CLK}}$ : System clock frequency                                                                                                   |                                  |
| Data phase           | Selectable by the DAPmn bit of the SCRmn register <ul style="list-style-type: none"> <li>• DAPmn = 0: Data input starts from the start of the operation of the serial clock.</li> <li>• DAPmn = 1: Data input starts half a clock before the start of the serial clock operation.</li> </ul> |                                  |
| Clock phase          | Selectable by the CKPmn bit of the SCRmn register <ul style="list-style-type: none"> <li>• CKPmn = 0: Non-reverse</li> <li>• CKPmn = 1: Reverse</li> </ul>                                                                                                                                   |                                  |
| Data direction       | MSB or LSB first                                                                                                                                                                                                                                                                             |                                  |

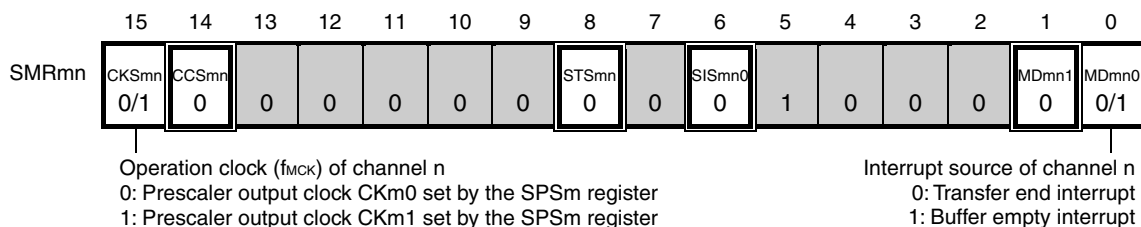
**Note** Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS**).

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01

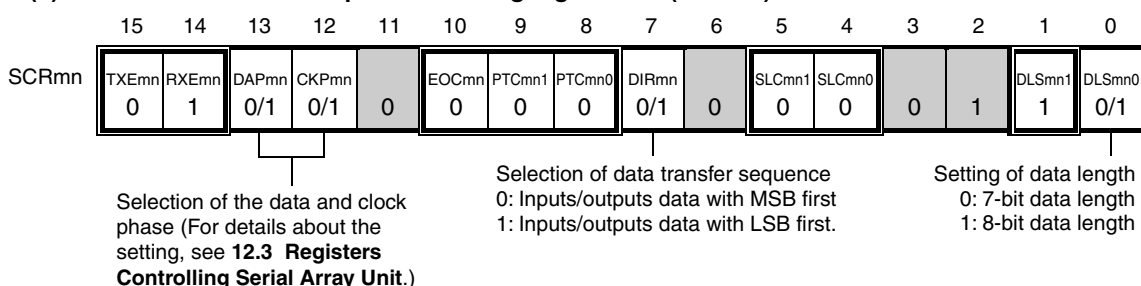
## (1) Register setting

**Figure 12-32. Example of Contents of Registers for Master Reception of 3-Wire Serial I/O  
(CSI00, CSI01) (1/2)**

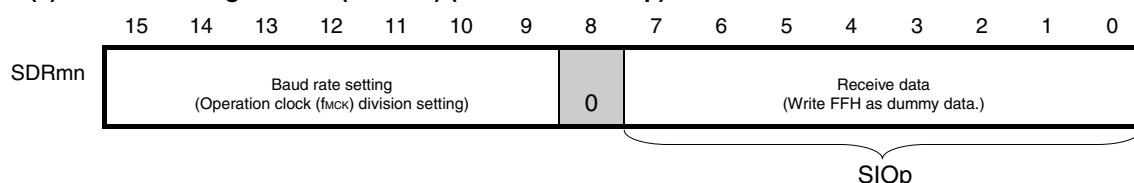
## (a) Serial mode register mn (SMRmn)



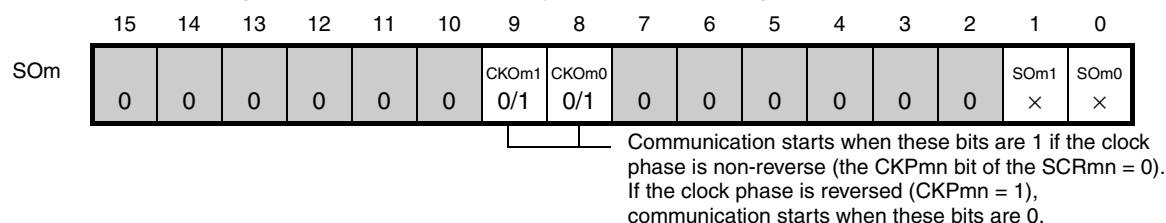
## (b) Serial communication operation setting register mn (SCRmn)



## (c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



## (d) Serial output register m (SOM) ... Sets only the bits of the target channel.



- Remarks**
- m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01
  - : Setting is fixed in the CSI master reception mode, ■: Setting disabled (set to the initial value)  
 ×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)  
 0/1: Set to 0 or 1 depending on the usage of the user

**Figure 12-32. Example of Contents of Registers for Master Reception of 3-Wire Serial I/O (CSI00, CSI01) (2/2)**

**(e) Serial output enable register m (SOEm) ...The register that not used in this mode.**

|      | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1          | 0          |
|------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|------------|------------|
| SOEm | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SOEm1<br>× | SOEm0<br>× |

**(f) Serial channel start register m (SSm) ... Sets only the bits of the target channel to 1.**

|     | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1           | 0           |
|-----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-------------|-------------|
| SSm | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SSm1<br>0/1 | SSm0<br>0/1 |

**Remarks 1.** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01)

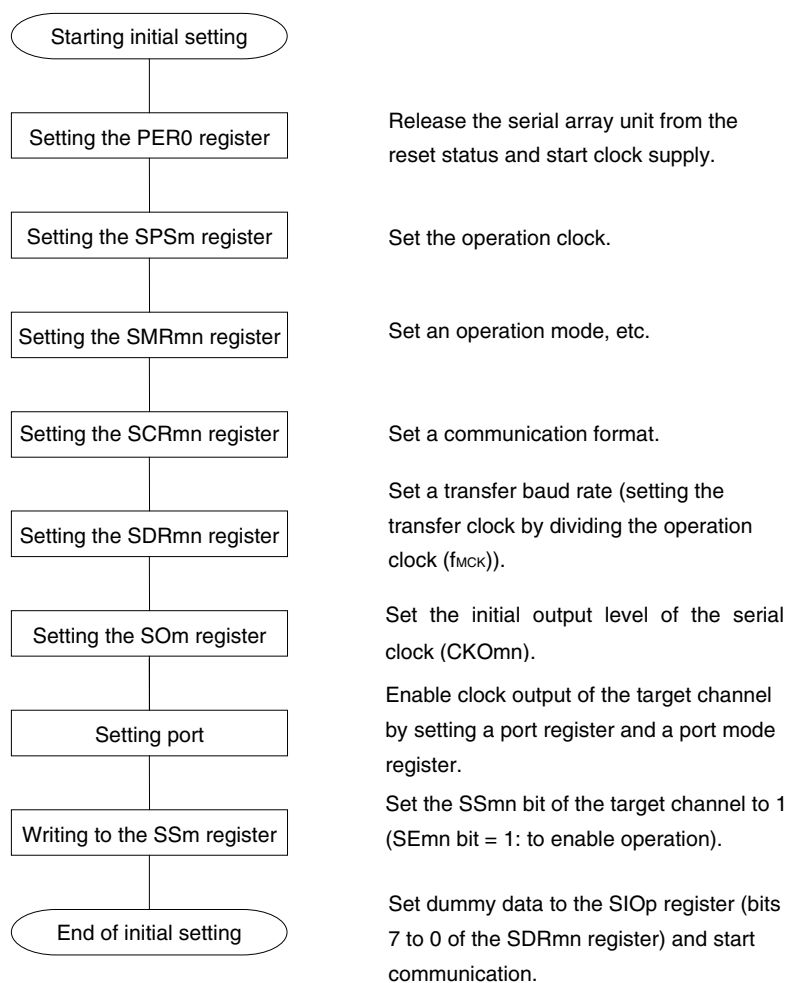
**2.**  : Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

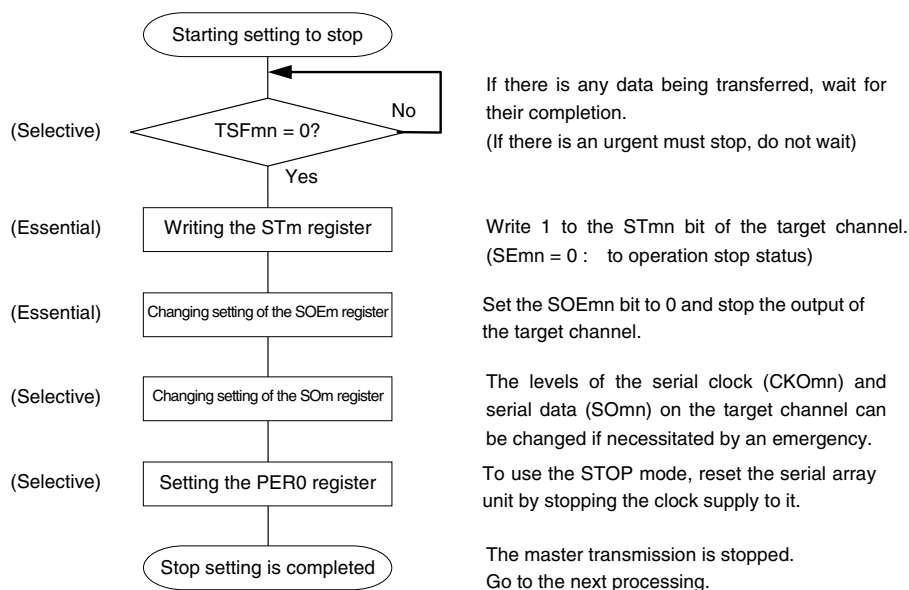
0/1: Set to 0 or 1 depending on the usage of the user

## (2) Operation procedure

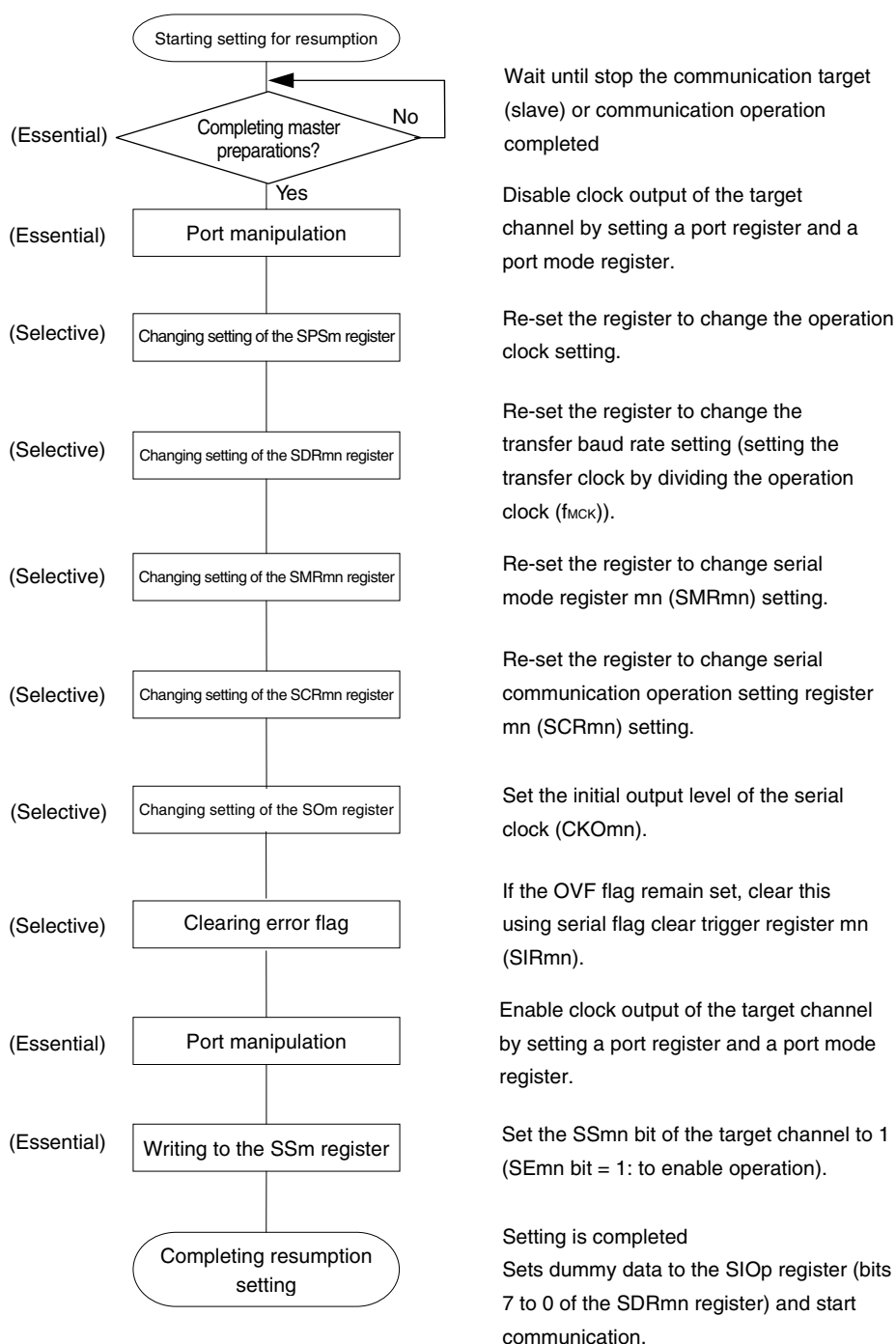
&lt;R&gt;

**Figure 12-33. Initial Setting Procedure for Master Reception**

&lt;R&gt;

**Figure 12-34. Procedure for Stopping Master Reception**

&lt;R&gt;

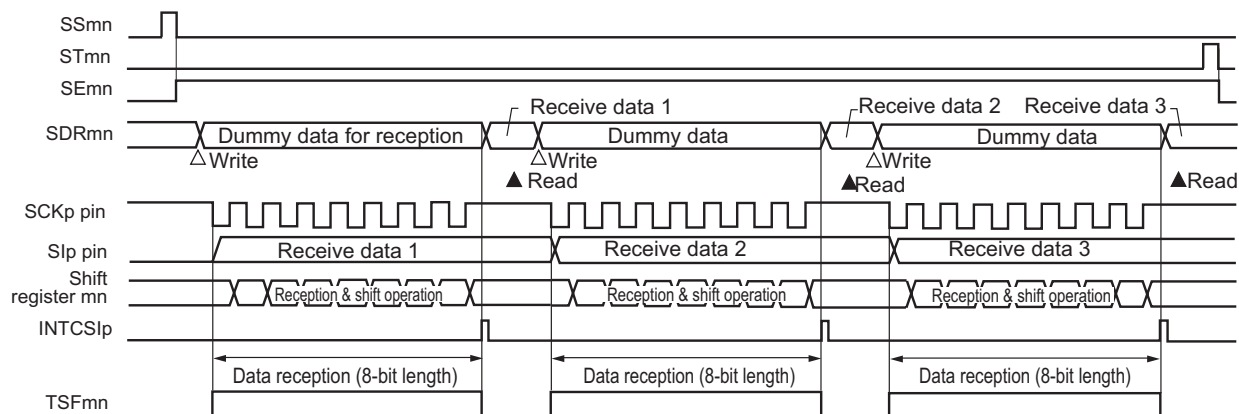
**Figure 12-35. Procedure for Resuming Master Reception**

**Remark** If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (slave) stops or transmission finishes, and then perform initialization instead of restarting the transmission.

## (3) Processing flow (in single-reception mode)

Figure 12-36. Timing Chart of Master Reception (in Single-Reception Mode)

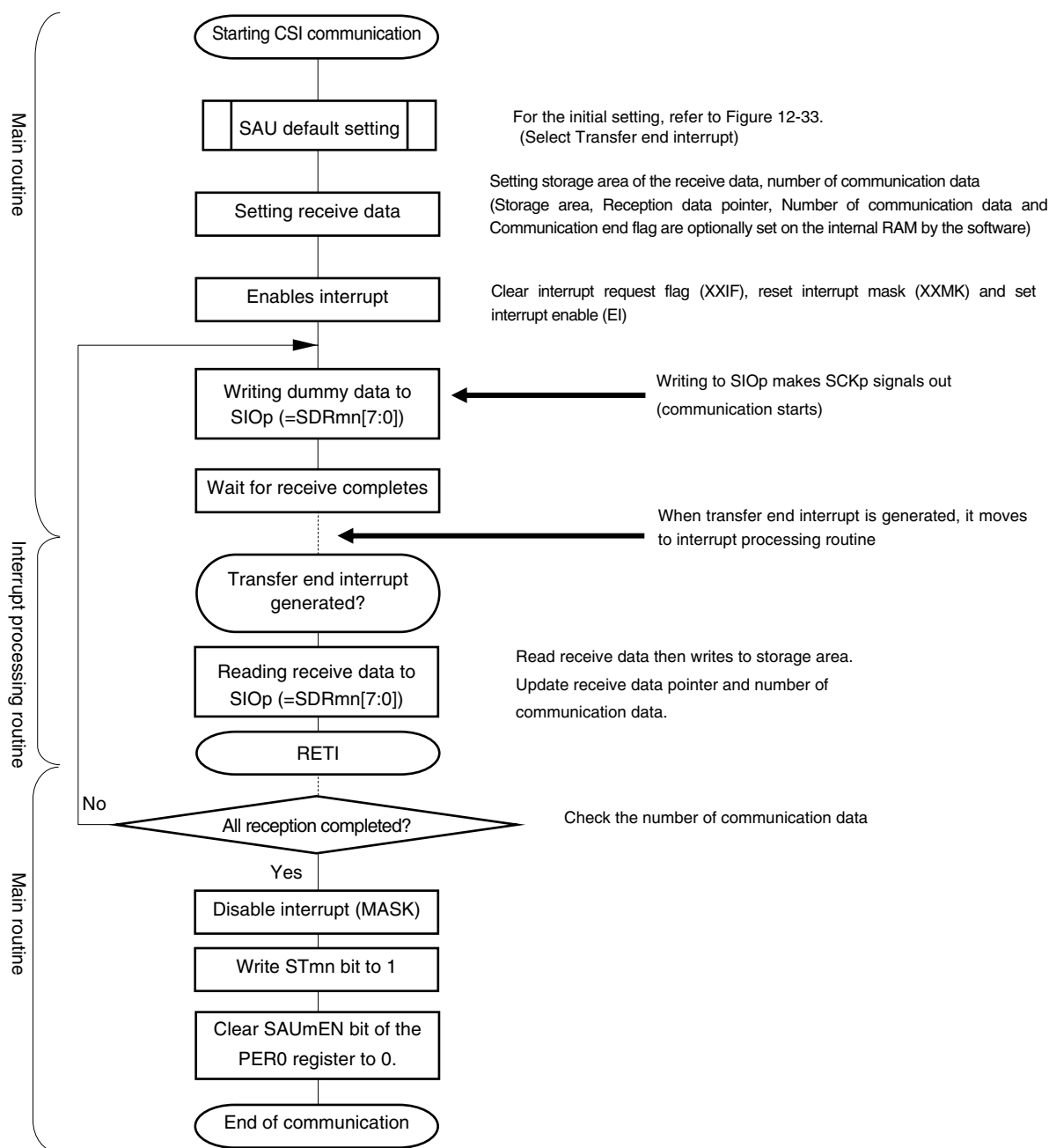
(Type 1: DAPmn = 0, CKPmn = 0)



**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01

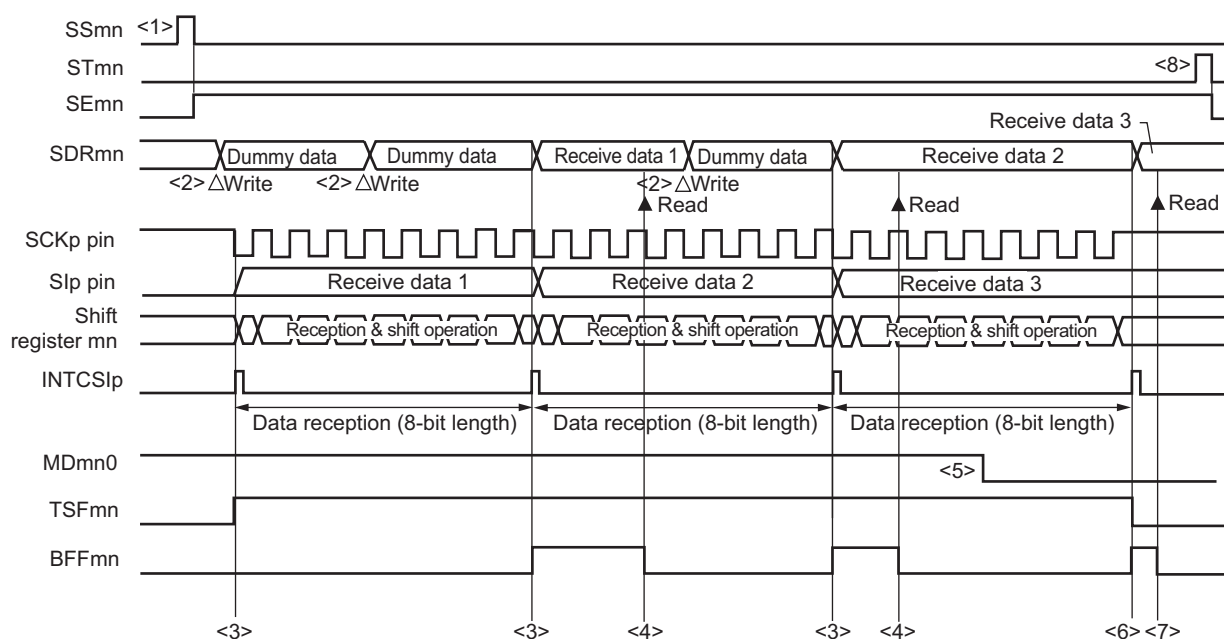


Figure 12-37. Flowchart of Master Reception (in Single-Reception Mode)



## (4) Processing flow (in continuous reception mode)

&lt;R&gt; Figure 12-38. Timing Chart of Master Reception (in Continuous Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)



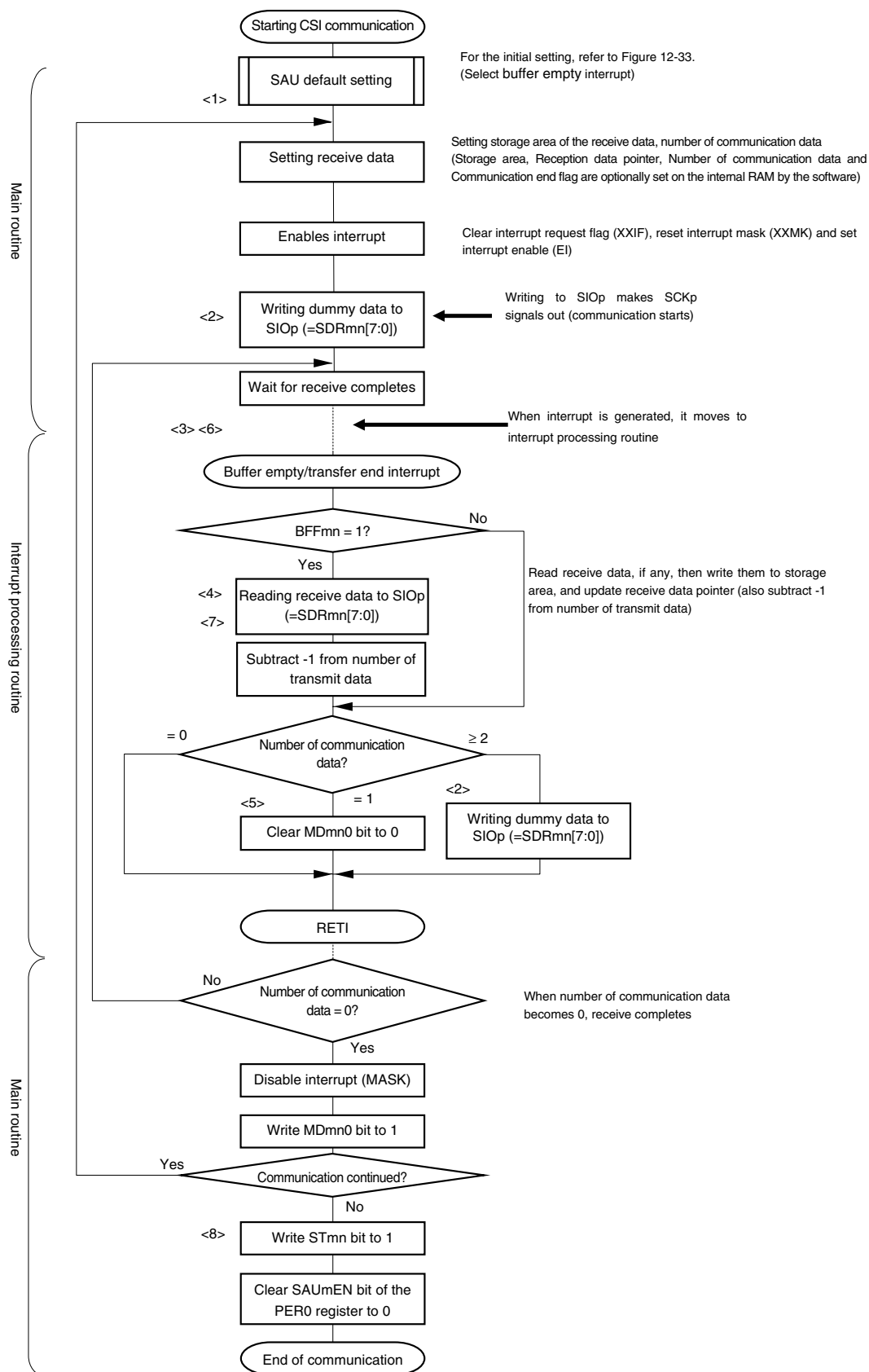
**Caution** The MDmn0 bit can be rewritten even during operation.

However, rewrite it before receive of the last bit is started, so that it has been rewritten before the transfer end interrupt of the last receive data.

**Remarks 1.** <1> to <8> in the figure correspond to <1> to <8> in **Figure 12-39 Flowchart of Master Reception (in Continuous Reception Mode)**.

**2.** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01

Figure 12-39. Flowchart of Master Reception (in Continuous Reception Mode)



**Remark** <1> to <8> in the figure correspond to <1> to <8> in **Figure 12-38 Timing Chart of Master Reception (in Continuous Reception Mode)**.

### 12.5.3 Master transmission/reception

Master transmission/reception is that the RL78/L12 outputs a transfer clock and transmits/receives data to/from other device.

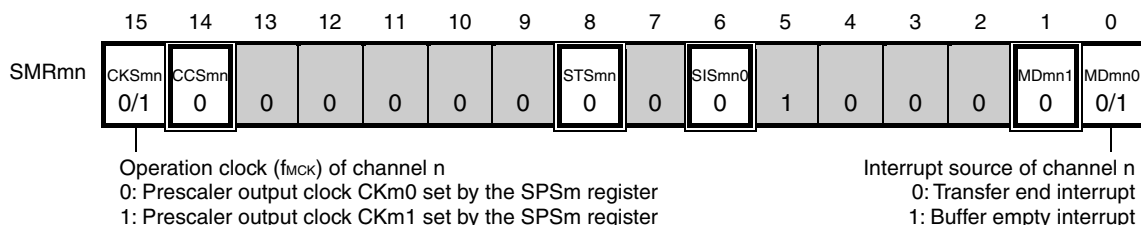
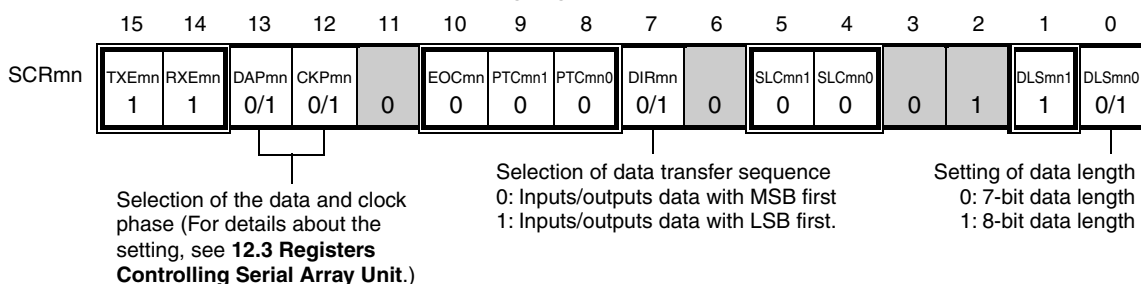
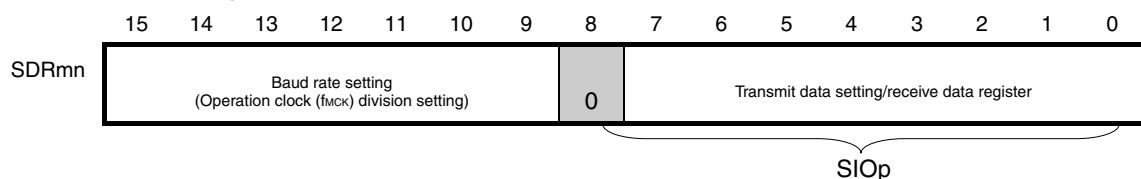
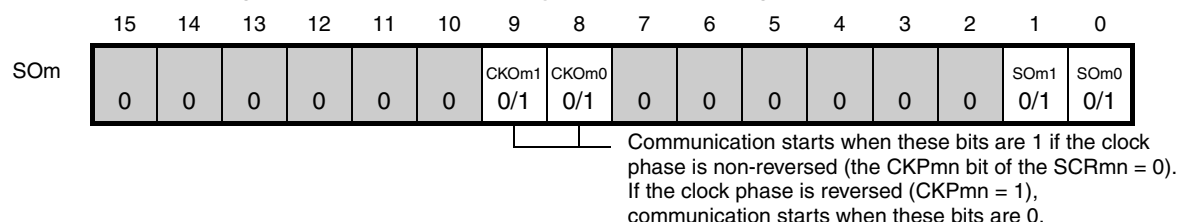
<R>

| 3-Wire Serial I/O    | CSI00                                                                                                                                                                                                                                                                                  | CSI01             |
|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|
| Target channel       | Channel 0                                                                                                                                                                                                                                                                              | Channel 1         |
| Pins used            | SCK00, SI00, SO00                                                                                                                                                                                                                                                                      | SCK01, SI01, SO01 |
| Interrupt            | INTCSI00                                                                                                                                                                                                                                                                               | INTCSI01          |
|                      | Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.                                                                                                                                                              |                   |
| Error detection flag | Overrun error detection flag (OVFmn) only                                                                                                                                                                                                                                              |                   |
| Transfer data length | 7 or 8 bits                                                                                                                                                                                                                                                                            |                   |
| Transfer rate        | Max. $f_{MCK}/2$ [Hz] (CSI00), $f_{MCK}/4$ [Hz] (CSI01)<br>Min. $f_{CLK}/(2 \times 2^{15} \times 128)$ [Hz] <sup>Note</sup> $f_{CLK}$ : System clock frequency                                                                                                                         |                   |
| Data phase           | Selectable by the DAPmn bit of the SCRmn register <ul style="list-style-type: none"> <li>• DAPmn = 0: Data I/O starts at the start of the operation of the serial clock.</li> <li>• DAPmn = 1: Data I/O starts half a clock before the start of the serial clock operation.</li> </ul> |                   |
| Clock phase          | Selectable by the CKPmn bit of the SCRmn register <ul style="list-style-type: none"> <li>• CKPmn = 0: Non-reverse</li> <li>• CKPmn = 1: Reverse</li> </ul>                                                                                                                             |                   |
| Data direction       | MSB or LSB first                                                                                                                                                                                                                                                                       |                   |

**Note** Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS**).

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01

## (1) Register setting

**Figure 12-40. Example of Contents of Registers for Master Transmission/Reception of 3-Wire Serial I/O (CSI00, CSI01) (1/2)****(a) Serial mode register mn (SMRmn)****(b) Serial communication operation setting register mn (SCRmn)****(c) Serial data register mn (SDRmn) (lower 8 bits: SI0p)****(d) Serial output register m (S0m) ... Sets only the bits of the target channel.**

- Remarks**
- m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01
  - : Setting is fixed in the CSI master transmission/reception mode  
 ■: Setting disabled (set to the initial value)  
 ×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)  
 0/1: Set to 0 or 1 depending on the usage of the user

**Figure 12-40. Example of Contents of Registers for Master Transmission/Reception of 3-Wire Serial I/O (CSI00, CSI01) (2/2)**

**(e) Serial output enable register m (SOEm) ... Sets only the bits of the target channel to 1.**

|      |    |    |    |    |    |    |   |   |   |   |   |   |   |   |       |       |
|------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-------|-------|
|      | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0     |
| SOEm |    |    |    |    |    |    |   |   |   |   |   |   |   |   | SOEm1 | SOEm0 |
|      | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0/1   | 0/1   |

**(f) Serial channel start register m (SSm) ... Sets only the bits of the target channel to 1.**

|     |    |    |    |    |    |    |   |   |   |   |   |   |   |   |      |      |
|-----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|------|------|
|     | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0    |
| SSm |    |    |    |    |    |    |   |   |   |   |   |   |   |   | SSm1 | SSm0 |
|     | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0/1  | 0/1  |

**Remarks 1.** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01

**2.**  : Setting disabled (set to the initial value)

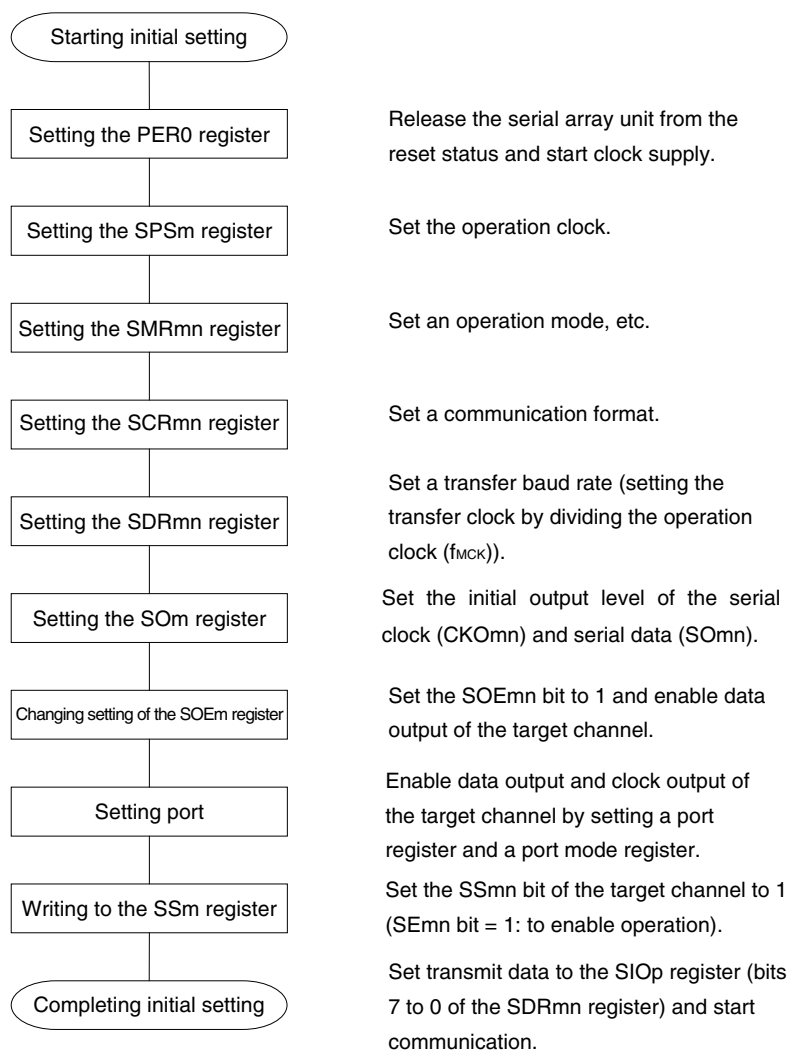
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

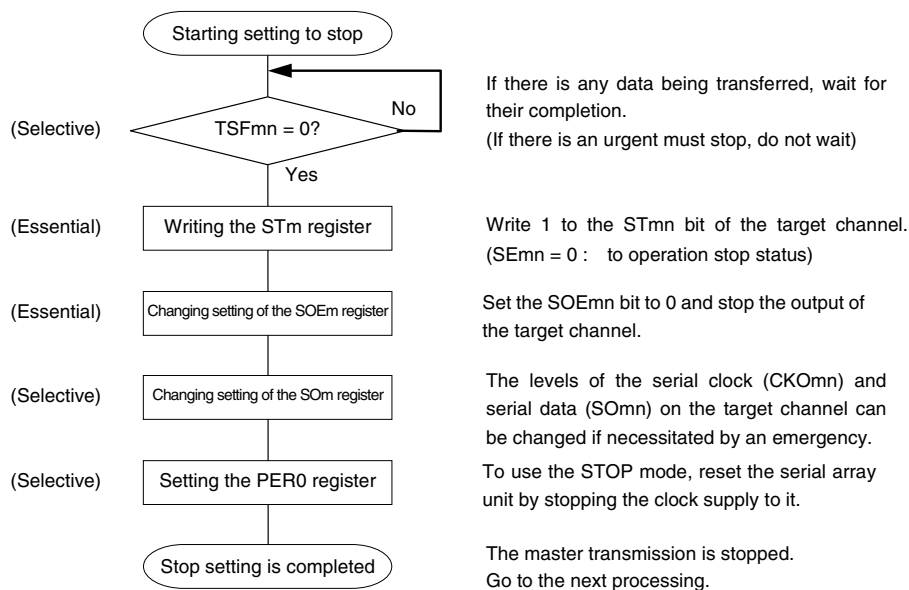
## (2) Operation procedure

&lt;R&gt;

Figure 12-41. Initial Setting Procedure for Master Transmission/Reception

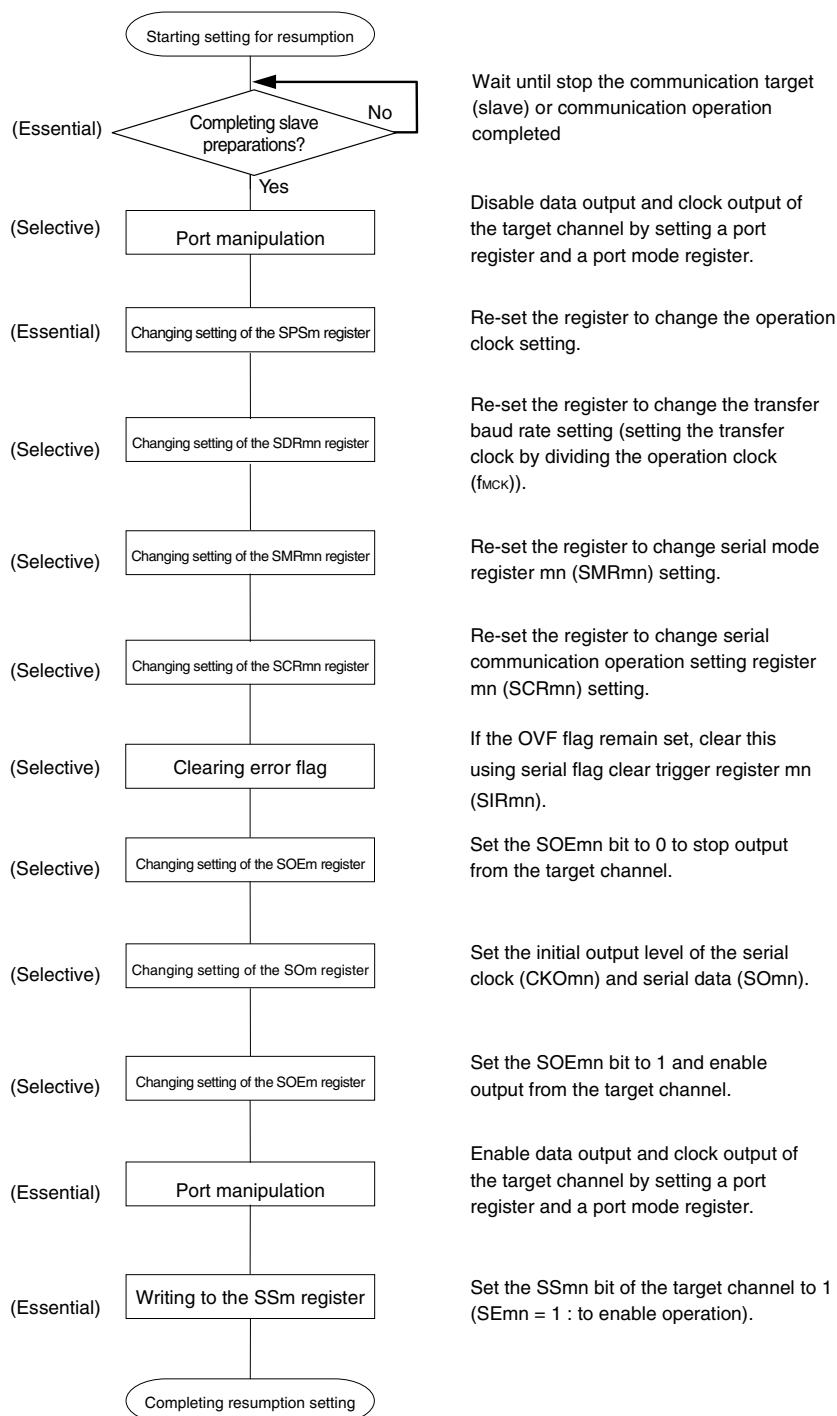


&lt;R&gt;

**Figure 12-42. Procedure for Stopping Master Transmission/Reception**

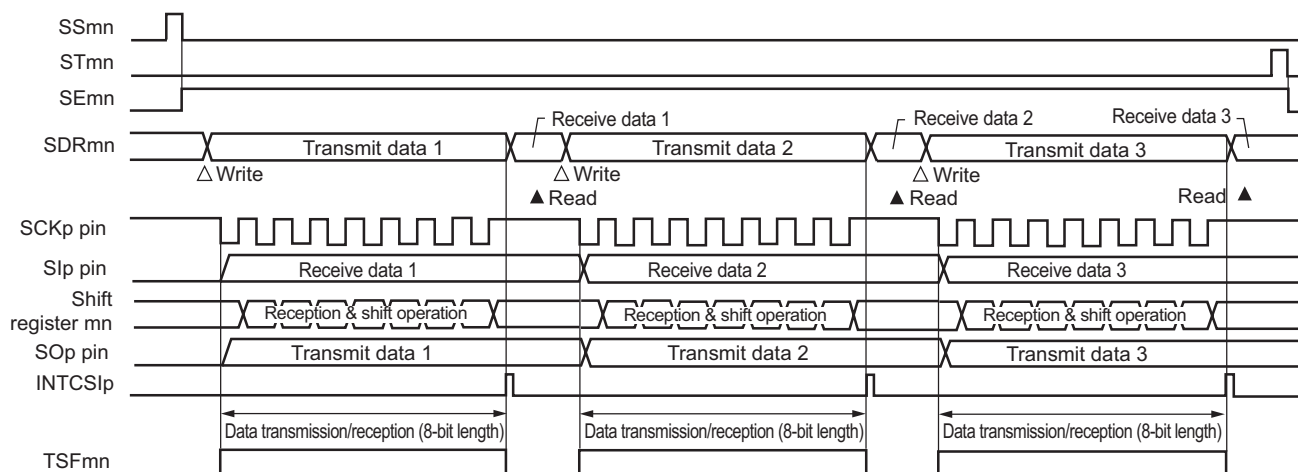


&lt;R&gt;

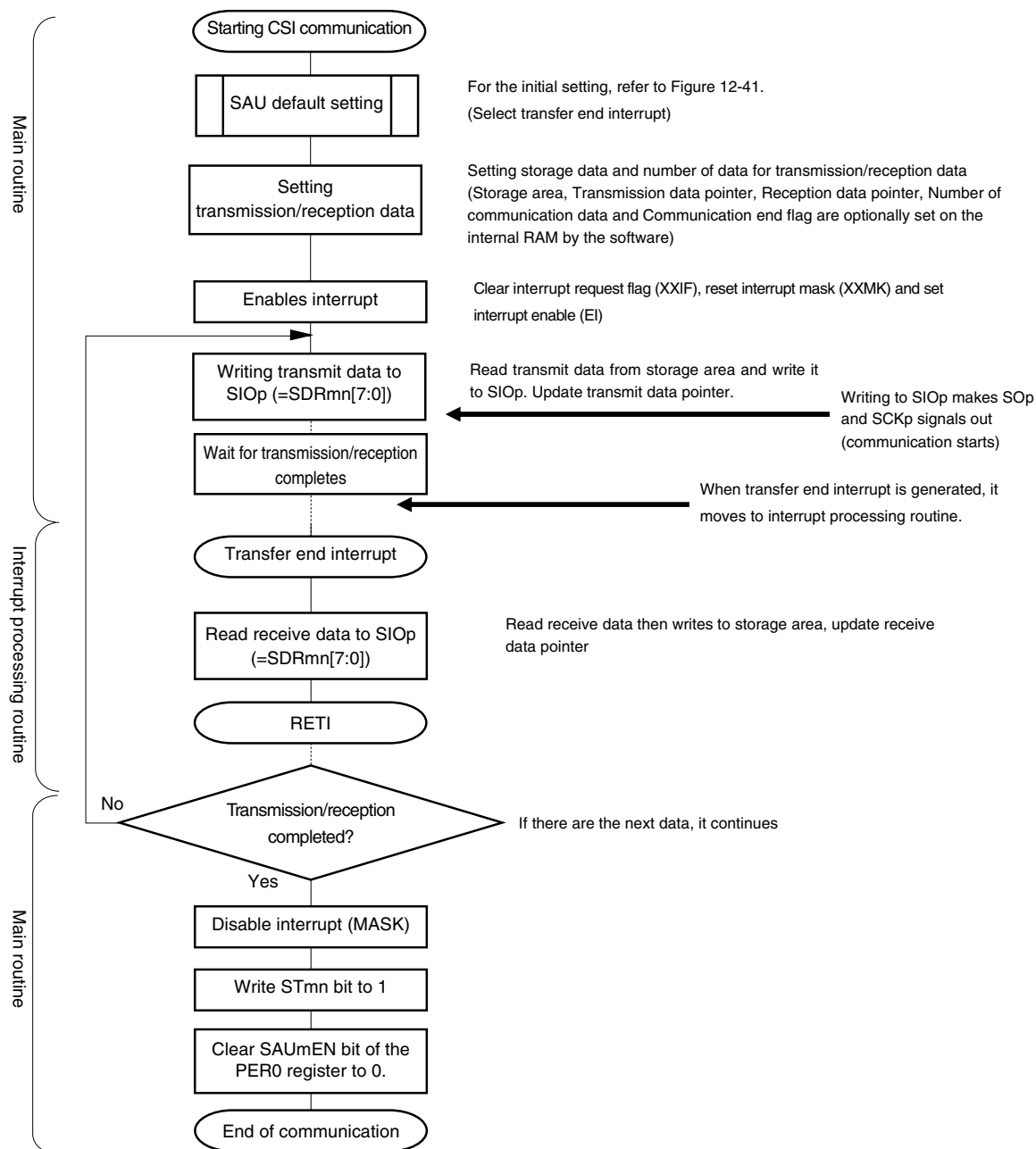
**Figure 12-43. Procedure for Resuming Master Transmission/Reception**

## (3) Processing flow (in single-transmission/reception mode)

<R> **Figure 12-44. Timing Chart of Master Transmission/Reception (in Single-Transmission/Reception Mode)**  
(Type 1: DAPmn = 0, CKPmn = 0)

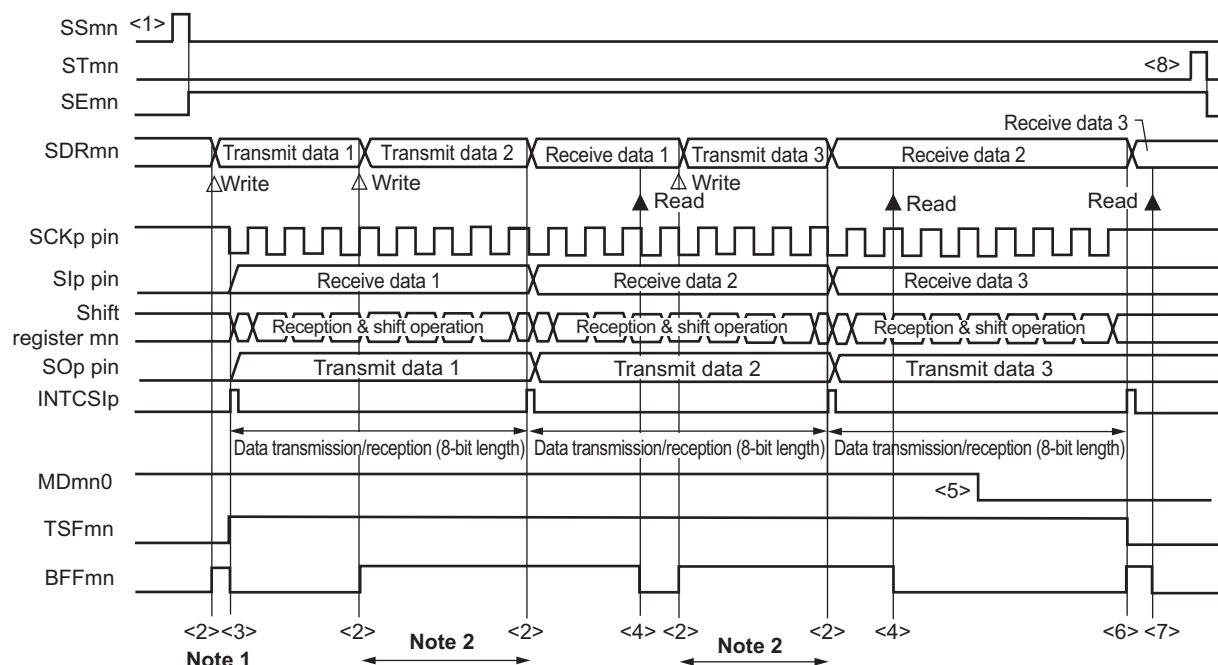


**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01

**Figure 12-45. Flowchart of Master Transmission/Reception (in Single- Transmission/Reception Mode)**

## (4) Processing flow (in continuous transmission/reception mode)

<R> **Figure 12-46. Timing Chart of Master Transmission/Reception (in Continuous Transmission/Reception Mode)**  
(Type 1: DAPmn = 0, CKPmn = 0)



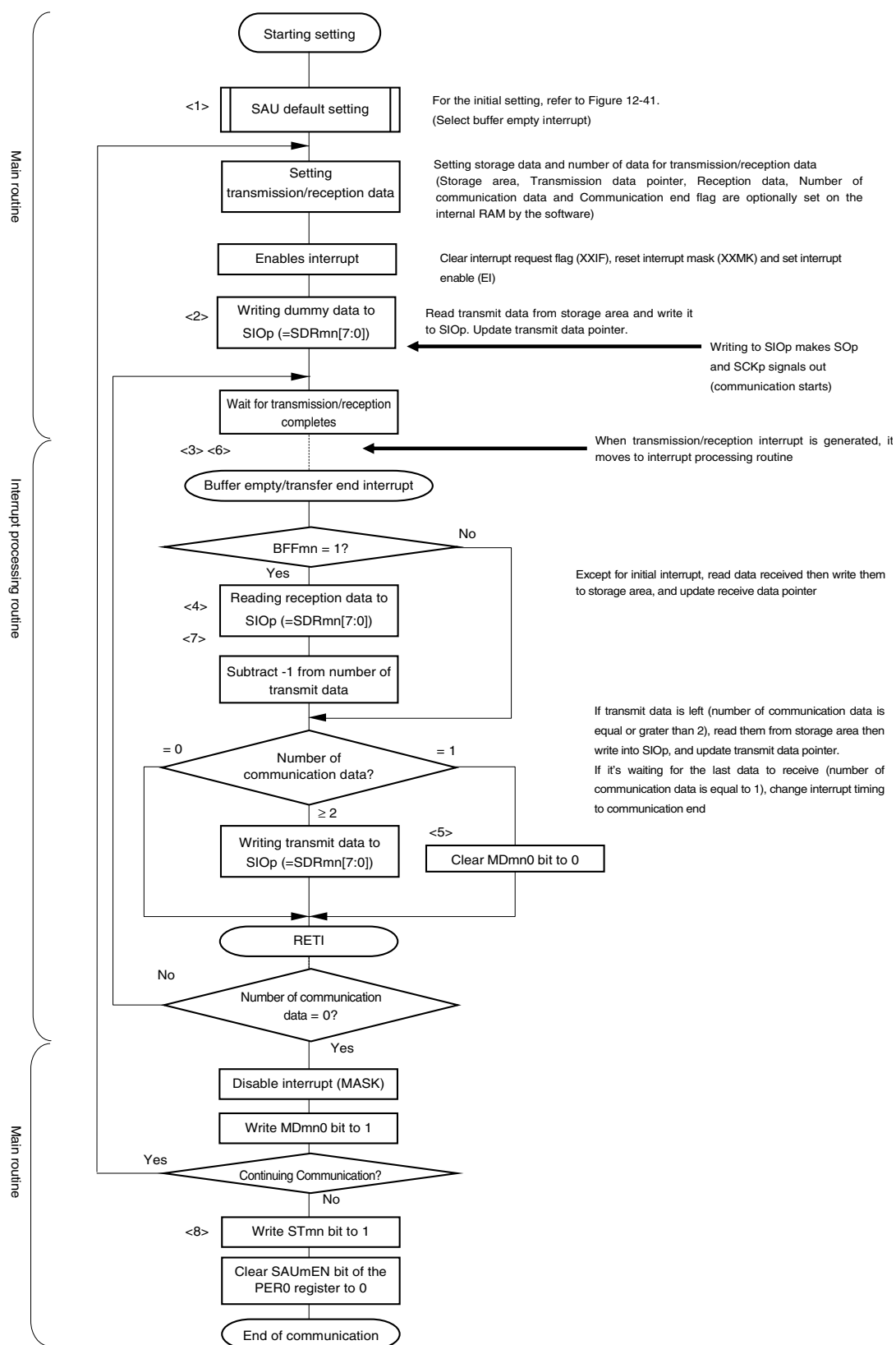
- Notes**
1. If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.
  2. The transmit data can be read by reading the SDRmn register during this period. At this time, the transfer operation is not affected.

**Caution** The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it has been rewritten before the transfer end interrupt of the last transmit data.

**Remarks** 1. <1> to <8> in the figure correspond to <1> to <8> in **Figure 12-47 Flowchart of Master Transmission/Reception (in Continuous Transmission/Reception Mode)**.

2. m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01

Figure 12-47. Flowchart of Master Transmission/Reception (in Continuous Transmission/Reception Mode)



**Remark** <1> to <8> in the figure correspond to <1> to <8> in **Figure 12-46 Timing Chart of Master Transmission/Reception (in Continuous Transmission/Reception Mode)**.

### 12.5.4 Slave transmission

Slave transmission is that the RL78/L12 transmits data to another device in the state of a transfer clock being input from another device.

| 3-Wire Serial I/O    | CSI00                                                                                                                                                                                                                                                                                          | CSI01                            |
|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|
| Target channel       | Channel 0                                                                                                                                                                                                                                                                                      | Channel 1                        |
| Pins used            | $\overline{\text{SCK00}}$ , SO00                                                                                                                                                                                                                                                               | $\overline{\text{SCK01}}$ , SO01 |
| Interrupt            | INTCSI00                                                                                                                                                                                                                                                                                       | INTCSI01                         |
|                      | Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.                                                                                                                                                                      |                                  |
| Error detection flag | Overrun error detection flag (OVFmn) only                                                                                                                                                                                                                                                      |                                  |
| Transfer data length | 7 or 8 bits                                                                                                                                                                                                                                                                                    |                                  |
| Transfer rate        | Max. $f_{\text{MCK}}/6$ [Hz] <sup>Notes 1, 2</sup>                                                                                                                                                                                                                                             |                                  |
| Data phase           | Selectable by the DAPmn bit of the SCRmn register <ul style="list-style-type: none"> <li>• DAPmn = 0: Data output starts from the start of the operation of the serial clock.</li> <li>• DAPmn = 1: Data output starts half a clock before the start of the serial clock operation.</li> </ul> |                                  |
| Clock phase          | Selectable by the CKPmn bit of the SCRmn register <ul style="list-style-type: none"> <li>• CKPmn = 0: Non-reverse</li> <li>• CKPmn = 1: Reverse</li> </ul>                                                                                                                                     |                                  |
| Data direction       | MSB or LSB first                                                                                                                                                                                                                                                                               |                                  |

**Notes 1.** Because the external serial clock input to the  $\overline{\text{SCK00}}$ , and  $\overline{\text{SCK01}}$  pins is sampled internally and used, the fastest transfer rate is  $f_{\text{MCK}}/6$  [Hz]. Set up the SPSm register so that this external clock is at least  $f_{\text{SCK}}/2$  as set by the SDRmn register.

**2.** Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS**).

**Remarks 1.**  $f_{\text{MCK}}$ : Operation clock frequency of target channel

$f_{\text{SCK}}$ : Serial clock frequency

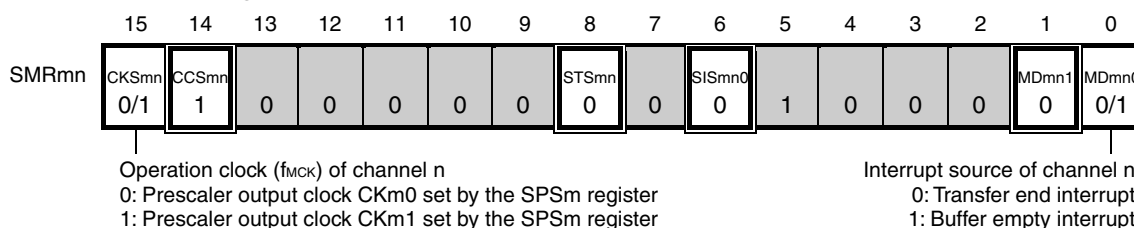
**2.** m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01

<R>

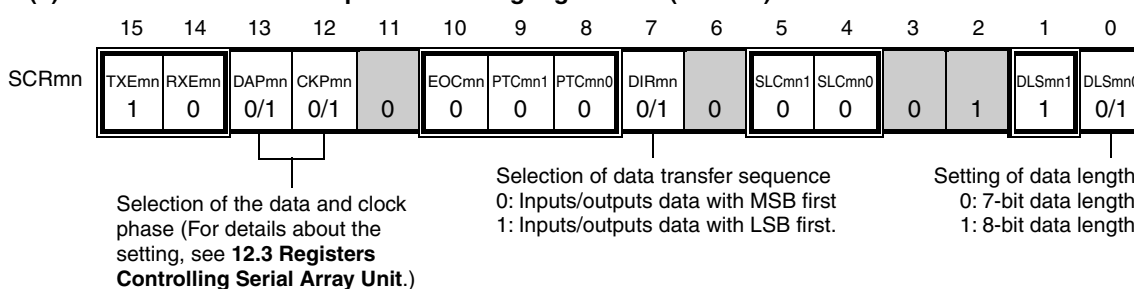
## (1) Register setting

**Figure 12-48. Example of Contents of Registers for Slave Transmission of 3-Wire Serial I/O (CSI00, CSI01) (1/2)**

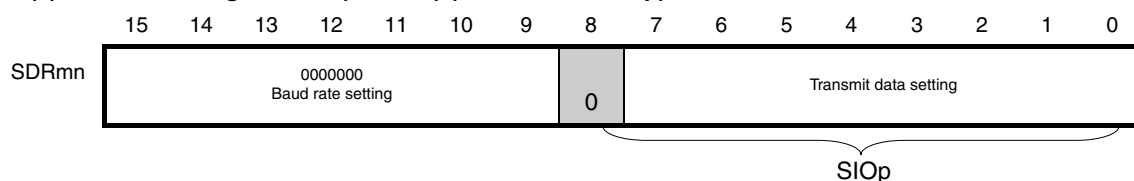
## (a) Serial mode register mn (SMRmn)



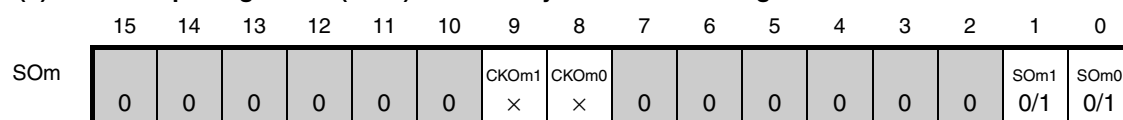
## (b) Serial communication operation setting register mn (SCRmn)



## (c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



## (d) Serial output register m (SOM) ... Sets only the bits of the target channel.



- Remarks**
- m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01
  - : Setting is fixed in the CSI slave transmission mode, ■: Setting disabled (set to the initial value)  
 ×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)  
 0/1: Set to 0 or 1 depending on the usage of the user

**Figure 12-48. Example of Contents of Registers for Slave Transmission of 3-Wire Serial I/O (CSI00, CSI01) (2/2)**

**(e) Serial output enable register m (SOEm) ... Sets only the bits of the target channel to 1.**

|      |    |    |    |    |    |    |   |   |   |   |   |   |   |   |              |              |
|------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|--------------|--------------|
|      | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1            | 0            |
| SOEm | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SOEm1<br>0/1 | SOEm0<br>0/1 |

**(f) Serial channel start register m (SSm) ... Sets only the bits of the target channel to 1.**

|     |    |    |    |    |    |    |   |   |   |   |   |   |   |   |             |             |
|-----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-------------|-------------|
|     | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1           | 0           |
| SSm | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SSm1<br>0/1 | SSm0<br>0/1 |

**Remarks 1.** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01

**2.** : Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

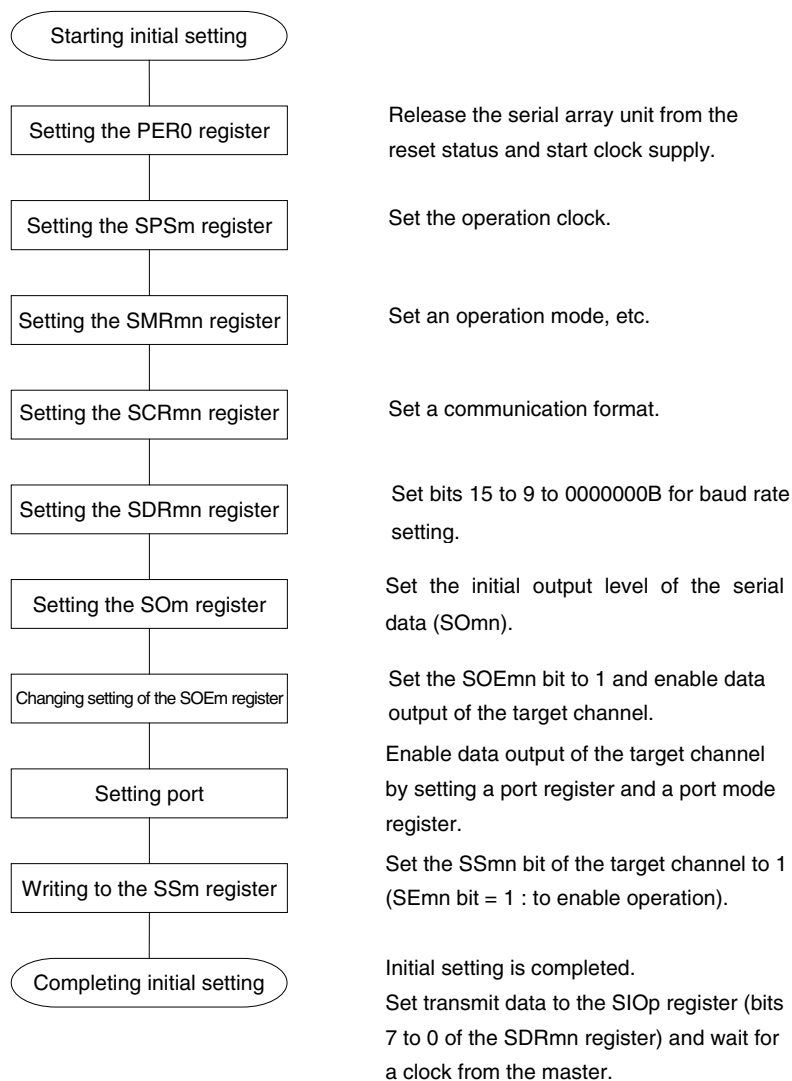
0/1: Set to 0 or 1 depending on the usage of the user



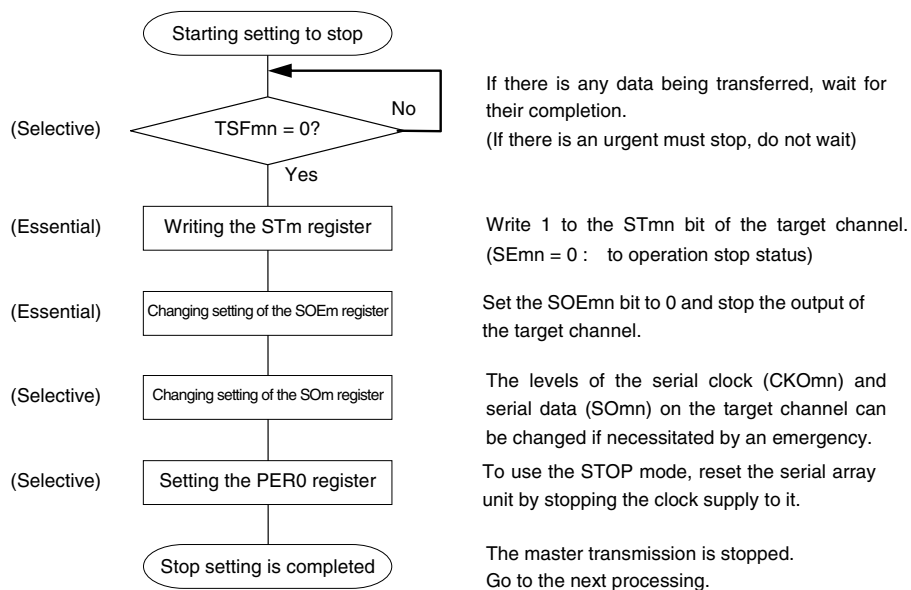
## (2) Operation procedure

&lt;R&gt;

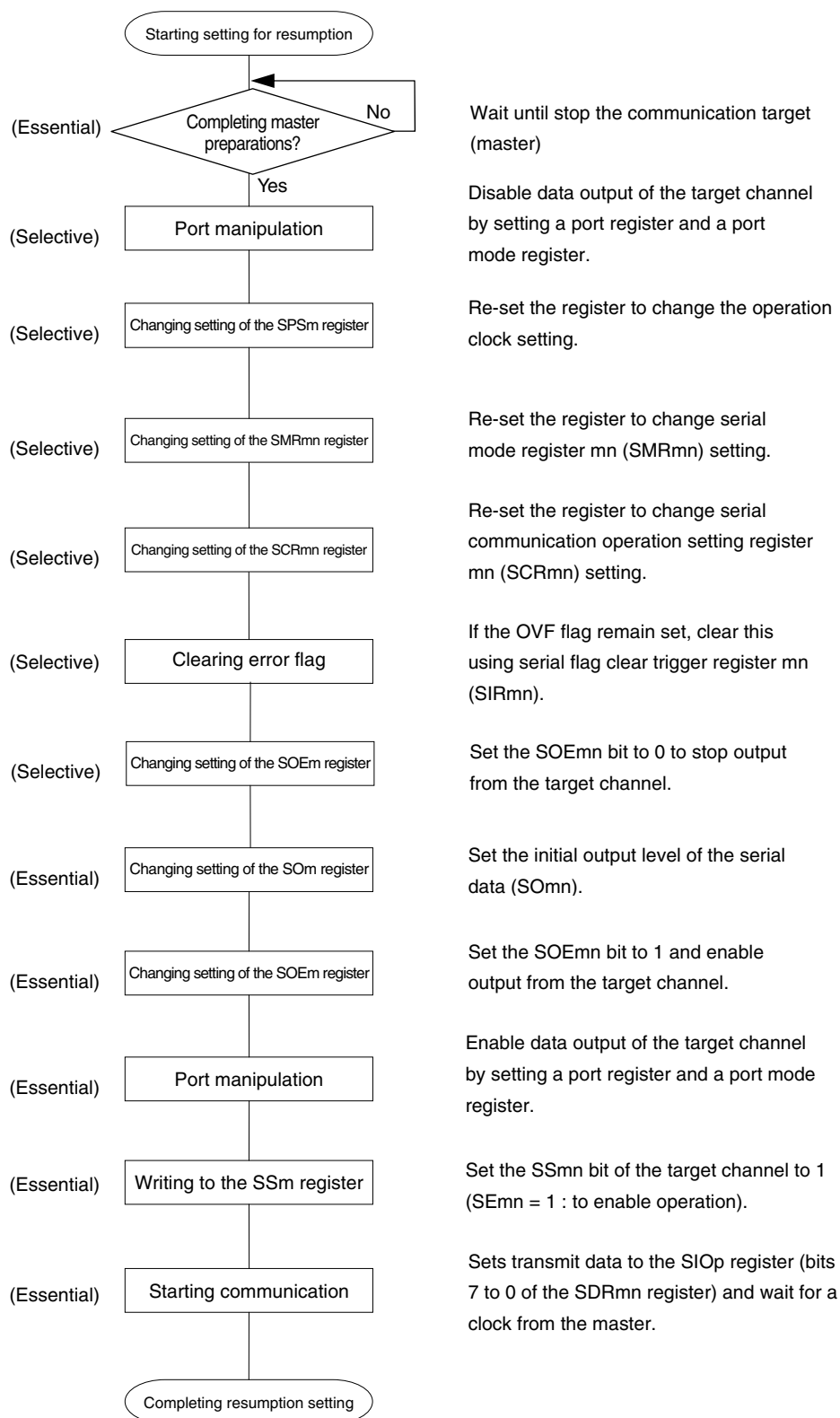
Figure 12-49. Initial Setting Procedure for Slave Transmission



&lt;R&gt;

**Figure 12-50. Procedure for Stopping Slave Transmission**

&lt;R&gt;

**Figure 12-51. Procedure for Resuming Slave Transmission**

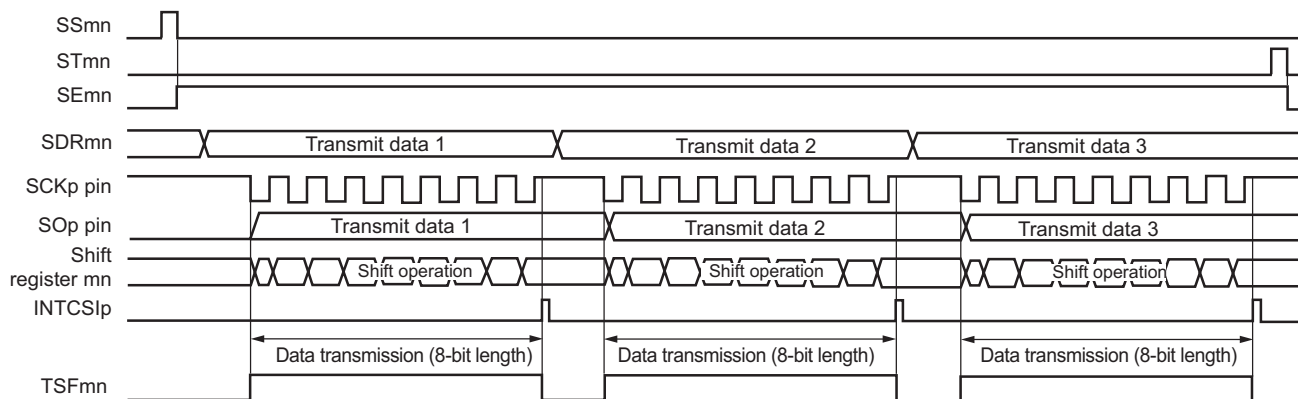
**Remark** If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (master) stops or transmission finishes, and then perform initialization instead of restarting the transmission.

## (3) Processing flow (in single-transmission mode)

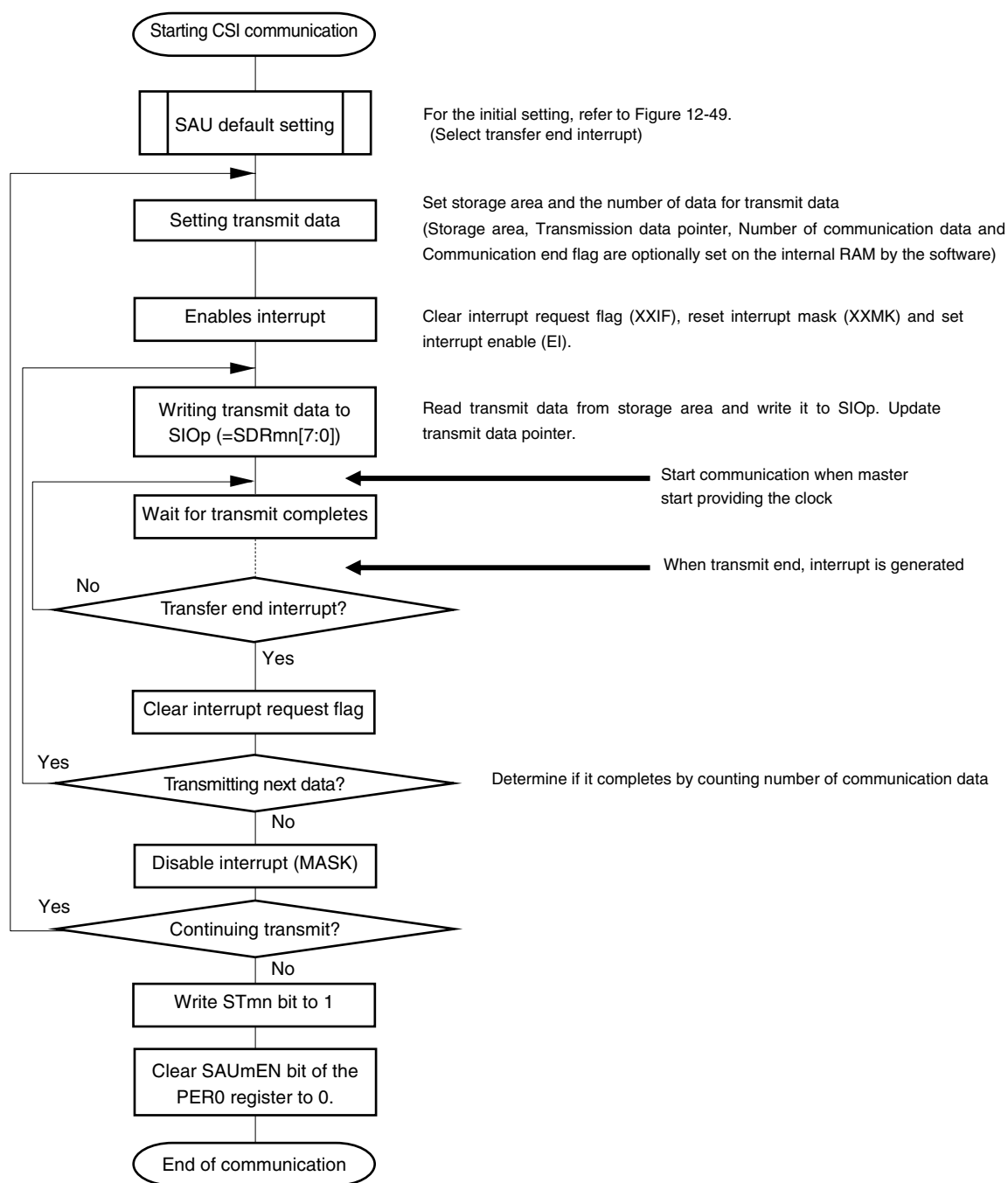
&lt;R&gt;

Figure 12-52. Timing Chart of Slave Transmission (in Single-Transmission Mode)

(Type 1: DAPmn = 0, CKPmn = 0)



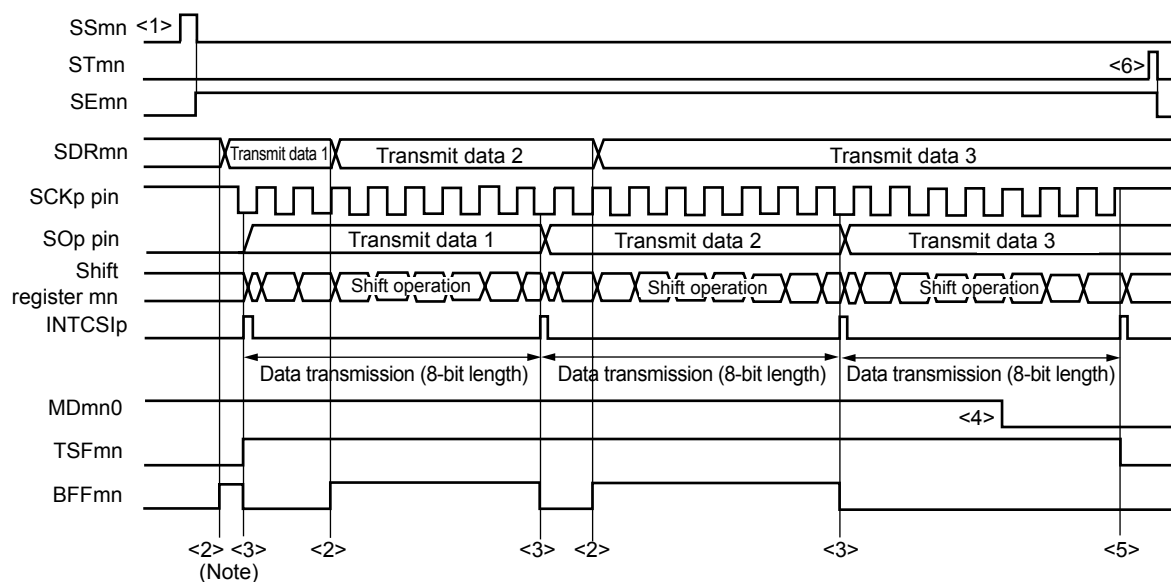
**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01

**Figure 12-53. Flowchart of Slave Transmission (in Single-Transmission Mode)**

## (4) Processing flow (in continuous transmission mode)

&lt;R&gt;

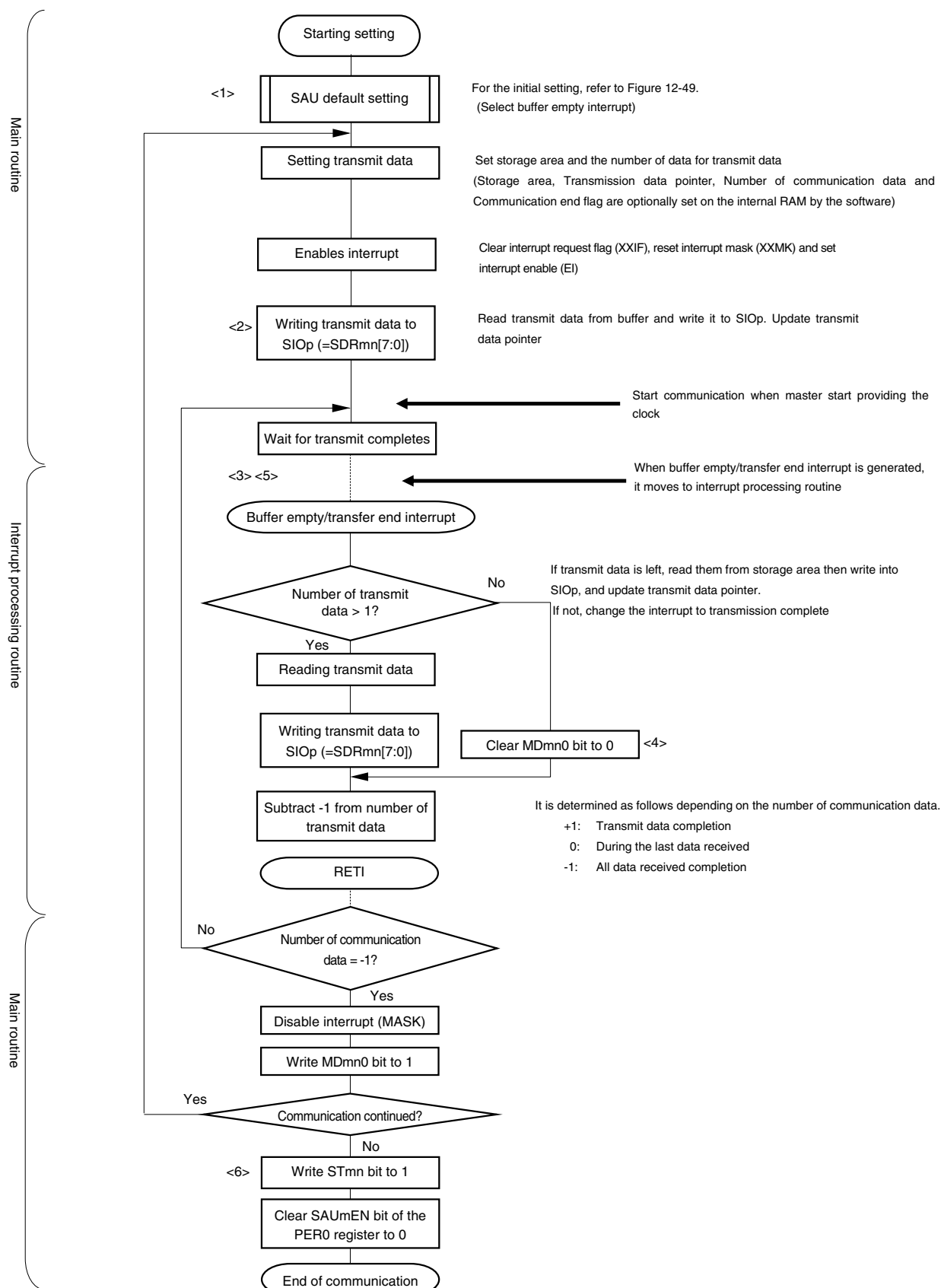
**Figure 12-54. Timing Chart of Slave Transmission (in Continuous Transmission Mode)**  
 (Type 1: DAPmn = 0, CKPmn = 0)



**Note** If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

**Caution** The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01

**Figure 12-55. Flowchart of Slave Transmission (in Continuous Transmission Mode)**

**Remark** <1> to <6> in the figure correspond to <1> to <6> in **Figure 12-54 Timing Chart of Slave Transmission (in Continuous Transmission Mode).**

### 12.5.5 Slave reception

Slave reception is that the RL78/L12 receives data from another device in the state of a transfer clock being input from another device.

| 3-Wire Serial I/O    | CSI00                                                                                                                                                                                                                                                                                        | CSI01                            |
|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|
| Target channel       | Channel 0                                                                                                                                                                                                                                                                                    | Channel 1                        |
| Pins used            | $\overline{\text{SCK00}}$ , SI00                                                                                                                                                                                                                                                             | $\overline{\text{SCK01}}$ , SI01 |
| Interrupt            | INTCSI00                                                                                                                                                                                                                                                                                     | INTCSI01                         |
|                      | Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)                                                                                                                                                                                                              |                                  |
| Error detection flag | Overrun error detection flag (OVFmn) only                                                                                                                                                                                                                                                    |                                  |
| Transfer data length | 7 or 8 bits                                                                                                                                                                                                                                                                                  |                                  |
| Transfer rate        | Max. $f_{\text{MCK}}/6$ [Hz] <sup>Notes 1, 2</sup>                                                                                                                                                                                                                                           |                                  |
| Data phase           | Selectable by the DAPmn bit of the SCRmn register <ul style="list-style-type: none"> <li>• DAPmn = 0: Data input starts from the start of the operation of the serial clock.</li> <li>• DAPmn = 1: Data input starts half a clock before the start of the serial clock operation.</li> </ul> |                                  |
| Clock phase          | Selectable by the CKPmn bit of the SCRmn register <ul style="list-style-type: none"> <li>• CKPmn = 0: Non-reverse</li> <li>• CKPmn = 1: Reverse</li> </ul>                                                                                                                                   |                                  |
| Data direction       | MSB or LSB first                                                                                                                                                                                                                                                                             |                                  |

- <R> **Notes 1.** Because the external serial clock input to the  $\overline{\text{SCK00}}$ , and  $\overline{\text{SCK01}}$  pins is sampled internally and used, the fastest transfer rate is  $f_{\text{MCK}}/6$  [Hz]. Set up the SPSm register so that this external clock is at least  $f_{\text{SCK}}/2$  as set by the SDRmn register.
- 2.** Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS**).

**Remarks 1.**  $f_{\text{MCK}}$ : Operation clock frequency of target channel

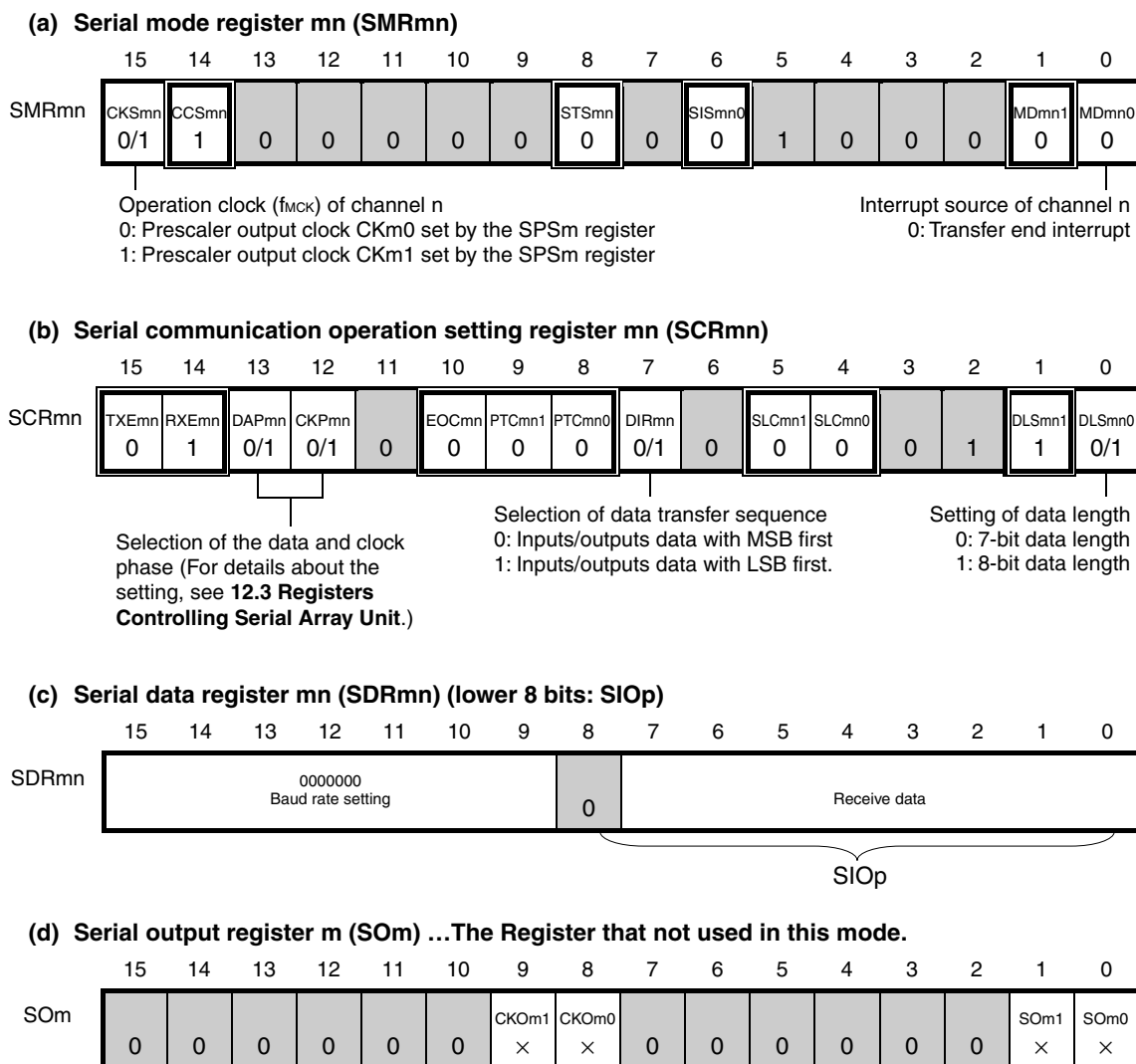
$f_{\text{SCK}}$ : Serial clock frequency

**2.** m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01



## (1) Register setting

**Figure 12-56. Example of Contents of Registers for Slave Reception of 3-Wire Serial I/O (CSI00, CSI01) (1/2)**



- Remarks**
1. m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01
  2.   : Setting is fixed in the CSI slave transmission mode,   : Setting disabled (set to the initial value)  
 ×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)  
 0/1: Set to 0 or 1 depending on the usage of the user

**Figure 12-56. Example of Contents of Registers for Slave Reception of 3-Wire Serial I/O  
(CSI00, CSI01) (2/2)**

**(e) Serial output enable register m (SOEm) ...The Register that not used in this mode.**

|      | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1          | 0          |
|------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|------------|------------|
| SOEm | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SOEm1<br>× | SOEm0<br>× |

**(f) Serial channel start register m (SSm) ... Sets only the bits of the target channel to 1.**

|     | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1           | 0           |
|-----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-------------|-------------|
| SSm | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SSm1<br>0/1 | SSm0<br>0/1 |

**Remarks 1.** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01

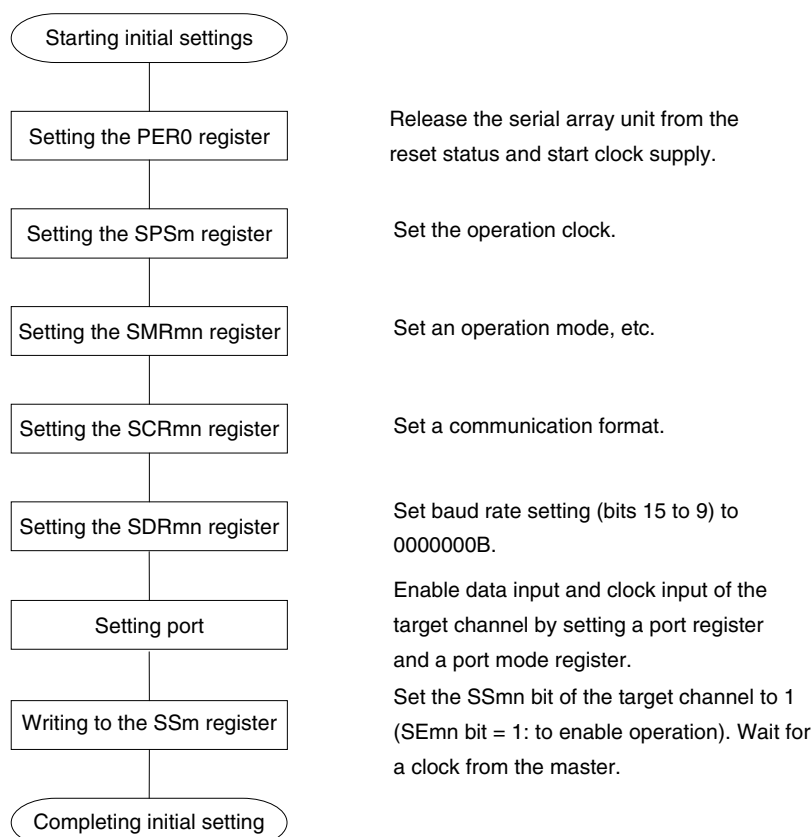
**2.**  : Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

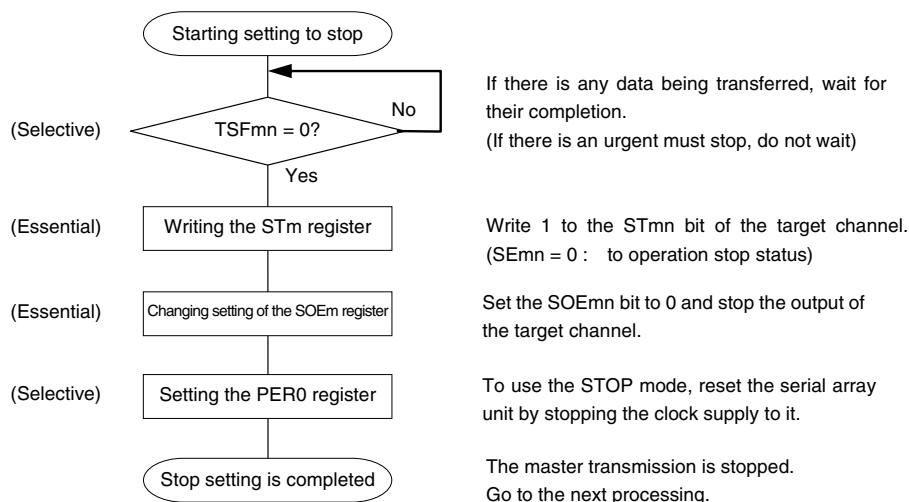
0/1: Set to 0 or 1 depending on the usage of the user

## (2) Operation procedure

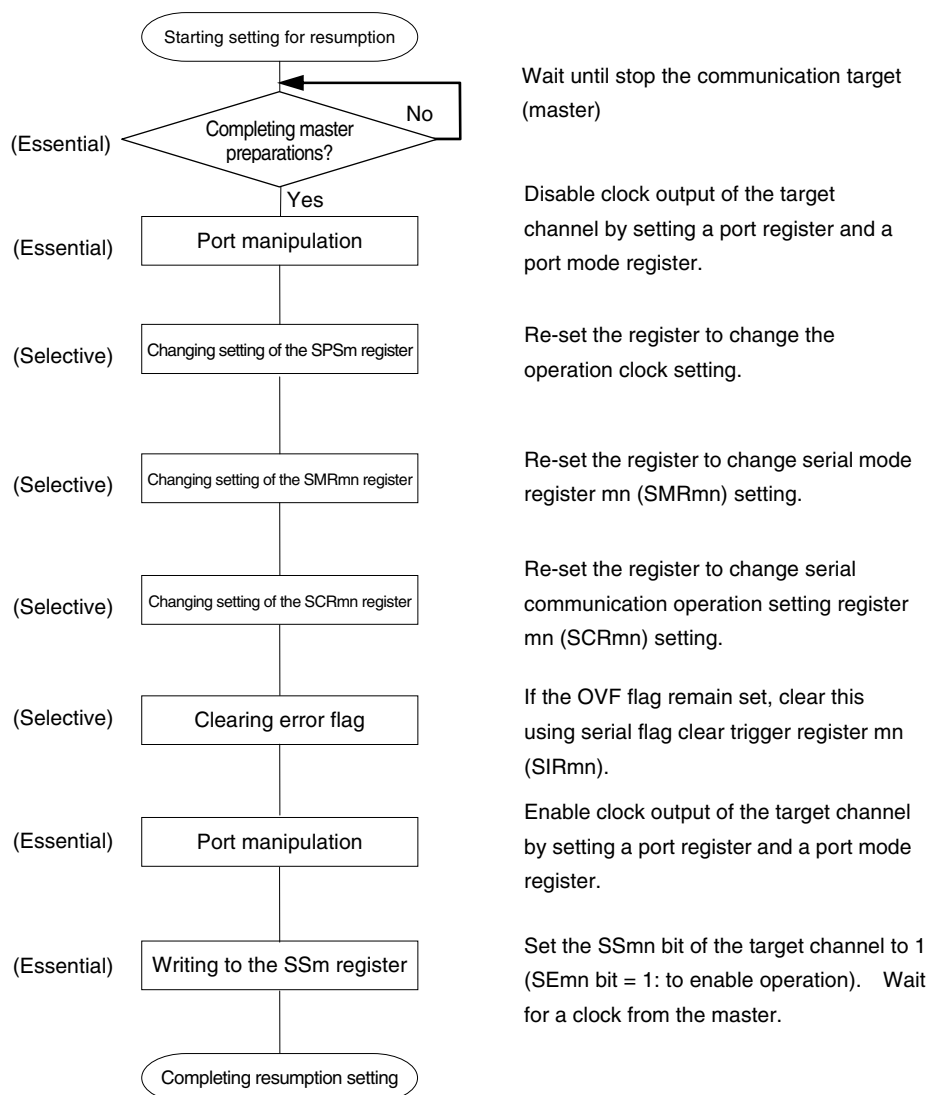
&lt;R&gt;

**Figure 12-57. Initial Setting Procedure for Slave Reception**

&lt;R&gt;

**Figure 12-58. Procedure for Stopping Slave Reception**

&lt;R&gt;

**Figure 12-59. Procedure for Resuming Slave Reception**

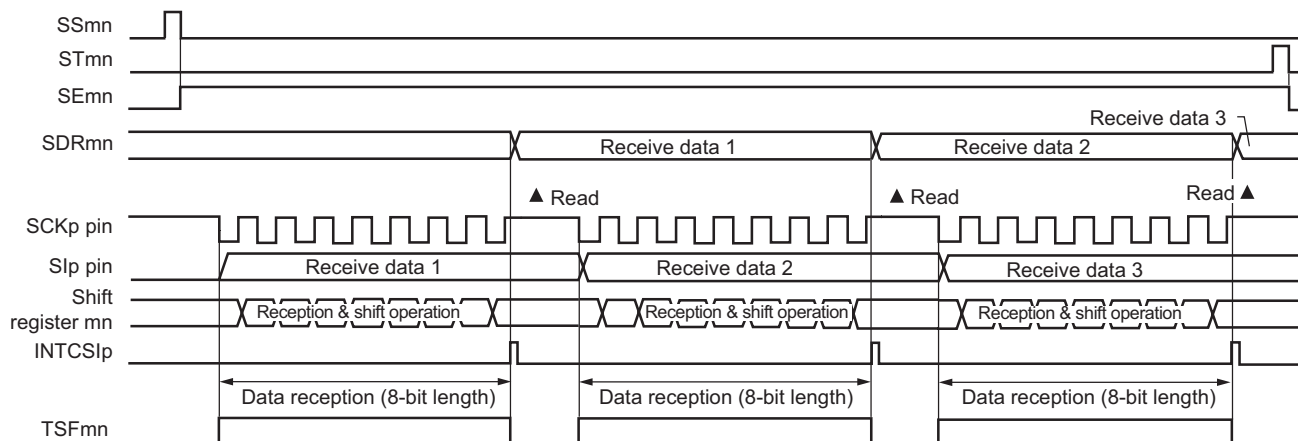
**Remark** If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (master) stops or transmission finishes, and then perform initialization instead of restarting the transmission.

## (3) Processing flow (in single-reception mode)

&lt;R&gt;

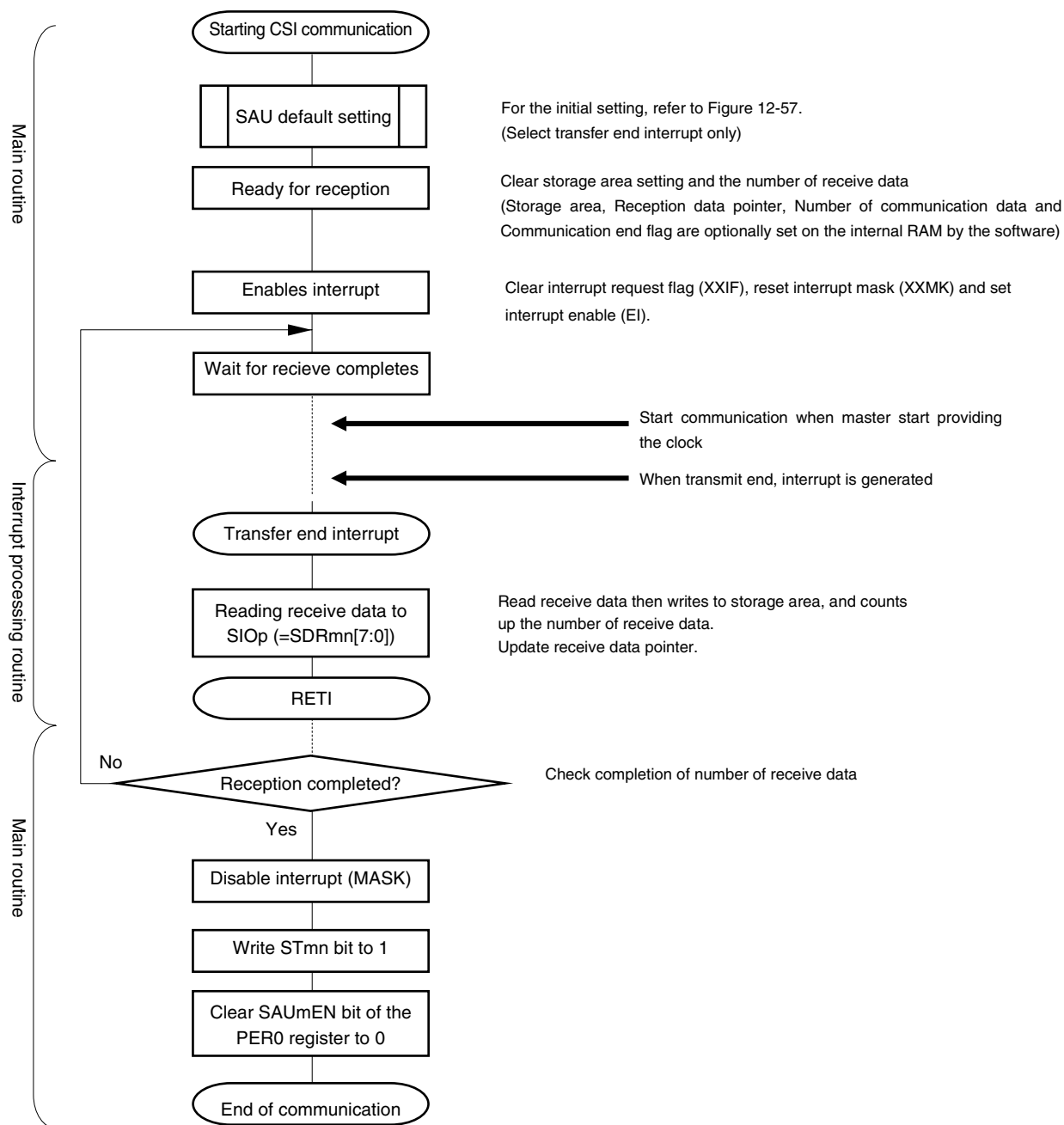
Figure 12-60. Timing Chart of Slave Reception (in Single-Reception Mode)

(Type 1: DAPmn = 0, CKPmn = 0)



**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01

Figure 12-61. Flowchart of Slave Reception (in Single-Reception Mode)



### 12.5.6 Slave transmission/reception

Slave transmission/reception is that the RL78/L12 transmits/receives data to/from another device in the state of a transfer clock being input from another device.

| 3-Wire Serial I/O    | CSI00                                                                                                                                                                                                                                                                                    | CSI01                                  |
|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|
| Target channel       | Channel 0                                                                                                                                                                                                                                                                                | Channel 1                              |
| Pins used            | $\overline{\text{SCK00}}$ , SI00, SO00                                                                                                                                                                                                                                                   | $\overline{\text{SCK01}}$ , SI01, SO01 |
| Interrupt            | INTCSI00                                                                                                                                                                                                                                                                                 | INTCSI01                               |
|                      | Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.                                                                                                                                                                |                                        |
| Error detection flag | Overrun error detection flag (OVFmn) only                                                                                                                                                                                                                                                |                                        |
| Transfer data length | 7 or 8 bits                                                                                                                                                                                                                                                                              |                                        |
| Transfer rate        | Max. $f_{\text{MCK}}/6$ [Hz] <sup>Notes 1, 2</sup>                                                                                                                                                                                                                                       |                                        |
| Data phase           | Selectable by the DAPmn bit of the SCRmn register <ul style="list-style-type: none"> <li>• DAPmn = 0: Data I/O starts from the start of the operation of the serial clock.</li> <li>• DAPmn = 1: Data I/O starts half a clock before the start of the serial clock operation.</li> </ul> |                                        |
| Clock phase          | Selectable by the CKPmn bit of the SCRmn register <ul style="list-style-type: none"> <li>• CKPmn = 0: Non-reversed</li> <li>• CKPmn = 1: Reverse</li> </ul>                                                                                                                              |                                        |
| Data direction       | MSB or LSB first                                                                                                                                                                                                                                                                         |                                        |

<R>

**Notes 1.** Because the external serial clock input to the  $\overline{\text{SCK00}}$ , and  $\overline{\text{SCK01}}$  pins is sampled internally and used, the fastest transfer rate is  $f_{\text{MCK}}/6$  [Hz]. Set up the SPSm register so that this external clock is at least  $f_{\text{SCK}}/2$  as set by the SDRmn register.

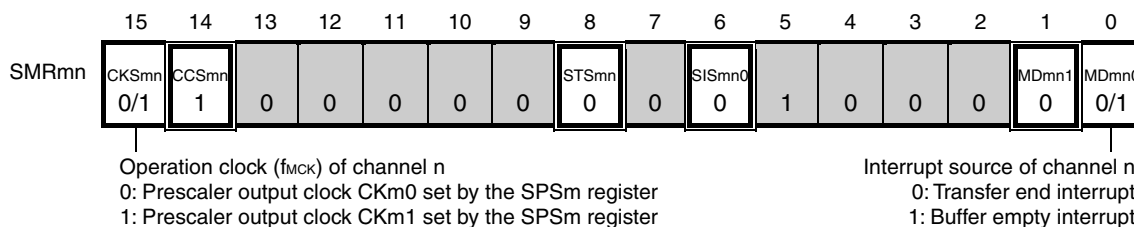
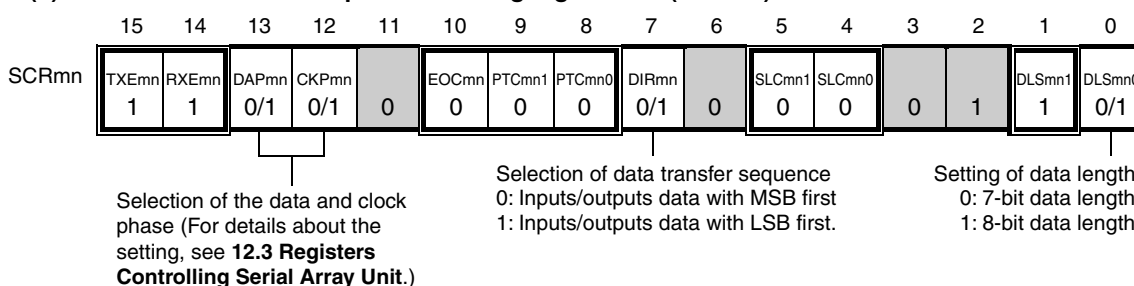
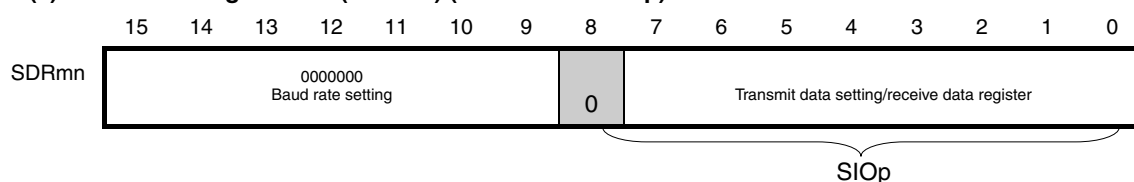
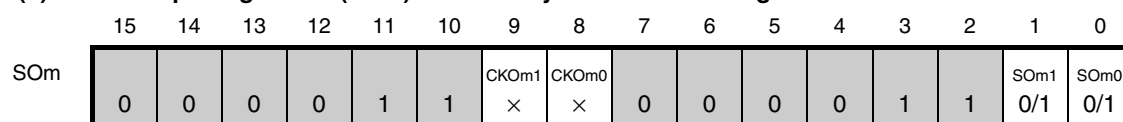
**2.** Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS**).

**Remarks 1.**  $f_{\text{MCK}}$ : Operation clock frequency of target channel

$f_{\text{SCK}}$ : Serial clock frequency

**2.** m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01

## (1) Register setting

**Figure 12-62. Example of Contents of Registers for Slave Transmission/Reception of 3-Wire Serial I/O (CSI00, CSI01) (1/2)****(a) Serial mode register mn (SMRmn)****(b) Serial communication operation setting register mn (SCRmn)****(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)****(d) Serial output register m (SOM) ... Sets only the bits of the target channel.**

**Caution** Be sure to set transmit data to the SIOp register before the clock from the master is started.

**Remarks 1.** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01

**2.**   : Setting is fixed in the CSI slave transmission/reception mode,

  : Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user



**Figure 12-62. Example of Contents of Registers for Slave Transmission/Reception of 3-Wire Serial I/O (CSI00, CSI01) (2/2)**

**(e) Serial output enable register m (SOEm) ... Sets only the bits of the target channel to 1.**

|      |    |    |    |    |    |    |   |   |   |   |   |   |   |   |              |              |
|------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|--------------|--------------|
|      | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1            | 0            |
| SOEm | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SOEm1<br>0/1 | SOEm0<br>0/1 |

**(f) Serial channel start register m (SSm) ... Sets only the bits of the target channel to 1.**

|     |    |    |    |    |    |    |   |   |   |   |   |   |   |   |             |             |
|-----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-------------|-------------|
|     | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1           | 0           |
| SSm | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SSm1<br>0/1 | SSm0<br>0/1 |

**Remarks 1.** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01

**2.**  : Setting disabled (set to the initial value)

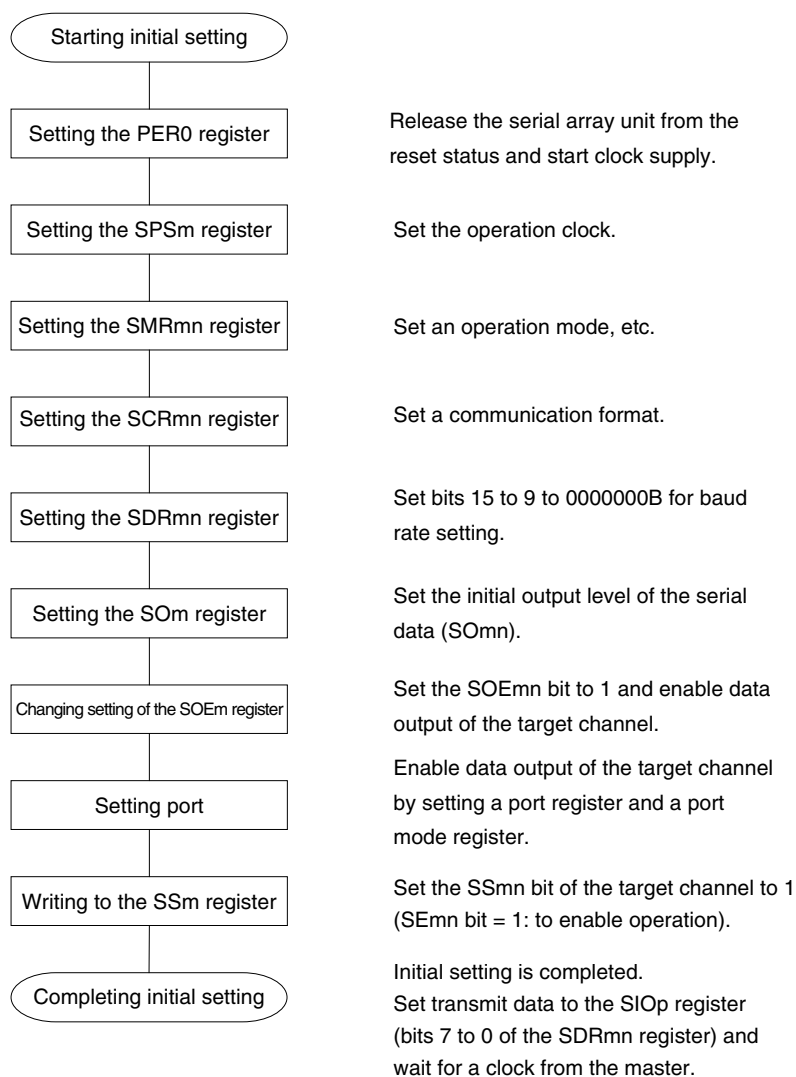
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

## (2) Operation procedure

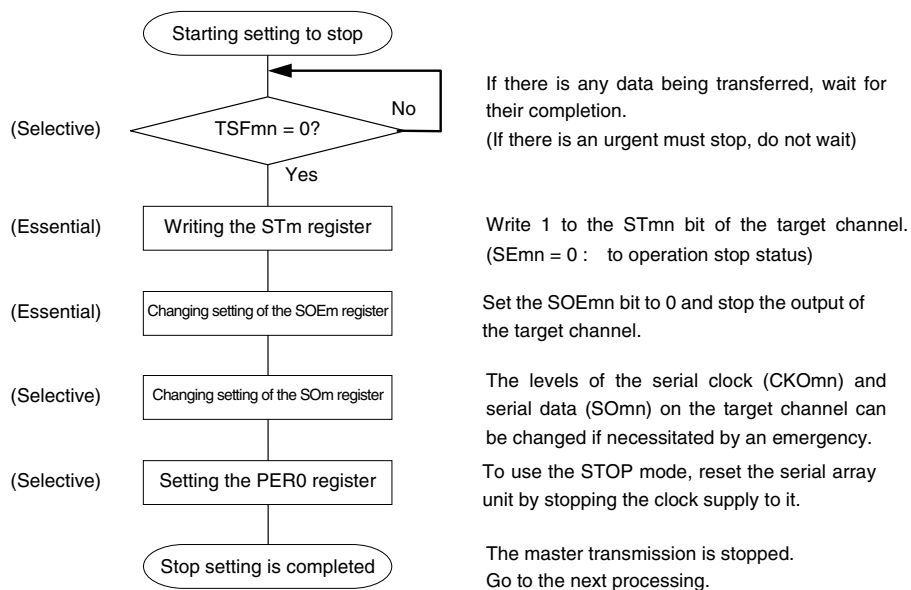
&lt;R&gt;

Figure 12-63. Initial Setting Procedure for Slave Transmission/Reception

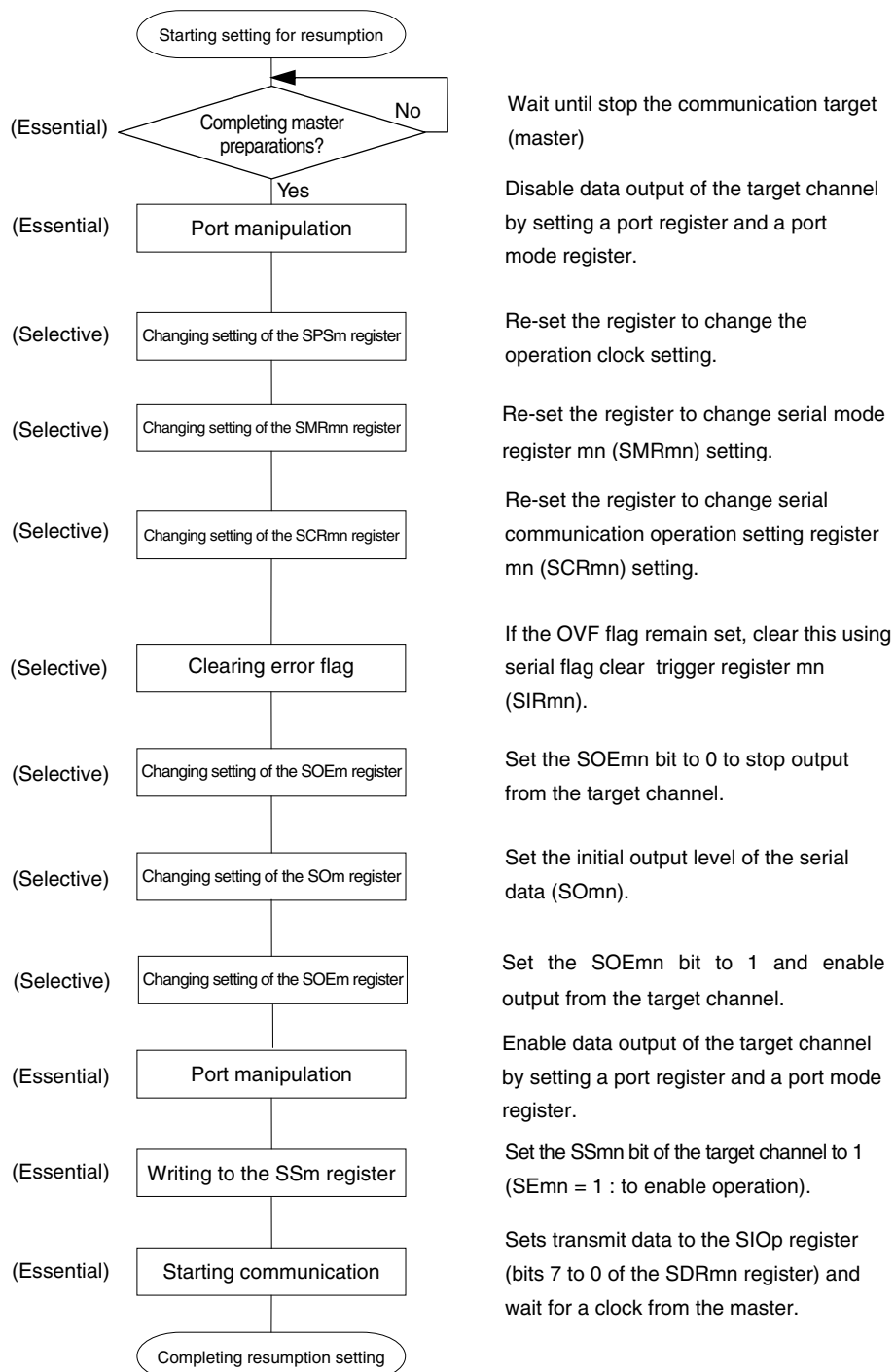


**Caution** Be sure to set transmit data to the SIOp register before the clock from the master is started.

&lt;R&gt;

**Figure 12-64. Procedure for Stopping Slave Transmission/Reception**

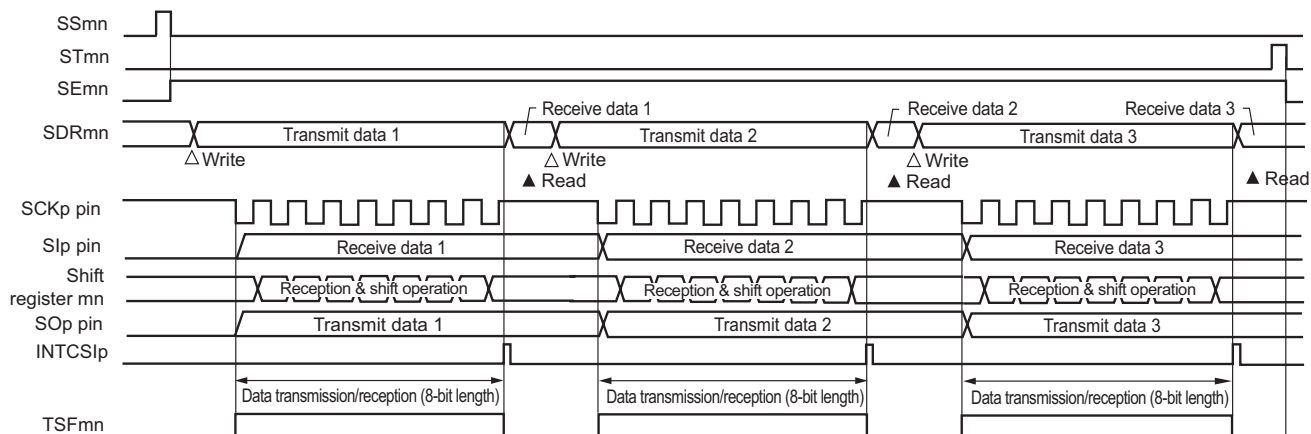
&lt;R&gt;

**Figure 12-65. Procedure for Resuming Slave Transmission/Reception**

- Cautions**
1. Be sure to set transmit data to the SIOp register before the clock from the master is started.
  2. If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (master) stops or transmission finishes, and then perform initialization instead of restarting the transmission.

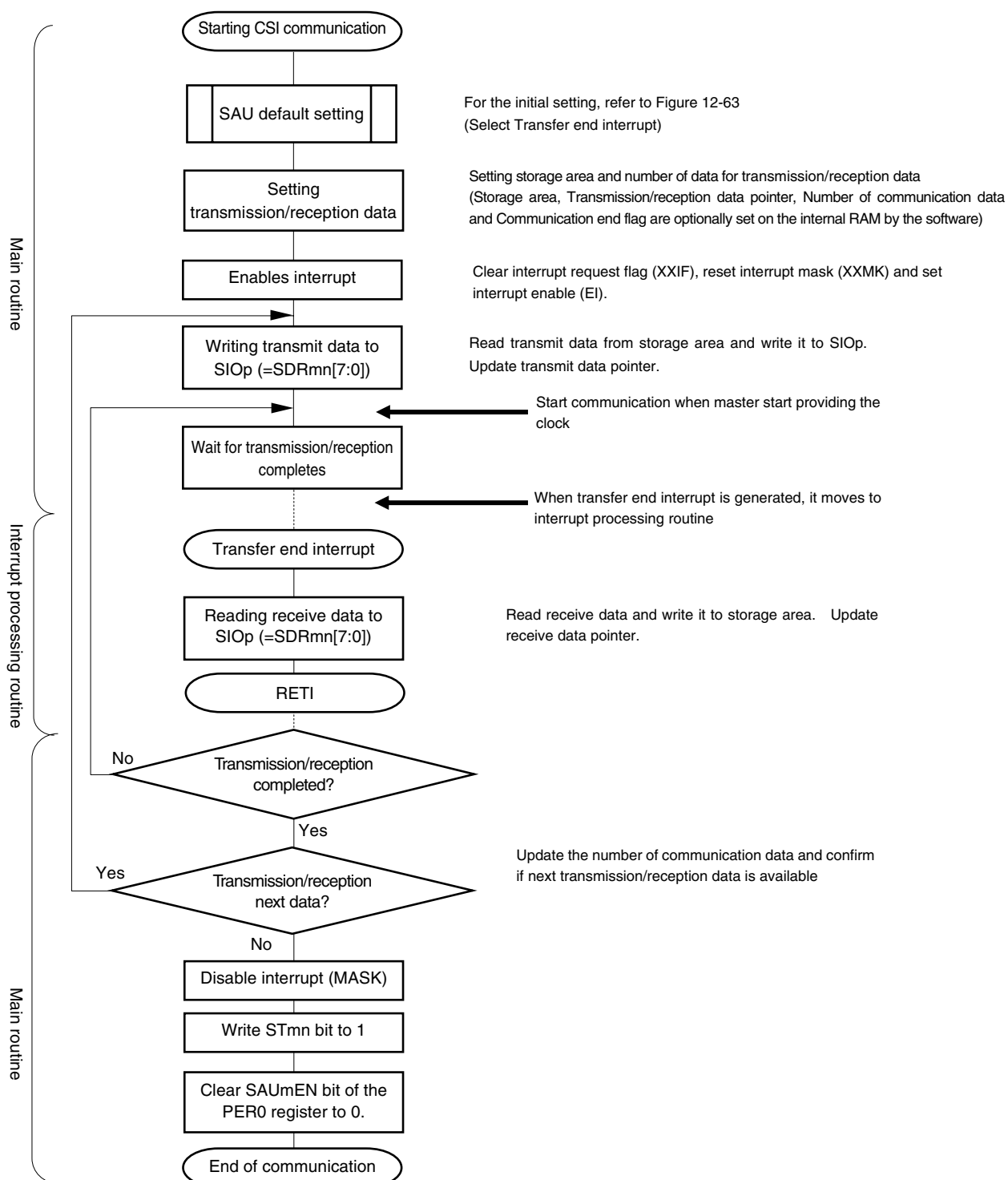
## (3) Processing flow (in single-transmission/reception mode)

<R> **Figure 12-66. Timing Chart of Slave Transmission/Reception (in Single-Transmission/Reception Mode)**  
(Type 1: DAPmn = 0, CKPmn = 0)



**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01

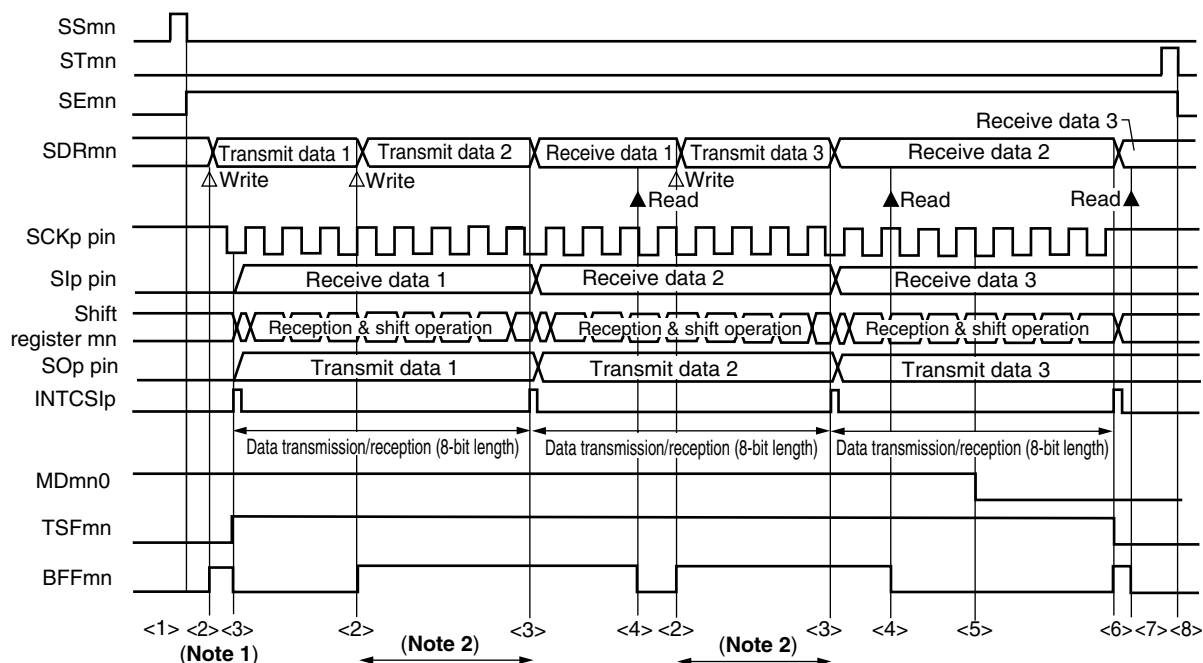
Figure 12-67. Flowchart of Slave Transmission/Reception (in Single- Transmission/Reception Mode)



**Caution** Be sure to set transmit data to the SIOp register before the clock from the master is started.

## (4) Processing flow (in continuous transmission/reception mode)

<R> **Figure 12-68. Timing Chart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)**  
(Type 1: DAPmn = 0, CKPmn = 0)



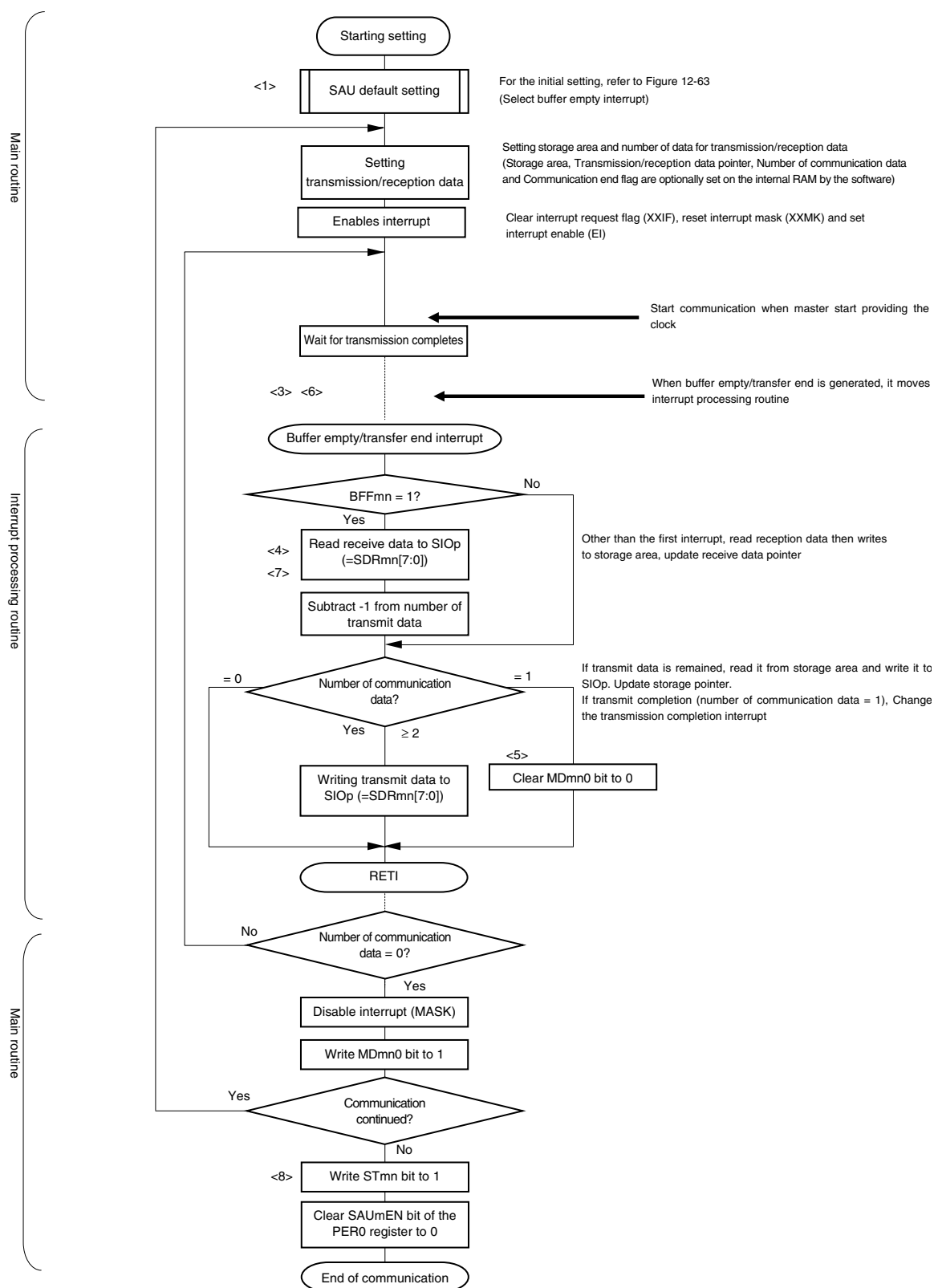
- Notes**
1. If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.
  2. The transmit data can be read by reading the SDRmn register during this period. At this time, the transfer operation is not affected.

**Caution** The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it has been rewritten before the transfer end interrupt of the last transmit data.

**Remarks** 1. <1> to <8> in the figure correspond to <1> to <8> in **Figure 12-69 Flowchart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)**.

2. m: Unit number (m = 0), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01), mn = 00, 01

Figure 12-69. Flowchart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)



**Caution** Be sure to set transmit data to the SIOp register before the clock from the master is started.

**Remark** <1> to <8> in the figure correspond to <1> to <8> in Figure 12-68 Timing Chart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode).



### 12.5.7 SNOOZE mode function

<R> SNOOZE mode makes CSI operate reception by  $\overline{\text{SCKp}}$  pin input detection while the STOP mode. Normally CSI stops communication in the STOP mode. But, using the SNOOZE mode makes reception CSI operate unless the CPU operation by detecting  $\overline{\text{SCKp}}$  pin input.

When using the SNOOZE mode function, set the SWCm bit of serial standby control register m (SSCm) to 1 just before switching to the STOP mode.

When shifting from the SNOOZE mode to operating mode, specify the register setting as below.

- If exiting the SNOOZE mode is triggered by the UART reception end interrupt:

SRMK (reception end interrupt mask bit) = 0<sup>Note 1</sup>

- If exiting the SNOOZE mode is triggered by the UART reception error interrupt:

SREMK (reception error interrupt mask bit) = 0<sup>Note 2</sup>

<R> **Notes 1.** If SRMK is 1, the UART reception end interrupt triggers shifting from the SNOOZE mode to STOP mode.

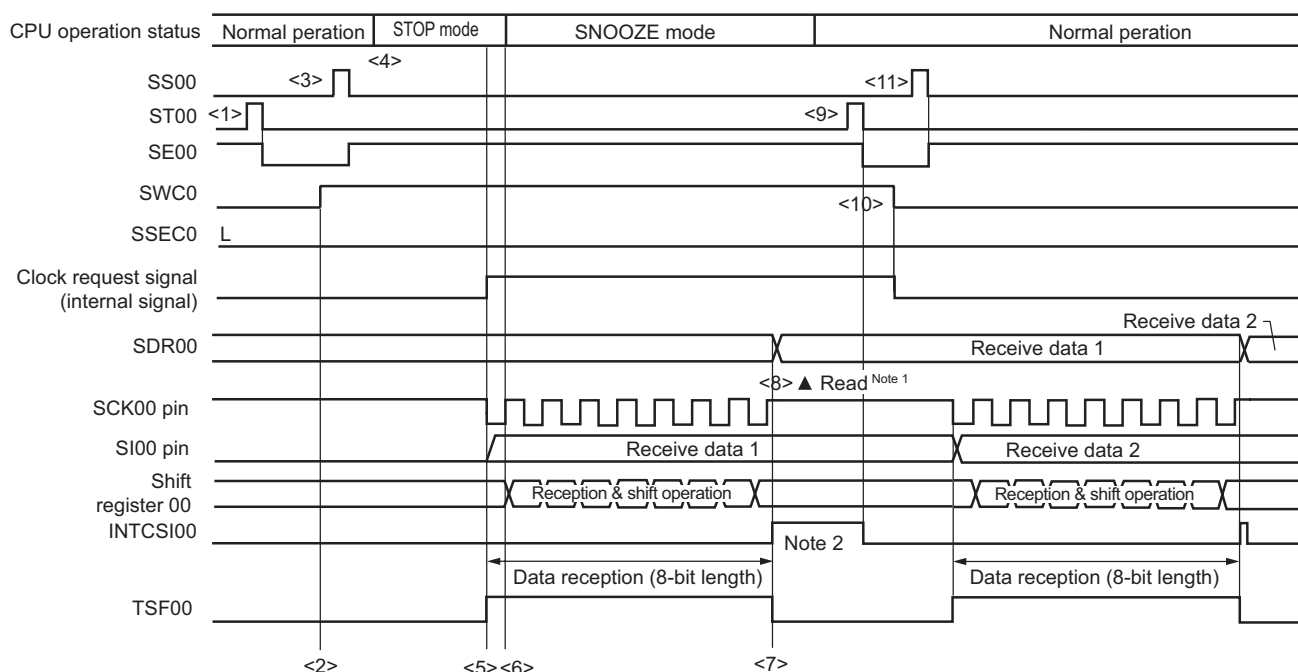
<R> **2.** If SSECm is 0 and SREMK is 1, the UART reception error interrupt does not trigger shifting of mode (the SNOOZE mode continues).

**Cautions 1. The SNOOZE mode can only be specified when the high-speed on-chip oscillator clock is selected for  $f_{\text{CLK}}$ .**

**2. The maximum transfer rate when using CSIp in the SNOOZE mode is 1 Mbps.**

## (1) SNOOZE mode operation (once startup)

Figure 12-70. Timing Chart of SNOOZE Mode Operation (once startup) (Type 1: DAPmn = 0, CKPmn = 0)



- Notes**
1. Only read received data while SWCm = 1 and before the next edge of the SCKp pin input is detected.
  2. The transfer end interrupt (INTCSIp) is cleared either when SWCm is cleared to 0 or when the next edge of the SCKp pin input is detected.

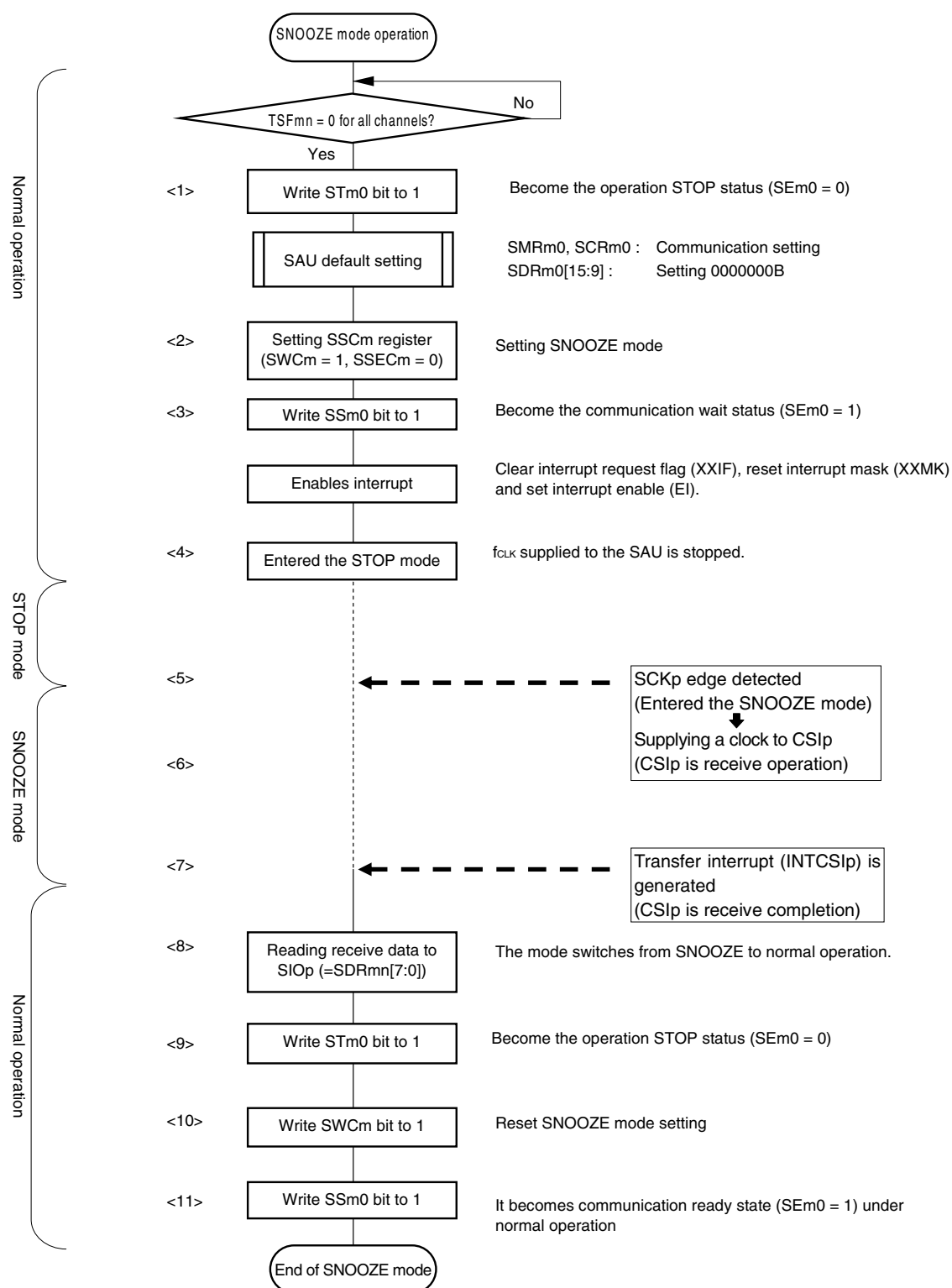
**Caution** Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the STm0 bit to 1 (clear the SEm0 bit, and stop the operation). And after completion the receive operation, also clearing SWCm bit to 0 (SNOOZE mode release).

**Remarks**

1. <1> to <11> in the figure correspond to <1> to <11> in Figure 12-71. Flowchart of SNOOZE Mode Operation (once startup).

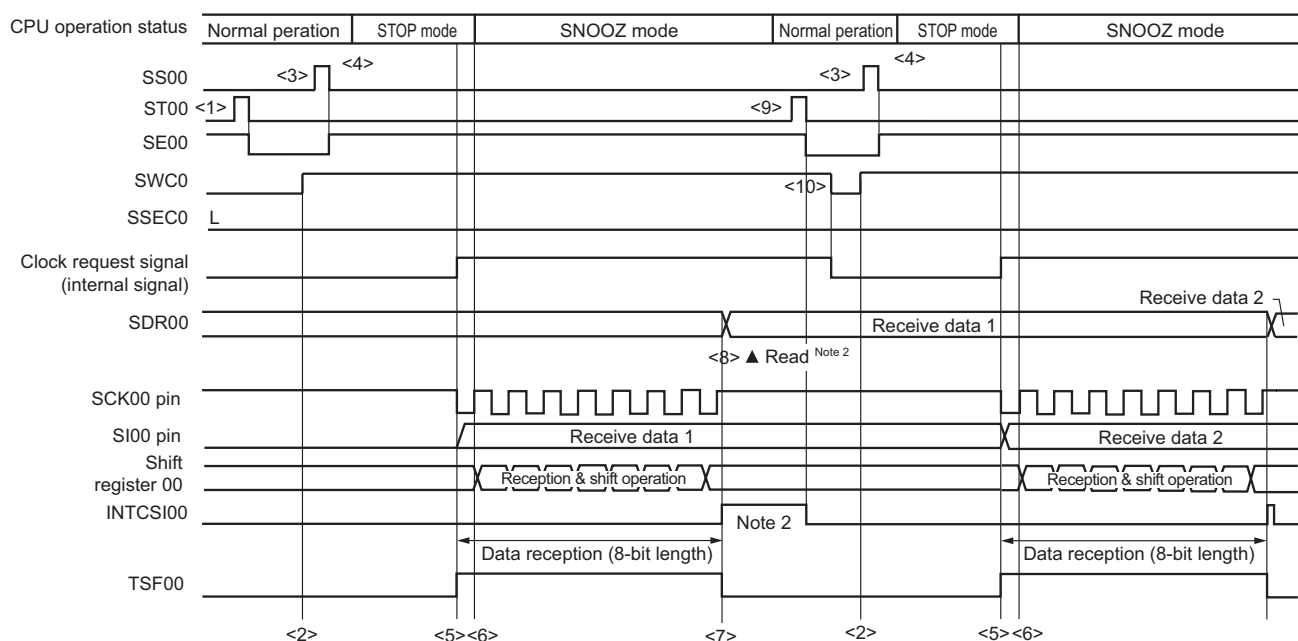
2. m = 0; p = 00

Figure 12-71. Flowchart of SNOOZE Mode Operation (once startup)



## (2) SNOOZE mode operation (continuous startup)

Figure 12-72. Timing Chart of SNOOZE Mode Operation (continuous startup) (Type 1: DAPmn = 0, CKPmn = 0)

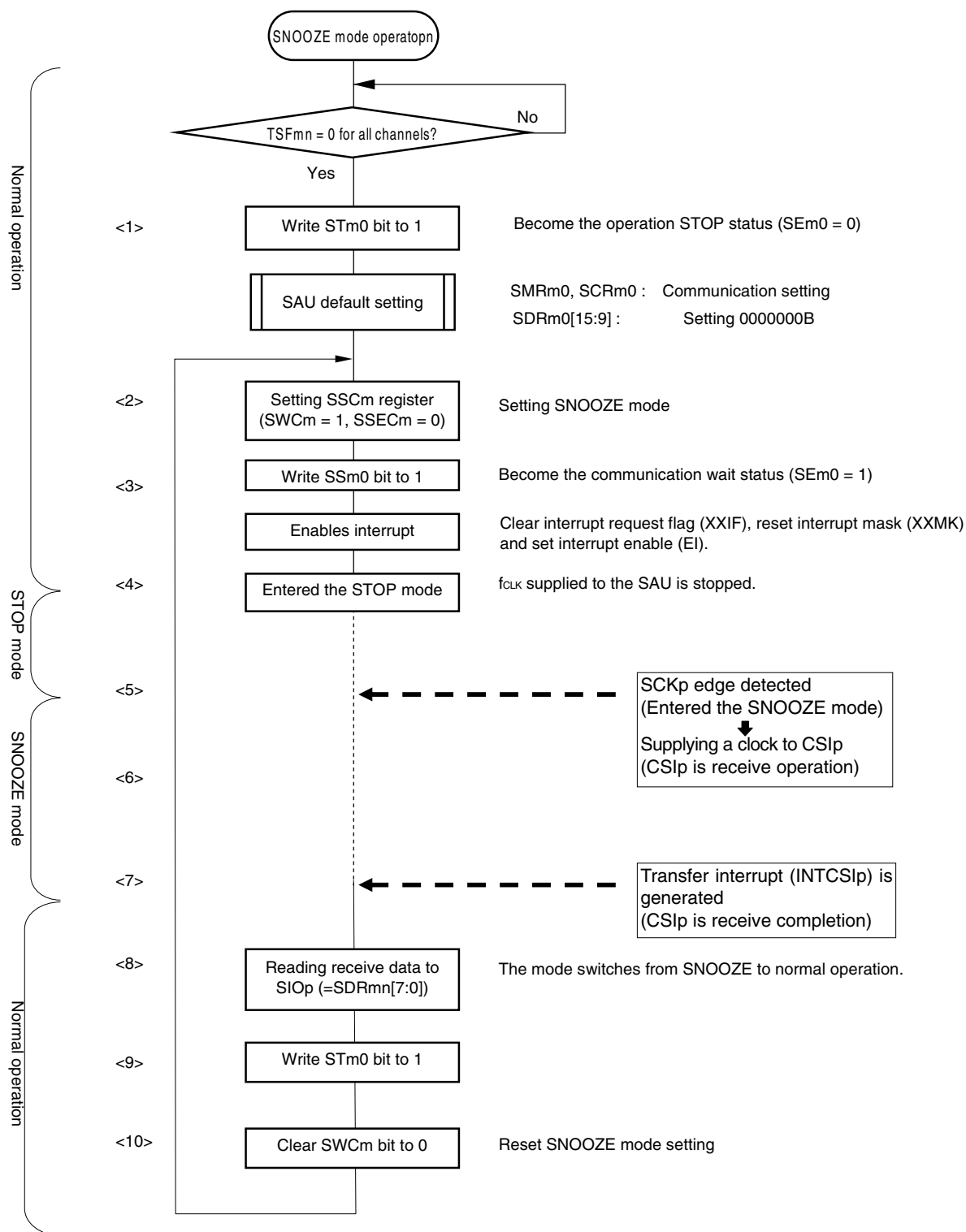


- Notes**
1. Only read received data while  $\overline{\text{SWCm}} = 1$  and before the next edge of the  $\overline{\text{SCKp}}$  pin input is detected.
  2. The transfer end interrupt ( $\text{INTCSIp}$ ) is cleared either when  $\overline{\text{SWCm}}$  is cleared to 0 or when the next edge of the  $\overline{\text{SCKp}}$  pin input is detected.

**<R> Caution** Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the  $\text{STm0}$  bit to 1 (clear the  $\text{SEm0}$  bit, and stop the operation). And after completion the receive operation, also clearing  $\text{SWCm}$  bit to 0 (SNOOZE release).

- Remarks**
1. <1> to <10> in the figure correspond to <1> to <10> in Figure 12-73. Flowchart of SNOOZE Mode Operation (continuous startup).
  2.  $m = 0$ ;  $p = 00$

Figure 12-73. Flowchart of SNOOZE Mode Operation (continuous startup)



**Remarks 1.** <1> to <10> in the figure correspond to <1> to <10> in **Figure 12-72. Timing Chart of SNOOZE Mode Operation (continuous startup).**

**2.** m = 0; p = 00

### 12.5.8 Calculating transfer clock frequency

The transfer clock frequency for 3-wire serial I/O (CSI00, CSI01) communication can be calculated by the following expressions.

#### (1) Master

$$(\text{Transfer clock frequency}) = \{ \text{Operation clock (f}_{\text{MCK}}) \text{ frequency of target channel} \} \div (\text{SDRmn}[15:9] + 1) \div 2 \text{ [Hz]}$$

#### (2) Slave

$$(\text{Transfer clock frequency}) = \{ \text{Frequency of serial clock (SCK) supplied by master} \}^{\text{Note}} \text{ [Hz]}$$

**Note** The permissible maximum transfer clock frequency is  $f_{\text{MCK}}/6$ .

**Remark** The value of SDRmn[15:9] is the value of bits 15 to 9 of serial data register mn (SDRmn) (0000000B to 1111111B) and therefore is 0 to 127.

The operation clock ( $f_{\text{MCK}}$ ) is determined by serial clock select register m (SPSm) and bit 15 (CKSmn) of serial mode register mn (SMRmn).

Table 12-2. Selection of Operation Clock For 3-Wire Serial I/O

| SMRmn Register   | SPSm Register |         |         |         |         |         |         |         | Operation Clock (f <sub>CLK</sub> ) <sup>Note</sup> |                           |
|------------------|---------------|---------|---------|---------|---------|---------|---------|---------|-----------------------------------------------------|---------------------------|
| CKSmn            | PRS m13       | PRS m12 | PRS m11 | PRS m10 | PRS m03 | PRS m02 | PRS m01 | PRS m00 |                                                     | f <sub>CLK</sub> = 24 MHz |
| 0                | X             | X       | X       | X       | 0       | 0       | 0       | 0       | f <sub>CLK</sub>                                    | 24 MHz                    |
|                  | X             | X       | X       | X       | 0       | 0       | 0       | 1       | f <sub>CLK</sub> /2                                 | 12 MHz                    |
|                  | X             | X       | X       | X       | 0       | 0       | 1       | 0       | f <sub>CLK</sub> /2 <sup>2</sup>                    | 6 MHz                     |
|                  | X             | X       | X       | X       | 0       | 0       | 1       | 1       | f <sub>CLK</sub> /2 <sup>3</sup>                    | 3 MHz                     |
|                  | X             | X       | X       | X       | 0       | 1       | 0       | 0       | f <sub>CLK</sub> /2 <sup>4</sup>                    | 1.5 MHz                   |
|                  | X             | X       | X       | X       | 0       | 1       | 0       | 1       | f <sub>CLK</sub> /2 <sup>5</sup>                    | 750 kHz                   |
|                  | X             | X       | X       | X       | 0       | 1       | 1       | 0       | f <sub>CLK</sub> /2 <sup>6</sup>                    | 375 kHz                   |
|                  | X             | X       | X       | X       | 0       | 1       | 1       | 1       | f <sub>CLK</sub> /2 <sup>7</sup>                    | 187.5 kHz                 |
|                  | X             | X       | X       | X       | 1       | 0       | 0       | 0       | f <sub>CLK</sub> /2 <sup>8</sup>                    | 93.8 kHz                  |
|                  | X             | X       | X       | X       | 1       | 0       | 0       | 1       | f <sub>CLK</sub> /2 <sup>9</sup>                    | 46.9 kHz                  |
|                  | X             | X       | X       | X       | 1       | 0       | 1       | 0       | f <sub>CLK</sub> /2 <sup>10</sup>                   | 23.4 kHz                  |
|                  | X             | X       | X       | X       | 1       | 0       | 1       | 1       | f <sub>CLK</sub> /2 <sup>11</sup>                   | 11.7 kHz                  |
|                  | X             | X       | X       | X       | 1       | 1       | 0       | 0       | f <sub>CLK</sub> /2 <sup>12</sup>                   | 5.86 kHz                  |
|                  | X             | X       | X       | X       | 1       | 1       | 0       | 1       | f <sub>CLK</sub> /2 <sup>13</sup>                   | 2.93 kHz                  |
|                  | X             | X       | X       | X       | 1       | 1       | 1       | 0       | f <sub>CLK</sub> /2 <sup>14</sup>                   | 1.46 kHz                  |
|                  | X             | X       | X       | X       | 1       | 1       | 1       | 1       | f <sub>CLK</sub> /2 <sup>15</sup>                   | 732 Hz                    |
| 1                | 0             | 0       | 0       | 0       | X       | X       | X       | X       | f <sub>CLK</sub>                                    | 24 MHz                    |
|                  | 0             | 0       | 0       | 1       | X       | X       | X       | X       | f <sub>CLK</sub> /2                                 | 12 MHz                    |
|                  | 0             | 0       | 1       | 0       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>2</sup>                    | 6 MHz                     |
|                  | 0             | 0       | 1       | 1       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>3</sup>                    | 3 MHz                     |
|                  | 0             | 1       | 0       | 0       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>4</sup>                    | 1.5 MHz                   |
|                  | 0             | 1       | 0       | 1       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>5</sup>                    | 750 kHz                   |
|                  | 0             | 1       | 1       | 0       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>6</sup>                    | 375 kHz                   |
|                  | 0             | 1       | 1       | 1       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>7</sup>                    | 187.5 kHz                 |
|                  | 1             | 0       | 0       | 0       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>8</sup>                    | 93.8 kHz                  |
|                  | 1             | 0       | 0       | 1       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>9</sup>                    | 46.9 kHz                  |
|                  | 1             | 0       | 1       | 0       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>10</sup>                   | 23.4 kHz                  |
|                  | 1             | 0       | 1       | 1       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>11</sup>                   | 11.7 kHz                  |
|                  | 1             | 1       | 0       | 0       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>12</sup>                   | 5.86 kHz                  |
|                  | 1             | 1       | 0       | 1       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>13</sup>                   | 2.93 kHz                  |
|                  | 1             | 1       | 1       | 0       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>14</sup>                   | 1.46 kHz                  |
|                  | 1             | 1       | 1       | 1       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>15</sup>                   | 732 Hz                    |
| Other than above |               |         |         |         |         |         |         |         | Setting prohibited                                  |                           |

**Note** When changing the clock selected for f<sub>CLK</sub> (by changing the system clock control register (CKC) value), do so after having stopped (serial channel stop register m (STm) = 000FH) the operation of the serial array unit (SAU).

**Remarks 1.** X: Don't care

**2.** m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01

### 12.5.9 Procedure for processing errors that occurred during 3-wire serial I/O (CSI00, CSI01) communication

The procedure for processing errors that occurred during 3-wire serial I/O (CSI00, CSI01) communication is described in Figure 12-74.

**Figure 12-74. Processing Procedure in Case of Overrun Error**

| Software Manipulation                                      | Hardware Status                                                                             | Remark                                                                                                                                  |
|------------------------------------------------------------|---------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| Reads serial data register mn (SDRmn).                     | → The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data. | This is to prevent an overrun error if the next reception is completed during error processing.                                         |
| Reads serial status register mn (SSRmn).                   |                                                                                             | Error type is identified and the read value is used to clear error flag.                                                                |
| Writes 1 to serial flag clear trigger register mn (SIRmn). | → Error flag is cleared.                                                                    | Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification. |

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01



## 12.6 Operation of UART (UART0) Communication

This is a start-stop synchronization function using two lines: serial data transmission (TxD) and serial data reception (RxD) lines. By using these two communication lines, each data frame, which consist of a start bit, data, parity bit, and stop bit, is transferred asynchronously (using the internal baud rate) between the microcontroller and the other communication party. Full-duplex UART communication can be performed by using a channel dedicated to transmission (even-numbered channel) and a channel dedicated to reception (odd-numbered channel). The LIN-bus can be implemented by using timer array unit with an external interrupt (INTP0).

### [Data transmission/reception]

- Data length of 7, 8, or 9 bits
- Select the MSB/LSB first
- Level setting of transmit/receive data (selecting whether to reverse the level)
- Parity bit appending and parity check functions
- Stop bit appending, stop bit check function

### [Interrupt function]

- Transfer end interrupt/buffer empty interrupt
- Error interrupt in case of framing error, parity error, or overrun error

### [Error detection flag]

- Framing error, parity error, or overrun error

In addition, UART0 reception (channel 1) supports the SNOOZE mode. When RxD0 pin input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible.

The LIN-bus is accepted in UART0 (channels 0 and 1).

### [LIN-bus functions]

- Wakeup signal detection
- Break field (BF) detection
- Sync field measurement, baud rate calculation

} Using the external interrupt (INTP0) and timer array unit

UART0 uses channels 0 and 1.

| Channel | Used as CSI | Used as UART               |
|---------|-------------|----------------------------|
| 0       | CSI00       | UART0 (supporting LIN-bus) |
| 1       | CSI01       |                            |

**Caution** When using serial array unit as UARTs, the channels of both the transmitting side (even-number channel) and the receiving side (odd-number channel) can be used only as UARTs.

UART performs the following four types of communication operations.

- UART transmission (See 12.6.1.)
- UART reception (See 12.6.2.)
- LIN transmission (See 12.7.1.)
- LIN reception (See 12.7.2.)

### 12.6.1 UART transmission

UART transmission is an operation to transmit data from the RL78/L12 to another device asynchronously (start-stop synchronization).

Of two channels used for UART, the even channel is used for UART transmission.

| UART                 | UART0                                                                                                                                                                                     |
|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Target channel       | Channel 0                                                                                                                                                                                 |
| Pins used            | TxD0                                                                                                                                                                                      |
| Interrupt            | INTST0                                                                                                                                                                                    |
|                      | Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected.                                                                 |
| Error detection flag | None                                                                                                                                                                                      |
| Transfer data length | 7, 8, or 9 bits                                                                                                                                                                           |
| Transfer rate        | Max. $f_{MCK}/6$ [bps] (SDRmn [15:9] = 2 or more), Min. $f_{CLK}/(2 \times 2^{15} \times 128)$ [bps] <sup>Note</sup>                                                                      |
| Data phase           | Non-reverse output (default: high level)<br>Reverse output (default: low level)                                                                                                           |
| Parity bit           | The following selectable <ul style="list-style-type: none"> <li>• No parity bit</li> <li>• Appending 0 parity</li> <li>• Appending even parity</li> <li>• Appending odd parity</li> </ul> |
| Stop bit             | The following selectable <ul style="list-style-type: none"> <li>• Appending 1 bit</li> <li>• Appending 2 bits</li> </ul>                                                                  |
| Data direction       | MSB or LSB first                                                                                                                                                                          |

**Note** Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS**).

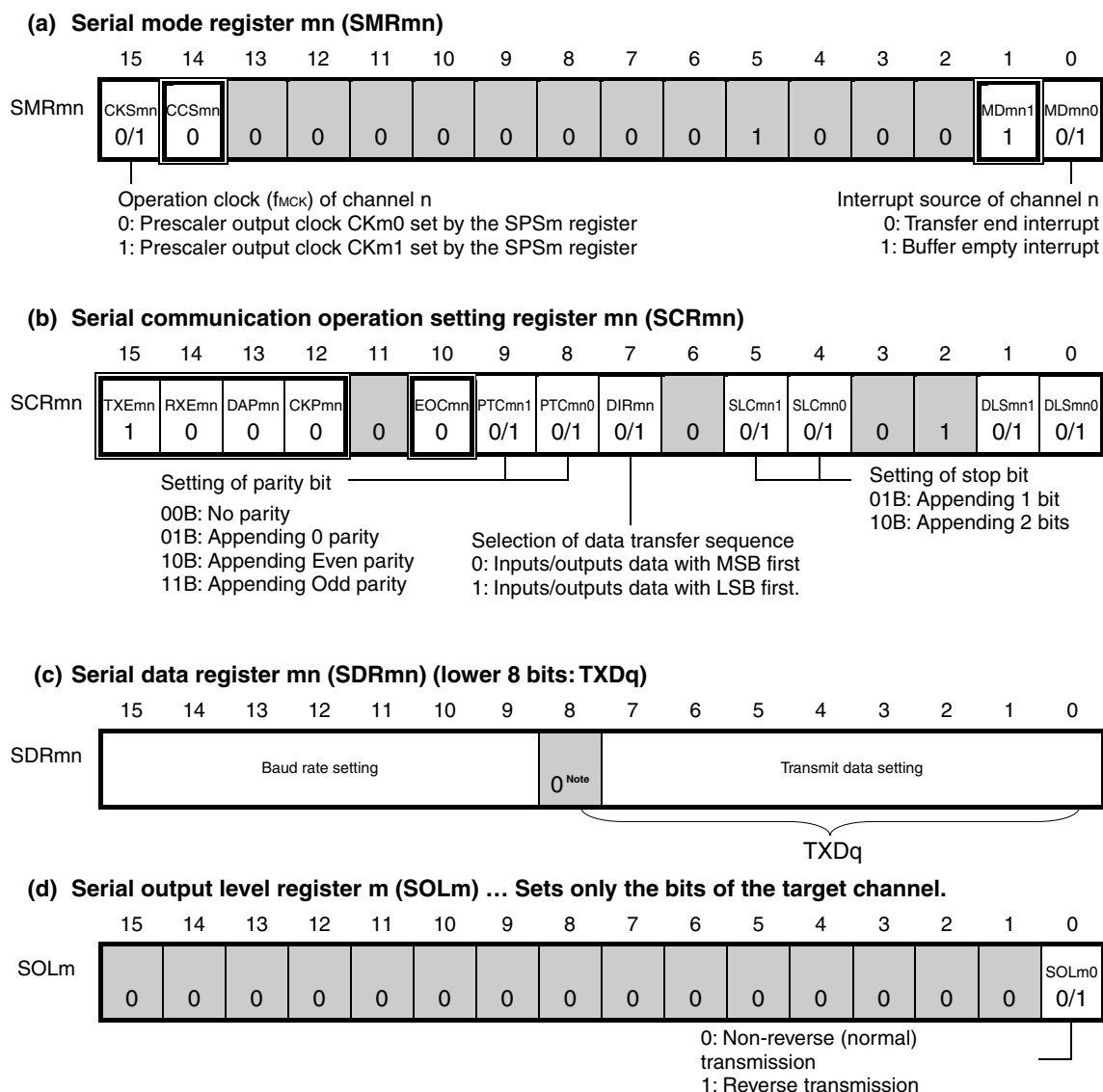
**Remarks 1.**  $f_{MCK}$ : Operation clock frequency of target channel

$f_{CLK}$ : System clock frequency

**2.** m: Unit number (m = 0), n: Channel number (n = 0), mn = 00

## (1) Register setting

Figure 12-75. Example of Contents of Registers for UART Transmission of UART (UART0) (1/2)



**Note** When UART0 performs 9-bit communication (by setting the DLS001 and DLS000 bits of the SCR00 register to 1), bits 0 to 8 of the SDR00 register are used as the transmission data specification area.

- Remarks**
1. m: Unit number (m = 0), n: Channel number (n = 0), q: UART number (q = 0), mn = 00
  2.  : Setting is fixed in the UART transmission mode,  : Setting disabled (set to the initial value)  
 ×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)  
 0/1: Set to 0 or 1 depending on the usage of the user

**Figure 12-75. Example of Contents of Registers for UART Transmission of UART (UART0) (2/2)**

**(e) Serial output register m (SOM) ... Sets only the bits of the target channel.**

|     | 15 | 14 | 13 | 12 | 11 | 10 | 9          | 8          | 7 | 6 | 5 | 4 | 3 | 2 | 1         | 0                           |
|-----|----|----|----|----|----|----|------------|------------|---|---|---|---|---|---|-----------|-----------------------------|
| SOM | 0  | 0  | 0  | 0  | 0  | 0  | CKOm1<br>× | CKOm0<br>× | 0 | 0 | 0 | 0 | 0 | 0 | SOM1<br>× | SOM0<br>0/1 <sup>Note</sup> |

0: Serial data output value is "0"  
1: Serial data output value is "1"

**(f) Serial output enable register m (SOEm) ... Sets only the bits of the target channel to 1.**

|      | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1          | 0            |
|------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|------------|--------------|
| SOEm | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SOEm1<br>× | SOEm0<br>0/1 |

**(g) Serial channel start register m (SSm) ... Sets only the bits of the target channel to 1.**

|     | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1         | 0           |
|-----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-----------|-------------|
| SSm | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SSm1<br>× | SSm0<br>0/1 |

**Note** Before transmission is started, be sure to set to 1 when the SOLm0 bit of the target channel is set to 0, and set to 0 when the SOLm0 bit of the target channel is set to 1. The value varies depending on the communication data during communication operation.

**Remarks 1.** m: Unit number (m = 0), n: Channel number (n = 0), mn = 00

**2.**  : Setting disabled (set to the initial value)

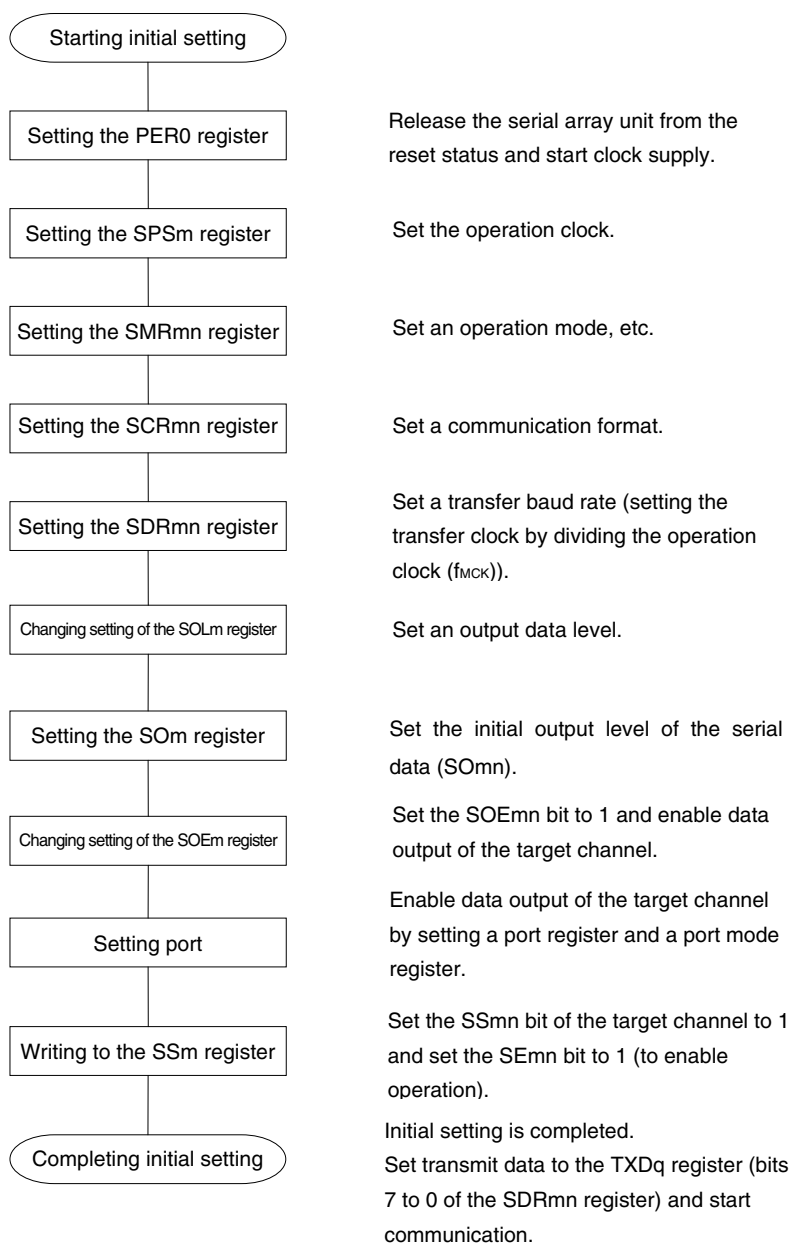
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

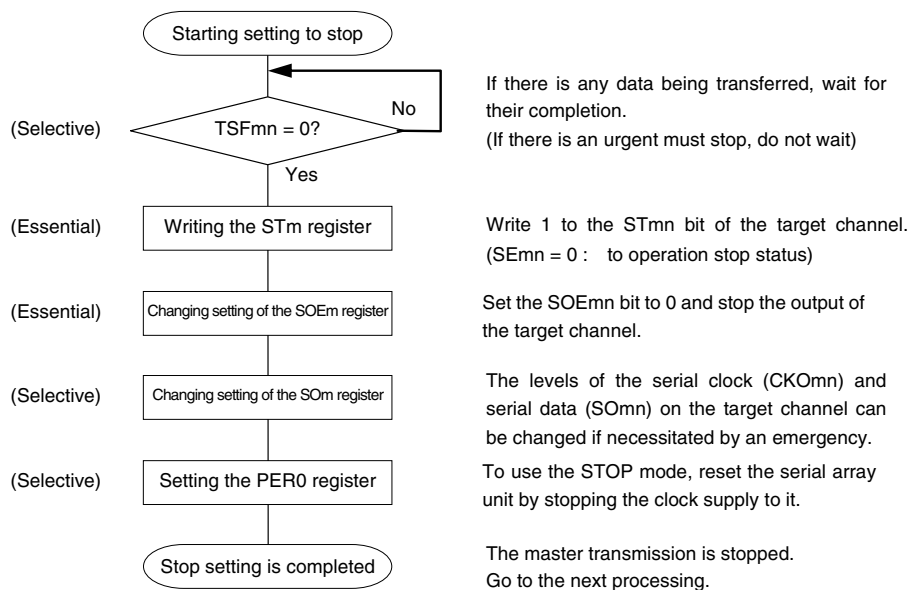
## (2) Operation procedure

&lt;R&gt;

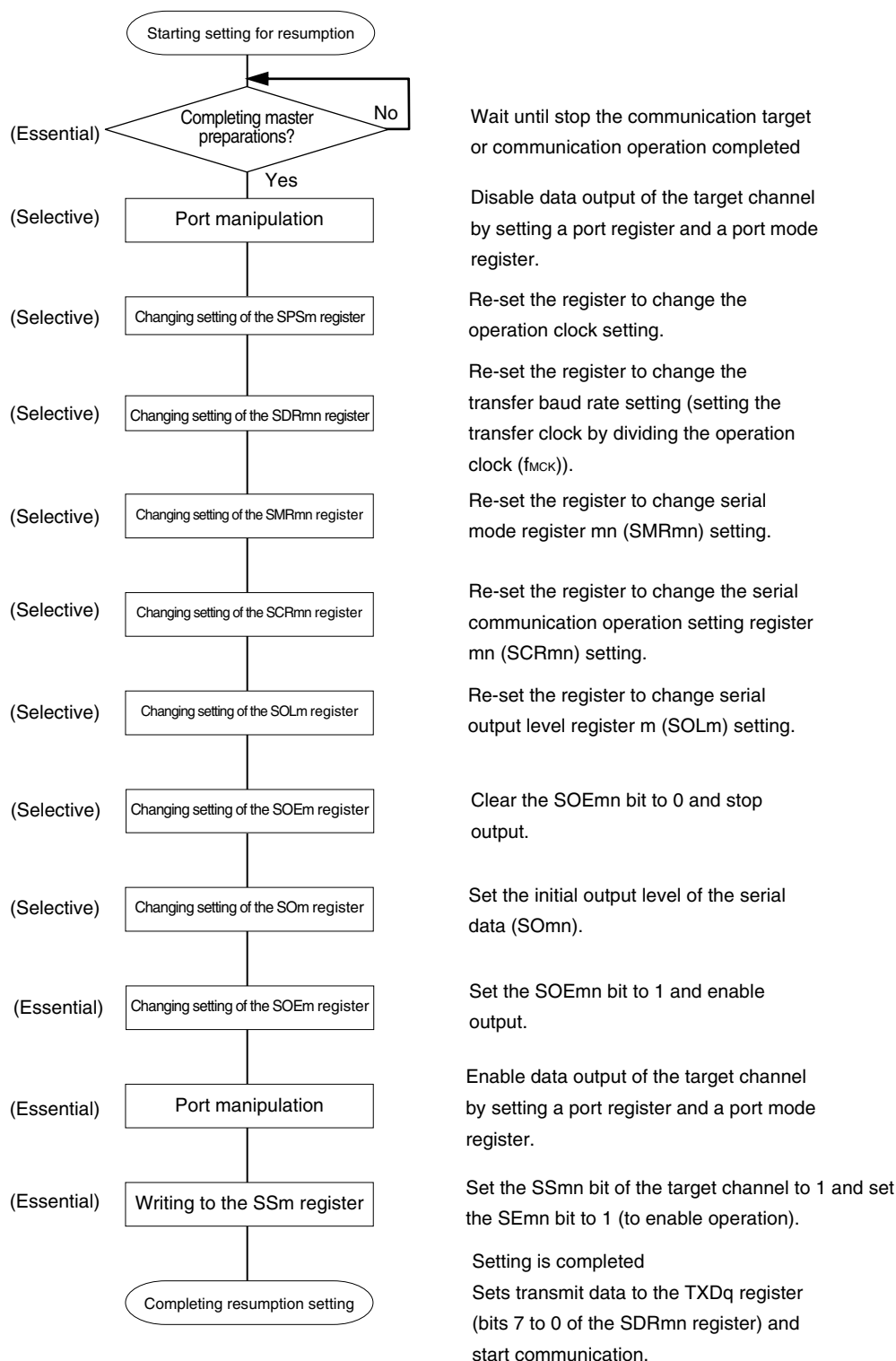
Figure 12-76. Initial Setting Procedure for UART Transmission



&lt;R&gt;

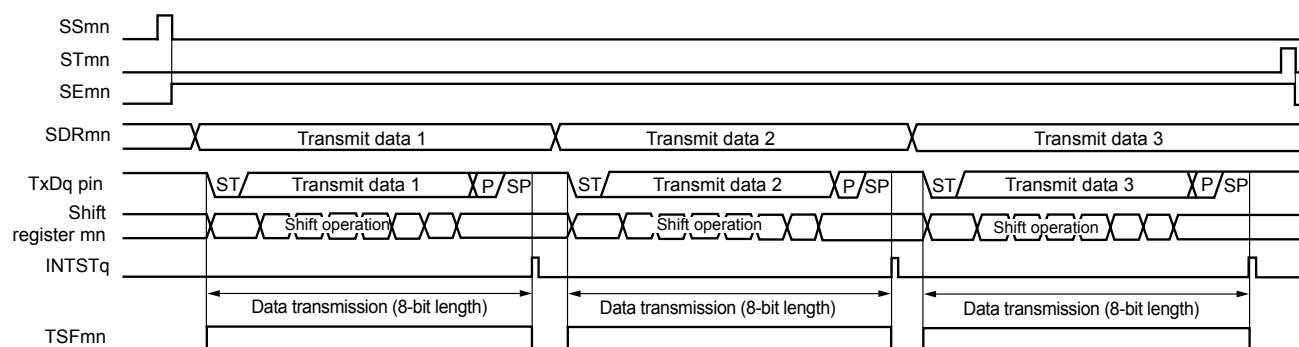
**Figure 12-77. Procedure for Stopping UART Transmission**

&lt;R&gt;

**Figure 12-78. Procedure for Resuming UART Transmission**

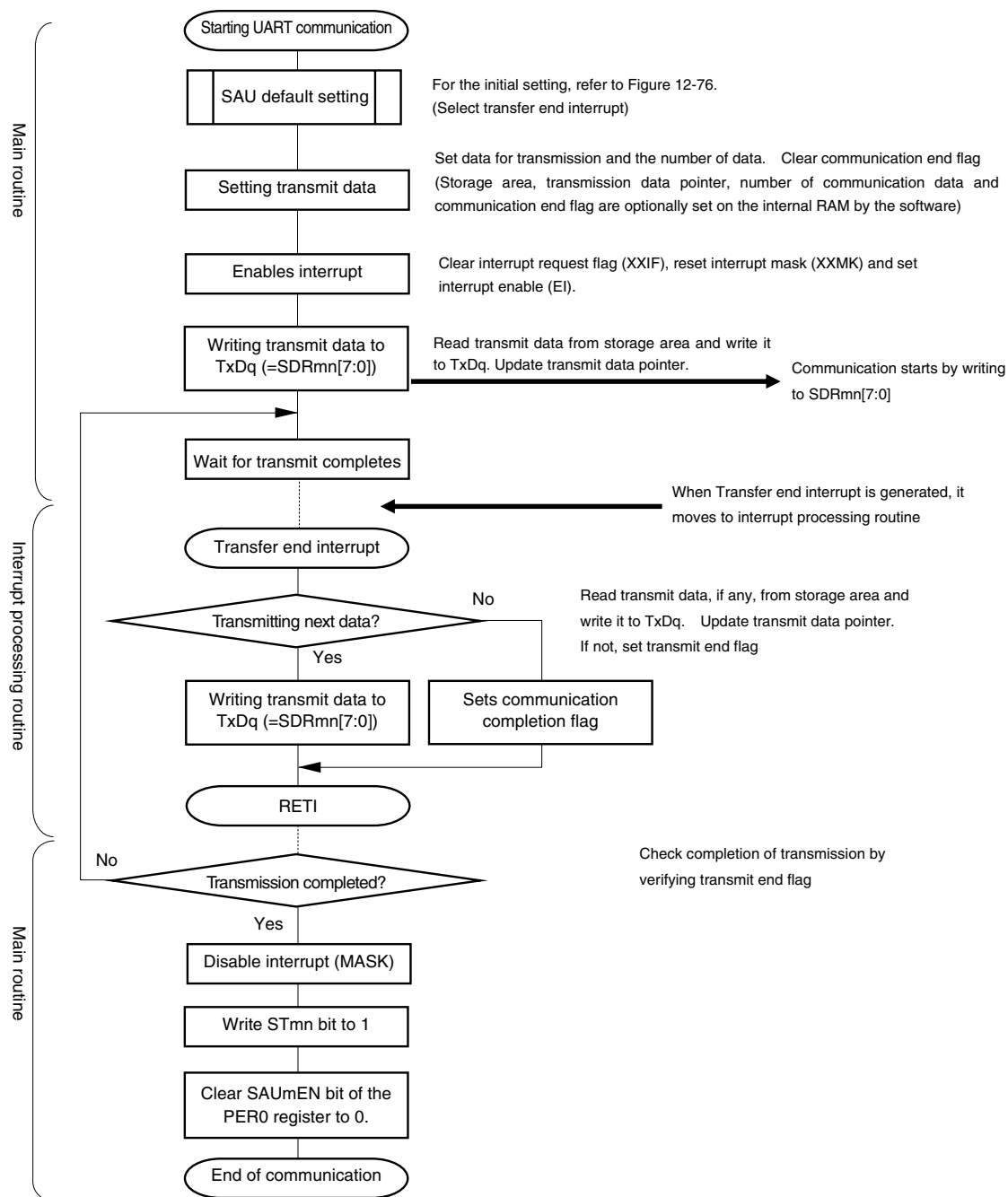
**Remark** If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target stops or transmission finishes, and then perform initialization instead of restarting the transmission.



**(3) Processing flow (in single-transmission mode)****Figure 12-79. Timing Chart of UART Transmission (in Single-Transmission Mode)**

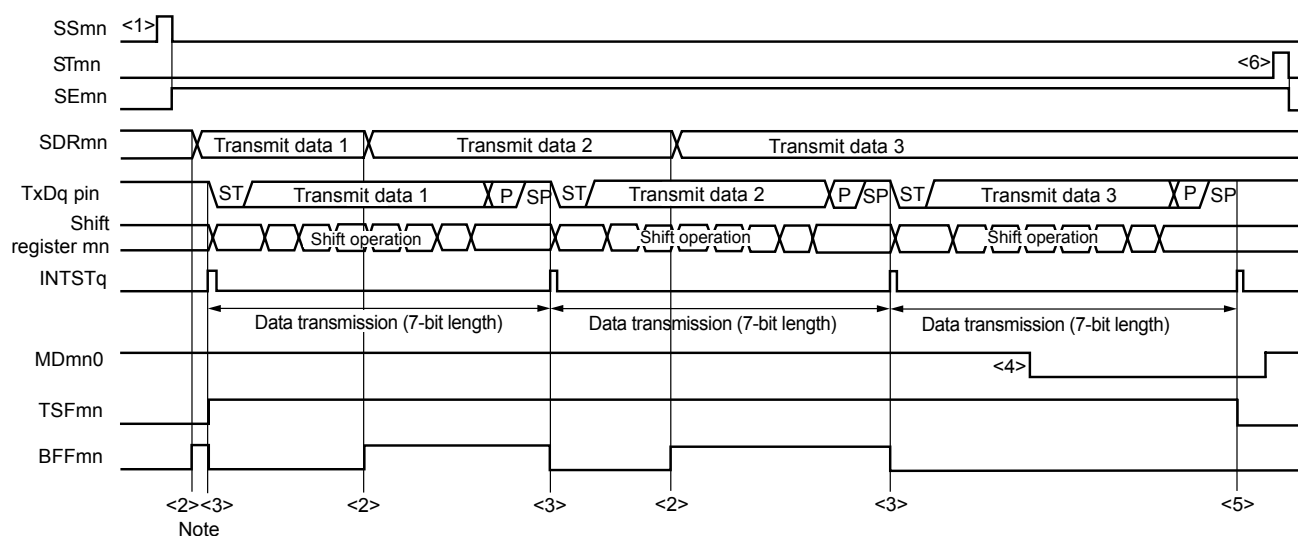
**Remark** m: Unit number (m = 0), n: Channel number (n = 0), q: UART number (q = 0)  
mn = 00

&lt;R&gt;

**Figure 12-80. Flowchart of UART Transmission (in Single-Transmission Mode)**

## (4) Processing flow (in continuous transmission mode)

Figure 12-81. Timing Chart of UART Transmission (in Continuous Transmission Mode)

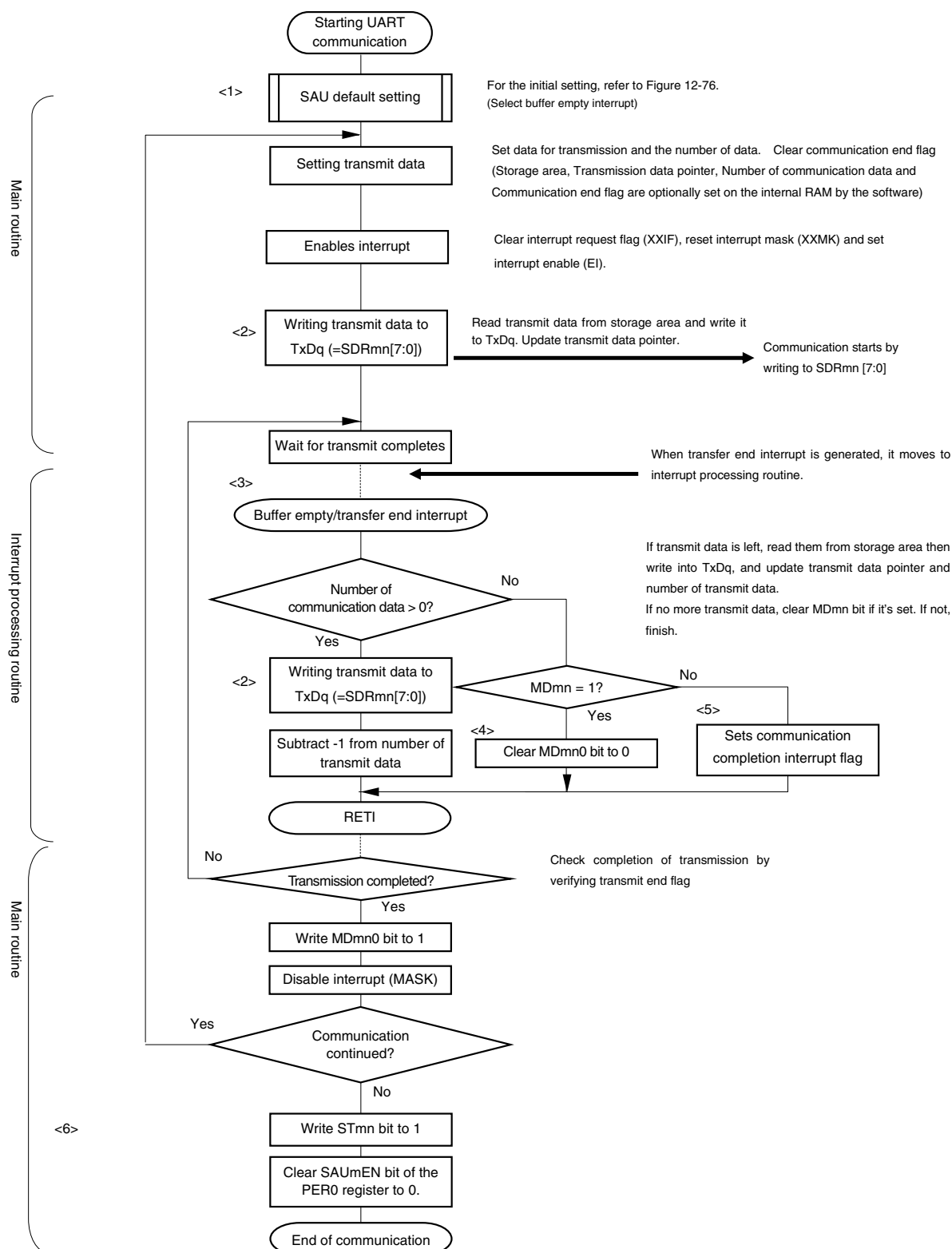


**Note** If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

**Caution** The MDmn0 bit of serial mode register mn (SSRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it will be rewritten before the transfer end interrupt of the last transmit data.

**Remark** m: Unit number (m = 0), n: Channel number (n = 0), q: UART number (q = 0)  
mn = 00

&lt;R&gt;

**Figure 12-82. Flowchart of UART Transmission (in Continuous Transmission Mode)**

**Remark** <1> to <6> in the figure correspond to <1> to <6> in **Figure 12-81 Timing Chart of UART Transmission (in Continuous Transmission Mode)**.

### 12.6.2 UART reception

UART reception is an operation wherein the RL78/L12 asynchronously receives data from another device (start-stop synchronization).

For UART reception, the odd-number channel of the two channels used for UART is used. The SMR register of both the odd- and even-numbered channels must be set.

&lt;R&gt;

| UART                 | UART0                                                                                                                                                                                                          |
|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Target channel       | Channel 1                                                                                                                                                                                                      |
| Pins used            | RxD0                                                                                                                                                                                                           |
| Interrupt            | INTSR0                                                                                                                                                                                                         |
|                      | Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)                                                                                                                                |
| Error interrupt      | INTSRE0                                                                                                                                                                                                        |
| Error detection flag | <ul style="list-style-type: none"> <li>Framing error detection flag (FEFmn)</li> <li>Parity error detection flag (PEFmn)</li> <li>Overrun error detection flag (OVFmn)</li> </ul>                              |
| Transfer data length | 7, 8 or 9 bits                                                                                                                                                                                                 |
| Transfer rate        | Max. $f_{MCK}/6$ [bps] (SDRmn [15:9] = 2 or more), Min. $f_{CLK}/(2 \times 2^{15} \times 128)$ [bps] <sup>Note</sup>                                                                                           |
| Data phase           | Non-reverse output (default: high level)<br>Reverse output (default: low level)                                                                                                                                |
| Parity bit           | The following selectable <ul style="list-style-type: none"> <li>No parity bit (no parity check)</li> <li>No parity judgment (0 parity)</li> <li>Appending even parity</li> <li>Appending odd parity</li> </ul> |
| Stop bit             | 1 bit check                                                                                                                                                                                                    |
| Data direction       | MSB or LSB first                                                                                                                                                                                               |

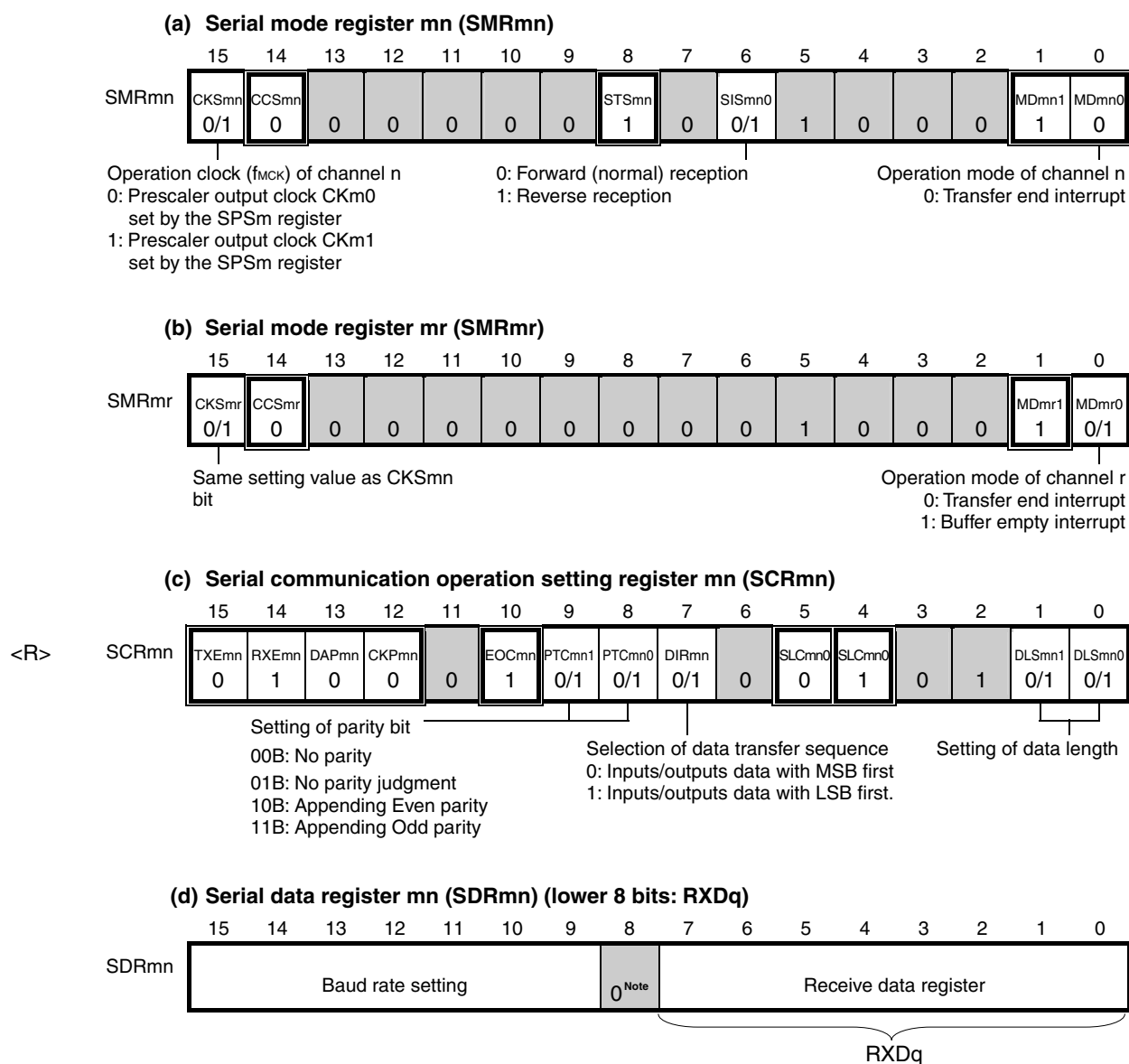
**Note** Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS**).

**Remarks 1.**  $f_{MCK}$ : Operation clock frequency of target channel

$f_{CLK}$ : System clock frequency

**2.** m: Unit number (m = 0), n: Channel number (n = 1), mn = 01

## (1) Register setting

**Figure 12-83. Example of Contents of Registers for UART Reception of UART (UART0) (1/2)**

**Note** When UART performs 9-bit communication, bits 0 to 8 of the SDRm1 register are used as the transmission data specification area.

**Caution** For the UART reception, be sure to set the SMRmr register of channel r to UART transmission mode that is to be paired with channel n.

**Remarks 1.** m: Unit number (m = 0), n: Channel number (n = 1), mn = 01

r: Channel number (r = n - 1), q: UART number (q = 0)

2. □: Setting is fixed in the UART reception mode, ■: Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

**Figure 12-83. Example of Contents of Registers for UART Reception of UART (UART0) (2/2)**

(e) Serial output register m (SOm) ... The register that not used in this mode.

|     |    |    |    |    |    |    |       |       |   |   |   |   |   |   |      |      |
|-----|----|----|----|----|----|----|-------|-------|---|---|---|---|---|---|------|------|
|     | 15 | 14 | 13 | 12 | 11 | 10 | 9     | 8     | 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0    |
| SOm |    |    |    |    |    |    | CKOm1 | CKOm0 |   |   |   |   |   |   | SOm1 | SOm0 |
|     | 0  | 0  | 0  | 0  | 0  | 0  | ×     | ×     | 0 | 0 | 0 | 0 | 0 | 0 | ×    | ×    |

(f) Serial output enable register m (SOEm) ...The register that not used in this mode.

|      |    |    |    |    |    |    |   |   |   |   |   |   |   |   |       |       |
|------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-------|-------|
|      | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0     |
| SOEm |    |    |    |    |    |    |   |   |   |   |   |   |   |   | SOEm1 | SOEm0 |
|      | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ×     | ×     |

(g) Serial channel start register m (SSm) ... Sets only the bits of the target channel is 1.

|     |    |    |    |    |    |    |   |   |   |   |   |   |   |   |      |      |
|-----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|------|------|
|     | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0    |
| SSm |    |    |    |    |    |    |   |   |   |   |   |   |   |   | SSm1 | SSm0 |
|     | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0/1  | ×    |

**Caution** For the UART reception, be sure to set the SMRmr register of channel r to UART Transmission mode that is to be paired with channel n.

**Remarks 1.** m: Unit number (m = 0), n: Channel number (n = 1), mn = 01

r: Channel number (r = n – 1), q: UART number (q = 0)

**2.** ☐: Setting is fixed in the UART reception mode, ☐: Setting disabled (set to the initial value)

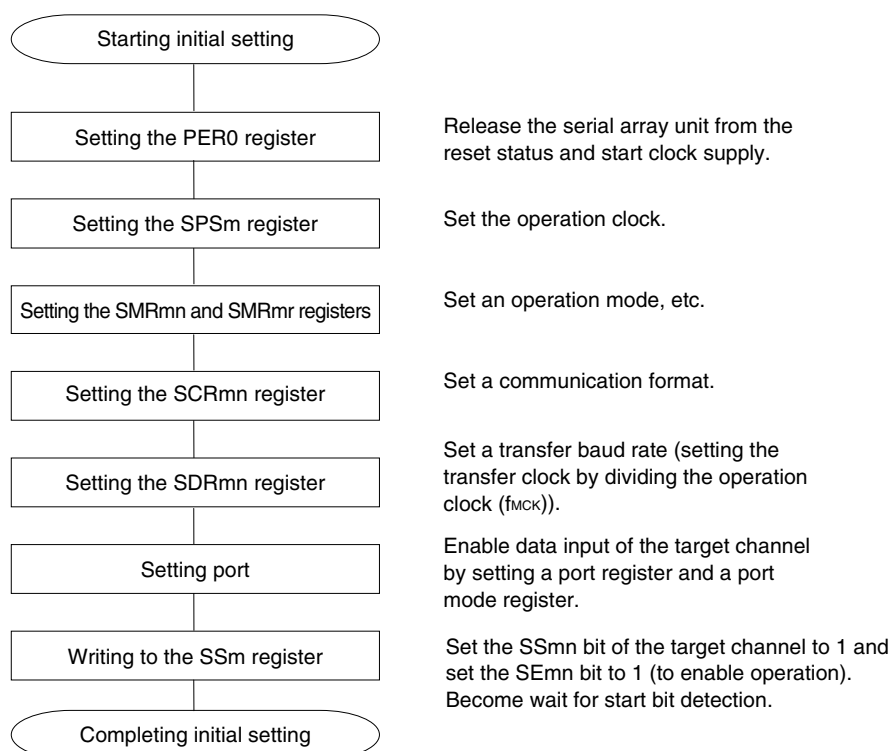
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

## (2) Operation procedure

&lt;R&gt;

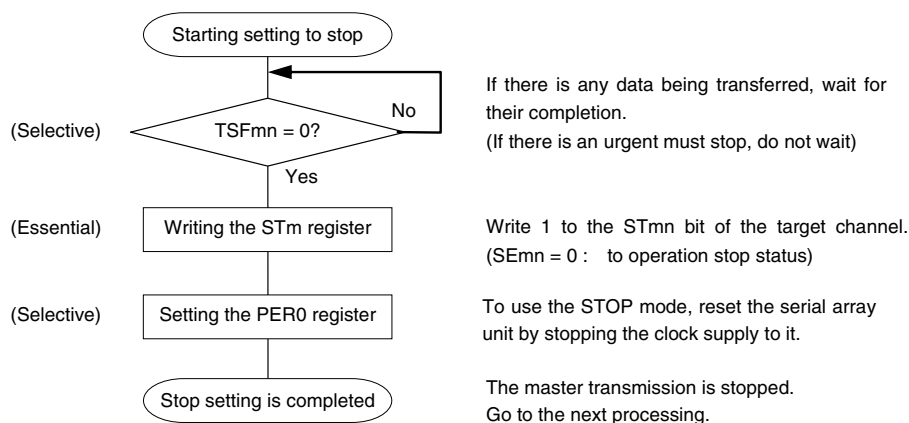
Figure 12-84. Initial Setting Procedure for UART Reception



**Caution** Set the RXEmn bit of SCRmn register to 1, and then be sure to set SSmn to 1 after 4 or more  $f_{CLK}$  clocks have elapsed.

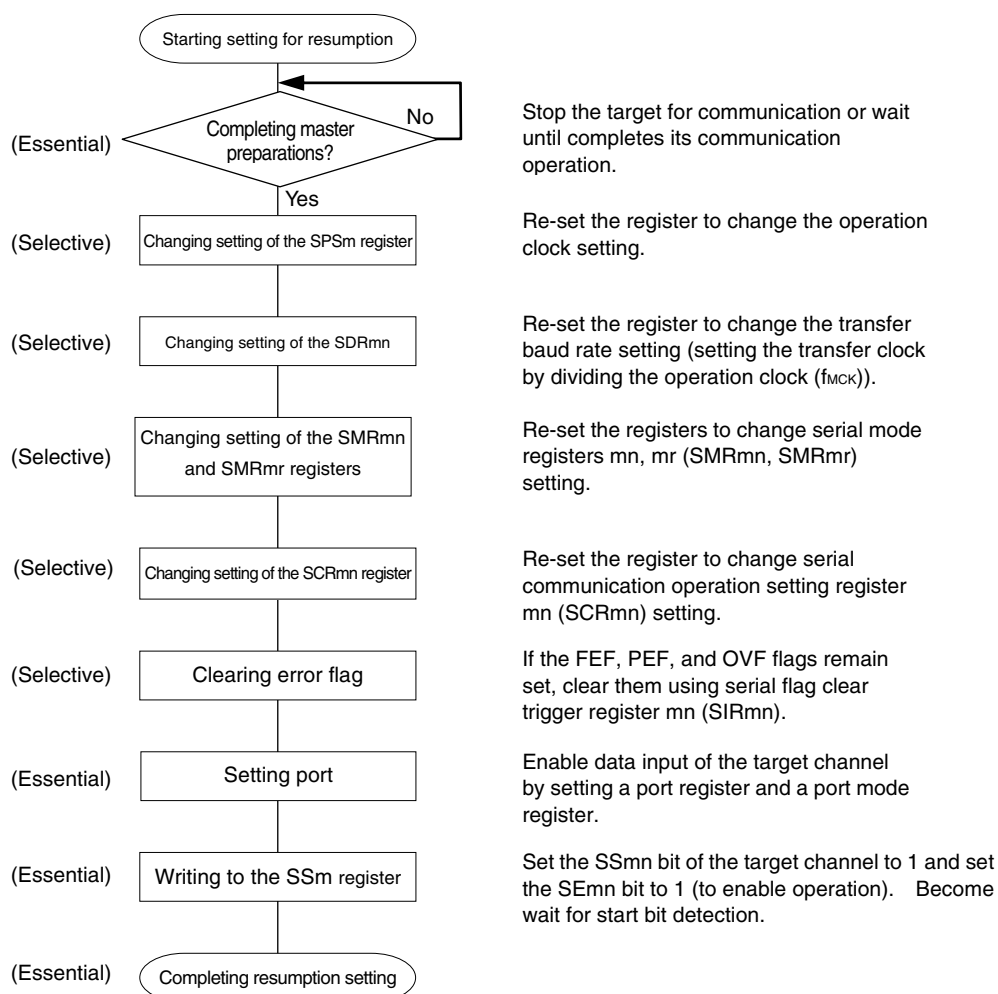
&lt;R&gt;

Figure 12-85. Procedure for Stopping UART Reception



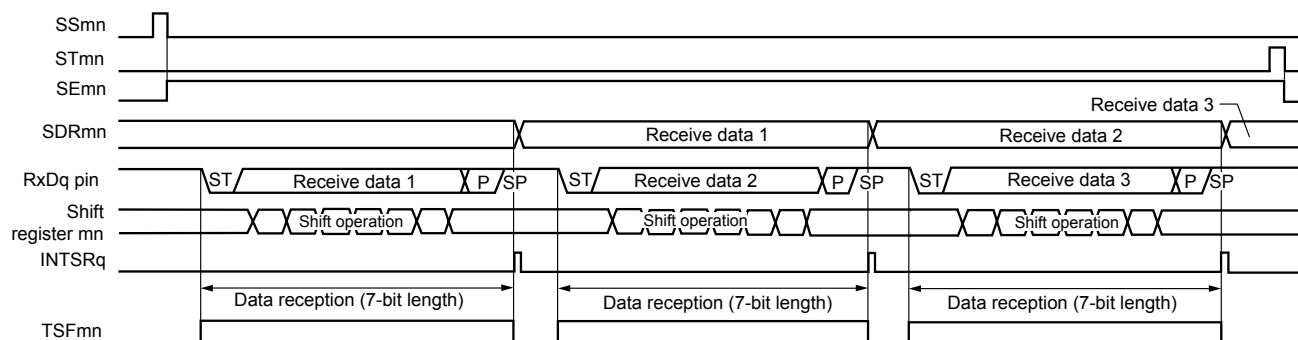


&lt;R&gt;

**Figure 12-86. Procedure for Resuming UART Reception**

**Caution** After is set RXEmn bit to 1 of SCRmn register, set the SSmn = 1 from an interval of at least four clocks of  $f_{MCK}$ .

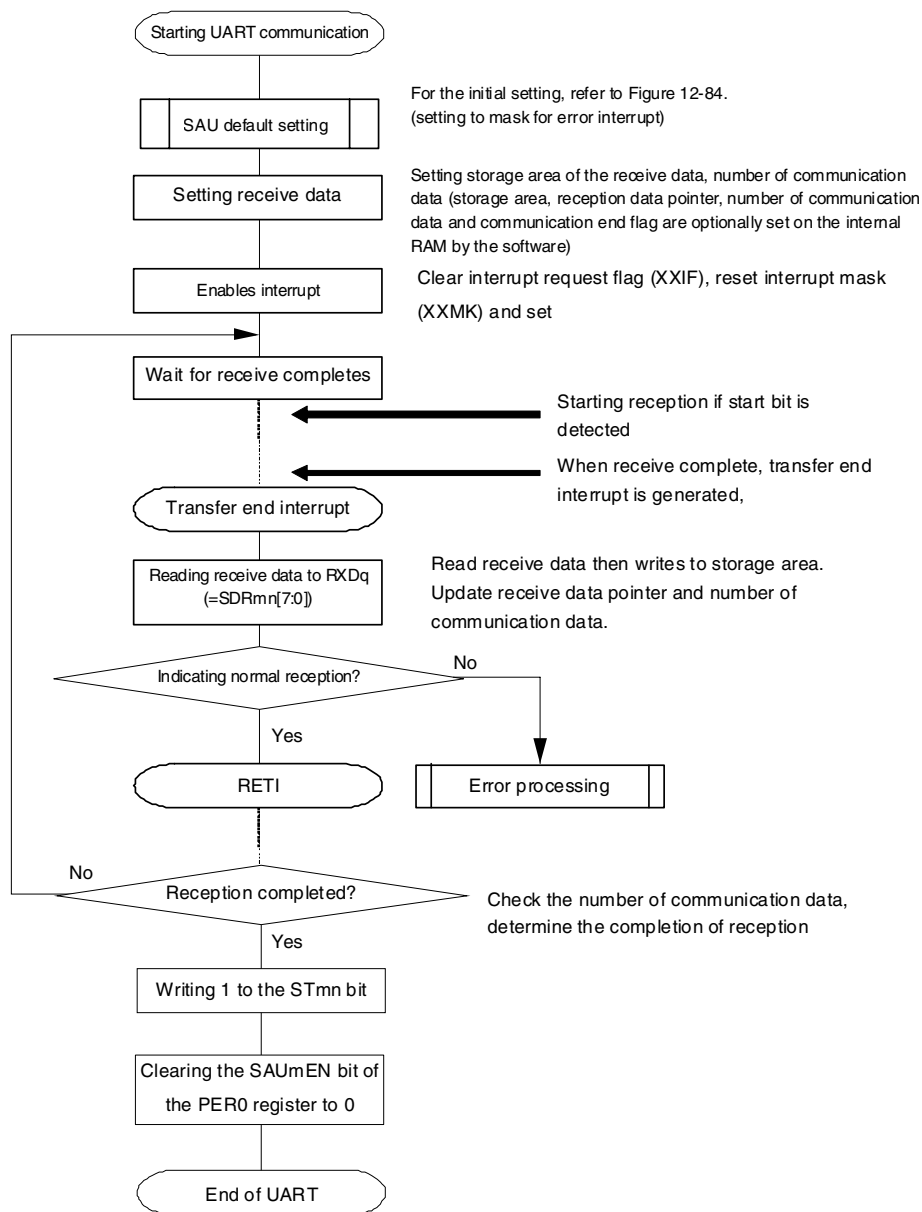
**Remark** If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target stops or transmission finishes, and then perform initialization instead of restarting the transmission.

**(3) Processing flow****Figure 12-87. Timing Chart of UART Reception**

**Remark** m: Unit number ( $m = 0$ ), n: Channel number ( $n = 1$ ),  $mn = 01$

r: Channel number ( $r = n - 1$ ), q: UART number ( $q = 0$ )

&lt;R&gt;

**Figure 12-88. Flowchart of UART Reception**

### 12.6.3 SNOOZE mode function

<R> SNOOZE mode makes UART operate reception by RxDq pin input detection while the STOP mode. Normally UART stops communication in the STOP mode. But, using the SNOOZE mode makes reception UART operate unless the CPU operation by detecting RxDq pin input.

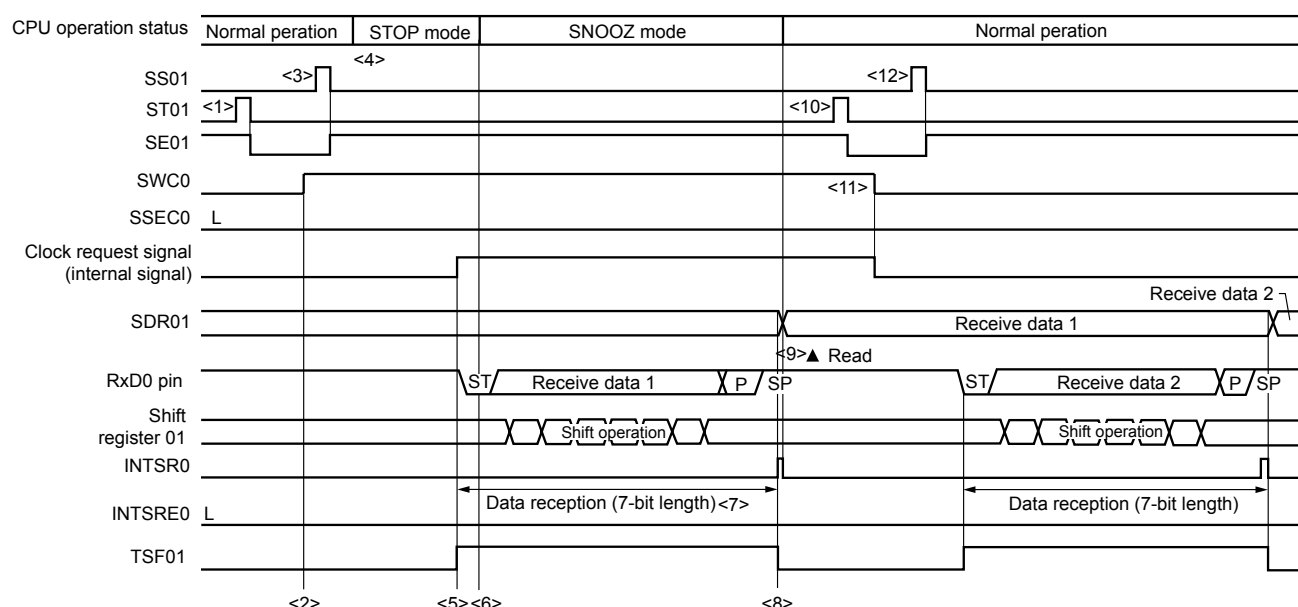
When using the SNOOZE mode function, set the SWCm bit of serial standby control register m (SSCm) to 1 just before switching to the STOP mode.

**Cautions 1. The SNOOZE mode can only be specified when the high-speed on-chip oscillator clock is selected for  $f_{CLK}$ .**

**2. The maximum transfer rate when using UARTq in the SNOOZE mode is 9600 bps.**

### (1) SNOOZE mode operation (Normal operation)

**Figure 12-89. Timing Chart of SNOOZE Mode Operation (Normal operation mode)**



<R> **Note** Read the received data when SWCm is 1

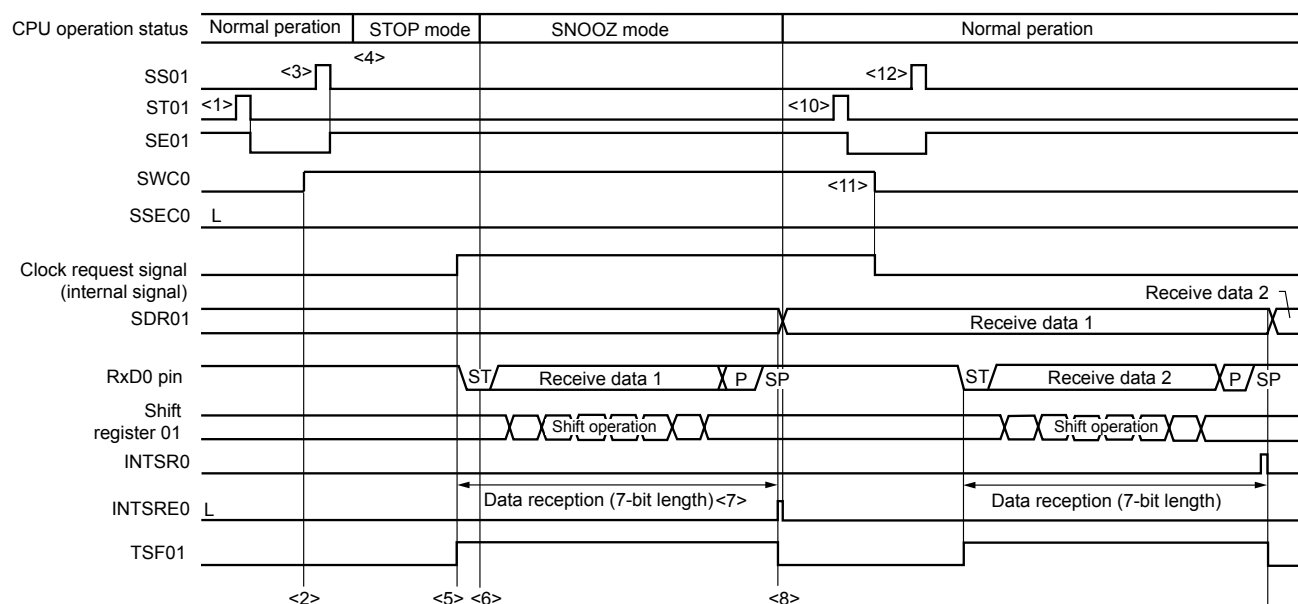
**<R> Caution** Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the STm1 bit to 1 (clear the SEm1 bit, and stop the operation).  
And after completion the receive operation, also clearing SWCm bit to 0 (SNOOZE mode release).

**Remarks 1.** <1> to <11> in the figure correspond to <1> to <11> in **Figure 12-91. Flowchart of SNOOZE Mode Operation (Normal Operation/Abnormal Operation <1>).**

**2.**  $m = 0$ ;  $q = 0$

**(2) SNOOZE mode operation (Abnormal Operation <1>)**

Abnormal operation <1> is the operation performed when a communication error occurs while SSECm = 0.  
Because SSECm = 0, an error interrupt (INTSREq) is generated when a communication error occurs.

**Figure 12-90. Timing Chart of SNOOZE Mode Operation (Abnormal Operation <1>)**

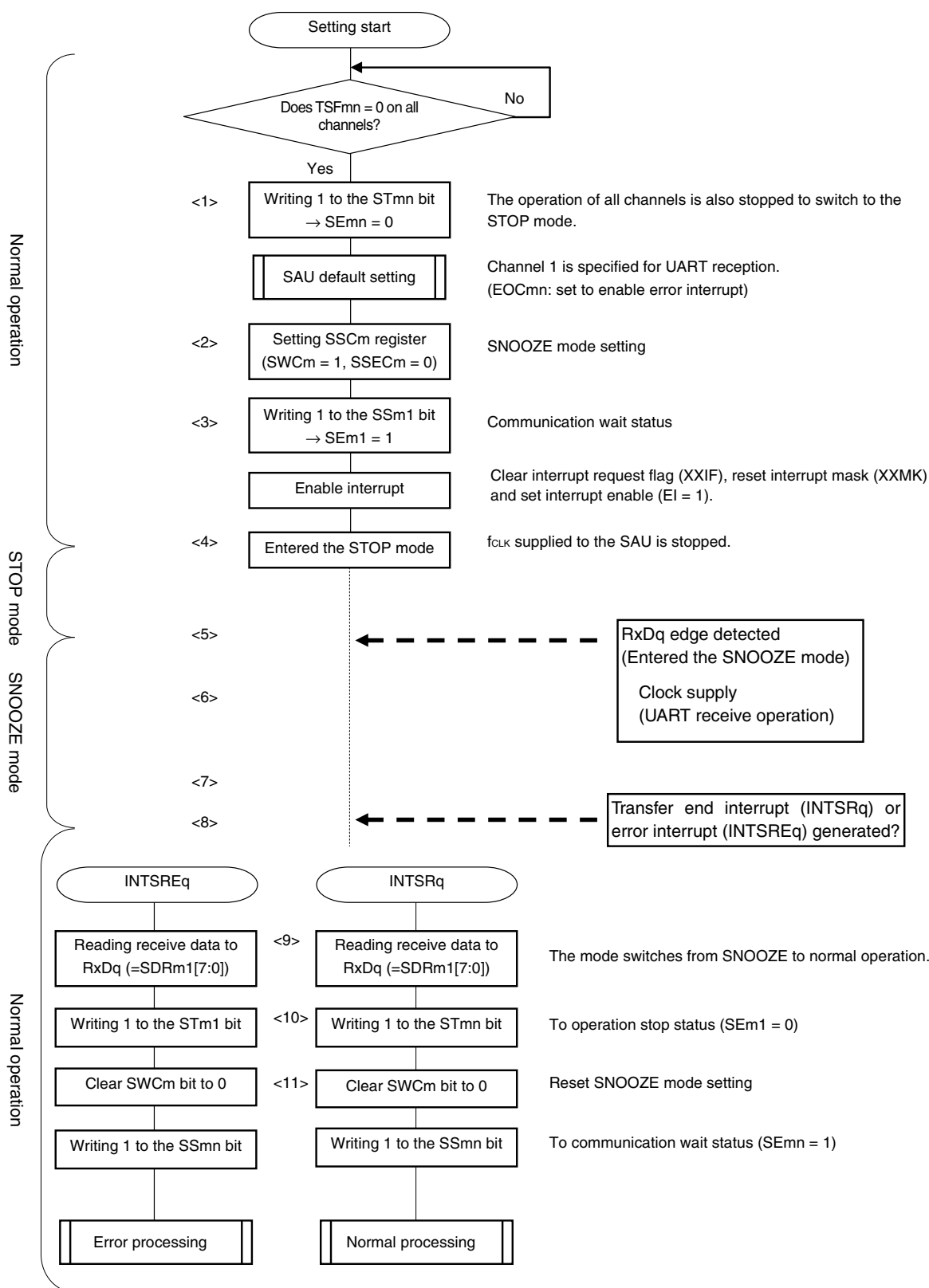
&lt;R&gt;

**Caution** Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the STm1 bit to 1 (clear the SEM1 bit, and stop the operation).  
And after completion the receive operation, also clearing SWCm bit to 0 (SNOOZE mode release).

**Remarks 1.** <1> to <11> in the figure correspond to <1> to <11> in Figure 12-91. Flowchart of SNOOZE Mode Operation (Normal Operation/Abnormal Operation <1>).

**2.** m = 0; q = 0

<R> **Figure 12-91. Flowchart of SNOOZE Mode Operation (Normal Operation/Abnormal Operation <1>)**

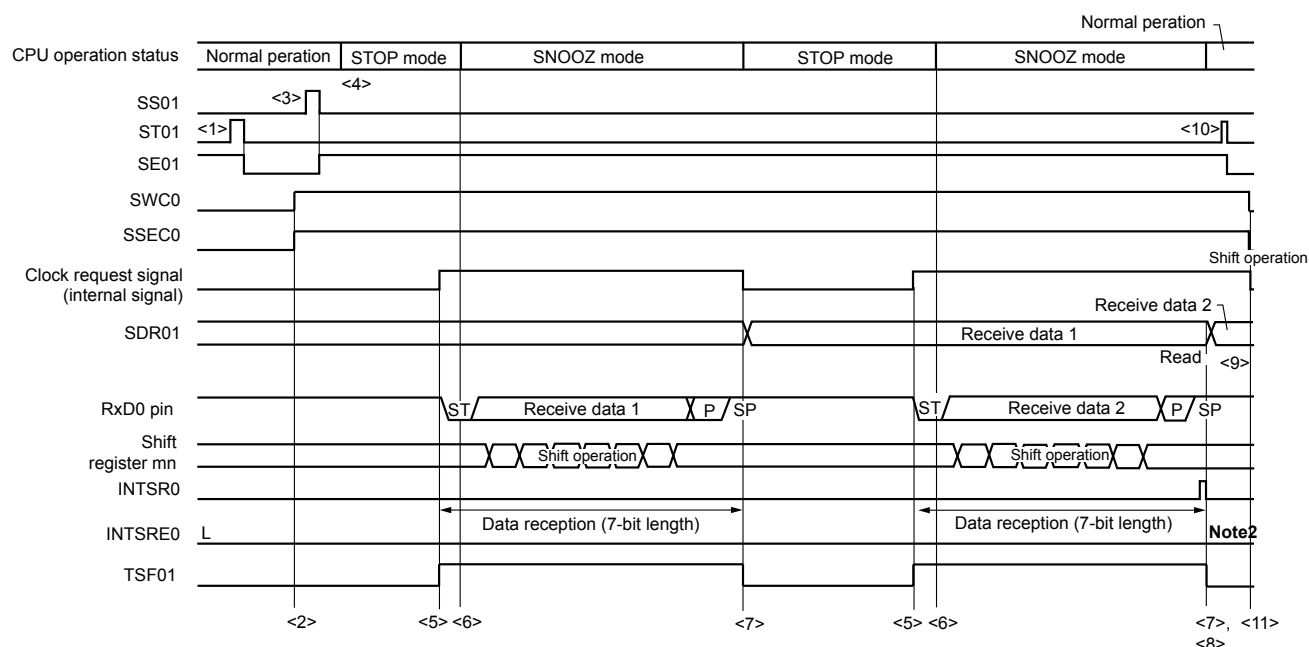


**Remarks 1.** <1> to <11> in the figure correspond to <1> to <11> in **Figure 12-89. Timing Chart of SNOOZE Mode Operation (Normal operation mode)** and **Figure 12-90. Timing Chart of SNOOZE Mode Operation (Abnormal Operation <1>).**

**2.** m = 0; q = 0

**(3) SNOOZE mode operation (Abnormal Operation <2>)**

Abnormal operation <2> is the operation performed when a communication error occurs while  $SSECm = 1$ . Because  $SSECm = 1$ , an error interrupt (INTSREq) is not generated when a communication error occurs.

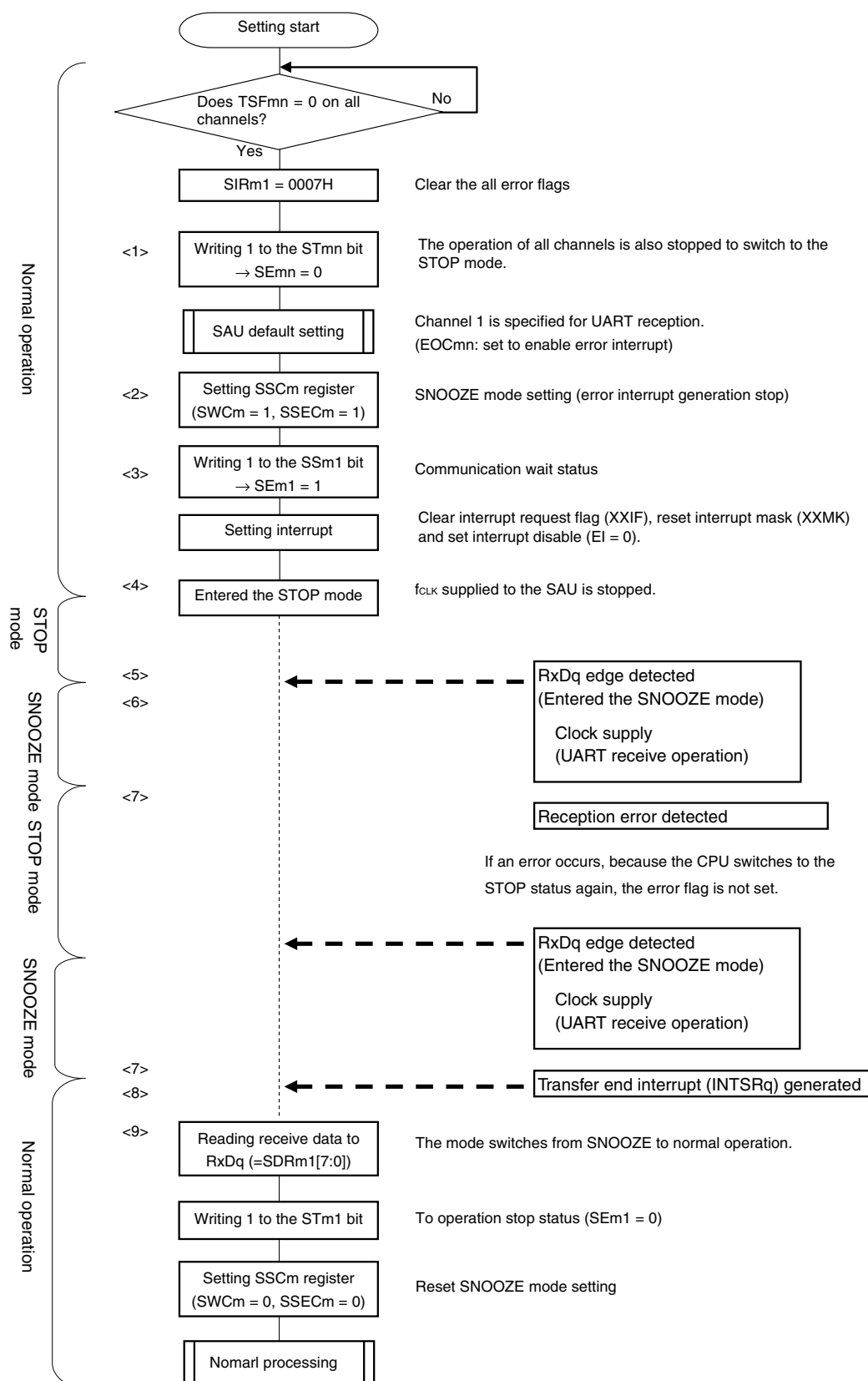
**Figure 12-92. Timing Chart of SNOOZE Mode Operation (Abnormal Operation <2>)**

- <R> **Notes**
1. Only read received data while  $SWCm = 1$  and before the next edge of the RxDq pin input is detected.
  2. After UARTq successfully finishes reception in the SNOOZE mode, it is possible to continue to perform normal reception operations without changing the settings, but, because  $SSECm = 1$ , the PEFm1 and FEFm1 bits are not set even if a framing error or parity error occurs. In addition, no error interrupt (INTSREq) is generated.

- <R> **Cautions**
1. Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, be sure to set the STm1 bit to 1 and clear the SEM1 bit (to stop the operation). And after completion the receive operation, also clearing SWCm bit to 0 (SNOOZE mode release).
  2. When using the SNOOZE mode while  $SSECm$  is set to 1, no overrun errors occur. Therefore, when using the SNOOZE mode, read bits 7 to 0 (RxDq) of the SDRm1 register before switching to the STOP mode.

- Remarks**
1. <1> to <9> in the figure correspond to <1> to <9> in **Figure 12-93. Flowchart of SNOOZE Mode Operation (Abnormal Operation <2>)**.
  2.  $m = 0$ ;  $q = 0$

&lt;R&gt;

**Figure 12-93. Flowchart of SNOOZE Mode Operation (Abnormal Operation <2>)**



**Caution** When using the SNOOZE mode while SSECm is set to 1, no overrun errors occur. Therefore, when using the SNOOZE mode, read bits 7 to 0 (RxDq) of the SDRm1 register before switching to the STOP mode.

**Remarks 1.** <1> to <9> in the figure correspond to <1> to <9> in **Figure 12-92. Timing Chart of SNOOZE Mode Operation (Abnormal Operation <2>).**

**2.** m = 0; q = 0

### 12.6.4 Calculating baud rate

#### (1) Baud rate calculation expression

The baud rate for UART (UART0) communication can be calculated by the following expressions.

$$(\text{Baud rate}) = \{\text{Operation clock (f}_{\text{MCK}}\text{) frequency of target channel}\} \div (\text{SDRmn}[15:9] + 1) \div 2 \text{ [bps]}$$

**Caution** Setting serial data register mn (SDRmn) SDRmn[15:9] = (0000000B, 0000001B) is prohibited.

**Remarks 1.** When UART is used, the value of SDRmn[15:9] is the value of bits 15 to 9 of the SDRmn register (0000010B to 1111111B) and therefore is 2 to 127.

**2.** m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01

The operation clock (f<sub>MCK</sub>) is determined by serial clock select register m (SPSm) and bit 15 (CKSmn) of serial mode register mn (SMRmn).

Table 12-3. Selection of Operation Clock For UART

| SMRmn Register   | SPSm Register |         |         |         |         |         |         |         | Operation Clock (f <sub>CLK</sub> ) <sup>Note</sup> |                           |
|------------------|---------------|---------|---------|---------|---------|---------|---------|---------|-----------------------------------------------------|---------------------------|
| CKSmn            | PRS m13       | PRS m12 | PRS m11 | PRS m10 | PRS m03 | PRS m02 | PRS m01 | PRS m00 |                                                     | f <sub>CLK</sub> = 24 MHz |
| 0                | X             | X       | X       | X       | 0       | 0       | 0       | 0       | f <sub>CLK</sub>                                    | 24 MHz                    |
|                  | X             | X       | X       | X       | 0       | 0       | 0       | 1       | f <sub>CLK</sub> /2                                 | 12 MHz                    |
|                  | X             | X       | X       | X       | 0       | 0       | 1       | 0       | f <sub>CLK</sub> /2 <sup>2</sup>                    | 6 MHz                     |
|                  | X             | X       | X       | X       | 0       | 0       | 1       | 1       | f <sub>CLK</sub> /2 <sup>3</sup>                    | 3 MHz                     |
|                  | X             | X       | X       | X       | 0       | 1       | 0       | 0       | f <sub>CLK</sub> /2 <sup>4</sup>                    | 1.5 MHz                   |
|                  | X             | X       | X       | X       | 0       | 1       | 0       | 1       | f <sub>CLK</sub> /2 <sup>5</sup>                    | 750 kHz                   |
|                  | X             | X       | X       | X       | 0       | 1       | 1       | 0       | f <sub>CLK</sub> /2 <sup>6</sup>                    | 375 kHz                   |
|                  | X             | X       | X       | X       | 0       | 1       | 1       | 1       | f <sub>CLK</sub> /2 <sup>7</sup>                    | 187.5 kHz                 |
|                  | X             | X       | X       | X       | 1       | 0       | 0       | 0       | f <sub>CLK</sub> /2 <sup>8</sup>                    | 93.8 kHz                  |
|                  | X             | X       | X       | X       | 1       | 0       | 0       | 1       | f <sub>CLK</sub> /2 <sup>9</sup>                    | 46.9 kHz                  |
|                  | X             | X       | X       | X       | 1       | 0       | 1       | 0       | f <sub>CLK</sub> /2 <sup>10</sup>                   | 23.4 kHz                  |
|                  | X             | X       | X       | X       | 1       | 0       | 1       | 1       | f <sub>CLK</sub> /2 <sup>11</sup>                   | 11.7 kHz                  |
|                  | X             | X       | X       | X       | 1       | 1       | 0       | 0       | f <sub>CLK</sub> /2 <sup>12</sup>                   | 5.86 kHz                  |
|                  | X             | X       | X       | X       | 1       | 1       | 0       | 1       | f <sub>CLK</sub> /2 <sup>13</sup>                   | 2.93 kHz                  |
|                  | X             | X       | X       | X       | 1       | 1       | 1       | 0       | f <sub>CLK</sub> /2 <sup>14</sup>                   | 1.46 kHz                  |
|                  | X             | X       | X       | X       | 1       | 1       | 1       | 1       | f <sub>CLK</sub> /2 <sup>15</sup>                   | 732 Hz                    |
| 1                | 0             | 0       | 0       | 0       | X       | X       | X       | X       | f <sub>CLK</sub>                                    | 24 MHz                    |
|                  | 0             | 0       | 0       | 1       | X       | X       | X       | X       | f <sub>CLK</sub> /2                                 | 12 MHz                    |
|                  | 0             | 0       | 1       | 0       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>2</sup>                    | 6 MHz                     |
|                  | 0             | 0       | 1       | 1       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>3</sup>                    | 3 MHz                     |
|                  | 0             | 1       | 0       | 0       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>4</sup>                    | 1.5 MHz                   |
|                  | 0             | 1       | 0       | 1       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>5</sup>                    | 750 kHz                   |
|                  | 0             | 1       | 1       | 0       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>6</sup>                    | 375 kHz                   |
|                  | 0             | 1       | 1       | 1       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>7</sup>                    | 187.5 kHz                 |
|                  | 1             | 0       | 0       | 0       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>8</sup>                    | 93.8 kHz                  |
|                  | 1             | 0       | 0       | 1       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>9</sup>                    | 46.9 kHz                  |
|                  | 1             | 0       | 1       | 0       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>10</sup>                   | 23.4 kHz                  |
|                  | 1             | 0       | 1       | 1       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>11</sup>                   | 11.7 kHz                  |
|                  | 1             | 1       | 0       | 0       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>12</sup>                   | 5.86 kHz                  |
|                  | 1             | 1       | 0       | 1       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>13</sup>                   | 2.93 kHz                  |
|                  | 1             | 1       | 1       | 0       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>14</sup>                   | 1.46 kHz                  |
|                  | 1             | 1       | 1       | 1       | X       | X       | X       | X       | f <sub>CLK</sub> /2 <sup>15</sup>                   | 732 Hz                    |
| Other than above |               |         |         |         |         |         |         |         | Setting prohibited                                  |                           |

**Note** When changing the clock selected for f<sub>CLK</sub> (by changing the system clock control register (CKC) value), do so after having stopped (serial channel stop register m (STm) = 000FH) the operation of the serial array unit (SAU).

**Remarks 1.** X: Don't care

**2.** m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01

**(2) Baud rate error during transmission**

The baud rate error of UART (UART0) communication during transmission can be calculated by the following expression. Make sure that the baud rate at the transmission side is within the permissible baud rate range at the reception side.

$$(\text{Baud rate error}) = (\text{Calculated baud rate value}) \div (\text{Target baud rate}) \times 100 - 100 [\%]$$

Here is an example of setting a UART baud rate at  $f_{\text{CLK}} = 24 \text{ MHz}$ .

| UART Baud Rate<br>(Target Baud Rate) | $f_{\text{CLK}} = 24 \text{ MHz}$    |             |                      |                             |
|--------------------------------------|--------------------------------------|-------------|----------------------|-----------------------------|
|                                      | Operation Clock ( $f_{\text{MCK}}$ ) | SDRmn[15:9] | Calculated Baud Rate | Error from Target Baud Rate |
| 300 bps                              | $f_{\text{CLK}}/2^9$                 | 77          | 300.48 bps           | +0.16 %                     |
| 600 bps                              | $f_{\text{CLK}}/2^8$                 | 77          | 600.96 bps           | +0.16 %                     |
| 1200 bps                             | $f_{\text{CLK}}/2^7$                 | 77          | 1201.92 bps          | +0.16 %                     |
| 2400 bps                             | $f_{\text{CLK}}/2^6$                 | 77          | 2403.85 bps          | +0.16 %                     |
| 4800 bps                             | $f_{\text{CLK}}/2^5$                 | 77          | 4807.69 bps          | +0.16 %                     |
| 9600 bps                             | $f_{\text{CLK}}/2^4$                 | 77          | 9615.38 bps          | +0.16 %                     |
| 19200 bps                            | $f_{\text{CLK}}/2^3$                 | 77          | 19230.8 bps          | +0.16 %                     |
| 31250 bps                            | $f_{\text{CLK}}/2^3$                 | 47          | 31250.0 bps          | $\pm 0.0 \%$                |
| 38400 bps                            | $f_{\text{CLK}}/2^2$                 | 77          | 38461.5 bps          | +0.16 %                     |
| 76800 bps                            | $f_{\text{CLK}}/2$                   | 77          | 76923.1 bps          | +0.16 %                     |
| 153600 bps                           | $f_{\text{CLK}}$                     | 77          | 153846 bps           | +0.16 %                     |
| 312500 bps                           | $f_{\text{CLK}}$                     | 37          | 315789 bps           | $\pm 1.05 \%$               |

**Remark** m: Unit number (m = 0), n: Channel number (n = 0), mn = 00

**(3) Permissible baud rate range for reception**

The permissible baud rate range for reception during UART (UART0) communication can be calculated by the following expression. Make sure that the baud rate at the transmission side is within the permissible baud rate range at the reception side.

$$(\text{Maximum receivable baud rate}) = \frac{2 \times k \times \text{Nfr}}{2 \times k \times \text{Nfr} - k + 2} \times \text{Brate}$$

$$(\text{Minimum receivable baud rate}) = \frac{2 \times k \times (\text{Nfr} - 1)}{2 \times k \times \text{Nfr} - k - 2} \times \text{Brate}$$

Brate: Calculated baud rate value at the reception side (See **12.6.4 (1) Baud rate calculation expression.**)

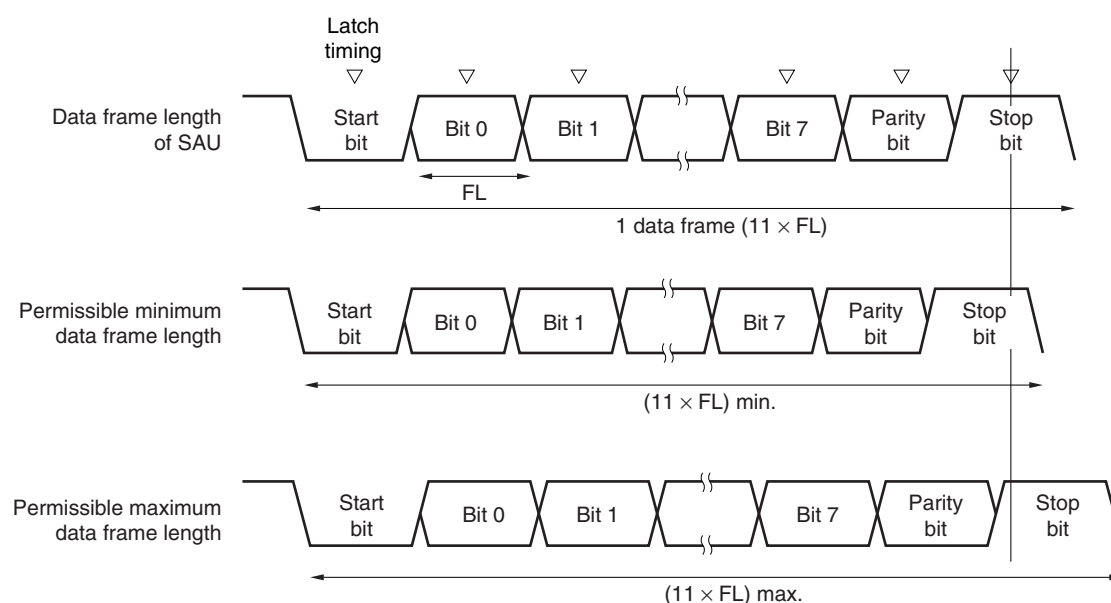
k: SDRmn[15:9] + 1

Nfr: 1 data frame length [bits]

= (Start bit) + (Data length) + (Parity bit) + (Stop bit)

**Remark** m: Unit number (m = 0), n: Channel number (n = 1), mn = 01

**Figure 12-94. Permissible Baud Rate Range for Reception (1 Data Frame Length = 11 Bits)**



As shown in Figure 12-94, the timing of latching receive data is determined by the division ratio set by bits 15 to 9 of serial data register mn (SDRmn) after the start bit is detected. If the last data (stop bit) is received before this latch timing, the data can be correctly received.

### 12.6.5 Procedure for processing errors that occurred during UART (UART0) communication

The procedure for processing errors that occurred during UART (UART0) communication is described in Figures 12-97 and 12-98.

**Figure 12-95. Processing Procedure in Case of Parity Error or Overrun Error**

| Software Manipulation                                        | Hardware Status                                                                           | Remark                                                                                                                                  |
|--------------------------------------------------------------|-------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| Reads serial data register mn (SDRmn). →                     | The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data. | This is to prevent an overrun error if the next reception is completed during error processing.                                         |
| Reads serial status register mn (SSRmn).                     |                                                                                           | Error type is identified and the read value is used to clear error flag.                                                                |
| Writes 1 to serial flag clear trigger register mn (SIRmn). → | Error flag is cleared.                                                                    | Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification. |

**Figure 12-96. Processing Procedure in Case of Framing Error**

| Software Manipulation                                              | Hardware Status                                                                                                | Remark                                                                                                                                                                                                  |
|--------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reads serial data register mn (SDRmn). →                           | The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data.                      | This is to prevent an overrun error if the next reception is completed during error processing.                                                                                                         |
| Reads serial status register mn (SSRmn).                           |                                                                                                                | Error type is identified and the read value is used to clear error flag.                                                                                                                                |
| Writes serial flag clear trigger register mn (SIRmn). →            | Error flag is cleared.                                                                                         | Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.                                                                 |
| Sets the STmn bit of serial channel stop register m (STm) to 1. →  | The SEMn bit of serial channel enable status register m (SEm) is set to 0 and channel n stops operating.       |                                                                                                                                                                                                         |
| Synchronization with other party of communication                  |                                                                                                                | Synchronization with the other party of communication is re-established and communication is resumed because it is considered that a framing error has occurred because the start bit has been shifted. |
| Sets the SSmn bit of serial channel start register m (SSm) to 1. → | The SEMn bit of serial channel enable status register m (SEm) is set to 1 and channel n is enabled to operate. |                                                                                                                                                                                                         |

**Remark** m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01

## 12.7 LIN Communication Operation

### 12.7.1 LIN transmission

UART0 transmission supports LIN communication.

For LIN transmission, channel 0 is used.

| UART                         | UART0                                                                                                                     |
|------------------------------|---------------------------------------------------------------------------------------------------------------------------|
| Support of LIN communication | Supported                                                                                                                 |
| Target channel               | Channel 0                                                                                                                 |
| Pins used                    | TxD0                                                                                                                      |
| Interrupt                    | INTST0                                                                                                                    |
|                              | Transfer end interrupt (in single-transfer mode) or buffer empty interrupt (in continuous transfer mode) can be selected. |
| Error detection flag         | None                                                                                                                      |
| Transfer data length         | 8 bits                                                                                                                    |
| <R> Transfer rate            | Max. $f_{MCK}/6$ [bps] (SDR00 [15:9] = 2 or more), Min. $f_{CLK}/(2 \times 2^{15} \times 128)$ [bps] <sup>Note</sup>      |
| Data phase                   | Non-reverse output (default: high level)                                                                                  |
|                              | Reverse output (default: low level)                                                                                       |
| <R> Parity bit               | No parity bit                                                                                                             |
| <R> Stop bit                 | Appending 1 bit                                                                                                           |
| <R> Data direction           | LSB first                                                                                                                 |

**Note** Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS**). In addition, LIN communication is usually 2.4/9.6/19.2 kbps is often used.

**Remark**  $f_{MCK}$ : Operation clock frequency of target channel  
 $f_{CLK}$ : System clock frequency

LIN stands for Local Interconnect Network and is a low-speed (1 to 20 kbps) serial communication protocol designed to reduce the cost of an automobile network.

Communication of LIN is single-master communication and up to 15 slaves can be connected to one master.

The slaves are used to control switches, actuators, and sensors, which are connected to the master via LIN.

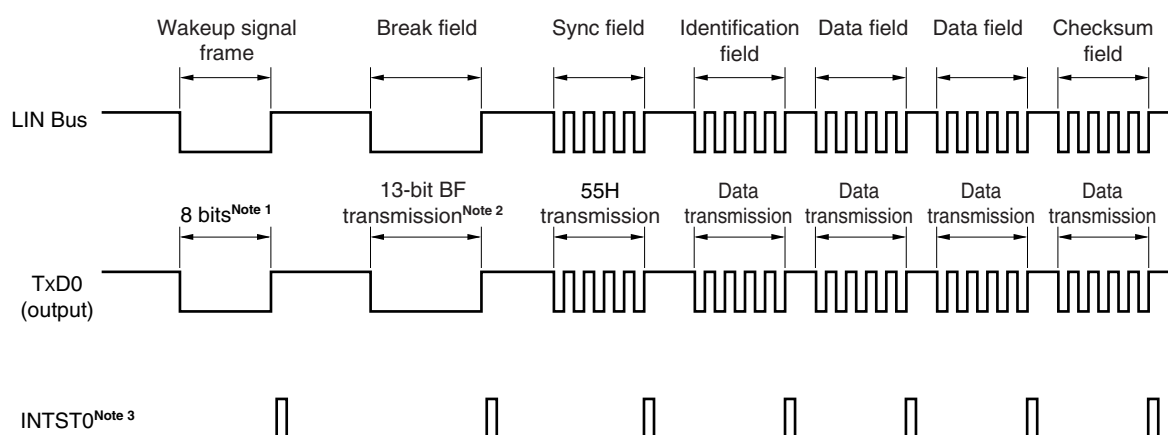
Usually, the master is connected to a network such as CAN (Controller Area Network).

A LIN bus is a single-wire bus to which nodes are connected via transceiver conforming to ISO9141.

According to the protocol of LIN, the master transmits a frame by attaching baud rate information to it. A slave receives this frame and corrects a baud rate error from the master. If the baud rate error of a slave is within  $\pm 15\%$ , communication can be established.

Figure 12-97 outlines a transmission operation of LIN.

**Figure 12-97. Transmission Operation of LIN**



<R> **Notes 1.** Data of 80H is transmitted.

**2.** A break field is defined to have a width of 13 bits and output a low level. Where the baud rate for main transfer is N [bps], therefore, the baud rate of the break field is calculated as follows.

$$(\text{Baud rate of break field}) = 9/13 \times N$$

By transmitting data of 00H at this baud rate, a break field is generated.

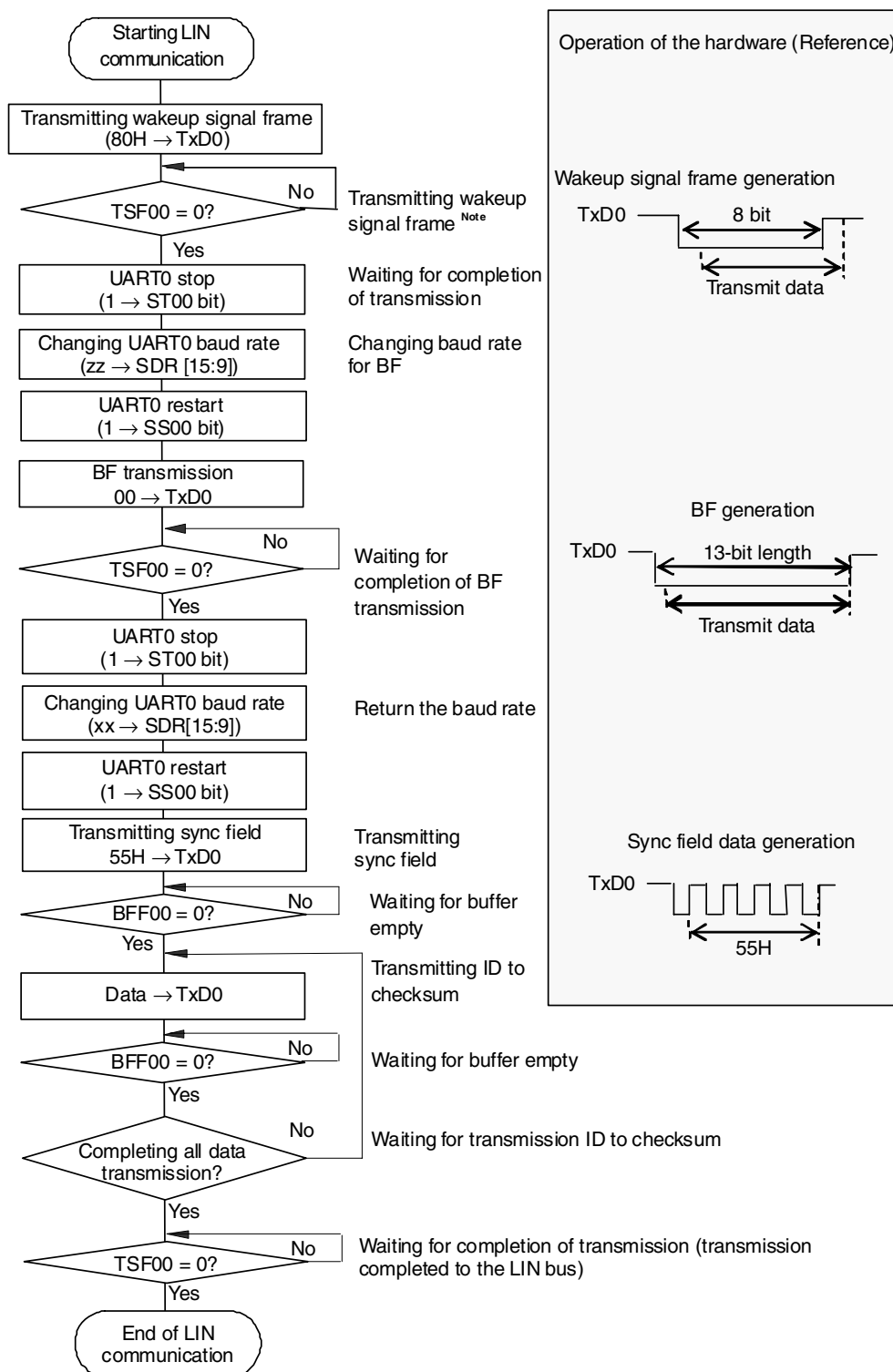
<R> **3.** INTST0 is output upon completion of transmission.

**Remark** The interval between fields is controlled by software.



&lt;R&gt;

Figure 12-98. Flowchart for LIN Transmission



**Note** When LIN-bus start from sleep status only

**Remark** Default setting of the UART is complete, and the flow from the transmission enable status.

### 12.7.2 LIN reception

UART0 reception supports LIN communication.

For LIN reception, channel 1 is used.

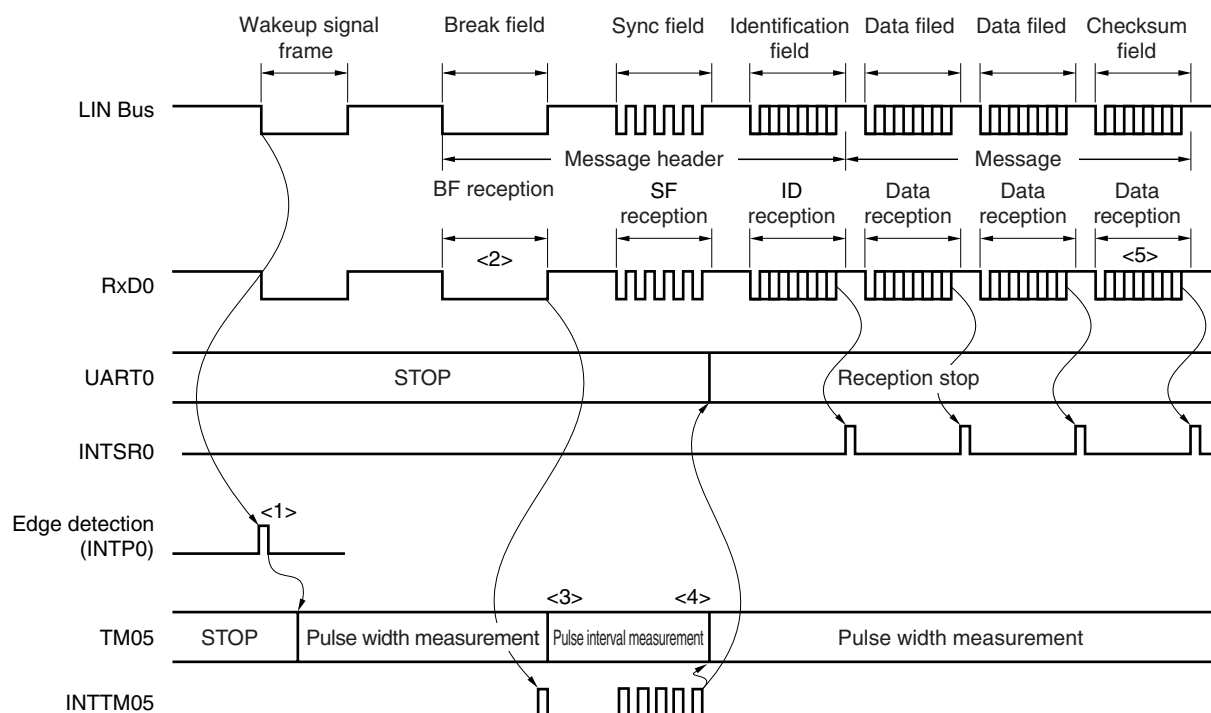
| UART                         | UART0                                                                                                                                    |
|------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|
| Support of LIN communication | Supported                                                                                                                                |
| Target channel               | Channel 1                                                                                                                                |
| Pins used                    | RxD0                                                                                                                                     |
| <R> Interrupt                | INTSR0                                                                                                                                   |
|                              | Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)                                                          |
| <R> Error interrupt          | INTSRE0                                                                                                                                  |
| <R> Error detection flag     | <ul style="list-style-type: none"> <li>• Framing error detection flag (FEF01)</li> <li>• Overrun error detection flag (OVF01)</li> </ul> |
| Transfer data length         | 8 bits                                                                                                                                   |
| Transfer rate                | Max. $f_{MCK}/6$ [bps] (SDR01 [15:9] = 2 or more), Min. $f_{CLK}/(2 \times 2^{15} \times 128)$ [bps] <sup>Note</sup>                     |
| Data phase                   | Non-reverse output (default: high level)<br>Reverse output (default: low level)                                                          |
| <R> Parity bit               | No parity bit (The parity bit is not checked.)                                                                                           |
| <R> Stop bit                 | Check the first bit                                                                                                                      |
| <R> Data direction           | LSB first                                                                                                                                |

**Note** Use this operation within a range that satisfies the conditions above and the peripheral functions characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS**).

**Remark**  $f_{MCK}$ : Operation clock frequency of target channel  
 $f_{CLK}$ : System clock frequency

Figure 12-99 outlines a reception operation of LIN.

Figure 12-99. Reception Operation of LIN



Here is the flow of signal processing.

- <R> <1> The wakeup signal is detected by detecting an interrupt edge (INTP0) on a pin. When the wakeup signal is detected, change TM05 to pulse width measurement upon detection of the wakeup signal to measure the low-level width of the BF signal. Then wait for BF signal reception.
- <R> <2> TM05 starts measuring the low-level width upon detection of the falling edge of the BF signal, and then captures the data upon detection of the rising edge of the BF signal. The captured data is used to judge whether it is the BF signal.
- <R> <3> When BF reception has been correctly completed, start channel 5 of the timer array unit and measure the bit interval (pulse width) of the sync field (see **6.7.4 Operation as input pulse interval measurement**).
- <4> Calculate a baud rate error from the bit interval of sync field (SF). Stop UART0 once and adjust (re-set) the baud rate.
- <5> The checksum field should be distinguished by software. In addition, processing to initialize UART0 after the checksum field is received and to wait for reception of BF should also be performed by software.

&lt;R&gt;

Figure 12-100. Flowchart for LIN Reception

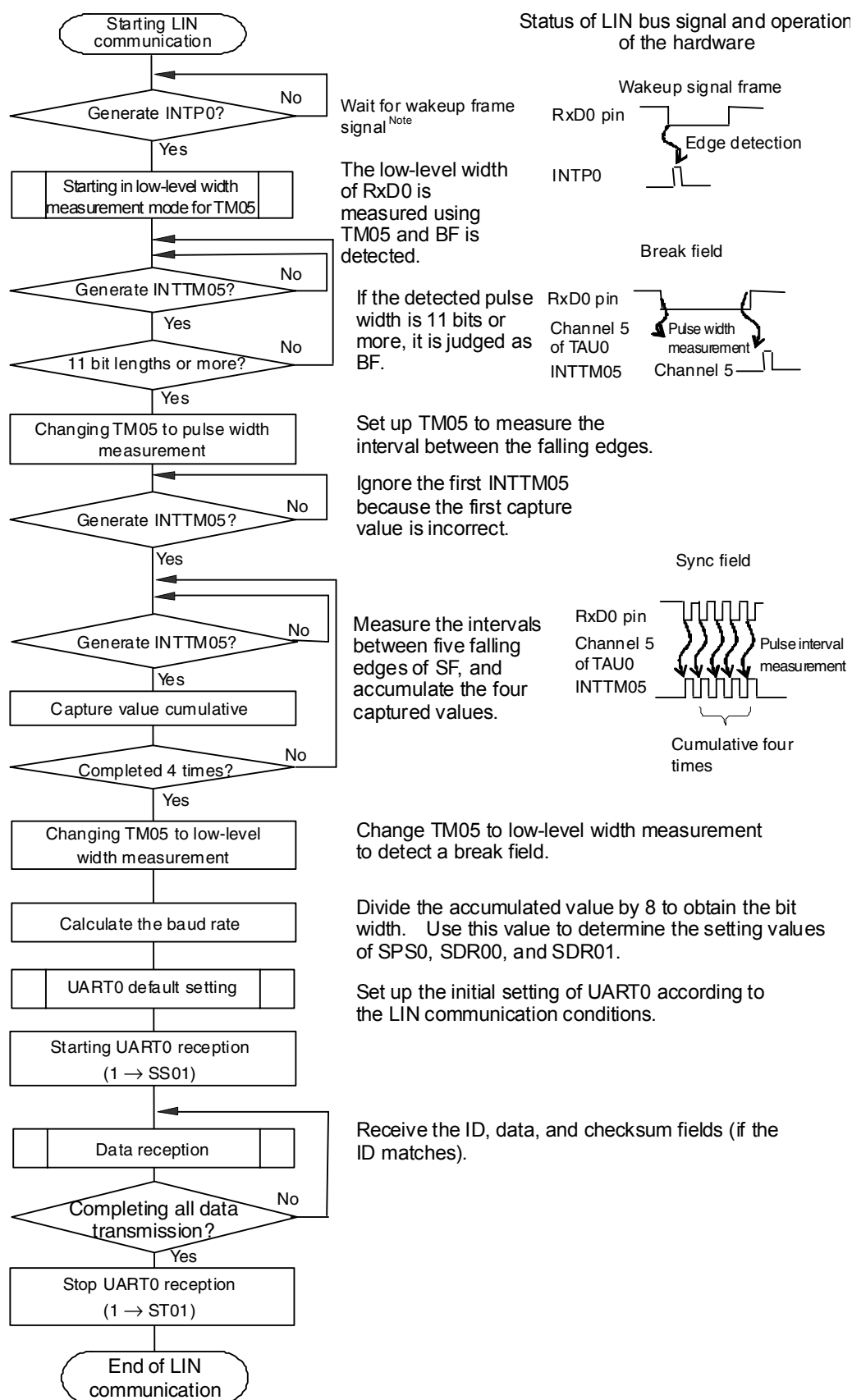
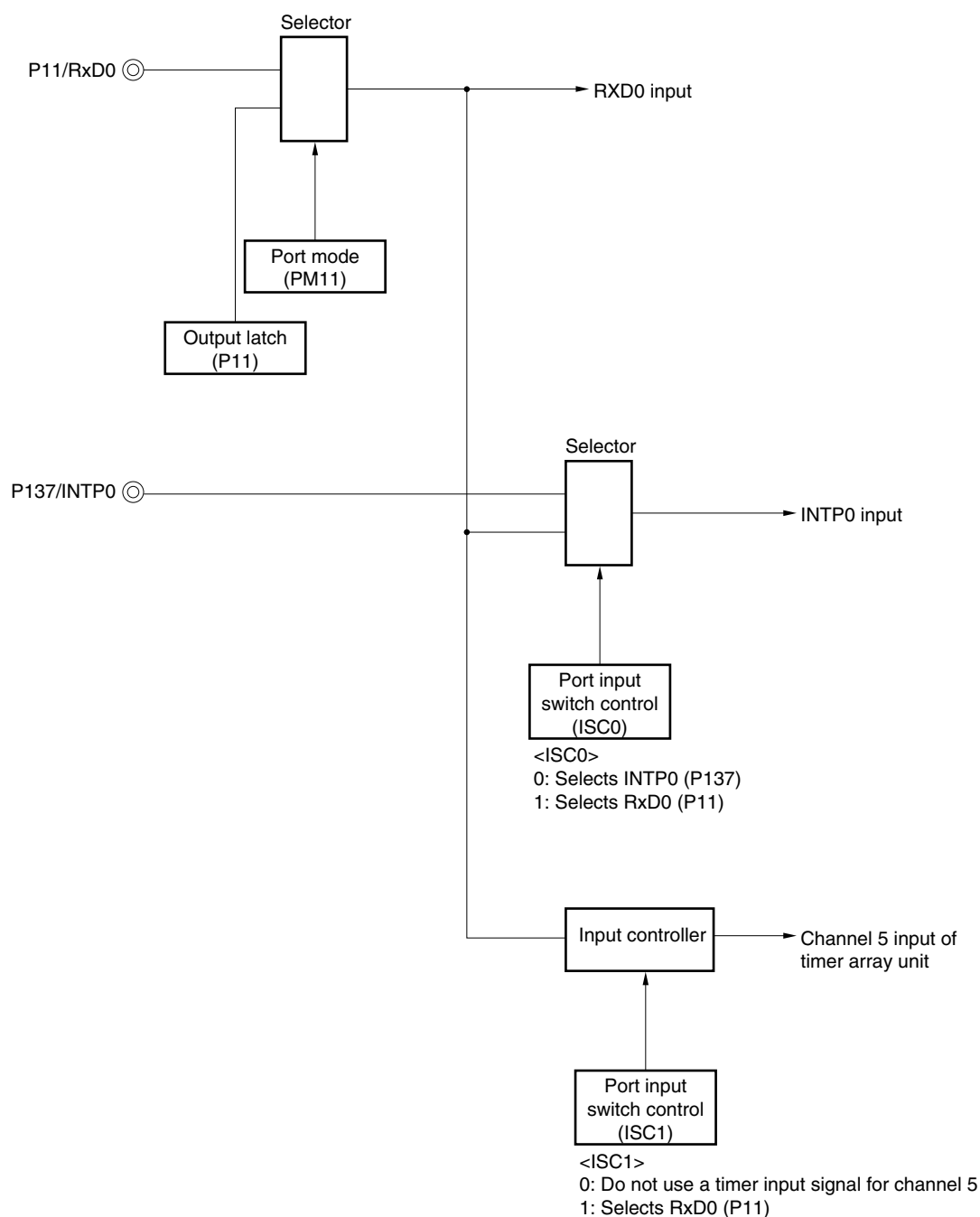
**Note** Required in the sleep status only.

Figure 12-101 and figure 12-102 show the configuration of a port that manipulates reception of LIN.

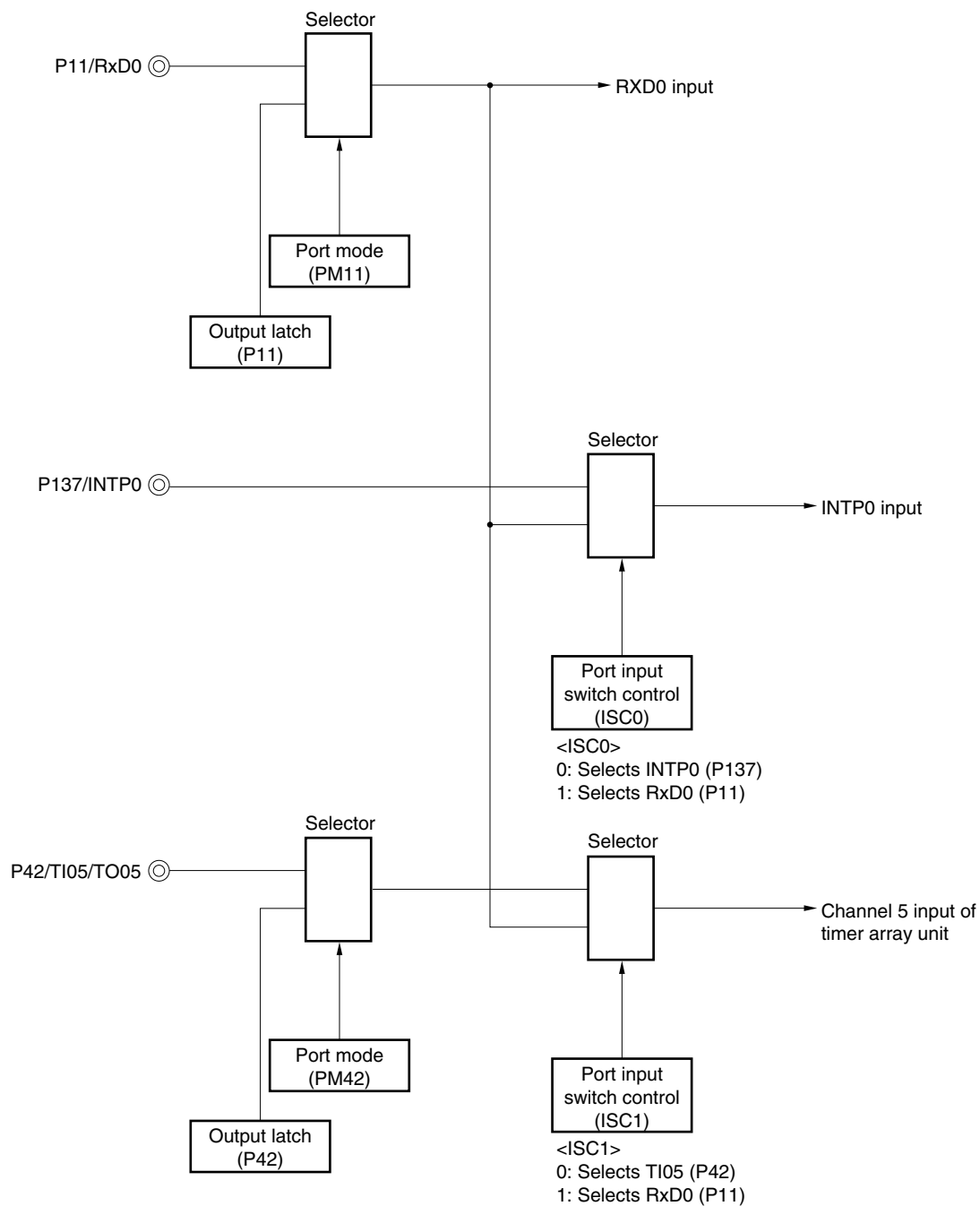
The wakeup signal transmitted from the master of LIN is received by detecting an edge of an external interrupt (INTP0). The length of the sync field transmitted from the master can be measured by using the external event capture operation of the timer array unit to calculate a baud-rate error.

By controlling switch of port input (ISC0/ISC1), the input source of port input (RxD0) for reception can be input to the external interrupt pin (INTP0) and timer array unit

**Figure 12-101. Port Configuration for Manipulating Reception of LIN (32, 44, 48-pin)**



**Remark** ISC0, ISC1: Bits 0 and 1 of the input switch control register (ISC) (See **Figure 12-17.**)

**Figure 12-102. Port Configuration for Manipulating Reception of LIN (52-, 64-pin)**

**Remark** ISC0, ISC1: Bits 0 and 1 of the input switch control register (ISC) (See **Figure 12-17**.)

The peripheral functions used for the LIN communication operation are as follows.

<Peripheral functions used>

- External interrupt (INTP0); Wakeup signal detection

Usage: To detect an edge of the wakeup signal and the start of communication

<R>

- Channel 5 of timer array unit; Baud rate error detection, break field detection.

Usage: To detect the length of the sync field (SF) and divide it by the number of bits in order to detect an error (The interval of the edge input to RxD0 is measured in the capture mode.)

Measured the low-level width, determine whether break field (BF).

- Channels 0 and 1 (UART0) of serial array unit (SAU)

## CHAPTER 13 SERIAL INTERFACE IICA

### 13.1 Functions of Serial Interface IICA

Serial interface IICA has the following three modes.

#### (1) Operation stop mode

This mode is used when serial transfers are not performed. It can therefore be used to reduce power consumption.

#### (2) I<sup>2</sup>C bus mode (multimaster supported)

This mode is used for 8-bit data transfers with several devices via two lines: a serial clock (SCLA0) line and a serial data bus (SDAA0) line.

This mode complies with the I<sup>2</sup>C bus format and the master device can generate “start condition”, “address”, “transfer direction specification”, “data”, and “stop condition” data to the slave device, via the serial data bus. The slave device automatically detects these received status and data by hardware. This function can simplify the part of application program that controls the I<sup>2</sup>C bus.

Since the SCLA0 and SDAA0 pins are used for open drain outputs, serial interface IICA requires pull-up resistors for the serial clock line and the serial data bus line.

#### (3) Wakeup mode

The STOP mode can be released by generating an interrupt request signal (INTIICA0) when an extension code from the master device or a local address has been received while in STOP mode. This can be set by using the WUP0 bit of IICA control register 01 (IICCTL01).

Figure 13-1 shows a block diagram of serial interface IICA.



Figure 13-1. Block Diagram of Serial Interface IICA

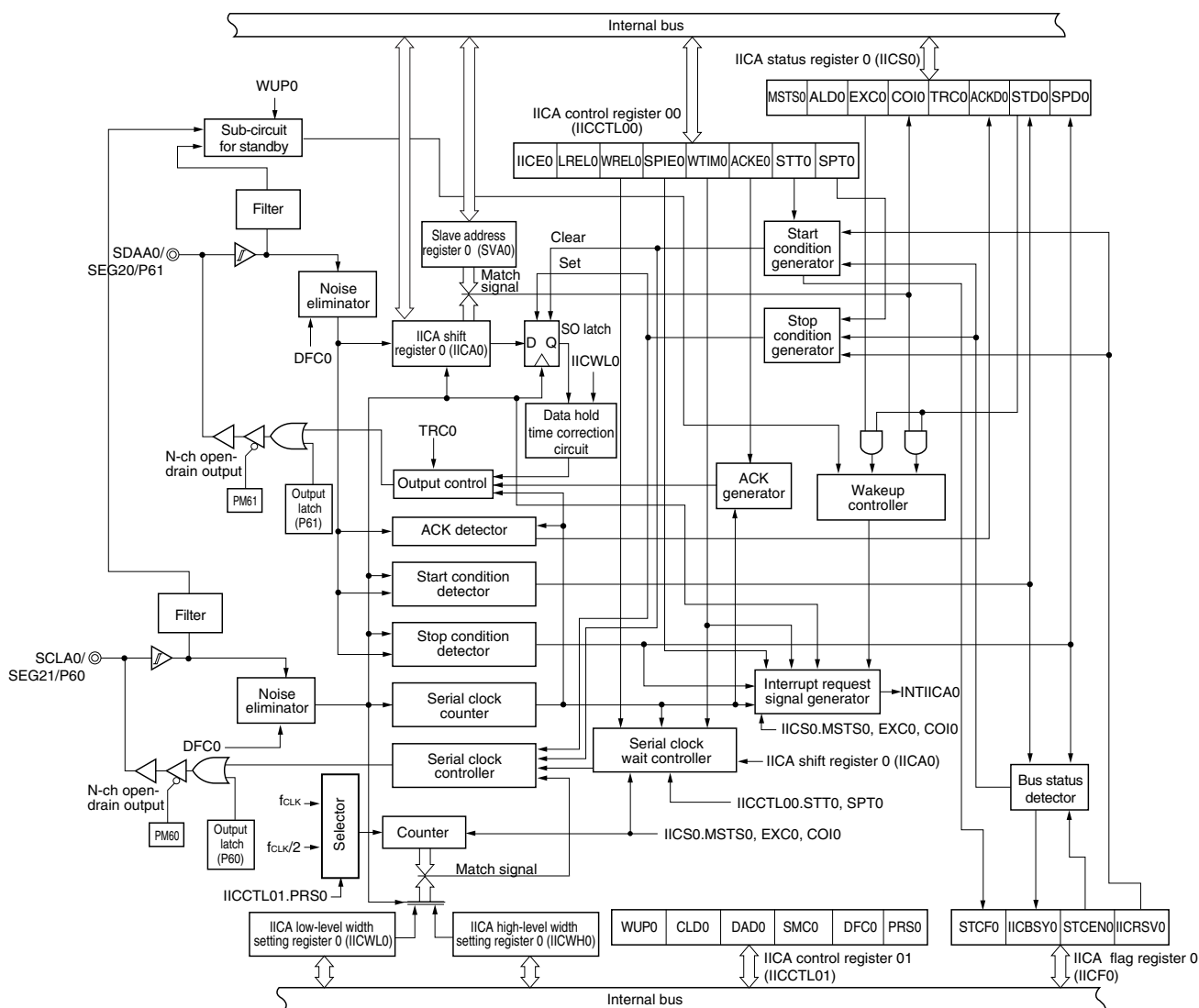
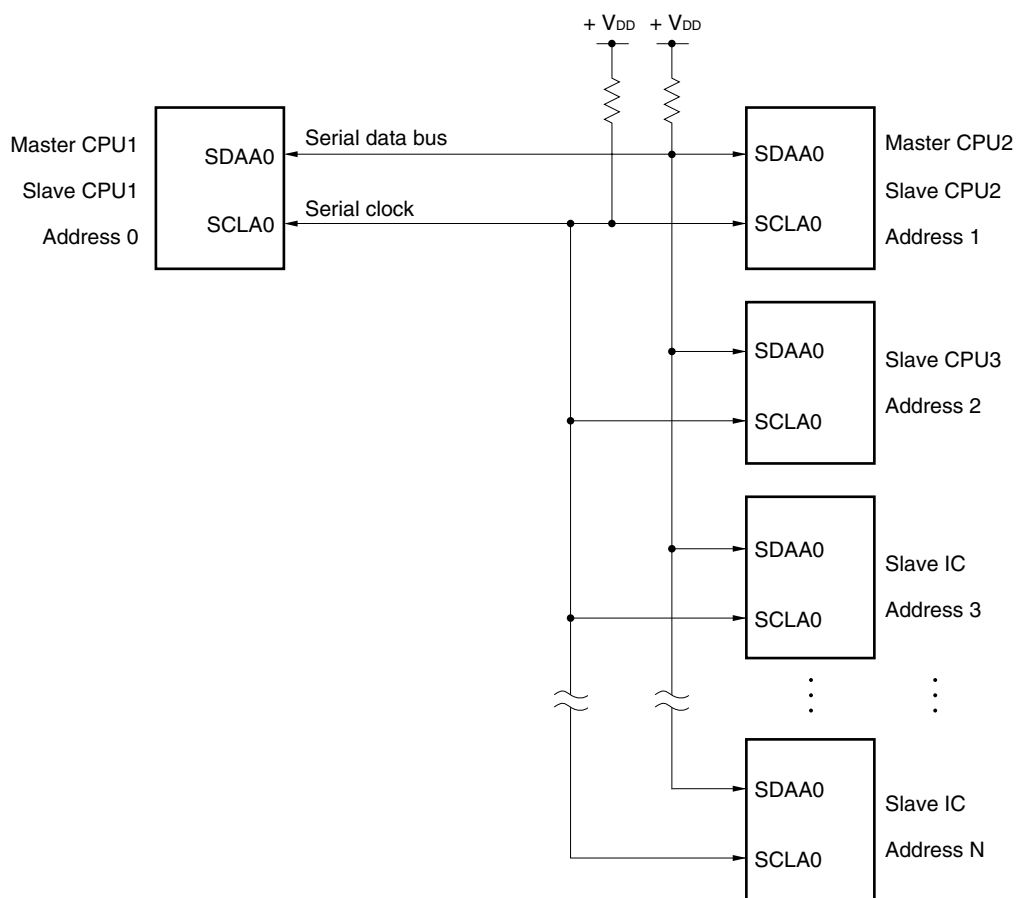


Figure 13-2 shows a serial bus configuration example.

**Figure 13-2. Serial Bus Configuration Example Using I<sup>2</sup>C Bus**



## 13.2 Configuration of Serial Interface IICA

Serial interface IICA includes the following hardware.

**Table 13-1. Configuration of Serial Interface IICA**

| Item              | Configuration                                                                                                                                                                                                                                                                                                                                      |
|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Registers         | IICA shift register 0 (IICA0)<br>Slave address register 0 (SVA0)                                                                                                                                                                                                                                                                                   |
| Control registers | Peripheral enable register 0 (PER0)<br>IICA control register 00 (IICCTL00)<br>IICA status register 0 (IICS0)<br>IICA flag register 0 (IICF0)<br>IICA control register 01 (IICCTL01)<br>IICA low-level width setting register 0 (IICWL0)<br>IICA high-level width setting register 0 (IICWH0)<br>Port mode register 6 (PM6)<br>Port register 6 (P6) |

### (1) IICA shift register 0 (IICA0)

The IICA0 register is used to convert 8-bit serial data to 8-bit parallel data and vice versa in synchronization with the serial clock. The IICA0 register can be used for both transmission and reception.

The actual transmit and receive operations can be controlled by writing and reading operations to the IICA0 register. Cancel the wait state and start data transfer by writing data to the IICA0 register during the wait period.

The IICA0 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears IICA0 to 00H.

**Figure 13-3. Format of IICA Shift Register 0 (IICA0)**

Address: FFF50H (IICA0)    After reset: 00H    R/W

|        |   |   |   |   |   |   |   |   |
|--------|---|---|---|---|---|---|---|---|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IICA0  |   |   |   |   |   |   |   |   |

**Cautions 1. Do not write data to the IICA0 register during data transfer.**

**2. Write or read the IICA0 register only during the wait period. Accessing the IICA0 register in a communication state other than during the wait period is prohibited. When the device serves as the master, however, the IICA0 register can be written only once after the communication trigger bit (STT0) is set to 1.**

**3. When communication is reserved, write data to the IICA0 register after the interrupt triggered by a stop condition is detected.**

### (2) Slave address register 0 (SVA0)

This register stores seven bits of local addresses {A6, A5, A4, A3, A2, A1, A0} when in slave mode.

The SVA0 register can be set by an 8-bit memory manipulation instruction.

However, rewriting to this register is prohibited while STD0 = 1 (while the start condition is detected).

Reset signal generation clears the SVA0 register to 00H.

**Figure 13-4. Format of Slave Address Register 0 (SVA0)**

Address: F0234H (SVA0)    After reset: 00H    R/W

|        |    |    |    |    |    |    |    |                   |
|--------|----|----|----|----|----|----|----|-------------------|
| Symbol | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                 |
| SVA0   | A6 | A5 | A4 | A3 | A2 | A1 | A0 | 0 <sup>Note</sup> |

**Note** Bit 0 is fixed to 0.**(3) SO latch**

The SO latch is used to retain the SDAA0 pin's output level.

**(4) Wakeup controller**

This circuit generates an interrupt request (INTIICA0) when the address received by this register matches the address value set to the slave address register 0 (SVA0) or when an extension code is received.

**(5) Serial clock counter**

This counter counts the serial clocks that are output or input during transmit/receive operations and is used to verify that 8-bit data was transmitted or received.

**(6) Interrupt request signal generator**

This circuit controls the generation of interrupt request signals (INTIICA0).

An I<sup>2</sup>C interrupt request is generated by the following two triggers.

- Falling edge of eighth or ninth clock of the serial clock (set by the WTIM0 bit)
- Interrupt request generated when a stop condition is detected (set by the SPIE0 bit)

**Remark** WTIM0 bit: Bit 3 of IICA control register 00 (IICCTL00)

SPIE0 bit: Bit 4 of IICA control register 00 (IICCTL00)

**(7) Serial clock controller**

In master mode, this circuit generates the clock output via the SCLA0 pin from a sampling clock.

**(8) Serial clock wait controller**

This circuit controls the wait timing.

**(9) ACK generator, stop condition detector, start condition detector, and ACK detector**

These circuits generate and detect each status.

**(10) Data hold time correction circuit**

This circuit generates the hold time for data corresponding to the falling edge of the serial clock.

**(11) Start condition generator**

This circuit generates a start condition when the STT0 bit is set to 1.

However, in the communication reservation disabled status (IICRSV bit = 1), when the bus is not released (IICBSY bit = 1), start condition requests are ignored and the STCF bit is set to 1.

**(12) Stop condition generator**

This circuit generates a stop condition when the SPT0 bit is set to 1.

**(13) Bus status detector**

This circuit detects whether or not the bus is released by detecting start conditions and stop conditions.

However, as the bus status cannot be detected immediately following operation, the initial status is set by the STCEN bit.

|               |             |                                              |
|---------------|-------------|----------------------------------------------|
| <b>Remark</b> | STT0 bit:   | Bit 1 of IICA control register 00 (IICCTL00) |
|               | SPT0 bit:   | Bit 0 of IICA control register 00 (IICCTL00) |
|               | IICRSV bit: | Bit 0 of IICA flag register 0 (IICF0)        |
|               | IICBSY bit: | Bit 6 of IICA flag register 0 (IICF0)        |
|               | STCF bit:   | Bit 7 of IICA flag register 0 (IICF0)        |
|               | STCEN bit:  | Bit 1 of IICA flag register 0 (IICF0)        |

### 13.3 Registers Controlling Serial Interface IICA

Serial interface IICA is controlled by the following eight registers.

- Peripheral enable register 0 (PER0)
- IICA control register 00 (IICCTL00)
- IICA flag register 0 (IICF0)
- IICA status register 0 (IICS0)
- IICA control register 01 (IICCTL01)
- IICA low-level width setting register 0 (IICWL0)
- IICA high-level width setting register 0 (IICWH0)
- Port mode register 6 (PM6)
- Port register 6 (P6)

#### 13.3.1 Peripheral enable register 0 (PER0)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When serial interface IICA0 is used, be sure to set bit 4 (IICA0EN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 13-5. Format of Peripheral Enable Register 0 (PER0)**

Address: F00F0H (PER0)    After reset: 00H    R/W

| Symbol | <7>   | 6 | <5>   | <4>     | 3 | <2>    | 1 | <0>    |
|--------|-------|---|-------|---------|---|--------|---|--------|
| PER0   | RTCEN | 0 | ADCEN | IICA0EN | 0 | SAU0EN | 0 | TAU0EN |

| IICA0EN | Control of serial interface IICA0 input clock supply                                                                                                                                          |
|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0       | Stops input clock supply. <ul style="list-style-type: none"> <li>• SFR used by serial interface IICA0 cannot be written.</li> <li>• Serial interface IICA0 is in the reset status.</li> </ul> |
| 1       | Enables input clock supply. <ul style="list-style-type: none"> <li>• SFR used by serial interface IICA0 can be read/written.</li> </ul>                                                       |

- Cautions**
1. When setting serial interface IICA0, be sure to set the IICA0EN bit to 1 first. If IICA0EN = 0, writing to a control register of serial interface IICA0 is ignored, and, even if the register is read, only the default value is read (except for port mode register 6 (PM6) and port register 6 (P6)).
  2. Be sure to clear the bits1, 3, and 6 to 0.

### 13.3.2 IICA control register 00 (IICCTL00)

This register is used to enable/stop I<sup>2</sup>C operations, set wait timing, and set other I<sup>2</sup>C operations.

The IICCTL00 register can be set by a 1-bit or 8-bit memory manipulation instruction. However, set the SPIE0, WTIM0, and ACKE0 bits while IICE0 = 0 or during the wait period. These bits can be set at the same time when the IICE0 bit is set from “0” to “1”.

Reset signal generation clears this register to 00H.

**Figure 13-6. Format of IICA Control Register 00 (IICCTL00) (1/4)**

Address: F0230H (IICCTL00)      After reset: 00H   R/W

|          |       |       |       |       |       |       |      |      |
|----------|-------|-------|-------|-------|-------|-------|------|------|
| Symbol   | <7>   | <6>   | <5>   | <4>   | <3>   | <2>   | <1>  | <0>  |
| IICCTL00 | IICE0 | LREL0 | WREL0 | SPIE0 | WTIM0 | ACKE0 | STT0 | SPT0 |

|                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                      |  |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------|--|
| IICE0                                                                                                                                                                                                                                                                                                                                               | I <sup>2</sup> C operation enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                                                      |  |
| 0                                                                                                                                                                                                                                                                                                                                                   | Stop operation. Reset the IICA status register 0 (IICS0) <sup>Note 1</sup> . Stop internal operation.                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                                                      |  |
| 1                                                                                                                                                                                                                                                                                                                                                   | Enable operation.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                                                      |  |
| Be sure to set this bit (1) while the SCLA0 and SDAA0 lines are at high level.                                                                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                      |  |
| Condition for clearing (IICE0 = 0)                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Condition for setting (IICE0 = 1)                                    |  |
| <ul style="list-style-type: none"><li>• Cleared by instruction</li><li>• Reset</li></ul>                                                                                                                                                                                                                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | <ul style="list-style-type: none"><li>• Set by instruction</li></ul> |  |
| LRELO <sup>Notes 2, 3</sup>                                                                                                                                                                                                                                                                                                                         | Exit from communications                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                      |  |
| 0                                                                                                                                                                                                                                                                                                                                                   | Normal operation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                      |  |
| 1                                                                                                                                                                                                                                                                                                                                                   | <p>This exits from the current communications and sets standby mode. This setting is automatically cleared to 0 after being executed.</p> <p>Its uses include cases in which a locally irrelevant extension code has been received.</p> <p>The SCLA0 and SDAA0 lines are set to high impedance.</p> <p>The following flags of IICA control register 00 (IICCTL00) and the IICA status register 0 (IICS0) are cleared to 0.</p> <ul style="list-style-type: none"><li>• STT0 • SPT0 • MSTS0 • EXC0 • COI0 • TRC0 • ACKD0 • STD0</li></ul> |                                                                      |  |
| <p>The standby mode following exit from communications remains in effect until the following communications entry conditions are met.</p> <ul style="list-style-type: none"><li>• After a stop condition is detected, restart is in master mode.</li><li>• An address match or extension code reception occurs after the start condition.</li></ul> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                      |  |
| Condition for clearing (LRELO = 0)                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Condition for setting (LRELO = 1)                                    |  |
| <ul style="list-style-type: none"><li>• Automatically cleared after execution</li><li>• Reset</li></ul>                                                                                                                                                                                                                                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | <ul style="list-style-type: none"><li>• Set by instruction</li></ul> |  |
| WRELO <sup>Notes 2, 3</sup>                                                                                                                                                                                                                                                                                                                         | Wait cancellation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                                                      |  |
| 0                                                                                                                                                                                                                                                                                                                                                   | Do not cancel wait                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                                                                      |  |
| 1                                                                                                                                                                                                                                                                                                                                                   | Cancel wait. This setting is automatically cleared after wait is canceled.                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                                                      |  |
| <p>When the WRELO bit is set (wait canceled) during the wait period at the ninth clock pulse in the transmission status (TRC0 = 1), the SDAA0 line goes into the high impedance state (TRC0 = 0).</p>                                                                                                                                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                      |  |
| Condition for clearing (WRELO = 0)                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Condition for setting (WRELO = 1)                                    |  |
| <ul style="list-style-type: none"><li>• Automatically cleared after execution</li><li>• Reset</li></ul>                                                                                                                                                                                                                                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | <ul style="list-style-type: none"><li>• Set by instruction</li></ul> |  |

**Notes 1.** The IICA status register 0 (IICS0), the STCF and IICBSY bits of the IICA flag register 0 (IICF0), and the CLD0 and DAD0 bits of IICA control register 01 (IICCTL01) are reset.

**2.** The signal of this bit is invalid while IICE0 is 0.

**3.** When the LREL0 and WREL0 bits are read, 0 is always read.

**Caution** If the operation of I<sup>2</sup>C is enabled (IICE0 = 1) when the SCLA0 line is high level, the SDAA0 line is low level, and the digital filter is turned on (DFC0 bit of IICCTL01 register = 1), a start condition will be inadvertently detected immediately. In this case, set (1) the LREL0 bit by using a 1-bit memory manipulation instruction immediately after enabling operation of I<sup>2</sup>C (IICE0 = 1).



Figure 13-6. Format of IICA Control Register 00 (IICCTL00) (2/4)

|                                                                                                                               |                                                                                |
|-------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------|
| SPIE0 <sup>Note 1</sup>                                                                                                       | Enable/disable generation of interrupt request when stop condition is detected |
| 0                                                                                                                             | Disable                                                                        |
| 1                                                                                                                             | Enable                                                                         |
| If the WUP0 bit of IICA control register 01 (IICCTL01) is 1, no stop condition interrupt will be generated even if SPIE0 = 1. |                                                                                |
| Condition for clearing (SPIE0 = 0)                                                                                            | Condition for setting (SPIE0 = 1)                                              |
| <ul style="list-style-type: none"> <li>• Cleared by instruction</li> <li>• Reset</li> </ul>                                   | <ul style="list-style-type: none"> <li>• Set by instruction</li> </ul>         |

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| WTIM0 <sup>Note 1</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Control of wait and interrupt request generation                                                                                                                                                                                                                                               |
| 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | <p>Interrupt request is generated at the eighth clock's falling edge.</p> <p>Master mode: After output of eight clocks, clock output is set to low level and wait is set.</p> <p>Slave mode: After input of eight clocks, the clock is set to low level and wait is set for master device.</p> |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | <p>Interrupt request is generated at the ninth clock's falling edge.</p> <p>Master mode: After output of nine clocks, clock output is set to low level and wait is set.</p> <p>Slave mode: After input of nine clocks, the clock is set to low level and wait is set for master device.</p>    |
| <p>An interrupt is generated at the falling edge of the ninth clock during address transfer independently of the setting of this bit. The setting of this bit is valid when the address transfer is completed. When in master mode, a wait is inserted at the falling edge of the ninth clock during address transfers. For a slave device that has received a local address, a wait is inserted at the falling edge of the ninth clock after an acknowledge (<math>\overline{ACK}</math>) is issued. However, when the slave device has received an extension code, a wait is inserted at the falling edge of the eighth clock.</p> |                                                                                                                                                                                                                                                                                                |
| Condition for clearing (WTIM0 = 0)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Condition for setting (WTIM0 = 1)                                                                                                                                                                                                                                                              |
| <ul style="list-style-type: none"> <li>• Cleared by instruction</li> <li>• Reset</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | <ul style="list-style-type: none"> <li>• Set by instruction</li> </ul>                                                                                                                                                                                                                         |

|                                                                                             |                                                                                           |
|---------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|
| ACKE0 <sup>Notes 1, 2</sup>                                                                 | Acknowledgment control                                                                    |
| 0                                                                                           | Disable acknowledgment.                                                                   |
| 1                                                                                           | Enable acknowledgment. During the ninth clock period, the SDAA0 line is set to low level. |
| Condition for clearing (ACKE0 = 0)                                                          | Condition for setting (ACKE0 = 1)                                                         |
| <ul style="list-style-type: none"> <li>• Cleared by instruction</li> <li>• Reset</li> </ul> | <ul style="list-style-type: none"> <li>• Set by instruction</li> </ul>                    |

- Notes**
1. The signal of this bit is invalid while IICE0 is 0. Set this bit during that period.
  2. The set value is invalid during address transfer and if the code is not an extension code.  
When the device serves as a slave and the addresses match, an acknowledgment is generated regardless of the set value.

Figure 13-6. Format of IICA Control Register 00 (IICCTL00) (3/4)

| STT0 <sup>Note</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Start condition trigger                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Do not generate a start condition.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | <p>When bus is released (in standby state, when IICBSY = 0):<br/>If this bit is set (1), a start condition is generated (startup as the master).</p> <p>When a third party is communicating:</p> <ul style="list-style-type: none"> <li>When communication reservation function is enabled (IICRSV = 0)<br/>Functions as the start condition reservation flag. When set to 1, automatically generates a start condition after the bus is released.</li> <li>When communication reservation function is disabled (IICRSV = 1)<br/>Even if this bit is set (1), the STT0 bit is cleared and the STT0 clear flag (STCF) is set (1). No start condition is generated.</li> </ul> <p>In the wait state (when master device):<br/>Generates a restart condition after releasing the wait.</p> |
| <p>Cautions concerning set timing</p> <ul style="list-style-type: none"> <li>For master reception: Cannot be set to 1 during transfer. Can be set to 1 only in the waiting period when the ACKEO bit has been cleared to 0 and slave has been notified of final reception.</li> <li>For master transmission: A start condition cannot be generated normally during the acknowledge period. Set to 1 during the wait period that follows output of the ninth clock.</li> <li>Cannot be set to 1 at the same time as stop condition trigger (SPT0).</li> <li>Once STT0 is set to 1, setting it again (1) before the clear condition is met is not allowed.</li> </ul> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| Condition for clearing (STT0 = 0)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Condition for setting (STT0 = 1)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <ul style="list-style-type: none"> <li>Cleared by setting the STT0 bit to 1 while communication reservation is prohibited.</li> <li>Cleared by loss in arbitration</li> <li>Cleared after start condition is generated by master device</li> <li>Cleared by LREL0 = 1 (exit from communications)</li> <li>When IICE0 = 0 (operation stop)</li> <li>Reset</li> </ul>                                                                                                                                                                                                                                                                                                 | <ul style="list-style-type: none"> <li>Set by instruction</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

**Note** The signal of this bit is invalid while IICE0 is 0.

**Remarks**

- Bit 1 (STT0) becomes 0 when it is read after data setting.
- IICRSV: Bit 0 of IIC flag register 0 (IICF0)  
STCF: Bit 7 of IIC flag register 0 (IICF0)

**Figure 13-6. Format of IICA Control Register 00 (IICCTL00) (4/4)**

| SPT0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Stop condition trigger                                                 |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------|
| 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Stop condition is not generated.                                       |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Stop condition is generated (termination of master device's transfer). |
| Cautions concerning set timing<br><ul style="list-style-type: none"> <li>For master reception: Cannot be set to 1 during transfer.<br/>Can be set to 1 only in the waiting period when the ACKE0 bit has been cleared to 0 and slave has been notified of final reception.</li> <li>For master transmission: A stop condition cannot be generated normally during the acknowledge period.<br/>Therefore, set it during the wait period that follows output of the ninth clock.</li> <li>Cannot be set to 1 at the same time as start condition trigger (STT0).</li> <li>The SPT0 bit can be set to 1 only when in master mode.</li> <li>When the WTIM0 bit has been cleared to 0, if the SPT0 bit is set to 1 during the wait period that follows output of eight clocks, note that a stop condition will be generated during the high-level period of the ninth clock. The WTIM0 bit should be changed from 0 to 1 during the wait period following the output of eight clocks, and the SPT0 bit should be set to 1 during the wait period that follows the output of the ninth clock.</li> <li>Once STT0 is set to 1, setting it again (1) before the clear condition is met is not allowed.</li> </ul> |                                                                        |
| Condition for clearing (SPT0 = 0)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Condition for setting (SPT0 = 1)                                       |
| <ul style="list-style-type: none"> <li>Cleared by loss in arbitration</li> <li>Automatically cleared after stop condition is detected</li> <li>Cleared by LREL0 = 1 (exit from communications)</li> <li>When IICE0 = 0 (operation stop)</li> <li>Reset</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | <ul style="list-style-type: none"> <li>Set by instruction</li> </ul>   |

**Caution** When bit 3 (TRC0) of the IICA status register 0 (IICS0) is set to 1 (transmission status), bit 5 (WREL0) of IICA control register 00 (IICCTL00) is set to 1 during the ninth clock and wait is canceled, after which the TRC0 bit is cleared (reception status) and the SDAA0 line is set to high impedance. Release the wait performed while the TRC0 bit is 1 (transmission status) by writing to the IICA shift register 0.

**Remark** Bit 0 (SPT0) becomes 0 when it is read after data setting.

### 13.3.3 IICA status register 0 (IICS0)

This register indicates the status of I<sup>2</sup>C.

The IICS0 register is read by a 1-bit or 8-bit memory manipulation instruction only when STT0 = 1 and during the wait period.

Reset signal generation clears this register to 00H.

**Caution** Reading the IICS0 register while the address match wakeup function is enabled (WUP0 = 1) in STOP mode is prohibited. When the WUP0 bit is changed from 1 to 0 (wakeup operation is stopped), regardless of the INTIICA0 interrupt request, the change in status is not reflected until the next start condition or stop condition is detected. To use the wakeup function, therefore, enable (SPIE0 = 1) the interrupt generated by detecting a stop condition and read the IICS0 register after the interrupt has been detected.

**Remark** STT0: bit 1 of IICA control register 00 (IICCTL00)  
WUP0: bit 7 of IICA control register 01 (IICCTL01)

**Figure 13-7. Format of IICA Status Register 0 (IICS0) (1/3)**

Address: FFF51H (IICS0)      After reset: 00H      R

| Symbol | <7>   | <6>  | <5>  | <4>  | <3>  | <2>   | <1>  | <0>  |
|--------|-------|------|------|------|------|-------|------|------|
| IICS0  | MSTS0 | ALD0 | EXC0 | COI0 | TRC0 | ACKD0 | STD0 | SPD0 |

|                                                                                                                                                                                                                                                                        |                                                     |                                                                                       |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------|---------------------------------------------------------------------------------------|
| MSTS0                                                                                                                                                                                                                                                                  | Master status check flag                            |                                                                                       |
| 0                                                                                                                                                                                                                                                                      | Slave device status or communication standby status |                                                                                       |
| 1                                                                                                                                                                                                                                                                      | Master device communication status                  |                                                                                       |
| Condition for clearing (MSTS0 = 0)                                                                                                                                                                                                                                     |                                                     | Condition for setting (MSTS0 = 1)                                                     |
| <ul style="list-style-type: none"> <li>When a stop condition is detected</li> <li>When ALD0 = 1 (arbitration loss)</li> <li>Cleared by LREL0 = 1 (exit from communications)</li> <li>When the IICE0 bit changes from 1 to 0 (operation stop)</li> <li>Reset</li> </ul> |                                                     | <ul style="list-style-type: none"> <li>When a start condition is generated</li> </ul> |

|                                                                                                                                                                                                         |                                                                                                    |                                                                                            |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|
| ALD0                                                                                                                                                                                                    | Detection of arbitration loss                                                                      |                                                                                            |
| 0                                                                                                                                                                                                       | This status means either that there was no arbitration or that the arbitration result was a "win". |                                                                                            |
| 1                                                                                                                                                                                                       | This status indicates the arbitration result was a "loss". The MSTS0 bit is cleared.               |                                                                                            |
| Condition for clearing (ALD0 = 0)                                                                                                                                                                       |                                                                                                    | Condition for setting (ALD0 = 1)                                                           |
| <ul style="list-style-type: none"> <li>Automatically cleared after the IICS0 register is read<sup>Note</sup></li> <li>When the IICE0 bit changes from 1 to 0 (operation stop)</li> <li>Reset</li> </ul> |                                                                                                    | <ul style="list-style-type: none"> <li>When the arbitration result is a "loss".</li> </ul> |

**Note** This register is also cleared when a 1-bit memory manipulation instruction is executed for bits other than the IICS0 register. Therefore, when using the ALD0 bit, read the data of this bit before the data of the other bits.

**Remark** LREL0: Bit 6 of IICA control register 00 (IICCTL00)  
IICE0: Bit 7 of IICA control register 00 (IICCTL00)

Figure 13-7. Format of IICA Status Register 0 (IICS0) (2/3)

| EXC0                                                                                                                                                                                                                                                                     | Detection of extension code reception |                                                                                                                                                                                   |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0                                                                                                                                                                                                                                                                        | Extension code was not received.      |                                                                                                                                                                                   |
| 1                                                                                                                                                                                                                                                                        | Extension code was received.          |                                                                                                                                                                                   |
| Condition for clearing (EXC0 = 0)                                                                                                                                                                                                                                        |                                       | Condition for setting (EXC0 = 1)                                                                                                                                                  |
| <ul style="list-style-type: none"> <li>When a start condition is detected</li> <li>When a stop condition is detected</li> <li>Cleared by LREL0 = 1 (exit from communications)</li> <li>When the IICE0 bit changes from 1 to 0 (operation stop)</li> <li>Reset</li> </ul> |                                       | <ul style="list-style-type: none"> <li>When the higher four bits of the received address data is either "0000" or "1111" (set at the rising edge of the eighth clock).</li> </ul> |

| COI0                                                                                                                                                                                                                                                                     | Detection of matching addresses |                                                                                                                                                                                       |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0                                                                                                                                                                                                                                                                        | Addresses do not match.         |                                                                                                                                                                                       |
| 1                                                                                                                                                                                                                                                                        | Addresses match.                |                                                                                                                                                                                       |
| Condition for clearing (COI0 = 0)                                                                                                                                                                                                                                        |                                 | Condition for setting (COI0 = 1)                                                                                                                                                      |
| <ul style="list-style-type: none"> <li>When a start condition is detected</li> <li>When a stop condition is detected</li> <li>Cleared by LREL0 = 1 (exit from communications)</li> <li>When the IICE0 bit changes from 1 to 0 (operation stop)</li> <li>Reset</li> </ul> |                                 | <ul style="list-style-type: none"> <li>When the received address matches the local address (slave address register 0 (SVA0)) (set at the rising edge of the eighth clock).</li> </ul> |

| TRC0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Detection of transmit/receive status                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Receive status (other than transmit status). The SDAA0 line is set for high impedance.                                                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Transmit status. The value in the SO0 latch is enabled for output to the SDAA0 line (valid starting at the falling edge of the first byte's ninth clock). |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| Condition for clearing (TRC0 = 0)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                                                                                           | Condition for setting (TRC0 = 1)                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <p>&lt;Both master and slave&gt;</p> <ul style="list-style-type: none"> <li>When a stop condition is detected</li> <li>Cleared by LREL0 = 1 (exit from communications)</li> <li>When the IICE0 bit changes from 1 to 0 (operation stop)</li> <li>Cleared by WREL0 = 1<sup>Note</sup> (wait cancel)</li> <li>When the ALD0 bit changes from 0 to 1 (arbitration loss)</li> <li>Reset</li> <li>When not used for communication (MSTS0, EXC0, COI0 = 0)</li> </ul> <p>&lt;Master&gt;</p> <ul style="list-style-type: none"> <li>When "1" is output to the first byte's LSB (transfer direction specification bit)</li> </ul> <p>&lt;Slave&gt;</p> <ul style="list-style-type: none"> <li>When a start condition is detected</li> <li>When "0" is input to the first byte's LSB (transfer direction specification bit)</li> </ul> |                                                                                                                                                           | <p>&lt;Master&gt;</p> <ul style="list-style-type: none"> <li>When a start condition is generated</li> <li>When 0 (master transmission) is output to the LSB (transfer direction specification bit) of the first byte (during address transfer)</li> </ul> <p>&lt;Slave&gt;</p> <ul style="list-style-type: none"> <li>When 1 (slave transmission) is input to the LSB (transfer direction specification bit) of the first byte from the master (during address transfer)</li> </ul> |

**Note** When bit 3 (TRC0) of the IICA status register 0 (IICS0) is set to 1 (transmission status), bit 5 (WREL0) of IICA control register 00 (IICCTL00) is set to 1 during the ninth clock and wait is canceled, after which the TRC0 bit is cleared (reception status) and the SDAA0 line is set to high impedance. Release the wait performed while the TRC0 bit is 1 (transmission status) by writing to the IICA shift register 0.

**Remark** LREL0: Bit 6 of IICA control register 00 (IICCTL00)  
IICE0: Bit 7 of IICA control register 00 (IICCTL00)

**Figure 13-7. Format of IICA Status Register 0 (IICS0) (3/3)**

| ACKD0                                                                                                                                                                                                                                                                                   | Detection of acknowledge ( $\overline{\text{ACK}}$ ) |                                                                                                                                           |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 0                                                                                                                                                                                                                                                                                       | Acknowledge was not detected.                        |                                                                                                                                           |
| 1                                                                                                                                                                                                                                                                                       | Acknowledge was detected.                            |                                                                                                                                           |
| Condition for clearing (ACKD0 = 0)                                                                                                                                                                                                                                                      |                                                      | Condition for setting (ACKD0 = 1)                                                                                                         |
| <ul style="list-style-type: none"> <li>When a stop condition is detected</li> <li>At the rising edge of the next byte's first clock</li> <li>Cleared by LREL0 = 1 (exit from communications)</li> <li>When the IICE0 bit changes from 1 to 0 (operation stop)</li> <li>Reset</li> </ul> |                                                      | <ul style="list-style-type: none"> <li>After the SDAA0 line is set to low level at the rising edge of SCLA0 line's ninth clock</li> </ul> |

| STD0                                                                                                                                                                                                                                                                                                               | Detection of start condition                                                                |                                                                                      |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| 0                                                                                                                                                                                                                                                                                                                  | Start condition was not detected.                                                           |                                                                                      |
| 1                                                                                                                                                                                                                                                                                                                  | Start condition was detected. This indicates that the address transfer period is in effect. |                                                                                      |
| Condition for clearing (STD0 = 0)                                                                                                                                                                                                                                                                                  |                                                                                             | Condition for setting (STD0 = 1)                                                     |
| <ul style="list-style-type: none"> <li>When a stop condition is detected</li> <li>At the rising edge of the next byte's first clock following address transfer</li> <li>Cleared by LREL0 = 1 (exit from communications)</li> <li>When the IICE0 bit changes from 1 to 0 (operation stop)</li> <li>Reset</li> </ul> |                                                                                             | <ul style="list-style-type: none"> <li>When a start condition is detected</li> </ul> |

| SPD0                                                                                                                                                                                                                                                                                                            | Detection of stop condition                                                                           |                                                                                     |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| 0                                                                                                                                                                                                                                                                                                               | Stop condition was not detected.                                                                      |                                                                                     |
| 1                                                                                                                                                                                                                                                                                                               | Stop condition was detected. The master device's communication is terminated and the bus is released. |                                                                                     |
| Condition for clearing (SPD0 = 0)                                                                                                                                                                                                                                                                               |                                                                                                       | Condition for setting (SPD0 = 1)                                                    |
| <ul style="list-style-type: none"> <li>At the rising edge of the address transfer byte's first clock following setting of this bit and detection of a start condition</li> <li>When the WUP0 bit changes from 1 to 0</li> <li>When the IICE0 bit changes from 1 to 0 (operation stop)</li> <li>Reset</li> </ul> |                                                                                                       | <ul style="list-style-type: none"> <li>When a stop condition is detected</li> </ul> |

**Remark** LREL0: Bit 6 of IICA control register 00 (IICCTL00)

IICE0: Bit 7 of IICA control register 00 (IICCTL00)

#### 13.3.4 IICA flag register 0 (IICF0)

This register sets the operation mode of I<sup>2</sup>C and indicates the status of the I<sup>2</sup>C bus.

The IICF0 register can be set by a 1-bit or 8-bit memory manipulation instruction. However, the STT0 clear flag (STCF) and I<sup>2</sup>C bus status flag (IICBSY) bits are read-only.

The IICRSV bit can be used to enable/disable the communication reservation function.

The STCEN bit can be used to set the initial value of the IICBSY bit.

The IICRSV and STCEN bits can be written only when the operation of I<sup>2</sup>C is disabled (bit 7 (IICE0) of IICA control register 00 (IICCTL00) = 0). When operation is enabled, the IICF0 register can be read.

Reset signal generation clears this register to 00H.

**Figure 13-8. Format of IICA Flag Register 0 (IICF0)**Address: FFF52H (IICF0)    After reset: 00H    R/W<sup>Note</sup>

|        |       |         |   |   |   |   |        |         |
|--------|-------|---------|---|---|---|---|--------|---------|
| Symbol | <7>   | <6>     | 5 | 4 | 3 | 2 | <1>    | <0>     |
| IICF0  | STCF0 | IICBSY0 | 0 | 0 | 0 | 0 | STCEN0 | IICRSV0 |

|                                                                                                                                                                                   |                                                              |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|
| STCF0                                                                                                                                                                             | STT0 clear flag                                              |
| 0                                                                                                                                                                                 | Generate start condition                                     |
| 1                                                                                                                                                                                 | Start condition generation unsuccessful: clear the STT0 flag |
| Condition for clearing (STCF0 = 0)                                                                                                                                                |                                                              |
| <ul style="list-style-type: none"> <li>Cleared by STT0 = 1</li> <li>When IICE0 = 0 (operation stop)</li> <li>Reset</li> </ul>                                                     |                                                              |
| Condition for setting (STCF0 = 1)                                                                                                                                                 |                                                              |
| <ul style="list-style-type: none"> <li>Generating start condition unsuccessful and the STT0 bit cleared to 0 when communication reservation is disabled (IICRSV0 = 1).</li> </ul> |                                                              |

|                                                                                                                                       |                                                                         |
|---------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------|
| IICBSY0                                                                                                                               | I <sup>2</sup> C bus status flag                                        |
| 0                                                                                                                                     | Bus release status (communication initial status when STCEN0 = 1)       |
| 1                                                                                                                                     | Bus communication status (communication initial status when STCEN0 = 0) |
| Condition for clearing (IICBSY0 = 0)                                                                                                  |                                                                         |
| <ul style="list-style-type: none"> <li>Detection of stop condition</li> <li>When IICE0 = 0 (operation stop)</li> <li>Reset</li> </ul> |                                                                         |
| Condition for setting (IICBSY0 = 1)                                                                                                   |                                                                         |
| <ul style="list-style-type: none"> <li>Detection of start condition</li> <li>Setting of the IICE0 bit when STCEN0 = 0</li> </ul>      |                                                                         |

|                                                                                                                               |                                                                                                                    |
|-------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|
| STCEN0                                                                                                                        | Initial start enable trigger                                                                                       |
| 0                                                                                                                             | After operation is enabled (IICE0 = 1), enable generation of a start condition upon detection of a stop condition. |
| 1                                                                                                                             | After operation is enabled (IICE0 = 1), enable generation of a start condition without detecting a stop condition. |
| Condition for clearing (STCEN0 = 0)                                                                                           |                                                                                                                    |
| <ul style="list-style-type: none"> <li>Cleared by instruction</li> <li>Detection of start condition</li> <li>Reset</li> </ul> |                                                                                                                    |
| Condition for setting (STCEN0 = 1)                                                                                            |                                                                                                                    |
| <ul style="list-style-type: none"> <li>Set by instruction</li> </ul>                                                          |                                                                                                                    |

|                                                                                         |                                                |
|-----------------------------------------------------------------------------------------|------------------------------------------------|
| IICRSV0                                                                                 | Communication reservation function disable bit |
| 0                                                                                       | Enable communication reservation               |
| 1                                                                                       | Disable communication reservation              |
| Condition for clearing (IICRSV0 = 0)                                                    |                                                |
| <ul style="list-style-type: none"> <li>Cleared by instruction</li> <li>Reset</li> </ul> |                                                |
| Condition for setting (IICRSV0 = 1)                                                     |                                                |
| <ul style="list-style-type: none"> <li>Set by instruction</li> </ul>                    |                                                |

**Note** Bits 6 and 7 are read-only.

- Cautions**
1. Write to the STCEN bit only when the operation is stopped (IICE0 = 0).
  2. As the bus release status (IICBSY = 0) is recognized regardless of the actual bus status when STCEN = 1, when generating the first start condition (STT0 = 1), it is necessary to verify that no third party communications are in progress in order to prevent such communications from being destroyed.
  3. Write to IICRSV only when the operation is stopped (IICE0 = 0).

**Remark** STT0: Bit 1 of IICA control register 00 (IICCTL00)  
 IICE0: Bit 7 of IICA control register 00 (IICCTL00)

### 13.3.5 IICA control register 01 (IICCTL01)

This register is used to set the operation mode of I<sup>2</sup>C and detect the statuses of the SCLA0 and SDAA0 pins.

The IICCTL01 register can be set by a 1-bit or 8-bit memory manipulation instruction. However, the CLD0 and DAD0 bits are read-only.

Set the IICCTL01 register, except the WUP0 bit, while operation of I<sup>2</sup>C is disabled (bit 7 (IICE0) of IICA control register 00 (IICCTL00) is 0).

Reset signal generation clears this register to 00H.

**Figure 13-9. Format of IICA Control Register 01 (IICCTL01) (1/2)**

Address: F0231H (IICCTL01) After reset: 00H R/W<sup>Note 1</sup>

|          |      |   |      |      |      |      |   |      |
|----------|------|---|------|------|------|------|---|------|
| Symbol   | 7    | 6 | <5>  | <4>  | <3>  | <2>  | 1 | <0>  |
| IICCTL01 | WUP0 | 0 | CLD0 | DAD0 | SMC0 | DFC0 | 0 | PRS0 |

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                                                                                                                                                                                           |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| WUP0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Control of address match wakeup                                                                                                                                                           |
| 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Stops operation of address match wakeup function in STOP mode.                                                                                                                            |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Enables operation of address match wakeup function in STOP mode.                                                                                                                          |
| <p>To shift to STOP mode when WUP0 = 1, execute the STOP instruction at least three clocks after setting (1) the WUP0 bit (see <b>Figure 13-22 Flow When Setting WUP0 = 1</b>).</p> <p>Clear (0) the WUP0 bit after the address has matched or an extension code has been received. The subsequent communication can be entered by the clearing (0) WUP0 bit. (The wait must be released and transmit data must be written after the WUP0 bit has been cleared (0).)</p> <p>The interrupt timing when the address has matched or when an extension code has been received, while WUP0 = 1, is identical to the interrupt timing when WUP0 = 0. (A delay of the difference of sampling by the clock will occur.) Furthermore, when WUP0 = 1, a stop condition interrupt is not generated even if the SPIE0 bit is set to 1.</p> <p>When WUP0 = 0 is set by a source other than an interrupt from serial interface IICA, operation as the master device cannot be performed until the subsequent start condition or stop condition is detected. Do not output a start condition by setting (1) the STT0 bit, without waiting for the detection of the subsequent start condition or stop condition.</p> |                                                                                                                                                                                           |
| Condition for clearing (WUP0 = 0)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Condition for setting (WUP0 = 1)                                                                                                                                                          |
| <ul style="list-style-type: none"> <li>Cleared by instruction (after address match or extension code reception)</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | <ul style="list-style-type: none"> <li>Set by instruction (when the MST0, EXC0, and COI0 bits are "0", and the STD0 bit also "0" (communication not entered))<sup>Note 2</sup></li> </ul> |

**Notes 1.** Bits 4 and 5 are read-only.

- The status of the IICA status register 0 (IICS0) must be checked and the WUP0 bit must be set during the period shown below.

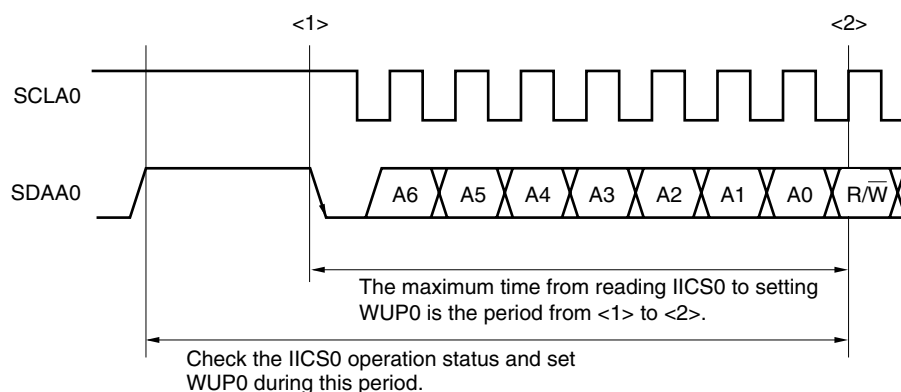




**Figure 13-9. Format of IICA Control Register 01 (IICCTL01) (2/2)**

|                                                                                                                                              |                                                          |                                                                                       |
|----------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|---------------------------------------------------------------------------------------|
| CLD0                                                                                                                                         | Detection of SCLA0 pin level (valid only when IICE0 = 1) |                                                                                       |
| 0                                                                                                                                            | The SCLA0 pin was detected at low level.                 |                                                                                       |
| 1                                                                                                                                            | The SCLA0 pin was detected at high level.                |                                                                                       |
| Condition for clearing (CLD0 = 0)                                                                                                            |                                                          | Condition for setting (CLD0 = 1)                                                      |
| <ul style="list-style-type: none"> <li>When the SCLA0 pin is at low level</li> <li>When IICE0 = 0 (operation stop)</li> <li>Reset</li> </ul> |                                                          | <ul style="list-style-type: none"> <li>When the SCLA0 pin is at high level</li> </ul> |

|                                                                                                                                              |                                                          |                                                                                       |
|----------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|---------------------------------------------------------------------------------------|
| DAD0                                                                                                                                         | Detection of SDAA0 pin level (valid only when IICE0 = 1) |                                                                                       |
| 0                                                                                                                                            | The SDAA0 pin was detected at low level.                 |                                                                                       |
| 1                                                                                                                                            | The SDAA0 pin was detected at high level.                |                                                                                       |
| Condition for clearing (DAD0 = 0)                                                                                                            |                                                          | Condition for setting (DAD0 = 1)                                                      |
| <ul style="list-style-type: none"> <li>When the SDAA0 pin is at low level</li> <li>When IICE0 = 0 (operation stop)</li> <li>Reset</li> </ul> |                                                          | <ul style="list-style-type: none"> <li>When the SDAA0 pin is at high level</li> </ul> |

|      |                                                                                                            |  |
|------|------------------------------------------------------------------------------------------------------------|--|
| SMC0 | Operation mode switching                                                                                   |  |
| 0    | Operates in standard mode (fastest transfer rate: 100 kbps).                                               |  |
| 1    | Operates in fast mode (fastest transfer rate: 400 kbps) or fast mode plus (fastest transfer rate: 1 Mbps). |  |

|      |                                  |
|------|----------------------------------|
| DFC0 | Digital filter operation control |
| 0    | Digital filter off.              |
| 1    | Digital filter on.               |

Digital filter can be used only in fast mode and fast mode plus.

In fast mode and fast mode plus, the transfer clock does not vary, regardless of the DFCn bit being set (1) or cleared (0).

The digital filter is used for noise elimination in fast mode and fast mode plus.

|      |                                         |  |
|------|-----------------------------------------|--|
| PRS0 | Division of the operation clock         |  |
| 0    | Selects $f_{CLK}$ as operation clock.   |  |
| 1    | Selects $f_{CLK}/2$ as operation clock. |  |

**Caution** The fastest operation frequency of the operation clock of the serial interface IICA is 20 MHz (Max.). If the  $f_{CLK}$  exceeds 20 MHz, set the clock to  $f_{CLK}/2$  by setting the PRS0 bit to 1.

**Remark** IICE0: Bit 7 of IICA control register 00 (IICCTL00)

&lt;R&gt;

### 13.3.6 IICA low-level width setting register 0 (IICWL0)

This register is used to set the low-level width ( $t_{LOW}$ ) and data hold time ( $t_{HD:DAT}$ ) of the SCLA0 pin signal that is output by serial interface IICA. The data hold time is decided by value the higher 6 bits of IICWL register.

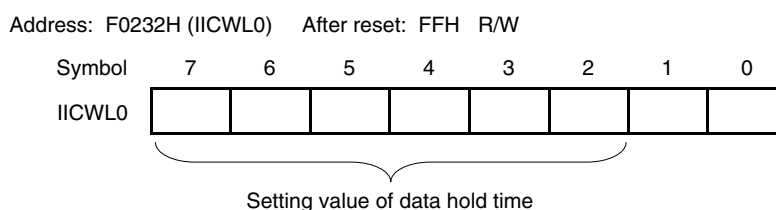
The IICWL0 register can be set by an 8-bit memory manipulation instruction.

Set the IICWL0 register while operation of I<sup>2</sup>C is disabled (bit 7 (IICE0) of IICA control register 00 (IICCTL00) is 0).

Reset signal generation sets this register to FFH.

For details about setting The IICWL0 register, see **13.4.2 Setting transfer clock by using IICWL0 and IICWH0 registers.**

**Figure 13-10. Format of IICA Low-Level Width Setting Register 0 (IICWL0)**



### 13.3.7 IICA high-level width setting register 0 (IICWH0)

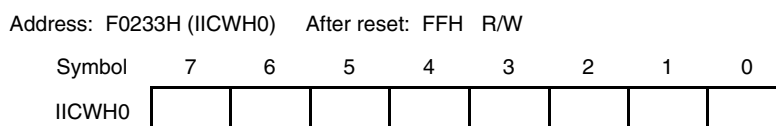
This register is used to set the high-level width of the SCLA0 pin signal that is output by serial interface IICA.

The IICWH0 register can be set by an 8-bit memory manipulation instruction.

Set the IICWH0 register while operation of I<sup>2</sup>C is disabled (bit 7 (IICE0) of IICA control register 00 (IICCTL00) is 0).

Reset signal generation sets this register to FFH.

**Figure 13-11. Format of IICA High-Level Width Setting Register 0 (IICWH0)**



**Remark** For how to set the transfer clock by using the IICWL0 and IICWH0 registers, see **13.4.2 Setting transfer clock by using IICWL0 and IICWH0 registers.**

### 13.3.8 Port mode register 6 (PM6)

This register sets the input/output of port 6 in 1-bit units.

When using the P60/SCLA0/SEG21 pin as clock I/O and the P61/SDAA0/SEG20 pin as serial data I/O, clear PM60 and PM61, and the output latches of P60 and P61 to 0.

Set the IICE0 bit (bit 7 of IICA control register 00 (IICCTL00)) to 1 before setting the output mode because the P60/SCLA0/SEG21 and P61/SDAA0/SEG20 pins output a low level (fixed) when the IICE0 bit is 0.

The PM6 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

**Figure 13-12. Format of Port Mode Register 6 (PM6)**

Address: FFF26H    After reset: FFH    R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0    |
|--------|---|---|---|---|---|---|------|------|
| PM6    | 1 | 1 | 1 | 1 | 1 | 1 | PM61 | PM60 |

| PM6n | P6n pin I/O mode selection (n = 0, 1) |
|------|---------------------------------------|
| 0    | Output mode (output buffer on)        |
| 1    | Input mode (output buffer off)        |

## 13.4 I<sup>2</sup>C Bus Mode Functions

### 13.4.1 Pin configuration

The serial clock pin (SCLA0) and the serial data bus pin (SDAA0) are configured as follows.

- (1) SCLA0 .... This pin is used for serial clock input and output.

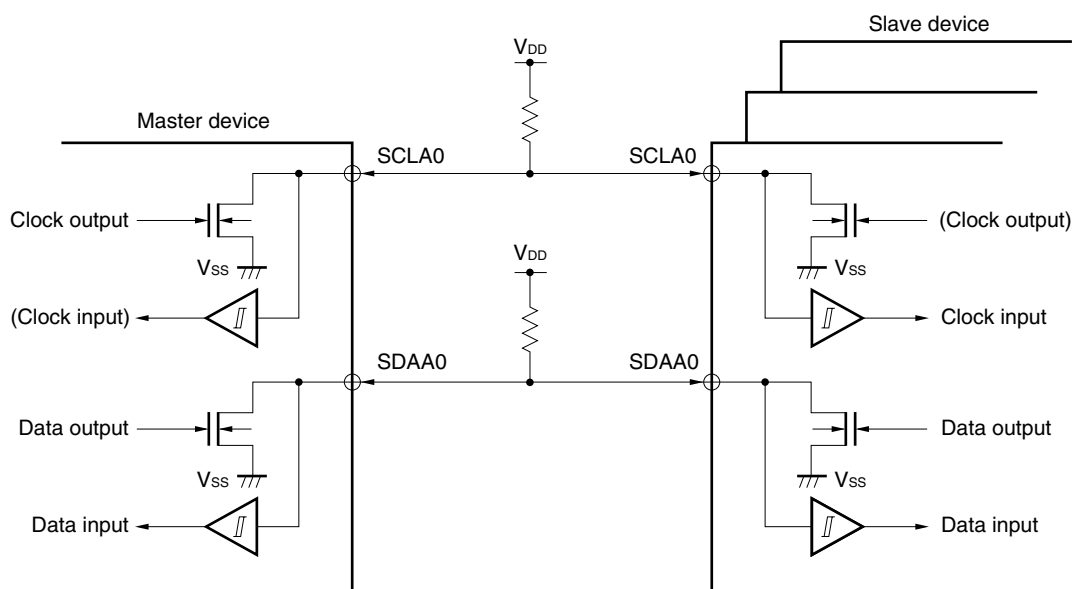
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.

- (2) SDAA0 .... This pin is used for serial data input and output.

This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.

Since outputs from the serial clock line and the serial data bus line are N-ch open-drain outputs, an external pull-up resistor is required.

**Figure 13-13. Pin Configuration Diagram**



### 13.4.2 Setting transfer clock by using IICWL0 and IICWH0 registers

#### (1) Setting transfer clock on master side

$$\text{Transfer clock} = \frac{f_{\text{CLK}}}{\text{IICWL0} + \text{IICWH0} + f_{\text{CLK}}(t_{\text{R}} + t_{\text{F}})}$$

At this time, the optimal setting values of the IICWL0 and IICWH0 registers are as follows.

(The fractional parts of all setting values are rounded up.)

- When the fast mode

$$\begin{aligned}\text{IICWL0} &= \frac{0.52}{\text{Transfer clock}} \times f_{\text{CLK}} \\ \text{IICWH0} &= \left( \frac{0.48}{\text{Transfer clock}} - t_{\text{R}} - t_{\text{F}} \right) \times f_{\text{CLK}}\end{aligned}$$

- When the normal mode

$$\begin{aligned}\text{IICWL0} &= \frac{0.47}{\text{Transfer clock}} \times f_{\text{CLK}} \\ \text{IICWH0} &= \left( \frac{0.53}{\text{Transfer clock}} - t_{\text{R}} - t_{\text{F}} \right) \times f_{\text{CLK}}\end{aligned}$$

- When the fast mode plus

$$\begin{aligned}\text{IICWL0} &= \frac{0.50}{\text{Transfer clock}} \times f_{\text{CLK}} \\ \text{IICWH0} &= \left( \frac{0.50}{\text{Transfer clock}} - t_{\text{R}} - t_{\text{F}} \right) \times f_{\text{CLK}}\end{aligned}$$

#### (2) Setting IICWL0 and IICWH0 registers on slave side

(The fractional parts of all setting values are truncated.)

- When the fast mode

$$\begin{aligned}\text{IICWL0} &= 1.3 \mu\text{s} \times f_{\text{CLK}} \\ \text{IICWH0} &= (1.2 \mu\text{s} - t_{\text{R}} - t_{\text{F}}) \times f_{\text{CLK}}\end{aligned}$$

- When the normal mode

$$\begin{aligned}\text{IICWL0} &= 4.7 \mu\text{s} \times f_{\text{CLK}} \\ \text{IICWH0} &= (5.3 \mu\text{s} - t_{\text{R}} - t_{\text{F}}) \times f_{\text{CLK}}\end{aligned}$$

- When the fast mode plus

$$\begin{aligned}\text{IICWL0} &= 0.50 \mu\text{s} \times f_{\text{CLK}} \\ \text{IICWH0} &= (0.50 \mu\text{s} - t_{\text{R}} - t_{\text{F}}) \times f_{\text{CLK}}\end{aligned}$$

(**Caution** and **Remarks** are listed on the next page.)

**Caution** Note the minimum  $f_{CLK}$  operation frequency when setting the transfer clock. The minimum  $f_{CLK}$  operation frequency for serial interface IICA is determined according to the mode.

Fast mode:  $f_{CLK} = 3.5 \text{ MHz (MIN.)}$

Fast mode plus:  $f_{CLK} = 10 \text{ MHz (MIN.)}$

Normal mode:  $f_{CLK} = 1 \text{ MHz (MIN.)}$

In addition, the fastest operation frequency of the operation clock of the serial interface IICA is 20 MHz (Max.). If the  $f_{CLK}$  exceeds 20 MHz, set the clock to  $f_{CLK}/2$  by setting the PRS0 bit of IICCTL01 register to 1.

**Remarks 1.** Calculate the rise time ( $t_R$ ) and fall time ( $t_F$ ) of the SDAA0 and SCLA0 signals separately, because they differ depending on the pull-up resistance and wire load.

**2.** IICWL0: IICA low-level width setting register 0

IICWH0: IICA high-level width setting register 0

$t_F$ : SDAA0 and SCLA0 signal falling times

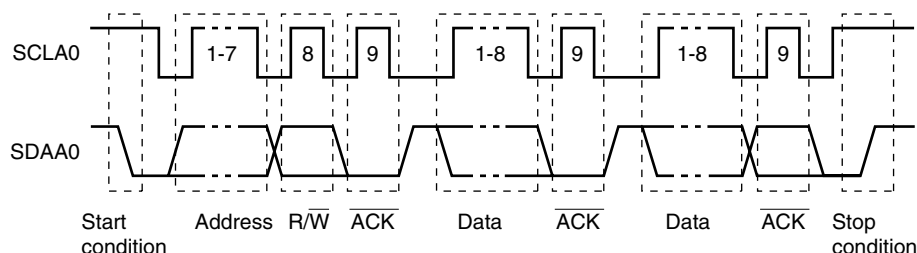
$t_R$ : SDAA0 and SCLA0 signal rising times

$f_{CLK}$ : CPU/peripheral hardware clock frequency

### 13.5 I<sup>2</sup>C Bus Definitions and Control Methods

The following section describes the I<sup>2</sup>C bus's serial data communication format and the signals used by the I<sup>2</sup>C bus. Figure 13-14 shows the transfer timing for the "start condition", "address", "data", and "stop condition" output via the I<sup>2</sup>C bus's serial data bus.

**Figure 13-14. I<sup>2</sup>C Bus Serial Data Transfer Timing**



The master device generates the start condition, slave address, and stop condition.

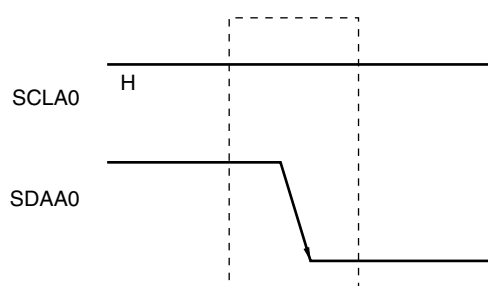
The acknowledge ( $\overline{\text{ACK}}$ ) can be generated by either the master or slave device (normally, it is output by the device that receives 8-bit data).

The serial clock (SCLA0) is continuously output by the master device. However, in the slave device, the SCLA0 pin low level period can be extended and a wait can be inserted.

#### 13.5.1 Start conditions

A start condition is met when the SCLA0 pin is at high level and the SDAA0 pin changes from high level to low level. The start conditions for the SCLA0 pin and SDAA0 pin are signals that the master device generates to the slave device when starting a serial transfer. When the device is used as a slave, start conditions can be detected.

**Figure 13-15. Start Conditions**



A start condition is output when bit 1 (STT0) of IICA control register 00 (IICCTL00) is set (1) after a stop condition has been detected (SPD0: Bit 0 of the IICA status register 0 (IICCS0) = 1). When a start condition is detected, bit 1 (STD0) of the IICCS0 register is set (1).

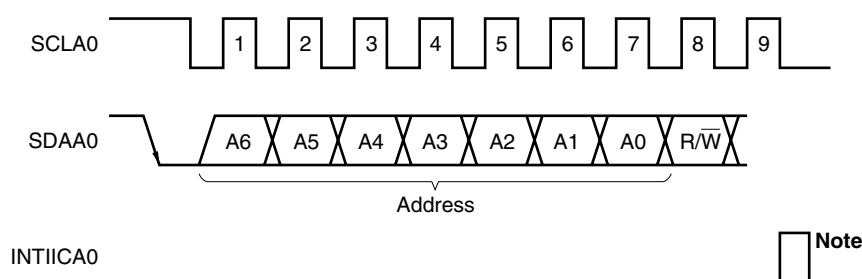
### 13.5.2 Addresses

The address is defined by the 7 bits of data that follow the start condition.

An address is a 7-bit data segment that is output in order to select one of the slave devices that are connected to the master device via the bus lines. Therefore, each slave device connected via the bus lines must have a unique address.

The slave devices include hardware that detects the start condition and checks whether or not the 7-bit address data matches the data values stored in the slave address register 0 (SVA0). If the address data matches the SVA0 register values, the slave device is selected and communicates with the master device until the master device generates a start condition or stop condition.

**Figure 13-16. Address**



**Note** INTIICA0 is not issued if data other than a local address or extension code is received during slave device operation.

Addresses are output when a total of 8 bits consisting of the slave address and the transfer direction described in **13.5.3 Transfer direction specification** are written to the IICA shift register 0 (IICA0). The received addresses are written to the IICA0 register.

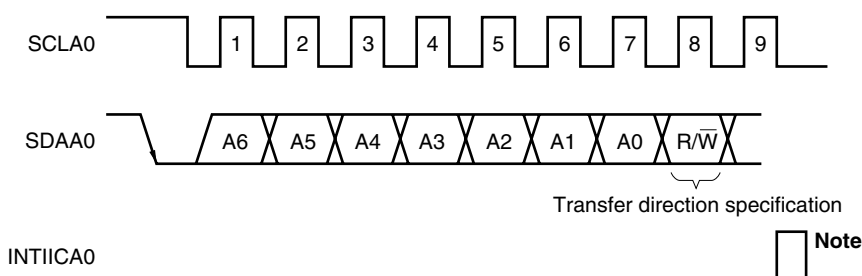
The slave address is assigned to the higher 7 bits of the IICA0 register.

### 13.5.3 Transfer direction specification

In addition to the 7-bit address data, the master device sends 1 bit that specifies the transfer direction.

When this transfer direction specification bit has a value of "0", it indicates that the master device is transmitting data to a slave device. When the transfer direction specification bit has a value of "1", it indicates that the master device is receiving data from a slave device.

**Figure 13-17. Transfer Direction Specification**



**Note** INTIICA0 is not issued if data other than a local address or extension code is received during slave device operation.



### 13.5.4 Acknowledge ( $\overline{\text{ACK}}$ )

$\overline{\text{ACK}}$  is used to check the status of serial data at the transmission and reception sides.

The reception side returns  $\overline{\text{ACK}}$  each time it has received 8-bit data.

The transmission side usually receives  $\overline{\text{ACK}}$  after transmitting 8-bit data. When  $\overline{\text{ACK}}$  is returned from the reception side, it is assumed that reception has been correctly performed and processing is continued. Whether  $\overline{\text{ACK}}$  has been detected can be checked by using bit 2 (ACKD0) of the IICA status register 0 (IICS0).

When the master receives the last data item, it does not return  $\overline{\text{ACK}}$  and instead generates a stop condition. If a slave does not return  $\overline{\text{ACK}}$  after receiving data, the master outputs a stop condition or restart condition and stops transmission. If  $\overline{\text{ACK}}$  is not returned, the possible causes are as follows.

- <1> Reception was not performed normally.
- <2> The final data item was received.
- <3> The reception side specified by the address does not exist.

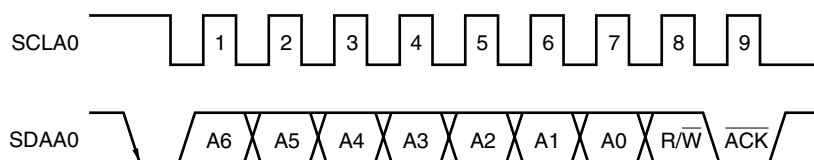
To generate  $\overline{\text{ACK}}$ , the reception side makes the SDAA0 line low at the ninth clock (indicating normal reception).

Automatic generation of  $\overline{\text{ACK}}$  is enabled by setting bit 2 (ACKE0) of IICA control register 00 (IICCTL00) to 1. Bit 3 (TRC0) of the IICS0 register is set by the data of the eighth bit that follows 7-bit address information. Usually, set the ACKE0 bit to 1 for reception (TRC0 = 0).

If a slave can receive no more data during reception (TRC0 = 0) or does not require the next data item, then the slave must inform the master, by clearing the ACKE0 bit to 0, that it will not receive any more data.

When the master does not require the next data item during reception (TRC0 = 0), it must clear the ACKE0 bit to 0 so that  $\overline{\text{ACK}}$  is not generated. In this way, the master informs a slave at the transmission side that it does not require any more data (transmission will be stopped).

Figure 13-18.  $\overline{\text{ACK}}$



When the local address is received,  $\overline{\text{ACK}}$  is automatically generated, regardless of the value of the ACKE0 bit. When an address other than that of the local address is received,  $\overline{\text{ACK}}$  is not generated (NACK).

When an extension code is received,  $\overline{\text{ACK}}$  is generated if the ACKE0 bit is set to 1 in advance.

How  $\overline{\text{ACK}}$  is generated when data is received differs as follows depending on the setting of the wait timing.

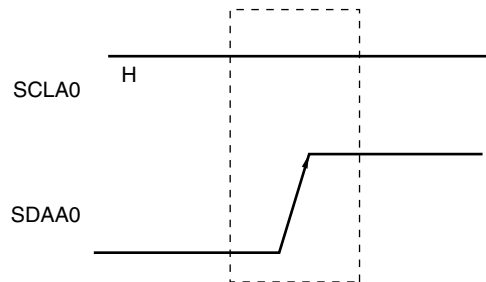
- When 8-clock wait state is selected (bit 3 (WTIM0) of IICCTL00 register = 0):  
By setting the ACKE0 bit to 1 before releasing the wait state,  $\overline{\text{ACK}}$  is generated at the falling edge of the eighth clock of the SCL A0 pin.
- When 9-clock wait state is selected (bit 3 (WTIM0) of IICCTL00 register = 1):  
 $\overline{\text{ACK}}$  is generated by setting the ACKE0 bit to 1 in advance.

### 13.5.5 Stop condition

When the SCLA0 pin is at high level, changing the SDAA0 pin from low level to high level generates a stop condition.

A stop condition is a signal that the master device generates to the slave device when serial transfer has been completed. When the device is used as a slave, stop conditions can be detected.

**Figure 13-19. Stop Condition**



A stop condition is generated when bit 0 (SPT0) of IICA control register 00 (IICCTL00) is set to 1. When the stop condition is detected, bit 0 (SPD0) of the IICA status register 0 (IICS0) is set to 1 and INTIICA0 is generated when bit 4 (SPIE0) of the IICCTL00 register is set to 1.

### 13.5.6 Wait

The wait is used to notify the communication partner that a device (master or slave) is preparing to transmit or receive data (i.e., is in a wait state).

Setting the SCLA0 pin to low level notifies the communication partner of the wait state. When wait state has been canceled for both the master and slave devices, the next data transfer can begin.

**Figure 13-20. Wait (1/2)**

- (1) When master device has a nine-clock wait and slave device has an eight-clock wait  
(master transmits, slave receives, and ACKE0 = 1)**

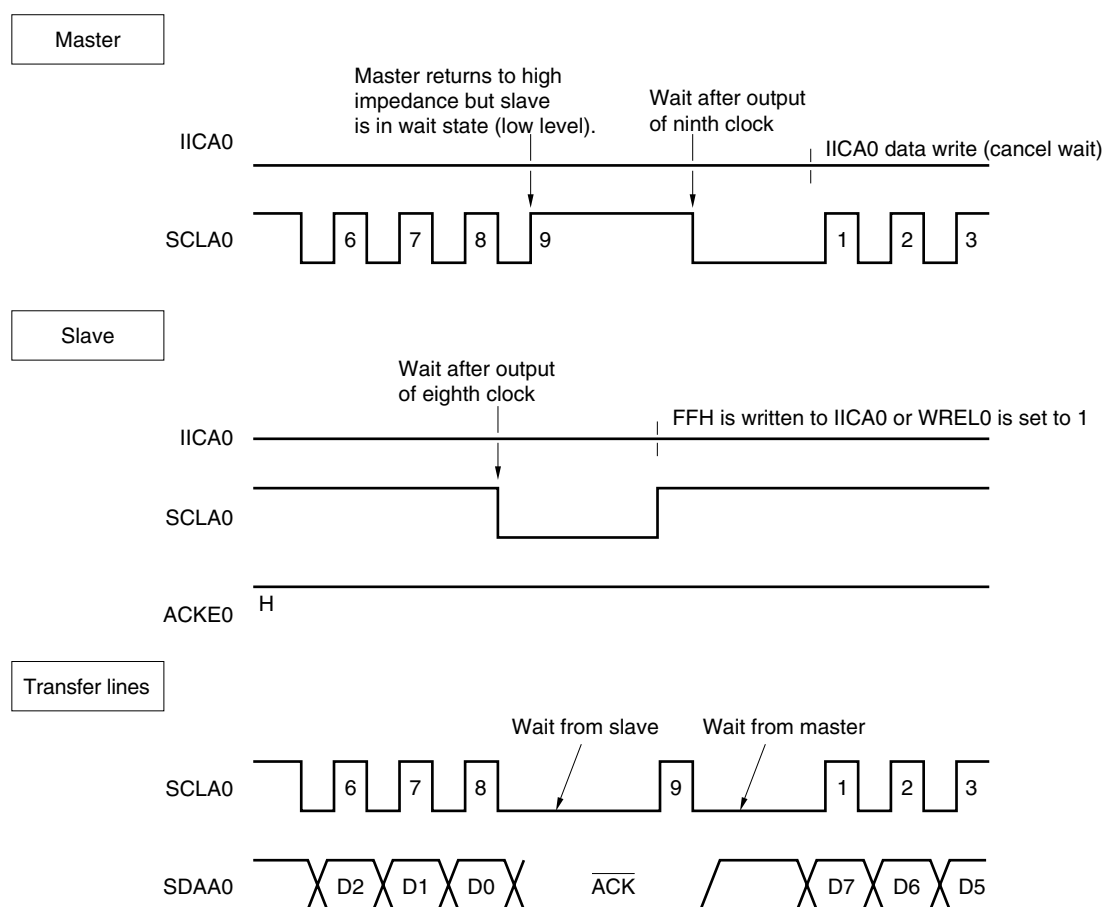
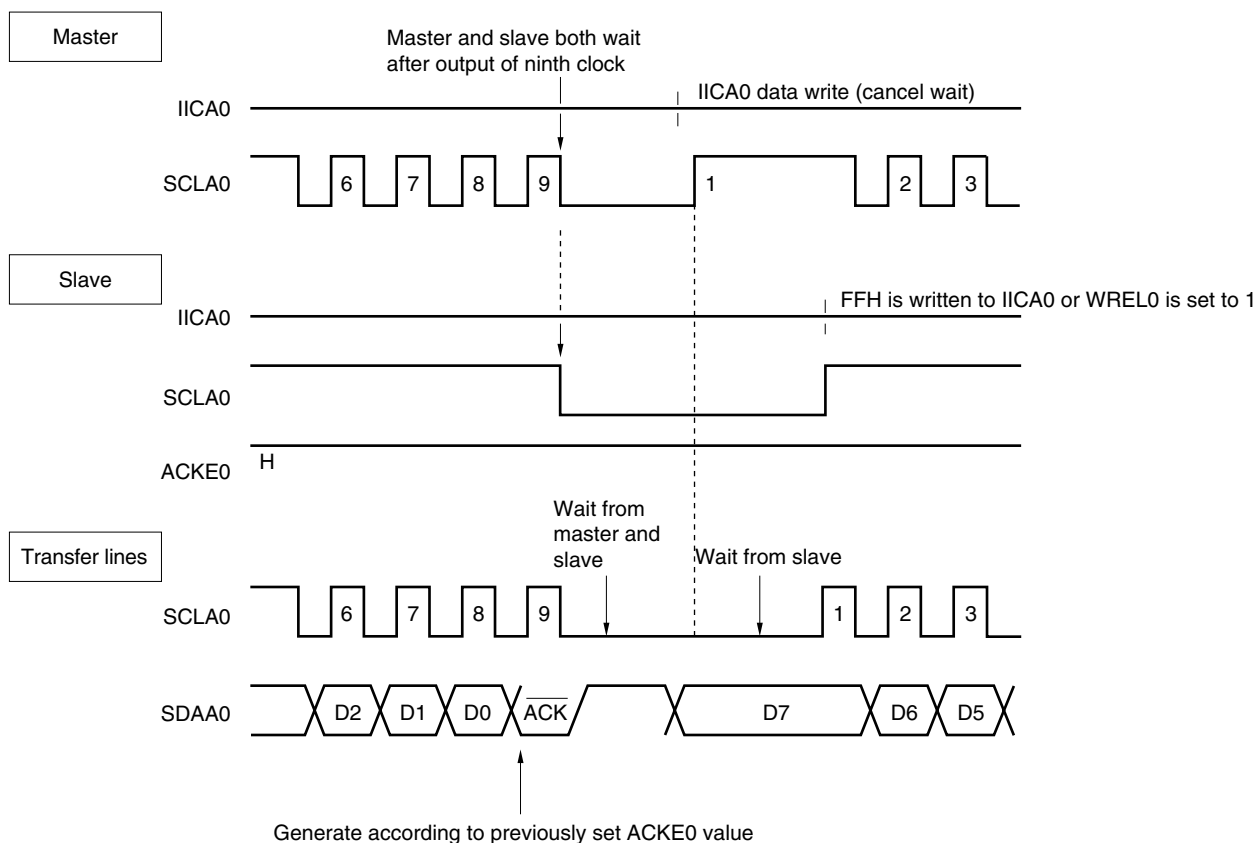


Figure 13-20. Wait (2/2)

**(2) When master and slave devices both have a nine-clock wait  
(master transmits, slave receives, and ACKE0 = 1)**



**Remark** ACKE0: Bit 2 of IICA control register 00 (IICCTL00)

WRELO: Bit 5 of IICA control register 00 (IICCTL00)

A wait may be automatically generated depending on the setting of bit 3 (WTIM0) of IICA control register 00 (IICCTL00).

Normally, the receiving side cancels the wait state when bit 5 (WRELO) of the IICCTL00 register is set to 1 or when FFH is written to the IICA shift register 0 (IICA0), and the transmitting side cancels the wait state when data is written to the IICA0 register.

The master device can also cancel the wait state via either of the following methods.

- By setting bit 1 (STT0) of the IICCTL00 register to 1
- By setting bit 0 (SPT0) of the IICCTL00 register to 1

### 13.5.7 Canceling wait

The I<sup>2</sup>C usually cancels a wait state by the following processing.

- Writing data to the IICA shift register 0 (IICA0)
- Setting bit 5 (WRELO) of IICA control register 00 (IICCTL00) (canceling wait)
- Setting bit 1 (STT0) of the IICCTL00 register (generating start condition)<sup>Note</sup>
- Setting bit 0 (SPT0) of the IICCTL00 register (generating stop condition)<sup>Note</sup>

**Note** Master only

When the above wait canceling processing is executed, the I<sup>2</sup>C cancels the wait state and communication is resumed.

To cancel a wait state and transmit data (including addresses), write the data to the IICA0 register.

To receive data after canceling a wait state, or to complete data transmission, set bit 5 (WRELO) of the IICCTL00 register to 1.

To generate a restart condition after canceling a wait state, set bit 1 (STT0) of the IICCTL00 register to 1.

To generate a stop condition after canceling a wait state, set bit 0 (SPT0) of the IICCTL00 register to 1.

Execute the canceling processing only once for one wait state.

If, for example, data is written to the IICA0 register after canceling a wait state by setting the WRELO bit to 1, an incorrect value may be output to SDAA0 line because the timing for changing the SDAA0 line conflicts with the timing for writing the IICA0 register.

In addition to the above, communication is stopped if the IICE0 bit is cleared to 0 when communication has been aborted, so that the wait state can be canceled.

If the I<sup>2</sup>C bus has deadlocked due to noise, processing is saved from communication by setting bit 6 (LRELO) of the IICCTL00 register, so that the wait state can be canceled.

**Caution** If a processing to cancel a wait state is executed when WUP0 = 1, the wait state will not be canceled.

### 13.5.8 Interrupt request (INTIICA0) generation timing and wait control

The setting of bit 3 (WTIM0) of IICA control register 00 (IICCTL00) determines the timing by which INTIICA0 is generated and the corresponding wait control, as shown in Table 13-2.

**Table 13-2. INTIICA0 Generation Timing and Wait Control**

| WTIM0 | During Slave Device Operation |                     |                     | During Master Device Operation |                |                   |
|-------|-------------------------------|---------------------|---------------------|--------------------------------|----------------|-------------------|
|       | Address                       | Data Reception      | Data Transmission   | Address                        | Data Reception | Data Transmission |
| 0     | 9 <sup>Notes 1, 2</sup>       | 8 <sup>Note 2</sup> | 8 <sup>Note 2</sup> | 9                              | 8              | 8                 |
| 1     | 9 <sup>Notes 1, 2</sup>       | 9 <sup>Note 2</sup> | 9 <sup>Note 2</sup> | 9                              | 9              | 9                 |

**Notes 1.** The slave device's INTIICA0 signal and wait period occurs at the falling edge of the ninth clock only when there is a match with the address set to the slave address register 0 (SVA0).

At this point,  $\overline{ACK}$  is generated regardless of the value set to the IICCTL00 register's bit 2 (ACKE0). For a slave device that has received an extension code, INTIICA0 occurs at the falling edge of the eighth clock.

However, if the address does not match after restart, INTIICA0 is generated at the falling edge of the 9th clock, but wait does not occur.

- 2.** If the received address does not match the contents of the slave address register 0 (SVA0) and extension code is not received, neither INTIICA0 nor a wait occurs.

**Remark** The numbers in the table indicate the number of the serial clock's clock signals. Interrupt requests and wait control are both synchronized with the falling edge of these clock signals.

#### (1) During address transmission/reception

- Slave device operation: Interrupt and wait timing are determined depending on the conditions described in Notes 1 and 2 above, regardless of the WTIM0 bit.
- Master device operation: Interrupt and wait timing occur at the falling edge of the ninth clock regardless of the WTIM0 bit.

#### (2) During data reception

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIM0 bit.

#### (3) During data transmission

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIM0 bit.

#### (4) Wait cancellation method

The four wait cancellation methods are as follows.

- Writing data to the IICA shift register 0 (IICA0)
- Setting bit 5 (WRELO) of IICA control register 00 (IICCTL00) (canceling wait)
- Setting bit 1 (STT0) of IICCTL00 register (generating start condition)<sup>Note</sup>
- Setting bit 0 (SPT0) of IICCTL00 register (generating stop condition)<sup>Note</sup>

**Note** Master only.

When an 8-clock wait has been selected (WTIM0 = 0), the presence/absence of  $\overline{ACK}$  generation must be determined prior to wait cancellation.

#### (5) Stop condition detection

INTIICA0 is generated when a stop condition is detected (only when SPIE0 = 1).

### 13.5.9 Address match detection method

In I<sup>2</sup>C bus mode, the master device can select a particular slave device by transmitting the corresponding slave address.

Address match can be detected automatically by hardware. An interrupt request (INTIICA0) occurs when the address set to the slave address register 0 (SVA0) matches the slave address sent by the master device, or when an extension code has been received.

### 13.5.10 Error detection

In I<sup>2</sup>C bus mode, the status of the serial data bus (SDAA0) during data transmission is captured by the IICA shift register 0 (IICA0) of the transmitting device, so the IICA data prior to transmission can be compared with the transmitted IICA data to enable detection of transmission errors. A transmission error is judged as having occurred when the compared data values do not match.

### 13.5.11 Extension code

- (1) When the higher 4 bits of the receive address are either "0000" or "1111", the extension code reception flag (EXC0) is set to 1 for extension code reception and an interrupt request (INTIICA0) is issued at the falling edge of the eighth clock. The local address stored in the slave address register 0 (SVA0) is not affected.
- (2) The settings below are specified if 11110xx0 is transferred from the master by using a 10-bit address transfer when the SVA0 register is set to 11110xx0. Note that INTIICA0 occurs at the falling edge of the eighth clock.
  - Higher four bits of data match: EXC0 = 1
  - Seven bits of data match: COI0 = 1

**Remark** EXC0: Bit 5 of IICA status register 0 (IICS0)

COI0: Bit 4 of IICA status register 0 (IICS0)

- (3) Since the processing after the interrupt request occurs differs according to the data that follows the extension code, such processing is performed by software.

If the extension code is received while a slave device is operating, then the slave device is participating in communication even if its address does not match.

For example, after the extension code is received, if you do not wish to operate the target device as a slave device, set bit 6 (LREL0) of IICA control register 00 (IICCTL00) to 1 to set the standby mode for the next communication operation.

**Table 13-3. Bit Definitions of Major Extension Codes**

| Slave Address | R/W Bit | Description                                                                           |
|---------------|---------|---------------------------------------------------------------------------------------|
| 0 0 0 0 0 0 0 | 0       | General call address                                                                  |
| 1 1 1 1 0 x x | 0       | 10-bit slave address specification (during address authentication)                    |
| 1 1 1 1 0 x x | 1       | 10-bit slave address specification (after address match, when read command is issued) |

**Remark** See the I<sup>2</sup>C bus specifications issued by NXP Semiconductors for details of extension codes other than those described above.

### 13.5.12 Arbitration

When several master devices simultaneously generate a start condition (when the STT0 bit is set to 1 before the STD0 bit is set to 1), communication among the master devices is performed as the number of clocks are adjusted until the data differs. This kind of operation is called arbitration.

When one of the master devices loses in arbitration, an arbitration loss flag (ALD0) in the IICA status register 0 (IICS0) is set (1) via the timing by which the arbitration loss occurred, and the SCLA0 and SDAA0 lines are both set to high impedance, which releases the bus.

The arbitration loss is detected based on the timing of the next interrupt request (the eighth or ninth clock, when a stop condition is detected, etc.) and the ALD0 = 1 setting that has been made by software.

For details of interrupt request timing, see **13.5.8 Interrupt request (INTIICA0) generation timing and wait control**.

**Remark** STD0: Bit 1 of IICA status register 0 (IICS0)  
STT0: Bit 1 of IICA control register 00 (IICCTL00)

**Figure 13-21. Arbitration Timing Example**

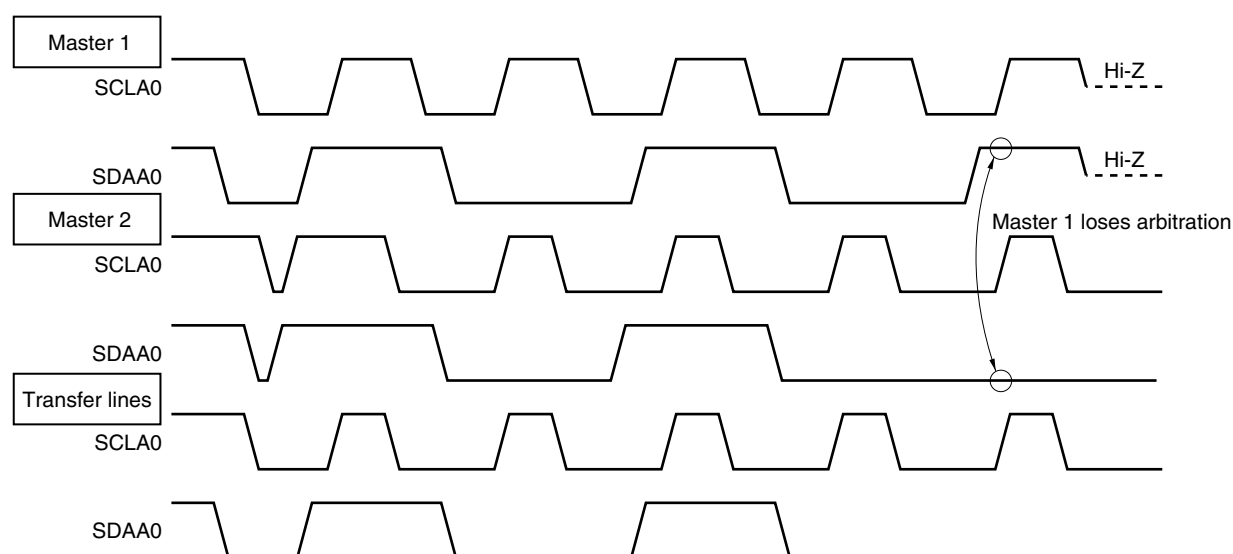




**Table 13-4. Status During Arbitration and Interrupt Request Generation Timing**

| Status During Arbitration                                                        | Interrupt Request Generation Timing                                                |
|----------------------------------------------------------------------------------|------------------------------------------------------------------------------------|
| During address transmission                                                      | At falling edge of eighth or ninth clock following byte transfer <sup>Note 1</sup> |
| Read/write data after address transmission                                       |                                                                                    |
| During extension code transmission                                               |                                                                                    |
| Read/write data after extension code transmission                                |                                                                                    |
| During data transmission                                                         |                                                                                    |
| During $\overline{\text{ACK}}$ transfer period after data transmission           |                                                                                    |
| When restart condition is detected during data transfer                          |                                                                                    |
| When stop condition is detected during data transfer                             | When stop condition is generated (when SPIE0 = 1) <sup>Note 2</sup>                |
| When data is at low level while attempting to generate a restart condition       | At falling edge of eighth or ninth clock following byte transfer <sup>Note 1</sup> |
| When stop condition is detected while attempting to generate a restart condition | When stop condition is generated (when SPIE0 = 1) <sup>Note 2</sup>                |
| When data is at low level while attempting to generate a stop condition          | At falling edge of eighth or ninth clock following byte transfer <sup>Note 1</sup> |
| When SCLA0 is at low level while attempting to generate a restart condition      |                                                                                    |

- Notes 1.** When the WTIM0 bit (bit 3 of IICA control register 00 (IICCTL00)) = 1, an interrupt request occurs at the falling edge of the ninth clock. When WTIM0 = 0 and the extension code's slave address is received, an interrupt request occurs at the falling edge of the eighth clock.
- 2.** When there is a chance that arbitration will occur, set SPIE0 = 1 for master device operation.

**Remark** SPIE0: Bit 4 of IICA control register 00 (IICCTL00)

### 13.5.13 Wakeup function

The I<sup>2</sup>C bus slave function is a function that generates an interrupt request signal (INTIICA0) when a local address and extension code have been received.

This function makes processing more efficient by preventing unnecessary INTIICA0 signal from occurring when addresses do not match.

When a start condition is detected, wakeup standby mode is set. This wakeup standby mode is in effect while addresses are transmitted due to the possibility that an arbitration loss may change the master device (which has generated a start condition) to a slave device.

<R>

To use the wakeup function in the STOP mode, set the WUP0 bit to 1. Addresses can be received regardless of the operation clock. An interrupt request signal (INTIICA0) is also generated when a local address and extension code have been received. Operation returns to normal operation by using an instruction to clear (0) the WUP0 bit after this interrupt has been generated.

Figure 13-22 shows the flow for setting WUP0 = 1 and Figure 13-23 shows the flow for setting WUP0 = 0 upon an address match.

**Figure 13-22. Flow When Setting WUP0 = 1**

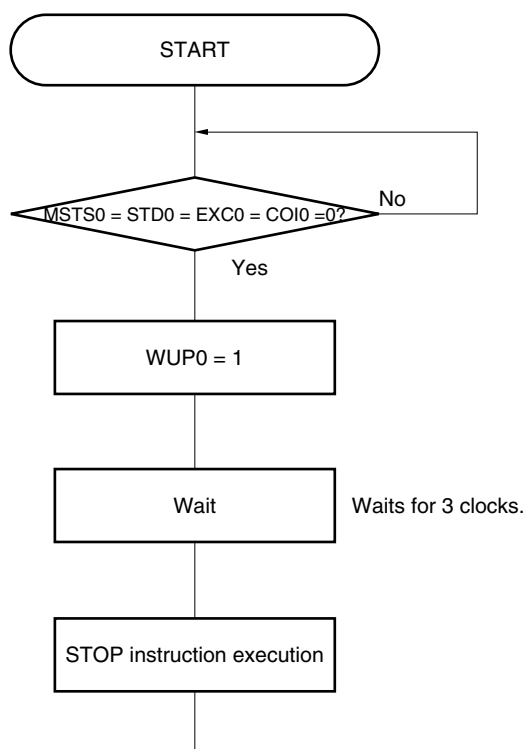
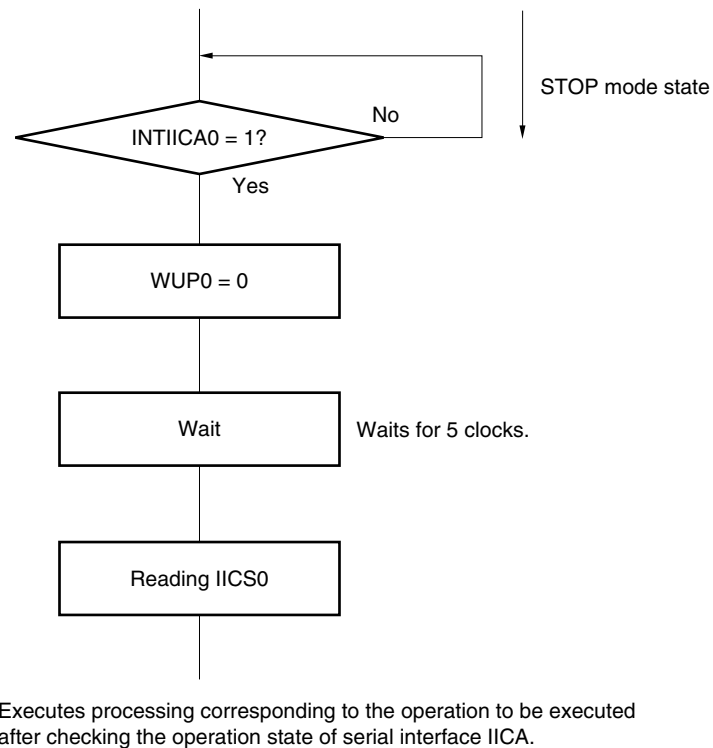
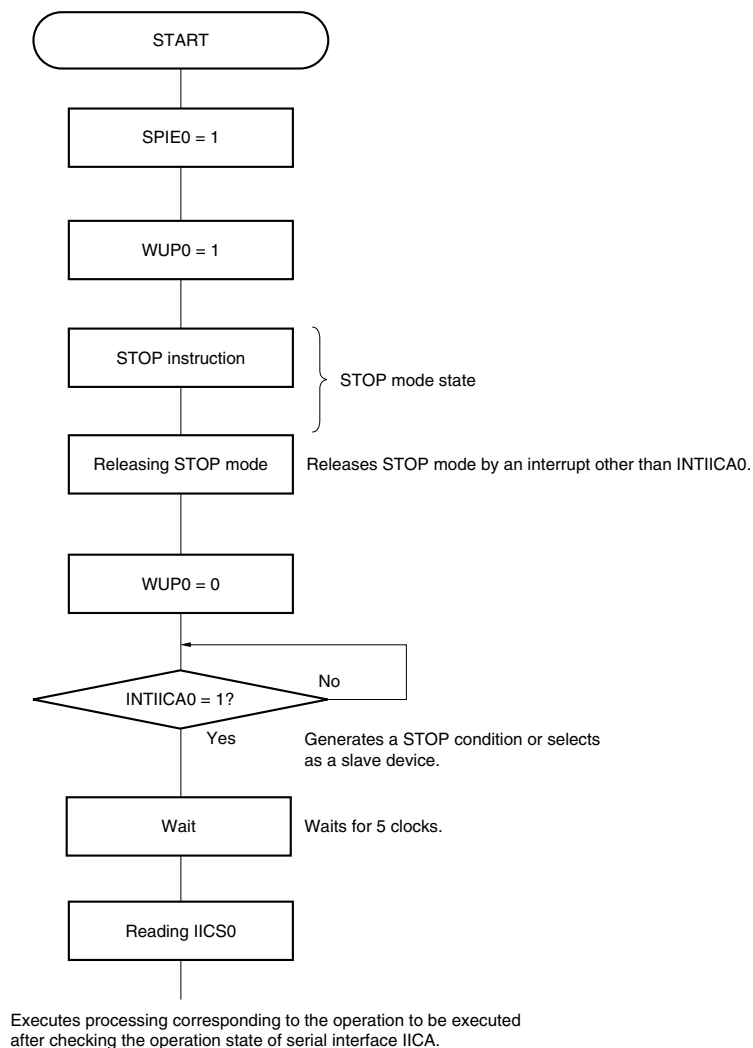


**Figure 13-23. Flow When Setting WUP0 = 0 upon Address Match (Including Extension Code Reception)**

Use the following flows to perform the processing to release the STOP mode other than by an interrupt request (INTIICA0) generated from serial interface IICA.

- Master device operation: Flow shown in Figure 13-24
- Slave device operation: Same as the flow in Figure 13-23

**Figure 13-24. When Operating as Master Device after Releasing STOP Mode other than by INTIICA0**

### 13.5.14 Communication reservation

#### (1) When communication reservation function is enabled (bit 0 (IICRSV) of IICA flag register 0 (IICF0) = 0)

To start master device communications when not currently using a bus, a communication reservation can be made to enable transmission of a start condition when the bus is released. There are two modes under which the bus is not used.

- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled ( $\overline{ACK}$  is not returned and the bus was released by setting bit 6 (LREL0) of IICA control register 00 (IICCTL00) to 1 and saving communication).

If bit 1 (STT0) of the IICCTL00 register is set to 1 while the bus is not used (after a stop condition is detected), a start condition is automatically generated and wait state is set.

If an address is written to the IICA shift register 0 (IICA0) after bit 4 (SPIE0) of the IICCTL00 register was set to 1, and it was detected by generation of an interrupt request signal (INTIICA0) that the bus was released (detection of the stop condition), then the device automatically starts communication as the master. Data written to the IICA0 register before the stop condition is detected is invalid.

When the STT0 bit has been set to 1, the operation mode (as start condition or as communication reservation) is determined according to the bus status.

- If the bus has been released ..... a start condition is generated
- If the bus has not been released (standby mode) ..... communication reservation

Check whether the communication reservation operates or not by using the MSTS0 bit (bit 7 of the IICA status register 0 (IICS0)) after the STT0 bit is set to 1 and the wait time elapses.

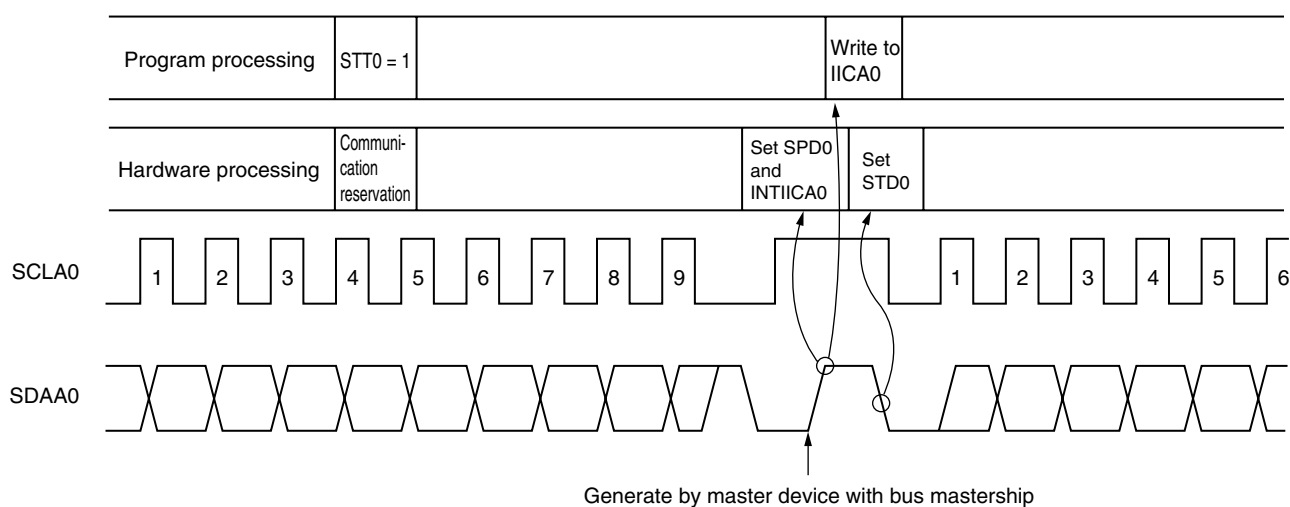
Use software to secure the wait time calculated by the following expression.

Wait time from setting STT0 = 1 to checking the MSTS0 flag:  
 $(IICWLO \text{ setting value} + IICWH0 \text{ setting value} + 4) + t_F \times 2 \times f_{CLK} [\text{clocks}]$

**Remark** IICWLO: IICA low-level width setting register 0  
 IICWH0: IICA high-level width setting register 0  
 $t_F$ : SDAA0 and SCLA0 signal falling times  
 $f_{CLK}$ : CPU/peripheral hardware clock frequency

Figure 13-25 shows the communication reservation timing.

**Figure 13-25. Communication Reservation Timing**



**Remark** IICA0: IICA shift register 0  
 STT0: Bit 1 of IICA control register 00 (IICCTL00)  
 STD0: Bit 1 of IICA status register 0 (IICS0)  
 SPD0: Bit 0 of IICA status register 0 (IICS0)

Communication reservations are accepted via the timing shown in Figure 13-26. After bit 1 (STD0) of the IICA status register 0 (IICS0) is set to 1, a communication reservation can be made by setting bit 1 (STT0) of IICA control register 00 (IICCTL00) to 1 before a stop condition is detected.

**Figure 13-26. Timing for Accepting Communication Reservations**

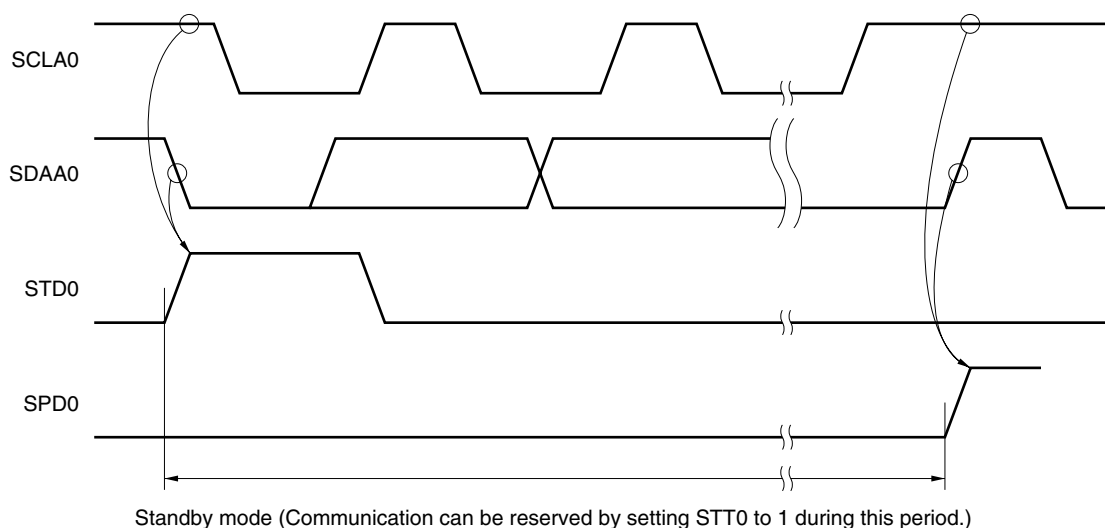
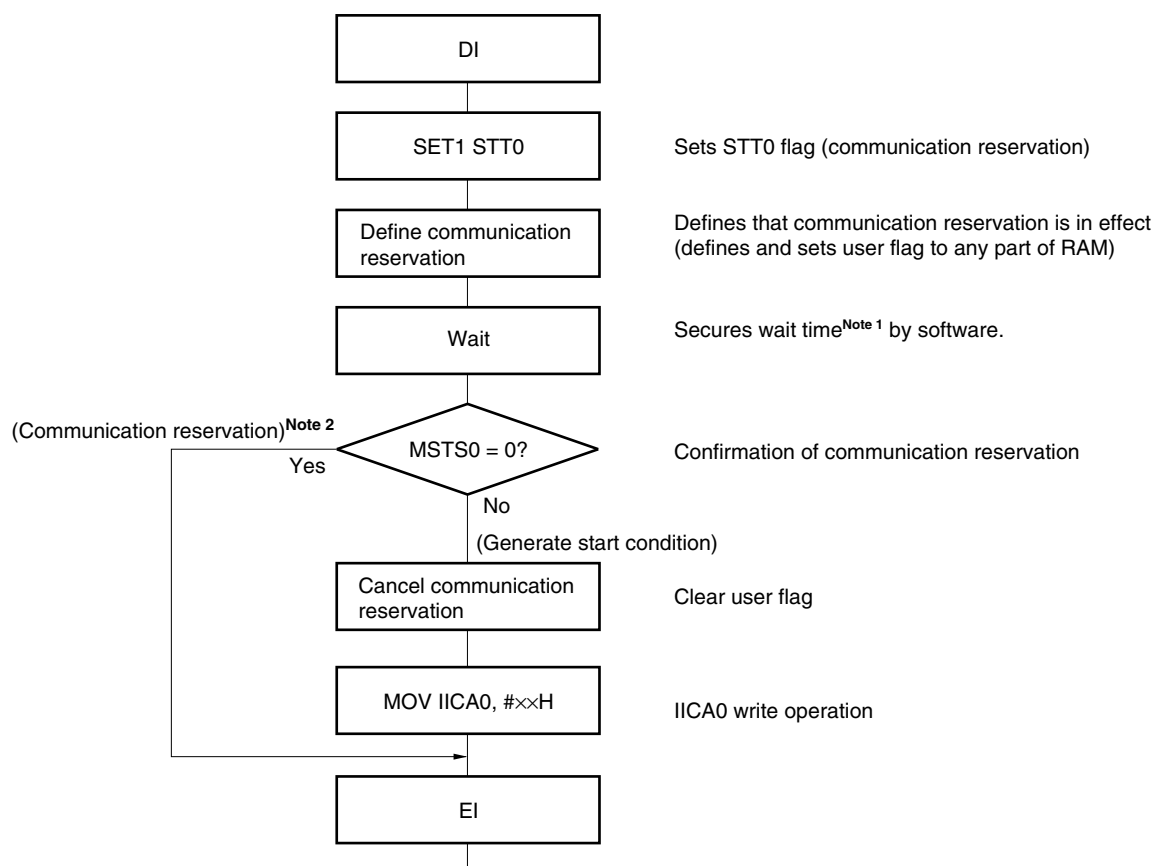


Figure 13-27 shows the communication reservation protocol.

**Figure 13-27. Communication Reservation Protocol**

**Notes 1.** The wait time is calculated as follows.

$(\text{IICWL0 setting value} + \text{IICWH0 setting value} + 4) + t_F \times 2 \times f_{\text{CLK}} [\text{clocks}]$

- 2.** The communication reservation operation executes a write to the IICA shift register 0 (IICA0) when a stop condition interrupt request occurs.

**Remark** STT0: Bit 1 of IICA control register 00 (IICCTL00)

MSTS0: Bit 7 of IICA status register 0 (IICS0)

IICA0: IICA shift register 0

IICWL0: IICA low-level width setting register 0

IICWH0: IICA high-level width setting register 0

$t_F$ : SDAA0 and SCLA0 signal falling times

$f_{\text{CLK}}$ : CPU/peripheral hardware clock frequency

**(2) When communication reservation function is disabled (bit 0 (IICRSV) of IICA flag register 0 (IICF0) = 1)**

When bit 1 (STT0) of IICA control register 00 (IICCTL00) is set to 1 when the bus is not used in a communication during bus communication, this request is rejected and a start condition is not generated. The following two statuses are included in the status where bus is not used.

- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled ( $\overline{\text{ACK}}$  is not returned and the bus was released by setting bit 6 (LREL0) of the IICCTL00 register to 1 and saving communication)

To confirm whether the start condition was generated or request was rejected, check STCF (bit 7 of the IICF0 register). It takes up to 5 clocks until the STCF bit is set to 1 after setting STT0 = 1. Therefore, secure the time by software.



### 13.5.15 Cautions

(1) When STCEN = 0

Immediately after I<sup>2</sup>C operation is enabled (IICE0 = 1), the bus communication status (IICBSY = 1) is recognized regardless of the actual bus status. When changing from a mode in which no stop condition has been detected to a master device communication mode, first generate a stop condition to release the bus, then perform master device communication.

When using multiple masters, it is not possible to perform master device communication when the bus has not been released (when a stop condition has not been detected).

Use the following sequence for generating a stop condition.

- <1> Set IICA control register 01 (IICCTL01).
- <2> Set bit 7 (IICE0) of IICA control register 00 (IICCTL00) to 1.
- <3> Set bit 0 (SPT0) of the IICCTL00 register to 1.

(2) When STCEN = 1

Immediately after I<sup>2</sup>C operation is enabled (IICE0 = 1), the bus released status (IICBSY = 0) is recognized regardless of the actual bus status. To generate the first start condition (STT0 = 1), it is necessary to confirm that the bus has been released, so as to not disturb other communications.

(3) If other I<sup>2</sup>C communications are already in progress

If I<sup>2</sup>C operation is enabled and the device participates in communication already in progress when the SDAA0 pin is low and the SCLA0 pin is high, the macro of I<sup>2</sup>C recognizes that the SDAA0 pin has gone low (detects a start condition). If the value on the bus at this time can be recognized as an extension code,  $\overline{ACK}$  is returned, but this interferes with other I<sup>2</sup>C communications. To avoid this, start I<sup>2</sup>C in the following sequence.

- <1> Clear bit 4 (SPIE0) of the IICCTL00 register to 0 to disable generation of an interrupt request signal (INTIICA0) when the stop condition is detected.
- <2> Set bit 7 (IICE0) of the IICCTL00 register to 1 to enable the operation of I<sup>2</sup>C.
- <3> Wait for detection of the start condition.
- <4> Set bit 6 (LREL0) of the IICCTL00 register to 1 before  $\overline{ACK}$  is returned (4 to 80 clocks after setting the IICE0 bit to 1), to forcibly disable detection.

(4) Setting the STT0 and SPT0 bits (bits 1 and 0 of the IICCTL00 register) again after they are set and before they are cleared to 0 is prohibited.

(5) When transmission is reserved, set the SPIE0 bit (bit 4 of the IICCTL0 register) to 1 so that an interrupt request is generated when the stop condition is detected. Transfer is started when communication data is written to the IICA shift register 0 (IICA0) after the interrupt request is generated. Unless the interrupt is generated when the stop condition is detected, the device stops in the wait state because the interrupt request is not generated when communication is started. However, it is not necessary to set the SPIE0 bit to 1 when the MST0 bit (bit 7 of the IICA status register 0 (IICS0)) is detected by software.

### 13.5.16 Communication operations

The following shows three operation procedures with the flowchart.

#### (1) Master operation in single master system

The flowchart when using the RL78/L12 as the master in a single master system is shown below.

This flowchart is broadly divided into the initial settings and communication processing. Execute the initial settings at startup. If communication with the slave is required, prepare the communication and then execute communication processing.

#### (2) Master operation in multimaster system

In the I<sup>2</sup>C bus multimaster system, whether the bus is released or used cannot be judged by the I<sup>2</sup>C bus specifications when the bus takes part in a communication. Here, when data and clock are at a high level for a certain period (1 frame), the RL78/L12 takes part in a communication with bus released state.

This flowchart is broadly divided into the initial settings, communication waiting, and communication processing. The processing when the RL78/L12 loses in arbitration and is specified as the slave is omitted here, and only the processing as the master is shown. Execute the initial settings at startup to take part in a communication. Then, wait for the communication request as the master or wait for the specification as the slave. The actual communication is performed in the communication processing, and it supports the transmission/reception with the slave and the arbitration with other masters.

#### (3) Slave operation

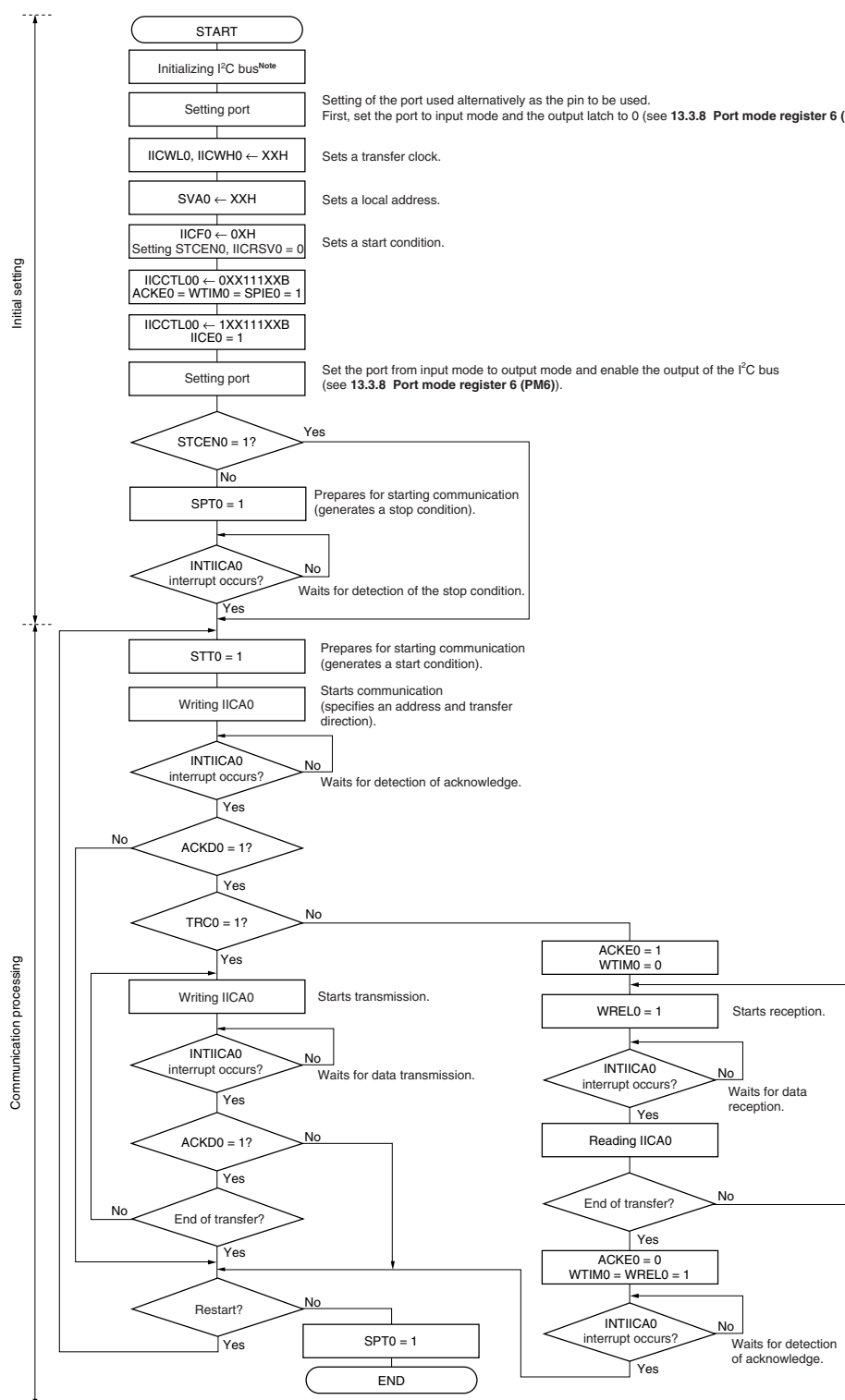
An example of when the RL78/L12 is used as the I<sup>2</sup>C bus slave is shown below.

When used as the slave, operation is started by an interrupt. Execute the initial settings at startup, then wait for the INTIICA0 interrupt occurrence (communication waiting). When an INTIICA0 interrupt occurs, the communication status is judged and its result is passed as a flag over to the main processing.

By checking the flags, necessary communication processing is performed.

### (1) Master operation in single-master system

**Figure 13-28. Master Operation in Single-Master System**

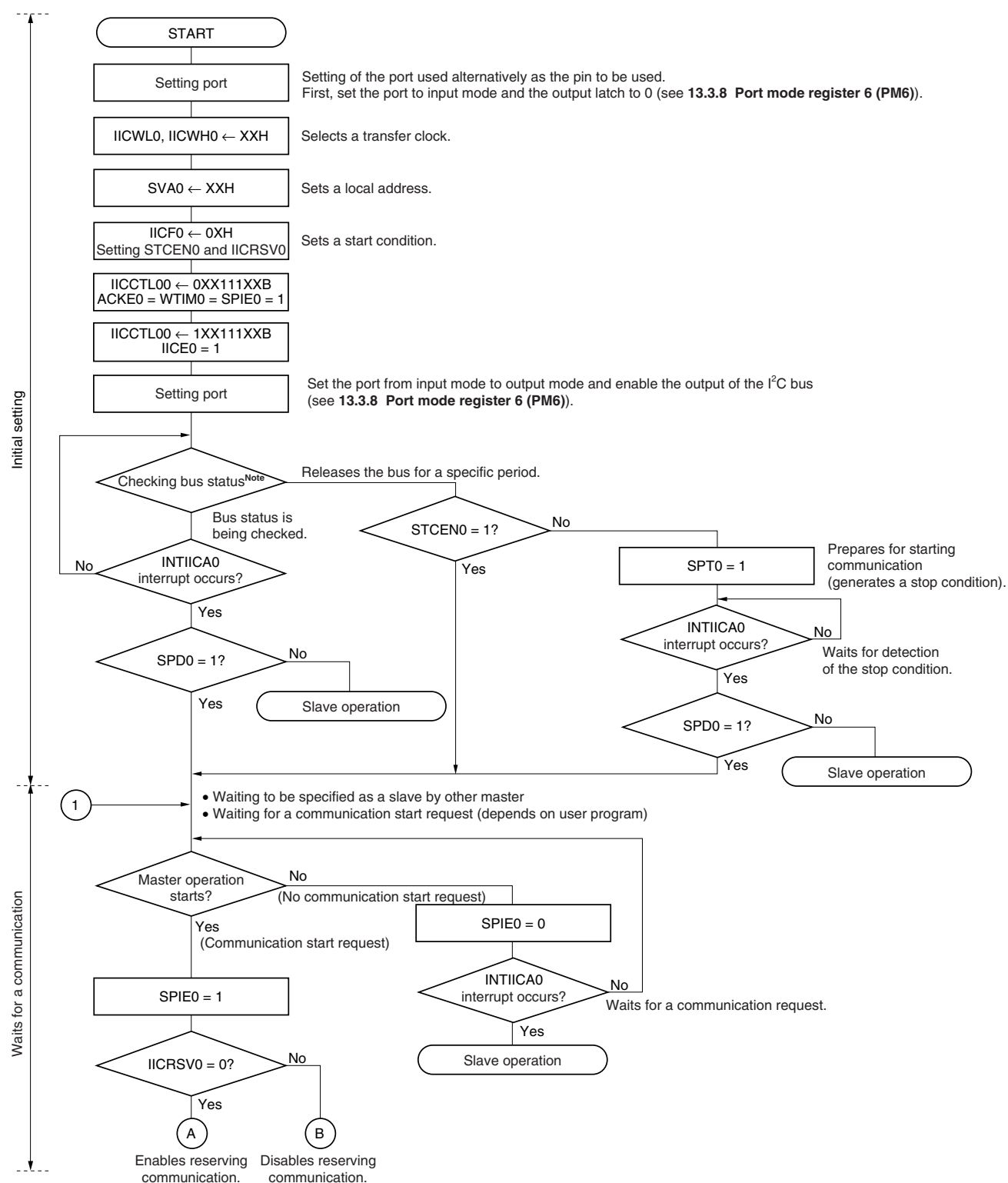


**Note** Release (SCLA0 and SDAA0 pins = high level) the I<sup>2</sup>C bus in conformance with the specifications of the product that is communicating. If EEPROM is outputting a low level to the SDAA0 pin, for example, set the SCLA0 pin in the output port mode, and output a clock pulse from the output port until the SDAA0 pin is constantly at high level.

**Remark** Conform to the specifications of the product that is communicating, with respect to the transmission and reception formats.

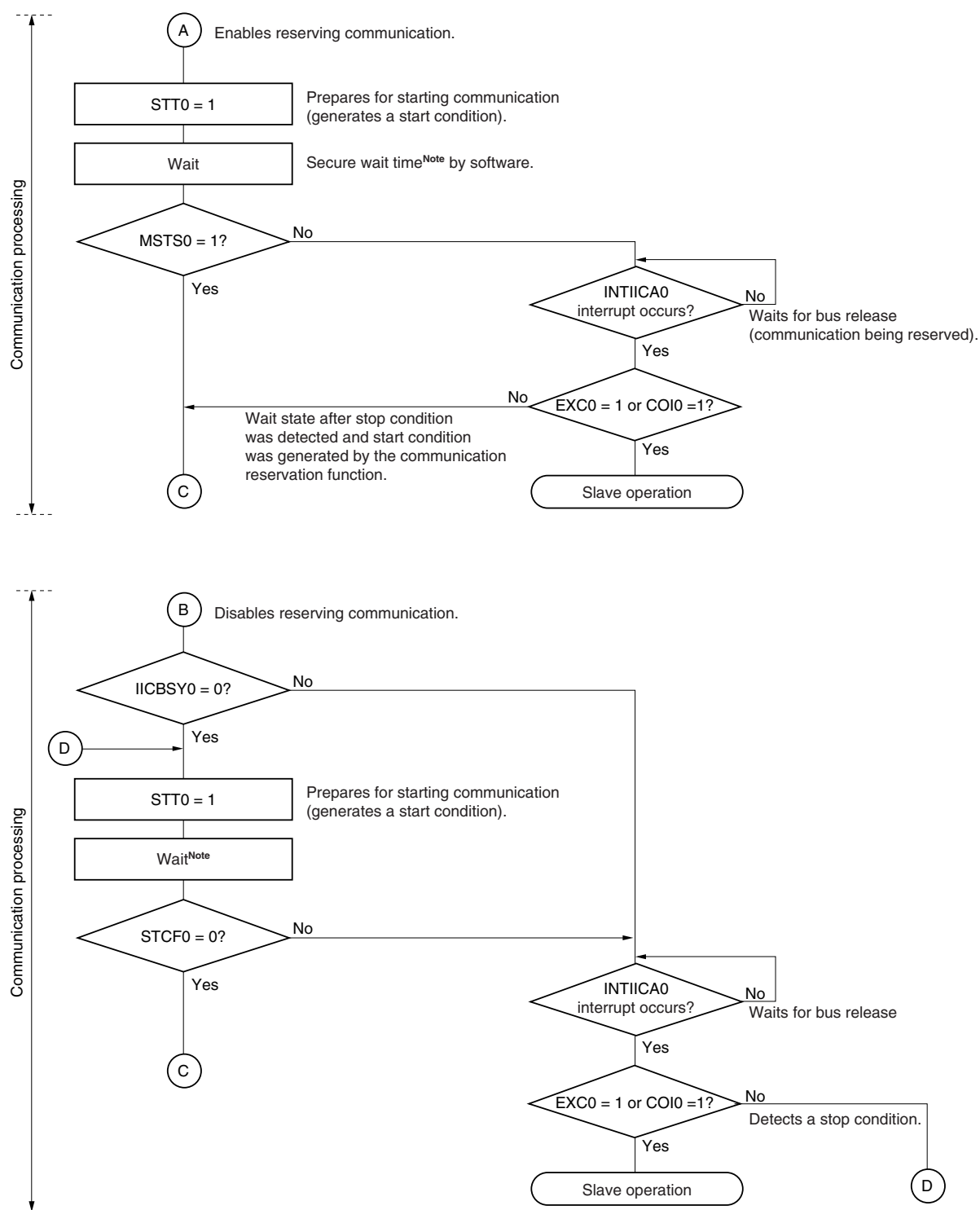
## (2) Master operation in multi-master system

Figure 13-29. Master Operation in Multi-Master System (1/3)



**Note** Confirm that the bus is released (CLD0 bit = 1, DAD0 bit = 1) for a specific period (for example, for a period of one frame). If the SDAA0 pin is constantly at low level, decide whether to release the I<sup>2</sup>C bus (SCLA0 and SDAA0 pins = high level) in conformance with the specifications of the product that is communicating.

Figure 13-29. Master Operation in Multi-Master System (2/3)



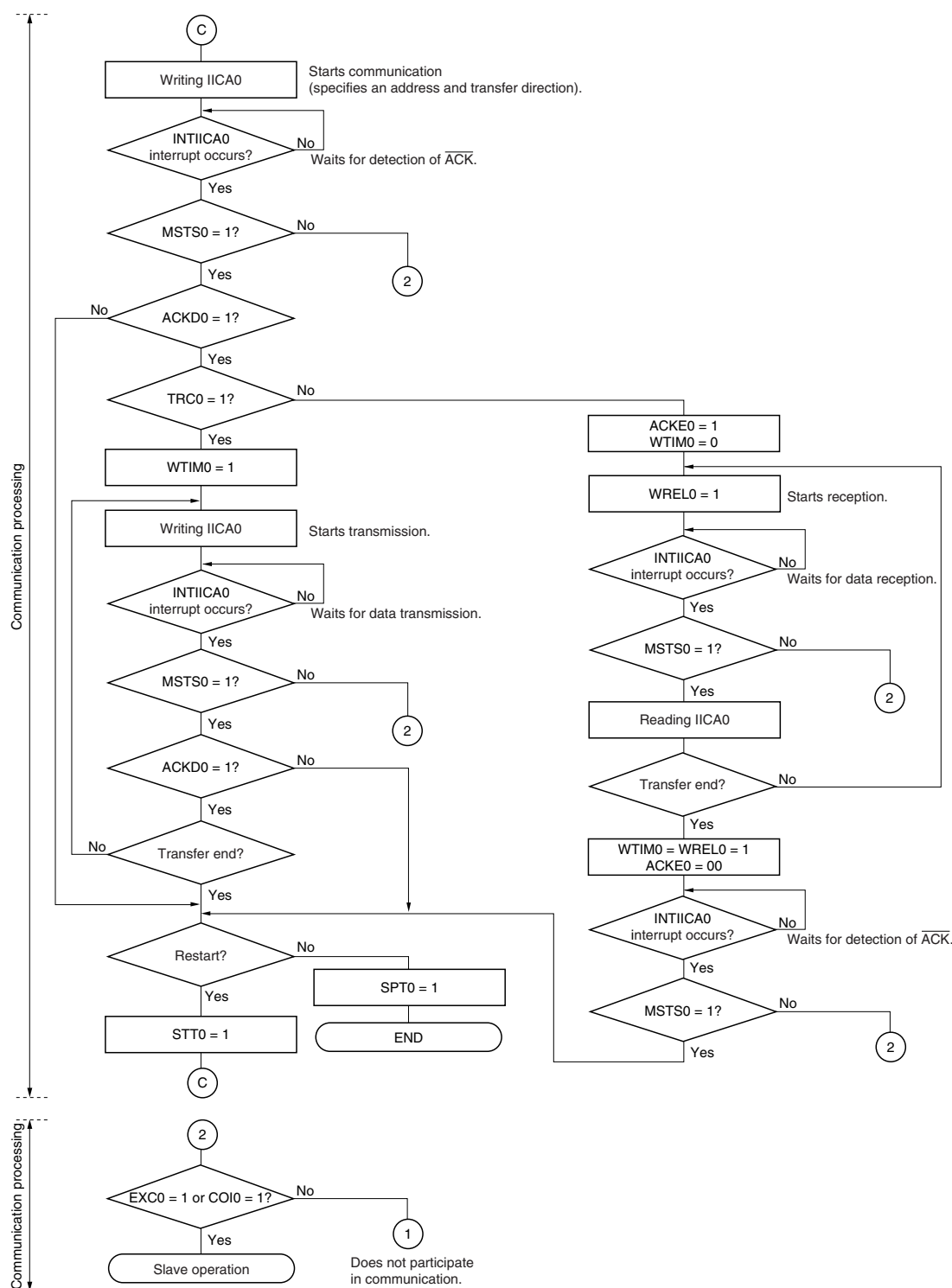
**Note** The wait time is calculated as follows.

$$(\text{IICWL0 setting value} + \text{IICWH0 setting value} + 4) \times f_{\text{CLK}} + t_{\text{F}} \times 2 \text{ [clocks]}$$

**Remark**

- IICWL0: IICA low-level width setting register 0
- IICWH0: IICA high-level width setting register 0
- $t_{\text{F}}$ : SDAA0 and SCLA0 signal falling times
- $f_{\text{CLK}}$ : CPU/peripheral hardware clock frequency

Figure 13-29. Master Operation in Multi-Master System (3/3)



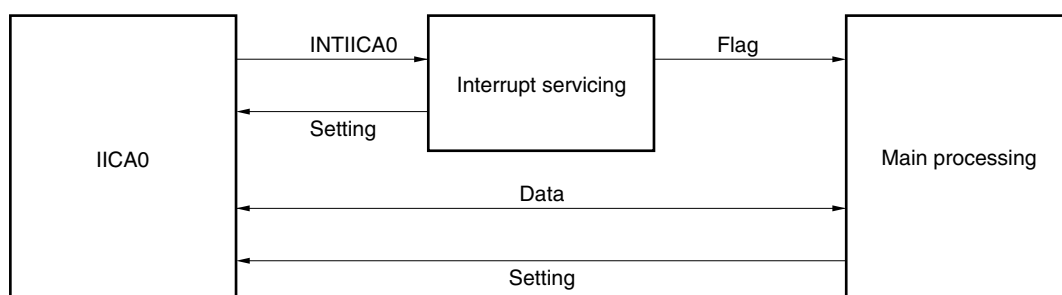
- Remarks**
1. Conform to the specifications of the product that is communicating, with respect to the transmission and reception formats.
  2. To use the device as a master in a multi-master system, read the MST0 bit each time interrupt INTIICA0 has occurred to check the arbitration result.
  3. To use the device as a slave in a multi-master system, check the status by using the IICA status register 0 (IICS0) and IICA flag register 0 (IICF0) each time interrupt INTIICA0 has occurred, and determine the processing to be performed next.

**(3) Slave operation**

The processing procedure of the slave operation is as follows.

Basically, the slave operation is event-driven. Therefore, processing by the INTIICA0 interrupt (processing that must substantially change the operation status such as detection of a stop condition during communication) is necessary.

In the following explanation, it is assumed that the extension code is not supported for data communication. It is also assumed that the INTIICA0 interrupt servicing only performs status transition processing, and that actual data communication is performed by the main processing.



Therefore, data communication processing is performed by preparing the following three flags and passing them to the main processing instead of INTIICA0.

**<1> Communication mode flag**

This flag indicates the following two communication statuses.

- Clear mode: Status in which data communication is not performed
- Communication mode: Status in which data communication is performed (from valid address detection to stop condition detection, no detection of  $\overline{\text{ACK}}$  from master, address mismatch)

**<2> Ready flag**

This flag indicates that data communication is enabled. Its function is the same as the INTIICA0 interrupt for ordinary data communication. This flag is set by interrupt servicing and cleared by the main processing. Clear this flag by interrupt servicing when communication is started. However, the ready flag is not set by interrupt servicing when the first data is transmitted. Therefore, the first data is transmitted without the flag being cleared (an address match is interpreted as a request for the next data).

**<3> Communication direction flag**

This flag indicates the direction of communication. Its value is the same as the TRC0 bit.

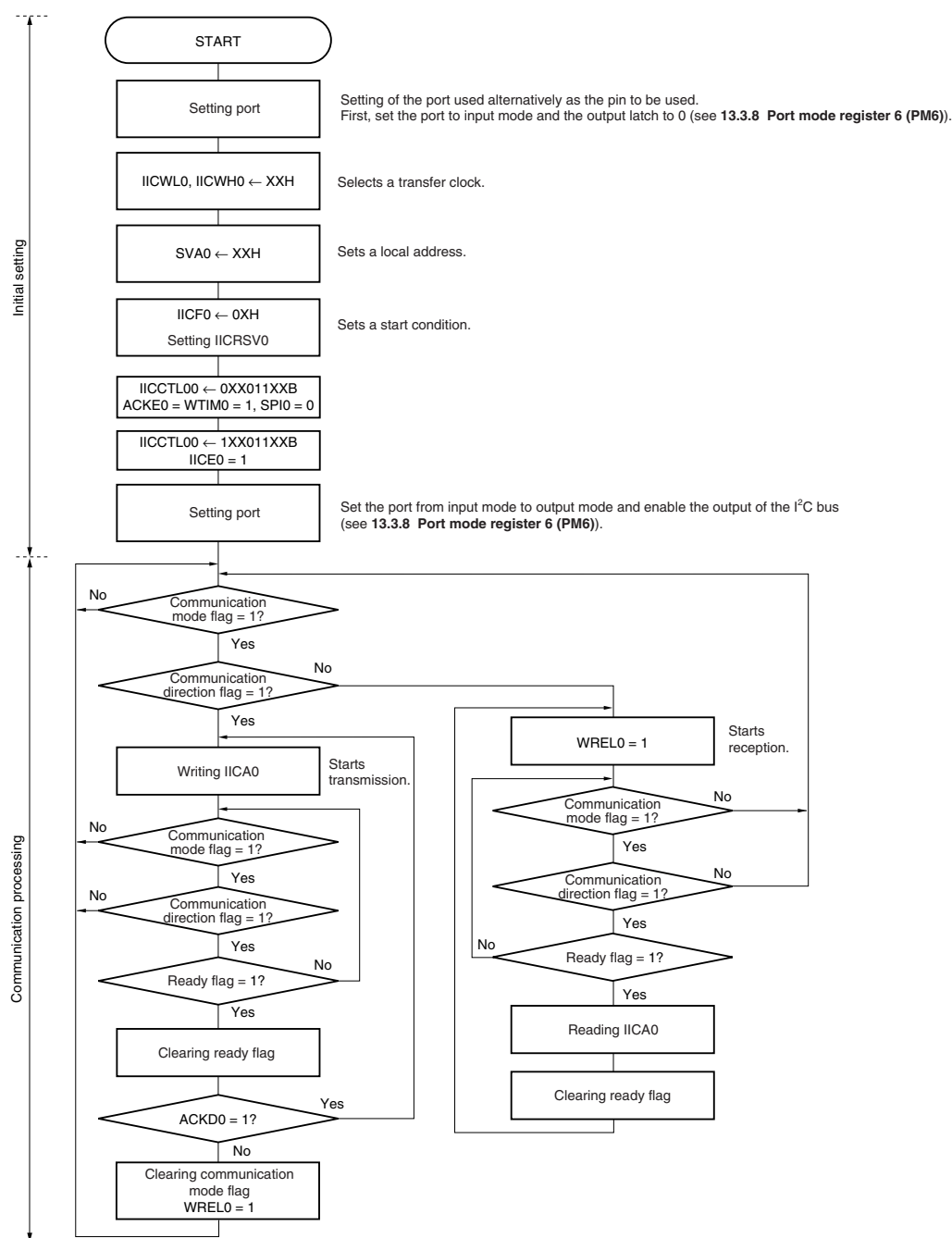
The main processing of the slave operation is explained next.

Start serial interface IICA and wait until communication is enabled. When communication is enabled, execute communication by using the communication mode flag and ready flag (processing of the stop condition and start condition is performed by an interrupt. Here, check the status by using the flags).

The transmission operation is repeated until the master no longer returns  $\overline{\text{ACK}}$ . If  $\overline{\text{ACK}}$  is not returned from the master, communication is completed.

For reception, the necessary amount of data is received. When communication is completed,  $\overline{\text{ACK}}$  is not returned as the next data. After that, the master generates a stop condition or restart condition. Exit from the communication status occurs in this way.

Figure 13-30. Slave Operation Flowchart (1)



**Remark** Conform to the specifications of the product that is in communication, regarding the transmission and reception formats.

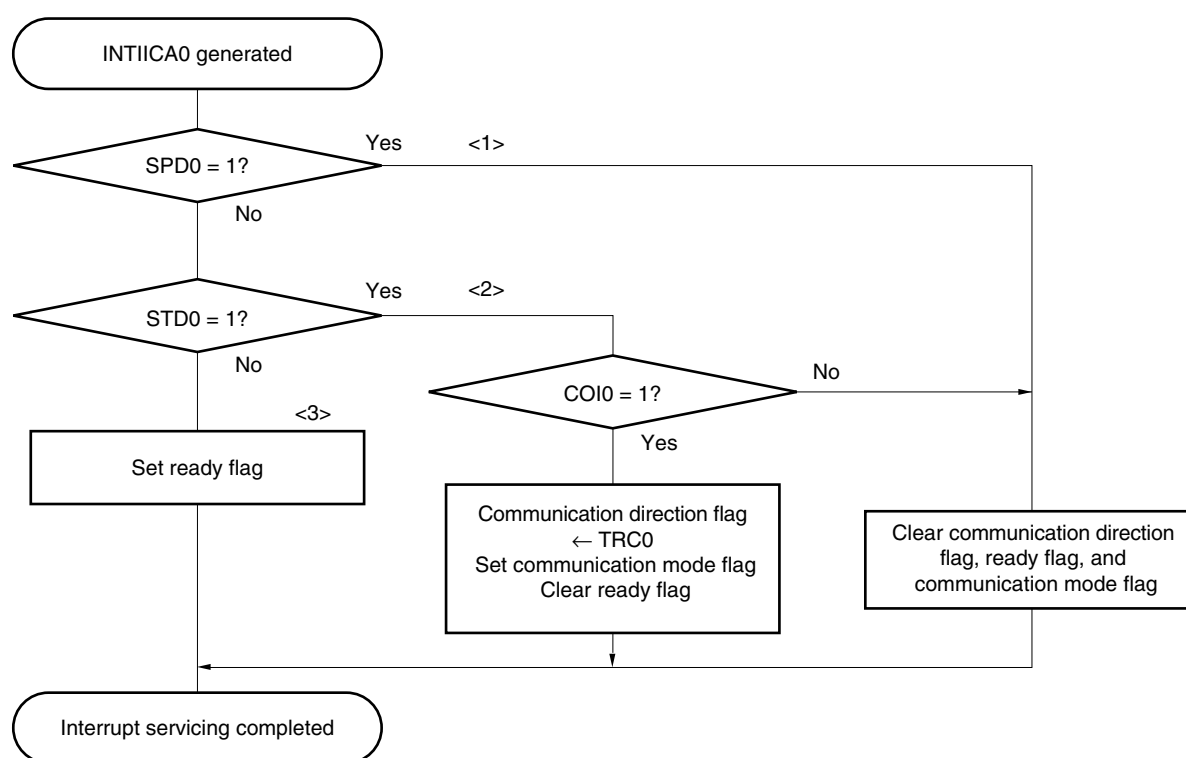


An example of the processing procedure of the slave with the INTIICA0 interrupt is explained below (processing is performed assuming that no extension code is used). The INTIICA0 interrupt checks the status, and the following operations are performed.

- <1> Communication is stopped if the stop condition is issued.
- <2> If the start condition is issued, the address is checked and communication is completed if the address does not match. If the address matches, the communication mode is set, wait is cancelled, and processing returns from the interrupt (the ready flag is cleared).
- <3> For data transmit/receive, only the ready flag is set. Processing returns from the interrupt with the I<sup>2</sup>C bus remaining in the wait state.

**Remark** <1> to <3> above correspond to <1> to <3> in Figure 13-31 Slave Operation Flowchart (2).

**Figure 13-31. Slave Operation Flowchart (2)**



### 13.5.17 Timing of I<sup>2</sup>C interrupt request (INTIICA0) occurrence

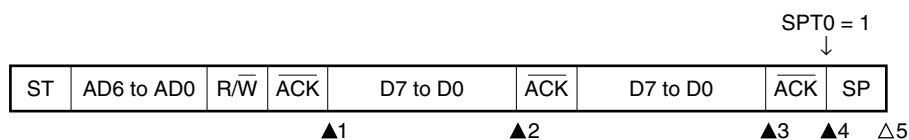
The timing of transmitting or receiving data and generation of interrupt request signal INTIICA0, and the value of the IICA status register 0 (IICS0) when the INTIICA0 signal is generated are shown below.

**Remark** ST: Start condition  
 AD6 to AD0: Address  
 R/W: Transfer direction specification  
 ACK: Acknowledge  
 D7 to D0: Data  
 SP: Stop condition

## (1) Master device operation

## (a) Start ~ Address ~ Data ~ Data ~ Stop (transmission/reception)

## (i) When WTIM0 = 0



▲1: IICS0 = 1000×110B

▲2: IICS0 = 1000×000B

▲3: IICS0 = 1000×000B (Sets the WTIM0 bit to 1)<sup>Note</sup>▲4: IICS0 = 1000××00B (Sets the SPT0 bit to 1)<sup>Note</sup>

Δ5: IICS0 = 00000001B

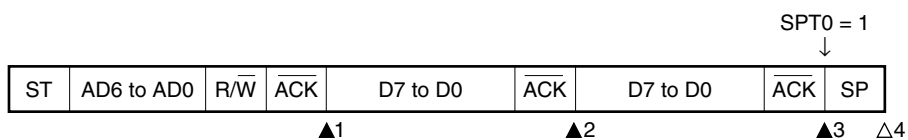
**Note** To generate a stop condition, set the WTIM0 bit to 1 and change the timing for generating the INTIICA0 interrupt request signal.

**Remark** ▲: Always generated

Δ: Generated only when SPIE0 = 1

×: Don't care

## (ii) When WTIM0 = 1



▲1: IICS0 = 1000×110B

▲2: IICS0 = 1000×100B

▲3: IICS0 = 1000××00B (Sets the SPT0 bit to 1)

Δ4: IICS0 = 00000001B

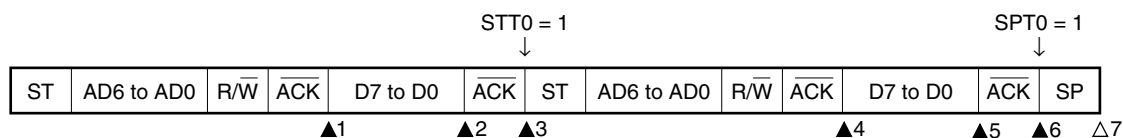
**Remark** ▲: Always generated

Δ: Generated only when SPIE0 = 1

×: Don't care

## (b) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop (restart)

## (i) When WTIM0 = 0



▲1: IICS0 = 1000×110B

▲2: IICS0 = 1000×000B (Sets the WTIM0 bit to 1)<sup>Note 1</sup>▲3: IICS0 = 1000××00B (Clears the WTIM0 bit to 0<sup>Note 2</sup>, sets the STT0 bit to 1)

▲4: IICS0 = 1000×110B

▲5: IICS0 = 1000×000B (Sets the WTIM0 bit to 1)<sup>Note 3</sup>

▲6: IICS0 = 1000××00B (Sets the SPT0 bit to 1)

Δ7: IICS0 = 00000001B

**Notes 1.** To generate a start condition, set the WTIM0 bit to 1 and change the timing for generating the INTIICA0 interrupt request signal.

**2.** Clear the WTIM0 bit to 0 to restore the original setting.

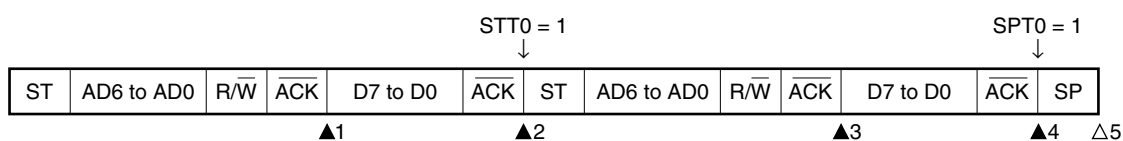
**3.** To generate a stop condition, set the WTIM0 bit to 1 and change the timing for generating the INTIICA0 interrupt request signal.

**Remark** ▲: Always generated

Δ: Generated only when SPIE0 = 1

×: Don't care

## (ii) When WTIM0 = 1



▲1: IICS0 = 1000×110B

▲2: IICS0 = 1000××00B (Sets the STT0 bit to 1)

▲3: IICS0 = 1000×110B

▲4: IICS0 = 1000××00B (Sets the SPT0 bit to 1)

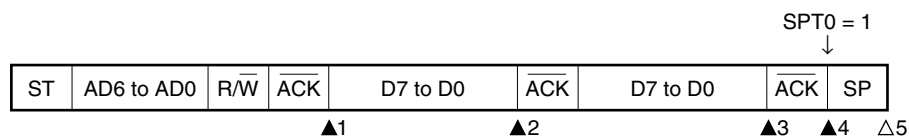
Δ5: IICS0 = 00000001B

**Remark** ▲: Always generated

Δ: Generated only when SPIE0 = 1

×: Don't care

## (c) Start ~ Code ~ Data ~ Data ~ Stop (extension code transmission)

(i) When  $WTIM0 = 0$ 

▲1: IICS0 = 1010×110B

▲2: IICS0 = 1010×000B

▲3: IICS0 = 1010×000B (Sets the  $WTIM0$  bit to 1)<sup>Note</sup>▲4: IICS0 = 1010××00B (Sets the  $SPT0$  bit to 1)

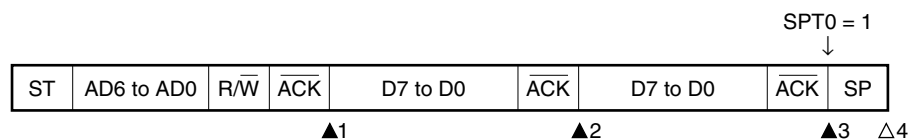
Δ5: IICS0 = 00000001B

**Note** To generate a stop condition, set the  $WTIM0$  bit to 1 and change the timing for generating the  $INTIICA0$  interrupt request signal.

**Remark** ▲: Always generated

Δ: Generated only when  $SPIE0 = 1$

×: Don't care

(ii) When  $WTIM0 = 1$ 

▲1: IICS0 = 1010×110B

▲2: IICS0 = 1010×100B

▲3: IICS0 = 1010××00B (Sets the  $SPT0$  bit to 1)

Δ4: IICS0 = 00001001B

**Remark** ▲: Always generated

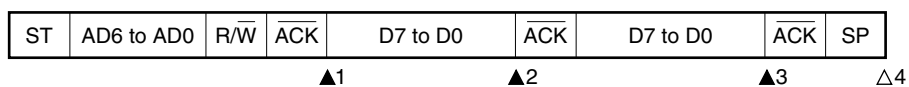
Δ: Generated only when  $SPIE0 = 1$

×: Don't care

## (2) Slave device operation (slave address data reception)

## (a) Start ~ Address ~ Data ~ Data ~ Stop

## (i) When WTIM0 = 0



▲1: IICS0 = 0001×110B

▲2: IICS0 = 0001×000B

▲3: IICS0 = 0001×000B

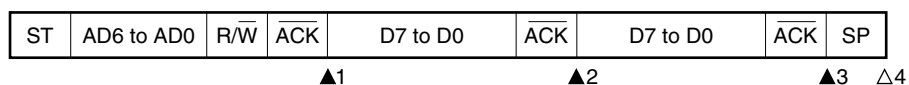
△4: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

## (ii) When WTIM0 = 1



▲1: IICS0 = 0001×110B

▲2: IICS0 = 0001×100B

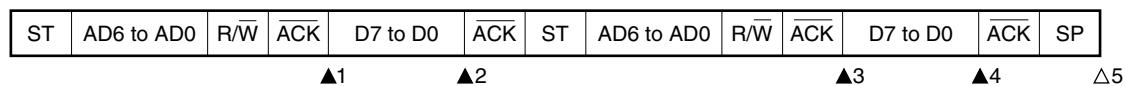
▲3: IICS0 = 0001××00B

△4: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

**(b) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop****(i) When WTIM0 = 0 (after restart, matches with SVA0)**

▲1: IICS0 = 0001×110B

▲2: IICS0 = 0001×000B

▲3: IICS0 = 0001×110B

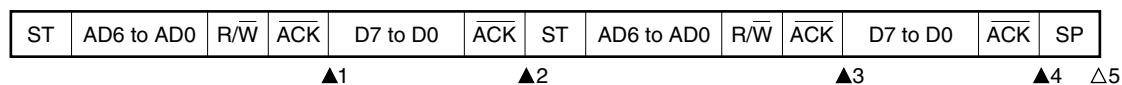
▲4: IICS0 = 0001×000B

△5: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

**(ii) When WTIM0 = 1 (after restart, matches with SVA0)**

▲1: IICS0 = 0001×110B

▲2: IICS0 = 0001××00B

▲3: IICS0 = 0001×110B

▲4: IICS0 = 0001××00B

△5: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

## (c) Start ~ Address ~ Data ~ Start ~ Code ~ Data ~ Stop

(i) When  $WTIM0 = 0$  (after restart, does not match address (= extension code))

▲1: IICS0 = 0001x110B

▲2: IICS0 = 0001x000B

▲3: IICS0 = 0010x010B

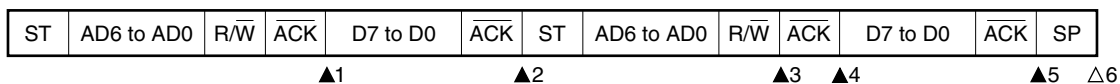
▲4: IICS0 = 0010x000B

△5: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

x: Don't care

(ii) When  $WTIM0 = 1$  (after restart, does not match address (= extension code))

▲1: IICS0 = 0001x110B

▲2: IICS0 = 0001xx00B

▲3: IICS0 = 0010x010B

▲4: IICS0 = 0010x110B

▲5: IICS0 = 0010xx00B

△6: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

x: Don't care

**(d) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop****(i) When WTIM0 = 0 (after restart, does not match address (= not extension code))**

&lt;R&gt;



▲1: IICS0 = 0001×110B

▲2: IICS0 = 0001×000B

▲3: IICS0 = 00000×10B

△4: IICS0 = 00000001B

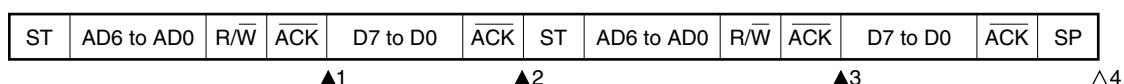
**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

x: Don't care

**(ii) When WTIM0 = 1 (after restart, does not match address (= not extension code))**

&lt;R&gt;



▲1: IICS0 = 0001×110B

▲2: IICS0 = 0001××00B

▲3: IICS0 = 00000×10B

△4: IICS0 = 00000001B

**Remark** ▲: Always generated

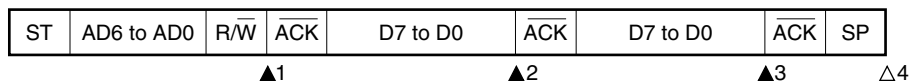
△: Generated only when SPIE0 = 1

x: Don't care



**(3) Slave device operation (when receiving extension code)**

The device is always participating in communication when it receives an extension code.

**(a) Start ~ Code ~ Data ~ Data ~ Stop****(i) When WTIM0 = 0**

▲1: IICS0 = 0010×010B

▲2: IICS0 = 0010×000B

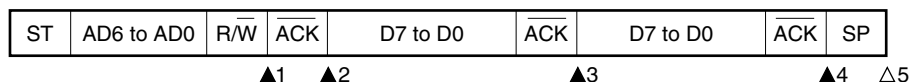
▲3: IICS0 = 0010×000B

△4: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

**(ii) When WTIM0 = 1**

▲1: IICS0 = 0010×010B

▲2: IICS0 = 0010×110B

▲3: IICS0 = 0010×100B

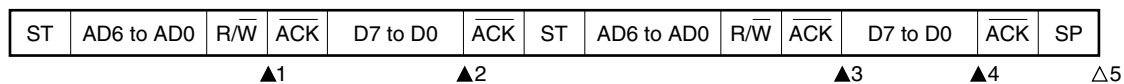
▲4: IICS0 = 0010××00B

△5: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

**(b) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop****(i) When WTIM0 = 0 (after restart, matches SVA0)**

▲1: IICS0 = 0010×010B

▲2: IICS0 = 0010×000B

▲3: IICS0 = 0001×110B

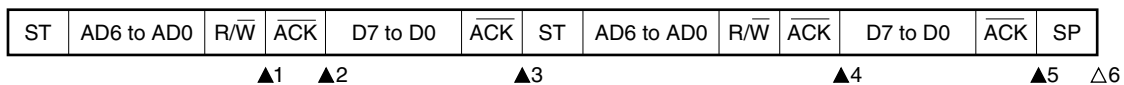
▲4: IICS0 = 0001×000B

△5: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

**(ii) When WTIM0 = 1 (after restart, matches SVA0)**

▲1: IICS0 = 0010×010B

▲2: IICS0 = 0010×110B

▲3: IICS0 = 0010××00B

▲4: IICS0 = 0001×110B

▲5: IICS0 = 0001××00B

△6: IICS0 = 00000001B

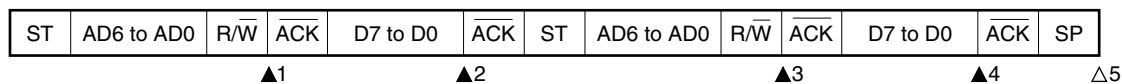
**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

## (c) Start ~ Code ~ Data ~ Start ~ Code ~ Data ~ Stop

## (i) When WTIM0 = 0 (after restart, extension code reception)



▲1: IICS0 = 0010×010B

▲2: IICS0 = 0010×000B

▲3: IICS0 = 0010×010B

▲4: IICS0 = 0010×000B

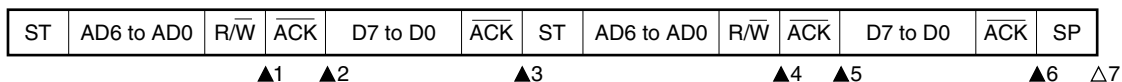
△5: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

## (ii) When WTIM0 = 1 (after restart, extension code reception)



▲1: IICS0 = 0010×010B

▲2: IICS0 = 0010×110B

▲3: IICS0 = 0010××00B

▲4: IICS0 = 0010×010B

▲5: IICS0 = 0010×110B

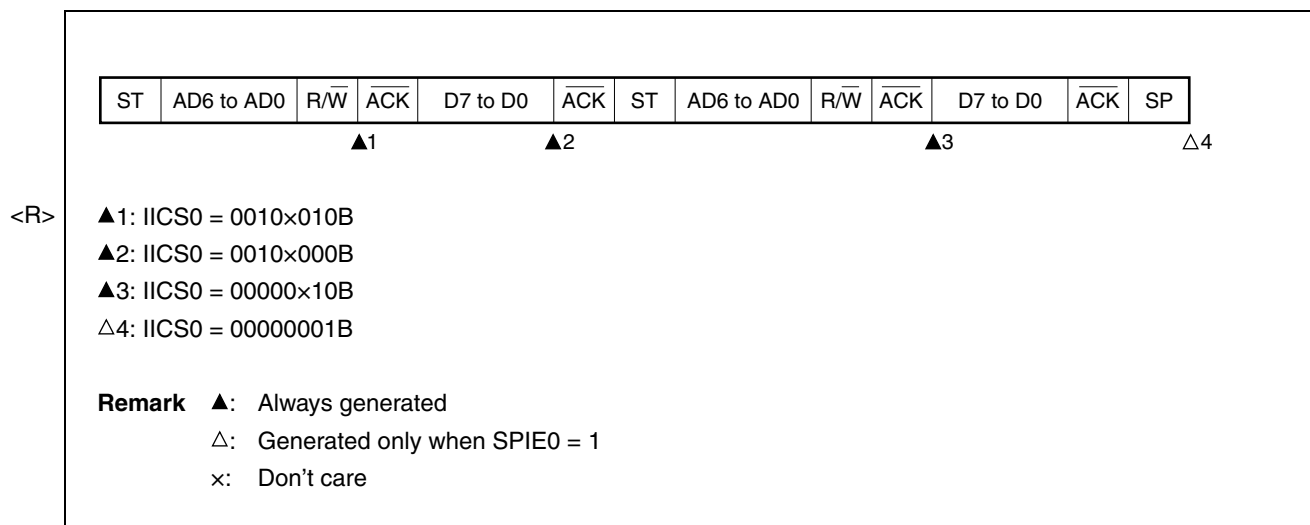
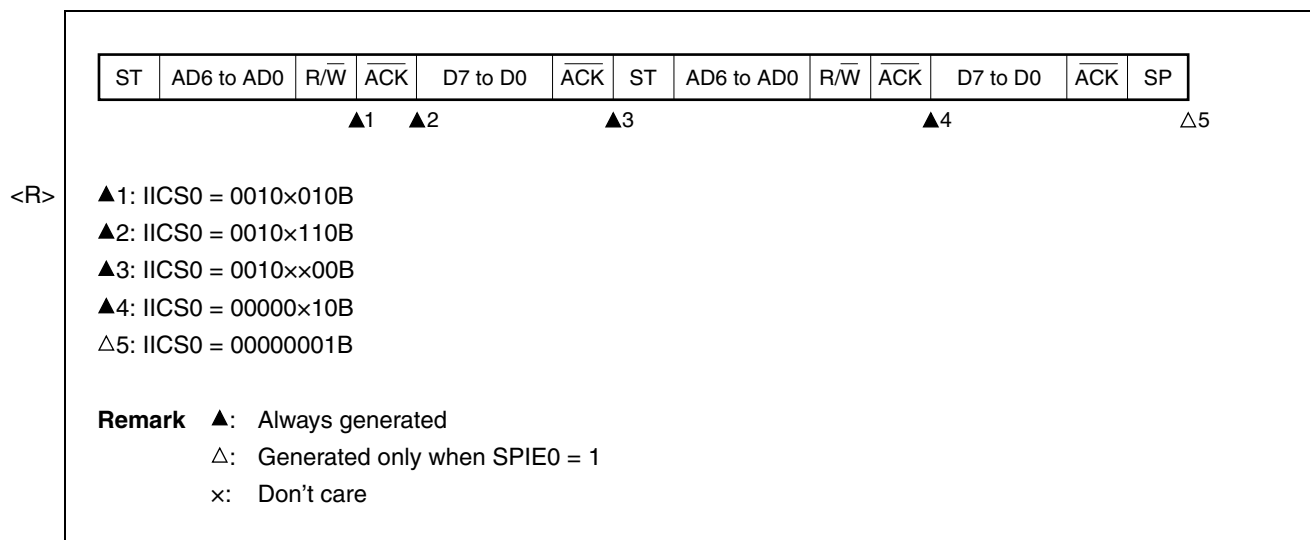
▲6: IICS0 = 0010××00B

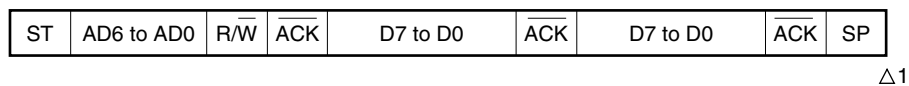
△7: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

**(d) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop****(i) When WTIM0 = 0 (after restart, does not match address (= not extension code))****(ii) When WTIM0 = 1 (after restart, does not match address (= not extension code))**

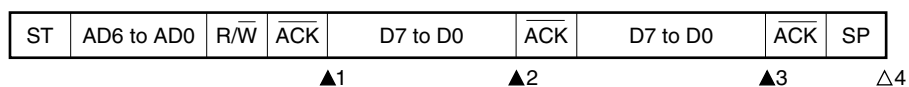
**(4) Operation without communication****(a) Start ~ Code ~ Data ~ Data ~ Stop**

△1: IICS0 = 00000001B

**Remark** △: Generated only when SPIE0 = 1

**(5) Arbitration loss operation (operation as slave after arbitration loss)**

When the device is used as a master in a multi-master system, read the MSTS0 bit each time interrupt request signal INTIICA0 has occurred to check the arbitration result.

**(a) When arbitration loss occurs during transmission of slave address data****(i) When WTIM0 = 0**

▲1: IICS0 = 0101x110B

▲2: IICS0 = 0001x000B

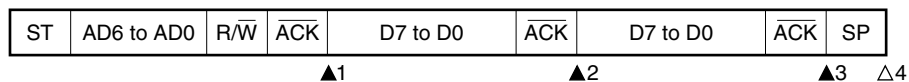
▲3: IICS0 = 0001x000B

△4: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

x: Don't care

(ii) When **WTIM0 = 1**

▲1: IICS0 = 0101×110B

▲2: IICS0 = 0001×100B

▲3: IICS0 = 0001××00B

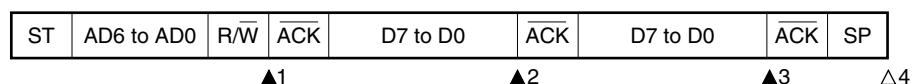
△4: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

## (b) When arbitration loss occurs during transmission of extension code

(i) When **WTIM0 = 0**

▲1: IICS0 = 0110×010B

▲2: IICS0 = 0010×000B

▲3: IICS0 = 0010×000B

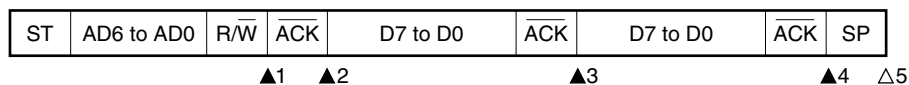
△4: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

×: Don't care

## (ii) When WTIM0 = 1



▲1: IICS0 = 0110x010B

▲2: IICS0 = 0010x110B

▲3: IICS0 = 0010x100B

▲4: IICS0 = 0010xx00B

△5: IICS0 = 00000001B

**Remark** ▲: Always generated

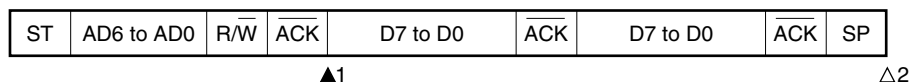
△: Generated only when SPIE0 = 1

x: Don't care

## (6) Operation when arbitration loss occurs (no communication after arbitration loss)

When the device is used as a master in a multi-master system, read the MSTS0 bit each time interrupt request signal INTIICA0 has occurred to check the arbitration result.

## (a) When arbitration loss occurs during transmission of slave address data (when WTIM0 = 1)

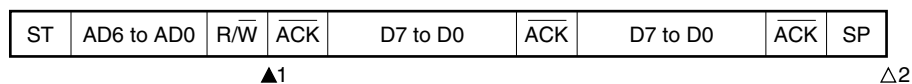


▲1: IICS0 = 01000110B

△2: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

**(b) When arbitration loss occurs during transmission of extension code**

▲1: IICS0 = 0110x010B

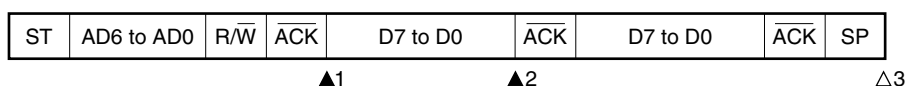
Sets LREL0 = 1 by software

△2: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

x: Don't care

**(c) When arbitration loss occurs during transmission of data****(i) When WTIM0 = 0**

▲1: IICS0 = 10001110B

▲2: IICS0 = 01000000B

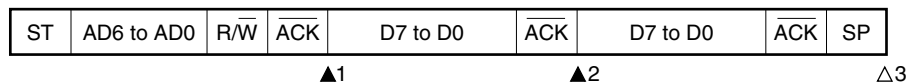
△3: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1



## (ii) When WTIM0 = 1



▲1: IICS0 = 10001110B

▲2: IICS0 = 01000100B

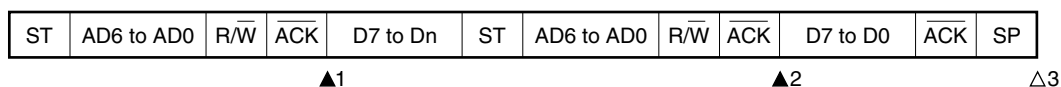
△3: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

## (d) When loss occurs due to restart condition during data transfer

## (i) Not extension code (Example: unmatched with SVA0)



▲1: IICS0 = 1000×110B

▲2: IICS0 = 01000110B

△3: IICS0 = 00000001B

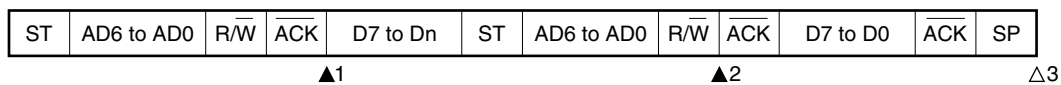
**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

x: Don't care

n = 6 to 0

## (ii) Extension code



▲1: IICS0 = 1000×110B

▲2: IICS0 = 01100010B

Sets LREL0 = 1 by software

△3: IICS0 = 00000001B

**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

x: Don't care

n = 6 to 0

## (e) When loss occurs due to stop condition during data transfer



▲1: IICS0 = 10000110B

△2: IICS0 = 01000001B

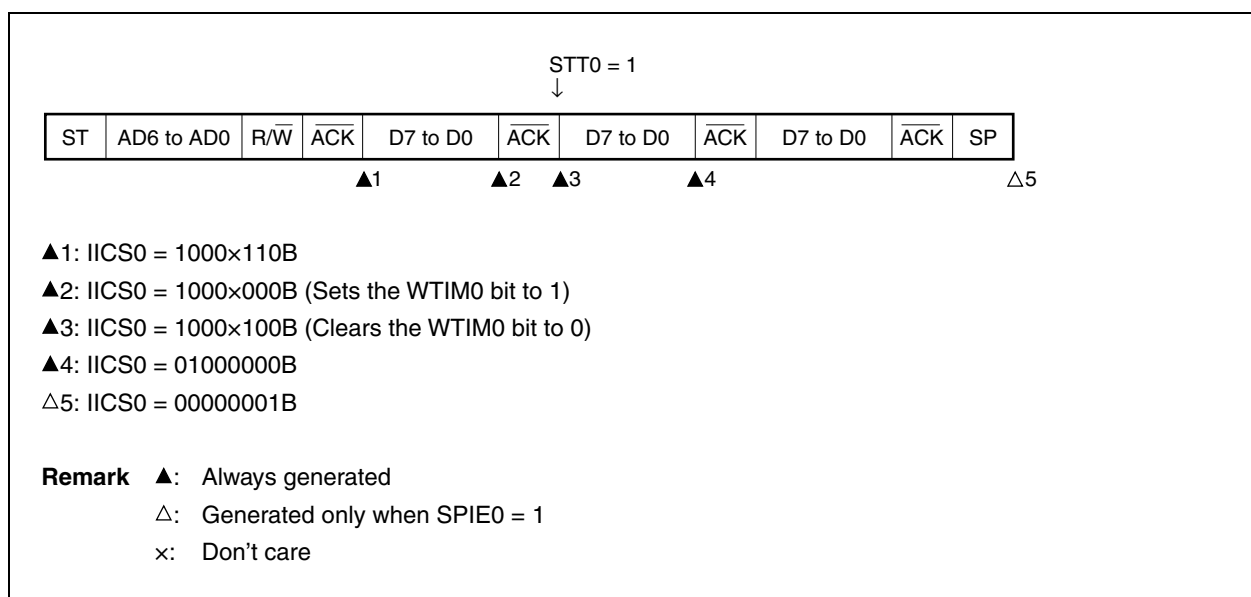
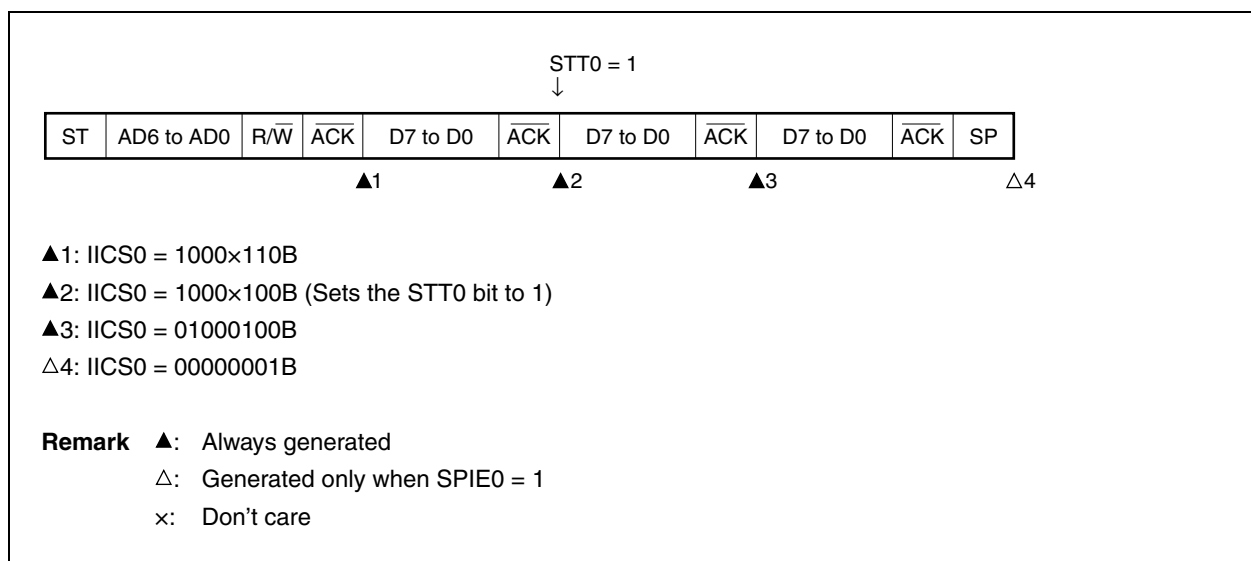
**Remark** ▲: Always generated

△: Generated only when SPIE0 = 1

x: Don't care

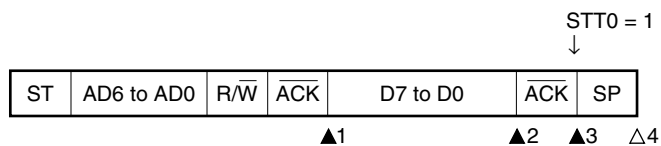
n = 6 to 0

## (f) When arbitration loss occurs due to low-level data when attempting to generate a restart condition

(i) When  $WTIM0 = 0$ (ii) When  $WTIM0 = 1$ 

(g) When arbitration loss occurs due to a stop condition when attempting to generate a restart condition

(i) When  $WTIM0 = 0$



▲1: IICS0 = 1000×110B

▲2: IICS0 = 1000×000B (Sets the  $WTIM0$  bit to 1)

▲3: IICS0 = 1000××00B (Sets the  $STT0$  bit to 1)

△4: IICS0 = 01000001B

**Remark** ▲: Always generated

△: Generated only when  $SPIE0 = 1$

x: Don't care

(ii) When  $WTIM0 = 1$



▲1: IICS0 = 1000×110B

▲2: IICS0 = 1000××00B (Sets the  $STT0$  bit to 1)

△3: IICS0 = 01000001B

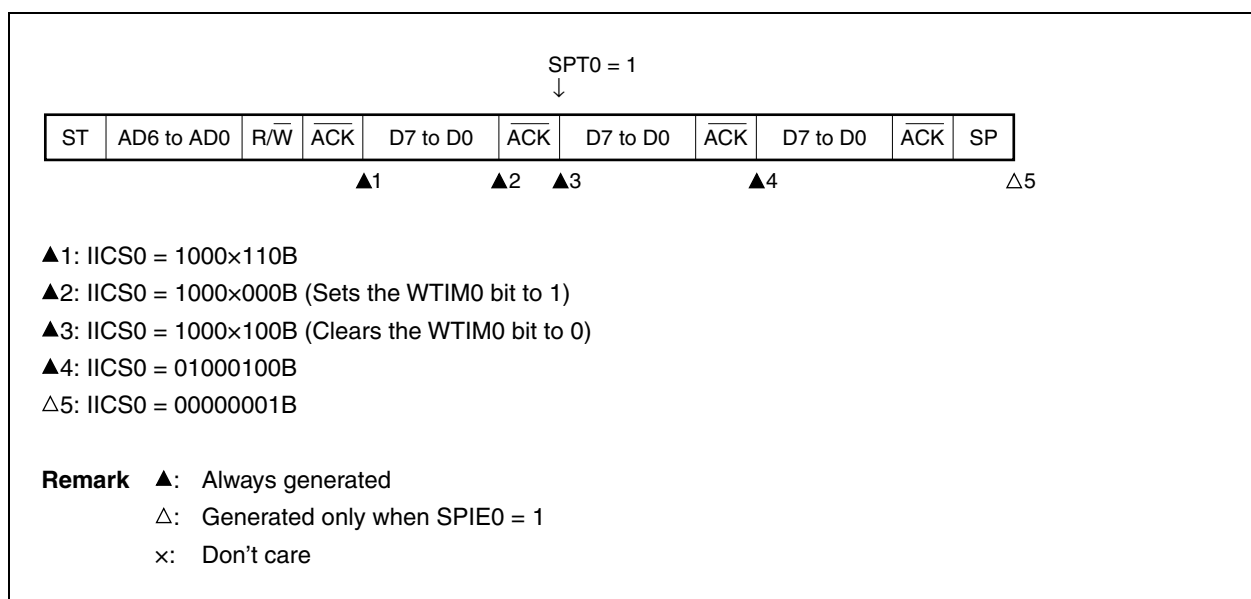
**Remark** ▲: Always generated

△: Generated only when  $SPIE0 = 1$

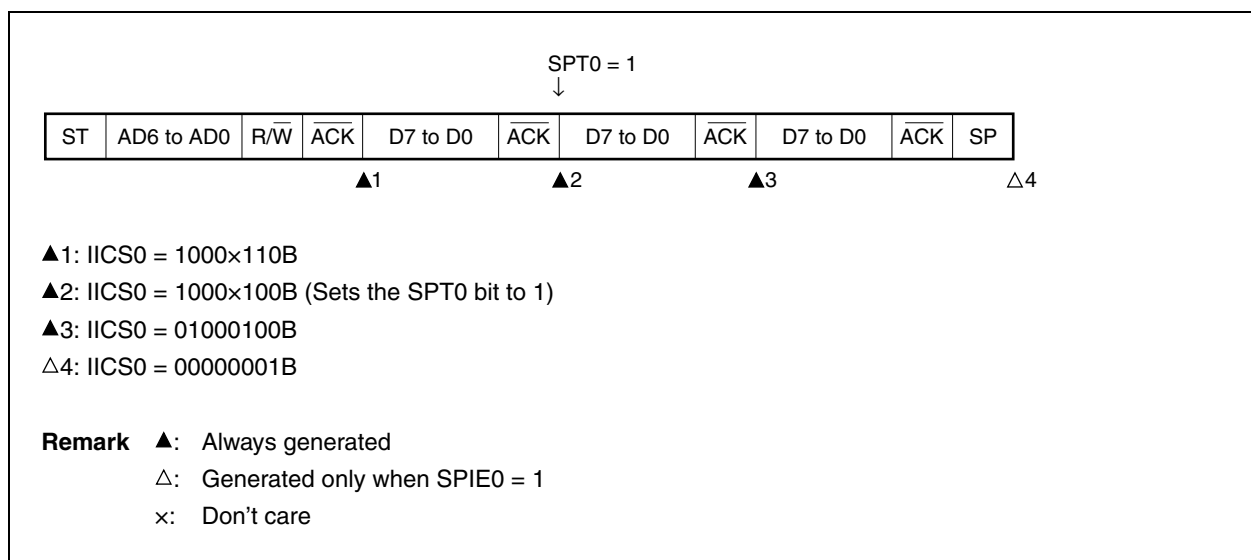
x: Don't care

(h) When arbitration loss occurs due to low-level data when attempting to generate a stop condition

(i) When  $WTIM0 = 0$



(ii) When  $WTIM0 = 1$



### 13.6 Timing Charts

When using the I<sup>2</sup>C bus mode, the master device outputs an address via the serial bus to select one of several slave devices as its communication partner.

After outputting the slave address, the master device transmits the TRC0 bit (bit 3 of the IICA status register 0 (IICS0)), which specifies the data transfer direction, and then starts serial communication with the slave device.

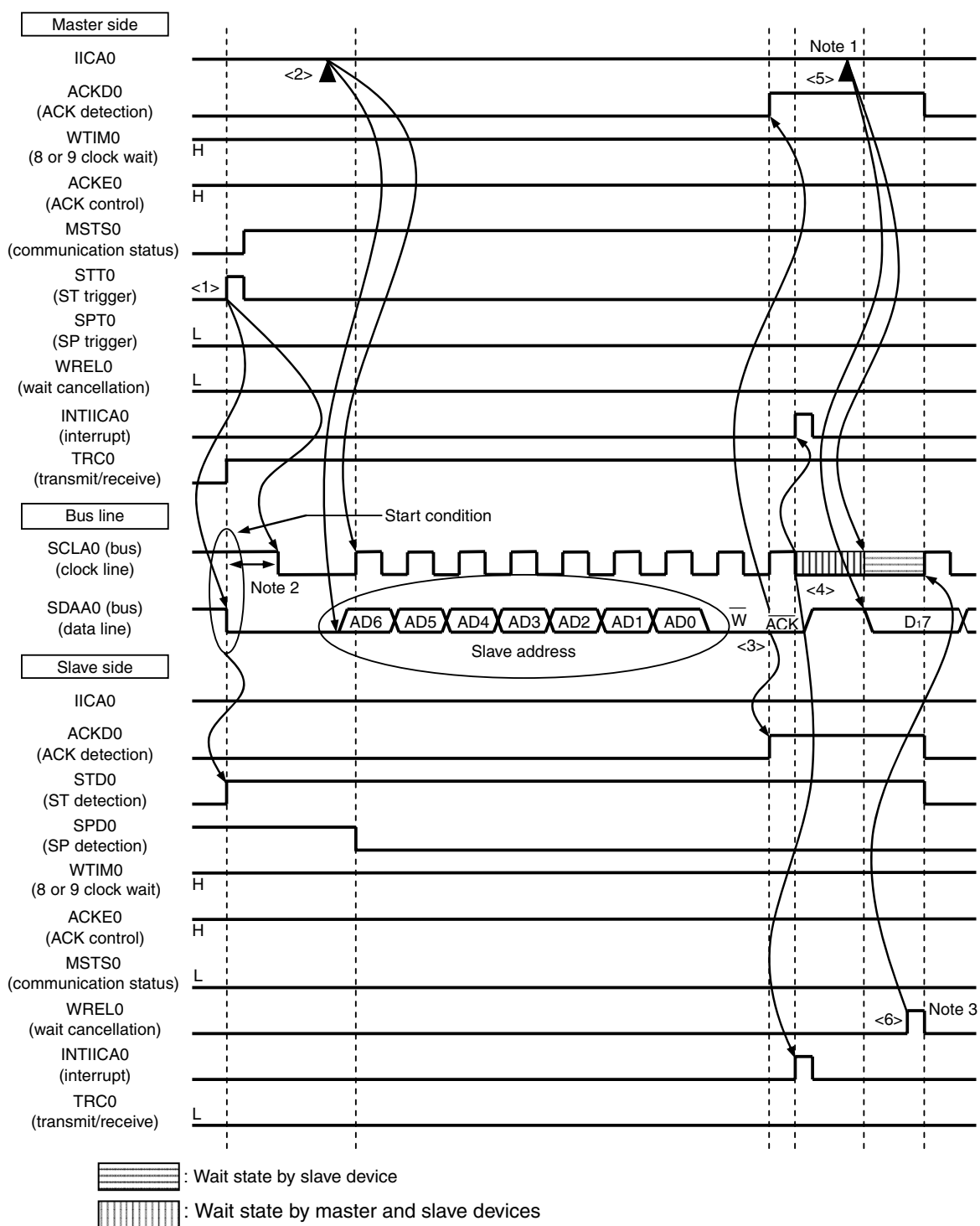
Figures 13-32 and 13-33 show timing charts of the data communication.

The IICA shift register 0 (IICA0)'s shift operation is synchronized with the falling edge of the serial clock (SCLA0). The transmit data is transferred to the SO latch and is output (MSB first) via the SDAA0 pin.

Data input via the SDAA0 pin is captured into IICA0 at the rising edge of SCLA0.

**Figure 13-32. Example of Master to Slave Communication**  
**(9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (1/4)**

**(1) Start condition ~ address ~ data**



- Notes**
1. Write data to IICA0, not setting the WREL0 bit, in order to cancel a wait state during transmission by a master device.
  2. Make sure that the time between the fall of the SDAA0 pin signal and the fall of the SCLA0 pin signal is at least 4.0  $\mu$ s when specifying standard mode and at least 0.6  $\mu$ s when specifying fast mode.
  3. For releasing wait state during reception of a slave device, write "FFH" to IICA0 or set the WREL0 bit.

The meanings of <1> to <6> in (1) Start condition ~ address ~ data in Figure 13-32 are explained below.

- <1> The start condition trigger is set by the master device (STT0 = 1) and a start condition (i.e. SCLA0 = 1 changes SDAA0 from 1 to 0) is generated once the bus data line goes low (SDAA0). When the start condition is subsequently detected, the master device enters the master device communication status (MSTS0 = 1). The master device is ready to communicate once the bus clock line goes low (SCLA0 = 0) after the hold time has elapsed.
- <2> The master device writes the address + W (transmission) to the IICA shift register 0 (IICA0) and transmits the slave address.
- <3> In the slave device if the address received matches the address (SVA0 value) of a slave device<sup>Note</sup>, that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.
- <4> The master device issues an interrupt (INTIICA0: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a wait status (SCLA0 = 0) and issues an interrupt (INTIICA0: address match)<sup>Note</sup>.
- <5> The master device writes the data to transmit to the IICA0 register and releases the wait status that it set by the master device.
- <6> If the slave device releases the wait status (WREL0 = 1), the master device starts transferring data to the slave device.

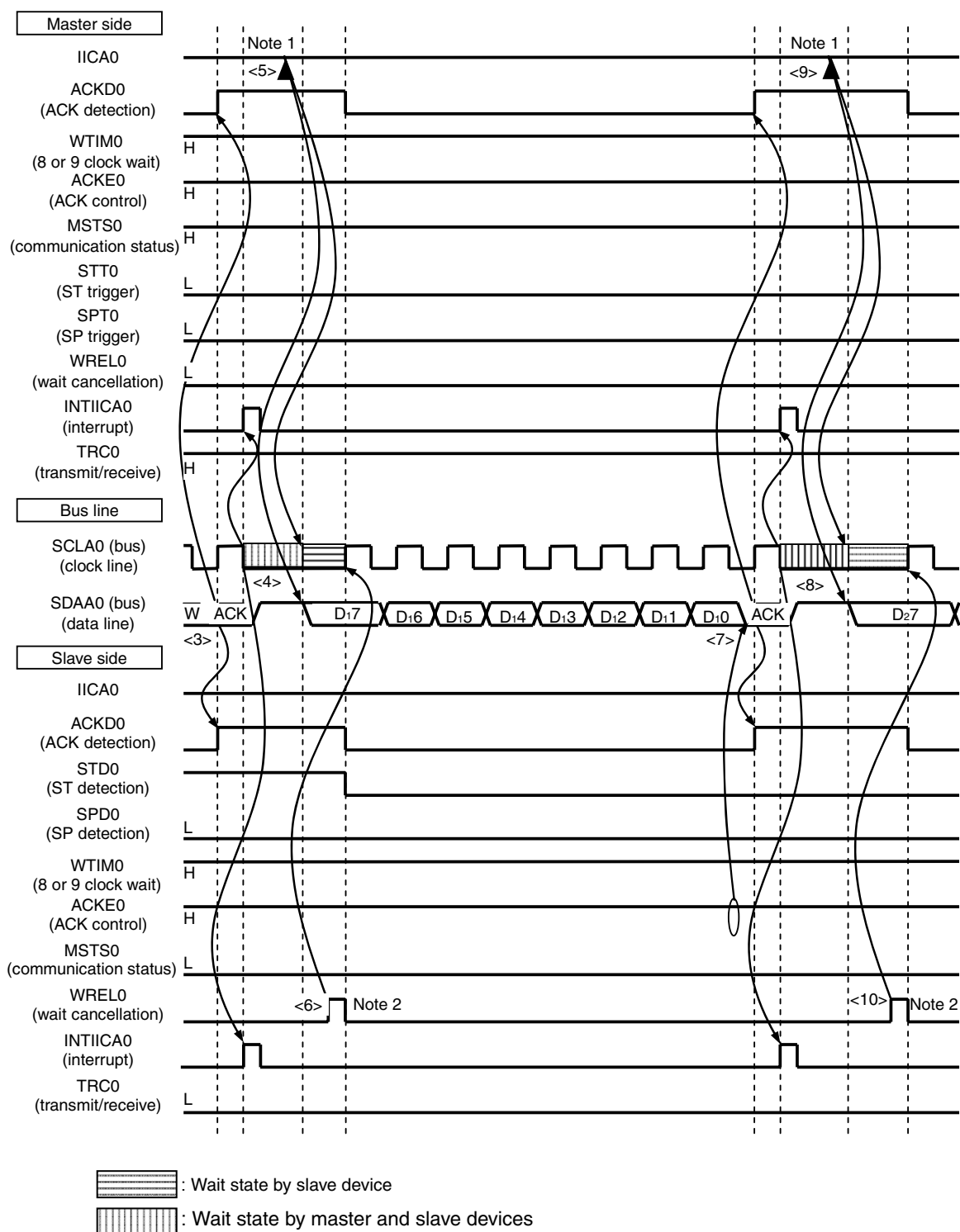
**Note** If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDAA0 = 1). The slave device also does not issue the INTIICA0 interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA0 interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

**Remark** <1> to <15> in Figure 13-32 represent the entire procedure for communicating data using the I<sup>2</sup>C bus. Figure 13-32 (1) Start condition ~ address ~ data shows the processing from <1> to <6>, Figure 13-32 (2) Address ~ data ~ data shows the processing from <3> to <10>, and Figure 13-32 (3) Data ~ data ~ stop condition shows the processing from <7> to <15>.



**Figure 13-32. Example of Master to Slave Communication**  
**(9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (2/4)**

**(2) Address ~ data ~ data**



**Notes** 1. Write data to IICA0, not setting the WREL0 bit, in order to cancel a wait state during transmission by a master device.

2. For releasing wait state during reception of a slave device, write "FFH" to IICA0 or set the WREL0 bit.

The meanings of <3> to <10> in (2) Address ~ data ~ data in Figure 13-32 are explained below.

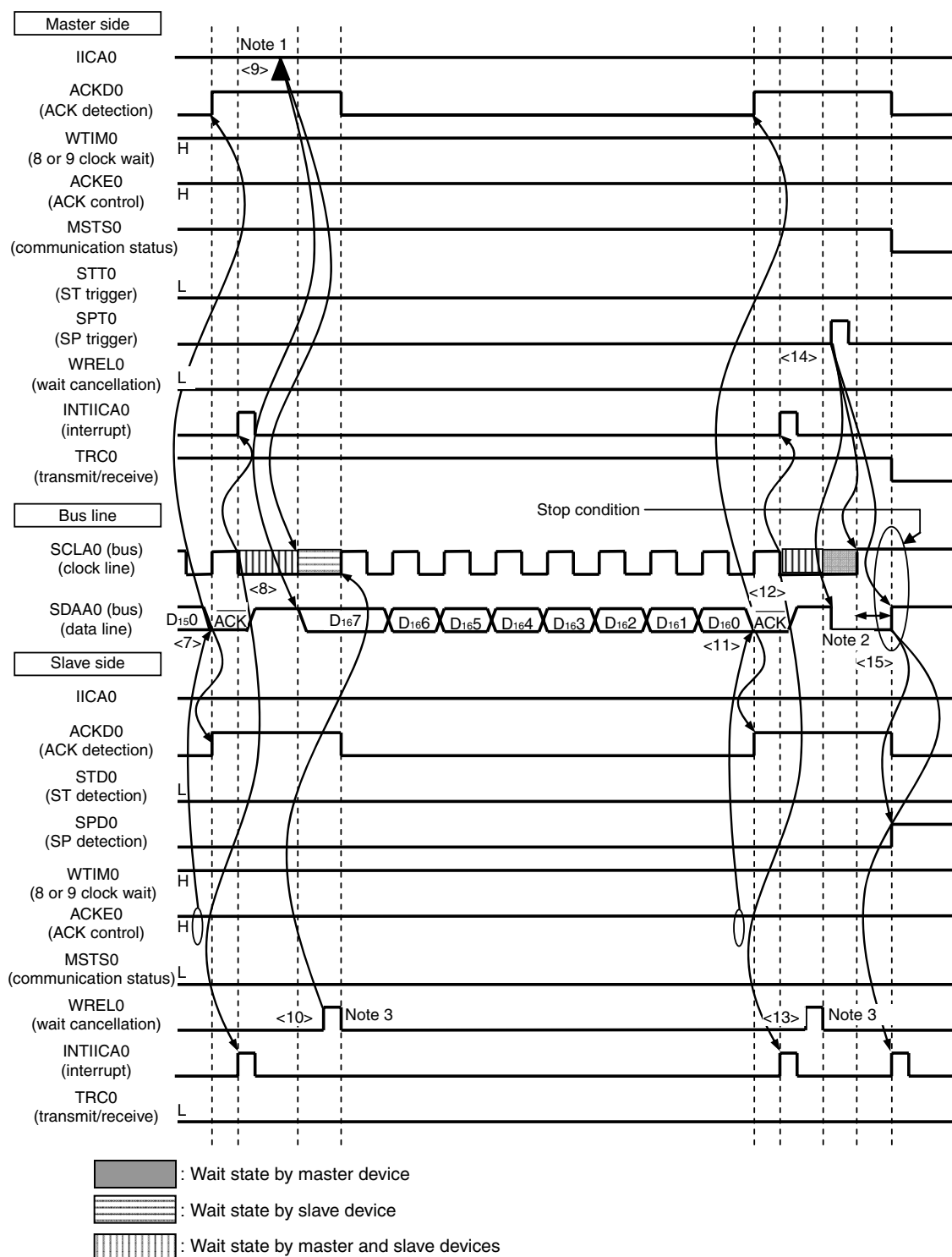
- <3> In the slave device if the address received matches the address (SVA0 value) of a slave device<sup>Note</sup>, that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.
- <4> The master device issues an interrupt (INTIICA0: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a wait status (SCLA0 = 0) and issues an interrupt (INTIICA0: address match)<sup>Note</sup>.
- <5> The master device writes the data to transmit to the IICA shift register 0 (IICA0) and releases the wait status that it set by the master device.
- <6> If the slave device releases the wait status (WREL0 = 1), the master device starts transferring data to the slave device.
- <7> After data transfer is completed, because of ACKEO = 1, the slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.
- <8> The master device and slave device set a wait status (SCLA0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA0: end of transfer).
- <9> The master device writes the data to transmit to the IICA0 register and releases the wait status that it set by the master device.
- <10> The slave device reads the received data and releases the wait status (WREL0 = 1). The master device then starts transferring data to the slave device.

**Note** If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDAA0 = 1). The slave device also does not issue the INTIICA0 interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA0 interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

**Remark** <1> to <15> in Figure 13-32 represent the entire procedure for communicating data using the I<sup>2</sup>C bus. Figure 13-32 (1) Start condition ~ address ~ data shows the processing from <1> to <6>, Figure 13-32 (2) Address ~ data ~ data shows the processing from <3> to <10>, and Figure 13-32 (3) Data ~ data ~ stop condition shows the processing from <7> to <15>.

**Figure 13-32. Example of Master to Slave Communication**  
**(9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (3/4)**

**(3) Data ~ data ~ Stop condition**



- Notes**
1. Write data to IICA0, not setting the WRELO bit, in order to cancel a wait state during transmission by a master device.
  2. Make sure that the time between the rise of the SCLA0 pin signal and the generation of the stop condition after a stop condition has been issued is at least 4.0  $\mu$ s when specifying standard mode and at least 0.6  $\mu$ s when specifying fast mode.
  3. For releasing wait state during reception of a slave device, write "FFH" to IICA0 or set the WRELO bit.

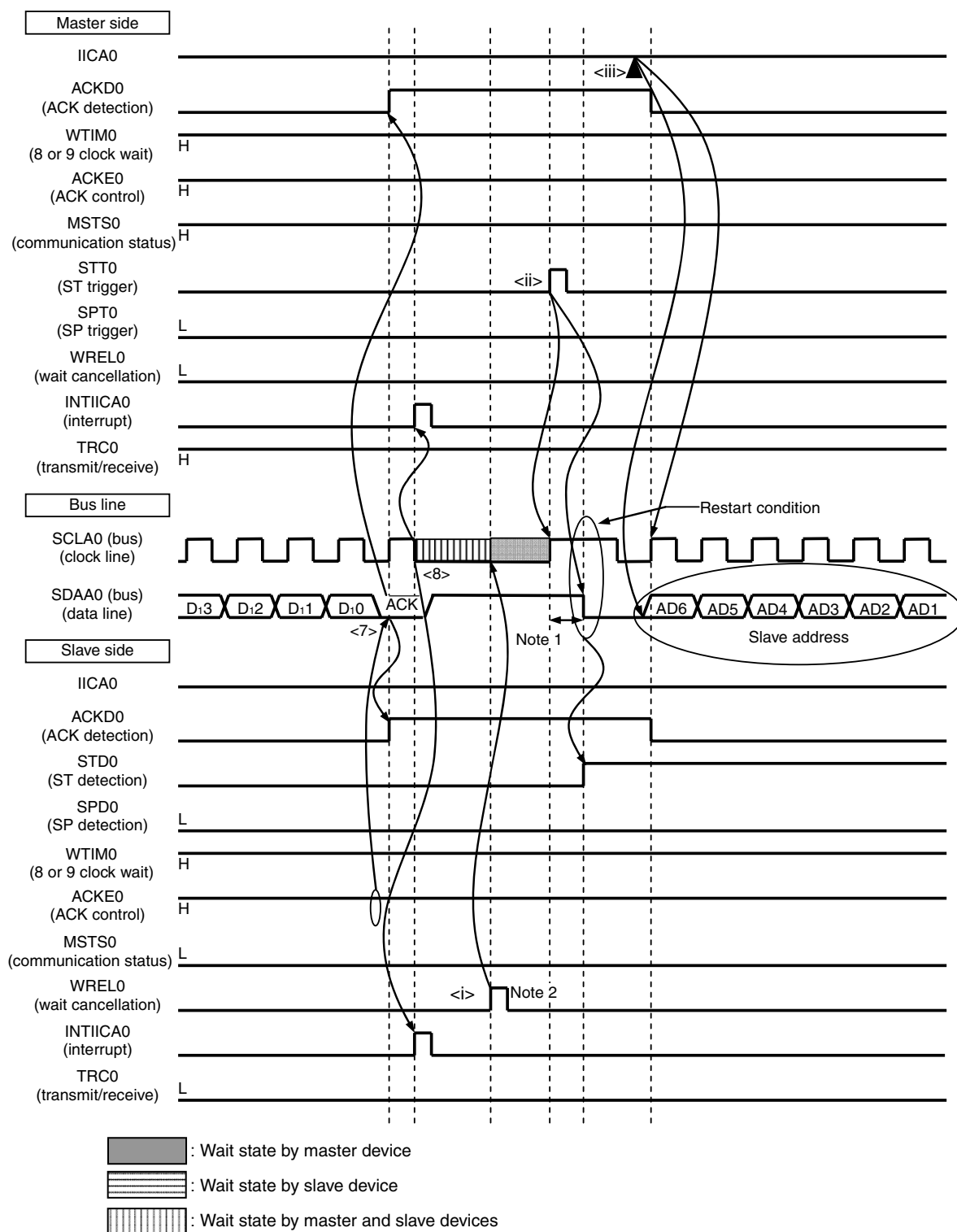
The meanings of <7> to <15> in (3) Data ~ data ~ stop condition in Figure 13-32 are explained below.

- <7> After data transfer is completed, because of ACKE0 = 1, the slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.
- <8> The master device and slave device set a wait status (SCLA0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA0: end of transfer).
- <9> The master device writes the data to transmit to the IICA shift register 0 (IICA0) and releases the wait status that it set by the master device.
- <10> The slave device reads the received data and releases the wait status (WREL0 = 1). The master device then starts transferring data to the slave device.
- <11> When data transfer is complete, the slave device (ACKE0 = 1) sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.
- <12> The master device and slave device set a wait status (SCLA0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA0: end of transfer).
- <13> The slave device reads the received data and releases the wait status (WREL0 = 1).
- <14> By the master device setting a stop condition trigger (SPT0 = 1), the bus data line is cleared (SDAA0 = 0) and the bus clock line is set (SCLA0 = 1). After the stop condition setup time has elapsed, by setting the bus data line (SDAA0 = 1), the stop condition is then generated (i.e. SCLA0 = 1 changes SDAA0 from 0 to 1).
- <15> When a stop condition is generated, the slave device detects the stop condition and issues an interrupt (INTIICA0: stop condition).

**Remark** <1> to <15> in Figure 13-32 represent the entire procedure for communicating data using the I<sup>2</sup>C bus. Figure 13-32 (1) Start condition ~ address ~ data shows the processing from <1> to <6>, Figure 13-32 (2) Address ~ data ~ data shows the processing from <3> to <10>, and Figure 13-32 (3) Data ~ data ~ stop condition shows the processing from <7> to <15>.

**Figure 13-32. Example of Master to Slave Communication**  
**(9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (4/4)**

**(4) Data ~ restart condition ~ address**

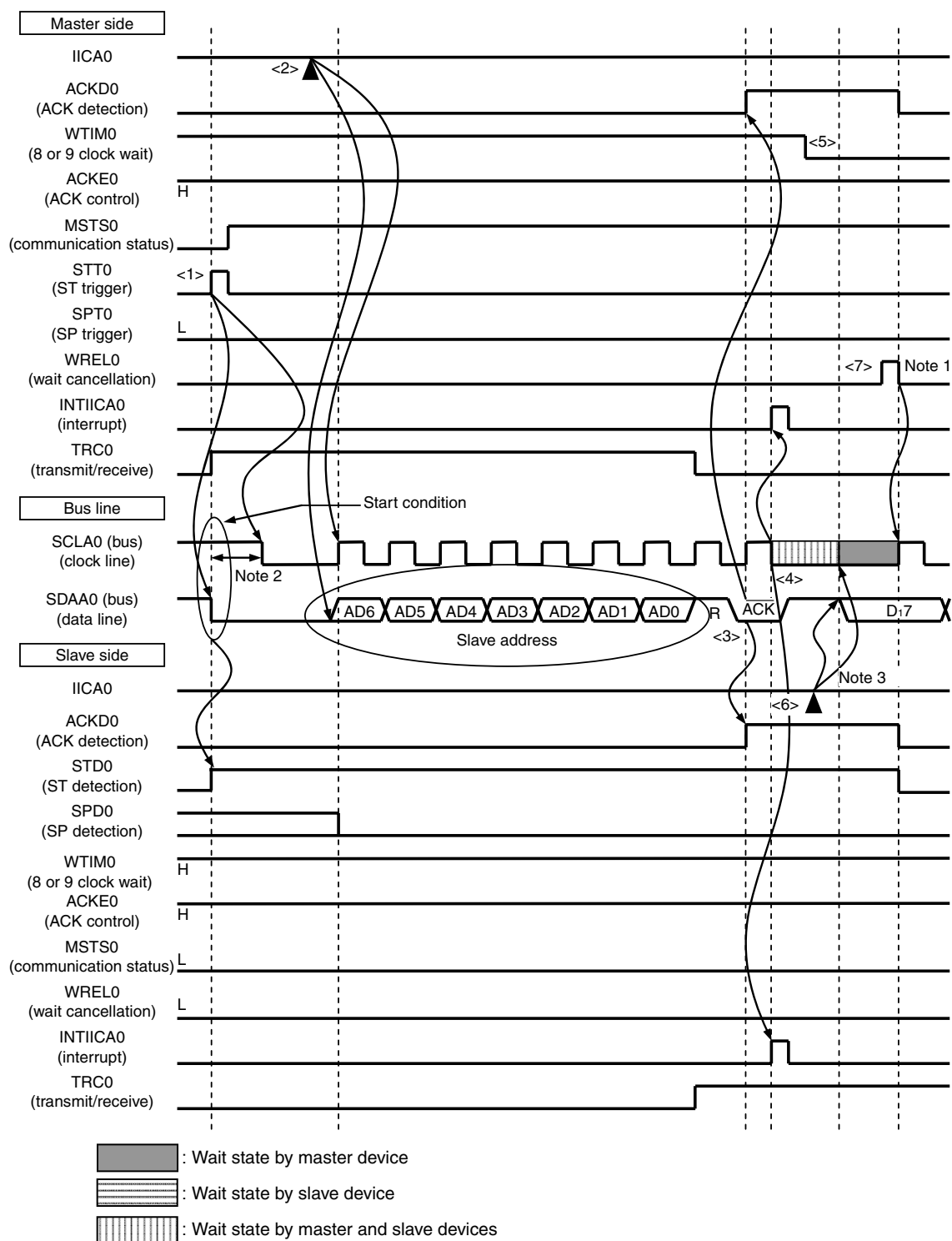


The following describes the operations in Figure 13-32 (4) Data ~ restart condition ~ address. After the operations in steps <7> and <8>, the operations in steps <1> to <3> are performed. These steps return the processing to step <3>, the data transmission step.

- <7> After data transfer is completed, because of  $ACKE0 = 1$ , the slave device sends an ACK by hardware to the master device. The ACK is detected by the master device ( $ACKD0 = 1$ ) at the rising edge of the 9th clock.
- <8> The master device and slave device set a wait status ( $SCLA0 = 0$ ) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt ( $INTIICA0$ : end of transfer).
- <i> The slave device reads the received data and releases the wait status ( $WREL0 = 1$ ).
- <ii> The start condition trigger is set again by the master device ( $STT0 = 1$ ) and a start condition (i.e.  $SCLA0 = 1$  changes  $SDAA0$  from 1 to 0) is generated once the bus clock line goes high ( $SCLA0 = 1$ ) and the bus data line goes low ( $SDAA0 = 0$ ) after the restart condition setup time has elapsed. When the start condition is subsequently detected, the master device is ready to communicate once the bus clock line goes low ( $SCLA0 = 0$ ) after the hold time has elapsed.
- <iii> The master device writing the address + R/W (transmission) to the IICA shift register ( $IICA0$ ) enables the slave address to be transmitted.

**Figure 13-33. Example of Slave to Master Communication**  
**(8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (1/3)**

**(1) Start condition ~ address ~ data**



The meanings of <1> to <7> in (1) Start condition ~ address ~ data in Figure 13-33 are explained below.

- <1> The start condition trigger is set by the master device (STT0 = 1) and a start condition (i.e. SCLA0 = 1 changes SDAA0 from 1 to 0) is generated once the bus data line goes low (SDAA0). When the start condition is subsequently detected, the master device enters the master device communication status (MSTS0 = 1). The master device is ready to communicate once the bus clock line goes low (SCLA0 = 0) after the hold time has elapsed.
- <2> The master device writes the address + R (reception) to the IICA shift register 0 (IICA0) and transmits the slave address.
- <3> In the slave device if the address received matches the address (SVA0 value) of a slave device<sup>Note</sup>, that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.
- <4> The master device issues an interrupt (INTIICA0: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a wait status (SCLA0 = 0) and issues an interrupt (INTIICA0: address match)<sup>Note</sup>.
- <5> The timing at which the master device sets the wait status changes to the 8th clock (WTIM0 = 0).
- <6> The slave device writes the data to transmit to the IICA0 register and releases the wait status that it set by the slave device.
- <7> The master device releases the wait status (WREL0 = 1) and starts transferring data from the slave device to the master device.

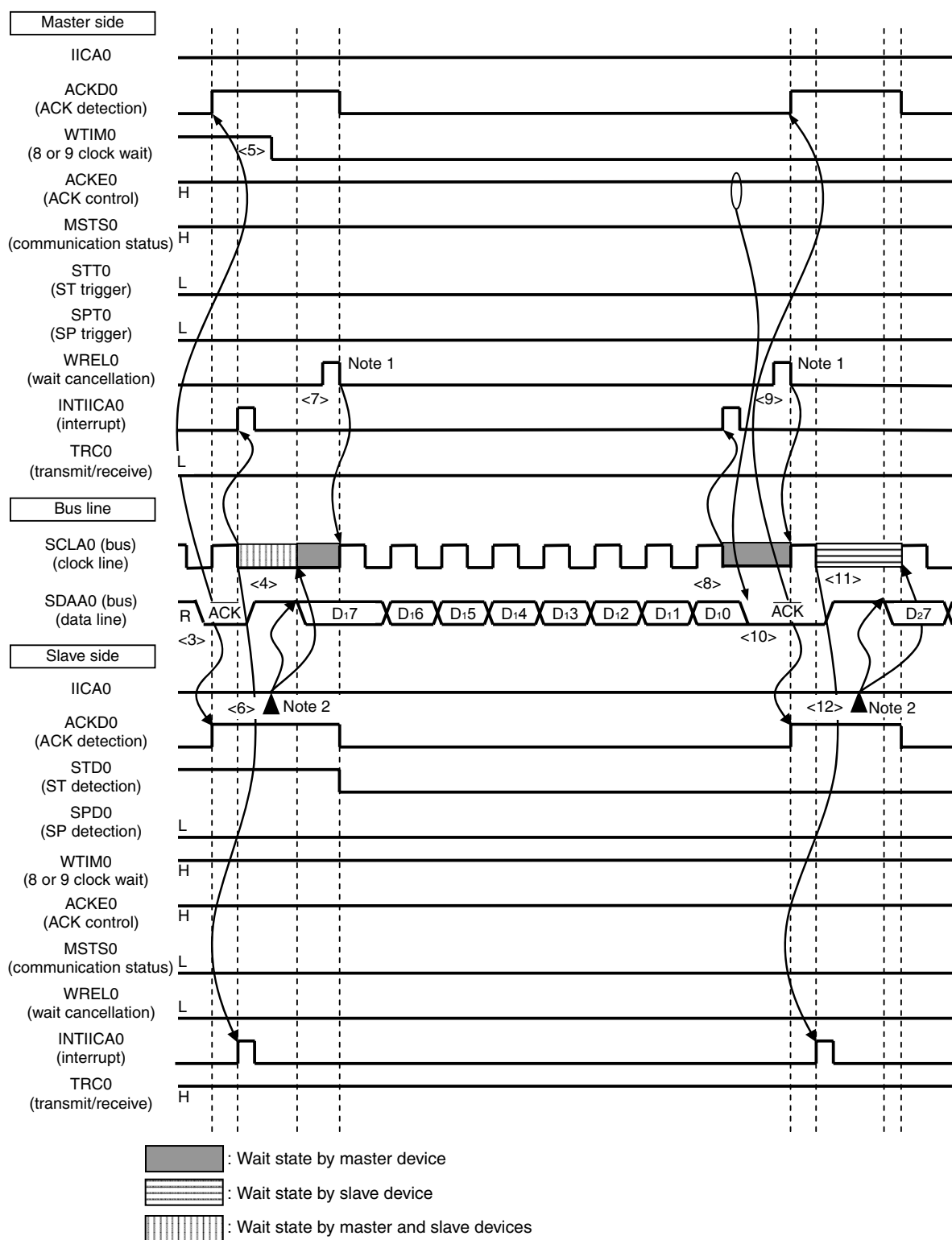
**Note** If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDAA0 = 1). The slave device also does not issue the INTIICA0 interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA0 interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

**Remark** <1> to <19> in Figure 13-33 represent the entire procedure for communicating data using the I<sup>2</sup>C bus. Figure 13-33 (1) Start condition ~ address ~ data shows the processing from <1> to <7>, Figure 13-33 (2) Address ~ data ~ data shows the processing from <3> to <12>, and Figure 13-33 (3) Data ~ data ~ stop condition shows the processing from <8> to <19>.



**Figure 13-33. Example of Slave to Master Communication**  
**(8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (2/3)**

**(2) Address ~ data ~ data**



- Notes**
- For releasing wait state during reception of a master device, write "FFH" to IICA0 or set the WREL0 bit.
  - Write data to IICA0, not setting the WREL0 bit, in order to cancel a wait state during transmission by a slave device.

The meanings of <3> to <12> in (2) Address ~ data ~ data in Figure 13-33 are explained below.

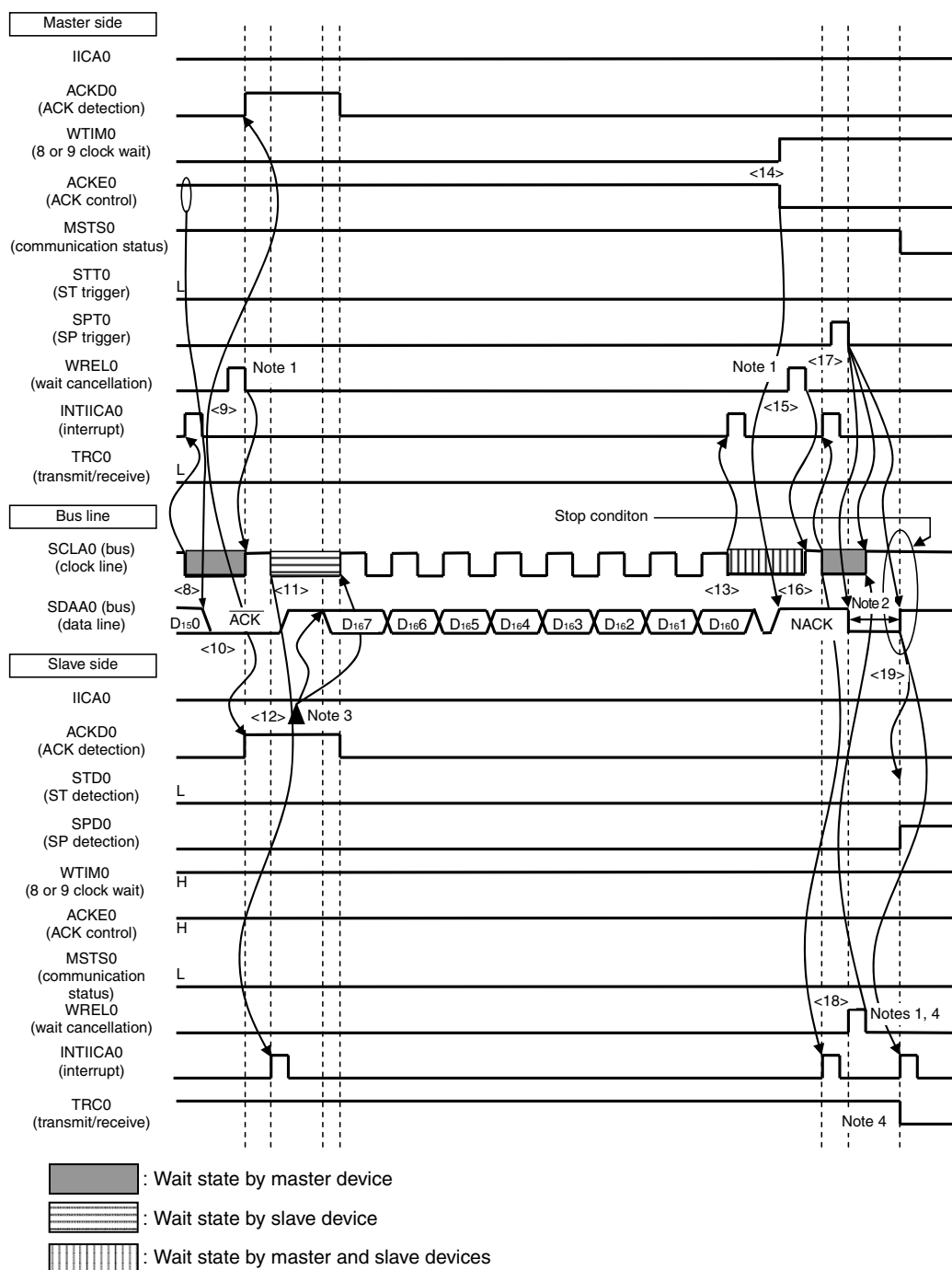
- <3> In the slave device if the address received matches the address (SVA0 value) of a slave device<sup>Note</sup>, that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.
- <4> The master device issues an interrupt (INTIICA0: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a wait status (SCLA0 = 0) and issues an interrupt (INTIICA0: address match)<sup>Note</sup>.
- <5> The master device changes the timing of the wait status to the 8th clock (WTIM0 = 0).
- <6> The slave device writes the data to transmit to the IICA shift register 0 (IICA0) and releases the wait status that it set by the slave device.
- <7> The master device releases the wait status (WREL0 = 1) and starts transferring data from the slave device to the master device.
- <8> The master device sets a wait status (SCLA0 = 0) at the falling edge of the 8th clock, and issues an interrupt (INTIICA0: end of transfer). Because of ACKE0 = 1 in the master device, the master device then sends an ACK by hardware to the slave device.
- <9> The master device reads the received data and releases the wait status (WREL0 = 1).
- <10> The ACK is detected by the slave device (ACKD0 = 1) at the rising edge of the 9th clock.
- <11> The slave device set a wait status (SCLA0 = 0) at the falling edge of the 9th clock, and the slave device issue an interrupt (INTIICA0: end of transfer).
- <12> By the slave device writing the data to transmit to the IICA0 register, the wait status set by the slave device is released. The slave device then starts transferring data to the master device.

**Note** If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDAA0 = 1). The slave device also does not issue the INTIICA0 interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA0 interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

**Remark** <1> to <19> in Figure 13-33 represent the entire procedure for communicating data using the I<sup>2</sup>C bus. Figure 13-33 (1) Start condition ~ address ~ data shows the processing from <1> to <7>, Figure 13-33 (2) Address ~ data ~ data shows the processing from <3> to <12>, and Figure 13-33 (3) Data ~ data ~ stop condition shows the processing from <8> to <19>.

**Figure 13-33. Example of Slave to Master Communication  
(8-Clock and 9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (3/3)**

**(3) Data ~ data ~ stop condition**



- Notes 1.** To cancel a wait state, write “FFH” to IICA0 or set the WREL0 bit.
- 2.** Make sure that the time between the rise of the SCLA0 pin signal and the generation of the stop condition after a stop condition has been issued is at least 4.0  $\mu$ s when specifying standard mode and at least 0.6  $\mu$ s when specifying fast mode.
- 3.** Write data to IICA0, not setting the WREL0 bit, in order to cancel a wait state during transmission by a slave device.
- 4.** If a wait state during transmission by a slave device is canceled by setting the WREL0 bit, the TRC0 bit will be cleared.

The meanings of <8> to <19> in (3) Data ~ data ~ stop condition in Figure 13-33 are explained below.

- <8> The master device sets a wait status (SCLA0 = 0) at the falling edge of the 8th clock, and issues an interrupt (INTIICA0: end of transfer). Because of ACKE0 = 0 in the master device, the master device then sends an ACK by hardware to the slave device.
- <9> The master device reads the received data and releases the wait status (WREL0 = 1).
- <10> The ACK is detected by the slave device (ACKD0 = 1) at the rising edge of the 9th clock.
- <11> The slave device set a wait status (SCLA0 = 0) at the falling edge of the 9th clock, and the slave device issue an interrupt (INTIICA0: end of transfer).
- <12> By the slave device writing the data to transmit to the IICA register, the wait status set by the slave device is released. The slave device then starts transferring data to the master device.
- <13> The master device issues an interrupt (INTIICA0: end of transfer) at the falling edge of the 8th clock, and sets a wait status (SCLA0 = 0). Because ACK control (ACKE0 = 1) is performed, the bus data line is at the low level (SDAA0 = 0) at this stage.
- <14> The master device sets NACK as the response (ACKE0 = 0) and changes the timing at which it sets the wait status to the 9th clock (WTIM0 = 1).
- <15> If the master device releases the wait status (WREL0 = 1), the slave device detects the NACK (ACKD0 = 0) at the rising edge of the 9th clock.
- <16> The master device and slave device set a wait status (SCLA0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA0: end of transfer).
- <17> When the master device issues a stop condition (SPT0 = 1), the bus data line is cleared (SDAA0 = 0) and the master device releases the wait status. The master device then waits until the bus clock line is set (SCLA0 = 1).
- <18> The slave device acknowledges the NACK, halts transmission, and releases the wait status (WREL0 = 1) to end communication. Once the slave device releases the wait status, the bus clock line is set (SCLA0 = 1).
- <19> Once the master device recognizes that the bus clock line is set (SCLA0 = 1) and after the stop condition setup time has elapsed, the master device sets the bus data line (SDAA0 = 1) and issues a stop condition (i.e. SCLA0 =1 changes SDAA0 from 0 to 1). The slave device detects the generated stop condition and slave device issue an interrupt (INTIICA0: stop condition).

**Remark** <1> to <19> in Figure 13-33 represent the entire procedure for communicating data using the I<sup>2</sup>C bus. Figure 13-33 (1) Start condition ~ address ~ data shows the processing from <1> to <7>, Figure 13-33 (2) Address ~ data ~ data shows the processing from <3> to <12>, and Figure 13-33 (3) Data ~ data ~ stop condition shows the processing from <8> to <19>.

## CHAPTER 14 LCD CONTROLLER/DRIVER

The number of LCD display function pins of the RL78/L12 differs depending on the product. The following table shows the number of pins of each product.

Table 14-1. Number of LCD Display Function Pins of Each Product (1/3)

## (a) 32-pin and 44-pin products

| Item                          | RL78/L12                                               |       |       |        |        |        |        |        |                                                                             |       |       |        |        |        |        |        |
|-------------------------------|--------------------------------------------------------|-------|-------|--------|--------|--------|--------|--------|-----------------------------------------------------------------------------|-------|-------|--------|--------|--------|--------|--------|
|                               | 32 pins (R5F10RBx (x = C, A, 8))                       |       |       |        |        |        |        |        | 44 pins (R5F10RFx (x = C, A, 8))                                            |       |       |        |        |        |        |        |
| LCD controller/driver         | Segment signal outputs: 13<br>Common signal outputs: 4 |       |       |        |        |        |        |        | Segment signal outputs: 22 (18) <sup>Note</sup><br>Common signal outputs: 8 |       |       |        |        |        |        |        |
| Multiplexed I/O port          | Bit 7                                                  | Bit 6 | Bit 5 | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  | Bit 7                                                                       | Bit 6 | Bit 5 | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  |
| P1                            | SEG 6                                                  | SEG 5 | SEG 4 | SEG 32 | SEG 31 | SEG 30 | SEG 29 | SEG 28 | SEG 6                                                                       | SEG 5 | SEG 4 | SEG 32 | SEG 31 | SEG 30 | SEG 29 | SEG 28 |
| P3                            | —                                                      | —     | —     | —      | —      | —      | —      | SEG 19 | —                                                                           | —     | —     | —      | —      | SEG 17 | SEG 18 | SEG 19 |
| P4                            | —                                                      | —     | —     | —      | —      | —      | —      | —      | —                                                                           | —     | —     | —      | —      | —      | —      | —      |
| P5                            | —                                                      | —     | —     | —      | —      | —      | —      | —      | —                                                                           | —     | —     | —      | —      | —      | —      | —      |
| P6                            | —                                                      | —     | —     | —      | —      | —      | SEG 20 | SEG 21 | —                                                                           | —     | —     | —      | —      | —      | SEG 20 | SEG 21 |
| P7                            | —                                                      | —     | —     | —      | —      | —      | —      | —      | —                                                                           | —     | —     | —      | —      | —      | —      | —      |
| P12                           | —                                                      | —     | —     | —      | —      | —      | —      | —      | —                                                                           | —     | —     | —      | —      | —      | —      | SEG 25 |
| P14                           | —                                                      | —     | —     | —      | —      | —      | —      | SEG 27 | —                                                                           | —     | —     | —      | SEG 34 | SEG 33 | SEG 26 | SEG 27 |
| Not multiplexed with I/O port |                                                        |       |       |        |        |        |        |        |                                                                             |       |       |        |        |        |        |        |
| COM4                          | COMEXP/SEG0                                            |       |       |        |        |        |        |        | COMEXP/SEG0                                                                 |       |       |        |        |        |        |        |
| COM5                          | —                                                      |       |       |        |        |        |        |        | SEG1                                                                        |       |       |        |        |        |        |        |
| COM6                          | —                                                      |       |       |        |        |        |        |        | SEG2                                                                        |       |       |        |        |        |        |        |
| COM7                          | —                                                      |       |       |        |        |        |        |        | SEG3                                                                        |       |       |        |        |        |        |        |

**Note** ( ) indicates the number of signal output pins when 8 com is used.

Table 14-1. Number of LCD Display Function Pins of Each Product (2/3)

## (b) 48-pin and 52-pin products

| Item                          | RL78/L12                                                                    |       |       |        |        |        |        |        |                                                                             |       |        |        |        |        |        |        |
|-------------------------------|-----------------------------------------------------------------------------|-------|-------|--------|--------|--------|--------|--------|-----------------------------------------------------------------------------|-------|--------|--------|--------|--------|--------|--------|
|                               | 48 pins (R5F10RGx (x = C, A, 8))                                            |       |       |        |        |        |        |        | 52 pins (R5F10RJx (x = C, A, 8))                                            |       |        |        |        |        |        |        |
| LCD controller/driver         | Segment signal outputs: 26 (22) <sup>Note</sup><br>Common signal outputs: 8 |       |       |        |        |        |        |        | Segment signal outputs: 30 (26) <sup>Note</sup><br>Common signal outputs: 8 |       |        |        |        |        |        |        |
| Multiplexed I/O port          | Bit 7                                                                       | Bit 6 | Bit 5 | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  | Bit 7                                                                       | Bit 6 | Bit 5  | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  |
| P1                            | SEG 6                                                                       | SEG 5 | SEG 4 | SEG 32 | SEG 31 | SEG 30 | SEG 29 | SEG 28 | SEG 6                                                                       | SEG 5 | SEG 4  | SEG 32 | SEG 31 | SEG 30 | SEG 29 | SEG 28 |
| P3                            | —                                                                           | —     | —     | —      | —      | SEG 17 | SEG 18 | SEG 19 | —                                                                           | —     | —      | —      | —      | SEG 17 | SEG 18 | SEG 19 |
| P4                            | —                                                                           | —     | —     | —      | —      | —      | SEG 24 | —      | —                                                                           | —     | —      | —      | —      | SEG 23 | SEG 24 | —      |
| P5                            | —                                                                           | —     | —     | —      | —      | —      | —      | SEG 7  | —                                                                           | —     | —      | —      | —      | —      | SEG 8  | SEG 7  |
| P6                            | —                                                                           | —     | —     | —      | —      | —      | SEG 20 | SEG 21 | —                                                                           | —     | —      | —      | —      | —      | SEG 20 | SEG 21 |
| P7                            | —                                                                           | —     | —     | —      | —      | —      | —      | SEG 16 | —                                                                           | —     | —      | —      | —      | —      | SEG 15 | SEG 16 |
| P12                           | —                                                                           | —     | —     | —      | —      | —      | —      | SEG 25 | —                                                                           | —     | —      | —      | —      | —      | —      | SEG 25 |
| P14                           | —                                                                           | —     | —     | SEG 35 | SEG 34 | SEG 33 | SEG 26 | SEG 27 | —                                                                           | —     | SEG 36 | SEG 35 | SEG 34 | SEG 33 | SEG 26 | SEG 27 |
| Not multiplexed with I/O port |                                                                             |       |       |        |        |        |        |        |                                                                             |       |        |        |        |        |        |        |
| COM4                          | COMEXP/SEG0                                                                 |       |       |        |        |        |        |        | COMEXP/SEG0                                                                 |       |        |        |        |        |        |        |
| COM5                          | SEG1                                                                        |       |       |        |        |        |        |        | SEG1                                                                        |       |        |        |        |        |        |        |
| COM6                          | SEG2                                                                        |       |       |        |        |        |        |        | SEG2                                                                        |       |        |        |        |        |        |        |
| COM7                          | SEG3                                                                        |       |       |        |        |        |        |        | SEG3                                                                        |       |        |        |        |        |        |        |

**Note** ( ) indicates the number of signal output pins when 8 com is used.

Table 14-1. Number of LCD Display Function Pins of Each Product (3/3)

## (c) 64-pin products

| Item                          | RL78/L12                                                    |        |        |        |        |        |        |        |
|-------------------------------|-------------------------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
|                               | 64 pins                                                     |        |        |        |        |        |        |        |
| LCD controller/driver         | Segment signal outputs: 39 (35)<br>Common signal outputs: 8 |        |        |        |        |        |        |        |
| Multiplexed I/O port          | Bit 7                                                       | Bit 6  | Bit 5  | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  |
| P1                            | SEG 6                                                       | SEG 5  | SEG 4  | SEG 32 | SEG 31 | SEG 30 | SEG 29 | SEG 28 |
| P3                            | –                                                           | –      | –      | –      | –      | SEG 17 | SEG 18 | SEG 19 |
| P4                            | –                                                           | –      | –      | –      | SEG 22 | SEG 23 | SEG 24 | –      |
| P5                            | –                                                           | –      | –      | SEG 11 | SEG 10 | SEG 9  | SEG 8  | SEG 7  |
| P6                            | –                                                           | –      | –      | –      | –      | –      | SEG 20 | SEG 21 |
| P7                            | –                                                           | –      | –      | SEG 12 | SEG 13 | SEG 14 | SEG 15 | SEG 16 |
| P12                           | –                                                           | –      | –      | –      | –      | –      | –      | SEG 25 |
| P14                           | SEG 38                                                      | SEG 37 | SEG 36 | SEG 35 | SEG 34 | SEG 33 | SEG 26 | SEG 27 |
| Not multiplexed with I/O port |                                                             |        |        |        |        |        |        |        |
| COM4                          | COMEXP/SEG0                                                 |        |        |        |        |        |        |        |
| COM5                          | SEG1                                                        |        |        |        |        |        |        |        |
| COM6                          | SEG2                                                        |        |        |        |        |        |        |        |
| COM7                          | SEG3                                                        |        |        |        |        |        |        |        |

### 14.1 Functions of LCD Controller/Driver

The functions of the LCD controller/driver in the RL78/L12 microcontrollers are as follows.

- (1) Normal liquid crystal waveform (waveform A or B) and memory-type liquid crystal waveform selectable
- (2) The LCD driver voltage generator can switch internal voltage boosting method, capacitor split method, and external resistance division method.
- (3) Automatic output of segment and common signals based on automatic display data register read
- (4) The reference voltage to be generated when operating the voltage boost circuit can be selected from 16 steps (contrast adjustment).
- (5) LCD blinking and display selectable<sup>Note</sup>
- (6) Interrupt generated at completion of display of memory-type liquid crystal waveform

**Note** Normal liquid crystal waveform only.

However, selecting  $f_{IL}$  as the LCD source clock ( $f_{LCD}$ ) is prohibited.

Table 14-2 lists the maximum number of pixels that can be displayed in each display mode.

**Table 14-2. Maximum Number of Pixels (1/5)**

**(a) 32-pin products**

| Drive Waveform for LCD Driver               | LCD Driver Voltage Generator                                             | Bias Mode | Number of Time Slices | Maximum Number of Pixels                  |
|---------------------------------------------|--------------------------------------------------------------------------|-----------|-----------------------|-------------------------------------------|
| Normal liquid crystal waveform (waveform A) | External resistance division                                             | –         | Static                | 13 (13 segment signals, 1 common signal)  |
|                                             |                                                                          | 1/2       | 2                     | 26 (13 segment signals, 2 common signals) |
|                                             |                                                                          |           | 3                     | 39 (13 segment signals, 3 common signals) |
|                                             |                                                                          | 1/3       | 3                     |                                           |
|                                             |                                                                          |           | 4                     | 52 (13 segment signals, 4 common signals) |
|                                             | Internal voltage boosting, capacitor split                               | 1/3       | 3                     | 39 (13 segment signals, 3 common signals) |
|                                             |                                                                          |           | 4                     | 52 (13 segment signals, 4 common signals) |
| Normal liquid crystal waveform (waveform B) | External resistance division, internal voltage boosting, capacitor split | 1/3       | 4                     |                                           |
| Memory-type liquid crystal waveform         | External resistance division                                             | 1/3       | 3                     | 39 (13 segment signals, 3 common signals) |
|                                             |                                                                          |           | 4                     | 52 (13 segment signals, 4 common signals) |



Table 14-2. Maximum Number of Pixels (2/5)

## (b) 44-pin products

| Drive Waveform for LCD Driver               | LCD Driver Voltage Generator                            | Bias Mode | Number of Time Slices | Maximum Number of Pixels                   |
|---------------------------------------------|---------------------------------------------------------|-----------|-----------------------|--------------------------------------------|
| Normal liquid crystal waveform (waveform A) | External resistance division                            | —         | Static                | 22 (22 segment signals, 1 common signal)   |
|                                             |                                                         | 1/2       | 2                     | 44 (22 segment signals, 2 common signals)  |
|                                             |                                                         |           | 3                     | 66 (22 segment signals, 3 common signals)  |
|                                             |                                                         | 1/3       | 3                     |                                            |
|                                             |                                                         |           | 4                     | 88 (22 segment signals, 4 common signals)  |
|                                             |                                                         | 1/4       | 8                     | 144 (18 segment signals, 8 common signals) |
|                                             | Internal voltage boosting                               | 1/3       | 3                     | 66 (22 segment signals, 3 common signals)  |
|                                             |                                                         |           | 4                     | 88 (22 segment signals, 4 common signals)  |
|                                             |                                                         | 1/4       | 8                     | 144 (18 segment signals, 8 common signals) |
|                                             | Capacitor split                                         | 1/3       | 3                     | 66 (22 segment signals, 3 common signals)  |
|                                             |                                                         |           | 4                     | 88 (22 segment signals, 4 common signals)  |
| Normal liquid crystal waveform (waveform B) | External resistance division, internal voltage boosting | 1/3       | 4                     |                                            |
|                                             |                                                         | 1/4       | 8                     | 176 (22 segment signals, 8 common signals) |
|                                             | Capacitor split                                         | 1/3       | 4                     | 88 (22 segment signals, 4 common signals)  |
| Memory-type liquid crystal waveform         | External resistance division                            | 1/3       | 3                     | 66 (22 segment signals, 3 common signals)  |
|                                             |                                                         |           | 4                     | 88 (22 segment signals, 4 common signals)  |

Table 14-2. Maximum Number of Pixels (3/5)

## (c) 48-pin products

| Drive Waveform for LCD Driver               | LCD Driver Voltage Generator                            | Bias Mode | Number of Time Slices | Maximum Number of Pixels                   |
|---------------------------------------------|---------------------------------------------------------|-----------|-----------------------|--------------------------------------------|
| Normal liquid crystal waveform (waveform A) | External resistance division                            | —         | Static                | 26 (26 segment signals, 1 common signal)   |
|                                             |                                                         | 1/2       | 2                     | 52 (26 segment signals, 2 common signals)  |
|                                             |                                                         |           | 3                     | 78 (26 segment signals, 3 common signals)  |
|                                             |                                                         | 1/3       | 3                     |                                            |
|                                             |                                                         |           | 4                     | 104 (26 segment signals, 4 common signals) |
|                                             |                                                         | 1/4       | 8                     | 176 (22 segment signals, 8 common signals) |
|                                             | Internal voltage boosting                               | 1/3       | 3                     | 78 (26 segment signals, 3 common signals)  |
|                                             |                                                         |           | 4                     | 104 (26 segment signals, 4 common signals) |
|                                             |                                                         | 1/4       | 8                     | 176 (22 segment signals, 8 common signals) |
|                                             | Capacitor split                                         | 1/3       | 3                     | 78 (26 segment signals, 3 common signals)  |
|                                             |                                                         |           | 4                     | 104 (26 segment signals, 4 common signals) |
| Normal liquid crystal waveform (waveform B) | External resistance division, internal voltage boosting | 1/3       | 4                     |                                            |
|                                             |                                                         | 1/4       | 8                     | 176 (22 segment signals, 8 common signals) |
|                                             | Capacitor split                                         | 1/3       | 4                     | 104 (26 segment signals, 4 common signals) |
| Memory-type liquid crystal waveform         | External resistance division                            | 1/3       | 3                     | 78 (26 segment signals, 3 common signals)  |
|                                             |                                                         |           | 4                     | 104 (26 segment signals, 4 common signals) |

Table 14-2. Maximum Number of Pixels (4/5)

## (d) 52-pin products

| Drive Waveform for LCD Driver               | LCD Driver Voltage Generator                            | Bias Mode | Number of Time Slices | Maximum Number of Pixels                   |
|---------------------------------------------|---------------------------------------------------------|-----------|-----------------------|--------------------------------------------|
| Normal liquid crystal waveform (waveform A) | External resistance division                            | —         | Static                | 30 (30 segment signals, 1 common signal)   |
|                                             |                                                         | 1/2       | 2                     | 60 (30 segment signals, 2 common signals)  |
|                                             |                                                         |           | 3                     | 90 (30 segment signals, 3 common signals)  |
|                                             |                                                         | 1/3       | 3                     |                                            |
|                                             |                                                         |           | 4                     | 120 (30 segment signals, 4 common signals) |
|                                             |                                                         | 1/4       | 8                     | 208 (26 segment signals, 8 common signals) |
|                                             | Internal voltage boosting                               | 1/3       | 3                     | 90 (30 segment signals, 3 common signals)  |
|                                             |                                                         |           | 4                     | 120 (30 segment signals, 4 common signals) |
|                                             |                                                         | 1/4       | 8                     | 208 (26 segment signals, 8 common signals) |
|                                             | Capacitor split                                         | 1/3       | 3                     | 90 (30 segment signals, 3 common signals)  |
|                                             |                                                         |           | 4                     | 120 (30 segment signals, 4 common signals) |
| Normal liquid crystal waveform (waveform B) | External resistance division, internal voltage boosting | 1/3       | 4                     |                                            |
|                                             |                                                         | 1/4       | 8                     | 208 (26 segment signals, 8 common signals) |
|                                             | Capacitor split                                         | 1/3       | 4                     | 120 (30 segment signals, 4 common signals) |
| Memory-type liquid crystal waveform         | External resistance division                            | 1/3       | 3                     | 90 (30 segment signals, 3 common signals)  |
|                                             |                                                         |           | 4                     | 120 (30 segment signals, 4 common signals) |

Table 14-2. Maximum Number of Pixels (5/5)

## (e) 64-pin products

| Drive Waveform for LCD Driver               | LCD Driver Voltage Generator                            | Bias Mode | Number of Time Slices | Maximum Number of Pixels                   |
|---------------------------------------------|---------------------------------------------------------|-----------|-----------------------|--------------------------------------------|
| Normal liquid crystal waveform (waveform A) | External resistance division                            | —         | Static                | 39 (39 segment signals, 1 common signal)   |
|                                             |                                                         | 1/2       | 2                     | 78 (39 segment signals, 2 common signals)  |
|                                             |                                                         |           | 3                     | 117 (39 segment signals, 3 common signals) |
|                                             |                                                         | 1/3       | 3                     |                                            |
|                                             |                                                         |           | 4                     | 156 (39 segment signals, 4 common signals) |
|                                             |                                                         | 1/4       | 8                     | 280 (35 segment signals, 8 common signals) |
|                                             | Internal voltage boosting                               | 1/3       | 3                     | 117 (39 segment signals, 3 common signals) |
|                                             |                                                         |           | 4                     | 156 (39 segment signals, 4 common signals) |
|                                             |                                                         | 1/4       | 8                     | 280 (35 segment signals, 8 common signals) |
|                                             | Capacitor split                                         | 1/3       | 3                     | 117 (39 segment signals, 3 common signals) |
|                                             |                                                         |           | 4                     | 156 (39 segment signals, 4 common signals) |
| Normal liquid crystal waveform (waveform B) | External resistance division, internal voltage boosting | 1/3       | 4                     |                                            |
|                                             |                                                         | 1/4       | 8                     | 280 (35 segment signals, 8 common signals) |
|                                             | Capacitor split                                         | 1/3       | 4                     | 156 (39 segment signals, 4 common signals) |
| Memory-type liquid crystal waveform         | External resistance division                            | 1/3       | 3                     | 117 (39 segment signals, 3 common signals) |
|                                             |                                                         |           | 4                     | 156 (39 segment signals, 4 common signals) |

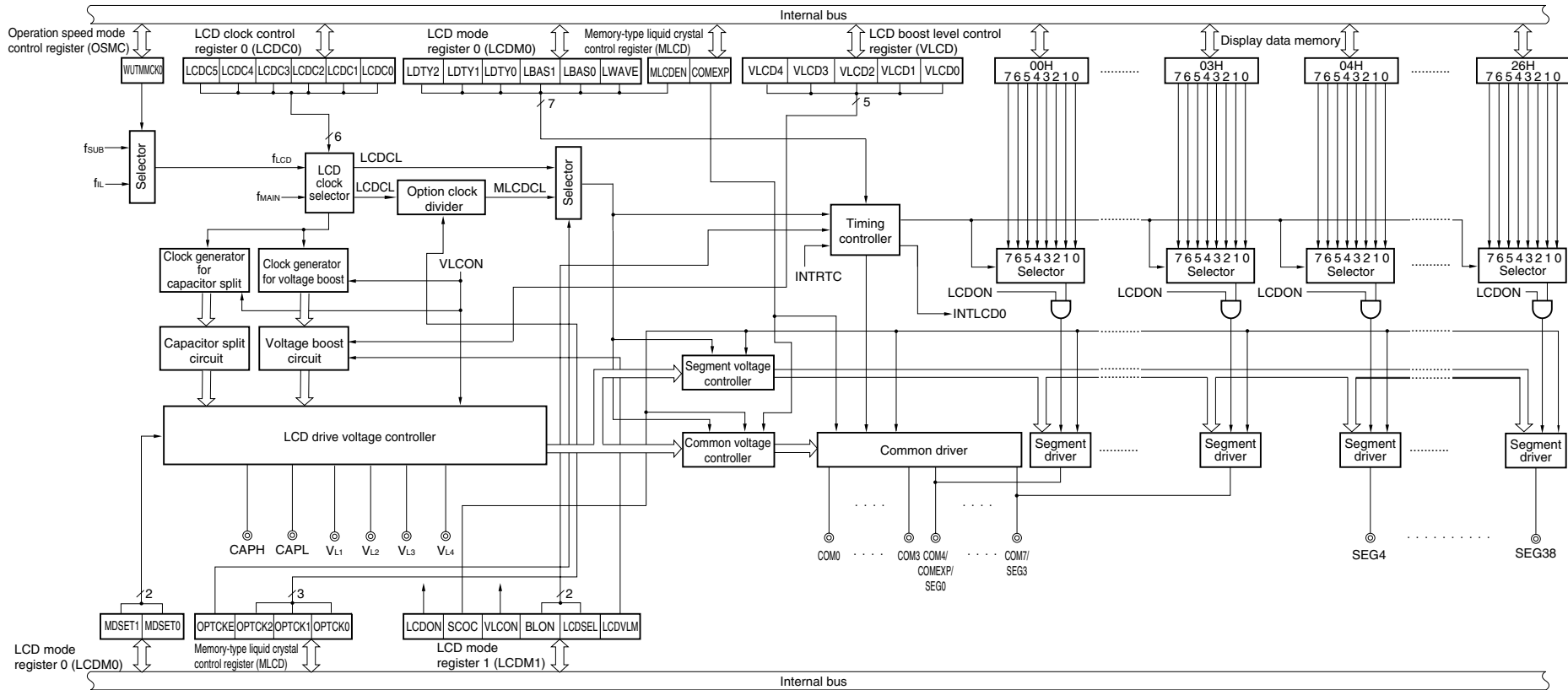
## 14.2 Configuration of LCD Controller/Driver

The LCD controller/driver consists of the following hardware.

**Table 14-3. Configuration of LCD Controller/Driver**

| Item              | Configuration                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Control registers | Peripheral enable register 0 (PER0)<br>LCD mode register 0 (LCDM0)<br>LCD mode register 1 (LCDM1)<br>Operation speed mode control register (OSMC)<br>LCD clock control register 0 (LCDC0)<br>Memory-type liquid crystal control register (MLCD)<br>LCD boost level control register (VLCD)<br>LCD input switch control register (ISCLCD)<br>LCD port function registers 0 to 4 (PFSEG0 to PFSEG4)<br>Port mode registers 1, 3 to 7, 12, 14 (PM1, PM3 to PM7, PM12, PM14) |

Figure 14-1. Block Diagram of LCD Controller/Driver



<R>

### 14.3 Registers Controlling LCD Controller/Driver

The following ten registers are used to control the LCD controller/driver.

- Peripheral enable register 0 (PER0)
- LCD mode register 0 (LCDM0)
- LCD mode register 1 (LCDM1)
- Operation speed mode control register (OSMC)
- LCD clock control register 0 (LCDC0)
- Memory-type liquid crystal control register (MLCD)
- LCD boost level control register (VLCD)
- LCD input switch control register (ISCLCD)
- LCD port function registers 0 to 4 (PFSEG0 to PFSEG4)
- Port mode registers 1, 3 to 7, 12, 14 (PM1, PM3 to PM7, PM12, PM14)

### 14.3.1 Peripheral enable register 0 (PER0)

PER0 enables or disables supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When the LCD controller/driver is used in subsystem clock ( $f_{SUB}$ ), be sure to set bit 7 (RTCEN) of this register to 1.

This register is set by using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

**Figure 14-2. Format of Peripheral Enable Register 0 (PER0)**

Address: F00F0H After reset: 00H R/W

| Symbol | <7>   | 6 | <5>   | <4>     | 3 | <2>    | 1 | <0>    |
|--------|-------|---|-------|---------|---|--------|---|--------|
| PER0   | RTCEN | 0 | ADCEN | IICA0EN | 0 | SAU0EN | 0 | TAU0EN |

| RTCEN | Real-time clock (RTC),<br>12-bit interval timer                                                                                                                                                                                                      | LCD controller/driver, clock output/buzzer output controller                                                                                                                                               |                                                                                                                                                                                                              |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |                                                                                                                                                                                                                                                      | When subsystem clock ( $f_{SUB}$ ) is<br>selected                                                                                                                                                          | When subsystem clock ( $f_{SUB}$ ) is<br>not selected                                                                                                                                                        |
| 0     | Stops input clock supply.<br><ul style="list-style-type: none"><li>SFR used by the real-time clock (RTC) and 12-bit interval timer cannot be written.</li><li>The real-time clock (RTC) and 12-bit interval timer are in the reset status.</li></ul> | Stops input clock and subsystem clock supply.<br><ul style="list-style-type: none"><li>SFR used by the LCD controller/driver and clock output/buzzer output controller can be read and written.</li></ul>  | Enables input clock and main system clock supply<br><ul style="list-style-type: none"><li>SFR used by the LCD controller/driver and clock output/buzzer output controller can be read and written.</li></ul> |
| 1     | Enables input clock supply.<br><ul style="list-style-type: none"><li>SFR used by the real-time clock (RTC) and 12-bit interval timer can be read and written.</li></ul>                                                                              | Enables input clock and subsystem clock supply<br><ul style="list-style-type: none"><li>SFR used by the LCD controller/driver and clock output/buzzer output controller can be read and written.</li></ul> |                                                                                                                                                                                                              |

- Cautions**
1. The subsystem clock supply to peripheral functions other than the real-time clock, 12-bit interval timer, and LCD controller/driver can be stopped in HALT mode when the subsystem clock is used, by setting the RTCLPC bit of the operation speed mode control register (OSMC) to 1. In this case, set the RTCEN bit of the PER0 register to 1 and the other bits (bits 0 to 6) to 0.
  2. Be sure to set bits 1, 3, and 6 to "0".



### 14.3.2 LCD mode register 0 (LCDM0)

LCDM0 specifies the LCD operation.

This register is set by using an 8-bit memory manipulation instruction.

Reset signal generation sets LCDM0 to 00H.

**Figure 14-3. Format of LCD Mode Register 0 (LCDM0) (1/2)**

Address: FFF40H After reset: 00H R/W

|        |        |        |       |       |       |       |       |       |
|--------|--------|--------|-------|-------|-------|-------|-------|-------|
| Symbol | 7      | 6      | 5     | 4     | 3     | 2     | 1     | 0     |
| LCDM0  | MDSET1 | MDSET0 | LWAVE | LDTY2 | LDTY1 | LDTY0 | LBAS1 | LBAS0 |

| MDSET1 | MDSET0 | LCD drive voltage generator selection |
|--------|--------|---------------------------------------|
| 0      | 0      | External resistance division method   |
| 0      | 1      | Internal voltage boosting method      |
| 1      | 0      | Capacitor split method                |
| 1      | 1      | Setting prohibited                    |

| MLCDEN <sup>Note 2</sup> | LWAVE <sup>Note 2</sup> | LCD display waveform selection                        |
|--------------------------|-------------------------|-------------------------------------------------------|
| 0                        | 0                       | Waveform A                                            |
| 0                        | 1                       | Waveform B                                            |
| 1                        | ×                       | Memory-type liquid crystal waveform <sup>Note 1</sup> |

| LDTY2            | LDTY1 | LDTY0 | Selection of time slice of LCD display |
|------------------|-------|-------|----------------------------------------|
| 0                | 0     | 0     | Static                                 |
| 0                | 0     | 1     | 2-time slice                           |
| 0                | 1     | 0     | 3-time slice                           |
| 0                | 1     | 1     | 4-time slice                           |
| 1                | 0     | 1     | 8-time slice                           |
| Other than above |       |       | Setting prohibited                     |

**Notes** 1. Selecting  $f_{IL}$  as the LCD source clock ( $f_{LCD}$ ) is prohibited.

2. LWAVE selects the LCD display waveform in combination with the MLCDEN bit of the MLCD register.

**Remark** MLCDEN: Bit 7 of MLCD

Figure 14-3. Format of LCD Mode Register 0 (LCDM0) (2/2)

Address: FFF40H After reset: 00H R/W

|        |        |        |       |       |       |       |       |       |
|--------|--------|--------|-------|-------|-------|-------|-------|-------|
| Symbol | 7      | 6      | 5     | 4     | 3     | 2     | 1     | 0     |
| LCDM0  | MDSET1 | MDSET0 | LWAVE | LDTY2 | LDTY1 | LDTY0 | LBAS1 | LBAS0 |

| LBAS1 | LBAS0 | LCD display bias mode selection |
|-------|-------|---------------------------------|
| 0     | 0     | 1/2 bias method                 |
| 0     | 1     | 1/3 bias method                 |
| 1     | 0     | 1/4 bias method                 |
| 1     | 1     | Setting prohibited              |

- Cautions**
1. Do not rewrite the LCDM0 value while the SCOC bit of the LCDM1 register = 1.
  2. When “Static” is selected (LDTY2 to LDTY0 bits = 000B), be sure to set the LBAS1 and LBAS0 bits to the default value (00B). Otherwise, the operation will not be guaranteed.
  3. Only the combinations of display waveform, number of time slices, and bias method shown in Table 14-4 are supported.  
Combinations of settings not shown in Table 14-4 are prohibited.

&lt;R&gt;

Table 14-4. Combinations of Display Waveform, Time Slices, and Bias Method

| Display Mode                        |                       |           | Set Value |       |       |       |       |       |       | Driving Voltage Generation Method |                           |                     |
|-------------------------------------|-----------------------|-----------|-----------|-------|-------|-------|-------|-------|-------|-----------------------------------|---------------------------|---------------------|
| Display Waveform                    | Number of Time Slices | Bias Mode | MLCDEN    | LWAVE | LDTY2 | LDTY1 | LDTY0 | LBAS1 | LBAS0 | External Resistance Division      | Internal Voltage Boosting | Capacitor Split     |
| Waveform A                          | 8                     | 1/4       | 0         | 0     | 1     | 0     | 1     | 1     | 0     | ○<br>(24 to 128 Hz)               | ○<br>(24 to 64 Hz)        | ×                   |
| Waveform A                          | 4                     | 1/3       | 0         | 0     | 0     | 1     | 1     | 0     | 1     | ○<br>(24 to 128 Hz)               | ○<br>(24 to 128 Hz)       | ○<br>(24 to 128 Hz) |
| Waveform A                          | 3                     | 1/3       | 0         | 0     | 0     | 1     | 0     | 0     | 1     | ○<br>(32 to 128 Hz)               | ○<br>(32 to 128 Hz)       | ○<br>(32 to 128 Hz) |
| Waveform A                          | 3                     | 1/2       | 0         | 0     | 0     | 1     | 0     | 0     | 0     | ○<br>(32 to 128 Hz)               | ×                         | ×                   |
| Waveform A                          | 2                     | 1/2       | 0         | 0     | 0     | 0     | 1     | 0     | 0     | ○<br>(24~128 Hz)                  | ×                         | ×                   |
| Waveform A                          | Static                |           | 0         | 0     | 0     | 0     | 0     | 0     | 0     | ○<br>(24~128 Hz)                  | ×                         | ×                   |
| Waveform B                          | 8                     | 1/4       | 0         | 1     | 1     | 0     | 1     | 1     | 0     | ○<br>(24~128 Hz)                  | ○<br>(24~64 Hz)           | ×                   |
| Waveform B                          | 4                     | 1/3       | 0         | 1     | 0     | 1     | 1     | 0     | 1     | ○<br>(24~128 Hz)                  | ○<br>(24~128 Hz)          | ○<br>(24~128 Hz)    |
| Memory-type liquid crystal waveform | 4                     | 1/3       | 1         | 0/1   | 0     | 1     | 1     | 0     | 1     | ○                                 | ×                         | ×                   |
| Memory-type liquid crystal waveform | 3                     | 1/3       | 1         | 0/1   | 0     | 1     | 0     | 0     | 1     | ○                                 | ×                         | ×                   |

**Caution** Set the minimum pulse width when using the memory-type liquid crystal in a range from 200  $\mu$ s to 7000  $\mu$ s.

**Remark** ○: Supported  
×: Not supported

### 14.3.3 LCD mode register 1 (LCDM1)

LCDM1 enables or disables display operation, voltage boost circuit operation, and capacitor split circuit operation, and specifies the display data area and the low voltage mode.

LCDM1 is set using a 1-bit or 8-bit memory manipulation instruction. Note, however, that LCDM1 is set by using an 8-bit memory manipulation instruction when the memory-type liquid crystal waveform is to be displayed.

Reset signal generation sets LCDM1 to 00H.

**Figure 14-4. Format of LCD Mode Register 1 (LCDM1) (1/2)**

Address: FFF41H After reset: 00H R/W

| Symbol | <7>   | <6>  | <5>   | <4>  | <3>    | 2 | 1 | <0>    |
|--------|-------|------|-------|------|--------|---|---|--------|
| LCDM1  | LCDON | SCOC | VLCON | BLON | LCDSEL | 0 | 0 | LCDVLM |

| SCOC | LCDON | LCD display enable/disable                                      |                                                                                                       |
|------|-------|-----------------------------------------------------------------|-------------------------------------------------------------------------------------------------------|
|      |       | When normal liquid crystal waveform (waveform A or B) is output | When memory-type liquid crystal waveform is output                                                    |
| 0    | 0     | Output ground level to segment/common pin                       |                                                                                                       |
| 0    | 1     |                                                                 |                                                                                                       |
| 1    | 0     | Display off (all segment outputs are deselected.)               | Output ground level to segment/common pin (when LCD display is hold and 2nd frame has been completed) |
| 1    | 1     | Display on                                                      |                                                                                                       |

| VLCON               | Voltage boost circuit or capacitor split circuit operation enable/disable |
|---------------------|---------------------------------------------------------------------------|
| 0                   | Stops voltage boost circuit or capacitor split circuit operation          |
| 1 <sup>Note 1</sup> | Enables voltage boost circuit or capacitor split circuit operation        |

| BLON <sup>Notes 2, 3</sup> | LCDSEL <sup>Note 3</sup> | Display data area control                                                                                                                                               |
|----------------------------|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0                          | 0                        | Displaying an A-pattern area data (lower four bits of LCD display data register)                                                                                        |
| 0                          | 1                        | Displaying a B-pattern area data (higher four bits of LCD display data register)                                                                                        |
| 1                          | 0                        | Alternately displaying A-pattern and B-pattern area data (blinking display corresponding to the constant-period interrupt (INTRTC) timing of the real-time clock (RTC)) |
| 1                          | 1                        |                                                                                                                                                                         |

- <R> **Notes 1.** Setting is prohibited when External resistance division method.
2. When  $f_{IL}$  is selected as the LCD source clock ( $f_{LCD}$ ), be sure to set the BLON bit to "0".
- <R> 3. Setting is prohibited BLON = 1 or LCDSEL = 1 when memory-type liquid crystal mode.

(Cautions are listed on the next page.)

Figure 14-4. Format of LCD Mode Register 1 (LCDM1) (2/2)

Address: FFF41H After reset: 00H R/W

| Symbol | <7>   | <6>  | <5>   | <4>  | <3>    | 2 | 1 | <0>    |
|--------|-------|------|-------|------|--------|---|---|--------|
| LCDM1  | LCDON | SCOC | VLCON | BLON | LCDSEL | 0 | 0 | LCDVLM |

| LCDVLM <sup>Note</sup> | Control of default value of voltage boosting pin |
|------------------------|--------------------------------------------------|
| 0                      | Set when $V_{DD} \geq 2.7$ V                     |
| 1                      | Set when $V_{DD} \leq 4.2$ V                     |

<R> **Note** This bit is used to boost the voltage efficiently when using the voltage boost circuit by setting the initial VLx pin status.

If  $V_{DD}$  is 2.7 V or higher when voltage boosting starts, set the LCDVLM bit to 0; if  $V_{DD}$  is 4.2 V or lower, set the LCDVLM bit to 1.

If  $V_{DD}$  is within the range between 2.7 V and 4.2 V, the LCDVLM bit may be set to 0 or 1.

- <R> **Cautions**
1. reduce power consumption when the normal liquid crystal waveform is not displayed on the LCD, set the SCOC and VLCON bits to “0”, and set the MDSET1 and MDSET0 bits to “00”. When DSET1 and MDSET0 = 01, power is consumed at reference voltage generator
  2. When the external resistance division method has been set (MDSET1 and MDSET0 of LCDM0 = 00B) or capacitor split method has been set (MDSET1 and MDSET0 = 10B), set the LCDVLM bit to 0.
  3. Do not rewrite the VLCON and LCDVLM bits while SCOC = 1.
  4. Set the BLON and LCDSEL bits to 0 when 8 has been selected as the number of time slices for the display mode.
  5. To use the internal voltage boosting method, specify the reference voltage by using the VLCD register (select the internal boosting method (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default reference voltage is used), wait for the reference voltage setup time (5 ms (min.)), and then set the VLCON bit to 1.
  6. When the LCD driving waveform is output (LCDON bit = 1) while the memory-type liquid crystal waveform is displayed, accessing the bits of the LCDM1 register is prohibited.

### 14.3.4 Operation speed mode control register (OSMC)

OSMC is used to reduce power consumption by stopping as many unnecessary clock functions as possible.

If the RTCLPC bit is set to 1, power consumption can be reduced, because clock supply to the peripheral functions, except the real-time clock, 12-bit interval timer, and LCD controller/driver, is stopped in HALT mode while the subsystem clock is selected as the CPU clock. Set bit 7 (RTCEN) of peripheral enable register 0 (PER0) to 1 before specifying this setting.

In addition, the OSMC register can be used to select the operation clock of the real-time clock, 12-bit interval timer, and LCD controller/driver.

This register is set by using an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

**Figure 14-5. Format of Operation Speed Mode Control Register (OSMC)**

Address: F00F3H After reset: 00H R/W

| Symbol | 7      | 6 | 5 | 4        | 3 | 2 | 1 | 0 |
|--------|--------|---|---|----------|---|---|---|---|
| OSMC   | RTCLPC | 0 | 0 | WUTMMCK0 | 0 | 0 | 0 | 0 |

|        |                                                                                                                                               |
|--------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| RTCLPC | Setting in HALT mode while subsystem clock is selected as CPU clock                                                                           |
| 0      | Enables subsystem clock supply to peripheral functions.<br>(See <b>Table 19-1</b> for the peripheral functions whose operations are enabled.) |
| 1      | Stops subsystem clock supply to peripheral functions except real-time clock, 12-bit interval timer, and LCD controller/driver.                |

|                          |                                                                                                    |                                                                          |
|--------------------------|----------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|
| WUTMMCK0 <sup>Note</sup> | Selection of operation clock for real-time clock, 12-bit interval timer, and LCD driver/controller | Selection of clock output from PCLBUZn pin of clock output/buzzer output |
| 0                        | Subsystem clock ( $f_{SUB}$ )                                                                      | Selecting the subsystem clock ( $f_{SUB}$ ) is enabled.                  |
| 1                        | Low-speed on-chip oscillator clock ( $f_{L}$ )                                                     | Selecting the subsystem clock ( $f_{SUB}$ ) is disabled.                 |

**Note** Be sure to select the subsystem clock (WUTMMCK0 bit = 0) if the subsystem clock is oscillating.

**Cautions 1. The subsystem clock and low-speed on-chip oscillator clock can only be switched by using the WUTMMCK0 bit if the real-time clock, 12-bit interval timer, and LCD driver/controller are all stopped. The setting must not be changed after the operation starts.**

**These are stopped as follows:**

**Real-time clock: Set the RTCE bit to 0.**

**12-bit interval timer: Set the RINTE bit to 0.**

**LCD driver/controller: Set the SCOC and VLCON bits to 0.**

- The 32-pin product does not have a subsystem clock. Therefore, be sure to select the low-speed on-chip oscillator clock (WUTMMCK0 = 1) when selecting a low-speed clock as the LCD source clock ( $f_{LCD}$ ).
- If the low-speed on-chip oscillator clock (WUTMMCK0 = 1) is selected, the following modes cannot be specified for the LCD controller/driver.
  - Memory-type liquid crystal waveform

**Remark** RTCE: Bit 7 of real-time clock control register 0 (RTCC0)  
 RINTE: Bit 15 of interval timer control register (ITMC)  
 SCOC: Bit 6 of LCD mode register 1 (LCDM1)  
 VLCON: Bit 5 of LCD mode register 1 (LCDM1)

### 14.3.5 LCD clock control register 0 (LCDC0)

LCDC0 specifies the LCD source clock and LCD clock.

The frame frequency is determined according to the LCD clock and the number of time slices.

This register is set by using an 8-bit memory manipulation instruction.

Reset signal generation sets LCDC0 to 00H.

<R>

Figure 14-6. Format of LCD Clock Control Register 0 (LCDC0) (1/2)

Address: FFF42H After reset: 00H R/W

|        |   |   |        |        |        |        |        |        |
|--------|---|---|--------|--------|--------|--------|--------|--------|
| Symbol | 7 | 6 | 5      | 4      | 3      | 2      | 1      | 0      |
| LCDC0  | 0 | 0 | LCDC05 | LCDC04 | LCDC03 | LCDC02 | LCDC01 | LCDC00 |

(1/2)

| LCDC05 | LCDC04 | LCDC03 | LCDC02 | LCDC01 | LCDC00 | LCD clock (LCDCL)                             |
|--------|--------|--------|--------|--------|--------|-----------------------------------------------|
| 0      | 0      | 0      | 0      | 0      | 1      | $f_{SUB}/2^2$ or $f_{IL}/2^2$ <sup>Note</sup> |
| 0      | 0      | 0      | 0      | 1      | 0      | $f_{SUB}/2^3$ or $f_{IL}/2^3$ <sup>Note</sup> |
| 0      | 0      | 0      | 0      | 1      | 1      | $f_{SUB}/2^4$ or $f_{IL}/2^4$ <sup>Note</sup> |
| 0      | 0      | 0      | 1      | 0      | 0      | $f_{SUB}/2^5$ or $f_{IL}/2^5$ <sup>Note</sup> |
| 0      | 0      | 0      | 1      | 0      | 1      | $f_{SUB}/2^6$ or $f_{IL}/2^6$ <sup>Note</sup> |
| 0      | 0      | 0      | 1      | 1      | 0      | $f_{SUB}/2^7$ or $f_{IL}/2^7$ <sup>Note</sup> |
| 0      | 0      | 0      | 1      | 1      | 1      | $f_{SUB}/2^8$ or $f_{IL}/2^8$ <sup>Note</sup> |
| 0      | 0      | 1      | 0      | 0      | 0      | $f_{SUB}/2^9$ or $f_{IL}/2^9$ <sup>Note</sup> |
| 0      | 0      | 1      | 0      | 0      | 1      | $f_{SUB}/2^{10}$                              |

**Note** When the memory-type liquid crystal waveform has been specified (MLCDEN bit of LCDM0 register = 1), selecting  $f_{IL}$  as the LCD source clock ( $f_{LCD}$ ) is prohibited.

**Cautions 1. Be sure to set bits 6 and 7 to “0”.**

<R>

2. Set the frame frequency in a range from 32 Hz to 128 Hz (24 Hz to 128 Hz when  $f_{IL}$  is selected). And set the LCD clock (LCDCL) to no more than 512 Hz (no more than 235 Hz when  $f_{IL}$  is selected) when the internal voltage boosting method, and the capacitor split method have been specified.

<R>

3. Do not set LCDC0 when the SCOC bit of the LCDM1 register is 1.
4. When the memory-type liquid crystal waveform is selected (the MLCDEN bit of the LCDM0 register is 1),  $f_{IL}$  cannot be selected as the LCD source clock ( $f_{LCD}$ ).

(Remark is listed on the next page.)

Figure 14-6. Format of LCD Clock Control Register 0 (LCDC0) (2/2)

Address: FFF42H After reset: 00H R/W

|        |   |   |        |        |        |        |        |        |
|--------|---|---|--------|--------|--------|--------|--------|--------|
| Symbol | 7 | 6 | 5      | 4      | 3      | 2      | 1      | 0      |
| LCDC0  | 0 | 0 | LCDC05 | LCDC04 | LCDC03 | LCDC02 | LCDC01 | LCDC00 |

(2/2)

| LCDC05           | LCDC04 | LCDC03 | LCDC02 | LCDC01 | LCDC00 | LCD clock (LCDCL)        |
|------------------|--------|--------|--------|--------|--------|--------------------------|
| 0                | 1      | 0      | 0      | 0      | 1      | $f_{\text{MAIN}}/2^8$    |
| 0                | 1      | 0      | 0      | 1      | 0      | $f_{\text{MAIN}}/2^9$    |
| 0                | 1      | 0      | 0      | 1      | 1      | $f_{\text{MAIN}}/2^{10}$ |
| 0                | 1      | 0      | 1      | 0      | 0      | $f_{\text{MAIN}}/2^{11}$ |
| 0                | 1      | 0      | 1      | 0      | 1      | $f_{\text{MAIN}}/2^{12}$ |
| 0                | 1      | 0      | 1      | 1      | 0      | $f_{\text{MAIN}}/2^{13}$ |
| 0                | 1      | 0      | 1      | 1      | 1      | $f_{\text{MAIN}}/2^{14}$ |
| 0                | 1      | 1      | 0      | 0      | 0      | $f_{\text{MAIN}}/2^{15}$ |
| 0                | 1      | 1      | 0      | 0      | 1      | $f_{\text{MAIN}}/2^{16}$ |
| 0                | 1      | 1      | 0      | 1      | 0      | $f_{\text{MAIN}}/2^{17}$ |
| 0                | 1      | 1      | 0      | 1      | 1      | $f_{\text{MAIN}}/2^{18}$ |
| 1                | 0      | 1      | 0      | 1      | 1      | $f_{\text{MAIN}}/2^{19}$ |
| Other than above |        |        |        |        |        | Setting prohibited       |

**Cautions** 1. Be sure to set bits 6 and 7 to “0”.

- <R> 2. Set the frame frequency in a range from 32 Hz to 128 Hz. and set the LCD clock (LCDCL) to no more than 512 Hz. When the internal voltage boosting method, and the capacitor split method have been specified.
- <R> 3. Set the minimum pulse width when using the memory-type liquid crystal in a range from 200  $\mu\text{s}$  to 7000  $\mu\text{s}$ .
4. Do not set LCDC0 when the SCOC bit of the LCDM1 register is 1.

**Remark**  $f_{\text{MAIN}}$ : Main system clock frequency  
 $f_{\text{SUB}}$ : Subsystem clock frequency  
 $f_{\text{IL}}$ : Low-speed on-chip oscillator clock frequency

### 14.3.6 Memory-type liquid crystal control register (MLCD)

MLCD specifies how the memory-type liquid crystal waveform is controlled.

This register is set by using a 1-bit or 8-bit memory manipulation instruction.

Set this register when the SCOC bit of the LCDM1 register is 0.

Reset signal generation sets MLCD to 00H.

**Figure 14-7. Format of Memory-Type Liquid Crystal Control Register (MLCD)**

Address: FFF4CH After reset: 00H R/W

|        |        |        |   |        |   |        |        |        |
|--------|--------|--------|---|--------|---|--------|--------|--------|
| Symbol | <7>    | <6>    | 5 | <4>    | 3 | 2      | 1      | 0      |
| MLCD   | MLCDEN | COMEXP | 0 | OPTCKE | 0 | OPTCK2 | OPTCK1 | OPTCK0 |

| MLCDEN <sup>Note</sup> | LWAVE <sup>Note</sup> | LCD display waveform selection              |
|------------------------|-----------------------|---------------------------------------------|
| 0                      | 0                     | Normal liquid crystal waveform (waveform A) |
| 0                      | 1                     | Normal liquid crystal waveform (waveform B) |
| 1                      | x                     | Memory-type liquid crystal waveform         |

| COMEXP                                                                                                                    | COM4/COMEXP/SEG0 pin selection |
|---------------------------------------------------------------------------------------------------------------------------|--------------------------------|
| 0                                                                                                                         | SEG0 pin                       |
| 1                                                                                                                         | COMEXP pin                     |
| For how to set the output mode of the COM4/COMEXP/SEG0, COM5/SEG1, COM6/SEG2, and COM7/SEG3 pins, see <b>Table 14-5</b> . |                                |

| OPTCKE | Option clock enable/disable |
|--------|-----------------------------|
| 0      | Option clock disabled       |
| 1      | Option clock enabled        |

| OPTCK2 | OPTCK1 | OPTCK0 | Selection of option clock (division ratio of LCD clock (LCDCL)) |
|--------|--------|--------|-----------------------------------------------------------------|
| 0      | 0      | 0      | Divided by 2                                                    |
| 0      | 0      | 1      | Divided by 3                                                    |
| 0      | 1      | 0      | Divided by 4                                                    |
| 0      | 1      | 1      | Divided by 5                                                    |
| 1      | 0      | 0      | Divided by 6                                                    |
| 1      | 0      | 1      | Divided by 7                                                    |
| 1      | 1      | 0      | Divided by 8                                                    |
| 1      | 1      | 1      | Divided by 9                                                    |

**Note** MLCDEN selects an LCD display waveform in combination with LWAVE of LCDM0.

**Caution** MLCD can be set only when the memory-type liquid crystal waveform is selected as the LCD display waveform (MLCDEN = 1). Setting MLCD is prohibited when waveform A or B is selected as the LCD display waveform (MLCDEN = 0).

**Remarks 1.** LWAVE: Bit 5 of LCDM0

- The COMEXP pin is a waveform output pin that prevents the part of the memory-type liquid crystal that is off from being turned on.
- Selecting the option clock means selecting an operating clock (MLCDCL) that is dedicated to the memory-type liquid crystal waveform and is the LCD clock (LCDCL) further divided.



**Table 14-5. Output Setting of COM4/COMEXP/SEG0, COM5/SEG1, COM6/SEG2, and COM7/SEG3 Pins**

| LDTY2 | COMEXP | COM4/COMEXP/<br>SEG0  | COM5/SEG1 | COM6/SEG2 | COM7/SEG3 |
|-------|--------|-----------------------|-----------|-----------|-----------|
| 0     | 0      | SEG0                  | SEG1      | SEG2      | SEG3      |
| 0     | 1      | COMEXP                | SEG1      | SEG2      | SEG3      |
| 1     | 0      | COM4                  | COM5      | COM6      | COM7      |
| 1     | 1      | Setting is prohibited |           |           |           |

&lt;R&gt;

**Remark** LDTY2: Bit 4 of LCDM0

### 14.3.7 LCD boost level control register (VLCD)

VLCD selects the reference voltage that is to be generated when operating the voltage boost circuit (contrast adjustment). The reference voltage can be selected from 16 steps.

This register is set by using an 8-bit memory manipulation instruction.

Reset signal generation sets VLCD to 04H.

**Figure 14-8. Format of LCD Boost Level Control Register (VLCD)**

Address: FFF43H After reset: 04H R/W

|        |   |   |   |       |       |       |       |       |
|--------|---|---|---|-------|-------|-------|-------|-------|
| Symbol | 7 | 6 | 5 | 4     | 3     | 2     | 1     | 0     |
| VLCD   | 0 | 0 | 0 | VLCD4 | VLCD3 | VLCD2 | VLCD1 | VLCD0 |

| VLCD4            | VLCD3 | VLCD2 | VLCD1 | VLCD0 | Reference voltage selection<br>(contrast adjustment) | VL <sub>L</sub> voltage |                    |
|------------------|-------|-------|-------|-------|------------------------------------------------------|-------------------------|--------------------|
|                  |       |       |       |       |                                                      | 1/3 bias method         | 1/4 bias method    |
| 0                | 0     | 1     | 0     | 0     | 1.00 V (default)                                     | 3.00 V                  | 4.00 V             |
| 0                | 0     | 1     | 0     | 1     | 1.05 V                                               | 3.15 V                  | 4.20 V             |
| 0                | 0     | 1     | 1     | 0     | 1.10 V                                               | 3.30 V                  | 4.40 V             |
| 0                | 0     | 1     | 1     | 1     | 1.15 V                                               | 3.45 V                  | 4.60 V             |
| 0                | 1     | 0     | 0     | 0     | 1.20 V                                               | 3.60 V                  | 4.80 V             |
| 0                | 1     | 0     | 0     | 1     | 1.25 V                                               | 3.75 V                  | 5.00 V             |
| 0                | 1     | 0     | 1     | 0     | 1.30 V                                               | 3.90 V                  | 5.20 V             |
| 0                | 1     | 0     | 1     | 1     | 1.35 V                                               | 4.05 V                  | Setting prohibited |
| 0                | 1     | 1     | 0     | 0     | 1.40 V                                               | 4.20 V                  | Setting prohibited |
| 0                | 1     | 1     | 0     | 1     | 1.45 V                                               | 4.35 V                  | Setting prohibited |
| 0                | 1     | 1     | 1     | 0     | 1.50 V                                               | 4.50 V                  | Setting prohibited |
| 0                | 1     | 1     | 1     | 1     | 1.55 V                                               | 4.65 V                  | Setting prohibited |
| 1                | 0     | 0     | 0     | 0     | 1.60 V                                               | 4.80 V                  | Setting prohibited |
| 1                | 0     | 0     | 0     | 1     | 1.65 V                                               | 4.95 V                  | Setting prohibited |
| 1                | 0     | 0     | 1     | 0     | 1.70 V                                               | 5.10 V                  | Setting prohibited |
| 1                | 0     | 0     | 1     | 1     | 1.75 V                                               | 5.25 V                  | Setting prohibited |
| Other than above |       |       |       |       | Setting prohibited                                   |                         |                    |

- Cautions**
1. The VLCD setting is valid only when the voltage boost circuit is operating.
  2. Be sure to set bits 5 to 7 to "0".
  3. Be sure to change the VLCD value after having stopped the operation of the voltage boost circuit (VLCON = 0).
  4. To use the internal voltage boosting method, specify the reference voltage by using the VLCD register (select the internal boosting method (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default reference voltage is used), wait for the reference voltage setup time (5 ms (min.)), and then set VLCON to 1.
  5. With the external resistance division method and the capacitor split method, use the default value (04H) for the VLCD resistor.

### 14.3.8 LCD input switch control register (ISCLCD)

Input to the schmitt trigger buffer must be invalid until the CAPL/P126, CAPH/P127, and VL3/P125 pins are set to operate as LCD function pins in order to prevent through-current from entering.

This register is set by using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets ISCLCD to 00H.

**Figure 14-9. Format of LCD Input Switch Control Register (ISCLCD)**

Address: F0308H After reset: 00H R/W

|        |   |   |   |   |   |   |        |        |
|--------|---|---|---|---|---|---|--------|--------|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1      | 0      |
| ISCLCD | 0 | 0 | 0 | 0 | 0 | 0 | ISCVL3 | ISCCAP |

|        |                                             |
|--------|---------------------------------------------|
| ISCVL3 | VL3/P125 pin Schmitt trigger buffer control |
| 0      | Input invalid                               |
| 1      | Input valid                                 |

|        |                                                          |
|--------|----------------------------------------------------------|
| ISCCAP | CAPL/P126, CAPH/P127 pins Schmitt trigger buffer control |
| 0      | Input invalid                                            |
| 1      | Input valid                                              |

**Cautions** 1. If ISCVL3 = 0, set the corresponding port registers as follows:

PU125 bit of PU12 register = 0, P125 bit of P12 register = 0

2. If ISCCAP = 0, set the corresponding port registers as follows:

PU127 bit of PU12 register = 0, P127 bit of P12 register = 0

PU126 bit of PU12 register = 0, P126 bit of P12 register = 0

**(a) Operation of ports that alternately function as VL3, CAPL, and CAPH pins**

The functions of the VL3/P125, CAPL/P126, and CAPH/P127 pins can be selected by using the LCD input switch control register (ISCLCD), LCD mode register 0 (LCDM0), and port mode register 12 (PM12).

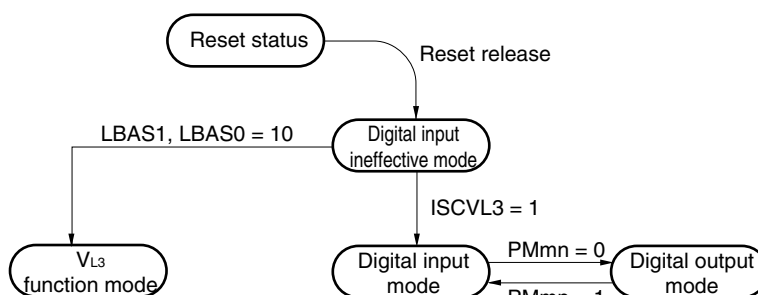
- VL3/P125

**Table 14-6. Settings of VL3/P125 Pin Function**

| Bias Setting<br>(LBAS1 and LBAS0 Bits of<br>LCDM0 Register ) | ISCVL3 Bit of<br>ISCLCD Register | PM125 Bit of<br>PM12 Register | Pin Function                   | Initial Status |
|--------------------------------------------------------------|----------------------------------|-------------------------------|--------------------------------|----------------|
| Other than 1/4 bias method<br>(LBAS1, LBAS0 = 00 or 01)      | 0                                | 1                             | Digital input ineffective mode | √              |
|                                                              | 1                                | 0                             | Digital output mode            | —              |
|                                                              | 1                                | 1                             | Digital input mode             | —              |
| 1/4 bias method<br>(LBAS1, LBAS0 = 10)                       | 0                                | 1                             | VL3 function mode              | —              |
| Other than above                                             |                                  |                               | Setting prohibited             |                |

The following shows the  $V_{L3}$ /P125 pin function status transitions.

**Figure 14-10.  $V_{L3}$ /P125 Pin Function Status Transitions**



**Caution** Be sure to set the  $V_{L3}$  function mode before segment output starts (while SCOC bit of LCD mode register 1 (LCDM1) is 0).

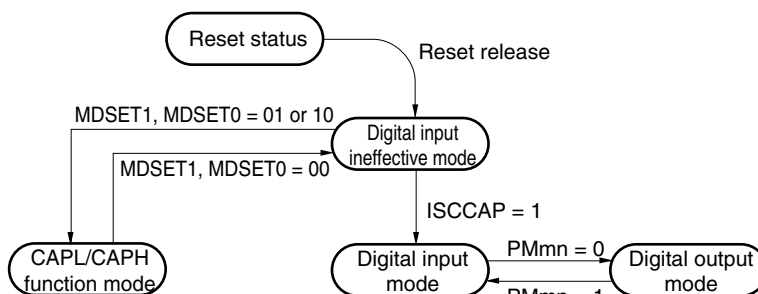
• CAPL/P126 and CAPH/P127

**Table 14-7. Settings of CAPL/P126 and CAPH/P127 Pin Functions**

| LCD Drive Voltage Generator<br>(MDSET1 and MDSET0 Bits of<br>LCDM0 Register)   | ISCCAP Bit of<br>ISCLCD Register | PM126 and<br>PM127 Bits of<br>PM12 Register | Pin Function                   | Initial Status |
|--------------------------------------------------------------------------------|----------------------------------|---------------------------------------------|--------------------------------|----------------|
| External resistance division<br>(MDSET1, MDSET0 = 00)                          | 0                                | 1                                           | Digital input ineffective mode | √              |
|                                                                                | 1                                | 0                                           | Digital output mode            | —              |
|                                                                                | 1                                | 1                                           | Digital input mode             | —              |
| Internal voltage boosting or<br>capacitor split<br>(MDSET1, MDSET0 = 01 or 10) | 0                                | 1                                           | CAPL/CAPH function mode        | —              |
| Other than above                                                               |                                  |                                             | Setting prohibited             |                |

The following shows the CAPL/P126 and CAPH/P127 pin function status transitions.

**Figure 14-11. CAPL/P126 and CAPH/P127 Pin Function Status Transitions**



**Caution** Be sure to set the CAPL/CAPH function mode before segment output starts (while SCOC bit of LCD mode register 1 (LCDM1) is 0).

### 14.3.9 LCD port function registers 0 to 4 (PFSEG0 to PFSEG4)

These registers specify whether to use pins P10 to P17, P30 to P32, P41 to P43, P50 to P54, P60, P61, P70 to P74, P120, and P140 to P147 as port pins (other than segment output pins) or segment output pins.

These registers are set by using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

**Remark** The correspondence between the segment output pins (SEGxx) and the PFSEG register (PFSEGxx bits) and the existence of SEGxx pins in each product are shown in Table 14-8 Segment Output Pins in Each Product and Correspondence with PFSEG Register (PFSEG Bits).

**Figure 14-12. Format of LCD Port Function Registers 0 to 4 (64-pin Products)**

Address: F0300H After reset: F0H R/W

|        |         |         |         |         |   |   |   |   |
|--------|---------|---------|---------|---------|---|---|---|---|
| Symbol | 7       | 6       | 5       | 4       | 3 | 2 | 1 | 0 |
| PFSEG0 | PFSEG07 | PFSEG06 | PFSEG05 | PFSEG04 | 0 | 0 | 0 | 0 |

Address: F0301H After reset: FFH R/W

|        |         |         |         |         |         |         |         |         |
|--------|---------|---------|---------|---------|---------|---------|---------|---------|
| Symbol | 7       | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
| PFSEG1 | PFSEG15 | PFSEG14 | PFSEG13 | PFSEG12 | PFSEG11 | PFSEG10 | PFSEG09 | PFSEG08 |

Address: F0302H After reset: FFH R/W

|        |         |         |         |         |         |         |         |         |
|--------|---------|---------|---------|---------|---------|---------|---------|---------|
| Symbol | 7       | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
| PFSEG2 | PFSEG23 | PFSEG22 | PFSEG21 | PFSEG20 | PFSEG19 | PFSEG18 | PFSEG17 | PFSEG16 |

Address: F0303H After reset: FFH R/W

|        |         |         |         |         |         |         |         |         |
|--------|---------|---------|---------|---------|---------|---------|---------|---------|
| Symbol | 7       | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
| PFSEG3 | PFSEG31 | PFSEG30 | PFSEG29 | PFSEG28 | PFSEG27 | PFSEG26 | PFSEG25 | PFSEG24 |

Address: F0304H After reset: 7FH R/W

|        |   |         |         |         |         |         |         |         |
|--------|---|---------|---------|---------|---------|---------|---------|---------|
| Symbol | 7 | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
| PFSEG4 | 0 | PFSEG38 | PFSEG37 | PFSEG36 | PFSEG35 | PFSEG34 | PFSEG33 | PFSEG32 |

|                            |                                                                                                                                                                |
|----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PFSEGxx<br>(xx = 04 to 46) | Port (other than segment output)/segment outputs specification of Pmn pins<br>(mn = 10 to 17, 30 to 32, 41 to 43, 50 to 54, 60, 61, 70 to 74, 120, 140 to 147) |
| 0                          | Used as port (other than segment output)                                                                                                                       |
| 1                          | Used as segment output                                                                                                                                         |

**Caution** To use the Pmn pins as segment output pins (PFSEGxx = 1), be sure to set the PUm<sub>n</sub> bit of the PUm register, POM<sub>mn</sub> bit of the POM<sub>m</sub> register, and PIM<sub>mn</sub> bit of the PIM<sub>m</sub> register to “0”.

**Table 14-8. Segment Output Pins in Each Product and Correspondence with PFSEG Register (PFSEG Bits)**

| Bit Name of PFSEG Register | Corresponding SEGxx Pins | Alternate Port | 64-pin | 52-pin | 48-pin | 44-pin | 32-pin |
|----------------------------|--------------------------|----------------|--------|--------|--------|--------|--------|
| PFSEG04                    | SEG4                     | P15            | √      | √      | √      | √      | √      |
| PFSEG05                    | SEG5                     | P16            | √      | √      | √      | √      | √      |
| PFSEG06                    | SEG6                     | P17            | √      | √      | √      | √      | √      |
| PFSEG07                    | SEG7                     | P50            | √      | √      | √      | –      | –      |
| PFSEG08                    | SEG8                     | P51            | √      | √      | –      | –      | –      |
| PFSEG09                    | SEG9                     | P52            | √      | –      | –      | –      | –      |
| PFSEG10                    | SEG10                    | P53            | √      | –      | –      | –      | –      |
| PFSEG11                    | SEG11                    | P54            | √      | –      | –      | –      | –      |
| PFSEG12                    | SEG12                    | P74            | √      | –      | –      | –      | –      |
| PFSEG13                    | SEG13                    | P73            | √      | –      | –      | –      | –      |
| PFSEG14                    | SEG14                    | P72            | √      | –      | –      | –      | –      |
| PFSEG15                    | SEG15                    | P71            | √      | √      | –      | –      | –      |
| PFSEG16                    | SEG16                    | P70            | √      | √      | √      | –      | –      |
| PFSEG17                    | SEG17                    | P32            | √      | √      | √      | √      | –      |
| PFSEG18                    | SEG18                    | P31            | √      | √      | √      | √      | –      |
| PFSEG19                    | SEG19                    | P30            | √      | √      | √      | √      | √      |
| PFSEG20                    | SEG20                    | P61            | √      | √      | √      | √      | √      |
| PFSEG21                    | SEG21                    | P60            | √      | √      | √      | √      | √      |
| PFSEG22                    | SEG22                    | P43            | √      | –      | –      | –      | –      |
| PFSEG23                    | SEG23                    | P42            | √      | √      | –      | –      | –      |
| PFSEG24                    | SEG24                    | P41            | √      | √      | √      | –      | –      |
| PFSEG25                    | SEG25                    | P120           | √      | √      | √      | √      | –      |
| PFSEG26                    | SEG26                    | P141           | √      | √      | √      | √      | –      |
| PFSEG27                    | SEG27                    | P140           | √      | √      | √      | √      | √      |
| PFSEG28                    | SEG28                    | P10            | √      | √      | √      | √      | √      |
| PFSEG29                    | SEG29                    | P11            | √      | √      | √      | √      | √      |
| PFSEG30                    | SEG30                    | P12            | √      | √      | √      | √      | √      |
| PFSEG31                    | SEG31                    | P13            | √      | √      | √      | √      | √      |
| PFSEG32                    | SEG32                    | P14            | √      | √      | √      | √      | √      |
| PFSEG33                    | SEG33                    | P142           | √      | √      | √      | √      | –      |
| PFSEG34                    | SEG34                    | P143           | √      | √      | √      | √      | –      |
| PFSEG35                    | SEG35                    | P144           | √      | √      | √      | –      | –      |
| PFSEG36                    | SEG36                    | P145           | √      | √      | –      | –      | –      |
| PFSEG37                    | SEG37                    | P146           | √      | –      | –      | –      | –      |
| PFSEG38                    | SEG38                    | P147           | √      | –      | –      | –      | –      |

**(a) Operation of ports that alternately function as SEGxx pins**

The functions of ports that also serve as segment output pins (SEGxx) can be selected by using the port mode control register (PMCxx), port mode register (PMxx), and LCD port function registers 0 to 4 (PFSEG0 to PFSEG4).

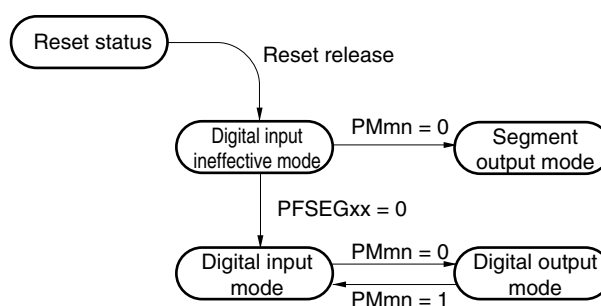
- P10 to P12, P15 to P17, P30 to P32, P42, P43, P50 to P54, P60, P61, P70 to P74, P140, P141  
(ports that do not serve as analog input pins (ANLxx))

**Table 14-9. Settings of SEGxx/Port Pin Function**

| PFSEGxx Bit of<br>PFSEG0 to PFSEG4 Registers | PMxx Bit of<br>PMxx Register | Pin Function                   | Initial Status |
|----------------------------------------------|------------------------------|--------------------------------|----------------|
| 1                                            | 1                            | Digital input ineffective mode | √              |
| 0                                            | 0                            | Digital output mode            | —              |
| 0                                            | 1                            | Digital input mode             | —              |
| 1                                            | 0                            | Segment output mode            | —              |

The following shows the SEGxx/port pin function status transitions.

**Figure 14-13. SEGxx/Port Pin Function Status Transitions**



**Caution** Be sure to set the segment output mode before segment output starts (while SCOC bit of LCD mode register 1 (LCDM1) is 0).

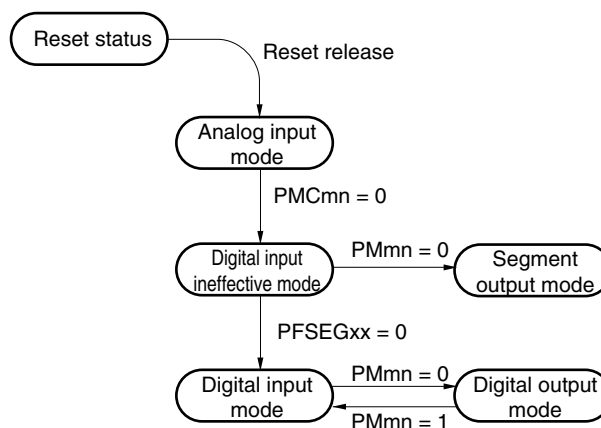
- P13, P14, P41, P120, P142 to P147 (ports that serve as analog input pins (ANLxx))

Table 14-10. Settings of ANLxx/SEGxx/Port Pin Function

| PMCxx Bit of<br>PMCxx Register | PFSEGxx Bit<br>PFSEG0 to PFSEG4 Registers | PMxx Bit of<br>PMxx Register | Pin Function                   | Initial Status |
|--------------------------------|-------------------------------------------|------------------------------|--------------------------------|----------------|
| 1                              | 1                                         | 1                            | Analog input mode              | √              |
| 0                              | 0                                         | 0                            | Digital output mode            | —              |
| 0                              | 0                                         | 1                            | Digital input mode             | —              |
| 0                              | 1                                         | 0                            | Segment output mode            | —              |
| 0                              | 1                                         | 1                            | Digital input ineffective mode | —              |
| Other than above               |                                           |                              | Setting prohibited             |                |

The following shows the ANLxx/SEGxx/port pin function status transitions.

Figure 14-14. ANLxx/SEGxx/Port Pin Function Status Transitions



**Caution** Be sure to set the segment output mode before segment output starts (while SCOC bit of LCD mode register 1 (LCDM1) is 0).



### 14.3.10 Port mode registers 1, 3 to 7, 12, 14 (PM1, PM3 to PM7, PM12, PM14)

These registers specify input/output of ports 1, 3 to 7, 12, and 14 in 1-bit units.

When using the ports (such as P10/ $\overline{\text{SCK00}}$ /SEG28, P120/ANI17/SEG25) to be shared with the segment output pin for segment output, set the port mode register (PMxx) bit and port register (Pxx) bit corresponding to each port to 0.

**Example:** When using P10/ $\overline{\text{SCK00}}$ /SEG28 for segment output

Set the PM10 bit of port mode register 1 to "0".

Set the P10 bit of port register 1 to "0".

These registers are set by using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

**Figure 14-15. Format of Port Mode Registers 1, 3 to 7, 12, 14 (PM1, PM3 to PM7, PM12, PM14) (64-pin Products)**

| Symbol | 7                                                                 | 6     | 5     | 4     | 3     | 2     | 1     | 0     | Address | After reset | R/W |
|--------|-------------------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|---------|-------------|-----|
| PM1    | PM17                                                              | PM16  | PM15  | PM14  | PM13  | PM12  | PM11  | PM10  | FFF21H  | FFH         | R/W |
| PM3    | 1                                                                 | 1     | 1     | 1     | 1     | PM32  | PM31  | PM30  | FFF23H  | FFH         | R/W |
| PM4    | 1                                                                 | 1     | 1     | 1     | PM43  | PM42  | PM41  | PM40  | FFF24H  | FFH         | R/W |
| PM5    | 1                                                                 | 1     | 1     | PM54  | PM53  | PM52  | PM51  | PM50  | FFF25H  | FFH         | R/W |
| PM6    | 1                                                                 | 1     | 1     | 1     | 1     | 1     | PM61  | PM60  | FFF26H  | FFH         | R/W |
| PM7    | 1                                                                 | 1     | 1     | PM74  | PM73  | PM72  | PM71  | PM70  | FFF27H  | FFH         | R/W |
| PM12   | PM127                                                             | PM126 | PM125 | 1     | 1     | 1     | 1     | PM120 | FFF2CH  | FFH         | R/W |
| PM14   | PM147                                                             | PM146 | PM145 | PM144 | PM143 | PM142 | PM141 | PM140 | FFF2EH  | FFH         | R/W |
| PMmn   | Pmn pin I/O mode selection<br>(m = 1, 3 to 7, 12, 14; n = 0 to 7) |       |       |       |       |       |       |       |         |             |     |
| 0      | Output mode (output buffer on)                                    |       |       |       |       |       |       |       |         |             |     |
| 1      | Input mode (output buffer off)                                    |       |       |       |       |       |       |       |         |             |     |

**Remark** The figure shown above presents the format of port mode registers 1, 3 to 7, 12, and 14 of the 64-pin products. The format of the port mode register of other products, see **Table 4-2 PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits mounted on each product.**

## 14.4 LCD Display Data Registers

The LCD display data registers are mapped as shown in Table 14-11. The contents displayed on the LCD can be changed by changing the contents of the LCD display data registers.

**Table 14-11. Relationship Between LCD Display Data Register Contents and Segment/Common Outputs (1/2)**

**(a) Other than 8-time-slice (static, 2-time slice, 3-time slice, and 4-time slice)**

| Register Name | Address | Bit 7                  | Bit 6 | Bit 5 | Bit 4 | Bit 3                  | Bit 2 | Bit 1 | Bit 0 | 64-pin | 52-pin | 48-pin | 44-pin | 32-pin |
|---------------|---------|------------------------|-------|-------|-------|------------------------|-------|-------|-------|--------|--------|--------|--------|--------|
|               |         | COM 7                  | COM 6 | COM 5 | COM 4 | COM 3                  | COM 2 | COM 1 | COM 0 |        |        |        |        |        |
| SEG0          | F0400H  | SEG0 (B-pattern area)  |       |       |       | SEG0 (A-pattern area)  |       |       |       | √      | √      | √      | √      | √      |
| SEG1          | F0401H  | SEG1 (B-pattern area)  |       |       |       | SEG1 (A-pattern area)  |       |       |       | √      | √      | √      | √      | —      |
| SEG2          | F0402H  | SEG2 (B-pattern area)  |       |       |       | SEG2 (A-pattern area)  |       |       |       | √      | √      | √      | √      | —      |
| SEG3          | F0403H  | SEG3 (B-pattern area)  |       |       |       | SEG3 (A-pattern area)  |       |       |       | √      | √      | √      | √      | —      |
| SEG4          | F0404H  | SEG4 (B-pattern area)  |       |       |       | SEG4 (A-pattern area)  |       |       |       | √      | √      | √      | √      | √      |
| SEG5          | F0405H  | SEG5 (B-pattern area)  |       |       |       | SEG5 (A-pattern area)  |       |       |       | √      | √      | √      | √      | √      |
| SEG6          | F0406H  | SEG6 (B-pattern area)  |       |       |       | SEG6 (A-pattern area)  |       |       |       | √      | √      | √      | √      | √      |
| SEG7          | F0407H  | SEG7 (B-pattern area)  |       |       |       | SEG7 (A-pattern area)  |       |       |       | √      | √      | √      | —      | —      |
| SEG8          | F0408H  | SEG8 (B-pattern area)  |       |       |       | SEG8 (A-pattern area)  |       |       |       | √      | √      | —      | —      | —      |
| SEG9          | F0409H  | SEG9 (B-pattern area)  |       |       |       | SEG9 (A-pattern area)  |       |       |       | √      | —      | —      | —      | —      |
| SEG10         | F040AH  | SEG10 (B-pattern area) |       |       |       | SEG10 (A-pattern area) |       |       |       | √      | —      | —      | —      | —      |
| SEG11         | F040BH  | SEG11 (B-pattern area) |       |       |       | SEG11 (A-pattern area) |       |       |       | √      | —      | —      | —      | —      |
| SEG12         | F040CH  | SEG12 (B-pattern area) |       |       |       | SEG12 (A-pattern area) |       |       |       | √      | —      | —      | —      | —      |
| SEG13         | F040DH  | SEG13 (B-pattern area) |       |       |       | SEG13 (A-pattern area) |       |       |       | √      | —      | —      | —      | —      |
| SEG14         | F040EH  | SEG14 (B-pattern area) |       |       |       | SEG14 (A-pattern area) |       |       |       | √      | —      | —      | —      | —      |
| SEG15         | F040FH  | SEG15 (B-pattern area) |       |       |       | SEG15 (A-pattern area) |       |       |       | √      | √      | —      | —      | —      |
| SEG16         | F0410H  | SEG16 (B-pattern area) |       |       |       | SEG16 (A-pattern area) |       |       |       | √      | √      | √      | —      | —      |
| SEG17         | F0411H  | SEG17 (B-pattern area) |       |       |       | SEG17 (A-pattern area) |       |       |       | √      | √      | √      | √      | —      |
| SEG18         | F0412H  | SEG18 (B-pattern area) |       |       |       | SEG18 (A-pattern area) |       |       |       | √      | √      | √      | √      | —      |
| SEG19         | F0413H  | SEG19 (B-pattern area) |       |       |       | SEG19 (A-pattern area) |       |       |       | √      | √      | √      | √      | √      |
| SEG20         | F0414H  | SEG20 (B-pattern area) |       |       |       | SEG20 (A-pattern area) |       |       |       | √      | √      | √      | √      | √      |
| SEG21         | F0415H  | SEG21 (B-pattern area) |       |       |       | SEG21 (A-pattern area) |       |       |       | √      | √      | √      | √      | √      |
| SEG22         | F0416H  | SEG22 (B-pattern area) |       |       |       | SEG22 (A-pattern area) |       |       |       | √      | —      | —      | —      | —      |
| SEG23         | F0417H  | SEG23 (B-pattern area) |       |       |       | SEG23 (A-pattern area) |       |       |       | √      | √      | —      | —      | —      |
| SEG24         | F0418H  | SEG24 (B-pattern area) |       |       |       | SEG24 (A-pattern area) |       |       |       | √      | √      | √      | —      | —      |
| SEG25         | F0419H  | SEG25 (B-pattern area) |       |       |       | SEG25 (A-pattern area) |       |       |       | √      | √      | √      | —      | —      |
| SEG26         | F041AH  | SEG26 (B-pattern area) |       |       |       | SEG26 (A-pattern area) |       |       |       | √      | √      | √      | √      | —      |
| SEG27         | F041BH  | SEG27 (B-pattern area) |       |       |       | SEG27 (A-pattern area) |       |       |       | √      | √      | √      | √      | √      |
| SEG28         | F041CH  | SEG28 (B-pattern area) |       |       |       | SEG28 (A-pattern area) |       |       |       | √      | √      | √      | √      | √      |
| SEG29         | F041DH  | SEG29 (B-pattern area) |       |       |       | SEG29 (A-pattern area) |       |       |       | √      | √      | √      | √      | √      |
| SEG30         | F041EH  | SEG30 (B-pattern area) |       |       |       | SEG30 (A-pattern area) |       |       |       | √      | √      | √      | √      | √      |
| SEG31         | F041FH  | SEG31 (B-pattern area) |       |       |       | SEG31 (A-pattern area) |       |       |       | √      | √      | √      | √      | √      |
| SEG32         | F0420H  | SEG32 (B-pattern area) |       |       |       | SEG32 (A-pattern area) |       |       |       | √      | √      | √      | √      | √      |
| SEG33         | F0421H  | SEG33 (B-pattern area) |       |       |       | SEG33 (A-pattern area) |       |       |       | √      | √      | √      | √      | —      |
| SEG34         | F0422H  | SEG34 (B-pattern area) |       |       |       | SEG34 (A-pattern area) |       |       |       | √      | √      | √      | √      | —      |
| SEG35         | F0423H  | SEG35 (B-pattern area) |       |       |       | SEG35 (A-pattern area) |       |       |       | √      | √      | √      | —      | —      |
| SEG36         | F0424H  | SEG36 (B-pattern area) |       |       |       | SEG36 (A-pattern area) |       |       |       | √      | √      | —      | —      | —      |
| SEG37         | F0425H  | SEG37 (B-pattern area) |       |       |       | SEG37 (A-pattern area) |       |       |       | √      | —      | —      | —      | —      |
| SEG38         | F0426H  | SEG38 (B-pattern area) |       |       |       | SEG38 (A-pattern area) |       |       |       | √      | —      | —      | —      | —      |

**Remark** √: Supported, —: Not supported

Table 14-11. Relationship Between LCD Display Data Register Contents and Segment/Common Outputs (2/2)

## (b) 8-time slice

| Register Name | Address | Bit 7                | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | 64-pin | 52-pin | 48-pin | 44-pin | 32-pin |
|---------------|---------|----------------------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|
|               |         | COM 7                | COM 6 | COM 5 | COM 4 | COM 3 | COM 2 | COM 1 | COM 0 |        |        |        |        |        |
| SEG0          | F0400H  | SEG0 <sup>Note</sup> |       |       |       |       |       |       |       | √      | √      | √      | √      | √      |
| SEG1          | F0401H  | SEG1 <sup>Note</sup> |       |       |       |       |       |       |       | √      | √      | √      | √      | —      |
| SEG2          | F0402H  | SEG2 <sup>Note</sup> |       |       |       |       |       |       |       | √      | √      | √      | √      | —      |
| SEG3          | F0403H  | SEG3 <sup>Note</sup> |       |       |       |       |       |       |       | √      | √      | √      | √      | —      |
| SEG4          | F0404H  | SEG4                 |       |       |       |       |       |       |       | √      | √      | √      | √      | √      |
| SEG5          | F0405H  | SEG5                 |       |       |       |       |       |       |       | √      | √      | √      | √      | √      |
| SEG6          | F0406H  | SEG6                 |       |       |       |       |       |       |       | √      | √      | √      | √      | √      |
| SEG7          | F0407H  | SEG7                 |       |       |       |       |       |       |       | √      | √      | √      | —      | —      |
| SEG8          | F0408H  | SEG8                 |       |       |       |       |       |       |       | √      | √      | —      | —      | —      |
| SEG9          | F0409H  | SEG9                 |       |       |       |       |       |       |       | √      | —      | —      | —      | —      |
| SEG10         | F040AH  | SEG10                |       |       |       |       |       |       |       | √      | —      | —      | —      | —      |
| SEG11         | F040BH  | SEG11                |       |       |       |       |       |       |       | √      | —      | —      | —      | —      |
| SEG12         | F040CH  | SEG12                |       |       |       |       |       |       |       | √      | —      | —      | —      | —      |
| SEG13         | F040DH  | SEG13                |       |       |       |       |       |       |       | √      | —      | —      | —      | —      |
| SEG14         | F040EH  | SEG14                |       |       |       |       |       |       |       | √      | —      | —      | —      | —      |
| SEG15         | F040FH  | SEG15                |       |       |       |       |       |       |       | √      | √      | —      | —      | —      |
| SEG16         | F0410H  | SEG16                |       |       |       |       |       |       |       | √      | √      | √      | —      | —      |
| SEG17         | F0411H  | SEG17                |       |       |       |       |       |       |       | √      | √      | √      | √      | —      |
| SEG18         | F0412H  | SEG18                |       |       |       |       |       |       |       | √      | √      | √      | √      | —      |
| SEG19         | F0413H  | SEG19                |       |       |       |       |       |       |       | √      | √      | √      | √      | √      |
| SEG20         | F0414H  | SEG20                |       |       |       |       |       |       |       | √      | √      | √      | √      | √      |
| SEG21         | F0415H  | SEG21                |       |       |       |       |       |       |       | √      | √      | √      | √      | √      |
| SEG22         | F0416H  | SEG22                |       |       |       |       |       |       |       | √      | —      | —      | —      | —      |
| SEG23         | F0417H  | SEG23                |       |       |       |       |       |       |       | √      | √      | —      | —      | —      |
| SEG24         | F0418H  | SEG24                |       |       |       |       |       |       |       | √      | √      | √      | —      | —      |
| SEG25         | F0419H  | SEG25                |       |       |       |       |       |       |       | √      | √      | √      | —      | —      |
| SEG26         | F041AH  | SEG26                |       |       |       |       |       |       |       | √      | √      | √      | √      | —      |
| SEG27         | F041BH  | SEG27                |       |       |       |       |       |       |       | √      | √      | √      | √      | √      |
| SEG28         | F041CH  | SEG28                |       |       |       |       |       |       |       | √      | √      | √      | √      | √      |
| SEG29         | F041DH  | SEG29                |       |       |       |       |       |       |       | √      | √      | √      | √      | √      |
| SEG30         | F041EH  | SEG30                |       |       |       |       |       |       |       | √      | √      | √      | √      | √      |
| SEG31         | F041FH  | SEG31                |       |       |       |       |       |       |       | √      | √      | √      | √      | √      |
| SEG32         | F0420H  | SEG32                |       |       |       |       |       |       |       | √      | √      | √      | √      | √      |
| SEG33         | F0421H  | SEG33                |       |       |       |       |       |       |       | √      | √      | √      | √      | —      |
| SEG34         | F0422H  | SEG34                |       |       |       |       |       |       |       | √      | √      | √      | √      | —      |
| SEG35         | F0423H  | SEG35                |       |       |       |       |       |       |       | √      | √      | √      | —      | —      |
| SEG36         | F0424H  | SEG36                |       |       |       |       |       |       |       | √      | √      | —      | —      | —      |
| SEG37         | F0425H  | SEG37                |       |       |       |       |       |       |       | √      | —      | —      | —      | —      |
| SEG38         | F0426H  | SEG38                |       |       |       |       |       |       |       | √      | —      | —      | —      | —      |

**Note** The COM4 to COM7 pins and SEG0 to SEG3 pins are used alternatively.

**Remark** √: Supported, —: Not supported

To use the LCD display data register when the number of time slices is static, two, three, or four, the lower four bits and higher four bits of each address of the LCD display data register become an A-pattern area and a B-pattern area, respectively.

The correspondences between A-pattern area data and COM signals are as follows: bit 0  $\Leftrightarrow$  COM0, bit 1  $\Leftrightarrow$  COM1, bit 2  $\Leftrightarrow$  COM2, and bit 3  $\Leftrightarrow$  COM3.

The correspondences between B-pattern area data and COM signals are as follows: bit 4  $\Leftrightarrow$  COM0, bit 5  $\Leftrightarrow$  COM1, bit 6  $\Leftrightarrow$  COM2, and bit 7  $\Leftrightarrow$  COM3.

A-pattern area data will be displayed on the LCD panel when BLON = LCDSEL = 0 has been selected, and B-pattern area data will be displayed on the LCD panel when BLON = 0 and LCDSEL = 1 have been selected.

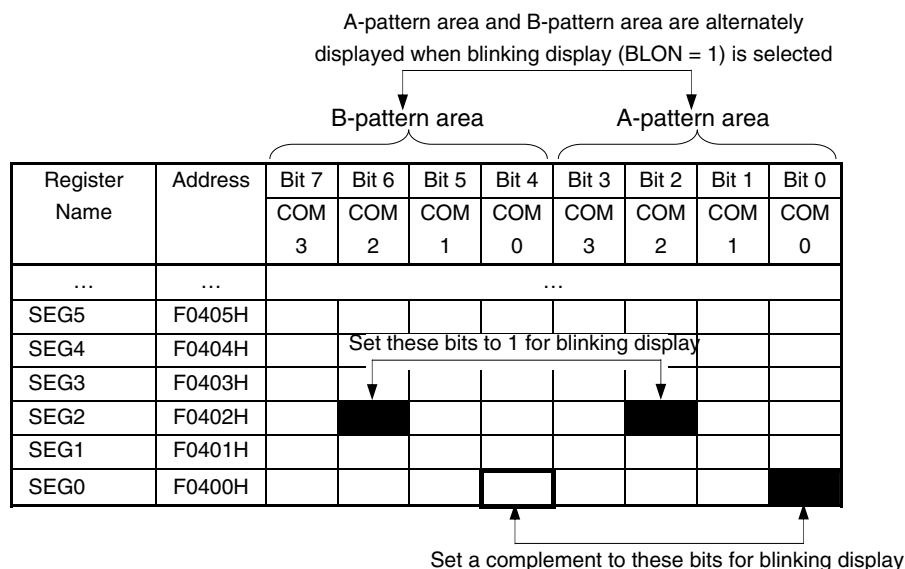
### 14.5 Selection of LCD Display Register

With RL78/L12, to use the LCD display data registers when the number of time slices is static, two, three, or four, the LCD display data register can be selected from the following three types, according to the BLON and LCDSEL bit settings.

- Displaying an A-pattern area data (lower four bits of LCD display data register)
- Displaying a B-pattern area data (higher four bits of LCD display data register)
- Alternately displaying A-pattern and B-pattern area data (blinking display corresponding to the constant-period interrupt timing of the real-time clock (RTC))

**Caution** If the normal liquid crystal waveform is displayed when the number of time slices is eight or if the memory-type liquid crystal waveform is displayed, LCD display data registers (A-pattern, B-pattern, or blinking display) cannot be selected.

Figure 14-16. Example of Setting LCD Display Registers When Pattern Is Changed



### 14.5.1 A-pattern area and B-pattern area data display

When BLON = LCDSEL = 0, A-pattern area (lower four bits of the LCD display data register) data will be output as the LCD display register.

When BLON = 0, and LCDSEL = 1, B-pattern area (higher four bits of the LCD display data register) data will be output as the LCD display register.

See **14.4 LCD Display Data Registers** about the display area.

### 14.5.2 Blinking display (Alternately displaying A-pattern and B-pattern area data)

When BLON = 1 has been set, A-pattern and B-pattern area data will be alternately displayed, according to the constant-period interrupt (INTRTC) timing of the real-time clock (RTC). See **CHAPTER 7 REAL-TIME CLOCK** about the setting of the RTC constant-period interrupt (INTRTC, 0.5 s setting only) timing.

For blinking display of the LCD, set inverted values to the B-pattern area bits corresponding to the A-pattern area bits. (Example: Set 1 to bit 0 of 00H, and set 0 to bit 4 of F0400H for blinking display.) When not setting blinking display of the LCD, set the same values. (Example: Set 1 to bit 2 of F0402H, and set 1 to bit 6 of F0402H for lighting display.)

See **14.4 LCD Display Data Registers** about the display area.

Next, the timing operation of display switching is shown.

**Figure 14-17. Switching Operation from A-Pattern Display to Blinking Display**

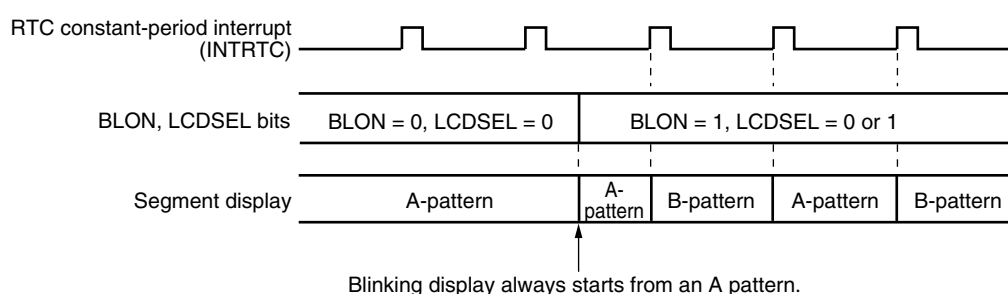
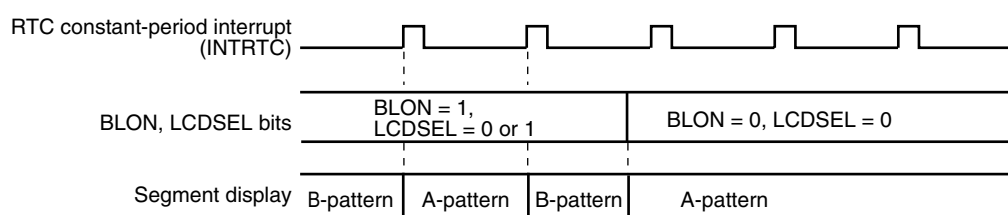


**Figure 14-18. Switching Operation from Blinking Display to A-Pattern Display**



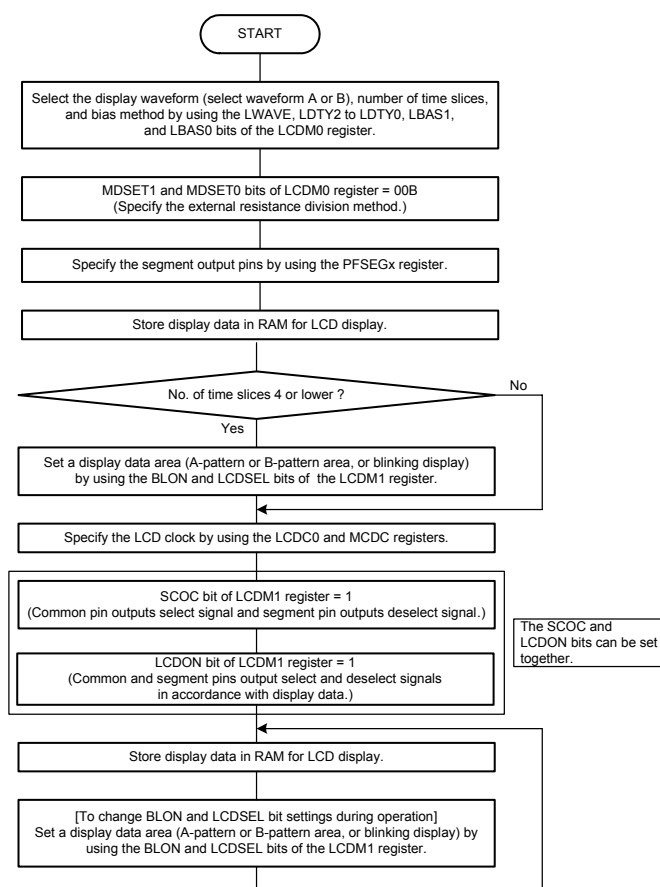
## 14.6 Setting the LCD Controller/Driver

Set the LCD controller/driver using the following procedure.

- Cautions**
1. To operate the LCD controller/driver, be sure to follow procedures (1) to (4). Unless these procedures are observed, the operation will not be guaranteed.
  2. The steps shown in the flowcharts in (1) to (4) are performed by the CPU except that the LCDON bit of the LCDM1 register is set to 0 by hardware when the second frame ends after the LCD panel display starts.

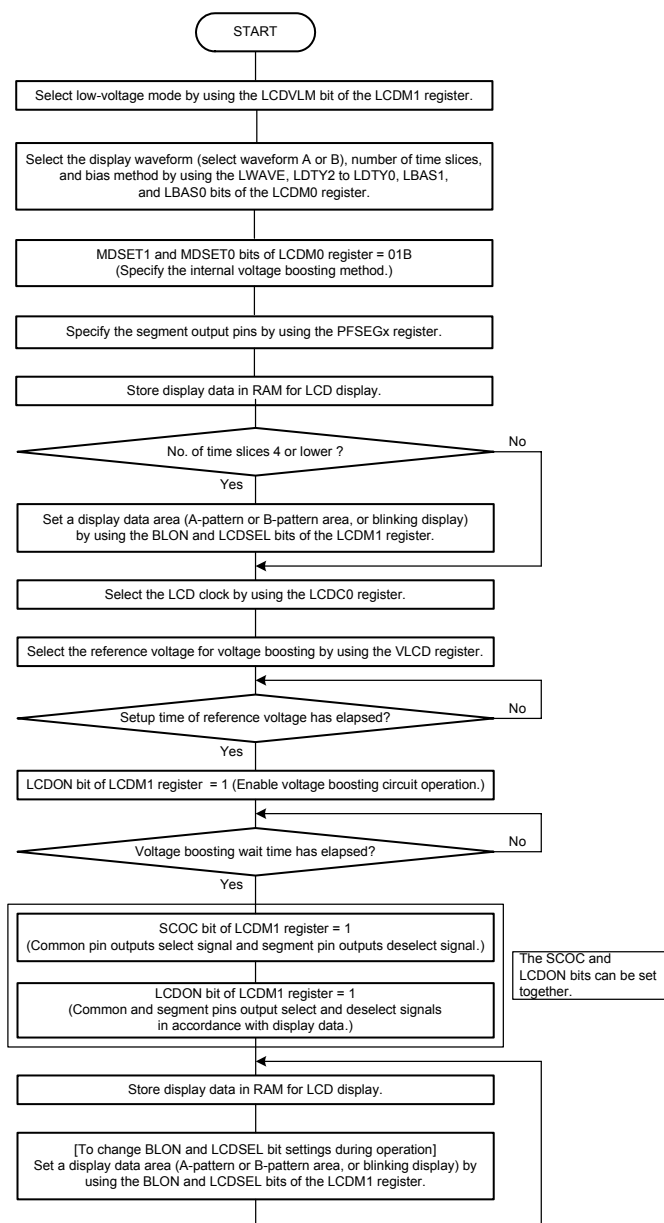
### (1) External resistance division method during normal liquid crystal waveform display

**Figure 14-19. External Resistance Division Method Setting Procedure During Normal Liquid Crystal Waveform Display**

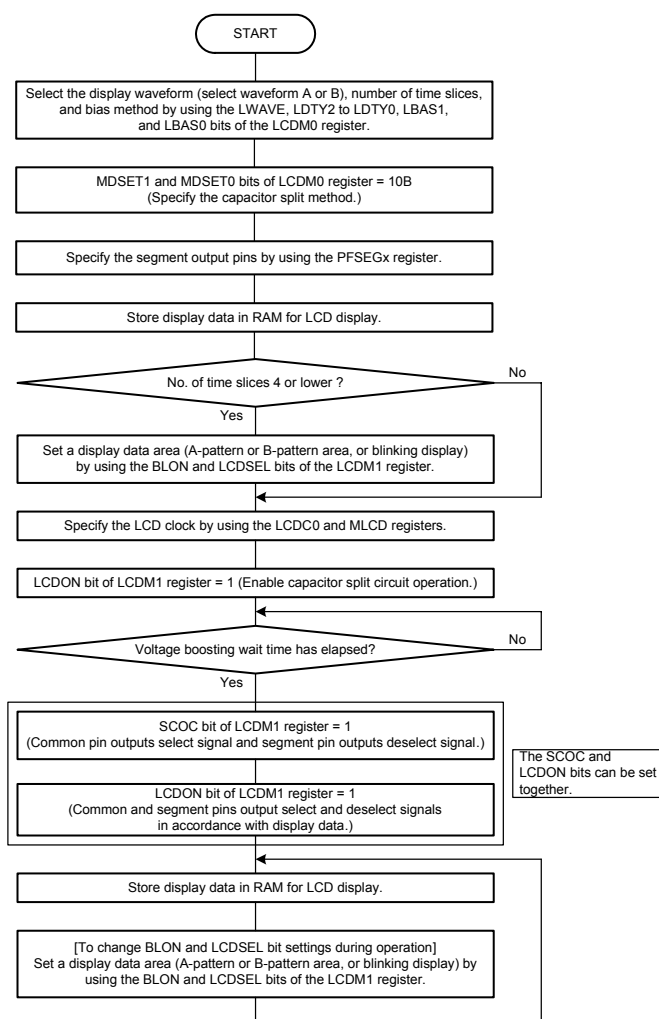


## (2) Internal voltage boosting method during normal liquid crystal waveform display

Figure 14-20. Internal Voltage Boosting Method Setting Procedure During Normal Liquid Crystal Waveform Display



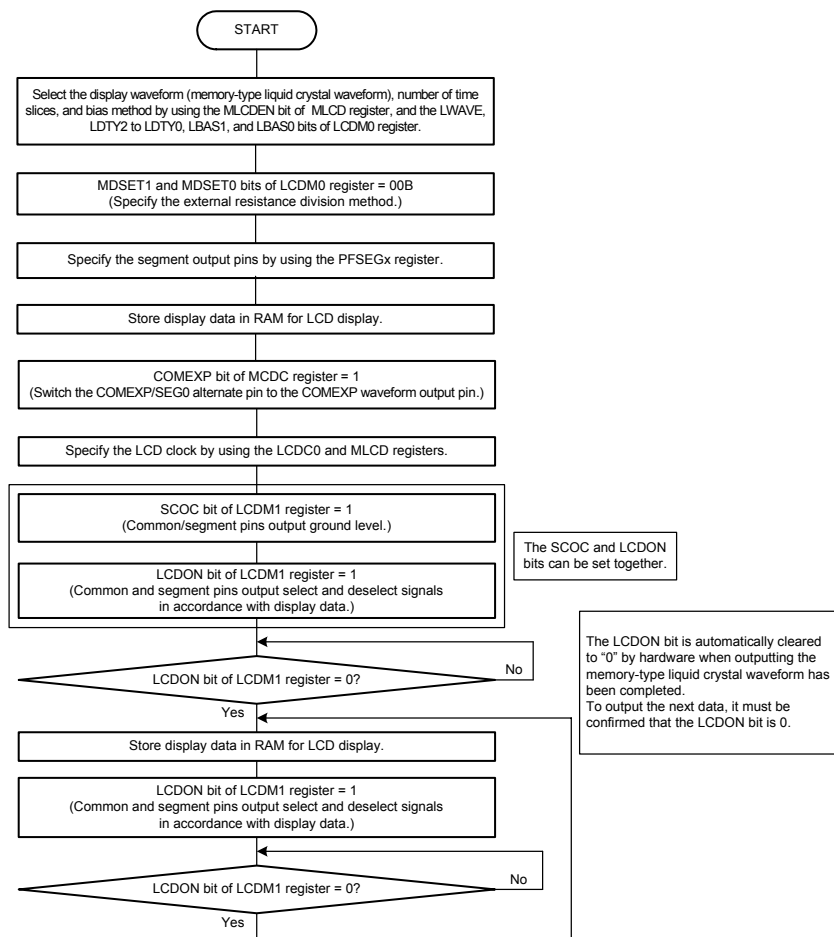
- Cautions**
1. Wait until the setup time has elapsed even if not changing the setting of the VLCD register.
  2. For the specifications of the reference voltage setup time and voltage boosting wait time, see CHAPTER 30 ELECTRICAL SPECIFICATIONS.

**(3) Capacitor split method during normal liquid crystal waveform display****Figure 14-21. Capacitor Split Method Setting Procedure During Normal Liquid Crystal Waveform Display**

**Caution** For the specifications of the voltage boosting wait time, see **CHAPTER 30 ELECTRICAL SPECIFICATIONS**.



## (4) External resistance division method during memory-type liquid crystal waveform display

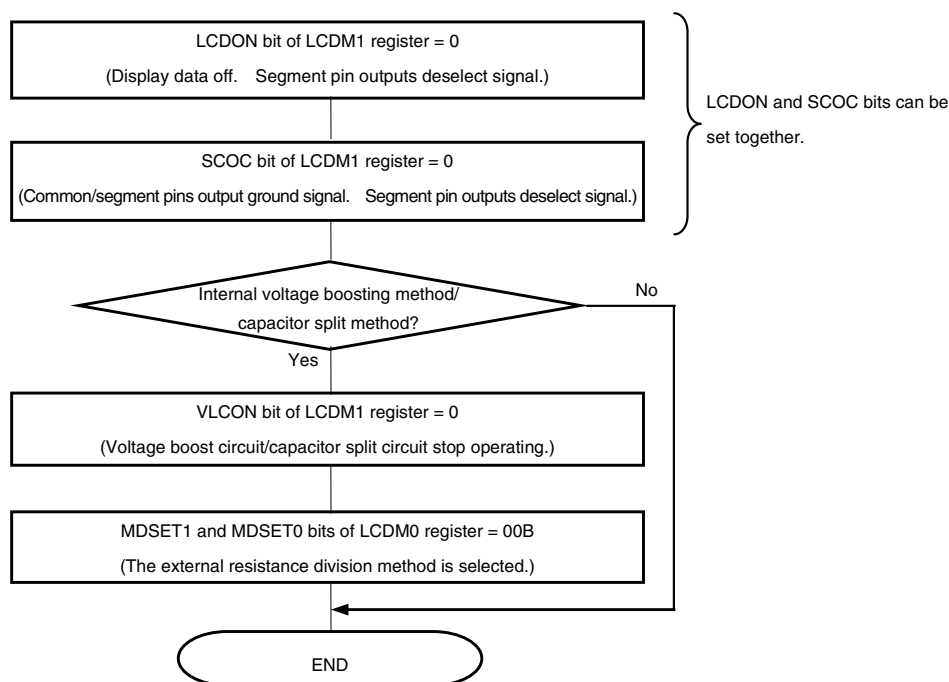
**Figure 14-22. External Resistance Division Method Setting Procedure  
During Memory-Type Liquid Crystal Waveform Display**

## 14.7 Operation stop procedure

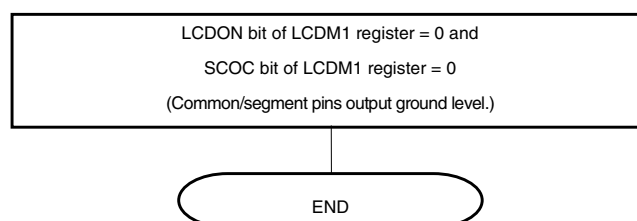
To stop the operation of the LCD while it is displaying waveforms, follow the steps shown in the flowchart below.  
The LCD stops operating when the LCDON bit of LCDM1 register and SCOC bit of the LCDM1 register are set to "0".

**Figure 14-23. Operation Stop Procedure**

### (a) During normal liquid crystal waveform (waveform A or B) display



### (b) During memory-type liquid crystal waveform display



- Cautions**
1. Stopping the voltage boost/capacitor split circuits is prohibited while the display is on (SCOC and LCDON bits of LCDM1 register = 00B). Otherwise, the operation will not be guaranteed. Be sure to turn off display (SCOC and LCDON bits of LCDM1 register = 00B) before stopping the voltage boost/capacitor split circuits (VLCON bit of LCDM1 register = 0).
  2. During memory-type liquid crystal waveform display, be sure to set the LCDON bit of the LCDM1 register and SCOC bit of the LCDM1 register to 0 at the same time. The operation will not be guaranteed unless these bits are set at the same time.

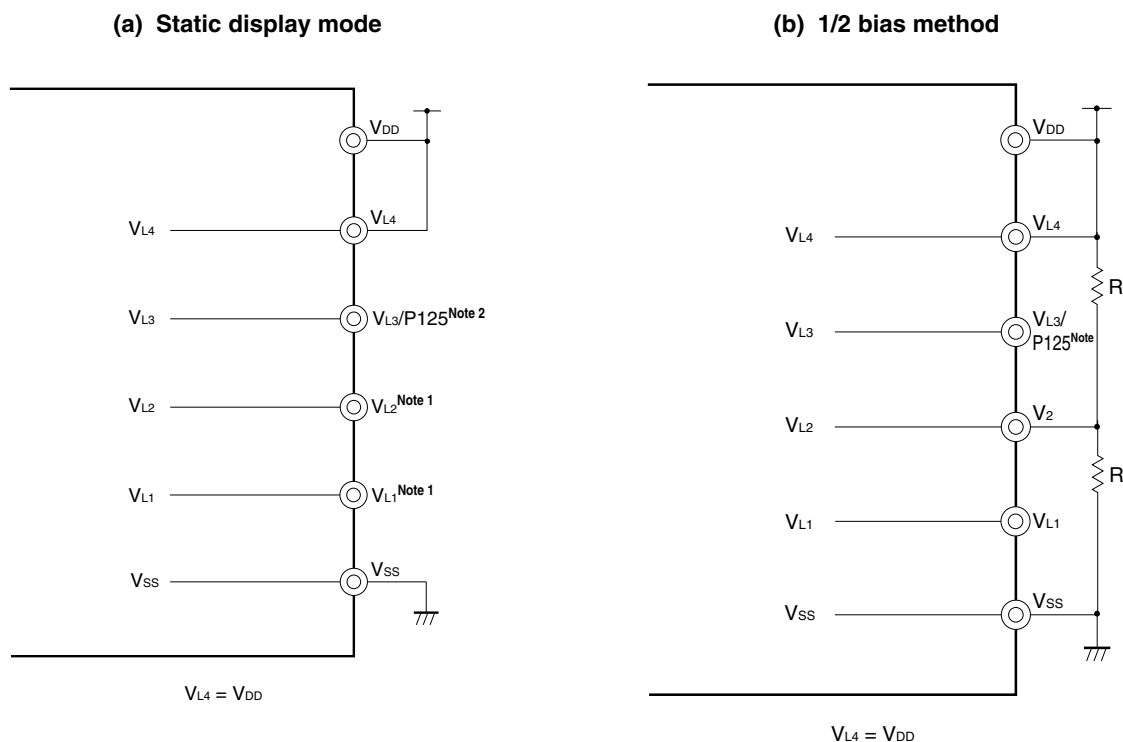
<R>

## 14.8 Supplying LCD Drive Voltages $V_{L1}$ , $V_{L2}$ , $V_{L3}$ , and $V_{L4}$

### 14.8.1 External resistance division method

Figure 14-24 shows examples of LCD drive voltage connection, corresponding to each bias method.

**Figure 14-24. Examples of LCD Drive Power Connections (External Resistance Division Method) (1/2)**



**Notes 1.** Connect  $V_{L1}$  and  $V_{L2}$  to GND or leave open.

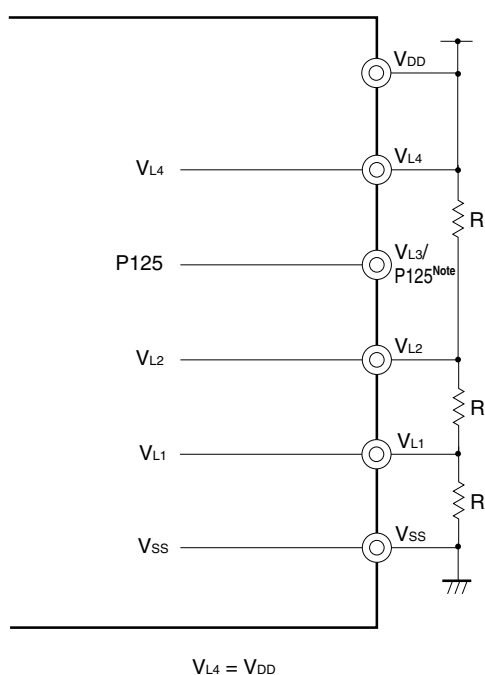
**2.**  $V_{L3}$  can be used as port (P125).

**Note**  $V_{L3}$  can be used as port (P125).

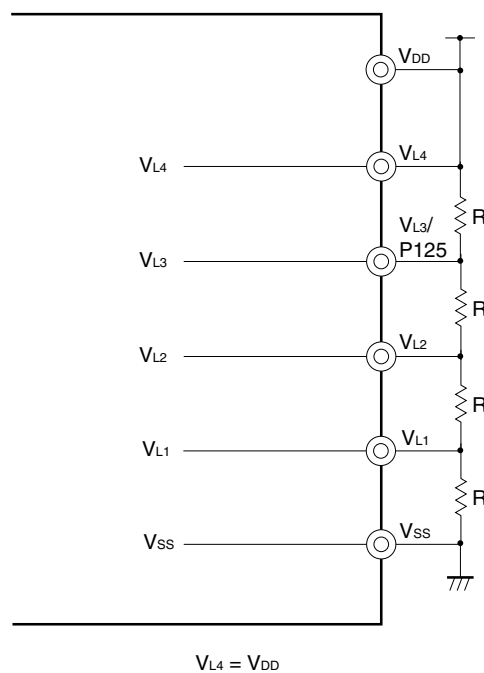
**Caution** To stabilize the potential of the  $V_{L1}$  to  $V_{L4}$  pins, it is recommended to connect a capacitor of about 0.1  $\mu\text{F}$  between each of the pins from  $V_{L1}$  to  $V_{L4}$  and the GND pin as needed.

Figure 14-24. Examples of LCD Drive Power Connections (External Resistance Division Method) (2/2)

(c) 1/3 bias method



(d) 1/4 bias method



**Note**  $V_{L3}$  can be used as port (P125).

<R> **Caution** The reference resistance “R” value for external resistance division is 10 kΩ to 1 MΩ. In addition, to stabilize the voltage of the  $V_{L1}$  to  $V_{L4}$  pins, connect a capacitor between each of pins  $V_{L1}$  to  $V_{L4}$  and the GND pin as needed. The reference capacitance is about 0.47 μF but it depends on the LCD panel used, the number of segment pins, the number of common pins, the frame frequency, and the operating environment. Thoroughly evaluate these values in accordance with your system and adjust and determine the capacitance.

### 14.8.2 Internal voltage boosting method

RL78/L12 contains an internal voltage boost circuit for generating LCD drive power supplies. The internal voltage boost circuit and external capacitors ( $0.47\ \mu\text{F} \pm 30\%$ ) are used to generate an LCD drive voltage. Only 1/3 bias mode or 1/4 bias mode can be set for the internal voltage boosting method.

The LCD drive voltage of the internal voltage boosting method can supply a constant voltage, regardless of changes in  $V_{DD}$ , because it is a power supply separate from the main unit.

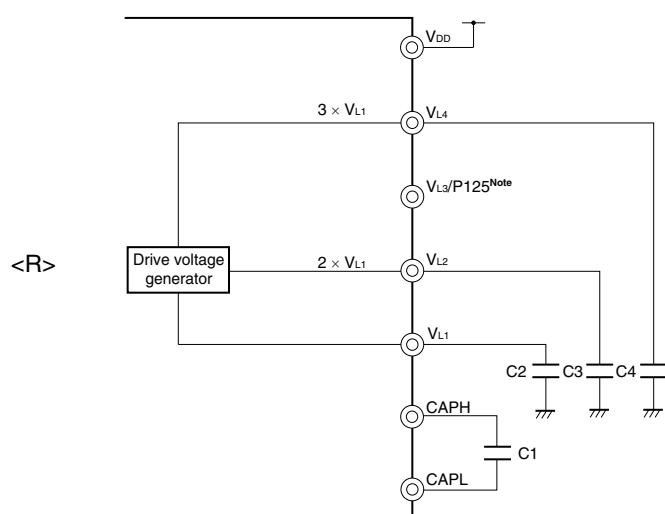
In addition, a contrast can be adjusted by using the LCD boost level control register (VLCD).

**Table 14-12. LCD Drive Voltages (Internal Voltage Boosting Method)**

| Bias Method<br>LCD Drive Voltage Pin | 1/3 Bias Method       | 1/4 Bias Method       |
|--------------------------------------|-----------------------|-----------------------|
| $V_{L4}$                             | $3 \times V_{L1}$     | $4 \times V_{L1}$     |
| $V_{L3}$                             | —                     | $3 \times V_{L1}$     |
| $V_{L2}$                             | $2 \times V_{L1}$     | $2 \times V_{L1}$     |
| $V_{L1}$                             | LCD reference voltage | LCD reference voltage |

**Figure 14-25. Examples of LCD Drive Power Connections (Internal Voltage Boosting Method)**

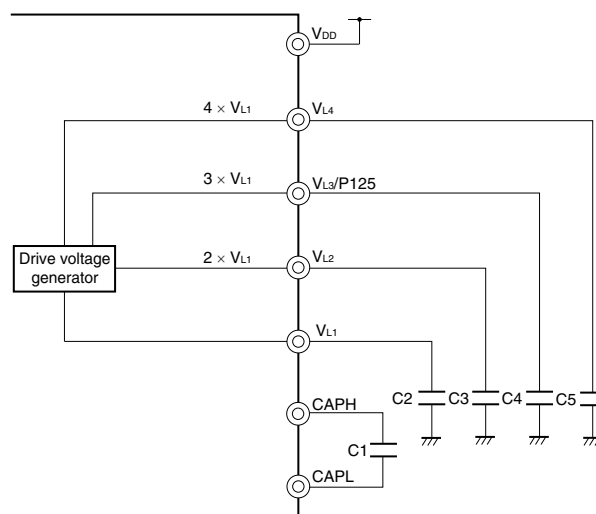
**(a) 1/3 bias method**



**Note**  $V_{L3}$  can be used as port (P125).

**Remark** Use a capacitor with as little leakage as possible.  
In addition, make C1 a nonpolar capacitor.

**(b) 1/4 bias method**



**Remark** Use a capacitor with as little leakage as possible.  
In addition, make C1 a nonpolar capacitor.

### 14.8.3 Capacitor split method

RL78/L12 contains an internal voltage reduction circuit for generating LCD drive power supplies. The internal voltage reduction circuit and external capacitors ( $0.47\ \mu\text{F} \pm 30\%$ ) are used to generate an LCD drive voltage. Only 1/3 bias mode can be set for the capacitor split method.

Different from the external resistance division method, there is always no current flowing with the capacitor split method, so current consumption can be reduced.

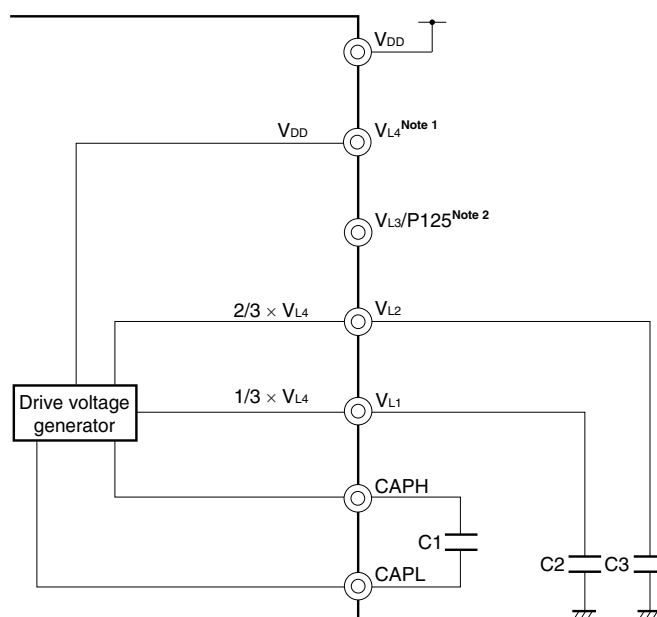
**Table 14-13. LCD Drive Voltages (Capacitor Split Method)**

| Bias Method<br>LCD Drive Voltage Pin | 1/3 Bias Method     |
|--------------------------------------|---------------------|
| $V_{L4}$                             | $V_{DD}$            |
| $V_{L3}$                             | —                   |
| $V_{L2}$                             | $2/3 \times V_{L4}$ |
| $V_{L1}$                             | $1/3 \times V_{L4}$ |

<R>

**Figure 14-26. Examples of LCD Drive Power Connections (Capacitor Split Method)**

• 1/3 bias method



**Notes 1.** When using the internal voltage boosting method, connect the C4 capacitor to this pin as shown in **Figure 14-25. Examples of LCD Drive Power Connections (Internal Voltage Boosting Method).**

**2.**  $V_{L3}$  can be used as port (P125).

**Remark** Use a capacitor with as little leakage as possible.  
In addition, make C1 a nonpolar capacitor.

## 14.9 Common and Segment Signals

### 14.9.1 Normal liquid crystal waveform

Each pixel of the LCD panel turns on when the potential difference between the corresponding common and segment signals becomes higher than a specific voltage (LCD drive voltage,  $V_{LCD}$ ). The pixels turn off when the potential difference becomes lower than  $V_{LCD}$ .

Applying DC voltage to the common and segment signals of an LCD panel causes deterioration. To avoid this problem, this LCD panel is driven by AC voltage.

#### (1) Common signals

Each common signal is selected sequentially according to a specified number of time slices at the timing listed in Table 14-14. In the static display mode, the same signal is output to COM0 to COM3.

In the two-time-slice mode, leave the COM2 and COM3 pins open. In the three-time-slice mode, leave the COM3 pin open.

Use the COM4 to COM7 pins other than in the eight-time-slice mode as open or segment pins.

**Table 14-14. COM Signals**

| COM Signal<br>Number of<br>Time Slices | COM0 | COM1 | COM2 | COM3 | COM4 | COM5 | COM6 | COM7 |
|----------------------------------------|------|------|------|------|------|------|------|------|
| Static display mode                    |      |      |      |      | Note | Note | Note | Note |
| Two-time-slice mode                    |      |      | Open | Open | Note | Note | Note | Note |
| Three-time-slice mode                  |      |      |      | Open | Note | Note | Note | Note |
| Four-time-slice mode                   |      |      |      |      | Note | Note | Note | Note |
| Eight-time-slice mode                  |      |      |      |      |      |      |      |      |

**Note** Use the pins as open or segment pins.

**(2) Segment signals**

The segment signals correspond to the LCD display data register (see **14.4 LCD Display Data Registers**).

When the number of time slices is eight, bits 0 to 7 of each display data register are read in synchronization with COM0 to COM7, respectively. If a bit is 1, it is converted to the select voltage, and if it is 0, it is converted to the deselect voltage. The conversion results are output to the segment pins (SEG4 to SEG38).

When the number of time slices is number other than eight, bits 0 to 3 of each byte in A-pattern area are read in synchronization with COM0 to COM3, and bits 4 to 7 of each byte in B-pattern area are read in synchronization with COM0 to COM3, respectively. If a bit is 1, it is converted to the select voltage, and if it is 0, it is converted to the deselect voltage. The conversion results are output to the segment pins (SEG0 to SEG38).

Check, with the information given above, what combination of front-surface electrodes (corresponding to the segment signals) and rear-surface electrodes (corresponding to the common signals) forms display patterns in the LCD display data register, and write the bit data that corresponds to the desired display pattern on a one-to-one basis.

**Remark** The mounted segment output pins vary depending on the product.

- 32-pin products: SEG0, SEG4 to SEG6, SEG19 to SEG21, SEG27 to SEG32
- 44-pin products: SEG0 to SEG6, SEG17 to SEG21, SEG25 to SEG34
- 48-pin products: SEG0 to SEG7, SEG16 to SEG21, SEG24 to SEG35
- 52-pin products: SEG0 to SEG8, SEG15 to SEG21, SEG23 to SEG36
- 64-pin products: SEG0 to SEG38



**(3) Output waveforms of common and segment signals**

The voltages listed in Table 14-15 are output as common and segment signals.

When both common and segment signals are at the select voltage, a display on-voltage of  $\pm V_{LCD}$  is obtained. The other combinations of the signals correspond to the display off-voltage.

**Table 14-15. LCD Drive Voltage****(a) Static display mode**

| Segment Signal  |  | Select Signal Level | Deselect Signal Level |
|-----------------|--|---------------------|-----------------------|
| Common Signal   |  | $V_{SS}/V_{L4}$     | $V_{L4}/V_{SS}$       |
| $V_{L4}/V_{SS}$ |  | $-V_{LCD}/+V_{LCD}$ | 0 V/0 V               |

**(b) 1/2 bias method**

| Segment Signal        |                 | Select Signal Level                       | Deselect Signal Level                     |
|-----------------------|-----------------|-------------------------------------------|-------------------------------------------|
| Common Signal         |                 | $V_{SS}/V_{L4}$                           | $V_{L4}/V_{SS}$                           |
| Select signal level   | $V_{L4}/V_{SS}$ | $-V_{LCD}/+V_{LCD}$                       | 0 V/0 V                                   |
| Deselect signal level | $V_{L2}$        | $-\frac{1}{2}V_{LCD}/+\frac{1}{2}V_{LCD}$ | $+\frac{1}{2}V_{LCD}/-\frac{1}{2}V_{LCD}$ |

**(c) 1/3 bias method (waveform A or B)**

| Segment Signal        |                 | Select Signal Level                       | Deselect Signal Level                     |
|-----------------------|-----------------|-------------------------------------------|-------------------------------------------|
| Common Signal         |                 | $V_{SS}/V_{L4}$                           | $V_{L2}/V_{L1}$                           |
| Select signal level   | $V_{L4}/V_{SS}$ | $-V_{LCD}/+V_{LCD}$                       | $-\frac{1}{3}V_{LCD}/+\frac{1}{3}V_{LCD}$ |
| Deselect signal level | $V_{L1}/V_{L2}$ | $-\frac{1}{3}V_{LCD}/+\frac{1}{3}V_{LCD}$ | $+\frac{1}{3}V_{LCD}/-\frac{1}{3}V_{LCD}$ |

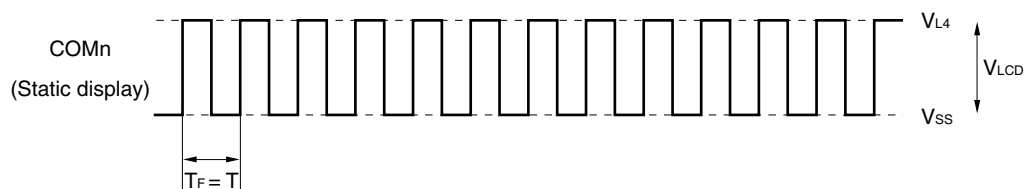
**(d) 1/4 bias method (waveform A or B)**

| Segment Signal        |                 | Select Signal Level                       | Deselect Signal Level                     |
|-----------------------|-----------------|-------------------------------------------|-------------------------------------------|
| Common Signal         |                 | $V_{SS}/V_{L4}$                           | $V_{L2}$                                  |
| Select signal level   | $V_{L4}/V_{SS}$ | $-V_{LCD}/+V_{LCD}$                       | $-\frac{1}{2}V_{LCD}/+\frac{1}{2}V_{LCD}$ |
| Deselect signal level | $V_{L1}/V_{L3}$ | $-\frac{1}{4}V_{LCD}/+\frac{1}{4}V_{LCD}$ | $+\frac{1}{4}V_{LCD}/-\frac{1}{4}V_{LCD}$ |

Figure 14-27 shows the common signal waveforms, and Figure 14-28 shows the voltages and phases of the common and segment signals.

**Figure 14-27. Common Signal Waveforms (1/2)**

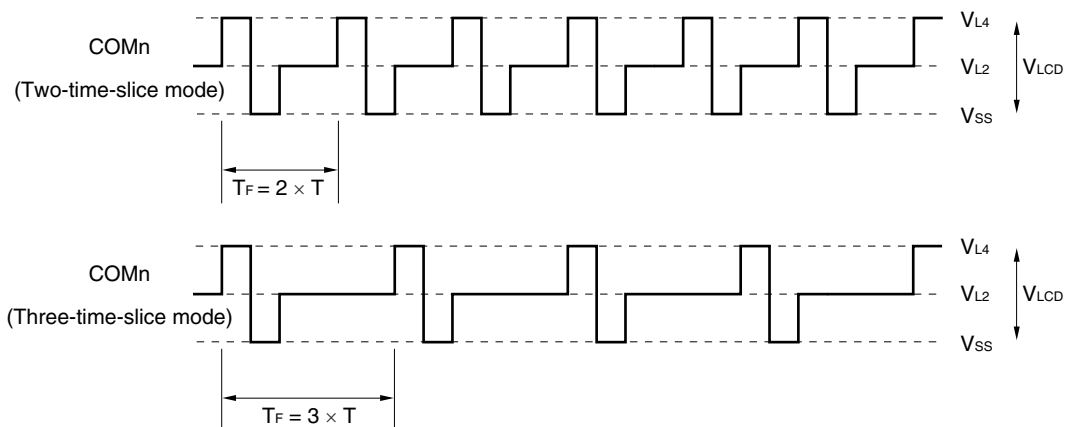
**(a) Static display mode**



T: One LCD clock period

$T_F$ : Frame frequency

**(b) 1/2 bias method**

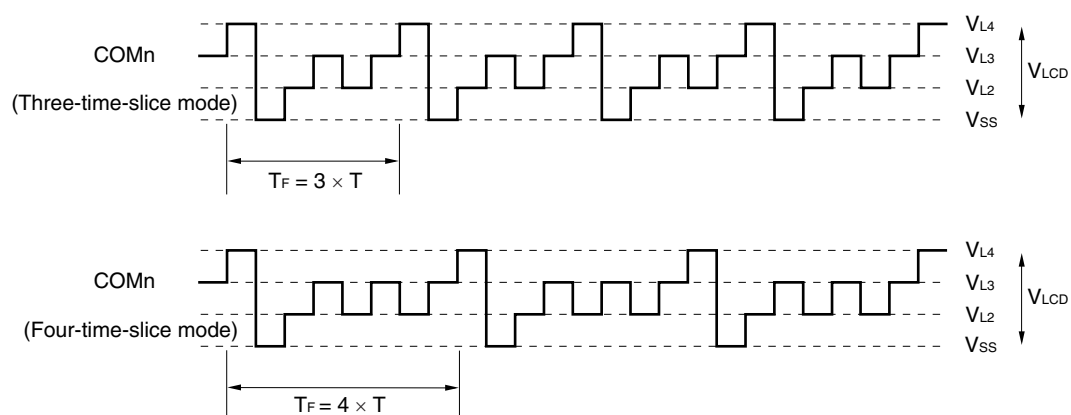


T: One LCD clock period

$T_F$ : Frame frequency

Figure 14-27. Common Signal Waveforms (2/2)

## (c) 1/3 bias method



T: One LCD clock period

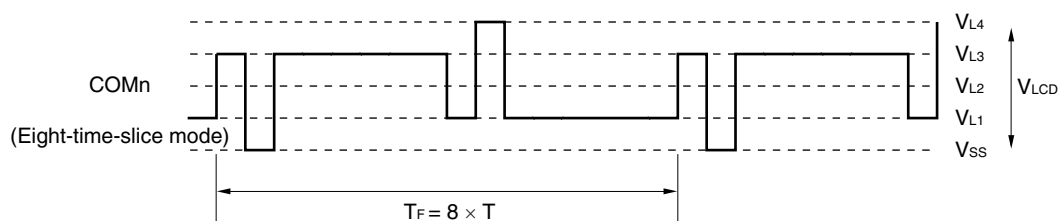
 $T_F$ : Frame frequency

&lt; Example of calculation of LCD frame frequency (When four-time slot mode is used) &gt;

LCD clock:  $32768/2^8 = 256$  Hz (When setting to LCDC0 = 07H)

LCD frame frequency: 64 Hz

## (d) 1/4 bias method



T: One LCD clock period

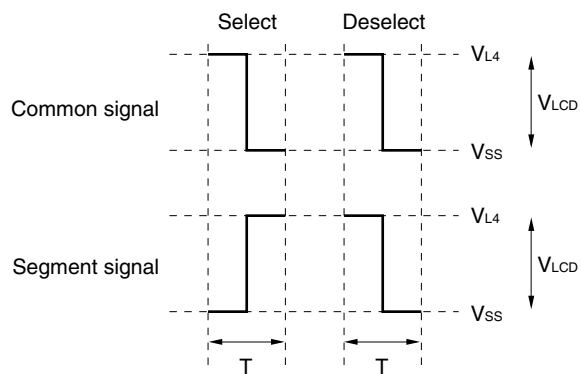
 $T_F$ : Frame frequency

&lt; Example of calculation of LCD frame frequency (When eight-time slot mode is used) &gt;

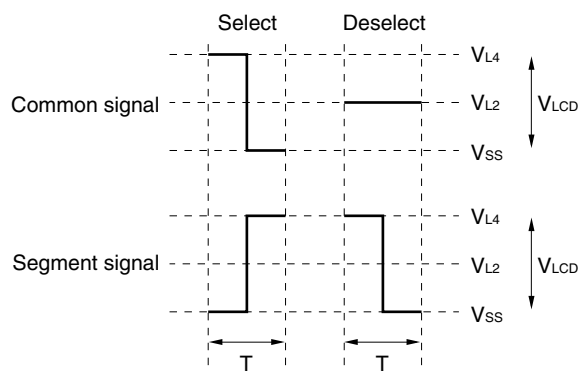
LCD clock:  $32768/2^8 = 256$  Hz (When setting to LCDC0 = 07H)

LCD frame frequency: 32 Hz

Figure 14-28. Voltages and Phases of Common and Segment Signals (1/3)

**(a) Static display mode (waveform A)**

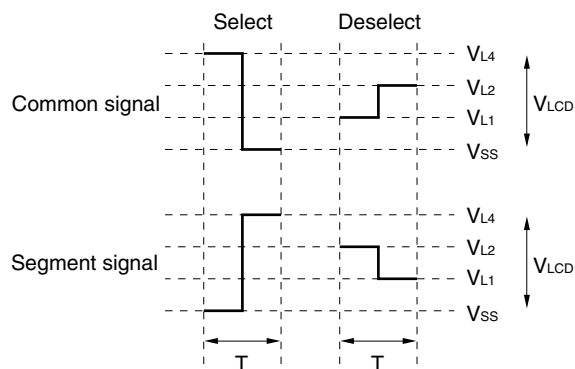
T: One LCD clock period

**(b) 1/2 bias method (waveform A)**

T: One LCD clock period

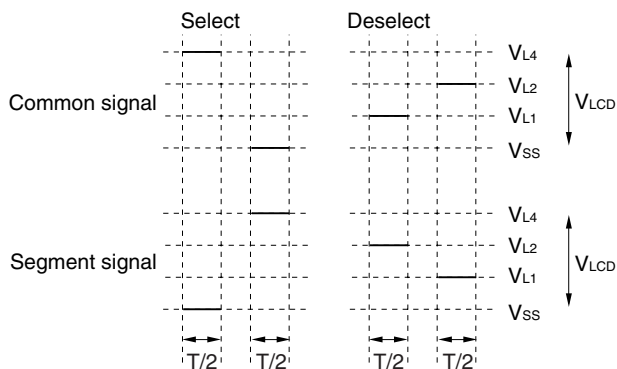
Figure 14-28. Voltages and Phases of Common and Segment Signals (2/3)

## (c) 1/3 bias method (waveform A)



T: One LCD clock period

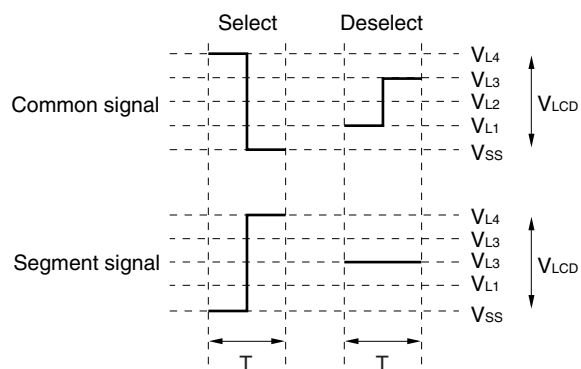
## (d) 1/3 bias method (waveform B)



T: One LCD clock period

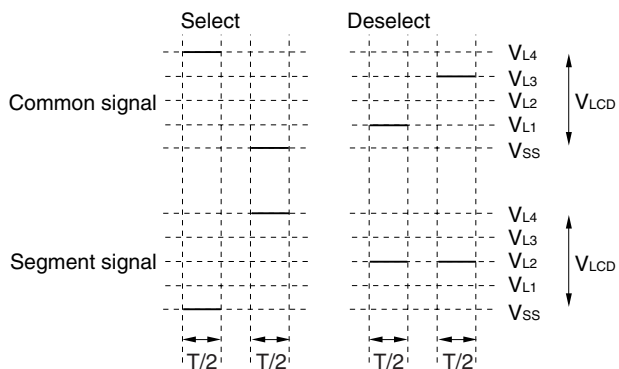
Figure 14-28. Voltages and Phases of Common and Segment Signals (3/3)

## (e) 1/4 bias method (waveform A)



T: One LCD clock period

## (f) 1/4 bias method (waveform B)



T: One LCD clock period

## 14.10 Display Modes

### 14.10.1 Static display example

Figure 14-30 shows how the three-digit LCD panel having the display pattern shown in Figure 14-29 is connected to the segment signals (SEG0 to SEG23) and the common signal (COM0). This example displays data “12.3” in the LCD panel. The contents of the display data register (F0400H to F0417H) correspond to this display.

The following description focuses on numeral “2.” (2.) displayed in the second digit. To display “2.” in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG8 to SEG15 pins according to Table 14-16 at the timing of the common signal COM0; see Figure 14-29 for the relationship between the segment signals and LCD segments.

**Table 14-16. Select and Deselect Voltages (COM0)**

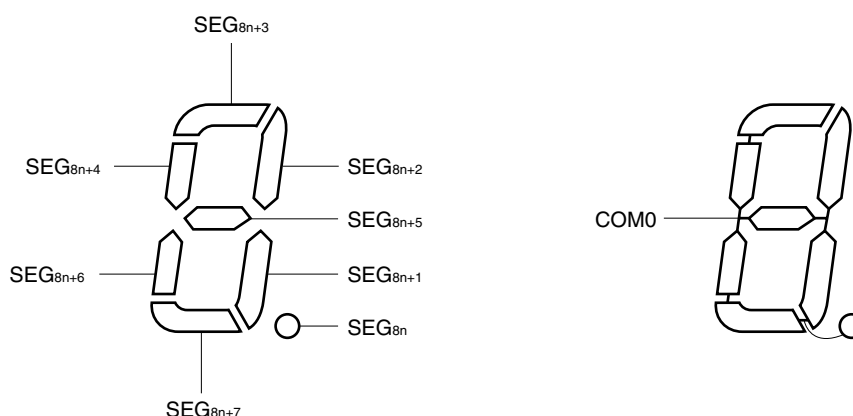
| Segment \ Common | SEG8   | SEG9     | SEG10  | SEG11  | SEG12    | SEG13  | SEG14  | SEG15  |
|------------------|--------|----------|--------|--------|----------|--------|--------|--------|
| COM0             | Select | Deselect | Select | Select | Deselect | Select | Select | Select |

According to Table 14-16, it is determined that the bit-0 pattern of the display data register locations (F0408H to F040FH) must be 10110111.

Figure 14-31 shows the LCD drive waveforms of SEG11 and SEG12, and COM0. When the select voltage is applied to SEG11 at the timing of COM0, an alternate rectangle waveform,  $+V_{LCD}/-V_{LCD}$ , is generated to turn on the corresponding LCD segment.

COM1 to COM3 are supplied with the same waveform as for COM0. So, COM0 to COM3 may be connected together to increase the driving capacity.

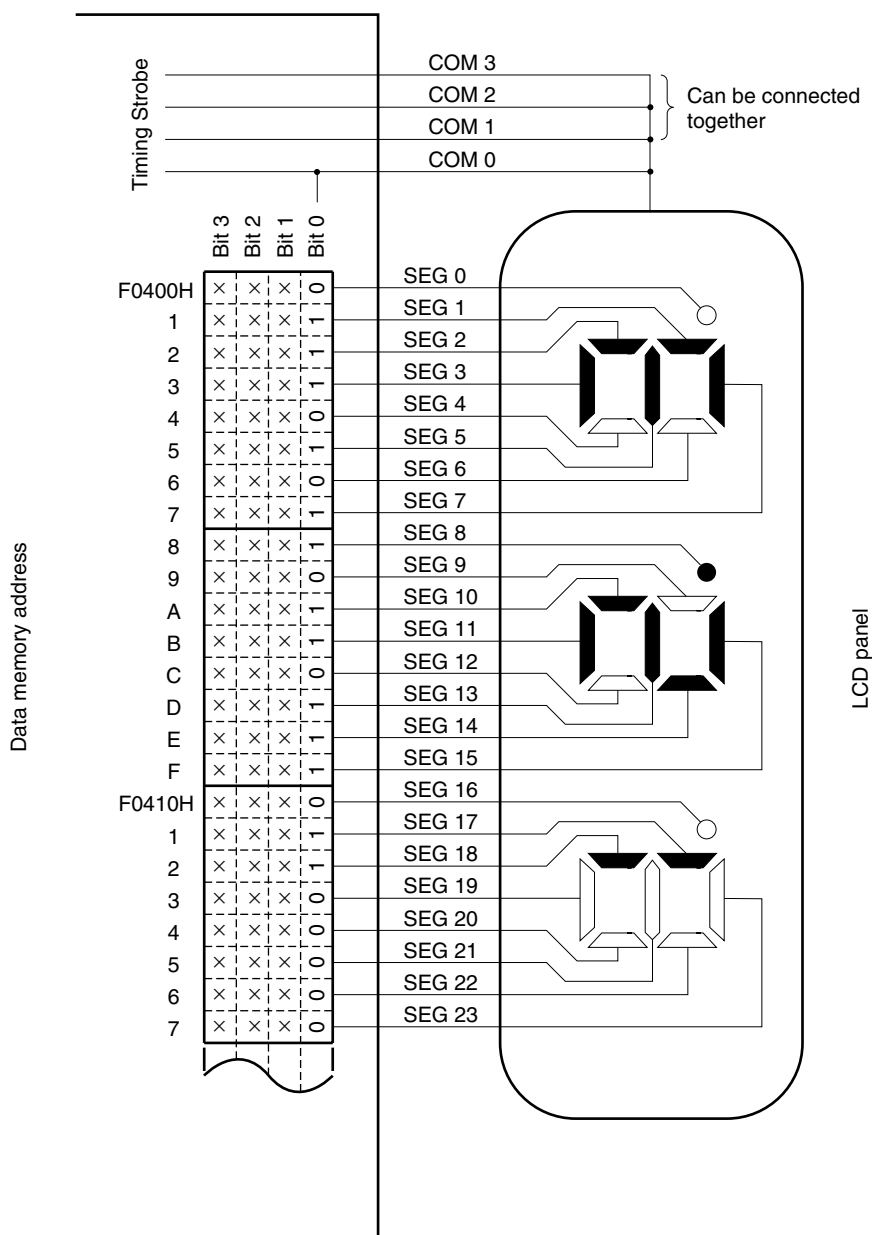
**Figure 14-29. Static LCD Display Pattern and Electrode Connections**



**Remark**

|                       |              |
|-----------------------|--------------|
| 30-pin products:      | $n = 0$      |
| 44-pin products:      | $n = 0, 1$   |
| 48-, 52-pin products: | $n = 0$ to 2 |
| 64-pin products:      | $n = 0$ to 3 |

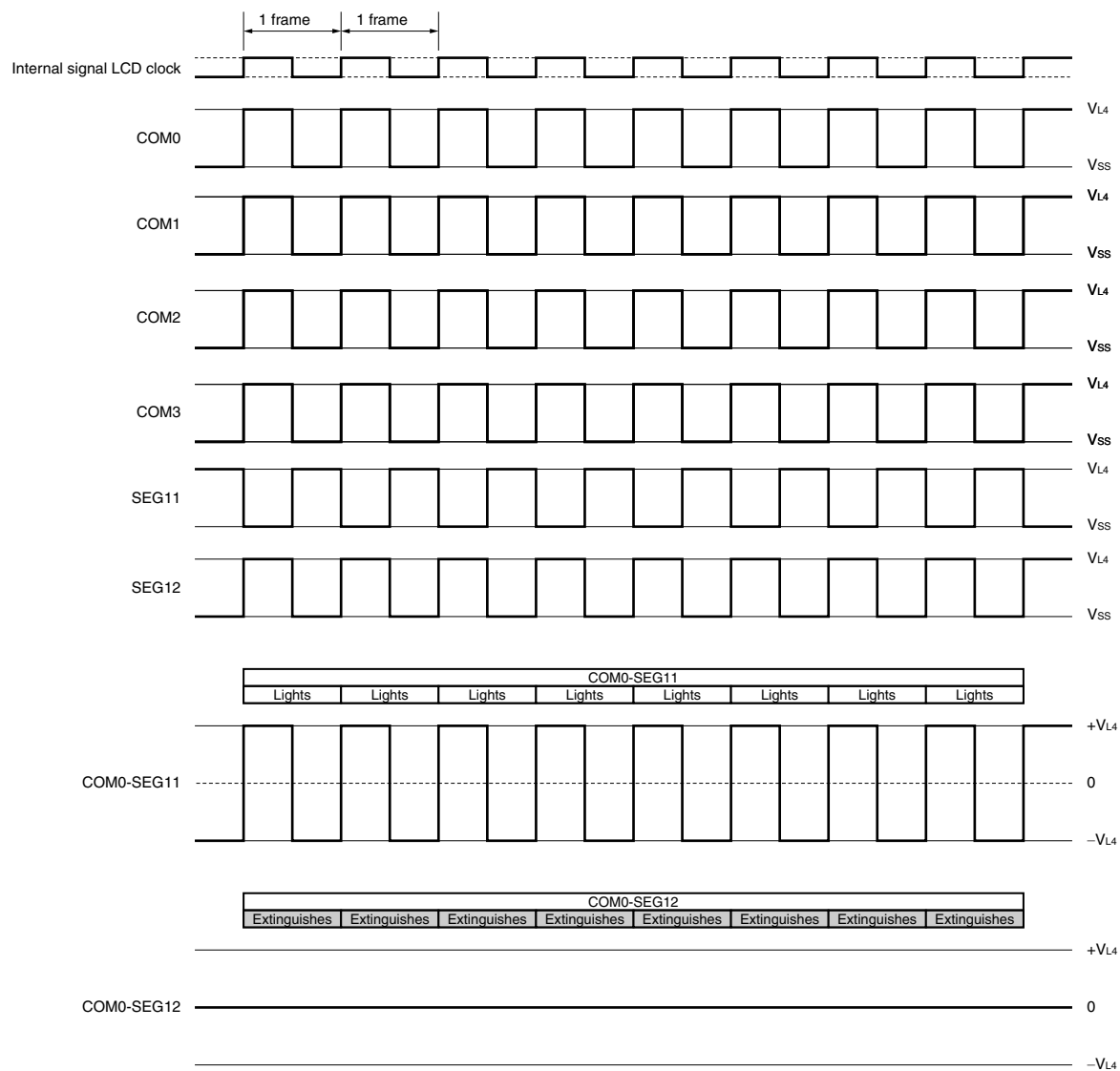
Figure 14-30. Example of Connecting Static LCD Panel



**Remark** x: Don't care.



&lt;R&gt;

**Figure 14-31. Static LCD Drive Waveform Examples for SEG11, SEG12, and COM0**

### 14.10.2 Two-time-slice display example

Figure 14-33 shows how the 6-digit LCD panel having the display pattern shown in Figure 14-32 is connected to the segment signals (SEG0 to SEG23) and the common signals (COM0 and COM1). This example displays data “12345.6” in the LCD panel. The contents of the display data register (F0400H to F0417H) correspond to this display.

The following description focuses on numeral “3” ( 3 ) displayed in the fourth digit. To display “3” in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG12 to SEG15 pins according to Table 14-17 at the timing of the common signals COM0 and COM1; see Figure 14-32 for the relationship between the segment signals and LCD segments.

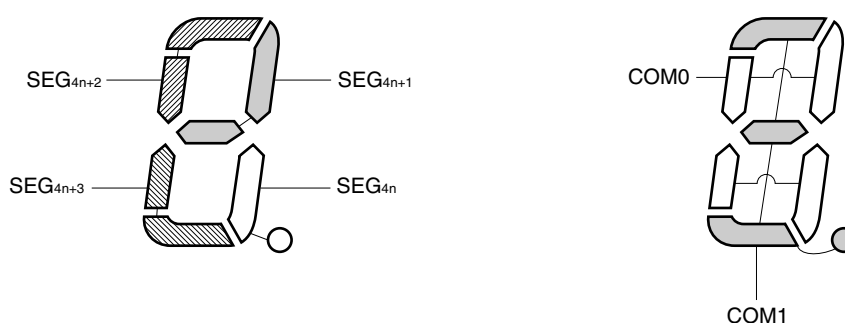
**Table 14-17. Select and Deselect Voltages (COM0 and COM1)**

| Segment | SEG12    | SEG13  | SEG14    | SEG15    |
|---------|----------|--------|----------|----------|
| Common  |          |        |          |          |
| COM0    | Select   | Select | Deselect | Deselect |
| COM1    | Deselect | Select | Select   | Select   |

According to Table 14-17, it is determined that the display data register location (F040FH) that corresponds to SEG15 must contain  $xx10$ .

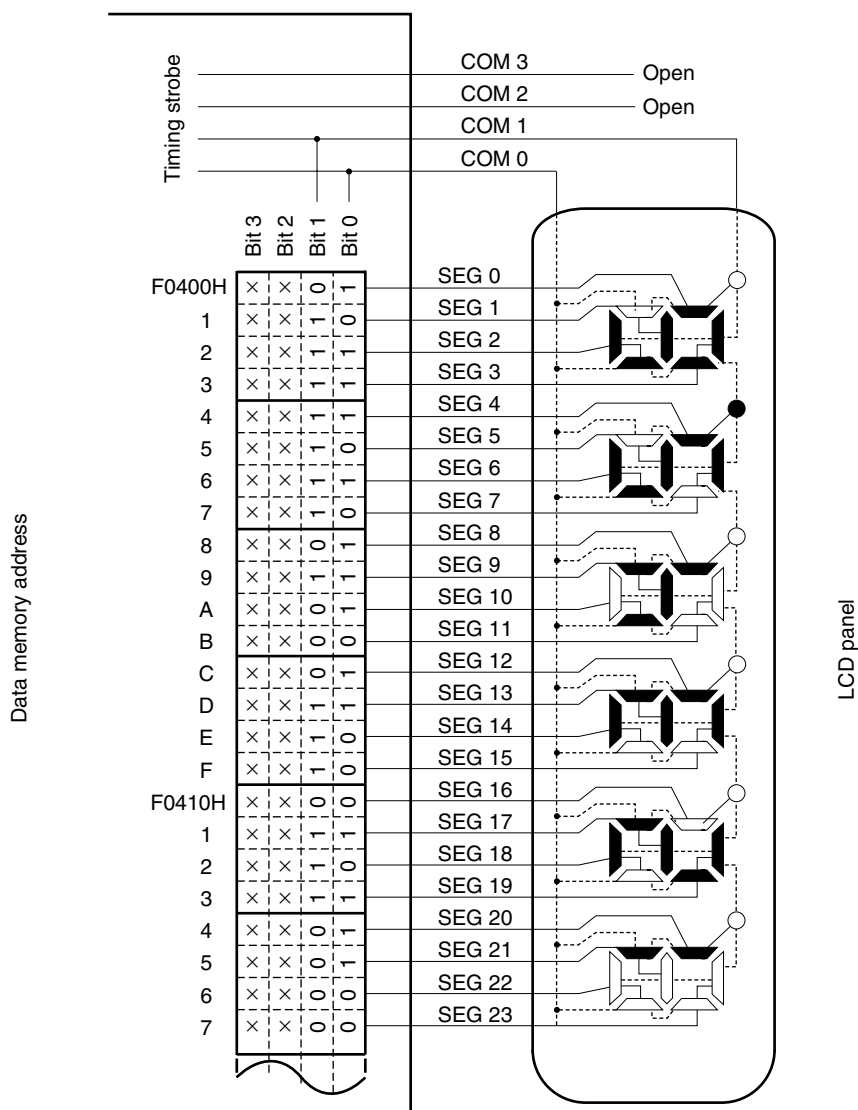
Figure 14-34 shows examples of LCD drive waveforms between the SEG15 signal and each common signal. When the select voltage is applied to SEG15 at the timing of COM1, an alternate rectangle waveform,  $+V_{LCD}/-V_{LCD}$ , is generated to turn on the corresponding LCD segment.

**Figure 14-32. Two-Time-Slice LCD Display Pattern and Electrode Connections**



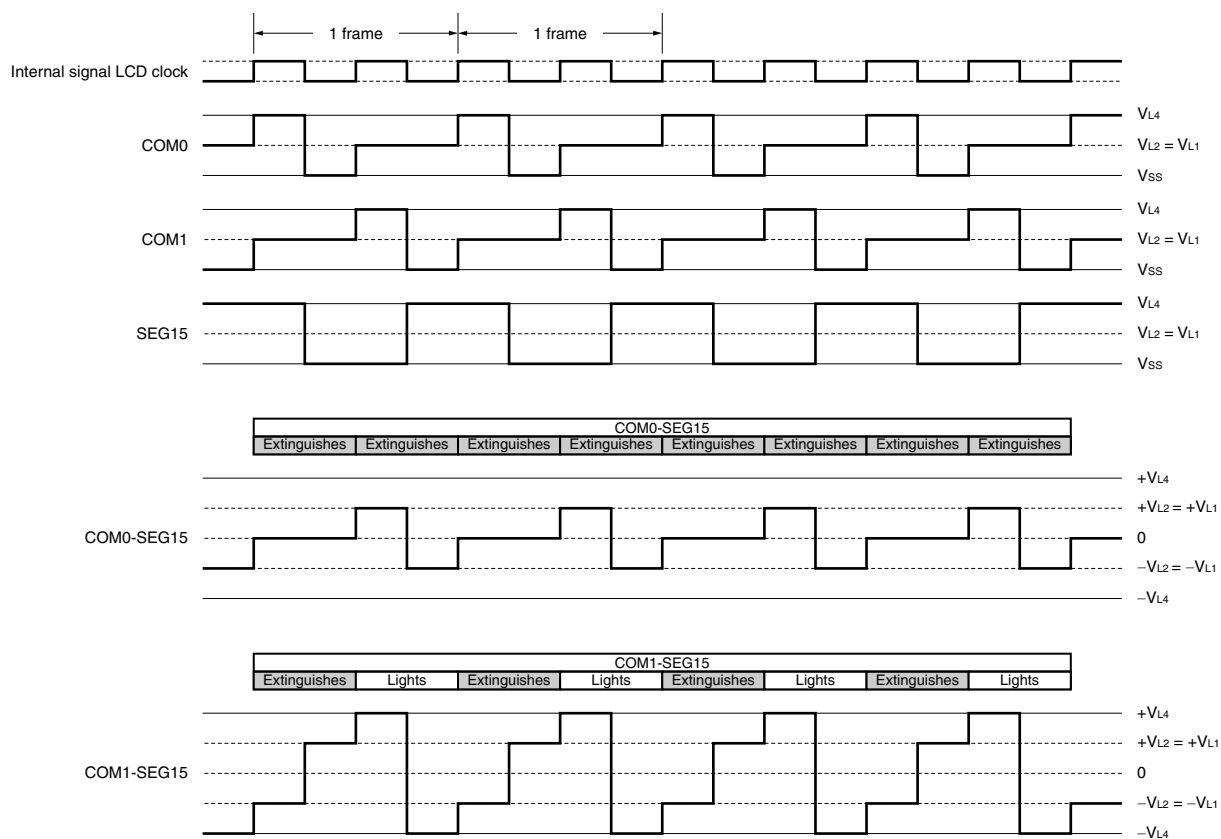
**Remark** 30-pin products:  $n = 0$  to 2  
 44-pin products:  $n = 0$  to 4  
 48-pin products:  $n = 0$  to 5  
 52-pin products:  $n = 0$  to 6  
 64-pin products:  $n = 0$  to 8

Figure 14-33. Example of Connecting Two-Time-Slice LCD Panel



**Remark** x: Don't care.

**Figure 14-34. Two-Time-Slice LCD Drive Waveform Examples Between SEG15 and Each Common Signals  
(1/2 Bias Method)**



### 14.10.3 Three-time-slice display example

Figure 14-36 shows how the 8-digit LCD panel having the display pattern shown in Figure 14-35 is connected to the segment signals (SEG0 to SEG23) and the common signals (COM0 to COM2). This example displays data “123456.78” in the LCD panel. The contents of the display data register (addresses F0400H to F0417H) correspond to this display.

The following description focuses on numeral “6.” ( ) displayed in the third digit. To display “6.” in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG6 to SEG8 pins according to Table 14-18 at the timing of the common signals COM0 to COM2; see Figure 14-35 for the relationship between the segment signals and LCD segments.

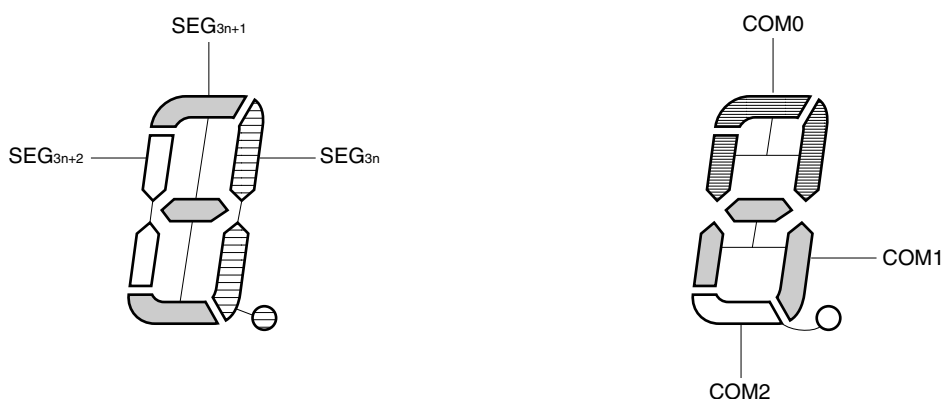
**Table 14-18. Select and Deselect Voltages (COM0 to COM2)**

| Segment<br>Common | SEG6     | SEG7   | SEG8   |
|-------------------|----------|--------|--------|
| COM0              | Deselect | Select | Select |
| COM1              | Select   | Select | Select |
| COM2              | Select   | Select | –      |

According to Table 14-18, it is determined that the display data register location (F0406H) that corresponds to SEG6 must contain x110.

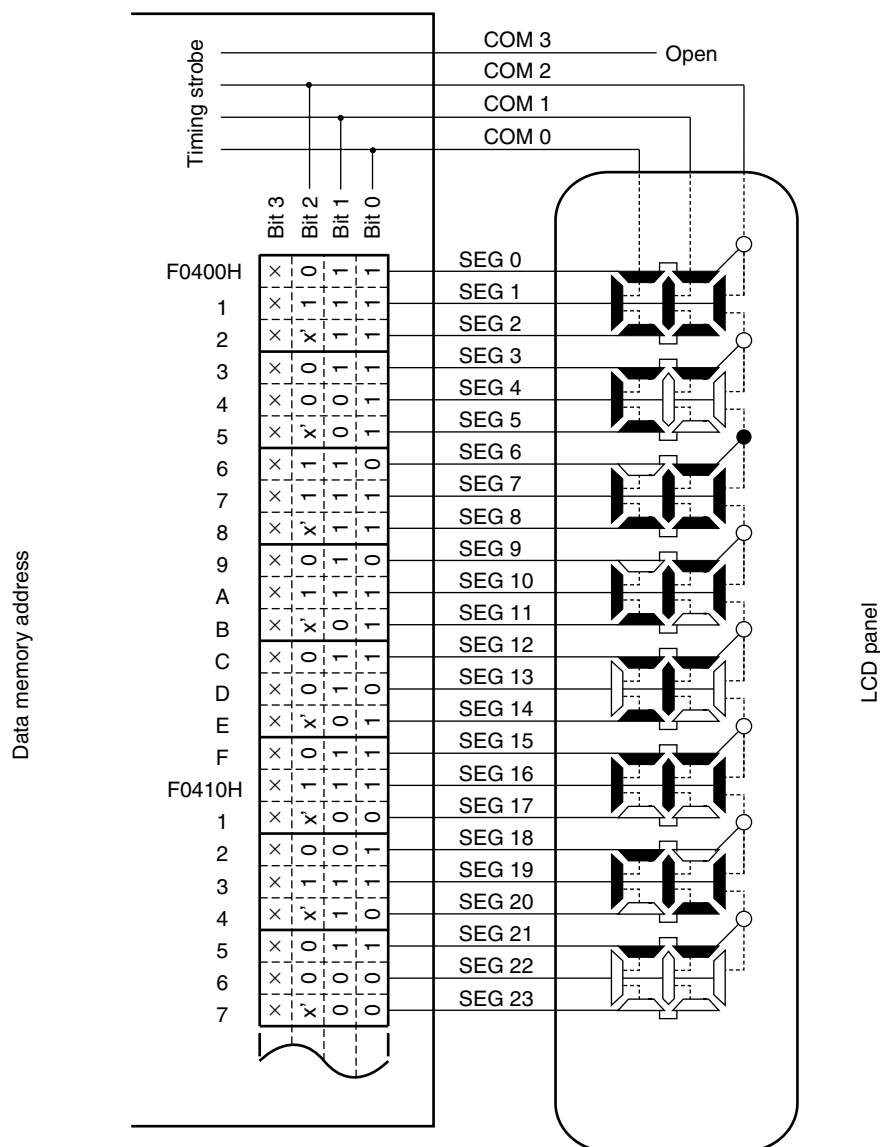
Figures 14-37 and 14-38 show examples of LCD drive waveforms between the SEG6 signal and each common signal in the 1/2 and 1/3 bias methods, respectively. When the select voltage is applied to SEG6 at the timing of COM1 or COM2, an alternate rectangle waveform,  $+V_{LCD}/-V_{LCD}$ , is generated to turn on the corresponding LCD segment.

**Figure 14-35. Three-Time-Slice LCD Display Pattern and Electrode Connections**



**Remark** 30-pin products:  $n = 0$  to 3  
 44-pin products:  $n = 0$  to 6  
 48-pin products:  $n = 0$  to 7  
 52-pin products:  $n = 0$  to 9  
 64-pin products:  $n = 0$  to 12

Figure 14-36. Example of Connecting Three-Time-Slice LCD Panel



**Remark** x: Don't care.

x': Can be used to store any data because there is no corresponding segment in the LCD panel.

**Figure 14-37. Three-Time-Slice LCD Drive Waveform Examples Between SEG6 and Each Common Signals (1/2 Bias Method)**

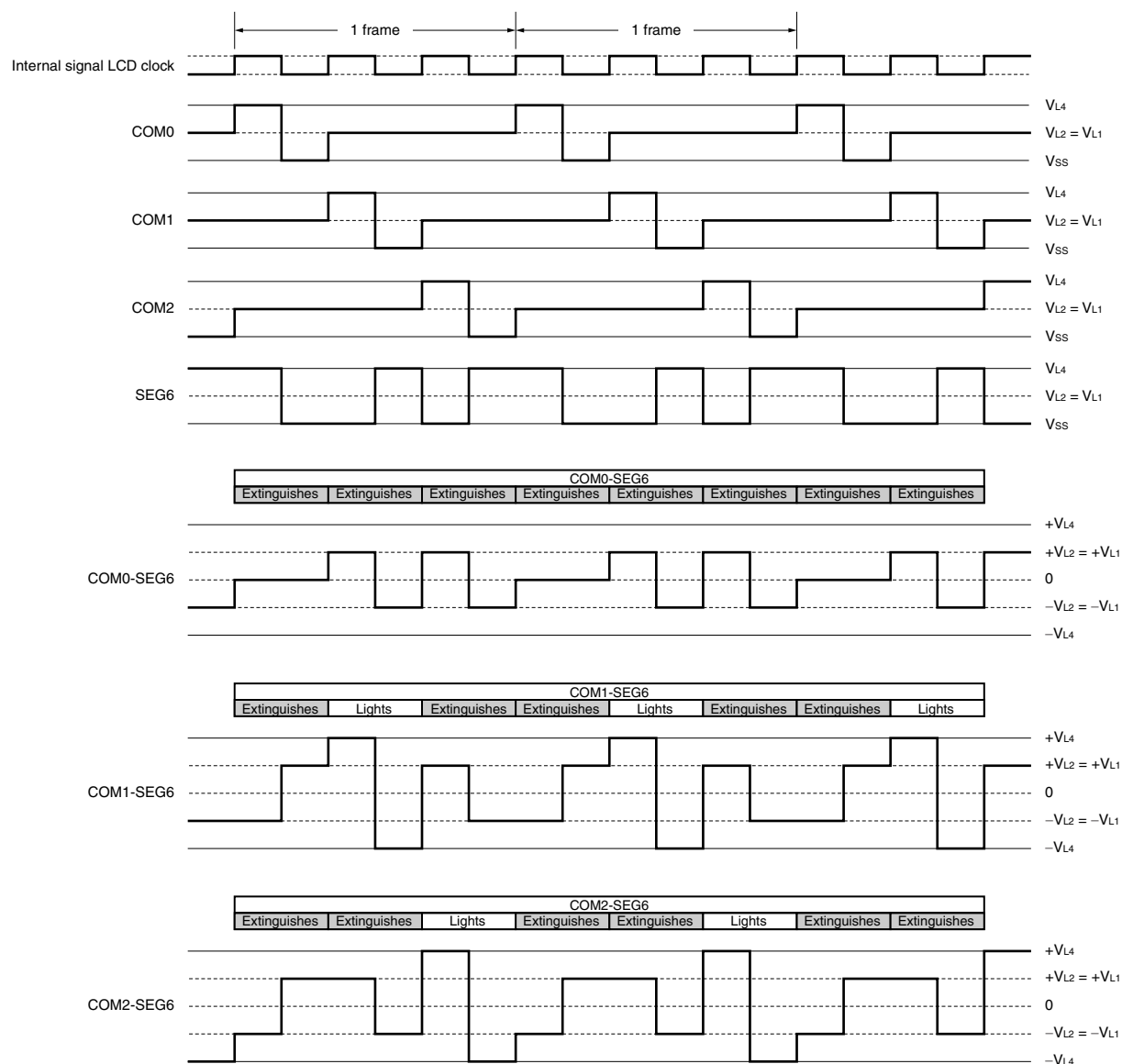
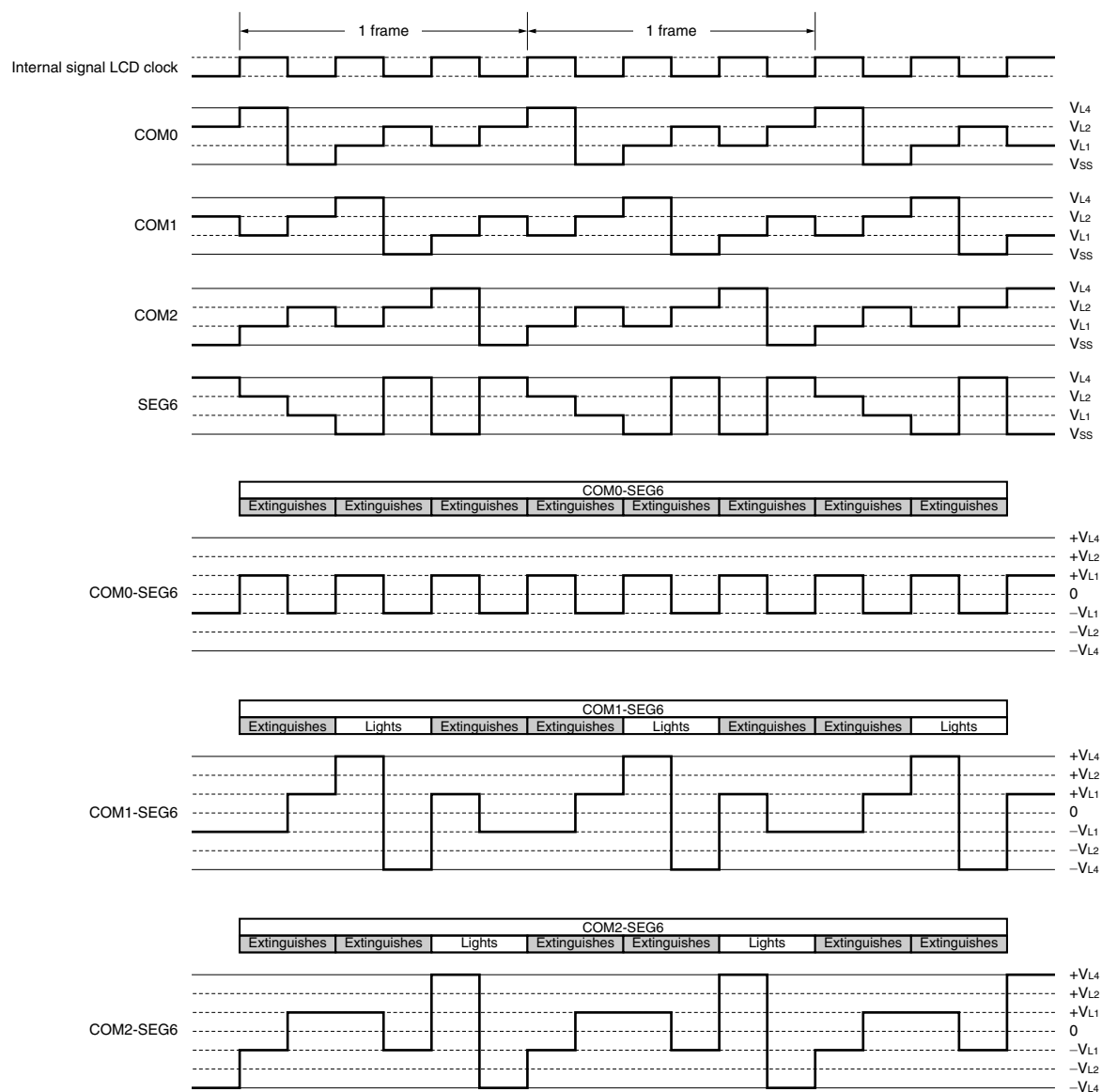


**Figure 14-38. Three-Time-Slice LCD Drive Waveform Examples Between SEG6 and Each Common Signals  
(1/3 Bias Method)**





#### 14.10.4 Four-time-slice display example

Figure 14-40 shows how the 12-digit LCD panel having the display pattern shown in Figure 14-39 is connected to the segment signals (SEG0 to SEG23) and the common signals (COM0 to COM3). This example displays data “123456.789012” in the LCD panel. The contents of the display data register (addresses F0400H to F0417H) correspond to this display.

The following description focuses on numeral “6.” (6.) displayed in the seventh digit. To display “6.” in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG12 and SEG13 pins according to Table 14-19 at the timing of the common signals COM0 to COM3; see Figure 14-39 for the relationship between the segment signals and LCD segments.

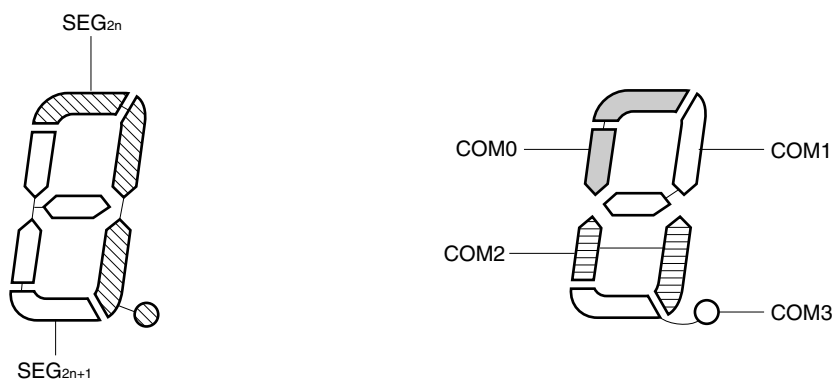
**Table 14-19. Select and Deselect Voltages (COM0 to COM3)**

| Segment<br>Common | SEG12    | SEG13  |
|-------------------|----------|--------|
| COM0              | Select   | Select |
| COM1              | Deselect | Select |
| COM2              | Select   | Select |
| COM3              | Select   | Select |

According to Table 14-19, it is determined that the display data register location (F040CH) that corresponds to SEG12 must contain 1101.

Figure 14-41 shows examples of LCD drive waveforms between the SEG12 signal and each common signal. When the select voltage is applied to SEG12 at the timing of COM0, an alternate rectangle waveform,  $+V_{LCD}/-V_{LCD}$ , is generated to turn on the corresponding LCD segment.

**Figure 14-39. Four-Time-Slice LCD Display Pattern and Electrode Connections**



**Remark** 30-pin products:  $n = 0$  to 5  
 44-pin products:  $n = 0$  to 10  
 48-pin products:  $n = 0$  to 12  
 52-pin products:  $n = 0$  to 14  
 64-pin products:  $n = 0$  to 18

Figure 14-40. Example of Connecting Four-Time-Slice LCD Panel

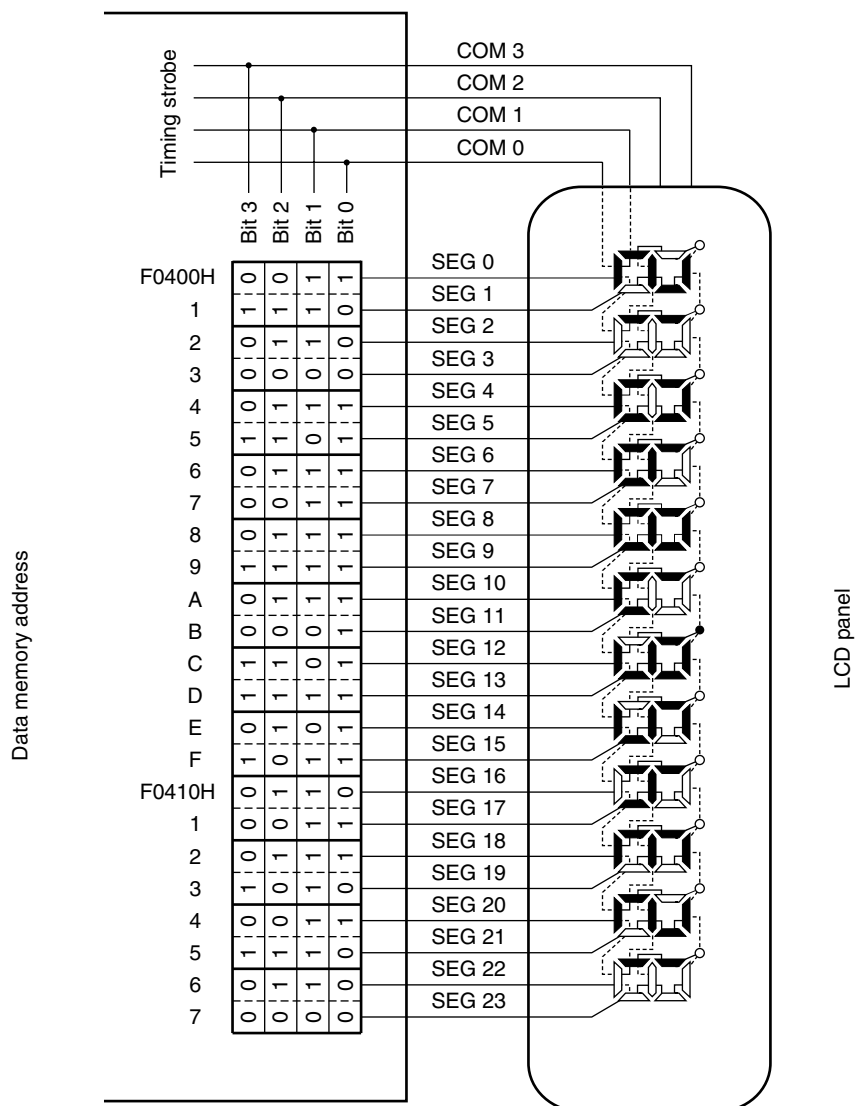


**Figure 14-41. Four-Time-Slice LCD Drive Waveform Examples Between SEG12 and Each Common Signals  
(1/3 Bias Method) (1/2)**

**(a) Waveform A**

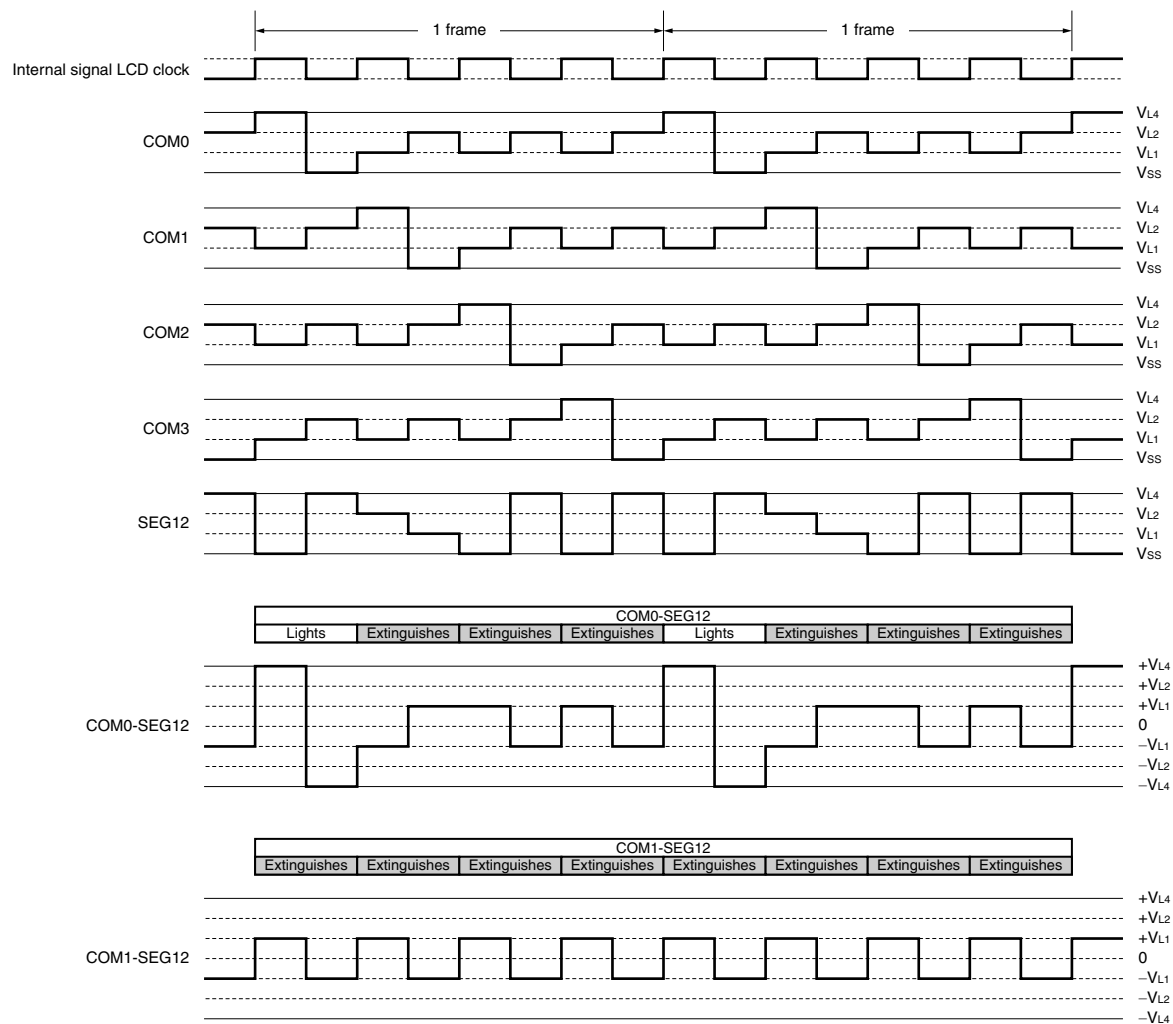
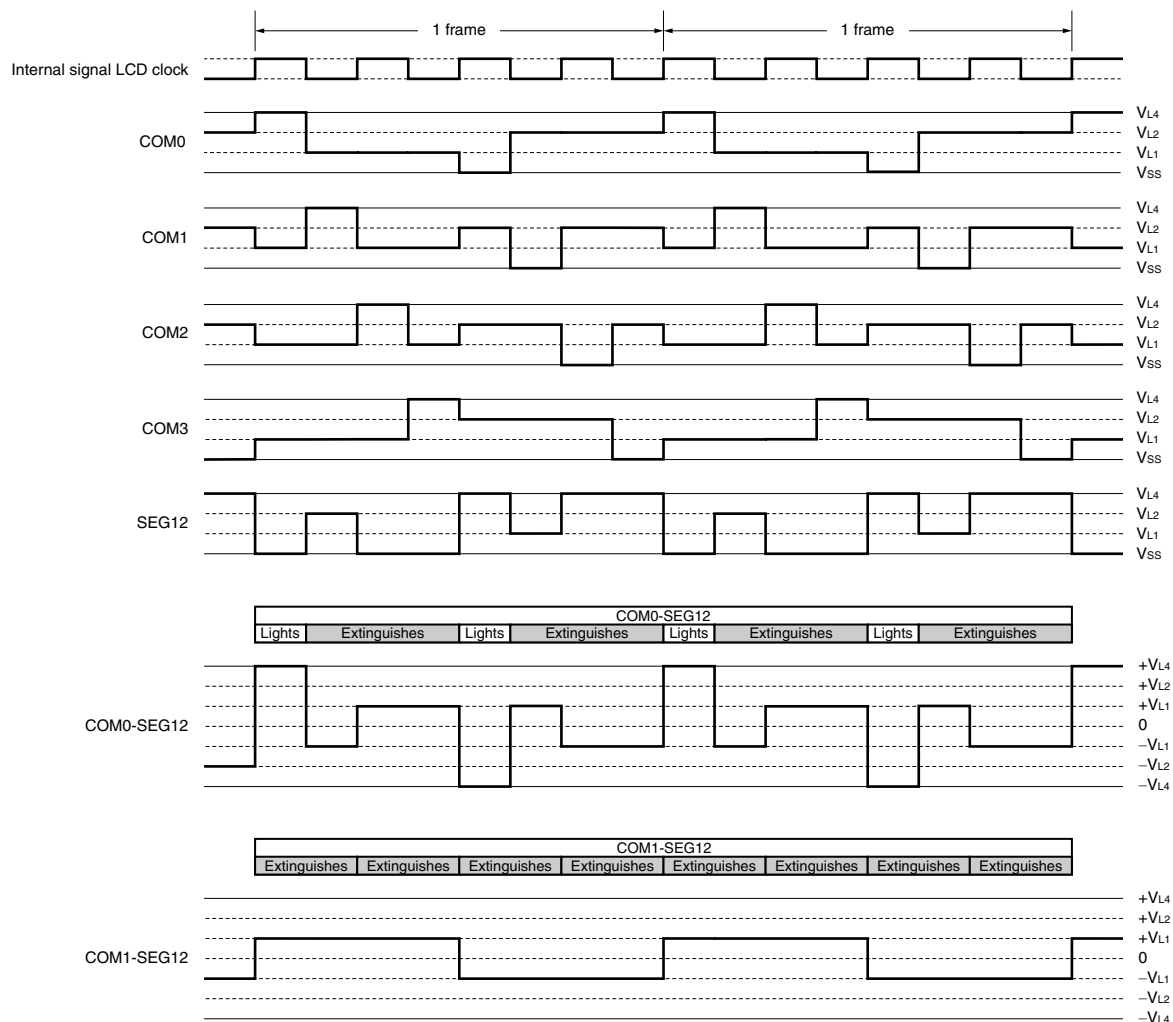


**Figure 14-41. Four-Time-Slice LCD Drive Waveform Examples Between SEG12 and Each Common Signals  
(1/3 Bias Method) (2/2)**

**(b) Waveform B**



### 14.10.5 Eight-time-slice display example

Figure 14-43 shows how the 15x8 dot LCD panel having the display pattern shown in Figure 14-42 is connected to the segment signals (SEG4 to SEG18) and the common signals (COM0 to COM7). This example displays data “123” in the LCD panel. The contents of the display data register (addresses F0404H to F0412H) correspond to this display.

The following description focuses on numeral “3.” ( 3 ) displayed in the first digit. To display “3.” in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG4 to SEG8 pins according to Table 14-20 at the timing of the common signals COM0 to COM7; see Figure 14-42 for the relationship between the segment signals and LCD segments.

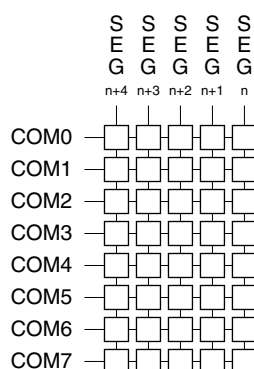
**Table 14-20. Select and Deselect Voltages (COM0 to COM7)**

| Segment<br>Common | SEG4     | SEG5     | SEG6     | SEG7     | SEG8     |
|-------------------|----------|----------|----------|----------|----------|
| COM0              | Select   | Select   | Select   | Select   | Select   |
| COM1              | Deselect | Select   | Deselect | Deselect | Deselect |
| COM2              | Deselect | Deselect | Select   | Deselect | Deselect |
| COM3              | Deselect | Select   | Deselect | Deselect | Deselect |
| COM4              | Select   | Deselect | Deselect | Deselect | Deselect |
| COM5              | Select   | Deselect | Deselect | Deselect | Select   |
| COM6              | Deselect | Select   | Select   | Select   | Deselect |
| COM7              | Deselect | Deselect | Deselect | Deselect | Deselect |

According to Table 14-21, it is determined that the display data register location (F0404H) that corresponds to SEG4 must contain 00110001.

Figure 14-44 shows examples of LCD drive waveforms between the SEG4 signal and each common signal. When the select voltage is applied to SEG4 at the timing of COM0, a waveform is generated to turn on the corresponding LCD segment.

**Figure 14-42. Eight-Time-Slice LCD Display Pattern and Electrode Connections**



**Remark** 30-pin products:  $n = 4$  to 8  
 44-pin products:  $n = 4$  to 17  
 48-pin products:  $n = 4$  to 21  
 52-pin products:  $n = 4$  to 25  
 64-pin products:  $n = 4$  to 34

Figure 14-43. Example of Connecting Eight-Time-Slice LCD Panel

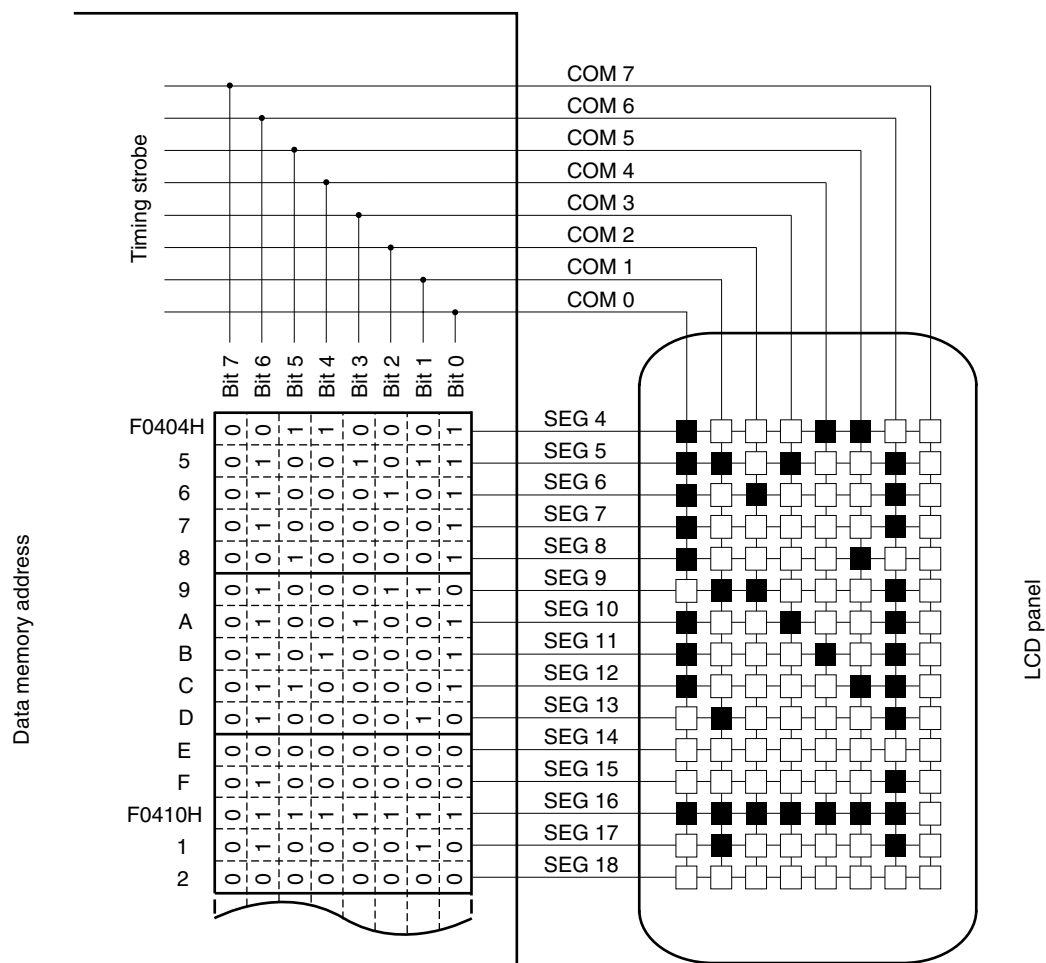


**Figure 14-44. Eight-Time-Slice LCD Drive Waveform Examples Between SEG4 and Each Common Signals  
(1/4 Bias Method) (1/2)**

**(a) Waveform A**

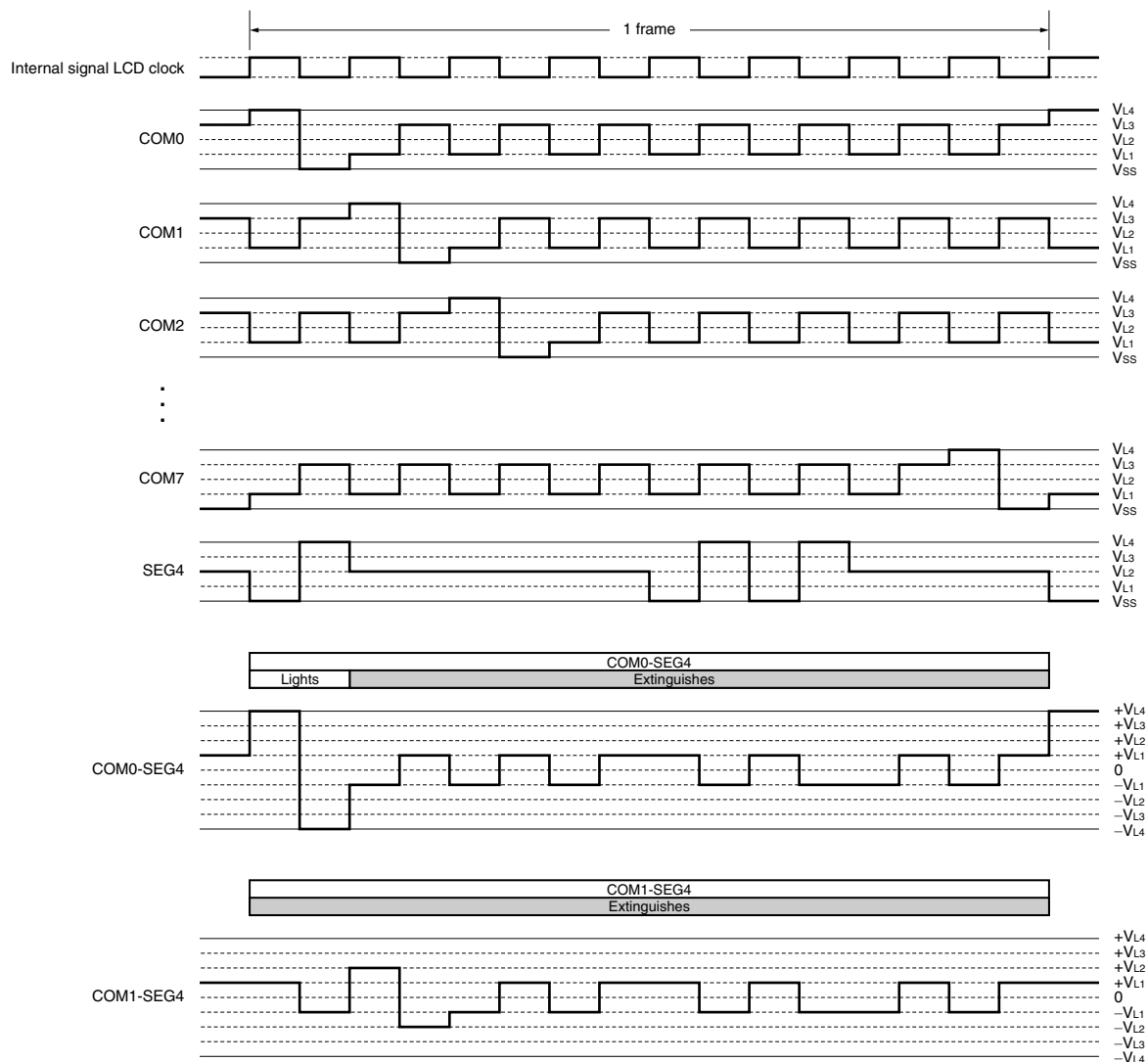
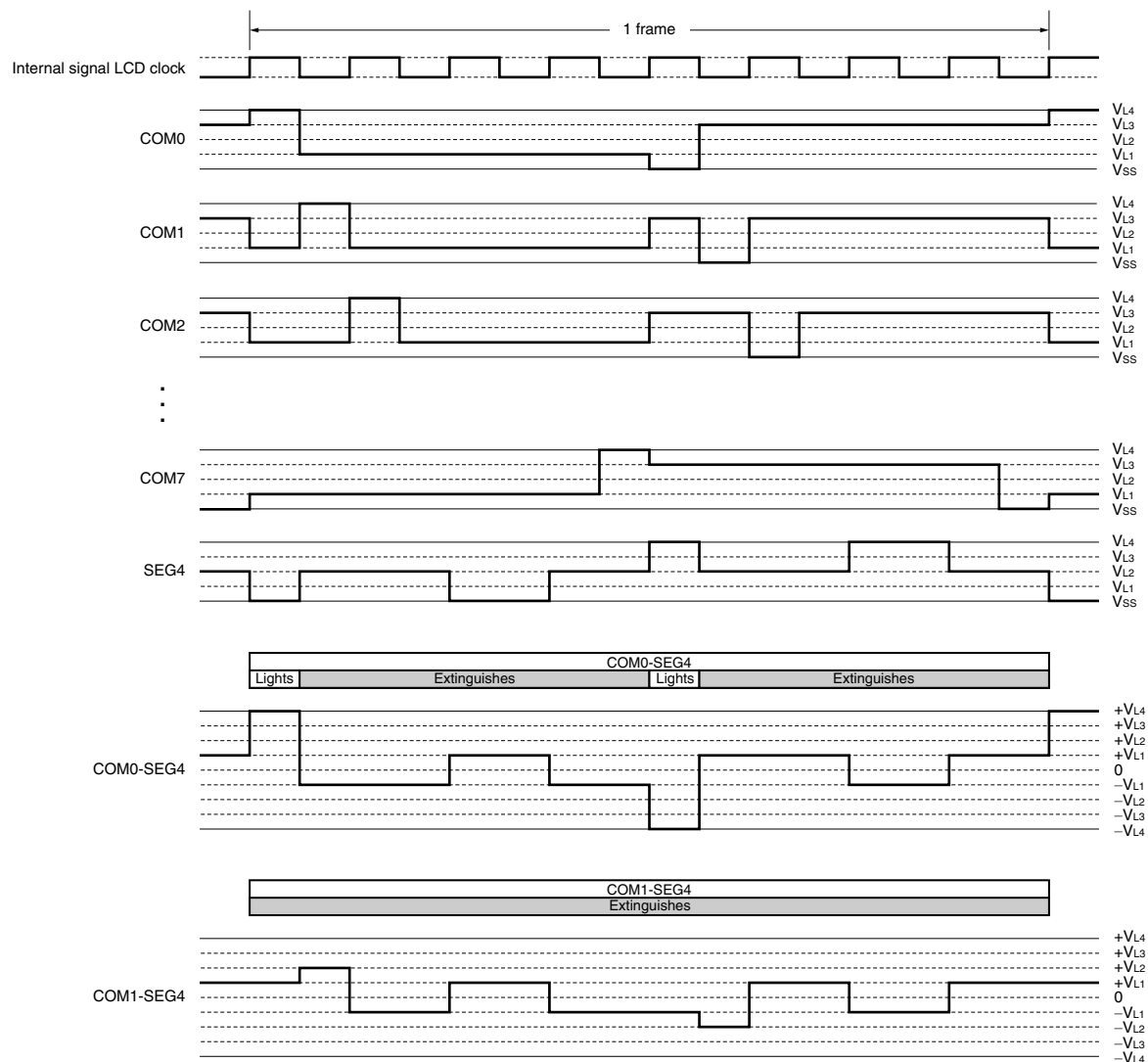


**Figure 14-44. Eight-Time-Slice LCD Drive Waveform Examples Between SEG4 and Each Common Signals  
(1/4 Bias Method) (2/2)**

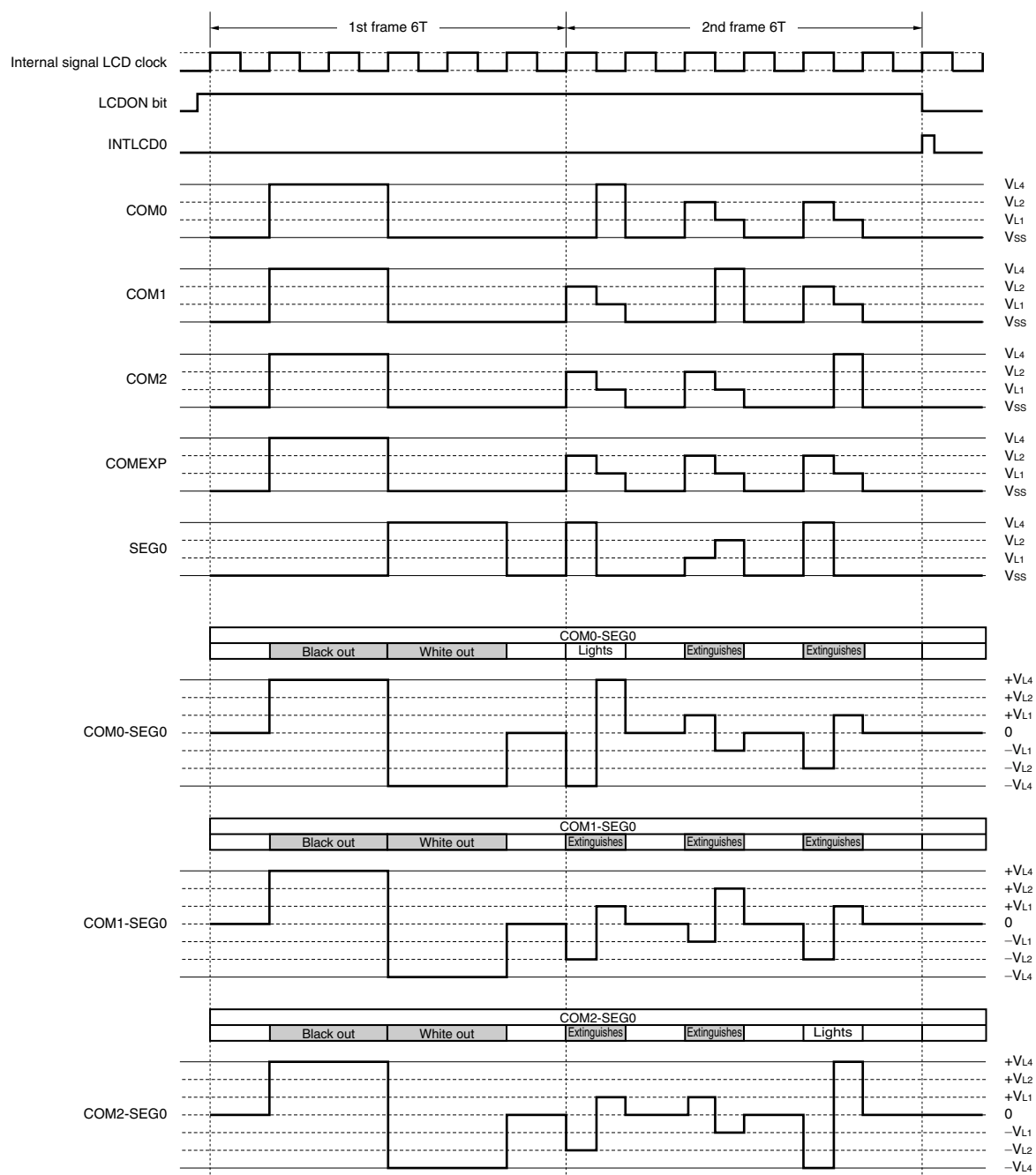
**(b) Waveform B**





## 14.11 Examples of Memory-Type Liquid Crystal Waveform

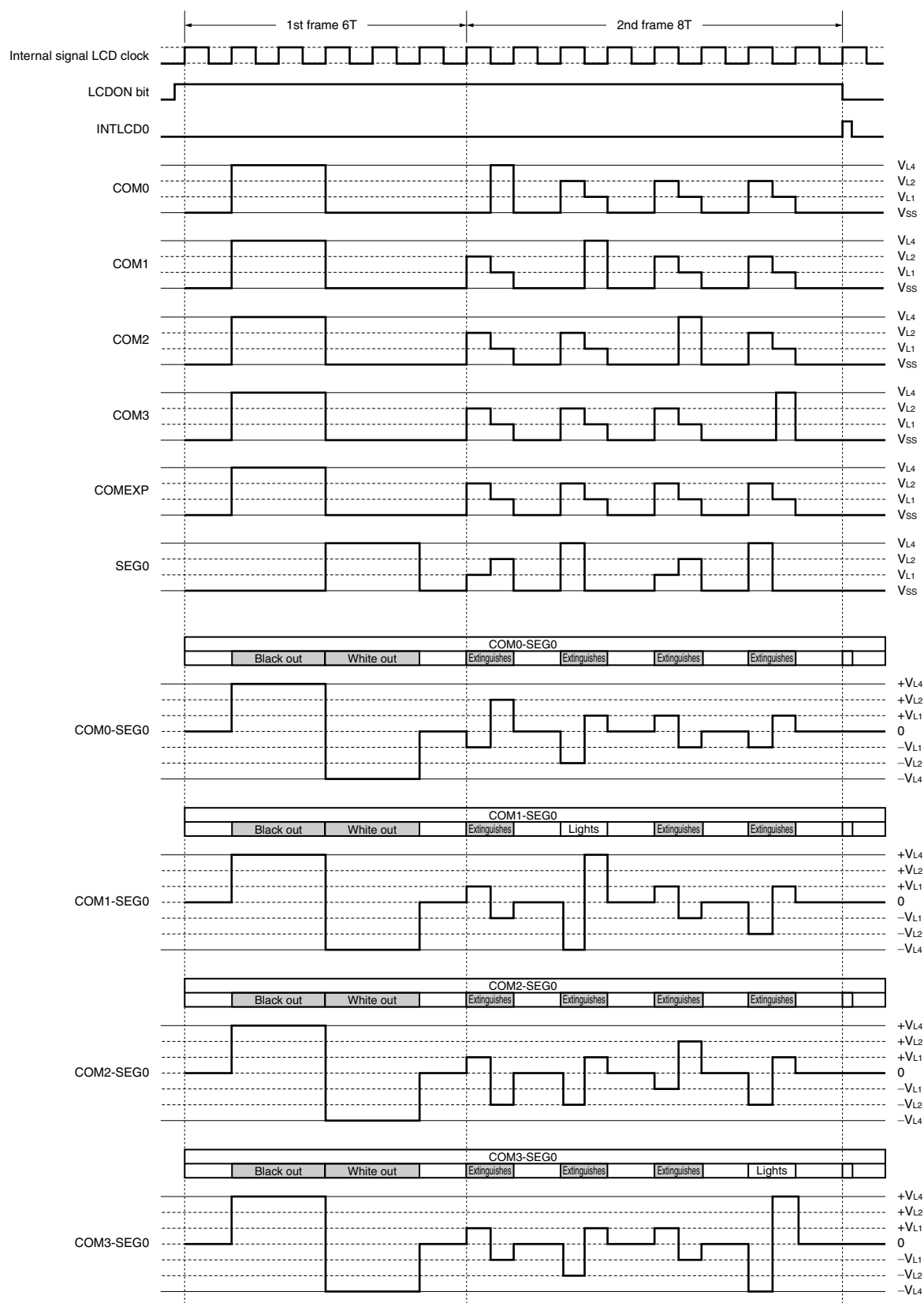
**Figure 14-45. LCD Drive Waveform Examples of Memory-Type Liquid Crystal Waveform  
(3-Time-Slice, 1/3 Bias Method)**



&lt;R&gt;

**Remark** In the 1st frame, the black-out and white-out sequences are output.  
Store the data to be output in the 2nd frame in the LCD display data register.

**Figure 14-46. LCD Drive Waveform Examples of Memory-Type Liquid Crystal Waveform (4-Time-Slice, 1/3 Bias Method)**



## CHAPTER 15 MULTIPLIER AND DIVIDER/MULTIPLY-ACCUMULATOR

### 15.1 Functions of Multiplier and Divider/Multiply-Accumulator

The multiplier and divider/multiply-accumulator has the following functions.

- $16 \text{ bits} \times 16 \text{ bits} = 32 \text{ bits}$  (Unsigned)
- $16 \text{ bits} \times 16 \text{ bits} = 32 \text{ bits}$  (Signed)
- $16 \text{ bits} \times 16 \text{ bits} + 32 \text{ bits} = 32 \text{ bits}$  (Unsigned)
- $16 \text{ bits} \times 16 \text{ bits} + 32 \text{ bits} = 32 \text{ bits}$  (Signed)
- $32 \text{ bits} \div 32 \text{ bits} = 32 \text{ bits}$ , 32-bits remainder (Unsigned)

### 15.2 Configuration of Multiplier and Divider/Multiply-Accumulator

The multiplier and divider/multiply-accumulator consists of the following hardware.

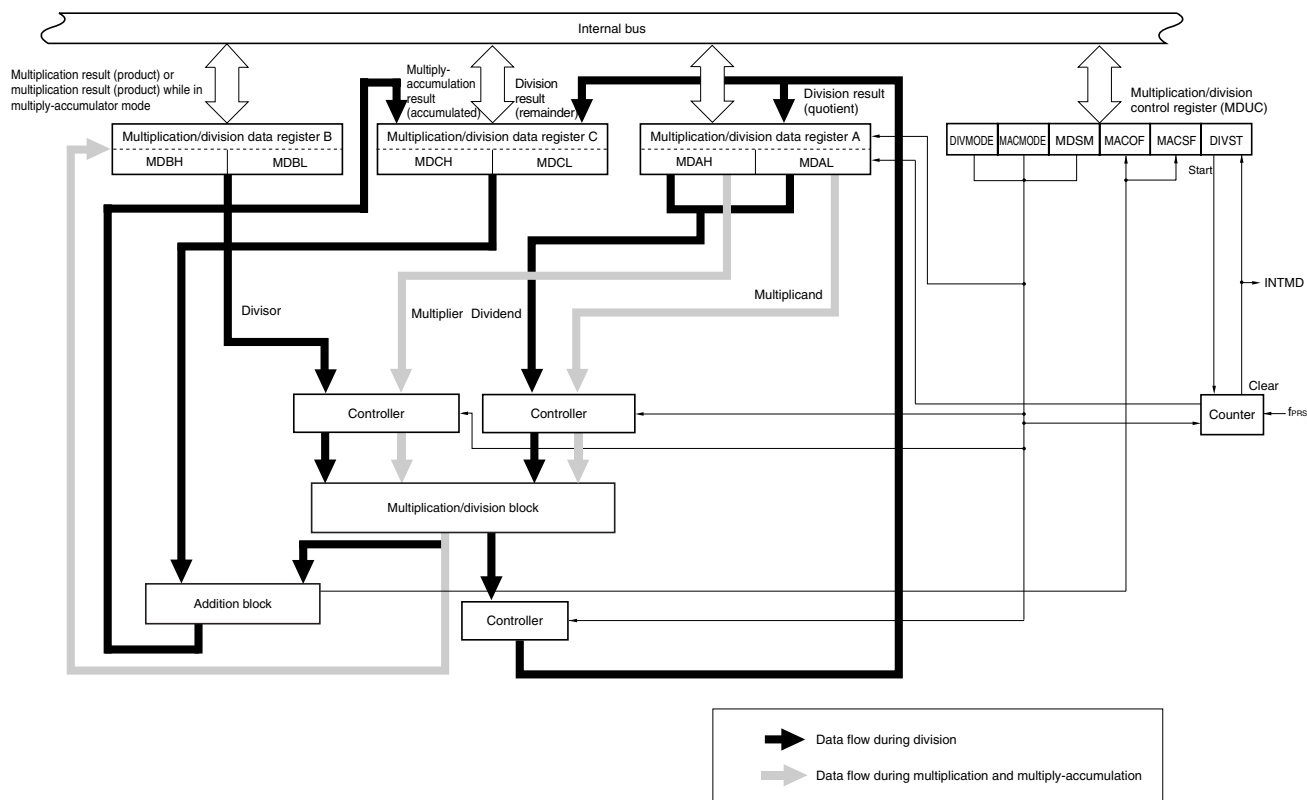
**Table 15-1. Configuration of Multiplier and Divider/Multiply-Accumulator**

| Item             | Configuration                                                                                                                                                                                                                                                                                                                    |
|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Registers        | Multiplication/division data register A (L) (MDAL)<br>Multiplication/division data register A (H) (MDAH)<br>Multiplication/division data register B (L) (MDBL)<br>Multiplication/division data register B (H) (MDBH)<br>Multiplication/division data register C (L) (MDCL)<br>Multiplication/division data register C (H) (MDCH) |
| Control register | Multiplication/division control register (MDUC)                                                                                                                                                                                                                                                                                  |

Figure 15-1 shows a block diagram of the multiplier and divider/multiply-accumulator.

&lt;R&gt;

Figure 15-1. Block Diagram of Multiplier and Divider/Multiply-Accumulator



### 15.2.1 Multiplication/division data register A (MDAH, MDAL)

The MDAH and MDAL registers set the values that are used for a multiplication or division operation and store the operation result. They set the multiplier and multiplicand data in the multiplication mode or multiply-accumulator mode, and set the dividend data in the division mode. Furthermore, the operation result (quotient) is stored in the MDAH and MDAL registers in the division mode.

The MDAH and MDAL registers can be set by a 16-bit manipulation instruction.

Reset signal generation clears these registers to 0000H.

**Figure 15-2. Format of Multiplication/Division Data Register A (MDAH, MDAL)**

Address: FFFF0H, FFFF1H, FFFF2H, FFFF3H After reset: 0000H, 0000H R/W



- Cautions**
1. Do not rewrite the MDAH and MDAL registers values during division operation processing (when the multiplication/division control register (MDUC) value is 81H or C1H). The operation will be executed in this case, but the operation result will be an undefined value.
  2. The MDAH and MDAL registers values read during division operation processing (when the MDUC register value is 81H or C1H) will not be guaranteed.
  3. The data is in the two's complement format in either the multiplication mode (signed) or multiply-accumulator mode (signed).

The following table shows the functions of the MDAH and MDAL registers during operation execution.

**Table 15-2. Functions of MDAH and MDAL Registers During Operation Execution**

| Operation Mode                                                         | Setting                                                                                       | Operation Result                                                                                                              |
|------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|
| Multiplication mode (unsigned)<br>Multiply-accumulator mode (unsigned) | MDAH: Multiplier (unsigned)<br>MDAL: Multiplicand (unsigned)                                  | —                                                                                                                             |
| Multiplication mode (signed)<br>Multiply-accumulator mode (signed)     | MDAH: Multiplier (signed)<br>MDAL: Multiplicand (signed)                                      | —                                                                                                                             |
| Division mode (unsigned)                                               | MDAH: Dividend (unsigned)<br>(higher 16 bits)<br>MDAL: Dividend (unsigned)<br>(lower 16 bits) | MDAH: Division result (quotient) (unsigned)<br>Higher 16 bits<br>MDAL: Division result (quotient) (unsigned)<br>Lower 16 bits |

<R>

### 15.2.2 Multiplication/division data register B (MDBL, MDBH)

The MDBH and MDBL registers set the values that are used for multiplication or division operation and store the operation result. They store the operation result (product) in the multiplication mode and multiply-accumulator mode, and set the divisor data in the division mode.

The MDBH and MDBL registers can be set by a 16-bit manipulation instruction.

Reset signal generation clears these registers to 0000H.

**Figure 15-3. Format of Multiplication/Division Data Register B (MDBH, MDBL)**

Address: FFFF4H, FFFF5H, FFFF6H, FFFF7H After reset: 0000H, 0000H R/W



- Cautions**
1. Do not rewrite the MDBH and MDBL registers values during division operation processing (when the multiplication/division control register (MDUC) value is 81H or C1H) or multiply-accumulation operation processing. The operation result will be an undefined value.
  2. Do not set the MDBH and MDBL registers to 0000H in the division mode. If they are set, the operation result will be an undefined value.
  3. The data is in the two's complement format in either the multiplication mode (signed) or multiply-accumulator mode (signed).

The following table shows the functions of the MDBH and MDBL registers during operation execution.

**Table 15-3. Functions of MDBH and MDBL Registers During Operation Execution**

| Operation Mode                                                         | Setting                                                                                     | Operation Result                                                                                                                        |
|------------------------------------------------------------------------|---------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| Multiplication mode (unsigned)<br>Multiply-accumulator mode (unsigned) | —                                                                                           | MDBH: Multiplication result (product) (unsigned)<br>Higher 16 bits<br>MDBL: Multiplication result (product) (unsigned)<br>Lower 16 bits |
| Multiplication mode (signed)<br>Multiply-accumulator mode (signed)     | —                                                                                           | MDBH: Multiplication result (product) (signed)<br>Higher 16 bits<br>MDBL: Multiplication result (product) (signed)<br>Lower 16 bits     |
| Division mode (unsigned)                                               | MDBH: Divisor (unsigned)<br>(higher 16 bits)<br>MDBL: Divisor (unsigned)<br>(lower 16 bits) | —                                                                                                                                       |

### 15.2.3 Multiplication/division data register C (MDCL, MDCH)

The MDCH and MDCL registers are used to store the accumulated result while in the multiply-accumulator mode or the remainder of the operation result while in the division mode. These registers are not used while in the multiplication mode.

The MDCH and MDCL registers can be set by a 16-bit manipulation instruction.

Reset signal generation clears these registers to 0000H.

**Figure 15-4. Format of Multiplication/Division Data Register C (MDCH, MDCL)**

Address: F00E0H, F00E1H, F00E2H, F00E3H    After reset: 0000H, 0000H    R/W

Symbol

F00E3H

F00E2H

MDCH

|      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| MDCH | MDCH | MDCH | MDCH | MDCH | MDCH | MDCH | MDCH | MDCH | MDCH | MDCH | MDCH | MDCH | MDCH | MDCH | MDCH | MDCH |
| 15   | 14   | 13   | 12   | 11   | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |      |

Symbol

F00E1H

FOOE0H

**Cautions**

1. The MDCH and MDCL registers values read during division operation processing (when the multiplication/division control register (MDUC) value is 81H or C1H) will not be guaranteed.
2. During multiply-accumulator processing, do not use software to rewrite the values of the MDCH and MDCL registers. If this is done, the operation result will be undefined.
3. The data is in the two's complement format in the multiply-accumulator mode (signed).

**Table 15-4. Functions of MDCH and MDCL Registers During Operation Execution**

| Operation Mode                           | Setting                                                                                                                         | Operation Result                                                                                                |
|------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|
| Multiplication mode (unsigned or signed) | –                                                                                                                               | –                                                                                                               |
| Multiply-accumulator mode (unsigned)     | MDCH: Initial accumulated value (unsigned)<br>(higher 16 bits)<br>MDCL: Initial accumulated value (unsigned)<br>(lower 16 bits) | MDCH: Accumulated value (unsigned)<br>(higher 16 bits)<br>MDCL: Accumulated value (unsigned)<br>(lower 16 bits) |
| Multiply-accumulator mode (signed)       | MDCH: Initial accumulated value (signed)<br>(higher 16 bits)<br>MDCL: Initial accumulated value (signed)<br>(lower 16 bits)     | MDCH: Accumulated value (signed)<br>(higher 16 bits)<br>MDCL: Accumulated value (signed)<br>(lower 16 bits)     |
| Division mode (unsigned)                 | –                                                                                                                               | MDCH: Remainder (unsigned)<br>(higher 16 bits)<br>MDCL: Remainder (unsigned)<br>(lower 16 bits)                 |

The register configuration differs between when multiplication is executed and when division is executed, as follows.

- Register configuration during multiplication

<Multiplier A>      <Multiplier B>                      <Product>

$$\text{MDAL (bits 15 to 0)} \times \text{MDAH (bits 15 to 0)} = [\text{MDBH (bits 15 to 0)}, \text{MDBL (bits 15 to 0)}]$$

- Register configuration during multiply-accumulation

<Multiplier A>      <Multiplier B>      < accumulated value >              < accumulated result >

$$\text{MDAL (bits 15 to 0)} \times \text{MDAH (bits 15 to 0)} + \text{MDC (bits 31 to 0)} = [\text{MDCH (bits 15 to 0)}, \text{MDCL (bits 15 to 0)}]$$

(The multiplication result is stored in the MDBH (bits 15 to 0) and MDBL (bits 15 to 0).)

- Register configuration during division

<Dividend>                                              <Divisor>

$$[\text{MDAH (bits 15 to 0)}, \text{MDAL (bits 15 to 0)}] \div [\text{MDBH (bits 15 to 0)}, \text{MDBL (bits 15 to 0)}] =$$

<Quotient>                                              <Remainder>

$$[\text{MDAH (bits 15 to 0)}, \text{MDAL (bits 15 to 0)}] \dots [\text{MDCH (bits 15 to 0)}, \text{MDCL (bits 15 to 0)}]$$



### 15.3 Register Controlling Multiplier and Divider/Multiply-Accumulator

The multiplier and divider/multiply-accumulator is controlled by using the multiplication/division control register (MDUC).

#### 15.3.1 Multiplication/division control register (MDUC)

The MDUC register is an 8-bit register that controls the operation of the multiplier and divider/multiply-accumulator.

The MDUC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 15-5. Format of Multiplication/Division Control Register (MDUC)**

Address: F00E8H After reset: 00H R/W

|        |         |         |   |   |      |       |       |       |
|--------|---------|---------|---|---|------|-------|-------|-------|
| Symbol | <7>     | <6>     | 5 | 4 | <3>  | <2>   | <1>   | <0>   |
| MDUC   | DIVMODE | MACMODE | 0 | 0 | MDSM | MACOF | MACSF | DIVST |

| DIVMODE          | MACMODE | MDSM | Operation mode selection                                                            |
|------------------|---------|------|-------------------------------------------------------------------------------------|
| 0                | 0       | 0    | Multiplication mode (unsigned) (default)                                            |
| 0                | 0       | 1    | Multiplication mode (signed)                                                        |
| 0                | 1       | 0    | Multiply-accumulator mode (unsigned)                                                |
| 0                | 1       | 1    | Multiply-accumulator mode (signed)                                                  |
| 1                | 0       | 0    | Division mode (unsigned), generation of a division completion interrupt (INTMD)     |
| 1                | 1       | 0    | Division mode (unsigned), not generation of a division completion interrupt (INTMD) |
| Other than above |         |      | Setting is prohibited                                                               |

| MACOF                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Overflow flag of multiply-accumulation result (accumulated value) |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | No overflow                                                       |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | With over flow                                                    |
| <Set condition> <ul style="list-style-type: none"> <li>For the multiply-accumulator mode (unsigned)<br/>The bit is set when the accumulated value goes outside the range from 00000000h to FFFFFFFFh.</li> <li>For the multiply-accumulator mode (signed)<br/>The bit is set when the result of adding a positive product to a positive accumulated value exceeds 7FFFFFFFh and is negative, or when the result of adding a negative product to a negative accumulated value exceeds 80000000h and is positive.</li> </ul> |                                                                   |

| MACSF                                                                                                                                                      | Sign flag of multiply-accumulation result (accumulated value) |
|------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------|
| 0                                                                                                                                                          | The accumulated value is positive.                            |
| 1                                                                                                                                                          | The accumulated value is negative.                            |
| Multiply-accumulator mode (unsigned): The bit is always 0.<br>Multiply-accumulator mode (signed): The bit indicates the sign bit of the accumulated value. |                                                               |

| DIVST <sup>Note</sup> | Division operation start/stop                                       |
|-----------------------|---------------------------------------------------------------------|
| 0                     | Division operation processing complete                              |
| 1                     | Starts division operation/division operation processing in progress |

(Note and caution are listed on the next page.)

**Note** The DIVST bit can only be set (1) in the division mode. In the division mode, division operation is started by setting (1) the DIVST bit. The DIVST bit is automatically cleared (0) when the operation ends. In the multiplication mode, operation is automatically started by setting the multiplier and multiplicand to multiplication/division data register A (MDAH, MDAL), respectively.

**Cautions**

1. Do not rewrite the DIVMODE, MDSM bits during operation processing (while the DIVST bit is 1). If it is rewritten, the operation result will be an undefined value.
2. The DIVST bit cannot be cleared (0) by using software during division operation processing (while the DIVST bit is 1).

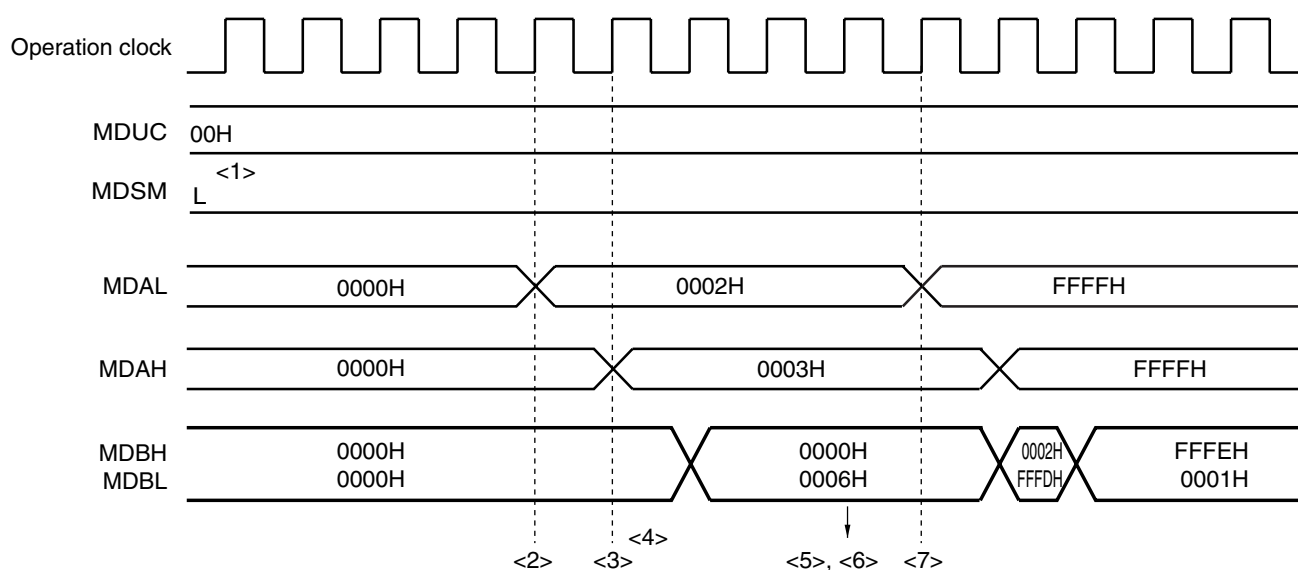
## 15.4 Operations of Multiplier and Divider/Multiply-Accumulator

### 15.4.1 Multiplication (unsigned) operation

- Initial setting
    - <1> Set the multiplication/division control register (MDUC) to 00H.
    - <2> Set the multiplicand to multiplication/division data register A (L) (MDAL).
    - <3> Set the multiplier to multiplication/division data register A (H) (MDAH).  
(There is no preference in the order of executing steps <2> and <3>. Multiplication operation is automatically started when the multiplier and multiplicand are set to the MDAH and MDAL registers, respectively.)
  - During operation processing
    - <4> Wait for at least one clock. The operation will end when one clock has been issued.
  - Operation end
    - <5> Read the product (lower 16 bits) from multiplication/division data register B (L) (MDBL).
    - <6> Read the product (higher 16 bits) from multiplication/division data register B (H) (MDBH).  
(There is no preference in the order of executing steps <5> and <6>.)
  - Next operation
    - <7> The next time multiplication, division, or multiply-accumulation is performed, start with the initial settings of each step.
- <R>

**Remark** Steps <1> to <7> correspond to <1> to <7> in Figure 15-6.

<R> **Figure 15-6. Timing Diagram of Multiplication (Unsigned) Operation ( $2 \times 3 = 6$ )**



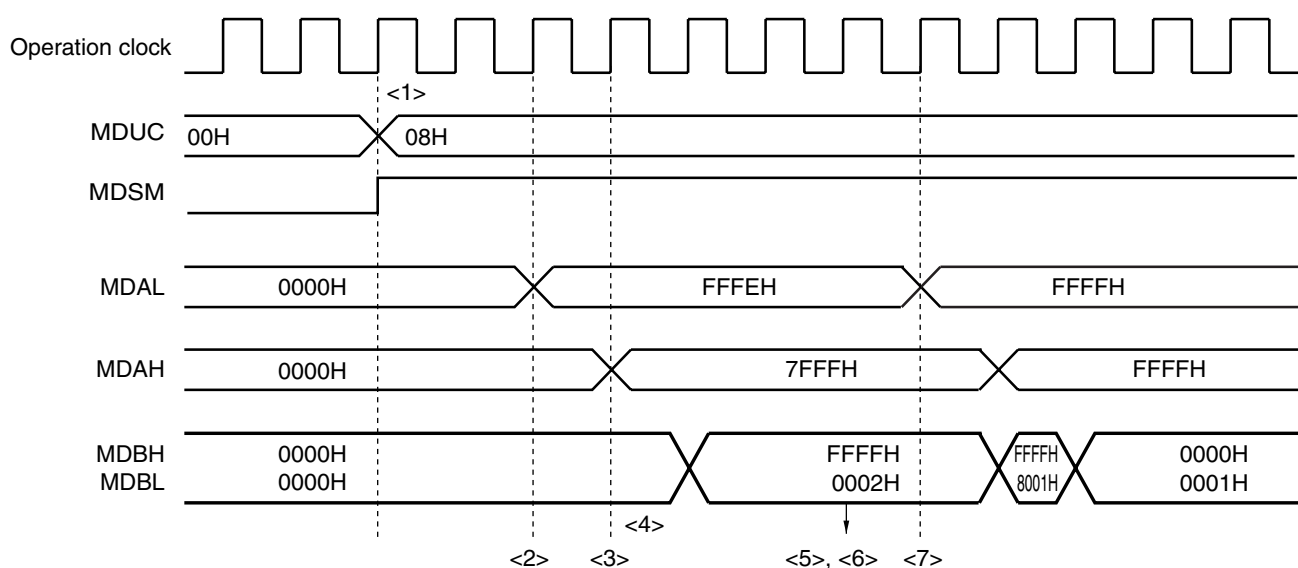
### 15.4.2 Multiplication (signed) operation

- Initial setting
  - <1> Set the multiplication/division control register (MDUC) to 08H.
  - <2> Set the multiplicand to multiplication/division data register A (L) (MDAL).
  - <3> Set the multiplier to multiplication/division data register A (H) (MDAH).
  - (There is no preference in the order of executing steps <2> and <3>. Multiplication operation is automatically started when the multiplier and multiplicand are set to the MDAH and MDAL registers, respectively.)
- During operation processing
  - <4> Wait for at least one clock. The operation will end when one clock has been issued.
- Operation end
  - <5> Read the product (lower 16 bits) from multiplication/division data register B (L) (MDBL).
  - <6> Read the product (higher 16 bits) from multiplication/division data register B (H) (MDBH).
  - (There is no preference in the order of executing steps <5> and <6>.)
- Next operation
  - <7> The next time multiplication, division, or multiply-accumulation is performed, start with the initial settings of each step.

**Caution** The data is in the two's complement format in multiplication mode (signed).

**Remark** Steps <1> to <7> correspond to <1> to <7> in Figure 15-7.

<R> **Figure 15-7. Timing Diagram of Multiplication (Signed) Operation ( $-2 \times 32767 = -65534$ )**



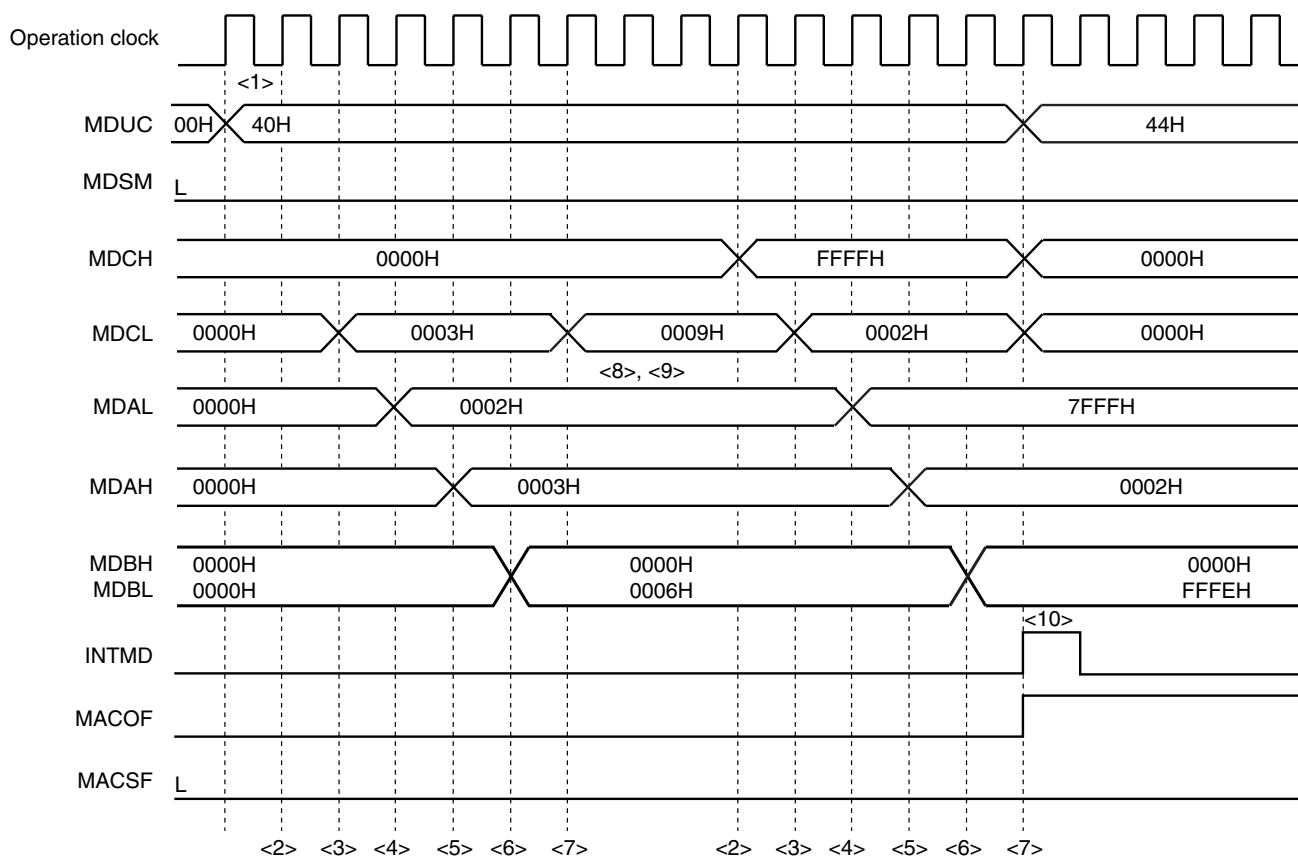
### 15.4.3 Multiply-accumulation (unsigned) operation

- Initial setting
    - <1> Set the multiplication/division control register (MDUC) to 40H.
    - <2> Set the initial accumulated value of higher 16 bits to multiplication/division data register C (L) (MDCL).
    - <3> Set the initial accumulated value of lower 16 bits to multiplication/division data register C (H) (MDCH).
    - <4> Set the multiplicand to multiplication/division data register A (L) (MDAL).
    - <5> Set the multiplier to multiplication/division data register A (H) (MDAH).  
(There is no preference in the order of executing steps <2>, <3>, and <4>. Multiplication operation is automatically started when the multiplier is set to the MDAH register, respectively.)
  - During operation processing
    - <6> The multiplication operation finishes in one clock cycle.  
(The multiplication result is stored in multiplication/division data register B (L) (MDBL) and multiplication/division data register B (H) (MDBH).)
    - <7> After <6>, the multiply-accumulation operation finishes in one additional clock cycle. (There is a wait of at least two clock cycles after specifying the initial settings is finished (<5>).)
  - Operation end
    - <8> Read the accumulated value (lower 16 bits) from the MDCL register.
    - <9> Read the accumulated value (higher 16 bits) from the MDCH register.  
(There is no preference in the order of executing steps <8> and <9>.)
    - (<10> If the result of the multiply-accumulation operation causes an overflow, the MACOF bit is set to 1, INTMD signal is occurred.)
  - Next operation
    - <11> The next time multiplication, division, or multiply-accumulation is performed, start with the initial settings of each step.
- <R>

**Remark** Steps <1> to <10> correspond to <1> to <10> in Figure 15-8.

&lt;R&gt;

**Figure 15-8. Timing Diagram of Multiply-Accumulation (Unsigned) Operation**  
 $(2 \times 3 + 3 = 9 \rightarrow 32767 \times 2 + 4294901762 = 0 \text{ (over flow generated)})$



#### 15.4.4 Multiply-accumulation (signed) operation

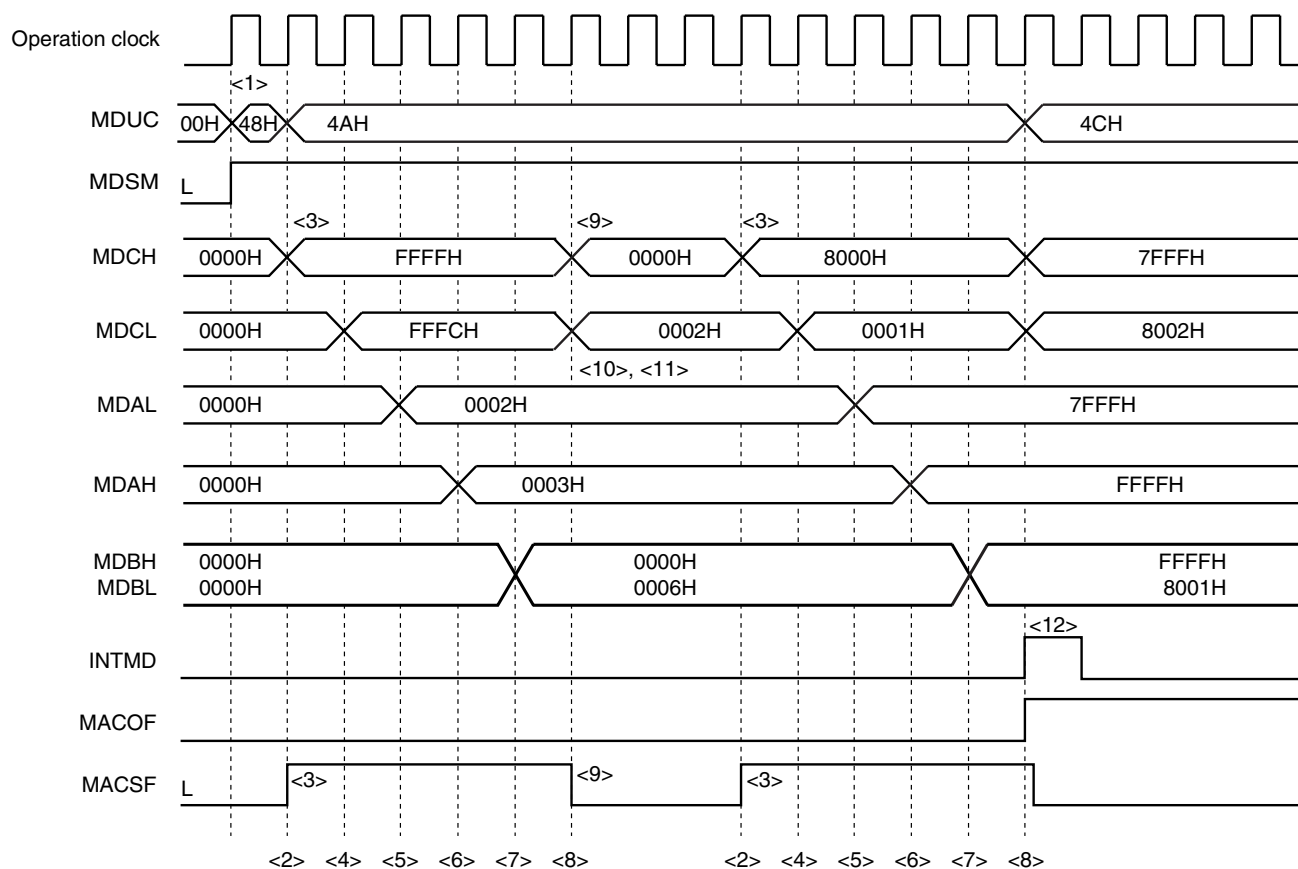
- Initial setting
  - <1> Set the multiplication/division control register (MDUC) to 48H.
  - <2> Set the initial accumulated value of higher 16 bits to multiplication/division data register C (H) (MDCH).  
(<3> If the accumulated value in the MDCH register is negative, the MACSF bit is set to 1.)
  - <4> Set the initial accumulated value of lower 16 bits to multiplication/division data register C (L) (MDCL).
  - <5> Set the multiplicand to multiplication/division data register A (L) (MDAL).
  - <6> Set the multiplier to multiplication/division data register A (H) (MDAH).  
(There is no preference in the order of executing steps <2>, <4>, and <5>. Multiplication operation is automatically started when the multiplier is set to the MDAH register, respectively.)
- During operation processing
  - <7> The multiplication operation finishes in one clock cycle.  
(The multiplication result is stored in multiplication/division data register B (L) (MDBL) and multiplication/division data register B (H) (MDBH).)
  - <8> After <7>, the multiply-accumulation operation finishes in one additional clock cycle. (There is a wait of at least two clock cycles after specifying the initial settings is finished (<6>).)
- Operation end
  - <9> If the accumulated value stored in the MDCL and MDCH registers is positive, the MACSF bit is cleared to 0.
  - <10> Read the accumulated value (lower 16 bits) from the MDCL register.
  - <11> Read the accumulated value (higher 16 bits) from the MDCH register.  
(There is no preference in the order of executing steps <10> and <11>.)
  - (<12> If the result of the multiply-accumulation operation causes an overflow, the MACOF bit is set to 1, INTMD signal is occurred.)
- Next operation
  - <R> <13> The next time multiplication, division, or multiply-accumulation is performed, start with the initial settings of each step.

**Caution** The data is in the two's complement format in multiply-accumulation (signed) operation.

**Remark** Steps <1> to <12> correspond to <1> to <12> in Figure 15-9.

&lt;R&gt;

**Figure 15-9. Timing Diagram of Multiply-Accumulation (signed) Operation**  
 $(2 \times 3 + (-4) = 2 \rightarrow 32767 \times (-1) + (-2147483647) = -2147450882 \text{ (overflow occurs.)})$





### 15.4.5 Division operation

- Initial setting
  - <1> Set the multiplication/division control register (MDUC) to 80H.
  - <2> Set the dividend (higher 16 bits) to multiplication/division data register A (H) (MDAH).
  - <3> Set the dividend (lower 16 bits) to multiplication/division data register A (L) (MDAL).
  - <4> Set the divisor (higher 16 bits) to multiplication/division data register B (H) (MDBH).
  - <5> Set the divisor (lower 16 bits) to multiplication/division data register B (L) (MDBL).
  - <6> Set bit 0 (DIVST) of the MDUC register to 1.

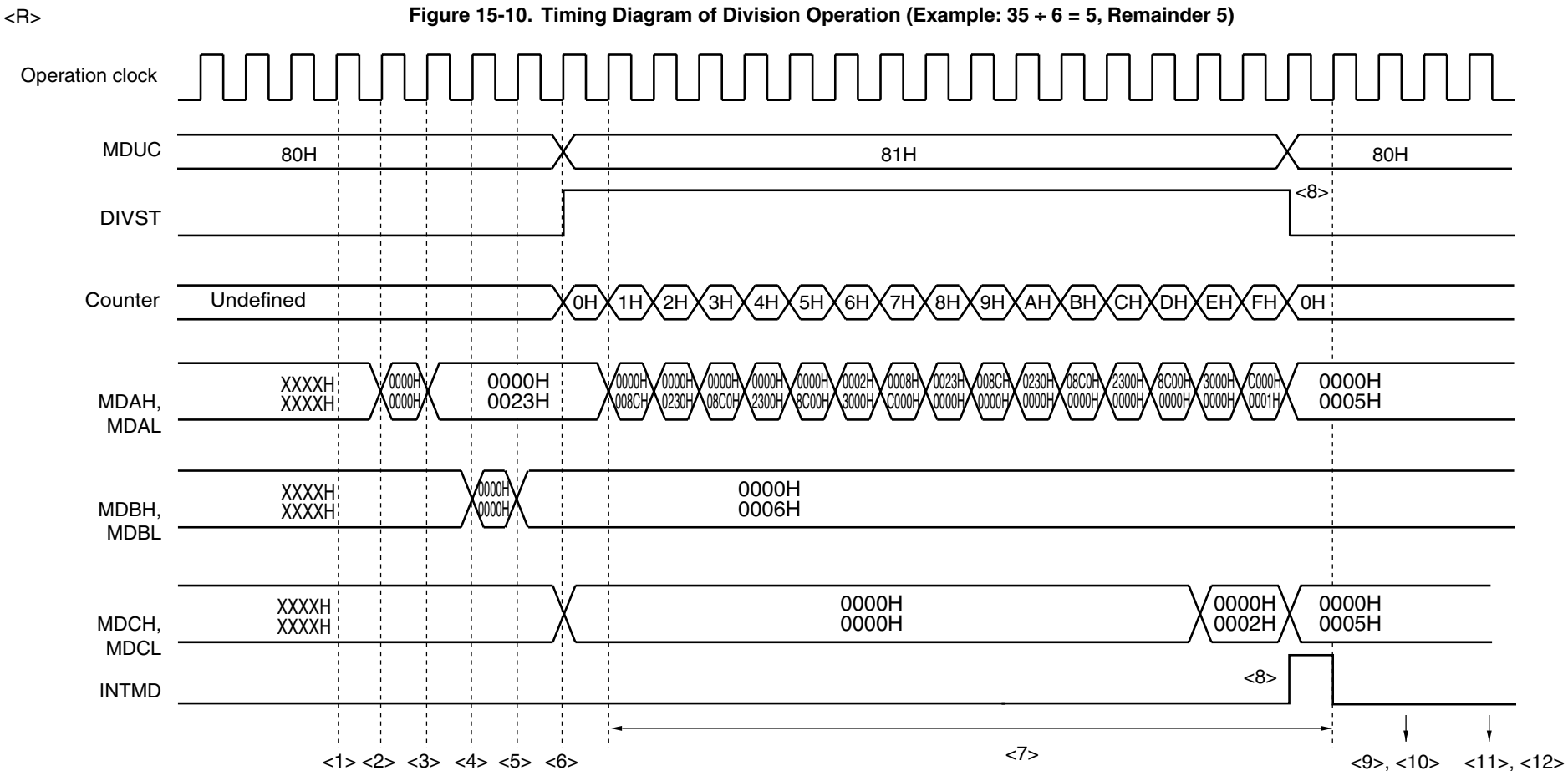
(There is no preference in the order of executing steps <2> to <5>.)
- During operation processing
  - <7> The operation will end when one of the following processing is completed.
    - A wait of at least 16 clocks (The operation will end when 16 clocks have been issued.)
    - A check whether the DIVST bit has been cleared

(The read values of the MDBL, MDBH, MDCL, and MDCH registers during operation processing are not guaranteed.)
- Operation end
  - <8> The DIVST bit is cleared and the operation ends. At this time, an interrupt request signal (INTMD) is generated if the operation was performed with MACMODE = 0.
  - <9> Read the quotient (lower 16 bits) from the MDAL register.
  - <10> Read the quotient (higher 16 bits) from the MDAH register.
  - <11> Read the remainder (lower 16 bits) from multiplication/division data register C (L) (MDCL).
  - <12> Read the remainder (higher 16 bits) from multiplication/division data register C (H) (MDCH).

(There is no preference in the order of executing steps <9> to <12>.)
- Next operation
  - <13> The next time multiplication, division, or multiply-accumulation is performed, start with the initial settings of each step

**Remark** Steps <1> to <12> correspond to <1> to <12> in Figure 15-10.

Figure 15-10. Timing Diagram of Division Operation (Example:  $35 \div 6 = 5$ , Remainder 5)



## CHAPTER 16 DMA CONTROLLER

The RL78/L12 has an internal DMA (Direct Memory Access) controller.

Data can be automatically transferred between the peripheral hardware supporting DMA, SFRs, and internal RAM without via CPU.

As a result, the normal internal operation of the CPU and data transfer can be executed in parallel with transfer between the SFR and internal RAM, and therefore, a large capacity of data can be processed. In addition, real-time control using communication, timer, and A/D can also be realized.

### 16.1 Functions of DMA Controller

- Number of DMA channels: 2 channels
- Transfer unit: 8 or 16 bits
- Maximum transfer unit: 1024 times
- Transfer type: 2-cycle transfer (One transfer is processed in 2 clocks and the CPU stops during that processing.)
- Transfer mode: Single-transfer mode
- Transfer request: Selectable from the following peripheral hardware interrupts
  - A/D converter
  - Serial interface  
(CSI00, CSI01, UART0)
  - Timer (channel 0, 1, 2, 3)
- Transfer target: Between SFR and internal RAM

Here are examples of functions using DMA.

- Successive transfer of serial interface
- Batch transfer of analog data
- Capturing A/D conversion result at fixed interval
- Capturing port value at fixed interval

## 16.2 Configuration of DMA Controller

The DMA controller includes the following hardware.

**Table 16-1. Configuration of DMA Controller**

| Item              | Configuration                                                                                                                                                |
|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Address registers | <ul style="list-style-type: none"> <li>• DMA SFR address registers 0, 1 (DSA0, DSA1)</li> <li>• DMA RAM address registers 0, 1 (DRA0, DRA1)</li> </ul>       |
| Count register    | <ul style="list-style-type: none"> <li>• DMA byte count registers 0, 1 (DBC0, DBC1)</li> </ul>                                                               |
| Control registers | <ul style="list-style-type: none"> <li>• DMA mode control registers 0, 1 (DMC0, DMC1)</li> <li>• DMA operation control register 0, 1 (DRC0, DRC1)</li> </ul> |

### 16.2.1 DMA SFR address register n (DSAn)

This is an 8-bit register that is used to set an SFR address that is the transfer source or destination of DMA channel n. Set the lower 8 bits of the SFR addresses FFF00H to FFFFH.

This register is not automatically incremented but fixed to a specific value.

In the 16-bit transfer mode, the least significant bit is ignored and is treated as an even address.

The DSAn register can be read or written in 8-bit units. However, it cannot be written during DMA transfer.

Reset signal generation clears this register to 00H.

**Figure 16-1. Format of DMA SFR Address Register n (DSAn)**

Address: FFFB0H (DSA0), FFFB1H (DSA1) After reset: 00H R/W

|      |                      |                      |                      |                      |                      |                      |                      |                      |
|------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
|      | 7                    | 6                    | 5                    | 4                    | 3                    | 2                    | 1                    | 0                    |
| DSAn | <input type="text"/> | <input type="text"/> | <input type="text"/> | <input type="text"/> | <input type="text"/> | <input type="text"/> | <input type="text"/> | <input type="text"/> |

**Remark** n: DMA channel number (n = 0, 1)

### 16.3.2 DMA RAM address register n (DRAn)

This is a 16-bit register that is used to set a RAM address that is the transfer source or destination of DMA channel n.

Addresses of the internal RAM area other than the general-purpose registers can be set to this register.

Set the lower 16 bits of the RAM address.

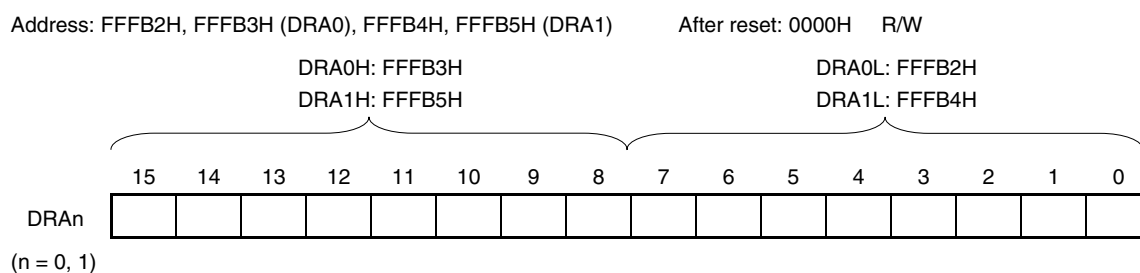
This register is automatically incremented when DMA transfer has been started. It is incremented by +1 in the 8-bit transfer mode and by +2 in the 16-bit transfer mode. DMA transfer is started from the address set to this DRAn register. When the data of the last address has been transferred, the DRAn register stops with the value of the last address +1 in the 8-bit transfer mode, and the last address +2 in the 16-bit transfer mode.

In the 16-bit transfer mode, the least significant bit is ignored and is treated as an even address.

The DRAn register can be read or written in 8-bit or 16-bit units. However, it cannot be written during DMA transfer.

Reset signal generation clears this register to 0000H.

**Figure 16-2. Format of DMA RAM Address Register n (DRAn)**



**Remark** n: DMA channel number (n = 0, 1)

### 16.3.3 DMA byte count register n (DBCn)

This is a 10-bit register that is used to set the number of times DMA channel n executes transfer. Be sure to set the number of times of transfer to this DBCn register before executing DMA transfer (up to 1024 times).

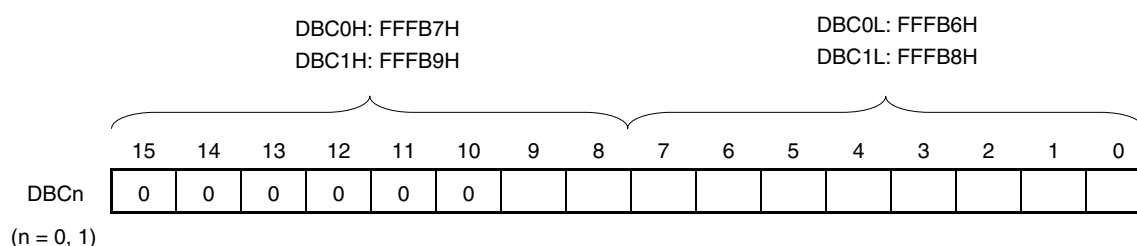
Each time DMA transfer has been executed, this register is automatically decremented. By reading this DBCn register during DMA transfer, the remaining number of times of transfer can be learned.

The DBCn register can be read or written in 8-bit or 16-bit units. However, it cannot be written during DMA transfer.

Reset signal generation clears this register to 0000H.

**Figure 16-3. Format of DMA Byte Count Register n (DBCn)**

Address: FFFB6H, FFFB7H (DBC0), FFFB8H, FFFB9H (DBC1) After reset: 0000H R/W



| DBCn[9:0] | Number of Times of Transfer<br>(When DBCn is Written) | Remaining Number of Times of Transfer<br>(When DBCn is Read)     |
|-----------|-------------------------------------------------------|------------------------------------------------------------------|
| 000H      | 1024                                                  | Completion of transfer or waiting for 1024 times of DMA transfer |
| 001H      | 1                                                     | Waiting for remaining one time of DMA transfer                   |
| 002H      | 2                                                     | Waiting for remaining two times of DMA transfer                  |
| 003H      | 3                                                     | Waiting for remaining three times of DMA transfer                |
| •         | •                                                     | •                                                                |
| •         | •                                                     | •                                                                |
| •         | •                                                     | •                                                                |
| 3FEH      | 1022                                                  | Waiting for remaining 1022 times of DMA transfer                 |
| 3FFH      | 1023                                                  | Waiting for remaining 1023 times of DMA transfer                 |

**Cautions** 1. Be sure to clear bits 15 to 10 to “0”.

2. If the general-purpose register is specified or the internal RAM space is exceeded as a result of continuous transfer, the general-purpose register or SFR space are written or read, resulting in loss of data in these spaces. Be sure to set the number of times of transfer that is within the internal RAM space.

**Remark** n: DMA channel number (n = 0, 1)

### 16.3 Registers Controlling DMA Controller

DMA controller is controlled by the following registers.

- DMA mode control register n (DMCn)
- DMA operation control register n (DRCn)

**Remark** n: DMA channel number (n = 0, 1)

### 16.3.1 DMA mode control register n (DMCn)

The DMCn register is a register that is used to set a transfer mode of DMA channel n. It is used to select a transfer direction, data size, setting of pending, and start source. Bit 7 (STGn) is a software trigger that starts DMA.

Rewriting bits 6, 5, and 3 to 0 of the DMCn register is prohibited during operation (when DSTn = 1).

The DMCn register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 16-4. Format of DMA Mode Control Register n (DMCn) (1/2)**

Address: FFFBAH (DMC0), FFFBBH (DMC1) After reset: 00H R/W

|        |      |      |     |        |       |       |       |       |
|--------|------|------|-----|--------|-------|-------|-------|-------|
| Symbol | <7>  | <6>  | <5> | <4>    | 3     | 2     | 1     | 0     |
| DMCn   | STGn | DRSn | DSn | DWAITn | IFCn3 | IFCn2 | IFCn1 | IFCn0 |

|                                                                                                                                                   |                                                                   |
|---------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| STGn <sup>Note 1</sup>                                                                                                                            | DMA transfer start software trigger                               |
| 0                                                                                                                                                 | No trigger operation                                              |
| 1                                                                                                                                                 | DMA transfer is started when DMA operation is enabled (DENn = 1). |
| DMA transfer is performed once by writing 1 to the STGn bit when DMA operation is enabled (DENn = 1).<br>When this bit is read, 0 is always read. |                                                                   |

|      |                                     |
|------|-------------------------------------|
| DRSn | Selection of DMA transfer direction |
| 0    | SFR to internal RAM                 |
| 1    | Internal RAM to SFR                 |

|     |                                                      |
|-----|------------------------------------------------------|
| DSn | Specification of transfer data size for DMA transfer |
| 0   | 8 bits                                               |
| 1   | 16 bits                                              |

|                                                                                                                                                                                                               |                                                                  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------|
| DWAITn <sup>Note 2</sup>                                                                                                                                                                                      | Pending of DMA transfer                                          |
| 0                                                                                                                                                                                                             | Executes DMA transfer upon DMA start request (not held pending). |
| 1                                                                                                                                                                                                             | Holds DMA start request pending if any.                          |
| DMA transfer that has been held pending can be started by clearing the value of the DWAITn bit to 0.<br>It takes 2 clocks to actually hold DMA transfer pending when the value of the DWAITn bit is set to 1. |                                                                  |

**Notes** 1. The software trigger (STGn) can be used regardless of the IFCn0 to IFCn3 bits values.

2. When DMA transfer is held pending while using both DMA channels, be sure to hold the DMA transfer pending for both channels (by setting the DWAIT0 and DWAIT1 bits to 1).

**Remark** n: DMA channel number (n = 0, 1)



**Figure 16-4. Format of DMA Mode Control Register n (DMCn) (2/2)**

Address: FFFBAH (DMC0), FFFBBH (DMC1) After reset: 00H R/W

| Symbol | <7>  | <6>  | <5> | <4>    | 3     | 2     | 1     | 0     |
|--------|------|------|-----|--------|-------|-------|-------|-------|
| DMCn   | STGn | DRSn | DSn | DWAItn | IFCn3 | IFCn2 | IFCn1 | IFCn0 |

(When n = 0 or 1)

| IFCn<br>3        | IFCn<br>2 | IFCn<br>1 | IFCn<br>0 | Selection of DMA start source <sup>Note</sup> |                                                                                            |
|------------------|-----------|-----------|-----------|-----------------------------------------------|--------------------------------------------------------------------------------------------|
|                  |           |           |           | Trigger signal                                | Trigger contents                                                                           |
| 0                | 0         | 0         | 0         | –                                             | Disables DMA transfer by interrupt.<br>(Only software trigger is enabled.)                 |
| 0                | 0         | 0         | 1         | INTAD                                         | A/D conversion end interrupt                                                               |
| 0                | 0         | 1         | 0         | INTTM00                                       | End of timer channel 0 count or capture<br>end interrupt                                   |
| 0                | 0         | 1         | 1         | INTTM01                                       | End of timer channel 1 count or capture<br>end interrupt                                   |
| 0                | 1         | 0         | 0         | INTTM02                                       | End of timer channel 2 count or capture<br>end interrupt                                   |
| 0                | 1         | 0         | 1         | INTTM03                                       | End of timer channel 3 count or capture<br>end interrupt                                   |
| 0                | 1         | 1         | 0         | INTST0/INTCSI00                               | UART0 transmission transfer end/<br>CSI00 transfer end or buffer empty<br>interrupt        |
| 0                | 1         | 1         | 1         | INTSR0/INTCSI01                               | UART0 reception transfer end interrupt/<br>CSI01 transfer end or buffer empty<br>interrupt |
| Other than above |           |           |           | Setting prohibited                            |                                                                                            |

**Note** The software trigger (STGn) can be used regardless of the IFCn0 to IFCn3 bits values.**Remark** n: DMA channel number (n = 0, 1)

### 16.3.2 DMA operation control register n (DRCn)

The DRCn register is a register that is used to enable or disable transfer of DMA channel n.

Rewriting bit 7 (DENn) of this register is prohibited during operation (when DSTn = 1).

The DRCn register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 16-5. Format of DMA Operation Control Register n (DRCn)**

Address: FFFBCH (DRC0), FFFBDH (DRC1) After reset: 00H R/W

| Symbol | <7>  | 6 | 5 | 4 | 3 | 2 | 1 | <0>  |
|--------|------|---|---|---|---|---|---|------|
| DRCn   | DENn | 0 | 0 | 0 | 0 | 0 | 0 | DSTn |

| DENn                                                                                  | DMA operation enable flag                                           |
|---------------------------------------------------------------------------------------|---------------------------------------------------------------------|
| 0                                                                                     | Disables operation of DMA channel n (stops operating clock of DMA). |
| 1                                                                                     | Enables operation of DMA channel n.                                 |
| DMAC waits for a DMA trigger when DSTn = 1 after DMA operation is enabled (DENn = 1). |                                                                     |

| DSTn                                                                                                                                                                                                                                                                                                                                                                                   | DMA transfer mode flag                                                  |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------|
| 0                                                                                                                                                                                                                                                                                                                                                                                      | DMA transfer of DMA channel n is completed.                             |
| 1                                                                                                                                                                                                                                                                                                                                                                                      | DMA transfer of DMA channel n is not completed (still under execution). |
| DMAC waits for a DMA trigger when DSTn = 1 after DMA operation is enabled (DENn = 1).<br>When a software trigger (STGn) or the start source trigger set by the IFCn3 to IFCn0 bits is input, DMA transfer is started.<br>When DMA transfer is completed after that, this bit is automatically cleared to 0.<br>Write 0 to this bit to forcibly terminate DMA transfer under execution. |                                                                         |

**Caution** The DSTn flag is automatically cleared to 0 when a DMA transfer is completed. Writing the DENn flag is enabled only when DSTn = 0. When a DMA transfer is terminated without waiting for generation of the interrupt (INTDMA<sub>n</sub>) of DMA<sub>n</sub>, therefore, set the DSTn bit to 0 and then the DENn bit to 0 (for details, refer to 16.5.5 Forced termination by software).

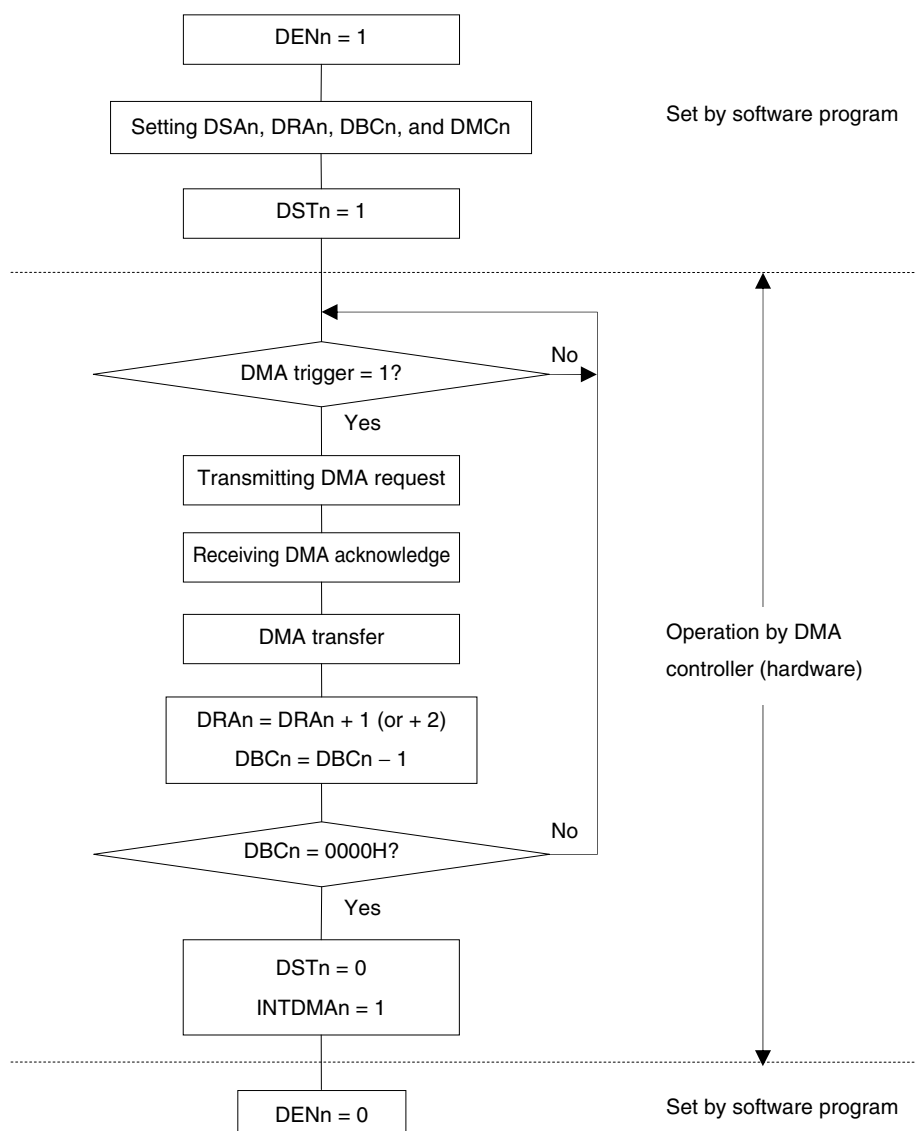
**Remark** n: DMA channel number (n = 0, 1)

## 16.4 Operation of DMA Controller

### 16.4.1 Operation procedure

- <1> The DMA controller is enabled to operate when DENn = 1. Before writing the other registers, be sure to set the DENn bit to 1. Use 80H to write with an 8-bit manipulation instruction.
- <2> Set an SFR address, a RAM address, the number of times of transfer, and a transfer mode of DMA transfer to DMA SFR address register n (DSAn), DMA RAM address register n (DRAn), DMA byte count register n (DBCn), and DMA mode control register n (DMCn).
- <3> The DMA controller waits for a DMA trigger when DSTn = 1. Use 81H to write with an 8-bit manipulation instruction.
- <4> When a software trigger (STGn) or a start source trigger specified by the IFCn3 to IFCn0 bits is input, a DMA transfer is started.
- <5> Transfer is completed when the number of times of transfer set by the DBCn register reaches 0, and transfer is automatically terminated by occurrence of an interrupt (INTDMA<sub>n</sub>).
- <6> Stop the operation of the DMA controller by clearing the DENn bit to 0 when the DMA controller is not used.

**Figure 16-6. Operation Procedure**



**Remark** n: DMA channel number (n = 0, 1)

### 16.4.2 Transfer mode

The following four modes can be selected for DMA transfer by using bits 6 and 5 (DRSn and DS<sub>n</sub>) of DMA mode control register n (DMCn).

| DRSn | DS <sub>n</sub> | DMA Transfer Mode                                                                      |
|------|-----------------|----------------------------------------------------------------------------------------|
| 0    | 0               | Transfer from SFR of 1-byte data (fixed address) to RAM (address is incremented by +1) |
| 0    | 1               | Transfer from SFR of 2-byte data (fixed address) to RAM (address is incremented by +2) |
| 1    | 0               | Transfer from RAM of 1-byte data (address is incremented by +1) to SFR (fixed address) |
| 1    | 1               | Transfer from RAM of 2-byte data (address is incremented by +2) to SFR (fixed address) |

By using these transfer modes, up to 1024 bytes of data can be consecutively transferred by using the serial interface, data resulting from A/D conversion can be consecutively transferred, and port data can be scanned at fixed time intervals by using a timer.

### 16.4.3 Termination of DMA transfer

When DBCn = 00H and DMA transfer is completed, the DSTn bit is automatically cleared to 0. An interrupt request (INTDMA<sub>n</sub>) is generated and transfer is terminated.

When the DSTn bit is cleared to 0 to forcibly terminate DMA transfer, DMA byte count register n (DBCn) and DMA RAM address register n (DRAn) hold the value when transfer is terminated.

The interrupt request (INTDMA<sub>n</sub>) is not generated if transfer is forcibly terminated.

**Remark** n: DMA channel number (n = 0, 1)

## 16.5 Example of Setting of DMA Controller

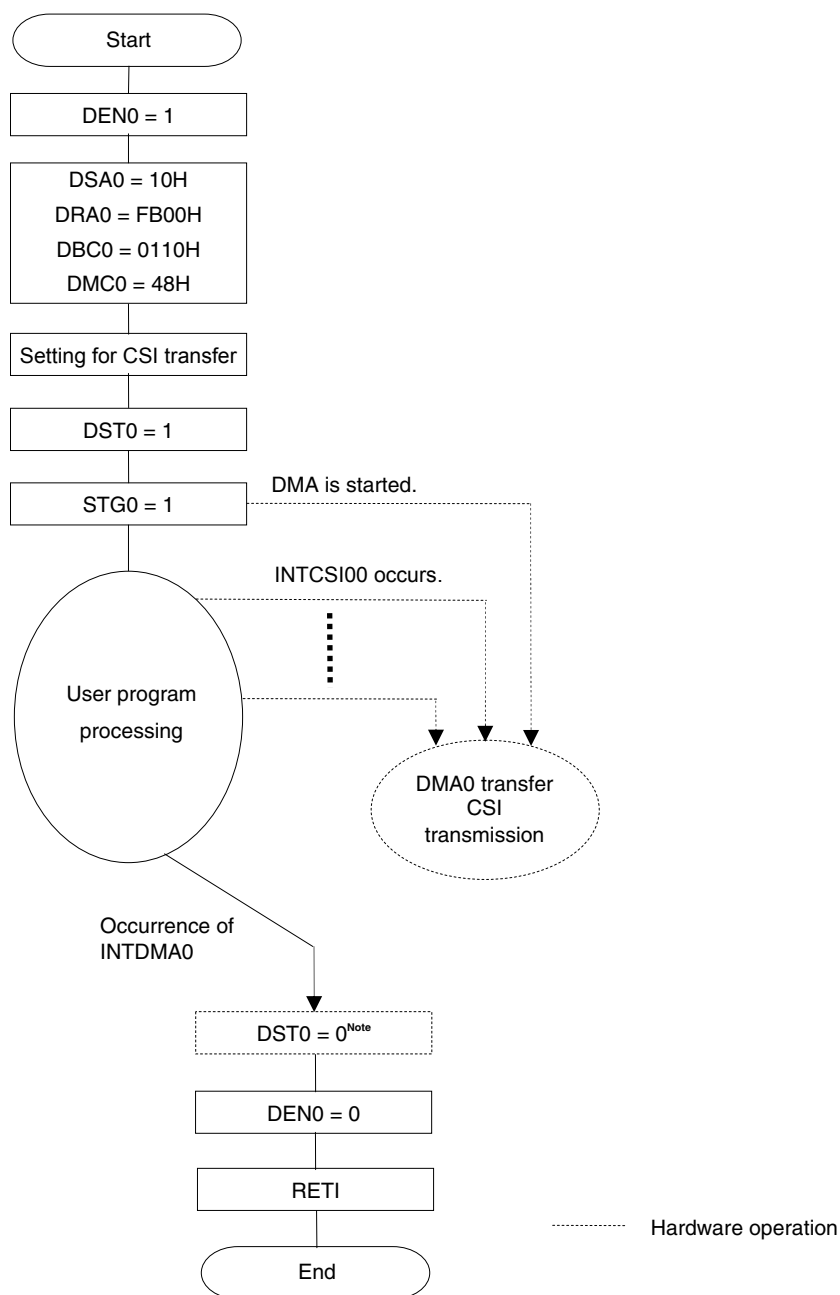
### 16.5.1 CSI consecutive transmission

A flowchart showing an example of setting for CSI consecutive transmission is shown below.

- Consecutive transmission of CSI00 (256 bytes)
- DMA channel 0 is used for DMA transfer.
- DMA start source: INTCSI00 (software trigger (STG0) only for the first start source)
- Interrupt of CSI00 is specified by IFC03 to IFC00 = 0110B.
- Transfers FFB00H to FFBFFH (256 bytes) of RAM to FFF10H of the data register (SIO00) of CSI.

**Remark** IFC03 to IFC00: Bits 3 to 0 of DMA mode control registers 0 (DMC0)

Figure 16-7. Example of Setting for CSI Consecutive Transmission



**Note** The DST0 flag is automatically cleared to 0 when a DMA transfer is completed.

Writing the DEN0 flag is enabled only when DST0 = 0. To terminate a DMA transfer without waiting for occurrence of the interrupt of DMA0 (INTDMA0), set the DST0 bit to 0 and then the DEN0 bit to 0 (for details, refer to **16.5.5 Forced termination by software**).

The first trigger for consecutive transmission is not started by the interrupt of CSI. In this example, it starts by a software trigger.

CSI transmission of the second time and onward is automatically executed.

A DMA interrupt (INTDMA0) occurs when the last transmit data has been written to the data register.

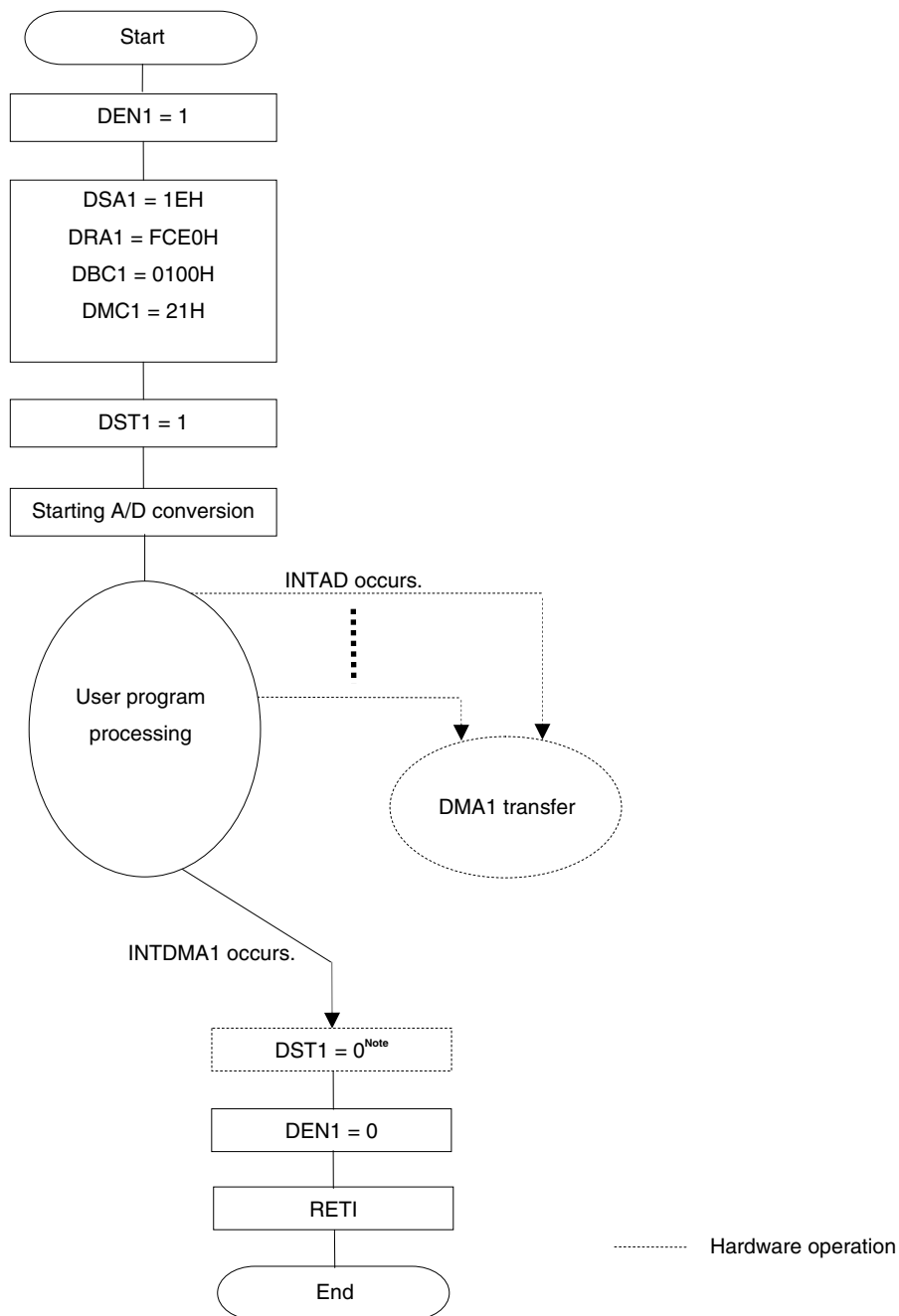
### 16.5.2 Consecutive capturing of A/D conversion results

A flowchart of an example of setting for consecutively capturing A/D conversion results is shown below.

- Consecutive capturing of A/D conversion results.
- DMA channel 1 is used for DMA transfer.
- DMA start source: INTAD
- Interrupt of A/D is specified by IFC13 to IFC10 = 0001B.
- Transfers FFF1EH and FFF1FH (2 bytes) of the 10-bit A/D conversion result register (ADCR) to 512 bytes of FFCE0H to FFEDFH of RAM.

**Remark** IFC13 to IFC10: Bits 3 to 0 of DMA mode control registers 1 (DMC1)

Figure 16-8. Example of Setting of Consecutively Capturing A/D Conversion Results



**Note** The DST1 flag is automatically cleared to 0 when a DMA transfer is completed.

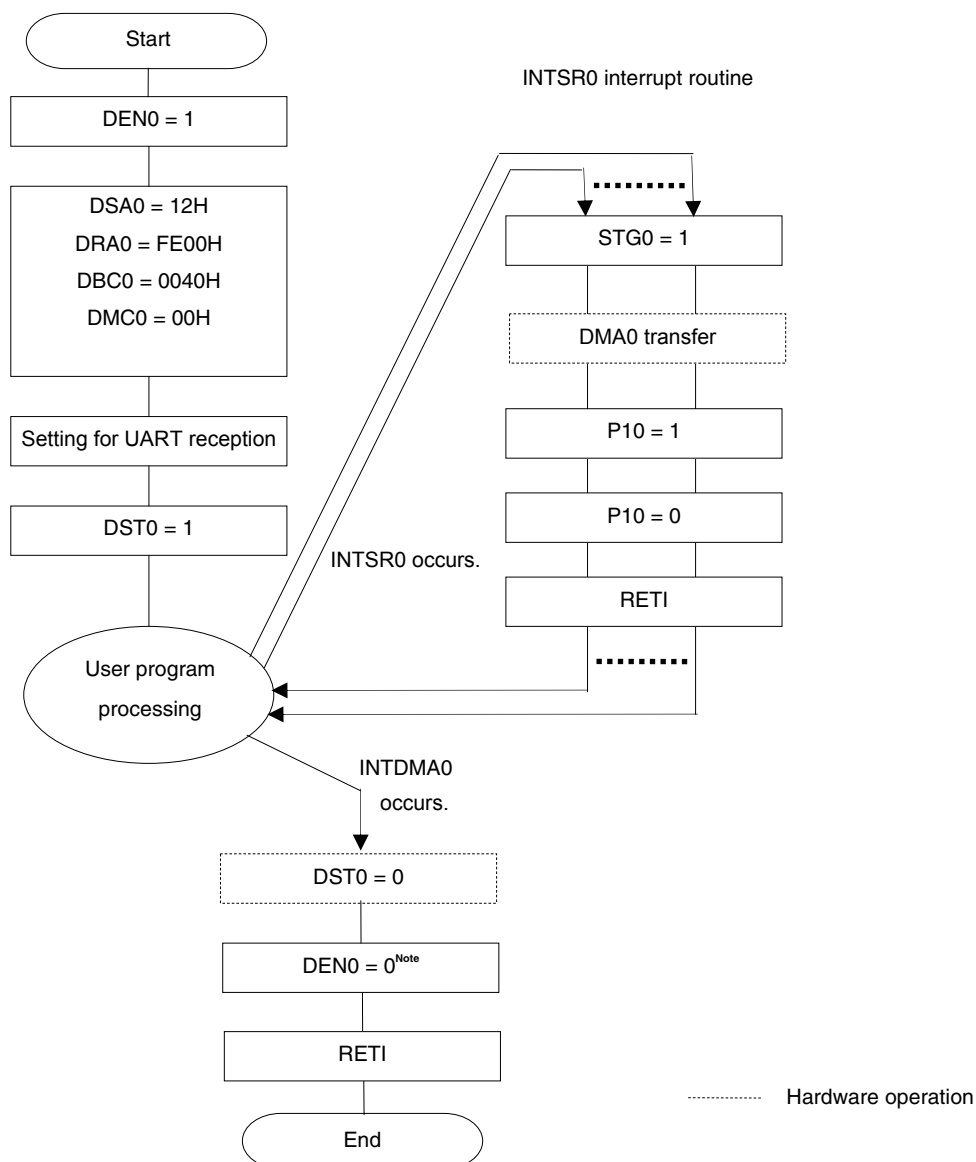
Writing the DEN1 flag is enabled only when DST1 = 0. To terminate a DMA transfer without waiting for occurrence of the interrupt of DMA1 (INTDMA1), set the DST1 bit to 0 and then the DEN1 bit to 0 (for details, refer to **16.5.5 Forced termination by software**).



### 16.5.3 UART consecutive reception + ACK transmission

A flowchart illustrating an example of setting for UART consecutive reception + ACK transmission is shown below.

- Consecutively receives data from UART0 and outputs ACK to P10 on completion of reception.
- DMA channel 0 is used for DMA transfer.
- DMA start source: Software trigger (DMA transfer on occurrence of an interrupt is disabled.)
- Transfers FFF12H of UART receive data register 0 (RXD0) to 64 bytes of FFE00H to FFE3FH of RAM.

**Figure 16-9. Example of Setting for UART Consecutive Reception + ACK Transmission**

**Note** The DST0 flag is automatically cleared to 0 when a DMA transfer is completed.

Writing the DEN0 flag is enabled only when DST0 = 0. To terminate a DMA transfer without waiting for occurrence of the interrupt of DMA0 (INTDMA0), set the DST0 bit to 0 and then the DEN0 bit to 0 (for details, refer to **16.5.5 Forced termination by software**).

**Remark** This is an example where a software trigger is used as a DMA start source.

If ACK is not transmitted and if only data is consecutively received from UART, the UART reception end interrupt (INTSR0) can be used to start DMA for data reception.

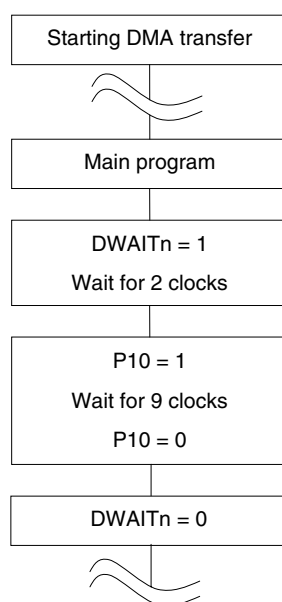
### 16.5.4 Holding DMA transfer pending by DWAITn bit

When DMA transfer is started, transfer is performed while an instruction is executed. At this time, the operation of the CPU is stopped and delayed for the duration of 2 clocks. If this poses a problem to the operation of the set system, a DMA transfer can be held pending by setting the DWAITn bit to 1. The DMA transfer for a transfer trigger that occurred while DMA transfer was held pending is executed after the pending status is canceled. However, because only one transfer trigger can be held pending for each channel, even if multiple transfer triggers occur for one channel during the pending status, only one DMA transfer is executed after the pending status is canceled.

To output a pulse with a width of 10 clocks of the operating frequency from the P10 pin, for example, the clock width increases to 12 if a DMA transfer is started midway. In this case, the DMA transfer can be held pending by setting the DWAITn bit to 1.

After setting the DWAITn bit to 1, it takes two clocks until a DMA transfer is held pending.

**Figure 16-10. Example of Setting for Holding DMA Transfer Pending by DWAITn Bit**



**Caution** When DMA transfer is held pending while using both DMA channels, be sure to held the DMA transfer pending for both channels (by setting DWAIT0 and DWAIT1 to 1). If the DMA transfer of one channel is executed while that of the other channel is held pending, DMA transfer might not be held pending for the latter channel.

**Remarks**

1. n: DMA channel number (n = 0, 1)
2. 1 clock:  $1/f_{CLK}$  ( $f_{CLK}$ : CPU clock)

### 16.5.5 Forced termination by software

After the DSTn bit is set to 0 by software, it takes up to 2 clocks until a DMA transfer is actually stopped and the DSTn bit is set to 0. To forcibly terminate a DMA transfer by software without waiting for occurrence of the interrupt (INTDMA<sub>n</sub>) of DMA<sub>n</sub>, therefore, perform either of the following processes.

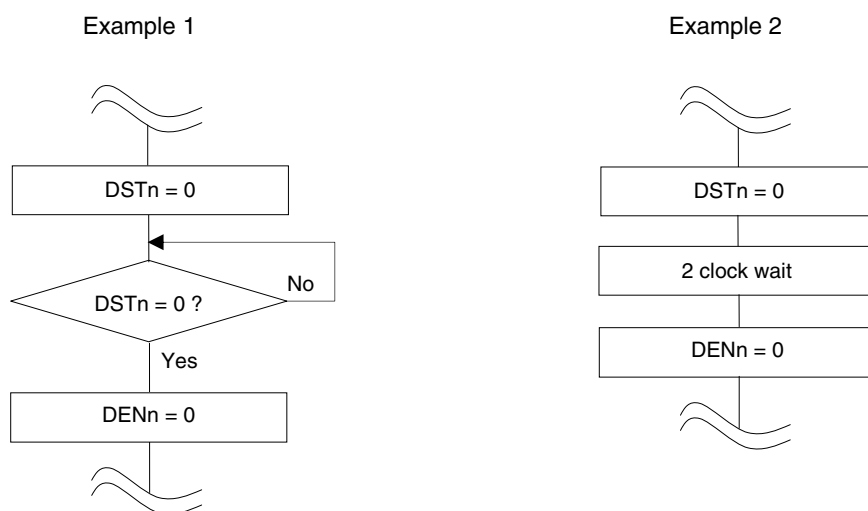
<When using one DMA channel>

- Set the DSTn bit to 0 (use DRCn = 80H to write with an 8-bit manipulation instruction) by software, confirm by polling that the DSTn bit has actually been cleared to 0, and then set the DENn bit to 0 (use DRCn = 00H to write with an 8-bit manipulation instruction).
- Set the DSTn bit to 0 (use DRCn = 80H to write with an 8-bit manipulation instruction) by software and then set the DENn bit to 0 (use DRCn = 00H to write with an 8-bit manipulation instruction) two or more clocks after.

<When using two or more DMA channels>

- To forcibly terminate DMA transfer by software when using both DMA channels (by setting DSTn to 0), clear the DSTn bit to 0 after the DMA transfer is held pending by setting the DWAIT0 and DWAIT1 bits of both channels to 1. Next, clear the DWAIT0 and DWAIT1 bits of both channels to 0 to cancel the pending status, and then clear the DENn bit to 0.

**Figure 16-11. Forced Termination of DMA Transfer (1/2)**

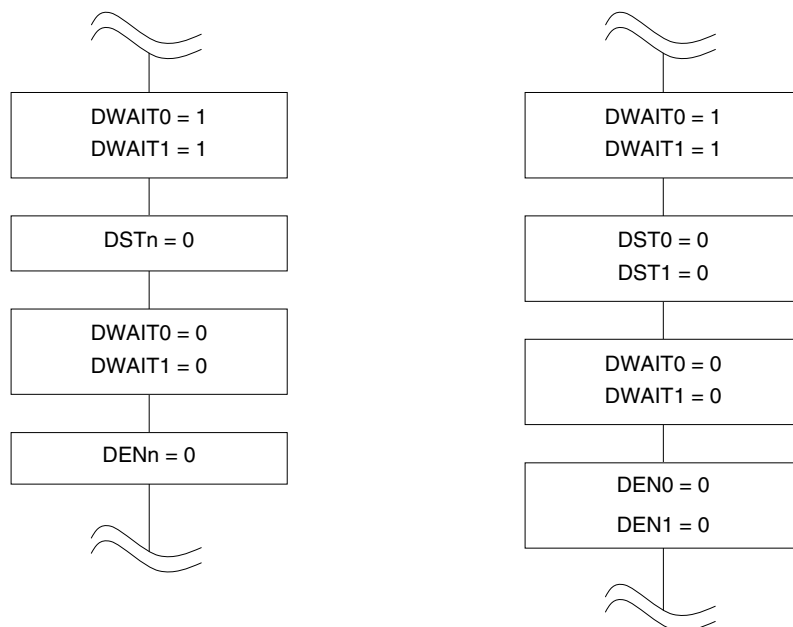


- Remarks**
1. n: DMA channel number (n = 0, 1)
  2. 1 clock:  $1/f_{CLK}$  ( $f_{CLK}$ : CPU clock)

**Figure 16-11. Forced Termination of DMA Transfer (2/2)****Example 3**

- Procedure for forcibly terminating the DMA transfer for one channel if both channels are used

- Procedure for forcibly terminating the DMA transfer for both channels if both channels are used



**Caution** In example 3, the system is not required to wait two clock cycles after the  $DWAITn$  bit is set to 1. In addition, the system does not have to wait two clock cycles after clearing the  $DSTn$  bit to 0, because more than two clock cycles elapse from when the  $DSTn$  bit is cleared to 0 to when the  $DENn$  bit is cleared to 0.

- Remarks**
1.  $n$ : DMA channel number ( $n = 0, 1$ )
  2. 1 clock:  $1/f_{CLK}$  ( $f_{CLK}$ : CPU clock)

## 16.6 Cautions on Using DMA Controller

### (1) Priority of DMA

During DMA transfer, a request from the other DMA channel is held pending even if generated. The pending DMA transfer is started after the ongoing DMA transfer is completed. If two or more DMA requests are generated at the same time, however, their priority are DMA channel 0 > DMA channel 1.

If a DMA request and an interrupt request are generated at the same time, the DMA transfer takes precedence, and then interrupt servicing is executed.

### (2) DMA response time

The response time of DMA transfer is as follows.

**Table 16-2. Response Time of DMA Transfer**

|               | Minimum Time | Maximum Time              |
|---------------|--------------|---------------------------|
| Response time | 3 clocks     | 10 clocks <sup>Note</sup> |

**Note** The maximum time necessary to execute an instruction from internal RAM is 16 clock cycles.

**Cautions 1.** The above response time does not include the two clock cycles required for a DMA transfer.

**2.** When executing a DMA pending instruction (see 16.6 (4)), the maximum response time is extended by the execution time of that instruction to be held pending.

**3.** Do not specify successive transfer triggers for a channel within a period equal to the maximum response time plus one clock cycle, because they might be ignored.

**Remark** 1 clock:  $1/f_{CLK}$  ( $f_{CLK}$ : CPU clock)

### (3) Operation in standby mode

The DMA controller operates as follows in the standby mode.

**Table 16-3. DMA Operation in Standby Mode**

| Status    | DMA Operation                                                                                                                                                       |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HALT mode | Normal operation                                                                                                                                                    |
| STOP mode | Stops operation.<br>If DMA transfer and STOP instruction execution contend, DMA transfer may be damaged. Therefore, stop DMA before executing the STOP instruction. |

**(4) DMA pending instruction**

Even if a DMA request is generated, DMA transfer is held pending immediately after the following instructions.

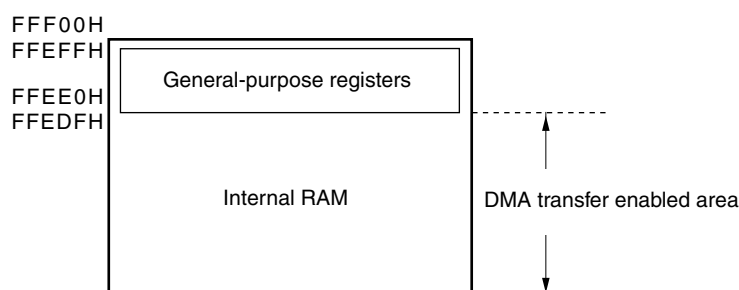
- CALL !addr16
- CALL \$!addr20
- CALL !!addr20
- CALL rp
- CALLT [addr5]
- BRK
- Bit manipulation instructions for registers IF0L, IF0H, IF1L, IF1H, IF2L, MK0L, MK0H, MK1L, MK1H, MK2L, PR00L, PR00H, PR01L, PR01H, PR02L, PR10L, PR10H, PR11L, PR11H, PR12L, and PSW each.
- Instruction for accessing the data flash memory

**(5) Operation if address in general-purpose register area or other than those of internal RAM area is specified**

The address indicated by DMA RAM address register n (DRAn) is incremented during DMA transfer. If the address is incremented to an address in the general-purpose register area or exceeds the area of the internal RAM, the following operation is performed.

- In mode of transfer from SFR to RAM  
The data of that address is lost.
- In mode of transfer from RAM to SFR  
Undefined data is transferred to SFR.

In either case, malfunctioning may occur or damage may be done to the system. Therefore, make sure that the address is within the internal RAM area other than the general-purpose register area.

**(6) Operation if instructions for accessing the data flash area**

- Because DMA transfer is suspended to access to the data flash area, be sure to add the DMA pending instruction.

If the data flash area is accessed after an next instruction execution from start of DMA transfer, a 3-clock wait will be inserted to the next instruction.

Instruction 1

DMA transfer

Instruction 2 ← The wait of three clock cycles occurs.

MOV A, ! DataFlash area

## CHAPTER 17 INTERRUPT FUNCTIONS

<R> The interrupt function switches the program execution to other processing. When the branch processing is finished, the program returns to the interrupted processing.

The number of interrupt sources differs, depending on the product.

|                     |          | 32-pin | 44-pin | 48-pin | 52-pin | 64-pin |
|---------------------|----------|--------|--------|--------|--------|--------|
| Maskable interrupts | External | 4      | 6      | 7      | 7      | 9      |
|                     | Internal | 23     | 23     | 23     | 23     | 23     |

### 17.1 Interrupt Function Types

The following two types of interrupt functions are used.

#### (1) Maskable interrupts

These interrupts undergo mask control. Maskable interrupts can be divided into four priority groups by setting the priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H). Multiple interrupt servicing can be applied to low-priority interrupts when high-priority interrupts are generated. If two or more interrupt requests, each having the same priority, are simultaneously generated, then they are processed according to the priority of vectored interrupt servicing. For the priority order, see **Table 17-1**.

A standby release signal is generated and STOP, HALT, and SNOOZE modes are released.

External interrupt requests and internal interrupt requests are provided as maskable interrupts.

#### (2) Software interrupt

This is a vectored interrupt generated by executing the BRK instruction. It is acknowledged even when interrupts are disabled. The software interrupt does not undergo interrupt priority control.

### 17.2 Interrupt Sources and Configuration

Interrupt sources include maskable interrupts and software interrupts. In addition, they also have up to seven reset sources (see **Table 17-1**). The vector codes that store the program start address when branching due to the generation of a reset or various interrupt requests are two bytes each, so interrupts jump to a 64 K address of 00000H to 0FFFFH.



Table 17-1. Interrupt Source List (1/3)

| Interrupt Type | Default Priority <sup>Note 1</sup> | Interrupt Source |                                                                                          | Internal/ External | Vector Table Address | Basic Configuration Type <sup>Note 2</sup> | 64-pin | 52-pin | 48-pin | 44-pin | 32-pin |
|----------------|------------------------------------|------------------|------------------------------------------------------------------------------------------|--------------------|----------------------|--------------------------------------------|--------|--------|--------|--------|--------|
|                |                                    | Name             | Trigger                                                                                  |                    |                      |                                            |        |        |        |        |        |
| Maskable       | 0                                  | INTWDTI          | Watchdog timer interval <sup>Note 3</sup><br>(75% of overflow time +1/2f <sub>IL</sub> ) | Internal           | 0004H                | (A)                                        | √      | √      | √      | √      | √      |
|                | 1                                  | INTLVI           | Voltage detection <sup>Note 4</sup>                                                      |                    | 0006H                |                                            | √      | √      | √      | √      | √      |
|                | 2                                  | INTP0            | Pin input edge detection                                                                 | External           | 0008H                | (B)                                        | √      | √      | √      | √      | √      |
|                | 3                                  | INTP1            |                                                                                          |                    | 000AH                |                                            | √      | √      | √      | √      | √      |
|                | 4                                  | INTP2            |                                                                                          |                    | 000CH                |                                            | √      | √      | √      | √      | √      |
|                | 5                                  | INTP3            |                                                                                          |                    | 000EH                |                                            | √      | √      | √      | √      | —      |
|                | 6                                  | INTP4            |                                                                                          |                    | 0010H                |                                            | √      | √      | √      | √      | —      |
|                | 7                                  | INTP5            |                                                                                          |                    | 0012H                |                                            | √      | √      | √      | —      | —      |
|                | 8                                  | INTDMA0          | End of DMA0 transfer                                                                     | Internal           | 0014H                | (A)                                        | √      | √      | √      | √      | √      |
|                | 9                                  | INTDMA1          | End of DMA1 transfer                                                                     |                    | 0016H                |                                            | √      | √      | √      | √      | √      |
|                | 10                                 | INTST0           | UART0 transmission transfer end or buffer empty interrupt                                |                    | 0018H                |                                            | √      | √      | √      | √      | √      |
|                |                                    | INTCSI00         | CSI00 transfer end or buffer empty interrupt                                             |                    |                      |                                            | √      | √      | √      | √      | √      |
|                | 11                                 | INTSR0           | UART0 reception transfer end                                                             |                    | 001AH                |                                            | √      | √      | √      | √      | √      |
|                |                                    | INTCSI01         | CSI01 transfer end or buffer empty interrupt                                             |                    |                      |                                            | √      | √      | √      | √      | √      |
|                | 12                                 | INTSRE0          | UART0 reception communication error occurrence                                           |                    | 001CH                |                                            | √      | √      | √      | √      | √      |
|                |                                    | INTTM01H         | End of timer channel 01 count or capture (at higher 8-bit timer operation)               |                    |                      |                                            | √      | √      | √      | √      | √      |
|                | 13                                 | INTTM00          | End of timer channel 00 count or capture                                                 |                    | 0020H                |                                            | √      | √      | √      | √      | √      |
|                | 14                                 | INTTM03H         | End of timer channel 03 count or capture (at higher 8-bit timer operation)               |                    | 0024H                |                                            | √      | √      | √      | √      | √      |

- Notes**
1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 31 indicates the lowest priority.
  2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 17-1.
  3. When bit 7 (WDTINT) of the option byte (000C0H) is set to 1.
  4. When bit 7 (LVIMD) of the voltage detection level register (LVIS) is cleared to 0.

**Remark**

√: Mounted  
—: Not mounted

Table 17-1. Interrupt Source List (2/3)

| Interrupt Type | Default Priority<br><small>Note 1</small> | Interrupt Source |                                                             | Internal/<br>External | Vector<br>Table<br>Address | Basic Configuration<br>Type<br><small>Note 2</small> | 64-pin | 52-pin | 48-pin | 44-pin | 32-pin |
|----------------|-------------------------------------------|------------------|-------------------------------------------------------------|-----------------------|----------------------------|------------------------------------------------------|--------|--------|--------|--------|--------|
|                |                                           | Name             | Trigger                                                     |                       |                            |                                                      |        |        |        |        |        |
| Maskable       | 15                                        | INTIICA0         | End of IICA0 communication                                  | Internal              | 0026H                      | (A)                                                  | √      | √      | √      | √      | √      |
|                | 16                                        | INTTM01          | End of timer channel 01 count or capture                    |                       | 0028H                      | (A)                                                  | √      | √      | √      | √      | √      |
|                | 17                                        | INTTM02          | End of timer channel 02 count or capture                    |                       | 002AH                      |                                                      | √      | √      | √      | √      | √      |
|                | 18                                        | INTTM03          | End of timer channel 03 count or capture                    |                       | 002CH                      |                                                      | √      | √      | √      | √      | √      |
|                | 19                                        | INTAD            | End of A/D conversion                                       |                       | 002EH                      |                                                      | √      | √      | √      | √      | √      |
|                | 20                                        | INTRTC           | Fixed-cycle signal of real-time clock/alarm match detection |                       | 0030H                      |                                                      | √      | √      | √      | √      | √      |
|                | 21                                        | INTIT            | Interval signal detection                                   |                       | 0032H                      |                                                      | √      | √      | √      | √      | √      |
|                | 22                                        | INTKR            | Key return signal detection                                 | External              | 0034H                      | (C)                                                  | √      | √      | √      | √      | √      |
|                | 23                                        | INTTM04          | End of timer channel 04 count or capture                    | Internal              | 003CH                      | (A)                                                  | √      | √      | √      | √      | √      |
|                | 24                                        | INTTM05          | End of timer channel 05 count or capture                    |                       | 003EH                      |                                                      | √      | √      | √      | √      | √      |
|                | 25                                        | INTTM06          | End of timer channel 06 count or capture                    |                       | 0040H                      |                                                      | √      | √      | √      | √      | √      |
|                | 26                                        | INTTM07          | End of timer channel 07 count or capture                    |                       | 0042H                      |                                                      | √      | √      | √      | √      | √      |
|                | 27                                        | INTLCD0          | LCD flame interrupt                                         |                       | 0044H                      |                                                      | √      | √      | √      | √      | √      |
|                | 28                                        | INTP6            | Pin input edge detection                                    | External              | 0046H                      | (B)                                                  | √      | —      | —      | —      | —      |
|                | 29                                        | INTP7            |                                                             |                       | 0048H                      |                                                      | √      | —      | —      | —      | —      |
|                | 30                                        | INTMD            | End of division operation/<br>Overflow occur                | Internal              | 004AH                      | (A)                                                  | √      | √      | √      | √      | √      |
|                | 31                                        | INTFL            | End of sequencer interrupt <small>Note 3</small>            |                       | 004CH                      |                                                      | √      | √      | √      | √      | √      |

- Notes**
1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 31 indicates the lowest priority.
  2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 17-1.
  3. Be used only at the self programming library.

**Remark**    √: Mounted  
                  —: Not mounted

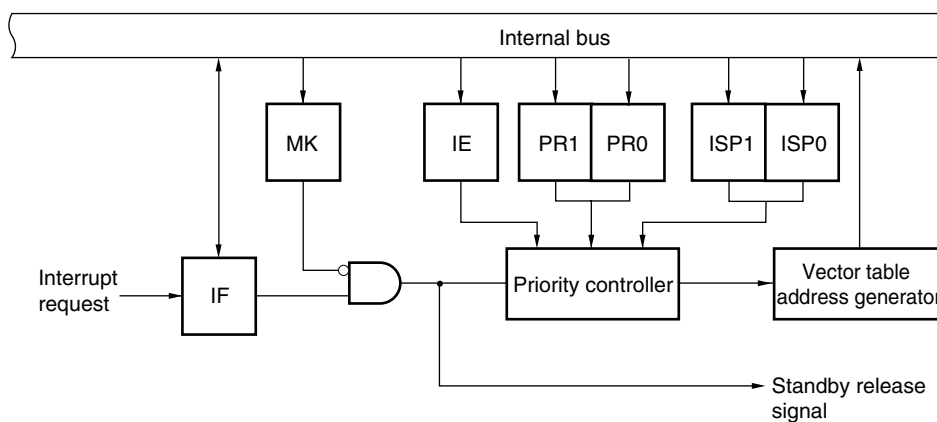
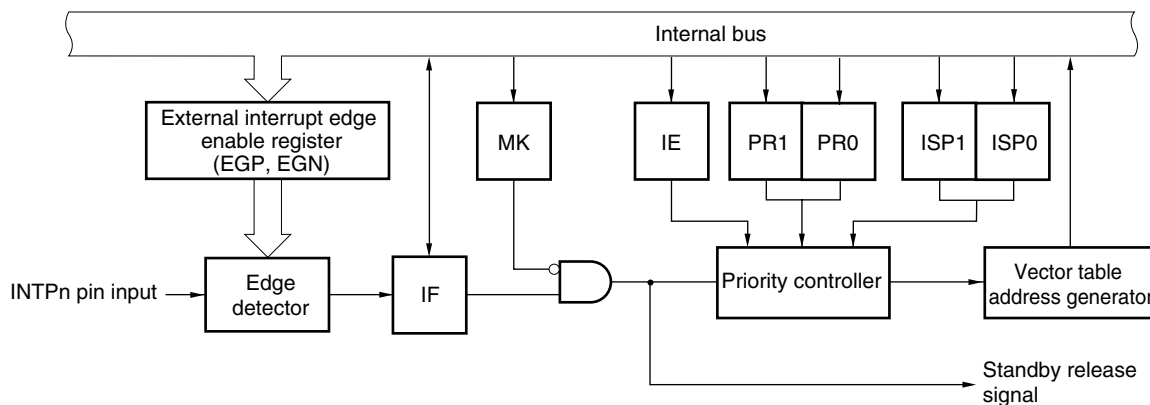
Table 17-1. Interrupt Source List (3/3)

| Interrupt Type | Default Priority<br><small>Note 1</small> | Interrupt Source |                                                    | Internal/<br>External | Vector<br>Table<br>Address | Basic Configuration<br>Type<br><small>Note 2</small> | 64-pin | 52-pin | 48-pin | 44-pin | 32-pin |
|----------------|-------------------------------------------|------------------|----------------------------------------------------|-----------------------|----------------------------|------------------------------------------------------|--------|--------|--------|--------|--------|
| Software       | –                                         | BRK              | Execution of BRK instruction                       | –                     | 007EH                      | (D)                                                  | √      | √      | √      | √      | √      |
| Reset          | –                                         | RESET            | RESET pin input                                    | –                     | 0000H                      | –                                                    | √      | √      | √      | √      | √      |
|                |                                           | POR              | Power-on-reset                                     |                       |                            |                                                      | √      | √      | √      | √      | √      |
|                |                                           | LVD              | Voltage detection <sup>Note 3</sup>                |                       |                            |                                                      | √      | √      | √      | √      | √      |
|                |                                           | WDT              | Overflow of watchdog timer                         |                       |                            |                                                      | √      | √      | √      | √      | √      |
|                |                                           | TRAP             | Execution of illegal instruction <sup>Note 4</sup> |                       |                            |                                                      | √      | √      | √      | √      | √      |
|                |                                           | IAW              | Illegal-memory access                              |                       |                            |                                                      | √      | √      | √      | √      | √      |
|                |                                           | RPE              | RAM parity error                                   |                       |                            |                                                      | √      | √      | √      | √      | √      |

- Notes**
1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 31 indicates the lowest priority.
  2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 17-1.
  3. When bit 7 (LVIMD) of the voltage detection level register (LVIS) is set to 1.
  4. When the instruction code in FFH is executed.  
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

**Remark**    √: Mounted

Figure 17-1. Basic Configuration of Interrupt Function (1/2)

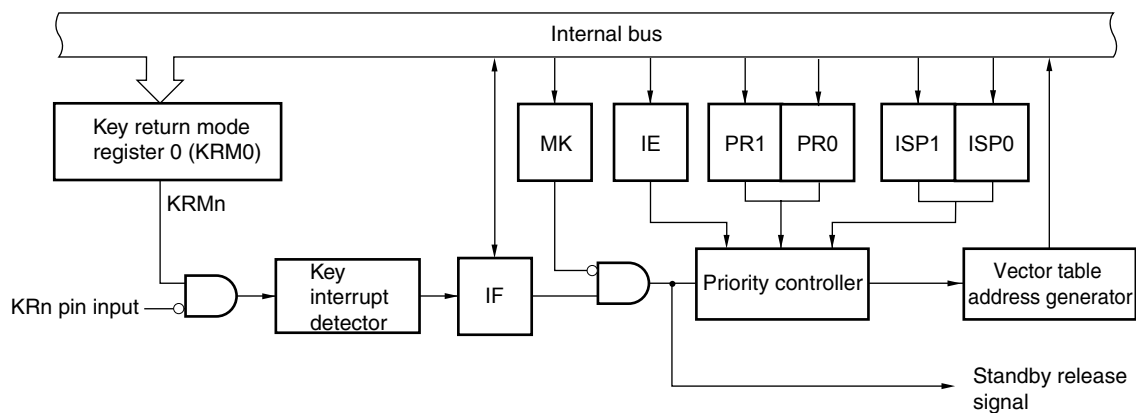
**(A) Internal maskable interrupt****(B) External maskable interrupt (INTPn)**

IF: Interrupt request flag  
 IE: Interrupt enable flag  
 ISP0: In-service priority flag 0  
 ISP1: In-service priority flag 1  
 MK: Interrupt mask flag  
 PR0: Priority specification flag 0  
 PR1: Priority specification flag 1

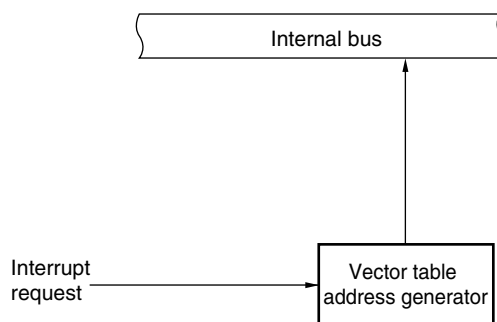
**Remark** 32-pin: n = 0 to 2  
 44-pin: n = 0 to 4  
 48, 52-pin: n = 0 to 5  
 64-pin: n = 0 to 7

Figure 17-1. Basic Configuration of Interrupt Function (2/2)

## (C) External maskable interrupt (INTKR)



## (D) Software interrupt



IF: Interrupt request flag  
 IE: Interrupt enable flag  
 ISP0: In-service priority flag 0  
 ISP1: In-service priority flag 1  
 MK: Interrupt mask flag  
 PR0: Priority specification flag 0  
 PR1: Priority specification flag 1

**Remark** n = 0 to 3

### 17.3 Registers Controlling Interrupt Functions

The following 6 types of registers are used to control the interrupt functions.

- Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L)
- Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H, MK2L)
- Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR10L, PR10H, PR11L, PR11H, PR12L)
- External interrupt rising edge enable register (EGP0)
- External interrupt falling edge enable register (EGN0)
- Program status word (PSW)

Table 17-2 shows a list of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

**Table 17-2. Flags Corresponding to Interrupt Request Sources (1/3)**

| Interrupt Source | Interrupt Request Flag |          | Interrupt Mask Flag |          | Priority Specification Flag |              | 64-pin | 52-pin | 48-pin | 44-pin | 32-pin |
|------------------|------------------------|----------|---------------------|----------|-----------------------------|--------------|--------|--------|--------|--------|--------|
|                  |                        | Register |                     | Register |                             | Register     |        |        |        |        |        |
| INTWDTI          | WDTIIF                 | IF0L     | WDTIMK              | MK0L     | WDTIPR0, WDTIPR1            | PR00L, PR10L | √      | √      | √      | √      | √      |
| INTLVI           | LVIIIF                 |          | LVIMK               |          | LVIPR0, LVIPR1              |              | √      | √      | √      | √      | √      |
| INTP0            | PIF0                   |          | PMK0                |          | PPR00, PPR10                |              | √      | √      | √      | √      | √      |
| INTP1            | PIF1                   |          | PMK1                |          | PPR01, PPR11                |              | √      | √      | √      | √      | √      |
| INTP2            | PIF2                   |          | PMK2                |          | PPR02, PPR12                |              | √      | √      | √      | √      | √      |
| INTP3            | PIF3                   |          | PMK3                |          | PPR03, PPR13                |              | √      | √      | √      | √      | —      |
| INTP4            | PIF4                   |          | PMK4                |          | PPR04, PPR14                |              | √      | √      | √      | √      | —      |
| INTP5            | PIF5                   |          | PMK5                |          | PPR05, PPR15                |              | √      | √      | √      | —      | —      |

**Remark**    √: Mounted  
                  —: Not mounted

Table 17-2. Flags Corresponding to Interrupt Request Sources (2/3)

| Interrupt Source           | Interrupt Request Flag    |          | Interrupt Mask Flag       |          | Priority Specification Flag          |                 | 64-pin | 52-pin | 48-pin | 44-pin | 32-pin |
|----------------------------|---------------------------|----------|---------------------------|----------|--------------------------------------|-----------------|--------|--------|--------|--------|--------|
|                            |                           | Register |                           | Register |                                      | Register        |        |        |        |        |        |
| INTDMA0                    | DMAIF0                    | IF0H     | DMAMK0                    | MK0H     | DMAPR00, DMAPR10                     | PR00H,<br>PR10H | √      | √      | √      | √      | √      |
| INTDMA1                    | DMAIF1                    |          | DMAMK1                    |          | DMAPR01, DMAPR11                     |                 | √      | √      | √      | √      | √      |
| INTST0 <sup>Note 1</sup>   | STIF0 <sup>Note 1</sup>   |          | STMK0 <sup>Note 1</sup>   |          | STPR00, STPR10 <sup>Note 1</sup>     |                 | √      | √      | √      | √      | √      |
| INTCSI00 <sup>Note 1</sup> | CSIF00 <sup>Note 1</sup>  |          | CSIMK00 <sup>Note 1</sup> |          | CSIPR000, CSIPR100 <sup>Note 1</sup> |                 | √      | √      | √      | √      | √      |
| INTSR0 <sup>Note 2</sup>   | SRIF0 <sup>Note 2</sup>   |          | SRMK0 <sup>Note 2</sup>   |          | SRPR00, SRPR10 <sup>Note 2</sup>     |                 | √      | √      | √      | √      | √      |
| INTCSI01 <sup>Note 2</sup> | CSIF01 <sup>Note 2</sup>  |          | CSIMK01 <sup>Note 2</sup> |          | CSIPR001, CSIPR101 <sup>Note 2</sup> |                 | √      | √      | √      | √      | √      |
| INTSRE0 <sup>Note 3</sup>  | SREIF0 <sup>Note 3</sup>  |          | SREMK0 <sup>Note 3</sup>  |          | SREPR00, SREPR10 <sup>Note 3</sup>   |                 | √      | √      | √      | √      | √      |
| INTTM01H <sup>Note 3</sup> | TMIF01H <sup>Note 3</sup> |          | TMMK01H <sup>Note 3</sup> |          | TMPR001H, TMPR101H <sup>Note 3</sup> |                 | √      | √      | √      | √      | √      |
| INTTM00                    | TMIF00                    | IF1L     | TMMK00                    | MK1L     | TMPR000, TMPR100                     | PR01L,<br>PR11L | √      | √      | √      | √      | √      |
| INTTM03H                   | TMIF03H                   |          | TMMK03H                   |          | TMPR003H, TMPR103H                   |                 | √      | √      | √      | √      | √      |
| INTIICA0                   | IICAIF0                   |          | IICAMK0                   |          | IICAPR00, IICAPR10                   |                 | √      | √      | √      | √      | √      |
| INTTM01                    | TMIF01                    |          | TMMK01                    |          | TMPR001, TMPR101                     |                 | √      | √      | √      | √      | √      |
| INTTM02                    | TMIF02                    |          | TMMK02                    |          | TMPR002, TMPR102                     |                 | √      | √      | √      | √      | √      |
| INTTM03                    | TMIF03                    |          | TMMK03                    |          | TMPR003, TMPR103                     |                 | √      | √      | √      | √      | √      |
| INTAD                      | ADIF                      |          | ADMK                      |          | ADPR0, ADPR1                         |                 | √      | √      | √      | √      | √      |
| INTRTC                     | RTCIF                     |          | RTCMK                     |          | RTCPR0, RTCPR1                       |                 | √      | √      | √      | √      | √      |
| INTIT                      | ITIF                      |          | ITMK                      |          | ITPR0, ITPR1                         |                 | √      | √      | √      | √      | √      |

**Notes 1.** If one of the interrupt sources INTST0 and INTCSI00 is generated, bit 2 of the IF0H register is set to 1. Bit 2 of the MK0H, PR00H, and PR10H registers supports these two interrupt sources.

**2.** If one of the interrupt sources INTSR0 and INTCSI01 is generated, bit 3 of the IF0H register is set to 1. Bit 3 of the MK0H, PR00H, and PR10H registers supports these two interrupt sources.

**3.** Do not use UART0 and channel 1 of TAU0 (at higher 8-bit timer operation) at the same time because they share flags for the interrupt request sources. If one of the interrupt sources INTSRE0 and INTTM01H is generated, bit 4 of the IF0H register is set to 1. Bit 4 of the MK0H, PR00H, and PR10H registers supports these two interrupt sources.

**Remark** √: Mounted

Table 17-2. Flags Corresponding to Interrupt Request Sources (3/3)

| Interrupt Source | Interrupt Request Flag |          | Interrupt Mask Flag |          | Priority Specification Flag |          | 64-pin | 52-pin | 48-pin | 44-pin | 32-pin |
|------------------|------------------------|----------|---------------------|----------|-----------------------------|----------|--------|--------|--------|--------|--------|
|                  |                        | Register |                     | Register |                             | Register |        |        |        |        |        |
| INTKR            | KRIF                   | IF1H     | KRMK                | MK1H     | KRPR0, KRPR1                | PR01H,   | √      | √      | √      | √      | √      |
| INTTM04          | TMIF04                 |          | TMMK04              |          | TMPR004, TMPR104            | PR11H    | √      | √      | √      | √      | √      |
| INTTM05          | TMIF05                 |          | TMMK05              |          | TMPR005, TMPR105            |          | √      | √      | √      | √      | √      |
| INTTM06          | TMIF06                 |          | TMMK06              |          | TMPR006, TMPR106            |          | √      | √      | √      | √      | √      |
| INTTM07          | TMIF07                 |          | TMMK07              |          | TMPR007, TMPR107            |          | √      | √      | √      | √      | √      |
| INTLCD0          | LCIF0                  | IF2L     | LCMK0               | MK2L     | LCPR00, LCPR10              | PR02L,   | √      | √      | √      | √      | √      |
| INTP6            | PIF6                   |          | PMK6                |          | PPR06, PPR16                | PR12L    | √      | –      | –      | –      | –      |
| INTP7            | PIF7                   |          | PMK7                |          | PPR07, PPR17                |          | √      | –      | –      | –      | –      |
| INTMD            | MDIF                   |          | MDMK                |          | MDPR0, MDPR1                |          | √      | √      | √      | √      | √      |
| INTFL            | FLIF                   |          | FLMK                |          | FLPR0, FLPR1                |          | √      | √      | √      | √      | √      |

**Remark**    √: Mounted  
                  –: Not mounted



### 17.3.1 Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L)

The interrupt request flags are set to 1 when the corresponding interrupt request is generated or an instruction is executed. They are cleared to 0 when an instruction is executed upon acknowledgment of an interrupt request or upon reset signal generation.

When an interrupt is acknowledged, the interrupt request flag is automatically cleared and then the interrupt routine is entered.

The IF0L, IF0H, IF1L, IF1H, and IF2L registers can be set by a 1-bit or 8-bit memory manipulation instruction. When the IF0L and IF0H registers, the IF1L and IF1H registers are combined to form 16-bit registers IF0 and IF1, they can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

**Remark** If an instruction that writes data to this register is executed, the number of instruction execution clocks increases by 2 clocks.

**Figure 17-2. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H, IF2L) (64-pin products)**

Address: FF0E0H After reset: 00H R/W

| Symbol | <7>  | <6>  | <5>  | <4>  | <3>  | <2>  | <1>  | <0>   |
|--------|------|------|------|------|------|------|------|-------|
| IF0L   | PIF5 | PIF4 | PIF3 | PIF2 | PIF1 | PIF0 | LVIF | WDTIF |

Address: FF0E1H After reset: 00H R/W

| Symbol | 7 | <6>    | <5> | <4>               | <3>             | <2>             | <1>    | <0>    |
|--------|---|--------|-----|-------------------|-----------------|-----------------|--------|--------|
| IF0H   | 0 | TMIF00 | 0   | SREIF0<br>TMIF01H | SRIF0<br>CSIF01 | STIF0<br>CSIF00 | DMAIF1 | DMAIF0 |

Address: FF0E2H After reset: 00H R/W

| Symbol | <7>  | <6>   | <5>  | <4>    | <3>    | <2>    | <1>    | <0>     |
|--------|------|-------|------|--------|--------|--------|--------|---------|
| IF1L   | ITIF | RTCIF | ADIF | TMIF03 | TMIF02 | TMIF01 | IICAF0 | TMIF03H |

Address: FF0E3H After reset: 00H R/W

| Symbol | <7>    | <6>    | <5>    | <4>    | 3 | 2 | 1 | <0>  |
|--------|--------|--------|--------|--------|---|---|---|------|
| IF1H   | TMIF07 | TMIF06 | TMIF05 | TMIF04 | 0 | 0 | 0 | KRIF |

Address: FF0D0H After reset: 00H R/W

| Symbol | 7 | 6 | 5 | <4>  | <3>  | <2>  | <1>  | <0>   |
|--------|---|---|---|------|------|------|------|-------|
| IF2L   | 0 | 0 | 0 | FLIF | MDIF | PIF7 | PIF6 | LCIF0 |

| XXIFX | Interrupt request flag                                   |
|-------|----------------------------------------------------------|
| 0     | No interrupt request signal is generated                 |
| 1     | Interrupt request is generated, interrupt request status |

(Cautions are listed on the next page)

&lt;R&gt;

**Cautions** 1. The above is the bit layout for the 64-pin products. The available bits differ depending on the product. For details about the bits available for each product, see Table 17-2. Be sure to clear bits that are not available to 0.

2. When manipulating a flag of the interrupt request flag register, use a 1-bit memory manipulation instruction (CLR1). When describing in C language, use a bit manipulation instruction such as “IF0L.0 = 0;” or “\_asm(“clr1 IF0L, 0”);” because the compiled assembler must be a 1-bit memory manipulation instruction (CLR1).

If a program is described in C language using an 8-bit memory manipulation instruction such as “IF0L &= 0xfe;” and compiled, it becomes the assembler of three instructions.

```
mov a, IF0L
and a, #0FEH
mov IF0L, a
```

In this case, even if the request flag of the another bit of the same interrupt request flag register (IF0L) is set to 1 at the timing between “mov a, IF0L” and “mov IF0L, a”, the flag is cleared to 0 at “mov IF0L, a”. Therefore, care must be exercised when using an 8-bit memory manipulation instruction in C language.

### 17.3.2 Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H, MK2L)

The interrupt mask flags are used to enable/disable the corresponding maskable interrupt servicing.

The MK0L, MK0H, MK1L, MK1H, and MK2L registers can be set by a 1-bit or 8-bit memory manipulation instruction. When the MK0L and MK0H registers, and the MK1L and MK1H registers are combined to form 16-bit registers MK0 and MK1, they can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

**Remark** If an instruction that writes data to this register is executed, the number of instruction execution clocks increases by 2 clocks.

**Figure 17-3. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H, MK2L)(64-pin products)**

Address: FFFE4H After reset: FFH R/W

| Symbol | <7>  | <6>  | <5>  | <4>  | <3>  | <2>  | <1>   | <0>    |
|--------|------|------|------|------|------|------|-------|--------|
| MK0L   | PMK5 | PMK4 | PMK3 | PMK2 | PMK1 | PMK0 | LVIMK | WDTIMK |

Address: FFFE5H After reset: FFH R/W

| Symbol | 7 | <6>    | <5> | <4>               | <3>              | <2>              | <1>    | <0>    |
|--------|---|--------|-----|-------------------|------------------|------------------|--------|--------|
| MK0H   | 1 | TMMK00 | 1   | SREMK0<br>TMMK01H | SRMK0<br>CSIMK01 | STMK0<br>CSIMK00 | DMAMK1 | DMAMK0 |

Address: FFFE6H After reset: FFH R/W

| Symbol | <7>  | <6>   | <5>  | <4>    | <3>    | <2>    | <1>     | <0>     |
|--------|------|-------|------|--------|--------|--------|---------|---------|
| MK1L   | ITMK | RTCMK | ADMK | TMMK03 | TMMK02 | TMMK01 | IICAMK0 | TMMK03H |

Address: FFFE7H After reset: FFH R/W

| Symbol | <7>    | <6>    | <5>    | <4>    | 3 | 2 | 1 | <0>  |
|--------|--------|--------|--------|--------|---|---|---|------|
| MK1H   | TMMK07 | TMMK06 | TMMK05 | TMMK04 | 1 | 1 | 1 | KRMK |

Address: FFFD4H After reset: FFH R/W

| Symbol | 7 | 6 | 5 | <4>  | <3>  | <2>  | <1>  | <0>   |
|--------|---|---|---|------|------|------|------|-------|
| MK2L   | 1 | 1 | 1 | FLMK | MDMK | PMK7 | PMK6 | LCMK0 |

| XXMKX | Interrupt servicing control  |
|-------|------------------------------|
| 0     | Interrupt servicing enabled  |
| 1     | Interrupt servicing disabled |

**Caution** The above is the bit layout for the 64-pin products. The available bits differ depending on the product. For details about the bits available for each product, see Table 17-2. Be sure to set bits that are not available to 1.

### 17.3.3 Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR10L, PR10H, PR11L, PR11H, PR12L)

The priority specification flag registers are used to set the corresponding maskable interrupt priority level.

A priority level is set by using the PR0xy and PR1xy registers in combination (xy = 0L, 0H, 1L, 1H, or 2L).

The PR00L, PR00H, PR01L, PR01H, PR02L, PR10L, PR10H, PR11L, PR11H, and PR12L registers can be set by a 1-bit or 8-bit memory manipulation instruction. If the PR00L and PR00H registers, the PR01L and PR01H registers, the PR10L and PR10H registers, and the PR11L and PR11H registers are combined to form 16-bit registers PR00, PR01, PR10, and PR11, they can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

**Remark** If an instruction that writes data to this register is executed, the number of instruction execution clocks increases by 2 clocks.

**Figure 17-4. Format of Priority Specification Flag Registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR10L, PR10H, PR11L, PR11H, PR12L) (64-pin products) (1/2)**

Address: FFFE8H After reset: FFH R/W

| Symbol | <7>   | <6>   | <5>   | <4>   | <3>   | <2>   | <1>    | <0>     |
|--------|-------|-------|-------|-------|-------|-------|--------|---------|
| PR00L  | PPR05 | PPR04 | PPR03 | PPR02 | PPR01 | PPR00 | LVIPR0 | WDTIPR0 |

Address: FFFECH After reset: FFH R/W

| Symbol | <7>   | <6>   | <5>   | <4>   | <3>   | <2>   | <1>    | <0>     |
|--------|-------|-------|-------|-------|-------|-------|--------|---------|
| PR10L  | PPR15 | PPR14 | PPR13 | PPR12 | PPR11 | PPR10 | LVIPR1 | WDTIPR1 |

Address: FFFE9H After reset: FFH R/W

| Symbol | 7 | <6>     | <5> | <4>                 | <3>                | <2>                | <1>     | <0>     |
|--------|---|---------|-----|---------------------|--------------------|--------------------|---------|---------|
| PR00H  | 1 | TMPR000 | 1   | SREPR00<br>TMPR001H | SRPR00<br>CSIPR001 | STPR00<br>CSIPR000 | DMAPR01 | DMAPR00 |

Address: FFFEDH After reset: FFH R/W

| Symbol | 7 | <6>     | <5> | <4>                 | <3>                | <2>                | <1>     | <0>     |
|--------|---|---------|-----|---------------------|--------------------|--------------------|---------|---------|
| PR10H  | 1 | TMPR100 | 1   | SREPR10<br>TMPR101H | SRPR10<br>CSIPR101 | STPR10<br>CSIPR100 | DMAPR11 | DMAPR10 |

Address: FFFEAH After reset: FFH R/W

| Symbol | <7>   | <6>     | <5>   | <4>     | <3>     | <2>     | <1>      | <0>      |
|--------|-------|---------|-------|---------|---------|---------|----------|----------|
| PR01L  | ITPR0 | RT CPR0 | ADPR0 | TMPR003 | TMPR002 | TMPR001 | IICAPR00 | TMPR003H |

Address: FFEEH After reset: FFH R/W

| Symbol | <7>   | <6>     | <5>   | <4>     | <3>     | <2>     | <1>      | <0>      |
|--------|-------|---------|-------|---------|---------|---------|----------|----------|
| PR11L  | ITPR1 | RT CPR1 | ADPR1 | TMPR103 | TMPR102 | TMPR101 | IICAPR10 | TMPR103H |

**Figure 17-4. Format of Priority Specification Flag Registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR10L, PR10H, PR11L, PR11H, PR12L) (64-pin products) (2/2)**

Address: FFFEBH After reset: FFH R/W

|        |         |         |         |         |   |   |   |       |
|--------|---------|---------|---------|---------|---|---|---|-------|
| Symbol | <7>     | <6>     | <5>     | <4>     | 3 | 2 | 1 | <0>   |
| PR01H  | TMPR007 | TMPR006 | TMPR005 | TMPR004 | 1 | 1 | 1 | KRPR0 |

Address: FFFE7H After reset: FFH R/W

|        |         |         |         |         |   |   |   |        |
|--------|---------|---------|---------|---------|---|---|---|--------|
| Symbol | <7>     | <6>     | <5>     | <4>     | 3 | 2 | 1 | <0>    |
| PR11H  | TMPR107 | TMPR106 | TMPR105 | TMPR104 | 1 | 1 | 1 | KRPR01 |

Address: FFFD8H After reset: FFH R/W

|        |   |   |   |       |       |       |       |        |
|--------|---|---|---|-------|-------|-------|-------|--------|
| Symbol | 7 | 6 | 5 | <4>   | <3>   | <2>   | <1>   | <0>    |
| PR02L  | 1 | 1 | 1 | FLPR0 | MDPR0 | PPR07 | PPR06 | LCPR00 |

Address: FFFDCH After reset: FFH R/W

|        |   |   |   |       |       |       |       |        |
|--------|---|---|---|-------|-------|-------|-------|--------|
| Symbol | 7 | 6 | 5 | <4>   | <3>   | <2>   | <1>   | <0>    |
| PR12L  | 1 | 1 | 1 | FLPR1 | MDPR1 | PPR17 | PPR16 | LCPR10 |

| XXPR1X | XXPR0X | Priority level selection              |
|--------|--------|---------------------------------------|
| 0      | 0      | Specify level 0 (high priority level) |
| 0      | 1      | Specify level 1                       |
| 1      | 0      | Specify level 2                       |
| 1      | 1      | Specify level 3 (low priority level)  |

**Caution** The above is the bit layout for the 64-pin products. The available bits differ depending on the product. For details about the bits available for each product, see Table 17-2. Be sure to set bits that are not available to 1.

### 17.3.4 External interrupt rising edge enable register (EGP0), external interrupt falling edge enable register (EGN0)

These registers specify the valid edge for INTP0 to INTP7.

The EGP0 and EGN0 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

**Figure 17-5. Format of External Interrupt Rising Edge Enable Register (EGP0) and External Interrupt Falling Edge Enable Register (EGN0) (64-pin products)**

Address: FFF38H After reset: 00H R/W

|        |      |      |      |      |      |      |      |      |
|--------|------|------|------|------|------|------|------|------|
| Symbol | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
| EGP0   | EGP7 | EGP6 | EGP5 | EGP4 | EGP3 | EGP2 | EGP1 | EGP0 |

Address: FFF39H After reset: 00H R/W

|        |      |      |      |      |      |      |      |      |
|--------|------|------|------|------|------|------|------|------|
| Symbol | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
| EGN0   | EGN7 | EGN6 | EGN5 | EGN4 | EGN3 | EGN2 | EGN1 | EGN0 |

| EGPn | EGNn | INTPn pin valid edge selection (n = 0 to 7) |
|------|------|---------------------------------------------|
| 0    | 0    | Edge detection disabled                     |
| 0    | 1    | Falling edge                                |
| 1    | 0    | Rising edge                                 |
| 1    | 1    | Both rising and falling edges               |

Table 17-3 shows the ports corresponding to the EGPn and EGNn bits.

**Table 17-3. Ports Corresponding to EGPn and EGNn bits**

| Detection Enable Bit |      | Edge Detection Port | Interrupt Request Signal | 64-pin | 48, 52-pin | 44-pin | 32-pin |
|----------------------|------|---------------------|--------------------------|--------|------------|--------|--------|
| EGP0                 | EGN0 | P137                | INTP0                    | √      | √          | √      | √      |
| EGP1                 | EGN1 | P15                 | INTP1                    | √      | √          | √      | √      |
| EGP2                 | EGN2 | P16                 | INTP2                    | √      | √          | √      | √      |
| EGP3                 | EGN3 | P31                 | INTP3                    | √      | √          | √      | –      |
| EGP4                 | EGN4 | P32                 | INTP4                    | √      | √          | √      | –      |
| EGP5                 | EGN5 | P50                 | INTP5                    | √      | √          | –      | –      |
| EGP6                 | EGN6 | P52                 | INTP6                    | √      | –          | –      | –      |
| EGP7                 | EGN7 | P43                 | INTP7                    | √      | –          | –      | –      |

**Caution** Select the port mode by clearing the EGPn and EGNn bits to 0 because an edge may be detected when the external interrupt function is switched to the port function.

- Remarks**
1. n = 0 to 7
  2. √: Mounted  
–: Not mounted

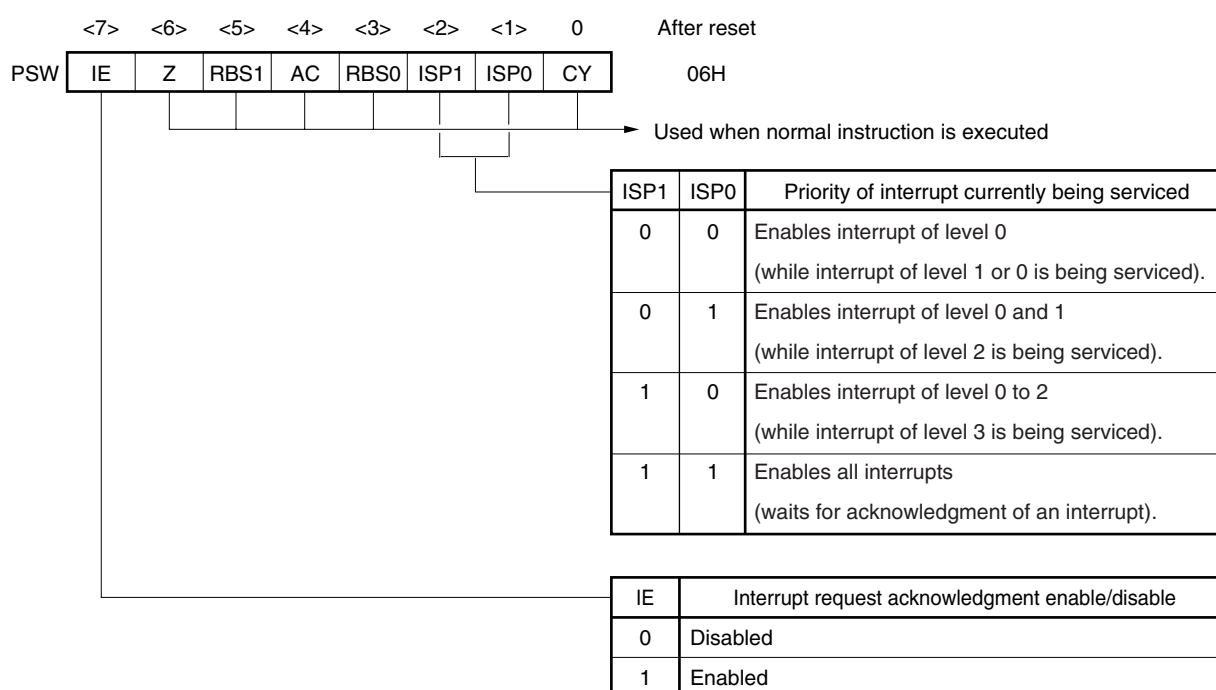
### 17.3.5 Program status word (PSW)

The program status word is a register used to hold the instruction execution result and the current status for an interrupt request. The IE flag that sets maskable interrupt enable/disable and the ISP0 and ISP1 flags that controls multiple interrupt servicing are mapped to the PSW.

Besides 8-bit read/write, this register can carry out operations using bit manipulation instructions and dedicated instructions (EI and DI). When a vectored interrupt request is acknowledged, if the BRK instruction is executed, the contents of the PSW are automatically saved into a stack and the IE flag is reset to 0. If a maskable interrupt request is acknowledged, the contents of the priority specification flag of the acknowledged interrupt are transferred to the ISP0 and ISP1 flags. The PSW contents are also saved into the stack with the PUSH PSW instruction. They are restored from the stack with the RETI, RETB, and POP PSW instructions.

Reset signal generation sets PSW to 06H.

**Figure 17-6. Configuration of Program Status Word**





## 17.4 Interrupt Servicing Operations

### 17.4.1 Maskable interrupt request acknowledgment

A maskable interrupt request becomes acknowledgeable when the interrupt request flag is set to 1 and the mask (MK) flag corresponding to that interrupt request is cleared to 0. A vectored interrupt request is acknowledged if interrupts are in the interrupt enabled state (when the IE flag is set to 1). However, a low-priority interrupt request is not acknowledged during servicing of a higher priority interrupt request.

The times from generation of a maskable interrupt request until vectored interrupt servicing is performed are listed in Table 17-4 below.

For the interrupt request acknowledgment timing, see **Figures 17-8 and 17-9**.

**Table 17-4. Time from Generation of Maskable Interrupt Until Servicing**

|                | Minimum Time | Maximum Time <sup>Note</sup> |
|----------------|--------------|------------------------------|
| Servicing time | 9 clocks     | 16 clocks                    |

**Note** Maximum time does not apply when an instruction from the internal RAM area is executed.

**Remark** 1 clock:  $1/f_{CLK}$  ( $f_{CLK}$ : CPU clock)

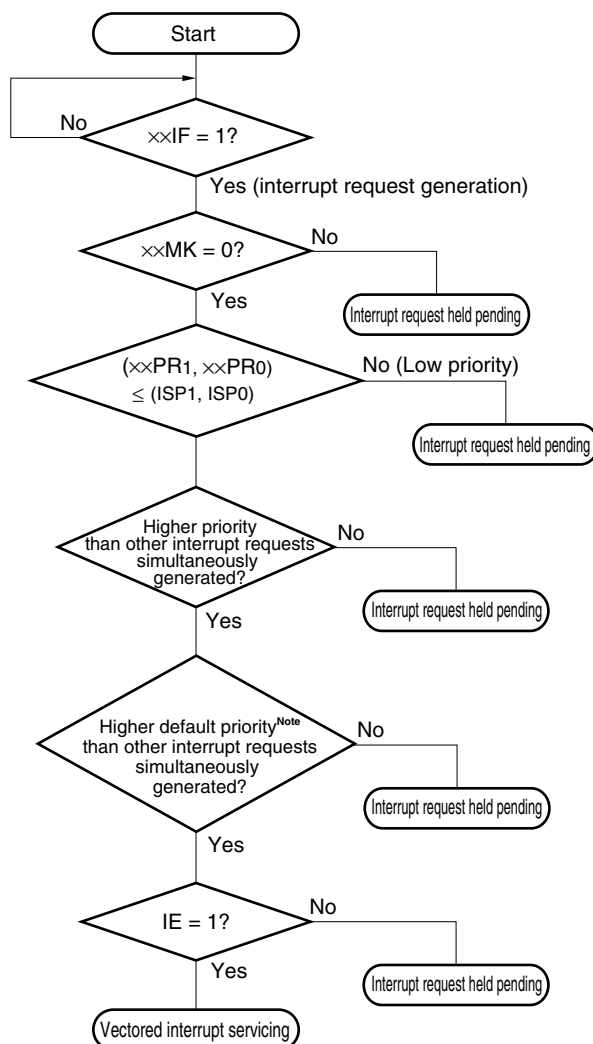
If two or more maskable interrupt requests are generated simultaneously, the request with a higher priority level specified in the priority specification flag is acknowledged first. If two or more interrupts requests have the same priority level, the request with the highest default priority is acknowledged first.

An interrupt request that is held pending is acknowledged when it becomes acknowledgeable.

Figure 17-7 shows the interrupt request acknowledgment algorithm.

If a maskable interrupt request is acknowledged, the contents are saved into the stacks in the order of PSW, then PC, the IE flag is reset (0), and the contents of the priority specification flag corresponding to the acknowledged interrupt are transferred to the ISP1 and ISP0 flags. The vector table data determined for each interrupt request is then loaded into the PC and branched.

Restoring from an interrupt is possible by using the RETI instruction.

**Figure 17-7. Interrupt Request Acknowledgment Processing Algorithm**

xxIF: Interrupt request flag

xxMK: Interrupt mask flag

xxPR0: Priority specification flag 0

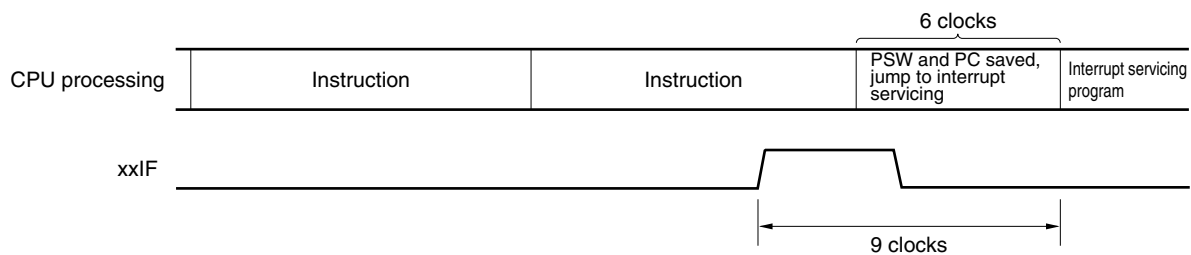
xxPR1: Priority specification flag 1

IE: Flag that controls acknowledgment of maskable interrupt request (1 = Enable, 0 = Disable)

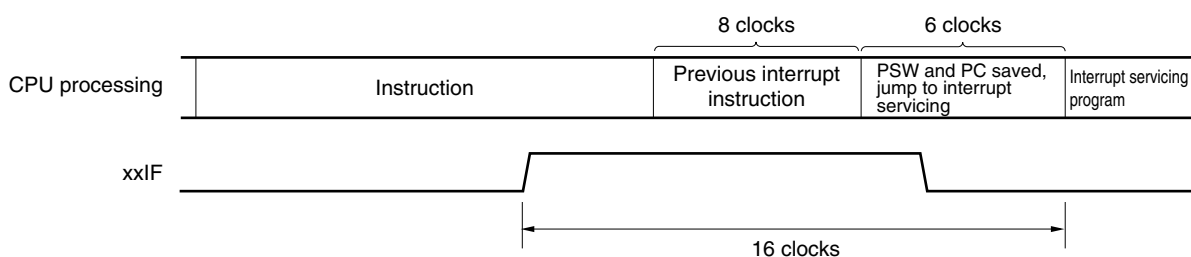
ISP0, ISP1: Flag that indicates the priority level of the interrupt currently being serviced (see **Figure 17-6**)

**Note** For the default priority, refer to **Table 17-1 Interrupt Source List**.

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**Figure 17-8. Interrupt Request Acknowledgment Timing (Minimum Time)****Remark** 1 clock:  $1/f_{CLK}$  ( $f_{CLK}$ : CPU clock)

&lt;R&gt;

**Figure 17-9. Interrupt Request Acknowledgment Timing (Maximum Time)****Remark** 1 clock:  $1/f_{CLK}$  ( $f_{CLK}$ : CPU clock)

### 17.4.2 Software interrupt request acknowledgment

A software interrupt request is acknowledged by BRK instruction execution. Software interrupts cannot be disabled.

If a software interrupt request is acknowledged, the contents are saved into the stacks in the order of the program status word (PSW), then program counter (PC), the IE flag is reset (0), and the contents of the vector table (0007EH, 0007FH) are loaded into the PC and branched.

Restoring from a software interrupt is possible by using the RETB instruction.

**Caution** Can not use the RETI instruction for restoring from the software interrupt.

### 17.4.3 Multiple interrupt servicing

Multiple interrupt servicing occurs when another interrupt request is acknowledged during execution of an interrupt.

Multiple interrupt servicing does not occur unless the interrupt request acknowledgment enabled state is selected (IE = 1). When an interrupt request is acknowledged, interrupt request acknowledgment becomes disabled (IE = 0). Therefore, to enable multiple interrupt servicing, it is necessary to set (1) the IE flag with the EI instruction during interrupt servicing to enable interrupt acknowledgment.

Moreover, even if interrupts are enabled, multiple interrupt servicing may not be enabled, this being subject to interrupt priority control. Two types of priority control are available: default priority control and programmable priority control. Programmable priority control is used for multiple interrupt servicing.

In the interrupt enabled state, if an interrupt request with a priority equal to or higher than that of the interrupt currently being serviced is generated, it is acknowledged for multiple interrupt servicing. If an interrupt with a priority lower than that of the interrupt currently being serviced is generated during interrupt servicing, it is not acknowledged for multiple interrupt servicing. Interrupt requests that are not enabled because interrupts are in the interrupt disabled state or because they have a lower priority are held pending. When servicing of the current interrupt ends, the pending interrupt request is acknowledged following execution of at least one main processing instruction execution.

Table 17-5 shows relationship between interrupt requests enabled for multiple interrupt servicing and Figure 17-10 shows multiple interrupt servicing examples.

**Table 17-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing**

| Multiple Interrupt Request<br><br>Interrupt Being Serviced |                      | Maskable Interrupt Request    |        |                               |        |                               |        |                               |        | Software Interrupt Request |
|------------------------------------------------------------|----------------------|-------------------------------|--------|-------------------------------|--------|-------------------------------|--------|-------------------------------|--------|----------------------------|
|                                                            |                      | Priority Level 0<br>(PR = 00) |        | Priority Level 1<br>(PR = 01) |        | Priority Level 2<br>(PR = 10) |        | Priority Level 3<br>(PR = 11) |        |                            |
|                                                            |                      | IE = 1                        | IE = 0 | IE = 1                        | IE = 0 | IE = 1                        | IE = 0 | IE = 1                        | IE = 0 |                            |
| Maskable interrupt                                         | ISP1 = 0<br>ISP0 = 0 | ○                             | ×      | ×                             | ×      | ×                             | ×      | ×                             | ×      | ○                          |
|                                                            | ISP1 = 0<br>ISP0 = 1 | ○                             | ×      | ○                             | ×      | ×                             | ×      | ×                             | ×      | ○                          |
|                                                            | ISP1 = 1<br>ISP0 = 0 | ○                             | ×      | ○                             | ×      | ○                             | ×      | ×                             | ×      | ○                          |
| Software interrupt                                         |                      | ○                             | ×      | ○                             | ×      | ○                             | ×      | ○                             | ×      | ○                          |

**Remarks 1.** ○: Multiple interrupt servicing enabled

**2.** ×: Multiple interrupt servicing disabled

**3.** ISP0, ISP1, and IE are flags contained in the PSW.

ISP1 = 0, ISP0 = 0: An interrupt of level 1 or level 0 is being serviced.

ISP1 = 0, ISP0 = 1: An interrupt of level 2 is being serviced.

ISP1 = 1, ISP0 = 0: An interrupt of level 3 is being serviced.

ISP1 = 1, ISP0 = 1: Wait for An interrupt acknowledgment.

IE = 0: Interrupt request acknowledgment is disabled.

IE = 1: Interrupt request acknowledgment is enabled.

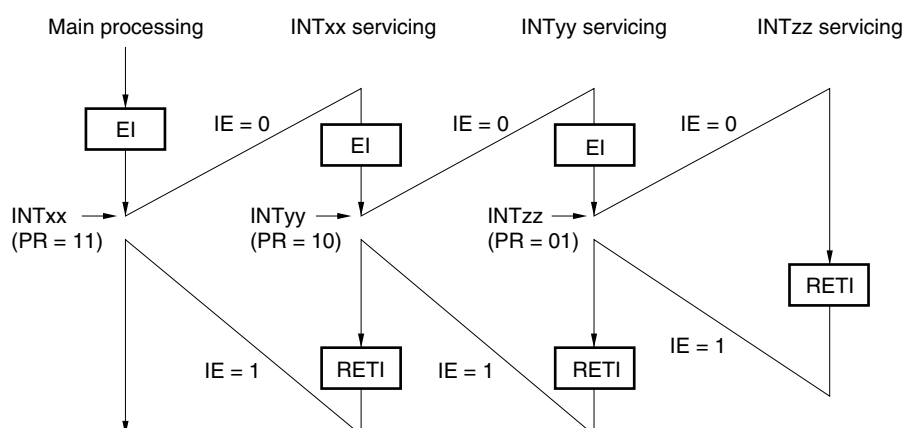
**4.** PR is a flag contained in the PR00L, PR00H, PR01L, PR01H, PR02L, PR10L, PR10H, PR11L, PR11H, and PR12L registers.

PR = 00: Specify level 0 with  $\times\times PR1\times = 0$ ,  $\times\times PR0\times = 0$  (higher priority level)

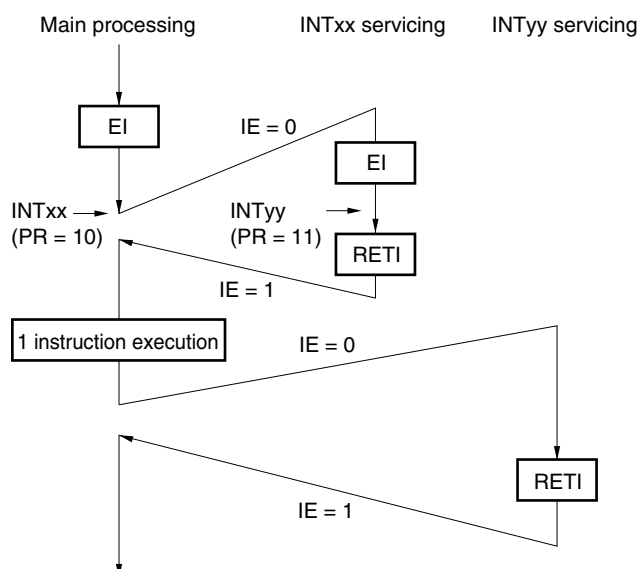
PR = 01: Specify level 1 with  $\times\times PR1\times = 0$ ,  $\times\times PR0\times = 1$

PR = 10: Specify level 2 with  $\times\times PR1\times = 1$ ,  $\times\times PR0\times = 0$

PR = 11: Specify level 3 with  $\times\times PR1\times = 1$ ,  $\times\times PR0\times = 1$  (lower priority level)

**Figure 17-10. Examples of Multiple Interrupt Servicing (1/2)****Example 1. Multiple interrupt servicing occurs twice**

During servicing of interrupt INTxx, two interrupt requests, INTyy and INTzz, are acknowledged, and multiple interrupt servicing takes place. Before each interrupt request is acknowledged, the EI instruction must always be issued to enable interrupt request acknowledgment.

**Example 2. Multiple interrupt servicing does not occur due to priority control**

Interrupt request INTyy issued during servicing of interrupt INTxx is not acknowledged because its priority is lower than that of INTxx, and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 00: Specify level 0 with  $\times\times PR1\times = 0$ ,  $\times\times PR0\times = 0$  (higher priority level)

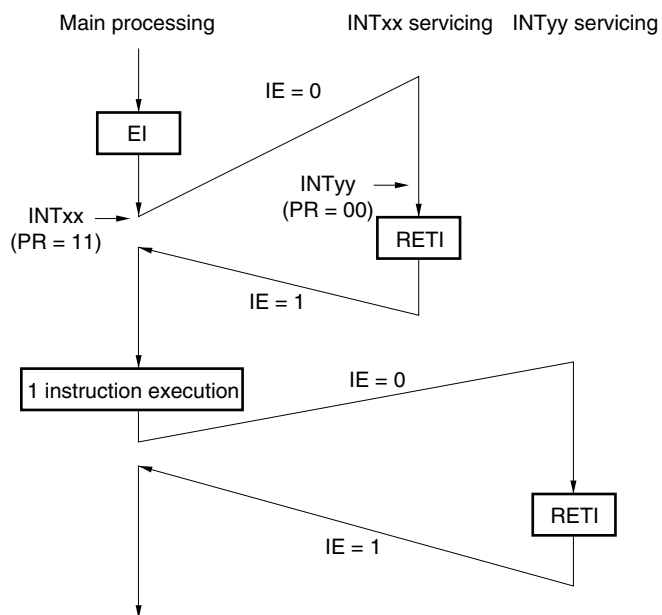
PR = 01: Specify level 1 with  $\times\times PR1\times = 0$ ,  $\times\times PR0\times = 1$

PR = 10: Specify level 2 with  $\times\times PR1\times = 1$ ,  $\times\times PR0\times = 0$

PR = 11: Specify level 3 with  $\times\times PR1\times = 1$ ,  $\times\times PR0\times = 1$  (lower priority level)

IE = 0: Interrupt request acknowledgment is disabled

IE = 1: Interrupt request acknowledgment is enabled.

**Figure 17-10. Examples of Multiple Interrupt Servicing (2/2)****Example 3. Multiple interrupt servicing does not occur because interrupts are not enabled**

Interrupts are not enabled during servicing of interrupt INTxx (EI instruction is not issued), therefore, interrupt request INTyy is not acknowledged and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 00: Specify level 0 with  $\times\times PR1\times = 0$ ,  $\times\times PR0\times = 0$  (higher priority level)

PR = 01: Specify level 1 with  $\times\times PR1\times = 0$ ,  $\times\times PR0\times = 1$

PR = 10: Specify level 2 with  $\times\times PR1\times = 1$ ,  $\times\times PR0\times = 0$

PR = 11: Specify level 3 with  $\times\times PR1\times = 1$ ,  $\times\times PR0\times = 1$  (lower priority level)

IE = 0: Interrupt request acknowledgment is disabled

IE = 1: Interrupt request acknowledgment is enabled.

#### 17.4.4 Interrupt request hold

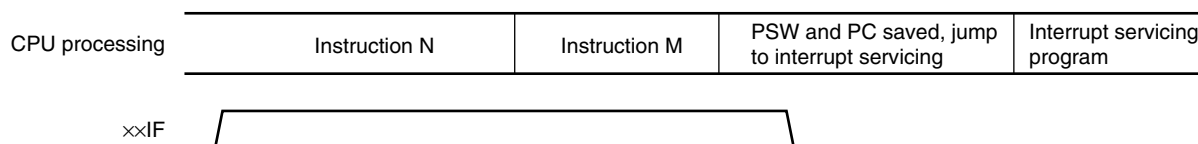
There are instructions where, even if an interrupt request is issued while the instructions are being executed, interrupt request acknowledgment is held pending until the end of execution of the next instruction. These instructions (interrupt request hold instructions) are listed below.

- MOV PSW, #byte
- MOV PSW, A
- MOV1 PSW. bit, CY
- SET1 PSW. bit
- CLR1 PSW. bit
- RETB
- RETI
- POP PSW
- BTCLR PSW. bit, \$addr20
- EI
- DI
- SKC
- SKNC
- SKZ
- SKNZ
- SKH
- SKNH
- Manipulation instructions for the IF0L, IF0H, IF1L, IF1H, IF2L, MK0L, MK0H, MK1L, MK1H, MK2L, PR00L, PR00H, PR01L, PR01H, PR02L, PR10L, PR10H, PR11L, PR11H, and PR12L registers

<R>

Figure 17-11 shows the timing at which interrupt requests are held pending.

**Figure 17-11. Interrupt Request Hold**



- Remarks**
1. Instruction N: Interrupt request hold instruction
  2. Instruction M: Instruction other than interrupt request hold instruction



&lt;R&gt;

**CHAPTER 18 KEY INTERRUPT FUNCTION****18.1 Functions of Key Interrupt**

A key interrupt (INTKR) can be generated by inputting a rising edge/falling edge to the key interrupt input pins (KR0 to KR3).

**Table 18-1. Assignment of Key Interrupt Detection Pins**

| Flag  | Description                         |
|-------|-------------------------------------|
| KRM00 | Controls KR0 signal in 1-bit units. |
| KRM01 | Controls KR1 signal in 1-bit units. |
| KRM02 | Controls KR2 signal in 1-bit units. |
| KRM03 | Controls KR3 signal in 1-bit units. |

## 18.2 Configuration of Key Interrupt

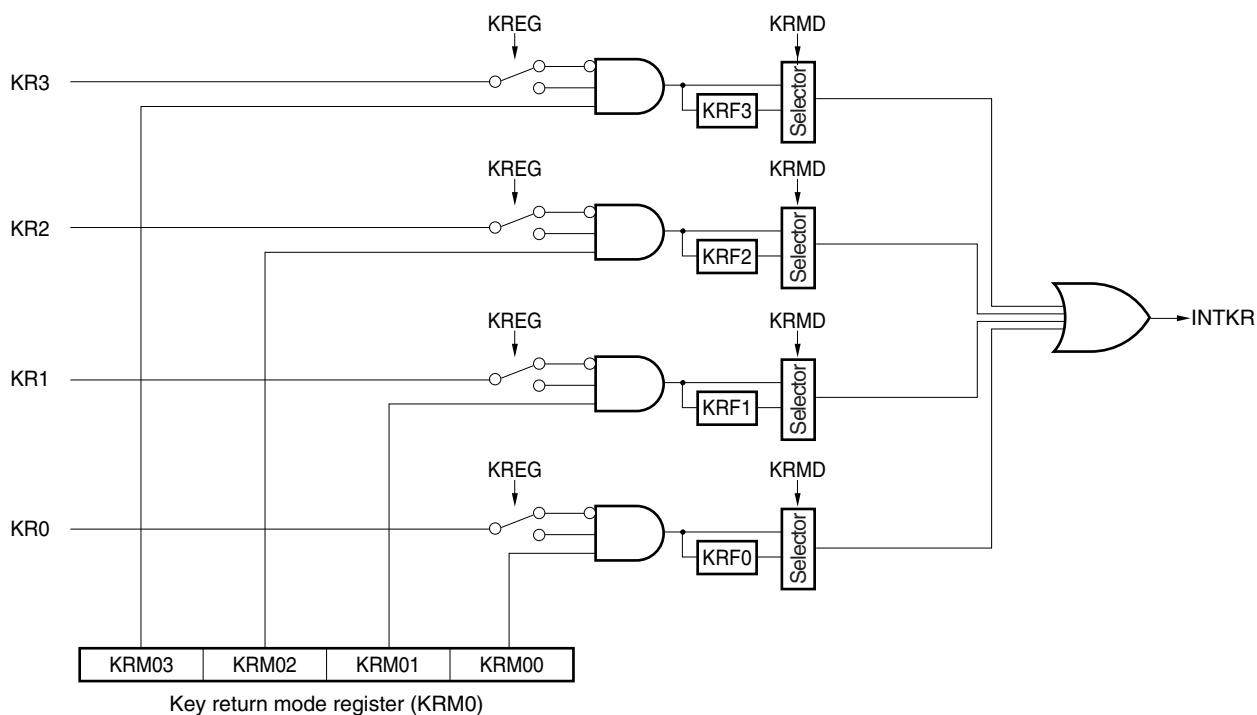
The key interrupt includes the following hardware.

**Table 18-2. Configuration of Key Interrupt**

| Item             | Configuration                                                         |
|------------------|-----------------------------------------------------------------------|
| Control register | Key return control register (KRCTL)                                   |
|                  | Key return mode register 0 (KRM0)                                     |
|                  | Key return flag register (KRF)                                        |
|                  | Port mode registers 1, 3, 7, 14 (PM1, PM3, PM7, PM14) <sup>Note</sup> |

**Note** The port mode registers (PMxx) to be set differ depending on the product. For details, see 18.3.4 Port mode registers 1, 3, 7, 14 (PM1, PM3, PM7, PM14).

**Figure 18-1. Block Diagram of Key Interrupt**



### 18.3 Register Controlling Key Interrupt

The key interrupt function is controlled by the following five registers:

- Key return control register (KRCTL)
- Key return mode register 0 (KRM0)
- Key return flag register (KRF)
- Port mode registers 1, 3, 7, and 14 (PM1, PM3, PM7, PM14)<sup>Note</sup>

**Note** The port mode registers (PMxx) to be set differ depending on the product. For details, see **18.3.4 Port mode registers 1, 3, 7, 14 (PM1, PM3, PM7, PM14)**.

#### 18.3.1 Key return control register (KRCTL)

This register controls the usage of the key interrupt flags (KRF0 to KRF3) and sets the detection edge.

The KRCTL register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 18-2. Format of Key Return Control Register (KRCTL)**

Address: FFF34H After reset: 00H R/W

| Symbol | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0    |
|--------|------|---|---|---|---|---|---|------|
| KRCTL  | KRMD | 0 | 0 | 0 | 0 | 0 | 0 | KREG |

| KRMD | Usage of t key interrupt flags (KRF0 to KRF3) |
|------|-----------------------------------------------|
| 0    | Does not use key interrupt flags              |
| 1    | Uses key interrupt flags                      |

| KRMD | Selection of Detection Edge (KR0 to KR3) |
|------|------------------------------------------|
| 0    | Falling edge                             |
| 1    | Rising edge                              |

### 18.3.2 Key return mode register 0 (KRM0)

This register sets the key interrupt mode.

The KRM0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

**Figure 18-3. Format of Key Return Mode Register 0 (KRM0)**

Address: FFF37H After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3     | 2     | 1     | 0     |
|--------|---|---|---|---|-------|-------|-------|-------|
| KRM0   | 0 | 0 | 0 | 0 | KRM03 | KRM02 | KRM01 | KRM00 |

| KRM0n | Key interrupt mode control           |
|-------|--------------------------------------|
| 0     | Does not detect key interrupt signal |
| 1     | Detects key interrupt signal         |

- Cautions**
1. The internal pull-up resistor can be used by setting the corresponding bits to 1 in the pull-up resistor registers 1, 3, 7, and 14 (PU1, PU3, PU7, PU14) of key interrupt input pins.
  2. An interrupt will be generated if the target bit of the KRM0 register is set while a low level (when KREG = 0)/high level (when KREG = 1) is being input to the key interrupt input pin. To ignore this interrupt, set the KRM0 register after disabling interrupt servicing by using the interrupt mask flag. Afterward, clear the interrupt request flag and enable interrupt servicing after waiting for the key interrupt input high-level width/low-level width (see 30.4 AC Characteristics).
  3. The pins not used in the key interrupt mode can be used as normal ports.

**Remark** n = 0 to 3

### 18.3.3 Key return flag register (KRF)

This register controls the key interrupt flags (KRF0 to KRF3).

The KRF register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 18-4. Format of Key return Flag Register (KRF)**

Address: FFF35H After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3    | 2    | 1    | 0    |
|--------|---|---|---|---|------|------|------|------|
| KRF    | 0 | 0 | 0 | 0 | KRF3 | KRF2 | KRF1 | KRF0 |

| KRFn | Key interrupt flag (n = 0 to 3)            |
|------|--------------------------------------------|
| 0    | No key interrupt signal has been detected. |
| 1    | A key interrupt signal has been detected.  |

**Caution** When KRMD = 0, setting the KRFn bit to 1 is prohibited.

### 18.3.4 Port mode registers 1, 3, 7, 14 (PM1, PM3, PM7, PM14)

These registers set the input and output of port 1, 3, 7, 14 in 1-bit units.

The presence or absence of key input pins depends on the product. When using the key interrupt function, set the following port mode registers according to the product used.

32, 44-pin products: PM1, PM14

48, 52-pin products: PM3, PM7

64-pin products: PM7

When using P10/KR2 to P12/KR0, P140/KR3, P30/KR3 to P32/KR1, or P70/KR0 to P73/KR3 as a key input pin, set the bit of the port mode registers (PM1, PM3, PM7, PM14) corresponding to the port pin to 1.

The PM1, PM3, PM7, and PM14 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to FFH.

**Figure 18-5. Format of Port Mode Register 7 (PM7) (64-pin products)**

Address: FFF27H After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4    | 3    | 2    | 1    | 0    |
|--------|---|---|---|------|------|------|------|------|
| PM7    | 1 | 1 | 1 | PM74 | PM73 | PM72 | PM71 | PM70 |

|      |                                             |
|------|---------------------------------------------|
| PM7n | I/O mode selection for P7n pin (n = 0 to 4) |
| 0    | Output mode (output buffer on)              |
| 1    | Input mode (output buffer off)              |

**Remark** The figure shown above presents the format of port mode register 7 of the 64-pin products. The format of the port mode register of other products, see **Table 4-2. PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits mounted on each product.**

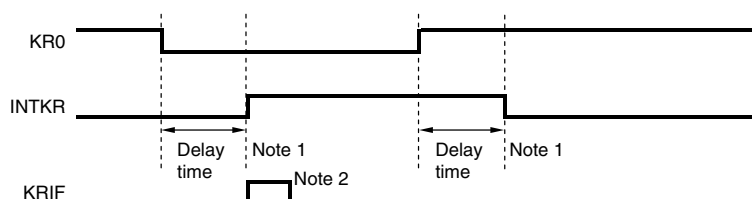
## 18.4 Key Interrupt Operation

### 18.4.1 When not using the key interrupt flag (KRMD = 0)

A key interrupt (INTKR) is generated when the valid edge specified by the setting of the KREG bit is input to a key interrupt pin (KR0 to KR3). The channel to which the valid edge was input can be identified by reading the port register and checking the port level after the key interrupt (INTKR) is generated.

The INTKR signal changes according to the input level of the key interrupt input pin (KR0 to KR3).

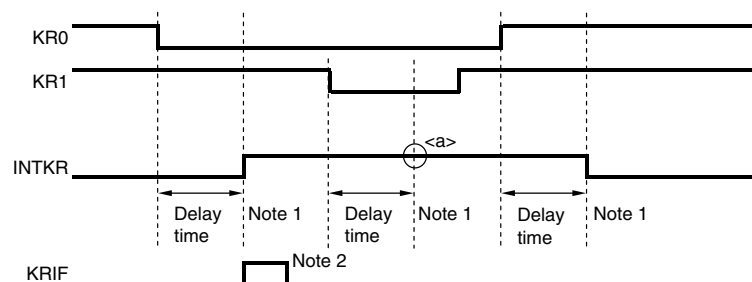
**Figure 18-6. Operation of INTKR Signal When a Key Interrupt is Input to a Single Channel**  
(When KRMD = 0 and KREG = 0)



- Notes 1.** The maximum delay time is the maximum value of the high-level width and low-level width of the key interrupt input (see **30.4 AC Characteristics** for details).
- 2.** Acknowledgment of vectored interrupt request or bit cleared by software

The operation when a valid edge is input to multiple key interrupt input pins is shown in Figure 18-7 below. The INTKR signal is set while a low level is being input to one pin (when KREG is set to 0). Therefore, even if a falling edge is input to another pin in this period, a key interrupt (INTKR) will not be generated again (<1> in the figure).

**Figure 18-7. Operation of INTKR Signal When Key Interrupts Are Input to Multiple Channels**  
(When KRMD = 0 and KREG = 0)



- Notes 1.** The maximum delay time is the maximum value of the high-level width and low-level width of the key interrupt input (see **30.4 AC Characteristics** for details).
- 2.** Acknowledgment of vectored interrupt request or bit cleared by software

### 18.4.2 When using the key interrupt flag (KRMD = 1)

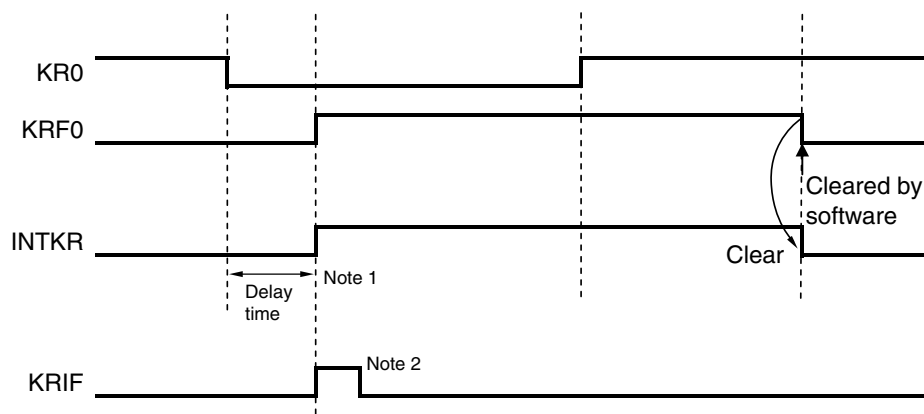
A key interrupt (INTKR) is generated when the valid edge specified by the setting of the KREG bit is input to a key interrupt pin (KR0 to KR3). The channels to which the valid edge was input can be identified by reading the key return flag register (KRF) after the key interrupt (INTKR) is generated.

If the KRMD bit is set to 1, the INTKR signal is cleared by clearing the corresponding bit in the KRF register.

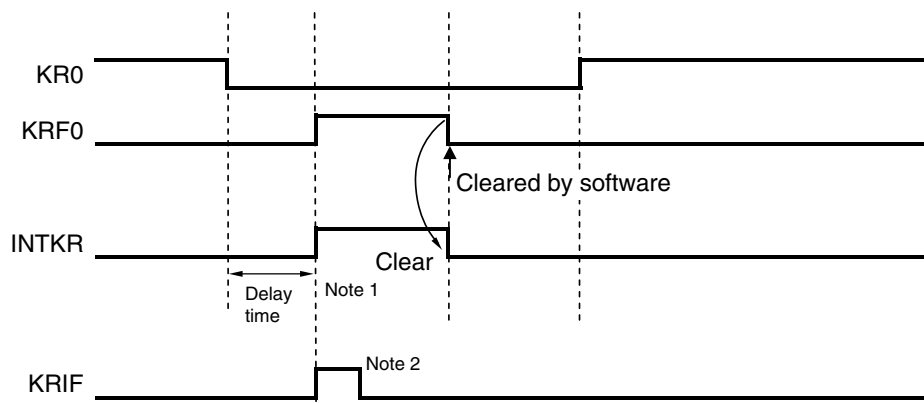
As shown in Figure 18-8, only one interrupt is generated each time a falling edge is input to one channel (when KREG = 0), regardless of whether the KRFn bit is cleared before or after a rising edge is input.

**Figure 18-8. Basic Operation of the INTKR Signal When the Key Interrupt Flag Is Used  
(When KRMD = 1 and KREG = 0)**

(a) When KRF0 is cleared after a rising edge is input to the KR0 pin



(b) When KRF0 is cleared before a rising edge is input to the KR0 pin

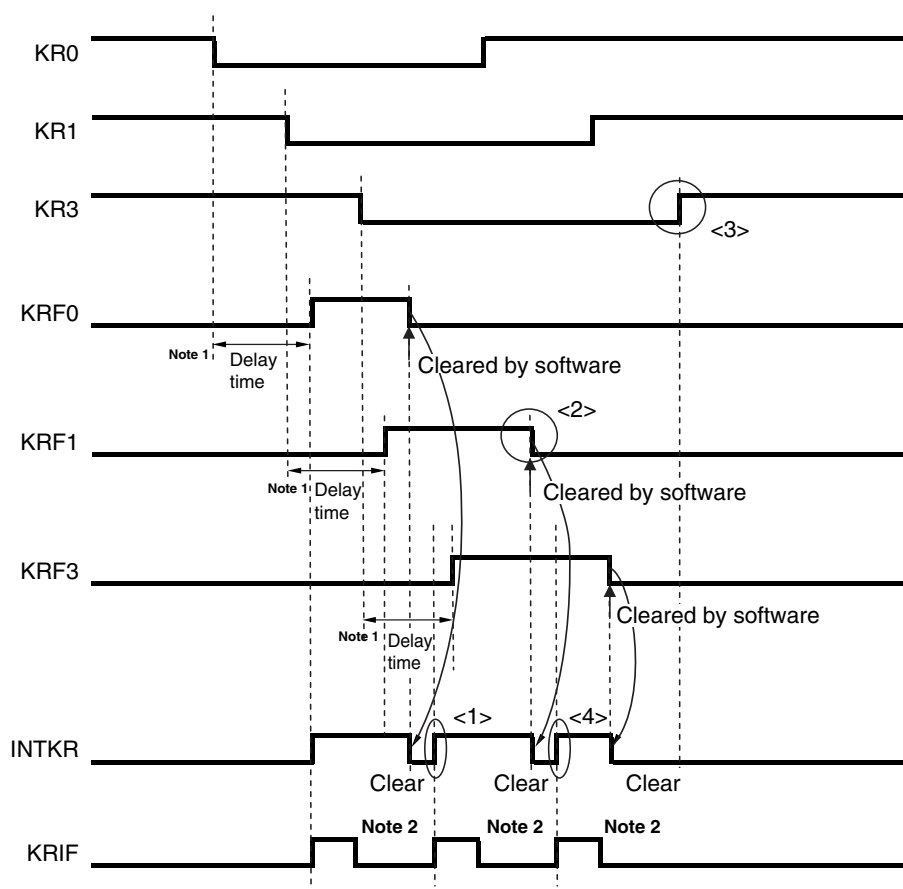


**Notes 1.** The maximum delay time is the maximum value of the high-level width and low-level width of the key interrupt input (see **30.4 AC Characteristics** for details).

**2.** Acknowledgment of vectored interrupt request or bit cleared by software

The operation when a valid edge is input to multiple key interrupt input pins is shown in Figure 18-9 below. A falling edge is also input to the KR1 and KR3 pins after a falling edge was input to the KR0 pin (when KREG = 0). The KRF1 bit is set when the KRF0 bit is cleared. A key interrupt (INTKR) is therefore generated one clock ( $f_{CLK}$ ) after the KRF0 bit is cleared (<1> in the figure). Also, after a falling edge has been input to the KR3 pin, a low level continues to be input to this pin (<3> in the figure) until the KRF1 bit is cleared (<2> in the figure). A key interrupt (INTKR) is therefore generated one clock ( $f_{CLK}$ ) after the KRF1 bit is cleared (<4> in the figure). It is thus possible to generate a key interrupt (INTKR) when a valid edge is input to multiple channels.

**Figure 18-9. Operation of INTKR Signal When Key Interrupts Are Input to Multiple Channels**  
(When KRMD = 1 and KREG = 0)



- Notes 1.** The maximum delay time is the maximum value of the high-level width and low-level width of the key interrupt input (see **30.4 AC Characteristics** for details).
- 2.** Acknowledgment of vectored interrupt request or bit cleared by software

**Remark**  $f_{CLK}$ : CPU/peripheral hardware clock frequency



## CHAPTER 19 STANDBY FUNCTION

### 19.1 Standby Function and Configuration

#### 19.1.1 Standby function

The standby function reduces the operating current of the system, and the following three modes are available.

##### (1) HALT mode

HALT instruction execution sets the HALT mode. In the HALT mode, the CPU operation clock is stopped. If the high-speed system clock oscillator, high-speed on-chip oscillator, or subsystem clock oscillator is operating before the HALT mode is set, oscillation of each clock continues. In this mode, the operating current is not decreased as much as in the STOP mode, but the HALT mode is effective for restarting operation immediately upon interrupt request generation and carrying out intermittent operations frequently.

##### (2) STOP mode

STOP instruction execution sets the STOP mode. In the STOP mode, the high-speed system clock oscillator and high-speed on-chip oscillator stop, stopping the whole system, thereby considerably reducing the CPU operating current.

Because this mode can be cleared by an interrupt request, it enables intermittent operations to be carried out. However, because a wait time is required to secure the oscillation stabilization time after the STOP mode is released when the X1 clock is selected, select the HALT mode if it is necessary to start processing immediately upon interrupt request generation.

##### (3) SNOOZE mode

In the case of CSI00 or UART0 data reception and an A/D conversion request by the timer trigger signal (the interrupt request signal (INTRTC/INTIT)), the STOP mode is exited, the CSI00 or UART0 data is received without operating the CPU, and A/D conversion is performed. This can only be specified when the high-speed on-chip oscillator is selected for the CPU/peripheral hardware clock ( $f_{CLK}$ ).

In either of these two modes, all the contents of registers, flags and data memory just before the standby mode is set are held. The I/O port output latches and output buffer statuses are also held.

- <R> **Cautions**
1. The STOP mode can be used only when the CPU is operating on the main system clock. Do not set to the STOP mode while the CPU operates with the subsystem clock. The HALT mode can be used when the CPU is operating on either the main system clock or the subsystem clock.
  2. When shifting to the STOP mode, be sure to stop the peripheral hardware operation operating with main system clock before executing STOP instruction (except SNOOZE mode setting unit).
  3. When using CSI00, UART0, or the A/D converter in the SNOOZE mode, set up serial standby control register 0 (SSC0) and A/D converter mode register 2 (ADM2) before switching to the STOP mode. For details, see 12.3 Registers Controlling Serial Array Unit and 11.3 Registers Used in A/D Converter.

4. The following sequence is recommended for power consumption reduction of the A/D converter when the standby function is used: First clear bit 7 (ADCS) and bit 0 (ADCE) of A/D converter mode register 0 (ADM0) to 0 to stop the A/D conversion operation, and then execute the STOP instruction.
5. It can be selected by the option byte whether the low-speed on-chip oscillator continues oscillating or stops in the HALT or STOP mode. For details, see CHAPTER 25 OPTION BYTE.

## 19.2 Registers controlling standby function

The standby function is controlled by the following two registers.

- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)

**Remark** For the registers that start, stop, or select the clock, see **CHAPTER 5 CLOCK GENERATOR**.

### 19.2.1 Oscillation stabilization time counter status register (OSTC)

This is the register that indicates the count status of the X1 clock oscillation stabilization time counter.

The X1 clock oscillation stabilization time can be checked in the following case.

- If the X1 clock starts oscillation while the high-speed on-chip oscillator clock or subsystem clock is being used as the CPU clock.
- If the STOP mode is entered and then released while the high-speed on-chip oscillator clock is being used as the CPU clock with the X1 clock oscillating.

The OSTC register can be read by a 1-bit or 8-bit memory manipulation instruction.

When reset is released (reset by RESET input, POR, LVD, WDT, and executing an illegal instruction), the STOP instruction and MSTOP bit (bit 7 of clock operation status control register (CSC)) = 1 clear this register to 00H.

**Figure 19-1. Format of Oscillation Stabilization Time Counter Status Register (OSTC)**

Address: FFFA2H After reset: 00H R

| Symbol | 7      | 6      | 5       | 4       | 3       | 2       | 1       | 0       |
|--------|--------|--------|---------|---------|---------|---------|---------|---------|
| OSTC   | MOST 8 | MOST 9 | MOST 10 | MOST 11 | MOST 13 | MOST 15 | MOST 17 | MOST 18 |

| MOST 8 | MOST 9 | MOST 10 | MOST 11 | MOST 13 | MOST 15 | MOST 17 | MOST 18 | Oscillation stabilization time status |                          |                          |
|--------|--------|---------|---------|---------|---------|---------|---------|---------------------------------------|--------------------------|--------------------------|
|        |        |         |         |         |         |         |         |                                       | $f_x = 10 \text{ MHz}$   | $f_x = 20 \text{ MHz}$   |
| 0      | 0      | 0       | 0       | 0       | 0       | 0       | 0       | $2^8/f_x \text{ max.}$                | 25.6 $\mu\text{s}$ max.  | 12.8 $\mu\text{s}$ max.  |
| 1      | 0      | 0       | 0       | 0       | 0       | 0       | 0       | $2^9/f_x \text{ min.}$                | 25.6 $\mu\text{s}$ min.  | 12.8 $\mu\text{s}$ min.  |
| 1      | 1      | 0       | 0       | 0       | 0       | 0       | 0       | $2^9/f_x \text{ min.}$                | 51.2 $\mu\text{s}$ min.  | 25.6 $\mu\text{s}$ min.  |
| 1      | 1      | 1       | 0       | 0       | 0       | 0       | 0       | $2^{10}/f_x \text{ min.}$             | 102.4 $\mu\text{s}$ min. | 51.2 $\mu\text{s}$ min.  |
| 1      | 1      | 1       | 1       | 0       | 0       | 0       | 0       | $2^{11}/f_x \text{ min.}$             | 204.8 $\mu\text{s}$ min. | 102.4 $\mu\text{s}$ min. |
| 1      | 1      | 1       | 1       | 1       | 0       | 0       | 0       | $2^{13}/f_x \text{ min.}$             | 819.2 $\mu\text{s}$ min. | 409.6 $\mu\text{s}$ min. |
| 1      | 1      | 1       | 1       | 1       | 1       | 0       | 0       | $2^{15}/f_x \text{ min.}$             | 3.27 ms min.             | 1.64 ms min.             |
| 1      | 1      | 1       | 1       | 1       | 1       | 1       | 0       | $2^{17}/f_x \text{ min.}$             | 13.11 ms min.            | 6.55 ms min.             |
| 1      | 1      | 1       | 1       | 1       | 1       | 1       | 1       | $2^{18}/f_x \text{ min.}$             | 26.21 ms min.            | 13.11 ms min.            |

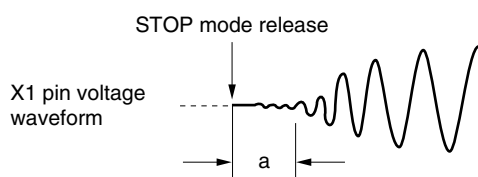
**Cautions** 1. After the above time has elapsed, the bits are set to 1 in order from the MOST8 bit and remain 1.

2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by the oscillation stabilization time select register (OSTS). If the STOP mode is entered and then released while the high-speed on-chip oscillator clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- Desired OSTC register oscillation stabilization time  $\leq$  Oscillation stabilization time set by OSTS register

**Note**, therefore, that only the status up to the oscillation stabilization time set by the OSTS register is set to the OSTC register after STOP mode is released.

3. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



**Remark**  $f_x$ : X1 clock oscillation frequency

### 19.2.2 Oscillation stabilization time select register (OSTS)

This register is used to select the X1 clock oscillation stabilization wait time when the STOP mode is released.

When the X1 clock is selected as the CPU clock, the operation waits for the time set using the OSTS register after the STOP mode is released.

When the high-speed on-chip oscillator clock is selected as the CPU clock, confirm with the oscillation stabilization time counter status register (OSTC) that the desired oscillation stabilization time has elapsed after the STOP mode is released. The oscillation stabilization time can be checked up to the time set using the OSTC register.

The OSTS register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 07H.

**Figure 19-2. Format of Oscillation Stabilization Time Select Register (OSTS)**

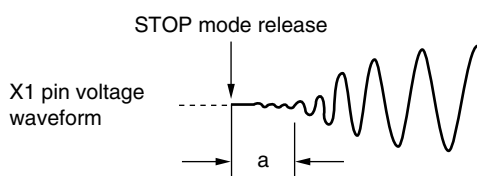
Address: FFFA3H After reset: 07H R/W

|        |   |   |   |   |   |       |       |       |
|--------|---|---|---|---|---|-------|-------|-------|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2     | 1     | 0     |
| OSTS   | 0 | 0 | 0 | 0 | 0 | OSTS2 | OSTS1 | OSTS0 |

| OSTS2 | OSTS1 | OSTS0 |              | Oscillation stabilization time selection |                        |
|-------|-------|-------|--------------|------------------------------------------|------------------------|
|       |       |       |              | $f_x = 10 \text{ MHz}$                   | $f_x = 20 \text{ MHz}$ |
| 0     | 0     | 0     | $2^8/f_x$    | 25.6 $\mu\text{s}$                       | 12.8 $\mu\text{s}$     |
| 0     | 0     | 1     | $2^9/f_x$    | 51.2 $\mu\text{s}$                       | 25.6 $\mu\text{s}$     |
| 0     | 1     | 0     | $2^{10}/f_x$ | 102.4 $\mu\text{s}$                      | 51.2 $\mu\text{s}$     |
| 0     | 1     | 1     | $2^{11}/f_x$ | 204.8 $\mu\text{s}$                      | 102.4 $\mu\text{s}$    |
| 1     | 0     | 0     | $2^{13}/f_x$ | 819.2 $\mu\text{s}$                      | 409.6 $\mu\text{s}$    |
| 1     | 0     | 1     | $2^{15}/f_x$ | 3.27 ms                                  | 1.64 ms                |
| 1     | 1     | 0     | $2^{17}/f_x$ | 13.11 ms                                 | 6.55 ms                |
| 1     | 1     | 1     | $2^{18}/f_x$ | 26.21 ms                                 | 13.11 ms               |

- Cautions**
1. To set the STOP mode when the X1 clock is used as the CPU clock, set the OSTS register before executing the STOP instruction.
  2. Before changing the setting of the OSTS register, confirm that the count operation of the OSTC register is completed.
  3. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.
  4. The oscillation stabilization time counter counts up to the oscillation stabilization time set by the OSTS register. If the STOP mode is entered and then released while the high-speed on-chip oscillator clock is being used as the CPU clock, set the oscillation stabilization time as follows.
    - Desired OSTC register oscillation stabilization time  $\leq$  Oscillation stabilization time set by OSTS register

Note, therefore, that only the status up to the oscillation stabilization time set by the OSTS register is set to the OSTC register after STOP mode is released.
  5. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



**Remark**  $f_x$ : X1 clock oscillation frequency

## 19.3 Standby Function Operation

### 19.3.1 HALT mode

#### (1) HALT mode

The HALT mode is set by executing the HALT instruction. HALT mode can be set regardless of whether the CPU clock before the setting was the high-speed system clock, high-speed on-chip oscillator clock, or subsystem clock.

The operating statuses in the HALT mode are shown below.

Table 19-1. Operating Statuses in HALT Mode (1/2)

| HALT Mode Setting<br><br>Item               |                     | When HALT Instruction Is Executed While CPU Is Operating on Main System Clock                                                                                                                                                                                                                                          |                                                     |                                                                        |
|---------------------------------------------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------|------------------------------------------------------------------------|
|                                             |                     | When CPU Is Operating on High-Speed On-Chip Oscillator Clock (f <sub>IH</sub> )                                                                                                                                                                                                                                        | When CPU Is Operating on X1 Clock (f <sub>X</sub> ) | When CPU Is Operating on External Main System Clock (f <sub>EX</sub> ) |
| System clock                                |                     | Clock supply to the CPU is stopped                                                                                                                                                                                                                                                                                     |                                                     |                                                                        |
| Main system clock                           | f <sub>IH</sub>     | Operation continues (cannot be stopped)                                                                                                                                                                                                                                                                                | Operation disabled                                  |                                                                        |
|                                             | f <sub>X</sub>      | Operation disabled                                                                                                                                                                                                                                                                                                     | Operation continues (cannot be stopped)             | Cannot operate                                                         |
|                                             | f <sub>EX</sub>     |                                                                                                                                                                                                                                                                                                                        | Cannot operate                                      | Operation continues (cannot be stopped)                                |
| Subsystem clock                             | f <sub>XT</sub>     | Status before HALT mode was set is retained                                                                                                                                                                                                                                                                            |                                                     |                                                                        |
|                                             | f <sub>EXS</sub>    |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |
| f <sub>IL</sub>                             |                     | Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC)<br>• WUTMMCK0 = 1: Oscillates<br>• WUTMMCK0 = 0 and WDTON = 0: Stops<br>• WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates<br>• WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops |                                                     |                                                                        |
| CPU                                         |                     | Operation stopped                                                                                                                                                                                                                                                                                                      |                                                     |                                                                        |
| Code flash memory                           |                     |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |
| Data flash memory                           |                     |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |
| RAM                                         |                     |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |
| Port (latch)                                |                     | Status before HALT mode was set is retained                                                                                                                                                                                                                                                                            |                                                     |                                                                        |
| Timer array unit                            |                     | Operable                                                                                                                                                                                                                                                                                                               |                                                     |                                                                        |
| Real-time clock (RTC)                       |                     |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |
| 12-bit interval timer                       |                     |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |
| Watchdog timer                              |                     |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |
| Clock output/buzzer output                  |                     | Operable                                                                                                                                                                                                                                                                                                               |                                                     |                                                                        |
| A/D converter                               |                     |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |
| Serial array unit (SAU)                     |                     |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |
| Serial interface (IICA)                     |                     |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |
| LCD driver/controller                       |                     | Operable (However, this depends on the status of the clock selected as the LCD source clock: operation is possible if the selected clock is operating, but operation will stop if the selected clock is stopped.)                                                                                                      |                                                     |                                                                        |
| Multiplier and divider/multiply-accumulator |                     | Operable                                                                                                                                                                                                                                                                                                               |                                                     |                                                                        |
| DMA controller                              |                     |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |
| Power-on-reset function                     |                     |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |
| Voltage detection function                  |                     |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |
| External interrupt                          |                     |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |
| Key interrupt function                      |                     |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |
| CRC operation function                      | High-speed CRC      | In the calculation of the RAM area, operable when DMA is executed only                                                                                                                                                                                                                                                 |                                                     |                                                                        |
|                                             | General-purpose CRC |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |
| RAM parity error detection function         |                     | Operable when DMA is executed only                                                                                                                                                                                                                                                                                     |                                                     |                                                                        |
| RAM guard function                          |                     |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |
| SFR guard function                          |                     |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |
| Illegal-memory access detection function    |                     |                                                                                                                                                                                                                                                                                                                        |                                                     |                                                                        |

**Remark** Operation stopped: Operation is automatically stopped before switching to the HALT mode.

Operation disabled: Operation is stopped before switching to the HALT mode.

f<sub>IH</sub>: High-speed on-chip oscillator clock

f<sub>IL</sub>: Low-speed on-chip oscillator clock

f<sub>X</sub>: X1 clock

f<sub>EX</sub>: External main system clock

f<sub>XT</sub>: XT1 clock

f<sub>EXS</sub>: External subsystem clock

Table 19-1. Operating Statuses in HALT Mode (2/2)

| HALT Mode Setting<br>Item                   |                     | When HALT Instruction Is Executed While CPU Is Operating on Subsystem Clock                                                                                                                                                                                                                                            |                                                                       |                                         |
|---------------------------------------------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------|-----------------------------------------|
|                                             |                     | When CPU Is Operating on XT1 Clock (f <sub>XT</sub> )                                                                                                                                                                                                                                                                  | When CPU Is Operating on External Subsystem Clock (f <sub>EXS</sub> ) |                                         |
| System clock                                |                     | Clock supply to the CPU is stopped                                                                                                                                                                                                                                                                                     |                                                                       |                                         |
| Main system clock                           | f <sub>IH</sub>     | Operation disabled                                                                                                                                                                                                                                                                                                     |                                                                       |                                         |
|                                             | f <sub>X</sub>      |                                                                                                                                                                                                                                                                                                                        |                                                                       |                                         |
|                                             | f <sub>EX</sub>     |                                                                                                                                                                                                                                                                                                                        |                                                                       |                                         |
|                                             | Subsystem clock     | f <sub>XT</sub>                                                                                                                                                                                                                                                                                                        | Operation continues (cannot be stopped)                               | Cannot operate                          |
|                                             |                     | f <sub>EXS</sub>                                                                                                                                                                                                                                                                                                       | Cannot operate                                                        | Operation continues (cannot be stopped) |
| f <sub>IL</sub>                             |                     | Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC)<br>• WUTMMCK0 = 1: Oscillates<br>• WUTMMCK0 = 0 and WDTON = 0: Stops<br>• WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates<br>• WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops |                                                                       |                                         |
| CPU                                         |                     | Operation stopped                                                                                                                                                                                                                                                                                                      |                                                                       |                                         |
| Code flash memory                           |                     |                                                                                                                                                                                                                                                                                                                        |                                                                       |                                         |
| Data flash memory                           |                     |                                                                                                                                                                                                                                                                                                                        |                                                                       |                                         |
| RAM                                         |                     |                                                                                                                                                                                                                                                                                                                        |                                                                       |                                         |
| Port (latch)                                |                     | Status before HALT mode was set is retained                                                                                                                                                                                                                                                                            |                                                                       |                                         |
| Timer array unit                            |                     | Operates when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).                                                                                                                                                                                                                                |                                                                       |                                         |
| Real-time clock (RTC)                       |                     | Operable                                                                                                                                                                                                                                                                                                               |                                                                       |                                         |
| 12-bit interval timer                       |                     |                                                                                                                                                                                                                                                                                                                        |                                                                       |                                         |
| Watchdog timer                              |                     | See <b>CHAPTER 10 WATCHDOG TIMER</b>                                                                                                                                                                                                                                                                                   |                                                                       |                                         |
| Clock output/buzzer output                  |                     | Operates when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).                                                                                                                                                                                                                                |                                                                       |                                         |
| A/D converter                               |                     | Operation disabled                                                                                                                                                                                                                                                                                                     |                                                                       |                                         |
| Serial array unit (SAU)                     |                     | Operates when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).                                                                                                                                                                                                                                |                                                                       |                                         |
| Serial interface (IICA)                     |                     | Operation disabled                                                                                                                                                                                                                                                                                                     |                                                                       |                                         |
| LCD driver/controller                       |                     | Operable (However, this depends on the status of the clock selected as the LCD source clock: operation is possible if the selected clock is operating, but operation will stop if the selected clock is stopped.)                                                                                                      |                                                                       |                                         |
| Multiplier and divider/multiply-accumulator |                     | Operates when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).                                                                                                                                                                                                                                |                                                                       |                                         |
| DMA controller                              |                     |                                                                                                                                                                                                                                                                                                                        |                                                                       |                                         |
| Power-on-reset function                     |                     | Operable                                                                                                                                                                                                                                                                                                               |                                                                       |                                         |
| Voltage detection function                  |                     |                                                                                                                                                                                                                                                                                                                        |                                                                       |                                         |
| External interrupt                          |                     |                                                                                                                                                                                                                                                                                                                        |                                                                       |                                         |
| Key interrupt function                      |                     |                                                                                                                                                                                                                                                                                                                        |                                                                       |                                         |
| CRC operation function                      | High-speed CRC      | Operation disabled                                                                                                                                                                                                                                                                                                     |                                                                       |                                         |
|                                             | General-purpose CRC | In the calculation of the RAM area, operable when DMA is executed only                                                                                                                                                                                                                                                 |                                                                       |                                         |
| RAM parity error detection function         |                     | Operable when DMA is executed only                                                                                                                                                                                                                                                                                     |                                                                       |                                         |
| RAM guard function                          |                     |                                                                                                                                                                                                                                                                                                                        |                                                                       |                                         |
| SFR guard function                          |                     |                                                                                                                                                                                                                                                                                                                        |                                                                       |                                         |
| Illegal-memory access detection function    |                     | Operation stopped                                                                                                                                                                                                                                                                                                      |                                                                       |                                         |

**Remark** Operation stopped: Operation is automatically stopped before switching to the HALT mode.

Operation disabled: Operation is stopped before switching to the HALT mode.

$f_{IH}$ : High-speed on-chip oscillator clock

$f_{EX}$ : External main system clock

$f_{IL}$ : Low-speed on-chip oscillator clock

$f_{XT}$ : XT1 clock

$f_X$ : X1 clock

$f_{EXS}$ : External subsystem clock

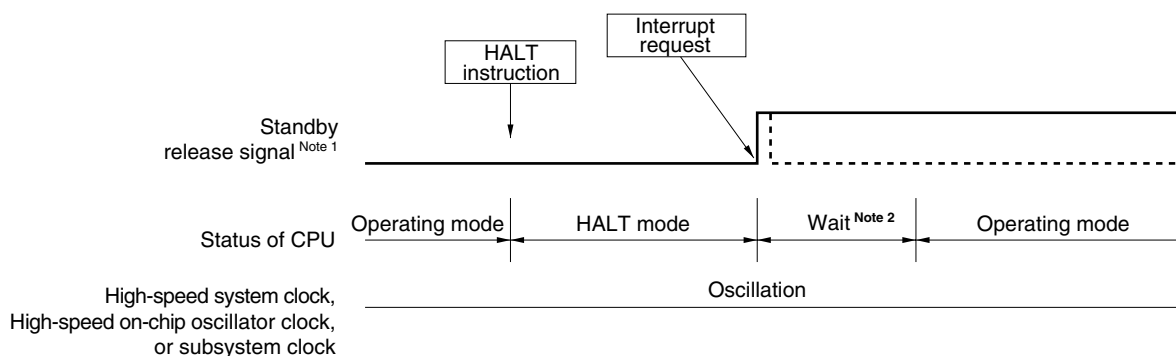
**(2) HALT mode release**

The HALT mode can be released by the following two sources.

**(a) Release by unmasked interrupt request**

When an unmasked interrupt request is generated, the HALT mode is released. If interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

**Figure 19-3. HALT Mode Release by Interrupt Request Generation**



<R>

**Notes 1.** For details of the standby release signal, see **Figure 17-1**

**2.** Wait time for HALT mode release

- When vectored interrupt servicing is carried out
  - Main system clock: 13 to 15 clock
  - Subsystem clock (RTCLPC = 0): 8 to 10 clock
  - Subsystem clock (RTCLPC = 1): 9 to 11 clock
- When vectored interrupt servicing is not carried out
  - Main system clock: 8 to 9 clock
  - Subsystem clock (RTCLPC = 0): 3 to 4 clock
  - Subsystem clock (RTCLPC = 1): 4 to 5 clock

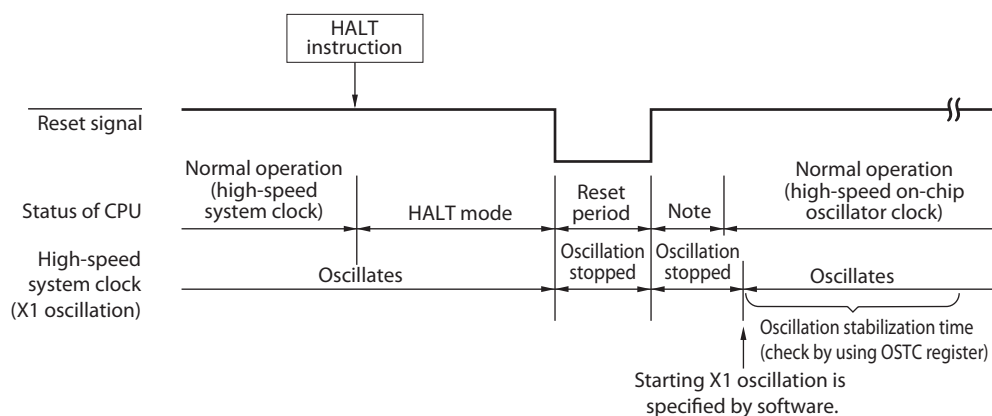
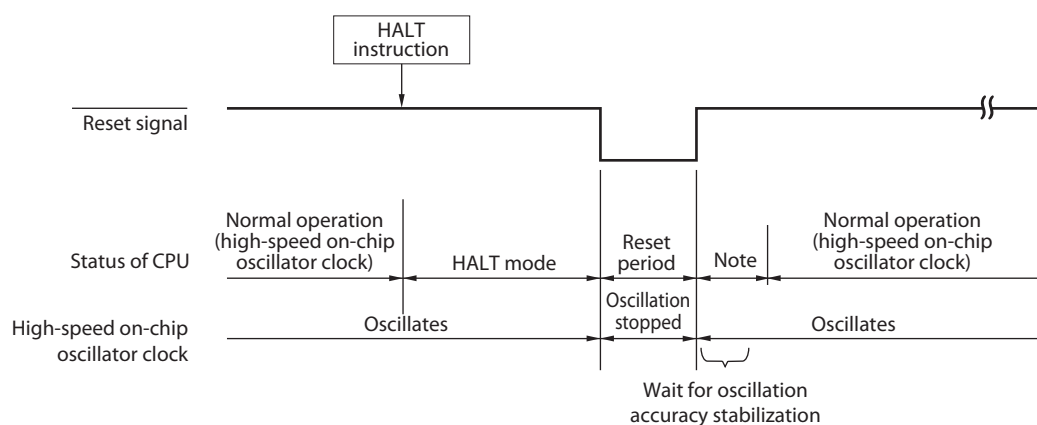
**Remark** The broken lines indicate the case when the interrupt request which has released the standby mode is acknowledged.



**(b) Release by reset signal generation**

When the reset signal is generated, HALT mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

&lt;R&gt;

**Figure 19-4. HALT Mode Release by Reset (1/2)****(1) When high-speed system clock is used as CPU clock****(2) When high-speed on-chip oscillator clock is used as CPU clock**

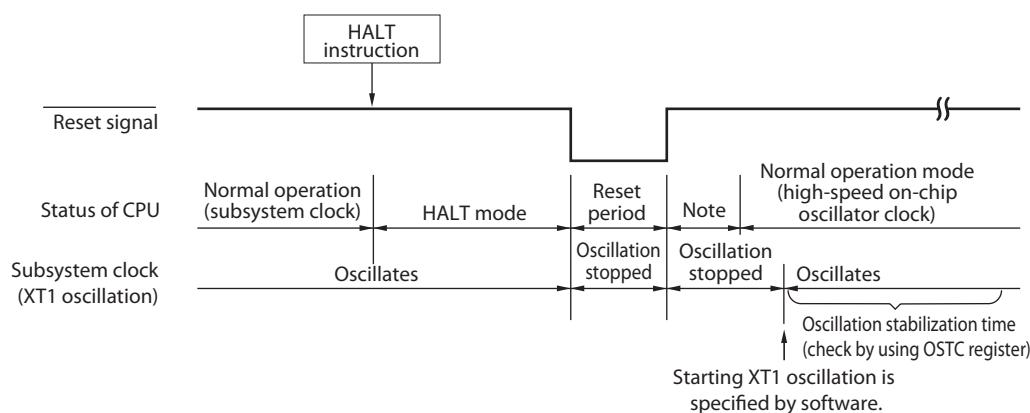
&lt;R&gt;

**Note** For the reset processing time, see **CHAPTER 20 RESET FUNCTION**.

For the reset processing time of the power-on-reset circuit (POR) and voltage detector (LVD), see **CHAPTER 21 POWER-ON-RESET CIRCUIT**.

**Remark** fx: X1 clock oscillation frequency

&lt;R&gt;

**Figure 19-4. HALT Mode Release by Reset (2/2)****(3) When subsystem clock is used as CPU clock**

&lt;R&gt;

**Note** For the reset processing time, see **CHAPTER 20 RESET FUNCTION**.For the reset processing time of the power-on-reset circuit (POR) and voltage detector (LVD), see **CHAPTER 21 POWER-ON-RESET CIRCUIT**.**19.3.2 STOP mode****(1) STOP mode setting and operating statuses**

The STOP mode is set by executing the STOP instruction, and it can be set only when the CPU clock before the setting was the main system clock.

&lt;R&gt;

- Cautions**
1. Because the interrupt request signal is used to clear the STOP mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the STOP mode is immediately cleared if set. Thus, when a STOP instruction is executed in this situation, the system returns to its normal operating mode as soon as the wait time set by using the oscillation stabilization time select register (OSTS) has elapsed. Note that the operating current during this period is the same as in the HALT mode because the clock is not stopped.
  2. When using CSI00, UART0, or the A/D converter in the SNOOZE mode, set up serial standby control register 0 (SSC0) and A/D converter mode register 2 (ADM2) before switching to the STOP mode. For details, see 12.3 Registers Controlling Serial Array Unit and 11.3 Registers Used in A/D Converter.

The operating statuses in the STOP mode are shown below.

Table 19-2. Operating Statuses in STOP Mode

| STOP Mode Setting<br><br>Item               |                                          |                                                                                                                                                                                                                                                                                                                        | When STOP Instruction Is Executed While CPU Is Operating on Main System Clock                                                                                                                                       |                                                     |                                                                        |
|---------------------------------------------|------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------|------------------------------------------------------------------------|
|                                             |                                          |                                                                                                                                                                                                                                                                                                                        | When CPU Is Operating on High-Speed On-Chip Oscillator Clock (f <sub>IH</sub> )                                                                                                                                     | When CPU Is Operating on X1 Clock (f <sub>x</sub> ) | When CPU Is Operating on External Main System Clock (f <sub>EX</sub> ) |
| System clock                                |                                          |                                                                                                                                                                                                                                                                                                                        | Clock supply to the CPU is stopped                                                                                                                                                                                  |                                                     |                                                                        |
|                                             | Main system clock                        | f <sub>IH</sub>                                                                                                                                                                                                                                                                                                        | Stopped                                                                                                                                                                                                             |                                                     |                                                                        |
|                                             |                                          | f <sub>x</sub>                                                                                                                                                                                                                                                                                                         |                                                                                                                                                                                                                     |                                                     |                                                                        |
|                                             |                                          | f <sub>EX</sub>                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                     |                                                     |                                                                        |
|                                             | Subsystem clock                          | f <sub>XT</sub>                                                                                                                                                                                                                                                                                                        | Status before STOP mode was set is retained                                                                                                                                                                         |                                                     |                                                                        |
|                                             |                                          | f <sub>EXS</sub>                                                                                                                                                                                                                                                                                                       |                                                                                                                                                                                                                     |                                                     |                                                                        |
| f <sub>IL</sub>                             |                                          | Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC)<br>• WUTMMCK0 = 1: Oscillates<br>• WUTMMCK0 = 0 and WDTON = 0: Stops<br>• WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates<br>• WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops |                                                                                                                                                                                                                     |                                                     |                                                                        |
| CPU                                         |                                          |                                                                                                                                                                                                                                                                                                                        | Operation stopped                                                                                                                                                                                                   |                                                     |                                                                        |
| Code flash memory                           |                                          |                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                     |                                                     |                                                                        |
| Data flash memory                           |                                          |                                                                                                                                                                                                                                                                                                                        | Operation stopped                                                                                                                                                                                                   |                                                     |                                                                        |
| RAM                                         |                                          |                                                                                                                                                                                                                                                                                                                        | Operation stopped                                                                                                                                                                                                   |                                                     |                                                                        |
| Port (latch)                                |                                          |                                                                                                                                                                                                                                                                                                                        | Status before STOP mode was set is retained                                                                                                                                                                         |                                                     |                                                                        |
| Timer array unit                            |                                          |                                                                                                                                                                                                                                                                                                                        | Operation disabled                                                                                                                                                                                                  |                                                     |                                                                        |
| Real-time clock (RTC)                       |                                          |                                                                                                                                                                                                                                                                                                                        | Operable                                                                                                                                                                                                            |                                                     |                                                                        |
| 12-bit interval timer                       |                                          |                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                     |                                                     |                                                                        |
| Watchdog timer                              |                                          |                                                                                                                                                                                                                                                                                                                        | See <b>CHAPTER 10 WATCHDOG TIMER</b>                                                                                                                                                                                |                                                     |                                                                        |
| <R>                                         | Clock output/buzzer output               |                                                                                                                                                                                                                                                                                                                        | Operates when the subsystem clock is selected as the clock source for counting and the RTCLPC bit is 0 (operation is disabled when a clock other than the subsystem clock is selected and the RTCLPC bit is not 0). |                                                     |                                                                        |
| A/D converter                               |                                          |                                                                                                                                                                                                                                                                                                                        | Wakeup operation is enabled (switching to the SNOOZE mode)                                                                                                                                                          |                                                     |                                                                        |
| Serial array unit (SAU)                     |                                          |                                                                                                                                                                                                                                                                                                                        | Wakeup operation is enabled only for CSI00 and UART0 (switching to the SNOOZE mode)<br>Operation is disabled for anything other than CSI00 and UART0                                                                |                                                     |                                                                        |
| Serial interface (IICA)                     |                                          |                                                                                                                                                                                                                                                                                                                        | Wakeup by address match operable                                                                                                                                                                                    |                                                     |                                                                        |
| LCD driver/controller                       |                                          |                                                                                                                                                                                                                                                                                                                        | Operable (However, this depends on the status of the clock selected as the LCD source clock: operation is possible if the selected clock is operating, but operation will stop if the selected clock is stopped.)   |                                                     |                                                                        |
| Multiplier and divider/multiply-accumulator |                                          |                                                                                                                                                                                                                                                                                                                        | Operation disabled                                                                                                                                                                                                  |                                                     |                                                                        |
| DMA controller                              |                                          |                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                     |                                                     |                                                                        |
| Power-on-reset function                     |                                          |                                                                                                                                                                                                                                                                                                                        | Operable                                                                                                                                                                                                            |                                                     |                                                                        |
| Voltage detection function                  |                                          |                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                     |                                                     |                                                                        |
| External interrupt                          |                                          |                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                     |                                                     |                                                                        |
| Key interrupt function                      |                                          |                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                     |                                                     |                                                                        |
| <R>                                         | CRC operation function                   | High-speed CRC                                                                                                                                                                                                                                                                                                         | Operation stopped                                                                                                                                                                                                   |                                                     |                                                                        |
|                                             |                                          | General-purpose CRC                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                                                     |                                                     |                                                                        |
|                                             | RAM parity error detection function      |                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                     |                                                     |                                                                        |
|                                             | RAM guard function                       |                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                     |                                                     |                                                                        |
|                                             | SFR guard function                       |                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                     |                                                     |                                                                        |
|                                             | Illegal-memory access detection function |                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                     |                                                     |                                                                        |

**Remark** Operation stopped: Operation is automatically stopped before switching to the STOP mode.

Operation disabled: Operation is stopped before switching to the STOP mode.

$f_{IH}$ : High-speed on-chip oscillator clock       $f_{IL}$ : Low-speed on-chip oscillator clock

$f_x$ : X1 clock       $f_{EX}$ : External main system clock

$f_{XT}$ : XT1 clock       $f_{EXS}$ : External subsystem clock

- <R> **Cautions**
1. To stop the low-speed on-chip oscillator clock in the STOP mode, must previously be set an option byte to stop the watchdog timer operation in the HALT/STOP mode (bit 0 (WDSTBYON) of 000C0H = 0).
  2. To shorten oscillation stabilization time after the STOP mode is released when the CPU operates with the high-speed system clock (X1 oscillation), temporarily switch the CPU clock to the high-speed on-chip oscillator clock before the execution of the STOP instruction. Before changing the CPU clock from the high-speed on-chip oscillator clock to the high-speed system clock (X1 oscillation) after the STOP mode is released, check the oscillation stabilization time with the oscillation stabilization time counter status register (OSTC).

## (2) STOP mode release

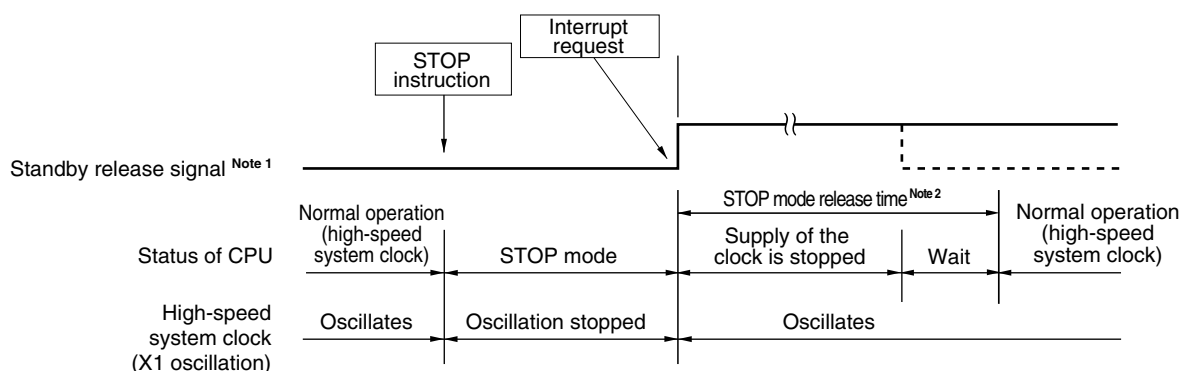
The STOP mode can be released by the following two sources.

### (a) Release by unmasked interrupt request

When an unmasked interrupt request is generated, the STOP mode is released. After the oscillation stabilization time has elapsed, if interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

<R> **Figure 19-5. STOP Mode Release by Interrupt Request Generation (1/2)**

#### (1) When high-speed system clock (X1 oscillation) is used as CPU clock



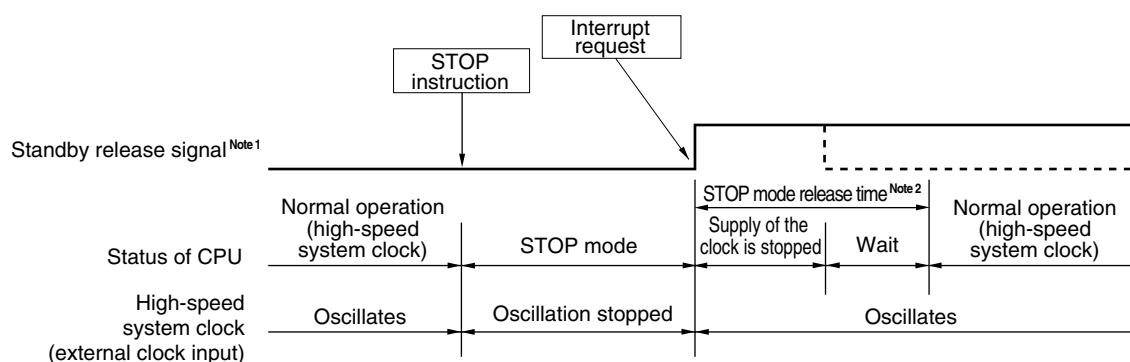
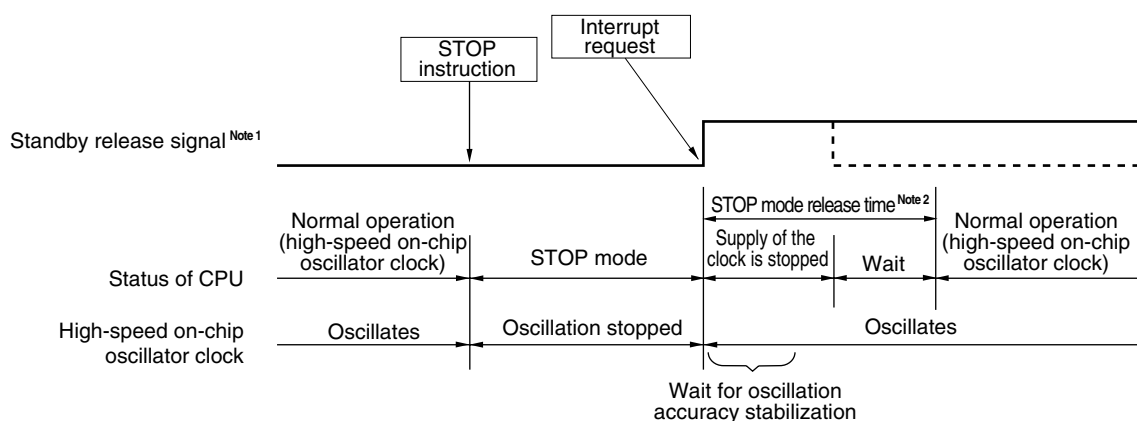
<R> **Notes**

1. For details of the standby release signal, see **Figure 17-1**.

2. Wait time for STOP mode release
  - High-speed system clock (X1 oscillation): 3-clock

**Remark** The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

&lt;R&gt;

**Figure 19-5. STOP Mode Release by Interrupt Request Generation (2/2)****(2) When high-speed system clock (external clock input) is used as CPU clock****(3) When high-speed on-chip oscillator clock is used as CPU clock**

&lt;R&gt;

**Notes 1.** For details of the standby release signal, see **Figure 17-1****2.** Supply of the clock is stopped: 19.08 to 32.99  $\mu$ s  
Wait

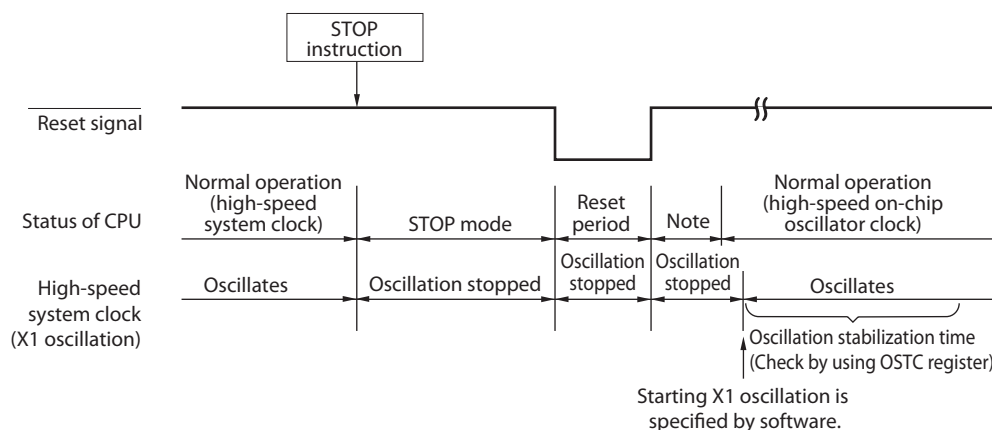
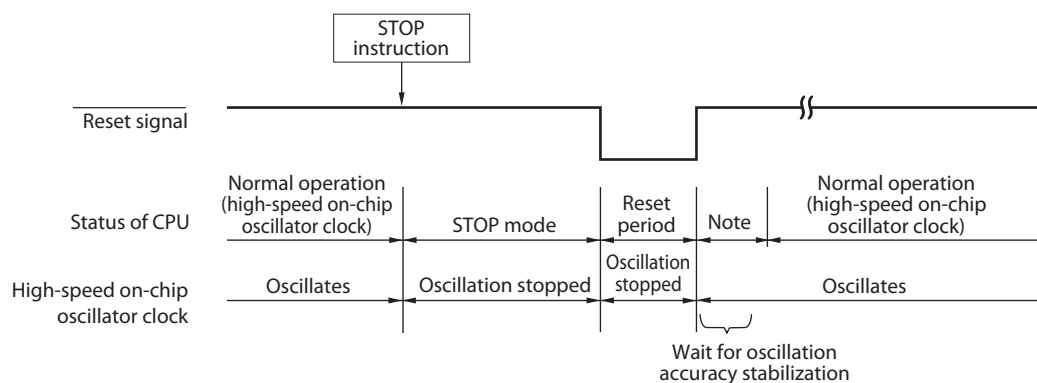
- When vectored interrupt servicing is carried out: 7 clocks
- When vectored interrupt servicing is not carried out: 1 clock

**Remark** The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

**(b) Release by reset signal generation**

When the reset signal is generated, STOP mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

&lt;R&gt;

**Figure 19-6. STOP Mode Release by Reset****(1) When high-speed system clock is used as CPU clock****(2) When high-speed on-chip oscillator clock is used as CPU clock**

&lt;R&gt;

**Note** For the reset processing time, see **CHAPTER 20 RESET FUNCTION**.

For the reset processing time of the power-on-reset circuit (POR) and voltage detector (LVD), see **CHAPTER 21 POWER-ON-RESET CIRCUIT**.

### 19.3.3 SNOOZE mode

#### <R> (1) SNOOZE mode setting and operating statuses

The SNOOZE mode can only be specified for CSI00, UART0, or the A/D converter. Note that this mode can only be specified if the CPU clock is the high-speed on-chip oscillator clock.

When using CSI00 or UART0 in the SNOOZE mode, set the SWCm bit of the serial standby control register m (SSCm) to 1 immediately before switching to the STOP mode. For details, see **12.3 Registers Controlling Serial Array Unit**.

When using the A/D converter in the SNOOZE mode, set the AWC bit of the A/D converter mode register 2 (ADM2) to 1 immediately before switching to the STOP mode. For details, see **11.3 Registers Used in A/D Converter**.

In SNOOZE mode transition, wait status to be only following time.

From STOP to SNOOZE

|                              |                        |
|------------------------------|------------------------|
| HS (High-speed main) mode :  | 18.96 to 28.95 $\mu$ s |
| LS (Low-speed main) mode :   | 20.24 to 28.95 $\mu$ s |
| LV (Low-voltage main) mode : | 20.98 to 28.95 $\mu$ s |

From SNOOZE to normal operation

- When vectored interrupt servicing is carried out:
 

|                              |                                  |
|------------------------------|----------------------------------|
| HS (High-speed main) mode :  | 6.79 to 12.4 $\mu$ s + 7 clocks  |
| LS (Low-speed main) mode :   | 2.58 to 7.8 $\mu$ s + 7 clocks   |
| LV (Low-voltage main) mode : | 12.45 to 17.3 $\mu$ s + 7 clocks |
- When vectored interrupt servicing is not carried out:
 

|                              |                                 |
|------------------------------|---------------------------------|
| HS (High-speed main) mode :  | 6.79 to 12.4 $\mu$ s + 1 clock  |
| LS (Low-speed main) mode :   | 2.58 to 7.8 $\mu$ s + 1 clock   |
| LV (Low-voltage main) mode : | 12.45 to 17.3 $\mu$ s + 1 clock |

The operating statuses in the SNOOZE mode are shown below.

Table 19-3. Operating Statuses in SNOOZE Mode

| STOP Mode Setting                           |                     | When Inputting CSI00/UART0 Data Reception Signal or A/D Converter Timer Trigger Signal While in STOP Mode                                                                                                                                                                                                              |  |
|---------------------------------------------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
| Item                                        |                     | When CPU Is Operating on High-Speed On-Chip Oscillator Clock (f <sub>IH</sub> )                                                                                                                                                                                                                                        |  |
| System clock                                |                     | Clock supply to the CPU is stopped                                                                                                                                                                                                                                                                                     |  |
| Main system clock                           | f <sub>IH</sub>     | Operation started                                                                                                                                                                                                                                                                                                      |  |
|                                             | f <sub>X</sub>      | Stopped                                                                                                                                                                                                                                                                                                                |  |
|                                             | f <sub>EX</sub>     |                                                                                                                                                                                                                                                                                                                        |  |
| Subsystem clock                             | f <sub>XT</sub>     | Use of the status while in the STOP mode continues                                                                                                                                                                                                                                                                     |  |
|                                             | f <sub>EXS</sub>    |                                                                                                                                                                                                                                                                                                                        |  |
| f <sub>IL</sub>                             |                     | Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC)<br>• WUTMMCK0 = 1: Oscillates<br>• WUTMMCK0 = 0 and WDTON = 0: Stops<br>• WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates<br>• WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops |  |
| CPU                                         |                     | Operation stopped                                                                                                                                                                                                                                                                                                      |  |
| Code flash memory                           |                     |                                                                                                                                                                                                                                                                                                                        |  |
| Data flash memory                           |                     |                                                                                                                                                                                                                                                                                                                        |  |
| RAM                                         |                     |                                                                                                                                                                                                                                                                                                                        |  |
| Port (latch)                                |                     | Use of the status while in the STOP mode continues                                                                                                                                                                                                                                                                     |  |
| Timer array unit                            |                     | Operation disabled                                                                                                                                                                                                                                                                                                     |  |
| Real-time clock (RTC)                       |                     | Operable                                                                                                                                                                                                                                                                                                               |  |
| 12-bit interval timer                       |                     |                                                                                                                                                                                                                                                                                                                        |  |
| Watchdog timer                              |                     | See <b>CHAPTER 10 WATCHDOG TIMER</b>                                                                                                                                                                                                                                                                                   |  |
| Clock output/buzzer output                  |                     | Operates when the subsystem clock is selected as the clock source for counting and the RTCLPC bit is 0 (operation is disabled when a clock other than the subsystem clock is selected and the RTCLPC bit is not 0).                                                                                                    |  |
| A/D converter                               |                     | Operable                                                                                                                                                                                                                                                                                                               |  |
| Serial array unit (SAU)                     |                     | Operable only CSI00 and UART0 only. Operation disabled other than CSI00 and UART0.                                                                                                                                                                                                                                     |  |
| Serial interface (IICA)                     |                     | Operation disabled                                                                                                                                                                                                                                                                                                     |  |
| LCD driver/controller                       |                     | Operable (However, this depends on the status of the clock selected as the LCD source clock: operation is possible if the selected clock is operating, but operation will stop if the selected clock is stopped.)                                                                                                      |  |
| Multiplier and divider/multiply-accumulator |                     | Operation disabled                                                                                                                                                                                                                                                                                                     |  |
| DMA controller                              |                     |                                                                                                                                                                                                                                                                                                                        |  |
| Power-on-reset function                     |                     | Operable                                                                                                                                                                                                                                                                                                               |  |
| Voltage detection function                  |                     |                                                                                                                                                                                                                                                                                                                        |  |
| External interrupt                          |                     |                                                                                                                                                                                                                                                                                                                        |  |
| Key interrupt function                      |                     |                                                                                                                                                                                                                                                                                                                        |  |
| CRC operation function                      | High-speed CRC      | Operation stopped                                                                                                                                                                                                                                                                                                      |  |
|                                             | General-purpose CRC |                                                                                                                                                                                                                                                                                                                        |  |
| RAM parity error detection function         |                     |                                                                                                                                                                                                                                                                                                                        |  |
| RAM guard function                          |                     |                                                                                                                                                                                                                                                                                                                        |  |
| SFR guard function                          |                     |                                                                                                                                                                                                                                                                                                                        |  |
| Illegal-memory access detection function    |                     |                                                                                                                                                                                                                                                                                                                        |  |

**Remark** Operation stopped: Operation is automatically stopped before switching to the SNOOZE mode.

Operation disabled: Operation is stopped before switching to the SNOOZE mode.

$f_{IH}$ : High-speed on-chip oscillator clock       $f_{IL}$ : Low-speed on-chip oscillator clock

$f_X$ : X1 clock       $f_{EX}$ : External main system clock

$f_{XT}$ : XT1 clock       $f_{EXS}$ : External subsystem clock



## CHAPTER 20 RESET FUNCTION

The following seven operations are available to generate a reset signal.

- (1) External reset input via  $\overline{\text{RESET}}$  pin
- (2) Internal reset by watchdog timer program loop detection
- (3) Internal reset by comparison of supply voltage and detection voltage of power-on-reset (POR) circuit
- (4) Internal reset by comparison of supply voltage of the voltage detector (LVD) and detection voltage
- (5) Internal reset by execution of illegal instruction<sup>Note</sup>
- (6) Internal reset by RAM parity error
- (7) Internal reset by illegal-memory access

External and internal resets start program execution from the address at 0000H and 0001H when the reset signal is generated.

A reset is effected when a low level is input to the  $\overline{\text{RESET}}$  pin, the watchdog timer overflows, or by POR and LVD circuit voltage detection, execution of illegal instruction<sup>Note</sup>, RAM parity error or illegal-memory access, and each item of hardware is set to the status shown in Tables 20-1.

When a low level is input to the  $\overline{\text{RESET}}$  pin, the device is reset. It is released from the reset status when a high level is input to the  $\overline{\text{RESET}}$  pin and program execution is started with the high-speed on-chip oscillator clock after reset processing. A reset by the watchdog timer is automatically released, and program execution starts using the high-speed on-chip oscillator clock (see **Figures 20-2** and **20-3**) after reset processing. Reset by POR and LVD circuit supply voltage detection is automatically released when  $V_{DD} \geq V_{POR}$  or  $V_{DD} \geq V_{LVD}$  after the reset, and program execution starts using the high-speed on-chip oscillator clock (see **CHAPTER 21 POWER-ON-RESET CIRCUIT** and **CHAPTER 22 VOLTAGE DETECTOR**) after reset processing.

**Note** The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

**Cautions** 1. For an external reset, input a low level for 10  $\mu\text{s}$  or more to the  $\overline{\text{RESET}}$  pin.

(To perform an external reset upon power application, a low level of at least 10  $\mu\text{s}$  must be continued during the period in which the supply voltage is within the operating range ( $V_{DD} \geq 1.6\text{ V}$ ).)

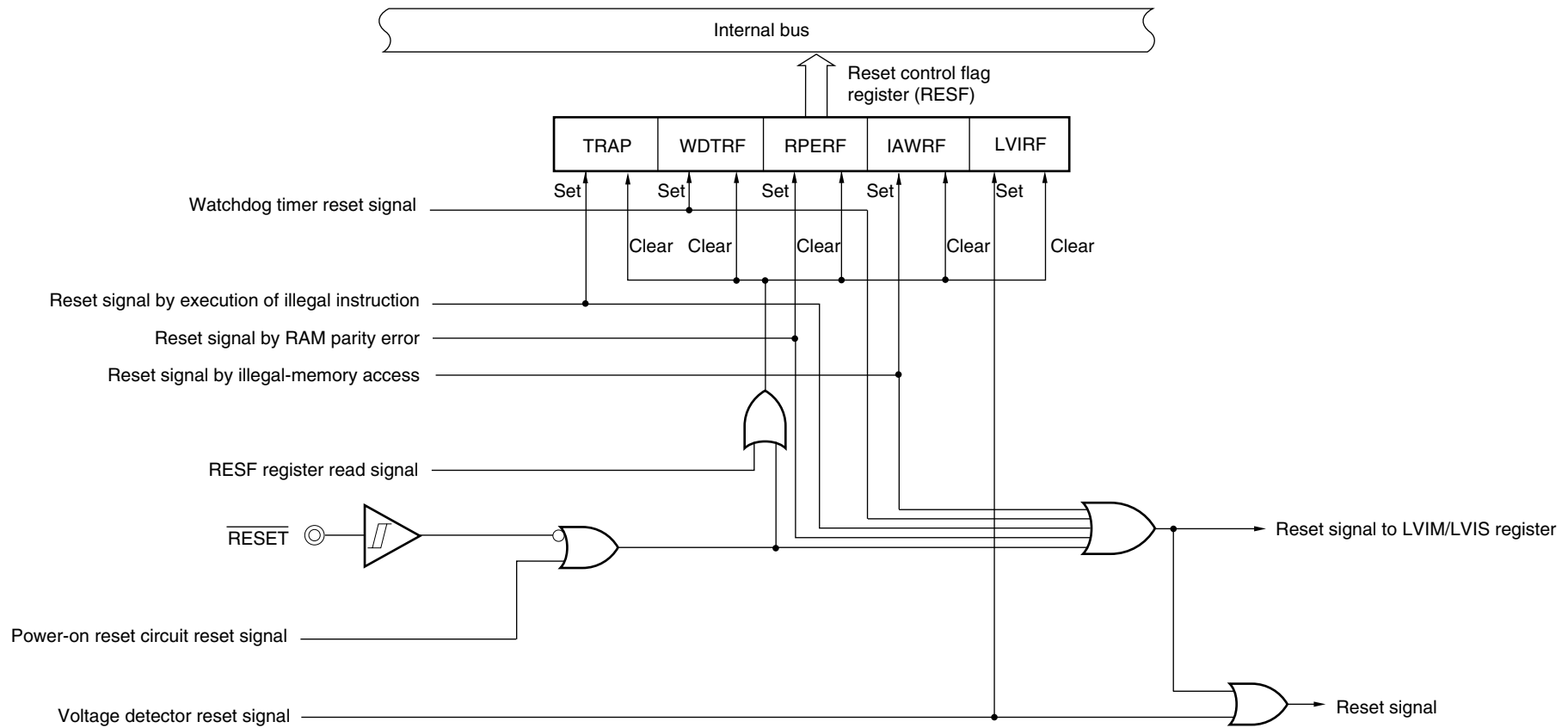
2. During reset input, the X1 clock, XT1 clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock stop oscillating. External main system clock input and external subsystem clock input become invalid.

3. Each of the SFRs and 2nd SFRs are initialized when a reset is applied, so port pin P130 is set for low-level output and P40 becomes high-impedance (in the case of an external reset or POR reset) or is pulled-up (in the case of other types of reset), and the other port pins become high-impedance.

<R>

**Remark**  $V_{POR}$ : POR power supply rise detection voltage

Figure 20-1. Block Diagram of Reset Function

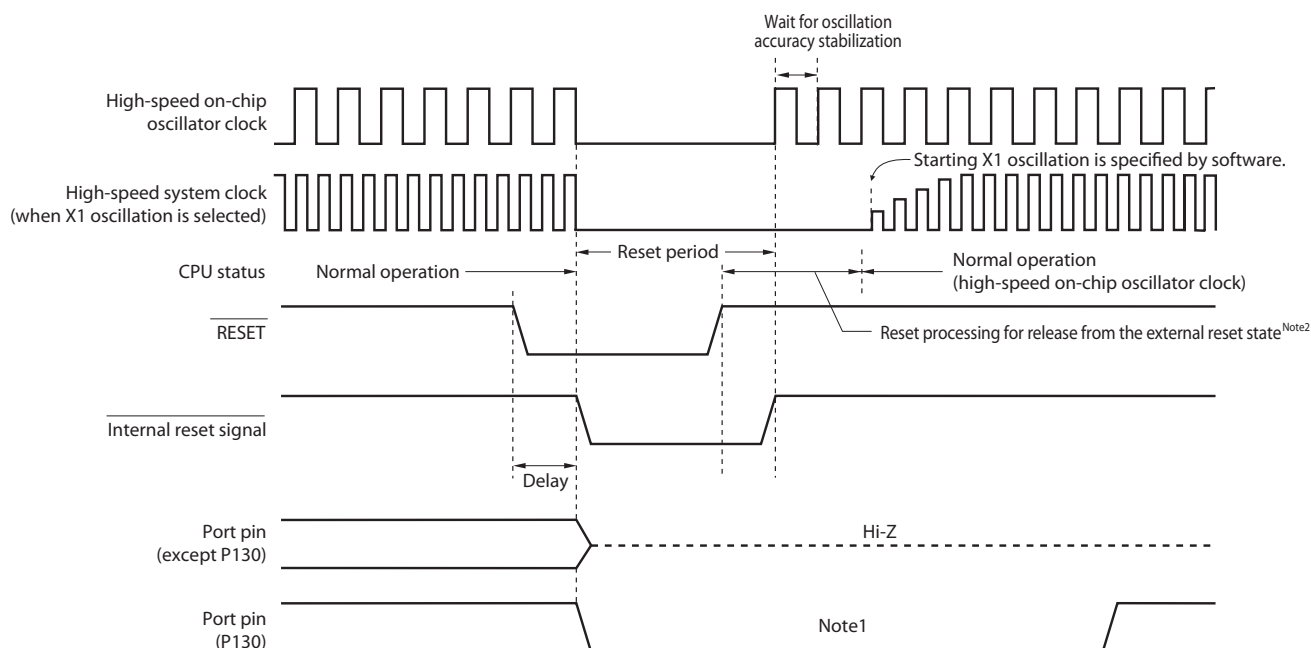
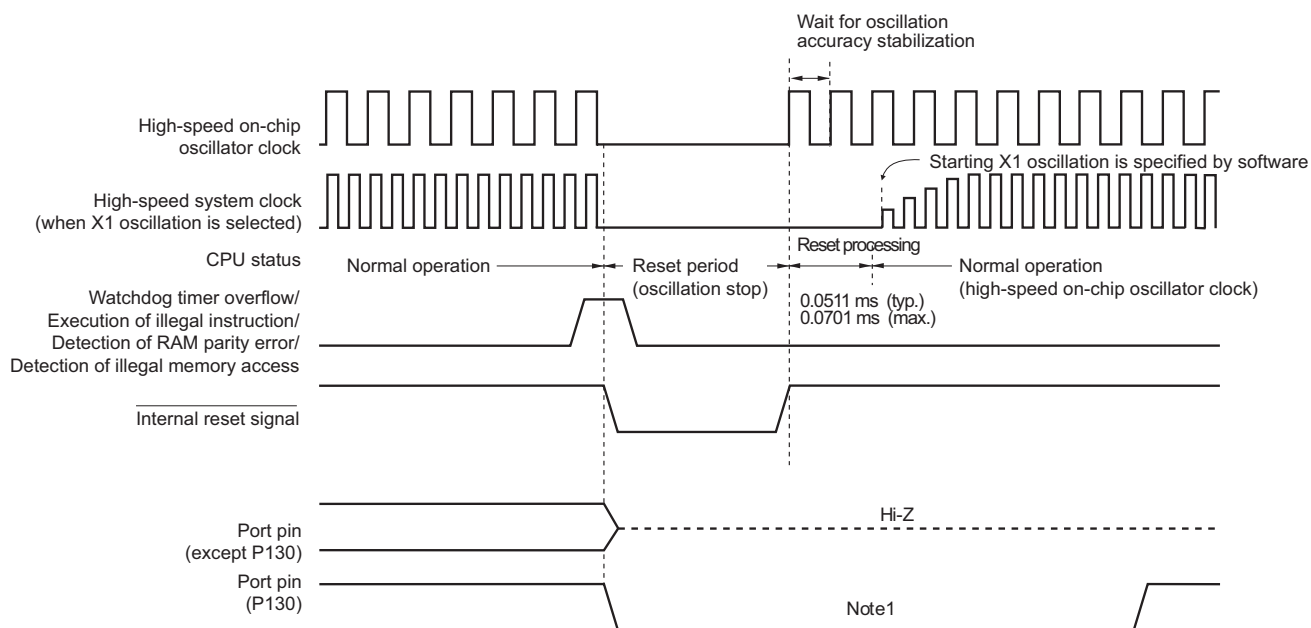


**Caution** An LVD circuit internal reset does not reset the LVD circuit.

**Remarks**

1. LVIM: Voltage detection register
2. LVIS: Voltage detection level register

&lt;R&gt;

**Figure 20-2. Timing of Reset by RESET Input****<R> Figure 20-3. Timing of Reset Due to Execution of Illegal Instruction, Watchdog Timer Overflow, RAM Parity Error, or Illegal Memory Access**

**Notes 1.** When P130 is set to high-level output before reset is effected, the output signal of P130 can be dummy-output as a reset signal to an external device, because P130 outputs a low level when reset is effected. To release a reset signal to an external device, set P130 to high-level output by software.

- <R> **Notes 2.** Reset times (times for release from the external reset state)
- After the first release of the POR: 0.672 ms (typ.), 0.832 ms (max.) when the LVD is in use.  
0.399 ms (typ.), 0.519 ms (max.) when the LVD is off.
- After the second release of the POR: 0.531 ms (typ.), 0.675 ms (max.) when the LVD is in use.  
0.259 ms (typ.), 0.362 ms (max.) when the LVD is off.
- After power is supplied, a voltage stabilization waiting time of about 0.99 ms (typ.) and up to 2.30 ms (max.) is required before reset processing starts after release of the external reset.

**Caution** A watchdog timer internal reset resets the watchdog timer.

**Remark** For the reset timing of the power-on-reset circuit and voltage detector, see **CHAPTER 21 POWER-ON-RESET CIRCUIT** and **CHAPTER 22 VOLTAGE DETECTOR**.

Table 20-1. Operation Statuses During Reset Period

| Item                                       |                     |                   | During Reset Period                                                                                                                                                                                                                         |
|--------------------------------------------|---------------------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| System clock                               |                     |                   | Clock supply to the CPU is stopped.                                                                                                                                                                                                         |
| Main system clock                          | f <sub>IH</sub>     |                   | Operation stopped                                                                                                                                                                                                                           |
|                                            | f <sub>X</sub>      |                   | Operation stopped (the X1 and X2 pins are input port mode)                                                                                                                                                                                  |
|                                            | f <sub>EX</sub>     |                   | Clock input invalid (the pin is input port mode)                                                                                                                                                                                            |
|                                            | Subsystem clock     | f <sub>XT</sub>   | Operation stopped (the XT1 and XT2 pins are input port mode)                                                                                                                                                                                |
|                                            |                     | f <sub>EXS</sub>  | Clock input invalid (the pin is input port mode)                                                                                                                                                                                            |
| f <sub>IL</sub>                            |                     | Operation stopped |                                                                                                                                                                                                                                             |
| CPU                                        |                     |                   |                                                                                                                                                                                                                                             |
| Code flash memory                          |                     |                   | Operation stopped                                                                                                                                                                                                                           |
| Data flash memory                          |                     |                   | Operation stopped                                                                                                                                                                                                                           |
| RAM                                        |                     |                   | Operation stopped                                                                                                                                                                                                                           |
| Port (latch)                               |                     |                   | P130 is set to low-level output.<br>P40 becomes high impedance (external reset or POR reset).<br>P40 is pulled-up (resets other than external reset and POR reset).<br>The port pins except for P130 and P40 become high impedance.         |
| Timer array unit                           |                     |                   | Operation stopped                                                                                                                                                                                                                           |
| Real-time clock (RTC)                      |                     |                   |                                                                                                                                                                                                                                             |
| 12-bit interval timer                      |                     |                   |                                                                                                                                                                                                                                             |
| Watchdog timer                             |                     |                   |                                                                                                                                                                                                                                             |
| Clock output/buzzer output                 |                     |                   |                                                                                                                                                                                                                                             |
| A/D converter                              |                     |                   |                                                                                                                                                                                                                                             |
| Serial array unit (SAU)                    |                     |                   |                                                                                                                                                                                                                                             |
| Serial interface (IICA)                    |                     |                   |                                                                                                                                                                                                                                             |
| LCD driver/controller                      |                     |                   |                                                                                                                                                                                                                                             |
| Multiplier & divider, multiply-accumulator |                     |                   | Operation stopped<br>(COM only pin, COM/SEG alternate pin: GND output,<br>SEG/general-purpose port alternate pin: high-impedance output,<br>VL1 to VL4 pins: high-impedance output,<br>CAPH/P127 pin, CAPL/P126 pin: high-impedance output) |
| DMA controller                             |                     |                   |                                                                                                                                                                                                                                             |
| Power-on-reset function                    |                     |                   | Detection operation possible                                                                                                                                                                                                                |
| Voltage detection function                 |                     |                   | Operation stopped                                                                                                                                                                                                                           |
| External interrupt                         |                     |                   | Operation stopped                                                                                                                                                                                                                           |
| Key interrupt function                     |                     |                   |                                                                                                                                                                                                                                             |
| CRC operation function                     | High-speed CRC      |                   |                                                                                                                                                                                                                                             |
|                                            | General-purpose CRC |                   |                                                                                                                                                                                                                                             |
| RAM parity error detection function        |                     |                   |                                                                                                                                                                                                                                             |
| RAM guard function                         |                     |                   |                                                                                                                                                                                                                                             |
| SFR guard function                         |                     |                   |                                                                                                                                                                                                                                             |
| Illegal-memory access detection function   |                     |                   |                                                                                                                                                                                                                                             |

**Remark** f<sub>IH</sub>: High-speed on-chip oscillator clock      f<sub>IL</sub>: Low-speed on-chip oscillator clock  
 f<sub>X</sub>: X1 oscillation clock      f<sub>EX</sub>: External main system clock  
 f<sub>XT</sub>: XT1 oscillation clock      f<sub>EXS</sub>: External subsystem clock

Table 20-2. Hardware Statuses After Reset Acknowledgment (1/4)

| Hardware                                                            |                                                          | After Reset Acknowledgment <sup>Note 1</sup>                   |
|---------------------------------------------------------------------|----------------------------------------------------------|----------------------------------------------------------------|
| Program counter (PC)                                                |                                                          | The contents of the reset vector table (0000H, 0001H) are set. |
| Stack pointer (SP)                                                  |                                                          | Undefined                                                      |
| Program status word (PSW)                                           |                                                          | 06H                                                            |
| RAM                                                                 | Data memory                                              | Undefined                                                      |
|                                                                     | General-purpose registers                                | Undefined                                                      |
| Processor mode control register (PMC)                               |                                                          | 00H                                                            |
| Port registers (P1 to P7, P12 to P14) (output latches)              |                                                          | 00H                                                            |
| Port mode registers                                                 | PM1 to PM7, PM12, PM14                                   | FFH                                                            |
| Port mode control registers 1, 4, 12, 14 (PMC1, PMC4, PMC12, PMC14) |                                                          | FFH                                                            |
| Port input mode register 1 (PIM1)                                   |                                                          | 00H                                                            |
| Port output mode register 1 (POM1)                                  |                                                          | 00H                                                            |
| Pull-up resistor option register (PU1, PU3 to PU5, PU7, PU12, PU14) |                                                          | 00H (PU4 is 01H)                                               |
| Peripheral I/O redirection register (PIOR)                          |                                                          | 00H                                                            |
| Clock operation mode control register (CMC)                         |                                                          | 00H                                                            |
| Clock operation status control register (CSC)                       |                                                          | C0H                                                            |
| System clock control register (CKC)                                 |                                                          | 00H                                                            |
| Oscillation stabilization time counter status register (OSTC)       |                                                          | 00H                                                            |
| Oscillation stabilization time select register (OSTS)               |                                                          | 07H                                                            |
| Noise filter enable registers 0, 1 (NFEN0, NFEN1)                   |                                                          | 00H                                                            |
| Peripheral enable register 0 (PER0)                                 |                                                          | 00H                                                            |
| High-speed on-chip oscillator frequency select register (HOCODIV)   |                                                          | Undefined                                                      |
| <R>                                                                 | High-speed on-chip oscillator trimming register (HIOTRM) | Undefined <sup>Note 2</sup>                                    |
|                                                                     | Operation speed mode control register (OSMC)             | 00H                                                            |
| Timer array unit                                                    | Timer data registers 00 to 07 (TDR00 to TDR07)           | 0000H                                                          |
|                                                                     | Timer mode registers 00 to 07 (TMR00 to TMR07)           | 0000H                                                          |
|                                                                     | Timer status registers 00 to 07 (TSR00 to TSR07)         | 0000H                                                          |
|                                                                     | Timer input select register 0 (TIS0)                     | 00H                                                            |
|                                                                     | Timer output select register (TOS)                       | 00H                                                            |
|                                                                     | Timer counter registers 00 to 07 (TCR00 to TCR07)        | FFFFH                                                          |
|                                                                     | Timer channel enable status register 0 (TE0)             | 0000H                                                          |
|                                                                     | Timer channel start register 0 (TS0)                     | 0000H                                                          |
|                                                                     | Timer channel stop register 0 (TT0)                      | 0000H                                                          |
|                                                                     | Timer clock select register 0 (TPS0)                     | 0000H                                                          |
|                                                                     | Timer output register 0 (TO0)                            | 0000H                                                          |
|                                                                     | Timer output enable register 0 (TOE0)                    | 0000H                                                          |
|                                                                     | Timer output level register 0 (TOL0)                     | 0000H                                                          |
|                                                                     | Timer output mode registers 0 (TOM0)                     | 0000H                                                          |

**Notes** 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

<R> 2. The value after a reset is acknowledged is the value adjusted at shipment.

**Remark** The special function register (SFR) mounted depend on the product. See 3.2.4 Special function registers (SFRs) and 3.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers).

Table 20-2. Hardware Statuses After Reset Acknowledgment (2/4)

| Hardware                              |                                                                        | Status After Reset Acknowledgment <sup>Note 1</sup> |
|---------------------------------------|------------------------------------------------------------------------|-----------------------------------------------------|
| Real-time clock                       | Second count register (SEC)                                            | 00H                                                 |
|                                       | Minute count register (MIN)                                            | 00H                                                 |
|                                       | Hour count register (HOUR)                                             | 12H                                                 |
|                                       | Week count register (WEEK)                                             | 00H                                                 |
|                                       | Day count register (DAY)                                               | 01H                                                 |
|                                       | Month count register (MONTH)                                           | 01H                                                 |
|                                       | Year count register (YEAR)                                             | 00H                                                 |
|                                       | Watch error correction register (SUBCUD)                               | 00H                                                 |
|                                       | Alarm minute register (ALARMWM)                                        | 00H                                                 |
|                                       | Alarm hour register (ALARMWH)                                          | 12H                                                 |
|                                       | Alarm week register (ALARMWW)                                          | 00H                                                 |
|                                       | Control register 0 (RTCC0)                                             | 00H                                                 |
|                                       | Control register 1 (RTCC1)                                             | 00H                                                 |
| Interval timer                        | Control register (ITMC)                                                | 0FFFH                                               |
| Clock output/buzzer output controller | Clock output select registers 0, 1 (CKS0, CKS1)                        | 00H                                                 |
| Watchdog timer                        | Enable register (WDTE)                                                 | 1AH/9AH <sup>Note 2</sup>                           |
| A/D converter                         | 10-bit A/D conversion result register (ADCR)                           | 0000H                                               |
|                                       | 8-bit A/D conversion result register (ADCRH)                           | 00H                                                 |
|                                       | Mode registers 0 to 2 (ADM0 to ADM2)                                   | 00H                                                 |
|                                       | Conversion result comparison upper limit setting register (ADUL)       | FFH                                                 |
|                                       | Conversion result comparison lower limit setting register (ADLL)       | 00H                                                 |
|                                       | A/D test register (ADTES)                                              | 00H                                                 |
|                                       | Analog input channel specification register (ADS)                      | 00H                                                 |
|                                       | A/D port configuration register (ADPC)                                 | 00H                                                 |
| Serial array unit (SAU)               | Serial data registers 00, 01 (SDR00, SDR01)                            | 0000H                                               |
|                                       | Serial status registers 00, 01 (SSR00, SSR01)                          | 0000H                                               |
|                                       | Serial flag clear trigger registers 00, 01 (SIR00, SIR01)              | 0000H                                               |
|                                       | Serial mode registers 00, 01 (SMR00, SMR01)                            | 0020H                                               |
|                                       | Serial communication operation setting registers 00, 01 (SCR00, SCR01) | 0087H                                               |
|                                       | Serial channel enable status register 0 (SE0)                          | 0000H                                               |
|                                       | Serial channel start register 0 (SS0)                                  | 0000H                                               |
|                                       | Serial channel stop register 0 (ST0)                                   | 0000H                                               |
|                                       | Serial clock select register 0 (SPS0)                                  | 0000H                                               |
|                                       | Serial output register 0 (SO0)                                         | 0303H                                               |
|                                       | Serial output enable register 0 (SOE0)                                 | 0000H                                               |
|                                       | Serial output level register 0 (SOL0)                                  | 0000H                                               |
|                                       | Serial standby control register 0 (SSC0)                               | 0000H                                               |
|                                       | Input switch control register (ISC)                                    | 00H                                                 |

- Notes**
1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.
  2. The reset value of WDTE is determined by the option byte setting.

**Remark** The special function register (SFR) mounted depend on the product. See **3.2.4 Special function registers (SFRs)** and **3.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.

Table 20-2. Hardware Statuses After Reset Acknowledgment (3/4)

| Hardware                                   |                                                       | Status After Reset Acknowledgment <sup>Note 1</sup> |
|--------------------------------------------|-------------------------------------------------------|-----------------------------------------------------|
| Serial interface IICA                      | IICA shift register 0 (IICA0)                         | 00H                                                 |
|                                            | IICA status register 0 (IICS0)                        | 00H                                                 |
|                                            | IICA flag register 0 (IICF0)                          | 00H                                                 |
|                                            | IICA control register 00 (IICCTL00)                   | 00H                                                 |
|                                            | IICA control register 01 (IICCTL01)                   | 00H                                                 |
|                                            | IICA low-level width setting register 0 (IICWL0)      | FFH                                                 |
|                                            | IICA high-level width setting register 0 (IICWH0)     | FFH                                                 |
|                                            | Slave address register 0 (SVA0)                       | 00H                                                 |
| LCD driver/controller                      | LCD mode registers 0, 1 (LCDM0, LCDM1)                | 00H                                                 |
|                                            | LCD clock control register (LCDC0)                    | 00H                                                 |
|                                            | LCD boost level control register (VLCD)               | 04H                                                 |
|                                            | Memory-type liquid crystal control register (MLCD)    | 00H                                                 |
|                                            | LCD port function registers 0 to 4 (PFSEG0 to PFSEG4) | FFH (PFSEG0 is F0H, PFSEG4 is 7FH)                  |
|                                            | LCD Input switch control register (ISCLCD)            | 00H                                                 |
|                                            | LCD display data memories 0 to 38 (SEG0 to SEG38)     | 00H                                                 |
| Multiplier & divider, multiply-accumulator | Multiplication/division data register A (L) (MDAL)    | 0000H                                               |
|                                            | Multiplication/division data register A (H) (MDAH)    | 0000H                                               |
|                                            | Multiplication/division data register B (L) (MDBL)    | 0000H                                               |
|                                            | Multiplication/division data register B (H) (MDBH)    | 0000H                                               |
|                                            | Multiplication/division data register C (L) (MDCL)    | 0000H                                               |
|                                            | Multiplication/division data register C (H) (MDCH)    | 0000H                                               |
|                                            | Multiplication/division control register (MDUC)       | 00H                                                 |
| Key interrupt                              | Key return control register (KRCTL)                   | 00H                                                 |
|                                            | Key return flag register (KRF)                        | 00H                                                 |
|                                            | Key return mode register 0 (KRM0)                     | 00H                                                 |

**Note** During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

**Remark** The special function register (SFR) mounted depend on the product. See **3.2.4 Special function registers (SFRs)** and **3.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.



**Table 20-2. Hardware Statuses After Reset Acknowledgment (4/4)**

| Hardware               |                                                                                                                                                               | Status After Reset Acknowledgment <sup>Note 1</sup> |
|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------|
| Reset function         | Reset control flag register (RESF)                                                                                                                            | Undefined <sup>Note 2</sup>                         |
| Voltage detector (LVD) | Voltage detection register (LVIM)                                                                                                                             | 00H <sup>Note 2</sup>                               |
|                        | Voltage detection level register (LVIS)                                                                                                                       | 00H/01H/81H <sup>Notes 2, 3</sup>                   |
| DMA controller         | SFR address registers 0, 1 (DSA0, DSA1)                                                                                                                       | 00H                                                 |
|                        | RAM address registers 0, 1 (DRA0, DRA1)                                                                                                                       | 0000H                                               |
|                        | Byte count registers 0, 1 (DBC0, DBC1)                                                                                                                        | 0000H                                               |
|                        | Mode control registers 0, 1 (DMC0, DMC1)                                                                                                                      | 00H                                                 |
|                        | Operation control registers 0, 1 (DRC0, DRC1)                                                                                                                 | 00H                                                 |
| Interrupt              | Request flag registers 0L, 0H, 1L, 1H, 2L (IF0L, IF0H, IF1L, IF1H, IF2L)                                                                                      | 00H                                                 |
|                        | Mask flag registers 0L, 0H, 1L, 1H, 2L (MK0L, MK0H, MK1L, MK1H, MK2L)                                                                                         | FFH                                                 |
|                        | Priority specification flag registers 00L, 00H, 01L, 01H, 02L, 10L, 10H, 11L, 11H, 12L (PR00L, PR00H, PR01L, PR01H, PR10L, PR10H, PR11L, PR11H, PR02L, PR12L) | FFH                                                 |
|                        | External interrupt rising edge enable register 0 (EGP0)                                                                                                       | 00H                                                 |
|                        | External interrupt falling edge enable register 0 (EGN0)                                                                                                      | 00H                                                 |
| Safety functions       | Flash memory CRC control register (CRC0CTL)                                                                                                                   | 00H                                                 |
|                        | Flash memory CRC operation result register (PGCRCL)                                                                                                           | 0000H                                               |
|                        | CRC input register (CRCIN)                                                                                                                                    | 00H                                                 |
|                        | CRC data register (CRCD)                                                                                                                                      | 0000H                                               |
|                        | Invalid memory access detection control register (IAWCTL)                                                                                                     | 00H                                                 |
|                        | RAM parity error control register (RPECTL)                                                                                                                    | 00H                                                 |
| Flash memory           | Data flash control register (DFLCTL)                                                                                                                          | 00H                                                 |
| BCD correction circuit | BCD correction result register (BCDAJ)                                                                                                                        | Undefined                                           |

(Notes and Remark are listed on the next page.)

- Notes**
1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.
  2. These values vary depending on the reset source.

<R>

| Reset Source<br>Register |           | RESET Input           | Reset by<br>POR | Reset by<br>Execution of<br>Illegal<br>Instruction | Reset by<br>WDT | Reset by<br>RAM parity<br>error | Reset by<br>illegal-<br>memory<br>access | Reset by<br>LVD |
|--------------------------|-----------|-----------------------|-----------------|----------------------------------------------------|-----------------|---------------------------------|------------------------------------------|-----------------|
| RESF                     | TRAP bit  | Cleared (0)           |                 | Set (1)                                            | Held            |                                 |                                          | Held            |
|                          | WDTRF bit |                       |                 | Held                                               | Set (1)         | Held                            |                                          |                 |
|                          | RPERF bit |                       |                 | Held                                               |                 | Set (1)                         | Held                                     |                 |
|                          | IAWRF bit |                       |                 | Held                                               |                 |                                 | Set (1)                                  |                 |
|                          | LVIRF bit |                       |                 | Held                                               |                 |                                 |                                          | Set (1)         |
| LVIM                     | LVISEN    | Cleared (0)           |                 |                                                    |                 |                                 |                                          | Held            |
|                          | LVIOMSK   | Held                  |                 |                                                    |                 |                                 |                                          |                 |
|                          | LVIF      |                       |                 |                                                    |                 |                                 |                                          |                 |
| LVIS                     |           | Cleared (00H/01H/81H) |                 |                                                    |                 |                                 |                                          |                 |

3. The generation of reset signal other than an LVD reset sets as follows.

- When option byte LVIMDS1, LVIMDS0 = 1, 0: 00H
- When option byte LVIMDS1, LVIMDS0 = 1, 1: 81H
- When option byte LVIMDS1, LVIMDS0 = 0, 1: 01H

**Remark** The special function register (SFR) mounted depend on the product. See **3.2.4 Special function registers (SFRs)** and **3.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.

## 20.1 Register for Confirming Reset Source

### 20.1.1 Reset Control Flag Register (RESF)

Many internal reset generation sources exist in the RL78/L12. The reset control flag register (RESF) is used to store which source has generated the reset request.

The RESF register can be read by an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$  input, reset by power-on-reset (POR) circuit, and reading the RESF register clear TRAP, WDTRF, RPERF, IAWRF, and LVIRF flags.

**Figure 20-4. Format of Reset Control Flag Register (RESF)**

Address: FFFA8H After reset: 00H<sup>Note 1</sup> R

| Symbol | 7    | 6 | 5 | 4     | 3 | 2     | 1     | 0     |
|--------|------|---|---|-------|---|-------|-------|-------|
| RESF   | TRAP | 0 | 0 | WDTRF | 0 | RPERF | IAWRF | LVIRF |

|      |                                                                              |
|------|------------------------------------------------------------------------------|
| TRAP | Internal reset request by execution of illegal instruction <sup>Note 2</sup> |
| 0    | Internal reset request is not generated, or the RESF register is cleared.    |
| 1    | Internal reset request is generated.                                         |

|       |                                                                           |
|-------|---------------------------------------------------------------------------|
| WDTRF | Internal reset request by watchdog timer (WDT)                            |
| 0     | Internal reset request is not generated, or the RESF register is cleared. |
| 1     | Internal reset request is generated.                                      |

|       |                                                                           |
|-------|---------------------------------------------------------------------------|
| RPERF | Internal reset request t by RAM parity                                    |
| 0     | Internal reset request is not generated, or the RESF register is cleared. |
| 1     | Internal reset request is generated.                                      |

|       |                                                                           |
|-------|---------------------------------------------------------------------------|
| IAWRF | Internal reset request t by illegal-memory access                         |
| 0     | Internal reset request is not generated, or the RESF register is cleared. |
| 1     | Internal reset request is generated.                                      |

|       |                                                                           |
|-------|---------------------------------------------------------------------------|
| LVIRF | Internal reset request by voltage detector (LVD)                          |
| 0     | Internal reset request is not generated, or the RESF register is cleared. |
| 1     | Internal reset request is generated.                                      |

- Notes**
1. The value after reset varies depending on the reset source.
  2. The illegal instruction is generated when instruction code FFH is executed.  
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

**Cautions** 1. Do not read data by a 1-bit memory manipulation instruction.

2. When enabling RAM parity error resets (RPERDIS = 0), be sure to initialize the used RAM area at data access or the used RAM area + 10 bytes at execution of instruction from the RAM area. Reset generation enables RAM parity error resets (RPERDIS = 0). For details, see 23.3.3 RAM parity error detection function.

<R>

The status of the RESF register when a reset request is generated is shown in Table 20-3.

**Table 20-3. RESF Register Status When Reset Request Is Generated**

| Reset Source<br>Flag | RESET Input | Reset by<br>POR | Reset by<br>Execution of<br>Illegal<br>Instruction | Reset by<br>WDT | Reset by<br>RAM parity<br>error | Reset by<br>illegal-<br>memory<br>access | Reset by<br>LVD |
|----------------------|-------------|-----------------|----------------------------------------------------|-----------------|---------------------------------|------------------------------------------|-----------------|
| TRAP bit             | Cleared (0) |                 | Set (1)                                            | Held            |                                 |                                          |                 |
| WDTRF bit            |             |                 | Held                                               | Set (1)         | Held                            |                                          |                 |
| RPERF bit            |             |                 | Held                                               |                 | Set (1)                         | Held                                     |                 |
| IAWRF bit            |             |                 | Held                                               |                 |                                 | Set (1)                                  | Held            |
| LVIRF bit            |             |                 | Held                                               |                 |                                 |                                          | Set (1)         |

## CHAPTER 21 POWER-ON-RESET CIRCUIT

### 21.1 Functions of Power-on-reset Circuit

The power-on-reset circuit (POR) has the following functions.

- Generates internal reset signal at power on.
- <R> The reset signal is released when the supply voltage ( $V_{DD}$ ) exceeds  $1.51\text{ V} \pm 0.04\text{ V}$ .
- Compares supply voltage ( $V_{DD}$ ) and detection voltage ( $V_{PDR} = 1.50\text{ V} \pm 0.04\text{ V}$ ), generates internal reset signal when  $V_{DD} < V_{PDR}$ .

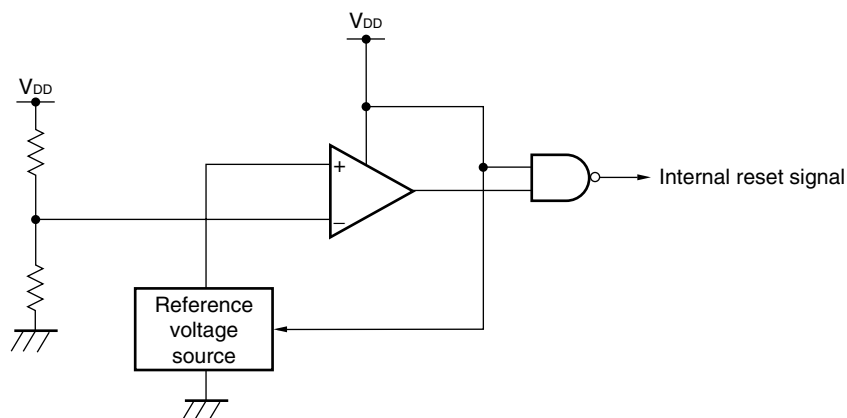
**Caution** If an internal reset signal is generated in the POR circuit, TRAP, WDTRF, RPERF, IAWRF, and LVIRF flags of the reset control flag register (RESF) is cleared.

**Remark** This product incorporates multiple hardware functions that generate an internal reset signal. A flag that indicates the reset source is located in the reset control flag register (RESF) for when an internal reset signal is generated by the watchdog timer (WDT), voltage-detector (LVD), illegal instruction execution, RAM parity error, or illegal-memory access. The RESF register is not cleared to 00H and the flag is set to 1 when an internal reset signal is generated by the watchdog timer (WDT), voltage-detector (LVD), illegal instruction execution, RAM parity error, or illegal-memory access.  
For details of the RESF register, see **CHAPTER 20 RESET FUNCTION**.

## 21.2 Configuration of Power-on-reset Circuit

The block diagram of the power-on-reset circuit is shown in Figure 21-1.

**Figure 21-1. Block Diagram of Power-on-reset Circuit**



## 21.3 Operation of Power-on-reset Circuit

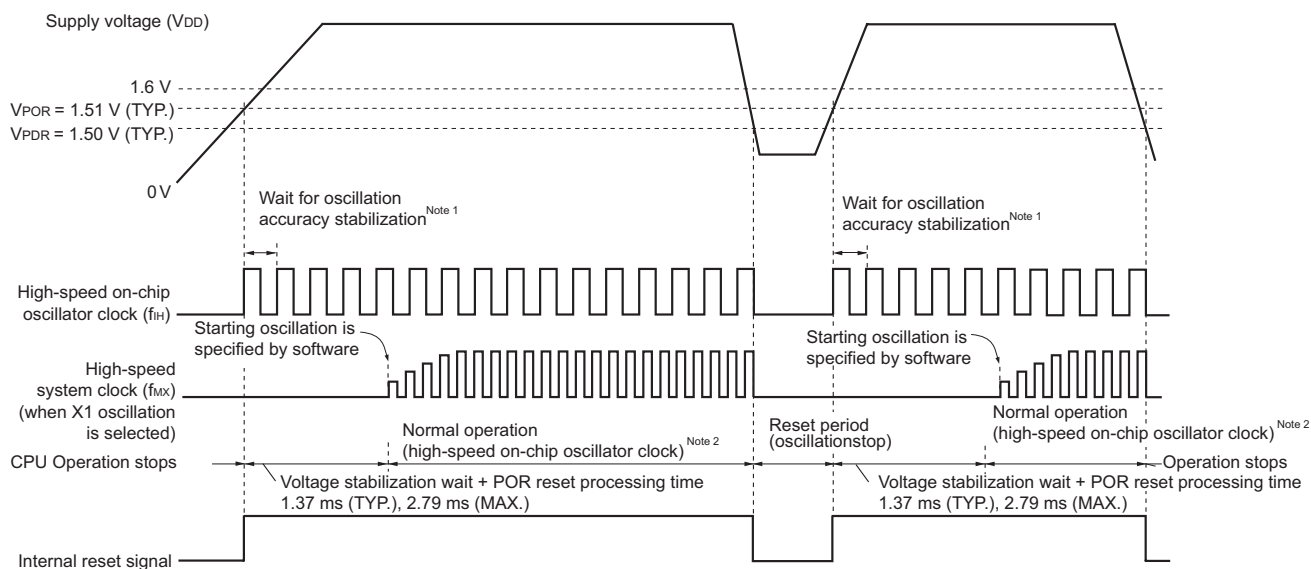
- An internal reset signal is generated on power application. When the supply voltage ( $V_{DD}$ ) exceeds the detection voltage ( $V_{PDR} = 1.51\text{ V} \pm 0.04\text{ V}$ ), the reset status is released.
- The supply voltage ( $V_{DD}$ ) and detection voltage ( $V_{PDR} = 1.50\text{ V} \pm 0.04\text{ V}$ ) are compared. When  $V_{DD} < V_{PDR}$ , the internal reset signal is generated.

The timing of generation of the internal reset signal by the power-on-reset circuit and voltage detector is shown below.

&lt;R&gt;

**Figure 21-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)**

**(1) When LVD is OFF (option byte 000C1H: VPOC2 = 1B)**



**Notes 1.** The internal reset processing time includes the oscillation accuracy stabilization time of the high-speed on-chip oscillator clock.

&lt;R&gt;

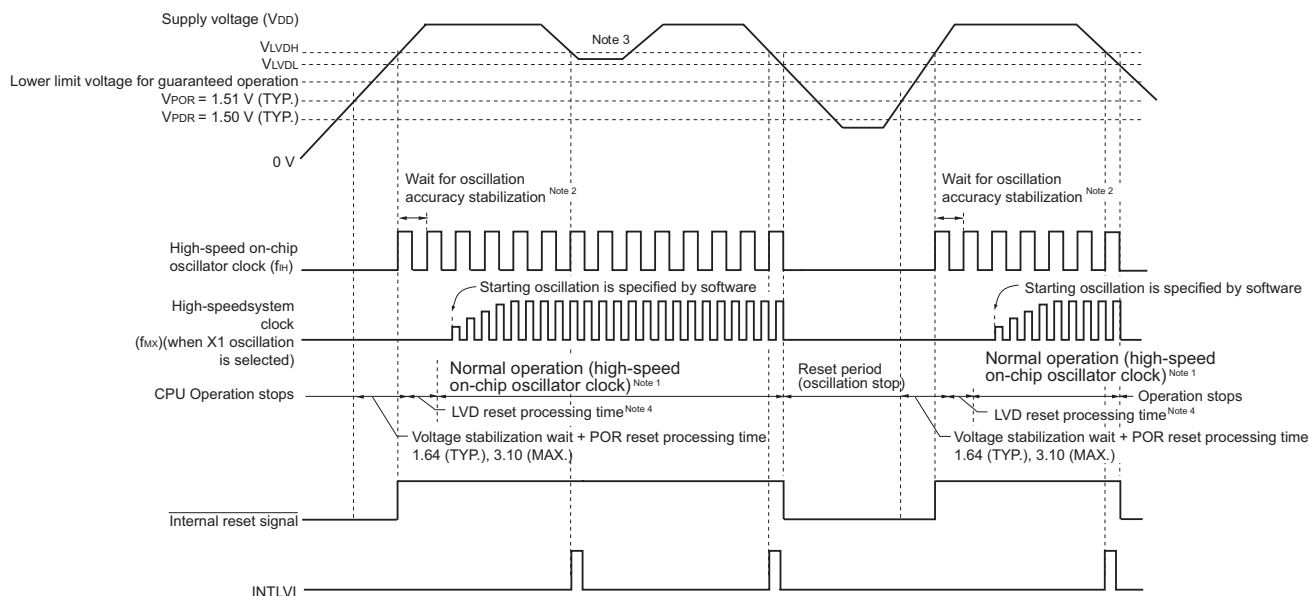
- 2.** The high-speed on-chip oscillator clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. To use the X1 clock, use the oscillation stabilization time counter status register (OSTC) to confirm the lapse of the oscillation stabilization time. To use the XT1 clock, use the timer function for confirmation of the lapse of the stabilization time.

**Remark** V<sub>POR</sub>: POR power supply rise detection voltage  
V<sub>PDR</sub>: POR power supply fall detection voltage

&lt;R&gt;

**Figure 21-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (2/3)**

**(2) When LVD is interrupt & reset mode (option byte 000C1: LVIMDS1, LVIMDS0 = 1, 0)**



**Notes 1.** The high-speed on-chip oscillator clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. To use the X1 clock, use the oscillation stabilization time counter status register (OSTC) to confirm the lapse of the oscillation stabilization time. To use the XT1 clock, use the timer function for confirmation of the lapse of the stabilization time.

**2.** The internal reset processing time includes the oscillation accuracy stabilization time of the high-speed on-chip oscillator clock.

&lt;R&gt;

**3.** After the first interrupt request signal (INTLVI) is generated, the LVIL and LVIMD bits of the voltage detection level register (LVIS) are automatically set to 1. If the operating voltage returns to 1.6 V or higher without falling below the voltage detection level (VLVDL), after INTLVI is generated, perform the required backup processing, and then use software to specify the initial settings in order.

&lt;R&gt;

**4.** The time until normal operation starts includes the following LVD reset processing time after the LVD detection level (VLVDH) is reached as well as the voltage stabilization wait + POR reset processing time after the VPOR (1.51 V, typ.) is reached.

LVD reset processing time: 0 ms to 0.0701 ms (max.)

**Remark** VLVDH, VLVDL: LVD detection voltage

VPOR: POR power supply rise detection voltage

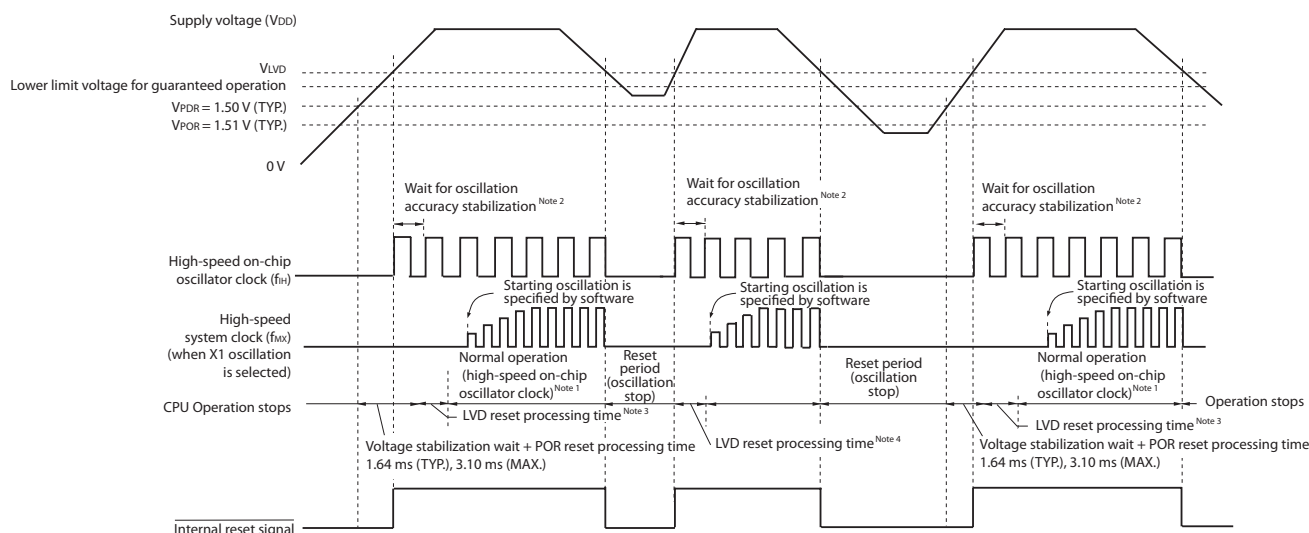
VPDR: POR power supply fall detection voltage



&lt;R&gt;

**Figure 21-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (3/3)**

**(3) When LVD is interrupt & reset mode (option byte 000C1/010C1H: LVIMDS1, LVIMDS0 = 1, 1)**



- Notes**
1. The high-speed on-chip oscillator clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. To use the X1 clock, use the oscillation stabilization time counter status register (OSTC) to confirm the lapse of the oscillation stabilization time. To use the XT1 clock, use the timer function for confirmation of the lapse of the stabilization time.
  2. The internal reset processing time includes the oscillation accuracy stabilization time of the high-speed on-chip oscillator clock.
  3. The time until normal operation starts includes the following LVD reset processing time after the LVD detection level ( $V_{LVD}$ ) is reached as well as the voltage stabilization wait + POR reset processing time after the  $V_{POR}$  (1.51 V, typ.) is reached.  
LVD reset processing time: 0 ms to 0.0701 ms (max.)
  4. When the power supply voltage is below the lower limit for operation and the power supply voltage is then restored after an internal reset is generated only by the voltage detector (LVD), the following LVD reset processing time is required after the LVD detection level ( $V_{LVD}$ ) is reached.  
LVD reset processing time: 0.0511 ms (typ.), 0.0701 ms (max.)

&lt;R&gt;

&lt;R&gt;

**Remark**  $V_{POR}$ : POR power supply rise detection voltage  
 $V_{PDR}$ : POR power supply fall detection voltage

## 21.4 Cautions for Power-on-reset Circuit

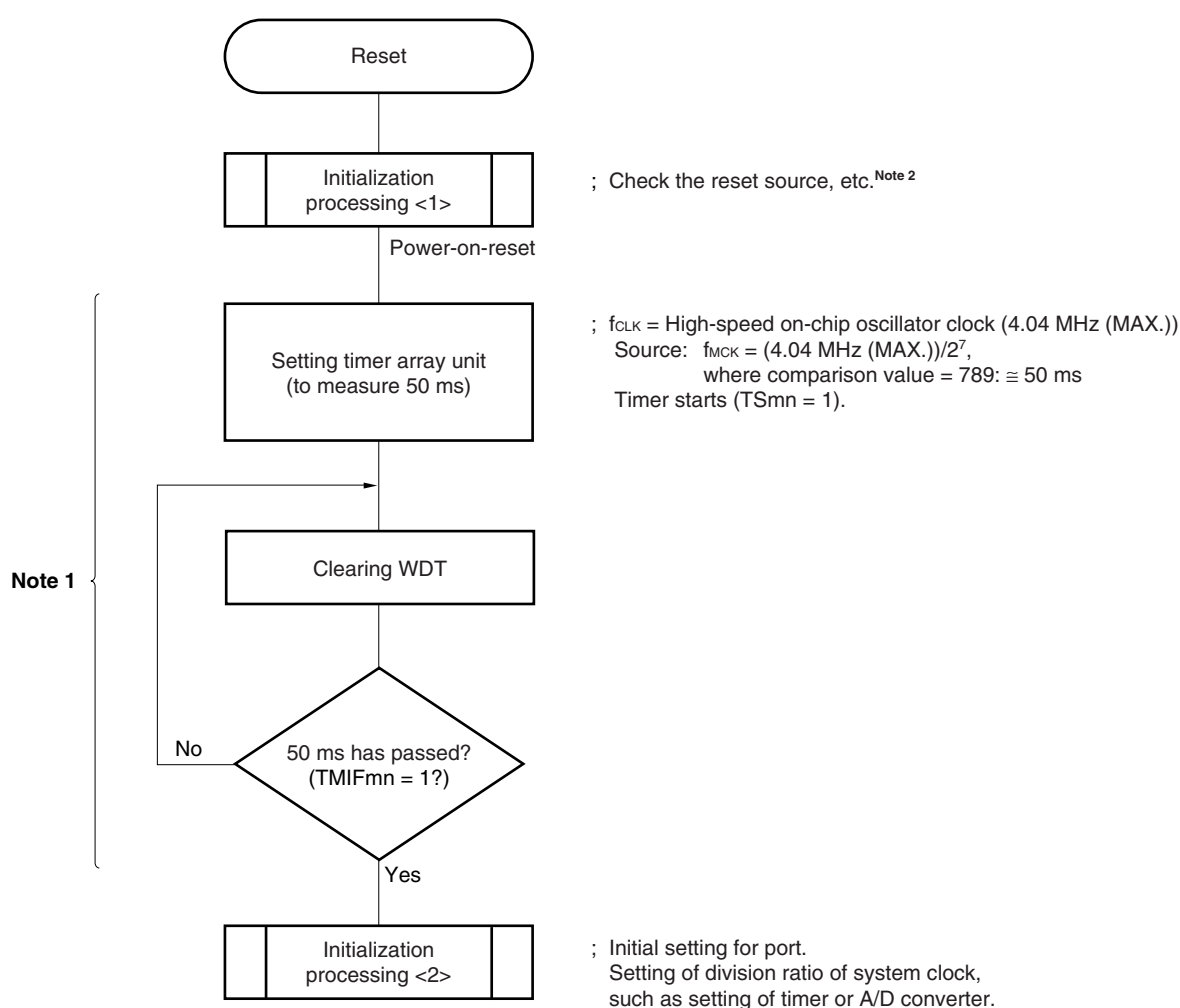
In a system where the supply voltage ( $V_{DD}$ ) fluctuates for a certain period in the vicinity of the POR detection voltage ( $V_{POR}$ ,  $V_{PDR}$ ), the system may be repeatedly reset and released from the reset status. In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking the following action.

### <Action>

After releasing the reset signal, wait for the supply voltage fluctuation period of each system by means of a software counter that uses a timer, and then initialize the ports.

**Figure 21-3. Example of Software Processing After Reset Release (1/2)**

- If supply voltage fluctuation is 50 ms or less in vicinity of POR detection voltage



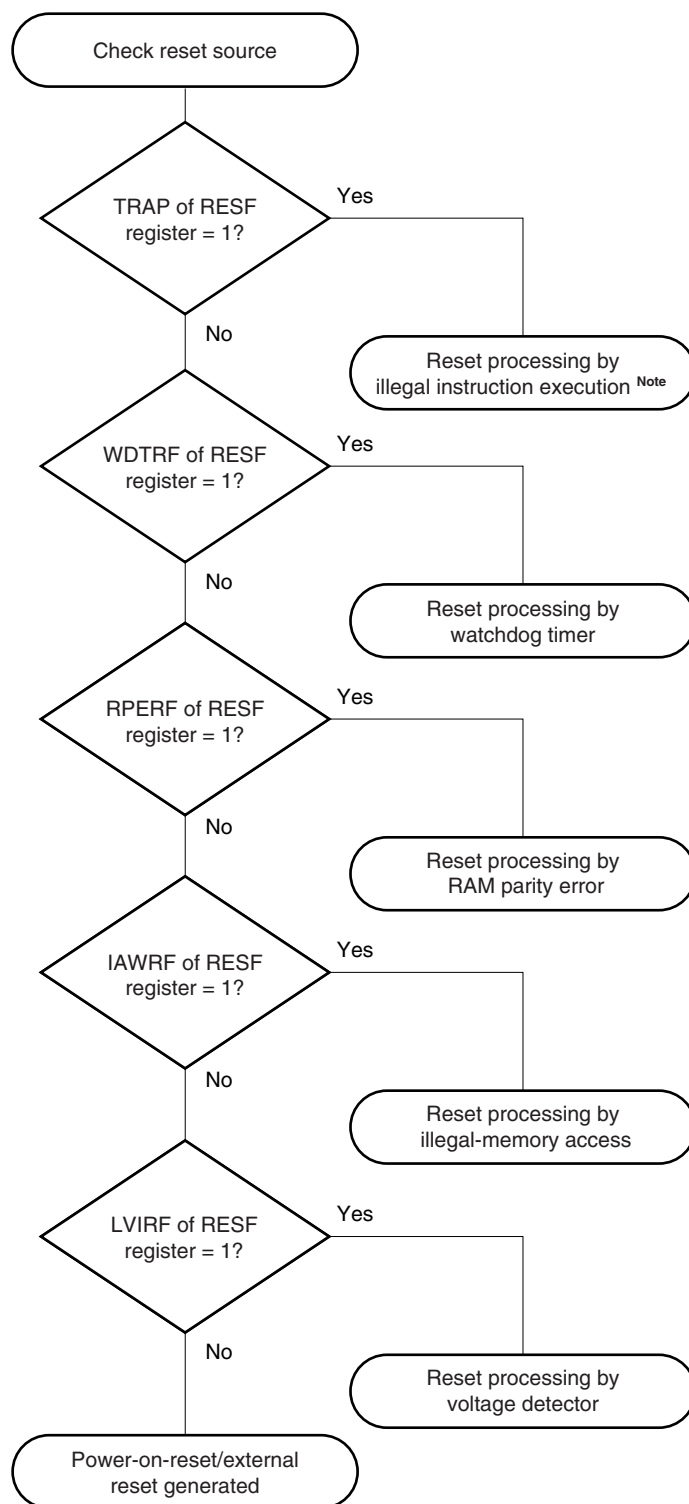
**Notes** 1. If reset is generated again during this period, initialization processing <2> is not started.

2. A flowchart is shown on the next page.

**Remark** m = 0  
 n = 0 to 7

**Figure 21-3. Example of Software Processing After Reset Release (2/2)**

- Checking reset source



**Note** The illegal instruction is generated when instruction code FFH is executed.  
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

## CHAPTER 22 VOLTAGE DETECTOR

### 22.1 Functions of Voltage Detector

The voltage detector (LVD) has the following functions.

- The LVD circuit compares the supply voltage ( $V_{DD}$ ) with the detection voltage ( $V_{LVDH}$ ,  $V_{LVDL}$ ), and generates an internal reset or internal interrupt signal.
- The detection level for the power supply detection voltage ( $V_{LVDH}$ ,  $V_{LVDL}$ ) can be selected by using the option byte as one of 14 levels (For details, see **CHAPTER 25 OPTION BYTE**).
- Operable in STOP mode.
- The following three operation modes can be selected by using the option byte.

(a) Interrupt & reset mode (option byte LVIMDS1, LVIMDS0 = 1, 0)

For the two detection voltages selected by the option byte 000C1H, the high-voltage detection level ( $V_{LVDH}$ ) is used for generating interrupts and ending resets, and the low-voltage detection level ( $V_{LVDL}$ ) is used for triggering resets.

(b) Reset mode (option byte LVIMDS1, LVIMDS0 = 1, 1)

The detection voltage ( $V_{LVD}$ ) selected by the option byte 000C1H is used for triggering and ending resets.

(c) Interrupt mode (option byte LVIMDS1, LVIMDS0 = 0, 1)

The detection voltage ( $V_{LVD}$ ) selected by the option byte 000C1H is used for generating interrupts/reset release.

Two detection voltages ( $V_{LVDH}$ ,  $V_{LVDL}$ ) can be specified in the interrupt & reset mode, and one ( $V_{LVD}$ ) can be specified in the reset mode and interrupt mode.

The reset and interrupt signals are generated as follows according to the option byte (LVIMDS0, LVIMDS1) selection.

| Interrupt & reset mode<br>(LVIMDS1, LVIMDS0 = 1, 0)                                                                                                                           | Reset mode<br>(LVIMDS1, LVIMDS0 = 1, 1)                                                                               | Interrupt mode<br>(LVIMDS1, LVIMDS0 = 0, 1)                                                                                                                                                                                                         |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Generates an internal interrupt signal when $V_{DD} < V_{LVDH}$ , and an internal reset when $V_{DD} < V_{LVDL}$ .<br>Releases the reset signal when $V_{DD} \geq V_{LVDH}$ . | Generates an internal reset signal when $V_{DD} < V_{LVD}$ and releases the reset signal when $V_{DD} \geq V_{LVD}$ . | Generates an internal interrupt signal when $V_{DD}$ drops lower than $V_{LVD}$ ( $V_{DD} < V_{LVD}$ ) or when $V_{DD}$ becomes $V_{LVD}$ or higher ( $V_{DD} \geq V_{LVD}$ ).<br>Releases the reset signal when $V_{DD} \geq V_{LVD}$ at power on. |

While the voltage detector is operating, whether the supply voltage or the input voltage from an external input pin is more than or less than the detection level can be checked by reading the voltage detection flag (LVIF: bit 0 of the voltage detection register (LVIM)).

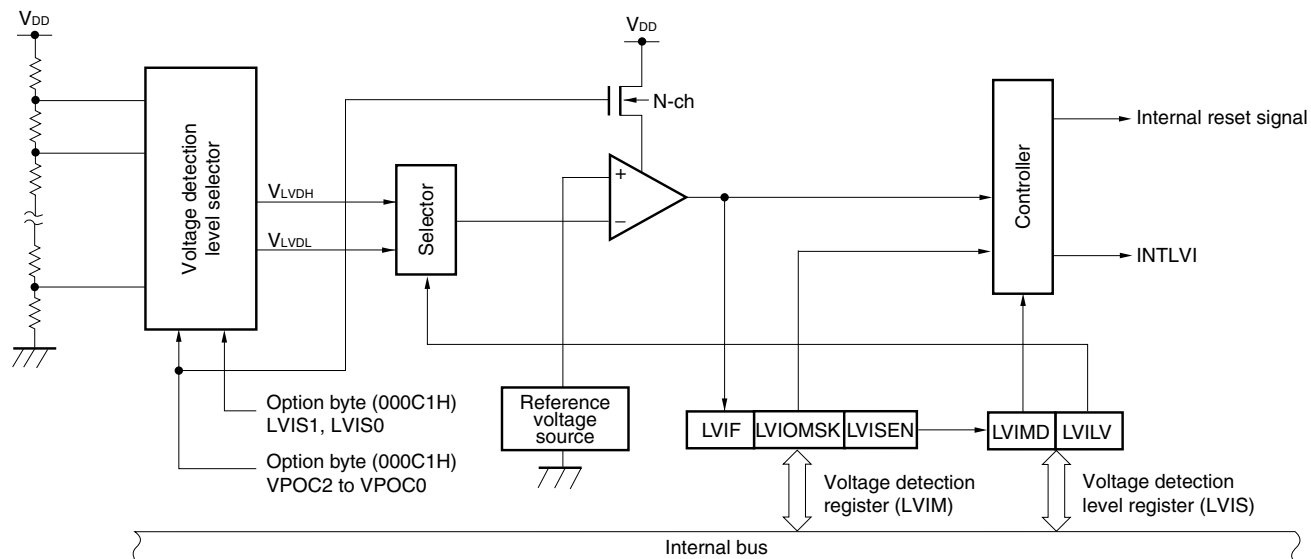
Bit 0 (LVIRF) of the reset control flag register (RESF) is set to 1 if reset occurs. For details of the RESF register, see **CHAPTER 20 RESET FUNCTION**.

## 22.2 Configuration of Voltage Detector

The block diagram of the voltage detector is shown in Figure 22-1.

<R>

Figure 22-1. Block Diagram of Voltage Detector



## 22.3 Registers Controlling Voltage Detector

The voltage detector is controlled by the following registers.

- Voltage detection register (LVIM)
- Voltage detection level register (LVIS)

### 22.3.1 Voltage detection register (LVIM)

This register is used to specify whether to enable or disable rewriting the voltage detection level register (LVIS), as well as to check the LVD output mask status.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 22-2. Format of Voltage Detection Register (LVIM)**

Address: FFFA9H    After reset: 00H <sup>Note 1</sup>    R/W <sup>Note 2</sup>

| Symbol | <7>    | 6 | 5 | 4 | 3 | 2 | <1>     | <0>  |
|--------|--------|---|---|---|---|---|---------|------|
| LVIM   | LVISEN | 0 | 0 | 0 | 0 | 0 | LVIOMSK | LVIF |

|        |                                                                                                     |
|--------|-----------------------------------------------------------------------------------------------------|
| LVISEN | Specification of whether to enable or disable rewriting the voltage detection level register (LVIS) |
| 0      | Disabling rewriting                                                                                 |
| 1      | Enabling rewriting <sup>Note 3</sup>                                                                |

|         |                                 |
|---------|---------------------------------|
| LVIOMSK | Mask status flag of LVD output  |
| 0       | Mask is invalid                 |
| 1       | Mask is valid <sup>Note 4</sup> |

|      |                                                                                                       |
|------|-------------------------------------------------------------------------------------------------------|
| LVIF | Voltage detection flag                                                                                |
| 0    | Supply voltage ( $V_{DD}$ ) $\geq$ detection voltage ( $V_{LVD}$ ), or when LVD operation is disabled |
| 1    | Supply voltage ( $V_{DD}$ ) $<$ detection voltage ( $V_{LVD}$ )                                       |

**Notes** 1. The reset value changes depending on the reset source.

<R> If the LVIS register is reset by LVD, it is not reset but holds the current value. In other reset, LVISEN is cleared to 0.

2. Bits 0 and 1 are read-only.

3. This can only be set when LVIMDS1 and LVIMDS0 are set to 1 and 0 (interrupt and reset mode) by the option byte (in the other mode is invalid)..

<R>

4. LVIOMSK bit is automatically set to "1" in the following periods and reset or interruption by LVD is masked.

- Period during LVISEN = 1
- Waiting period from the time when LVD interrupt is generated until LVD detection voltage becomes stable
- Waiting period from the time when the value of LVILV bit changes until LVD detection voltage becomes stable

### 22.3.2 Voltage detection level register (LVIS)

This register selects the voltage detection level.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation input sets this register to 00H/01H/81H <sup>Note1</sup>.

**Figure 22-3. Format of Voltage Detection Level Select Register (LVIS)**

|          |        |              |                               |     |   |   |   |       |  |  |
|----------|--------|--------------|-------------------------------|-----|---|---|---|-------|--|--|
| Address: | FFFAAH | After reset: | 00H/01H/81H <sup>Note 1</sup> | R/W |   |   |   |       |  |  |
| Symbol   | <7>    | 6            | 5                             | 4   | 3 | 2 | 1 | <0>   |  |  |
| LVIS     | LVIMD  | 0            | 0                             | 0   | 0 | 0 | 0 | LVILV |  |  |

|                         |                                     |
|-------------------------|-------------------------------------|
| LVIMD <sup>Note 2</sup> | Operation mode of voltage detection |
| 0                       | Interrupt mode                      |
| 1                       | Reset mode                          |

|                         |                                                                      |
|-------------------------|----------------------------------------------------------------------|
| LVILV <sup>Note 2</sup> | LVD detection level                                                  |
| 0                       | High-voltage detection level (V <sub>LVDH</sub> )                    |
| 1                       | Low-voltage detection level (V <sub>LVDL</sub> or V <sub>LVD</sub> ) |

**Notes 1.** The reset value changes depending on the reset source and the setting of the option byte.

This register is not cleared (00H) by LVD reset.

The generation of reset signal other than an LVD reset sets as follows.

- When option byte LVIMDS1, LVIMDS0 = 1, 0: 00H
- When option byte LVIMDS1, LVIMDS0 = 1, 1: 81H
- When option byte LVIMDS1, LVIMDS0 = 0, 1: 01H

2. Writing "0" can only be allowed when LVIMDS1 and LVIMDS0 are set to 1 and 0 (interrupt and reset mode) by the option byte. In other cases, writing is not allowed and the value is switched automatically when reset or interrupt is generated.

**Cautions 1.** Only rewrite the value of the LVIS register after setting the LVISEN bit (bit 7 of the LVIM register) to 1.

2. Specify the LVD operation mode and detection voltage (V<sub>LVDH</sub>, V<sub>LVDL</sub>) by using the option byte (000C1H). Table 22-1 shows the option byte (000C1H) settings. For details about the option byte, see **CHAPTER 25 OPTION BYTE**.

<R> **Table 22-1. LVD Operation Mode and Detection Voltage Settings for User Option Byte (000C1H) (1/2)**

Address: 000C1H

|       |       |       |   |       |       |         |         |
|-------|-------|-------|---|-------|-------|---------|---------|
| 7     | 6     | 5     | 4 | 3     | 2     | 1       | 0       |
| VPOC2 | VPOC1 | VPOC0 | 1 | LVIS1 | LVIS0 | LVIMDS1 | LVIMDS0 |

## • LVD setting (interrupt &amp; reset mode)

| Detection voltage |              |              | Option byte Setting Value |         |       |       |       |       |       |
|-------------------|--------------|--------------|---------------------------|---------|-------|-------|-------|-------|-------|
| VLVDH             |              | VLVDL        | Mode setting              |         | VPOC2 | VPOC1 | VPOC0 | LVIS1 | LVIS0 |
| Rising edge       | Falling edge | Falling edge | LVIMDS1                   | LVIMDS0 |       |       |       |       |       |
| 1.77 V            | 1.73 V       | 1.63 V       | 1                         | 0       | 0     | 0     | 0     | 1     | 0     |
| 1.88 V            | 1.84 V       |              |                           |         |       |       |       | 0     | 1     |
| 2.92 V            | 2.86 V       |              |                           |         |       |       |       | 0     | 0     |
| 1.98 V            | 1.94 V       | 1.84 V       |                           |         | 0     | 0     | 1     | 1     | 0     |
| 2.09 V            | 2.04 V       |              |                           |         |       |       |       | 0     | 1     |
| 3.13 V            | 3.06 V       |              |                           |         |       |       |       | 0     | 0     |
| 2.61 V            | 2.55 V       | 2.45 V       |                           |         | 0     | 1     | 0     | 1     | 0     |
| 2.71 V            | 2.65 V       |              |                           |         |       |       |       | 0     | 1     |
| 3.75 V            | 3.67 V       |              |                           |         |       |       |       | 0     | 0     |
| 2.92 V            | 2.86 V       | 2.75 V       |                           |         | 0     | 1     | 1     | 1     | 0     |
| 3.02 V            | 2.96 V       |              |                           |         |       |       |       | 0     | 1     |
| 4.06 V            | 3.98 V       |              |                           |         |       |       |       | 0     | 0     |
| Other than above  |              |              | Setting prohibited        |         |       |       |       |       |       |

## • LVD setting (reset mode)

| Detection voltage |              | Option byte Setting Value |         |       |       |       |       |       |
|-------------------|--------------|---------------------------|---------|-------|-------|-------|-------|-------|
| V <sub>LVD</sub>  |              | Mode setting              |         | VPOC2 | VPOC1 | VPOC0 | LVIS1 | LVIS0 |
| Rising edge       | Falling edge | LVIMDS1                   | LVIMDS0 |       |       |       |       |       |
| 1.67 V            | 1.63 V       | 1                         | 1       | 0     | 0     | 0     | 1     | 1     |
| 1.77 V            | 1.73 V       |                           |         | 0     | 0     | 0     | 1     | 0     |
| 1.88 V            | 1.84 V       |                           |         | 0     | 0     | 1     | 1     | 1     |
| 1.98 V            | 1.94 V       |                           |         | 0     | 0     | 1     | 1     | 0     |
| 2.09 V            | 2.04 V       |                           |         | 0     | 0     | 1     | 0     | 1     |
| 2.50 V            | 2.45 V       |                           |         | 0     | 1     | 0     | 1     | 1     |
| 2.61 V            | 2.55 V       |                           |         | 0     | 1     | 0     | 1     | 0     |
| 2.71 V            | 2.65 V       |                           |         | 0     | 1     | 0     | 0     | 1     |
| 2.81 V            | 2.75 V       |                           |         | 0     | 1     | 1     | 1     | 1     |
| 2.92 V            | 2.86 V       |                           |         | 0     | 1     | 1     | 1     | 0     |
| 3.02 V            | 2.96 V       |                           |         | 0     | 1     | 1     | 0     | 1     |
| 3.13 V            | 3.06 V       |                           |         | 0     | 0     | 1     | 0     | 0     |
| 3.75 V            | 3.67 V       |                           |         | 0     | 1     | 0     | 0     | 0     |
| 4.06 V            | 3.98 V       |                           |         | 0     | 1     | 1     | 0     | 0     |
| Other than above  |              | Setting prohibited        |         |       |       |       |       |       |

**Caution** Be sure to set bit 4 to "1".



<R> **Table 22-1. LVD Operation Mode and Detection Voltage Settings for User Option Byte (000C1H) (2/2)**

Address: 000C1H

|       |       |       |   |       |       |         |         |
|-------|-------|-------|---|-------|-------|---------|---------|
| 7     | 6     | 5     | 4 | 3     | 2     | 1       | 0       |
| VPOC2 | VPOC1 | VPOC0 | 1 | LVIS1 | LVIS0 | LVIMDS1 | LVIMDS0 |

## • LVD setting (interrupt mode)

| Detection voltage |              | Option byte Setting Value |         |       |       |       |       |       |
|-------------------|--------------|---------------------------|---------|-------|-------|-------|-------|-------|
| V <sub>LVD</sub>  |              | Mode setting              |         | VPOC2 | VPOC1 | VPOC0 | LVIS1 | LVIS0 |
| Rising edge       | Falling edge | LVIMDS1                   | LVIMDS0 |       |       |       |       |       |
| 1.67 V            | 1.63 V       | 0                         | 1       | 0     | 0     | 0     | 1     | 1     |
| 1.77 V            | 1.73 V       |                           |         | 0     | 0     | 0     | 1     | 0     |
| 1.88 V            | 1.84 V       |                           |         | 0     | 0     | 1     | 1     | 1     |
| 1.98 V            | 1.94 V       |                           |         | 0     | 0     | 1     | 1     | 0     |
| 2.09 V            | 2.04 V       |                           |         | 0     | 0     | 1     | 0     | 1     |
| 2.50 V            | 2.45 V       |                           |         | 0     | 1     | 0     | 1     | 1     |
| 2.61 V            | 2.55 V       |                           |         | 0     | 1     | 0     | 1     | 0     |
| 2.71 V            | 2.65 V       |                           |         | 0     | 1     | 0     | 0     | 1     |
| 2.81 V            | 2.75 V       |                           |         | 0     | 1     | 1     | 1     | 1     |
| 2.92 V            | 2.86 V       |                           |         | 0     | 1     | 1     | 1     | 0     |
| 3.02 V            | 2.96 V       |                           |         | 0     | 1     | 1     | 0     | 1     |
| 3.13 V            | 3.06 V       |                           |         | 0     | 0     | 1     | 0     | 0     |
| 3.75 V            | 3.67 V       |                           |         | 0     | 1     | 0     | 0     | 0     |
| 4.06 V            | 3.98 V       |                           |         | 0     | 1     | 1     | 0     | 0     |
| Other than above  |              | Setting prohibited        |         |       |       |       |       |       |

## • LVD setting (LVDOFF)

| Detection voltage |              | Option byte Setting Value |         |       |       |       |       |       |
|-------------------|--------------|---------------------------|---------|-------|-------|-------|-------|-------|
| V <sub>LVD</sub>  |              | Mode setting              |         | VPOC2 | VPOC1 | VPOC0 | LVIS1 | LVIS0 |
| Rising edge       | Falling edge | LVIMDS1                   | LVIMDS0 |       |       |       |       |       |
| –                 | –            | 0/1                       | 1       | 1     | ×     | ×     | ×     | ×     |
| Other than above  |              | Setting prohibited        |         |       |       |       |       |       |

**Cautions** 1. Be sure to set bit 4 to “1”.

2. When the LVD circuit is off, use the external reset pin to execute a reset.

**Remark** ×: don't care

## 22.4 Operation of Voltage Detector

### 22.4.1 When used as reset mode

- When starting operation

Start in the following initial setting state.

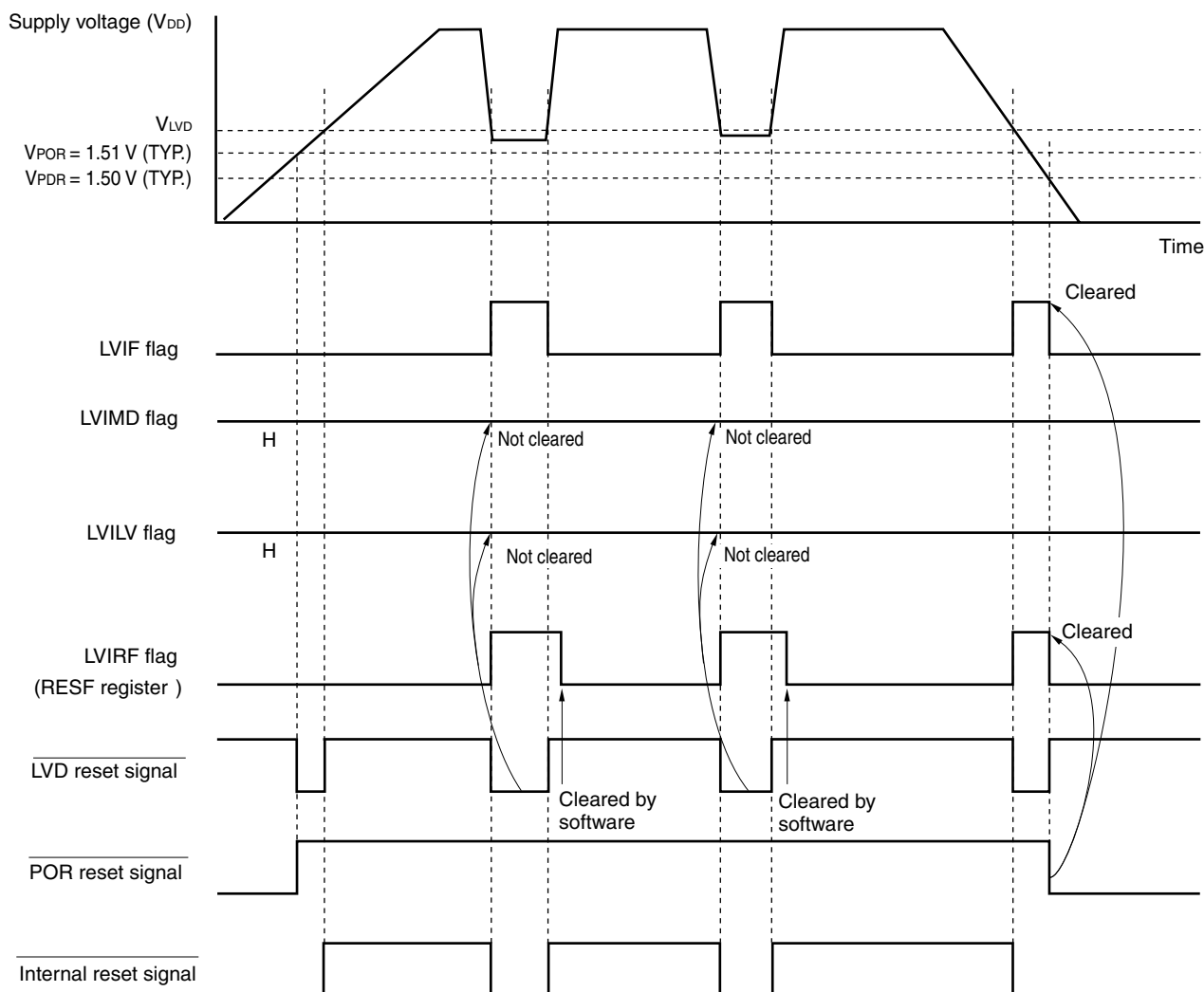
Specify the operation mode (the reset mode (LVIMDS1, LVIMDS0 = 1, 1)) and the detection voltage ( $V_{LVD}$ ) by using the option byte 000C1H.

- Set bit 7 (LVISEN) of the voltage detection register (LVIM) to 0 (disable rewriting of voltage detection level register (LVIS))
- When the option byte LVIMDS1 and LVIMDS0 are set to 1, the initial value of the LVIS register is set to 81H.
  - Bit 7 (LVIMD) is 1 (reset mode).
  - Bit 0 (LVILV) is 1 (low-voltage detection level:  $V_{LVDL}$  or  $V_{LVD}$ ).

<R>

Figure 22-4 shows the timing of the internal reset signal generated by the voltage detector.

**Figure 22-4. Timing of Voltage Detector Internal Reset Signal Generation**  
**(Option Byte LVIMDS1, LVIMDS0 = 1, 1)**



**Remark**  $V_{POR}$ : POR power supply rise detection voltage  
 $V_{PDR}$ : POR power supply fall detection voltage

### 22.4.2 When used as interrupt mode

- When starting operation

Specify the operation mode (the interrupt mode (LVIMDS1, LVIMDS0 = 0, 1)) and the detection voltage (V<sub>LVD</sub>) by using the option byte 000C1H.

Start in the following initial setting state.

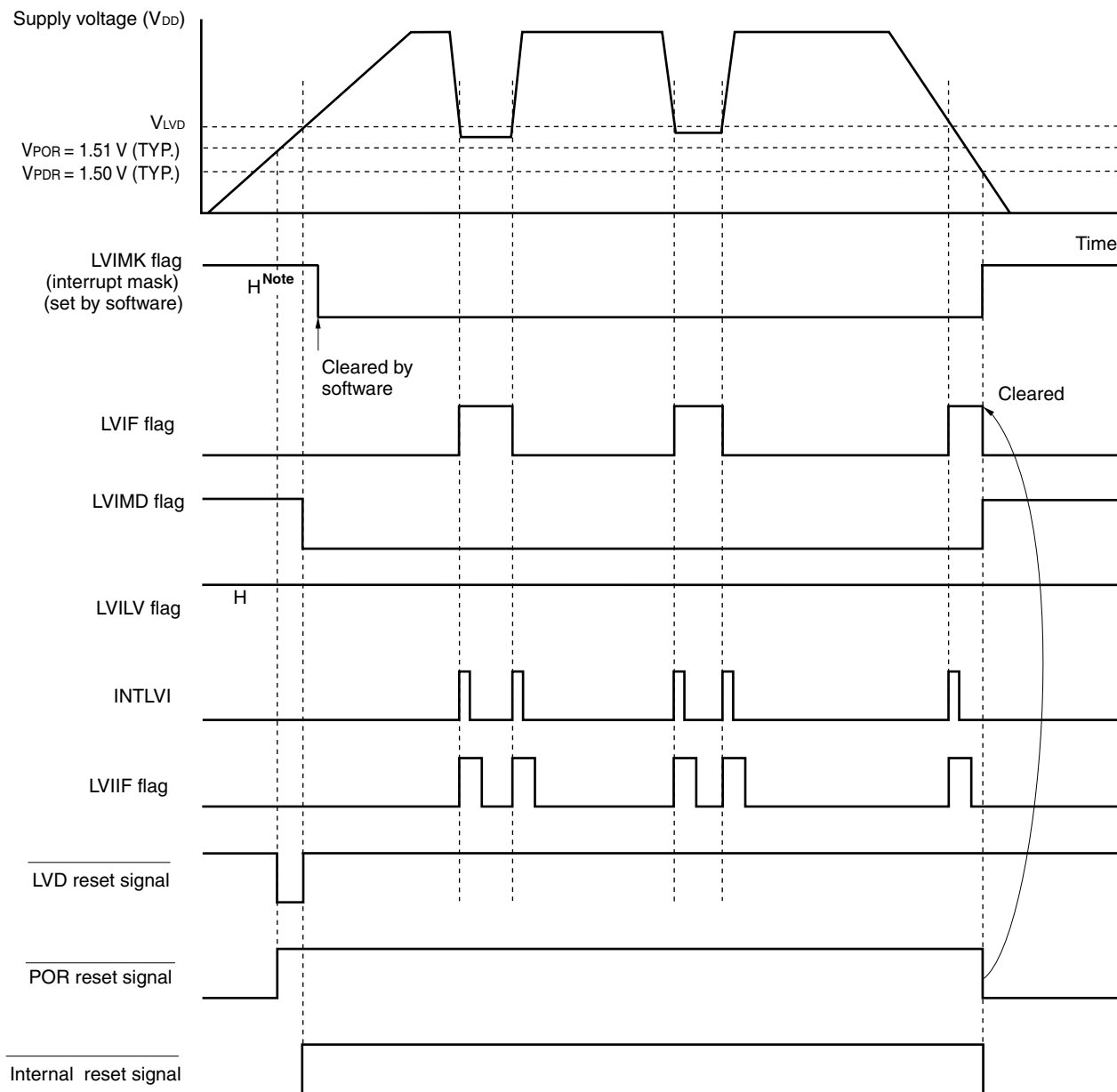
- Set bit 7 (LVISEN) of the voltage detection register (LVIM) to 0 (disable rewriting of voltage detection level register (LVIS))
- When the option byte LVIMDS1 is clear to 0 and LVIMDS0 is set to 1, the initial value of the LVIS register is set to 00H.

Bit 7 (LVIMD) is 0 (interrupt mode).

<R> Bit 0 (LVILV) is 1 (low-voltage detection level: V<sub>LVDL</sub> or V<sub>LVD</sub>).

Figure 22-5 shows the timing of the internal interrupt signal generated by the voltage detector.

**Figure 22-5. Timing of Voltage Detector Internal Interrupt Signal Generation**  
 (Option Byte LVIMDS1, LVIMDS0 = 0, 1)



**Note** The LVIMK flag is set to "1" by reset signal generation.

**Remark**  $V_{POR}$ : POR power supply rise detection voltage  
 $V_{PDR}$ : POR power supply fall detection voltage

### 22.4.3 When used as interrupt and reset mode

- When starting operation

Specify the operation mode (the interrupt and reset (LVIMDS1, LVIMDS0 = 1, 0)) and the detection voltage (VLVDH, VLVDL) by using the option byte 000C1H.

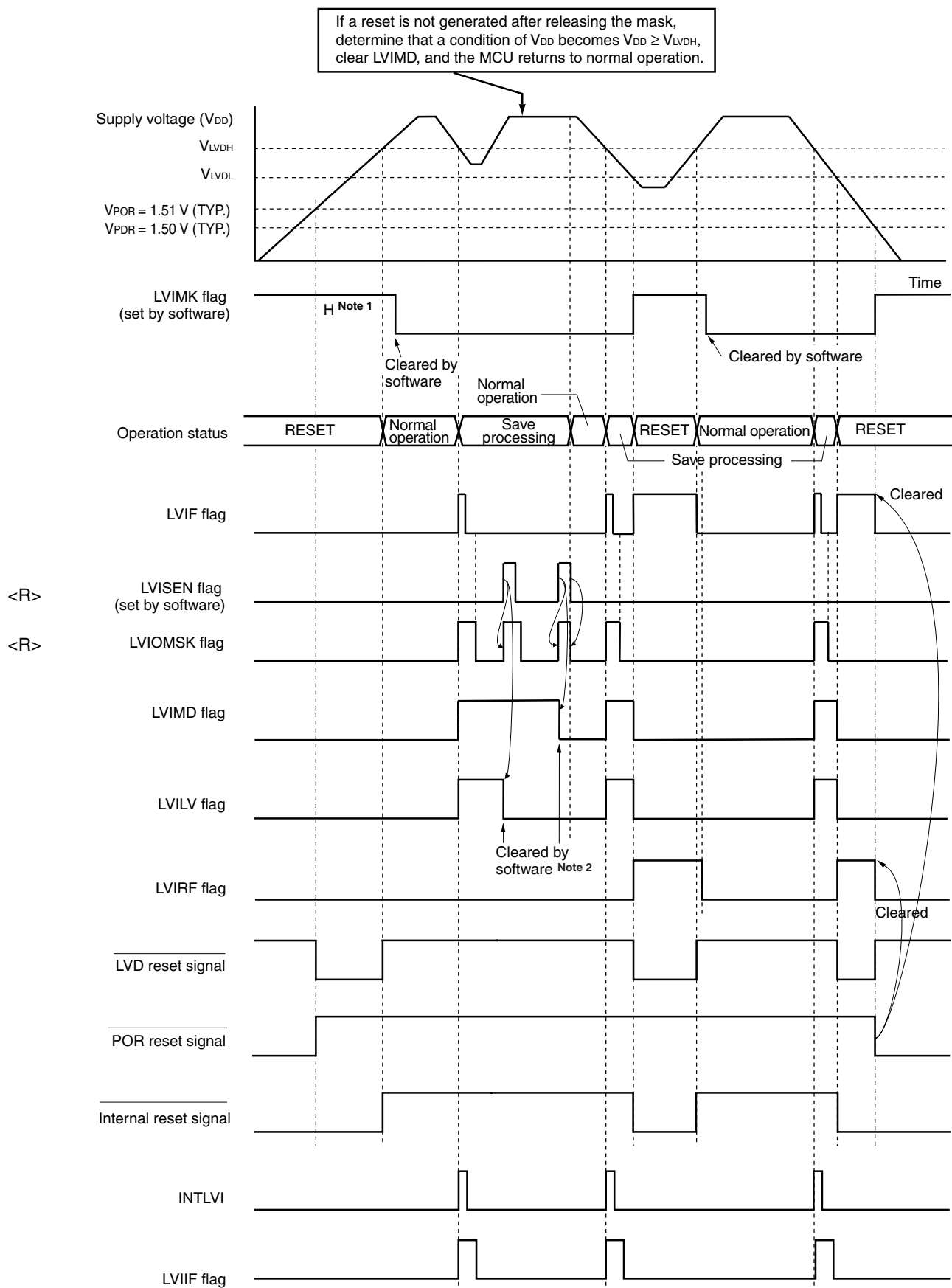
Start in the following initial setting state.

- Set bit 7 (LVISEN) of the voltage detection register (LVIM) to 0 (disable rewriting of voltage detection level register (LVIS))
- When the option byte LVIMDS1 is set to 1 and LVIMDS0 is clear to 0, the initial value of the LVIS register is set to 00H.
  - Bit 7 (LVIMD) is 0 (interrupt mode).
  - Bit 0 (LVILV) is 0 (high-voltage detection level: VLVDH).

Figures 22-6 shows the Timing of Voltage Detector Reset Signal and Interrupt Signal Generation.

<R> Perform the processing according to **Figure 22-7. Processing Procedure After an Interrupt Is Generated in interrupt and reset mode.**

**Figure 22-6. Timing of Voltage Detector Reset Signal and Interrupt Signal Generation  
(Option Byte LVIMDS1, LVIMDS0 = 1, 0) (1/2)**



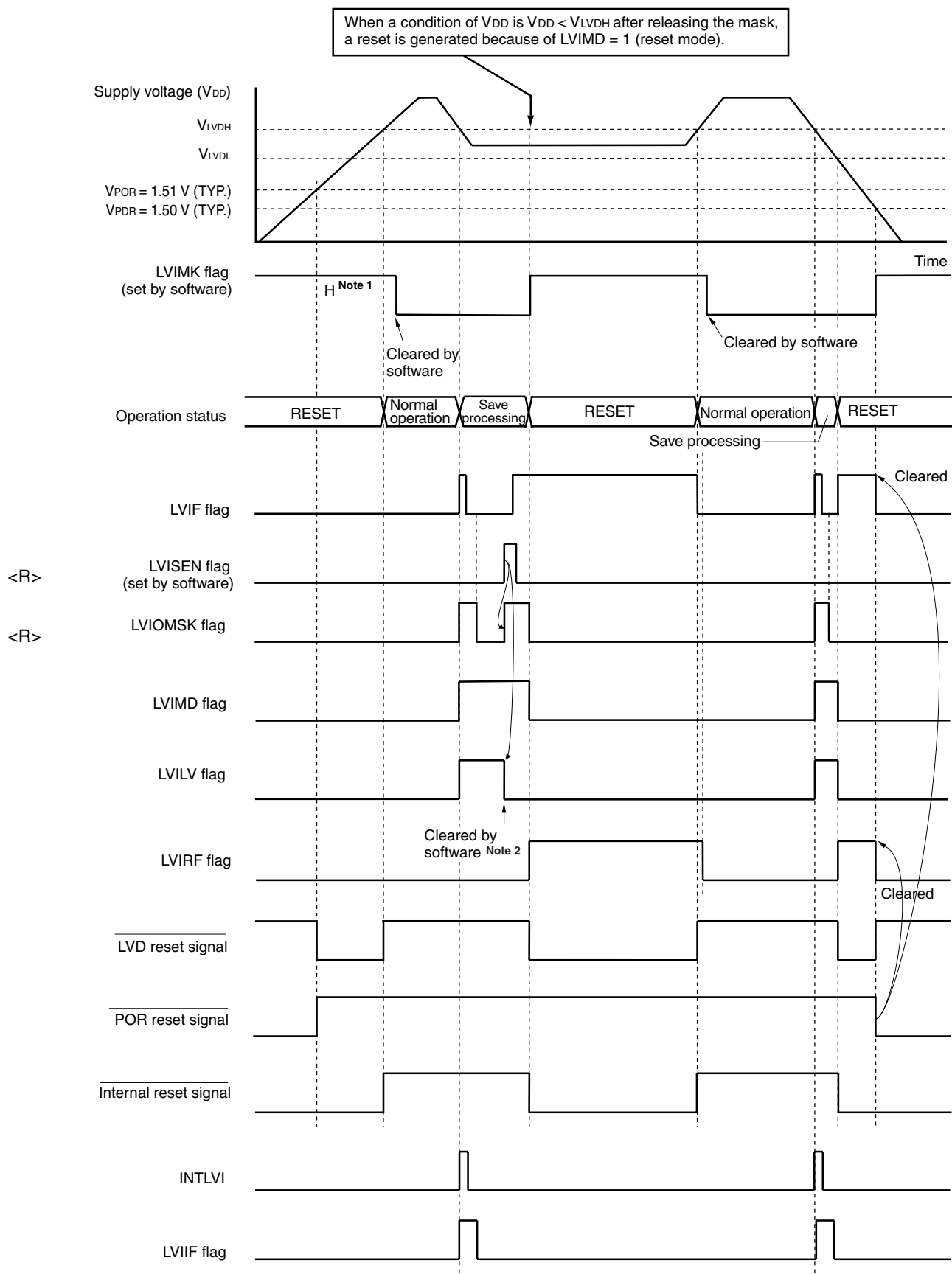
(Notes and Remark are listed on the next page.)

- <R> **Notes**
1. The LVIMK flag is set to “1” by reset signal generation.
  2. After an interrupt is generated, perform the processing according to **Figure 22-7. Processing Procedure After an Interrupt Is Generated in interrupt and reset mode.**

**Remark**  $V_{POR}$ : POR power supply rise detection voltage  
 $V_{PDR}$ : POR power supply fall detection voltage



**Figure 22-6. Timing of Voltage Detector Reset Signal and Interrupt Signal Generation  
(Option Byte LVIMDS1, LVIMDS0 = 1, 0) (2/2)**



(Notes and Remark are listed on the next page.)

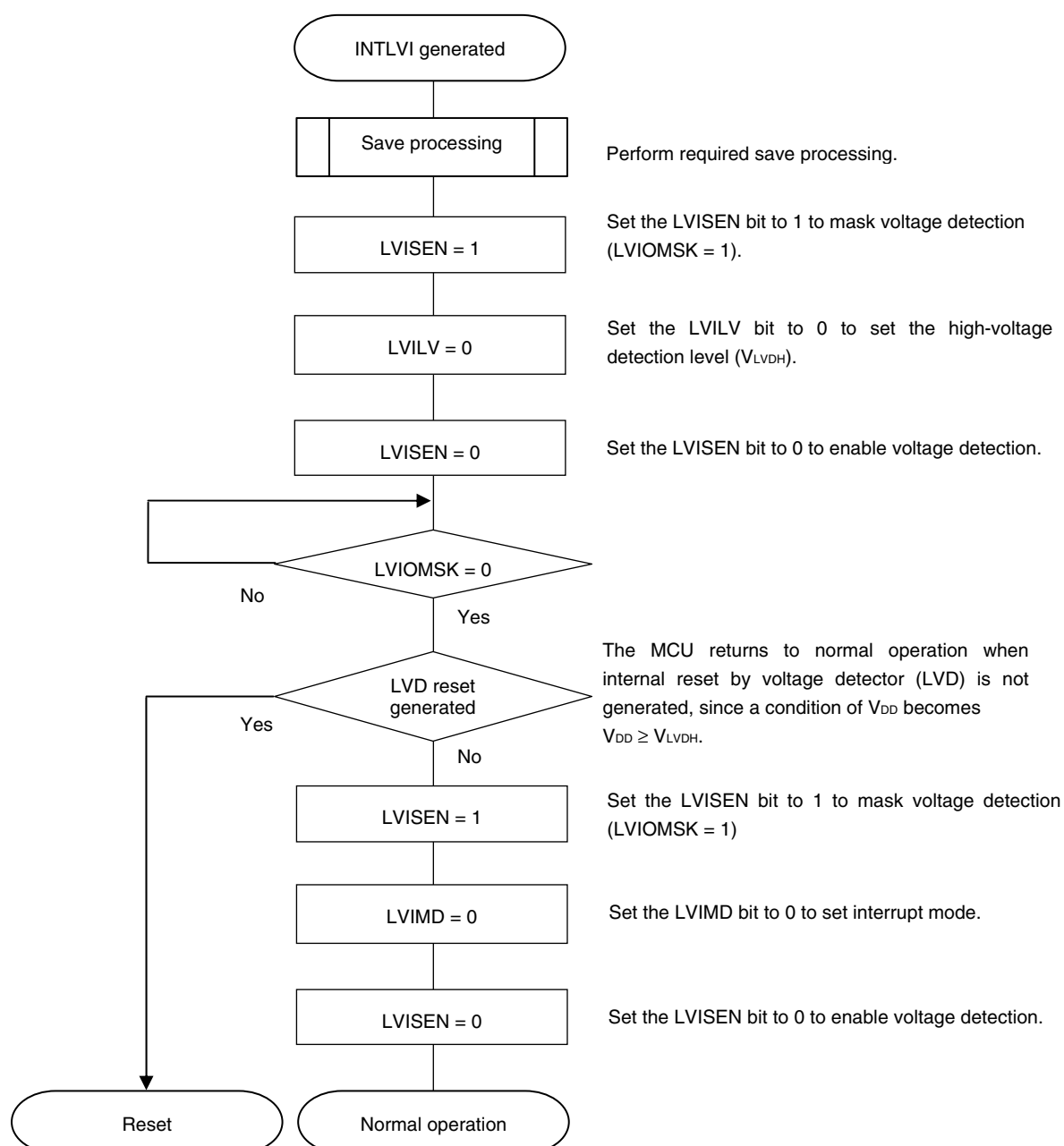
**Notes** 1. The LVIMK flag is set to "1" by reset signal generation.

<R> 2. After an interrupt is generated, perform the processing according to **Figure 22-7. Processing Procedure After an Interrupt Is Generated in interrupt and reset mode.**

**Remark**  $V_{POR}$ : POR power supply rise detection voltage

$V_{PDR}$ : POR power supply fall detection voltage

**Figure 22-7. Processing Procedure After an Interrupt Is Generated in interrupt and reset mode**

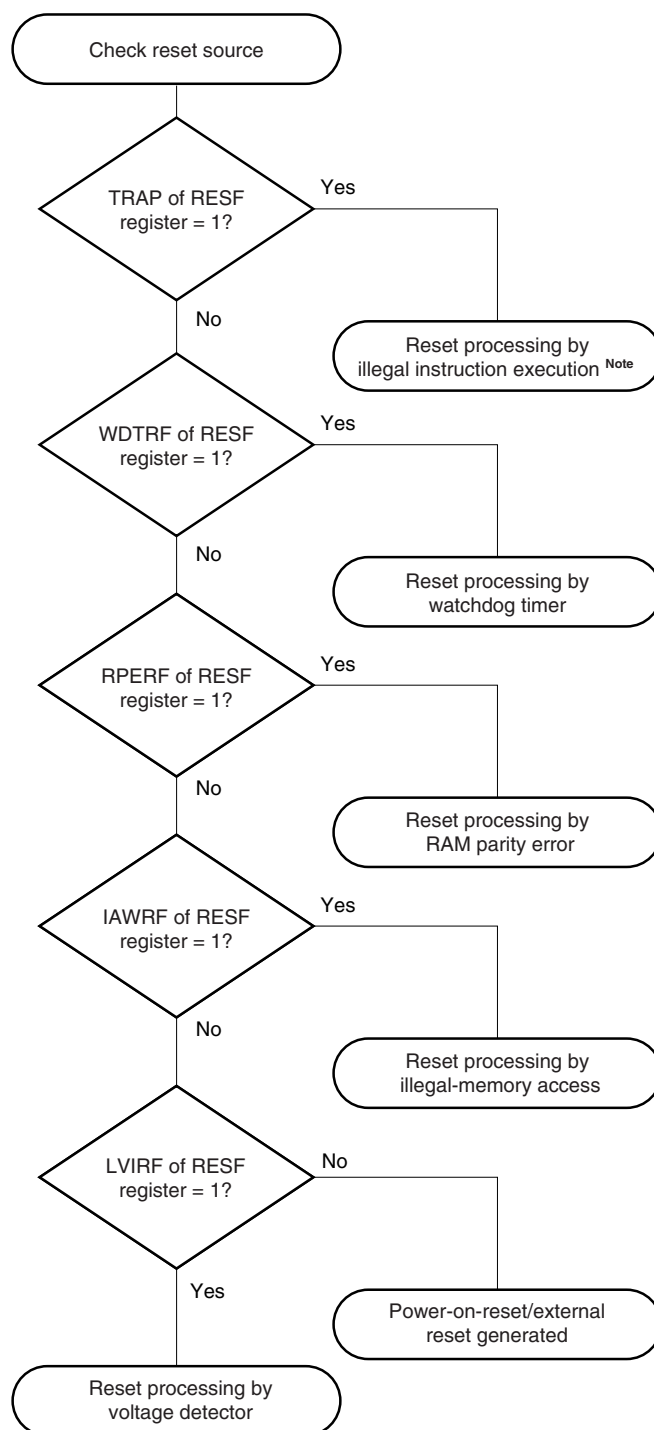


## 22.5 Cautions for Voltage Detector

### (1) Checking reset source

When a reset occurs, check the reset source by using the following method.

**Figure 22-8. Checking reset source**



**Note** When instruction code FFH is executed.

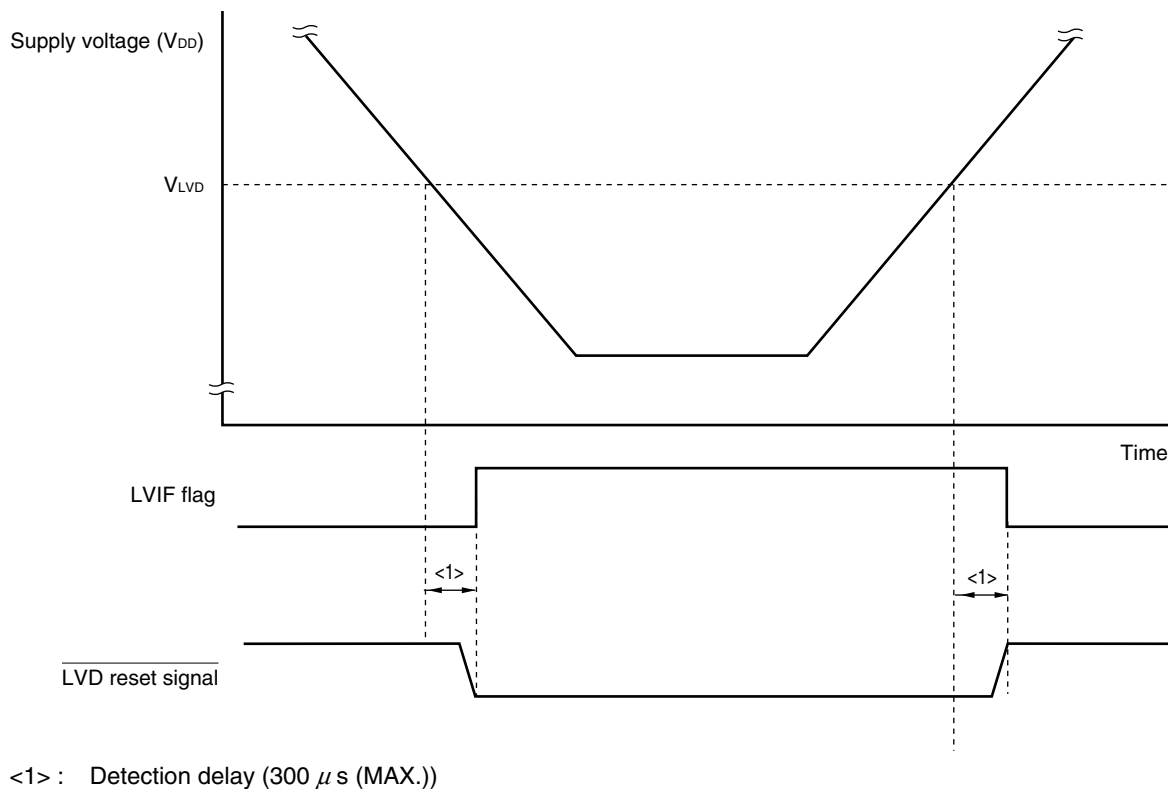
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

**(2) Delay from the time LVD reset source is generated until the time LVD reset has been generated or released**

There is some delay from the time supply voltage ( $V_{DD}$ ) < LVD detection voltage ( $V_{LVD}$ ) until the time LVD reset has been generated.

In the same way, there is also some delay from the time LVD detection voltage ( $V_{LVD}$ )  $\leq$  supply voltage ( $V_{DD}$ ) until the time LVD reset has been released (see **Figure 22-9**).

**Figure 22-9. Delay from the time LVD reset source is generated until the time LVD reset has been generated or released**



## CHAPTER 23 SAFETY FUNCTIONS

### 23.1 Overview of Safety Functions

The following safety functions are provided in the RL78/L12 to comply with the IEC60730 and IEC61508 safety standards.

These functions enable the microcontroller to self-diagnose abnormalities and stop operating if an abnormality is detected.

#### (1) Flash memory CRC operation function (high-speed CRC, general-purpose CRC)

This detects data errors in the flash memory by performing CRC operations.

Two CRC functions are provided in the RL78/L12 that can be used according to the application or purpose of use.

- High-speed CRC: The CPU can be stopped and a high-speed check executed on its entire code flash memory area during the initialization routine.
- General CRC: This can be used for checking various data in addition to the code flash memory area while the CPU is running.

**Caution** The high-speed CRC function cannot be used in products with an 8 KB code flash memory (R5F10RB8, R5F10RF8, R5F10RG8, and R5F10RJ8).

#### (2) RAM parity error detection function

This detects parity errors when reading RAM data..

#### (3) RAM guard function

This prevents RAM data from being rewritten when the CPU freezes.

#### (4) SFR guard function

This prevents SFRs from being rewritten when the CPU freezes.

#### (5) Invalid memory access detection function

This detects illegal accesses to invalid memory areas (such as areas where no memory is allocated and areas to which access is restricted).

#### (6) Frequency detection function

This uses TAU to detect the oscillation frequency.

#### (7) A/D test function

This is used to perform a self-check of A/D conversion by performing A/D conversion on the internal reference voltage.

<R> **Remark** See the application note (R01AN0749) for the features required to comply with the IEC60730 standards.

## 23.2 Registers Used by Safety Functions

The safety functions use the following registers for each function.

| Register                                                                                                                                                   | Each Function of Safety Function                     |
|------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------|
| <ul style="list-style-type: none"> <li>Flash memory CRC control register (CRC0CTL)</li> <li>Flash memory CRC operation result register (PGCRCL)</li> </ul> | Flash memory CRC operation function (high-speed CRC) |
| <ul style="list-style-type: none"> <li>CRC input register (CRCIN)</li> <li>CRC data register (CRCD)</li> </ul>                                             | CRC operation function (general-purpose CRC)         |
| <ul style="list-style-type: none"> <li>RAM parity error control register (RPECTL)</li> </ul>                                                               | RAM parity error detection function                  |
| <ul style="list-style-type: none"> <li>Invalid memory access detection control register (IAWCTL)</li> </ul>                                                | RAM guard function                                   |
|                                                                                                                                                            | SFR guard function                                   |
|                                                                                                                                                            | Invalid memory access detection function             |
| <ul style="list-style-type: none"> <li>Timer input select register 0 (TIS0)</li> </ul>                                                                     | Frequency detection function                         |
| <ul style="list-style-type: none"> <li>A/D test register (ADTES)</li> </ul>                                                                                | A/D test function                                    |

The content of each register is described in **23.3 Operation of Safety Functions**.

## 23.3 Operation of Safety Functions

### 23.3.1 Flash memory CRC operation function (high-speed CRC)

The IEC60730 standard mandates the checking of data in the flash memory, and recommends using CRC to do it. The high-speed CRC provided in the RL78/L12 can be used to check the entire code flash memory area during the initialization routine. The high-speed CRC can be executed only when the program is allocated on the RAM and in the HALT mode of the main system clock.

- <R> The high-speed CRC performs an operation by reading 32-bit data per clock from the flash memory while stopping the CPU. This function therefore can finish a check in a shorter time (for example, 512  $\mu$ s@24 MHz with 64-KB flash memory). The CRC generator polynomial used complies with “ $X^{16} + X^{12} + X^5 + 1$ ” of CRC-16-CCITT. The high-speed CRC operates in MSB first order from bit 31 to bit 0.

**Cautions 1. The high-speed CRC function cannot be used in products with an 8 KB code flash memory (R5F10RB8, R5F10RF8, R5F10RG8, and R5F10RJ8).**

- <R> **2. The CRC operation result might differ during on-chip debugging because the monitor program is allocated.**

**Remark** The operation result is different between the high-speed CRC and the general CRC, because the general CRC operates in LSB first order.

### 23.3.1.1 Flash memory CRC control register (CRC0CTL)

This register is used to control the operation of the high-speed CRC ALU, as well as to specify the operation range.

The CRC0CTL register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 23-1. Format of Flash Memory CRC Control Register (CRC0CTL)**

Address: F02F0H After reset: 00H R/W

|         |        |   |      |      |      |      |      |      |
|---------|--------|---|------|------|------|------|------|------|
| Symbol  | <7>    | 6 | 5    | 4    | 3    | 2    | 1    | 0    |
| CRC0CTL | CRC0EN | 0 | FEA5 | FEA4 | FEA3 | FEA2 | FEA1 | FEA0 |

|        |                                                              |
|--------|--------------------------------------------------------------|
| CRC0EN | Control of CRC ALU operation                                 |
| 0      | Stop the operation.                                          |
| 1      | Start the operation according to HALT instruction execution. |

|                      |      |      |      |      |      |                                  |
|----------------------|------|------|------|------|------|----------------------------------|
| FEA5                 | FEA4 | FEA3 | FEA2 | FEA1 | FEA0 | High-speed CRC operation range   |
| 0                    | 0    | 0    | 0    | 0    | 0    | 0000H to 3FFBH (16 K to 4 bytes) |
| 0                    | 0    | 0    | 0    | 0    | 1    | 0000H to 7FFBH (32 K to 4 bytes) |
| Other than the above |      |      |      |      |      | Setting prohibited               |

**Remark** Input the expected CRC operation result value to be used for comparison in the lowest 4 bytes of the flash memory. Note that the operation range will thereby be reduced by 4 bytes.

### 22.3.1.2 Flash memory CRC operation result register (PGCRCL)

This register is used to store the high-speed CRC operation results.

The PGCRCL register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

**Figure 23-2. Format of Flash Memory CRC Operation Result Register (PGCRCL)**

Address: F02F2H    After reset: 0000H    R/W

|        |                   |         |                                             |         |         |         |        |        |
|--------|-------------------|---------|---------------------------------------------|---------|---------|---------|--------|--------|
| Symbol | 15                | 14      | 13                                          | 12      | 11      | 10      | 9      | 8      |
| PGCRCL | PGCRC15           | PGCRC14 | PGCRC13                                     | PGCRC12 | PGCRC11 | PGCRC10 | PGCRC9 | PGCRC8 |
|        | 7                 | 6       | 5                                           | 4       | 3       | 2       | 1      | 0      |
|        | PGCRC7            | PGCRC6  | PGCRC5                                      | PGCRC4  | PGCRC3  | PGCRC2  | PGCRC1 | PGCRC0 |
|        | PGCRC15 to PGCRC0 |         | High-speed CRC operation results            |         |         |         |        |        |
|        | 0000H to FFFFH    |         | Store the high-speed CRC operation results. |         |         |         |        |        |

**Caution** The PGCRCL register can only be written if CRC0EN (bit 7 of the CRC0CTL register) = 1.

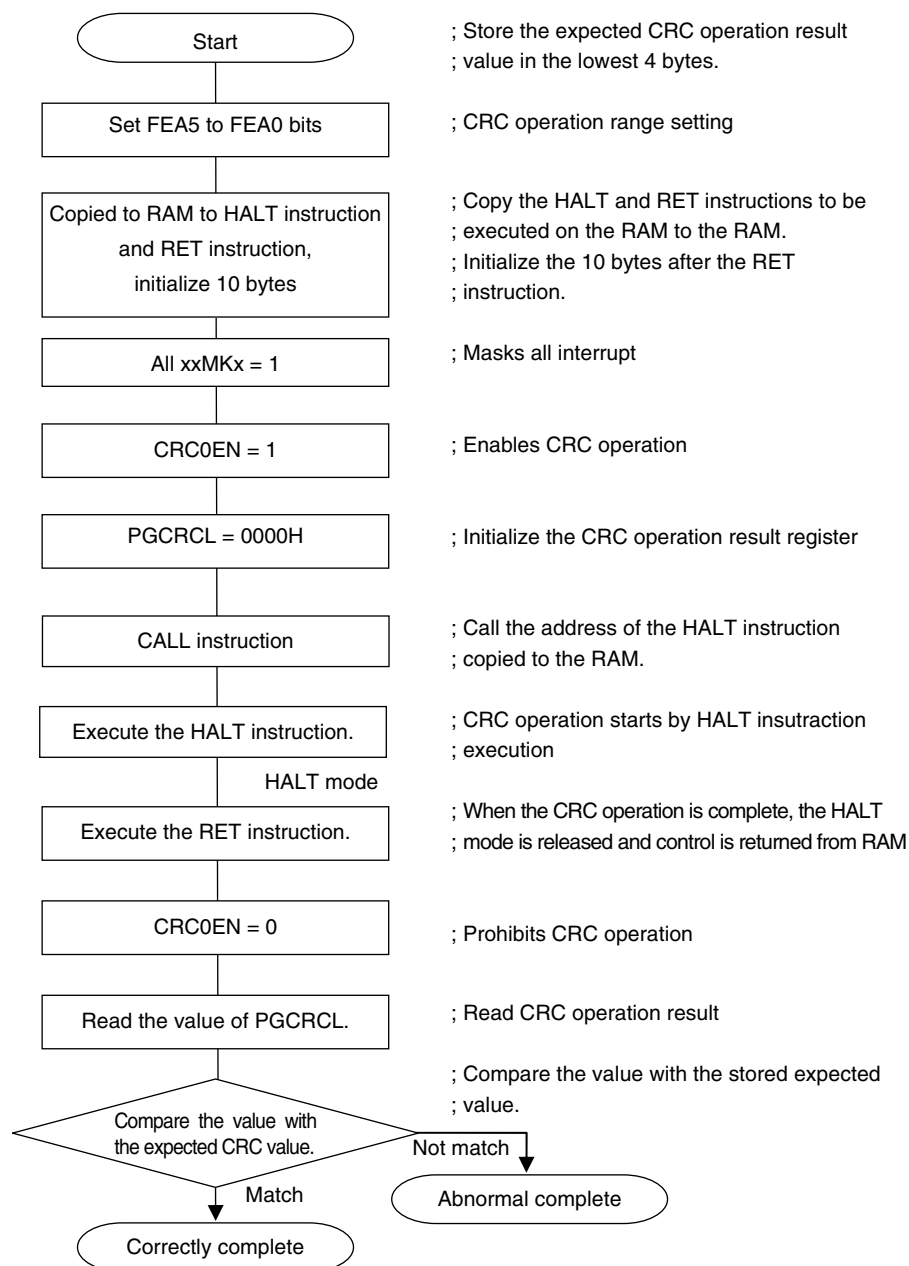
Figure 23-3 shows the flowchart of flash memory CRC operation function (high-speed CRC).



## &lt;Operation flow&gt;

&lt;R&gt;

Figure 23-3. Flowchart of Flash Memory CRC Operation Function (High-speed CRC)



**Cautions 1. The CRC operation is executed only on the code flash.**

**2. Store the expected CRC operation value in the area below the operation range in the code flash.**

**3. The CRC operation is enabled by executing the HALT instruction in the RAM area.**

**Be sure to execute the HALT instruction in RAM area.**

The expected CRC value can be calculated by using tools such as the CubeSuite+ development environment. (See the CubeSuite+ user's manual for details.)

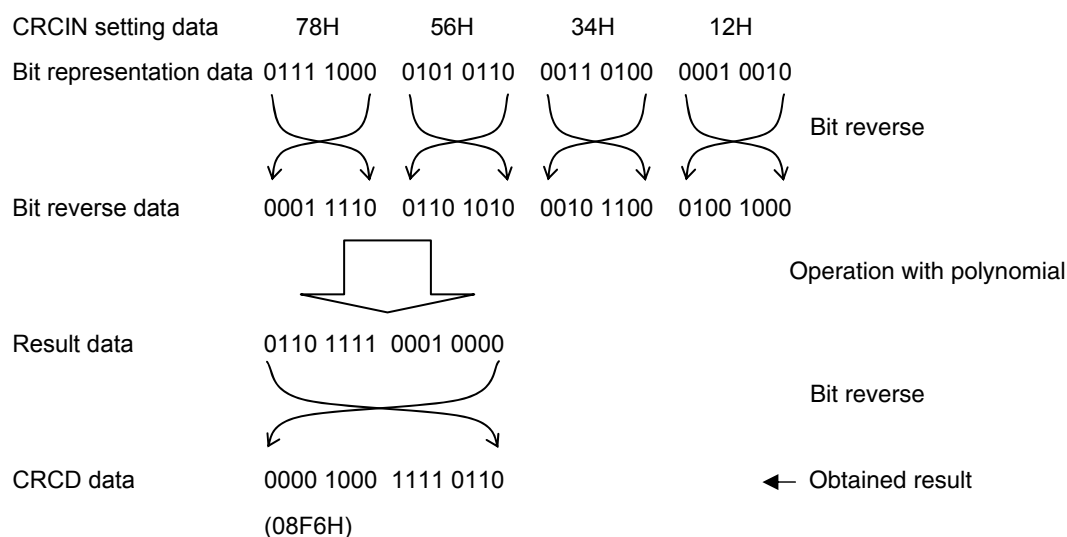
### 23.3.2 CRC operation function (general-purpose CRC)

In order to guarantee safety during operation, the IEC61508 standard mandates the checking of data even while the CPU is operating.

In the RL78/L12, a general CRC operation can be executed as a peripheral function while the CPU is operating. The general CRC can be used for checking various data in addition to the code flash memory area. The data to be checked <R> can be specified by using software (a user-created program). CRC calculation function in the HALT mode can be used only during the DMA transmission.

The general CRC operation can be executed in the main system clock operation mode as well as the subsystem clock operation mode.

The CRC generator polynomial used is " $X^{16} + X^{12} + X^5 + 1$ " of CRC-16-CCITT. The data to be input is inverted in bit order and then calculated to allow for LSB-first communication. For example, if the data 12345678H is sent from the LSB, values are written to the CRCIN register in the order of 78H, 56H, 34H, and 12H, enabling a value of 08F6H to be obtained from the CRCD register. This is the result obtained by executing a CRC operation on the bit rows shown below, which consist of the data 12345678H inverted in bit order.



<R> **Caution** Because the debugger rewrites the software break setting line to a break instruction during program execution, the CRC operation result differs if a software break is set in the CRC operation target area.

#### 23.3.2.1 CRC input register (CRCIN)

CRCIN register is an 8-bit register that is used to set the CRC operation data of general-purpose CRC.

The possible setting range is 00H to FFH.

The CRCIN register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 23-4. Format of CRC Input Register (CRCIN)

Address: FFFACH After reset: 00H R/W

| Symbol      | 7 | 6 | 5 | 4           | 3 | 2 | 1 | 0 |
|-------------|---|---|---|-------------|---|---|---|---|
| CRCIN       |   |   |   |             |   |   |   |   |
| Bits 7 to 0 |   |   |   | Function    |   |   |   |   |
| 00H to FFH  |   |   |   | Data input. |   |   |   |   |

### 23.3.2.2 CRC data register (CRCD)

This register is used to store the CRC operation result of the general-purpose CRC.

The setting range is 0000H to FFFFH.

After 1 clock of CPU/peripheral hardware clock ( $f_{CLK}$ ) has elapsed from the time CRCIN register is written, the CRC operation result is stored to the CRCD register.

The CRCD register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

**Figure 23-5. Format of CRC Data Register (CRCD)**

Address: F02FAH After reset: 0000H R/W

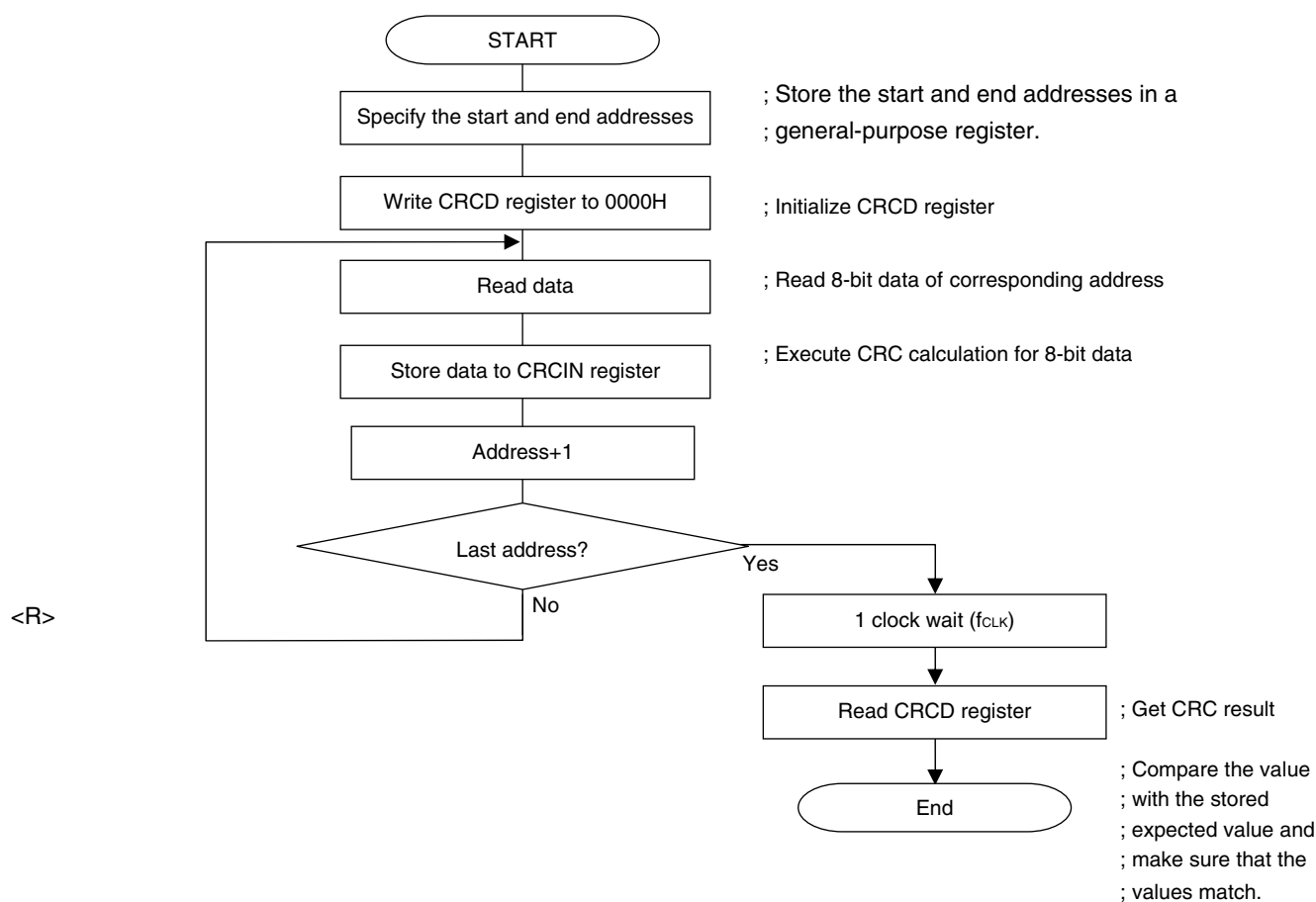
| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| CRCD   |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**Cautions** 1. Read the value written to CRCD register before writing to CRCIN register.

2. If conflict between writing and storing operation result to CRCD register occurs, the writing is ignored.

#### <Operation flow>

**Figure 23-6. CRC Operation Function (General-Purpose CRC)**



### 23.3.3 RAM parity error detection function

The IEC60730 standard mandates the checking of RAM data. A single-bit parity bit is therefore added to all 8-bit data in the RL78/L12's RAM. By using this RAM parity error detection function, the parity bit is appended when data is written, and the parity is checked when the data is read. This function can also be used to trigger a reset when a parity error occurs.

#### 23.3.3.1 RAM parity error control register (RPECTL)

This register is used to control parity error generation check bit and reset generation due to parity errors.

The RPECTL register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 23-7. Format of RAM Parity Error Control Register (RPECTL)**

Address: F00F5H After reset: 00H R/W

| Symbol | <7>     | 6 | 5 | 4 | 3 | 2 | 1 | <0>  |
|--------|---------|---|---|---|---|---|---|------|
| RPECTL | RPERDIS | 0 | 0 | 0 | 0 | 0 | 0 | RPEF |

| RPERDIS | Parity error reset mask flag |
|---------|------------------------------|
| 0       | Enable parity error resets.  |
| 1       | Disable parity error resets. |

| RPEF | Parity error status flag      |
|------|-------------------------------|
| 0    | No parity error has occurred. |
| 1    | A parity error has occurred.  |

**<R> Caution** The parity bit is appended when data is written, and the parity is checked when the data is read. Therefore, while RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize RAM areas where data access is to proceed before reading data.

The RL78's CPU executes look-ahead due to the pipeline operation, the CPU might read an uninitialized RAM area that is allocated beyond the RAM used, which causes a RAM parity error. Therefore, while RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize the RAM area + 10 bytes when instructions are fetched from RAM areas. When using the self-programming function while RAM parity error resets are enabled (RPERDIS = 0), be sure to initialize the RAM area to overwrite + 10 bytes before overwriting.

- Remarks**
1. The RAM parity check is always on, and the result can be confirmed by checking the RPEF flag.
  2. The parity error reset is enabled by default (RPERDIS = 0).  
Even if the parity error reset is disabled (RPERDIS = 1), the RPEF flag will be set (1) if a parity error occurs.
  3. The RPEF flag is set (1) by RAM parity errors and cleared (0) by writing 0 to it or by any reset source.  
When RPEF = 1, the value is retained even if RAM for which no parity error has occurred is read.

### 23.3.4 RAM guard function

In order to guarantee safety during operation, the IEC61508 standard mandates that important data stored in the RAM be protected, even if the CPU freezes.

This RAM guard function is used to protect data in the specified memory space.

If the RAM guard function is specified, writing to the specified RAM space is disabled, but reading from the space can be carried out as usual.

#### 23.3.4.1 Invalid memory access detection control register (IAWCTL)

This register is used to control the detection of invalid memory access and RAM/SFR guard function.

GRAM1 and GRAM0 bits are used in RAM guard function.

The IAWCTL register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 23-8. Format of Invalid Memory Access Detection Control Register (IAWCTL)**

Address: F0078H After reset: 00H R/W

| Symbol | 7     | 6 | 5     | 4     | 3 | 2     | 1    | 0    |
|--------|-------|---|-------|-------|---|-------|------|------|
| IAWCTL | IAWEN | 0 | GRAM1 | GRAM0 | 0 | GPORT | GINT | GCSC |

| GRAM1 | GRAM0 | RAM guard space <sup>Note</sup>           |
|-------|-------|-------------------------------------------|
| 0     | 0     | Disabled. RAM can be written to.          |
| 0     | 1     | The 128 bytes starting at the RAM address |
| 1     | 0     | The 256 bytes starting at the RAM address |
| 1     | 1     | The 512 bytes starting at the RAM address |

**Note** The RAM start address differs depending on the size of the RAM provided with the product.

### 23.3.5 SFR guard function

In order to guarantee safety during operation, the IEC61508 standard mandates that important SFRs be protected from being overwritten, even if the CPU freezes.

This SFR guard function is used to protect data in the control registers used by the port function, interrupt function, clock control function, voltage detection function, and RAM parity error detection function.

If the SFR guard function is specified, writing to the specified SFRs is disabled, but reading from the SFRs can be carried out as usual.

#### 23.3.5.1 Invalid memory access detection control register (IAWCTL)

This register is used to control the detection of invalid memory access and RAM/SFR guard function.

GPORT, GINT and GCSC bits are used in SFR guard function.

The IAWCTL register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 23-9. Format of Invalid Memory Access Detection Control Register (IAWCTL)**

Address: F0078H After reset: 00H R/W

| Symbol | 7     | 6 | 5     | 4     | 3 | 2     | 1    | 0    |
|--------|-------|---|-------|-------|---|-------|------|------|
| IAWCTL | IAWEN | 0 | GRAM1 | GRAM0 | 0 | GPORT | GINT | GCSC |

| GPORT | Control registers of port function guard                                                                                                                                                |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | Disabled. Control registers of port function can be read or written to.                                                                                                                 |
| 1     | Enabled. Writing to control registers of port function is disabled. Reading is enabled.<br>[Guarded SFR] PMxx, PUxx, PIMxx, POMxx, PMCxx, ADPC, PIOR, PFSEGxx, ISCLCD <sup>Note 1</sup> |

| GINT | Registers of interrupt function guard                                                                                              |
|------|------------------------------------------------------------------------------------------------------------------------------------|
| 0    | Disabled. Registers of interrupt function can be read or written to.                                                               |
| 1    | Enabled. Writing to registers of interrupt function is disabled. Reading is enabled.<br>[Guarded SFR] IFxx, MKxx, PRxx, EGPx, EGNx |

| GCSC <sup>Notes 2</sup> | Control registers of clock control function, voltage detector and RAM parity error detection function guard                                                                                                                     |
|-------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0                       | Disabled. Control registers of clock control function, voltage detector and RAM parity error detection function can be read or written to.                                                                                      |
| 1                       | Enabled. Writing to control registers of clock control function, voltage detector and RAM parity error detection function is disabled. Reading is enabled.<br>[Guarded SFR] CMC, CSC, OSTs, CKC, PERx, OSMC, LVIM, LVIS, RPECTL |

**Notes** 1. Pxx (Port register) is not guarded.

2. Clear GCSC bit to 0, during self programming /serial programming.

### 23.3.6 Invalid memory access detection function

The IEC60730 standard mandates checking that the CPU and interrupts are operating correctly.

The illegal memory access detection function triggers a reset if a memory space specified as access-prohibited is accessed.

The illegal memory access detection function applies to the areas indicated by NG in Figure 23-10.

**Figure 23-10. Invalid access detection area**

|                  |                                                | Possibility access |       | Fetching instructions (execute) |
|------------------|------------------------------------------------|--------------------|-------|---------------------------------|
|                  |                                                | Read               | Write |                                 |
| FFFFFH           | Special function register (SFR)<br>256 byte    |                    |       | NG                              |
| FFF00H<br>FFEFH  | General-purpose register<br>32 byte            |                    | OK    |                                 |
| FFEE0H<br>FFEDFH |                                                |                    |       | OK                              |
|                  | RAM <sup>Note</sup>                            |                    |       |                                 |
| yyyyyH           |                                                |                    |       |                                 |
|                  | Mirror                                         | OK                 | NG    | NG                              |
|                  | Data flash memory                              |                    |       |                                 |
| F1000H<br>F0FFFH | Reserved                                       |                    |       | OK                              |
| F0800H<br>F07FFH |                                                |                    | OK    | NG                              |
|                  | Special function register (2nd SFR)<br>2 Kbyte |                    |       |                                 |
| F0000H<br>EFFFFH |                                                |                    |       | OK                              |
| E000H<br>EEFFH   |                                                |                    |       |                                 |
|                  | Reserved                                       | NG                 | NG    | NG                              |
|                  |                                                |                    |       |                                 |
| 10000H<br>0FFFFH |                                                |                    |       |                                 |
|                  |                                                |                    |       |                                 |
| xxxxxH           |                                                |                    |       |                                 |
|                  | Code flash memory <sup>Note</sup>              | OK                 |       | OK                              |
| 00000H           |                                                |                    |       |                                 |

**Note** Code flash memory and RAM address of each product are as follows.

| Products                     | Code flash memory<br>(00000H to xxxxxH) | RAM<br>(yyyyyH to FFEFFH)       |
|------------------------------|-----------------------------------------|---------------------------------|
| R5F10Rx8 (x = B, F, G, J)    | 8192 × 8 bit (00000H to 01FFFFH)        | 1024 × 8 bit (FFB00H to FFEFFH) |
| R5F10RxA (x = B, F, G, J, L) | 16384 × 8 bit (00000H to 03FFFFH)       | 1024 × 8 bit (FFB00H to FFEFFH) |
| R5F10RxC (x = B, F, G, J, L) | 32768 × 8 bit (00000H to 07FFFFH)       | 1536 × 8 bit (FF900H to FFEFFH) |

### 23.3.6.1 Invalid memory access detection control register (IAWCTL)

This register is used to control the detection of invalid memory access and RAM/SFR guard function.

IAWEN bit is used in invalid memory access detection function.

The IAWCTL register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 23-11. Format of Invalid Memory Access Detection Control Register (IAWCTL)**

Address: F0078H After reset: 00H R/W

| Symbol | 7     | 6 | 5     | 4     | 3 | 2     | 1    | 0    |
|--------|-------|---|-------|-------|---|-------|------|------|
| IAWCTL | IAWEN | 0 | GRAM1 | GRAM0 | 0 | GPORT | GINT | GCSC |

|                       |                                                 |
|-----------------------|-------------------------------------------------|
| IAWEN <sup>Note</sup> | Control of invalid memory access detection      |
| 0                     | Disable the detection of invalid memory access. |
| 1                     | Enable the detection of invalid memory access.  |

**Note** Only writing 1 to the IAWEN bit is enabled, not writing 0 to it after setting it to 1.

**Remark** By specifying WDTON = 1 for the option byte, the invalid memory access function is always enabled regardless of the setting for the IAWEN bit. (For details, see **CHAPTER 25 OPTION BYTE**.)

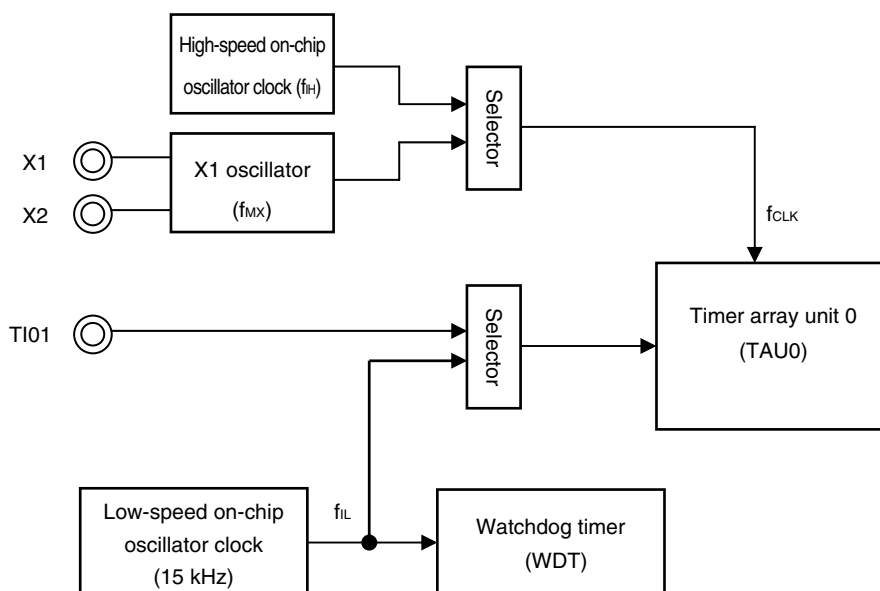


### 23.3.7 Frequency detection function

The IEC60730 standard mandates checking that the oscillation frequency is correct.

The frequency detection function can detect whether the clock is operating on an abnormal frequency by comparing the high-speed on-chip oscillator clock or external X1 oscillation clock with the low-speed on-chip oscillator clock (15 kHz).

**Figure 23-12. Configuration of Frequency Detection Function**



#### <Operational overview>

Whether the clock frequency is correct or not can be judged by measuring the pulse interval under the following conditions:

- The high-speed on-chip oscillator clock ( $f_H$ ) or the external X1 oscillation clock ( $f_{MX}$ ) is selected as the CPU/peripheral hardware clock ( $f_{CLK}$ ).
- The low-speed on-chip oscillator clock ( $f_L$ : 15 kHz) is selected as the timer input for channel 1 of timer array unit 0 (TAU0).

If pulse interval measurement results in an abnormal value, it can be concluded that the clock frequency is abnormal. For how to execute pulse interval measurement, see **6.7.4 Operation as input pulse interval measurement**.

### 23.3.7.1 Timer input select register 0 (TIS0)

This register is used to select the timer input of channel 1.

By selecting the low-speed on-chip oscillator clock for the timer input, its pulse width can be measured to determine whether the proportional relationship between the low-speed on-chip oscillator clock and the timer operation clock is correct.

The TIS0 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 23-13. Format of Timer Input Select Register 0 (TIS0)**

Address: F0074H    After reset: 00H    R/W

|        |   |   |   |   |   |       |       |       |
|--------|---|---|---|---|---|-------|-------|-------|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2     | 1     | 0     |
| TIS0   | 0 | 0 | 0 | 0 | 0 | TIS02 | TIS01 | TIS00 |

| TIS02                | TIS01 | TIS00 | Selection of timer input used with channel 1    |
|----------------------|-------|-------|-------------------------------------------------|
| 0                    | 0     | 0     | Input signal of timer input pin (TI01)          |
| 1                    | 0     | 0     | Low-speed on-chip oscillator clock ( $f_{IL}$ ) |
| 1                    | 0     | 1     | Subsystem clock ( $f_{SUB}$ )                   |
| Other than the above |       |       | Setting prohibited                              |

### 23.3.8 A/D test function

The IEC60730 standard mandates testing the A/D converter. The A/D test function is used to check whether the A/D converter is operating normally by executing A/D conversions of an internal voltage of 0 V, the  $AV_{REF}$  voltage, and the internal reference voltage (1.45 V).

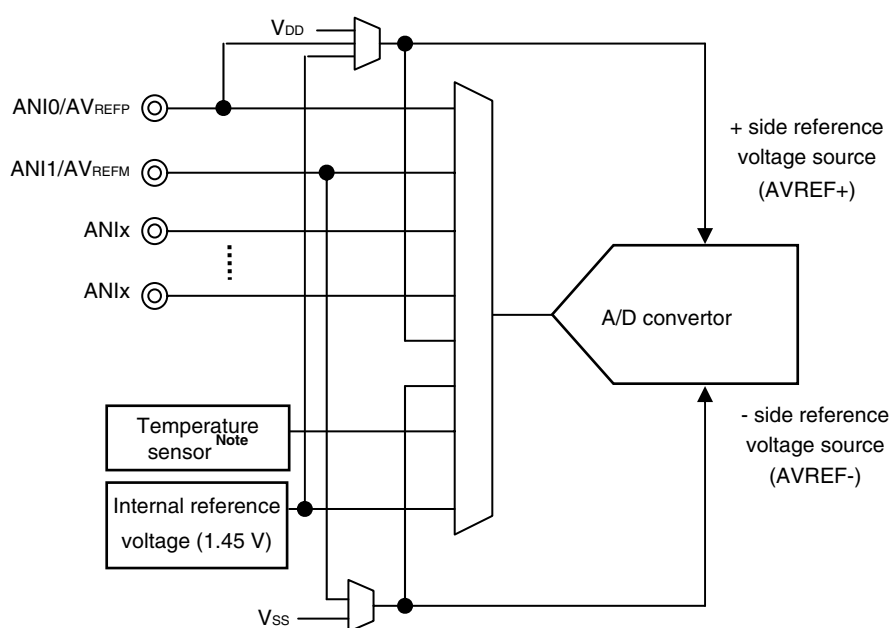
<R> The analog multiplexer can be checked using the following procedure.

- (1) Perform A/D conversion for the ANIx pin (conversion result 1).
- (2) Select  $AV_{REFM}$  using the ADTES register, perform A/D conversion, and then set the voltage potential difference between the terminals of the sampling capacitor of the A/D converter to 0 V.
- (3) Perform A/D conversion for the ANIx pin (conversion result 2).
- (4) Select  $AV_{REFP}$  using the ADTES register, perform A/D conversion, and then set the voltage potential difference between the terminals of the sampling capacitor of the A/D converter to  $AV_{REF}$ .
- (5) Perform A/D conversion for the ANIx pin (conversion result 3).
- (6) Make sure that conversion results 1, 2, and 3 are equal.

Using the procedure above can confirm that the analog multiplexer is selected and all wiring is connected.

- Remarks**
1. If the analog input voltage is variable during A/D conversion in steps <1> to <5> above, use another method to check the analog multiplexer.
  2. The conversion results might contain an error. Consider an appropriate level of error when comparing the conversion results.

**Figure 23-14. Configuration of A/D Test Function**



**Note** This setting can be used only in HS (high-speed main) mode

### 23.3.8.1 A/D test register (ADTES)

This register is used to select the A/D converter's positive reference voltage  $AV_{REFP}$ , the A/D converter's negative reference voltage  $AV_{REFM}$ , or the analog input channel (ANLxx) as the target of A/D conversion.

When using the A/D test function, specify the following settings:

- Select  $AV_{REFM}$  as the target of A/D conversion when converting the internal 0 V.
- Select  $AV_{REFP}$  as the target of A/D conversion when converting  $AV_{REF}$ .

The ADTES register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 23-15. Format of A/D Test Register (ADTES)**

Address: F0013H    After reset: 00H    R/W

|        |   |   |   |   |   |   |        |        |
|--------|---|---|---|---|---|---|--------|--------|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1      | 0      |
| ADTES  | 0 | 0 | 0 | 0 | 0 | 0 | ADTES1 | ADTES0 |

| ADTES1               | ADTES0 | A/D conversion target                                                                                                                                                                 |
|----------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0                    | 0      | ANLxx/temperature sensor output <sup>Note</sup> /internal reference voltage (1.45 V) <sup>Note</sup> (This is specified using the analog input channel specification register (ADS).) |
| 1                    | 0      | $AV_{REFM}$                                                                                                                                                                           |
| 1                    | 1      | $AV_{REFP}$                                                                                                                                                                           |
| Other than the above |        | Setting prohibited                                                                                                                                                                    |

**Note** Temperature sensor output/internal reference voltage (1.45 V) can be used only in HS (high-speed main) mode.

### 23.3.8.2 Analog input channel specification register (ADS)

This register specifies the input channel of the analog voltage to be A/D converted.

Set A/D test register (ADTES) to 00H when measuring the ANIxx/temperature sensor output/internal reference voltage (1.45 V).

The ADS register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 23-16. Format of Analog Input Channel Specification Register (ADS)**

Address: FFF31H After reset: 00H R/W

| Symbol | 7     | 6 | 5 | 4    | 3    | 2    | 1    | 0    |
|--------|-------|---|---|------|------|------|------|------|
| ADS    | ADISS | 0 | 0 | ADS4 | ADS3 | ADS2 | ADS1 | ADS0 |

| ADISS                | ADS4 | ADS3 | ADS2 | ADS1 | ADS0 | Analog input channel | Input source                                             |
|----------------------|------|------|------|------|------|----------------------|----------------------------------------------------------|
| 0                    | 0    | 0    | 0    | 0    | 0    | ANI0                 | P20/ANI0/AV <sub>REFP</sub> pin                          |
| 0                    | 0    | 0    | 0    | 0    | 1    | ANI1                 | P21/ANI1/AV <sub>REFM</sub> pin                          |
| 0                    | 1    | 0    | 0    | 0    | 0    | ANI16                | P41/ANI16 pin                                            |
| 0                    | 1    | 0    | 0    | 0    | 1    | ANI17                | P120/ANI17 pin                                           |
| 0                    | 1    | 0    | 0    | 1    | 0    | ANI18                | P13/ANI18 pin                                            |
| 0                    | 1    | 0    | 0    | 1    | 1    | ANI19                | P14/ANI19 pin                                            |
| 0                    | 1    | 0    | 1    | 0    | 0    | ANI20                | P142/ANI20 pin                                           |
| 0                    | 1    | 0    | 1    | 0    | 1    | ANI21                | P143/ANI21 pin                                           |
| 0                    | 1    | 0    | 1    | 1    | 0    | ANI22                | P144/ANI22 pin                                           |
| 0                    | 1    | 0    | 1    | 1    | 1    | ANI23                | P145/ANI23 pin                                           |
| 1                    | 0    | 0    | 0    | 0    | 0    | –                    | Temperature sensor output<br>Notes 1, 2                  |
| 1                    | 0    | 0    | 0    | 0    | 1    | –                    | Internal reference voltage<br>output (1.45 V) Notes 1, 2 |
| Other than the above |      |      |      |      |      | Setting prohibited   |                                                          |

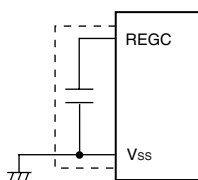
- Notes**
1. Do not select when shifting to STOP mode, or to HALT mode while the CPU is operating on the subsystem clock.
  2. Can only be used in HS (high-speed main) mode.

- Cautions**
1. Be sure to clear bits 5 and 6 to 0.
  2. Only rewrite the value of the ADISS bit while A/D voltage comparator operation is stopped (which is indicated by the ADCS bit of A/D converter mode register 0 (ADM0) being 0).
  3. If using AV<sub>REFP</sub> as the + side reference voltage source of the A/D converter, do not select ANI0 as an A/D conversion channel.
  4. If using AV<sub>REFM</sub> as the – side reference voltage source of the A/D converter, do not select ANI1 as an A/D conversion channel.
  5. If ADISS is set to 1, the internal reference voltage (1.45 V) cannot be used for the + side reference

## CHAPTER 24 REGULATOR

## 24.1 Regulator Overview

The RL78/L12 contains a circuit for operating the device with a constant voltage. At this time, in order to stabilize the regulator output voltage, connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F). Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.



**Caution** Keep the wiring length as short as possible for the broken-line part in the above figure.

The regulator output voltage, see table 24-1.

**Table 24-1. Regulator Output Voltage Conditions**

| Mode                       | Output Voltage | Condition                                                                                                                                                                                                                                |
|----------------------------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LV (low voltage main) mode | 1.8 V          | -                                                                                                                                                                                                                                        |
| LS (low-speed main) mode   |                |                                                                                                                                                                                                                                          |
| HS (high-speed main) mode  | 1.8 V          | In STOP mode                                                                                                                                                                                                                             |
|                            |                | When both the high-speed system clock (f <sub>MX</sub> ) and the high-speed on-chip oscillator clock (f <sub>IH</sub> ) are stopped during CPU operation with the subsystem clock (f <sub>XT</sub> )                                     |
|                            |                | When both the high-speed system clock (f <sub>MX</sub> ) and the high-speed on-chip oscillator clock (f <sub>IH</sub> ) are stopped during the HALT mode when the CPU operation with the subsystem clock (f <sub>XT</sub> ) has been set |
|                            | 2.1 V          | Other than above (include during OCD mode) <sup>Note</sup>                                                                                                                                                                               |

**Note** When it shifts to the subsystem clock operation or STOP mode during the on-chip debugging, the regulator output voltage is kept at 2.1 V (not decline to 1.8 V).

## CHAPTER 25 OPTION BYTE

### 25.1 Functions of Option Bytes

Addresses 000C0H to 000C3H of the flash memory of the RL78/L12 form an option byte area.

Option bytes consist of user option byte (000C0H to 000C2H) and on-chip debug option byte (000C3H).

Upon power application or resetting and starting, an option byte is automatically referenced and a specified function is set. When using the product, be sure to set the following functions by using the option bytes.

<R> For the bits to which no function is allocated, be sure to set the value specified in this manual.

#### 25.1.1 User option byte (000C0H to 000C2H)

##### (1) 000C0H

- ☐ Operation of watchdog timer
  - Operation is stopped or enabled in the HALT or STOP mode.
- ☐ Setting of interval time of watchdog timer
- ☐ Operation of watchdog timer
  - Operation is stopped or enabled.
- ☐ Setting of window open period of watchdog timer
- ☐ Setting of interval interrupt of watchdog timer
  - Used or not used

##### (2) 000C1H

- ☐ Setting of LVD operation mode
  - Interrupt & reset mode.
  - Reset mode.
  - Interrupt mode.
- ☐ Setting of LVD detection level ( $V_{LVDH}$ ,  $V_{LVDL}$ ,  $V_{LVD}$ )

##### (3) 000C2H

- ☐ Setting of flash operation mode
  - LV (low voltage main) mode
  - LS (low speed main) mode
  - HS (high speed main) mode
- ☐ Setting of the frequency of the high-speed on-chip oscillator
  - Select from 1 MHz, 4 MHz, 8 MHz, 12 MHz, 16 MHz, and 24 MHz.

**25.1.2 On-chip debug option byte (000C3H)**

- Control of on-chip debug operation
  - On-chip debug operation is disabled or enabled.
- Handling of data of flash memory in case of failure in on-chip debug security ID authentication
  - Data of flash memory is erased or not erased in case of failure in on-chip debug security ID authentication.



## 25.2 Format of User Option Byte

The format of user option byte is shown below.

**Figure 25-1. Format of User Option Byte (000C0H)**

Address: 000C0H

<R>

| 7        | 6                                                                                              | 5                                                   | 4                                                                    | 3     | 2     | 1     | 0        |
|----------|------------------------------------------------------------------------------------------------|-----------------------------------------------------|----------------------------------------------------------------------|-------|-------|-------|----------|
| WDTINIT  | WINDOW1                                                                                        | WINDOW0                                             | WDTON                                                                | WDCS2 | WDCS1 | WDCS0 | WDSTBYON |
| WDTINIT  | Use of interval interrupt of watchdog timer                                                    |                                                     |                                                                      |       |       |       |          |
| 0        | Interval interrupt is not used.                                                                |                                                     |                                                                      |       |       |       |          |
| 1        | Interval interrupt is generated when 75% + 1/2f <sub>IL</sub> of the overflow time is reached. |                                                     |                                                                      |       |       |       |          |
| WINDOW1  | WINDOW0                                                                                        | Watchdog timer window open period <sup>Note 2</sup> |                                                                      |       |       |       |          |
| 0        | 0                                                                                              | Setting prohibited                                  |                                                                      |       |       |       |          |
| 0        | 1                                                                                              | 50%                                                 |                                                                      |       |       |       |          |
| 1        | 0                                                                                              | 75%                                                 |                                                                      |       |       |       |          |
| 1        | 1                                                                                              | 100%                                                |                                                                      |       |       |       |          |
| WDTON    | Operation control of watchdog timer counter                                                    |                                                     |                                                                      |       |       |       |          |
| 0        | Counter operation disabled (counting stopped after reset)                                      |                                                     |                                                                      |       |       |       |          |
| 1        | Counter operation enabled (counting started after reset)                                       |                                                     |                                                                      |       |       |       |          |
| WDCS2    | WDCS1                                                                                          | WDCS0                                               | Watchdog timer overflow time<br>(f <sub>IL</sub> = 17.25 kHz (MAX.)) |       |       |       |          |
| 0        | 0                                                                                              | 0                                                   | 2 <sup>6</sup> /f <sub>IL</sub> (3.71 ms)                            |       |       |       |          |
| 0        | 0                                                                                              | 1                                                   | 2 <sup>7</sup> /f <sub>IL</sub> (7.42 ms)                            |       |       |       |          |
| 0        | 1                                                                                              | 0                                                   | 2 <sup>8</sup> /f <sub>IL</sub> (14.84 ms)                           |       |       |       |          |
| 0        | 1                                                                                              | 1                                                   | 2 <sup>9</sup> /f <sub>IL</sub> (29.68 ms)                           |       |       |       |          |
| 1        | 0                                                                                              | 0                                                   | 2 <sup>11</sup> /f <sub>IL</sub> (118.72 ms)                         |       |       |       |          |
| 1        | 0                                                                                              | 1                                                   | 2 <sup>13</sup> /f <sub>IL</sub> (474.90 ms)                         |       |       |       |          |
| 1        | 1                                                                                              | 0                                                   | 2 <sup>14</sup> /f <sub>IL</sub> (949.80 ms)                         |       |       |       |          |
| 1        | 1                                                                                              | 1                                                   | 2 <sup>16</sup> /f <sub>IL</sub> (3799.19m s)                        |       |       |       |          |
| WDSTBYON | Operation control of watchdog timer counter (HALT/STOP mode)                                   |                                                     |                                                                      |       |       |       |          |
| 0        | Counter operation stopped in HALT/STOP mode <sup>Note</sup>                                    |                                                     |                                                                      |       |       |       |          |
| 1        | Counter operation enabled in HALT/STOP mode                                                    |                                                     |                                                                      |       |       |       |          |

**Note** The window open period is 100% when WDSTBYON = 0, regardless the value of the WINDOW1 and WINDOW0 bits.

<R> **Caution** The watchdog timer continues its operation even during self-programming or data flash rewrite. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

**Remark**  $f_{IL}$ : Low-speed on-chip oscillator clock frequency

&lt;R&gt;

Figure 25-2. Format of User Option Byte (000C1H) (1/2)

Address: 000C1H

|       |       |       |   |       |       |         |         |
|-------|-------|-------|---|-------|-------|---------|---------|
| 7     | 6     | 5     | 4 | 3     | 2     | 1       | 0       |
| VPOC2 | VPOC1 | VPOC0 | 1 | LVIS1 | LVIS0 | LVIMDS1 | LVIMDS0 |

- LVD setting (interrupt & reset mode)

| Detection voltage |              |              | Option byte Setting Value |         |       |       |       |       |       |
|-------------------|--------------|--------------|---------------------------|---------|-------|-------|-------|-------|-------|
| VLVDH             |              | VLVDL        | Mode setting              |         | VPOC2 | VPOC1 | VPOC0 | LVIS1 | LVIS0 |
| Rising edge       | Falling edge | Falling edge | LVIMDS1                   | LVIMDS0 |       |       |       |       |       |
| 1.77 V            | 1.73 V       | 1.63 V       | 1                         | 0       | 0     | 0     | 0     | 1     | 0     |
| 1.88 V            | 1.84 V       |              |                           |         |       |       |       | 0     | 1     |
| 2.92 V            | 2.86 V       |              |                           |         |       |       |       | 0     | 0     |
| 1.98 V            | 1.94 V       | 1.84 V       |                           |         |       | 0     | 1     | 1     | 0     |
| 2.09 V            | 2.04 V       |              |                           |         |       |       |       | 0     | 1     |
| 3.13 V            | 3.06 V       |              |                           |         |       |       |       | 0     | 0     |
| 2.61 V            | 2.55 V       | 2.45 V       |                           |         |       | 1     | 0     | 1     | 0     |
| 2.71 V            | 2.65 V       |              |                           |         |       |       |       | 0     | 1     |
| 3.75 V            | 3.67 V       |              |                           |         |       |       |       | 0     | 0     |
| 2.92 V            | 2.86 V       | 2.75 V       |                           |         | 1     | 1     | 1     | 0     |       |
| 3.02 V            | 2.96 V       |              |                           |         |       |       | 0     | 1     |       |
| 4.06 V            | 3.98 V       |              |                           |         |       |       | 0     | 0     |       |
| Other than above  |              |              | Setting prohibited        |         |       |       |       |       |       |

- LVD setting (reset mode)

| LVD setting (reset mode) |              | Option byte Setting Value |         |       |       |       |       |       |
|--------------------------|--------------|---------------------------|---------|-------|-------|-------|-------|-------|
| Detection voltage        |              | Mode setting              |         | VPOC2 | VPOC1 | VPOC0 | LVIS1 | LVIS0 |
| V <sub>LVD</sub>         |              |                           |         |       |       |       |       |       |
| Rising edge              | Falling edge | LVIMDS1                   | LVIMDS0 |       |       |       |       |       |
| 1.67 V                   | 1.63 V       | 1                         | 1       | 0     | 0     | 0     | 1     | 1     |
| 1.77 V                   | 1.73 V       |                           |         |       | 0     | 0     | 1     | 0     |
| 1.88 V                   | 1.84 V       |                           |         |       | 0     | 1     | 1     | 1     |
| 1.98 V                   | 1.94 V       |                           |         |       | 0     | 1     | 1     | 0     |
| 2.09 V                   | 2.04 V       |                           |         |       | 0     | 1     | 0     | 1     |
| 2.50 V                   | 2.45 V       |                           |         |       | 1     | 0     | 1     | 1     |
| 2.61 V                   | 2.55 V       |                           |         |       | 1     | 0     | 1     | 0     |
| 2.71 V                   | 2.65 V       |                           |         |       | 1     | 0     | 0     | 1     |
| 2.81 V                   | 2.75 V       |                           |         |       | 1     | 1     | 1     | 1     |
| 2.92 V                   | 2.86 V       |                           |         |       | 1     | 1     | 1     | 0     |
| 3.02 V                   | 2.96 V       |                           |         |       | 1     | 1     | 0     | 1     |
| 3.13 V                   | 3.06 V       |                           |         |       | 0     | 1     | 0     | 0     |
| 3.75 V                   | 3.67 V       |                           |         |       | 1     | 0     | 0     | 0     |
| 4.06 V                   | 3.98 V       |                           |         |       | 1     | 1     | 0     | 0     |
| Other than above         |              | Setting prohibited        |         |       |       |       |       |       |

**Caution** Be sure to set bit 4 to “1”.

**Remark** Refer to LVD setting, see 22.1 Functions of Voltage Detector.

&lt;R&gt;

**Figure 25-2. Format of User Option Byte (000C1H) (2/2)**

Address: 000C1H

|       |       |       |   |       |       |         |         |
|-------|-------|-------|---|-------|-------|---------|---------|
| 7     | 6     | 5     | 4 | 3     | 2     | 1       | 0       |
| VPOC2 | VPOC1 | VPOC0 | 1 | LVIS1 | LVIS0 | LVIMDS1 | LVIMDS0 |

- LVD setting (interrupt mode)

| Detection voltage |                    | Option byte Setting Value |         |       |       |       |       |       |
|-------------------|--------------------|---------------------------|---------|-------|-------|-------|-------|-------|
| V <sub>LVD</sub>  |                    | Mode setting              |         | VPOC2 | VPOC1 | VPOC0 | LVIS1 | LVIS0 |
| Rising edge       | Falling edge       | LVIMDS1                   | LVIMDS0 |       |       |       |       |       |
| 1.67 V            | 1.63 V             | 0                         | 1       | 0     | 0     | 0     | 1     | 1     |
| 1.77 V            | 1.73 V             |                           |         |       | 0     | 0     | 1     | 0     |
| 1.88 V            | 1.84 V             |                           |         |       | 0     | 1     | 1     | 1     |
| 1.98 V            | 1.94 V             |                           |         |       | 0     | 1     | 1     | 0     |
| 2.09 V            | 2.04 V             |                           |         |       | 0     | 1     | 0     | 1     |
| 2.50 V            | 2.45 V             |                           |         |       | 1     | 0     | 1     | 1     |
| 2.61 V            | 2.55 V             |                           |         |       | 1     | 0     | 1     | 0     |
| 2.71 V            | 2.65 V             |                           |         |       | 1     | 0     | 0     | 1     |
| 2.81 V            | 2.75 V             |                           |         |       | 1     | 1     | 1     | 1     |
| 2.92 V            | 2.86 V             |                           |         |       | 1     | 1     | 1     | 0     |
| 3.02 V            | 2.96 V             |                           |         |       | 1     | 1     | 0     | 1     |
| 3.13 V            | 3.06 V             |                           |         |       | 0     | 1     | 0     | 0     |
| 3.75 V            | 3.67 V             |                           |         |       | 1     | 0     | 0     | 0     |
| 4.06 V            | 3.98 V             |                           |         |       | 1     | 1     | 0     | 0     |
| Other than above  | Setting prohibited |                           |         |       |       |       |       |       |

- LVD setting (LVDOFF)

| Detection voltage |              | Option byte Setting Value |         |       |       |       |       |       |
|-------------------|--------------|---------------------------|---------|-------|-------|-------|-------|-------|
| V <sub>LVD</sub>  |              | Mode setting              |         | VPOC2 | VPOC1 | VPOC0 | LVIS1 | LVIS0 |
| Rising edge       | Falling edge | LVIMDS1                   | LVIMDS0 |       |       |       |       |       |
| –                 | –            | 0/1                       | 1       | 1     | ×     | ×     | ×     | ×     |
| Other than above  |              | Setting prohibited        |         |       |       |       |       |       |

- Cautions**
1. Be sure to set bit 4 to “1”.
  2. When the LVD circuit is off, use the external reset pin to execute a reset.

- Remarks**
1. ×: don't care
  2. Refer to LVD setting, see 22.1 Functions of Voltage Detector.

**Figure 25-3. Format of Option Byte (000C2H)**

Address: 000C2H

|        |        |   |   |         |         |         |         |
|--------|--------|---|---|---------|---------|---------|---------|
| 7      | 6      | 5 | 4 | 3       | 2       | 1       | 0       |
| CMODE1 | CMODE0 | 1 | 0 | FRQSEL3 | FRQSEL2 | FRQSEL1 | FRQSEL0 |

| CMODE1           | CMODE0 | Setting of flash operation mode |                           |                         |
|------------------|--------|---------------------------------|---------------------------|-------------------------|
|                  |        |                                 | Operating Frequency Range | Operating Voltage Range |
| 0                | 0      | LV (low voltage main) mode      | 1 to 4 MHz                | 1.6 to 5.5 V            |
| 1                | 0      | LS (low speed main) mode        | 1 to 8 MHz                | 1.8 to 5.5 V            |
| 1                | 1      | HS (high speed main) mode       | 1 to 16 MHz               | 2.4 to 5.5 V            |
|                  |        |                                 | 1 to 24 MHz               | 2.7 to 5.5 V            |
| Other than above |        | Setting prohibited              |                           |                         |

| FRQSEL3          | FRQSEL2 | FRQSEL1 | FRQSEL0 | Frequency of the high-speed on-chip oscillator |
|------------------|---------|---------|---------|------------------------------------------------|
| 0                | 0       | 0       | 0       | 24 MHz                                         |
| 1                | 0       | 0       | 1       | 16 MHz                                         |
| 0                | 0       | 0       | 1       | 12 MHz                                         |
| 1                | 0       | 1       | 0       | 8 MHz                                          |
| 1                | 0       | 1       | 1       | 4 MHz                                          |
| 1                | 1       | 0       | 1       | 1 MHz                                          |
| Other than above |         |         |         | Setting prohibited                             |

**Caution** Be sure to set 10B to bits 5 and 4.

### 25.3 Format of On-chip Debug Option Byte

The format of on-chip debug option byte is shown below.

**Figure 25-4. Format of On-chip Debug Option Byte (000C3H)**

Address: 000C3H

|          |   |   |   |   |   |   |         |
|----------|---|---|---|---|---|---|---------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0       |
| OCDENSET | 0 | 0 | 0 | 0 | 1 | 0 | OCDERSD |

| OCDENSET | OCDERSD | Control of on-chip debug operation                                                                                                  |
|----------|---------|-------------------------------------------------------------------------------------------------------------------------------------|
| 0        | 0       | Disables on-chip debug operation.                                                                                                   |
| 0        | 1       | Setting prohibited                                                                                                                  |
| 1        | 0       | Enables on-chip debugging.<br>Erases data of flash memory in case of failures in authenticating on-chip debug security ID.          |
| 1        | 1       | Enables on-chip debugging.<br>Does not erases data of flash memory in case of failures in authenticating on-chip debug security ID. |

**Caution** Bits 7 and 0 (OCDENSET and OCDERSD) can only be specified a value.

Be sure to set 000010B to bits 6 to 1.

**Remark** The value on bits 3 to 1 will be written over when the on-chip debug function is in use and thus it will become unstable after the setting.

However, be sure to set the default values (0, 1, and 0) to bits 3 to 1 at setting.

## 25.4 Setting of Option Byte

The user option byte and on-chip debug option byte can be set using the assembler linker option, in addition to describing to the source. When doing so, the contents set by using the linker option take precedence, even if descriptions exist in the source, as mentioned below.

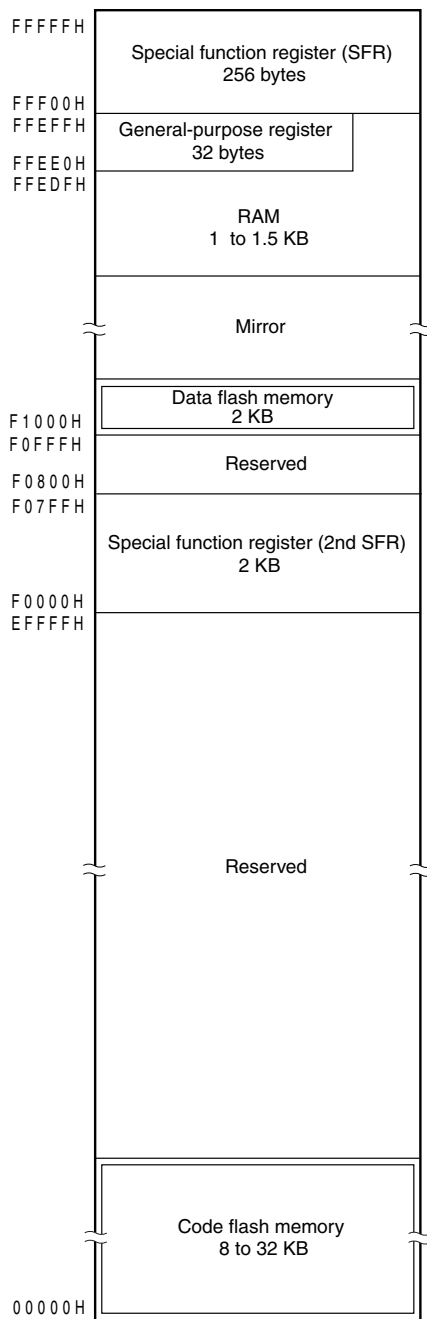
A software description example of the option byte setting is shown below.

| OPT | CSEG | OPT_BYTE |                                                                                                                                                                                                                                                                |
|-----|------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     | DB   | 36H      | ; Does not use interval interrupt of watchdog timer,<br>; Enables watchdog timer operation,<br>; Window open period of watchdog timer is 50%,<br>; Overflow time of watchdog timer is $2^9/f_{IL}$ ,<br>; Stops watchdog timer operation during HALT/STOP mode |
|     | DB   | 1AH      | ; Select 1.63 V for $V_{LVDL}$<br>; Select rising edge 1.77 V, falling edge 1.73 V for $V_{LVDH}$<br>; Select the interrupt & reset mode as the LVD operation mode                                                                                             |
|     | DB   | 2DH      | ; Select the LV (low voltage main) mode as the flash operation mode<br>and 1 MHz as the frequency of the high-speed on-chip oscillator clock                                                                                                                   |
|     | DB   | 85H      | ; Enables on-chip debug operation, does not erase flash memory<br>data when security ID authorization fails                                                                                                                                                    |

**Caution** To specify the option byte by using assembly language, use **OPT\_BYTE** as the relocation attribute name of the CSEG pseudo instruction.

## CHAPTER 26 FLASH MEMORY

The RL78/L12 incorporates the flash memory to which a program can be written, erased, and overwritten while mounted on the board. The flash memory includes the “code flash memory”, in which programs can be executed, and the “data flash memory”, an area for storing data.



The following three methods for programming the flash memory are available:

- Writing to flash memory by using flash memory programmer (see 26.1)
- Writing to flash memory by using external device (that Incorporates UART) (see 26.2)
- Self-programming (see 26.7)

## 26.1 Writing to Flash Memory by Using Flash Memory Programmer

The following dedicated flash memory programmer can be used to write data to the internal flash memory of the RL78/L12.

- PG-FP5, FL-PR5
- E1 on-chip debugging emulator

Data can be written to the flash memory on-board or off-board, by using a dedicated flash memory programmer.

### (1) On-board programming

The contents of the flash memory can be rewritten after the RL78/L12 has been mounted on the target system. The connectors that connect the dedicated flash memory programmer must be mounted on the target system.

### (2) Off-board programming

Data can be written to the flash memory with a dedicated program adapter (FA series) before the RL78/L12 is mounted on the target system.

**Remark** FL-PR5 and FA series are products of Naito Densei Machida Mfg. Co., Ltd.



**Table 26-1. Wiring Between RL78/L12 and Dedicated Flash Memory Programmer**

| Pin Configuration of Dedicated Flash Memory Programmer |                               |        |                                                         | Pin Name             | Pin No.    |              |            |              |                                              |
|--------------------------------------------------------|-------------------------------|--------|---------------------------------------------------------|----------------------|------------|--------------|------------|--------------|----------------------------------------------|
|                                                        |                               |        |                                                         |                      | 32-pin     | 44-pin       | 48-pin     | 52-pin       | 64-pin                                       |
| Signal Name                                            |                               | I/O    | Pin Function                                            |                      | WQFN (5x5) | LQFP (10x10) | LQFP (7x7) | LQFP (10x10) | LQFP (12x12),<br>LQFP (10x10),<br>WQFN (8x8) |
| PG-FP5, FL-PR5                                         | E1 on-chip debugging emulator |        |                                                         |                      |            |              |            |              |                                              |
| –                                                      | TOOL0                         | I/O    | Transmit/receive signal                                 | TOOL0/<br>P40        | 1          | 2            | 3          | 4            | 5                                            |
| SI/RxD                                                 | –                             | I/O    | Transmit/receive signal                                 |                      |            |              |            |              |                                              |
| SCK                                                    | –                             | Output | –                                                       | –                    | –          | –            | –          | –            | –                                            |
| CLK                                                    | –                             | Output | –                                                       | –                    | –          | –            | –          | –            | –                                            |
| –                                                      | RESET                         | Output | Reset signal                                            | RESET                | 2          | 3            | 4          | 5            | 6                                            |
| /RESET                                                 | –                             | Output |                                                         |                      |            |              |            |              |                                              |
| FLMD0                                                  | –                             | Output | Mode signal                                             | –                    | –          | –            | –          | –            | –                                            |
| V <sub>DD</sub>                                        |                               | I/O    | V <sub>DD</sub> voltage generation/<br>power monitoring | V <sub>DD</sub>      | 8          | 11           | 12         | 13           | 15                                           |
| GND                                                    |                               | –      | Ground                                                  | V <sub>SS</sub>      | 7          | 10           | 11         | 12           | 13                                           |
|                                                        |                               |        |                                                         | EV <sub>SS</sub>     | –          | –            | –          | –            | 14                                           |
|                                                        |                               |        |                                                         | REGC <sup>Note</sup> | 6          | 9            | 10         | 11           | 12                                           |
| EMV <sub>DD</sub>                                      |                               | –      | Driving power for TOOL pin                              | V <sub>DD</sub>      | 8          | 11           | 12         | 13           | –                                            |
|                                                        |                               |        |                                                         | EV <sub>DD</sub>     | –          | –            | –          | –            | 16                                           |

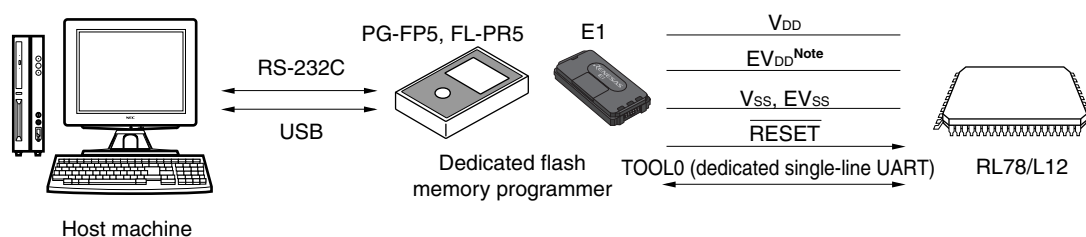
**Note** Connect REGC pin to ground via a capacitor (default: 0.47  $\mu$ F).

**Remark** Pins that are not indicated in the above table can be left open when using the flash memory programmer for flash programming.

### 26.1.1 Programming Environment

The environment required for writing a program to the flash memory of the RL78/L12 is illustrated below.

**Figure 26-1. Environment for Writing Program to Flash Memory**



**Note** 64-pin products only.

A host machine that controls the dedicated flash memory programmer is necessary.

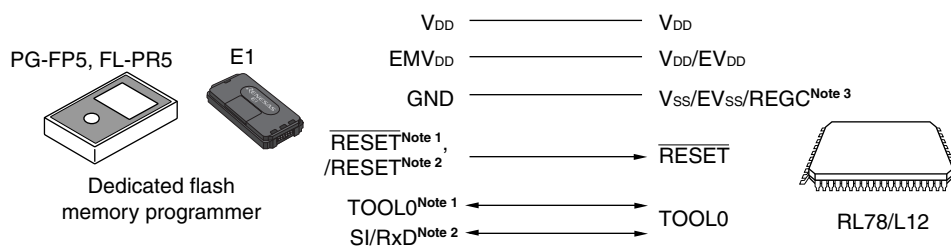
<R> To interface between the dedicated flash memory programmer and the RL78/L12, the TOOL0 pin is used for manipulation such as writing and erasing via a dedicated single-line UART.

### 26.1.2 Communication Mode

Communication between the dedicated flash memory programmer and the RL78/L12 is established by serial communication using the TOOL0 pin via a dedicated single-line UART of the RL78/L12.

Transfer rate: 1 M, 500 k, 250 k, 115.2 kbps

**Figure 26-2. Communication with Dedicated Flash Memory Programmer**



- Notes**
1. When using E1 on-chip debugging emulator.
  2. When using PG-FP5 or FL-PR5.
  3. Connect REGC pin to ground via a capacitor (default: 0.47  $\mu F$ ).

The dedicated flash memory programmer generates the following signals for the RL78/L12. See the manual of PG-FP5, FL-PR5, or E1 on-chip debugging emulator for details.

**Table 26-2. Pin Connection**

| Dedicated Flash Memory Programmer |                                     |        |                                                     | RL78/L12                                                  | Connection |
|-----------------------------------|-------------------------------------|--------|-----------------------------------------------------|-----------------------------------------------------------|------------|
| Signal Name                       |                                     | I/O    | Pin Function                                        | Pin Name                                                  |            |
| PG-FP5,<br>FL-PR5                 | E1 on-chip<br>debugging<br>emulator |        |                                                     |                                                           |            |
| FLMD0                             | —                                   | Output | Mode signal                                         | —                                                         | ×          |
| V <sub>DD</sub>                   |                                     | I/O    | V <sub>DD</sub> voltage generation/power monitoring | V <sub>DD</sub>                                           | ⊙          |
| GND                               |                                     | —      | Ground                                              | V <sub>SS</sub> , EV <sub>SS</sub> , REGC <sup>Note</sup> | ⊙          |
| EMV <sub>DD</sub>                 |                                     | —      | Driving power for TOOL pin                          | V <sub>DD</sub> , EV <sub>DD</sub>                        | ⊙          |
| CLK                               | —                                   | Output | Clock output                                        | —                                                         | ×          |
| /RESET                            | —                                   | Output | Reset signal                                        | $\overline{\text{RESET}}$                                 | ⊙          |
| —                                 | $\overline{\text{RESET}}$           | Output |                                                     |                                                           |            |
| —                                 | TOOL0                               | I/O    | Transmit/receive signal                             | TOOL0                                                     | ⊙          |
| SI/RxD                            | —                                   | I/O    | Transmit/receive signal                             |                                                           |            |
| SCK                               | —                                   | Output | Transfer clock                                      | —                                                         | ×          |

**Note** Connect REGC pin to ground via a capacitor (default: 0.47  $\mu$ F).

**Remark** ○: Be sure to connect the pin.

×: The pin does not have to be connected.

## 26.2 Writing to Flash Memory by Using External Device (that Incorporates UART)

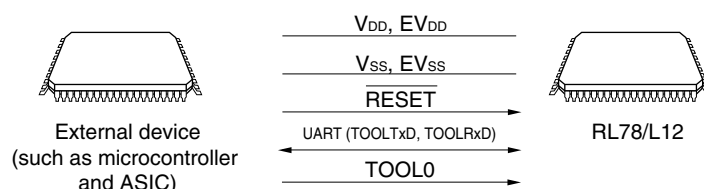
On-board data writing to the internal flash memory is possible by using the RL78/L12 and an external device (a microcontroller or ASIC) connected to a UART.

<R> On the development of flash memory programmer by user, refer to the RL78 Microcontrollers (RL78 Protocol A) Programmer Edition Application Note (R01AN0815).

### 26.2.1 Programming Environment

The environment required for writing a program to the flash memory of the RL78/L12 is illustrated below.

**Figure 26-3. Environment for Writing Program to Flash Memory**



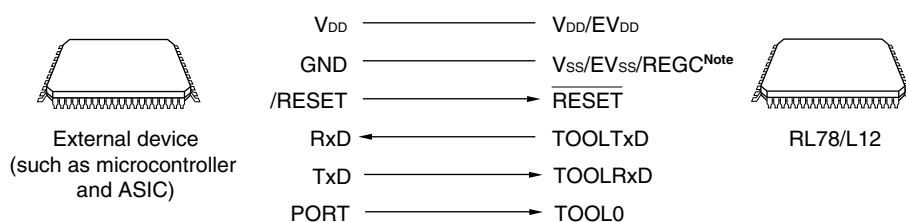
Processing to write data to or delete data from the RL78/L12 by using an external device is performed on-board. Off-board writing is not possible.

## 26.2.2 Communication Mode

Communication between the external device and the RL78/L12 is established by serial communication using the TOOLTxD and TOOLRxD pins via the dedicated UART of the RL78/L12.

Transfer rate: 1 M, 500 k, 250 k, 115.2 kbps

**Figure 26-4. Communication with External Device**



**Note** Connect REGC pin to ground via a capacitor (default: 0.47  $\mu$ F).

**Caution** Make EV<sub>DD</sub> the same potential as V<sub>DD</sub>.

The external device generates the following signals for the RL78/L12.

**Table 26-3. Pin Connection**

| External Device |        |                                                     | RL78/L12                                                  | Connection |
|-----------------|--------|-----------------------------------------------------|-----------------------------------------------------------|------------|
| Signal Name     | I/O    | Pin Function                                        | Pin Name                                                  |            |
| V <sub>DD</sub> | I/O    | V <sub>DD</sub> voltage generation/power monitoring | V <sub>DD</sub> , EV <sub>DD</sub>                        | ○          |
| GND             | —      | Ground                                              | V <sub>SS</sub> , EV <sub>SS</sub> , REGC <sup>Note</sup> | ○          |
| CLK             | Output | Clock output                                        | —                                                         | ×          |
| RESETOUT        | Output | Reset signal output                                 | RESET                                                     | ○          |
| RxD             | Input  | Receive signal                                      | TOOL0TxD                                                  | ○          |
| TxD             | Output | Transmit signal                                     | TOOL0RxD                                                  | ○          |
| PORT            | Output | Mode signal                                         | TOOL0                                                     | ○          |
| SCK             | Output | Transfer clock                                      | —                                                         | ×          |

**Note** Connect REGC pin to ground via a capacitor (default: 0.47  $\mu$ F).

**Caution** Make EV<sub>DD</sub> the same potential as V<sub>DD</sub>.

**Remark** ○: Be sure to connect the pin.

×: The pin does not have to be connected.

## 26.3 Connection of Pins on Board

To write the flash memory on-board by using the flash memory programmer, connectors that connect the dedicated flash memory programmer must be provided on the target system. First provide a function that selects the normal operation mode or flash memory programming mode on the board.

When the flash memory programming mode is set, all the pins not used for programming the flash memory are in the same status as immediately after reset. Therefore, if the external device does not recognize the state immediately after reset, the pins must be handled as described below.

<R> **Remark** Refer to flash programming mode, see **26.7 Flash Memory Programming by Self-Programming**.

### 26.3.1 P40/TOOL0 pin

In the flash memory programming mode, connect this pin to the dedicated flash memory programmer via an external 1 kΩ pull-up resistor.

When this pin is used as the port pin, use that by the following method.

When used as an input pin: Input of low-level is prohibited for 1 ms period after external pin reset release.  
Furthermore, when this pin is used via pull-down resistors, use the 500 kΩ or more resistors.

When used as an output pin: When this pin is used via pull-down resistors, use the 500 kΩ or more resistors.

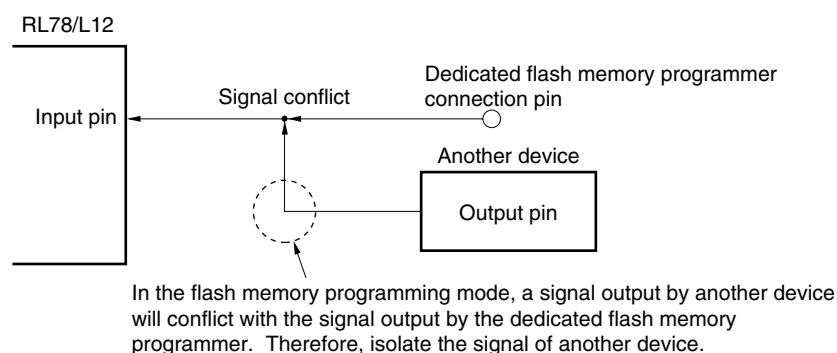
**Remark** The SAU and IICA pins are not used for communication between the RL78/L12 and dedicated flash memory programmer, because single-line UART (TOOL0 pin) is used.

### 26.3.2 $\overline{\text{RESET}}$ pin

Signal conflict will occur if the reset signal of the dedicated flash memory programmer and external device are connected to the  $\overline{\text{RESET}}$  pin that is connected to the reset signal generator on the board. To prevent this conflict, isolate the connection with the reset signal generator.

The flash memory will not be correctly programmed if the reset signal is input from the user system while the flash memory programming mode is set. Do not input any signal other than the reset signal of the dedicated flash memory programmer and external device.

**Figure 26-5. Signal Conflict ( $\overline{\text{RESET}}$  Pin)**



### 26.3.3 Port pins

When the flash memory programming mode is set, all the pins not used for flash memory programming enter the same status as that immediately after reset. If external devices connected to the ports do not recognize the port status immediately after reset, the port pin must be connected to either to  $V_{DD}$  or  $EV_{DD}$ , or  $V_{SS}$  or  $EV_{SS}$ , via a resistor.

### 26.3.4 REGC pin

Connect the REGC pin to GND via a capacitor (0.47 to 1  $\mu$ F) in the same manner as during normal operation. Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.

### 26.3.5 X1 and X2 pins

Connect X1 and X2 in the same status as in the normal operation mode.

**Remark** In the flash memory programming mode, the high-speed on-chip oscillator clock ( $f_{IH}$ ) is used.

### 26.3.6 Power supply

To use the supply voltage output of the flash memory programmer, connect the  $V_{DD}$  pin to  $V_{DD}$  of the flash memory programmer, and the  $V_{SS}$  pin to GND of the flash memory programmer.

To use the on-board supply voltage, connect in compliance with the normal operation mode.

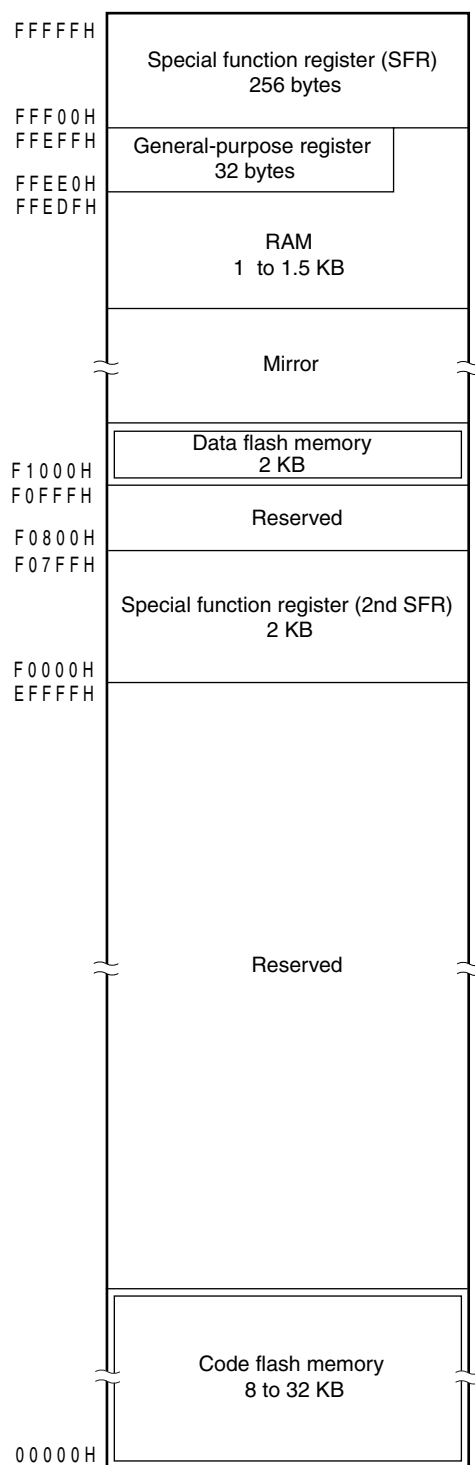
However, when writing to the flash memory by using the flash memory programmer and using the on-board supply voltage, be sure to connect the  $V_{DD}$  and  $V_{SS}$  pins to  $V_{DD}$  and GND of the flash memory programmer to use the power monitor function with the flash memory programmer.

Supply the same other power supplies ( $EV_{DD}$ ,  $EV_{SS}$ ) as those  $V_{DD}$  and  $V_{SS}$ .

## 26.4 Data Flash

### 26.4.1 Data flash overview

In addition to 8 to 32 KB of code flash memory, the RL78/L12 includes 2 KB of data flash memory for storing data.



<R> An overview of the data flash memory is provided below. For details of a method for rewriting the data flash memory, refer to RL78 Family Data Flash Library User's Manual.

- The data flash memory can be written to by using the flash memory programmer or an external device
- Programming is performed in 8-bit units
- Blocks can be deleted in 1 KB units

<R>

- The only access by CPU instructions is byte reading (1 clock cycle + wait 3 clock cycles)
- Because the data flash memory is an area exclusively used for data, it cannot be used to execute instructions (code fetching)
- Instructions can be executed from the code flash memory while rewriting the data flash memory (That is, back ground operation (BGO) is supported)
- Accessing the data flash memory is not possible while rewriting the code flash memory (during self programming)
- Because the data flash memory is stopped after a reset ends, the data flash control register (DFLCTL) must be set up in order to use the data flash memory
- Manipulating the DFLCTL register is not possible while rewriting the data flash memory
- Transition the HALT/STOP status is not possible while rewriting the data flash memory

<R> **Caution** The high-speed on-chip oscillator should be kept operating during data flash rewrite. If it is kept stopping, it should be operated (HIOSTOP = 0). The data flash library should be executed after 30  $\mu$ s have elapsed.

<R> **Remark** Refer to flash programming mode, see 26.7 Flash Memory Programming by Self-Programming.

## 26.4.2 Register controlling data flash memory

### 26.4.2.1 Data flash control register (DFLCTL)

This register is used to enable or disable accessing to the data flash.

The DFLCTL register is set by a 1-bit or 8-bit memory manipulation instruction.

Reset input sets this register to 00H.

**Figure 26-6. Format of Data Flash Control Register (DFLCTL)**

Address: F0090H After reset: 00H R/W

|        |   |   |   |   |   |   |   |                                                                 |
|--------|---|---|---|---|---|---|---|-----------------------------------------------------------------|
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | <span style="border: 1px solid black; padding: 0 2px;">0</span> |
| DFLCTL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DFLEN                                                           |

| DFLEN | Data flash access control  |
|-------|----------------------------|
| 0     | Disables data flash access |
| 1     | Enables data flash access  |

**Caution** Manipulating the DFLCTL register is not possible while rewriting the data flash memory.



### 26.4.3 Procedure for accessing data flash memory

The data flash memory is initially stopped after a reset ends and cannot be accessed (read or programmed). To access the memory, perform the following procedure:

<1> Write 1 to bit 0 (DFLEN) of the data flash control register (DFLCTL).

<2> Wait for the setup to finish for software timer. etc.

The time setup takes differs for each main clock mode.

<Setup time for each main clock mode>

- HS (High-speed main): 5  $\mu$ s
- LS (Low-speed main): 720 ns
- LV (Low-voltage main): 10  $\mu$ s

<3> After the wait, the data flash memory can be accessed.

**Cautions** 1. Accessing the data flash memory is not possible during the setup time.

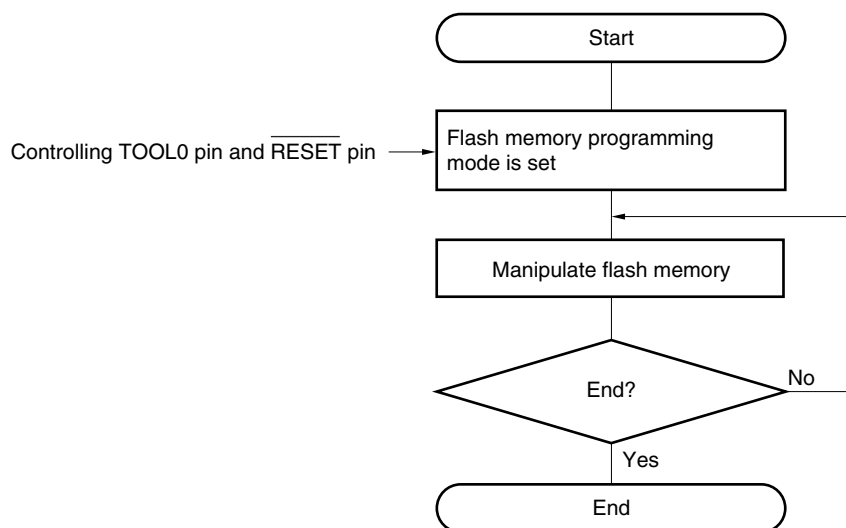
2. Before executing a STOP instruction during the setup time, temporarily clear DFLEN to 0.

## 26.5 Programming Method

### 26.5.1 Controlling flash memory

The following figure illustrates the procedure to manipulate the flash memory.

**Figure 26-7. Flash Memory Manipulation Procedure**



### 26.5.2 Flash memory programming mode

To rewrite the contents of the flash memory, set the RL78/L12 in the flash memory programming mode. To enter the mode, set as follows.

<When programming by using the dedicated flash memory programmer>

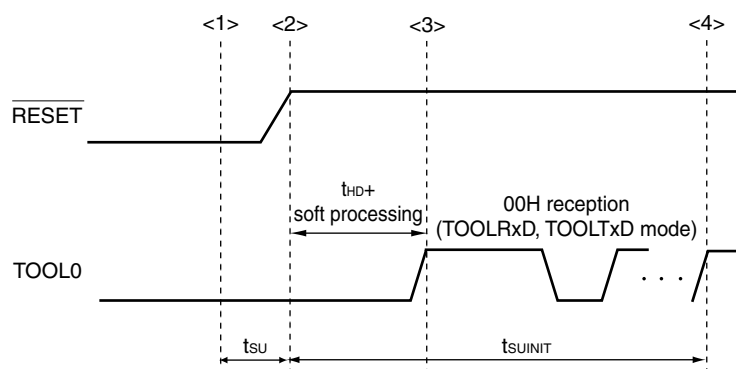
Communication from the dedicated flash memory programmer is performed to automatically switch to the flash memory programming mode.

<When programming by using an external device>

Set the TOOL0 pin to the low level, and then cancel the reset. Keep the TOOL0 pin at the low level from the reset ends to 1 ms + software processing end, and then use UART communication to send the data "00H" from the external device. Finish UART communication within 100 ms after the reset ends.

<R>

**Figure 26-8. Setting of Flash Memory Programming Mode**



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark**  $t_{SUINIT}$ : The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

$t_{SU}$ : How long from when the TOOL0 pin is placed at the low level until an external reset ends

$t_{HD}$ : How long to keep the TOOL0 pin at the low level from when the external and internal resets end (except soft processing time)

**Table 26-4. Relationship Between TOOL0 Pin and Operation Mode After Reset Release**

&lt;R&gt;

| TOOL0            | Operation Mode                |
|------------------|-------------------------------|
| EV <sub>DD</sub> | Normal operation mode         |
| 0                | Flash memory programming mode |

There are two flash memory programming modes for which the voltage range in which to write, erase, or verify data differs.

&lt;R&gt;

**Table 26-5. Programming Modes and Voltages at Which Data Can Be Written, Erased, or Verified**

| Mode                            | Voltages at which data can be written, erased, or verified | Writing Clock Frequency |
|---------------------------------|------------------------------------------------------------|-------------------------|
| Wide voltage mode               | 1.8 V to 5.5 V                                             | 8 MHz (MAX.)            |
|                                 | 2.4 V to 5.5 V                                             | 16 MHz (MAX.)           |
|                                 | 2.7 V to 5.5 V                                             | 24 MHz (MAX.)           |
| Full speed mode <sup>Note</sup> | 2.4 V to 5.5 V                                             | 16 MHz (MAX.)           |
|                                 | 2.7 V to 5.5 V                                             | 24 MHz (MAX.)           |

**Note** This can only be specified if the CMODE1 and CMODE0 bits of the option byte 000C2H are 1.

Specify the mode that corresponds to the voltage range in which to write data. When programming by using the dedicated flash memory programmer, the mode is automatically selected by the voltage setting on GUI.

- Remarks**
1. Using both the wide voltage mode and full speed mode imposes no restrictions on writing, deletion, or verification.
  2. For details about communication commands, see **26.5.4 Communication commands**.

### 26.5.3 Selecting communication mode

Communication mode of the RL78/L12 as follows.

**Table 26-6. Communication Modes**

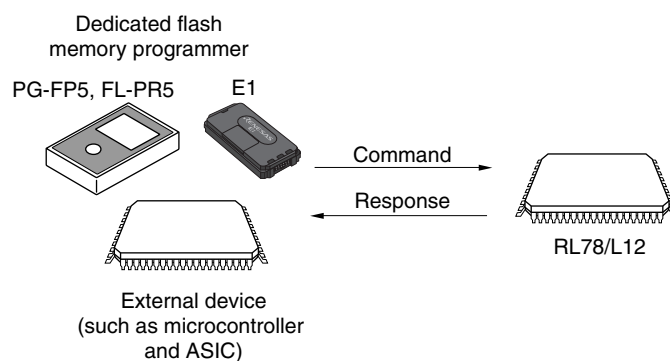
| Communication Mode                                    | Standard Setting <sup>Note 1</sup> |                                                     |           |               | Pins Used           |
|-------------------------------------------------------|------------------------------------|-----------------------------------------------------|-----------|---------------|---------------------|
|                                                       | Port                               | Speed <sup>Note 2</sup>                             | Frequency | Multiply Rate |                     |
| 1-line mode<br>(when flash memory programmer is used) | UART                               | 115200 bps,<br>250000 bps,<br>500000 bps,<br>1 Mbps | —         | —             | TOOL0               |
| Dedicated UART<br>(when external device is used)      | UART                               | 115200 bps,<br>250000 bps,<br>500000 bps,<br>1 Mbps | —         | —             | TOOLTxD,<br>TOOLRxD |

- Notes**
1. Selection items for Standard settings on GUI of the flash memory programmer.
  2. Because factors other than the baud rate error, such as the signal waveform slew, also affect UART communication, thoroughly evaluate the slew as well as the baud rate error.

### 26.5.4 Communication commands

The RL78/L12 communicates with the dedicated flash memory programmer or external device by using commands. The signals sent from the flash memory programmer or external device to the RL78/L12 are called commands, and the signals sent from the RL78/L12 to the dedicated flash memory programmer or external device are called response.

**Figure 26-9. Communication Commands**



The flash memory control commands of the RL78/L12 are listed in the table below. All these commands are issued from the programmer or external device, and the RL78/L12 perform processing corresponding to the respective commands.

**Table 26-7. Flash Memory Control Commands**

| Classification      | Command Name      | Function                                                                                                 |
|---------------------|-------------------|----------------------------------------------------------------------------------------------------------|
| Verify              | Verify            | Compares the contents of a specified area of the flash memory with data transmitted from the programmer. |
| Erase               | Block Erase       | Erases a specified area in the flash memory.                                                             |
| Blank check         | Block Blank Check | Checks if a specified block in the flash memory has been correctly erased.                               |
| Write               | Programming       | Writes data to a specified area in the flash memory.                                                     |
| Getting information | Silicon Signature | Gets the RL78/L12 information (such as the part number, flash memory, and programming firmware version). |
|                     | Checksum          | Gets the checksum data for a specified area.                                                             |
| Security            | Security Set      | Sets security information.                                                                               |
|                     | Security Get      | Gets security information.                                                                               |
|                     | Security Release  | Release setting of prohibition of writing.                                                               |
| Others              | Reset             | Used to detect synchronization status of communication.                                                  |
|                     | Baud Rate Set     | Sets baud rate when UART communication mode is selected.                                                 |

The RL78/L12 returns a response for the command issued by the dedicated flash memory programmer or external device. The response names sent from the RL78/L12 are listed below.

**Table 26-8. Response Names**

| Response Name | Function                           |
|---------------|------------------------------------|
| ACK           | Acknowledges command/data.         |
| NAK           | Acknowledges illegal command/data. |

### 26.5.5 Description of signature data

When the “silicon signature” command is performed, the RL78/L12 information (such as the part number, flash memory configuration, and programming firmware version) can be obtained.

Table 26-9 and 26-10 show signature data list and example of signature data list.

**Table 26-9. Signature Data List**

| Field name                          | Description                                                                                                                | Number of transmit data |
|-------------------------------------|----------------------------------------------------------------------------------------------------------------------------|-------------------------|
| Device code                         | The serial number assigned to the device                                                                                   | 3 bytes                 |
| Device name                         | Device name (ASCII code)                                                                                                   | 10 bytes                |
| Code flash memory area last address | Last address of code flash memory area<br>(Sent from lower address.<br>Example. 00000H to 07FFFH (32 KB) → FFH, 7FH, 00H)  | 3 bytes                 |
| Data flash memory area last address | Last address of data flash memory area<br>(Sent from lower address.<br>Example. F1000H to F17FFH (1.5 KB) → FFH, 17H, 0FH) | 3 bytes                 |
| Firmware version                    | Version information of firmware for programming<br>(Sent from upper address.<br>Example. From Ver. 1.23 → 01H, 02H, 03H)   | 3 bytes                 |

**Table 26-10. Example of Signature Data**

| Field name                          | Description                                         | Number of transmit data | Data (hexadecimal)                                                                                                   |
|-------------------------------------|-----------------------------------------------------|-------------------------|----------------------------------------------------------------------------------------------------------------------|
| <R> Device code                     | RL78 protocol A                                     | 3 bytes                 | 10<br>00<br>06                                                                                                       |
| Device name                         | R5F10RLC                                            | 10 bytes                | 52 = “R”<br>35 = “5”<br>46 = “F”<br>31 = “1”<br>30 = “0”<br>52 = “R”<br>4C = “L”<br>43 = “C”<br>20 = “ ”<br>20 = “ ” |
| Code flash memory area last address | Code flash memory area<br>00000H to 07FFFH (32 KB)  | 3 bytes                 | FF<br>7F<br>00                                                                                                       |
| Data flash memory area last address | Data flash memory area<br>F1000H to F17FFH (1.5 KB) | 3 bytes                 | FF<br>17<br>0F                                                                                                       |
| Firmware version                    | Ver.1.23                                            | 3 bytes                 | 01<br>02<br>03                                                                                                       |

## 26.6 Security Settings

The RL78/L12 supports a security function that prohibits rewriting the user program written to the internal flash memory, so that the program cannot be changed by an unauthorized person.

The operations shown below can be performed using the Security Set command.

- Disabling block erase

Execution of the block erase command for a specific block in the flash memory is prohibited during on-board/off-board programming. However, blocks can be erased by means of self programming.

- Disabling write

Execution of the write command for entire blocks in the flash memory is prohibited during on-board/off-board programming. However, blocks can be written by means of self programming.

<R> 

- Disabling rewriting boot cluster 0

Execution of the block erase command and write command on boot cluster 0 (00000H to 00FFFH) in the flash memory is prohibited by this setting.

<R> After the security settings are specified, releasing the security settings by the Security Release command is enabled by a reset.

The block erase, write commands and rewriting boot cluster 0 are enabled by the default setting when the flash memory is shipped. The security settings can only be specified during on-board/off-board programming. Each security setting can be used in combination.

Table 26-11 shows the relationship between the erase and write commands when the RL78/L12 security function is enabled.

<R> **Caution** The security function of the flash programmer does not support self-programming.

**Remark** To prohibit writing and erasing during self-programming, use the flash shield window function (see 26.7.1 for detail).

&lt;R&gt;

**Table 26-11. Relationship Between Enabling Security Function and Command****(1) During on-board/off-board programming**

| Valid Security                          | Executed Command                 |                                   |
|-----------------------------------------|----------------------------------|-----------------------------------|
|                                         | Block Erase                      | Write                             |
| Prohibition of block erase              | Blocks cannot be erased.         | Can be performed. <sup>Note</sup> |
| Prohibition of writing                  | Blocks can be erased.            | Cannot be performed.              |
| Prohibition of rewriting boot cluster 0 | Boot cluster 0 cannot be erased. | Boot cluster 0 cannot be written. |

**Note** Confirm that no data has been written to the write area. Because data cannot be erased after block erase is prohibited, do not write data if the data has not been erased.

**(2) During self programming**

| Valid Security                          | Executed Command                 |                                   |
|-----------------------------------------|----------------------------------|-----------------------------------|
|                                         | Block Erase                      | Write                             |
| Prohibition of block erase              | Blocks can be erased.            | Can be performed.                 |
| Prohibition of writing                  |                                  |                                   |
| Prohibition of rewriting boot cluster 0 | Boot cluster 0 cannot be erased. | Boot cluster 0 cannot be written. |

**Remark** To prohibit writing and erasing during self-programming, use the flash shield window function (see **26.7.1** for detail).

&lt;R&gt;

**Table 26-12. Setting Security in Each Programming Mode****(1) On-board/off-board programming**

| Security                                | Security Setting                                       | How to Disable Security Setting  |
|-----------------------------------------|--------------------------------------------------------|----------------------------------|
| Prohibition of block erase              | Set via GUI of dedicated flash memory programmer, etc. | Cannot be disabled after set.    |
| Prohibition of writing                  |                                                        | Execute security release command |
| Prohibition of rewriting boot cluster 0 |                                                        | Cannot be disabled after set.    |

**Caution** The security release command can be applied only when the security is not set as the block erase prohibition and the boot cluster 0 rewrite prohibition with code flash memory area and data flash memory area being blanks.



## 26.7 Flash Memory Programming by Self-Programming

The RL78/L12 supports a self-programming function that can be used to rewrite the flash memory via a user program. Because this function allows a user application to rewrite the flash memory by using the RL78/L12 self-programming library, it can be used to upgrade the program in the field.

- Cautions**
- 1. The self-programming function cannot be used when the CPU operates with the subsystem clock.
  - 2. Interrupt servicing is prohibited during self-programming. Execute the self-programming library in the state where the IE flag is cleared (0) by the DI instruction.
  - 3. When enabling RAM parity error resets (RPERDIS = 0), be sure to initialize the RAM area to use + 10 bytes before overwriting.
  - 4. The high-speed on-chip oscillator should be kept operating during self-programming. If it is kept stopping, it should be operated (HIOSTOP = 0). The self-programming library should be executed after 30  $\mu$ s have elapsed.

- Remarks**
- 1. For details of the self-programming function and the RL78/L12 self-programming library, refer to **RL78 Microcontroller Self Programming Library Type01 User's Manual (R01AN0350E)**.
  - 2. For details of the time required to execute self programming, see the notes on use that accompany the flash self programming library tool.

Similar to when writing data by using the flash memory programmer, there are two flash memory programming modes for which the voltage range in which to write, erase, or verify data differs.

**Table 26-13. Programming Modes and Voltages at Which Data Can Be Written, Erased, or Verified**

| Mode                            | Voltages at which data can be written, erased, or verified | Writing Clock Frequency |
|---------------------------------|------------------------------------------------------------|-------------------------|
| Wide voltage mode               | 1.8 V to 5.5 V                                             | 8 MHz (MAX.)            |
|                                 | 2.4 V to 5.5 V                                             | 16 MHz (MAX.)           |
|                                 | 2.7 V to 5.5 V                                             | 24 MHz (MAX.)           |
| Full speed mode <sup>Note</sup> | 2.4 V to 5.5 V                                             | 16 MHz (MAX.)           |
|                                 | 2.7 V to 5.5 V                                             | 24 MHz (MAX.)           |

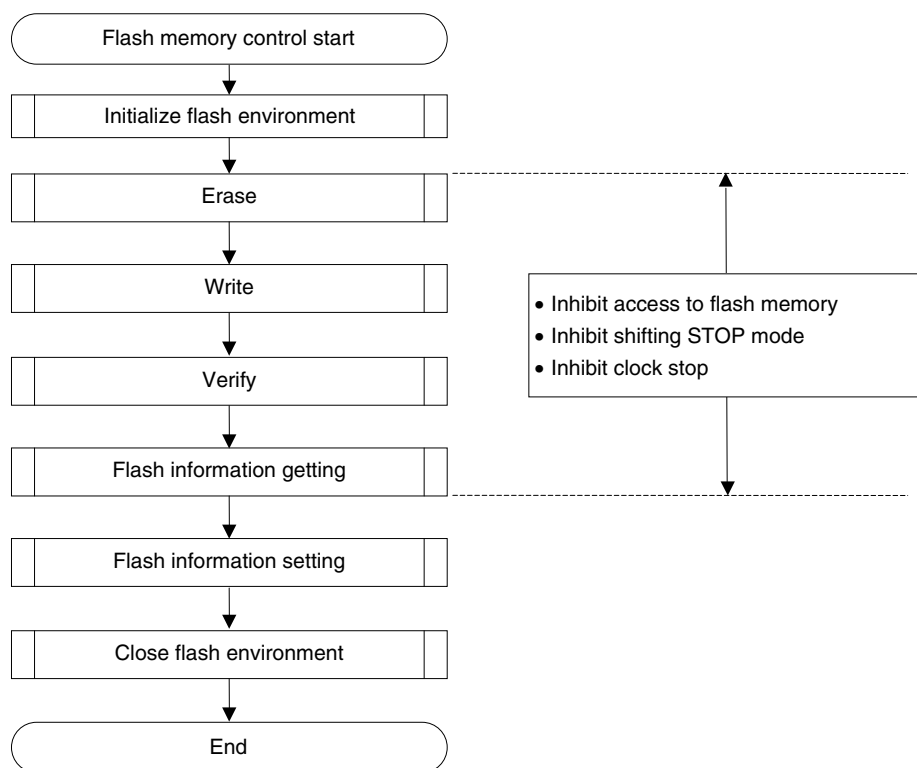
**Note** This can only be specified if the CMODE1 and CMODE0 bits of the option byte 000C2H are 1.

Specify the mode that corresponds to the voltage range in which to write data. If the argument fsl\_flash\_voltage\_u08 is other than 00H when the FSL\_Init function of the self programming library provided by Renesas Electronics is executed, wide-voltage mode is specified. If the argument is 00H, full-speed mode is specified.

- Remarks**
- 1. Using both the wide voltage mode and full speed mode imposes no restrictions on writing, deletion, or verification.
  - 2. For details of the self-programming function and the RL78/L12 self-programming library, refer to **RL78 Microcontroller Self Programming Library Type01 User's Manual (R01AN0350E)**.

The following figure illustrates a flow of rewriting the flash memory by using a self programming library.

**Figure 26-10. Flow of Self Programming (Rewriting Flash Memory)**



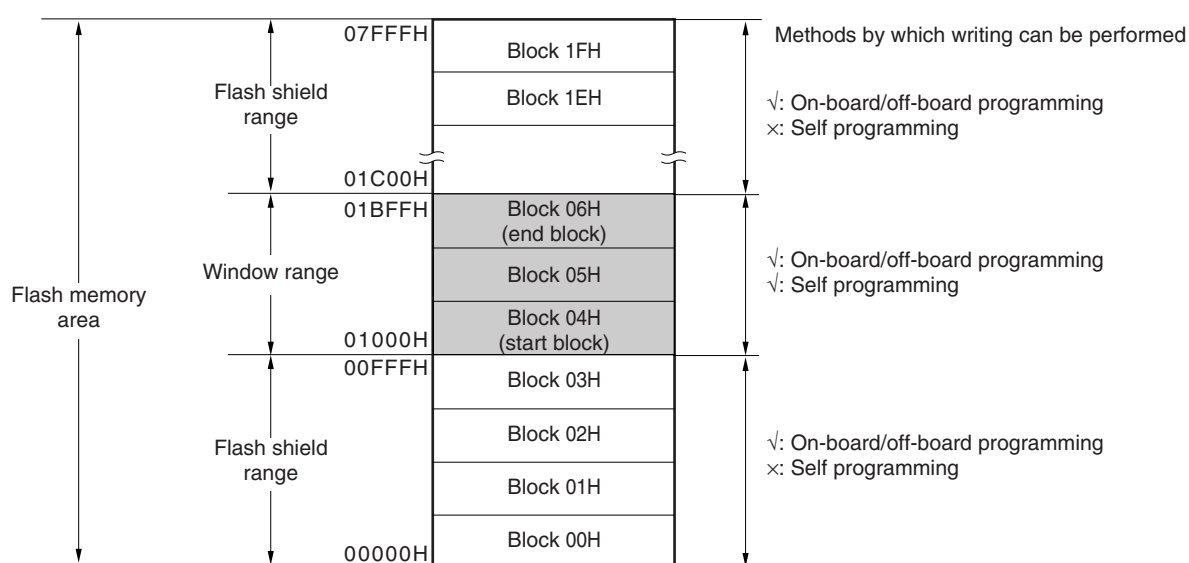
### 26.7.1 Flash shield window function

The flash shield window function is provided as one of the security functions for self programming. It disables writing to and erasing areas outside the range specified as a window only during self programming.

The window range can be set by specifying the start and end blocks. The window range can only be specified and changed during on-board/off-board programming.

Writing to and erasing areas outside the window range are disabled during self programming. During on-board/off-board programming, however, areas outside the range specified as a window can be written and erased.

**Figure 26-11. Flash Shield Window Setting Example**  
(Target Devices: R5F10Rx C (x = B, F, G, J, L), Start Block: 04H, End Block: 06H)



**Caution** The flash shield window can only be used for the code flash memory (and is not supported for the data flash memory).

<R> **Table 26-14. Relationship between Flash Shield Window Function Setting/Change Methods and Commands**

| Programming conditions         | Window Range Setting/Change Methods                                                      | Execution Commands                                      |                                                   |
|--------------------------------|------------------------------------------------------------------------------------------|---------------------------------------------------------|---------------------------------------------------|
|                                |                                                                                          | Block erase                                             | Write                                             |
| On-board/Off-board programming | Specify the starting and ending blocks on GUI of dedicated flash memory programmer, etc. | Block erasing is enabled also outside the window range. | Writing is enabled also outside the window range. |

**Remark** See 26.6 Security Settings to prohibit writing/erasing during on-board/off-board programming.

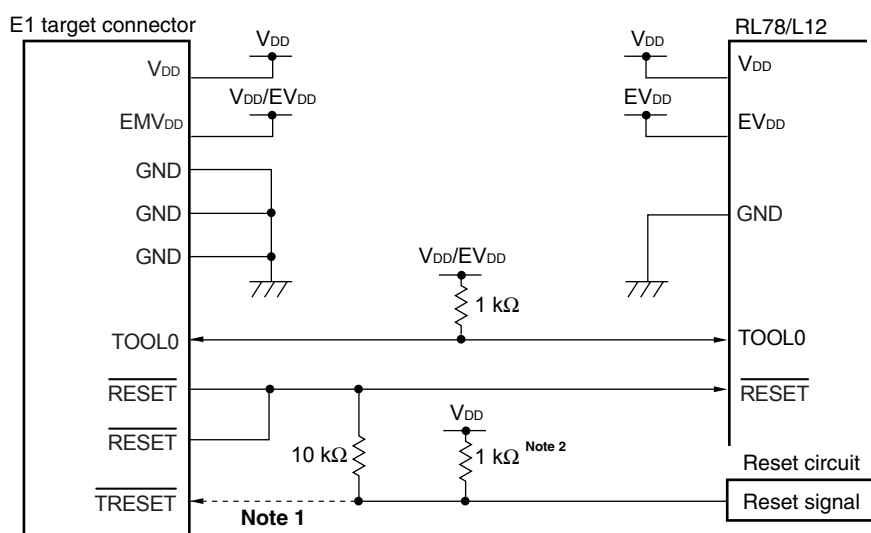
## CHAPTER 27 ON-CHIP DEBUG FUNCTION

## 27.1 Connecting E1 On-chip Debugging Emulator to RL78/L12

The RL78/L12 uses the  $V_{DD}$ ,  $\overline{\text{RESET}}$ , TOOL0, and  $V_{SS}$  pins to communicate with the host machine via an E1 on-chip debugging emulator. Serial communication is performed by using a single-line UART that uses the TOOL0 pin.

**Caution** The RL78/L12 has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Figure 27-1. Connection Example of E1 On-chip Debugging Emulator and RL78/L12



**Notes** 1. Connecting the dotted line is not necessary during flash programming.

2. If the reset circuit on the target system does not have a buffer and generates a reset signal only with resistors and capacitors, this pull-up resistor is not necessary.

**Caution** This circuit diagram is assumed that the reset signal outputs from an N-ch O.D. buffer (output resistor: 100  $\Omega$  or less)

## 27.2 On-Chip Debug Security ID

The RL78/L12 has an on-chip debug operation control bit in the flash memory at 000C3H (see **CHAPTER 25 OPTION BYTE**) and an on-chip debug security ID setting area at 000C4H to 000CDH, to prevent third parties from reading memory content.

**Table 27-1. On-Chip Debug Security ID**

| Address          | On-Chip Debug Security ID |
|------------------|---------------------------|
| 000C4H to 000CDH | Any ID code of 10 bytes   |

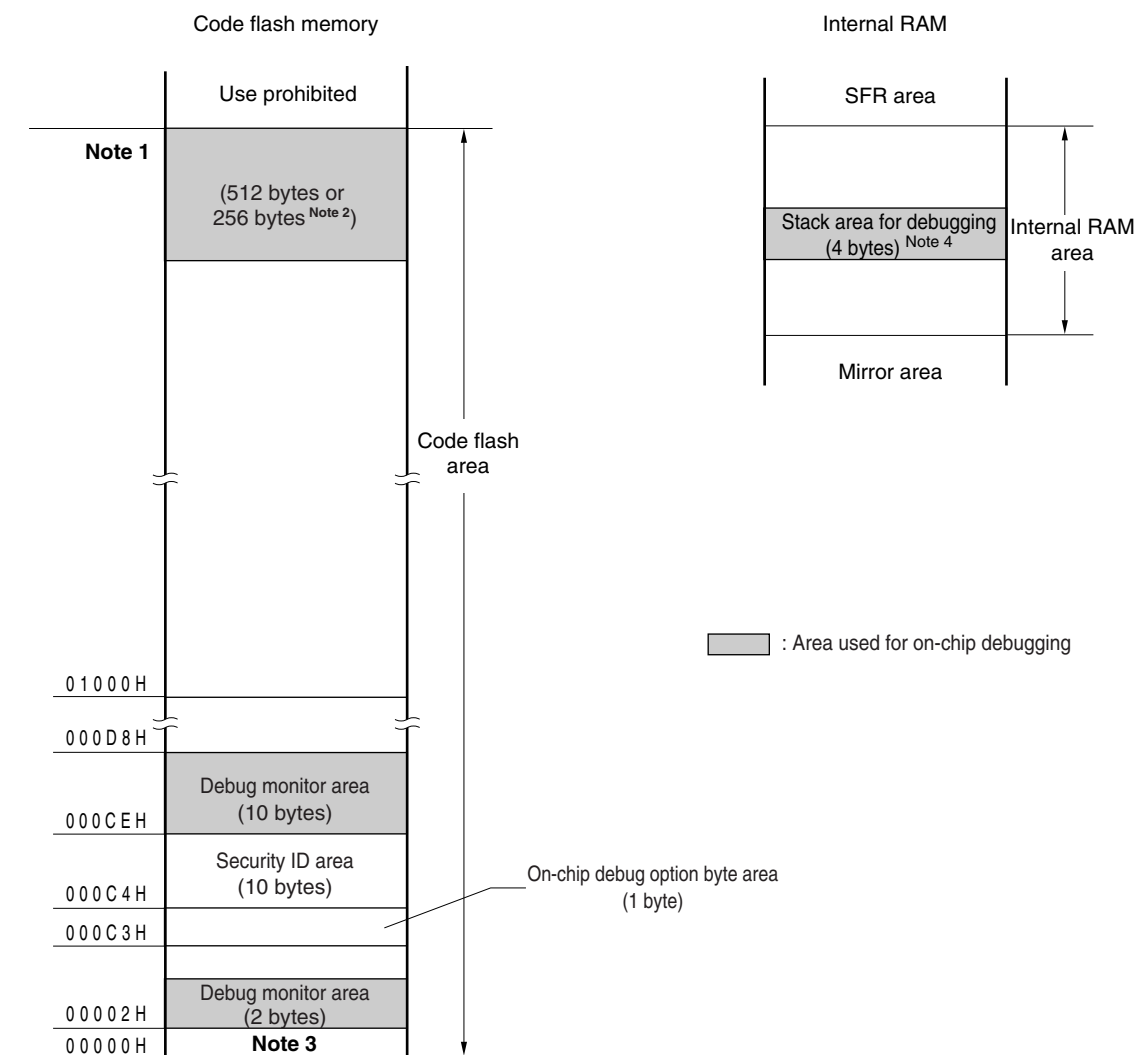
## 27.3 Securing of User Resources

To perform communication between the RL78/L12 and E1 on-chip debugging emulator, as well as each debug function, the securing of memory space must be done beforehand.

If Renesas Electronics assembler or compiler is used, the items can be set by using linker options.

### (1) Securement of memory space

The shaded portions in Figure 27-2 are the areas reserved for placing the debug monitor program, so user programs or data cannot be allocated in these spaces. When using the on-chip debug function, these spaces must be secured so as not to be used by the user program. Moreover, this area must not be rewritten by the user program.

**Figure 27-2. Memory Spaces Where Debug Monitor Programs Are Allocated**

**Notes 1.** Address differs depending on products as follows.

| Products (code flash memory capacity) | Address of <b>Note 1</b> |
|---------------------------------------|--------------------------|
| R5F10Rx8 (x = B, F, G, J)             | 01FFFH                   |
| R5F10RxA (x = B, F, G, J, L)          | 03FFFH                   |
| R5F10RxC (x = B, F, G, J, L)          | 07FFFH                   |

- When real-time RAM monitor (RRM) function and dynamic memory modification (DMM) function are not used, it is 256 bytes.
- In debugging, reset vector is rewritten to address allocated to a monitor program.
- Since this area is allocated immediately before the stack area, the address of this area varies depending on the stack increase and decrease. That is, 4 extra bytes are consumed for the stack area used. When using self-programming, 12 extra bytes are consumed for the stack area used.

## CHAPTER 28 BCD CORRECTION CIRCUIT

### 28.1 BCD Correction Circuit Function

The result of addition/subtraction of the BCD (binary-coded decimal) code and BCD code can be obtained as BCD code with this circuit.

The decimal correction operation result is obtained by performing addition/subtraction having the A register as the operand and then adding/ subtracting the BCD correction result register (BCDADJ).

### 28.2 Registers Used by BCD Correction Circuit

The BCD correction circuit uses the following registers.

- BCD correction result register (BCDADJ)

#### 28.2.1 BCD correction result register (BCDADJ)

The BCDADJ register stores correction values for obtaining the add/subtract result as BCD code through add/subtract instructions using the A register as the operand.

The value read from the BCDADJ register varies depending on the value of the A register when it is read and those of the CY and AC flags.

The BCDADJ register is read by an 8-bit memory manipulation instruction.

Reset input sets this register to undefined.

**Figure 28-1. Format of BCD Correction Result Register (BCDADJ)**

|                 |                        |   |   |   |   |   |   |   |
|-----------------|------------------------|---|---|---|---|---|---|---|
| Address: F00FEH | After reset: undefined | R |   |   |   |   |   |   |
| Symbol          | 7                      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BCDADJ          |                        |   |   |   |   |   |   |   |

### 28.3 BCD Correction Circuit Operation

The basic operation of the BCD correction circuit is as follows.

**(1) Addition: Calculating the result of adding a BCD code value and another BCD code value by using a BCD code value**

- <1> The BCD code value to which addition is performed is stored in the A register.
- <2> By adding the value of the A register and the second operand (value of one more BCD code to be added) as are in binary, the binary operation result is stored in the A register and the correction value is stored in the BCD correction result register (BCDADJ).
- <3> Decimal correction is performed by adding in binary the value of the A register (addition result in binary) and the BCDADJ register (correction value), and the correction result is stored in the A register and CY flag.

**Caution** The value read from the BCDADJ register varies depending on the value of the A register when it is read and those of the CY and AC flags. Therefore, execute the instruction <3> after the instruction <2> instead of executing any other instructions. To perform BCD correction in the interrupt enabled state, saving and restoring the A register is required within the interrupt function. PSW (CY flag and AC flag) is restored by the RETI instruction.

An example is shown below.

Examples 1:  $99 + 89 = 188$

| Instruction          | A Register | CY Flag | AC Flag | BCDADJ Register |
|----------------------|------------|---------|---------|-----------------|
| MOV A, #99H ; <1>    | 99H        | –       | –       | –               |
| ADD A, #89H ; <2>    | 22H        | 1       | 1       | 66H             |
| ADD A, !BCDADJ ; <3> | 88H        | 1       | 0       | –               |

Examples 2:  $85 + 15 = 100$

| Instruction          | A Register | CY Flag | AC Flag | BCDADJ Register |
|----------------------|------------|---------|---------|-----------------|
| MOV A, #85H ; <1>    | 85H        | –       | –       | –               |
| ADD A, #15H ; <2>    | 9AH        | 0       | 0       | 66H             |
| ADD A, !BCDADJ ; <3> | 00H        | 1       | 1       | –               |

Examples 3:  $80 + 80 = 160$

| Instruction          | A Register | CY Flag | AC Flag | BCDADJ Register |
|----------------------|------------|---------|---------|-----------------|
| MOV A, #80H ; <1>    | 80H        | –       | –       | –               |
| ADD A, #80H ; <2>    | 00H        | 1       | 0       | 60H             |
| ADD A, !BCDADJ ; <3> | 60H        | 1       | 0       | –               |



**(2) Subtraction: Calculating the result of subtracting a BCD code value from another BCD code value by using a BCD code value**

- <1> The BCD code value from which subtraction is performed is stored in the A register.
- <2> By subtracting the value of the second operand (value of BCD code to be subtracted) from the A register as is in binary, the calculation result in binary is stored in the A register, and the correction value is stored in the BCD correction result register (BCDADJ).
- <3> Decimal correction is performed by subtracting the value of the BCDADJ register (correction value) from the A register (subtraction result in binary) in binary, and the correction result is stored in the A register and CY flag.

**Caution** The value read from the BCDADJ register varies depending on the value of the A register when it is read and those of the CY and AC flags. Therefore, execute the instruction <3> after the instruction <2> instead of executing any other instructions. To perform BCD correction in the interrupt enabled state, saving and restoring the A register is required within the interrupt function. PSW (CY flag and AC flag) is restored by the RETI instruction.

An example is shown below.

Example:  $91 - 52 = 39$

| Instruction          | A Register | CY Flag | AC Flag | BCDADJ Register |
|----------------------|------------|---------|---------|-----------------|
| MOV A, #91H ; <1>    | 91H        | –       | –       | –               |
| SUB A, #52H ; <2>    | 3FH        | 0       | 1       | 06H             |
| SUB A, !BCDADJ ; <3> | 39H        | 0       | 0       | –               |

## CHAPTER 29 INSTRUCTION SET

This chapter lists the instructions in the RL78 microcontroller instruction set. For details of each operation and operation code, refer to the separate document **RL78 Family User's Manual: software**.

## 29.1 Conventions Used in Operation List

### 29.1.1 Operand identifiers and specification methods

Operands are described in the “Operand” column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more description methods, select one of them. Alphabetic letters in capitals and the symbols, #, !, !!, \$, \$!, [ ], and ES: are keywords and are described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: 16-bit absolute address specification
- !!: 20-bit absolute address specification
- \$: 8-bit relative address specification
- \$!: 16-bit relative address specification
- [ ]: Indirect address specification
- ES:: Extension address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #, !, !!, \$, \$!, [ ], and ES: symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

**Table 29-1. Operand Identifiers and Specification Methods**

| Identifier | Description Method                                                                                                         |
|------------|----------------------------------------------------------------------------------------------------------------------------|
| r          | X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)                                                             |
| rp         | AX (RP0), BC (RP1), DE (RP2), HL (RP3)                                                                                     |
| sfr        | Special-function register symbol (SFR symbol) FFF00H to FFFFFH                                                             |
| sfrp       | Special-function register symbols (16-bit manipulatable SFR symbol. Even addresses only <sup>Note</sup> ) FFF00H to FFFFFH |
| saddr      | FFE20H to FFF1FH Immediate data or labels                                                                                  |
| saddrp     | FFE20H to FF1FH Immediate data or labels (even addresses only <sup>Note</sup> )                                            |
| addr20     | 00000H to FFFFFH Immediate data or labels                                                                                  |
| addr16     | 0000H to FFFFH Immediate data or labels (only even addresses for 16-bit data transfer instructions <sup>Note</sup> )       |
| addr5      | 0080H to 00BFH Immediate data or labels (even addresses only)                                                              |
| word       | 16-bit immediate data or label                                                                                             |
| byte       | 8-bit immediate data or label                                                                                              |
| bit        | 3-bit immediate data or label                                                                                              |
| RBn        | RB0 to RB3                                                                                                                 |

**Note** Bit 0 = 0 when an odd address is specified.

**Remark** The special function registers can be described to operand sfr as symbols. See **Table 3-5 SFR List** for the symbols of the special function registers. The extended special function registers can be described to operand laddr16 as symbols. See **Table 3-6 Extended SFR (2nd SFR) List** for the symbols of the extended special function registers.

### 29.1.2 Description of operation column

The operation when the instruction is executed is shown in the “Operation” column using the following symbols.

**Table 29-2. Symbols in “Operation” Column**

| Symbol                                           | Function                                                                                                            |
|--------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|
| A                                                | A register; 8-bit accumulator                                                                                       |
| X                                                | X register                                                                                                          |
| B                                                | B register                                                                                                          |
| C                                                | C register                                                                                                          |
| D                                                | D register                                                                                                          |
| E                                                | E register                                                                                                          |
| H                                                | H register                                                                                                          |
| L                                                | L register                                                                                                          |
| ES                                               | ES register                                                                                                         |
| CS                                               | CS register                                                                                                         |
| AX                                               | AX register pair; 16-bit accumulator                                                                                |
| BC                                               | BC register pair                                                                                                    |
| DE                                               | DE register pair                                                                                                    |
| HL                                               | HL register pair                                                                                                    |
| PC                                               | Program counter                                                                                                     |
| SP                                               | Stack pointer                                                                                                       |
| PSW                                              | Program status word                                                                                                 |
| CY                                               | Carry flag                                                                                                          |
| AC                                               | Auxiliary carry flag                                                                                                |
| Z                                                | Zero flag                                                                                                           |
| RBS                                              | Register bank select flag                                                                                           |
| IE                                               | Interrupt request enable flag                                                                                       |
| ()                                               | Memory contents indicated by address or register contents in parentheses                                            |
| X <sub>H</sub> , X <sub>L</sub>                  | 16-bit registers: X <sub>H</sub> = higher 8 bits, X <sub>L</sub> = lower 8 bits                                     |
| X <sub>S</sub> , X <sub>H</sub> , X <sub>L</sub> | 20-bit registers: X <sub>S</sub> = (bits 19 to 16), X <sub>H</sub> = (bits 15 to 8), X <sub>L</sub> = (bits 7 to 0) |
| ^                                                | Logical product (AND)                                                                                               |
| ∨                                                | Logical sum (OR)                                                                                                    |
| ⊕                                                | Exclusive logical sum (exclusive OR)                                                                                |
| —                                                | Inverted data                                                                                                       |
| addr5                                            | 16-bit immediate data (even addresses only in 0080H to 00BFH)                                                       |
| addr16                                           | 16-bit immediate data                                                                                               |
| addr20                                           | 20-bit immediate data                                                                                               |
| jdisp8                                           | Signed 8-bit data (displacement value)                                                                              |
| jdisp16                                          | Signed 16-bit data (displacement value)                                                                             |

### 29.1.3 Description of flag operation column

The change of the flag value when the instruction is executed is shown in the “Flag” column using the following symbols.

**Table 29-3. Symbols in “Flag” Column**

| Symbol  | Change of Flag Value                |
|---------|-------------------------------------|
| (Blank) | Unchanged                           |
| 0       | Cleared to 0                        |
| 1       | Set to 1                            |
| ×       | Set/cleared according to the result |
| R       | Previously saved value is restored  |

### 29.1.4 PREFIX instruction

Instructions with “ES:” have a PREFIX operation code as a prefix to extend the accessible data area to the 1 MB space (00000H to FFFFFH), by adding the ES register value to the 64 KB space from F0000H to FFFFFH. When a PREFIX operation code is attached as a prefix to the target instruction, only one instruction immediately after the PREFIX operation code is executed as the addresses with the ES register value added.

A interrupt and DMA transfer are not acknowledged between a PREFIX instruction code and the instruction immediately after.

**Table 29-4. Use Example of PREFIX Operation Code**

| Instruction           | Opcode |         |         |       |       |
|-----------------------|--------|---------|---------|-------|-------|
|                       | 1      | 2       | 3       | 4     | 5     |
| MOV !addr16, #byte    | CFH    | !addr16 |         | #byte | –     |
| MOV ES:!addr16, #byte | 11H    | CFH     | !addr16 |       | #byte |
| MOV A, [HL]           | 8BH    | –       | –       | –     | –     |
| MOV A, ES:[HL]        | 11H    | 8BH     | –       | –     | –     |

**Caution** Set the ES register value with MOV ES, A, etc., before executing the PREFIX instruction.

## 29.2 Operation List

Table 29-5. Operation List (1/17)

| Instruction Group   | Mnemonic | Operands                   | Bytes | Clocks |        | Clocks                                                        | Flag |    |    |
|---------------------|----------|----------------------------|-------|--------|--------|---------------------------------------------------------------|------|----|----|
|                     |          |                            |       | Note 1 | Note 2 |                                                               | Z    | AC | CY |
| 8-bit data transfer | MOV      | r, #byte                   | 2     | 1      | —      | $r \leftarrow \text{byte}$                                    |      |    |    |
|                     |          | PSW, #byte                 | 3     | 3      | —      | $\text{PSW} \leftarrow \text{byte}$                           | ×    | ×  | ×  |
|                     |          | CS, #byte                  | 3     | 1      | —      | $\text{CS} \leftarrow \text{byte}$                            |      |    |    |
|                     |          | ES, #byte                  | 2     | 1      | —      | $\text{ES} \leftarrow \text{byte}$                            |      |    |    |
|                     |          | !addr16, #byte             | 4     | 1      | —      | $(\text{addr16}) \leftarrow \text{byte}$                      |      |    |    |
|                     |          | ES:!addr16, #byte          | 5     | 2      | —      | $(\text{ES}, \text{addr16}) \leftarrow \text{byte}$           |      |    |    |
|                     |          | saddr, #byte               | 3     | 1      | —      | $(\text{saddr}) \leftarrow \text{byte}$                       |      |    |    |
|                     |          | sfr, #byte                 | 3     | 1      | —      | $\text{sfr} \leftarrow \text{byte}$                           |      |    |    |
|                     |          | [DE+byte], #byte           | 3     | 1      | —      | $(\text{DE}+\text{byte}) \leftarrow \text{byte}$              |      |    |    |
|                     |          | ES:[DE+byte], #byte        | 4     | 2      | —      | $((\text{ES}, \text{DE})+\text{byte}) \leftarrow \text{byte}$ |      |    |    |
|                     |          | [HL+byte], #byte           | 3     | 1      | —      | $(\text{HL}+\text{byte}) \leftarrow \text{byte}$              |      |    |    |
|                     |          | ES:[HL+byte], #byte        | 4     | 2      | —      | $((\text{ES}, \text{HL})+\text{byte}) \leftarrow \text{byte}$ |      |    |    |
|                     |          | [SP+byte], #byte           | 3     | 1      | —      | $(\text{SP}+\text{byte}) \leftarrow \text{byte}$              |      |    |    |
|                     |          | word[B], #byte             | 4     | 1      | —      | $(\text{B}+\text{word}) \leftarrow \text{byte}$               |      |    |    |
|                     |          | ES:word[B], #byte          | 5     | 2      | —      | $((\text{ES}, \text{B})+\text{word}) \leftarrow \text{byte}$  |      |    |    |
|                     |          | word[C], #byte             | 4     | 1      | —      | $(\text{C}+\text{word}) \leftarrow \text{byte}$               |      |    |    |
|                     |          | ES:word[C], #byte          | 5     | 2      | —      | $((\text{ES}, \text{C})+\text{word}) \leftarrow \text{byte}$  |      |    |    |
|                     |          | word[BC], #byte            | 4     | 1      | —      | $(\text{BC}+\text{word}) \leftarrow \text{byte}$              |      |    |    |
|                     |          | ES:word[BC], #byte         | 5     | 2      | —      | $((\text{ES}, \text{BC})+\text{word}) \leftarrow \text{byte}$ |      |    |    |
|                     |          | A, r <small>Note 3</small> | 1     | 1      | —      | $\text{A} \leftarrow r$                                       |      |    |    |
|                     |          | r, A <small>Note 3</small> | 1     | 1      | —      | $r \leftarrow \text{A}$                                       |      |    |    |
|                     |          | A, PSW                     | 2     | 1      | —      | $\text{A} \leftarrow \text{PSW}$                              |      |    |    |
|                     |          | PSW, A                     | 2     | 3      | —      | $\text{PSW} \leftarrow \text{A}$                              | ×    | ×  | ×  |
|                     |          | A, CS                      | 2     | 1      | —      | $\text{A} \leftarrow \text{CS}$                               |      |    |    |
|                     |          | CS, A                      | 2     | 1      | —      | $\text{CS} \leftarrow \text{A}$                               |      |    |    |
|                     |          | A, ES                      | 2     | 1      | —      | $\text{A} \leftarrow \text{ES}$                               |      |    |    |
|                     |          | ES, A                      | 2     | 1      | —      | $\text{ES} \leftarrow \text{A}$                               |      |    |    |
|                     |          | A, !addr16                 | 3     | 1      | 4      | $\text{A} \leftarrow (\text{addr16})$                         |      |    |    |
|                     |          | A, ES:!addr16              | 4     | 2      | 5      | $\text{A} \leftarrow (\text{ES}, \text{addr16})$              |      |    |    |
|                     |          | !addr16, A                 | 3     | 1      | —      | $(\text{addr16}) \leftarrow \text{A}$                         |      |    |    |
|                     |          | ES:!addr16, A              | 4     | 2      | —      | $(\text{ES}, \text{addr16}) \leftarrow \text{A}$              |      |    |    |
|                     |          | A, saddr                   | 2     | 1      | —      | $\text{A} \leftarrow (\text{saddr})$                          |      |    |    |
|                     |          | saddr, A                   | 2     | 1      | —      | $(\text{saddr}) \leftarrow \text{A}$                          |      |    |    |

- Notes**
1. Number of CPU clocks ( $f_{\text{CLK}}$ ) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
  2. Number of CPU clocks ( $f_{\text{CLK}}$ ) when the program memory area is accessed.
  3. Except  $r = \text{A}$

**Remark** Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 29-5. Operation List (2/17)

| Instruction Group   | Mnemonic | Operands        | Bytes | Clocks |        | Clocks                                                | Flag |    |    |
|---------------------|----------|-----------------|-------|--------|--------|-------------------------------------------------------|------|----|----|
|                     |          |                 |       | Note 1 | Note 2 |                                                       | Z    | AC | CY |
| 8-bit data transfer | MOV      | A, sfr          | 2     | 1      | –      | $A \leftarrow \text{sfr}$                             |      |    |    |
|                     |          | sfr, A          | 2     | 1      | –      | $\text{sfr} \leftarrow A$                             |      |    |    |
|                     |          | A, [DE]         | 1     | 1      | 4      | $A \leftarrow (\text{DE})$                            |      |    |    |
|                     |          | [DE], A         | 1     | 1      | –      | $(\text{DE}) \leftarrow A$                            |      |    |    |
|                     |          | A, ES:[DE]      | 2     | 2      | 5      | $A \leftarrow (\text{ES}, \text{DE})$                 |      |    |    |
|                     |          | ES:[DE], A      | 2     | 2      | –      | $(\text{ES}, \text{DE}) \leftarrow A$                 |      |    |    |
|                     |          | A, [HL]         | 1     | 1      | 4      | $A \leftarrow (\text{HL})$                            |      |    |    |
|                     |          | [HL], A         | 1     | 1      | –      | $(\text{HL}) \leftarrow A$                            |      |    |    |
|                     |          | A, ES:[HL]      | 2     | 2      | 5      | $A \leftarrow (\text{ES}, \text{HL})$                 |      |    |    |
|                     |          | ES:[HL], A      | 2     | 2      | –      | $(\text{ES}, \text{HL}) \leftarrow A$                 |      |    |    |
|                     |          | A, [DE+byte]    | 2     | 1      | 4      | $A \leftarrow (\text{DE} + \text{byte})$              |      |    |    |
|                     |          | [DE+byte], A    | 2     | 1      | –      | $(\text{DE} + \text{byte}) \leftarrow A$              |      |    |    |
|                     |          | A, ES:[DE+byte] | 3     | 2      | 5      | $A \leftarrow ((\text{ES}, \text{DE}) + \text{byte})$ |      |    |    |
|                     |          | ES:[DE+byte], A | 3     | 2      | –      | $((\text{ES}, \text{DE}) + \text{byte}) \leftarrow A$ |      |    |    |
|                     |          | A, [HL+byte]    | 2     | 1      | 4      | $A \leftarrow (\text{HL} + \text{byte})$              |      |    |    |
|                     |          | [HL+byte], A    | 2     | 1      | –      | $(\text{HL} + \text{byte}) \leftarrow A$              |      |    |    |
|                     |          | A, ES:[HL+byte] | 3     | 2      | 5      | $A \leftarrow ((\text{ES}, \text{HL}) + \text{byte})$ |      |    |    |
|                     |          | ES:[HL+byte], A | 3     | 2      | –      | $((\text{ES}, \text{HL}) + \text{byte}) \leftarrow A$ |      |    |    |
|                     |          | A, [SP+byte]    | 2     | 1      | –      | $A \leftarrow (\text{SP} + \text{byte})$              |      |    |    |
|                     |          | [SP+byte], A    | 2     | 1      | –      | $(\text{SP} + \text{byte}) \leftarrow A$              |      |    |    |
|                     |          | A, word[B]      | 3     | 1      | 4      | $A \leftarrow (\text{B} + \text{word})$               |      |    |    |
|                     |          | word[B], A      | 3     | 1      | –      | $(\text{B} + \text{word}) \leftarrow A$               |      |    |    |
|                     |          | A, ES:word[B]   | 4     | 2      | 5      | $A \leftarrow ((\text{ES}, \text{B}) + \text{word})$  |      |    |    |
|                     |          | ES:word[B], A   | 4     | 2      | –      | $((\text{ES}, \text{B}) + \text{word}) \leftarrow A$  |      |    |    |
|                     |          | A, word[C]      | 3     | 1      | 4      | $A \leftarrow (\text{C} + \text{word})$               |      |    |    |
|                     |          | word[C], A      | 3     | 1      | –      | $(\text{C} + \text{word}) \leftarrow A$               |      |    |    |
|                     |          | A, ES:word[C]   | 4     | 2      | 5      | $A \leftarrow ((\text{ES}, \text{C}) + \text{word})$  |      |    |    |
|                     |          | ES:word[C], A   | 4     | 2      | –      | $((\text{ES}, \text{C}) + \text{word}) \leftarrow A$  |      |    |    |
|                     |          | A, word[BC]     | 3     | 1      | 4      | $A \leftarrow (\text{BC} + \text{word})$              |      |    |    |
|                     |          | word[BC], A     | 3     | 1      | –      | $(\text{BC} + \text{word}) \leftarrow A$              |      |    |    |
|                     |          | A, ES:word[BC]  | 4     | 2      | 5      | $A \leftarrow ((\text{ES}, \text{BC}) + \text{word})$ |      |    |    |
|                     |          | ES:word[BC], A  | 4     | 2      | –      | $((\text{ES}, \text{BC}) + \text{word}) \leftarrow A$ |      |    |    |

**Notes 1.** Number of CPU clocks ( $f_{\text{CLK}}$ ) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

**2.** Number of CPU clocks ( $f_{\text{CLK}}$ ) when the program memory area is accessed.

**Remark** Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 29-5. Operation List (3/17)

| Instruction Group   | Mnemonic | Operands               | Bytes                             | Clocks |        | Clocks                                       | Flag    |
|---------------------|----------|------------------------|-----------------------------------|--------|--------|----------------------------------------------|---------|
|                     |          |                        |                                   | Note 1 | Note 2 |                                              | Z AC CY |
| 8-bit data transfer | MOV      | A, [HL+B]              | 2                                 | 1      | 4      | $A \leftarrow (HL + B)$                      |         |
|                     |          | [HL+B], A              | 2                                 | 1      | —      | $(HL + B) \leftarrow A$                      |         |
|                     |          | A, ES:[HL+B]           | 3                                 | 2      | 5      | $A \leftarrow ((ES, HL) + B)$                |         |
|                     |          | ES:[HL+B], A           | 3                                 | 2      | —      | $((ES, HL) + B) \leftarrow A$                |         |
|                     |          | A, [HL+C]              | 2                                 | 1      | 4      | $A \leftarrow (HL + C)$                      |         |
|                     |          | [HL+C], A              | 2                                 | 1      | —      | $(HL + C) \leftarrow A$                      |         |
|                     |          | A, ES:[HL+C]           | 3                                 | 2      | 5      | $A \leftarrow ((ES, HL) + C)$                |         |
|                     |          | ES:[HL+C], A           | 3                                 | 2      | —      | $((ES, HL) + C) \leftarrow A$                |         |
|                     |          | X, laddr16             | 3                                 | 1      | 4      | $X \leftarrow (addr16)$                      |         |
|                     |          | X, ES:laddr16          | 4                                 | 2      | 5      | $X \leftarrow (ES, addr16)$                  |         |
|                     |          | X, saddr               | 2                                 | 1      | —      | $X \leftarrow (saddr)$                       |         |
|                     |          | B, laddr16             | 3                                 | 1      | 4      | $B \leftarrow (addr16)$                      |         |
|                     |          | B, ES:laddr16          | 4                                 | 2      | 5      | $B \leftarrow (ES, addr16)$                  |         |
|                     |          | B, saddr               | 2                                 | 1      | —      | $B \leftarrow (saddr)$                       |         |
|                     |          | C, laddr16             | 3                                 | 1      | 4      | $C \leftarrow (addr16)$                      |         |
|                     |          | C, ES:laddr16          | 4                                 | 2      | 5      | $C \leftarrow (ES, addr16)$                  |         |
|                     |          | C, saddr               | 2                                 | 1      | —      | $C \leftarrow (saddr)$                       |         |
|                     |          | ES, saddr              | 3                                 | 1      | —      | $ES \leftarrow (saddr)$                      |         |
|                     | XCH      | A, r <sup>Note 3</sup> | 1 (r = X)<br>2 (other than r = X) | 1      | —      | $A \leftrightarrow r$                        |         |
|                     |          | A, laddr16             | 4                                 | 2      | —      | $A \leftrightarrow (addr16)$                 |         |
|                     |          | A, ES:laddr16          | 5                                 | 3      | —      | $A \leftrightarrow (ES, addr16)$             |         |
|                     |          | A, saddr               | 3                                 | 2      | —      | $A \leftrightarrow (saddr)$                  |         |
|                     |          | A, sfr                 | 3                                 | 2      | —      | $A \leftrightarrow sfr$                      |         |
|                     |          | A, [DE]                | 2                                 | 2      | —      | $A \leftrightarrow (DE)$                     |         |
|                     |          | A, ES:[DE]             | 3                                 | 3      | —      | $A \leftrightarrow (ES, DE)$                 |         |
|                     |          | A, [HL]                | 2                                 | 2      | —      | $A \leftrightarrow (HL)$                     |         |
|                     |          | A, ES:[HL]             | 3                                 | 3      | —      | $A \leftrightarrow (ES, HL)$                 |         |
|                     |          | A, [DE+byte]           | 3                                 | 2      | —      | $A \leftrightarrow (DE + \text{byte})$       |         |
|                     |          | A, ES:[DE+byte]        | 4                                 | 3      | —      | $A \leftrightarrow ((ES, DE) + \text{byte})$ |         |
|                     |          | A, [HL+byte]           | 3                                 | 2      | —      | $A \leftrightarrow (HL + \text{byte})$       |         |
|                     |          | A, ES:[HL+byte]        | 4                                 | 3      | —      | $A \leftrightarrow ((ES, HL) + \text{byte})$ |         |

- Notes**
1. Number of CPU clocks ( $f_{CLK}$ ) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
  2. Number of CPU clocks ( $f_{CLK}$ ) when the program memory area is accessed.
  3. Except  $r = A$

**Remark** Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.



Table 29-5. Operation List (4/17)

| Instruction Group    | Mnemonic | Operands                 | Bytes | Clocks |        | Clocks                           | Flag |    |    |
|----------------------|----------|--------------------------|-------|--------|--------|----------------------------------|------|----|----|
|                      |          |                          |       | Note 1 | Note 2 |                                  | Z    | AC | CY |
| 8-bit data transfer  | XCH      | A, [HL+B]                | 2     | 2      | –      | $A \leftrightarrow (HL+B)$       |      |    |    |
|                      |          | A, ES:[HL+B]             | 3     | 3      | –      | $A \leftrightarrow ((ES, HL)+B)$ |      |    |    |
|                      |          | A, [HL+C]                | 2     | 2      | –      | $A \leftrightarrow (HL+C)$       |      |    |    |
|                      |          | A, ES:[HL+C]             | 3     | 3      | –      | $A \leftrightarrow ((ES, HL)+C)$ |      |    |    |
|                      | ONEB     | A                        | 1     | 1      | –      | $A \leftarrow 01H$               |      |    |    |
|                      |          | X                        | 1     | 1      | –      | $X \leftarrow 01H$               |      |    |    |
|                      |          | B                        | 1     | 1      | –      | $B \leftarrow 01H$               |      |    |    |
|                      |          | C                        | 1     | 1      | –      | $C \leftarrow 01H$               |      |    |    |
|                      |          | !addr16                  | 3     | 1      | –      | $(addr16) \leftarrow 01H$        |      |    |    |
|                      |          | ES:!addr16               | 4     | 2      | –      | $(ES, addr16) \leftarrow 01H$    |      |    |    |
|                      |          | saddr                    | 2     | 1      | –      | $(saddr) \leftarrow 01H$         |      |    |    |
|                      | CLRB     | A                        | 1     | 1      | –      | $A \leftarrow 00H$               |      |    |    |
|                      |          | X                        | 1     | 1      | –      | $X \leftarrow 00H$               |      |    |    |
|                      |          | B                        | 1     | 1      | –      | $B \leftarrow 00H$               |      |    |    |
|                      |          | C                        | 1     | 1      | –      | $C \leftarrow 00H$               |      |    |    |
|                      |          | !addr16                  | 3     | 1      | –      | $(addr16) \leftarrow 00H$        |      |    |    |
|                      |          | ES:!addr16               | 4     | 2      | –      | $(ES, addr16) \leftarrow 00H$    |      |    |    |
|                      |          | saddr                    | 2     | 1      | –      | $(saddr) \leftarrow 00H$         |      |    |    |
|                      | MOVS     | [HL+byte], X             | 3     | 1      | –      | $(HL+byte) \leftarrow X$         | ×    |    | ×  |
|                      |          | ES:[HL+byte], X          | 4     | 2      | –      | $(ES, HL+byte) \leftarrow X$     | ×    |    | ×  |
| 16-bit data transfer | MOVW     | rp, #word                | 3     | 1      | –      | $rp \leftarrow word$             |      |    |    |
|                      |          | saddrp, #word            | 4     | 1      | –      | $(saddrp) \leftarrow word$       |      |    |    |
|                      |          | sfrp, #word              | 4     | 1      | –      | $sfrp \leftarrow word$           |      |    |    |
|                      |          | AX, rp <sup>Note 3</sup> | 1     | 1      | –      | $AX \leftarrow rp$               |      |    |    |
|                      |          | rp, AX <sup>Note 3</sup> | 1     | 1      | –      | $rp \leftarrow AX$               |      |    |    |
|                      |          | AX, !addr16              | 3     | 1      | 4      | $AX \leftarrow (addr16)$         |      |    |    |
|                      |          | !addr16, AX              | 3     | 1      | –      | $(addr16) \leftarrow AX$         |      |    |    |
|                      |          | AX, ES:!addr16           | 4     | 2      | 5      | $AX \leftarrow (ES, addr16)$     |      |    |    |
|                      |          | ES:!addr16, AX           | 4     | 2      | –      | $(ES, addr16) \leftarrow AX$     |      |    |    |
|                      |          | AX, saddrp               | 2     | 1      | –      | $AX \leftarrow (saddrp)$         |      |    |    |
|                      |          | saddrp, AX               | 2     | 1      | –      | $(saddrp) \leftarrow AX$         |      |    |    |
|                      |          | AX, sfrp                 | 2     | 1      | –      | $AX \leftarrow sfrp$             |      |    |    |
|                      |          | sfrp, AX                 | 2     | 1      | –      | $sfrp \leftarrow AX$             |      |    |    |

- Notes**
1. Number of CPU clocks ( $f_{CLK}$ ) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
  2. Number of CPU clocks ( $f_{CLK}$ ) when the program memory area is accessed.
  3. Except  $rp = AX$

**Remark** Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 29-5. Operation List (5/17)

| Instruction Group    | Mnemonic | Operands         | Bytes | Clocks |        | Clocks                            | Flag |    |    |
|----------------------|----------|------------------|-------|--------|--------|-----------------------------------|------|----|----|
|                      |          |                  |       | Note 1 | Note 2 |                                   | Z    | AC | CY |
| 16-bit data transfer | MOVW     | AX, [DE]         | 1     | 1      | 4      | $AX \leftarrow (DE)$              |      |    |    |
|                      |          | [DE], AX         | 1     | 1      | –      | $(DE) \leftarrow AX$              |      |    |    |
|                      |          | AX, ES:[DE]      | 2     | 2      | 5      | $AX \leftarrow (ES, DE)$          |      |    |    |
|                      |          | ES:[DE], AX      | 2     | 2      | –      | $(ES, DE) \leftarrow AX$          |      |    |    |
|                      |          | AX, [HL]         | 1     | 1      | 4      | $AX \leftarrow (HL)$              |      |    |    |
|                      |          | [HL], AX         | 1     | 1      | –      | $(HL) \leftarrow AX$              |      |    |    |
|                      |          | AX, ES:[HL]      | 2     | 2      | 5      | $AX \leftarrow (ES, HL)$          |      |    |    |
|                      |          | ES:[HL], AX      | 2     | 2      | –      | $(ES, HL) \leftarrow AX$          |      |    |    |
|                      |          | AX, [DE+byte]    | 2     | 1      | 4      | $AX \leftarrow (DE+byte)$         |      |    |    |
|                      |          | [DE+byte], AX    | 2     | 1      | –      | $(DE+byte) \leftarrow AX$         |      |    |    |
|                      |          | AX, ES:[DE+byte] | 3     | 2      | 5      | $AX \leftarrow ((ES, DE) + byte)$ |      |    |    |
|                      |          | ES:[DE+byte], AX | 3     | 2      | –      | $((ES, DE) + byte) \leftarrow AX$ |      |    |    |
|                      |          | AX, [HL+byte]    | 2     | 1      | 4      | $AX \leftarrow (HL + byte)$       |      |    |    |
|                      |          | [HL+byte], AX    | 2     | 1      | –      | $(HL + byte) \leftarrow AX$       |      |    |    |
|                      |          | AX, ES:[HL+byte] | 3     | 2      | 5      | $AX \leftarrow ((ES, HL) + byte)$ |      |    |    |
|                      |          | ES:[HL+byte], AX | 3     | 2      | –      | $((ES, HL) + byte) \leftarrow AX$ |      |    |    |
|                      |          | AX, [SP+byte]    | 2     | 1      | –      | $AX \leftarrow (SP + byte)$       |      |    |    |
|                      |          | [SP+byte], AX    | 2     | 1      | –      | $(SP + byte) \leftarrow AX$       |      |    |    |
|                      |          | AX, word[B]      | 3     | 1      | 4      | $AX \leftarrow (B + word)$        |      |    |    |
|                      |          | word[B], AX      | 3     | 1      | –      | $(B + word) \leftarrow AX$        |      |    |    |
|                      |          | AX, ES:word[B]   | 4     | 2      | 5      | $AX \leftarrow ((ES, B) + word)$  |      |    |    |
|                      |          | ES:word[B], AX   | 4     | 2      | –      | $((ES, B) + word) \leftarrow AX$  |      |    |    |
|                      |          | AX, word[C]      | 3     | 1      | 4      | $AX \leftarrow (C + word)$        |      |    |    |
|                      |          | word[C], AX      | 3     | 1      | –      | $(C + word) \leftarrow AX$        |      |    |    |
|                      |          | AX, ES:word[C]   | 4     | 2      | 5      | $AX \leftarrow ((ES, C) + word)$  |      |    |    |
|                      |          | ES:word[C], AX   | 4     | 2      | –      | $((ES, C) + word) \leftarrow AX$  |      |    |    |
|                      |          | AX, word[BC]     | 3     | 1      | 4      | $AX \leftarrow (BC + word)$       |      |    |    |
|                      |          | word[BC], AX     | 3     | 1      | –      | $(BC + word) \leftarrow AX$       |      |    |    |
|                      |          | AX, ES:word[BC]  | 4     | 2      | 5      | $AX \leftarrow ((ES, BC) + word)$ |      |    |    |
|                      |          | ES:word[BC], AX  | 4     | 2      | –      | $((ES, BC) + word) \leftarrow AX$ |      |    |    |

**Notes 1.** Number of CPU clocks ( $f_{CLK}$ ) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

**2.** Number of CPU clocks ( $f_{CLK}$ ) when the program memory area is accessed.

**Remark** Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 29-5. Operation List (6/17)

| Instruction Group    | Mnemonic | Operands                 | Bytes | Clocks |        | Clocks                                                       | Flag |    |    |
|----------------------|----------|--------------------------|-------|--------|--------|--------------------------------------------------------------|------|----|----|
|                      |          |                          |       | Note 1 | Note 2 |                                                              | Z    | AC | CY |
| 16-bit data transfer | MOVW     | BC, laddr16              | 3     | 1      | 4      | $BC \leftarrow (\text{addr16})$                              |      |    |    |
|                      |          | BC, ES:laddr16           | 4     | 2      | 5      | $BC \leftarrow (ES, \text{addr16})$                          |      |    |    |
|                      |          | DE, laddr16              | 3     | 1      | 4      | $DE \leftarrow (\text{addr16})$                              |      |    |    |
|                      |          | DE, ES:laddr16           | 4     | 2      | 5      | $DE \leftarrow (ES, \text{addr16})$                          |      |    |    |
|                      |          | HL, laddr16              | 3     | 1      | 4      | $HL \leftarrow (\text{addr16})$                              |      |    |    |
|                      |          | HL, ES:laddr16           | 4     | 2      | 5      | $HL \leftarrow (ES, \text{addr16})$                          |      |    |    |
|                      |          | BC, saddrp               | 2     | 1      | –      | $BC \leftarrow (\text{saddrp})$                              |      |    |    |
|                      |          | DE, saddrp               | 2     | 1      | –      | $DE \leftarrow (\text{saddrp})$                              |      |    |    |
|                      |          | HL, saddrp               | 2     | 1      | –      | $HL \leftarrow (\text{saddrp})$                              |      |    |    |
|                      | XCHW     | AX, rp <sup>Note 3</sup> | 1     | 1      | –      | $AX \leftrightarrow rp$                                      |      |    |    |
|                      | ONEW     | AX                       | 1     | 1      | –      | $AX \leftarrow 0001H$                                        |      |    |    |
|                      |          | BC                       | 1     | 1      | –      | $BC \leftarrow 0001H$                                        |      |    |    |
|                      | CLRW     | AX                       | 1     | 1      | –      | $AX \leftarrow 0000H$                                        |      |    |    |
|                      |          | BC                       | 1     | 1      | –      | $BC \leftarrow 0000H$                                        |      |    |    |
| 8-bit operation      | ADD      | A, #byte                 | 2     | 1      | –      | $A, CY \leftarrow A + \text{byte}$                           | x    | x  | x  |
|                      |          | saddr, #byte             | 3     | 2      | –      | $(\text{saddr}), CY \leftarrow (\text{saddr}) + \text{byte}$ | x    | x  | x  |
|                      |          | A, r <sup>Note 4</sup>   | 2     | 1      | –      | $A, CY \leftarrow A + r$                                     | x    | x  | x  |
|                      |          | r, A                     | 2     | 1      | –      | $r, CY \leftarrow r + A$                                     | x    | x  | x  |
|                      |          | A, laddr16               | 3     | 1      | 4      | $A, CY \leftarrow A + (\text{addr16})$                       | x    | x  | x  |
|                      |          | A, ES:laddr16            | 4     | 2      | 5      | $A, CY \leftarrow A + (ES, \text{addr16})$                   | x    | x  | x  |
|                      |          | A, saddr                 | 2     | 1      | –      | $A, CY \leftarrow A + (\text{saddr})$                        | x    | x  | x  |
|                      |          | A, [HL]                  | 1     | 1      | 4      | $A, CY \leftarrow A + (HL)$                                  | x    | x  | x  |
|                      |          | A, ES:[HL]               | 2     | 2      | 5      | $A, CY \leftarrow A + (ES, HL)$                              | x    | x  | x  |
|                      |          | A, [HL+byte]             | 2     | 1      | 4      | $A, CY \leftarrow A + (HL + \text{byte})$                    | x    | x  | x  |
|                      |          | A, ES:[HL+byte]          | 3     | 2      | 5      | $A, CY \leftarrow A + ((ES, HL) + \text{byte})$              | x    | x  | x  |
|                      |          | A, [HL+B]                | 2     | 1      | 4      | $A, CY \leftarrow A + (HL + B)$                              | x    | x  | x  |
|                      |          | A, ES:[HL+B]             | 3     | 2      | 5      | $A, CY \leftarrow A + ((ES, HL) + B)$                        | x    | x  | x  |
|                      |          | A, [HL+C]                | 2     | 1      | 4      | $A, CY \leftarrow A + (HL + C)$                              | x    | x  | x  |
|                      |          | A, ES:[HL+C]             | 3     | 2      | 5      | $A, CY \leftarrow A + ((ES, HL) + C)$                        | x    | x  | x  |

- Notes**
1. Number of CPU clocks ( $f_{CLK}$ ) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
  2. Number of CPU clocks ( $f_{CLK}$ ) when the program memory area is accessed.
  3. Except  $rp = AX$
  4. Except  $r = A$

**Remark** Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 29-5. Operation List (7/17)

| Instruction Group | Mnemonic | Operands               | Bytes | Clocks |        | Clocks                                                             | Flag |    |    |
|-------------------|----------|------------------------|-------|--------|--------|--------------------------------------------------------------------|------|----|----|
|                   |          |                        |       | Note 1 | Note 2 |                                                                    | Z    | AC | CY |
| 8-bit operation   | ADDC     | A, #byte               | 2     | 1      | –      | $A, CY \leftarrow A + \text{byte} + CY$                            | x    | x  | x  |
|                   |          | saddr, #byte           | 3     | 2      | –      | $(\text{saddr}), CY \leftarrow (\text{saddr}) + \text{byte} + CY$  | x    | x  | x  |
|                   |          | A, r <sup>Note 3</sup> | 2     | 1      | –      | $A, CY \leftarrow A + r + CY$                                      | x    | x  | x  |
|                   |          | r, A                   | 2     | 1      | –      | $r, CY \leftarrow r + A + CY$                                      | x    | x  | x  |
|                   |          | A, laddr16             | 3     | 1      | 4      | $A, CY \leftarrow A + (\text{addr16}) + CY$                        | x    | x  | x  |
|                   |          | A, ES:laddr16          | 4     | 2      | 5      | $A, CY \leftarrow A + (\text{ES}, \text{addr16}) + CY$             | x    | x  | x  |
|                   |          | A, saddr               | 2     | 1      | –      | $A, CY \leftarrow A + (\text{saddr}) + CY$                         | x    | x  | x  |
|                   |          | A, [HL]                | 1     | 1      | 4      | $A, CY \leftarrow A + (\text{HL}) + CY$                            | x    | x  | x  |
|                   |          | A, ES:[HL]             | 2     | 2      | 5      | $A, CY \leftarrow A + (\text{ES}, \text{HL}) + CY$                 | x    | x  | x  |
|                   |          | A, [HL+byte]           | 2     | 1      | 4      | $A, CY \leftarrow A + (\text{HL} + \text{byte}) + CY$              | x    | x  | x  |
|                   |          | A, ES:[HL+byte]        | 3     | 2      | 5      | $A, CY \leftarrow A + ((\text{ES}, \text{HL}) + \text{byte}) + CY$ | x    | x  | x  |
|                   |          | A, [HL+B]              | 2     | 1      | 4      | $A, CY \leftarrow A + (\text{HL} + B) + CY$                        | x    | x  | x  |
|                   |          | A, ES:[HL+B]           | 3     | 2      | 5      | $A, CY \leftarrow A + ((\text{ES}, \text{HL}) + B) + CY$           | x    | x  | x  |
|                   |          | A, [HL+C]              | 2     | 1      | 4      | $A, CY \leftarrow A + (\text{HL} + C) + CY$                        | x    | x  | x  |
|                   |          | A, ES:[HL+C]           | 3     | 2      | 5      | $A, CY \leftarrow A + ((\text{ES}, \text{HL}) + C) + CY$           | x    | x  | x  |
|                   | SUB      | A, #byte               | 2     | 1      | –      | $A, CY \leftarrow A - \text{byte}$                                 | x    | x  | x  |
|                   |          | saddr, #byte           | 3     | 2      | –      | $(\text{saddr}), CY \leftarrow (\text{saddr}) - \text{byte}$       | x    | x  | x  |
|                   |          | A, r <sup>Note 3</sup> | 2     | 1      | –      | $A, CY \leftarrow A - r$                                           | x    | x  | x  |
|                   |          | r, A                   | 2     | 1      | –      | $r, CY \leftarrow r - A$                                           | x    | x  | x  |
|                   |          | A, laddr16             | 3     | 1      | 4      | $A, CY \leftarrow A - (\text{addr16})$                             | x    | x  | x  |
|                   |          | A, ES:laddr16          | 4     | 2      | 5      | $A, CY \leftarrow A - (\text{ES}, \text{addr16})$                  | x    | x  | x  |
|                   |          | A, saddr               | 2     | 1      | –      | $A, CY \leftarrow A - (\text{saddr})$                              | x    | x  | x  |
|                   |          | A, [HL]                | 1     | 1      | 4      | $A, CY \leftarrow A - (\text{HL})$                                 | x    | x  | x  |
|                   |          | A, ES:[HL]             | 2     | 2      | 5      | $A, CY \leftarrow A - (\text{ES}, \text{HL})$                      | x    | x  | x  |
|                   |          | A, [HL+byte]           | 2     | 1      | 4      | $A, CY \leftarrow A - (\text{HL} + \text{byte})$                   | x    | x  | x  |
|                   |          | A, ES:[HL+byte]        | 3     | 2      | 5      | $A, CY \leftarrow A - ((\text{ES}, \text{HL}) + \text{byte})$      | x    | x  | x  |
|                   |          | A, [HL+B]              | 2     | 1      | 4      | $A, CY \leftarrow A - (\text{HL} + B)$                             | x    | x  | x  |
|                   |          | A, ES:[HL+B]           | 3     | 2      | 5      | $A, CY \leftarrow A - ((\text{ES}, \text{HL}) + B)$                | x    | x  | x  |
|                   |          | A, [HL+C]              | 2     | 1      | 4      | $A, CY \leftarrow A - (\text{HL} + C)$                             | x    | x  | x  |
|                   |          | A, ES:[HL+C]           | 3     | 2      | 5      | $A, CY \leftarrow A - ((\text{ES}, \text{HL}) + C)$                | x    | x  | x  |

**Notes 1.** Number of CPU clocks ( $f_{CLK}$ ) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

**2.** Number of CPU clocks ( $f_{CLK}$ ) when the program memory area is accessed.

**3.** Except  $r = A$

**Remark** Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 29-5. Operation List (8/17)

| Instruction Group | Mnemonic | Operands                   | Bytes | Clocks |        | Clocks                                              | Flag |    |    |
|-------------------|----------|----------------------------|-------|--------|--------|-----------------------------------------------------|------|----|----|
|                   |          |                            |       | Note 1 | Note 2 |                                                     | Z    | AC | CY |
| 8-bit operation   | SUBC     | A, #byte                   | 2     | 1      | –      | $A, CY \leftarrow A - \text{byte} - CY$             | x    | x  | x  |
|                   |          | saddr, #byte               | 3     | 2      | –      | $(saddr), CY \leftarrow (saddr) - \text{byte} - CY$ | x    | x  | x  |
|                   |          | A, r <small>Note 3</small> | 2     | 1      | –      | $A, CY \leftarrow A - r - CY$                       | x    | x  | x  |
|                   |          | r, A                       | 2     | 1      | –      | $r, CY \leftarrow r - A - CY$                       | x    | x  | x  |
|                   |          | A, laddr16                 | 3     | 1      | 4      | $A, CY \leftarrow A - (\text{addr16}) - CY$         | x    | x  | x  |
|                   |          | A, ES:laddr16              | 4     | 2      | 5      | $A, CY \leftarrow A - (ES, \text{addr16}) - CY$     | x    | x  | x  |
|                   |          | A, saddr                   | 2     | 1      | –      | $A, CY \leftarrow A - (saddr) - CY$                 | x    | x  | x  |
|                   |          | A, [HL]                    | 1     | 1      | 4      | $A, CY \leftarrow A - (HL) - CY$                    | x    | x  | x  |
|                   |          | A, ES:[HL]                 | 2     | 2      | 5      | $A, CY \leftarrow A - (ES, HL) - CY$                | x    | x  | x  |
|                   |          | A, [HL+byte]               | 2     | 1      | 4      | $A, CY \leftarrow A - (HL+\text{byte}) - CY$        | x    | x  | x  |
|                   |          | A, ES:[HL+byte]            | 3     | 2      | 5      | $A, CY \leftarrow A - ((ES, HL)+\text{byte}) - CY$  | x    | x  | x  |
|                   |          | A, [HL+B]                  | 2     | 1      | 4      | $A, CY \leftarrow A - (HL+B) - CY$                  | x    | x  | x  |
|                   |          | A, ES:[HL+B]               | 3     | 2      | 5      | $A, CY \leftarrow A - ((ES, HL)+B) - CY$            | x    | x  | x  |
|                   |          | A, [HL+C]                  | 2     | 1      | 4      | $A, CY \leftarrow A - (HL+C) - CY$                  | x    | x  | x  |
|                   |          | A, ES:[HL+C]               | 3     | 2      | 5      | $A, CY \leftarrow A - ((ES:HL)+C) - CY$             | x    | x  | x  |
|                   | AND      | A, #byte                   | 2     | 1      | –      | $A \leftarrow A \wedge \text{byte}$                 | x    |    |    |
|                   |          | saddr, #byte               | 3     | 2      | –      | $(saddr) \leftarrow (saddr) \wedge \text{byte}$     | x    |    |    |
|                   |          | A, r <small>Note 3</small> | 2     | 1      | –      | $A \leftarrow A \wedge r$                           | x    |    |    |
|                   |          | r, A                       | 2     | 1      | –      | $R \leftarrow r \wedge A$                           | x    |    |    |
|                   |          | A, laddr16                 | 3     | 1      | 4      | $A \leftarrow A \wedge (\text{addr16})$             | x    |    |    |
|                   |          | A, ES:laddr16              | 4     | 2      | 5      | $A \leftarrow A \wedge (ES:\text{addr16})$          | x    |    |    |
|                   |          | A, saddr                   | 2     | 1      | –      | $A \leftarrow A \wedge (saddr)$                     | x    |    |    |
|                   |          | A, [HL]                    | 1     | 1      | 4      | $A \leftarrow A \wedge (HL)$                        | x    |    |    |
|                   |          | A, ES:[HL]                 | 2     | 2      | 5      | $A \leftarrow A \wedge (ES:HL)$                     | x    |    |    |
|                   |          | A, [HL+byte]               | 2     | 1      | 4      | $A \leftarrow A \wedge (HL+\text{byte})$            | x    |    |    |
|                   |          | A, ES:[HL+byte]            | 3     | 2      | 5      | $A \leftarrow A \wedge ((ES:HL)+\text{byte})$       | x    |    |    |
|                   |          | A, [HL+B]                  | 2     | 1      | 4      | $A \leftarrow A \wedge (HL+B)$                      | x    |    |    |
|                   |          | A, ES:[HL+B]               | 3     | 2      | 5      | $A \leftarrow A \wedge ((ES:HL)+B)$                 | x    |    |    |
|                   |          | A, [HL+C]                  | 2     | 1      | 4      | $A \leftarrow A \wedge (HL+C)$                      | x    |    |    |
|                   |          | A, ES:[HL+C]               | 3     | 2      | 5      | $A \leftarrow A \wedge ((ES:HL)+C)$                 | x    |    |    |

- Notes**
1. Number of CPU clocks ( $f_{CLK}$ ) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
  2. Number of CPU clocks ( $f_{CLK}$ ) when the program memory area is accessed.
  3. Except  $r = A$

**Remark** Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 29-5. Operation List (9/17)

| Instruction Group | Mnemonic | Operands                   | Bytes | Clocks |        | Clocks                                                        | Flag |    |    |
|-------------------|----------|----------------------------|-------|--------|--------|---------------------------------------------------------------|------|----|----|
|                   |          |                            |       | Note 1 | Note 2 |                                                               | Z    | AC | CY |
| 8-bit operation   | OR       | A, #byte                   | 2     | 1      | –      | $A \leftarrow A \vee \text{byte}$                             | x    |    |    |
|                   |          | saddr, #byte               | 3     | 2      | –      | $(\text{saddr}) \leftarrow (\text{saddr}) \vee \text{byte}$   | x    |    |    |
|                   |          | A, r <small>Note 3</small> | 2     | 1      | –      | $A \leftarrow A \vee r$                                       | x    |    |    |
|                   |          | r, A                       | 2     | 1      | –      | $r \leftarrow r \vee A$                                       | x    |    |    |
|                   |          | A, laddr16                 | 3     | 1      | 4      | $A \leftarrow A \vee (\text{addr16})$                         | x    |    |    |
|                   |          | A, ES:laddr16              | 4     | 2      | 5      | $A \leftarrow A \vee (\text{ES:addr16})$                      | x    |    |    |
|                   |          | A, saddr                   | 2     | 1      | –      | $A \leftarrow A \vee (\text{saddr})$                          | x    |    |    |
|                   |          | A, [HL]                    | 1     | 1      | 4      | $A \leftarrow A \vee (\text{H})$                              | x    |    |    |
|                   |          | A, ES:[HL]                 | 2     | 2      | 5      | $A \leftarrow A \vee (\text{ES:HL})$                          | x    |    |    |
|                   |          | A, [HL+byte]               | 2     | 1      | 4      | $A \leftarrow A \vee (\text{HL} + \text{byte})$               | x    |    |    |
|                   |          | A, ES:[HL+byte]            | 3     | 2      | 5      | $A \leftarrow A \vee ((\text{ES:HL}) + \text{byte})$          | x    |    |    |
|                   |          | A, [HL+B]                  | 2     | 1      | 4      | $A \leftarrow A \vee (\text{HL} + \text{B})$                  | x    |    |    |
|                   |          | A, ES:[HL+B]               | 3     | 2      | 5      | $A \leftarrow A \vee ((\text{ES:HL}) + \text{B})$             | x    |    |    |
|                   |          | A, [HL+C]                  | 2     | 1      | 4      | $A \leftarrow A \vee (\text{HL} + \text{C})$                  | x    |    |    |
|                   |          | A, ES:[HL+C]               | 3     | 2      | 5      | $A \leftarrow A \vee ((\text{ES:HL}) + \text{C})$             | x    |    |    |
|                   | XOR      | A, #byte                   | 2     | 1      | –      | $A \leftarrow A \oplus \text{byte}$                           | x    |    |    |
|                   |          | saddr, #byte               | 3     | 2      | –      | $(\text{saddr}) \leftarrow (\text{saddr}) \oplus \text{byte}$ | x    |    |    |
|                   |          | A, r <small>Note 3</small> | 2     | 1      | –      | $A \leftarrow A \oplus r$                                     | x    |    |    |
|                   |          | r, A                       | 2     | 1      | –      | $r \leftarrow r \oplus A$                                     | x    |    |    |
|                   |          | A, laddr16                 | 3     | 1      | 4      | $A \leftarrow A \oplus (\text{addr16})$                       | x    |    |    |
|                   |          | A, ES:laddr16              | 4     | 2      | 5      | $A \leftarrow A \oplus (\text{ES:addr16})$                    | x    |    |    |
|                   |          | A, saddr                   | 2     | 1      | –      | $A \leftarrow A \oplus (\text{saddr})$                        | x    |    |    |
|                   |          | A, [HL]                    | 1     | 1      | 4      | $A \leftarrow A \oplus (\text{HL})$                           | x    |    |    |
|                   |          | A, ES:[HL]                 | 2     | 2      | 5      | $A \leftarrow A \oplus (\text{ES:HL})$                        | x    |    |    |
|                   |          | A, [HL+byte]               | 2     | 1      | 4      | $A \leftarrow A \oplus (\text{HL} + \text{byte})$             | x    |    |    |
|                   |          | A, ES:[HL+byte]            | 3     | 2      | 5      | $A \leftarrow A \oplus ((\text{ES:HL}) + \text{byte})$        | x    |    |    |
|                   |          | A, [HL+B]                  | 2     | 1      | 4      | $A \leftarrow A \oplus (\text{HL} + \text{B})$                | x    |    |    |
|                   |          | A, ES:[HL+B]               | 3     | 2      | 5      | $A \leftarrow A \oplus ((\text{ES:HL}) + \text{B})$           | x    |    |    |
|                   |          | A, [HL+C]                  | 2     | 1      | 4      | $A \leftarrow A \oplus (\text{HL} + \text{C})$                | x    |    |    |
|                   |          | A, ES:[HL+C]               | 3     | 2      | 5      | $A \leftarrow A \oplus ((\text{ES:HL}) + \text{C})$           | x    |    |    |

**Notes 1.** Number of CPU clocks ( $f_{\text{CLK}}$ ) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

**2.** Number of CPU clocks ( $f_{\text{CLK}}$ ) when the program memory area is accessed.

**3.** Except  $r = A$

**Remark** Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 29-5. Operation List (10/17)

| Instruction Group   | Mnemonic | Operands              | Bytes | Clocks |        | Clocks             | Flag |    |    |
|---------------------|----------|-----------------------|-------|--------|--------|--------------------|------|----|----|
|                     |          |                       |       | Note 1 | Note 2 |                    | Z    | AC | CY |
| <R> 8-bit operation | CMP      | A, #byte              | 2     | 1      | –      | A – byte           | x    | x  | x  |
|                     |          | !addr16, #byte        | 4     | 1      | 4      | (addr16) – byte    | x    | x  | x  |
|                     |          | ES:!addr16, #byte     | 5     | 2      | 5      | (ES:addr16) – byte | x    | x  | x  |
|                     |          | saddr, #byte          | 3     | 1      | –      | (saddr) – byte     | x    | x  | x  |
|                     |          | A, r <sup>Note3</sup> | 2     | 1      | –      | A – r              | x    | x  | x  |
|                     |          | r, A                  | 2     | 1      | –      | r – A              | x    | x  | x  |
|                     |          | A, !addr16            | 3     | 1      | 4      | A – (addr16)       | x    | x  | x  |
|                     |          | A, ES:!addr16         | 4     | 2      | 5      | A – (ES:addr16)    | x    | x  | x  |
|                     |          | A, saddr              | 2     | 1      | –      | A – (saddr)        | x    | x  | x  |
|                     |          | A, [HL]               | 1     | 1      | 4      | A – (HL)           | x    | x  | x  |
|                     |          | A, ES:[HL]            | 2     | 2      | 5      | A – (ES:HL)        | x    | x  | x  |
|                     |          | A, [HL+byte]          | 2     | 1      | 4      | A – (HL+byte)      | x    | x  | x  |
|                     |          | A, ES:[HL+byte]       | 3     | 2      | 5      | A – ((ES:HL)+byte) | x    | x  | x  |
|                     |          | A, [HL+B]             | 2     | 1      | 4      | A – (HL+B)         | x    | x  | x  |
|                     |          | A, ES:[HL+B]          | 3     | 2      | 5      | A – ((ES:HL)+B)    | x    | x  | x  |
|                     |          | A, [HL+C]             | 2     | 1      | 4      | A – (HL+C)         | x    | x  | x  |
|                     |          | A, ES:[HL+C]          | 3     | 2      | 5      | A – ((ES:HL)+C)    | x    | x  | x  |
|                     | CMP0     | A                     | 1     | 1      | –      | A – 00H            | x    | 0  | 0  |
|                     |          | X                     | 1     | 1      | –      | X – 00H            | x    | 0  | 0  |
|                     |          | B                     | 1     | 1      | –      | B – 00H            | x    | 0  | 0  |
|                     |          | C                     | 1     | 1      | –      | C – 00H            | x    | 0  | 0  |
|                     |          | !addr16               | 3     | 1      | 4      | (addr16) – 00H     | x    | 0  | 0  |
|                     |          | ES:!addr16            | 4     | 2      | 5      | (ES:addr16) – 00H  | x    | 0  | 0  |
|                     |          | saddr                 | 2     | 1      | –      | (saddr) – 00H      | x    | 0  | 0  |
|                     | CMPS     | X, [HL+byte]          | 3     | 1      | 4      | X – (HL+byte)      | x    | x  | x  |
|                     |          | X, ES:[HL+byte]       | 4     | 2      | 5      | X – ((ES:HL)+byte) | x    | x  | x  |

- Notes**
1. Number of CPU clocks ( $f_{CLK}$ ) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
  2. Number of CPU clocks ( $f_{CLK}$ ) when the program memory area is accessed.
  3. Except  $r = A$

**Remark** Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 29-5. Operation List (11/17)

| Instruction Group | Mnemonic | Operands          | Bytes | Clocks |        | Clocks                       | Flag |    |    |
|-------------------|----------|-------------------|-------|--------|--------|------------------------------|------|----|----|
|                   |          |                   |       | Note 1 | Note 2 |                              | Z    | AC | CY |
| 16-bit operation  | ADDW     | AX, #word         | 3     | 1      | –      | AX, CY ← AX+word             | x    | x  | x  |
|                   |          | AX, AX            | 1     | 1      | –      | AX, CY ← AX+AX               | x    | x  | x  |
|                   |          | AX, BC            | 1     | 1      | –      | AX, CY ← AX+BC               | x    | x  | x  |
|                   |          | AX, DE            | 1     | 1      | –      | AX, CY ← AX+DE               | x    | x  | x  |
|                   |          | AX, HL            | 1     | 1      | –      | AX, CY ← AX+HL               | x    | x  | x  |
|                   |          | AX, !addr16       | 3     | 1      | 4      | AX, CY ← AX+(addr16)         | x    | x  | x  |
|                   |          | AX, ES:!addr16    | 4     | 2      | 5      | AX, CY ← AX+(ES:addr16)      | x    | x  | x  |
|                   |          | AX, saddrp        | 2     | 1      | –      | AX, CY ← AX+(saddrp)         | x    | x  | x  |
|                   |          | AX, [HL+byte]     | 3     | 1      | 4      | AX, CY ← AX+(HL+byte)        | x    | x  | x  |
|                   |          | AX, ES: [HL+byte] | 4     | 2      | 5      | AX, CY ← AX+((ES:HL)+byte)   | x    | x  | x  |
|                   | SUBW     | AX, #word         | 3     | 1      | –      | AX, CY ← AX – word           | x    | x  | x  |
|                   |          | AX, BC            | 1     | 1      | –      | AX, CY ← AX – BC             | x    | x  | x  |
|                   |          | AX, DE            | 1     | 1      | –      | AX, CY ← AX – DE             | x    | x  | x  |
|                   |          | AX, HL            | 1     | 1      | –      | AX, CY ← AX – HL             | x    | x  | x  |
|                   |          | AX, !addr16       | 3     | 1      | 4      | AX, CY ← AX – (addr16)       | x    | x  | x  |
|                   |          | AX, ES:!addr16    | 4     | 2      | 5      | AX, CY ← AX – (ES:addr16)    | x    | x  | x  |
|                   |          | AX, saddrp        | 2     | 1      | –      | AX, CY ← AX – (saddrp)       | x    | x  | x  |
|                   |          | AX, [HL+byte]     | 3     | 1      | 4      | AX, CY ← AX – (HL+byte)      | x    | x  | x  |
|                   |          | AX, ES: [HL+byte] | 4     | 2      | 5      | AX, CY ← AX – ((ES:HL)+byte) | x    | x  | x  |
|                   | CMPW     | AX, #word         | 3     | 1      | –      | AX – word                    | x    | x  | x  |
|                   |          | AX, BC            | 1     | 1      | –      | AX – BC                      | x    | x  | x  |
|                   |          | AX, DE            | 1     | 1      | –      | AX – DE                      | x    | x  | x  |
|                   |          | AX, HL            | 1     | 1      | –      | AX – HL                      | x    | x  | x  |
|                   |          | AX, !addr16       | 3     | 1      | 4      | AX – (addr16)                | x    | x  | x  |
|                   |          | AX, ES:!addr16    | 4     | 2      | 5      | AX – (ES:addr16)             | x    | x  | x  |
|                   |          | AX, saddrp        | 2     | 1      | –      | AX – (saddrp)                | x    | x  | x  |
|                   |          | AX, [HL+byte]     | 3     | 1      | 4      | AX – (HL+byte)               | x    | x  | x  |
|                   |          | AX, ES: [HL+byte] | 4     | 2      | 5      | AX – ((ES:HL)+byte)          | x    | x  | x  |
| Multiply          | MULU     | X                 | 1     | 1      | –      | AX ← A×X                     |      |    |    |

**Notes 1.** Number of CPU clocks ( $f_{CLK}$ ) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

**2.** Number of CPU clocks ( $f_{CLK}$ ) when the program memory area is accessed.

**Remark** Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.



Table 29-5. Operation List (12/17)

| Instruction Group   | Mnemonic | Operands      | Bytes | Clocks |        | Clocks                                                                                  | Flag |    |    |
|---------------------|----------|---------------|-------|--------|--------|-----------------------------------------------------------------------------------------|------|----|----|
|                     |          |               |       | Note 1 | Note 2 |                                                                                         | Z    | AC | CY |
| Increment/decrement | INC      | r             | 1     | 1      | –      | $r \leftarrow r+1$                                                                      | x    | x  |    |
|                     |          | !addr16       | 3     | 2      | –      | $(addr16) \leftarrow (addr16)+1$                                                        | x    | x  |    |
|                     |          | ES:!addr16    | 4     | 3      | –      | $(ES, addr16) \leftarrow (ES, addr16)+1$                                                | x    | x  |    |
|                     |          | saddr         | 2     | 2      | –      | $(saddr) \leftarrow (saddr)+1$                                                          | x    | x  |    |
|                     |          | [HL+byte]     | 3     | 2      | –      | $(HL+byte) \leftarrow (HL+byte)+1$                                                      | x    | x  |    |
|                     |          | ES: [HL+byte] | 4     | 3      | –      | $((ES:HL)+byte) \leftarrow ((ES:HL)+byte)+1$                                            | x    | x  |    |
|                     | DEC      | r             | 1     | 1      | –      | $r \leftarrow r-1$                                                                      | x    | x  |    |
|                     |          | !addr16       | 3     | 2      | –      | $(addr16) \leftarrow (addr16)-1$                                                        | x    | x  |    |
|                     |          | ES:!addr16    | 4     | 3      | –      | $(ES, addr16) \leftarrow (ES, addr16)-1$                                                | x    | x  |    |
|                     |          | saddr         | 2     | 2      | –      | $(saddr) \leftarrow (saddr)-1$                                                          | x    | x  |    |
|                     |          | [HL+byte]     | 3     | 2      | –      | $(HL+byte) \leftarrow (HL+byte)-1$                                                      | x    | x  |    |
|                     |          | ES: [HL+byte] | 4     | 3      | –      | $((ES:HL)+byte) \leftarrow ((ES:HL)+byte)-1$                                            | x    | x  |    |
|                     | INCW     | rp            | 1     | 1      | –      | $rp \leftarrow rp+1$                                                                    |      |    |    |
|                     |          | !addr16       | 3     | 2      | –      | $(addr16) \leftarrow (addr16)+1$                                                        |      |    |    |
|                     |          | ES:!addr16    | 4     | 3      | –      | $(ES, addr16) \leftarrow (ES, addr16)+1$                                                |      |    |    |
|                     |          | saddrp        | 2     | 2      | –      | $(saddrp) \leftarrow (saddrp)+1$                                                        |      |    |    |
|                     |          | [HL+byte]     | 3     | 2      | –      | $(HL+byte) \leftarrow (HL+byte)+1$                                                      |      |    |    |
|                     |          | ES: [HL+byte] | 4     | 3      | –      | $((ES:HL)+byte) \leftarrow ((ES:HL)+byte)+1$                                            |      |    |    |
|                     | DECW     | rp            | 1     | 1      | –      | $rp \leftarrow rp-1$                                                                    |      |    |    |
|                     |          | !addr16       | 3     | 2      | –      | $(addr16) \leftarrow (addr16)-1$                                                        |      |    |    |
|                     |          | ES:!addr16    | 4     | 3      | –      | $(ES, addr16) \leftarrow (ES, addr16)-1$                                                |      |    |    |
|                     |          | saddrp        | 2     | 2      | –      | $(saddrp) \leftarrow (saddrp)-1$                                                        |      |    |    |
|                     |          | [HL+byte]     | 3     | 2      | –      | $(HL+byte) \leftarrow (HL+byte)-1$                                                      |      |    |    |
|                     |          | ES: [HL+byte] | 4     | 3      | –      | $((ES:HL)+byte) \leftarrow ((ES:HL)+byte)-1$                                            |      |    |    |
| Shift               | SHR      | A, cnt        | 2     | 1      | –      | $(CY \leftarrow A_0, A_{m-1} \leftarrow A_m, A_7 \leftarrow 0) \times cnt$              |      |    | x  |
|                     | SHRW     | AX, cnt       | 2     | 1      | –      | $(CY \leftarrow AX_0, AX_{m-1} \leftarrow AX_m, AX_{15} \leftarrow 0) \times cnt$       |      |    | x  |
|                     | SHL      | A, cnt        | 2     | 1      | –      | $(CY \leftarrow A_7, A_m \leftarrow A_{m-1}, A_0 \leftarrow 0) \times cnt$              |      |    | x  |
|                     |          | B, cnt        | 2     | 1      | –      | $(CY \leftarrow B_7, B_m \leftarrow B_{m-1}, B_0 \leftarrow 0) \times cnt$              |      |    | x  |
|                     |          | C, cnt        | 2     | 1      | –      | $(CY \leftarrow C_7, C_m \leftarrow C_{m-1}, C_0 \leftarrow 0) \times cnt$              |      |    | x  |
|                     | SHLW     | AX, cnt       | 2     | 1      | –      | $(CY \leftarrow AX_{15}, AX_m \leftarrow AX_{m-1}, AX_0 \leftarrow 0) \times cnt$       |      |    | x  |
|                     |          | BC, cnt       | 2     | 1      | –      | $(CY \leftarrow BC_{15}, BC_m \leftarrow BC_{m-1}, BC_0 \leftarrow 0) \times cnt$       |      |    | x  |
|                     | SAR      | A, cnt        | 2     | 1      | –      | $(CY \leftarrow A_0, A_{m-1} \leftarrow A_m, A_7 \leftarrow A_7) \times cnt$            |      |    | x  |
|                     | SARW     | AX, cnt       | 2     | 1      | –      | $(CY \leftarrow AX_0, AX_{m-1} \leftarrow AX_m, AX_{15} \leftarrow AX_{15}) \times cnt$ |      |    | x  |

**Notes 1.** Number of CPU clocks ( $f_{CLK}$ ) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

**2.** Number of CPU clocks ( $f_{CLK}$ ) when the program memory area is accessed.

**Remarks 1.** Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

**2.** cnt indicates the bit shift count.

Table 29-5. Operation List (13/17)

| Instruction Group | Mnemonic | Operands        | Bytes | Clocks |        | Clocks                                                                           | Flag |    |    |
|-------------------|----------|-----------------|-------|--------|--------|----------------------------------------------------------------------------------|------|----|----|
|                   |          |                 |       | Note 1 | Note 2 |                                                                                  | Z    | AC | CY |
| Rotate            | ROR      | A, 1            | 2     | 1      | –      | $(CY, A_7 \leftarrow A_0, A_{m-1} \leftarrow A_m) \times 1$                      |      |    | ×  |
|                   | ROL      | A, 1            | 2     | 1      | –      | $(CY, A_0 \leftarrow A_7, A_{m+1} \leftarrow A_m) \times 1$                      |      |    | ×  |
|                   | RORC     | A, 1            | 2     | 1      | –      | $(CY \leftarrow A_0, A_7 \leftarrow CY, A_{m-1} \leftarrow A_m) \times 1$        |      |    | ×  |
|                   | ROLC     | A, 1            | 2     | 1      | –      | $(CY \leftarrow A_7, A_0 \leftarrow CY, A_{m+1} \leftarrow A_m) \times 1$        |      |    | ×  |
|                   | ROLWC    | AX, 1           | 2     | 1      | –      | $(CY \leftarrow AX_{15}, AX_0 \leftarrow CY, AX_{m+1} \leftarrow AX_m) \times 1$ |      |    | ×  |
|                   |          | BC, 1           | 2     | 1      | –      | $(CY \leftarrow BC_{15}, BC_0 \leftarrow CY, BC_{m+1} \leftarrow BC_m) \times 1$ |      |    | ×  |
| Bit manipulate    | MOV1     | CY, A.bit       | 2     | 1      | –      | $CY \leftarrow A.bit$                                                            |      |    | ×  |
|                   |          | A.bit, CY       | 2     | 1      | –      | $A.bit \leftarrow CY$                                                            |      |    |    |
|                   |          | CY, PSW.bit     | 3     | 1      | –      | $CY \leftarrow PSW.bit$                                                          |      |    | ×  |
|                   |          | PSW.bit, CY     | 3     | 4      | –      | $PSW.bit \leftarrow CY$                                                          | ×    | ×  |    |
|                   |          | CY, saddr.bit   | 3     | 1      | –      | $CY \leftarrow (saddr).bit$                                                      |      |    | ×  |
|                   |          | saddr.bit, CY   | 3     | 2      | –      | $(saddr).bit \leftarrow CY$                                                      |      |    |    |
|                   |          | CY, sfr.bit     | 3     | 1      | –      | $CY \leftarrow sfr.bit$                                                          |      |    | ×  |
|                   |          | sfr.bit, CY     | 3     | 2      | –      | $sfr.bit \leftarrow CY$                                                          |      |    |    |
|                   |          | CY, [HL].bit    | 2     | 1      | 4      | $CY \leftarrow (HL).bit$                                                         |      |    | ×  |
|                   |          | [HL].bit, CY    | 2     | 2      | –      | $(HL).bit \leftarrow CY$                                                         |      |    |    |
|                   |          | CY, ES:[HL].bit | 3     | 2      | 5      | $CY \leftarrow (ES, HL).bit$                                                     |      |    | ×  |
|                   |          | ES:[HL].bit, CY | 3     | 3      | –      | $(ES, HL).bit \leftarrow CY$                                                     |      |    |    |
|                   | AND1     | CY, A.bit       | 2     | 1      | –      | $CY \leftarrow CY \wedge A.bit$                                                  |      |    | ×  |
|                   |          | CY, PSW.bit     | 3     | 1      | –      | $CY \leftarrow CY \wedge PSW.bit$                                                |      |    | ×  |
|                   |          | CY, saddr.bit   | 3     | 1      | –      | $CY \leftarrow CY \wedge (saddr).bit$                                            |      |    | ×  |
|                   |          | CY, sfr.bit     | 3     | 1      | –      | $CY \leftarrow CY \wedge sfr.bit$                                                |      |    | ×  |
|                   |          | CY, [HL].bit    | 2     | 1      | 4      | $CY \leftarrow CY \wedge (HL).bit$                                               |      |    | ×  |
|                   |          | CY, ES:[HL].bit | 3     | 2      | 5      | $CY \leftarrow CY \wedge (ES, HL).bit$                                           |      |    | ×  |
|                   | OR1      | CY, A.bit       | 2     | 1      | –      | $CY \leftarrow CY \vee A.bit$                                                    |      |    | ×  |
|                   |          | CY, PSW.bit     | 3     | 1      | –      | $CY \leftarrow CY \vee PSW.bit$                                                  |      |    | ×  |
|                   |          | CY, saddr.bit   | 3     | 1      | –      | $CY \leftarrow CY \vee (saddr).bit$                                              |      |    | ×  |
|                   |          | CY, sfr.bit     | 3     | 1      | –      | $CY \leftarrow CY \vee sfr.bit$                                                  |      |    | ×  |
|                   |          | CY, [HL].bit    | 2     | 1      | 4      | $CY \leftarrow CY \vee (HL).bit$                                                 |      |    | ×  |
|                   |          | CY, ES:[HL].bit | 3     | 2      | 5      | $CY \leftarrow CY \vee (ES, HL).bit$                                             |      |    | ×  |

**Notes 1.** Number of CPU clocks ( $f_{CLK}$ ) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

**2.** Number of CPU clocks ( $f_{CLK}$ ) when the program memory area is accessed.

**Remark** Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 29-5. Operation List (14/17)

| Instruction Group | Mnemonic | Operands        | Bytes | Clocks |        | Clocks                                 | Flag |    |    |
|-------------------|----------|-----------------|-------|--------|--------|----------------------------------------|------|----|----|
|                   |          |                 |       | Note 1 | Note 2 |                                        | Z    | AC | CY |
| Bit manipulate    | XOR1     | CY, A.bit       | 2     | 1      | –      | $CY \leftarrow CY \nabla A.bit$        |      |    | ×  |
|                   |          | CY, PSW.bit     | 3     | 1      | –      | $CY \leftarrow CY \nabla PSW.bit$      |      |    | ×  |
|                   |          | CY, saddr.bit   | 3     | 1      | –      | $CY \leftarrow CY \nabla (saddr).bit$  |      |    | ×  |
|                   |          | CY, sfr.bit     | 3     | 1      | –      | $CY \leftarrow CY \nabla sfr.bit$      |      |    | ×  |
|                   |          | CY, [HL].bit    | 2     | 1      | 4      | $CY \leftarrow CY \nabla (HL).bit$     |      |    | ×  |
|                   |          | CY, ES:[HL].bit | 3     | 2      | 5      | $CY \leftarrow CY \nabla (ES, HL).bit$ |      |    | ×  |
|                   | SET1     | A.bit           | 2     | 1      | –      | $A.bit \leftarrow 1$                   |      |    |    |
|                   |          | PSW.bit         | 3     | 4      | –      | $PSW.bit \leftarrow 1$                 | ×    | ×  | ×  |
|                   |          | !addr16.bit     | 4     | 2      | –      | $(addr16).bit \leftarrow 1$            |      |    |    |
|                   |          | ES:!addr16.bit  | 5     | 3      | –      | $(ES, addr16).bit \leftarrow 1$        |      |    |    |
|                   |          | saddr.bit       | 3     | 2      | –      | $(saddr).bit \leftarrow 1$             |      |    |    |
|                   |          | sfr.bit         | 3     | 2      | –      | $sfr.bit \leftarrow 1$                 |      |    |    |
|                   |          | [HL].bit        | 2     | 2      | –      | $(HL).bit \leftarrow 1$                |      |    |    |
|                   |          | ES:[HL].bit     | 3     | 3      | –      | $(ES, HL).bit \leftarrow 1$            |      |    |    |
|                   | CLR1     | A.bit           | 2     | 1      | –      | $A.bit \leftarrow 0$                   |      |    |    |
|                   |          | PSW.bit         | 3     | 4      | –      | $PSW.bit \leftarrow 0$                 | ×    | ×  | ×  |
|                   |          | !addr16.bit     | 4     | 2      | –      | $(addr16).bit \leftarrow 0$            |      |    |    |
|                   |          | ES:!addr16.bit  | 5     | 3      | –      | $(ES, addr16).bit \leftarrow 0$        |      |    |    |
|                   |          | saddr.bit       | 3     | 2      | –      | $(saddr).bit \leftarrow 0$             |      |    |    |
|                   |          | sfr.bit         | 3     | 2      | –      | $sfr.bit \leftarrow 0$                 |      |    |    |
|                   |          | [HL].bit        | 2     | 2      | –      | $(HL).bit \leftarrow 0$                |      |    |    |
|                   |          | ES:[HL].bit     | 3     | 3      | –      | $(ES, HL).bit \leftarrow 0$            |      |    |    |
|                   | SET1     | CY              | 2     | 1      | –      | $CY \leftarrow 1$                      |      |    | 1  |
|                   | CLR1     | CY              | 2     | 1      | –      | $CY \leftarrow 0$                      |      |    | 0  |
|                   | NOT1     | CY              | 2     | 1      | –      | $CY \leftarrow CY$                     |      |    | ×  |

**Notes 1.** Number of CPU clocks ( $f_{CLK}$ ) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed

**2.** Number of CPU clocks ( $f_{CLK}$ ) when the program memory area is accessed.

**Remark** Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 29-5. Operation List (15/17)

| Instruction Group | Mnemonic | Operands  | Bytes | Clocks |        | Clocks                                                                                                                                                                                                                             | Flag |    |    |
|-------------------|----------|-----------|-------|--------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|----|----|
|                   |          |           |       | Note 1 | Note 2 |                                                                                                                                                                                                                                    | Z    | AC | CY |
| Call/<br>return   | CALL     | rp        | 2     | 3      | –      | (SP – 2) ← (PC+2) <sub>S</sub> , (SP – 3) ← (PC+2) <sub>H</sub> ,<br>(SP – 4) ← (PC+2) <sub>L</sub> , PC ← CS, rp,<br>SP ← SP – 4                                                                                                  |      |    |    |
|                   |          | \$!addr20 | 3     | 3      | –      | (SP – 2) ← (PC+3) <sub>S</sub> , (SP – 3) ← (PC+3) <sub>H</sub> ,<br>(SP – 4) ← (PC+3) <sub>L</sub> , PC ← PC+3+jdisp16,<br>SP ← SP – 4                                                                                            |      |    |    |
|                   |          | !addr16   | 3     | 3      | –      | (SP – 2) ← (PC+3) <sub>S</sub> , (SP – 3) ← (PC+3) <sub>H</sub> ,<br>(SP – 4) ← (PC+3) <sub>L</sub> , PC ← 0000, addr16,<br>SP ← SP – 4                                                                                            |      |    |    |
|                   |          | !!addr20  | 4     | 3      | –      | (SP – 2) ← (PC+4) <sub>S</sub> , (SP – 3) ← (PC+4) <sub>H</sub> ,<br>(SP – 4) ← (PC+4) <sub>L</sub> , PC ← addr20,<br>SP ← SP – 4                                                                                                  |      |    |    |
|                   | CALLT    | [addr5]   | 2     | 5      | –      | (SP – 2) ← (PC+2) <sub>S</sub> , (SP – 3) ← (PC+2) <sub>H</sub> ,<br>(SP – 4) ← (PC+2) <sub>L</sub> , PC <sub>S</sub> ← 0000,<br>PC <sub>H</sub> ← (0000, addr5+1),<br>PC <sub>L</sub> ← (0000, addr5),<br>SP ← SP – 4             |      |    |    |
|                   | BRK      | -         | 2     | 5      | –      | (SP – 1) ← PSW, (SP – 2) ← (PC+2) <sub>S</sub> ,<br>(SP – 3) ← (PC+2) <sub>H</sub> , (SP – 4) ← (PC+2) <sub>L</sub> ,<br>PC <sub>S</sub> ← 0000,<br>PC <sub>H</sub> ← (0007FH), PC <sub>L</sub> ← (0007EH),<br>SP ← SP – 4, IE ← 0 |      |    |    |
|                   | RET      | -         | 1     | 6      | –      | PC <sub>L</sub> ← (SP), PC <sub>H</sub> ← (SP+1),<br>PC <sub>S</sub> ← (SP+2), SP ← SP+4                                                                                                                                           |      |    |    |
|                   | RETI     | -         | 2     | 6      | –      | PC <sub>L</sub> ← (SP), PC <sub>H</sub> ← (SP+1),<br>PC <sub>S</sub> ← (SP+2), PSW ← (SP+3),<br>SP ← SP+4                                                                                                                          | R    | R  | R  |
|                   | RETB     | -         | 2     | 6      | –      | PC <sub>L</sub> ← (SP), PC <sub>H</sub> ← (SP+1),<br>PC <sub>S</sub> ← (SP+2), PSW ← (SP+3),<br>SP ← SP+4                                                                                                                          | R    | R  | R  |

- Notes**
1. Number of CPU clocks ( $f_{CLK}$ ) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
  2. Number of CPU clocks ( $f_{CLK}$ ) when the program memory area is accessed.

**Remark** Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 29-5. Operation List (16/17)

| Instruction Group    | Mnemonic | Operands              | Bytes | Clocks               |        | Clocks                                                                          | Flag |    |    |
|----------------------|----------|-----------------------|-------|----------------------|--------|---------------------------------------------------------------------------------|------|----|----|
|                      |          |                       |       | Note 1               | Note 2 |                                                                                 | Z    | AC | CY |
| Stack manipulate     | PUSH     | PSW                   | 2     | 1                    | –      | $(SP - 1) \leftarrow PSW, (SP - 2) \leftarrow 00H,$<br>$SP \leftarrow SP - 2$   |      |    |    |
|                      |          | rp                    | 1     | 1                    | –      | $(SP - 1) \leftarrow rp_H, (SP - 2) \leftarrow rp_L,$<br>$SP \leftarrow SP - 2$ |      |    |    |
|                      | POP      | PSW                   | 2     | 3                    | –      | $PSW \leftarrow (SP + 1), SP \leftarrow SP + 2$                                 | R    | R  | R  |
|                      |          | rp                    | 1     | 1                    | –      | $rp_L \leftarrow (SP), rp_H \leftarrow (SP + 1), SP \leftarrow SP + 2$          |      |    |    |
|                      | MOVW     | SP, #word             | 4     | 1                    | –      | $SP \leftarrow word$                                                            |      |    |    |
|                      |          | SP, AX                | 2     | 1                    | –      | $SP \leftarrow AX$                                                              |      |    |    |
|                      |          | AX, SP                | 2     | 1                    | –      | $AX \leftarrow SP$                                                              |      |    |    |
|                      |          | HL, SP                | 3     | 1                    | –      | $HL \leftarrow SP$                                                              |      |    |    |
|                      |          | BC, SP                | 3     | 1                    | –      | $BC \leftarrow SP$                                                              |      |    |    |
|                      |          | DE, SP                | 3     | 1                    | –      | $DE \leftarrow SP$                                                              |      |    |    |
|                      |          |                       |       |                      |        |                                                                                 |      |    |    |
|                      | ADDW     | SP, #byte             | 2     | 1                    | –      | $SP \leftarrow SP + byte$                                                       |      |    |    |
|                      | SUBW     | SP, #byte             | 2     | 1                    | –      | $SP \leftarrow SP - byte$                                                       |      |    |    |
| Unconditional branch | BR       | AX                    | 2     | 3                    | –      | $PC \leftarrow CS, AX$                                                          |      |    |    |
|                      |          | \$addr20              | 2     | 3                    | –      | $PC \leftarrow PC + 2 + jdisp8$                                                 |      |    |    |
|                      |          | !\$addr20             | 3     | 3                    | –      | $PC \leftarrow PC + 3 + jdisp16$                                                |      |    |    |
|                      |          | !addr16               | 3     | 3                    | –      | $PC \leftarrow 0000, addr16$                                                    |      |    |    |
|                      |          | !!addr20              | 4     | 3                    | –      | $PC \leftarrow addr20$                                                          |      |    |    |
| Conditional branch   | BC       | \$addr20              | 2     | 2/4 <sup>Note3</sup> | –      | $PC \leftarrow PC + 2 + jdisp8$ if $CY = 1$                                     |      |    |    |
|                      | BNC      | \$addr20              | 2     | 2/4 <sup>Note3</sup> | –      | $PC \leftarrow PC + 2 + jdisp8$ if $CY = 0$                                     |      |    |    |
|                      | BZ       | \$addr20              | 2     | 2/4 <sup>Note3</sup> | –      | $PC \leftarrow PC + 2 + jdisp8$ if $Z = 1$                                      |      |    |    |
|                      | BNZ      | \$addr20              | 2     | 2/4 <sup>Note3</sup> | –      | $PC \leftarrow PC + 2 + jdisp8$ if $Z = 0$                                      |      |    |    |
|                      | BH       | \$addr20              | 3     | 2/4 <sup>Note3</sup> | –      | $PC \leftarrow PC + 3 + jdisp8$ if $(Z \vee CY) = 0$                            |      |    |    |
|                      | BNH      | \$addr20              | 3     | 2/4 <sup>Note3</sup> | –      | $PC \leftarrow PC + 3 + jdisp8$ if $(Z \vee CY) = 1$                            |      |    |    |
|                      | BT       | saddr.bit, \$addr20   | 4     | 3/5 <sup>Note3</sup> | –      | $PC \leftarrow PC + 4 + jdisp8$ if (saddr).bit = 1                              |      |    |    |
|                      |          | sfr.bit, \$addr20     | 4     | 3/5 <sup>Note3</sup> | –      | $PC \leftarrow PC + 4 + jdisp8$ if sfr.bit = 1                                  |      |    |    |
|                      |          | A.bit, \$addr20       | 3     | 3/5 <sup>Note3</sup> | –      | $PC \leftarrow PC + 3 + jdisp8$ if A.bit = 1                                    |      |    |    |
|                      |          | PSW.bit, \$addr20     | 4     | 3/5 <sup>Note3</sup> | –      | $PC \leftarrow PC + 4 + jdisp8$ if PSW.bit = 1                                  |      |    |    |
|                      |          | [HL].bit, \$addr20    | 3     | 3/5 <sup>Note3</sup> | 6/7    | $PC \leftarrow PC + 3 + jdisp8$ if (HL).bit = 1                                 |      |    |    |
|                      |          | ES:[HL].bit, \$addr20 | 4     | 4/6 <sup>Note3</sup> | 7/8    | $PC \leftarrow PC + 4 + jdisp8$ if (ES, HL).bit = 1                             |      |    |    |

- Notes**
1. Number of CPU clocks ( $f_{CLK}$ ) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
  2. Number of CPU clocks ( $f_{CLK}$ ) when the program memory area is accessed.
  3. This indicates the number of clocks “when condition is not met/when condition is met”.

**Remark** Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 29-5. Operation List (17/17)

| Instruction Group  | Mnemonic             | Operands              | Bytes | Clocks               |        | Clocks                                                              | Flag |    |    |
|--------------------|----------------------|-----------------------|-------|----------------------|--------|---------------------------------------------------------------------|------|----|----|
|                    |                      |                       |       | Note 1               | Note 2 |                                                                     | Z    | AC | CY |
| Conditional branch | BF                   | saddr.bit, \$addr20   | 4     | 3/5 <sup>Note3</sup> | –      | PC ← PC + 4 + jdisp8 if (saddr).bit = 0                             |      |    |    |
|                    |                      | sfr.bit, \$addr20     | 4     | 3/5 <sup>Note3</sup> | –      | PC ← PC + 4 + jdisp8 if sfr.bit = 0                                 |      |    |    |
|                    |                      | A.bit, \$addr20       | 3     | 3/5 <sup>Note3</sup> | –      | PC ← PC + 3 + jdisp8 if A.bit = 0                                   |      |    |    |
|                    |                      | PSW.bit, \$addr20     | 4     | 3/5 <sup>Note3</sup> | –      | PC ← PC + 4 + jdisp8 if PSW.bit = 0                                 |      |    |    |
|                    |                      | [HL].bit, \$addr20    | 3     | 3/5 <sup>Note3</sup> | 6/7    | PC ← PC + 3 + jdisp8 if (HL).bit = 0                                |      |    |    |
|                    |                      | ES:[HL].bit, \$addr20 | 4     | 4/6 <sup>Note3</sup> | 7/8    | PC ← PC + 4 + jdisp8 if (ES, HL).bit = 0                            |      |    |    |
|                    | BTCLR                | saddr.bit, \$addr20   | 4     | 3/5 <sup>Note3</sup> | –      | PC ← PC + 4 + jdisp8 if (saddr).bit = 1<br>then reset (saddr).bit   |      |    |    |
|                    |                      | sfr.bit, \$addr20     | 4     | 3/5 <sup>Note3</sup> | –      | PC ← PC + 4 + jdisp8 if sfr.bit = 1<br>then reset sfr.bit           |      |    |    |
|                    |                      | A.bit, \$addr20       | 3     | 3/5 <sup>Note3</sup> | –      | PC ← PC + 3 + jdisp8 if A.bit = 1<br>then reset A.bit               |      |    |    |
|                    |                      | PSW.bit, \$addr20     | 4     | 3/5 <sup>Note3</sup> | –      | PC ← PC + 4 + jdisp8 if PSW.bit = 1<br>then reset PSW.bit           | ×    | ×  | ×  |
|                    |                      | [HL].bit, \$addr20    | 3     | 3/5 <sup>Note3</sup> | –      | PC ← PC + 3 + jdisp8 if (HL).bit = 1<br>then reset (HL).bit         |      |    |    |
|                    |                      | ES:[HL].bit, \$addr20 | 4     | 4/6 <sup>Note3</sup> | –      | PC ← PC + 4 + jdisp8 if (ES, HL).bit = 1<br>then reset (ES, HL).bit |      |    |    |
| Conditional skip   | SKC                  | –                     | 2     | 1                    | –      | Next instruction skip if CY = 1                                     |      |    |    |
|                    | SKNC                 | –                     | 2     | 1                    | –      | Next instruction skip if CY = 0                                     |      |    |    |
|                    | SKZ                  | –                     | 2     | 1                    | –      | Next instruction skip if Z = 1                                      |      |    |    |
|                    | SKNZ                 | –                     | 2     | 1                    | –      | Next instruction skip if Z = 0                                      |      |    |    |
|                    | SKH                  | –                     | 2     | 1                    | –      | Next instruction skip if (Z∨CY)=0                                   |      |    |    |
|                    | SKNH                 | –                     | 2     | 1                    | –      | Next instruction skip if (Z∨CY)=1                                   |      |    |    |
| CPU control        | SEL <sup>Note4</sup> | RBn                   | 2     | 1                    | –      | RBS[1:0] ← n                                                        |      |    |    |
|                    | NOP                  | –                     | 1     | 1                    | –      | No Operation                                                        |      |    |    |
|                    | EI                   | –                     | 3     | 4                    | –      | IE ← 1 (Enable Interrupt)                                           |      |    |    |
|                    | DI                   | –                     | 3     | 4                    | –      | IE ← 0 (Disable Interrupt)                                          |      |    |    |
|                    | HALT                 | –                     | 2     | 3                    | –      | Set HALT Mode                                                       |      |    |    |
|                    | STOP                 | –                     | 2     | 3                    | –      | Set STOP Mode                                                       |      |    |    |

- Notes**
1. Number of CPU clocks ( $f_{CLK}$ ) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
  2. Number of CPU clocks ( $f_{CLK}$ ) when the program memory area is accessed.
  3. This indicates the number of clocks “when condition is not met/when condition is met”.

**Remark** Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

**CHAPTER 30 ELECTRICAL SPECIFICATIONS**

**Cautions** 1. The RL78/L12 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

<R> 2. With products not provided with an EV<sub>DD</sub>, or EV<sub>SS</sub> pin, replace EV<sub>DD</sub> with V<sub>DD</sub>, or replace EV<sub>SS</sub> with V<sub>SS</sub>.

<R> 3. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.1.6 Pins for each product (pins other than port pins).

### 30.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings (T<sub>A</sub> = 25°C) (1/3)

| Parameter                | Symbols            | Conditions                                                                                                         | Ratings                                                                                      | Unit |
|--------------------------|--------------------|--------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------|------|
| Supply voltage           | V <sub>DD</sub>    | V <sub>DD</sub> = EV <sub>DD</sub>                                                                                 | −0.5 to +6.5                                                                                 | V    |
|                          | EV <sub>DD</sub>   | V <sub>DD</sub> = EV <sub>DD</sub>                                                                                 | −0.5 to +6.5                                                                                 | V    |
|                          | V <sub>SS</sub>    |                                                                                                                    | −0.5 to +0.3                                                                                 | V    |
|                          | EV <sub>SS</sub>   |                                                                                                                    | −0.5 to +0.3                                                                                 | V    |
| REGC pin input voltage   | V <sub>IREGC</sub> | REGC                                                                                                               | −0.3 to +2.8<br>and −0.3 to V <sub>DD</sub> +0.3 <sup>Note 1</sup>                           | V    |
| <R> Input voltage        | V <sub>I1</sub>    | P10 to P17, P30 to P32, P40 to P43, P50 to P54,<br>P70 to P74, P120, P125 to P127, P140 to P147                    | −0.3 to EV <sub>DD</sub> +0.3<br>and −0.3 to V <sub>DD</sub> +0.3 <sup>Note 2</sup>          | V    |
|                          | V <sub>I2</sub>    | P60, P61 (N-ch open-drain)                                                                                         | −0.3 to EV <sub>DD</sub> +0.3<br>and −0.3 to V <sub>DD</sub> +0.3 <sup>Note 2</sup>          | V    |
|                          | V <sub>I3</sub>    | P20, P21, P121 to P124, P137, EXCLK,<br>EXCLKS, RESET                                                              | −0.3 to V <sub>DD</sub> +0.3 <sup>Note 2</sup>                                               | V    |
| Output voltage           | V <sub>O1</sub>    | P10 to P17, P30 to P32, P40 to P43,<br>P50 to P54, P60, P61, P70 to P74, P120,<br>P125 to P127, P130, P140 to P147 | −0.3 to EV <sub>DD</sub> +0.3<br>and −0.3 to V <sub>DD</sub> +0.3 <sup>Note 2</sup>          | V    |
|                          | V <sub>O2</sub>    | P20, P21                                                                                                           | −0.3 to V <sub>DD</sub> +0.3 <sup>Note 2</sup>                                               | V    |
| <R> Analog input voltage | V <sub>AI1</sub>   | ANI16 to ANI23                                                                                                     | −0.3 to EV <sub>DD</sub> +0.3 and<br>−0.3 to AV <sub>REF(+)</sub> +0.3 <sup>Notes 2, 3</sup> | V    |
|                          | V <sub>AI2</sub>   | ANI0, ANI1                                                                                                         | −0.3 to V <sub>DD</sub> +0.3 and<br>−0.3 to AV <sub>REF(+)</sub> +0.3 <sup>Notes 2, 3</sup>  | V    |

**Notes 1.** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**2.** Must be 6.5 V or lower.

<R> **3.** Do not exceed AV<sub>REF(+)</sub> + 0.3 V in case of A/D conversion target pin.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

<R> **2.** AV<sub>REF(+)</sub> : + side reference voltage of the A/D converter.



**Absolute Maximum Ratings (T<sub>A</sub> = 25°C) (2/3)**

| Parameter       | Symbols         | Conditions                                         | Ratings      | Unit |
|-----------------|-----------------|----------------------------------------------------|--------------|------|
| <R> LCD voltage | V <sub>L1</sub> | V <sub>L1</sub> voltage <sup>Note</sup>            | −0.3 to +2.8 | V    |
|                 | V <sub>L2</sub> | V <sub>L2</sub> voltage <sup>Note</sup>            | −0.3 to +6.5 | V    |
|                 | V <sub>L3</sub> | V <sub>L3</sub> voltage <sup>Note</sup>            | −0.3 to +6.5 | V    |
|                 | V <sub>L4</sub> | V <sub>L4</sub> voltage <sup>Note</sup>            | −0.3 to +6.5 | V    |
|                 | V <sub>L5</sub> | CAPL, CAPH voltage <sup>Note</sup>                 | −0.3 to +6.5 | V    |
|                 | V <sub>L6</sub> | COM0 to COM7, SEG0 to SEG38, COMEXP output voltage | −0.3 to +6.5 | V    |

<R> **Note** This value only indicates the absolute maximum ratings when applying voltage to the V<sub>L1</sub>, V<sub>L2</sub>, V<sub>L3</sub>, and V<sub>L4</sub> pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V<sub>SS</sub> via a capacitor (0.47  $\mu$ F  $\pm$  30%) and connect a capacitor (0.47  $\mu$ F  $\pm$  30%) between the CAPL and CAPH pins.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Absolute Maximum Ratings (TA = 25°C) (3/3)**

| Parameter                     | Symbols | Conditions                       |                                                                                                              | Ratings     | Unit |
|-------------------------------|---------|----------------------------------|--------------------------------------------------------------------------------------------------------------|-------------|------|
| Output current, high          | IOH1    | Per pin                          | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147           | −40         | mA   |
|                               |         | Total of all pins<br>−170 mA     | P10 to P14, P40 to P43, P120, P130, P140 to P147                                                             | −70         | mA   |
|                               |         |                                  | P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127                                                 | −100        | mA   |
|                               | IOH2    | Per pin                          | P20, P21                                                                                                     | −0.5        | mA   |
|                               |         | Total of all pins                |                                                                                                              | −1          | mA   |
| Output current, low           | IOL1    | Per pin                          | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147 | 40          | mA   |
|                               |         | Total of all pins<br>170 mA      | P10 to P14, P40 to P43, P120, P130, P140 to P147                                                             | 70          | mA   |
|                               |         |                                  | P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127                                       | 100         | mA   |
|                               | IOL2    | Per pin                          | P20, P21                                                                                                     | 1           | mA   |
|                               |         | Total of all pins                |                                                                                                              | 2           | mA   |
| Operating ambient temperature | TA      | In normal operation mode         |                                                                                                              | −40 to +85  | °C   |
|                               |         | In flash memory programming mode |                                                                                                              |             |      |
| Storage temperature           | Tstg    |                                  |                                                                                                              | −65 to +150 | °C   |

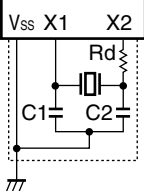
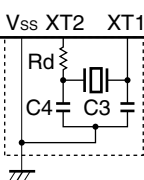
**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## &lt;R&gt; 30.2 Oscillator Characteristics

## 30.2.1 X1, XT1 oscillator characteristics

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ E<sub>VDD</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = E<sub>VSS</sub> = 0 V)

| Parameter                                                          | Resonator                               | Recommended Circuit                                                               | Conditions                      | MIN. | TYP.   | MAX. | Unit |
|--------------------------------------------------------------------|-----------------------------------------|-----------------------------------------------------------------------------------|---------------------------------|------|--------|------|------|
| X1 clock oscillation frequency (f <sub>x</sub> ) <sup>Note</sup>   | Ceramic resonator/<br>crystal resonator |  | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V | 1.0  |        | 20.0 | MHz  |
|                                                                    |                                         |                                                                                   | 1.8 V ≤ V <sub>DD</sub> < 2.7 V | 1.0  |        | 8.0  | MHz  |
|                                                                    |                                         |                                                                                   | 1.6 V ≤ V <sub>DD</sub> < 1.8 V | 1.0  |        | 4.0  | MHz  |
| XT1 clock oscillation frequency (f <sub>XT</sub> ) <sup>Note</sup> | Crystal resonator                       |  |                                 | 32   | 32.768 | 35   | kHz  |

**Note** Indicates only oscillator characteristics. Refer to 30.4 AC Characteristics for instruction execution time.

**Cautions 1.** When using the X1 oscillator, XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
  - Do not cross the wiring with the other signal lines.
  - Do not route the wiring near a signal line through which a high fluctuating current flows.
  - Always make the ground point of the oscillator capacitor the same potential as V<sub>SS</sub>.
  - Do not ground the capacitor to a ground pattern through which a high current flows.
  - Do not fetch signals from the oscillator.
2. Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.
  3. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the X1 oscillator. Particular care is therefore required with the wiring method when the XT1 clock is used.

### 30.2.2 On-chip oscillator characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.6\text{ V} \leq E_{VDD} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = E_{VSS} = 0\text{ V}$ )

| Oscillators                                                              | Parameters | Conditions                   |                                              | MIN. | TYP. | MAX. | Unit |
|--------------------------------------------------------------------------|------------|------------------------------|----------------------------------------------|------|------|------|------|
| High-speed on-chip oscillator clock frequency <sup>Note 1</sup>          | $f_{IH}$   |                              |                                              | 1    |      | 24   | MHz  |
| High-speed on-chip oscillator clock frequency accuracy <sup>Note 2</sup> |            | $-20$ to $+85^\circ\text{C}$ | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | -1   |      | +1   | %    |
|                                                                          |            |                              | $1.6\text{ V} \leq V_{DD} \leq 1.8\text{ V}$ | -5   |      | +5   | %    |
|                                                                          |            | $-40$ to $-20^\circ\text{C}$ | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | -1.5 |      | +1.5 | %    |
|                                                                          |            |                              | $1.6\text{ V} \leq V_{DD} \leq 1.8\text{ V}$ | -5.5 |      | +5.5 | %    |
| Low-speed on-chip oscillator clock frequency                             | $f_{IL}$   |                              |                                              |      | 15   |      | kHz  |
| Low-speed on-chip oscillator clock frequency accuracy                    |            |                              |                                              | -15  |      | +15  | %    |

**Notes 1.** High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

**2.** This indicates the oscillator characteristics only. Refer to **30.4 AC Characteristics** for instruction execution time.

### 30.3 DC Characteristics

#### 30.3.1 Pin characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.6\text{ V} \leq E_{VDD} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = E_{VSS} = 0\text{ V}$ )

(1/5)

| Items                                  | Symbol    | Conditions                                                                                                     |                                                           | MIN.                                         | TYP. | MAX.                    | Unit |
|----------------------------------------|-----------|----------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------|----------------------------------------------|------|-------------------------|------|
| Output current, high <sup>Note 1</sup> | $I_{OH1}$ | Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147 |                                                           |                                              |      | -10.0 <sup>Note 3</sup> | mA   |
|                                        |           | Total of P10 to P14, P40 to P43, P120, P130, P140 to P147<br>(When duty = 70% <sup>Note 2</sup> )              | $4.0\text{ V} \leq E_{VDD} \leq 5.5\text{ V}$             |                                              |      | -40.0                   | mA   |
|                                        |           |                                                                                                                | $2.7\text{ V} \leq E_{VDD} < 4.0\text{ V}$                |                                              |      | -8.0                    | mA   |
|                                        |           |                                                                                                                | $1.8\text{ V} \leq E_{VDD} < 2.7\text{ V}$                |                                              |      | -4.0                    | mA   |
|                                        |           |                                                                                                                | $1.6\text{ V} \leq E_{VDD} < 1.8\text{ V}$                |                                              |      | -2.0                    | mA   |
|                                        |           | Total of P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127<br>(When duty = 70% <sup>Note 2</sup> )  | $4.0\text{ V} \leq E_{VDD} \leq 5.5\text{ V}$             |                                              |      | -60.0                   | mA   |
|                                        |           |                                                                                                                | $2.7\text{ V} \leq E_{VDD} < 4.0\text{ V}$                |                                              |      | -15.0                   | mA   |
|                                        |           |                                                                                                                | $1.8\text{ V} \leq E_{VDD} < 2.7\text{ V}$                |                                              |      | -8.0                    | mA   |
|                                        |           |                                                                                                                | $1.6\text{ V} \leq E_{VDD} < 1.8\text{ V}$                |                                              |      | -4.0                    | mA   |
|                                        |           | Total of all pins<br>(When duty = 70% <sup>Note 2</sup> )                                                      |                                                           |                                              |      | -100.0                  | mA   |
|                                        | $I_{OH2}$ | P20, P21                                                                                                       | Per pin                                                   |                                              |      | -0.1 <sup>Note 3</sup>  | mA   |
|                                        |           |                                                                                                                | Total of all pins<br>(When duty = 70% <sup>Note 2</sup> ) | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |      | -1.5                    | mA   |

**Notes** 1. Value of current at which the device operation is guaranteed even if the current flows from the  $V_{DD}$ ,  $E_{VDD}$  pins to an output pin.

2. Specification under conditions where the duty factor is 70%.

The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to  $n\%$ ).

- Total output current of pins =  $(I_{OH} \times 0.7)/(n \times 0.01)$

<Example> Where  $n = 50\%$  and  $I_{OH} = -10.0\text{ mA}$

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(50 \times 0.01) = -14.0\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

3. Do not exceed the total current value.

**Caution** P10, P12, P15, P17 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 1.6 V ≤ EVDD = VDD ≤ 5.5 V, VSS = EVSS = 0 V)

(2/5)

| Items                                 | Symbol | Conditions                                                                                                              |                                                           | MIN.                | TYP. | MAX.                   | Unit |
|---------------------------------------|--------|-------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------|---------------------|------|------------------------|------|
| Output current, low <sup>Note 1</sup> | IOL1   | Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147          |                                                           |                     |      | 20.0 <sup>Note 3</sup> | mA   |
|                                       |        | Per pin for P60, P61                                                                                                    |                                                           |                     |      | 15.0 <sup>Note 3</sup> | mA   |
|                                       |        | Total of P10 to P14, P40 to P43, P120, P130, P140 to P147<br>(When duty = 70% <sup>Note 2</sup> )                       | 4.0 V ≤ EVDD ≤ 5.5 V                                      |                     |      | 70.0                   | mA   |
|                                       |        |                                                                                                                         | 2.7 V ≤ EVDD < 4.0 V                                      |                     |      | 15.0                   | mA   |
|                                       |        |                                                                                                                         | 1.8 V ≤ EVDD < 2.7 V                                      |                     |      | 9.0                    | mA   |
|                                       |        |                                                                                                                         | 1.6 V ≤ EVDD < 1.8 V                                      |                     |      | 4.5                    | mA   |
|                                       |        | Total of P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127<br>(When duty = 70% <sup>Note 2</sup> ) | 4.0 V ≤ EVDD ≤ 5.5 V                                      |                     |      | 80.0                   | mA   |
|                                       |        |                                                                                                                         | 2.7 V ≤ EVDD < 4.0 V                                      |                     |      | 35.0                   | mA   |
|                                       |        |                                                                                                                         | 1.8 V ≤ EVDD < 2.7 V                                      |                     |      | 20.0                   | mA   |
|                                       |        |                                                                                                                         | 1.6 V ≤ EVDD < 1.8 V                                      |                     |      | 10.0                   | mA   |
|                                       |        | Total of all pins<br>(When duty = 70% <sup>Note 2</sup> )                                                               |                                                           |                     |      | 150.0                  | mA   |
|                                       | IOL2   | P20, P21                                                                                                                | Per pin for                                               |                     |      | 0.4 <sup>Note 3</sup>  | mA   |
|                                       |        |                                                                                                                         | Total of all pins<br>(When duty = 70% <sup>Note 2</sup> ) | 1.6 V ≤ VDD ≤ 5.5 V |      | 5.0                    | mA   |

**Notes** 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EVSS and VSS pin.

2. Specification under conditions where the duty factor is 70%.

The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 50% and IOL = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(50 \times 0.01) = 14.0 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

3. Do not exceed the total current value.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ E<sub>VDD</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = E<sub>VSS</sub> = 0 V)

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| Items                  | Symbol           | Conditions                                                                                         |                                                      | MIN.                | TYP. | MAX.                | Unit |
|------------------------|------------------|----------------------------------------------------------------------------------------------------|------------------------------------------------------|---------------------|------|---------------------|------|
| Input voltage,<br>high | V <sub>IH1</sub> | P10 to P17, P30 to P32, P40 to P43,<br>P50 to P54, P70 to P74, P120,<br>P125 to P127, P140 to P147 | Normal input buffer                                  | 0.8E <sub>VDD</sub> |      | E <sub>VDD</sub>    | V    |
|                        | V <sub>IH2</sub> | P10, P11, P15, P16                                                                                 | TTL input buffer<br>4.0 V ≤ E <sub>VDD</sub> ≤ 5.5 V | 2.2                 |      | E <sub>VDD</sub>    | V    |
|                        |                  |                                                                                                    | TTL input buffer<br>3.3 V ≤ E <sub>VDD</sub> < 4.0 V | 2.0                 |      | E <sub>VDD</sub>    | V    |
|                        |                  |                                                                                                    | TTL input buffer<br>1.6 V ≤ E <sub>VDD</sub> < 3.3 V | 1.50                |      | E <sub>VDD</sub>    | V    |
|                        | V <sub>IH3</sub> | P20, P21                                                                                           |                                                      | 0.7V <sub>DD</sub>  |      | V <sub>DD</sub>     | V    |
|                        | V <sub>IH4</sub> | P60, P61                                                                                           |                                                      | 0.7E <sub>VDD</sub> |      | E <sub>VDD</sub>    | V    |
|                        | V <sub>IH5</sub> | P121 to P124, P137, EXCLK, EXCLKS, RESET                                                           |                                                      | 0.8V <sub>DD</sub>  |      | V <sub>DD</sub>     | V    |
| Input voltage,<br>low  | V <sub>IL1</sub> | P10 to P17, P30 to P32, P40 to P43,<br>P50 to P54, P70 to P74, P120,<br>P125 to P127, P140 to P147 | Normal input buffer                                  | 0                   |      | 0.2E <sub>VDD</sub> | V    |
|                        | V <sub>IL2</sub> | P10, P11, P15, P16                                                                                 | TTL input buffer<br>4.0 V ≤ E <sub>VDD</sub> ≤ 5.5 V | 0                   |      | 0.8                 | V    |
|                        |                  |                                                                                                    | TTL input buffer<br>3.3 V ≤ E <sub>VDD</sub> < 4.0 V | 0                   |      | 0.5                 | V    |
|                        |                  |                                                                                                    | TTL input buffer<br>1.6 V ≤ E <sub>VDD</sub> < 3.3 V | 0                   |      | 0.32                | V    |
|                        | V <sub>IL3</sub> | P20, P21                                                                                           |                                                      | 0                   |      | 0.3V <sub>DD</sub>  | V    |
|                        | V <sub>IL4</sub> | P60, P61                                                                                           |                                                      | 0                   |      | 0.3E <sub>VDD</sub> | V    |
|                        | V <sub>IL5</sub> | P121 to P124, P137, EXCLK, EXCLKS, RESET                                                           |                                                      | 0                   |      | 0.2V <sub>DD</sub>  | V    |

**Caution** The maximum value of V<sub>IH</sub> of P10, P12, P15, P17 is E<sub>VDD</sub>, even in the N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 1.6 V ≤ EVDD = VDD ≤ 5.5 V, VSS = EVSS = 0 V)

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| Items                | Symbol | Conditions                                                                                         | MIN.                                 | TYP.     | MAX. | Unit |
|----------------------|--------|----------------------------------------------------------------------------------------------------|--------------------------------------|----------|------|------|
| Output voltage, high | VOH1   | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147 | 4.0 V ≤ EVDD ≤ 5.5 V, IOH1 = -10 mA  | EVDD-1.5 |      | V    |
|                      |        |                                                                                                    | 4.0 V ≤ EVDD ≤ 5.5 V, IOH1 = -3.0 mA | EVDD-0.7 |      | V    |
|                      |        |                                                                                                    | 2.7 V ≤ EVDD ≤ 5.5 V, IOH1 = -2.0 mA | EVDD-0.6 |      | V    |
|                      |        |                                                                                                    | 1.8 V ≤ EVDD ≤ 5.5 V, IOH1 = -1.5 mA | EVDD-0.5 |      | V    |
|                      |        |                                                                                                    | 1.6 V ≤ EVDD < 5.5 V, IOH1 = -1.0 mA | EVDD-0.5 |      | V    |
|                      | VOH2   | P20, P21                                                                                           | 1.6 V ≤ VDD ≤ 5.5 V, IOH2 = -100 μA  | VDD-0.5  |      | V    |
| Output voltage, low  | VOL1   | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147 | 4.0 V ≤ EVDD ≤ 5.5 V, IOL1 = 20 mA   |          | 1.3  | V    |
|                      |        |                                                                                                    | 4.0 V ≤ EVDD ≤ 5.5 V, IOL1 = 8.5 mA  |          | 0.7  | V    |
|                      |        |                                                                                                    | 2.7 V ≤ EVDD ≤ 5.5 V, IOL1 = 3.0 mA  |          | 0.6  | V    |
|                      |        |                                                                                                    | 2.7 V ≤ EVDD ≤ 5.5 V, IOL1 = 1.5 mA  |          | 0.4  | V    |
|                      |        |                                                                                                    | 1.8 V ≤ EVDD ≤ 5.5 V, IOL1 = 0.6 mA  |          | 0.4  | V    |
|                      |        |                                                                                                    | 1.6 V ≤ EVDD < 5.5 V, IOL1 = 0.3 mA  |          | 0.4  | V    |
|                      | VOL2   | P20, P21                                                                                           | 1.6 V ≤ VDD ≤ 5.5 V, IOL2 = 400 μA   |          | 0.4  | V    |
|                      | VOL3   | P60, P61                                                                                           | 4.0 V ≤ EVDD ≤ 5.5 V, IOL3 = 15.0 mA |          | 2.0  | V    |
|                      |        |                                                                                                    | 4.0 V ≤ EVDD ≤ 5.5 V, IOL3 = 5.0 mA  |          | 0.4  | V    |
|                      |        |                                                                                                    | 2.7 V ≤ EVDD ≤ 5.5 V, IOL3 = 3.0 mA  |          | 0.4  | V    |
|                      |        |                                                                                                    | 1.8 V ≤ EVDD ≤ 5.5 V, IOL3 = 2.0 mA  |          | 0.4  | V    |
|                      |        |                                                                                                    | 1.6 V ≤ EVDD < 5.5 V, IOL3 = 1.0 mA  |          | 0.4  | V    |

**Caution** P10, P12, P15, P17 do not output high level in N-ch open-drain mode.**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



(T<sub>A</sub> = –40 to +85°C, 1.6 V ≤ E<sub>VDD</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = E<sub>VSS</sub> = 0 V)

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| Items                       | Symbol            | Conditions                                                                                             |                                                        | MIN.                                  | TYP. | MAX. | Unit |    |
|-----------------------------|-------------------|--------------------------------------------------------------------------------------------------------|--------------------------------------------------------|---------------------------------------|------|------|------|----|
| Input leakage current, high | I <sub>LIH1</sub> | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P140 to P147 | V <sub>I</sub> = EV <sub>DD</sub>                      |                                       |      |      | 1    | μA |
|                             | I <sub>LIH2</sub> | P20, P21, P137, RESET                                                                                  | V <sub>I</sub> = V <sub>DD</sub>                       |                                       |      |      | 1    | μA |
|                             | I <sub>LIH3</sub> | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)                                                         | V <sub>I</sub> = V <sub>DD</sub>                       | In input port or external clock input |      |      | 1    | μA |
|                             |                   |                                                                                                        |                                                        | In resonator connection               |      |      | 10   | μA |
| Input leakage current, low  | I <sub>LIL1</sub> | P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P140 to P147 | V <sub>I</sub> = EV <sub>SS</sub>                      |                                       |      |      | −1   | μA |
|                             | I <sub>LIL2</sub> | P20, P21, P137, RESET                                                                                  | V <sub>I</sub> = V <sub>SS</sub>                       |                                       |      |      | −1   | μA |
|                             | I <sub>LIL3</sub> | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)                                                         | V <sub>I</sub> = V <sub>SS</sub>                       | In input port or external clock input |      |      | −1   | μA |
|                             |                   |                                                                                                        |                                                        | In resonator connection               |      |      | −10  | μA |
| On-chip pll-up resistance   | R <sub>U1</sub>   | V <sub>I</sub> = EV <sub>SS</sub>                                                                      | SEGxx port                                             |                                       |      |      |      |    |
|                             |                   |                                                                                                        | 2.4 V ≤ EV <sub>DD</sub> = V <sub>DD</sub> ≤ 5.5 V     |                                       | 10   | 20   | 100  | kΩ |
|                             |                   |                                                                                                        | 1.6 V ≤ EV <sub>DD</sub> = V <sub>DD</sub> < 2.4 V     |                                       | 10   | 30   | 100  | kΩ |
|                             | R <sub>U2</sub>   |                                                                                                        | Ports other than above (Except for P60, P61, and P130) | 10                                    | 20   | 100  | kΩ   |    |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 30.3.2 Supply current characteristics

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ E<sub>VDD</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = E<sub>VSS</sub> = 0 V)

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| Parameter      | Symbol                             | Conditions                |                                              |                                                                          |                  | MIN.                    | TYP. | MAX. | Unit |
|----------------|------------------------------------|---------------------------|----------------------------------------------|--------------------------------------------------------------------------|------------------|-------------------------|------|------|------|
| Supply current | I <sub>DD1</sub> <sup>Note 1</sup> | Operating mode            | HS (high-speed main) mode <sup>Note 5</sup>  | f <sub>IH</sub> = 24 MHz <sup>Note 3</sup>                               | Basic operation  | V <sub>DD</sub> = 5.0 V |      | 1.5  | mA   |
|                |                                    |                           |                                              |                                                                          |                  | V <sub>DD</sub> = 3.0 V |      | 1.5  | mA   |
|                |                                    |                           |                                              |                                                                          | Normal operation | V <sub>DD</sub> = 5.0 V |      | 3.3  | mA   |
|                |                                    |                           |                                              |                                                                          |                  | V <sub>DD</sub> = 3.0 V |      | 3.3  | mA   |
|                |                                    |                           |                                              | f <sub>IH</sub> = 16 MHz <sup>Note 3</sup>                               | Normal operation | V <sub>DD</sub> = 5.0 V |      | 2.5  | mA   |
|                |                                    |                           |                                              |                                                                          |                  | V <sub>DD</sub> = 3.0 V |      | 2.5  | mA   |
|                |                                    |                           | LS (low-speed main) mode <sup>Note 5</sup>   | f <sub>IH</sub> = 8 MHz <sup>Note 3</sup>                                | Normal operation | V <sub>DD</sub> = 3.0 V |      | 1.2  | mA   |
|                |                                    |                           |                                              |                                                                          |                  | V <sub>DD</sub> = 2.0 V |      | 1.2  | mA   |
|                |                                    |                           | LV (low-voltage main) mode <sup>Note 5</sup> | f <sub>IH</sub> = 4 MHz <sup>Note 3</sup>                                | Normal operation | V <sub>DD</sub> = 3.0 V |      | 1.2  | mA   |
|                |                                    |                           |                                              |                                                                          |                  | V <sub>DD</sub> = 2.0 V |      | 1.2  | mA   |
|                |                                    |                           | HS (high-speed main) mode <sup>Note 5</sup>  | f <sub>MX</sub> = 20 MHz <sup>Note 2</sup> , V <sub>DD</sub> = 5.0 V     | Normal operation | Square wave input       |      | 2.8  | mA   |
|                |                                    |                           |                                              |                                                                          |                  | Resonator connection    |      | 3.0  | mA   |
|                |                                    |                           |                                              | f <sub>MX</sub> = 20 MHz <sup>Note 2</sup> , V <sub>DD</sub> = 3.0 V     | Normal operation | Square wave input       |      | 2.8  | mA   |
|                |                                    |                           |                                              |                                                                          |                  | Resonator connection    |      | 3.0  | mA   |
|                |                                    |                           |                                              | f <sub>MX</sub> = 10 MHz <sup>Note 2</sup> , V <sub>DD</sub> = 5.0 V     | Normal operation | Square wave input       |      | 1.8  | mA   |
|                |                                    |                           |                                              |                                                                          |                  | Resonator connection    |      | 1.8  | mA   |
|                |                                    |                           |                                              | f <sub>MX</sub> = 10 MHz <sup>Note 2</sup> , V <sub>DD</sub> = 3.0 V     | Normal operation | Square wave input       |      | 1.8  | mA   |
|                |                                    |                           |                                              |                                                                          |                  | Resonator connection    |      | 1.8  | mA   |
|                |                                    |                           | LS (low-speed main) mode <sup>Note 5</sup>   | f <sub>MX</sub> = 8 MHz <sup>Note 2</sup> , V <sub>DD</sub> = 3.0 V      | Normal operation | Square wave input       |      | 1.1  | mA   |
|                |                                    |                           |                                              |                                                                          |                  | Resonator connection    |      | 1.1  | mA   |
|                |                                    |                           |                                              | f <sub>MX</sub> = 8 MHz <sup>Note 2</sup> , V <sub>DD</sub> = 2.0 V      | Normal operation | Square wave input       |      | 1.1  | mA   |
|                |                                    |                           |                                              |                                                                          |                  | Resonator connection    |      | 1.1  | mA   |
|                |                                    | Subsystem clock operation |                                              | f <sub>SUB</sub> = 32.768 kHz <sup>Note 4</sup> , T <sub>A</sub> = -40°C | Normal operation | Square wave input       |      | 3.5  | μA   |
|                |                                    |                           |                                              |                                                                          |                  | Resonator connection    |      | 3.6  | μA   |
|                |                                    |                           |                                              | f <sub>SUB</sub> = 32.768 kHz <sup>Note 4</sup> , T <sub>A</sub> = +25°C | Normal operation | Square wave input       |      | 3.6  | μA   |
|                |                                    |                           |                                              |                                                                          |                  | Resonator connection    |      | 3.7  | μA   |
|                |                                    |                           |                                              | f <sub>SUB</sub> = 32.768 kHz <sup>Note 4</sup> , T <sub>A</sub> = +50°C | Normal operation | Square wave input       |      | 3.7  | μA   |
|                |                                    |                           |                                              |                                                                          |                  | Resonator connection    |      | 3.8  | μA   |
|                |                                    |                           |                                              | f <sub>SUB</sub> = 32.768 kHz <sup>Note 4</sup> , T <sub>A</sub> = +70°C | Normal operation | Square wave input       |      | 3.8  | μA   |
|                |                                    |                           |                                              |                                                                          |                  | Resonator connection    |      | 3.9  | μA   |
|                |                                    |                           |                                              | f <sub>SUB</sub> = 32.768 kHz <sup>Note 4</sup> , T <sub>A</sub> = +85°C | Normal operation | Square wave input       |      | 4.1  | μA   |
|                |                                    |                           |                                              |                                                                          |                  | Resonator connection    |      | 4.2  | μA   |

(Notes and Remarks are listed on the next page.)

**Notes** 1. Total current flowing into  $V_{DD}$  and  $EV_{DD}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD}$  or  $V_{SS}$ ,  $EV_{SS}$ . The values below the MAX. column include the peripheral operation current (except for back ground operation (BGO)). However, not including the current flowing into the watchdog timer, 12-bit interval timer, A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, and LCD controller driver.

&lt;R&gt;

2. When high-speed on-chip oscillator and subsystem clock are stopped. When real-time clock is stopped.

&lt;R&gt;

3. When high-speed system clock and subsystem clock are stopped. When real-time clock is stopped.

&lt;R&gt;

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When real-time clock, serial interface IICA, multiplier and divider/multiply-accumulator, and DMA controller are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

&lt;R&gt;

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 24 MHz

$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 16 MHz

LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 8 MHz

LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 4 MHz

**Remarks** 1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency

3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ E<sub>VDD</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = E<sub>VSS</sub> = 0 V)

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| Parameter                | Symbol                             | Conditions          |                                                                           |                                                                           |                         | MIN. | TYP. | MAX. | Unit |    |
|--------------------------|------------------------------------|---------------------|---------------------------------------------------------------------------|---------------------------------------------------------------------------|-------------------------|------|------|------|------|----|
| Supply current<br>Note 1 | I <sub>DD2</sub><br>Note 2         | HALT mode           | HS (high-speed main) mode<br>Note 7                                       | f <sub>IH</sub> = 24 MHz <sup>Note 4</sup>                                | V <sub>DD</sub> = 5.0 V |      | 0.44 | 1.28 | mA   |    |
|                          |                                    |                     |                                                                           |                                                                           | V <sub>DD</sub> = 3.0 V |      | 0.44 | 1.28 | mA   |    |
|                          |                                    |                     |                                                                           | f <sub>IH</sub> = 16 MHz <sup>Note 4</sup>                                | V <sub>DD</sub> = 5.0 V |      | 0.40 | 1.00 | mA   |    |
|                          |                                    |                     |                                                                           |                                                                           | V <sub>DD</sub> = 3.0 V |      | 0.40 | 1.00 | mA   |    |
|                          |                                    |                     | LS (low-speed main) mode<br>Note 7                                        | f <sub>IH</sub> = 8 MHz <sup>Note 4</sup>                                 | V <sub>DD</sub> = 3.0 V |      | 260  | 530  | μA   |    |
|                          |                                    |                     |                                                                           |                                                                           | V <sub>DD</sub> = 2.0 V |      | 260  | 530  | μA   |    |
|                          |                                    |                     | LV (low-voltage main) mode<br>Note 7                                      | f <sub>IH</sub> = 4 MHz <sup>Note 4</sup>                                 | V <sub>DD</sub> = 3.0 V |      | 420  | 640  | μA   |    |
|                          |                                    |                     |                                                                           |                                                                           | V <sub>DD</sub> = 2.0 V |      | 420  | 640  | μA   |    |
|                          |                                    |                     | HS (high-speed main) mode<br>Note 7                                       | f <sub>MX</sub> = 20 MHz <sup>Note 3</sup> ,<br>V <sub>DD</sub> = 5.0 V   | Square wave input       |      | 0.28 | 1.00 | mA   |    |
|                          |                                    |                     |                                                                           |                                                                           | Resonator connection    |      | 0.45 | 1.17 | mA   |    |
|                          |                                    |                     |                                                                           | f <sub>MX</sub> = 20 MHz <sup>Note 3</sup> ,<br>V <sub>DD</sub> = 3.0 V   | Square wave input       |      | 0.28 | 1.00 | mA   |    |
|                          |                                    |                     |                                                                           |                                                                           | Resonator connection    |      | 0.45 | 1.17 | mA   |    |
|                          |                                    |                     |                                                                           | f <sub>MX</sub> = 10 MHz <sup>Note 3</sup> ,<br>V <sub>DD</sub> = 5.0 V   | Square wave input       |      | 0.19 | 0.60 | mA   |    |
|                          |                                    |                     |                                                                           |                                                                           | Resonator connection    |      | 0.26 | 0.67 | mA   |    |
|                          |                                    |                     |                                                                           | f <sub>MX</sub> = 10 MHz <sup>Note 3</sup> ,<br>V <sub>DD</sub> = 3.0 V   | Square wave input       |      | 0.19 | 0.60 | mA   |    |
|                          |                                    |                     |                                                                           |                                                                           | Resonator connection    |      | 0.26 | 0.67 | mA   |    |
|                          |                                    |                     | LS (low-speed main) mode<br>Note 7                                        | f <sub>MX</sub> = 8 MHz <sup>Note 3</sup> ,<br>V <sub>DD</sub> = 3.0 V    | Square wave input       |      | 95   | 330  | μA   |    |
|                          |                                    |                     |                                                                           |                                                                           | Resonator connection    |      | 145  | 380  | μA   |    |
|                          |                                    |                     |                                                                           | f <sub>MX</sub> = 8 MHz <sup>Note 3</sup> ,<br>V <sub>DD</sub> = 2.0 V    | Square wave input       |      | 95   | 330  | μA   |    |
|                          |                                    |                     |                                                                           |                                                                           | Resonator connection    |      | 145  | 380  | μA   |    |
|                          |                                    |                     | Subsystem clock operation                                                 | f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup><br>T <sub>A</sub> = −40°C | Square wave input       |      | 0.31 | 0.57 | μA   |    |
|                          |                                    |                     |                                                                           |                                                                           | Resonator connection    |      | 0.50 | 0.76 | μA   |    |
|                          |                                    |                     |                                                                           | f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup><br>T <sub>A</sub> = +25°C | Square wave input       |      | 0.37 | 0.57 | μA   |    |
|                          |                                    |                     |                                                                           |                                                                           | Resonator connection    |      | 0.56 | 0.76 | μA   |    |
|                          |                                    |                     |                                                                           | f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup><br>T <sub>A</sub> = +50°C | Square wave input       |      | 0.46 | 1.17 | μA   |    |
|                          |                                    |                     |                                                                           |                                                                           | Resonator connection    |      | 0.65 | 1.36 | μA   |    |
|                          |                                    |                     |                                                                           | f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup><br>T <sub>A</sub> = +70°C | Square wave input       |      | 0.57 | 1.97 | μA   |    |
|                          |                                    |                     |                                                                           |                                                                           | Resonator connection    |      | 0.76 | 2.16 | μA   |    |
|                          |                                    |                     | f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup><br>T <sub>A</sub> = +85°C | Square wave input                                                         |                         | 0.85 | 3.37 | μA   |      |    |
|                          |                                    |                     |                                                                           | Resonator connection                                                      |                         | 1.04 | 3.56 | μA   |      |    |
|                          | I <sub>DD3</sub> <sup>Note 6</sup> | STOP mode<br>Note 8 | T <sub>A</sub> = −40°C                                                    |                                                                           |                         |      |      | 0.17 | 0.50 | μA |
|                          |                                    |                     | T <sub>A</sub> = +25°C                                                    |                                                                           |                         |      |      | 0.23 | 0.50 | μA |
|                          |                                    |                     | T <sub>A</sub> = +50°C                                                    |                                                                           |                         |      |      | 0.32 | 1.10 | μA |
|                          |                                    |                     | T <sub>A</sub> = +70°C                                                    |                                                                           |                         |      |      | 0.43 | 1.90 | μA |
|                          |                                    |                     | T <sub>A</sub> = +85°C                                                    |                                                                           |                         |      |      | 0.71 | 3.30 | μA |

(Notes and Remarks are listed on the next page.)

- |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Notes | <p><b>1.</b> Total current flowing into V<sub>DD</sub> and EV<sub>DD</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD</sub> or V<sub>SS</sub>, EV<sub>SS</sub>. The values below the MAX. column include the peripheral operation current (except for back ground operation (BGO)). However, not including the current flowing into the watchdog timer, 12-bit interval timer, A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, and LCD controller driver.</p> |
|       | <p><b>2.</b> During HALT instruction execution by flash memory.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <R>   | <p><b>3.</b> When high-speed on-chip oscillator and subsystem clock are stopped. When real-time clock and multiplier and divider/multiply-accumulator are stopped.</p>                                                                                                                                                                                                                                                                                                                                                                                           |
| <R>   | <p><b>4.</b> When high-speed system clock and subsystem clock are stopped. When real-time clock and multiplier and divider/multiply-accumulator are stopped.</p>                                                                                                                                                                                                                                                                                                                                                                                                 |
| <R>   | <p><b>5.</b> When operating real-time clock (RTC) and setting ultra-low current consumption (AMP<sub>HS1</sub> = 1). When high-speed on-chip oscillator and high-speed system clock are stopped. When real-time clock, serial interface IIC, multiplier and divider/multiply-accumulator, and DMA controller are stopped. The values below the MAX. column include the leakage current.</p>                                                                                                                                                                      |
| <R>   | <p><b>6.</b> When high-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. When real-time clock, serial interface IIC, multiplier and divider/multiply-accumulator, and DMA controller are stopped. The values below the MAX. column include the leakage current.</p>                                                                                                                                                                                                                                                            |
|       | <p><b>7.</b> Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|       | <p>HS (high-speed main) mode: <math>2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }24\text{ MHz}</math><br/> <math>2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}</math></p>                                                                                                                                                                                                                                                                                                                                               |
|       | <p>LS (low-speed main) mode: <math>1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}</math></p>                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <R>   | <p>LV (low-voltage main) mode: <math>1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}</math></p> <p><b>8.</b> Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.</p>                                                                                                                                                                                                                                                                                                                   |

- Remarks 1.** f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
3. f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

(TA = -40 to +85°C, 1.6 V ≤ EVDD = VDD ≤ 5.5 V, VSS = EVSS = 0 V)

(3/3)

| Parameter                                | Symbol                       | Conditions                          |                                                                                     | MIN. | TYP.                    | MAX.  | Unit |
|------------------------------------------|------------------------------|-------------------------------------|-------------------------------------------------------------------------------------|------|-------------------------|-------|------|
| RTC operating current                    | IRTC <sup>Notes 1, 2</sup>   | fMAIN is stopped                    |                                                                                     |      | 0.08 <sup>Note 12</sup> |       | μA   |
| 12-bit interval timer current            | IT <sup>Notes 1, 2</sup>     | fMAIN is stopped                    |                                                                                     |      | 0.08 <sup>Note 12</sup> |       | μA   |
| Watchdog timer operating current         | IWDT <sup>Notes 2, 3</sup>   | fIL = 15 kHz, fMAIN is stopped      |                                                                                     |      | 0.24                    |       | μA   |
| A/D converter operating current          | IADC <sup>Note 4</sup>       | When conversion at maximum speed    | Normal mode, AVREFP = VDD = 5.0 V                                                   |      | 1.3                     | 1.7   | mA   |
|                                          |                              |                                     | Low voltage mode, AVREFP = VDD = 3.0 V                                              |      | 0.5                     | 0.7   | mA   |
| A/D converter reference voltage current  | IADREF                       |                                     |                                                                                     |      | 75.0                    |       | μA   |
| Temperature sensor operating current     | ITMPS                        |                                     |                                                                                     |      | 75.0                    |       | μA   |
| LVD operating current                    | ILVD <sup>Note 5</sup>       |                                     |                                                                                     |      | 0.08                    |       | μA   |
| BGO operating current                    | IBGO <sup>Notes 6, 7</sup>   |                                     |                                                                                     |      | 2.00                    | 12.20 | mA   |
| Flash self-programming operating current | IFSP <sup>Note 8</sup>       |                                     |                                                                                     |      | 2.00                    | 12.20 | mA   |
| LCD operating current                    | ILCD1 <sup>Notes 9, 10</sup> | External resistance division method | VDD = EVDD = 5.0 V<br>VL4 = 5.0 V                                                   |      | 0.04                    | 0.2   | μA   |
|                                          | ILCD2 <sup>Note 9</sup>      | Internal voltage boosting method    | VDD = EVDD = 5.0 V<br>VL4 = 5.1 V (VLCD = 12H)                                      |      | 1.12                    | 3.7   | μA   |
|                                          |                              |                                     | VDD = EVDD = 3.0 V<br>VL4 = 3.0 V (VLCD = 04H)                                      |      | 0.63                    | 2.2   | μA   |
|                                          | ILCD3 <sup>Note 9</sup>      | Capacitor split method              | VDD = EVDD = 3.0 V<br>VL4 = 3.0 V                                                   |      | 0.12                    | 0.5   | μA   |
| SNOOZE operating current                 | ISNOZ                        | ADC operation                       | The mode is performed <sup>Note 11</sup>                                            |      | 0.50                    | 0.60  | mA   |
|                                          |                              |                                     | The A/D conversion operations are performed, Low voltage mode, AVREFP = VDD = 3.0 V |      | 1.20                    | 1.44  | mA   |
|                                          |                              | CSI/UART operation                  |                                                                                     |      | 0.70                    | 0.84  | mA   |

(Note, Caution and Remark are listed on the next page)

- Notes**
1. Current flowing only to the real-time clock (excluding the operating current of the XT1 oscillator). The TYP. value of the current value of the RL78/L12 is the sum of the TYP. values of either  $I_{DD1}$  or  $I_{DD2}$ , and  $I_{RTC}$ , when the real-time clock operates in operation mode or HALT mode. The  $I_{DD1}$  and  $I_{DD2}$  MAX. values also include the real-time clock operating current. However,  $I_{DD2}$  subsystem clock operation includes the operational current of the real-time clock.
  2. When high-speed on-chip oscillator and high-speed system clock are stopped.
  3. Current flowing only to the watchdog timer (including the operating current of the 15 kHz low-speed on-chip oscillator). The supply current value of the RL78/L12 is the sum of  $I_{DD1}$ ,  $I_{DD2}$  or  $I_{DD3}$  and  $I_{WDT}$  when the watchdog timer operates.
  4. Current flowing only to the A/D converter. The supply current value of the RL78/L12 is the sum of  $I_{DD1}$  or  $I_{DD2}$  and  $I_{ADC}$  when the A/D converter operates in an operation mode or the HALT mode.
  5. Current flowing only to the LVD circuit. The supply current value of the RL78/L12 is the sum of  $I_{DD1}$ ,  $I_{DD2}$  or  $I_{DD3}$  and  $I_{LVD}$  when the LVD circuit operates.
  6. Current flowing only when the BGO operates. The supply current value of the RL78/L12 is the sum of  $I_{DD1}$  or  $I_{DD2}$  and  $I_{BGO}$  when the BGO operates in an operation mode.
  - <R> 7. Current flowing during data flash programming (not including the CPU operating current). The TYP. value indicates the averaged current for repeated writing and erasing of contiguous 1 KB on the flash memory. The MAX. value indicates the inrush current that flows during flash programming.
  - <R> 8. Current flowing during code flash programming (not including the CPU operating current). The TYP. value indicates the averaged current for repeated writing and erasing of contiguous 1 KB on the flash memory. The MAX. value indicates the inrush current that flows during flash programming.
  - <R> 9. Current flowing only to the LCD controller/driver ( $V_{DD}$  pin). The supply current value of the RL78/L12 microcontrollers is the sum of the LCD operating current ( $I_{LCD1}$ ,  $I_{LCD2}$  or  $I_{LCD3}$ ) to the supply current ( $I_{DD1}$ , or  $I_{DD2}$ ) when the LCD controller/driver operates in an operation mode or HALT mode. Not including the current that flows through the LCD panel.
  - <R> The TYP. value and MAX. value are following conditions.
    - Set 20 pins as a segment function, all lighting
    - When  $f_{SUB}$  is selected for system clock, LCD clock = 128 Hz (LCDC0 = 07H)
    - 4-Time-Slice, 1/3 Bias Method
  10. Not including the current that flows through the external divider resistor when the external resistance division method is used.
  11. For shift time to the SNOOZE mode, see **19.3.3 SNOOZE mode**.
  - <R> 12. Add 200 nA when using  $f_{IL}$ .

- Remarks**
1.  $f_{IL}$ : Low-speed on-chip oscillator clock frequency
  2.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  3.  $f_{CLK}$ : CPU/peripheral hardware clock frequency
  4. Temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$

## 30.4 AC Characteristics

### 30.4.1 Basic operation

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.6\text{ V} \leq E_{VDD} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = E_{VSS} = 0\text{ V}$ )

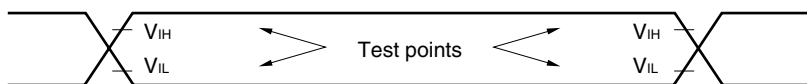
| Items                                                              | Symbol               | Conditions                                   |                                               | MIN.                                         | TYP.    | MAX. | Unit          |
|--------------------------------------------------------------------|----------------------|----------------------------------------------|-----------------------------------------------|----------------------------------------------|---------|------|---------------|
| Instruction cycle (minimum instruction execution time)             | $T_{CY}$             | Main system clock ( $f_{MAIN}$ ) operation   | HS (high-speed main) mode                     | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 0.04167 | 1    | $\mu\text{s}$ |
|                                                                    |                      |                                              |                                               | $2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$    | 0.0625  | 1    | $\mu\text{s}$ |
|                                                                    |                      |                                              | LV (low voltage main) mode                    | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 0.25    | 1    | $\mu\text{s}$ |
|                                                                    |                      |                                              | LS (low-speed main) mode                      | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 0.125   | 1    | $\mu\text{s}$ |
|                                                                    |                      | Subsystem clock ( $f_{SUB}$ ) operation      |                                               | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 28.5    | 30.5 | $\mu\text{s}$ |
|                                                                    |                      | In the self programming mode                 | HS (high-speed main) mode                     | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 0.04167 | 1    | $\mu\text{s}$ |
|                                                                    |                      |                                              |                                               | $2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$    | 0.0625  | 1    | $\mu\text{s}$ |
|                                                                    |                      |                                              | LV (low voltage main) mode                    | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 0.25    | 1    | $\mu\text{s}$ |
|                                                                    |                      |                                              | LS (low-speed main) mode                      | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 0.125   | 1    | $\mu\text{s}$ |
| External main system clock frequency                               | $f_{EX}$             | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |                                               | 1.0                                          |         | 20.0 | MHz           |
|                                                                    |                      | $1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$    |                                               | 1.0                                          |         | 8.0  | MHz           |
|                                                                    |                      | $1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$    |                                               | 1.0                                          |         | 4.0  | MHz           |
|                                                                    | $f_{EXS}$            |                                              |                                               | 32                                           |         | 35   | kHz           |
| External main system clock input high-level width, low-level width | $t_{EXH}, t_{EXL}$   | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |                                               | 24                                           |         |      | ns            |
|                                                                    |                      | $1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$    |                                               | 60                                           |         |      | ns            |
|                                                                    |                      | $1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$    |                                               | 120                                          |         |      | ns            |
|                                                                    | $t_{EXHS}, t_{EXLS}$ |                                              |                                               | 13.7                                         |         |      | $\mu\text{s}$ |
| TI00 to TI07 input high-level width, low-level width               | $t_{TIH}, t_{TIL}$   |                                              |                                               | $1/f_{MCK} + 10$                             |         |      | ns            |
| TO00 to TO07 output frequency                                      | $f_{TO}$             | HS (high-speed main) mode                    | $4.0\text{ V} \leq E_{VDD} \leq 5.5\text{ V}$ |                                              |         | 12   | MHz           |
|                                                                    |                      |                                              | $2.7\text{ V} \leq E_{VDD} < 4.0\text{ V}$    |                                              |         | 8    | MHz           |
|                                                                    |                      |                                              | $2.4\text{ V} \leq E_{VDD} < 2.7\text{ V}$    |                                              |         | 4    | MHz           |
|                                                                    |                      | LV (low voltage main) mode                   | $1.6\text{ V} \leq E_{VDD} \leq 5.5\text{ V}$ |                                              |         | 2    | MHz           |
|                                                                    |                      | LS (low-speed main) mode                     | $1.8\text{ V} \leq E_{VDD} \leq 5.5\text{ V}$ |                                              |         | 4    | MHz           |
| PCLBUZ0, PCLBUZ1 output frequency                                  | $f_{PCL}$            | HS (high-speed main) mode                    | $4.0\text{ V} \leq E_{VDD} \leq 5.5\text{ V}$ |                                              |         | 16   | MHz           |
|                                                                    |                      |                                              | $2.7\text{ V} \leq E_{VDD} < 4.0\text{ V}$    |                                              |         | 8    | MHz           |
|                                                                    |                      |                                              | $2.4\text{ V} \leq E_{VDD} < 2.7\text{ V}$    |                                              |         | 4    | MHz           |
|                                                                    |                      | LV (low voltage main) mode                   | $1.8\text{ V} \leq E_{VDD} \leq 5.5\text{ V}$ |                                              |         | 4    | MHz           |
|                                                                    |                      |                                              | $1.6\text{ V} \leq E_{VDD} < 1.8\text{ V}$    |                                              |         | 2    | MHz           |
|                                                                    |                      | LS (low-speed main) mode                     | $1.8\text{ V} \leq E_{VDD} \leq 5.5\text{ V}$ |                                              |         | 4    | MHz           |
| Interrupt input high-level width, low-level width                  | $t_{INTH}, t_{INTL}$ | INTP0                                        | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  | 1                                            |         |      | $\mu\text{s}$ |
|                                                                    |                      | INTP1 to INTP7                               | $1.6\text{ V} \leq E_{VDD} \leq 5.5\text{ V}$ | 1                                            |         |      | $\mu\text{s}$ |
| Key interrupt input low-level width                                | $t_{KR}$             | KR0 to KR3                                   | $1.8\text{ V} \leq E_{VDD} \leq 5.5\text{ V}$ | 250                                          |         |      | ns            |
|                                                                    |                      |                                              | $1.6\text{ V} \leq E_{VDD} < 1.8\text{ V}$    | 1                                            |         |      | $\mu\text{s}$ |
| $\overline{\text{RESET}}$ low-level width                          | $t_{RSL}$            |                                              |                                               | 10                                           |         |      | $\mu\text{s}$ |

**Remark**  $f_{MCK}$ : Timer array unit operation clock frequency

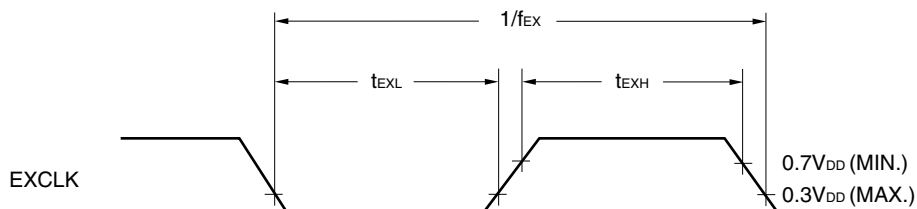
(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))



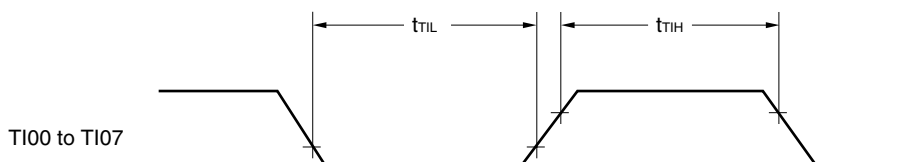
## &lt;R&gt; AC Timing Test Points



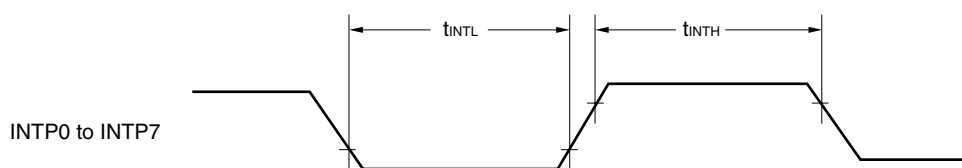
## External System Clock Timing



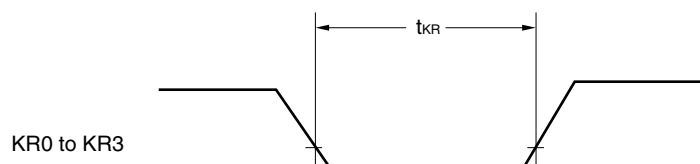
## TI/TO Timing

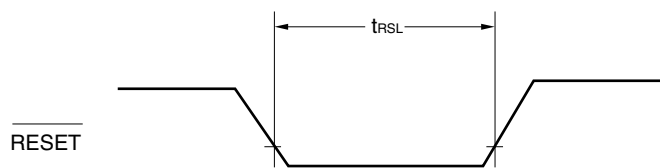


## Interrupt Request Input Timing



## Key Interrupt Input Timing



**RESET Input Timing**

## 30.5 Peripheral Functions Characteristics

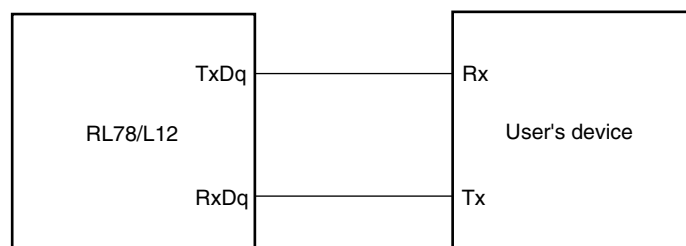
### 30.5.1 Serial array unit

#### (1) During communication at same potential (UART mode) (dedicated baud rate generator output)

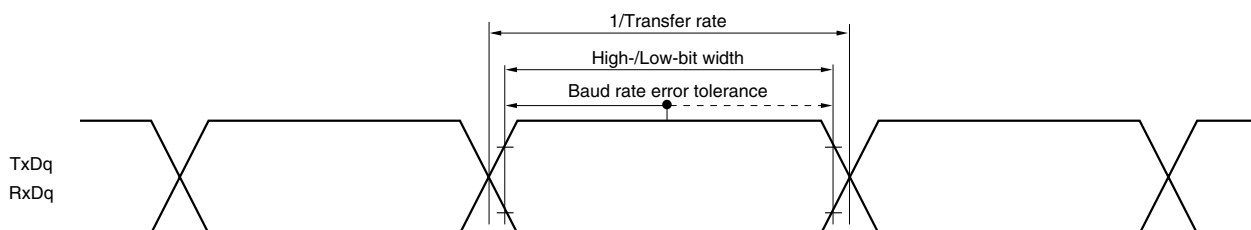
( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.6\text{ V} \leq \text{EV}_{\text{DD}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}} = 0\text{ V}$ )

| <R> | Parameter     | Symbol | Conditions                                                                                            | HS <sup>Note 1</sup> |                                         | LS <sup>Note 2</sup> |                                         | LV <sup>Note 3</sup> |                                         | Unit |
|-----|---------------|--------|-------------------------------------------------------------------------------------------------------|----------------------|-----------------------------------------|----------------------|-----------------------------------------|----------------------|-----------------------------------------|------|
|     |               |        |                                                                                                       | MIN.                 | MAX.                                    | MIN.                 | MAX.                                    | MIN.                 | MAX.                                    |      |
|     | Transfer rate |        | $2.4\text{ V} \leq \text{EV}_{\text{DD}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$                    |                      | $f_{\text{MCK}}/6$<br><sup>Note 4</sup> |                      | $f_{\text{MCK}}/6$<br><sup>Note 4</sup> |                      | $f_{\text{MCK}}/6$<br><sup>Note 4</sup> | bps  |
|     |               |        | Theoretical value of the maximum transfer rate<br>$f_{\text{MCK}} = f_{\text{CLK}}$ <sup>Note 5</sup> |                      | 4.0                                     |                      | 1.3                                     |                      | 0.7                                     | Mbps |
|     |               |        | $1.8\text{ V} \leq \text{EV}_{\text{DD}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$                    |                      |                                         |                      | $f_{\text{MCK}}/6$<br><sup>Note 4</sup> |                      | $f_{\text{MCK}}/6$<br><sup>Note 4</sup> | bps  |
|     |               |        | Theoretical value of the maximum transfer rate<br>$f_{\text{MCK}} = f_{\text{CLK}}$ <sup>Note 5</sup> |                      |                                         |                      | 1.3                                     |                      | 0.7                                     | Mbps |
|     |               |        | $1.6\text{ V} \leq \text{EV}_{\text{DD}} = \text{V}_{\text{DD}} \leq 5.5\text{ V}$                    |                      |                                         |                      |                                         |                      | $f_{\text{MCK}}/6$<br><sup>Note 4</sup> | bps  |
|     |               |        | Theoretical value of the maximum transfer rate<br>$f_{\text{MCK}} = f_{\text{CLK}}$ <sup>Note 5</sup> |                      |                                         |                      |                                         |                      | 0.7                                     | Mbps |

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



- <R> **Notes**
1. HS is condition of HS (high-speed main) mode.
  2. LS is condition of LS (low-speed main) mode.
  3. LV is condition of LV (low-voltage main) mode.
  4. Transfer rate in the SNOOZE mode is max. 9600 bps, min. 4800 bps.
  5.  $f_{\text{CLK}}$  in each operating mode is as below.
    - HS (high-speed main) mode:  $f_{\text{CLK}} = 24\text{ MHz}$
    - LS (low-speed main) mode:  $f_{\text{CLK}} = 8\text{ MHz}$
    - LV (low-voltage main) mode:  $f_{\text{CLK}} = 4\text{ MHz}$

**Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. q: UART number (q = 0), g: PIM and POM number (g = 1)
  2.  $f_{\text{MCK}}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,  
n: Channel number (mn = 00, 01))

(2) During communication at same potential (CSI mode) (master mode ( $f_{MCK}/2$ ,  $f_{MCK}/4$ ),  $\overline{SCKp}$ ... internal clock output)

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.6\text{ V} \leq EV_{DD} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS} = 0\text{ V}$ )

| <R> Parameter                                                                  | Symbol                   | Conditions                                    | HS <sup>Note 1</sup>                          |      | LS <sup>Note 2</sup>  |      | LV <sup>Note 3</sup>   |      | Unit |
|--------------------------------------------------------------------------------|--------------------------|-----------------------------------------------|-----------------------------------------------|------|-----------------------|------|------------------------|------|------|
|                                                                                |                          |                                               | MIN.                                          | MAX. | MIN.                  | MAX. | MIN.                   | MAX. |      |
| $\overline{SCKp}$ cycle time                                                   | $t_{KCY1}$               | $2.7\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ | 167 <sup>Note 4</sup>                         |      | 500 <sup>Note 4</sup> |      | 1000 <sup>Note 4</sup> |      | ns   |
|                                                                                |                          | $2.4\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ | 250 <sup>Note 4</sup>                         |      | 500 <sup>Note 4</sup> |      | 1000 <sup>Note 4</sup> |      | ns   |
|                                                                                |                          | $1.8\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ |                                               |      | 500 <sup>Note 4</sup> |      | 1000 <sup>Note 4</sup> |      | ns   |
|                                                                                |                          | $1.6\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ |                                               |      |                       |      | 1000 <sup>Note 4</sup> |      | ns   |
| $\overline{SCKp}$ high-/low-level width                                        | $t_{KH1}$ ,<br>$t_{KL1}$ | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ | $t_{KCY1}/2$<br>-12                           |      | $t_{KCY1}/2$<br>-50   |      | $t_{KCY1}/2$<br>-100   |      | ns   |
|                                                                                |                          | $2.7\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ | $t_{KCY1}/2$<br>-18                           |      | $t_{KCY1}/2$<br>-50   |      | $t_{KCY1}/2$<br>-100   |      | ns   |
|                                                                                |                          | $2.4\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ | $t_{KCY1}/2$<br>-38                           |      | $t_{KCY1}/2$<br>-50   |      | $t_{KCY1}/2$<br>-100   |      | ns   |
|                                                                                |                          | $1.8\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ |                                               |      | $t_{KCY1}/2$<br>-50   |      | $t_{KCY1}/2$<br>-100   |      | ns   |
|                                                                                |                          | $1.6\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ |                                               |      |                       |      | $t_{KCY1}/2$<br>-100   |      | ns   |
| Slp setup time (to $\overline{SCKp}\uparrow$ )<br><sup>Note 5</sup>            | $t_{SIK1}$               | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ | 44                                            |      | 110                   |      | 220                    |      | ns   |
|                                                                                |                          | $2.7\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ | 44                                            |      | 110                   |      | 220                    |      | ns   |
|                                                                                |                          | $2.4\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ | 75                                            |      | 110                   |      | 220                    |      | ns   |
|                                                                                |                          | $1.8\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ |                                               |      | 110                   |      | 220                    |      | ns   |
|                                                                                |                          | $1.6\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ |                                               |      |                       |      | 220                    |      | ns   |
| Slp hold time (from $\overline{SCKp}\uparrow$ )<br><sup>Note 6</sup>           | $t_{SH1}$                | $2.4\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ | 19                                            |      | 19                    |      | 19                     |      | ns   |
|                                                                                |                          | $1.8\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ |                                               |      | 19                    |      | 19                     |      |      |
|                                                                                |                          | $1.6\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ |                                               |      |                       |      | 19                     |      |      |
| Delay time from $\overline{SCKp}\downarrow$ to<br>SOp output <sup>Note 7</sup> | $t_{SO1}$                | $C = 30\text{ pF}$<br><sup>Note 8</sup>       | $2.4\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ | 25   |                       | 25   |                        | 25   | ns   |
|                                                                                |                          |                                               | $1.8\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ |      |                       | 25   |                        | 25   |      |
|                                                                                |                          |                                               | $1.6\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ |      |                       |      |                        | 25   |      |

<R> **Notes 1.** HS is condition of HS (high-speed main) mode.

<R> **2.** LS is condition of LS (low-speed main) mode.

<R> **3.** LV is condition of LV (low-voltage main) mode.

**4.** For CSI00, set a cycle of  $2/f_{MCK}$  or longer. For CSI01, set a cycle of  $4/f_{MCK}$  or longer.

**5.** When  $DAPmn = 0$  and  $CKPmn = 0$ , or  $DAPmn = 1$  and  $CKPmn = 1$ . The Slp setup time becomes “to  $\overline{SCKp}\downarrow$ ” when  $DAPmn = 0$  and  $CKPmn = 1$ , or  $DAPmn = 1$  and  $CKPmn = 0$ .

**6.** When  $DAPmn = 0$  and  $CKPmn = 0$ , or  $DAPmn = 1$  and  $CKPmn = 1$ . The Slp hold time becomes “from  $\overline{SCKp}\downarrow$ ” when  $DAPmn = 0$  and  $CKPmn = 1$ , or  $DAPmn = 1$  and  $CKPmn = 0$ .

**7.** When  $DAPmn = 0$  and  $CKPmn = 0$ , or  $DAPmn = 1$  and  $CKPmn = 1$ . The delay time to SOp output becomes “from  $\overline{SCKp}\uparrow$ ” when  $DAPmn = 0$  and  $CKPmn = 1$ , or  $DAPmn = 1$  and  $CKPmn = 0$ .

**8.** C is the load capacitance of the  $\overline{SCKp}$  and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and  $\overline{SCKp}$  pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remarks 1.** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),

g: PIM and POM numbers (g = 1)

**2.**  $f_{MCK}$ : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00, 01))

(3) During communication at same potential (CSI mode) (slave mode,  $\overline{\text{SCKp}}$ ... external clock input)(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS</sub> = 0 V)

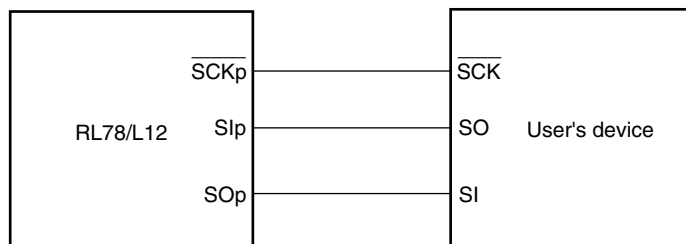
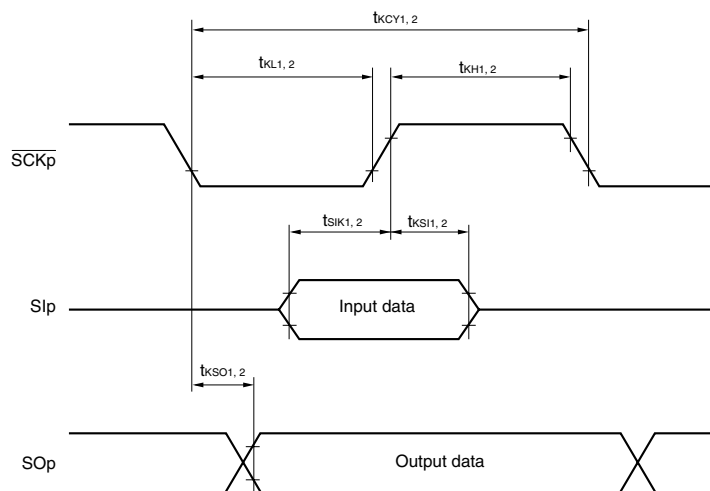
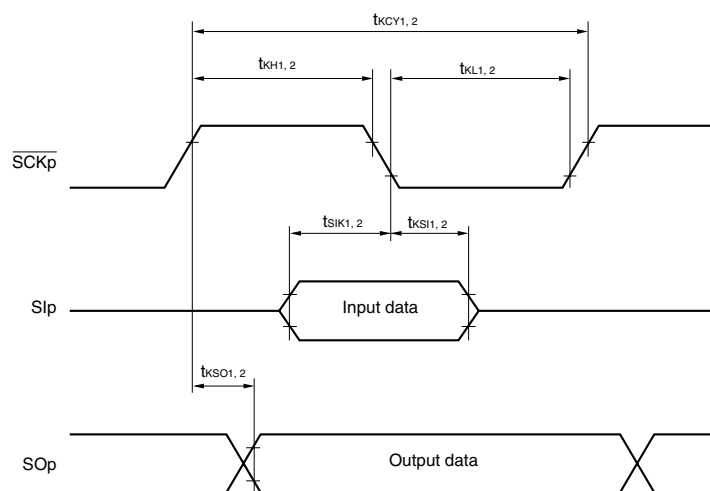
| <R> Parameter                                                                         | Symbol                                 | Conditions                       |                                  | HS <sup>Note 1</sup>        |                           | LS <sup>Note 2</sup>        |                            | LV <sup>Note 3</sup>        |                            | Unit |
|---------------------------------------------------------------------------------------|----------------------------------------|----------------------------------|----------------------------------|-----------------------------|---------------------------|-----------------------------|----------------------------|-----------------------------|----------------------------|------|
|                                                                                       |                                        |                                  |                                  | MIN.                        | MAX.                      | MIN.                        | MAX.                       | MIN.                        | MAX.                       |      |
| $\overline{\text{SCKp}}$ cycle time <sup>Note 4</sup>                                 | t <sub>KCY2</sub>                      | 4.0 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 20 MHz < f <sub>MCK</sub>        | 8/f <sub>MCK</sub>          |                           |                             |                            |                             |                            | ns   |
|                                                                                       |                                        |                                  | f <sub>MCK</sub> ≤ 20 MHz        | 6/f <sub>MCK</sub>          |                           | 6/f <sub>MCK</sub>          |                            | 6/f <sub>MCK</sub>          |                            | ns   |
|                                                                                       |                                        | 2.7 V ≤ EV <sub>DD</sub> < 4.0 V | 16 MHz < f <sub>MCK</sub>        | 8/f <sub>MCK</sub>          |                           |                             |                            |                             |                            | ns   |
|                                                                                       |                                        |                                  | f <sub>MCK</sub> ≤ 16 MHz        | 6/f <sub>MCK</sub>          |                           | 6/f <sub>MCK</sub>          |                            | 6/f <sub>MCK</sub>          |                            | ns   |
|                                                                                       |                                        | 2.4 V ≤ EV <sub>DD</sub> < 2.7 V | 12 MHz < f <sub>MCK</sub>        | 8/f <sub>MCK</sub>          |                           |                             |                            |                             |                            | ns   |
|                                                                                       |                                        |                                  | f <sub>MCK</sub> ≤ 12 MHz        | 6/f <sub>MCK</sub>          |                           | 6/f <sub>MCK</sub>          |                            | 6/f <sub>MCK</sub>          |                            | ns   |
|                                                                                       |                                        | 1.8 V ≤ EV <sub>DD</sub> < 2.4 V |                                  |                             |                           | 6/f <sub>MCK</sub>          |                            | 6/f <sub>MCK</sub>          |                            | ns   |
| $\overline{\text{SCKp}}$ high-/low-level width                                        | t <sub>KH2</sub> ,<br>t <sub>KL2</sub> | 4.0 V ≤ EV <sub>DD</sub> ≤ 5.5 V |                                  | t <sub>KCY2</sub> /2<br>-7  |                           | t <sub>KCY2</sub> /2<br>-7  |                            | t <sub>KCY2</sub> /2<br>-7  |                            | ns   |
|                                                                                       |                                        | 2.7 V ≤ EV <sub>DD</sub> < 4.0 V |                                  | t <sub>KCY2</sub> /2<br>-8  |                           | t <sub>KCY2</sub> /2<br>-8  |                            | t <sub>KCY2</sub> /2<br>-8  |                            | ns   |
|                                                                                       |                                        | 2.4 V ≤ EV <sub>DD</sub> < 2.7 V |                                  | t <sub>KCY2</sub> /2<br>-18 |                           | t <sub>KCY2</sub> /2<br>-18 |                            | t <sub>KCY2</sub> /2<br>-18 |                            | ns   |
|                                                                                       |                                        | 1.8 V ≤ EV <sub>DD</sub> < 2.4 V |                                  |                             |                           | t <sub>KCY2</sub> /2<br>-18 |                            | t <sub>KCY2</sub> /2<br>-18 |                            | ns   |
|                                                                                       |                                        | 1.6 V ≤ EV <sub>DD</sub> < 1.8 V |                                  |                             |                           |                             |                            | t <sub>KCY2</sub> /2<br>-66 |                            | ns   |
| Slp setup time<br>(to $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 5</sup>            | t <sub>SIK2</sub>                      | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V |                                  | 1/f <sub>MCK</sub><br>+20   |                           | 1/f <sub>MCK</sub><br>+30   |                            | 1/f <sub>MCK</sub><br>+30   |                            | ns   |
|                                                                                       |                                        | 2.4 V ≤ EV <sub>DD</sub> < 2.7 V |                                  | 1/f <sub>MCK</sub><br>+30   |                           | 1/f <sub>MCK</sub><br>+30   |                            | 1/f <sub>MCK</sub><br>+30   |                            |      |
|                                                                                       |                                        | 1.8 V ≤ EV <sub>DD</sub> < 2.4 V |                                  |                             |                           | 1/f <sub>MCK</sub><br>+30   |                            | 1/f <sub>MCK</sub><br>+30   |                            | ns   |
|                                                                                       |                                        | 1.6 V ≤ EV <sub>DD</sub> < 1.8 V |                                  |                             |                           |                             |                            | 1/f <sub>MCK</sub><br>+40   |                            | ns   |
| Slp hold time<br>(from $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 6</sup>           | t <sub>SH2</sub>                       | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V |                                  | 1/f <sub>MCK</sub><br>+31   |                           | 1/f <sub>MCK</sub><br>+31   |                            | 1/f <sub>MCK</sub><br>+31   |                            | ns   |
|                                                                                       |                                        | 1.8 V ≤ EV <sub>DD</sub> < 2.4 V |                                  |                             |                           | 1/f <sub>MCK</sub><br>+31   |                            | 1/f <sub>MCK</sub><br>+31   |                            | ns   |
|                                                                                       |                                        | 1.6 V ≤ EV <sub>DD</sub> < 1.8 V |                                  |                             |                           |                             |                            | 1/f <sub>MCK</sub> +<br>250 |                            | ns   |
| Delay time from $\overline{\text{SCKp}}\downarrow$<br>to SOp output <sup>Note 7</sup> | t <sub>KSO2</sub>                      | C = 30 pF <sup>Note 8</sup>      | 4.0 V ≤ EV <sub>DD</sub> ≤ 5.5 V |                             | 2/f <sub>MCK</sub><br>+44 |                             | 2/f <sub>MCK</sub><br>+110 |                             | 2/f <sub>MCK</sub><br>+110 | ns   |
|                                                                                       |                                        |                                  | 2.7 V ≤ EV <sub>DD</sub> < 4.0 V |                             | 2/f <sub>MCK</sub><br>+44 |                             | 2/f <sub>MCK</sub><br>+110 |                             | 2/f <sub>MCK</sub><br>+110 | ns   |
|                                                                                       |                                        |                                  | 2.4 V ≤ EV <sub>DD</sub> < 2.7 V |                             | 2/f <sub>MCK</sub><br>+75 |                             | 2/f <sub>MCK</sub><br>+110 |                             | 2/f <sub>MCK</sub><br>+110 | ns   |
|                                                                                       |                                        |                                  | 1.8 V ≤ EV <sub>DD</sub> < 2.4 V |                             |                           |                             | 2/f <sub>MCK</sub><br>+110 |                             | 2/f <sub>MCK</sub><br>+110 | ns   |
|                                                                                       |                                        |                                  | 1.6 V ≤ EV <sub>DD</sub> < 1.8 V |                             |                           |                             |                            | 2/f <sub>MCK</sub> +<br>220 |                            | ns   |

(Note, Caution and Remark are listed on the next page.)

- <R> **Notes**
1. HS is condition of HS (high-speed main) mode.
  2. LS is condition of LS (low-speed main) mode.
  3. LV is condition of LV (low-voltage main) mode.
  4. Transfer rate in the SNOOZE mode : MAX. 1 Mbps
  5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to  $\overline{\text{SCKp}}\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
  6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from  $\overline{\text{SCKp}}\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
  7. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from  $\overline{\text{SCKp}}\uparrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
  8. C is the load capacitance of the SOp output lines.

<R> **Caution** Select the normal input buffer for the SIp pin and  $\overline{\text{SCKp}}$  pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01), m: Unit number (m = 0),  
n: Channel number (n = 0, 1), g: PIM number (g = 1)
  2.  $f_{\text{MCK}}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

**CSI mode connection diagram (during communication at same potential)**
**CSI mode serial transfer timing (during communication at same potential)**  
 (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

**CSI mode serial transfer timing (during communication at same potential)**  
 (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)


- Remarks**
1. p: CSI number (p = 00, 01)
  2. m: Unit number, n: Channel number (mn = 00, 01)



(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (dedicated baud rate generator output) (1/2)  
 (T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS</sub> = 0 V)

| <R> | Parameter     | Symbol | Conditions |                                                                     | HS <sup>Note 1</sup> |                                          | LS <sup>Note 2</sup> |                                              | LV <sup>Note 3</sup> |                                              | Unit |
|-----|---------------|--------|------------|---------------------------------------------------------------------|----------------------|------------------------------------------|----------------------|----------------------------------------------|----------------------|----------------------------------------------|------|
|     |               |        |            |                                                                     | MIN.                 | MAX.                                     | MIN.                 | MAX.                                         | MIN.                 | MAX.                                         |      |
|     | Transfer rate |        | reception  | 4.0 V ≤ EV <sub>DD</sub> ≤ 5.5 V,<br>2.7 V ≤ V <sub>b</sub> ≤ 4.0 V |                      | f <sub>MCK</sub> /6<br><sup>Note 4</sup> |                      | f <sub>MCK</sub> /6<br><sup>Notes 4, 5</sup> |                      | f <sub>MCK</sub> /6<br><sup>Notes 4, 5</sup> | bps  |
|     |               |        |            |                                                                     |                      | 4.0                                      |                      | 1.3                                          |                      | 0.7                                          | Mbps |
|     |               |        |            | 2.7 V ≤ EV <sub>DD</sub> < 4.0 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V |                      | f <sub>MCK</sub> /6<br><sup>Note 4</sup> |                      | f <sub>MCK</sub> /6<br><sup>Notes 4, 5</sup> |                      | f <sub>MCK</sub> /6<br><sup>Notes 4, 5</sup> | bps  |
|     |               |        |            |                                                                     |                      | 4.0                                      |                      | 1.3                                          |                      | 0.7                                          | Mbps |
|     |               |        |            | 2.4 V ≤ EV <sub>DD</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V |                      | f <sub>MCK</sub> /6<br><sup>Note 4</sup> |                      | f <sub>MCK</sub> /6<br><sup>Notes 4, 5</sup> |                      | f <sub>MCK</sub> /6<br><sup>Notes 4, 5</sup> | bps  |
|     |               |        |            |                                                                     |                      | 4.0                                      |                      | 1.3                                          |                      | 0.7                                          | Mbps |
|     |               |        |            | 1.8 V ≤ EV <sub>DD</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V |                      |                                          |                      | f <sub>MCK</sub> /6<br><sup>Notes 4, 5</sup> |                      | f <sub>MCK</sub> /6<br><sup>Notes 4, 5</sup> | bps  |
|     |               |        |            |                                                                     |                      |                                          |                      | 1.3                                          |                      | 0.7                                          | Mbps |
|     |               |        |            |                                                                     |                      |                                          |                      |                                              |                      |                                              |      |
|     |               |        |            |                                                                     |                      |                                          |                      |                                              |                      |                                              |      |
|     |               |        |            |                                                                     |                      |                                          |                      |                                              |                      |                                              |      |
|     |               |        |            |                                                                     |                      |                                          |                      |                                              |                      |                                              |      |

<R> **Notes 1.** HS is condition of HS (high-speed main) mode.

<R> **2.** LS is condition of LS (low-speed main) mode.

<R> **3.** LV is condition of LV (low-voltage main) mode.

**4.** Transfer rate in the SNOOZE mode : MAX. 9600 bps, MIN. 4800 bps

**5.** Use it with EV<sub>DD</sub> ≥ V<sub>b</sub>.

<R> **6.** f<sub>CLK</sub> in each operating mode is as below.

HS (high-speed main) mode: f<sub>CLK</sub> = 24 MHz

LS (low-speed main) mode: f<sub>CLK</sub> = 8 MHz

LV (low-voltage main) mode: f<sub>CLK</sub> = 4 MHz

**Caution** Select the TTL input buffer for the Rx<sub>Dq</sub> pin and the N-ch open drain output (V<sub>DD</sub> tolerance (32-pin to 52-pin products)/EV<sub>DD</sub> tolerance (64-pin products)) mode for the Tx<sub>Dq</sub> pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remarks 1.** V<sub>b</sub>[V]: Communication line voltage

**2.** q: UART number (q = 0), g: PIM and POM number (g = 1)

**3.** f<sub>MCK</sub>: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

**(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (dedicated baud rate generator output) (2/2)**  
**(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS</sub> = 0 V)**

| <R> | Parameter     | Symbol | Conditions   |                                                                     | HS <sup>Note 1</sup> |                            | LS <sup>Note 2</sup> |                            | LV <sup>Note 3</sup> |                            | Unit |
|-----|---------------|--------|--------------|---------------------------------------------------------------------|----------------------|----------------------------|----------------------|----------------------------|----------------------|----------------------------|------|
|     |               |        |              |                                                                     | MIN.                 | MAX.                       | MIN.                 | MAX.                       | MIN.                 | MAX.                       |      |
|     | Transfer rate |        | transmission | 4.0 V ≤ EV <sub>DD</sub> ≤ 5.5 V,<br>2.7 V ≤ V <sub>b</sub> ≤ 4.0 V |                      | Notes<br>4, 5              |                      | Notes<br>4, 5              |                      | Notes<br>4, 5              | bps  |
|     |               |        |              |                                                                     |                      | 2.8<br><sup>Note 6</sup>   |                      | 2.8<br><sup>Note 6</sup>   |                      | 2.8<br><sup>Note 6</sup>   | Mbps |
|     |               |        |              | 2.7 V ≤ EV <sub>DD</sub> < 4.0 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V |                      | Notes<br>5, 7              |                      | Notes<br>5, 7              |                      | Notes<br>5, 7              | bps  |
|     |               |        |              |                                                                     |                      | 1.2<br><sup>Note 8</sup>   |                      | 1.2<br><sup>Note 8</sup>   |                      | 1.2<br><sup>Note 8</sup>   | Mbps |
|     |               |        |              | 2.4 V ≤ EV <sub>DD</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V |                      | Notes<br>5, 9,<br>10       |                      | Notes<br>5, 9,<br>10       |                      | Notes<br>5, 9,<br>10       | bps  |
|     |               |        |              |                                                                     |                      | 0.43<br><sup>Note 11</sup> |                      | 0.43<br><sup>Note 11</sup> |                      | 0.43<br><sup>Note 11</sup> | Mbps |
|     |               |        |              | 1.8 V ≤ EV <sub>DD</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V |                      |                            |                      | Notes<br>5, 9,<br>10       |                      | Notes<br>5, 9,<br>10       | bps  |
|     |               |        |              |                                                                     |                      |                            |                      | 0.43<br><sup>Note 11</sup> |                      | 0.43<br><sup>Note 11</sup> | Mbps |
|     |               |        |              |                                                                     |                      |                            |                      |                            |                      |                            |      |
|     |               |        |              |                                                                     |                      |                            |                      |                            |                      |                            |      |
|     |               |        |              |                                                                     |                      |                            |                      |                            |                      |                            |      |
|     |               |        |              |                                                                     |                      |                            |                      |                            |                      |                            |      |

<R> **Notes 1.** HS is condition of HS (high-speed main) mode.

<R> **2.** LS is condition of LS (low-speed main) mode.

<R> **3.** LV is condition of LV (low-voltage main) mode.

**4.** The smaller maximum transfer rate derived by using f<sub>MCK</sub>/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV<sub>DD</sub> ≤ 5.5 V and 2.7 V ≤ V<sub>b</sub> ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

**5.** Transfer rate in the SNOOZE mode : MAX. 9600 bps, MIN. 4800 bps

**6.** This value as an example is calculated when the conditions described in the “Conditions” column are met.  
Refer to Note 4 above to calculate the maximum transfer rate under conditions of the customer.

**Notes 7.** The smaller maximum transfer rate derived by using  $f_{MCK}/6$  or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when  $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$  and  $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

8. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 7 above to calculate the maximum transfer rate under conditions of the customer.

9. Use it with  $EV_{DD} \geq V_b$ .

10. The smaller maximum transfer rate derived by using  $f_{MCK}/6$  or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when  $1.8\text{ V} \leq EV_{DD} < 3.3\text{ V}$  and  $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

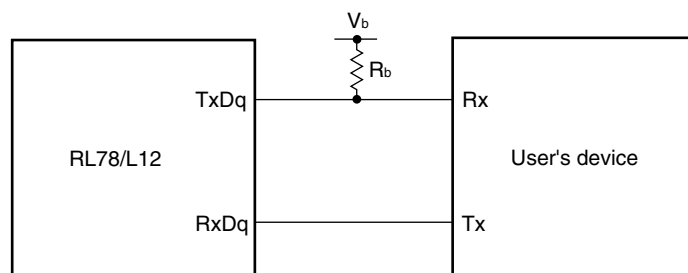
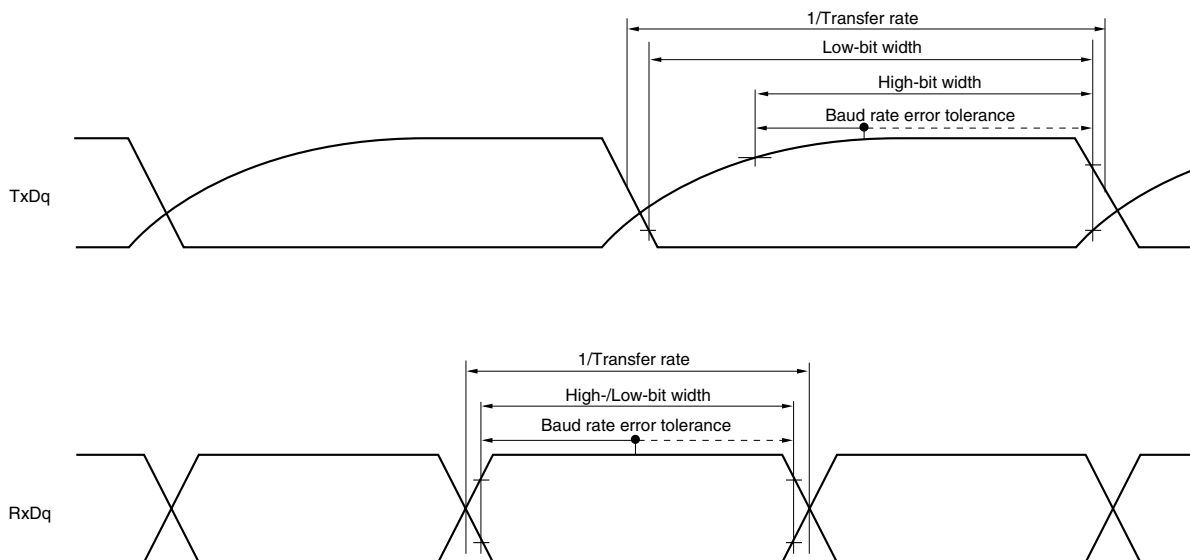
\* This value is the theoretical value of the relative difference between the transmission and reception sides.

11. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 10 above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output ( $V_{DD}$  tolerance (32-pin to 52-pin products)/ $EV_{DD}$  tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remarks 1.**  $R_b[\Omega]$ : Communication line (TxDq) pull-up resistance,  
 $C_b[F]$ : Communication line (TxDq) load capacitance,  $V_b[V]$ : Communication line voltage  
 2. q: UART number (q = 0, 1), g: PIM and POM number (g = 1)  
 3.  $f_{MCK}$ : Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
 m: Unit number, n: Channel number (mn = 00, 01))

<R>

**UART mode connection diagram (during communication at different potential)****UART mode bit width (during communication at different potential) (reference)**

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output ( $V_{DD}$  tolerance (32-pin to 52-pin products)/ $EV_{DD}$  tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remarks**

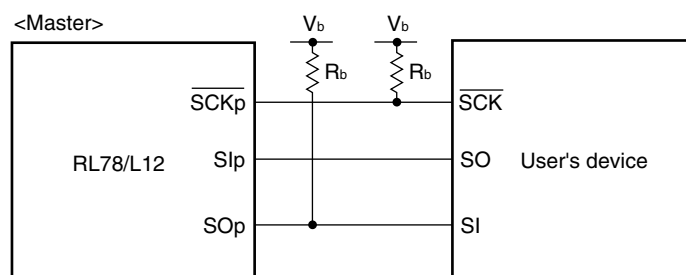
1.  $R_b[\Omega]$ : Communication line (TxDq) pull-up resistance,  $V_b[V]$ : Communication line voltage
2. q: UART number (q = 0), g: PIM and POM number (g = 1)

(5) Communication at different potential (2.5 V, 3 V) ( $f_{MCK}/2$ ) (CSI mode) (master mode,  $\overline{SCKp}$ ... internal clock output, corresponding CSI00 only)

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $2.7\text{ V} \leq EV_{DD} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS} = 0\text{ V}$ )

| <R> | Parameter                                                                      | Symbol     | Conditions                                                                                                                                       | HS <sup>Note 1</sup>     |      | LS <sup>Note 2</sup>      |      | LV <sup>Note 3</sup>      |      | Unit |
|-----|--------------------------------------------------------------------------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|------|---------------------------|------|---------------------------|------|------|
|     |                                                                                |            |                                                                                                                                                  | MIN.                     | MAX. | MIN.                      | MAX. | MIN.                      | MAX. |      |
|     | $\overline{SCKp}$ cycle time                                                   | $t_{KCY1}$ | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ ,<br>$C_b = 20\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ | 200<br><sup>Note 4</sup> |      | 1150<br><sup>Note 4</sup> |      | 1150<br><sup>Note 4</sup> |      | ns   |
|     |                                                                                |            | $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 20\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    | 300<br><sup>Note 4</sup> |      | 1150<br><sup>Note 4</sup> |      | 1150<br><sup>Note 4</sup> |      | ns   |
|     | $\overline{SCKp}$ high-level width                                             | $t_{KH1}$  | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ ,<br>$C_b = 20\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ | $t_{KCY1}/2$<br>– 50     |      | $t_{KCY1}/2$<br>– 50      |      | $t_{KCY1}/2$<br>– 50      |      | ns   |
|     |                                                                                |            | $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 20\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    | $t_{KCY1}/2$<br>– 120    |      | $t_{KCY1}/2$<br>– 120     |      | $t_{KCY1}/2$<br>– 120     |      | ns   |
|     | $\overline{SCKp}$ low-level width                                              | $t_{KL1}$  | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ ,<br>$C_b = 20\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ | $t_{KCY1}/2$<br>– 7      |      | $t_{KCY1}/2$<br>– 50      |      | $t_{KCY1}/2$<br>– 50      |      | ns   |
|     |                                                                                |            | $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 20\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    | $t_{KCY1}/2$<br>– 10     |      | $t_{KCY1}/2$<br>– 50      |      | $t_{KCY1}/2$<br>– 50      |      | ns   |
|     | Slp setup time<br>(to $\overline{SCKp}\uparrow$ ) <sup>Note 5</sup>            | $t_{SIK1}$ | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ ,<br>$C_b = 20\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ | 58                       |      | 479                       |      | 479                       |      | ns   |
|     |                                                                                |            | $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 20\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    | 121                      |      | 479                       |      | 479                       |      | ns   |
|     | Slp hold time<br>(from $\overline{SCKp}\uparrow$ ) <sup>Note 5</sup>           | $t_{KSI1}$ | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ ,<br>$C_b = 20\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ | 10                       |      | 10                        |      | 10                        |      | ns   |
|     |                                                                                |            | $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 20\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    | 10                       |      | 10                        |      | 10                        |      | ns   |
|     | Delay time from $\overline{SCKp}\downarrow$ to<br>SOp output <sup>Note 5</sup> | $t_{KSO1}$ | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ ,<br>$C_b = 20\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ |                          | 60   |                           | 60   |                           | 60   | ns   |
|     |                                                                                |            | $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 20\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    |                          | 130  |                           | 130  |                           | 130  | ns   |
|     | Slp setup time<br>(to $\overline{SCKp}\downarrow$ ) <sup>Note 6</sup>          | $t_{SIK1}$ | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ ,<br>$C_b = 20\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ | 23                       |      | 110                       |      | 110                       |      | ns   |
|     |                                                                                |            | $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 20\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    | 33                       |      | 110                       |      | 110                       |      | ns   |
|     | Slp hold time<br>(from $\overline{SCKp}\downarrow$ ) <sup>Note 6</sup>         | $t_{KSI1}$ | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ ,<br>$C_b = 20\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ | 10                       |      | 10                        |      | 10                        |      | ns   |
|     |                                                                                |            | $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 20\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    | 10                       |      | 10                        |      | 10                        |      | ns   |
|     | Delay time from $\overline{SCKp}\uparrow$ to<br>SOp output <sup>Note 6</sup>   | $t_{KSO1}$ | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ ,<br>$C_b = 20\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ |                          | 10   |                           | 10   |                           | 10   | ns   |
|     |                                                                                |            | $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 20\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    |                          | 10   |                           | 10   |                           | 10   | ns   |

(Note, Caution and Remark are listed on the next page.)

**CSI mode connection diagram (during communication at different potential)**

<R> **Notes** 1. HS is condition of HS (high-speed main) mode.

<R> 2. LS is condition of LS (low-speed main) mode.

<R> 3. LV is condition of LV (low-voltage main) mode.

4. The value must also be  $2/f_{MCK}$  or more.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

6. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output ( $V_{DD}$  tolerance (32-pin to 52-pin products)/ $EV_{DD}$  tolerance (64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remarks** 1.  $R_b[\Omega]$ : Communication line ( $\overline{SCKp}$ , SOp) pull-up resistance,  $C_b[F]$ : Communication line ( $\overline{SCKp}$ , SOp) load capacitance,  $V_b[V]$ : Communication line voltage

2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),  
g: PIM and POM number (g = 1)

3.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,  
n: Channel number (mn = 00, 01))

<R>

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) ( $f_{MCK}/4$ ) (CSI mode) (master mode,  $\overline{SCKp}$ ... internal clock output) (1/2)**

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq EV_{DD} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS} = 0\text{ V}$ )

| <R> | Parameter                          | Symbol     | Conditions                                                                                                                                       | HS <sup>Note 1</sup>      |      | LS <sup>Note 2</sup>      |      | LV <sup>Note 3</sup>      |      | Unit |
|-----|------------------------------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|------|---------------------------|------|---------------------------|------|------|
|     |                                    |            |                                                                                                                                                  | MIN.                      | MAX. | MIN.                      | MAX. | MIN.                      | MAX. |      |
|     | $\overline{SCKp}$ cycle time       | $t_{KCY1}$ | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ | 300<br><sup>Note 4</sup>  |      | 1150<br><sup>Note 4</sup> |      | 1150<br><sup>Note 4</sup> |      | ns   |
|     |                                    |            | $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    | 500<br><sup>Note 4</sup>  |      | 1150<br><sup>Note 4</sup> |      | 1150<br><sup>Note 4</sup> |      | ns   |
|     |                                    |            | $2.4\text{ V} \leq EV_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    | 1150<br><sup>Note 4</sup> |      | 1150<br><sup>Note 4</sup> |      | 1150<br><sup>Note 4</sup> |      | ns   |
|     |                                    |            | $1.8\text{ V} \leq EV_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    |                           |      | 1150<br><sup>Note 4</sup> |      | 1150<br><sup>Note 4</sup> |      | ns   |
|     | $\overline{SCKp}$ high-level width | $t_{KH1}$  | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ | $t_{KCY1}/2$<br>– 75      |      | $t_{KCY1}/2$<br>– 75      |      | $t_{KCY1}/2$<br>– 75      |      | ns   |
|     |                                    |            | $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    | $t_{KCY1}/2$<br>– 170     |      | $t_{KCY1}/2$<br>– 170     |      | $t_{KCY1}/2$<br>– 170     |      | ns   |
|     |                                    |            | $2.4\text{ V} \leq EV_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    | $t_{KCY1}/2$<br>– 458     |      | $t_{KCY1}/2$<br>– 458     |      | $t_{KCY1}/2$<br>– 458     |      | ns   |
|     |                                    |            | $1.8\text{ V} \leq EV_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    |                           |      | $t_{KCY1}/2$<br>– 458     |      | $t_{KCY1}/2$<br>– 458     |      | ns   |
|     | $\overline{SCKp}$ low-level width  | $t_{KL1}$  | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ | $t_{KCY1}/2$<br>– 12      |      | $t_{KCY1}/2$<br>– 50      |      | $t_{KCY1}/2$<br>– 50      |      | ns   |
|     |                                    |            | $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    | $t_{KCY1}/2$<br>– 18      |      | $t_{KCY1}/2$<br>– 50      |      | $t_{KCY1}/2$<br>– 50      |      | ns   |
|     |                                    |            | $2.4\text{ V} \leq EV_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    | $t_{KCY1}/2$<br>– 50      |      | $t_{KCY1}/2$<br>– 50      |      | $t_{KCY1}/2$<br>– 50      |      | ns   |
|     |                                    |            | $1.8\text{ V} \leq EV_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    |                           |      | $t_{KCY1}/2$<br>– 50      |      | $t_{KCY1}/2$<br>– 50      |      | ns   |

<R> **Notes 1.** HS is condition of HS (high-speed main) mode.

<R> **2.** LS is condition of LS (low-speed main) mode.

<R> **3.** LV is condition of LV (low-voltage main) mode.

**4.** The value must also be  $4/f_{MCK}$  or more.

**Cautions 1.** Select the TTL input buffer for the SIp pin and the N-ch open drain output ( $V_{DD}$  tolerance (32-pin to 52-pin products)/ $EV_{DD}$  tolerance (64-pin products)) mode for the SOp pin and  $\overline{SCKp}$  pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**2.** Use it with  $EV_{DD} \geq V_b$ .

**Remarks 1.**  $R_b[\Omega]$ : Communication line ( $\overline{SCKp}$ , SOp) pull-up resistance,  $C_b[F]$ : Communication line ( $\overline{SCKp}$ , SOp) load capacitance,  $V_b[V]$ : Communication line voltage

**2.** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)

<R>

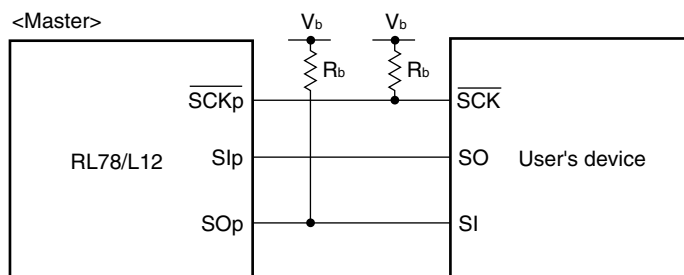
**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) ( $f_{MCK}/4$ ) (CSI mode) (master mode,  $\overline{SCKp}$ ... internal clock output) (2/2)**

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq EV_{DD} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS} = 0\text{ V}$ )

| <R> | Parameter                                                                      | Symbol     | Conditions                                                                                                                                       | HS <sup>Note 1</sup> |      | LS <sup>Note 2</sup> |      | LV <sup>Note 3</sup> |      | Unit |
|-----|--------------------------------------------------------------------------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------|----------------------|------|----------------------|------|------|
|     |                                                                                |            |                                                                                                                                                  | MIN.                 | MAX. | MIN.                 | MAX. | MIN.                 | MAX. |      |
|     | Slp setup time<br>(to $\overline{SCKp}\uparrow$ ) <sup>Note 4</sup>            | $t_{SIK1}$ | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ | 81                   |      | 479                  |      | 479                  |      | ns   |
|     |                                                                                |            | $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    | 177                  |      | 479                  |      | 479                  |      | ns   |
|     |                                                                                |            | $2.4\text{ V} \leq EV_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    | 479                  |      | 479                  |      | 479                  |      | ns   |
|     |                                                                                |            | $1.8\text{ V} \leq EV_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    |                      |      | 479                  |      | 479                  |      | ns   |
|     | Slp hold time<br>(from $\overline{SCKp}\uparrow$ ) <sup>Note 4</sup>           | $t_{KSI1}$ | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ | 19                   |      | 19                   |      | 19                   |      | ns   |
|     |                                                                                |            | $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    | 19                   |      | 19                   |      | 19                   |      | ns   |
|     |                                                                                |            | $2.4\text{ V} \leq EV_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    | 19                   |      | 19                   |      | 19                   |      | ns   |
|     |                                                                                |            | $1.8\text{ V} \leq EV_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    |                      |      | 19                   |      | 19                   |      | ns   |
|     | Delay time from $\overline{SCKp}\downarrow$ to<br>SOp output <sup>Note 4</sup> | $t_{KSO1}$ | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ |                      | 100  |                      | 100  |                      | 100  | ns   |
|     |                                                                                |            | $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    |                      | 195  |                      | 195  |                      | 195  | ns   |
|     |                                                                                |            | $2.4\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    |                      | 483  |                      | 483  |                      | 483  | ns   |
|     |                                                                                |            | $1.8\text{ V} \leq EV_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    |                      |      |                      | 483  |                      | 483  | ns   |
|     | Slp setup time<br>(to $\overline{SCKp}\downarrow$ ) <sup>Note 5</sup>          | $t_{SIK1}$ | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ | 44                   |      | 110                  |      | 110                  |      | ns   |
|     |                                                                                |            | $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    | 44                   |      | 110                  |      | 110                  |      | ns   |
|     |                                                                                |            | $2.4\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    | 110                  |      | 110                  |      | 110                  |      | ns   |
|     |                                                                                |            | $1.8\text{ V} \leq EV_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    |                      |      | 110                  |      | 110                  |      | ns   |
|     | Slp hold time<br>(from $\overline{SCKp}\downarrow$ ) <sup>Note 5</sup>         | $t_{KSI1}$ | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ | 19                   |      | 19                   |      | 19                   |      | ns   |
|     |                                                                                |            | $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    | 19                   |      | 19                   |      | 19                   |      | ns   |
|     |                                                                                |            | $2.4\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    | 19                   |      | 19                   |      | 19                   |      | ns   |
|     |                                                                                |            | $1.8\text{ V} \leq EV_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    |                      |      | 19                   |      | 19                   |      | ns   |
|     | Delay time from $\overline{SCKp}\uparrow$ to<br>SOp output <sup>Note 5</sup>   | $t_{KSO1}$ | $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$ |                      | 25   |                      | 25   |                      | 25   | ns   |
|     |                                                                                |            | $2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$    |                      | 25   |                      | 25   |                      | 25   | ns   |
|     |                                                                                |            | $2.4\text{ V} \leq EV_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    |                      | 25   |                      | 25   |                      | 25   | ns   |
|     |                                                                                |            | $1.8\text{ V} \leq EV_{DD} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ,<br>$C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$    |                      |      |                      | 25   |                      | 25   | ns   |

(Note, Caution and Remark are listed on the next page.)



**CSI mode connection diagram (during communication at different potential)**

<R> **Notes** 1. HS is condition of HS (high-speed main) mode.

<R> 2. LS is condition of LS (low-speed main) mode.

<R> 3. LV is condition of LV (low-voltage main) mode.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

5. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Cautions** 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output ( $V_{DD}$  tolerance (32-pin to 52-pin products)/ $EV_{DD}$  tolerance (64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

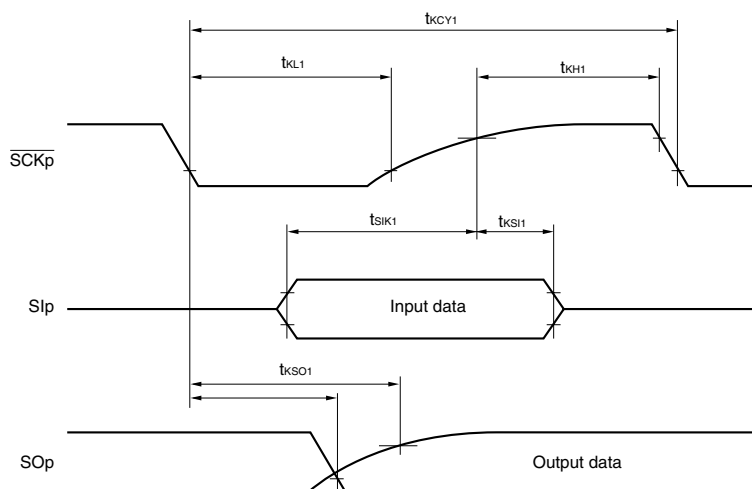
2. Use it with  $EV_{DD} \geq V_b$ .

**Remarks** 1.  $R_b[\Omega]$ : Communication line ( $\overline{SCKp}$ , SOp) pull-up resistance,  $C_b[F]$ : Communication line ( $\overline{SCKp}$ , SOp) load capacitance,  $V_b[V]$ : Communication line voltage

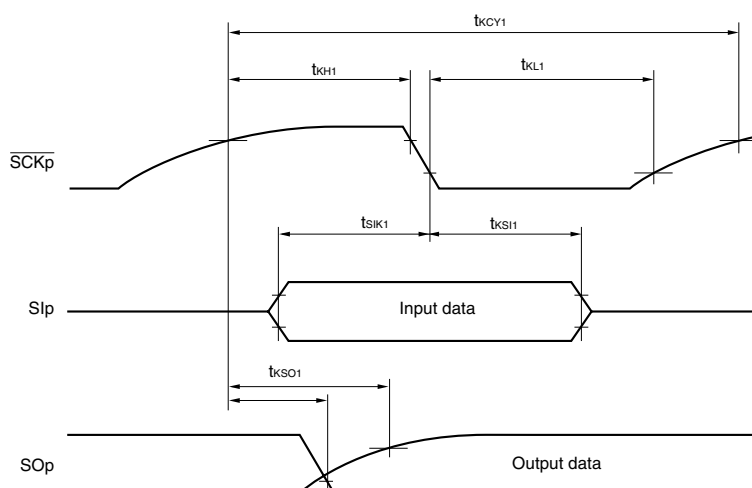
2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),

g: PIM and POM number (g = 1)

**CSI mode serial transfer timing (master mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (master mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



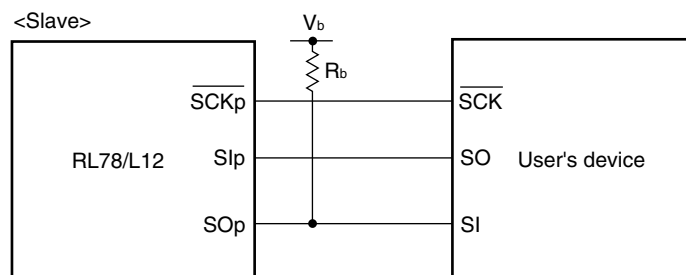
**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output ( $V_{DD}$  tolerance (32-pin to 52-pin products)/ $EV_{DD}$  tolerance (64-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remark** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),  
 g: PIM and POM number (g = 1)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode,  $\overline{\text{SCKp}}$ ... external clock input)  
 (T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS</sub> = 0 V)

| <R> | Parameter                                                                                 | Symbol                                 | Conditions                                                                                                           | HS <sup>Note 1</sup>               |                             | LS <sup>Note 2</sup>         |                             | LV <sup>Note 3</sup>         |                             | Unit |
|-----|-------------------------------------------------------------------------------------------|----------------------------------------|----------------------------------------------------------------------------------------------------------------------|------------------------------------|-----------------------------|------------------------------|-----------------------------|------------------------------|-----------------------------|------|
|     |                                                                                           |                                        |                                                                                                                      | MIN.                               | MAX.                        | MIN.                         | MAX.                        | MIN.                         | MAX.                        |      |
|     | $\overline{\text{SCKp}}$ cycle time <sup>Note 4</sup>                                     | t <sub>KCY2</sub>                      | 4.0 V ≤ EV <sub>DD</sub> ≤ 5.5 V,<br>2.7 V ≤ V <sub>b</sub> ≤ 4.0 V                                                  | 20 MHz < f <sub>MCK</sub> ≤ 24 MHz | 12/f <sub>MCK</sub>         |                              |                             |                              |                             | ns   |
|     |                                                                                           |                                        |                                                                                                                      | 8 MHz < f <sub>MCK</sub> ≤ 20 MHz  | 10/f <sub>MCK</sub>         |                              |                             |                              |                             | ns   |
|     |                                                                                           |                                        |                                                                                                                      | 4 MHz < f <sub>MCK</sub> ≤ 8 MHz   | 8/f <sub>MCK</sub>          |                              | 16/f <sub>MCK</sub>         |                              |                             | ns   |
|     |                                                                                           |                                        |                                                                                                                      | f <sub>MCK</sub> ≤ 4 MHz           | 6/f <sub>MCK</sub>          |                              | 10/f <sub>MCK</sub>         |                              | 10/f <sub>MCK</sub>         | ns   |
|     |                                                                                           |                                        | 2.7 V ≤ EV <sub>DD</sub> < 4.0 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V                                                  | 20 MHz < f <sub>MCK</sub> ≤ 24 MHz | 16/f <sub>MCK</sub>         |                              |                             |                              |                             | ns   |
|     |                                                                                           |                                        |                                                                                                                      | 16 MHz < f <sub>MCK</sub> ≤ 20 MHz | 14/f <sub>MCK</sub>         |                              |                             |                              |                             | ns   |
|     |                                                                                           |                                        |                                                                                                                      | 8 MHz < f <sub>MCK</sub> ≤ 16 MHz  | 12/f <sub>MCK</sub>         |                              |                             |                              |                             | ns   |
|     |                                                                                           |                                        |                                                                                                                      | 4 MHz < f <sub>MCK</sub> ≤ 8 MHz   | 8/f <sub>MCK</sub>          |                              | 16/f <sub>MCK</sub>         |                              |                             | ns   |
|     |                                                                                           |                                        |                                                                                                                      | f <sub>MCK</sub> ≤ 4 MHz           | 6/f <sub>MCK</sub>          |                              | 10/f <sub>MCK</sub>         |                              | 10/f <sub>MCK</sub>         | ns   |
|     |                                                                                           |                                        | 2.4 V ≤ EV <sub>DD</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 5</sup>                                | 20 MHz < f <sub>MCK</sub> ≤ 24 MHz | 36/f <sub>MCK</sub>         |                              |                             |                              |                             | ns   |
|     |                                                                                           |                                        |                                                                                                                      | 16 MHz < f <sub>MCK</sub> ≤ 20 MHz | 32/f <sub>MCK</sub>         |                              |                             |                              |                             | ns   |
|     |                                                                                           |                                        |                                                                                                                      | 8 MHz < f <sub>MCK</sub> ≤ 16 MHz  | 26/f <sub>MCK</sub>         |                              |                             |                              |                             | ns   |
|     |                                                                                           |                                        |                                                                                                                      | 4 MHz < f <sub>MCK</sub> ≤ 8 MHz   | 16/f <sub>MCK</sub>         |                              | 16/f <sub>MCK</sub>         |                              |                             | ns   |
|     |                                                                                           |                                        |                                                                                                                      | f <sub>MCK</sub> ≤ 4 MHz           | 10/f <sub>MCK</sub>         |                              | 10/f <sub>MCK</sub>         |                              | 10/f <sub>MCK</sub>         | ns   |
|     |                                                                                           |                                        | 1.8 V ≤ EV <sub>DD</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 5</sup>                                | 4 MHz < f <sub>MCK</sub> ≤ 8 MHz   |                             |                              | 16/f <sub>MCK</sub>         |                              |                             | ns   |
|     |                                                                                           |                                        |                                                                                                                      | f <sub>MCK</sub> ≤ 4 MHz           |                             |                              | 10/f <sub>MCK</sub>         |                              | 10/f <sub>MCK</sub>         | ns   |
|     | $\overline{\text{SCKp}}$ high-/low-level width <sup>Note 5</sup>                          | t <sub>KH2</sub> ,<br>t <sub>KL2</sub> | 4.0 V ≤ EV <sub>DD</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V                                                     | t <sub>KCY2</sub> /2<br>- 12       |                             | t <sub>KCY2</sub> /2<br>- 50 |                             | t <sub>KCY2</sub> /2<br>- 50 |                             | ns   |
|     |                                                                                           |                                        | 2.7 V ≤ EV <sub>DD</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V                                                     | t <sub>KCY2</sub> /2<br>- 18       |                             | t <sub>KCY2</sub> /2<br>- 50 |                             | t <sub>KCY2</sub> /2<br>- 50 |                             | ns   |
|     |                                                                                           |                                        | 2.4 V ≤ EV <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V                                                     | t <sub>KCY2</sub> /2<br>- 50       |                             | t <sub>KCY2</sub> /2<br>- 50 |                             | t <sub>KCY2</sub> /2<br>- 50 |                             | ns   |
|     |                                                                                           |                                        | 1.8 V ≤ EV <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V                                                     |                                    |                             | t <sub>KCY2</sub> /2<br>- 50 |                             | t <sub>KCY2</sub> /2<br>- 50 |                             | ns   |
|     | Slp setup time<br>(to $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 6</sup>                | t <sub>SIK2</sub>                      | 2.7 V ≤ EV <sub>DD</sub> < 5.5 V, 2.3 V ≤ V <sub>b</sub> ≤ 4.0 V                                                     | 1/f <sub>MCK</sub> +<br>20         |                             | 1/f <sub>MCK</sub> +<br>30   |                             | 1/f <sub>MCK</sub> +<br>30   |                             | ns   |
|     |                                                                                           |                                        | 2.4 V ≤ EV <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V                                                     | 1/f <sub>MCK</sub> +<br>30         |                             | 1/f <sub>MCK</sub> +<br>30   |                             | 1/f <sub>MCK</sub> +<br>30   |                             | ns   |
|     |                                                                                           |                                        | 1.8 V ≤ EV <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V                                                     |                                    |                             | 1/f <sub>MCK</sub> +<br>30   |                             | 1/f <sub>MCK</sub> +<br>30   |                             | ns   |
|     | Slp hold time<br>(from $\overline{\text{SCKp}}\uparrow$ ) <sup>Note 7</sup>               | t <sub>KSI2</sub>                      | 2.7 V ≤ EV <sub>DD</sub> < 5.5 V, 2.3 V ≤ V <sub>b</sub> ≤ 4.0 V                                                     | 1/f <sub>MCK</sub> +<br>31         |                             | 1/f <sub>MCK</sub> +<br>31   |                             | 1/f <sub>MCK</sub> +<br>31   |                             | ns   |
|     |                                                                                           |                                        | 2.4 V ≤ EV <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V                                                     | 1/f <sub>MCK</sub> +<br>31         |                             | 1/f <sub>MCK</sub> +<br>31   |                             | 1/f <sub>MCK</sub> +<br>31   |                             | ns   |
|     |                                                                                           |                                        | 1.8 V ≤ EV <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V                                                     |                                    |                             | 1/f <sub>MCK</sub> +<br>31   |                             | 1/f <sub>MCK</sub> +<br>31   |                             | ns   |
|     | Delay time from $\overline{\text{SCKp}}\downarrow$<br>to SOp output <sup>Notes 5, 8</sup> | t <sub>KSO2</sub>                      | 4.0 V ≤ EV <sub>DD</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ |                                    | 2/f <sub>MCK</sub><br>+ 120 |                              | 2/f <sub>MCK</sub><br>+ 573 |                              | 2/f <sub>MCK</sub><br>+ 573 | ns   |
|     |                                                                                           |                                        | 2.7 V ≤ EV <sub>DD</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ |                                    | 2/f <sub>MCK</sub><br>+ 214 |                              | 2/f <sub>MCK</sub><br>+ 573 |                              | 2/f <sub>MCK</sub><br>+ 573 | ns   |
|     |                                                                                           |                                        | 2.4 V ≤ EV <sub>DD</sub> < 4.0 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ |                                    | 2/f <sub>MCK</sub><br>+ 573 |                              | 2/f <sub>MCK</sub><br>+ 573 |                              | 2/f <sub>MCK</sub><br>+ 573 | ns   |
|     |                                                                                           |                                        | 1.8 V ≤ EV <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V,<br>C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ |                                    |                             |                              | 2/f <sub>MCK</sub><br>+ 573 |                              | 2/f <sub>MCK</sub><br>+ 573 | ns   |

(Note, Caution and Remark are listed on the next page.)

**CSI mode connection diagram (during communication at different potential)**

<R> **Notes 1.** HS is condition of HS (high-speed main) mode.

<R> **2.** LS is condition of LS (low-speed main) mode.

<R> **3.** LV is condition of LV (low-voltage main) mode.

**4.** Transfer rate in the SNOOZE mode : MAX. 1 Mbps

**5.** Use it with  $EV_{DD} \geq V_b$ .

**6.** When  $DAP_{mn} = 0$  and  $CKP_{mn} = 0$ , or  $DAP_{mn} = 1$  and  $CKP_{mn} = 1$ . The SIp setup time becomes "to  $\overline{SCKp}\downarrow$ " when  $DAP_{mn} = 0$  and  $CKP_{mn} = 1$ , or  $DAP_{mn} = 1$  and  $CKP_{mn} = 0$ .

**7.** When  $DAP_{mn} = 0$  and  $CKP_{mn} = 0$ , or  $DAP_{mn} = 1$  and  $CKP_{mn} = 1$ . The SIp hold time becomes "from  $\overline{SCKp}\downarrow$ " when  $DAP_{mn} = 0$  and  $CKP_{mn} = 1$ , or  $DAP_{mn} = 1$  and  $CKP_{mn} = 0$ .

**8.** When  $DAP_{mn} = 0$  and  $CKP_{mn} = 0$ , or  $DAP_{mn} = 1$  and  $CKP_{mn} = 1$ . The delay time to SOp output becomes "from  $\overline{SCKp}\uparrow$ " when  $DAP_{mn} = 0$  and  $CKP_{mn} = 1$ , or  $DAP_{mn} = 1$  and  $CKP_{mn} = 0$ .

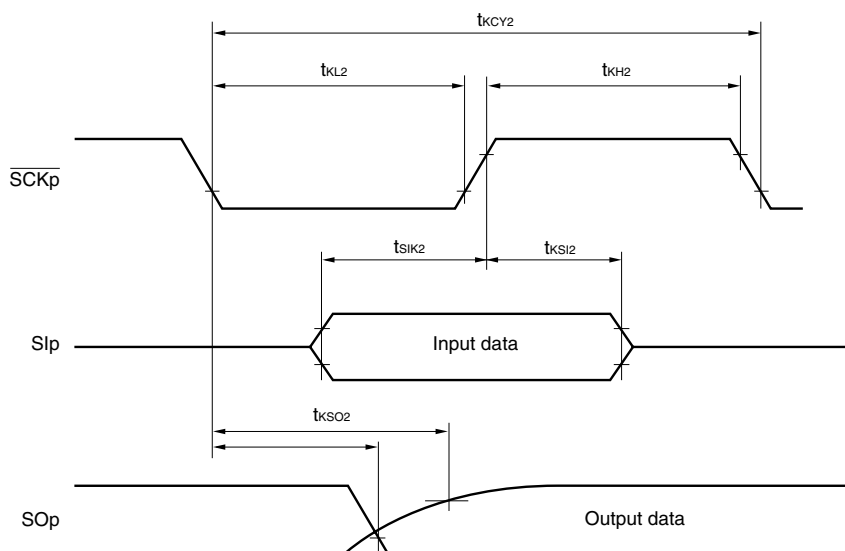
**Caution** Select the TTL input buffer for the SIp pin and  $\overline{SCKp}$  pin and the N-ch open drain output ( $V_{DD}$  tolerance (32-pin to 52-pin products)/ $EV_{DD}$  tolerance (64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remarks 1.**  $R_b[\Omega]$ : Communication line (SO<sub>p</sub>) pull-up resistance,  $C_b[F]$ : Communication line (SO<sub>p</sub>) load capacitance,  $V_b[V]$ : Communication line voltage

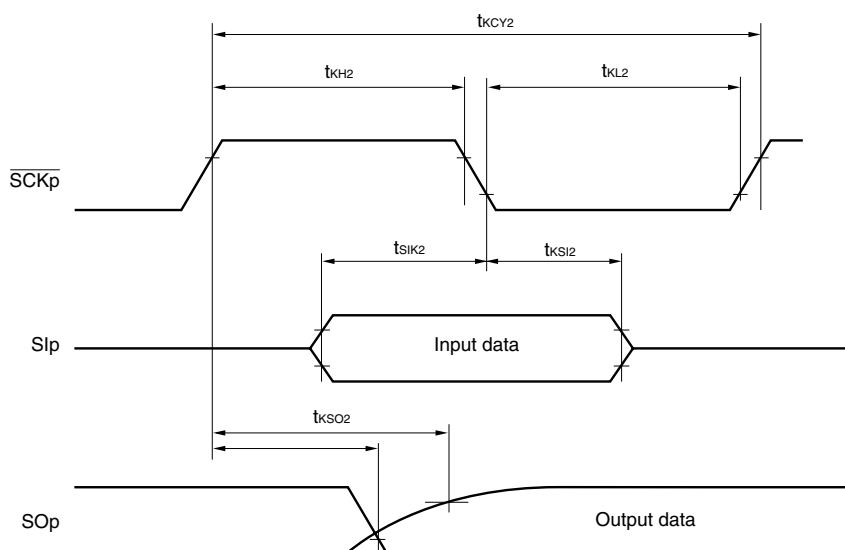
**2.** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)

**3.**  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00, 01))

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



**Caution** Select the TTL input buffer for the Slp pin and SCKp pin and the N-ch open drain output ( $V_{DD}$  tolerance (32-pin to 52-pin products)/ $EV_{DD}$  tolerance (64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remark** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),  
 g: PIM and POM number (g = 1)

## 30.5.2 Serial interface IICA

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS</sub> = 0 V)

(1/2)

| <R>                                               | Parameter           | Symbol                           | Conditions | Standard Mode <sup>Note 1</sup> |      |                      |      |                      |      | Unit |
|---------------------------------------------------|---------------------|----------------------------------|------------|---------------------------------|------|----------------------|------|----------------------|------|------|
|                                                   |                     |                                  |            | HS <sup>Note 2</sup>            |      | LS <sup>Note 3</sup> |      | LV <sup>Note 4</sup> |      |      |
|                                                   |                     |                                  |            | MIN.                            | MAX. | MIN.                 | MIN. | MAX.                 | MIN. |      |
| SCLA0 clock frequency                             | f <sub>SCL</sub>    | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 0          | 100                             | 0    | 100                  | 0    | 100                  | kHz  |      |
|                                                   |                     | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 0          | 100                             | 0    | 100                  | 0    | 100                  |      |      |
|                                                   |                     | 1.8 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                                 | 0    | 100                  | 0    | 100                  |      |      |
|                                                   |                     | 1.6 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                                 |      |                      | 0    | 100                  |      |      |
| Setup time of restart condition <sup>Note 5</sup> | t <sub>SU:STA</sub> | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 4.7        |                                 | 4.7  |                      | 4.7  |                      | μs   |      |
|                                                   |                     | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 4.7        |                                 | 4.7  |                      | 4.7  |                      |      |      |
|                                                   |                     | 1.8 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                                 | 4.7  |                      | 4.7  |                      |      |      |
|                                                   |                     | 1.6 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                                 |      |                      | 4.7  |                      |      |      |
| Hold time                                         | t <sub>HD:STA</sub> | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 4.0        |                                 | 4.0  |                      | 4.0  |                      | μs   |      |
|                                                   |                     | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 4.0        |                                 | 4.0  |                      | 4.0  |                      |      |      |
|                                                   |                     | 1.8 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                                 | 4.0  |                      | 4.0  |                      |      |      |
|                                                   |                     | 1.6 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                                 |      |                      | 4.0  |                      |      |      |
| Hold time when SCLA0 = “L”                        | t <sub>LOW</sub>    | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 4.7        |                                 | 4.7  |                      | 4.7  |                      | μs   |      |
|                                                   |                     | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 4.7        |                                 | 4.7  |                      | 4.7  |                      |      |      |
|                                                   |                     | 1.8 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                                 | 4.7  |                      | 4.7  |                      |      |      |
|                                                   |                     | 1.6 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                                 |      |                      | 4.7  |                      |      |      |
| Hold time when SCLA0 = “H”                        | t <sub>HIGH</sub>   | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 4.0        |                                 | 4.0  |                      | 4.0  |                      | μs   |      |
|                                                   |                     | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 4.0        |                                 | 4.0  |                      | 4.0  |                      |      |      |
|                                                   |                     | 1.8 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                                 | 4.0  |                      | 4.0  |                      |      |      |
|                                                   |                     | 1.6 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                                 |      |                      | 4.0  |                      |      |      |
| Data setup time (reception)                       | t <sub>SU:DAT</sub> | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 250        |                                 | 250  |                      | 250  |                      | ns   |      |
|                                                   |                     | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 250        |                                 | 250  |                      | 250  |                      |      |      |
|                                                   |                     | 1.8 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                                 | 250  |                      | 250  |                      |      |      |
|                                                   |                     | 1.6 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                                 |      |                      | 250  |                      |      |      |
| Data hold time (transmission) <sup>Note 6</sup>   | t <sub>HD:DAT</sub> | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 0          | 3.45                            | 0    | 3.45                 | 0    | 3.45                 | μs   |      |
|                                                   |                     | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 0          | 3.45                            | 0    | 3.45                 | 0    | 3.45                 |      |      |
|                                                   |                     | 1.8 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                                 | 0    | 3.45                 | 0    | 3.45                 |      |      |
|                                                   |                     | 1.6 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                                 |      |                      | 0    | 3.45                 |      |      |
| Setup time of stop condition                      | t <sub>SU:STO</sub> | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 4.0        |                                 | 4.0  |                      | 4.0  |                      | μs   |      |
|                                                   |                     | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 4.0        |                                 | 4.0  |                      | 4.0  |                      |      |      |
|                                                   |                     | 1.8 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                                 | 4.0  |                      | 4.0  |                      |      |      |
|                                                   |                     | 1.6 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                                 |      |                      | 4.0  |                      |      |      |
| Bus-free time                                     | t <sub>BUF</sub>    | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 4.7        |                                 | 4.7  |                      | 4.7  |                      | μs   |      |
|                                                   |                     | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 4.7        |                                 | 4.7  |                      | 4.7  |                      |      |      |
|                                                   |                     | 1.8 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                                 | 4.7  |                      | 4.7  |                      |      |      |
|                                                   |                     | 1.6 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                                 |      |                      | 4.7  |                      |      |      |

(Note and Remark are listed on the next page.)

(TA = -40 to +85°C, 1.6 V ≤ EVDD = VDD ≤ 5.5 V, VSS = EVSS = 0 V)

(2/2)

| <R>                                               | Parameter           | Symbol                           | Conditions | Fast Mode <sup>Note 7</sup> |      |                      |      |                      |      | Fast Mode Plus <sup>Note 8</sup> |      | Unit |
|---------------------------------------------------|---------------------|----------------------------------|------------|-----------------------------|------|----------------------|------|----------------------|------|----------------------------------|------|------|
|                                                   |                     |                                  |            | HS <sup>Note 2</sup>        |      | LS <sup>Note 3</sup> |      | LV <sup>Note 4</sup> |      | HS <sup>Note 2</sup>             |      |      |
|                                                   |                     |                                  |            | MIN.                        | MAX. | MIN.                 | MIN. | MAX.                 | MIN. | MAX.                             | MIN. |      |
| SCLA0 clock frequency                             | f <sub>SCL</sub>    | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 0          | 400                         | 0    | 400                  | 0    | 400                  | 0    | 1000                             | kHz  |      |
|                                                   |                     | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 0          | 400                         | 0    | 400                  | 0    | 400                  |      |                                  |      |      |
|                                                   |                     | 1.8 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                             | 0    | 400                  | 0    | 400                  |      |                                  |      |      |
| Setup time of restart condition <sup>Note 5</sup> | t <sub>SU:STA</sub> | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 0.6        |                             | 0.6  |                      | 0.6  |                      | 0.26 |                                  | μs   |      |
|                                                   |                     | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 0.6        |                             | 0.6  |                      | 0.6  |                      |      |                                  |      |      |
|                                                   |                     | 1.8 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                             | 0.6  |                      | 0.6  |                      |      |                                  |      |      |
| Hold time                                         | t <sub>HD:STA</sub> | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 0.6        |                             | 0.6  |                      | 0.6  |                      | 0.26 |                                  | μs   |      |
|                                                   |                     | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 0.6        |                             | 0.6  |                      | 0.6  |                      |      |                                  |      |      |
|                                                   |                     | 1.8 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                             | 0.6  |                      | 0.6  |                      |      |                                  |      |      |
| Hold time when SCLA0 = “L”                        | t <sub>LOW</sub>    | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 1.3        |                             | 1.3  |                      | 1.3  |                      | 0.5  |                                  | μs   |      |
|                                                   |                     | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 1.3        |                             | 1.3  |                      | 1.3  |                      |      |                                  |      |      |
|                                                   |                     | 1.8 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                             | 1.3  |                      | 1.3  |                      |      |                                  |      |      |
| Hold time when SCLA0 = “H”                        | t <sub>HIGH</sub>   | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 0.6        |                             | 0.6  |                      | 0.6  |                      | 0.26 |                                  | μs   |      |
|                                                   |                     | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 0.6        |                             | 0.6  |                      | 0.6  |                      |      |                                  |      |      |
|                                                   |                     | 1.8 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                             | 0.6  |                      | 0.6  |                      |      |                                  |      |      |
| Data setup time (reception)                       | t <sub>SU:DAT</sub> | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 100        |                             | 100  |                      | 100  |                      | 50   |                                  | ns   |      |
|                                                   |                     | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 100        |                             | 100  |                      | 100  |                      |      |                                  |      |      |
|                                                   |                     | 1.8 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                             | 100  |                      | 100  |                      |      |                                  |      |      |
| Data hold time (transmission) <sup>Note 6</sup>   | t <sub>HD:DAT</sub> | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 0          | 0.9                         | 0    | 0.9                  | 0    | 0.9                  | 0    | 450                              | μs   |      |
|                                                   |                     | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 0          | 0.9                         | 0    | 0.9                  | 0    | 0.9                  |      |                                  |      |      |
|                                                   |                     | 1.8 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                             | 0    | 0.9                  | 0    | 0.9                  |      |                                  |      |      |
| Setup time of stop condition                      | t <sub>SU:STO</sub> | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 0.6        |                             | 0.6  |                      | 0.6  |                      | 0.26 |                                  | μs   |      |
|                                                   |                     | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 0.6        |                             | 0.6  |                      | 0.6  |                      |      |                                  |      |      |
|                                                   |                     | 1.8 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                             | 0.6  |                      | 0.6  |                      |      |                                  |      |      |
| Bus-free time                                     | t <sub>BUF</sub>    | 2.7 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 1.3        |                             | 1.3  |                      | 1.3  |                      | 0.5  |                                  | μs   |      |
|                                                   |                     | 2.4 V ≤ EV <sub>DD</sub> ≤ 5.5 V | 1.3        |                             | 1.3  |                      | 1.3  |                      |      |                                  |      |      |
|                                                   |                     | 1.8 V ≤ EV <sub>DD</sub> ≤ 5.5 V |            |                             | 1.3  |                      | 1.3  |                      |      |                                  |      |      |

<R> **Notes** 1. In normal mode, use it with f<sub>CLK</sub> ≥ 1 MHz, 1.6 V ≤ EVDD ≤ 5.5 V.

&lt;R&gt; 2. HS is condition of HS (high-speed main) mode.

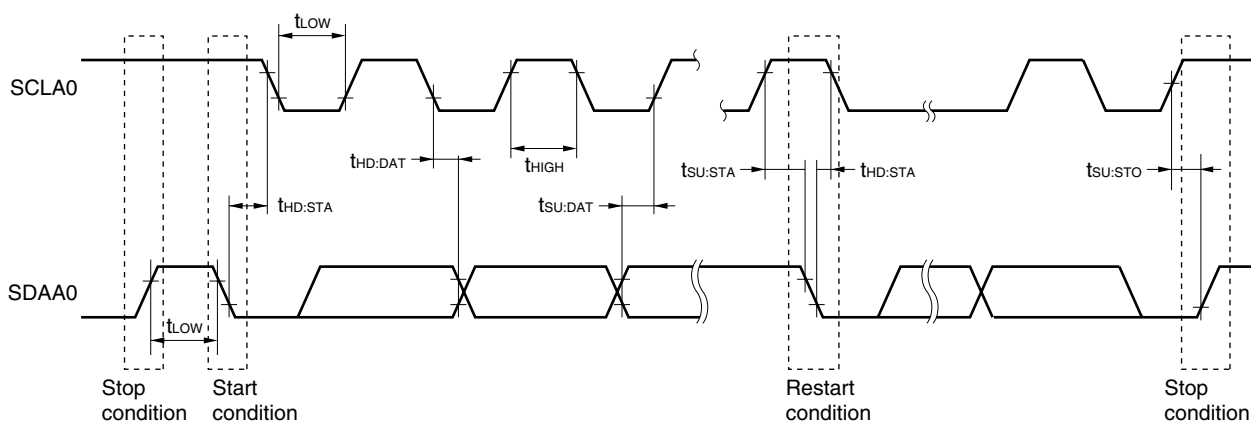
&lt;R&gt; 3. LS is condition of LS (low-speed main) mode.

&lt;R&gt; 4. LV is condition of LV (low-voltage main) mode.

5. The first clock pulse is generated after this period when the start/restart condition is detected.

6. The maximum value (MAX.) of t<sub>HD:DAT</sub> is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.<R> 7. In fast mode, use it with f<sub>CLK</sub> ≥ 3.5 MHz, 1.8 V ≤ EVDD ≤ 5.5 V.<R> 8. In fast mode plus, use it with f<sub>CLK</sub> ≥ 10 MHz, 2.7 V ≤ EVDD ≤ 5.5 V.**Remark** The maximum value of C<sub>b</sub> (communication line capacitance) and the value of R<sub>b</sub> (communication line pull-up resistor) at that time in each mode are as follows.Standard mode: C<sub>b</sub> = 400 pF, R<sub>b</sub> = 2.7 kΩFast mode: C<sub>b</sub> = 320 pF, R<sub>b</sub> = 1.1 kΩFast mode plus: C<sub>b</sub> = 120 pF, R<sub>b</sub> = 1.1 kΩ

## IICA serial transfer timing



## 30.5.3 On-chip debug (UART)

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq EV_{DD} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS} = 0\text{ V}$ )

| Parameter     | Symbol | Conditions | MIN.    | TYP. | MAX. | Unit |
|---------------|--------|------------|---------|------|------|------|
| Transfer rate |        |            | 115.2 k |      | 1 M  | bps  |



## 30.6 Analog Characteristics

### 30.6.1 A/D converter characteristics

(1) When  $AV_{REF(+)} = AV_{REFP}/ANI0$  ( $ADREFP1 = 0$ ,  $ADREFP0 = 1$ ),  $AV_{REF(-)} = AV_{REFM}/ANI1$  ( $ADREFM = 1$ ), target ANI pin : ANI16 to ANI23 (supply ANI pin to  $EV_{DD}$ )

( $T_A = -40$  to  $+85^{\circ}\text{C}$ ,  $1.6\text{ V} \leq EV_{DD} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS} = 0\text{ V}$ , Reference voltage (+) =  $AV_{REFP}$ , Reference voltage (-) =  $AV_{REFM}$ )

| Parameter                                      | Symbol      | Conditions                                                                                                                 | MIN.                                         | TYP.   | MAX.                         | Unit          |
|------------------------------------------------|-------------|----------------------------------------------------------------------------------------------------------------------------|----------------------------------------------|--------|------------------------------|---------------|
| Resolution                                     | $R_{ES}$    |                                                                                                                            | 8                                            |        | 10                           | bit           |
| Overall error <sup>Note 1</sup>                | $AINL$      | 10-bit resolution<br>$AV_{REFP} = V_{DD}$                                                                                  | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 1.2    | $\pm 5.0$                    | LSB           |
|                                                |             |                                                                                                                            | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 1.2    | $\pm 8.5$                    | LSB           |
| Conversion time                                | $t_{CONV}$  | 10-bit resolution<br>$AV_{REFP} = V_{DD}$                                                                                  | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.125  | 39                           | $\mu\text{s}$ |
|                                                |             |                                                                                                                            | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.1875 | 39                           | $\mu\text{s}$ |
|                                                |             |                                                                                                                            | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 17     | 39                           | $\mu\text{s}$ |
|                                                |             |                                                                                                                            | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 57     | 95                           | $\mu\text{s}$ |
| Zero-scale error <sup>Notes 1, 2</sup>         | $E_{ZS}$    | 10-bit resolution<br>$AV_{REFP} = V_{DD}$                                                                                  | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |        | $\pm 0.35$                   | %FSR          |
|                                                |             |                                                                                                                            | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |        | $\pm 0.60$                   | %FSR          |
| Full-scale error <sup>Notes 1, 2</sup>         | $E_{FS}$    | 10-bit resolution<br>$AV_{REFP} = V_{DD}$                                                                                  | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |        | $\pm 0.35$                   | %FSR          |
|                                                |             |                                                                                                                            | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |        | $\pm 0.60$                   | %FSR          |
| Integral linearity error <sup>Note 1</sup>     | $ILE$       | 10-bit resolution<br>$AV_{REFP} = V_{DD}$                                                                                  | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |        | $\pm 3.5$                    | LSB           |
|                                                |             |                                                                                                                            | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |        | $\pm 6.0$                    | LSB           |
| Differential linearity error <sup>Note 1</sup> | $DLE$       | 10-bit resolution<br>$AV_{REFP} = V_{DD}$                                                                                  | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |        | $\pm 2.0$                    | LSB           |
|                                                |             |                                                                                                                            | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |        | $\pm 2.5$                    | LSB           |
| Reference voltage (+)                          | $AV_{REFP}$ |                                                                                                                            | 1.6                                          |        | $V_{DD}$                     | V             |
| Analog input voltage                           | $V_{AIN}$   |                                                                                                                            | 0                                            |        | $AV_{REFP}$<br>and $EV_{DD}$ | V             |
|                                                | $V_{BGR}$   | Select internal reference voltage output,<br>$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , HS (high-speed main) mode only | 1.38                                         | 1.45   | 1.5                          | V             |

**Notes** 1. Excludes quantization error ( $\pm 1/2$  LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

(2) When  $AV_{REF(+)} = V_{DD}$  ( $ADREFP1 = 0$ ,  $ADREFP0 = 0$ ),  $AV_{REF(-)} = V_{SS}$  ( $ADREFM = 0$ ), target ANI pin : ANI0, ANI1, ANI16 to ANI23

( $T_A = -40$  to  $+85^{\circ}\text{C}$ ,  $1.6\text{ V} \leq EV_{DD} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS} = 0\text{ V}$ , Reference voltage (+) =  $V_{DD}$ , Reference voltage (-) =  $V_{SS}$ )

| Parameter                                      | Symbol     | Conditions                                                                                                                 |                                              | MIN.   | TYP. | MAX.       | Unit          |
|------------------------------------------------|------------|----------------------------------------------------------------------------------------------------------------------------|----------------------------------------------|--------|------|------------|---------------|
| Resolution                                     | $R_{ES}$   |                                                                                                                            |                                              | 8      |      | 10         | bit           |
| Overall error <sup>Note 1</sup>                | $AINL$     | 10-bit resolution                                                                                                          | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |        | 1.2  | $\pm 7.0$  | LSB           |
|                                                |            |                                                                                                                            | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |        | 1.2  | $\pm 10.5$ | LSB           |
| Conversion time                                | $t_{CONV}$ | 10-bit resolution                                                                                                          | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.125  |      | 39         | $\mu\text{s}$ |
|                                                |            |                                                                                                                            | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.1875 |      | 39         | $\mu\text{s}$ |
|                                                |            |                                                                                                                            | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 17     |      | 39         | $\mu\text{s}$ |
|                                                |            |                                                                                                                            | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 57     |      | 95         | $\mu\text{s}$ |
| Zero-scale error <sup>Notes 1, 2</sup>         | $EZS$      | 10-bit resolution                                                                                                          | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |        |      | $\pm 0.60$ | %FSR          |
|                                                |            |                                                                                                                            | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |        |      | $\pm 0.85$ | %FSR          |
| Full-scale error <sup>Notes 1, 2</sup>         | $EFS$      | 10-bit resolution                                                                                                          | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |        |      | $\pm 0.60$ | %FSR          |
|                                                |            |                                                                                                                            | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |        |      | $\pm 0.85$ | %FSR          |
| Integral linearity error <sup>Note 1</sup>     | $ILE$      | 10-bit resolution                                                                                                          | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |        |      | $\pm 4.0$  | LSB           |
|                                                |            |                                                                                                                            | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |        |      | $\pm 6.5$  | LSB           |
| Differential linearity error <sup>Note 1</sup> | $DLE$      | 10-bit resolution                                                                                                          | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |        |      | $\pm 2.0$  | LSB           |
|                                                |            |                                                                                                                            | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |        |      | $\pm 2.5$  | LSB           |
| Analog input voltage                           | $V_{AIN}$  | ANI0, ANI1                                                                                                                 |                                              | 0      |      | $V_{DD}$   | V             |
|                                                |            | ANI16 to ANI23                                                                                                             |                                              | 0      |      | $EV_{DD}$  | V             |
|                                                | $V_{BGR}$  | Select internal reference voltage output,<br>$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , HS (high-speed main) mode only |                                              | 1.38   | 1.45 | 1.5        | V             |

**Notes** 1. Excludes quantization error ( $\pm 1/2$  LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

(3) When  $AV_{REF(+)} =$  Internal reference voltage ( $ADREFP1 = 1$ ,  $ADREFP0 = 0$ ),  $AV_{REF(-)} = AV_{REFM}/ANI1$  ( $ADREFM = 1$ ), target ANI pin : ANI0, ANI16 to ANI23

( $T_A = -40$  to  $+85^{\circ}\text{C}$ ,  $2.4\text{ V} \leq V_{DD} = EV_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS} = 0\text{ V}$ , Reference voltage (+) =  $V_{BGR}$ , Reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ ) (HS (high-speed main) mode only)

| Parameter                                      | Symbol     | Conditions       |                                              | MIN. | TYP. | MAX.       | Unit          |
|------------------------------------------------|------------|------------------|----------------------------------------------|------|------|------------|---------------|
| Resolution                                     | $R_{ES}$   |                  |                                              | 8    |      |            | bit           |
| Conversion time                                | $t_{CONV}$ | 8-bit resolution | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 17   |      | 39         | $\mu\text{s}$ |
| Zero-scale error <sup>Notes 1, 2</sup>         | $E_{ZS}$   | 8-bit resolution | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |      |      | $\pm 0.60$ | %FSR          |
| Integral linearity error <sup>Note 1</sup>     | $I_{LE}$   | 8-bit resolution | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |      |      | $\pm 2.0$  | LSB           |
| Differential linearity error <sup>Note 1</sup> | $D_{LE}$   | 8-bit resolution | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |      |      | $\pm 1.0$  | LSB           |
| Reference voltage (+)                          | $V_{BGR}$  |                  |                                              | 1.38 | 1.45 | 1.5        | V             |
| Analog input voltage                           | $V_{AIN}$  |                  |                                              | 0    |      | $V_{BGR}$  | V             |

**Notes** 1. Excludes quantization error ( $\pm 1/2$  LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

### 30.6.2 Temperature sensor/internal reference voltage characteristics

( $T_A = -40$  to  $+85^{\circ}\text{C}$ ,  $2.4\text{ V} \leq V_{DD} = EV_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS} = 0\text{ V}$ ) (HS (high-speed main) mode only)

| Parameter                         | Symbol       | Conditions                                              | MIN. | TYP. | MAX. | Unit                   |
|-----------------------------------|--------------|---------------------------------------------------------|------|------|------|------------------------|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A = +25^{\circ}\text{C}$ |      | 1.05 |      | V                      |
| Internal reference voltage        | $V_{CONST}$  | Setting ADS register = 81H                              | 1.38 | 1.45 | 1.5  | V                      |
| Temperature coefficient           | $F_{VTMPS}$  | Temperature sensor that depends on the temperature      |      | -3.6 |      | mV/ $^{\circ}\text{C}$ |
| Operation stabilization wait time | $t_{AMP}$    |                                                         | 5    |      |      | $\mu\text{s}$          |

<R>

### 30.6.3 POR circuit characteristics

( $T_A = -40$  to  $+85^{\circ}\text{C}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter            | Symbol    | Conditions             | MIN. | TYP. | MAX. | Unit          |
|----------------------|-----------|------------------------|------|------|------|---------------|
| Detection voltage    | $V_{POR}$ | Power supply rise time | 1.47 | 1.51 | 1.55 | V             |
|                      | $V_{PDR}$ | Power supply fall time | 1.46 | 1.50 | 1.54 | V             |
| Minimum pulse width  | $T_{PW}$  |                        | 300  |      |      | $\mu\text{s}$ |
| Detection delay time |           |                        |      |      | 350  | $\mu\text{s}$ |

## 30.6.4 LVD circuit characteristics

(T<sub>A</sub> = -40 to +85°C, V<sub>PDR</sub> ≤ EV<sub>DD</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS</sub> = 0 V)

| Parameter            |                      | Symbol | Conditions             | MIN. | TYP. | MAX. | Unit |
|----------------------|----------------------|--------|------------------------|------|------|------|------|
| Detection voltage    | Supply voltage level | VLVD0  | Power supply rise time | 3.98 | 4.06 | 4.14 | V    |
|                      |                      |        | Power supply fall time | 3.90 | 3.98 | 4.06 | V    |
|                      |                      | VLVD1  | Power supply rise time | 3.68 | 3.75 | 3.82 | V    |
|                      |                      |        | Power supply fall time | 3.60 | 3.67 | 3.74 | V    |
|                      |                      | VLVD2  | Power supply rise time | 3.07 | 3.13 | 3.19 | V    |
|                      |                      |        | Power supply fall time | 3.00 | 3.06 | 3.12 | V    |
|                      |                      | VLVD3  | Power supply rise time | 2.96 | 3.02 | 3.08 | V    |
|                      |                      |        | Power supply fall time | 2.90 | 2.96 | 3.02 | V    |
|                      |                      | VLVD4  | Power supply rise time | 2.86 | 2.92 | 2.97 | V    |
|                      |                      |        | Power supply fall time | 2.80 | 2.86 | 2.91 | V    |
|                      |                      | VLVD5  | Power supply rise time | 2.76 | 2.81 | 2.87 | V    |
|                      |                      |        | Power supply fall time | 2.70 | 2.75 | 2.81 | V    |
|                      |                      | VLVD6  | Power supply rise time | 2.66 | 2.71 | 2.76 | V    |
|                      |                      |        | Power supply fall time | 2.60 | 2.65 | 2.70 | V    |
|                      |                      | VLVD7  | Power supply rise time | 2.56 | 2.61 | 2.66 | V    |
|                      |                      |        | Power supply fall time | 2.50 | 2.55 | 2.60 | V    |
|                      |                      | VLVD8  | Power supply rise time | 2.45 | 2.50 | 2.55 | V    |
|                      |                      |        | Power supply fall time | 2.40 | 2.45 | 2.50 | V    |
|                      |                      | VLVD9  | Power supply rise time | 2.05 | 2.09 | 2.13 | V    |
|                      |                      |        | Power supply fall time | 2.00 | 2.04 | 2.08 | V    |
|                      |                      | VLVD10 | Power supply rise time | 1.94 | 1.98 | 2.02 | V    |
|                      |                      |        | Power supply fall time | 1.90 | 1.94 | 1.98 | V    |
|                      |                      | VLVD11 | Power supply rise time | 1.84 | 1.88 | 1.91 | V    |
|                      |                      |        | Power supply fall time | 1.80 | 1.84 | 1.87 | V    |
|                      |                      | VLVD12 | Power supply rise time | 1.74 | 1.77 | 1.81 | V    |
|                      |                      |        | Power supply fall time | 1.70 | 1.73 | 1.77 | V    |
|                      |                      | VLVD13 | Power supply rise time | 1.64 | 1.67 | 1.70 | V    |
|                      |                      |        | Power supply fall time | 1.60 | 1.63 | 1.66 | V    |
| Minimum pulse width  |                      | tLW    |                        | 300  |      |      | μs   |
| Detection delay time |                      | tLD    |                        |      |      | 300  | μs   |

**LVD Detection Voltage of Interrupt & Reset Mode**(T<sub>A</sub> = -40 to +85°C, V<sub>PDR</sub> ≤ EV<sub>DD</sub> = V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS</sub> = 0 V)

| Parameter                | Symbol             | Conditions                                                                                 |                              | MIN. | TYP. | MAX. | Unit |
|--------------------------|--------------------|--------------------------------------------------------------------------------------------|------------------------------|------|------|------|------|
| Interrupt and reset mode | V <sub>LVD13</sub> | V <sub>POC2</sub> , V <sub>POC1</sub> , V <sub>POC0</sub> = 0, 0, 0, falling reset voltage |                              | 1.60 | 1.63 | 1.66 | V    |
|                          | V <sub>LVD12</sub> | LVIS1, LVIS0 = 1, 0 (+0.1 V)                                                               | Rising release reset voltage | 1.74 | 1.77 | 1.81 | V    |
|                          |                    |                                                                                            | Falling interrupt voltage    | 1.70 | 1.73 | 1.77 | V    |
|                          | V <sub>LVD11</sub> | LVIS1, LVIS0 = 0, 1 (+0.2 V)                                                               | Rising release reset voltage | 1.84 | 1.88 | 1.91 | V    |
|                          |                    |                                                                                            | Falling interrupt voltage    | 1.80 | 1.84 | 1.87 | V    |
|                          | V <sub>LVD4</sub>  | LVIS1, LVIS0 = 0, 0 (+1.2 V)                                                               | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V    |
|                          |                    |                                                                                            | Falling interrupt voltage    | 2.80 | 2.86 | 2.91 | V    |
|                          | V <sub>LVD11</sub> | V <sub>POC2</sub> , V <sub>POC1</sub> , V <sub>POC0</sub> = 0, 0, 1, falling reset voltage |                              | 1.80 | 1.84 | 1.87 | V    |
|                          | V <sub>LVD10</sub> | LVIS1, LVIS0 = 1, 0 (+0.1 V)                                                               | Rising release reset voltage | 1.94 | 1.98 | 2.02 | V    |
|                          |                    |                                                                                            | Falling interrupt voltage    | 1.90 | 1.94 | 1.98 | V    |
|                          | V <sub>LVD9</sub>  | LVIS1, LVIS0 = 0, 1 (+0.2 V)                                                               | Rising release reset voltage | 2.05 | 2.09 | 2.13 | V    |
|                          |                    |                                                                                            | Falling interrupt voltage    | 2.00 | 2.04 | 2.08 | V    |
|                          | V <sub>LVD2</sub>  | LVIS1, LVIS0 = 0, 0 (+1.2 V)                                                               | Rising release reset voltage | 3.07 | 3.13 | 3.19 | V    |
|                          |                    |                                                                                            | Falling interrupt voltage    | 3.00 | 3.06 | 3.12 | V    |
|                          | V <sub>LVD8</sub>  | V <sub>POC2</sub> , V <sub>POC1</sub> , V <sub>POC0</sub> = 0, 1, 0, falling reset voltage |                              | 2.40 | 2.45 | 2.50 | V    |
|                          | V <sub>LVD7</sub>  | LVIS1, LVIS0 = 1, 0 (+0.1 V)                                                               | Rising release reset voltage | 2.56 | 2.61 | 2.66 | V    |
|                          |                    |                                                                                            | Falling interrupt voltage    | 2.50 | 2.55 | 2.60 | V    |
|                          | V <sub>LVD6</sub>  | LVIS1, LVIS0 = 0, 1 (+0.2 V)                                                               | Rising release reset voltage | 2.66 | 2.71 | 2.76 | V    |
|                          |                    |                                                                                            | Falling interrupt voltage    | 2.60 | 2.65 | 2.70 | V    |
|                          | V <sub>LVD1</sub>  | LVIS1, LVIS0 = 0, 0 (+1.2 V)                                                               | Rising release reset voltage | 3.68 | 3.75 | 3.82 | V    |
|                          |                    |                                                                                            | Falling interrupt voltage    | 3.60 | 3.67 | 3.74 | V    |
|                          | V <sub>LVD5</sub>  | V <sub>POC2</sub> , V <sub>POC1</sub> , V <sub>POC0</sub> = 0, 1, 1, falling reset voltage |                              | 2.70 | 2.75 | 2.81 | V    |
|                          | V <sub>LVD4</sub>  | LVIS1, LVIS0 = 1, 0 (+0.1 V)                                                               | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V    |
|                          |                    |                                                                                            | Falling interrupt voltage    | 2.80 | 2.86 | 2.91 | V    |
|                          | V <sub>LVD3</sub>  | LVIS1, LVIS0 = 0, 1 (+0.2 V)                                                               | Rising release reset voltage | 2.96 | 3.02 | 3.08 | V    |
|                          |                    |                                                                                            | Falling interrupt voltage    | 2.90 | 2.96 | 3.02 | V    |
|                          | V <sub>LVD0</sub>  | LVIS1, LVIS0 = 0, 0 (+1.2 V)                                                               | Rising release reset voltage | 3.98 | 4.06 | 4.14 | V    |
|                          |                    |                                                                                            | Falling interrupt voltage    | 3.90 | 3.98 | 4.06 | V    |

**30.6.5 Supply voltage rise time**(T<sub>A</sub> = -40 to +85°C, V<sub>SS</sub> = 0 V)

| Parameter                                                                                        | Symbol           | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------------------------------------------------------------------------------------------|------------------|------------|------|------|------|------|
| V <sub>DD</sub> rise slope<br>(V <sub>DD</sub> : 0 V to V <sub>DD</sub> (MIN.) <sup>Note</sup> ) | SV <sub>DD</sub> |            |      |      | 54   | V/ms |

<R> **Note** V<sub>DD</sub> (MIN.) in each operating mode is as below.

HS (high-speed main) mode: 2.7 V@1 MHz to 24 MHz

2.4 V@1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V@1 MHz to 8 MHz

LV (low-voltage main) mode: 1.6 V@1 MHz to 4 MHz

<R> **Caution** When LVD off, be sure to use external RESET pin.

### 30.7 LCD Characteristics

#### 30.7.1 Resistance division method

##### (1) Static display mode

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{L4} \text{ (MIN.)} \leq V_{DD} \leq 5.5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ )

| Parameter         | Symbol   | Conditions | MIN. | TYP. | MAX.     | Unit |
|-------------------|----------|------------|------|------|----------|------|
| LCD drive voltage | $V_{L4}$ |            | 2.0  |      | $V_{DD}$ | V    |

##### (2) 1/2 bias method, 1/4 bias method

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{L4} \text{ (MIN.)} \leq V_{DD} \leq 5.5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ )

| Parameter         | Symbol   | Conditions | MIN. | TYP. | MAX.     | Unit |
|-------------------|----------|------------|------|------|----------|------|
| LCD drive voltage | $V_{L4}$ |            | 2.7  |      | $V_{DD}$ | V    |

##### (3) 1/3 bias method

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{L4} \text{ (MIN.)} \leq V_{DD} \leq 5.5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ )

| Parameter         | Symbol   | Conditions | MIN. | TYP. | MAX.                   | Unit |
|-------------------|----------|------------|------|------|------------------------|------|
| LCD drive voltage | $V_{L4}$ |            | 2.5  |      | $V_{DD}^{\text{Note}}$ | V    |

**Note** 5.5 V (MAX) when driving a memory-type liquid crystal (the MLCDEN bit of the MLCD register = 1).

## 30.7.2 Internal voltage boosting method

## (1) 1/3 bias method

(TA = -40 to +85°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter                                      | Symbol              | Conditions                                                | MIN.                       | TYP.              | MAX.              | Unit |   |
|------------------------------------------------|---------------------|-----------------------------------------------------------|----------------------------|-------------------|-------------------|------|---|
| LCD output voltage variation range             | V <sub>L1</sub>     | C1 to C4 <sup>Note 1</sup><br>= 0.47 μF <sup>Note 2</sup> | VLCD = 04H                 | 0.90              | 1.00              | 1.08 | V |
|                                                |                     |                                                           | VLCD = 05H                 | 0.95              | 1.05              | 1.13 | V |
|                                                |                     |                                                           | VLCD = 06H                 | 1.00              | 1.10              | 1.18 | V |
|                                                |                     |                                                           | VLCD = 07H                 | 1.05              | 1.15              | 1.23 | V |
|                                                |                     |                                                           | VLCD = 08H                 | 1.10              | 1.20              | 1.28 | V |
|                                                |                     |                                                           | VLCD = 09H                 | 1.15              | 1.25              | 1.33 | V |
|                                                |                     |                                                           | VLCD = 0AH                 | 1.20              | 1.30              | 1.38 | V |
|                                                |                     |                                                           | VLCD = 0BH                 | 1.25              | 1.35              | 1.43 | V |
|                                                |                     |                                                           | VLCD = 0CH                 | 1.30              | 1.40              | 1.48 | V |
|                                                |                     |                                                           | VLCD = 0DH                 | 1.35              | 1.45              | 1.53 | V |
|                                                |                     |                                                           | VLCD = 0EH                 | 1.40              | 1.50              | 1.58 | V |
|                                                |                     |                                                           | VLCD = 0FH                 | 1.45              | 1.55              | 1.63 | V |
|                                                |                     |                                                           | VLCD = 10H                 | 1.50              | 1.60              | 1.68 | V |
|                                                |                     |                                                           | VLCD = 11H                 | 1.55              | 1.65              | 1.73 | V |
|                                                |                     |                                                           | VLCD = 12H                 | 1.60              | 1.70              | 1.78 | V |
|                                                |                     |                                                           | VLCD = 13H                 | 1.65              | 1.75              | 1.83 | V |
| Doubler output voltage                         | V <sub>L2</sub>     | C1 to C4 <sup>Note 1</sup> = 0.47 μF                      | 2 V <sub>L1</sub><br>-0.1  | 2 V <sub>L1</sub> | 2 V <sub>L1</sub> | V    |   |
| Tripler output voltage                         | V <sub>L4</sub>     | C1 to C4 <sup>Note 1</sup> = 0.47 μF                      | 3 V <sub>L1</sub><br>-0.15 | 3 V <sub>L1</sub> | 3 V <sub>L1</sub> | V    |   |
| Reference voltage setup time <sup>Note 2</sup> | t <sub>VWAIT1</sub> |                                                           | 5                          |                   |                   | ms   |   |
| Voltage boost wait time <sup>Note 3</sup>      | t <sub>VWAIT2</sub> | C1 to C4 <sup>Note 1</sup> = 0.47 μF                      | 500                        |                   |                   | ms   |   |

**Notes 1.** This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND

C3: A capacitor connected between VL2 and GND

C4: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = 0.47 pF±30 %

- This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).
- This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

## (2) 1/4 bias method

(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

| Parameter                                      | Symbol              | Conditions                                                | MIN.                    | TYP.              | MAX.              | Unit |   |
|------------------------------------------------|---------------------|-----------------------------------------------------------|-------------------------|-------------------|-------------------|------|---|
| LCD output voltage variation range             | V <sub>L1</sub>     | C1 to C5 <sup>Note 1</sup><br>= 0.47 μF <sup>Note 2</sup> | VLCD = 04H              | 0.90              | 1.00              | 1.08 | V |
|                                                |                     |                                                           | VLCD = 05H              | 0.95              | 1.05              | 1.13 | V |
|                                                |                     |                                                           | VLCD = 06H              | 1.00              | 1.10              | 1.18 | V |
|                                                |                     |                                                           | VLCD = 07H              | 1.05              | 1.15              | 1.23 | V |
|                                                |                     |                                                           | VLCD = 08H              | 1.10              | 1.20              | 1.28 | V |
|                                                |                     |                                                           | VLCD = 09H              | 1.15              | 1.25              | 1.33 | V |
|                                                |                     |                                                           | VLCD = 0AH              | 1.20              | 1.30              | 1.38 | V |
|                                                |                     |                                                           | VLCD = 0BH              | 1.25              | 1.35              | 1.43 | V |
|                                                |                     |                                                           | VLCD = 0CH              | 1.30              | 1.40              | 1.48 | V |
|                                                |                     |                                                           | VLCD = 0DH              | 1.35              | 1.45              | 1.53 | V |
|                                                |                     |                                                           | VLCD = 0EH              | 1.40              | 1.50              | 1.58 | V |
|                                                |                     |                                                           | VLCD = 0FH              | 1.45              | 1.55              | 1.63 | V |
|                                                |                     |                                                           | VLCD = 10H              | 1.50              | 1.60              | 1.68 | V |
|                                                |                     |                                                           | VLCD = 11H              | 1.55              | 1.65              | 1.73 | V |
|                                                |                     |                                                           | VLCD = 12H              | 1.60              | 1.70              | 1.78 | V |
|                                                |                     |                                                           | VLCD = 13H              | 1.65              | 1.75              | 1.83 | V |
| Doubler output voltage                         | V <sub>L2</sub>     | C1 to C5 <sup>Note 1</sup> = 0.47 μF                      | 2 V <sub>L1</sub> −0.08 | 2 V <sub>L1</sub> | 2 V <sub>L1</sub> | V    |   |
| Tripler output voltage                         | V <sub>L3</sub>     | C1 to C5 <sup>Note 1</sup> = 0.47 μF                      | 3 V <sub>L1</sub> −0.12 | 3 V <sub>L1</sub> | 3 V <sub>L1</sub> | V    |   |
| Quadruply output voltage                       | V <sub>L4</sub>     | C1 to C5 <sup>Note 1</sup> = 0.47 μF                      | 4 V <sub>L1</sub> −0.16 | 4 V <sub>L1</sub> | 4 V <sub>L1</sub> | V    |   |
| Reference voltage setup time <sup>Note 2</sup> | t <sub>VWAIT1</sub> |                                                           | 5                       |                   |                   | ms   |   |
| Voltage boost wait time <sup>Note 3</sup>      | t <sub>VWAIT2</sub> | C1 to C5 <sup>Note 1</sup> = 0.47 μF                      | 500                     |                   |                   | ms   |   |

**Notes** 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V<sub>L1</sub> and GNDC3: A capacitor connected between V<sub>L2</sub> and GNDC4: A capacitor connected between V<sub>L3</sub> and GNDC5: A capacitor connected between V<sub>L4</sub> and GND

C1 = C2 = C3 = C4 = C5 = 0.47 pF ± 30 %

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).



### 30.7.3 Capacitor split method

#### (1) 1/3 bias method

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $2.2\text{ V} \leq V_{DD} = EV_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                                   | Symbol      | Conditions                                                      | MIN.                         | TYP.                 | MAX.                         | Unit |
|---------------------------------------------|-------------|-----------------------------------------------------------------|------------------------------|----------------------|------------------------------|------|
| $V_{L4}$ voltage                            | $V_{L4}$    | $C1 \text{ to } C4 = 0.47\text{ }\mu\text{F}$ <sup>Note 2</sup> |                              | $V_{DD}$             |                              | V    |
| $V_{L2}$ voltage                            | $V_{L2}$    | $C1 \text{ to } C4 = 0.47\text{ }\mu\text{F}$ <sup>Note 2</sup> | $\frac{2}{3} V_{L4}$<br>-0.1 | $\frac{2}{3} V_{L4}$ | $\frac{2}{3} V_{L4}$<br>+0.1 | V    |
| $V_{L1}$ voltage                            | $V_{L1}$    | $C1 \text{ to } C4 = 0.47\text{ }\mu\text{F}$ <sup>Note 2</sup> | $\frac{1}{3} V_{L4}$<br>-0.1 | $\frac{1}{3} V_{L4}$ | $\frac{1}{3} V_{L4}$<br>+0.1 | V    |
| Capacitor split wait time <sup>Note 1</sup> | $t_{VWAIT}$ |                                                                 | 100                          |                      |                              | ms   |

**Notes** 1. This is the wait time from when voltage bucking is started ( $VLCON = 1$ ) until display is enabled ( $LCDON = 1$ ).

2. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between  $V_{L1}$  and GND

C3: A capacitor connected between  $V_{L2}$  and GND

C4: A capacitor connected between  $V_{L4}$  and GND

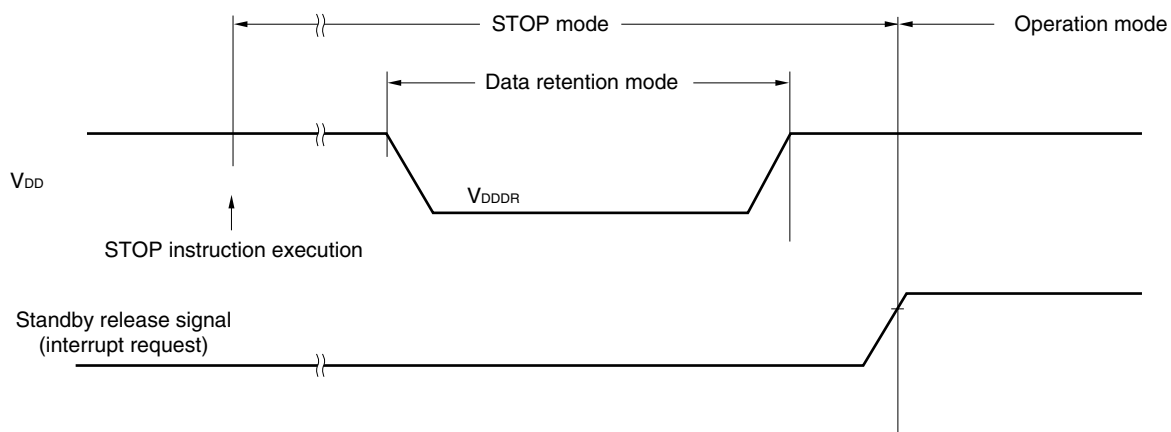
$C1 = C2 = C3 = C4 = 0.47\text{ }\mu\text{F} \pm 30\%$

### 30.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ )

| Parameter                         | Symbol     | Conditions | MIN.                 | TYP. | MAX. | Unit |
|-----------------------------------|------------|------------|----------------------|------|------|------|
| <R> Data retention supply voltage | $V_{DDDR}$ |            | 1.46 <sup>Note</sup> |      | 5.5  | V    |

**Note** The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



### <R> 30.9 Flash Memory Programming Characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq EV_{DD} = V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS} = 0\text{ V}$ )

| Parameter                                                    | Symbol     | Conditions                                                       | MIN.    | TYP.      | MAX. | Unit  |
|--------------------------------------------------------------|------------|------------------------------------------------------------------|---------|-----------|------|-------|
| System clock frequency                                       | $f_{CLK}$  | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                     | 1       |           | 24   | MHz   |
| Number of code flash rewrites<br><small>Note 1, 2, 3</small> | $C_{erwr}$ | Retained for 20 years $T_A = 85^\circ\text{C}$ <sup>Note 3</sup> | 1,000   |           |      | Times |
| Number of data flash rewrites<br><small>Note 1, 2, 3</small> |            | Retained for 1 year $T_A = 25^\circ\text{C}$ <sup>Note 3</sup>   |         | 1,000,000 |      |       |
|                                                              |            | Retained for 5 years $T_A = 85^\circ\text{C}$ <sup>Note 3</sup>  | 100,000 |           |      |       |
|                                                              |            | Retained for 20 years $T_A = 85^\circ\text{C}$ <sup>Note 3</sup> | 10,000  |           |      |       |

**Notes 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

**2.** When using flash memory programmer and Renesas Electronics self programming library

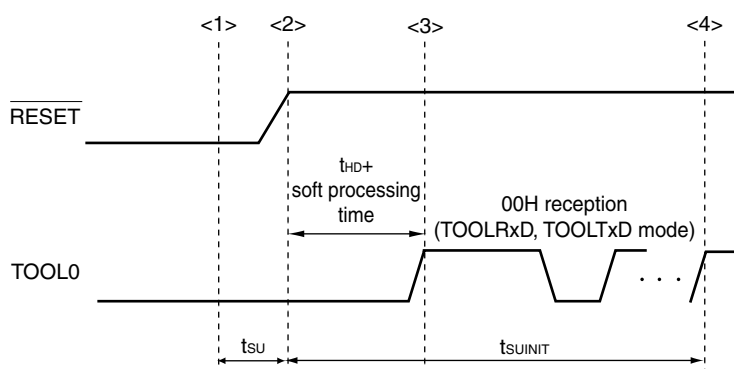
**3.** This characteristic indicates the flash memory characteristic and based on Renesas Electronics reliability test.

**Remark** When updating data multiple times, use the flash memory as one for updating data.

## 30.10 Timing Specifications for Switching Flash Memory Programming Modes

| Parameter                                                                                             | Symbol             | Conditions                                            | MIN. | TYP. | MAX. | Unit          |
|-------------------------------------------------------------------------------------------------------|--------------------|-------------------------------------------------------|------|------|------|---------------|
| How long from when a pin reset ends until the initial communication settings are specified            | $t_{\text{SUNIT}}$ | POR and LVD reset must end before the pin reset ends. |      |      | 100  | ms            |
| How long from when the TOOL0 pin is placed at the low level until a pin reset ends                    | $t_{\text{SU}}$    | POR and LVD reset must end before the pin reset ends. | 10   |      |      | $\mu\text{s}$ |
| How long the TOOL0 pin must be kept at the low level after a reset ends (except soft processing time) | $t_{\text{HD}}$    | POR and LVD reset must end before the pin reset ends. | 1    |      |      | ms            |

&lt;R&gt;



&lt;1&gt; The low level is input to the TOOL0 pin.

&lt;2&gt; The pins reset ends. (POR and LVD reset must end before the pin reset ends.)

&lt;3&gt; The TOOL0 pin is set to the high level.

&lt;4&gt; Setting of the flash memory programming mode by UART reception and completion of the baud rate setting

**Remark**  $t_{\text{SUNIT}}$ : The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the reset ends.

$t_{\text{SU}}$ : How long from when the TOOL0 pin is placed at the low level until a pin reset ends (MIN. 10  $\mu\text{s}$ )

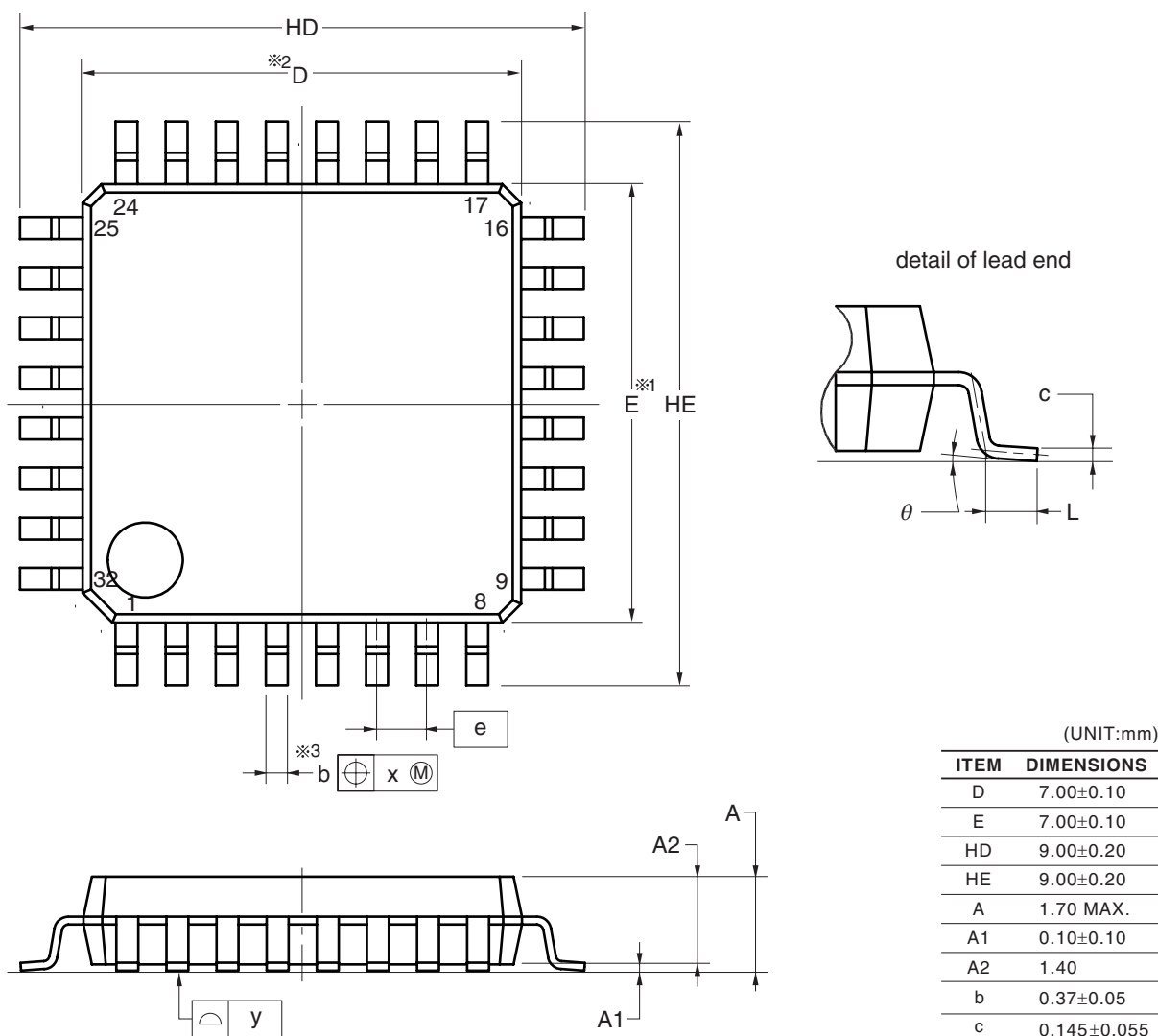
$t_{\text{HD}}$ : How long to keep the TOOL0 pin at the low level from when the external or internal reset ends (except software processing time)

## CHAPTER 31 PACKAGE DRAWINGS

## 31.1 32-pin products

R5F10RB8AFP, R5F10RBAAFP, R5F10RBCAFP

| JEITA Package Code | RENESAS Code | Previous Code  | MASS (TYP.) [g] |
|--------------------|--------------|----------------|-----------------|
| P-LQFP32-7x7-0.80  | PLQP0032GB-A | P32GA-80-GBT-1 | 0.2             |



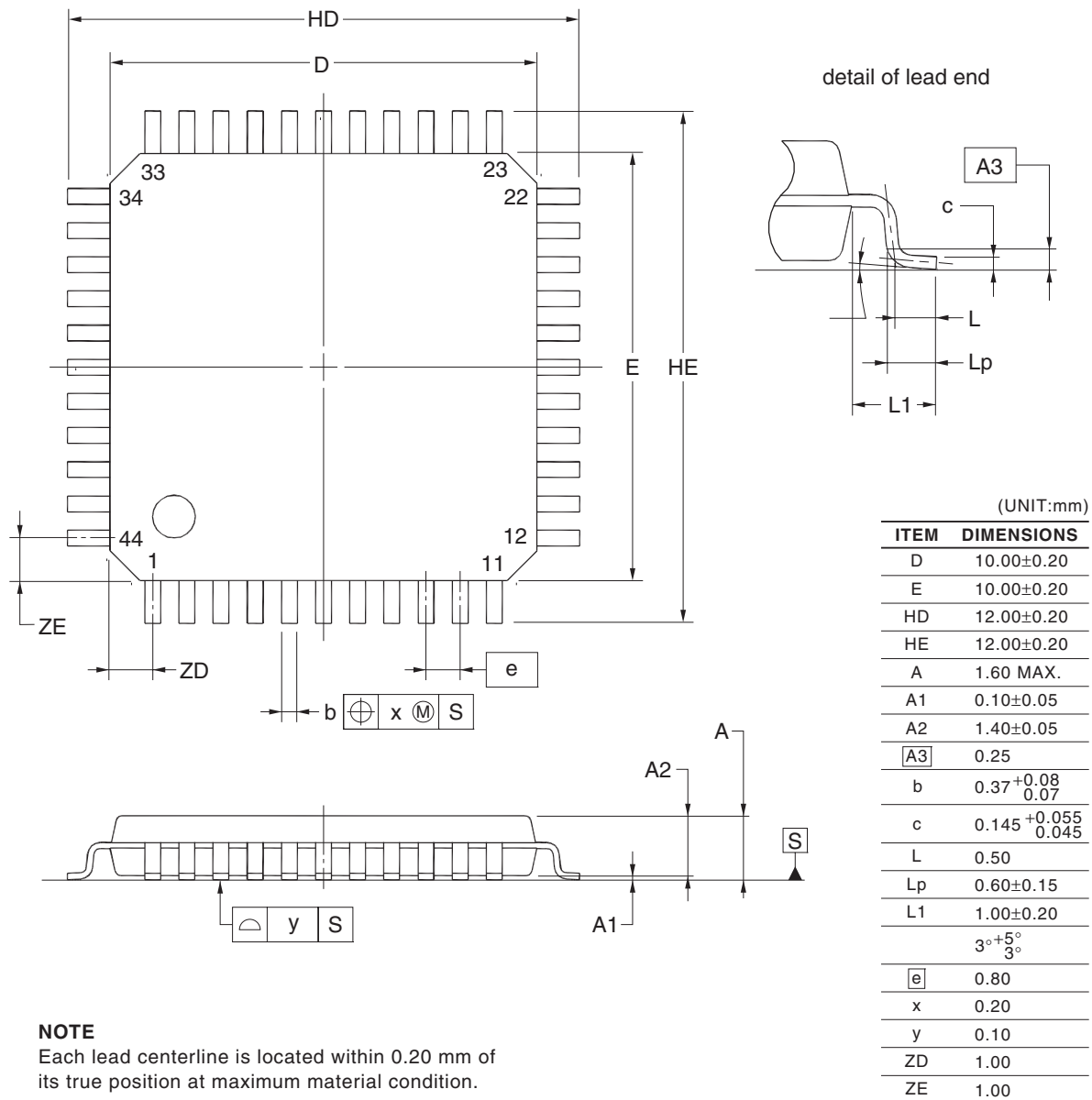
## NOTE

1. Dimensions "※1" and "※2" do not include mold flash.
2. Dimension "※3" does not include trim offset.

## 31.2 44-pin products

R5F10RF8AFP, R5F10RFAAFP, R5F10RFCAFP

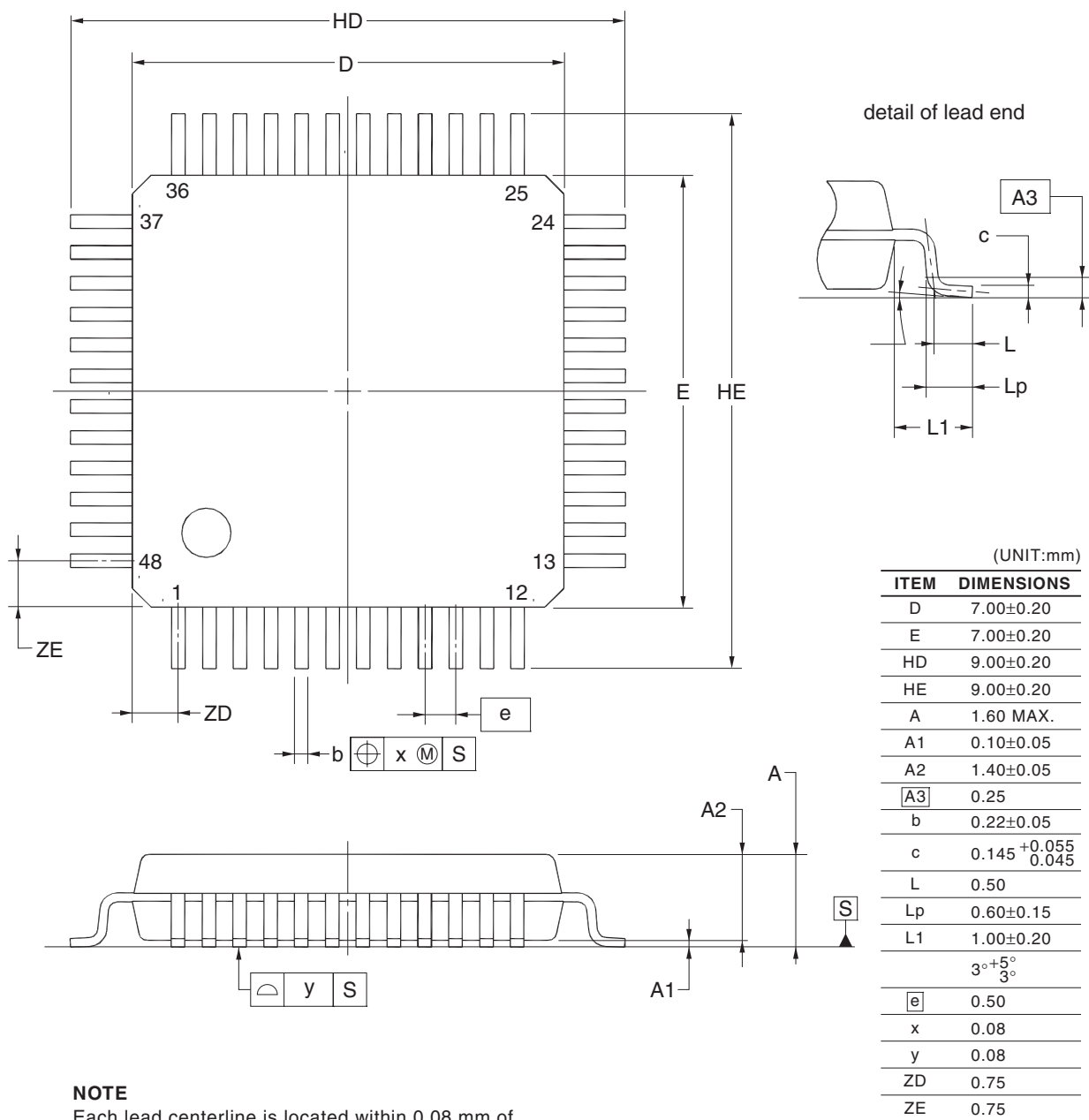
| JEITA Package Code  | RENESAS Code | Previous Code  | MASS (TYP.) [g] |
|---------------------|--------------|----------------|-----------------|
| P-LQFP44-10x10-0.80 | PLQP0044GC-A | P44GB-80-UES-2 | 0.36            |



## 31.3 48-pin products

R5F10RG8AFB, R5F10RGAAFB, R5F10RGCAFB

| JEITA Package Code | RENESAS Code | Previous Code  | MASS (TYP.) [g] |
|--------------------|--------------|----------------|-----------------|
| P-LFQFP48-7x7-0.50 | PLQP0048KF-A | P48GA-50-8EU-1 | 0.16            |

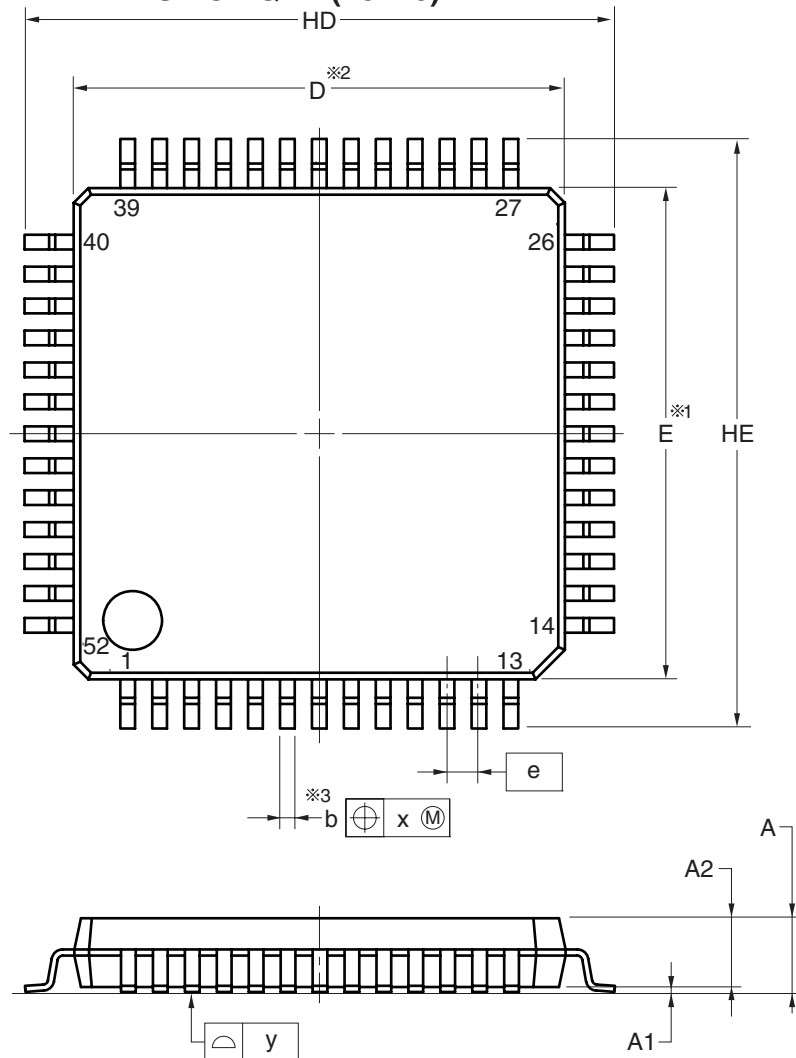
**NOTE**

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

## 31.4 52-pin products

R5F10RJ8AFA, R5F10RJAAFA, R5F10RJCAFA

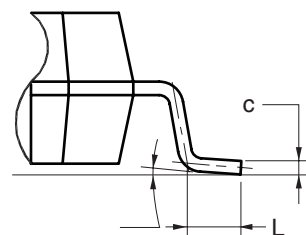
## 52-PIN PLASTIC LQFP (10x10)



## NOTE

1. Dimensions "※1" and "※2" do not include mold flash.
2. Dimension "※3" does not include trim offset.

detail of lead end



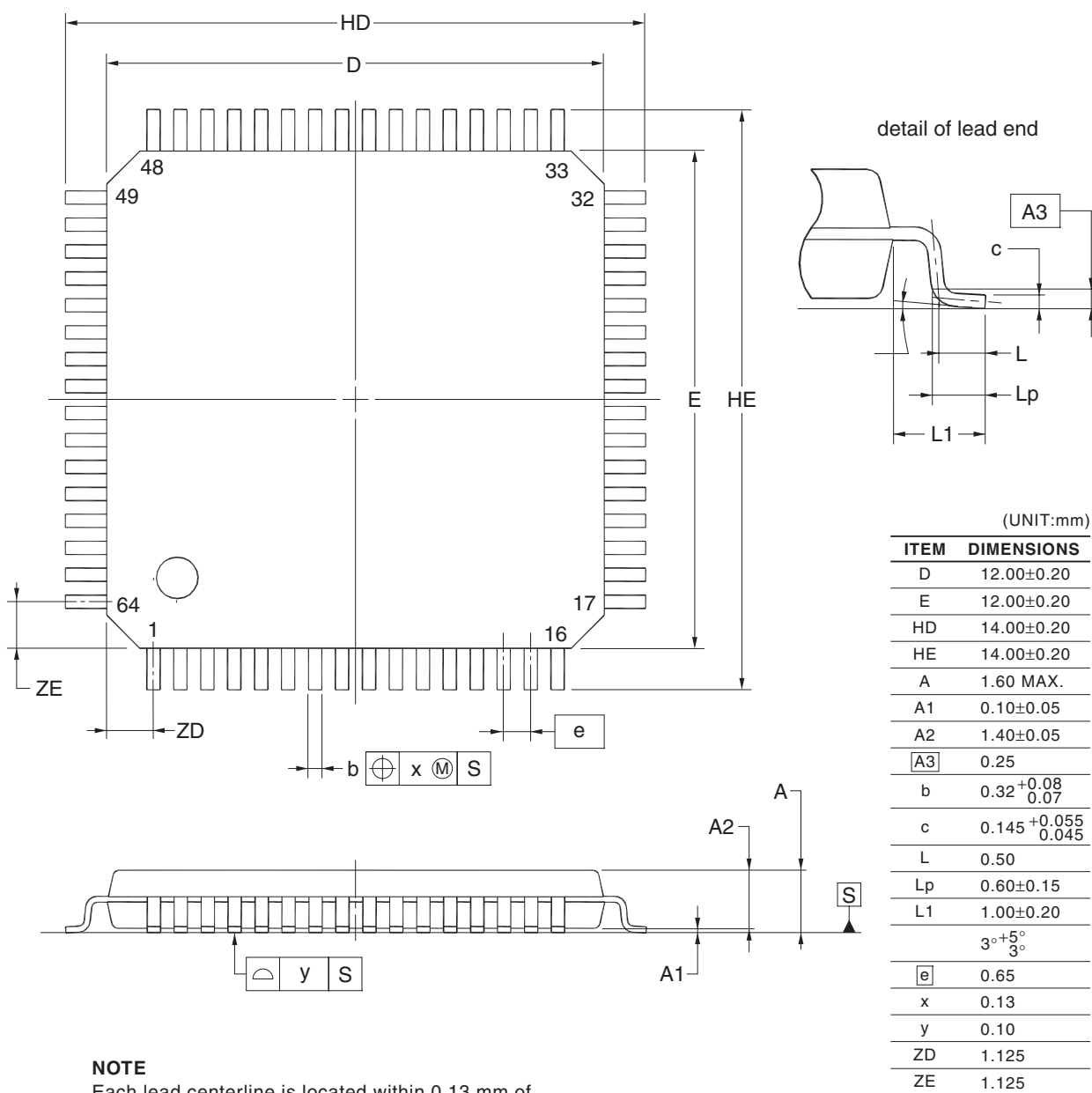
(UNIT:mm)

| ITEM         | DIMENSIONS  |
|--------------|-------------|
| D            | 10.00±0.10  |
| E            | 10.00±0.10  |
| HD           | 12.00±0.20  |
| HE           | 12.00±0.20  |
| A            | 1.70 MAX.   |
| A1           | 0.10±0.05   |
| A2           | 1.40        |
| b            | 0.32±0.05   |
| c            | 0.145±0.055 |
| L            | 0.50±0.15   |
|              | 0° to 8°    |
| e            | 0.65        |
| x            | 0.13        |
| y            | 0.10        |
| P52GB-65-GBS |             |

## 31.5 64-pin products

R5F10RLAAFA, R5F10RLCAFA

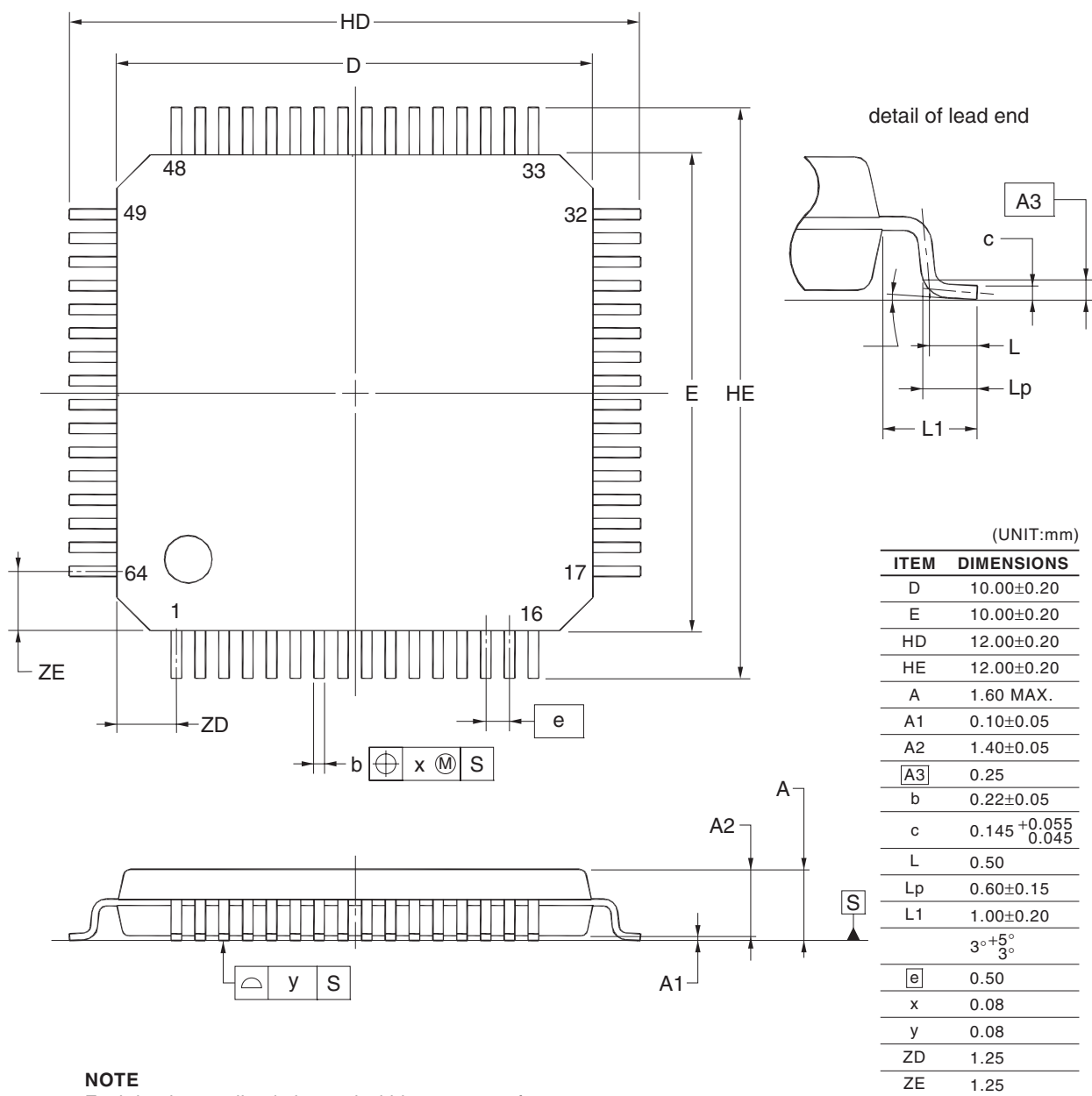
| JEITA Package Code  | RENESAS Code | Previous Code  | MASS (TYP.) [g] |
|---------------------|--------------|----------------|-----------------|
| P-LQFP64-12x12-0.65 | PLQP0064JA-A | P64GK-65-UET-2 | 0.51            |





## R5F10RLAAFB, R5F10RLCAFB

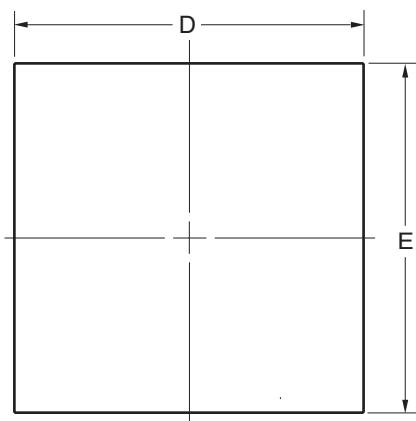
| JEITA Package Code   | RENESAS Code | Previous Code  | MASS (TYP.) [g] |
|----------------------|--------------|----------------|-----------------|
| P-LFQFP64-10x10-0.50 | PLQP0064KF-A | P64GB-50-UEU-2 | 0.35            |



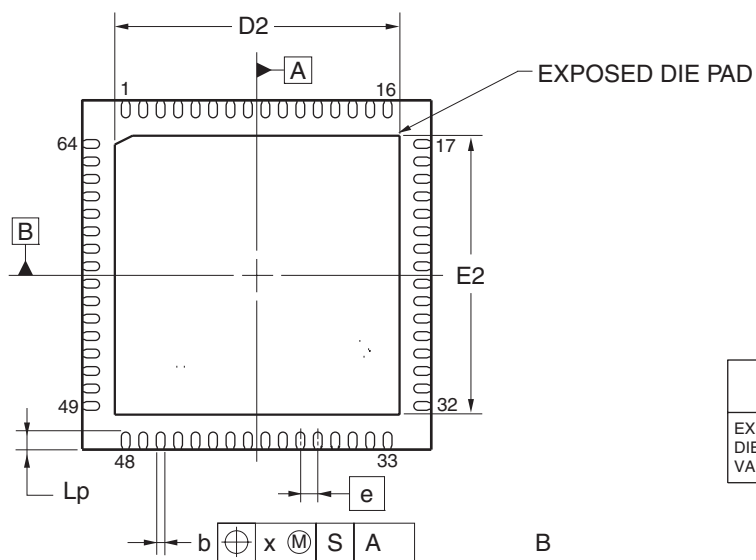
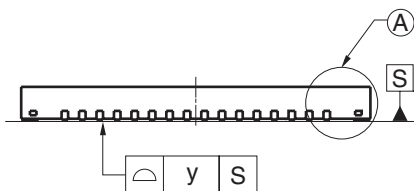
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## R5F10RLAANB, R5F10RLCANB

| JEITA Package Code | RENESAS Code | Previous Code  | MASS (TYP.) [g] |
|--------------------|--------------|----------------|-----------------|
| P-HWQFN64-8x8-0.40 | PWQN0064LA-A | P64K8-40-9B5-1 | 0.16            |



DETAIL OF (A) PART



(UNIT:mm)

| ITEM | DIMENSIONS |
|------|------------|
| D    | 8.00±0.05  |
| E    | 8.00±0.05  |
| A    | 0.75±0.05  |
| b    | 0.20±0.05  |
| e    | 0.40       |
| Lp   | 0.40±0.10  |
| x    | 0.05       |
| y    | 0.05       |

| ITEM                       |   | D2   |      |      | E2   |      |      |
|----------------------------|---|------|------|------|------|------|------|
|                            |   | MIN  | NOM  | MAX  | MIN  | NOM  | MAX  |
| EXPOSED DIE PAD VARIATIONS | A | 6.45 | 6.50 | 6.55 | 6.45 | 6.50 | 6.55 |

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## APPENDIX A REVISION HISTORY

## A.1 Major Revisions in This Edition

(1/10)

| Page                              | Description                                                                                                                    | Classification |
|-----------------------------------|--------------------------------------------------------------------------------------------------------------------------------|----------------|
| Though out                        | Renamed interval timer (unit) to 12-bit interval timer                                                                         | (b)            |
|                                   | Addition of pin name of the peripheral I/O redirection function                                                                | (c)            |
|                                   | Renamed $V_{LVI}$ , $V_{LVIH}$ , $V_{LVIL}$ to $V_{LVD}$ , $V_{LVDH}$ , $V_{LVDL}$ (LVD detection voltage)                     | (b)            |
|                                   | Renamed interrupt source of RAM parity error (RAMTOP) to RPE                                                                   | (b)            |
| <b>CHAPTER 1 OUTLINE</b>          |                                                                                                                                |                |
| p.3                               | Modification from <b>1.2 Ordering Information</b> to <b>1.2 List of Part Numbers</b>                                           | (b, c)         |
| p.3                               | Addition of <b>Figure 1-1. Part Number, Memory Size, and Package of RL78/L12</b>                                               | (c)            |
| p.10                              | Modification of description of INTP0 to INTP7 in <b>1.4 Pin Identification</b>                                                 | (c)            |
| p.11 to 15                        | Modification of <b>1.5 Block Diagram</b>                                                                                       | (c)            |
| p.16, 17                          | Addition and Modification of description in <b>1.6 Outline of Functions</b>                                                    | (a, b)         |
| <b>CHAPTER 2 PIN FUNCTIONS</b>    |                                                                                                                                |                |
| p.19 to 28                        | Modification of <b>2.1 Port Function</b>                                                                                       | (c)            |
| p.43                              | Addition of <b>remark</b> to <b>2.3 Pin I/O Circuits and Recommended Connection of Unused Pins</b>                             | (c)            |
| p.46 to 49                        | Change of <b>Figure 2-1. Pin I/O Circuit List</b>                                                                              | (c)            |
| <b>CHAPTER 3 CPU ARCHITECTURE</b> |                                                                                                                                |                |
| p.50                              | Modification of description in <b>3.1 Memory Space</b>                                                                         | (c)            |
| p.51 to 53                        | Modification of <b>Figures 3-1 to 3-3</b>                                                                                      | (c)            |
| p.54                              | Addition of <b>remark</b> to <b>Table 3-1. Correspondence Between Address Values and Block Numbers in Flash Memory</b>         | (c)            |
| p.57                              | Modification of description in <b>3.1.1 (4) On-chip debug security ID setting area</b>                                         | (c)            |
| p.58                              | Modification of description in <b>3.1.2 Mirror area</b>                                                                        | (a)            |
| p.59                              | Deletion of <b>caution 2</b> in <b>Figure 3-4. Format of Processor Mode Control Register (PMC)</b>                             | (c)            |
| p.60                              | Modification of description and <b>cautions 1, 2</b> in <b>3.1.3 Internal data memory space</b>                                | (c)            |
| p.61                              | Modification of description in <b>3.1.6 Data memory addressing</b>                                                             | (c)            |
| p.61 to 63                        | Addition of <b>Figures 3-5 to 3-7</b>                                                                                          | (c)            |
| p.64 to 67                        | Modification of <b>3.2.1 Control registers</b> , <b>3.2.2 General-purpose registers</b> , and <b>3.2.3 ES and CS registers</b> | (c)            |
| p.69                              | Modification of description in <b>3.2.4 Special function registers (SFRs)</b>                                                  | (c)            |
| p.71                              | Addition of <b>note 5</b> to <b>Table 3-5. SFR List (3/4)</b>                                                                  | (c)            |
| p.74                              | Modification of description in <b>3.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)</b>     | (c)            |
| p.77                              | Modification of After Reset of HIOTRM register and <b>notes 1, 2</b> in <b>Table 3-6. Extended SFR (2nd SFR) List (1/6)</b>    | (c)            |
| p.81, 83 to 97                    | Modification of <b>Figures 3-14 to 3-16, 3-18 to 3-41</b>                                                                      | (c)            |

**Remark** "Classification" in the above table classifies revisions as follows.

- (a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents

(2/10)

| Page                             | Description                                                                                                                                                                   | Classification |
|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| p.84                             | Modification of [Operand format] in <b>3.4.1 Implied addressing</b>                                                                                                           | (c)            |
| p.85                             | Modification of [Operand format] in <b>3.4.3 Direct addressing</b>                                                                                                            | (c)            |
| p.89                             | Modification of [Function] in <b>3.4.7 Based addressing</b>                                                                                                                   | (b)            |
| p.94                             | Modification from [Operand format] to [Description format], modification of [Function] and [Description format], and addition of description in <b>3.4.9 Stack addressing</b> | (b)            |
| <b>CHAPTER 4 PORT FUNCTIONS</b>  |                                                                                                                                                                               |                |
| p.98                             | Modification of description in <b>4.1 Port Functions</b>                                                                                                                      | (c)            |
| p.100                            | Addition of <b>caution</b> to <b>4.3 Registers Controlling Port Function</b>                                                                                                  | (c)            |
| p.105                            | Modification of <b>Figure 4-2. Format of Port Register (64-pin products)</b>                                                                                                  | (c)            |
| p.106                            | Modification of description and addition of <b>caution</b> to <b>4.3.3 Pull-up resistor option registers (PUxx)</b>                                                           | (c)            |
| p.107                            | Addition of description in <b>4.3.5 Port output mode registers (POM1)</b>                                                                                                     | (b)            |
| p.108                            | Addition of <b>cautions 1 and 2</b> to <b>Figure 4-6. Format of Port Mode Control Register</b>                                                                                | (b)            |
| p.110                            | Modification of description in <b>4.3.8 Peripheral I/O redirection register (PIOR)</b>                                                                                        | (c)            |
| p.114                            | Modification of description in <b>4.4.1 (2) Input mode</b> and <b>4.4.3 (2) Input mode</b>                                                                                    | (b)            |
| p.115                            | Modification of description in <b>4.4.4 Connecting to external device with different potential (1.8 V, 2.5 V, 3 V)</b>                                                        | (c)            |
| p.117                            | Addition of <b>caution</b> to <b>4.5 Settings of Port Mode Register, and Output Latch When Using Alternate Function</b>                                                       | (c)            |
| p.127                            | Addition of <b>4.6.2 Notes on specifying the pin settings</b>                                                                                                                 | (c)            |
| <b>CHAPTER 5 CLOCK GENERATOR</b> |                                                                                                                                                                               |                |
| p.128                            | Addition of <b>5.1 (1) &lt;2&gt; High-speed on-chip oscillator</b>                                                                                                            | (b)            |
| p.131                            | Modification of <b>Figure 5-1. Block Diagram of Clock Generator</b>                                                                                                           | (b)            |
| p.133, 134                       | Modification of <b>cautions 1, 7</b> and addition of <b>cautions 4 to 6</b> to <b>Figure 5-2. Format of Clock Operation Mode Control Register (CMC)</b>                       | (c)            |
| p.144                            | Deletion of <b>cautions 1 to 4</b> and addition of <b>cautions 1 to 3</b> in <b>5.3.8 High-speed on-chip oscillator frequency select register (HOCODIV)</b>                   | (b)            |
| p.147                            | Modification of <b>caution</b> in <b>Figure 5-12. Example of External Circuit of XT1 Oscillator</b>                                                                           | (c)            |
| p.152                            | Modification of <b>note 3</b> in <b>Figure 5-14. Clock Generator Operation When Power Supply Voltage Is Turned On</b>                                                         | (b)            |
| p.153                            | Modification of description of [Option byte setting] in <b>5.6.1 Example of setting high-speed on-chip oscillator</b>                                                         | (c)            |
| p.154                            | Addition of description to <b>5.6.2 Example of setting X1 oscillation clock</b>                                                                                               | (c)            |
| p.156                            | Addition of description to <b>Figure 5-15. CPU Clock Status Transition Diagram</b>                                                                                            | (c)            |
| p.157                            | Addition of description to <b>Table 5-3. CPU Clock Transition and SFR Register Setting Examples</b>                                                                           | (c)            |
| p.162, 163                       | Modification and deletion of description in <b>Table 5-4. Changing CPU Clock</b>                                                                                              | (c)            |
| p.164                            | Modification of <b>remark 2</b> to <b>5.6.6 Time required for switchover of CPU clock and system clock</b>                                                                    | (b)            |

**Remark** "Classification" in the above table classifies revisions as follows.

- (a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents

(3/10)

| Page                                                   | Description                                                                                                                                                    | Classification |
|--------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| <b>CHAPTER 6 TIMER ARRAY UNIT</b>                      |                                                                                                                                                                |                |
| p.168                                                  | Modification of description in 6.1.1 (7) Delay counter                                                                                                         | (a)            |
| p.169                                                  | Modification of <b>caution</b> in 6.1.2 (4) Remote control output function                                                                                     | (c)            |
| p.174                                                  | Modification of <b>Figure 6-2. Internal Block Diagram of Channels 0, 2, 4, 6 of Timer Array Unit 0</b>                                                         | (a)            |
| p.174 to 176                                           | Addition of <b>Figures 6-3 to 6-6</b>                                                                                                                          | (c)            |
| p.177                                                  | Modification of <b>Table 6-3. Timer Count Register mn (TCRmn) Read Value in Various Operation Modes</b>                                                        | (c)            |
| p.178                                                  | Modification of description in 6.2.2 Timer data register mn (TDRmn)                                                                                            | (b)            |
| p.180                                                  | Modification of <b>caution 1</b> in <b>Figure 6-10. Format of Peripheral Enable Register 0 (PER0)</b>                                                          | (c)            |
| p.182                                                  | Modification of <b>note</b> and <b>remark 2</b> and addition of <b>caution 2</b> to <b>Figure 6-11. Format of Timer Clock Select register m (TPSm) (1/2)</b>   | (c)            |
| p.185 to 188                                           | Modification of <b>note 1</b> in <b>Figure 6-12. Format of Timer Mode Register mn (TMRmn)</b>                                                                  | (a)            |
| p.188                                                  | Modification of Setting of starting counting and interrupt and addition of <b>note 3</b> in <b>Figure 6-12. Format of Timer Mode Register mn (TMRmn) (4/4)</b> | (b)            |
| p.192                                                  | Modification of description in <b>Figure 6-16. Format of Timer Channel Stop register m (TTm)</b>                                                               | (c)            |
| p.193                                                  | Addition of <b>caution</b> to <b>Figure 6-17. Format of Timer Input Select register 0 (TIS0)</b>                                                               | (b)            |
| p.194                                                  | Modification of description in <b>Figure 6-19. Format of Timer Output Enable register m (TOEm)</b>                                                             | (c)            |
| p.208                                                  | Modification of description in <b>Table 6-6. Operations from Count Operation Enabled State to Timer count Register mn (TCRmn) Count Start</b>                  | (c)            |
| p.209                                                  | Addition of title and <b>remark</b> to <b>6.5.3 Operation of counter</b>                                                                                       | (c)            |
| p.211                                                  | Modification of description, <b>remark</b> and addition <b>note</b> to <b>Figure 6-30. Start Timing (In Capture Mode : Input Pulse Interval Measurement)</b>   | (a, c)         |
| p.215                                                  | Modification of description in <b>6.6.2 TOMn Pin Output Setting</b>                                                                                            | (c)            |
| p.217 to 219                                           | Modification of <b>Figures 6-35 to 6-37</b>                                                                                                                    | (c)            |
| p.229, 234, 238, 243, 246, 252                         | Modification of <b>Figures 6-47, 6-51, 6-55, 6-59, 6-63, 6-67 Block Diagram</b>                                                                                | (b)            |
| p.265, 266, 268, 270                                   | Modification of <b>remark</b> in <b>6.8.3 Operation as multiple PWM output function</b>                                                                        | (a)            |
| p.274, 275                                             | Modification of <b>Figure 6-83. Procedure for Setting Remote control Output</b>                                                                                | (b)            |
| <b>CHAPTER 7 REAL-TIME CLOCK</b>                       |                                                                                                                                                                |                |
| p.294                                                  | Modification of <b>7.4.2 Shifting to HALT/STOP mode after starting operation</b>                                                                               | (c)            |
| p.301                                                  | Modification of figure title in <b>Figure 7-23</b>                                                                                                             | (c)            |
| <b>CHAPTER 8 INTERVAL TIMER</b>                        |                                                                                                                                                                |                |
| p.307                                                  | Modification of <b>Figure 8-5. 12-bit Interval Timer Operation Timing (ITMCMP11 to ITMCMP0 = 0FFH, count clock: f<sub>SUB</sub> = 32.768 kHz)</b>              | (a, b)         |
| <b>CHAPTER 9 CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER</b> |                                                                                                                                                                |                |
| p.314                                                  | Addition of <b>9.3.3 Port mode registers 5, 14 (PM5, PM14)</b>                                                                                                 | (b)            |
| p.315                                                  | Addition of <b>9.5 Cautions of clock output/buzzer output controller</b>                                                                                       | (c)            |

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(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents

(4/10)

| Page                             | Description                                                                                                                                                             | Classification |
|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| <b>CHAPTER 10 WATCHDOG TIMER</b> |                                                                                                                                                                         |                |
| p.316, 322                       | Modification of description in 10.1 Functions of Watchdog Timer, 10.4.4 Setting watchdog timer interval interrupt                                                       | (b)            |
| <b>CHAPTER 11 A/D CONVERTER</b>  |                                                                                                                                                                         |                |
| p.324                            | Modification of Figure 11-1. Block Diagram of A/D Converter                                                                                                             | (a)            |
| p.326                            | Modification of error in 11.2 (9) AV <sub>REFP</sub> pin                                                                                                                | (a)            |
| p.328                            | Modification of caution 1 in 11.3.1 Peripheral enable register 0 (PER0)                                                                                                 | (c)            |
| p.329                            | Modification of cautions 1 and 3 and addition of caution 2 in 11.3.2 A/D converter mode register 0 (ADM0)                                                               | (b)            |
| p.330                            | Modification of Table 11-1. Settings of ADCS and ADCE Bits                                                                                                              | (b)            |
| p.331, 332                       | Modification of description and addition of note 2 and caution 4 to Figure 11-4. Timing Chart When A/D Voltage Comparator Is Used                                       | (b)            |
| p.333 to 336                     | Modification of Table 11-3. A/D Conversion Time Selection                                                                                                               | (c)            |
| p.338                            | Modification of cautions 1, 2 and addition of caution 3 in 11.3.3 A/D converter mode register 1 (ADM1)                                                                  | (c)            |
| p.339                            | Modification of description and cautions 1 to 3 and addition of note in Figure 11-7. Format of A/D Converter Mode register 2 (ADM2) (1/2)                               | (c)            |
| p.340                            | Modification of caution and addition of note and remark in Figure 11-7. Format of A/D Converter Mode register 2 (ADM2) (2/2)                                            | (c)            |
| p.341, 342                       | Addition of note to 11.3.5 10-bit A/D conversion result register (ADCR), and 11.3.6 8-bit A/D conversion result register (ADCRH)                                        | (c)            |
| p.343, 344                       | Modification of caution 5 and addition of cautions 9, 10 in 11.3.7 Analog input channel specification register (ADS)                                                    | (c)            |
| p.345                            | Addition of caution to 11.3.10 A/D test register (ADTES)                                                                                                                | (c)            |
| p.345                            | Addition of caution 3 to 11.3.11 A/D port configuration register (ADPC)                                                                                                 | (c)            |
| p.346                            | Addition of caution to 11.3.12 Port mode control registers 1, 4, 12, 14 (PMC1, PMC4, PMC12, PMC14)                                                                      | (c)            |
| p.347                            | Modification of description and addition of caution to 11.3.13 Port mode register 1, 4, 12, 14 (PM1, PM4, PM12, PM14)                                                   | (c)            |
| p.349                            | Addition of note 1 to 11.4 A/D Converter Conversion Operations                                                                                                          | (c)            |
| p.359 to 361, 363                | Modification of Figures 11-26 to 11-28, 11-30                                                                                                                           | (c)            |
| p.362                            | Modification from 11.7.4 Setup when using temperature sensor (~) to 11.7.4 Setup when temperature sensor output/internal reference voltage output is selected (~)       | (b)            |
|                                  | Modification from Figure 11-29. Setup When Using Temperature Sensor to Figure 11-29. Setup when temperature sensor output/internal reference voltage output is selected | (b)            |
| p.364, 365                       | Modification of description in 11.8 SNOOZE Mode Function                                                                                                                | (c)            |
| p.370                            | Addition of caution to 11.10 (2) Input range of ANI0 to ANI14 and ANI16 to ANI26 pins                                                                                   | (c)            |
| p.373                            | Modification of value in Table 11-6. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)                                                         | (b)            |

**Remark** "Classification" in the above table classifies revisions as follows.

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| Page                                                                                       | Description                                                                                                                                          | Classification |
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| <b>CHAPTER 12 SERIAL ARRAY UNIT</b>                                                        |                                                                                                                                                      |                |
| p.374                                                                                      | Modification of description and addition of <b>note 1</b> to <b>12.1.1 3-wire serial I/O (CSI00, CSI01)</b>                                          | (c)            |
| p.386                                                                                      | Modification of description in <b>Figure 12-6. Format of Serial Communication Operation Setting Register mn (SCRmn)</b>                              | (c)            |
| p.392                                                                                      | Modification of <b>note</b> to <b>Figure 12-10. Format of Serial Channel Start Register m (SSm)</b>                                                  | (c)            |
| p.393                                                                                      | Modification of <b>note</b> to <b>Figure 12-11. Format of Serial Channel Stop Register m (STm)</b>                                                   | (c)            |
| p.396                                                                                      | Modification of <b>Figure 12-14. Format of Serial Output Register m (SOM)</b>                                                                        | (b)            |
| p.398                                                                                      | Modification of description in <b>Figure 12-16. Format of Serial Standby Control Register m (SSCm)</b>                                               | (c)            |
| p.402                                                                                      | Modification of description in <b>12.3.18 Port output mode register 1 (POM1)</b>                                                                     | (c)            |
| p.403                                                                                      | Addition of description to <b>12.3.19 Port mode register 1 (PM1)</b>                                                                                 | (a)            |
| p.406                                                                                      | Modification of <b>note 1</b> in <b>12.5 Operation of 3-Wire Serial I/O (CSI00, CSI01) Communication</b>                                             | (c)            |
| p.407                                                                                      | Modification of description in <b>12.5.1 Master transmission</b>                                                                                     | (c)            |
| p.410 to 412, 420, 421, 429 to 431, 439 to 441, 449, 450, 456 to 458, 476 to 478, 486, 487 | Modification of description in <b>Figure 12-25 to 27, 33 to 35, 41 to 43, 49 to 51, 57 to 59, 63 to 65, 76 to 78, 84 to 86 (operation procedure)</b> | (a)            |
| p.413, 415, 424, 432, 434, 442, 444, 451, 459, 461                                         | Modification of <b>Figure 12-28, 30, 38, 44, 46, 52, 54, 60, 66, 68 (timing chart)</b>                                                               | (a)            |
| p.417                                                                                      | Modification of description in <b>12.5.2 Master reception</b>                                                                                        | (c)            |
| p.426                                                                                      | Modification of description in <b>12.5.3 Master transmission/reception</b>                                                                           | (c)            |
| p.436, 446, 453                                                                            | Modification of <b>note</b> to <b>12.5.4 Slave transmission, 12.5.5 Slave reception, 12.5.6 Slave transmission/reception</b>                         | (c)            |
| p.463                                                                                      | Modification of description in <b>12.5.7 SNOOZE mode function</b>                                                                                    | (c)            |
| p.464, 466                                                                                 | Modification of <b>caution</b> in <b>Figures 12-70 and 12-72</b>                                                                                     | (c)            |
| p.473, 483                                                                                 | Modification of description in <b>12.6.1 UART transmission and 12.6.2 UART reception</b>                                                             | (a)            |
| p.480, 482                                                                                 | Modification of <b>Figure 12-80, 82 (flow chart)</b>                                                                                                 | (a)            |
| p.484                                                                                      | Modification of <b>Figure 12-83 (Example of Contents of Registers)</b> .                                                                             | (a)            |
| p.489                                                                                      | Modification of <b>Figure 12-88. Flowchart of UART Reception</b>                                                                                     | (c)            |
| p.490                                                                                      | Addition of description in <b>12.6.3 SNOOZE mode function</b>                                                                                        | (c)            |
| p.490                                                                                      | Modification of <b>note</b> and <b>caution</b> in <b>Figure 12-89. Timing Chart of SNOOZE Mode Operation (Normal operation mode)</b>                 | (c)            |
| p.491                                                                                      | Modification of <b>caution</b> in <b>Figure 12-90. Timing Chart of SNOOZE Mode Operation (Abnormal Operation &lt;1&gt;)</b>                          | (c)            |
| p.492                                                                                      | Modification of <b>Figure 12-91. Flowchart of SNOOZE Mode Operation (Normal Operation/Abnormal Operation &lt;1&gt;)</b>                              | (c)            |
| p.493                                                                                      | Modification of <b>note 1</b> and <b>caution 1</b> in <b>Figure 12-92. Timing Chart of SNOOZE Mode Operation (Abnormal Operation &lt;2&gt;)</b>      | (c)            |

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| Page                                                          | Description                                                                                                                                                                                   | Classification |
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| p.494                                                         | Modification of <b>Figure 12-93. Flowchart of SNOOZE Mode Operation (Abnormal Operation &lt;2&gt;)</b>                                                                                        | (c)            |
| p.501, 504, 509                                               | Modification of description and <b>note</b> in <b>12.7.1 LIN transmission</b> and <b>12.7.2 LIN reception</b>                                                                                 | (c)            |
| p.502                                                         | Modification of <b>Figure 12-97. Master Transmission Operation of LIN</b>                                                                                                                     | (c)            |
| p.503                                                         | Modification of <b>Figure 12-98. Flowchart for LIN Transmission</b>                                                                                                                           | (c)            |
| p.505                                                         | Modification of <b>Figure 12-99. Reception Operation of LIN</b>                                                                                                                               | (c)            |
| p.506                                                         | Modification of <b>Figure 12-100. Flowchart for LIN Reception</b>                                                                                                                             | (c)            |
| <b>CHAPTER 13 SERIAL INTERFACE IICA</b>                       |                                                                                                                                                                                               |                |
| p.527                                                         | Modification of <b>Figure 13-9. Format of IICA Control Register n1 (IICCTLn1) (2/2)</b>                                                                                                       | (c)            |
| p.544                                                         | Modification of <b>13.5.13 Wakeup function</b>                                                                                                                                                | (c)            |
| p.566                                                         | Modification of <b>13.5.17 (2) (d) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop</b>                                                                                                 | (c)            |
| p.570                                                         | Modification of <b>13.5.17 (3) (d) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop</b>                                                                                                    | (c)            |
| <b>CHAPTER 14 LCD CONTROLLER/DRIVER</b>                       |                                                                                                                                                                                               |                |
| p.604                                                         | Modification of <b>Table 14-1. Number of LCD Display Function Pins of Each Product</b>                                                                                                        | (c)            |
| p.608                                                         | Modification of <b>Table 14-4. Combinations of Display Waveform, Time Slices, and Bias Method</b>                                                                                             | (c)            |
| p.609                                                         | Addition of <b>notes 1, 3</b> to <b>Figure 14-4. Format of LCD Mode Register 1 (LCDM1) (1/2)</b>                                                                                              | (c)            |
| p.610                                                         | Modification of <b>note</b> and <b>caution 1</b> in <b>Figure 14-4. Format of LCD Mode Register 1 (LCDM1) (2/2)</b>                                                                           | (c)            |
| p.611                                                         | Modification of <b>cautions 1, 3</b> in <b>Figure 14-5. Format of Operation Speed Mode Control Register (OSMC)</b>                                                                            | (c)            |
| p.612                                                         | Modification of description and <b>cautions 2, 4</b> in <b>Figure 14-6. Format of LCD Clock Control Register 0 (LCDC0) (1/2)</b>                                                              | (c)            |
| p.613                                                         | Modification of description and <b>cautions 2, 3</b> in <b>Figure 14-6. Format of LCD Clock Control Register 0 (LCDC0) (2/2)</b>                                                              | (c)            |
| p.615                                                         | Modification of <b>Table 14-5. Output Setting of COM4/COMEXP/SEG0, COM5/SEG1, COM6/SEG2, and COM7/SEG3 Pins</b>                                                                               | (c)            |
| p.632                                                         | Modification of <b>caution 1</b> in <b>Figure 14-23. Operation Stop Procedure</b>                                                                                                             | (c)            |
| p.634                                                         | Modification of <b>caution</b> in <b>Figure 14-24. Examples of LCD Drive Power Connections (External Resistance Division Method)</b>                                                          | (c)            |
| p.635                                                         | Modification of <b>Figure 14-25. Examples of LCD Drive Power Connections (Internal Voltage Boosting Method)</b>                                                                               | (a)            |
| p.636                                                         | Modification of <b>Figure 14-26. Examples of LCD Drive Power Connections (Capacitor Split Method)</b>                                                                                         | (a)            |
| p.647                                                         | Modification of <b>Figure 14-31. Static LCD Drive Waveform Examples for SEG11, SEG12, and COM0</b>                                                                                            | (c)            |
| p.663                                                         | Addition of <b>remark</b> to <b>Figure 14-45. LCD Drive Waveform Examples of Memory-Type Liquid Crystal Waveform (3-Time-Slice, 1/3 Bias Method)</b>                                          | (c)            |
| <b>CHAPTER 15 MULTIPLIER AND DIVIDER/MULTIPLY-ACCUMULATOR</b> |                                                                                                                                                                                               |                |
| p.666                                                         | Modification of <b>Figure 15-1. Block Diagram of Multiplier and Divider/Multiply-Accumulator</b>                                                                                              | (a)            |
| p.667                                                         | Modification of <b>Table 15-2. Functions of MDAH and MDAL Registers During Operation Execution</b>                                                                                            | (c)            |
| p.668                                                         | Modification of <b>caution 1</b> to <b>15.2.2 Multiplication/division data register B (MDBL, MDBH)</b> and <b>Table 15-3. Functions of MDBH and MDBL Registers During Operation Execution</b> | (c)            |

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| Page                                     | Description                                                                                                                                                                                                                   | Classification |
|------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| p.669                                    | Modification of <b>caution 2</b> to <b>15.2.3 Multiplication/division data register C (MDCL, MDCH)</b> and <b>Table 15-4. Functions of MDCH and MDCL Registers During Operation Execution</b>                                 | (c)            |
| p.671                                    | Modification of description in <b>Figure 15-5. Format of Multiplication/Division Control Register (MDUC)</b>                                                                                                                  | (a, c)         |
| p.673                                    | Modification of description in <b>15.4.1 Multiplication (unsigned) operation</b> , and modification of value in <b>Figure 15-6. Timing Diagram of Multiplication (Unsigned) Operation (<math>2 \times 3 = 6</math>)</b>       | (a)            |
| p.674                                    | Modification of description in <b>15.4.2 Multiplication (signed) operation</b> , and modification of value in <b>Figure 15-7. Timing Diagram of Multiplication (Signed) Operation (<math>-2 \times 32767 = -65534</math>)</b> | (a)            |
| p.675                                    | Modification of description in <b>15.4.3 Multiply-accumulation (unsigned) operation</b>                                                                                                                                       | (a)            |
| p.676                                    | Modification of value in <b>Figure 15-8. Timing Diagram of Multiply-Accumulation (Unsigned) Operation</b>                                                                                                                     | (c)            |
| p.677                                    | Addition of description to <b>15.4.4 Multiply-accumulation (signed) operation</b>                                                                                                                                             | (c)            |
| p.678                                    | Modification of value in <b>Figure 15-9. Timing Diagram of Multiply-Accumulation (signed) Operation</b>                                                                                                                       | (b, c)         |
| p.679                                    | Modification of description in <b>15.4.5 Division operation</b>                                                                                                                                                               | (c)            |
| p.680                                    | Modification of value in <b>Figure 15-10. Timing Diagram of Division Operation (Example: <math>35 \div 6 = 5</math>, Remainder 5)</b>                                                                                         | (c)            |
| <b>CHAPTER 17 INTERRUPT FUNCTION</b>     |                                                                                                                                                                                                                               |                |
| p.702                                    | Addition of description                                                                                                                                                                                                       | (c)            |
| p.712                                    | Deletion of <b>caution 2</b> in <b>Figure 17-2. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H, IF2L) (64-pin)</b>                                                                                        | (c)            |
| p.721                                    | Modification of <b>Figure 17-8. Interrupt Request Acknowledgment Timing (Minimum Time)</b> and <b>Figure 17-9. Interrupt Request Acknowledgment Timing (Maximum Time)</b>                                                     | (c)            |
| p.723                                    | Modification of <b>Table 17-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing</b>                                                                                | (c)            |
| p.726                                    | Deletion of <b>caution</b> in <b>17.4.4 Interrupt request hold</b>                                                                                                                                                            | (c)            |
| <b>CHAPTER 18 KEY INTERRUPT FUNCTION</b> |                                                                                                                                                                                                                               |                |
| Though out                               | Modification of all                                                                                                                                                                                                           | (c)            |
| <b>CHAPTER 19 STANDBY FUNCTION</b>       |                                                                                                                                                                                                                               |                |
| p.735                                    | Modification <b>caution 1</b> in <b>19.1.1 Standby function</b>                                                                                                                                                               | (a)            |
| p.740, 741                               | Modification of <b>Table 19-1. Operating Statuses in HALT Mode</b>                                                                                                                                                            | (a)            |
| p.742                                    | Addition of <b>note 1</b> in <b>Figure 19-3. HALT Mode Release by Interrupt Request Generation</b>                                                                                                                            | (c)            |
| p.743, 744                               | Modification of description in <b>Figure 19-4. HALT Mode Release by Reset</b>                                                                                                                                                 | (c)            |
| p.744                                    | Modification of <b>caution 1</b> in <b>19.3.2 (1) STOP mode setting and operating statuses</b>                                                                                                                                | (c)            |
| p.745, 746                               | Modification of description and deletion of <b>caution 1</b> in <b>Table 19-2. Operating Statuses in STOP Mode</b>                                                                                                            | (c)            |
| p.746, 747                               | Modification of description in <b>Figure 19-5. STOP Mode Release by Interrupt Request Generation</b>                                                                                                                          | (c)            |
| p.748                                    | Modification of description in <b>Figure 19-6. STOP Mode Release by Reset</b>                                                                                                                                                 | (c)            |
| p.749                                    | Modification of description in <b>19.3.3 (1) SNOOZE mode setting and operating statuses</b>                                                                                                                                   | (c)            |
| p.750                                    | Modification of description in <b>Table 19-3. Operating Statuses in SNOOZE Mode</b>                                                                                                                                           | (c)            |

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| Page                                     | Description                                                                                                                                                                  | Classification |
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| <b>CHAPTER 20 RESET FUNCTION</b>         |                                                                                                                                                                              |                |
| p.751                                    | Modification of <b>caution 3</b> in <b>CHAPTER 20 RESET FUNCTION</b>                                                                                                         | (c)            |
| p.753                                    | Modification of description in <b>Figure 20-2</b>                                                                                                                            | (c)            |
| p.753, 754                               | Modification and addition of <b>caution 2</b> to <b>Figure 20-3</b>                                                                                                          | (c)            |
| p.754                                    | Deletion of <b>Figure 20-4</b>                                                                                                                                               | (c)            |
| p.755                                    | Modification of port (latch) in <b>Table 20-1. Operation Statuses During Reset Period</b>                                                                                    | (c)            |
| p.756                                    | Modification of description of high-speed on-chip oscillator trimming register (HIOTRM) and <b>note 2</b> in <b>Table 20-2. Hardware Statuses After Reset Acknowledgment</b> | (c)            |
| p.760                                    | Modification of <b>note 2</b> in <b>Table 20-2. Hardware Statuses After Reset Acknowledgment (4/4)</b>                                                                       | (c)            |
| p.761                                    | Modification of <b>caution 2</b> in <b>Figure 20-5. Format of Reset Control Flag Register (RESF)</b>                                                                         | (c)            |
| <b>CHAPTER 21 POWER-ON-RESET CIRCUIT</b> |                                                                                                                                                                              |                |
| p.763                                    | Modification of description in <b>21.1 Functions of Power-on-reset Circuit</b>                                                                                               | (c)            |
| p.764                                    | Modification of description in <b>21.3 Operation of Power-on-reset Circuit</b>                                                                                               | (c)            |
| p.765 to 767                             | Modification of description and <b>notes</b> in <b>Figure 21-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector</b>             | (c)            |
| <b>CHAPTER 22 VOLTAGE DETECTOR</b>       |                                                                                                                                                                              |                |
| p.771                                    | Modification of <b>Figure 22-1. Block Diagram of Voltage Detector</b>                                                                                                        | (a)            |
| p.772                                    | Modification of <b>notes 1, 3</b> in <b>Figure 22-2. Format of Voltage Detection Register (LVIM)</b>                                                                         | (a)            |
| p.774, 775                               | Addition of <b>Table 22-1. LVD Operation Mode and Detection Voltage Settings for User Option Byte (000C1H)</b>                                                               | (a)            |
| p.776                                    | Modification of <b>22.4.1 When used as reset mode</b>                                                                                                                        | (c)            |
| p.778                                    | Modification of <b>22.4.2 When used as interrupt mode</b>                                                                                                                    | (c)            |
| p.780                                    | Modification of description in <b>22.4.3 When used as interrupt and reset mode</b>                                                                                           | (c)            |
| p.781, 782                               | Modification of <b>figure 22-6 (1/2)</b>                                                                                                                                     | (c)            |
| p.783, 784                               | Modification of <b>figure 22-6 (2/2)</b>                                                                                                                                     | (c)            |
| <b>CHAPTER 23 SAFETY FUNCTIONS</b>       |                                                                                                                                                                              |                |
| p.787                                    | Modification of <b>remark</b> in <b>23.1 Overview of Safety Functions</b>                                                                                                    | (c)            |
| p.788                                    | Addition of description and <b>caution 2</b> to <b>23.3.1 Flash memory CRC operation function (high-speed CRC)</b>                                                           | (c)            |
| p.791                                    | Modification of <b>Figure 23-3. Flowchart of Flash Memory CRC Operation Function (High-speed CRC)</b>                                                                        | (b)            |
| p.792                                    | Addition of description and <b>caution</b> to <b>23.3.2 CRC operation function (general-purpose CRC)</b>                                                                     | (c)            |
| p.793                                    | Modification of <b>Figure 23-6. CRC Operation Function (General-Purpose CRC)</b>                                                                                             | (a)            |
| p.794                                    | Modification of <b>caution</b> in <b>Figure 23-7. Format of RAM Parity Error Control Register (RPECTL)</b>                                                                   | (c)            |
| p.797                                    | Modification of <b>Figure 23-10. Invalid access detection area</b>                                                                                                           | (c)            |
| p.801                                    | Addition of description to <b>23.3.8 A/D test function</b>                                                                                                                   | (c)            |
| <b>CHAPTER 24 REGULATOR</b>              |                                                                                                                                                                              |                |
| p.804                                    | Addition of Figure (move from 2.2 Description to Pin Function (preceding editions))                                                                                          | (c)            |

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| <b>CHAPTER 25 OPTION BYTE</b>                       |                                                                                                                                                                   |                |
| p.805                                               | Modification of description in <b>25.1 Functions of Option Bytes</b>                                                                                              | (c)            |
| p.807                                               | Modification of description in <b>Figure 25-1. Format of User Option Byte (000C0H)</b>                                                                            | (b)            |
| p.808, 809                                          | Modification of <b>Figure 25-2. Format of User Option Byte (000C1H)</b>                                                                                           | (a)            |
| <b>CHAPTER 26 FLASH MEMORY</b>                      |                                                                                                                                                                   |                |
| p.816                                               | Deletion of description in <b>26.1.1 Programming Environment</b>                                                                                                  | (a)            |
| p.817                                               | Addition of description to <b>26.2 Writing to Flash Memory by Using External Device (that Incorporates UART)</b>                                                  | (c)            |
| p.819                                               | Addition of <b>remark</b> to <b>26.3 Connection of Pins on Board</b>                                                                                              | (c)            |
| p.822                                               | Addition of description, <b>caution</b> and <b>remark</b> to <b>26.4.1 Data flash overview</b>                                                                    | (c)            |
| p.825                                               | Modification of <b>Figure 26-8. Setting of Flash Memory Programming Mode</b>                                                                                      | (c)            |
| p.826                                               | Modification of error in <b>Table 26-4. Relationship Between TOOL0 Pin and Operation Mode After Reset Release</b>                                                 | (a, c)         |
| p.826                                               | Modification of <b>Table 26-5. Programming Modes and Voltages at Which Data Can Be Written, Erased, or Verified</b>                                               | (c)            |
| p.828                                               | Modification of description in <b>Table 26-10. Example of Signature Data</b>                                                                                      | (a)            |
| p.829                                               | Addition of description and <b>caution</b> to <b>26.6 Security Settings</b>                                                                                       | (a)            |
| p.830                                               | Modification of <b>Table 26-11. Relationship Between Enabling Security Function and Command</b> and <b>Table 26-12. Setting Security in Each Programming Mode</b> | (c)            |
| p.831                                               | Modification of <b>cautions 2 to 4</b> to <b>26.7 Flash Memory Programming by Self-Programming</b>                                                                | (c)            |
| p.831                                               | Modification of <b>Table 26-13. Programming Modes and Voltages at Which Data Can Be Written, Erased, or Verified</b>                                              | (c)            |
| p.833                                               | Modification of <b>Table 26-14. Relationship between Flash Shield Window Function Setting/Change Methods and Commands</b>                                         | (c)            |
| <b>CHAPTER 29 INSTRUCTION SET</b>                   |                                                                                                                                                                   |                |
| p.853                                               | Modification of error in <b>Table 29-5. Operation List (10/17)</b>                                                                                                | (a)            |
| <b>CHAPTER 30 ELECTRICAL SPECIFICATIONS</b>         |                                                                                                                                                                   |                |
| p.861                                               | Addition of <b>cautions 2, 3</b> to <b>CHAPTER 30 ELECTRICAL SPECIFICATIONS</b> (deletion of Pins Mounted According to Product)                                   | (c)            |
| p.862                                               | Addition of description, <b>note 3</b> , and <b>remark 2</b> to <b>30.1 Absolute Maximum Ratings</b>                                                              | (c)            |
| p.863                                               | Modification of description and addition of <b>note</b> to <b>30.1 Absolute Maximum Ratings</b>                                                                   | (c)            |
| p.865, 866                                          | Modification of <b>30.2 Oscillator Characteristics</b>                                                                                                            | (c)            |
| p.871                                               | Modification of <b>30.3.1 Pin characteristics</b>                                                                                                                 | (c)            |
| p.873                                               | Modification of <b>notes 1 to 4</b> in <b>30.3.2 Supply current characteristics</b>                                                                               | (c)            |
| p.875 to 877                                        | Modification of <b>notes 1, 3 to 6, 8</b> to <b>30.3.2 Supply current characteristics</b>                                                                         | (c)            |
| p.879, 880                                          | Addition of description to <b>30.4 AC Characteristics</b>                                                                                                         | (c)            |
| p.881, 883 to 885, 887 to 889, 891 to 895, 897, 898 | Modification of <b>30.5.1 Serial array unit</b>                                                                                                                   | (a, c)         |
| p.900, 901                                          | Modification of <b>30.5.2 Serial interface IICA</b>                                                                                                               | (c)            |

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| p.905 | Modification of <b>30.6.2 Temperature sensor/internal reference voltage characteristics</b>         | (c)            |
| p.907 | Addition of <b>note</b> and <b>caution</b> in <b>30.6.5 Supply voltage rise time</b>                | (c)            |
| p.912 | Modification of <b>30.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics</b> | (c)            |
| p.912 | Modification of conditions in <b>30.9 Timing Specs for Switching Flash Memory Programming Modes</b> | (b)            |
| p.913 | Modification of <b>30.10 Timing Specifications for Switching Flash Memory Programming Modes</b>     | (c)            |

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## A.2 Revision History of Preceding Editions

Here is the revision history of the preceding editions. Chapter indicates the chapter of each edition.

| Edition  | Description                                                                                                                       | Chapter                              |
|----------|-----------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|
| Ver.0.03 | Modification of <b>caution 2</b> in 1.3.5 64-pin products                                                                         | CHAPTER 1 OUTLINE                    |
|          | Modification of <b>I/O port</b> in 1.6 Outline of Functions                                                                       |                                      |
|          | Modification of <b>Function</b> in 2.1.5 64-pin products                                                                          | CHAPTER 2 PIN FUNCTIONS              |
|          | Modification of description in 2.2 Description of Pin Functions                                                                   |                                      |
|          | Modification of 2.2.6 (1) Port mode                                                                                               |                                      |
|          | Modification of <b>Table 2-3. Connection of Unused Pins (64-pin products)</b>                                                     |                                      |
|          | Modification of <b>Figure 2-1. Pin I/O Circuit List</b>                                                                           |                                      |
|          | Modification of <b>Table 3-5. SFR List</b>                                                                                        | CHAPTER 3 CPU ARCHITECTURE           |
|          | Modification of 4.3 (5) Port output mode register (POM1)                                                                          | CHAPTER 4 PORT FUNCTIONS             |
|          | Modification of 4.4.4 Connecting to external device with different potential (1.8 V, 2.5 V, 3 V)                                  |                                      |
|          | Addition of <b>cautions 6, 7</b> to Figure 6-79. Procedure for Setting Remote control Output                                      | CHAPTER 6 TIMER ARRAY UNIT           |
|          | Modification of <b>Figure 12-14. Format of Serial Output Register m (S0m)</b>                                                     | CHAPTER 12 SERIAL ARRAY UNIT         |
|          | Modification of <b>Figure 12-20. Format of Port Output Mode Register 1 (POM1)</b>                                                 |                                      |
|          | Modification of 14.1 Functions of LCD Controller/Driver                                                                           | CHAPTER 14 LCD CONTROLLER/DRIVER     |
|          | Modification of Figure 14-6. Format of LCD Clock Control Register 0 (LCDC0)                                                       |                                      |
|          | Modification of Figure 14-8. Format of LCD Boost Level Control Register (VLCD)                                                    |                                      |
|          | Modification of Figure 14-41. Four-Time-Slice LCD Drive Waveform Examples Between SEG12 and Each Common Signals (1/3 Bias Method) |                                      |
|          | Modification of Figure 14-44. Eight-Time-Slice LCD Drive Waveform Examples Between SEG4 and Each Common Signals (1/4 Bias Method) |                                      |
|          | Modification of throughout the document                                                                                           | CHAPTER 18 KEY INTERRUPT FUNCTION    |
|          | Modification of 21.3 Operation of Power-on-reset Circuit                                                                          | CHAPTER 21 POWER-ON-RESET CIRCUIT    |
|          | Modification of throughout the document                                                                                           | CHAPTER 30 ELECTRICAL SPECIFICATIONS |
|          | Package drawings are updated.                                                                                                     | CHAPTER 31 PACKAGE DRAWINGS          |

**Remark** "Classification" in the above table classifies revisions as follows.

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