# KSZ9477S EDS2 Daughter Card User Guide

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# Preface

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## INTRODUCTION

This chapter contains general information that will be useful to know before using the KSZ9477S EDS2 Daughter Card User Guide. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- Warranty Registration
- The Microchip Web Site
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

## DOCUMENT LAYOUT

This document features the KSZ9477S EDS2 Daughter Card. The manual layout is as follows:

- **Chapter 1. "Overview"** – This chapter provides an overview of the KSZ9477S EDS2 Daughter Card and a brief description of the card's features.
- **Chapter 2. "Getting Started"** – This chapter provides information on the setup and operation of the KSZ9477S EDS2 Daughter Card.
- **Chapter 3. "Hardware"** – This chapter shows the different connection types found on the KSZ9477S EDS2 Daughter Card.
- **Chapter 4. "System Boot"** – This chapter explains how to use device tree overlays when booting the host system.
- **Appendix A. "Schematics"** – This section shows the schematic drawings of the KSZ9477S EDS2 Daughter Card.
- **Appendix B. "Bill of Materials"** – This section shows the Bill of Materials (BOM) for the KSZ9477S EDS2 Daughter Card.
- **Appendix C. "PCB Layers"** – This section shows the PCB layers of the KSZ9477S EDS2 Daughter Card.

## CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

**DOCUMENTATION CONVENTIONS**

| Description | Represents | Examples |
|---|---|---|
| **Arial font:** | | |
| Italic characters | Referenced books | *MPLAB® IDE User's Guide* |
| | Emphasized text | ...is the *only* compiler... |
| Initial caps | A window | the Output window |
| | A dialog | the Settings dialog |
| | A menu selection | select Enable Programmer |
| Quotes | A field name in a window or dialog | "Save project before build" |
| Underlined, italic text with right angle bracket | A menu path | *File>Save* |
| Bold characters | A dialog button | Click **OK** |
| | A tab | Click the **Power** tab |
| N'Rnnnn | A number in verilog format, where N is the total number of digits, R is the radix and n is a digit. | 4'b0010, 2'hF1 |
| Text in angle brackets < > | A key on the keyboard | Press <Enter>, <F1> |
| **Courier New font:** | | |
| Plain Courier New | Sample source code | `#define START` |
| | Filenames | `autoexec.bat` |
| | File paths | `c:\mcc18\h` |
| | Keywords | `_asm, _endasm, static` |
| | Command-line options | `-Opa+, -Opa-` |
| | Bit values | `0, 1` |
| | Constants | `0xFF, 'A'` |
| Italic Courier New | A variable argument | *`file`*`.o`, where *`file`* can be any valid filename |
| Square brackets [ ] | Optional arguments | `mcc18 [options]` *`file`* `[options]` |
| Curly brackets and pipe character: { \| } | Choice of mutually exclusive arguments; an OR selection | `errorlevel {0\|1}` |
| Ellipses... | Replaces repeated text | `var_name [, var_name...]` |
| | Represents code supplied by user | `void main (void) { ... }` |

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- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PIC-kit 2 and 3.

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## DOCUMENT REVISION HISTORY

| Revisions | Section/Figure/Entry | Correction |
|---|---|---|
| DS50003928A (08-18-25) | Initial release | |

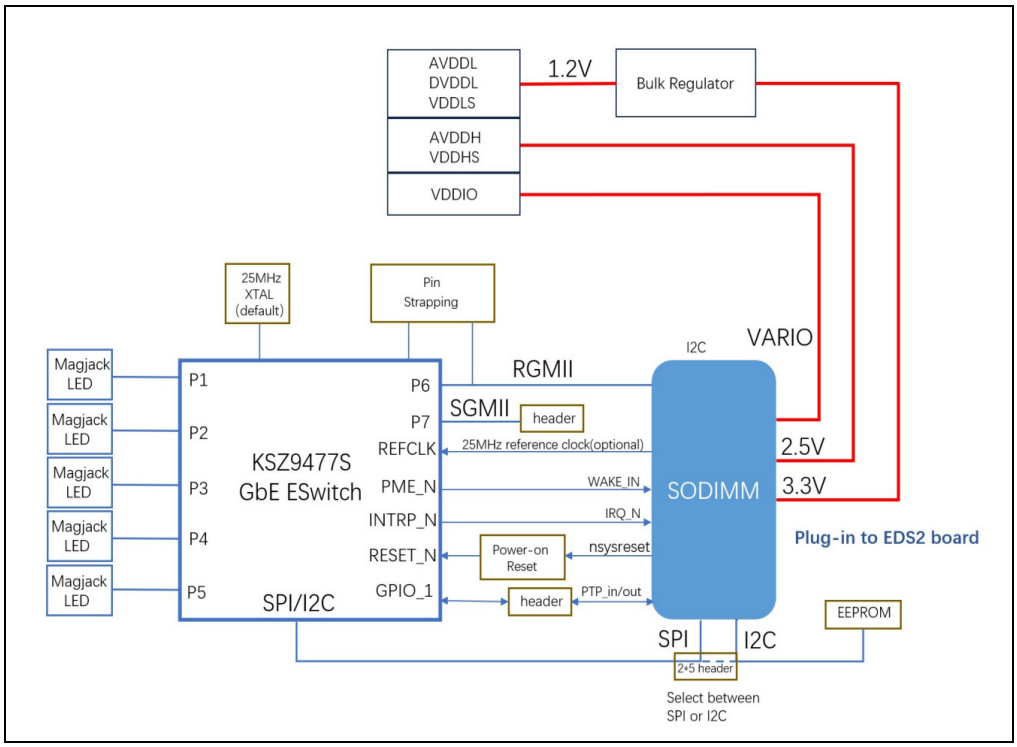
# Chapter 1. Overview

## 1.1 INTRODUCTION

The KSZ9477S is designed for evaluation of the Microchip KSZ9477S Gigabit Ethernet Switch when used with a Microchip EDS2 compatible host board. A SODIMM 260-pin connector for the EDS2 Host - KSZ9477S Interface is used due to its high performance, high pin count, and low cost.

This document describes the KSZ9477S EDS2 Daughter Card setup and user interface features. A simplified block diagram is shown in Figure 1-1.

**FIGURE 1-1: KSZ9477S EDS2 DAUGHTER CARD BLOCK DIAGRAM**



## 1.2 FEATURES

These are the features of the KSZ9477S EDS2 Daughter Card:

- Microchip KSZ9477S Gigabit Ethernet Switch with SGMII and RGMII/MII/RMII
- Microchip VXM7-9013-25M0000 crystal for 25 MHz
- Microchip MIC23303YML-TR 4 MHz Buck PWM regulator for 1.2V generation
- Microchip MIC2790N Reset supervisor with Reset LED indicator
- Microchip 24AA014H $I^2C$ Serial EEPROM for board identification
- Two Dual 10/100/1000 Mb RJ45 Integrated Connector and Magnetics with LEDs
- One Single 10/100/1000 Mb RJ45 Integrated Connector and Magnetics with LEDs
- 1x5-pin SGMII header
- Selectable SPI or $I^2C$ Management interface
- Compliant with the SODIMM EDS2 Interface Specification with RGMII interface to the Host processor
- SPST switch for Reset
- Green LED indicator for 1.2V
- Test points for power rails and GND
- Configurable GPIO pins for IEEE1588 (Precision Time Protocol) timestamp capture input or event trigger output

## 1.3 REFERENCES

Concepts and materials available in the following documents may be helpful when reading this document. Visit the KSZ9477S EDS2 Daughter Card product page at www.microchip.com for the latest documentation.

- *KSZ9477S Data Sheet*
- *KSZ9477S EDS2 Daughter Card Schematics*
- *KSZ9477S Hardware Design Checklist*
- *SAMA7D65 Curiosity Rev 2 Schematics*
- *SAMA7D65 Curiosity Rev 2 User's Guide*
- *EDS2 SODIMM IF Development Guide*

## 1.4 ACRONYMS AND DEFINITIONS

Table 1-1 shows the terms used in this user guide.

**TABLE 1-1: ACRONYMS AND DEFINITIONS**

| Term | Definition |
|---|---|
| ARP | Address Resolution Protocol |
| COM | Communications Port |
| DHCP | Dynamic Host Configuration Protocol |
| DIP | Dual In-line Package |
| DSUB | D - Subminiature |
| EP | Extended Page |
| GPIO | General Purpose Input/Output |
| HSR | High-reliability Seamless Redundancy |
| ICM | Integrated Connector Magnetic |
| IEEE | Institute of Electrical and Electronics Engineers |
| I/O | Input/Output |

**TABLE 1-1: ACRONYMS AND DEFINITIONS (CONTINUED)**

| Term | Definition |
|---|---|
| IP | Internet Protocol |
| LAN | Local Area Network |
| LSB | Least Significant Byte/Bit |
| MAC | Media Access Controller |
| MDIO | Management/Data Input/Output |
| MII | Media Independent Interface |
| NIC | Network Interface Card |
| OUI | Organizationally Unique Identifier |
| PC | Personal Computer |
| PCB | Printed Circuit Board |
| PCS | Physical Coding Sublayer |
| PDU | Payload Data Unit |
| PHY | Physical Layer Transceiver |
| PN | Part Number |
| PRP | Parallel Redundancy Protocol |
| RGMII | Reduced Gigabit Media Independent Interface |
| SGMII | Serial Gigabit Media Independent Interface |
| QSGMII | Quad Serial Gigabit Media Independent Interface |
| Q-USGMII | Quad Universal Serial Gigabit Media Independent Interface |
| SMA | Sub-Miniature version A |
| SODIMM | Small Outline Dual In-line Memory Module |
| TCXO | Temperature-Compensated Crystal Oscillator |
| TFTP | Trivial File Transfer Protocol |
| UART | Universal Asynchronous Receiver/Transmitter |
| USB | Universal Serial Bus |
| VDFN | Very-small Dual Flat, No Leads |
| VM | Virtual Machine |
| VREG | Voltage Regulator |
| XO | Crystal oscillator |

**NOTES:**

# Chapter 2. Getting Started

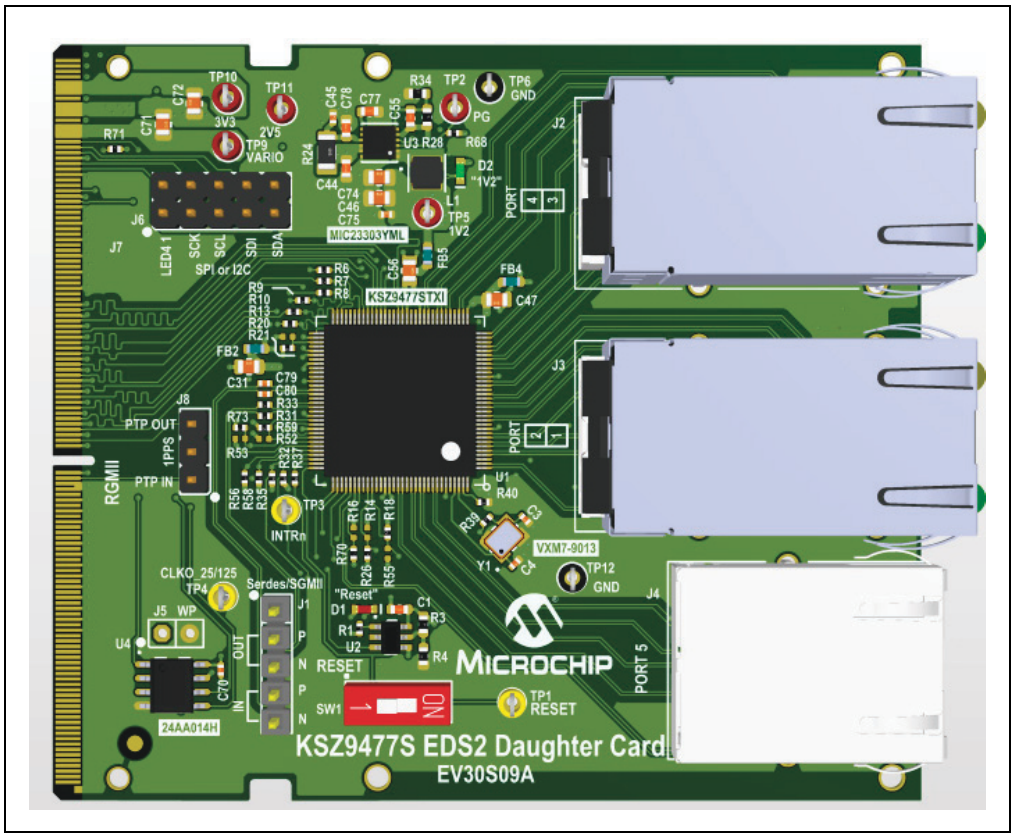
## 2.1 OVERVIEW

This chapter provides a quick start guide for using the KSZ9477S EDS2 Daughter Card. The SAMA7D65 Curiosity (Rev 2) serves as the host board. Refer to the *SAMA7D65 Curiosity User Guide* for the correct jumper configuration.

## 2.2 KSZ9477S INSTALLATION

Figure 2-1 shows the KSZ9477S EDS2 Daughter Card.

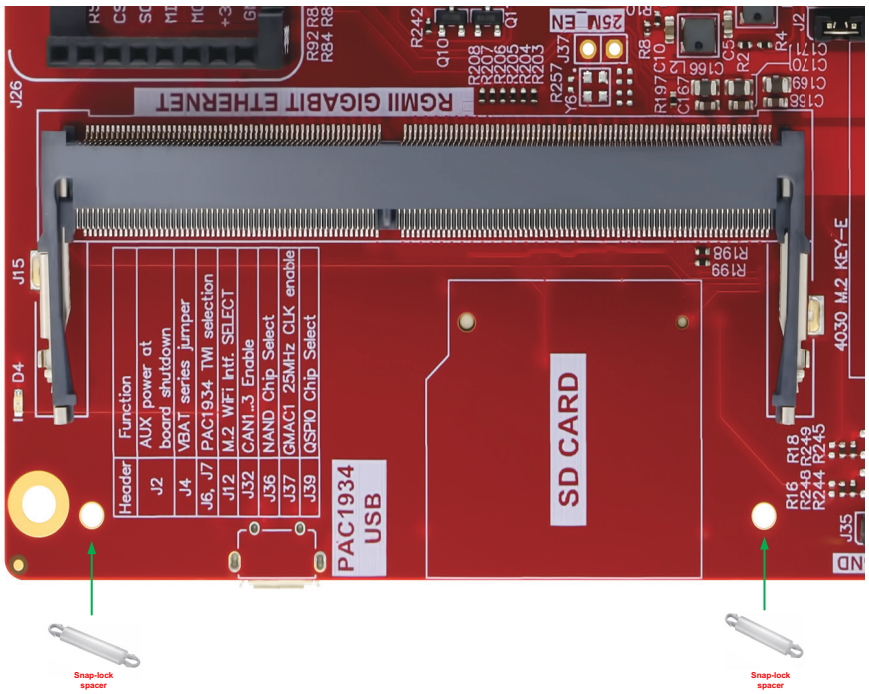
**FIGURE 2-1: KSZ9477S EDS2 DAUGHTER CARD**



Perform the following steps to install the KSZ9477S EDS2 Daughter Card in the EDS2 connector:

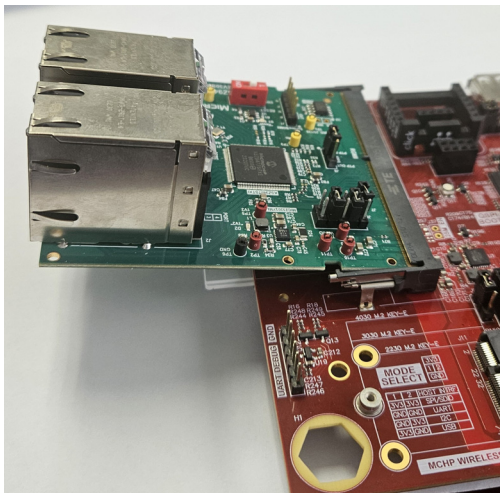
1. Verify that the host board power is OFF.
2. Install the two snap lock spacers (Wurth Elektronik part number 709652500) included in the kit on the SAMA7D65 Curiosity mounting holes for mechanical support. See Figure 2-2.

**FIGURE 2-2: SNAP LOCK SPACERS**



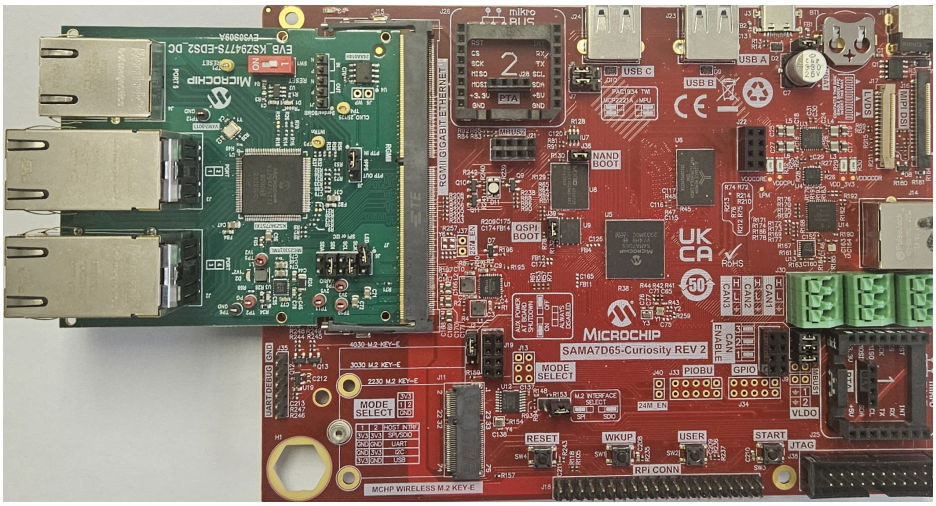

3. Grab the daughter card by its board edges. Align to SODIMM EDS2 receptacle and insert the board fingers' edge at a 45-degree angle into the SODIMM connector as shown in Figure 2-3.

**FIGURE 2-3: KSZ9477S EDS2 DAUGHTER CARD INSTALLATION**



4. Push down the daughter card until it latches into the SODIMM receptacle latches.
5. After installation, the boards should appear as shown in Figure 2-4.

**FIGURE 2-4: KSZ9477S EDS2 DAUGHTER CARD INSTALLED**




6. Connect an Ethernet cable between the Daughter Card's RJ45 port and a link partner device.

**CAUTION**

**Connecting or disconnecting Ethernet cables after powering up the board is not recommended as the board fingers could be disconnected from the SODIMM receptacle and leave the board in an inconsistent state or even cause damage to the board.**

## 2.3 QUICK START

Conduct the following steps to start using the KSZ9477S EDS2 Daughter Card:

1. Verify if the SW1 slide switch is set as shown in Figure 2-5.

**FIGURE 2-5: SW1 SLIDE SWITCH**


2. Insert a programmed microSD card on SAMA7D65 Curiosity microSD card slot J10.
3. Connect an FTDI TTL-232R-3V3 USB cable between J35 of SAMA7D65 and a Windows PC.
4. Power on the SAMA7D65 board by plugging a 5V DC power supply from the AC/DC adapter to J1 of the SAMA7D65 board.
5. See **Chapter 4. "System Boot"** for details of the boot process.

## 2.4 KSZ9477S EDS2 DAUGHTER CARD REMOVAL

Complete the following procedure to remove the KSZ9477S EDS2 Daughter Card from the SODIMM EDS2 receptacle:

1. Verify that the host board power is OFF.
2. Disconnect the RJ45 cables.
3. If snap locks are used, release them from the daughter card. A pair of long-nose pliers can be used to close the latch pins for easy release.
4. Gently pull the SODIMM receptacle arms away from the daughter card. It should snap upwards.
5. Grab the daughter card by its edges and remove it from the SODIMM EDS2 receptacle.

# Chapter 3. Hardware

## 3.1 INTRODUCTION

This chapter provides a description of the KSZ9477S hardware, including the headers, test points, LEDs, and switches on the board.

The top side and bottom side of the KSZ9477S EDS2 Daughter Card are shown in Figure 3-1 and Figure 3-2, respectively.

**FIGURE 3-1: KSZ9477S EDS2 DAUGHTER CARD (TOP SIDE)**

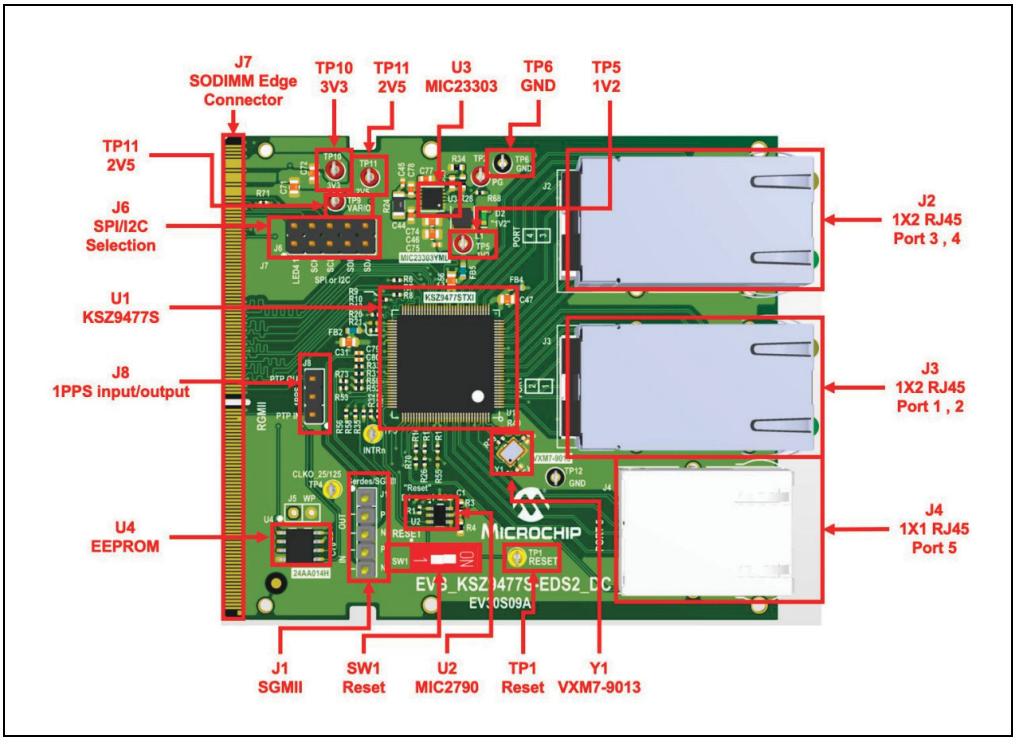
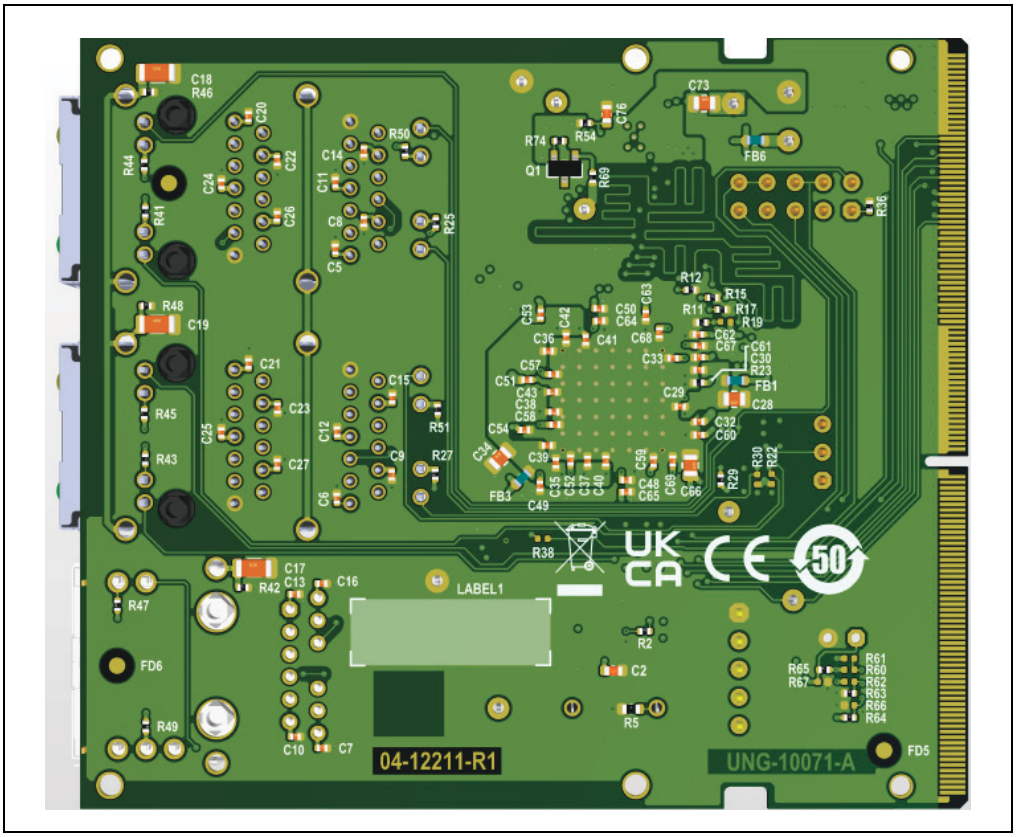


**FIGURE 3-2: KSZ9477S (BOTTOM SIDE)**




## 3.2 CONNECTORS

Table 3-1 describes the connectors on the KSZ9477S EDS2 Daughter Card.

**TABLE 3-1: KSZ9477S EDS2 DAUGHTER CARD CONNECTORS**

| Reference Designator | Name | Description |
|---|---|---|
| J1 | SGMII header 1x5 | Provides access to the SGMII port of the KSZ9477S switch |
| J2 | RJ45 ICM 1x2 | Ethernet RJ45 connector with integrated magnetics for two 1 Gb ports |
| J3 | RJ45 ICM 1x2 | Ethernet RJ45 connector with integrated magnetics for two 1 Gb ports |
| J4 | RJ45 ICM 1x1 | Single-port Ethernet RJ45 connector with integrated magnetics |
| J5 | EEPROM WP header 1x2 | EEPROM write protection (header not installed). Used to disable write protection during EEPROM programming. |
| J6 | SPI/$I^2C$ selection header 2x5 | Used to select between SPI or $I^2C$ management interface from Microchip EDS2 compatible host to KSZ9477S |

**TABLE 3-1: KSZ9477S EDS2 DAUGHTER CARD CONNECTORS**

| Reference Designator | Name | Description |
|---|---|---|
| J7 | SODIMM-260 pin Edge Connector | Provides power and signals for operation. Connects to Microchip EDS2 compatible host. |

## 3.3 TEST POINTS

Table 3-2 lists the test points on the KSZ9477S EDS2 Daughter Card.

**TABLE 3-2: KSZ9477S EDS2 DAUGHTER CARD TEST POINTS**

| Test Point | Color | Description |
|---|---|---|
| TP1 | Yellow | RESET_SW |
| TP2 | Red | 1V2 power good |
| TP3 | Yellow | INTR_N |
| TP4 | Yellow | CLKO_25_125 |
| TP5 | Red | 1V2 |
| TP6 | Black | GND |
| TP9 | Red | VARIO |
| TP10 | Red | 3V3 |
| TP11 | Red | 2V5 |
| TP12 | Black | GND |

## 3.4 LEDS

Table 3-3 details the LEDS on the KSZ9477S EDS2 Daughter Card.

**TABLE 3-3: KSZ9477S EDS2 DAUGHTER CARD LEDS**

| Reference Designator | Name | Description |
|---|---|---|
| D1 | RESET | Red LED RESET indicator |
| D2 | 1V2 | Green LED 1V2 indicator |
| J3A - Left | RJ45 Port 1 - Left | Green LED connected to KSZ9477S LED1_1 |
| J3A - Right | RJ45 Port 1 - Right | Yellow LED connected to KSZ9477S LED1_0 |
| J3B - Left | RJ45 Port 2 - Left | Green LED connected to KSZ9477S LED2_1 |
| J3B - Right | RJ45 Port 2 - Right | Yellow LED connected to KSZ9477S LED2_0 |
| J2A - Left | RJ45 Port 3 - Left | Green LED connected to KSZ9477S LED3_1 |
| J2A - Right | RJ45 Port 3 - Right | Yellow LED connected to KSZ9477S LED3_0 |
| J2B - Left | RJ45 Port 4 - Left | Green LED connected to KSZ9477S LED4_1 |
| J2B - Right | RJ45 Port 4 - Right | Yellow LED connected to KSZ9477S LED4_0 |
| J4 - Left | RJ45 Port 5 - Left | Green LED connected to KSZ9477S LED5_1 |
| J4 - Right | RJ45 Port 5 - Right | Yellow LED connected to KSZ9477S LED5_0 |

## 3.5 CONFIGURATION STRAPS

Table 3-4 shows the configuration straps on the KSZ9477S EDS2 Daughter Card.

**TABLE 3-4: KSZ9477S EDS2 DAUGHTER CARD CONFIGURATION STRAP**

| Reference Designator PU/PD | Name | Description |
|---|---|---|
| R14/R26* | Quite Wire Filtering | 0 – Enable, 1* – Disable |
| R18/R55* | Flow Control | 0 – Disable 1* – Enable |
| R30/R58* | Link-up mode | 0 – Fast Link-up<br>1* – Normal Link-up |
| R52/R59* | Auto-negotiation bit 1 | 0 0 – Reserved<br>0 1 – Auto-negotiation Disabled<br>1 0 – Test Mode<br>1 1* – Auto- negotiation Enabled |
| R22/R56* | Auto-negotiation bit 0 | |
| R36 (note 3) | Management I/F Bit 1 | Management I/F [1:0]<br>0 0 – MIIM<br>0 1 – $I^2C$*<br>1 X – SPI* |
| R53/R73* | Management I/F Bit 0 | |

**Note 1:** Only one of the two PU/PD resistors is installed.

**2:** * indicates default.

**3:** See **Section 3.6 "Management Interface Selection"** for more configurations for the management interface.

**TABLE 3-4: KSZ9477S EDS2 DAUGHTER CARD CONFIGURATION STRAP**

| Reference Designator PU/PD | Name | Description |
|---|---|---|
| R16/R70* | SW_EN | 0 – Switch disabled at startup<br>1* – Switch enabled at startup |
| R20/R21* | IBA | 0 – Disable In-Band Management*<br>1 – Enable In-Band Management |
| R19/R11* | Port 6 Speed Select | 0* – 1000 Mbps Mode 1 – 100 Mbps Mode |
| R12* | Port 6 Mode Bit 1 | Port 6 Mode [1:0]<br>00 – RGMII*<br>01 – RMII<br>10 – Reserved<br>11 – MII |
| R15* | Port 6 Mode Bit 0 | |

**Note 1:** Only one of the two PU/PD resistors is installed.

**2:** * indicates default.

**3:** See **Section 3.6 "Management Interface Selection"** for more configurations for the management interface.

## 3.6 MANAGEMENT INTERFACE SELECTION

The management interface types supported by KSZ9477S include SPI, $I^2C$, and MIIM which are determined by two strapping bits as shown in Table 3-5:

**TABLE 3-5: STRAPPING PINS TO SELECT MANAGEMENT INTERFACE**

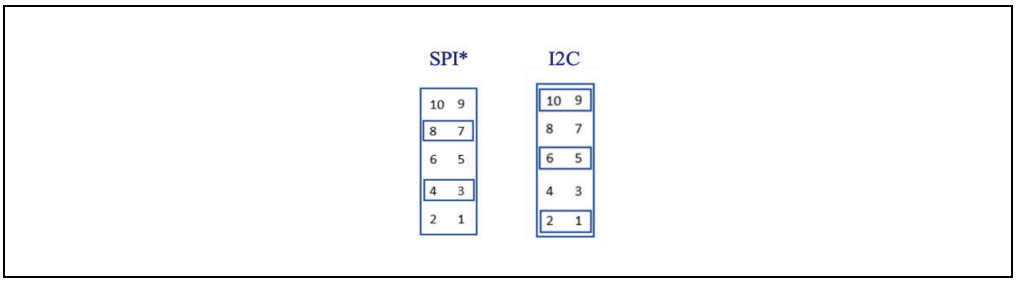
| Reference Designator | Name | Description |
|---|---|---|
| R36 and J6 | Management I/F Bit 1 | Management I/F [1:0]<br>00 – MIIM<br>01 – $I^2C$*<br>1X – SPI* |
| R53/R73* | Management I/F Bit 0 | |

R73 is installed by default, so Management I/F Bit 0 is set to 1. Therefore, $I^2C$ or SPI can be further determined by Management I/F Bit 1. In this design, Management I/F Bit 1 is connected to pin 2 of J6 and pin 1, and J6 is connected to R36 and then to GND. Shorting pin 1 and 2 results in Management I/F Bit 1 being low, allowing $I^2C$ mode selection. Leaving pin 1 and 2 open results in Management I/F Bit 1 being high by default, allowing SPI mode selection. Figure 3-3 shows the jumper placement for selecting either SPI or $I^2C$ mode.

Short pins 3, 4, 7, and 8 of J6 to select SPI mode.

Short pins 1, 2, 5, 6, 9, and 10 of J6 to select $I^2C$ mode.

**FIGURE 3-3: JUMPER PLACEMENT TO SELECT MANAGEMENT INTERFACE**

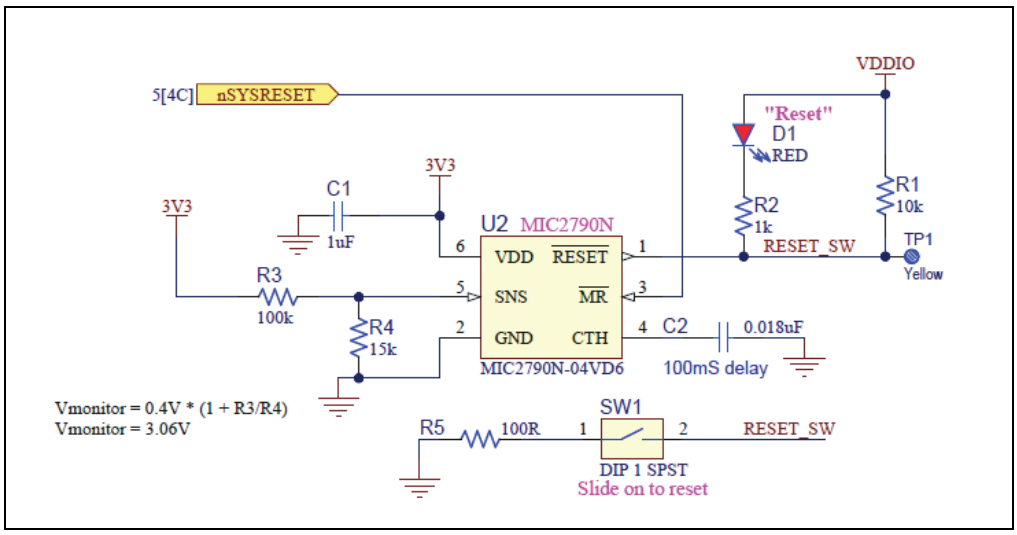



MIIM mode is not supported on the KSZ9477S EDS2 Daughter Card.

## 3.7 RESET

The KSZ9477S includes a Reset circuit using the Microchip MIC2790N Reset supervisor as shown in Figure 3-4. The system Reset signal, **nSYSRESET,** is driven from the SODIMM EDS2 host interface and is connected to the MIC2790 master Reset input MR. When MR goes low, the MIC2790N Reset output on net **RESET_SW** goes low, resetting the KSZ9477S and turning on the Reset LED D1. The **RESET_SW** net goes high 100 milliseconds after **nSYSRESET** goes high, turning off the Reset LED and releasing the KSZ9477S from Reset. The configuration straps are sampled when **RESET_SW** goes high.

**FIGURE 3-4: KSZ9477S EDS2 DAUGHTER CARD RESET CIRCUIT**




The DIP Switch (SW1), as shown in Figure 3-4, can be used to place the KSZ9477S in Reset without affecting the rest of the system. This feature is useful when testing and updating the KSZ9477S Linux® driver after the system has booted up.

## 3.8 CLOCKS

The KSZ9477S EDS2 Daughter Card uses a Microchip VXM7-9013-25M0000 25 MHz crystal for the KSZ9477S clock reference.

The KSZ9477S generates a 25 MHz or 125 MHz clock for Synchronous Ethernet (SyncE) applications.

## 3.9 POWER

The KSZ9477S EDS2 Daughter Card requires 3.3V, 2.5V, and 1.2V. The EDS2 SODIMM EDS2 interface provides 3.3V, 2.5V, and VARIO (3.3V or 2.5V). An on-board Microchip MIC23303YML switching regulator is used to generate the 1.2V required by the KSZ9477S analog, digital core, and PLL power inputs.

## 3.10 KSZ9477S EDS2 DAUGHTER CARD EEPROM

The KSZ9477S includes a Microchip 24AA014H EEPROM with half-array write protection (40H to 7Fh) for identification. Only some locations in the protected area starting at 40h are programmed as shown in Figure 3-5. Details on these fields are specified in Table 3-6.

**FIGURE 3-5: EEPROM CONTENTS**


**TABLE 3-6: EDS2 DAUGHTER CARD EEPROM**

| Byte Address | Name | Type | Description | Value |
|---|---|---|---|---|
| 40 | KEY | INT | Magic number = A3h | A3h |
| 41 | REV | INT | EEPROM Revision | 01h |
| 42 | DCTYPE | INT | Daughter card type: 0 = PHY, 1 = SWITCH | 01h |
| 43 | NPORTS | INT | Number of ports including the host port | 07h |
| 44 | MACIF | INT | MAC interface:<br>RMII 07h<br>RGMII 09h<br>RGMII_ID 0Ah<br>RGMII_RXID 0Bh<br>RGMII_TXID 0Ch<br>SGMII 04h<br>QSGMII 13h | 0Ah |
| 45 | DPN_PNUM | INT | Device part number:[23:20] Product family<br>– KSZ<br>– LAN<br>– VSC | [23:20]=0h=KSZ |
| | | | Device part number:[19:16] Part number | [19:16]=1h=PN0 |
| 46 | | | Device Part number bits [15:8] | [15:08]=94h=PN1 |
| 47 | | | Device Part number bits [7:0] | [7:0]=77h=PN2 |
| 48 | CTRLIF | INT | Control interface:[7:5] Reserved | [7:5]=000b |
| | | | Control interface:[4:3] SPI Mode | [4:3]=01b |
| | | | Control interface:[2] SPI Control available | [2]=1b |
| | | | Control interface:[1] $I^2C$ Control available | [1]=1b |
| | | | Control interface:[0] MIIM Control available | [0]=0b |
| 49 | SPIR | INT | SPI rate | 21h |

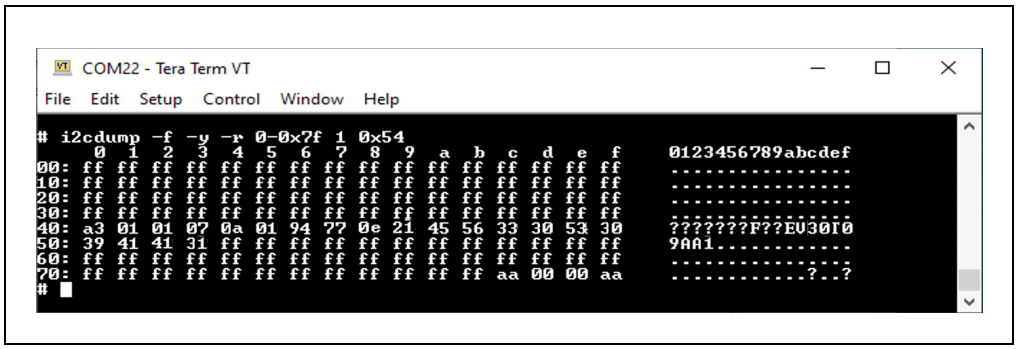
**TABLE 3-6: EDS2 DAUGHTER CARD EEPROM (CONTINUED)**

| Byte Address | Name | Type | Description | Value |
|---|---|---|---|---|
| 4A | DEVT | ASCII | Dev Tools part number | 45h = 'E' |
| 4B | | | | 56h = 'V' |
| 4C | | | | 39h = '3' |
| 4D | | | | 34h = '0' |
| 4E | | | | 54h = 'S' |
| 4F | | | | 39h = '0' |
| 50 | | | | 39h = '9' |
| 51 | | | | 41h = 'A' |
| 52 | BREVU | ASCII | UNG board revision letter | 41h = 'A' |
| 53 | BREVD | ASCII | Dev tools board revision number | 31h = '1' |

After the host board boots up with Linux (refer to **Chapter 4. "System Boot"**), the EEPROM's contents can be read within Linux via the following command:

```
# i2cdump -f -y -r 0-0x7F 1 0x54
```

**FIGURE 3-6: EEPROM DUMP**



# Chapter 4. System Boot

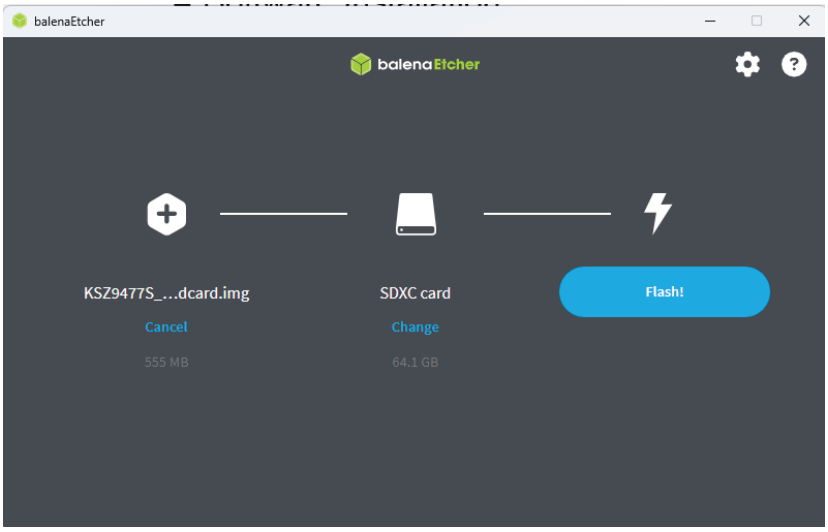
## 4.1 OVERVIEW

This chapter describes the boot process using the SAMA7D65 Curiosity EDS2 host using Linux software running on the SAMA7D65. The boot process for other EDS2 host platforms should be similar.

The EDS2 host board should be properly configured with Linux and driver supporting the KSZ9477S EDS2 Daughter Card. Refer to the software documentation on the KSZ9477S EDS2 Daughter Card product page at https://www.microchip.com/en-us/development-tool/EV30S09A. Download the microSD card image and program into an microSD card using a tool, such as balenaEtcher, with the following steps:

1. Download the SD card image file from the Microchip website.
2. Download and install balenaEtcher. This tool is an open-source software which can be downloaded here: https://www.balena.io/etcher/.
3. Insert the SD card into the PC with either an internal or external SD card reader and launch Etcher.

**FIGURE 4-1: BALENAETCHER**



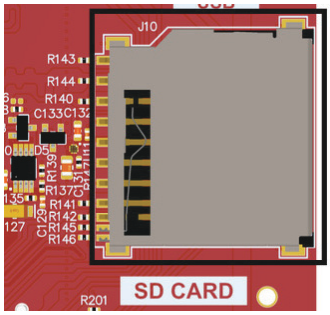
4. Select `KSZ9477S_EDS2_DC_sdcard.img`.
5. Select the device corresponding to the SD card reader.
6. Click on the **Flash!** button and wait for the programming to be completed.

## 4.2 KSZ9477S EDS2 SYSTEM POWER-UP

At this point, the KSZ9477S should be installed in the SODIMM EDS2 connector (refer to **Section 2.2 "KSZ9477S Installation"**). Perform the following steps to power up the SAMA7D65 Curiosity EDS2:

1. Verify the host board's default jumper settings within the *SAMA7D65 Curiosity EDS2 User's Guide*.
2. Insert the microSD card in SAMA7D65 Curiosity microSD card slot J10. See Figure 4-2.

**FIGURE 4-2: MICROSD CARD**

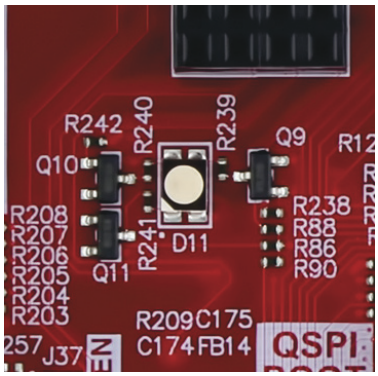



3. Connect the 1x6 female header of an FTDI or compatible TTL-232R-3V3 USB-to-serial cable into the UART debug header J35 on the SAMA7D65 Curiosity EDS2 host board. Note that the header black wire must connect to pin GND of J35. See Figure 4-3.

**FIGURE 4-3: SAMA7D65 UART DEBUG HEADER**

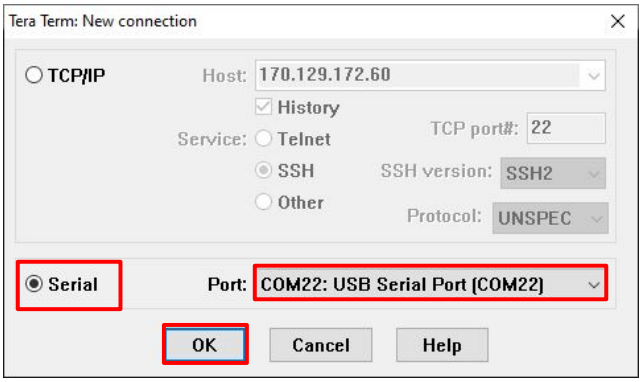
4. Connect a 5V 1A (minimum) power supply with a DC plug to DC Jack J1 on the SAMA7D65 Curiosity EDS2 host. The RGB LED LD11 should begin its startup sequence. See Figure 4-4.

**FIGURE 4-4: SAMA7D65 CURIOSITY RGB LED**



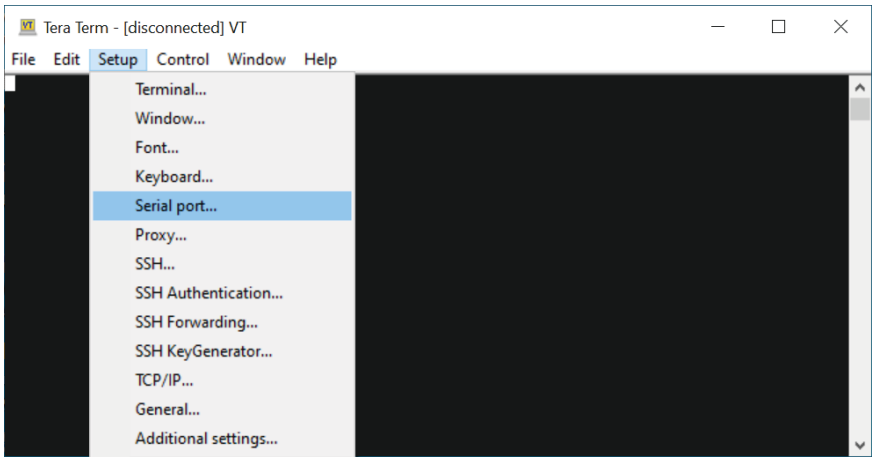

5. Open Tera Term. Tick the **Serial** radial button and look for COMx:USB Serial Port. See Figure 4-5.
6. Click on **OK**. Noted that Figure 4-5 shows COM22. Windows may assign a different port number.

**FIGURE 4-5: TERA TERM SERIAL PORT SELECTION**



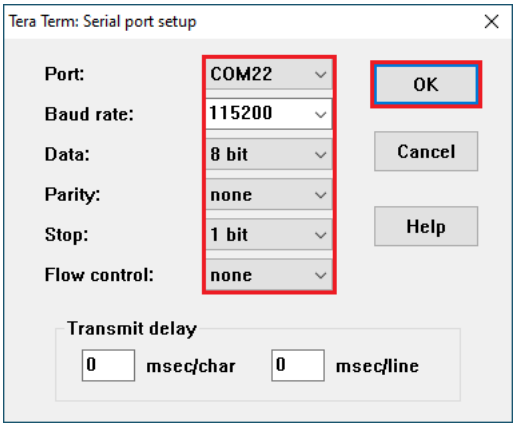
7. Go to the setup menu and select Serial port. See Figure 4-6.

**FIGURE 4-6: TERA TERM SETUP MENU**




8. Set the selected port to 115200, 8-bit, no parity, 1 stop bit, no flow control, and 40 msec/line. Click on **OK**. See Figure 4-7.

**FIGURE 4-7: TERA TERM SERIAL PORT SETUP**

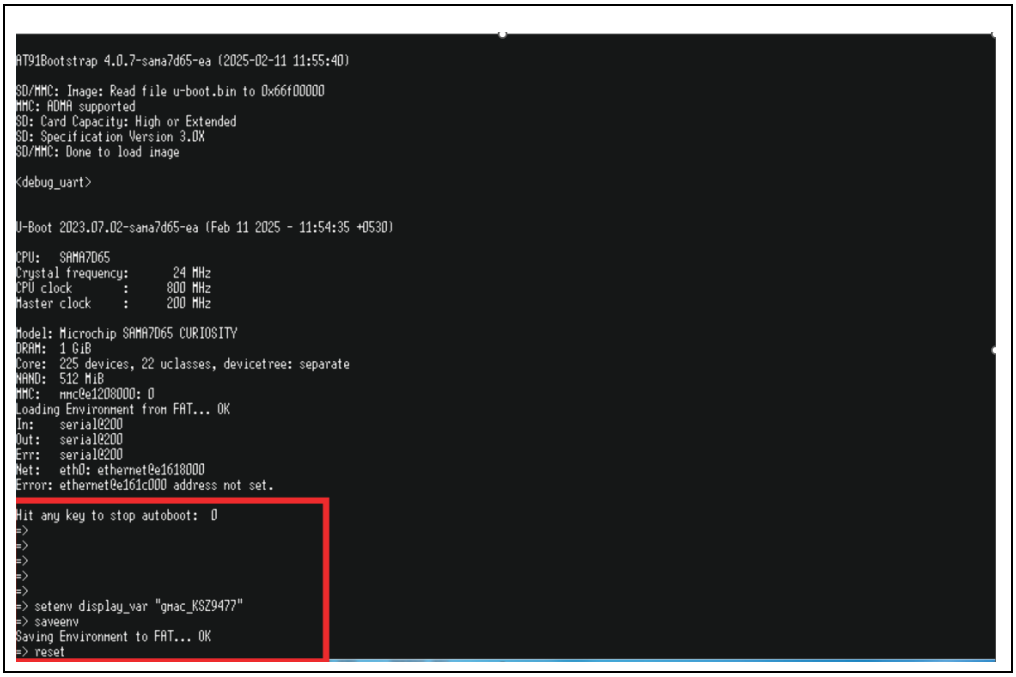



9. Setup the u-boot environment to activate KSZ9477S DSA driver with the following steps:
   a) Power cycle the SAMA7D65 EDS2 host.
   b) Hold down any key immediately to stop autoboot and wait for the message, "Hit any key to stop autoboot : 0," to appear on the console before releasing the key.
   c) Enter the following commands on the console:

```
=>setenv display_var 'gmac_ksz9477'
=>saveenv
=>reset
```

See u-boot environment setup to activate the KSZ9477S DSA driver in Figure 4-8.

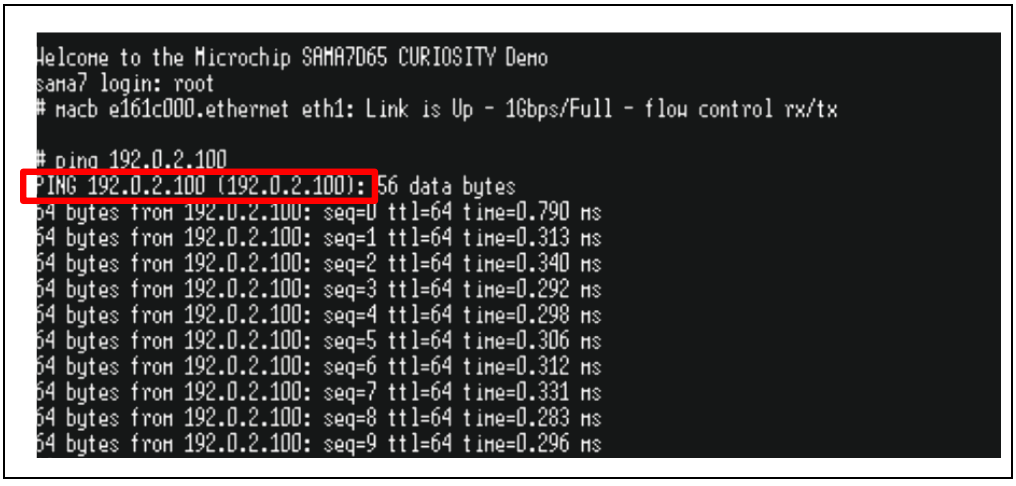
**FIGURE 4-8: KSZ9477S DSA DRIVER ACTIVATION**




| **Note:** | For the succeeding steps, it is assumed that the IP address of the SAMA7D65 is not changed from the default 192.0.2.1 and that a host PC with an Ethernet port that can be pinged at `192.0.2.100` is available. |
|---|---|

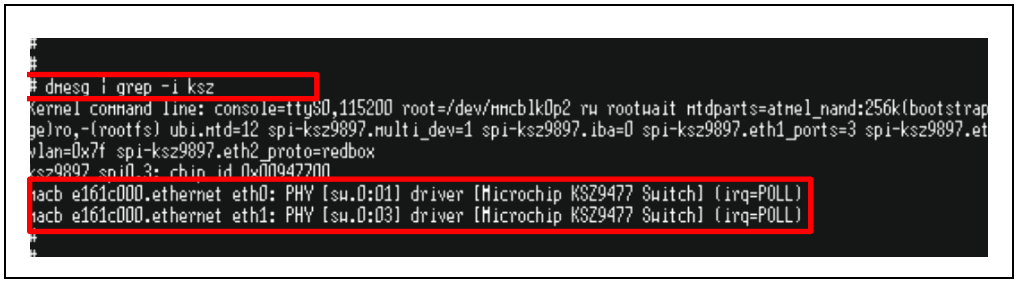
10. Enter the following command to perform a ping test (see Figure 4-9):
    `#ping 192.0.2.100.`

**FIGURE 4-9: PINGS FROM SAMA7D65 TO THE HOST PC**



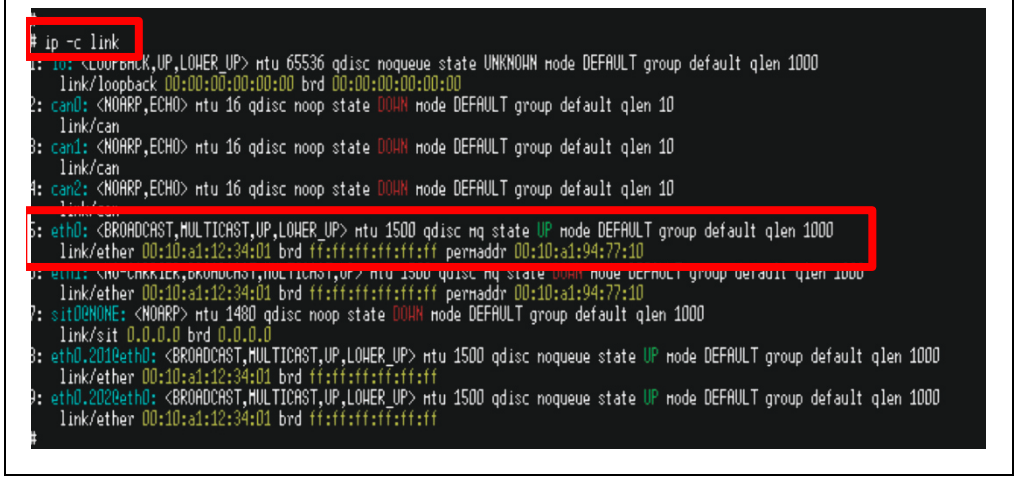
11. Verify that the KSZ9477S driver has loaded into the kernel. This switch utilizes DSA drivers from prior existing switch models. It should display KSZ9897 or KSZ9477, depending on how the image was built. Either option is fine. See Figure 4-10.

**FIGURE 4-10: # DMESG | GREP -I KSZ**




12. Plug an Ethernet cable into one of the RJ45 ports. Check the link status with the IP utility. One of the LAN ports shows an “Up” status indicator. See Figure 4-11.

**FIGURE 4-11: # IP -C LINK**



13. Verify that your IP configuration is compatible with your network. The example in Figure 4-12 indicates the switch is configured with an IP address of 192.0.2.101 with 24 bits for the network mask which is equivalent to 255.255.255.0. This configuration provides access to other devices on the 192.0.2.x addressed network.

**FIGURE 4-12: # IP -C ADDR**

```
# ip -c addr
1: lo: <LOOPBACK,UP,LOWER_UP> mtu 65536 qdisc noqueue state UNKNOWN group default qlen 1000
    link/loopback 00:00:00:00:00:00 brd 00:00:00:00:00:00
    inet 127.0.0.1/8 scope host lo
       valid_lft forever preferred_lft forever
    inet6 ::1/128 scope host
       valid_lft forever preferred_lft forever
2: can0: <NOARP,ECHO> mtu 16 qdisc noop state DOWN group default qlen 10
    link/can
3: can1: <NOARP,ECHO> mtu 16 qdisc noop state DOWN group default qlen 10
    link/can
4: can2: <NOARP,ECHO> mtu 16 qdisc noop state DOWN group default qlen 10
    link/can
5: eth0: <BROADCAST,MULTICAST,UP,LOWER_UP> mtu 1500 qdisc mq state UP group default qlen 1000
    link/ether 00:10:a1:12:34:01 brd ff:ff:ff:ff:ff:ff permaddr 00:10:a1:94:77:10
    inet 192.0.2.101/24 brd 255.255.255.0 scope global eth0
       valid_lft forever preferred_lft forever
    inet6 fe80::210:a1ff:fe12:3401/64 scope link
       valid_lft forever preferred_lft forever
6: eth1: <NO-CARRIER,BROADCAST,MULTICAST,UP> mtu 1500 qdisc mq state DOWN group default qlen 1000
    link/ether 00:10:a1:12:34:01 brd ff:ff:ff:ff:ff:ff permaddr 00:10:a1:94:77:10
    inet6 fe80::210:a1ff:fe12:3401/64 scope link
       valid_lft forever preferred_lft forever
7: sit0@NONE: <NOARP> mtu 1480 qdisc noop state DOWN group default qlen 1000
    link/sit 0.0.0.0 brd 0.0.0.0
8: eth0.201@eth0: <BROADCAST,MULTICAST,UP,LOWER_UP> mtu 1500 qdisc noqueue state UP group default qlen 1000
    link/ether 00:10:a1:12:34:01 brd ff:ff:ff:ff:ff:ff
    inet6 fe80::210:a1ff:fe12:3401/64 scope link
       valid_lft forever preferred_lft forever
9: eth0.202@eth0: <BROADCAST,MULTICAST,UP,LOWER_UP> mtu 1500 qdisc noqueue state UP group default qlen 1000
    link/ether 00:10:a1:12:34:01 brd ff:ff:ff:ff:ff:ff
    inet6 fe80::210:a1ff:fe12:3401/64 scope link
       valid_lft forever preferred_lft forever
#
```

**NOTES:**

# Appendix A. Schematics

## A.1 INTRODUCTION

This appendix shows the KSZ9477S schematics.

**FIGURE A-1: KSZ9477S EDS2 DAUGHTER CARD**

# KSZ9477S Gigabit Ethernet Switch EDS2 Daughter Card

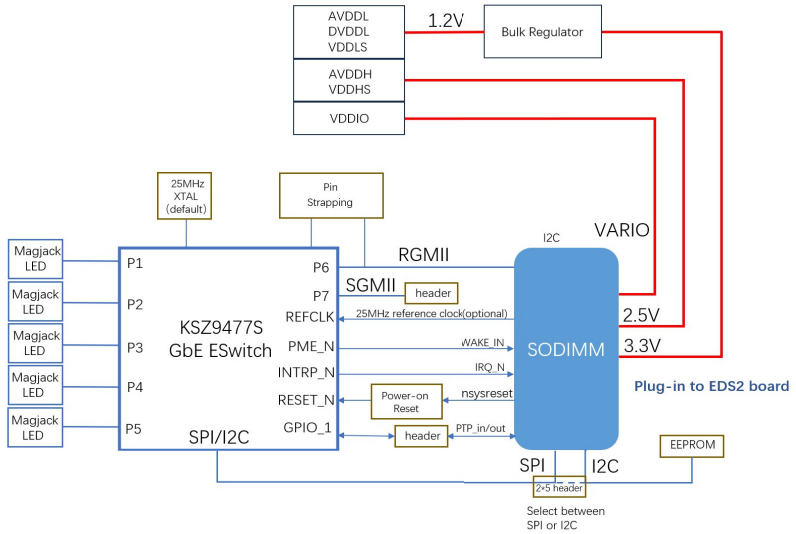
**Table of Contents**

| Sheet | Description |
|---|---|
| 1 | Title Page & Block Diagram |
| 2 | KSZ9477S Device |
| 3 | RJ45 front Ports |
| 4 | Board Power |
| 5 | I/O Connector |

**Revision History**

| Revision | Date | Revision Summary | Author |
|---|---|---|---|
| A | 04/05/2025 | Initial Release | Wayne Lu |

**Block Diagram**




Project Owner: Wayne Lu
PCB Layout Contact: Sam Charles
PartNumber: EV30S09A
Project Title: KSZ9477S EDS2 Daughter Card
Variant: V1
Sheet Title: Table of contents, block diagram, revision history
Size: Tabloid | SCH #: 02-01146 | Rev: 1 | Date: 4/8/2025
PCB #: 04-12211 | Rev: 1 | Sheet 1 of 5
Designed with Altium — Altium.com

**FIGURE A-2: KSZ9477S EDS2 DAUGHTER CARD SWITCH AND RESET**

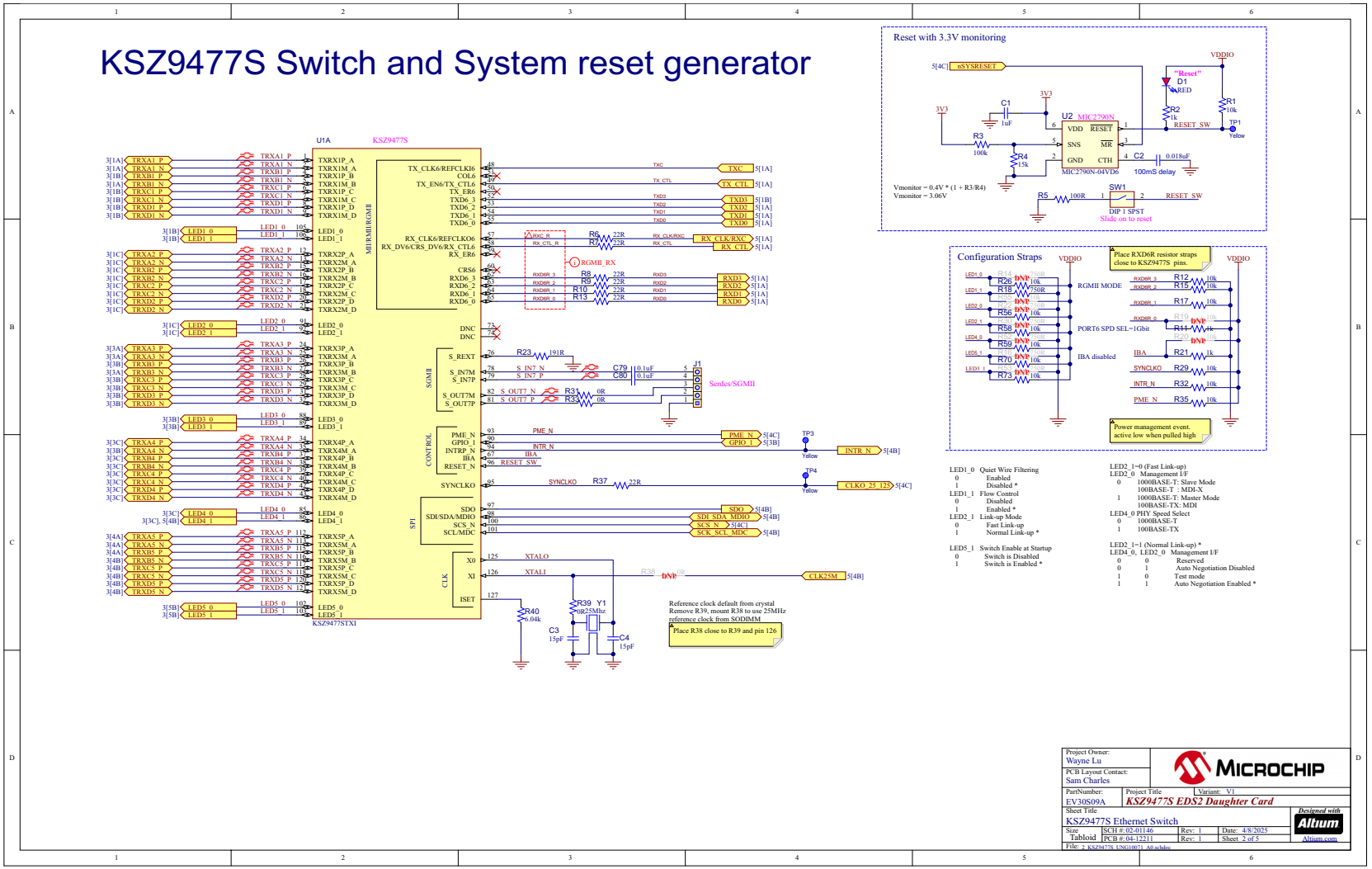


**FIGURE A-3: KSZ9477S EDS2 DAUGHTER CARD RJ45 PORTS**

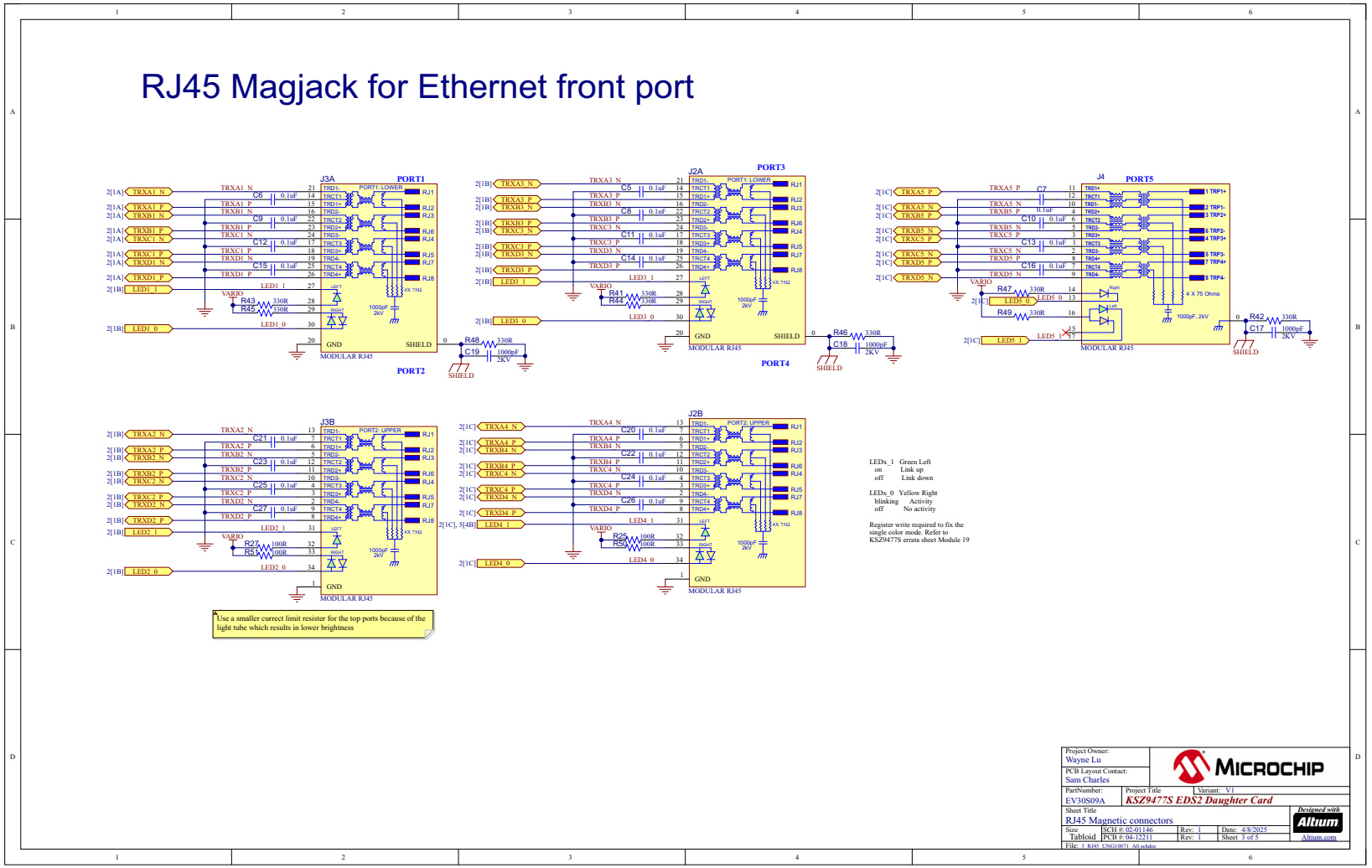


**FIGURE A-4: KSZ9477S EDS2 DAUGHTER CARD POWER**

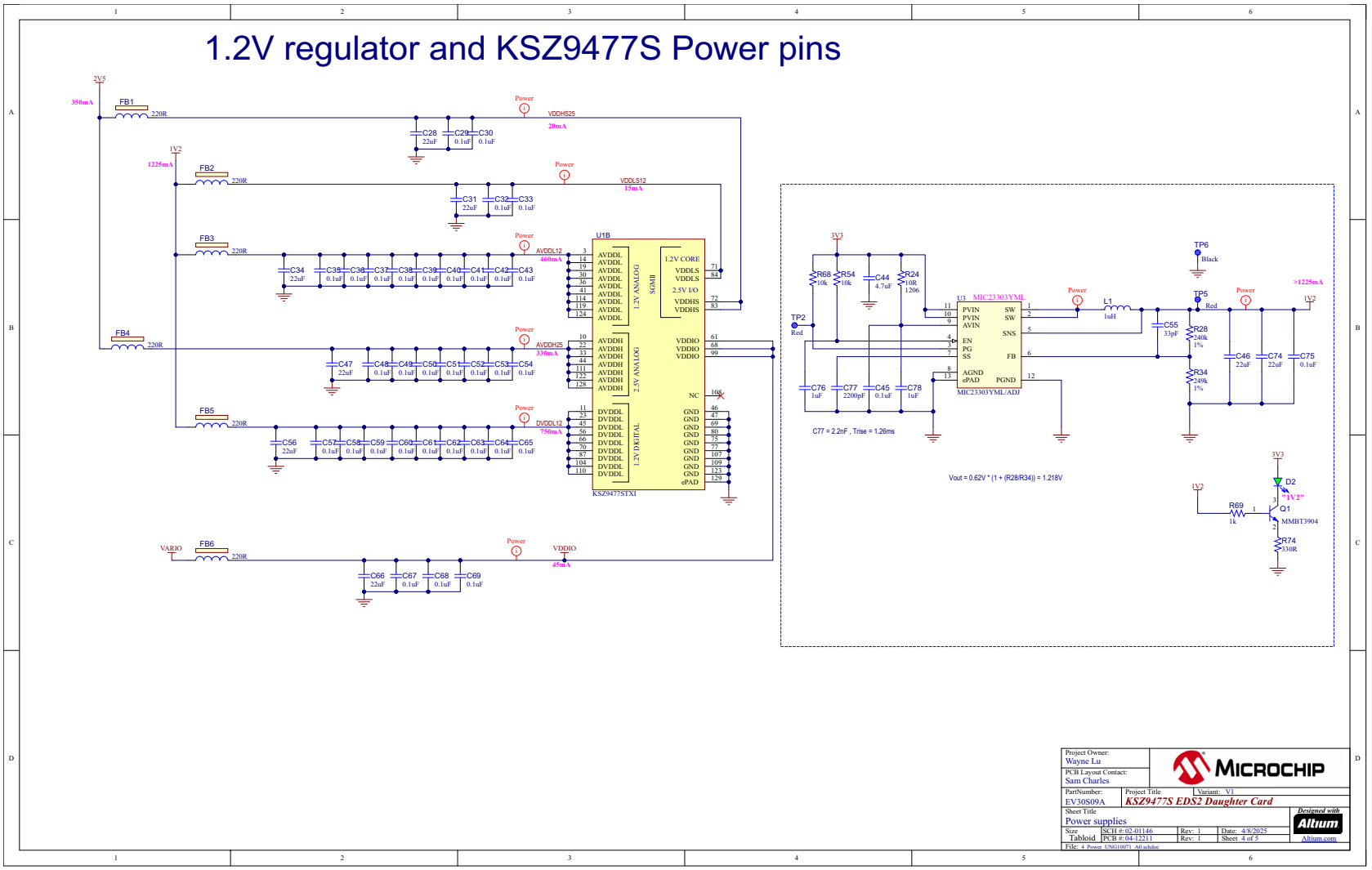
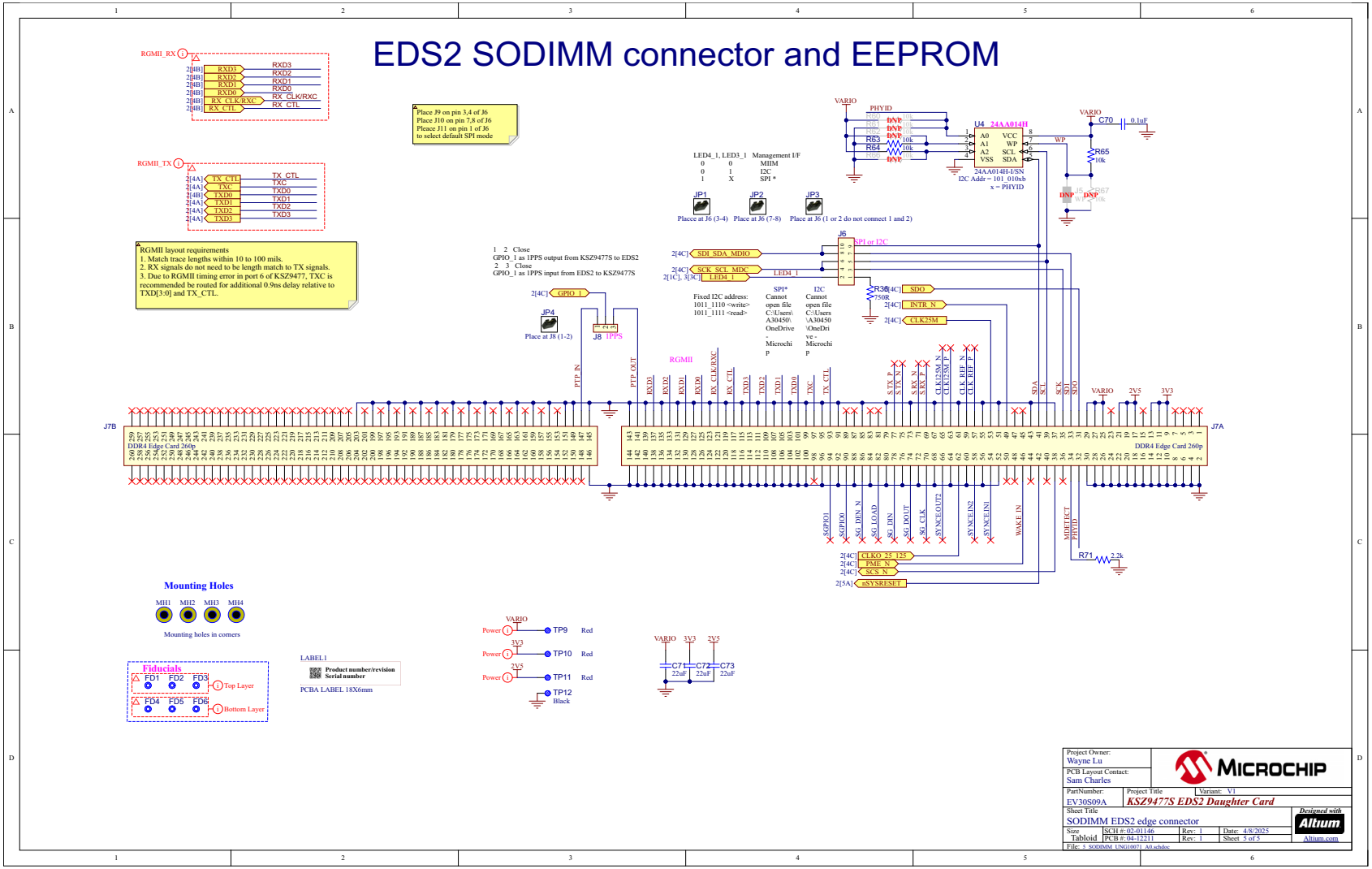


**FIGURE A-5: KSZ9477S EDS2 DAUGHTER CARD SODIMM EDS2 INTERFACE AND EEPROM**



# Appendix B. Bill of Materials

## B.1 INTRODUCTION

This appendix contains the KSZ9477S Bill of Materials (BOM).

**TABLE B-1: BILL OF MATERIALS (BOM)**

| Item | Qty | Reference | Description | Populated | Manufacturer | Manufacturer Part Number |
|---|---|---|---|---|---|---|
| 1 | 3 | C1, C76, C78 | CAP CER 1uF 16V 10% X5R SMD 0603 | Yes | Yageo | CC0603KRX5R7BB105 |
| 2 | 1 | C2 | CAP CER 0.018uF 50V 10% X7R SMD 0603 | Yes | KEMET | C0603C183K5RACTU |
| 3 | 2 | C3, C4 | CAP HiQ 15pF 50V 5% NP0 2.32GHz SMD 0402 | Yes | Johanson | 500R07S150JV4T |
| 4 | 57 | C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C20, C21, C22, C23, C24, C25, C26, C27, C29, C30, C32, C33, C35, C36, C37, C38, C39, C40, C41, C42, C43, C45, C48, C49, C50, C51, C52, C53, C54, C57, C58, C59, C60, C61, C62, C63, C64, C65, C67, C68, C69, C70, C75, C79, C80 | CAP CER 0.1uF 35V 10% X7R SMD 0402 | Yes | TDK | CGA2B3X7R1V104K050BB |
| 5 | 3 | C17, C18, C19 | CAP CER 1000pF 2KV 10% X7R SMD 1206 | Yes | Johanson | 202R18W102KV4E |
| 6 | 11 | C28, C31, C34, C46, C47, C56, C66, C71, C72, C73, C74 | CAP CER 22uF 16V 10% X5R SMD 0805 | Yes | Samsung | CL21A226KOQNNNG |
| 7 | 1 | C44 | CAP CER 4.7uF 10V 10% X5R SMD 0603 | Yes | Taiyo Yuden | LMK107BJ475KA-T |
| 8 | 1 | C55 | CAP CER 33pF 50V 5% NP0 SMD 0603 | Yes | NIC Components | NMC0603NPO330J50TRPF |
| 9 | 1 | C77 | CAP CER 2200pF 16V 10% X7R SMD 0603 | Yes | Kyocera AVX | 0603YC222KAT2A |
| 10 | 1 | D1 | DIO RED 2V 20mA 54mcd CLEAR SMD 0603 | Yes | Vishay Lite-On | LTSTC191KRKT |
| 11 | 1 | D2 | DIO LED GREEN 2V 30mA 35mcd Clear SMD 0603 | Yes | Vishay Lite-On | LTST-C191KGKT |
| 12 | 6 | FB1, FB2, FB3, FB4, FB5, FB6 | FERRITE 220R @ 100MHz 2A SMD 0603 | Yes | Murata | BLM18EG221SN1D |
| 13 | 1 | J1 | CON HDR-2.54 Male 1x5 Gold 5.84MH TH VERT | Yes | Samtec | TSW-105-07-S-S |
| 14 | 2 | J2, J3 | CON MODULAR JACK RJ45 10/100/1000 MAGNETICS 2xLEDS SHIELD TH RA | Yes | Bel | 0845-2R1T-E4 |
| 15 | 1 | J4 | CON MODULAR JACK RJ45 10/100/1000 MAGNETICS 2xLEDs SHIELD TH | Yes | Bel | L829-1J1T-43 |
| 16 | 0 | J5 | CON HDR-2.54 Male 1x2 Gold 5.84MH TH VERT | Yes | Sullins | PBC02SAAN |
| 17 | 1 | J6 | CON HDR-2.54 Male 2x5 Tin 5.84MH TH VERT | Yes | Sullins | PEC05DAAN |
| 18 | 1 | J8 | CON HDR-2.54 Male 1x3 Gold 5.84MH TH VERT | Yes | Burndy | 68000-103HLF |
| 19 | 4 | JP1, JP2, JP3, JP4 | MECH HW JUMPER 2.54mm 1x2 GOLD | MECH | Sullins | QPC02SXGN-RC |
| 20 | 1 | L1 | INDUCTOR 1uH 2.1A 30% SMD L3W3H1.5 | Yes | Taiyo Yuden | NR3015T1R0N |
| 21 | 1 | Q1 | TRANS BJT NPN MMBT3904 40V 200mA 310mW SOT-23-3 | Yes | Diodes Zetex | MMBT3904-7-F |
| 22 | 18 | R1, R12, R15, R17, R26, R29, R32, R35, R54, R56, R58, R59, R63, R64, R65, R68, R70, R73 | RES TF 10k 1% 1/10W SMD 0402 AEC-Q200 | Yes | KOA Speer | RK73H1ERTTP1002F |
| 23 | 4 | R2, R11, R21, R69 | RES TKF 1k 1% 1/10W SMD 0402 | Yes | Panasonic | ERJ-2RKF1001X |
| 24 | 1 | R3 | RES TKF 100k 1% 1/4W SMD 0603 | Yes | Vishay | CRCW0603100KFKEAHP |

**TABLE B-1: BILL OF MATERIALS (BOM) (CONTINUED)**

| Item | Qty | Reference | Description | Populated | Manufacturer | Manufacturer Part Number |
|---|---|---|---|---|---|---|
| 25 | 1 | R4 | RES TF 15k 0.5% 1/10W SMD 0603 | Yes | Yageo | RT0603DRD0715KL |
| 26 | 1 | R5 | RES TKF 100R 1% 1/10W SMD 0603 AEC-Q200 | Yes | Yageo | AC0603FR-10100RL |
| 27 | 7 | R6, R7, R8, R9, R10, R13, R37 | RES TKF 22R 1% 1/20W SMD 0402 | Yes | Panasonic | ERJ-2RKF22R0X |
| 28 | 0 | R14, R16, R22, R30, R52, R53 | RES TKF 750R 1/10W 1% SMD 0402 | Yes | Panasonic Electronic Components | ERJ-2RKF7500X |
| 29 | 2 | R18, R36 | RES TKF 750R 1/10W 1% SMD 0402 | Yes | Panasonic Electronic Components | ERJ-2RKF7500X |
| 30 | 0 | R19, R20, R55, R60, R61, R62, R66, R67 | RES TF 10k 1% 1/10W SMD 0402 AEC-Q200 | Yes | KOA Speer | RK73H1ERTTP1002F |
| 31 | 1 | R23 | RES TKF 191R 1% 1/16W SMD 0402 | Yes | Yageo | RC0402FR-07191RL |
| 32 | 1 | R24 | RES TKF 10R 1% 1/4W SMD 1206 AEC-Q200 | Yes | Vishay | CRCW120610R0FKEA |
| 33 | 4 | R25, R27, R50, R51 | RES TKF 100R 5% 1/16W SMD 0402 | Yes | Bourns | CR0402AJW-101GAS |
| 34 | 1 | R28 | RES TKF 240k 1% 1/10W SMD 0603 | Yes | Panasonic | ERJ-3EKF2403V |
| 35 | 3 | R31, R33, R39 | RES TKF 0R SMD 0402 AEC-Q200 | Yes | Panasonic | ERJ-2GE0R00X |
| 36 | 1 | R34 | RES TKF 249k 1% 1/10W SMD 0603 | Yes | Panasonic | ERJ-3EKF2493V |
| 37 | 0 | R38 | RES TKF 0R SMD 0402 AEC-Q200 | Yes | Panasonic | ERJ-2GE0R00X |
| 38 | 1 | R40 | RES TKF 6.04k 1% 1/10W SMD 0402 AEC-Q200 | Yes | KOA Speer | RK73H1ETTP6041F |
| 39 | 10 | R41, R42, R43, R44, R45, R46, R47, R48, R49, R74 | RES TKF 330R 1% 1/10W SMD 0402 AEC-Q200 | Yes | Panasonic | ERJ-2RKF3300X |
| 40 | 1 | R71 | RES TKF 2.2k 1% 1/10W SMD 0402 | Yes | Panasonic | ERJ-2RKF2201X |
| 41 | 1 | SW1 | SWITCH DIP 1 SPST 24V 25mA 418117270901 TH | Yes | Wurth Electronics | 418117270901 |
| 42 | 3 | TP1, TP3, TP4 | MISC, TEST POINT PC MINI, 0.040" D YELLOW | Yes | Keystone Electronics | 5004 |
| 43 | 5 | TP2, TP5, TP9, TP10, TP11 | MISC, TEST POINT MULTI PURPOSE MINI RED | Yes | Keystone Electronics | 5000 |
| 44 | 2 | TP6, TP12 | MISC, TEST POINT MULTI PURPOSE MINI BLACK | Yes | Keystone Electronics | 5001 |
| 45 | 1 | U1 | MCHP INTERFACE ETHERNET KSZ9477STXI TQFP-128 | Yes | Microchip | KSZ9477STXI |
| 46 | 1 | U2 | MCHP ANALOG SUPERVISOR 0.4V to 5.5V MIC2790N-04VD6 SOT-23-3 | Yes | Microchip Technology | MIC2790N-04VD6 |
| 47 | 1 | U3 | MCHP ANALOG SWITCHER ADJ MIC23303YML-TR DFN-12 | Yes | Microchip | MIC23303YML-TR |
| 48 | 1 | U4 | MCHP MEMORY SERIAL EEPROM 1kb I2C 24AA014H-I/SN 8SOIC | Yes | Microchip | 24AA014H-I/SN |
| 49 | 1 | Y1 | MCHP CRYSTAL 25Mhz 10pF SMD L3.2W2.5H0.8 | Yes | Microchip | VXM7-9013-25M0000000 |

**NOTES:**

# Appendix C. PCB Layers

## C.1 INTRODUCTION

This appendix contains the KSZ9477S's silkscreen top and bottom layers.

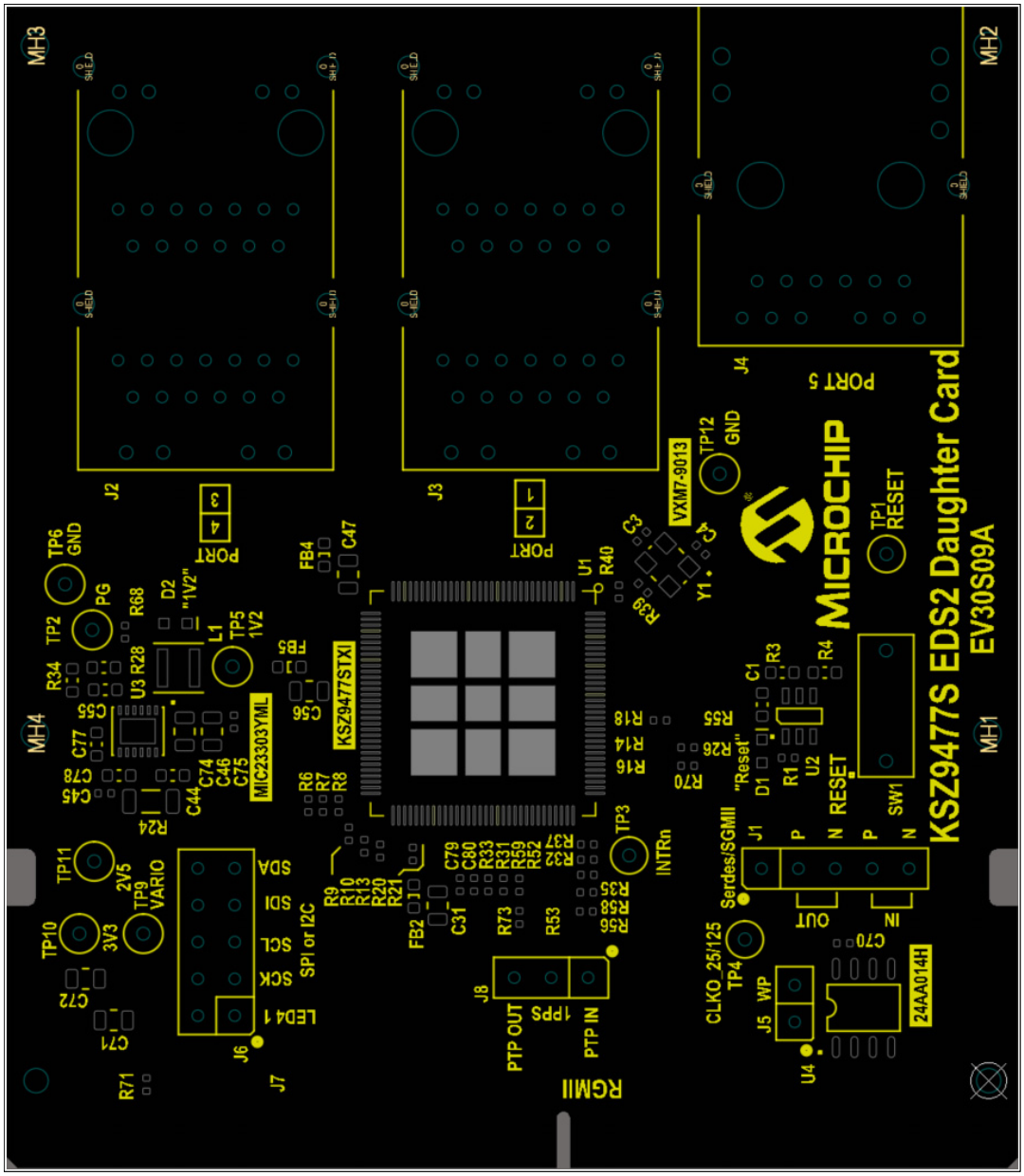



FIGURE C-1: KSZ9477S EDS2 DAUGHTER CARD TOP SILK SCREEN

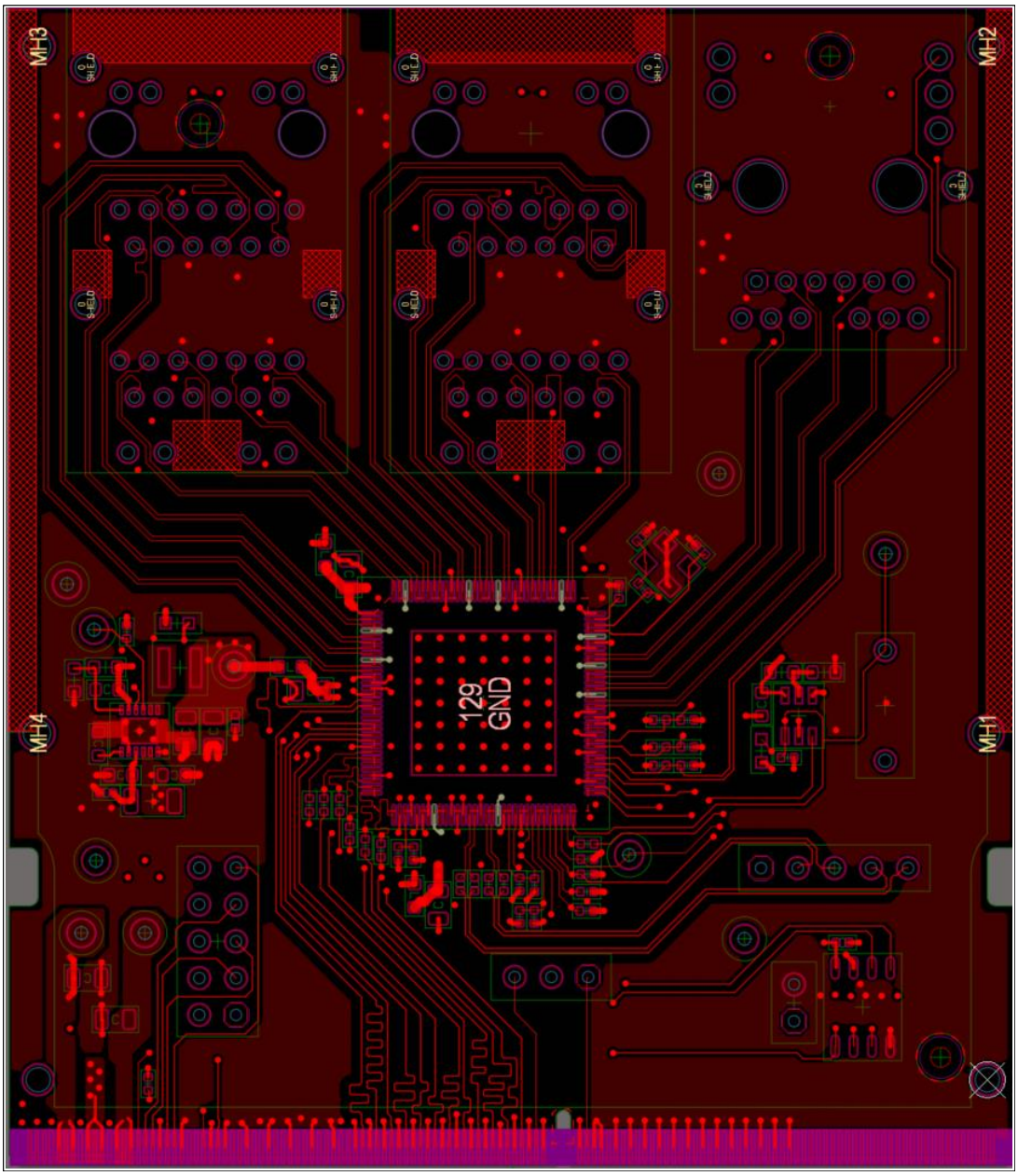



FIGURE C-2: KSZ9477S EDS2 DAUGHTER CARD TOP LAYER

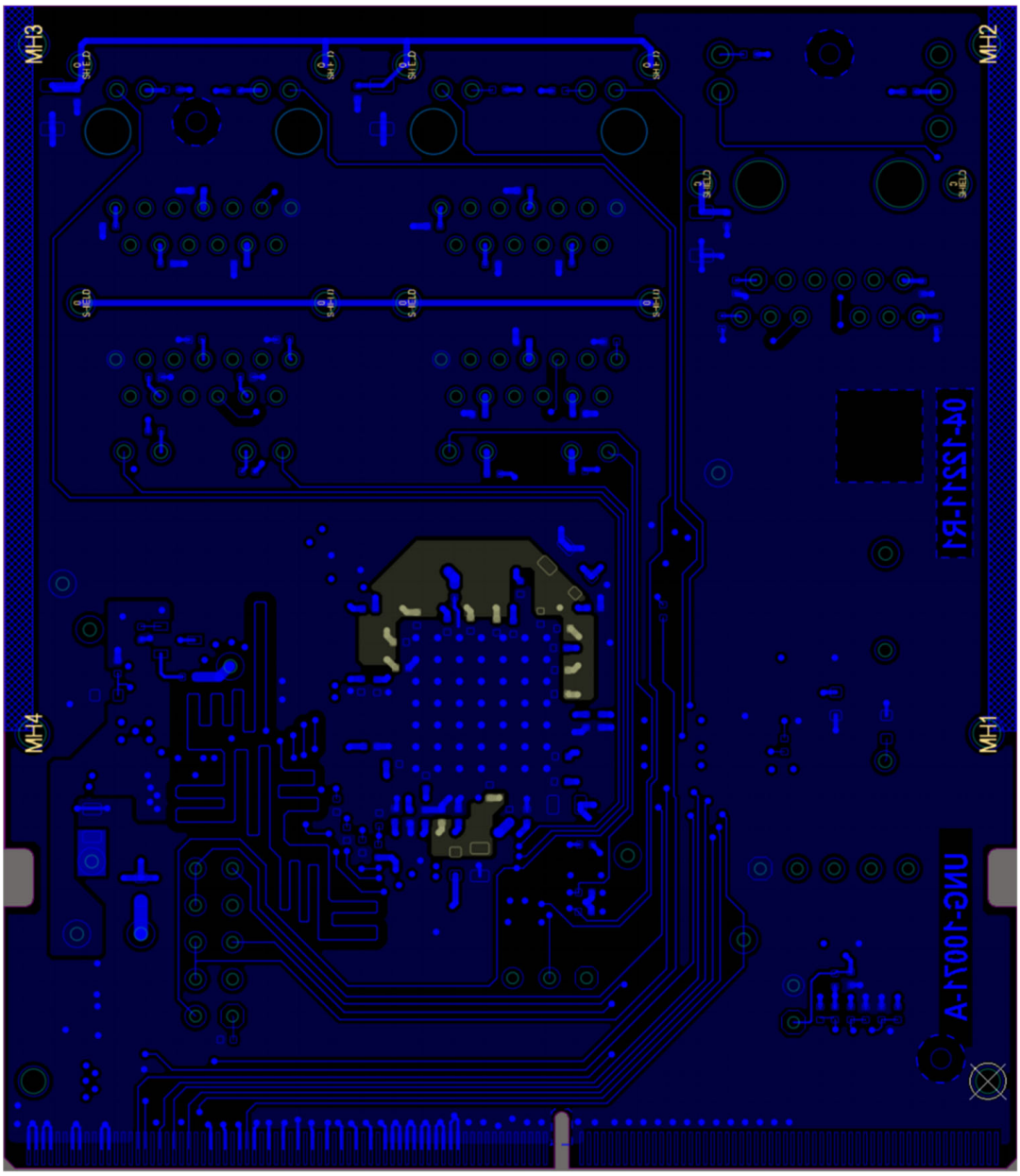



FIGURE C-3: KSZ9477S EDS2 DAUGHTER CARD BOTTOM LAYER

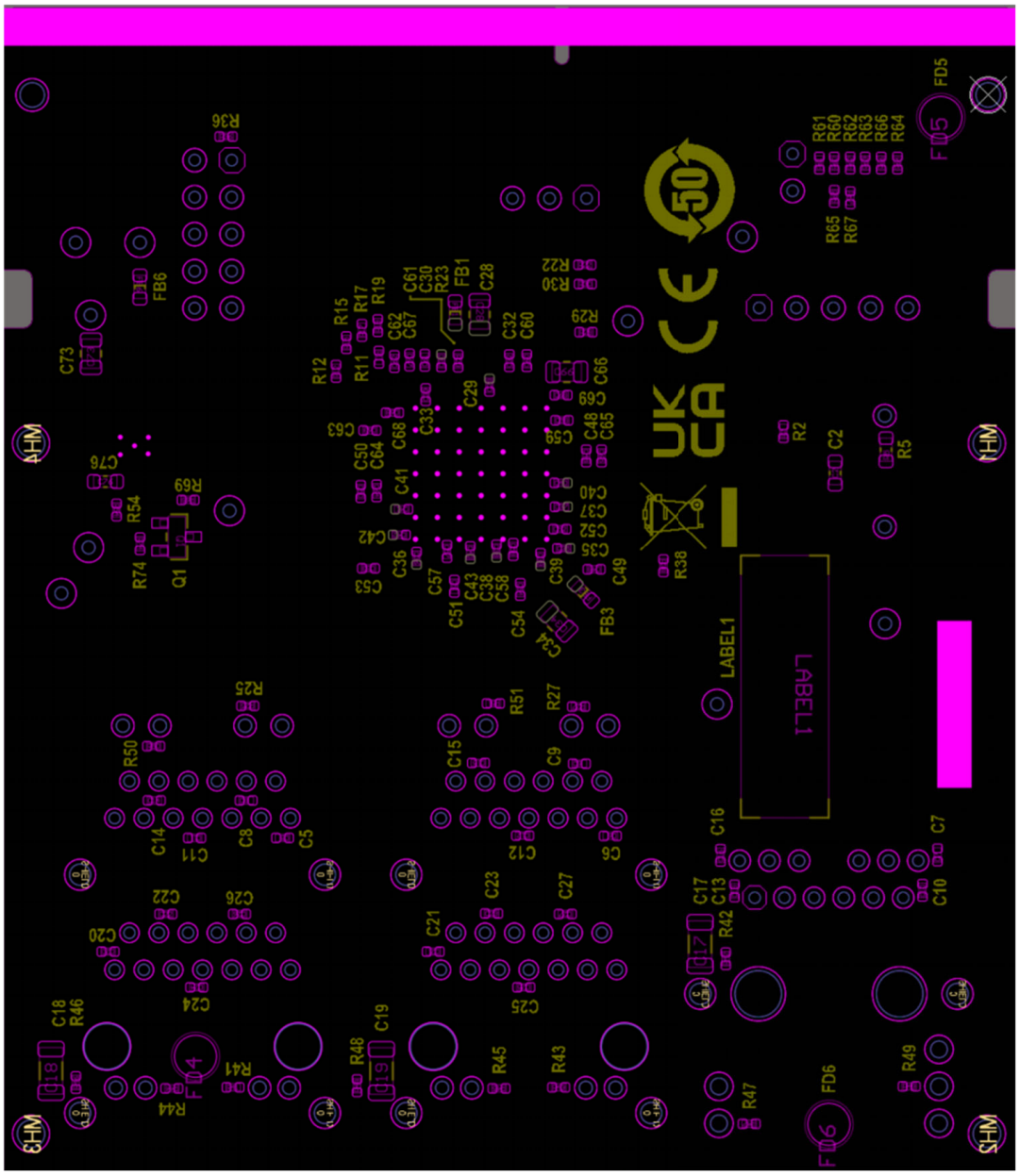



FIGURE C-4: KSZ9477S EDS2 DAUGHTER CARD BOTTOM SILK SCREEN