Evaluation Board User Guide

ADPL13602EVKIT# Evaluation Kit

Evaluates: ADPL13602 in 5V Output-Voltage Application

General Description

The ADPL13602EVKIT# evaluation kit (EV kit) provides a proven design to evaluate the ADPL13602 high-efficiency, synchronous step-down DC-DC converter. The EV kit provides 5V/2.4A at the output from a 6.5V to 36V input supply. The switching frequency of the EV kit is preset to 500kHz for optimum efficiency and component size. The EV kit features adjustable input undervoltage lockout, adjustable soft-start, and open-drain RESET signal.

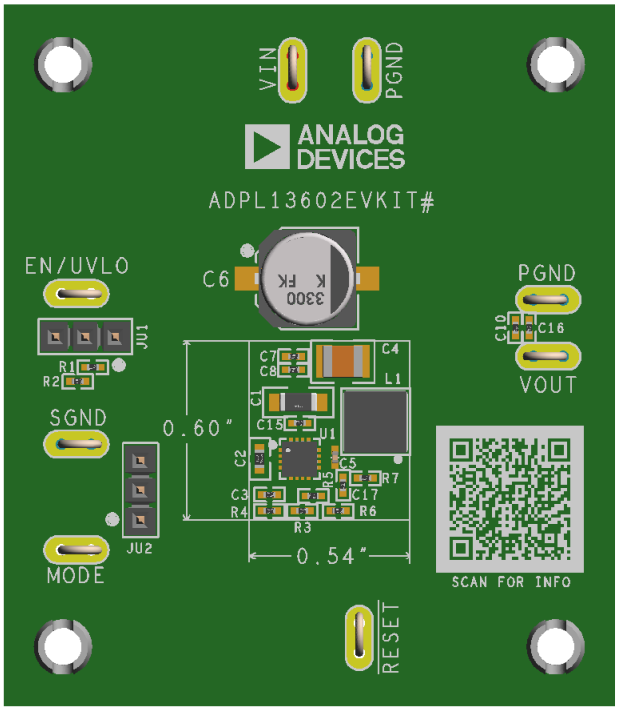
The EV kit also provides a good layout example, which is optimized for thermal performance. For more details about the IC benefits and features, refer to the ADPL13602 data sheet.

Features and Benefits

- Operates from a 6.5V to 36V Input Supply
- 5V Output Voltage
- Delivers Up to 2.4A Output Current
- 500kHz Switching Frequency
- Enable/Undervoltage Lockout Input, Resistor–Programmable UVLO Threshold
- Adjustable Soft-Start Time
- Open-Drain $\overline{\text{RESET}}$ Output
- Overcurrent and Overtemperature Protection
- Proven Printed Circuit Board (PCB) Layout
- Fully Assembled and Tested

Ordering Information *appears at end of data sheet.*

EV Kit Photo



319-101041; Rev 0; 12/23

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.329.4700

Quick Start

Required Equipment

- ADPL13602EVKIT#
- 6.5V to 36V, 2.5A DC-input power supply
- Load capable of sinking 2.4A
- One digital voltmeter (DVM)

Equipment Setup and Test Procedure

The EV kit is fully assembled and tested. Follow the steps below to verify the board operation.

Caution: Do not turn on power supply until all connections are completed.

1. Set the power supply at a voltage between 6.5V and 36V. Then, disable the power supply.
2. Connect the positive terminal of the power supply to the VIN PCB pad and the negative terminal to the nearest PGND PCB pad. Connect the positive terminal of the 2.4A load to the VOUT PCB pad and the negative terminal to the nearest PGND PCB pad.
3. Connect the DVM across the VOUT PCB pad and the nearest PGND PCB pad.
4. Verify that the shunt is installed across pins 1-2 on jumper JU1 (see *Table 1* for more details).
5. Select the shunt position on JU2 according to the intended mode of operation (see *Table 2* for details)
6. Turn on the DC power supply.
7. Enable the load.
8. Verify that the DVM displays 5V.
9. Verify that the DVM displays 1.8V across $\overline{\text{RESET}}$ and SGND PCB pads.

Detailed Description

The ADPL13602EVKIT# EV kit is designed to deliver load current up to 2.4A at 5V output voltage from a 6.5V to 36V input supply. The switching frequency of the EV kit is configured at 500kHz by leaving the RT resistor open.

The EV kit includes an EN/UVLO PCB pad and jumper JU1 to enable the output at a desired minimum input voltage. Jumper JU2 allows the selection of the mode of operation based on light load performance requirements. An additional $\overline{\text{RESET}}$ PCB pad is available to monitor whether the converter output is in regulation.

Soft-Start Input (SS)

The EV kit offers an adjustable soft-start function to limit inrush current during the startup. The soft-start time is adjusted by the value of C3, the external capacitor connected between SS and SGND. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum value of C3, as shown by the following equation:

$$C3 \geq 28 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the soft-start capacitor C3 by the following equation:

$$t_{SS} = \frac{C3}{(8.325 \times 10^{-6})}$$

For example, to program a 0.82ms soft-start time, C3 should be 6800pF.

Enable/Undervoltage-Lockout (EN/UVLO) Programming

The ADPL13602 offers an enable and an adjustable input undervoltage lockout feature. In this EV kit, leave the EN/UVLO jumper (JU1) open for normal operation. When JU1 is left open, the ADPL13602 is enabled when the input voltage rises above 6.3V. To disable ADPL13602, install a jumper across pins 2-3 on JU1. See *Table 1* for JU1 settings. The EN/UVLO PCB pad on the EV kit supports external enable/disable control of the device. Leave jumper JU1 open when external enable/disable control is desired. A potential divider formed by R1 and R2 sets the input voltage (V_{INU}) above which the converter is enabled when JU1 is left open.

Choose R1 to be 3.32MΩ max, then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.25}{(V_{INU} - 1.25)}$$

where, V_{INU} is the voltage at which the device is required to turn on.

R1 and R2 are in kΩ,

Refer to the ADPL13602 data sheet for more details on setting the input undervoltage lockout level.

Table 1. Converter EN/UVLO Jumper (JU1) Settings

SHUNT POSITION	EN/UVLO PIN	ADPL13602 OUTPUT
1-2	Connected to V_{IN}	Always Enabled
Not installed*	Connected to the center node of resistor-divider R1 and R2	Enabled, UVLO level is set by the resistor-divider between V_{IN} and SGND
2-3	Connected to SGND	Disabled

**Default position.*

Mode Selection (MODE)

The ADPL13602EVKIT# EV kit provides a jumper (JU2) that allows the ADPL13602B to operate in Pulse-Width Modulation (PWM) and Discontinuous conduction mode (DCM) modes. The EV kit also provides a MODE PCB pad to monitor the MODE pin voltage of the converter in the desired mode of operation. Refer to the ADPL13602 data sheet for more details on the modes of operation.

Table 2 shows the mode selection (JU2) settings that can be used to configure the desired mode of operation.

Table 2. Mode Selection (JU2) Settings

SHUNT POSITION	MODE PIN	ADPL13602 OPERATION
1-2	Connected to VCC	DCM mode of operation
2-3*	Connected to SGND	PWM mode of operation

**Default position.*

Active-Low, Open-Drain Reset Output ($\overline{\text{RESET}}$)

The ADPL13602EVKIT# EV kit provides a $\overline{\text{RESET}}$ PCB pad to monitor the status of the converter. $\overline{\text{RESET}}$ goes high when VOUT rises above 95% (typ) of its nominal regulated voltage. $\overline{\text{RESET}}$ goes low when V_{OUT} falls below 92% (typ) of its nominal regulated voltage.

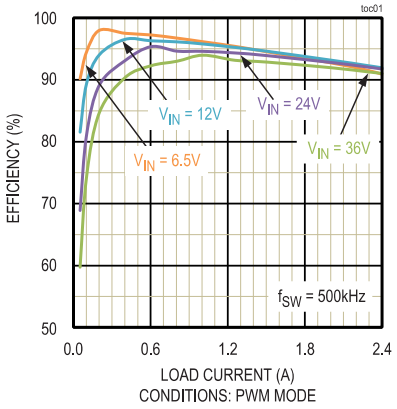
Hot Plug-In and Long Input Cables

The ADPL13602EVKIT# PCB layout provides an optional electrolytic capacitor (C6 = 47µF/50V). This capacitor limits the peak voltage at the input of the ADPL13602 when the DC input source is “hot-plugged” to the EV kit input terminals with long input cables. The equivalent series resistance (ESR) of the electrolytic capacitor dampens the oscillations caused by the interaction of the inductance of the long input cables and the ceramic capacitors at the buck converter input.

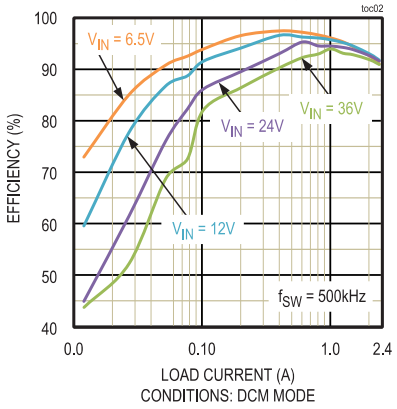
ADPL13602EVKIT# EV Kit Performance Report

(V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 2.4A, f_{SW} = 500kHz, T_A = +25ºC, unless otherwise noted.)

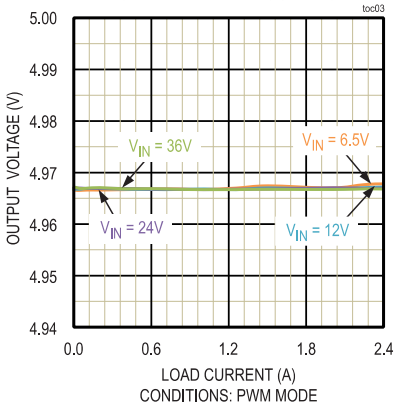
EFFICIENCY vs. LOAD CURRENT



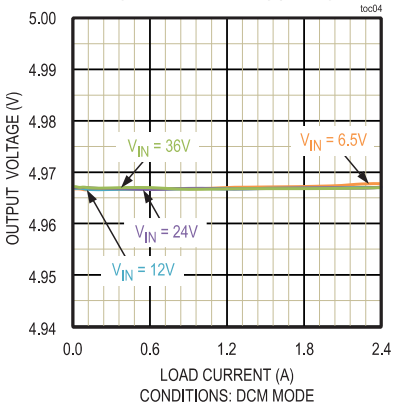
EFFICIENCY vs. LOAD CURRENT



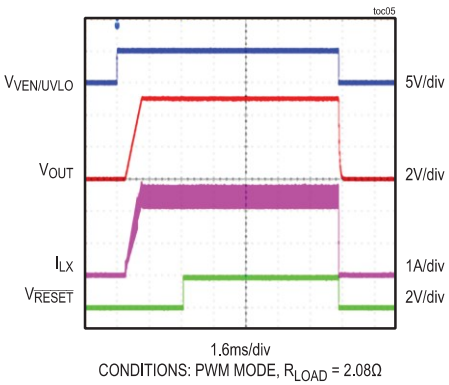
LOAD AND LINE REGULATION



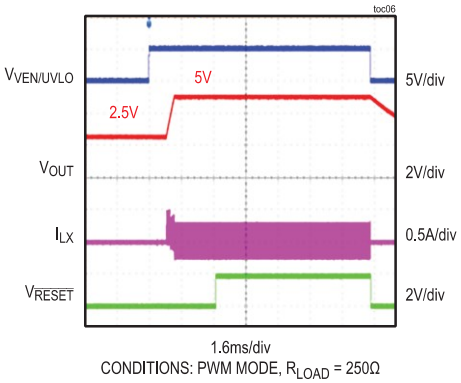
LOAD AND LINE REGULATION



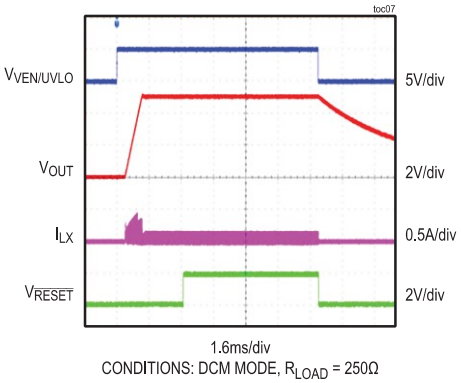
SOFT-START/SHUTDOWN THROUGH EN/UVLO



SOFT-START WITH PREBIAS VOLTAGE OF 2.5V

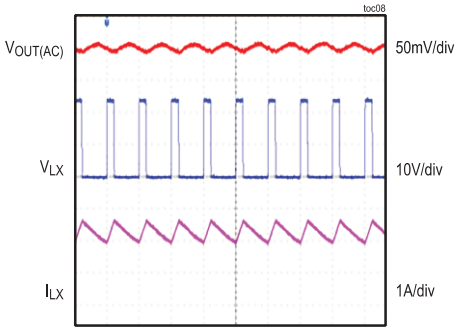


SOFT-START/SHUTDOWN THROUGH EN/UVLO



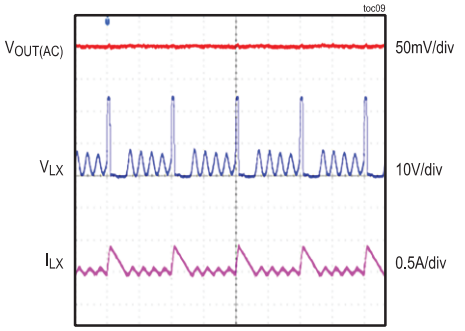
(V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 2.4A, f_{SW} = 500kHz, T_A = +25ºC, unless otherwise noted.)

STEADY-STATE PERFORMANCE



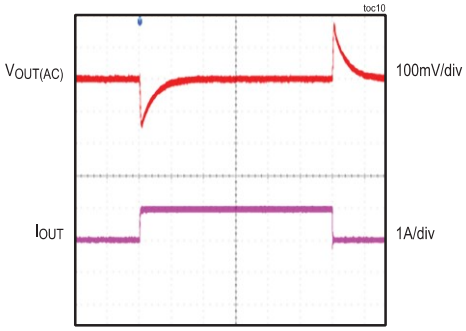
CONDITIONS: PWM MODE, 2.4A LOAD

STEADY-STATE PERFORMANCE



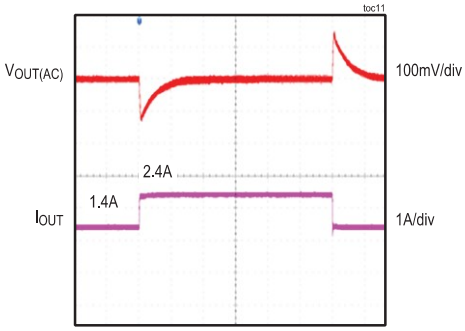
CONDITIONS: DCM MODE, 20mA LOAD

LOAD TRANSIENT BETWEEN 0A AND 1A



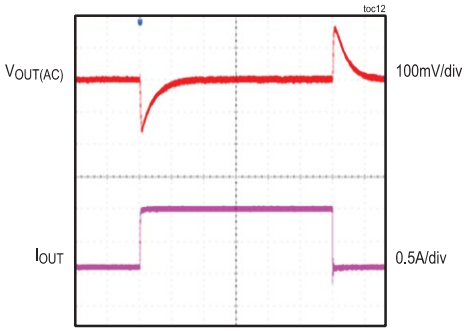
CONDITIONS: PWM MODE

LOAD TRANSIENT BETWEEN 1.4A AND 2.4A



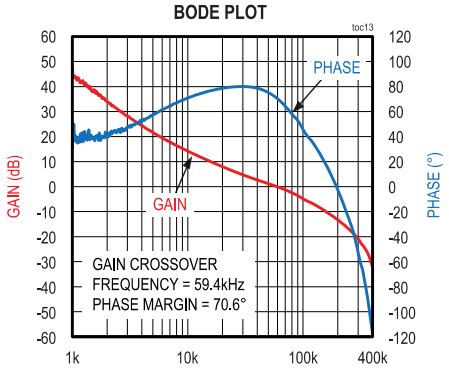
CONDITIONS: PWM/DCM MODE

LOAD TRANSIENT BETWEEN 100mA AND 1A



CONDITIONS: DCM MODE

BODE PLOT



CONDITIONS: 5V OUTPUT, 2.4A LOAD

Component Suppliers

SUPPLIER	WEBSITE
Coilcraft	www.coilcraft.com
Murata Americas	www.murata.com
Panasonic	www.panasonic.com
Vishay Dale	www.vishay.com
TDK Corp.	www.tdk.com
SullinsCorp	www.sullinscorp.com
Taiyo yuden	www.ty-top.com

Note: *Indicate that you are using the ADPL13602 when contacting these component suppliers.*

Ordering Information

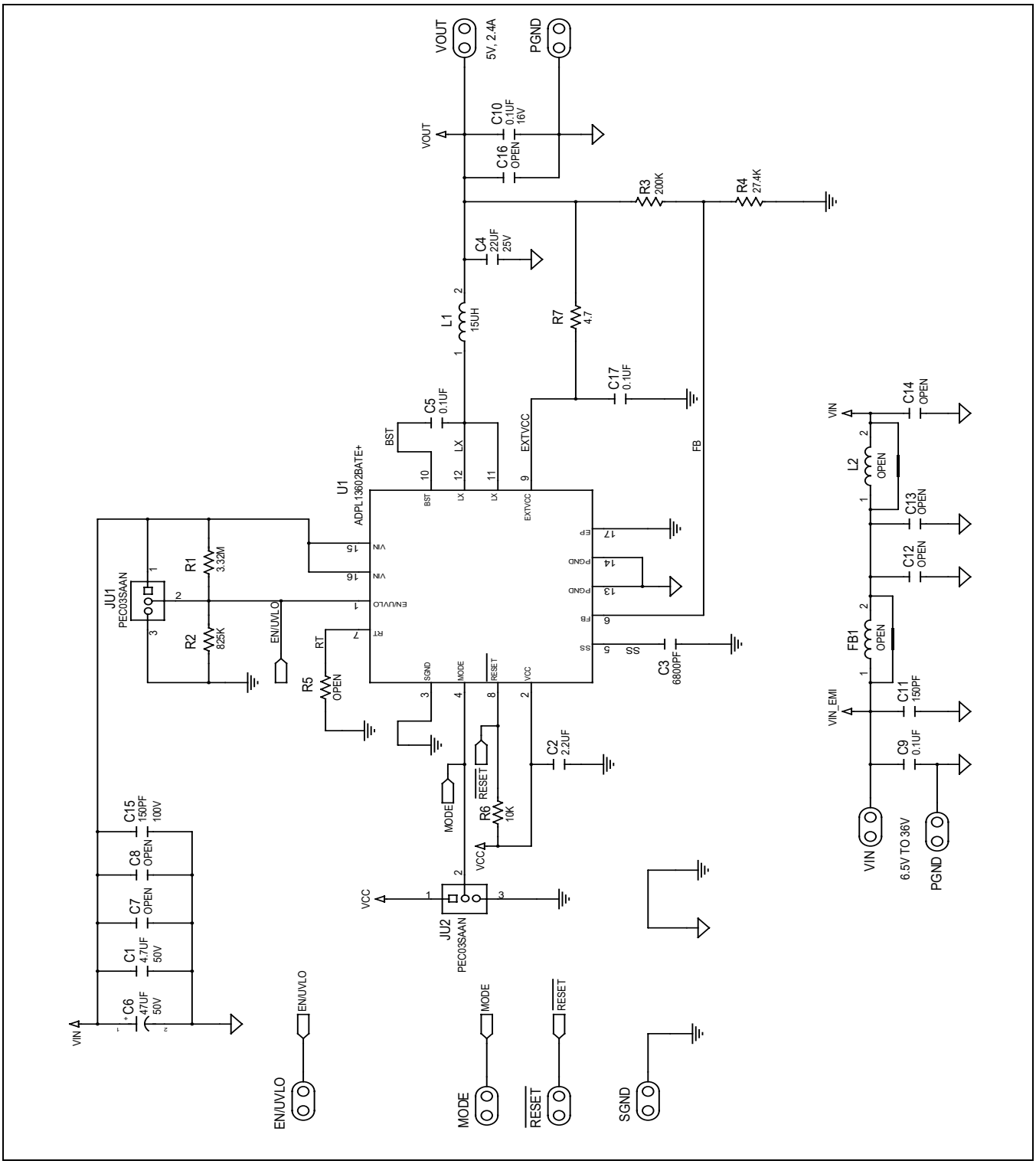
PART	TYPE
ADPL13602EVKIT#	EV kit

ADPL13602EVKIT# Bill of Materials

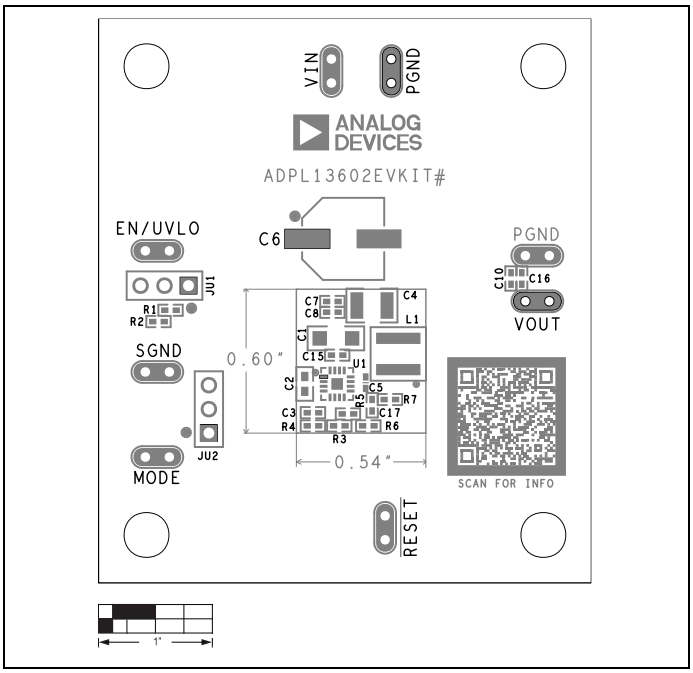
SL. NO	DESIGNATOR	DESCRIPTION	QUANTITY	MANUFACTURER PART NUMBER
1	C1	4.7µF, 10%, 50V, X7R, Ceramic capacitor (1206)	1	MURATA GRM31CR71H475KA12
2	C2	2.2µF, 10%, 10V, X7R, Ceramic capacitor (0603)	1	MURATA GRM188R71A225KE15
3	C3	6800pF, 10%, 50V, X7R, Ceramic capacitor (0402)	1	MURATA GCM155R71H682KA55
4	C4	22µF, 20%, 16V, X7R, Ceramic capacitor (1210)	1	TDK C3225X7R1C226M250AC
5	C5, C10, C17	0.1µF, 10%, 16V, X7R, Ceramic capacitor (0402)	3	TAIYO YUDEN EMK105B7104KV
6	C6	ALUMINUM-ELECTROLYTIC; 47UF; 50V; TOL=20%; MODEL=EEV SERIES	1	PANASONIC EEE-TG1H470UP
7	C9	0.1µF, 10%, 50V, X7R, Ceramic capacitor (0402)	1	TDK C1005X7R1H104K050BE
8	C11, C15	150pF, 5%, 100V, COG, Ceramic capacitor (0402)	2	TDK C1005C0G2A151J050BA
9	L1	INDUCTOR, 15µH, 3.4A (5mm x 5mm)	1	COILCRAFT XGL5050-153ME
10	R1	RES+, 3.32MΩ, 1% (0402)	1	VISHAY DALE CRCW04023M32FK
11	R2	RES+, 825KΩ, 1% (0402)	1	VISHAY DALE CRCW0402825KFK
12	R3	RES+, 200KΩ, 1% (0402)	1	VISHAY DALE CRCW0402200KFK
13	R4	RES+, 27.4KΩ, 1% (0402)	1	VISHAY DALE CRCW040227K4FK
14	R6	RES+, 10KΩ, 1% (0402)	1	BOURNS CR0402-FX-1002GLF
15	R7	RES+, 4.7Ω, 1% (0402)	1	VISHAY DALE CRCW04024R70FK
16	U1	HIGH-EFFICIENCY SYNCHRONOUS STEP-DOWN DC-DC CONVERTER WITH INTERNAL COMPENSATION (TQFN16-EP 3mm x 3mm)	1	ADPL13602BATE+
17	JU1-JU2	3-pin header (36-pin header 0.1” centers)	2	Sullins: PEC03SAAN
18	-	Shunts	2	SULLINS STC02SYAN
19	MH1-MH4	MACHINE FABRICATED; ROUND-THRU HOLE SPACER; NO THREAD; M3.5; 5/8IN; NYLON	4	KEYSTONE 9032
20	C13, C14	OPEN: Capacitor (1206)	0	—
21	L2	OPEN: INDUCTOR	0	—
22	FB1	OPEN: Ferrite Bead (0805)	0	—
23	C7, C8, C12, C16	OPEN: Capacitor (0402)	0	—
24	R5	OPEN: Resistor (0402)	0	—

DEFAULT JUMPER TABLE	
JUMPER	SHUNT POSITION
JU1	Open
JU2	2-3

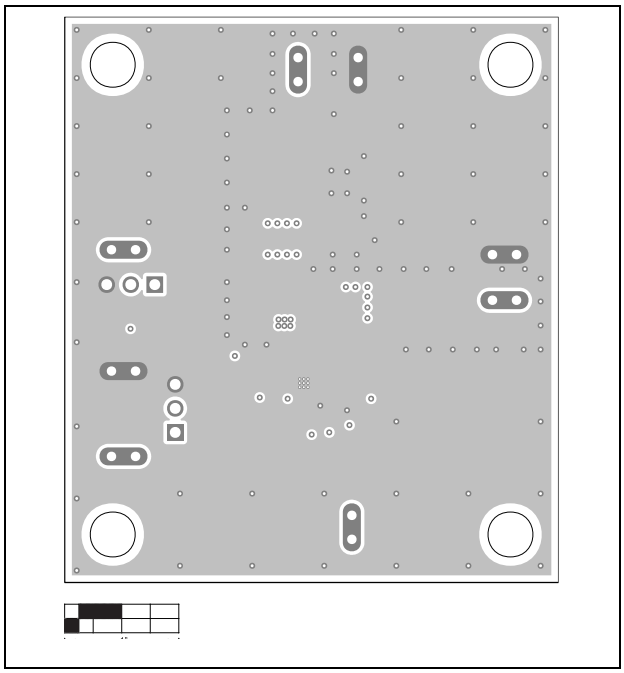
ADPL13602EVKIT# Schematic



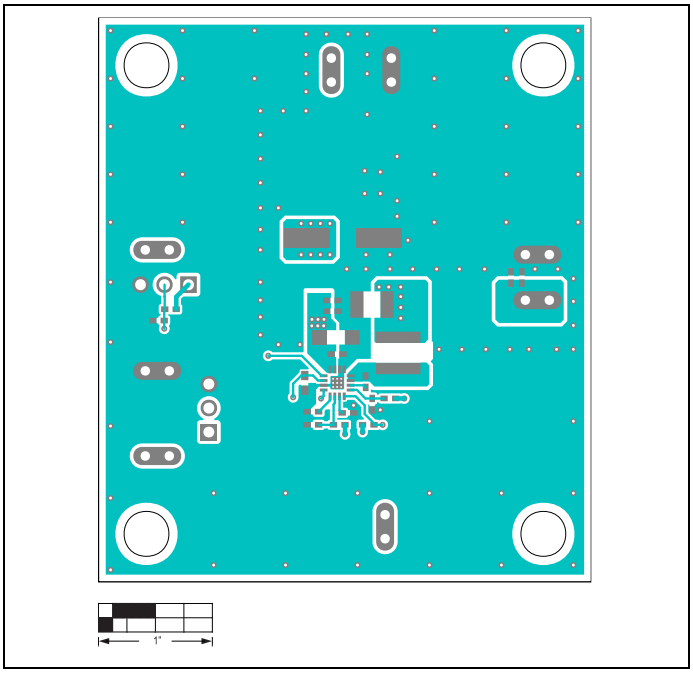
ADPL13602EVKIT# PCB Layout Diagram



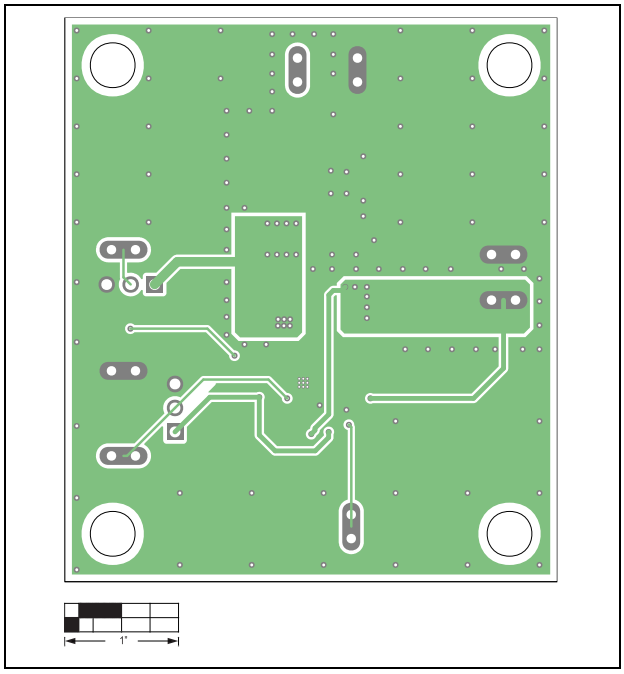
ADPL13602EVKIT# —Top Silkscreen



ADPL13602EVKIT# —Layer 2

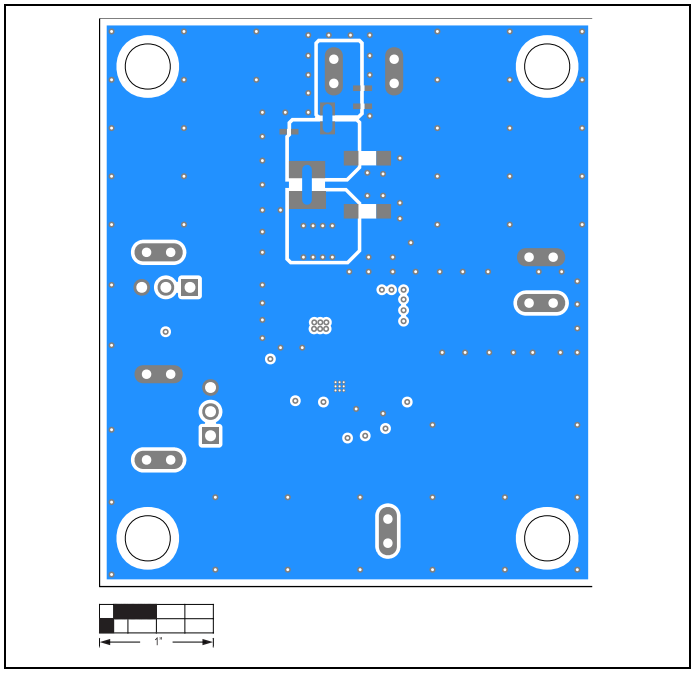


ADPL13602EVKIT# —Top Layer

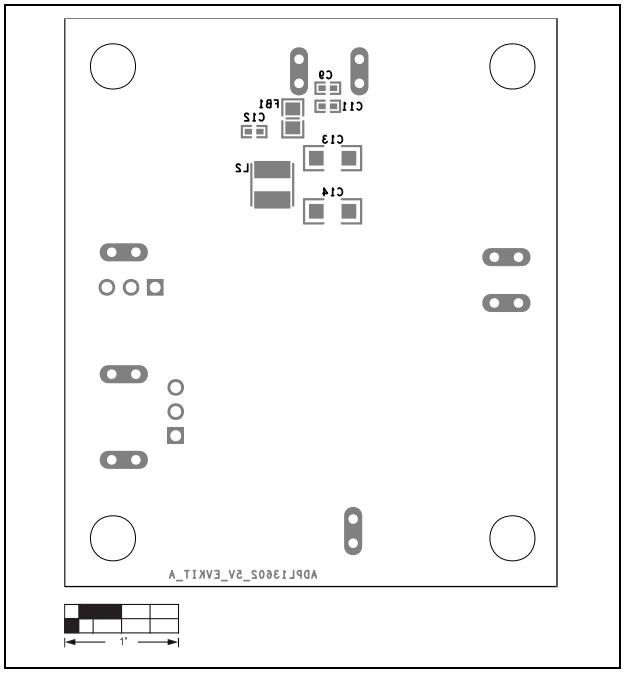


ADPL13602EVKIT# —Layer 3

ADPL13602EVKIT# PCB Layout Diagram (continued)



ADPL13602EVKIT# —Bottom Layer



ADPL13602EVKIT# —Bottom Silkscreen

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/23	Initial release	—