TI Designs：TIDA-01576
采用双同步采样 ADC 的隔离式 16 通道交流模拟输入模块参考设计

说明

此参考设计可在宽输入范围内使用精密的 16 位 SAR ADC 准确测量 16 通道交流电压和电流输入。该范围涵盖了保护和测量要求（包括符合 IEC 61850-9-2 的采样要求），可简化系统设计并改善跳闸时间可重复性、性能和可靠性。此参考设计使用带有集成电源转换器的数字隔离器或使用六通道数字隔离器将模拟输入模块 (AIM) 与主机处理器相隔离。在最简单的配置中，仅使用五个 TI 产品即可设计出完整的 AC AIM，因此可优化系统成本和尺寸。警报功能可基于样本确定交流 AIM 故障，从而更快地检测故障。ADC 具有额外的辅助通道可用于诊断数字隔离器电源的输出，或用于为测得的模拟输入进行温度漂移补偿。

资源

TIDA-01576	设计文件夹
ADS8688	产品文件夹
ADS8688A	产品文件夹
ISOW7841	产品文件夹
ISO7763	产品文件夹
SN6505b	产品文件夹
TPS3836K33	产品文件夹
LM35	产品文件夹
LMT70	产品文件夹
REG71055	产品文件夹
REF5040	产品文件夹
REF6041	产品文件夹
ISO7820	产品文件夹
TPS79101	产品文件夹
TPS7A4901	产品文件夹
ISO7820	产品文件夹

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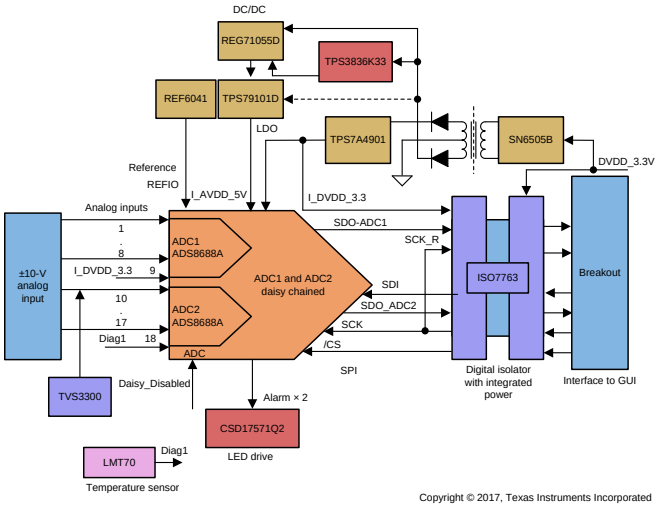
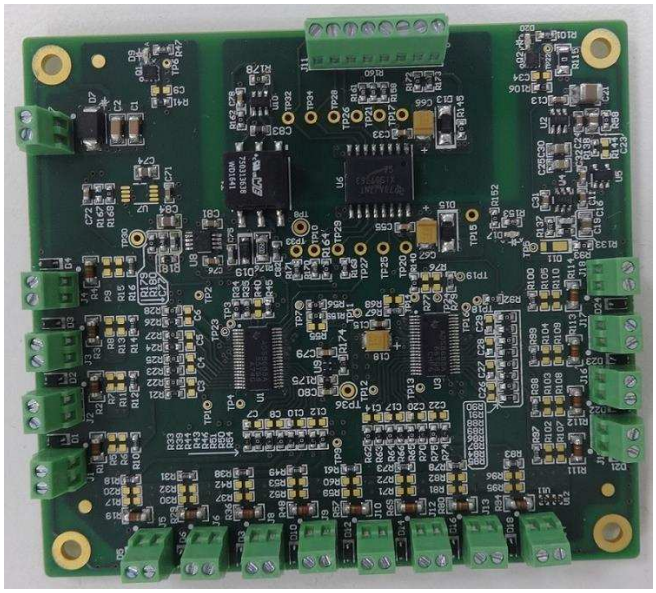
特性

- 交流 AIM 提供 ENOB 大于 14.9 位、SNR 大于 91dB 且 THD 大于 –110dB 的频谱性能，并具有隔离接口和 ±0.2% 以内的测量精度
- 基于 ADS8688A 16 位 ADC（与 ADS8668 或 ADS8698 兼容），并采用菊链方式连接两个 ADC 或在双 SDO 输出配置中连接两个 ADC 以支持多达 16 路模拟输入
- 使用具有集成电源转换器（提供大于 60mA 的电流输出且效率不低于 45%）的 ISOW7841 数字隔离器或将 ISO7763 数字隔离器与外部隔离式电源相结合，使 ADC 接口与主机实现隔离以提高严苛工作条件下的系统安全性
- 诊断 特性 包括监控电源输出和纹波、电压监控器、板载温度传感器以及电源和警报输出 LED
- 四层电路板采用基于拼接电容器的板面布局，能够根据 CISPR 22 要求降低辐射发射
- 精密主机接口 (PHI) 处理器板使用分线板连接到设计和 GUI，便于快速评估性能
- 用 GUI 进行相位补偿以实现对输入样本的同时采样

应用

- 多功能保护继电器
- 变电站间隔控制器
- 独立合并单元 (SAMU)
- RTU、FTU、DTU 或 FRTU
- 适用于工厂自动化的 PLC





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1 System Description

Power system failures is one of the common problems faced by power generation, transmission, and distribution companies. Power outages result in loss of revenue and reduces generation capacity. Power utilities are working towards providing reliable power by using secondary protection, control, monitoring, and measurement systems to the power systems efficiency and reliability.

1.1 Introduction to Protection Relays

Digital protection relays detect defective lines, equipment, or other power system conditions that are abnormal or dangerous in nature. Digital protection relays detect and locate faults by measuring electrical quantities in the power system, which is different during normal and intolerable conditions. Measuring AC voltage and current inputs accurately over a wide input range is critical for the digital protection relays. The major functional components of a digital protection relay include data acquisition (analog filtering and sampling), measurement (phasor estimation), and logic (tripping, alarming, carrier send, and so on).

1.1.1 Multifunction Protection Relay for Generation, Transmission, or Distribution Applications

The key inputs for the functioning of the protection relay are AC voltages and currents. Most of the protection algorithms are based on the amplitude, frequency, and the phase of the AC voltages and currents. The AC AIM captures the output of the voltage and current transformers connected across the equipment being monitored. Depending on the monitored equipment and the protection function configured, the number of analog inputs can be 4, 8, 12, or 16.

1.1.2 Stand-Alone Merging Unit

The merging unit captures the voltage and current inputs from the equipment it connects to and provides the digital data to different IEDs using IEC 61850-9-2 protocol. Depending on the monitored equipment, the number of analog inputs can be 4, 8, 12, or 16.

1.1.3 Substation Bay Controller and Terminal Unit

The bay controller monitors analog and digital inputs from different primary equipments connected on the bay in a substation. The number of analog inputs depends on the bay controller configuration and can vary from 8 to 24.

1.2 Key System Specifications

表 1 shows the key system specifications for the isolated, high-accuracy, 16-channel AIM reference design.

表 **1. Key System Specifications**

SERIAL NUMBER	PARAMETER	DESCRIPTION	COMMENT
1	ADC	16-bit SAR ADC with configurable input ranges	SPI
2	Number of channels	16 channels by daisy chaining multiple ADCs or using individual SDO outputs	Additional aux channels for diagnostics
3	Input range	±10.24 V, ±5.12 V, ±2.56 V	With programmable input ranges
4	Sampling rate	500 kHz max per ADC in dual SDO configuration	Meets IEC 61850-9-2 sampling requirements for protection and measurement
5	Input impedance	> 1 MΩ	Same for all the input ranges
6	Digital isolation	Digital isolator with integrated power	Reinforced
7		Six-channel digital isolator with external isolated power	Reinforced, provides flexibility in digital isolator selection
8	ADC SCLK return	Clock return signal provided from the ADC side to the host side	
9	Reference	External reference with op amp buffer	Depends on performance requirement
		External reference with integrated buffer	Depends on performance requirement
10	Host interface	SPI	Simplifies isolated communication interface
11		Screw-type terminals for connecting to host	
12	Diagnostics	Digital and analog power supply using auxiliary channels	Displayed on GUI
13		LED indication for alarm, power, and activity (chip select)	Visual indication
14	Power supply	Onboard DC/DC and LDO	With low ripple
15		Isolated power using transformer driver	Efficiency > 60%
16	Temperature compensation	Onboard analog temperature sensor for compensation of onboard temperature variation	Accuracy < ± 0.2%
17	Analog input connectors	8 × 2-pin screw terminal block for analog input connection for each ADC, 2-pin for protective earth connection	

2 System Overview

This reference design accurately measures AC voltage and current inputs using a precision 16-bit successive approximation (SAR) analog-to-digital converter (ADC) over a wide input range covering protection and measurement range (including sampling requirements of IEC 61850-9-2), simplifying system design and improving trip time performance and reliability. The AIM is isolated from the host processor using a digital isolator with an integrated power converter. A complete AC AIM can be designed using only TI products, optimizing system cost and size. The alarm feature identifies the AC analog input faults on a sample basis for faster fault detection. The ADC has an additional auxiliary channel to diagnose the supply output of the digital isolator. Two ADCs have been connected together to increase the number of analog input channels to 16 using daisy chain mode or dual SDO output mode with the input signals connected together and driven by common pins.

2.1 Block Diagram

This reference design showcases the following configurations for improved system performance:

- ADS8688A-based, 16-channel input with dual SDO for measurement of AC or DC analog input
- ADS8688A-based, isolated, 16-channel input with dual SDO with integrated power
- ADS8688A-based, isolated, 16-channel input with dual SDO using 6-channel digital isolator

Choose the design architecture based on the accuracy and board size requirements.

2.1.1 ADS8688A-Based, 16-Channel AC AIM With Dual SDO

The ADS8688A-based, 16-channel AC AIM with dual SDO has the following functional blocks:

- 2× ADS8688A ADCs connected together to sample 16 channels of AC analog input with a ±10.24-V input range
- External reference for improving measurement accuracy between two ADCs
- LDOs to generate the required analog and digital power supply
- Host interface with dual SDO outputs
- LEDs driven by MOSFET for Alarm indication
- Host interface and GUI for evaluating the performance of the ADC

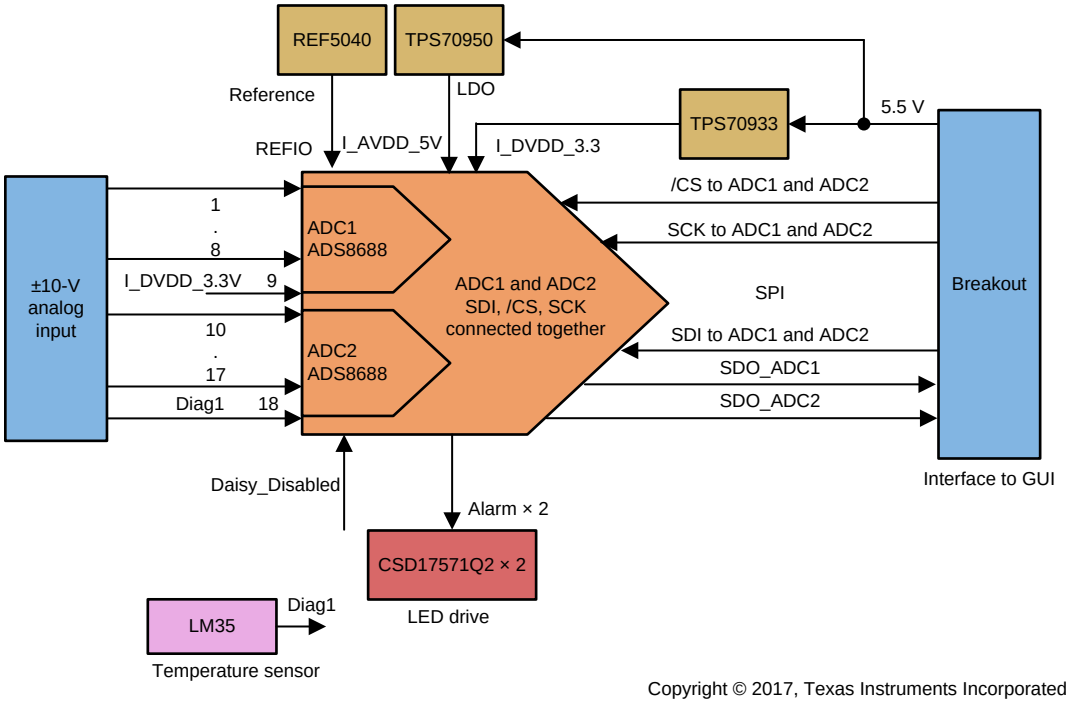

图 1. ADS8688A 16-Bit SAR ADC-Based 16-Channel AC AIM With Dual SDO Output

2.1.2 ADS8688A-Based, Isolated, 16-Channel AC AIM With Dual SDO and Digital Isolator With Integrated Power

The ADS8688A-based, isolated, 16-channel AC AIM with a dual SDO, digital isolator, and integrated power block diagram has the following functional blocks:

- ADS8688A-based, 16-channel input with dual SDO to measure AC or DC analog inputs with a ±10.24-V input range
- Host interface isolation provided using four-channel digital isolator with integrated power and two-channel digital isolator
- Provision for SCKL loop back from the ADC side to the host side for improved performance
- DC/DC converter and LDO to provide the required analog and digital power supply to the module
- Analog temperature sensor to compensate the measurement error due to ambient temperature variation
- Reference with integrated buffer for providing external reference to the ADCs for improved performance
- Host interface to evaluate the performance of the ADC using a PHI card and GUI

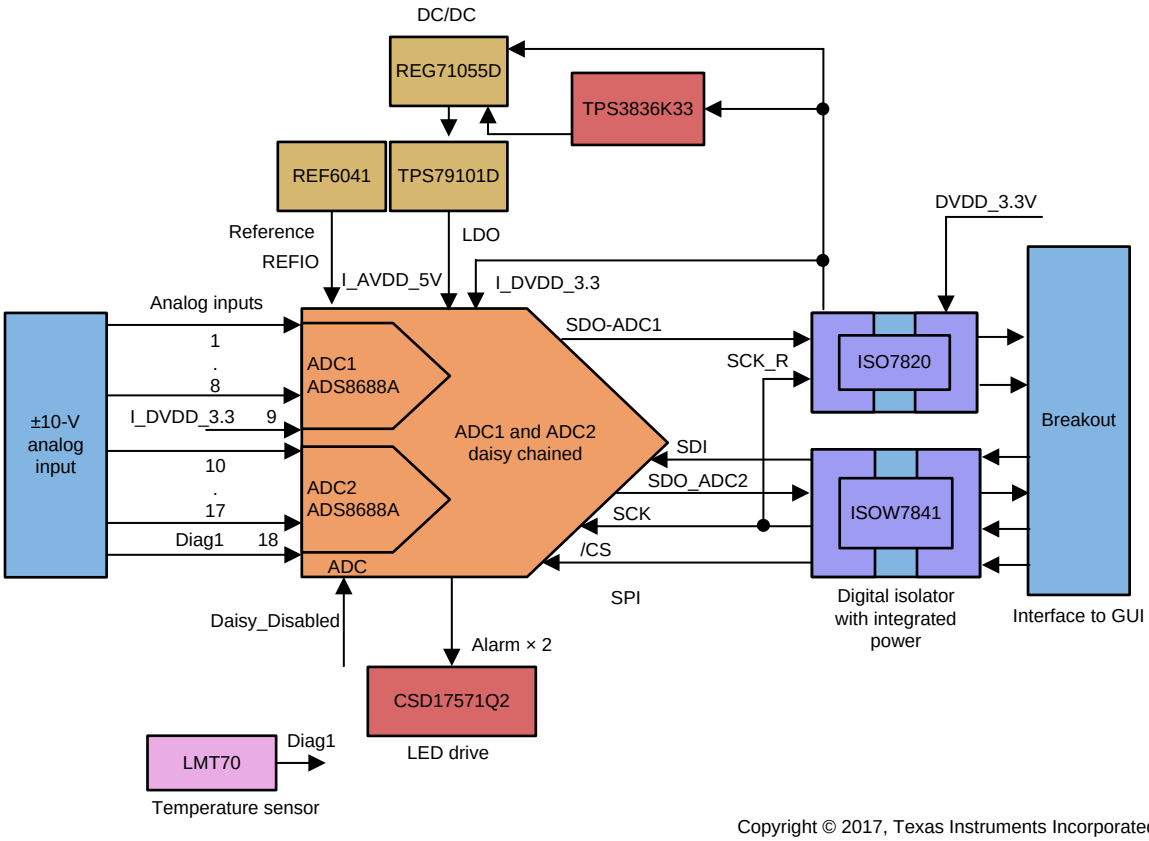

图 2. ADS8688A 16-Bit SAR ADC-Based, Isolated 16-Channel AC AIM With ISOW7841 and Dual SDO

2.1.3 ADS8688A-Based Isolated 16-Channel Input With Dual SDO Using ISO7763 Six-Channel Digital Isolator

The ADS8688A-based, isolated, 16-channel input with dual SDO using ISO7763 six-channel digital isolator block diagram has the following functional blocks:

- ADS8688A-based 16-channel input with dual SDO to measure AC or DC analog inputs with a ±10.24-V input range
- Host interface isolation provided using six-channel digital isolator
- Isolated power generated using transformer driver
- Provision for SCKL loop back from the ADC side to the host side for improved performance
- DC/DC converter and LDO to provide the required analog and digital power supply to the module
- Analog temperature sensor to compensate the measurement error due to temperature variation
- Reference with integrated buffer for providing external reference to the ADC for improved performance
- Host interface and GUI for evaluating the performance of the reference design

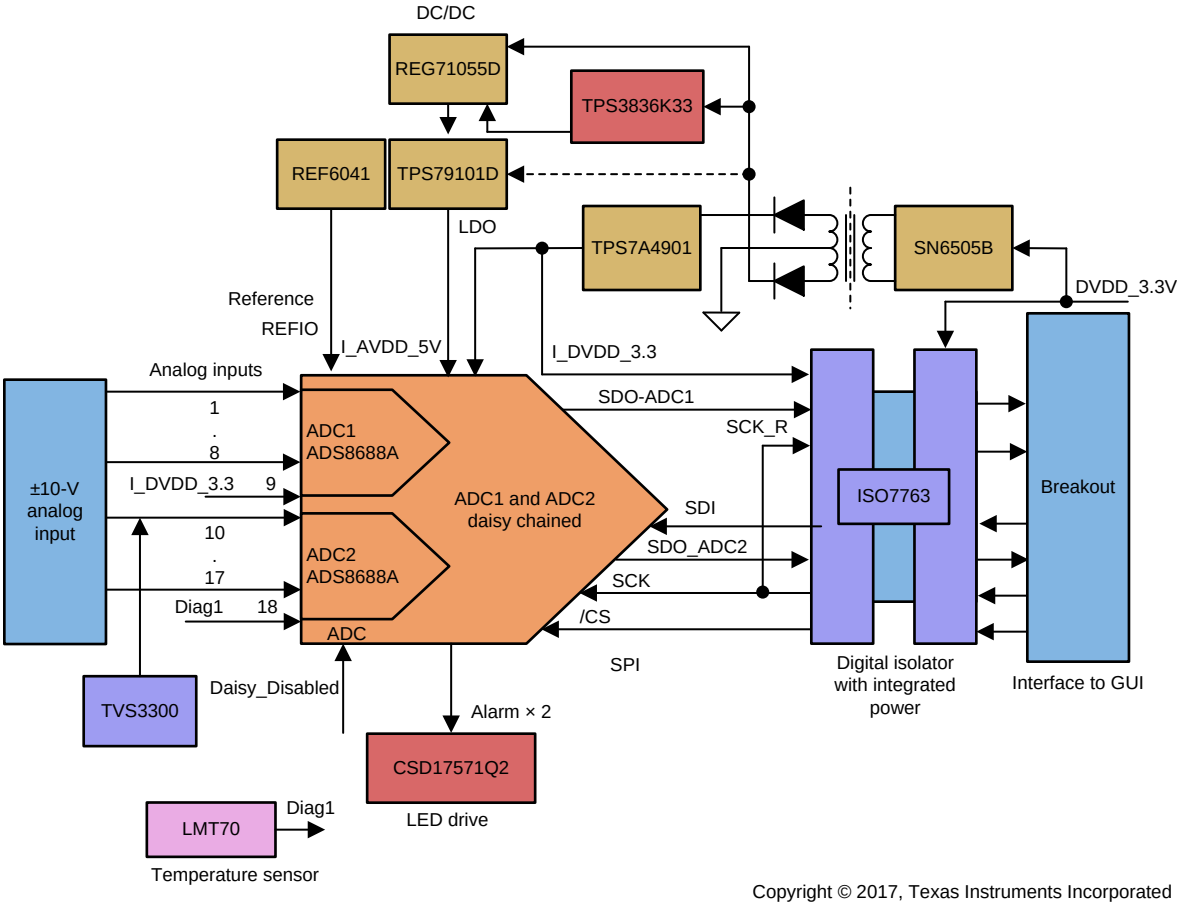

图 3. ADS8688A 16-Bit, SAR ADC-Based, Isolated AC AIM Using Six-Channel Digital Isolator

2.1.4 Precision ADC With External Reference

The key subsystem for the AC AIM is the ADC used to measure up to 16 inputs. A 16-Bit ADC ADS8688 or ADS8688A with an alarm output can be used to measure wide inputs using the internal programmable input ranges. The reference internal to the ADC that has low drift can be used for measurement. Alternatively, for improved performance, an external reference REF5025 with the buffer OPA322 can be used or REF6025 with an internal buffer can be used.

2.1.5 Digital Isolator

The isolated interface for the AC AIM is designed using digital isolators. The ADCs have SPI with /CS, CLK, SDI, SDOA, and SDOB signals. A four-channel digital isolator ISOW7841 with reinforced isolation and integrated power can be used along with a two-channel digital isolator or a six-channel digital isolator with external power can be used. For design flexibility, digital isolators with external isolated power can also be considered. The ISO7841 or ISO7763 can provide the required isolation.

2.1.6 Power Supply

The output of the ISOW7841 is configured to provide 3.3 V. The output is used for ADC digital interface supply DVDD. The 3.3 V is stepped to the 5-V analog supply using the 5.5-V boost converter REG71055 and TPS71750 LDO. A transformer driver SN6505 can generate an isolated power supply as an alternative to the power converter integrated with the digital isolator when using a six-channel digital isolator.

2.2 Design Considerations

2.2.1 AC Current and Voltage Measurement Module

The data acquisition function in the protection relay is performed by the AC AIM and consists of the following subsystems.

2.2.1.1 Current Sensor Input

Current measurement sensors that can be used include current transformers, shunts, Rogowski coils, Hall effect or flux gate current sensors, optical current transformers, or low-power current transformers (LPCTs). In applications using shunt for current sensing, the required isolation is provided by the isolation amplifier or isolated delta-sigma modulator.

2.2.1.2 Voltage Sensor Input

Voltage measurement sensors that can be used include potential transformers, potential dividers, or capacitor voltage transformers. In applications, using potential divider for voltage measurement, the required isolation can be provided by the isolation amplifier or isolated delta-sigma modulator.

2.2.1.3 Signal Conditioning

A signal conditioning circuit is used to scale the voltage or current sensor output to the ADC range. A signal conditioning circuit depends on its application. The circuit can be a precision operational amplifier, instrumentation amplifier, programmable gain amplifier, or a differential or isolation amplifier. The amplifier selection depends on the accuracy and temperature drift requirements.

2.2.1.4 Host Interface

The ADC is interfaced to a host that captures the digital values from the ADC and computes the electrical parameters used for protection, measurement, and control and monitoring applications.

2.2.1.5 ADC

Accurate measurements of voltage and current inputs are key performance requirements for grid infrastructure applications. Selecting an ADC is critical to the digital protection relay performance, and the measurement accuracy for protection, monitoring, and control depends on the ADC selection. Key performance parameters for ADC selection include ADC architecture, ADC resolution, ADC input sampling method, ADC input type and range, ADC power supply, clock, and reference. Another important ADC requirement is scaling the sampling rate to meet IEC 61850-9-2 standards for both protection and measurement.

2.2.2 Need for Isolation, Challenges, and Solutions

Power system equipment that fail are responsible for a large proportion of power system outages and associated interruption of electricity supply to customers. Other causes of interruption include extreme weather conditions, among others. If failures can be predicted before they occur, action can be taken to reduce the occurrence of unplanned outages of equipment, thus contributing to meeting performance targets and reducing the cost of interruptions. The inputs are isolated using an isolation amplifier, isolated delta-sigma modulators, or current or potential transformers. Some of the common requirements for isolation of an AC AIM include isolation type (basic or reinforced), jitter in pS, power supply integrated with an isolator or external, and the number of channels for an I^2C, SPI, or UART interface.

2.2.3 Reference Design Advantage

This reference design using the ADS8688A with daisy chain or with dual SDO output provides the following advantages during the design of the AC AIM:

- Meets ADC dynamic specification including ENOB, SNR, and THD with isolated interface
- Can measure 16 channels of analog inputs with programmable input ranges
- Provides isolation of the interface using a digital isolator with integrated power or external isolated power
- Simplifies overall design by use of six channel digital isolator in a 16-pin
- Allows looping back the clock from the ADC side to the host side for improved measurement performance with a higher clock output
- Simplifies the power supply design through isolated power and improves efficiency through external isolated power
- Has programmable input ranges to scale the input range based on the sensor output
- The performance can be scaled to >19 bits by using the programmable internal ranges
- Can measure bidirectional inputs up to ±10.24 V using a single 5-V analog input
- Provides options for power supply diagnostics (analog and digital supply) and alarm indication
- Interfaces to the host using a simple SPI with dual SDO output or daisy chained mode

2.3 Highlighted Products—System Design

2.3.1 Precision Dual ADC

图 4 shows the ADC used and the configuration.

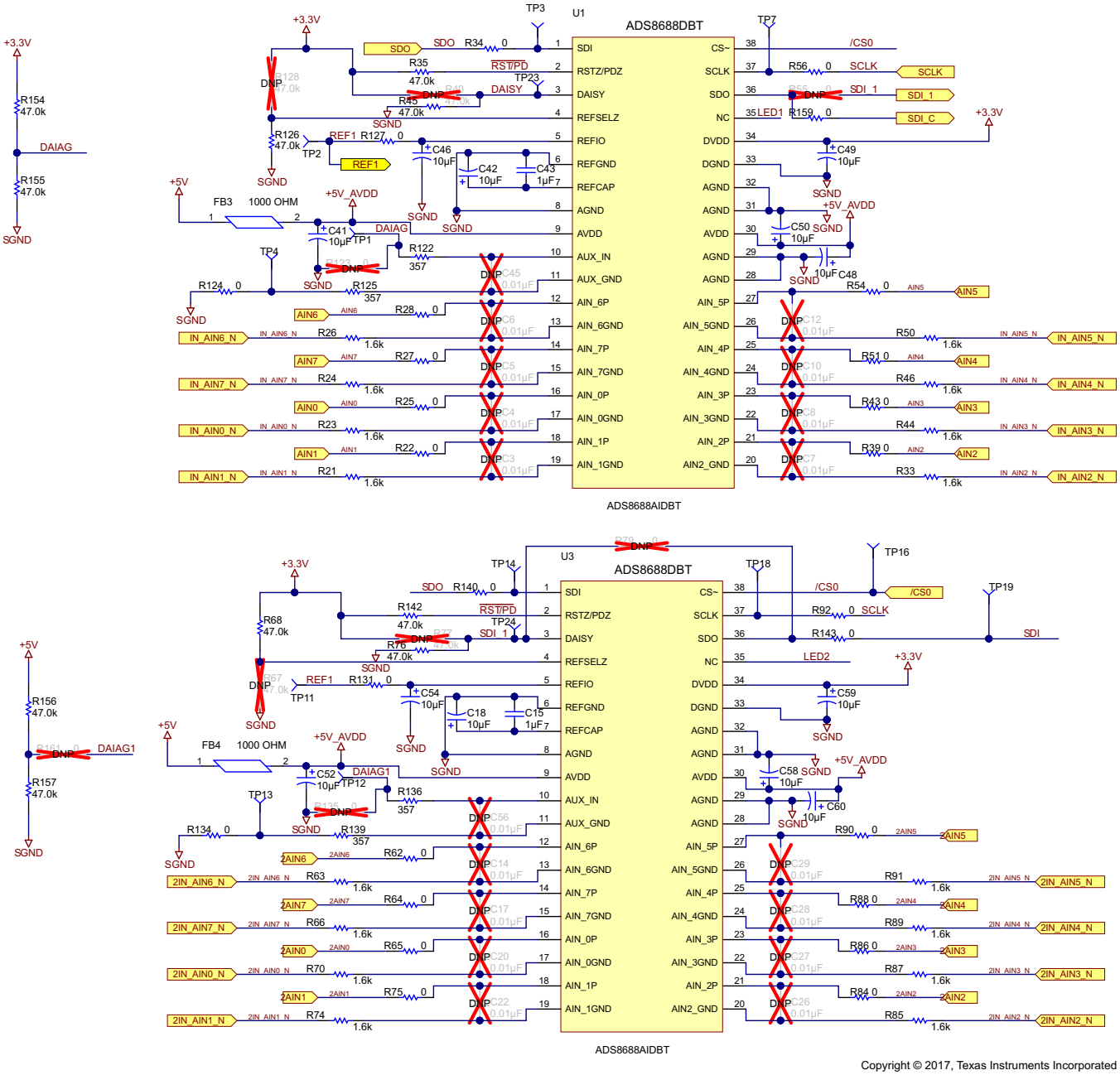

图 4. Schematic of ADS8688A Interface

2.3.1.1 16-Bit ADC ADS8688

The ADS8688 is an eight-channel, integrated data acquisition system based on a 16-bit SAR ADC, operating at a throughput of 500 kSPS. The devices feature integrated analog front-end circuitry for each input channel with overvoltage protection up to ±20 V, an eight-channel multiplexer with automatic and manual scanning modes, and an on-chip, 4.096-V reference with low temperature drift. Operating on a single 5-V analog supply, each input channel on the devices can support true bipolar input ranges of ±10.24 V, ±5.12 V, and ±2.56 V. The input range selection is software-programmable and independent for each channel. The devices offer a 1-MΩ constant resistive input impedance irrespective of the selected input range. The ADS8688 offers a simple SPI-compatible serial interface to the digital host and also support daisy-chaining of multiple devices. The digital supply operates from 1.65 to 5.25 V, enabling direct interface to a wide range of host controllers.

For more details, see the ADS8688 product page.

2.3.1.2 16-Bit ADC ADS8688A With Alarm Output

The ADS8688A is a eight-channel, integrated data acquisition system based on a 16-bit SAR ADC, operating at a throughput of 500 kSPS. Operating on a single 5-V analog supply, each input channel on the devices can support true bipolar input ranges of ±10.24 V, ±5.12 V, ±2.56 V, ±1.28 V, and ±0.64 V.

For more details, see the ADS8688A product page.

2.3.1.3 Low-Noise, Low-Drift, High-Precision Reference REF5040

The REF5040 is a low-noise, low-drift, very high-precision voltage reference. This reference is capable of both sinking and sourcing current and has excellent line and load regulation. Excellent temperature drift (3 ppm/°C) and high accuracy (0.05%) are achieved using proprietary design techniques. Combined with very low noise, these features make the REF5040 ideal for use in high-precision data acquisition systems.

For more details, see the REF5040 product page.

2.3.1.4 High-Precision Voltage Reference With Integrated High-Bandwidth Buffer REF6041

The REF6041 voltage reference has an integrated, low-output impedance buffer that enables the user to directly drive the REF pin of precision data converters while preserving linearity, distortion, and noise performance. Most precision SAR and Delta-Sigma ADCs switch binary-weighted capacitors onto the REF pin during the conversion process. To support this dynamic load, the output of the voltage reference must be buffered with a low-output impedance (high-bandwidth) buffer. The REF6000 family devices are well suited, but not limited, to drive the REF pin of the ADS88xx family of SAR ADCs and ADS127xx family of delta-sigma ADCs.

For more details, see the REF6041 product page.

2.3.2 Interface Isolation Using Digital Isolator With Integrated Power ISOW7841 Family

This section provides information on different digital isolator options to consider for the design of the AC AIM.

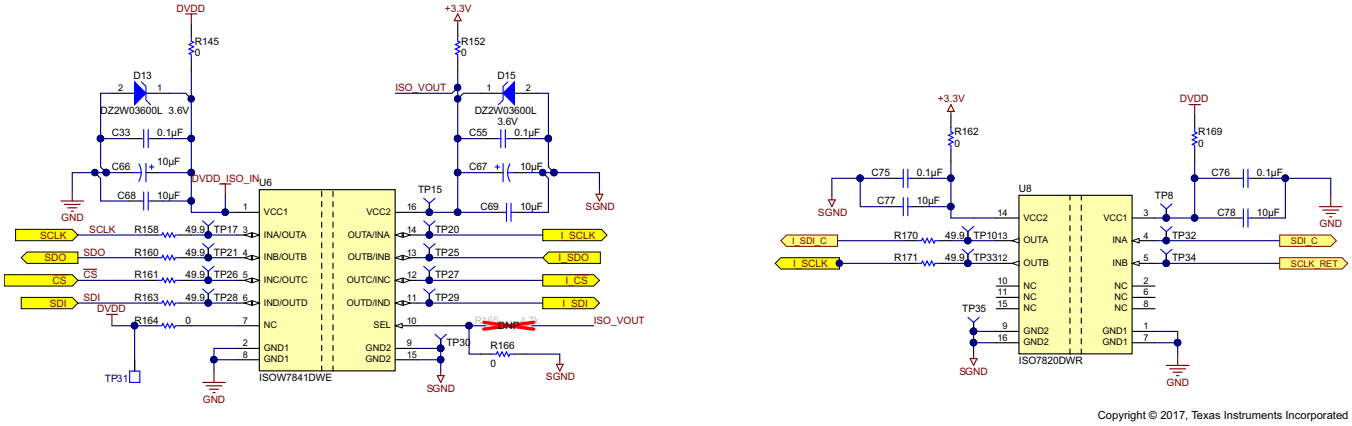

图 5. Schematic of ISOW7841 Configuration for ADC Interface

2.3.2.1 *Digital Isolator With Integrated Power ISOW7841*

The ISOW7841 is a high-performance, quad-channel reinforced digital isolator with an integrated high-efficiency power converter. The integrated DC/DC converter provides up to 650 mW of isolated power at high efficiency and can be configured for various input and output voltage configurations. Therefore, these devices eliminate the need for a separate isolated power supply in space-constrained isolated designs.

For more details, see the ISOW7841 product page.

2.3.2.2 *Digital Isolator ISO7820*

The ISO7820 is a high-performance, dual-channel digital isolator with 8000-V_{PK} isolation voltage. The isolator provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. The ISO7820 device has two forward channels and no reverse-direction channel. If the input power or signal is lost, the default output is ‘high’ for the ISO7820 device and ‘low’ for the ISO7820F device. Used in conjunction with isolated power supplies, this isolator prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

For more details, see the ISO7820 product page.

2.3.3 Interface Isolation Using Digital Isolator ISO7763 Family

This section provides information on different digital isolator options to consider for the design of the AC AIM.

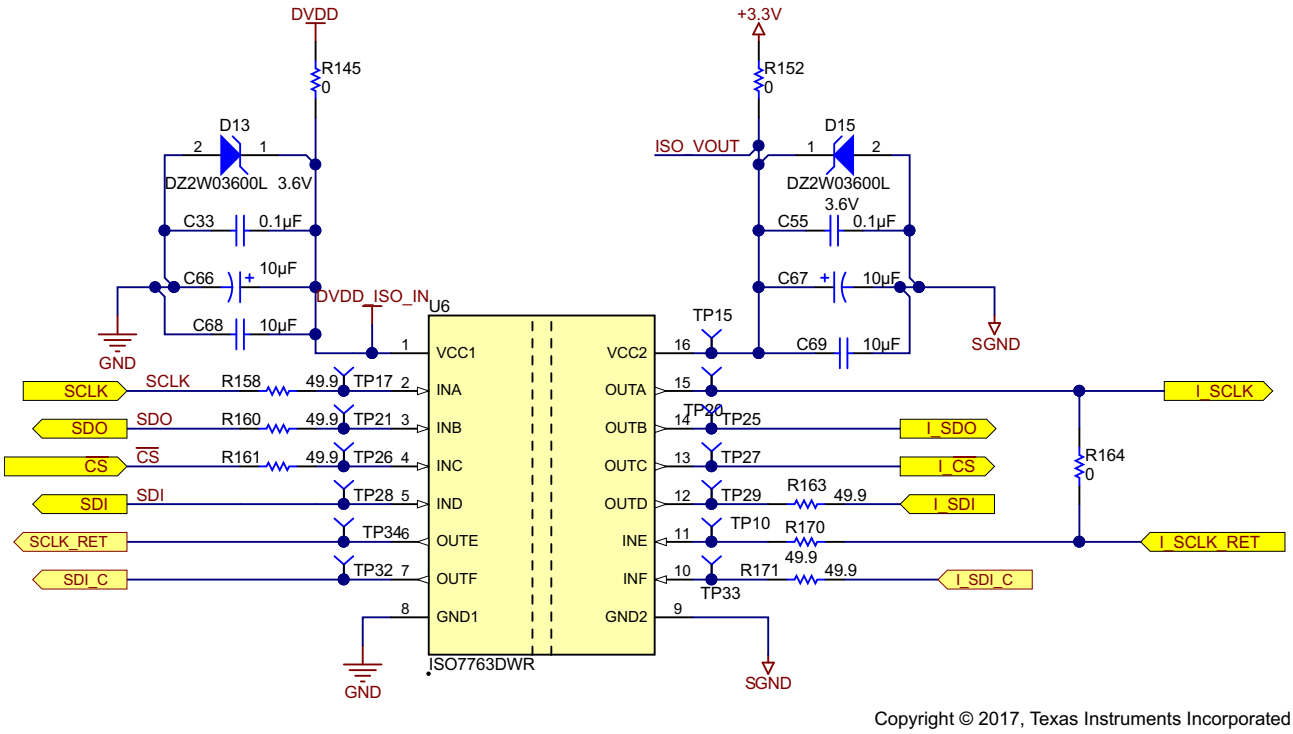

图 **6. Schematic of ISO7763 Configuration for Dual SDO Interface**

2.3.3.1 Digital Isolator ISO7763

The ISO776x devices are high-performance, six-channel digital isolators with 5000-V_{RMS} (DW package) isolation ratings per UL 1577. The ISO776x family of devices provides high-electromagnetic immunity and low emissions at low-power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic-input and logic-output buffer separated by a silicon dioxide (SiO_2) insulation barrier. The ISO776x family of devices is available in all possible pin configurations such that all six channels are in the same direction, or one, two, or three channels are in reverse direction while the remaining channels are in forward direction. Used in conjunction with isolated power supplies, this family of devices helps prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, the electromagnetic compatibility of the ISO776x family of devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance.

For more details, see the ISO7763 product page.

2.3.4 Power Supply

The ISOW7841 device can generate the required isolated power supply. An alternative approach to isolate the AIM from the host is to use a digital isolator and isolated power generated using a transformer driver.

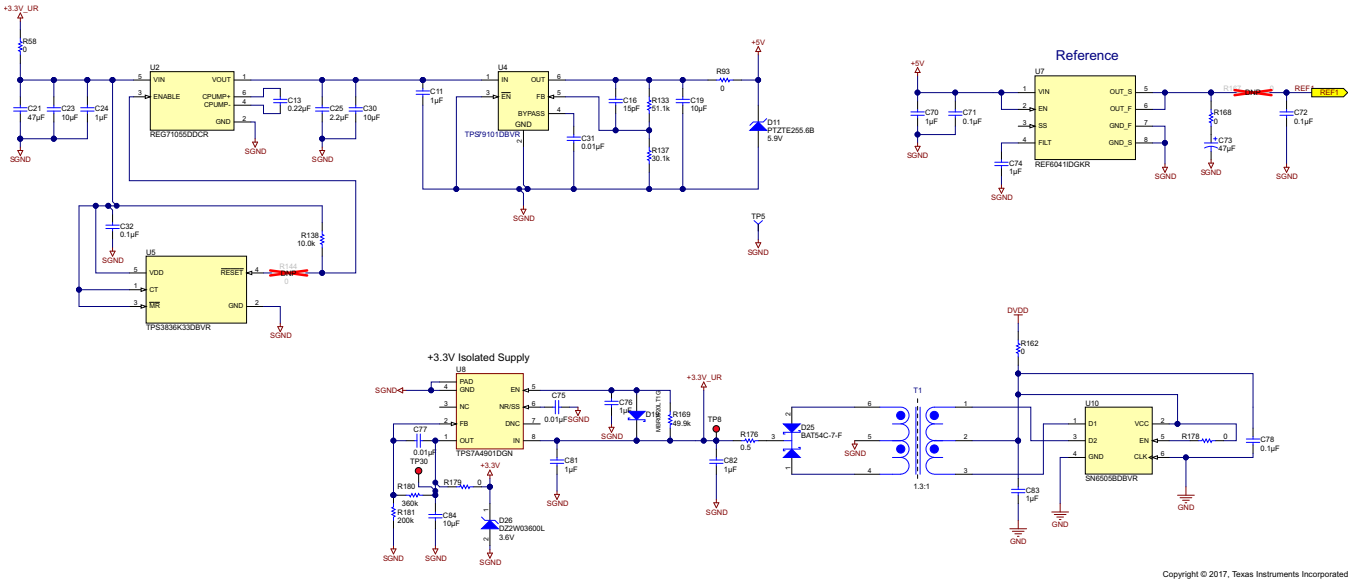

图 7. Schematic of ADC Analog and Digital Power Supply

2.3.4.1 5-V AVDD

This section provides details for generating a 5-V power supply for the ADCs.

2.3.4.1.1 REG71055

The REG71055D is a switched capacitor voltage converter that generates regulated, low-ripple output voltage from an unregulated input voltage. A wide input supply voltage from 1.8 to 5.5 V can be applied. The input voltage may vary above and below the output voltage and the output remains in regulation. The device works as step-up or step-down converters without the need of an inductor, providing low EMI DC/DC conversion.

For more details, see the REG71055 product page.

2.3.4.1.2 Isolated Power Supply Using Transformer Driver SN6505B or SN6501

The SN6505B is a low-noise, low-EMI push-pull transformer driver, specifically designed for small form factor, isolated power supplies. This device drives low-profile, center-tapped transformers from a 2.25- to 5-V DC power supply. The SN6505B includes a soft-start feature that prevents high inrush current during power-up with large load capacitors.

For more details, see the SN6505B product page.

2.3.5 Diagnostics and Protection

The following subsections describe the diagnostics and protection features.

2.3.5.1 Load Switch TPS22944

The TPS22944 load switch protects systems and loads in high-current conditions. The device contains a 0.4-Ω current-limited P-channel MOSFET that can operate over an input voltage range of 1.62 to 5.5 V. The load switch prevents current from flowing when the MOSFET is off. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals. The TPS22944 includes thermal shutdown protection that prevents damage to the device when a continuous overcurrent condition causes excessive heating by turning off the switch.

For more details, see the TPS22944 product page. For details on the selection of load switches based on the power requirements, see 表 2.

表 2. Load Switch Selection Options

SERIAL NUMBER	PART NUMBER	DESCRIPTION
1	LM34902	300-mA Current Limited Power Switch
2	TPS2010	0.4-A, 2.7- to 5.5-V, Single High-Side MOSFET Switch IC, No Fault Reporting, Active-Low Enable
3	TPS22946	5.5-V, 0.2-A, 400-mΩ Selectable Current Limit Load Switch

2.3.5.2 Power-on Reset TPS3836K33

The TPS3836 family of supervisory circuits provides circuit initialization and timing supervision, primarily for DSP and processor-based systems. During power-on, RESET is asserted when the supply voltage VDD becomes higher than 1.1 V. Then, the supervisory circuit monitors VDD and keeps the RESET output active as long as VDD remains below the threshold voltage of VIT. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after VDD has risen above the threshold voltage VIT.

For more details, see the TPS3836K33 product page.

2.3.6 Board Layout With ISOW7841

The ISOW7841 integrated signal and power isolation device simplifies system design and reduces board area. The use of low-inductance micro-transformers in the ISOW7841 device necessitates the use of high-frequency switching, resulting in higher radiated emissions compared to discrete solutions. The ISOW7841 device uses on-chip circuit techniques to reduce emissions compared to competing solutions. Techniques such as lower supply operation, using interlayer stitching capacitance, filters, and common-mode chokes can further reduce radiated emissions at the system level.

For more details, see *Low-Emission Designs with ISOW7841 Integrated Signal and Power Isolator*.

2.3.7 Design Enhancements

The following subsections provide some of the design enhancement options.

2.3.7.1 Non-Simultaneous Sampling ADC Phase Compensation

The design uses a 16-bit, multiplexed input (non-simultaneous sampling) SAR based ADC with an integrated AFE circuit simplifying system hardware design and minimizing the number of components used. An additional phase delay is introduced between the input channels of a non-simultaneous sampling ADC as compared to simultaneous sampling ADC. The phase delay can be compensated in the software. In this design phase, correction is applied to all the analog channels and the results are provided.

A precision design implements an optimum software solution to compensate for the phase delay, and the same procedure is used to compensate 16 channels. For more details, see the *Phase-Compensated, 8-Ch, Multiplexed Data Acquisition System for Power Automation Reference Design*.

2.3.7.2 Multiplexed ADS86xx ADC Selection

The measurement accuracy of the AC MIN can be increased by using an external precision gain amplifier, a higher resolution ADC, or both. TI provides a range of ADCs to select based on the application requirement. The resolution varies from 12-bit to 18-bit. The ADS8698 18-Bit SAR ADC can measure the analog input with a higher resolution, resulting in improved measurement accuracy. 表 3 provides a range of SAR ADCs to consider.

表 **3. 8-Channel Multiplexed SAR ADC Selection**

ADC NUMBER	DESCRIPTION
ADS8698	18-Bit SAR ADC, 8 Channels, 500 kSPS, and Bipolar Inputs off 5-V Supply
ADS8688	16-Bit SAR ADC, 8 Channels, 500 kSPS, and Bipolar Inputs off 5-V Supply
ADS8678	14-Bit SAR ADC, 8 Channels, 500 kSPS, and Bipolar Inputs off 5-V Supply
ADS8668	12-Bit SAR ADC, 8 Channels, 500 kSPS, and Bipolar Inputs off 5-V Supply

2.3.7.3 Gain Amplifier Selection

A gain amplifier can be used to scale the input in applications where the sensor output is low for improvement of measurement accuracy. Gain amplifiers improve the measurement accuracy and dynamic range. 表 4 provides a range of op amps to consider.

表 **4. Gain Scaling Amplifier Selection**

OP AMP NUMBER	DESCRIPTION
OPA2180	0.1-µV/C Drift, Dual, Low-Noise, Rail-to-Rail, 36-V Zero Drift Op Amp
OPA2188	0.03-µV/°C, 6-µV Vos, Low-Noise, Rail-to-Rail Output, 36-V Zero-Drift Op Amp
OPA4188	0.03-µV/°C, 6-µV Vos, Low-Noise, Rail-to-Rail Output, 36-V Zero-Drift Op Amp
OPA4180	0.1-µV/C Drift, Quad, Low-Noise, Rail-to-Rail, 36-V Zero-Drift Op Amp
OPA4197	36-V, precision, Rail-to-Rail Output, Low Offset Voltage Op Amp
OPA2197	36-V, Precision, Rail-to-Rail Output, Low Offset Voltage Op Amp

2.3.7.4 Dual Output Power Supplies for Gain Amplifier

A dual power supply is required when using gain amplifiers. The dual power supply output can be > ±5.12 V or > ±10.24 V. 表 5 provides a range of power supplies to generate the required dual power supply from a single 5-V or 3.3-V input.

表 **5. Dual Output DC/DC and LDO Selection**

DEVICE	DESCRIPTION
TPS65131	Split-Rail Converter With Dual Positive and Negative Outputs (300 mA typ)
TPS7A39	Dual, 150-mA, Wide V_{IN}, Positive and Negative LDO Voltage Regulator
LM27762	Low-Noise, Positive- and Negative-Output Charge Pump With Integrated LDO

2.3.7.5 Isolated Interface Approaches and Advantages

Two different approaches can provide isolated power and data interface using TI's digital isolator family.

2.3.7.5.1 Isolated Interface With Transformer Driver and Digital Isolator

As shown in 表 6, this approach consists of the following blocks that require multiple products:

- Digital isolator
- Isolation transformer
- Transformer driver
- LDO

The advantage of this approach is that the module can be a design using any of the digital isolators highlighted in 表 6 or with any of the digital isolator families, including devices with reinforced digital isolation or basic digital isolation.

表 6. Digital Isolator Families With External Isolated Power

SERIAL NUMBER	PART NUMBER	DESCRIPTION	INTERFACE TYPE
1	ISO7721	High-Speed, 5000-V_{RMS} Dual-Channel Digital Isolators	UART
2	ISO7740	High-Speed, Low-Power, Robust EMC Quad-Channel Digital Isolator	GPIO
3	ISO7841	High-Immunity, 5.7-kV_{RMS} Reinforced Quad-Channel 3/1 Digital Isolator, 100 Mbps	SPI
4	ISO7840	High-Immunity, 5.7-kV_{RMS} Reinforced Quad-Channel 4/0 Digital Isolator, 100 Mbps	GPIO
5	ISO7821	High-Immunity, 5.7-kV_{RMS} Reinforced Dual-Channel 1/1 Digital Isolator, 100 Mbps	UART
6	ISO7641	6-kV_{PK}, Low-Power Quad Channels, 150-Mbps Digital Isolators	SPI
7	ISO7763	High-Speed, Robust, EMC Six-Channel Digital Isolators	SPI
8	ISO7762	High-Speed, Robust, EMC Six-Channel Digital Isolators	SPI

2.3.7.5.2 Isolated Interface Using ISOW7841

In this approach, all of these components are integrated into one device, simplifying the design, reducing the solution size, and optimizing the cost, as shown in 图 8. In applications where the required interface matches with the ISOW784x family, this approach is recommended.

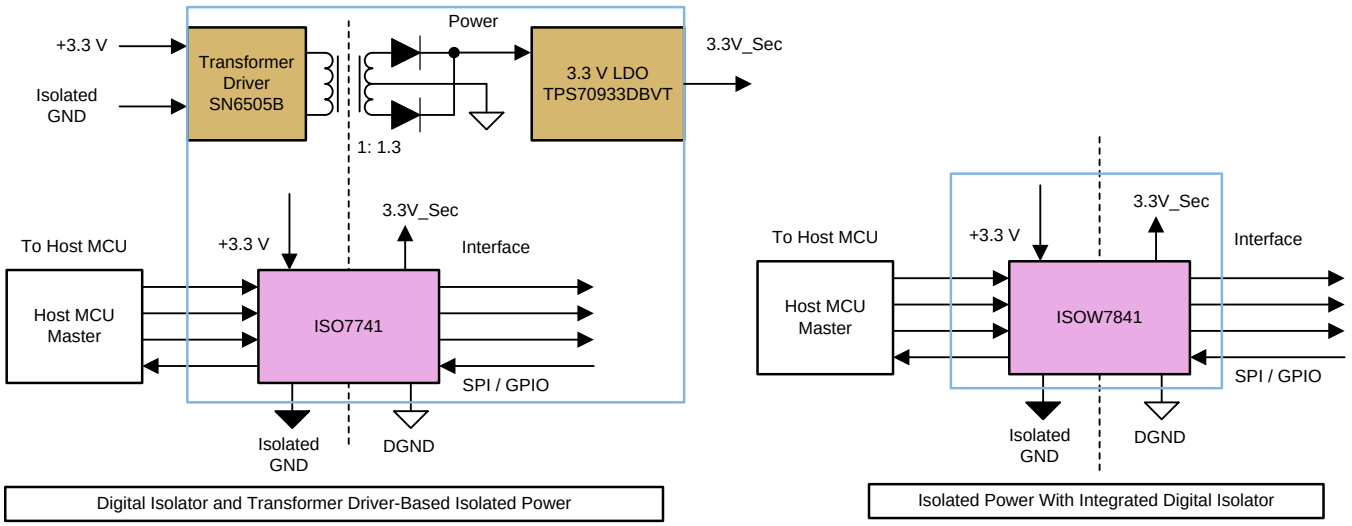

图 8. ISOW7841 Integrated Data and Power

The ISOW7841 with an integrated power converter provides the following advantages:

- Simplifies system design with increased reliability
- Provides current output > 65 mA with 46% efficiency
- Provides current limit and thermal overload protection
- Has a lower temperature rise and overall heat dissipation

2.3.8 Achieving Higher Output Efficiency With Transformer Driver SN6505B

The digital isolator with integrated power provides a peak efficiency of ≈ 48%. In applications requiring greater efficiencies with no space constraint, the SN6501 or SN6505 transformer driver can generate the isolated power. The transformer drivers provide efficiency between 60% to 75% as shown in 表 7.

表 7. Transformer Driver Efficiency at Lower Output Currents

OUTPUT VOLTAGE (V)	LOAD CURRENT (mA)	EFFICIENCY
4.022	8.4	61%
4.022	11.0	64%
4.022	19.0	71%
4.022	30.0	73%

2.3.9 Achieving Higher Efficiency With DC/DC Converters

表 8 provides details on the different DC/DC converters that can generate a split rail output up to 12 V for an AC AIM with high efficiency.

表 8. DC/DC Converters for to Generate Isolated Split Rail Output

DEVICE	DESCRIPTION	APPLICATION NOTE
TPS61040	Boost converter to generate an 18-V output from a single-cell Li-Ion battery (3 to 4.2 V)	TPS61040EVM-001
LM5001	±5-V isolated, low-noise, split rail generator (0.25 A, 2.5 W total)	RD-171
LM5002	Low-noise, split rail, non-isolated power supply	RD-184
LM2733	9- to 14-V_{IN}, isolated ±15-V/100-mA output flyback reference design	PMP10703

2.3.10 Interface With High-Precision ADCs With Serial Interface

The digital isolators ISOW7841 or ISO7741 can interface to ADCs or other TI products with SPI. 表 9 provides some of the options for an ADC interface.

表 9. ADC to Interface With Data Acquisition Front-End With ISOW7841

SERIAL NUMBER	TI ADC PART	ADC DESCRIPTION	INTERFACE TYPE
1	ADS8688 or ADS8688A	16-Bit, 500-kSPS, 8-Channel, Single-Supply, SAR ADCs With Bipolar Input Ranges	SPI-compatible interface with daisy chain
2	ADS8681	16-Bit, 1-MSPS, 5-V SAR ADC With Integrated Analog Front-End and Bipolar Inputs	multiSPI™ interface with daisy chain
3	ADS8588S, ADS8586S, ADS8584S, or ADS8578S	16-Bit, 200-kSPS, 8/6/4 Ch, Simultaneous-Sampling ADCs With Bipolar Inputs on a Single Supply	Serial interface
4	ADS131E08, ADS131E04, or ADS131E08S	Analog Front End for Power Monitoring, Control, and Protection	SPI data interface

表 **9. ADC to Interface With Data Acquisition Front-End With ISOW7841 (continued)**

SERIAL NUMBER	TI ADC PART	ADC DESCRIPTION	INTERFACE TYPE
5	ADS131A04	24-Bit, 128-kSPS, 4-Ch, Simultaneous Sampling, Delta-Sigma ADC	Multiple SPI data interface modes
6	ADS131A02	24-Bit, 128-kSPS, 4-Ch, Simultaneous Sampling, Delta-Sigma ADC	Multiple SPI data interface modes

2.3.10.1 Voltage Supervisor Selection and Options

During an output overload condition, the output of the ISOW7841 reduces proportional to the output current. To ensure the MCU operates within a specified range, consider an external programmable-delay supervisory circuit. The TPS3808 has been provided in this reference design. 表 10 provides a range of other supervisory circuits to consider:

表 10. Voltage Supervisor Selections

SERIAL NUMBER	PART NUMBER	DESCRIPTION
1	TPS3836	Nano-power supervisory circuits
2	TPS3837	Nano-power supervisory circuits
3	TPS3838	Nano-power supervisory circuits
4	TPS3839	Ultra-low-power, supply voltage supervisor
5	TPS3820	Voltage monitor with watchdog timer

2.3.11 ADC Current Consumption

表 11 provides summary of the current consumption for different ADCs. The ISOW7841 can power all the ADCs listed with high efficiency.

表 11. Power Consumption of Different ADCs

POWER (NOMINAL, MAX)	ADS8588S (mA)	ADS8688A (mA)	ADS8698 (mA)	ADS131E08, ADS131E08S (mA)	ADS131A04 (mA)
Analog, AVDD_DYN, internal ref	17.7, 24	13, 16	13, 16	5.8	4.0
DVDD	0.15, 0.3	0.5	0.5	1.0	0.8

2.3.12 Load Switch Selection

The load switch along with the ISOW7841 can protect against overload. The TPS22944 load switch protects systems and loads in high-current conditions. These devices contain a 0.4-Ω current-limited P-channel MOSFET that can operate over an input voltage range of 1.62 V to 5.5 V. Current is prevented from flowing when the MOSFET is off. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals.

For more details, see the TPS22944 product page.

表 12. Load Switch Selection Options

SERIAL NUMBER	PART NUMBER	DESCRIPTION
1	LM34902	300-mA Current Limited Power Switch
2	TPS2010A	0.4-A, 2.7- to 5.5-V Single High-Side MOSFET Switch IC, No Fault Reporting, Active-Low Enable
3	TPS22946	5.5-V, 0.2-A, 400-mΩ Selectable Current Limit Load Switch
4	TPS22960	5.5-V, 0.5-A, 435-mΩ, 2-Channel Load Switch With Quick Output Discharge

2.3.13 ADC Measurement Performance With Higher Clock Frequency and Digital Isolator

In an isolated AC AIM, the ADC and MCU are on opposite sides of the isolation barrier. The SCLK signal experiences a delay, t_{PD_ISO}, as it travels from the MCU to the ADC. The ADC responds to the delayed version of SCLK with an SDO signal that experiences an additional delay of t_{PD_ISO} as it arrives at the MCU. Therefore, the total skew between the SCLK edge and the corresponding ADC data bit at the MCU is ($2 \times t_{PD\_ISO}$). This delay is acceptable as long as the data bit arrives at the MCU before the MCU performs a read operation.

In a standard SPI, a read event occurs on the opposite SCLK edge relative to the SCLK edge corresponding to a write event. For large values of f_{SCLK}, the t_{PD_ISO} requirement becomes challenging to meet. To mitigate this issue, an additional delay of t_{PD_ISO} is introduced in the already delayed version of SCLK by routing SCLK back across the isolation barrier to the MCU along with the SDO signal of the ADC through a multi-channel isolator. This rerouting results in minimal skew between the SDO and SCLK_RET so that the MCU can capture SDO relative to SCLK_RET without error. The following approaches can be used for returning SCLK across the isolation barrier.

2.3.13.1 ADS8681 Using Two Four-Channel Digital Isolators

图 9 provides the interface between the MCU and host interface by using multiple digital isolators.

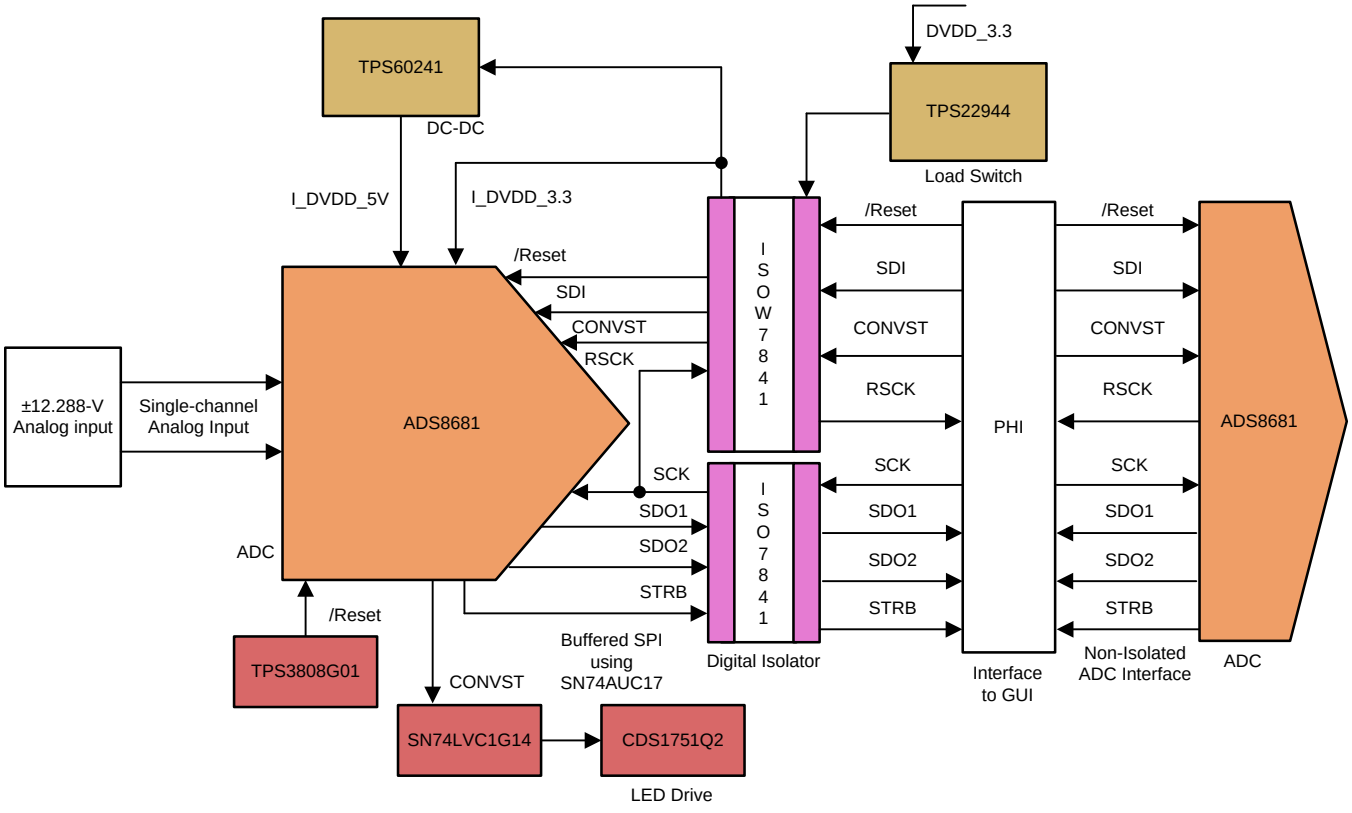

图 9. Block Diagram of ADS8681 Interface With SCK and RSCK Using Multiple Digital Isolators

表 13 provides the system performance with the SCLK returned back across the isolation barrier.

表 13. ADS8681 Performance With Clock Returned to Host From Isolated Side

TEST	INPUT RMS	INPUT RANGE	CH1 (500 KSPS) 60-Hz INPUT	CH1 (500 KSPS) 1-kHz INPUT	CH1 (1000 KSPS) 1-kHz INPUT
ENOB	8.2 V	±12.288 V	14.973	14.951	14.913
SNR	8.2 V	±12.288 V	91.913	91.825	91.630
THD	8.2 V	±12.288 V	–116.866	–110.437	–108.239

2.3.13.2 ADS8920B Using Single Digital Isolator With Integrated Power

图 10 provides the interface between the ADC and host interface by using a single digital isolator with the ADC using default configuration.

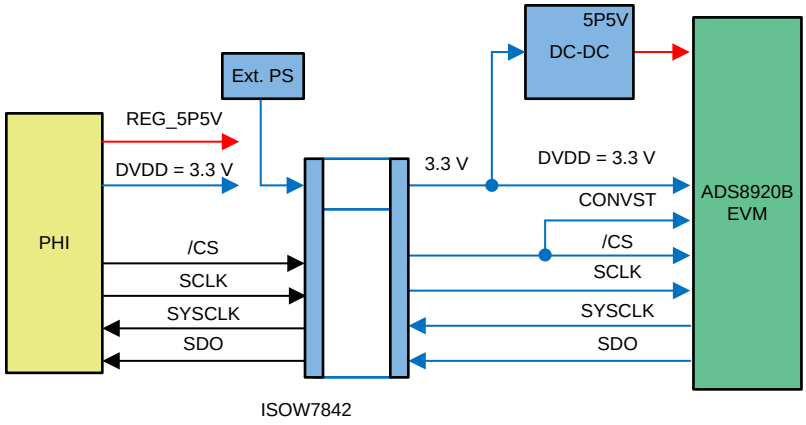

图 10. Block Diagram of ADS8920B Interface Using Single Digital Isolator

表 14 provides the system performance with the SCLK returned back across the isolation barrier.

表 14. ADS8920B Measurement Performance With Clock Fold Back

CONFIGURATION	INPUT FREQ	SNR (dB)	THD (dB)
ADS8920BEVM-PDK	2 kHz	96.10	–125.21
ADS8920BEVM-PDK + ISOW Adapter	2 kHz	96.05	–124.64
ADS8920BEVM-PDK + ISOW Adapter	50 Hz	96.16	–119.31

2.3.14 Temperature Compensation of Measured Analog Input for Improved Measurement Accuracy

The auxiliary ADC channel of the ADS8688 or ADS8668 can be used to measure ambient temperature for real-time compensation of the measured electrical parameters. There are two approaches to measure temperature.

2.3.14.1 Onboard High-Accuracy Analog Temperature Sensor Interface

The first approach is to use an onboard high-accuracy analog temperature sensor interface. 表 15 provides details of different sensors to consider interfacing to the auxiliary channel of ADC.

表 15. High-Accuracy Analog Temperature for Sensor for AC AIM

SENSOR	DESCRIPTION
LMT70	±0.1°C precision analog temperature sensor
LM35	±0.5°C temperature sensor with analog output with 30-V capability

2.3.14.2 Using Remote Temperature Sensor

The second approach is to use a remote temperature sensor, including resistance temperature detectors (RTDs). 表 16 lists some of the common types of RTDs used:

表 16. Common RTD Sensors for AC AIM

SENSOR	DESCRIPTION
100 Ω PT	Platinum
120 Ω NI	Nickel
10 Ω CU	Copper

The auxiliary ADC input can be configured to measure the analog temperature sensor output. For more details, see the Isolated, High-Accuracy Analog Input Module Reference Design Using 16-Bit ADC and Digital Isolator.

2.3.15 Improving Analog Input Measurement Accuracy Using 18-Bit ADC

The measurement accuracy of the AC AIM can be increased by using an external precision gain amplifier, a higher resolution ADC, or both. Precision gain amplifiers like the OPA4180, OPA4188, or INA188 can provide the required gain. The ADS8698 18-Bit SAR ADC can measure the analog input with higher resolution, resulting in improved measurement accuracy.

2.3.16 Design of Wide Input AC or DC Digital, Contact, or Binary Input Module

The TIDA-00847 reference design showcases a DC or DC BIM using a 10-bit SAR ADC internal to the MCU MSP430G2332. Most grid applications allow measurements of 16 digital or binary inputs with a DC voltage up to 300 V. The ADS8668 connected in a daisy-chain configuration with a 12-bit resolution can be used to implement a 16-channel group isolated DC BIM using only four TI products with improved accuracy performance over a wide input range.

2.3.17 DC Transducer Input Module With Unidirectional or Bidirectional Signal Input

This reference design can be designed as a DC AIM to measure unipolar or bipolar inputs ranging from 0 to 20 mA, 4 to 20 mA, 0 to 10 V, ±20 mA, and ±10 V. Similar reference designs include the TIDA-00550, TIDA-00764, TIDA-00164, TIDA-00119, and TIDA-00310. This reference design with an integrated digital isolator and power converter simplifies the module design.

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

This section describes the setup for performance testing of the AC AIM.

3.1.1 AC AIM

The following subsections provide information on the different interface connectors for connecting power supply, host interface, and AC analog inputs.

3.1.1.1 16-Channel ADS8688A and ISOW7763-Based AC AIM

表 17 lists the different connectors used for applying the inputs and power supply for performance evaluation of the AC AIM.

表 17. 16-Channel ADS8688A-Based AIM Connections

CONNECTOR	FUNCTION	COMMENTS
J11.1, J11.8	DC power supply	Do not exceed 3.6-V inputs for proper performance
Analog Input 0 of ADC1 and ADC2	J2, J13	
Analog Input 1 of ADC1 and ADC2	J1, J14	
Analog Input 2 of ADC1 and ADC2	J5, J15	
Analog Input 3 of ADC1 and ADC2	J6, J16	
Analog Input 4 of ADC1 and ADC2	J8, J17	
Analog Input 5 of ADC1 and ADC2	J9, J18	
Analog Input 6 of ADC1 and ADC2	J4, J10	
Analog Input 7 of ADC1 and ADC2	J3, J12	
J11	PHI	For connecting the AC AIM to GUI

3.1.1.2 PHI Board Connections

To evaluate the ADC performance quickly, use the PHI board for evaluation. The PHI board is connected to the design board through a breakout board. The breakout board allows the PHI board to interface the signals from the reference design using wires. If users has their own signal processing board based on the TMS320C6748, AM3359, AM4372, or AM5278, the interface signals from the reference design can be directly connected to the processing board. 表 18 details the interface between the breakout board and the interface connector of the reference design for daisy chain configuration

表 18. PHI Board Connections for Daisy Chain

CONNECTOR J11	BREAK OUT BOARD CONNECTIONS	FUNCTION
1		DVDD
2	J4_8	/CS
3	J4_10	SCLK
4	J4_7	SDO (SDI from interface board)
5	J4_17	SDI1 (SDO1 from interface board)
6		
7	Not used	SCLK_RET
8	J5-22	GND

Contact TI for more details on the breakout board and the PHI connector.

表 19 details the interface between the breakout board and the interface connector of the reference design for a dual SDO output configuration.

表 19. PHI Board Connections for Dual SDO

CONNECTOR J11	BREAK OUT BOARD CONNECTIONS	FUNCTION
1		DVDD
2	J4_9	/CS
3	J4_10	SCLK
4	J4_7	SDO (SDI from interface board)
5	J4_17	SDI1 (SDO1 from interface board)
6	J4_18	SDI2 (SDO1 from interface board)
7	Not used	SCLK_RET
8	J5-22	GND

3.2 Testing and Results

3.2.1 Test Setup

图 11 provides information on the setup used for functional and performance testing of the AC AIM.

The test setup for the AC AIM consists of:

- DC power supply (3.3 V)
- TIDA-01576 reference design board
- Function generator to simulate the AC analog inputs, ±10.24 max input
- PHI breakout board
- PHI card and GUI for HMI and data capture

注: While testing, ensure the analog inputs do not exceed the ADC input range of ±10.24 V for proper operation. For the purpose of performance testing, PHI is used as the host.

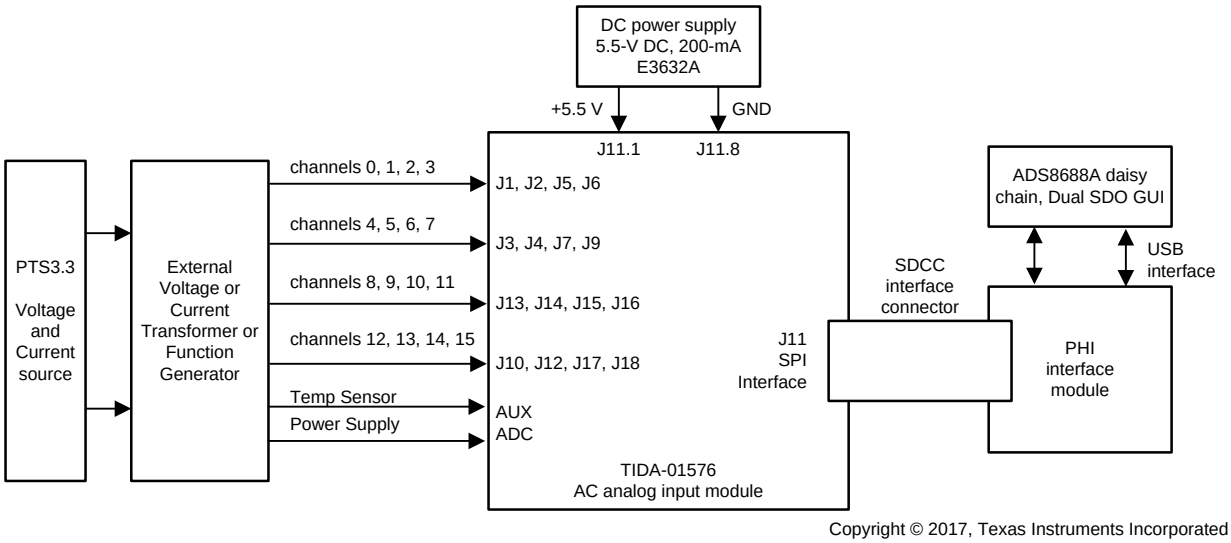

图 11. Test Setup for Performance Testing of AC AIM

The reference design board is designed to evaluate with any of the customer boards. The PHI board used to evaluate performance is not part of the reference design. Contact TI for details on the availability of PHI boards.

3.2.2 Test Results

Note the following test conditions for performance measurement of the AC AIM:

- The tests are done using a function generator or programmable AC voltage and current source.
- GUI is to evaluate performance.

3.2.2.1 Functional Testing

表 20 details the different functional tests that are done.

表 20. AC AIM Functional Test Observations

PARAMETER	SPECIFICATION	MEASUREMENT
Isolated supply ISOW7841 output	3.3 V	3.36 V
Output ripple on isolated supply for ISOW7841	100 mV	≈ 100 mV
Transformer driver-based isolated supply	3.3 V	3.32 V
3.3-V to 5-V DC/DC converter	5.35 V	5.33 V
5-V LDO output	5.15 V	5.15 V
Temperature sensor output	979.313 mV	979.72 mV
ISOW7841-based digital isolator functionality	Communication functionality	OK
6-channel digital isolator functionality	Communication functionality	OK
Measurement of ADC analog inputs with different ADC input ranges	Measurement of inputs RMS and display	OK
Frequency measurement	50 or 60 Hz	OK
Alarm function	Based on set high and low thresholds	OK
Alarm output LED	Alarm indication and reset	OK
Diagnostics	Output of auxiliary channel	OK
HOST	PHI	OK

3.2.2.2 ADC Performance

This section details the different tests performed on this reference design and the performance results. A custom GUI is used to analyze performance. Contact TI fir availability of GUI for performance analysis.

3.2.2.2.1 ADS8688A Time Domain Measurement Performance for Dual SDO With Isolated Interface

图 12 (snapshot of the GUI) shows the performance analysis of the time domain done on the reference design. The time domain analysis includes a display of the waveform and RMS values.

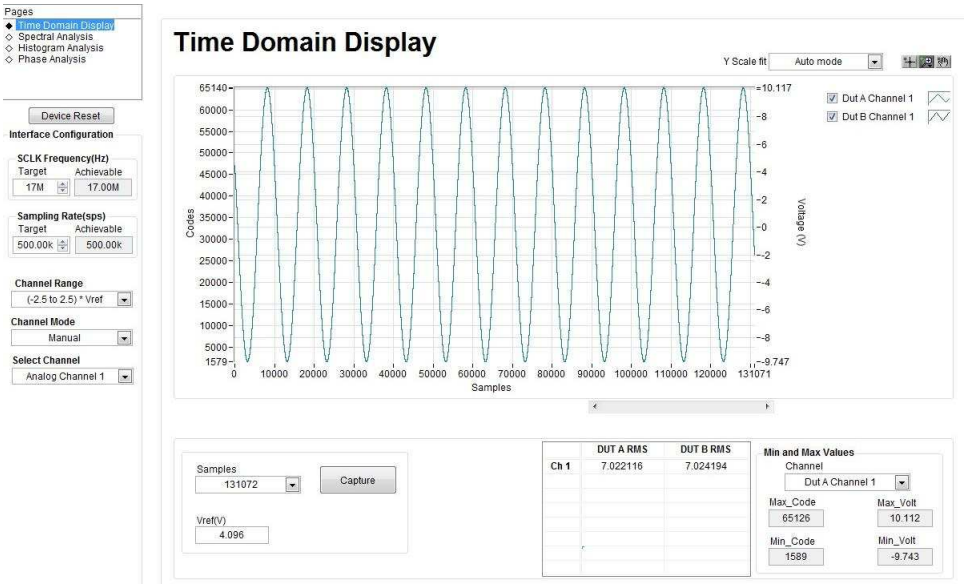

图 12. Time Domain Analysis of ADS8688A ADC Using GUI and PHI Card

3.2.2.2.2 ADS8688A Time Domain Measurement Performance for Dual SDO With Isolated Interface

图 13 shows the spectral analysis tests done on the design board. The spectral analysis is captured for DUT A and DUT B.

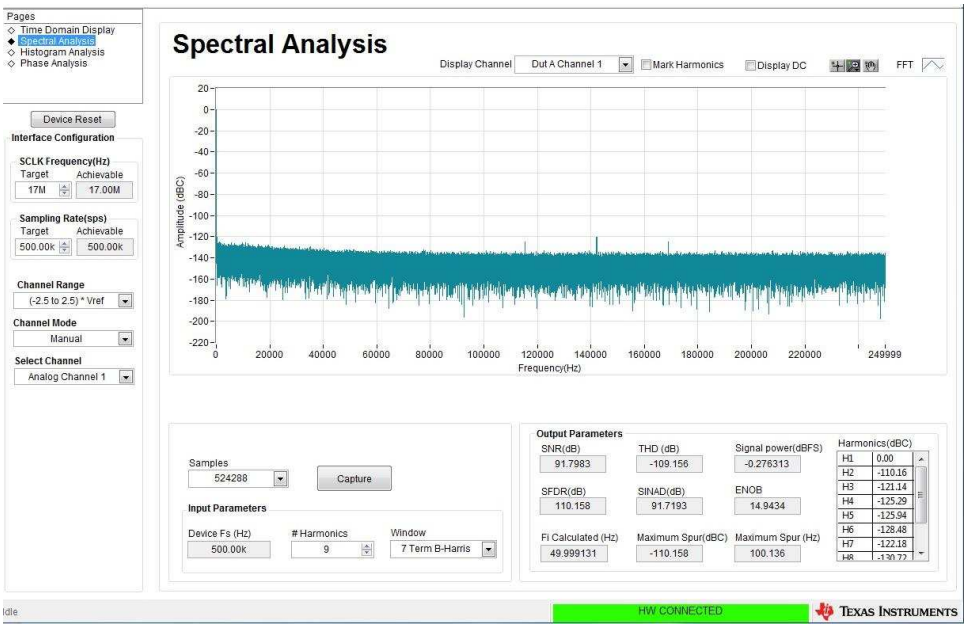

图 13. Spectral Analysis of ADS8688A ADC Using GUI and PHI Card

3.2.2.2.3 ADS8688A Measurement Performance for Dual SDO With Isolated Interface

This section provides details of different tests performed on this reference design and the performance results. 表 21 provides performance test results for the ADS8688A ADC. A custom GUI is used to analyze performance. Contact TI for availability of GUI for performance analysis with different input ranges.

表 21. ADS8688-Based Isolated Dual SDO Output AC AIM Performance Test Board 1

TESTS	INPUT (V)	INPUT RANGE (V)	ADC1 CH1	ADC2 CH1	ADC 1 CH7	ADC2 CH7
ENOB	7	±10.24	14.9896	15.005	15.009	14.9923
	3.45	±5.12	14.79	14.78	14.79	14.779
SNR	7	±10.24	92.858	92.118	92.078	92.074
	3.45	±5.12	90.95	90.865	90.91	90.866
THD	7	±10.24	–108.95	–114.742	–111.125	–110.579
	3.45	±5.12	–107.75	–108.05	–109.5	–106.1

These tests are repeated with the second board. 表 22 shows the results.

表 22. ADS8688-Based Isolated Dual SDO Output AC AIM Performance Test Board 2

TESTS	INPUT (V)	INPUT RANGE (V)	ADC1 CH1	ADC2 CH1
ENOB	7	±10.24	14.975	14.9913
	3.45	±5.12	14.775	14.775
SNR	7	±10.24	91.98	92.038
	3.45	±5.12	90.808	90.805
THD	7	±10.24	–109.35	–113.565
	3.45	±5.12	–107.2	–107.341

The AIM meets the ADC performance requirements in isolated interface configuration.

3.2.2.2.4 Measurement With DUTB Configured as External Reference

The tests in 节 3.2.2.2.3 are repeated with a change in the reference configuration. DUT A is configured for internal reference and DUT B is configured for external reference. The reference output of DUT A is connected to DUT B.

表 23. ADS8688-Based Isolated Dual SDO Output With Reference Configuration Changed

TESTS	INPUT (V)	INPUT RANGE (V)	ADC1 CH1	ADC2 CH1
ENOB	7	±10.24	14.9746	14.943
	3.45	±5.12	14.779	14.804
SNR	7	±10.24	91.96	91.7983
	3.45	±5.12	90.7826	90.928
THD	7	±10.24	–111.097	–109.56
	3.45	±5.12	–109.978	–110.888

The AIM meets the ADC performance requirements with DUT A configured for internal reference and DUT B configured for external reference.

3.2.2.2.5 Measurement With Non-Isolated Interface and Daisy

The tests in 节 3.2.2.2.3 are repeated with the board configured in daisy chain mode and using a non-isolated interface. 表 24 shows the results.

表 **24. ADS8688-Based AC AIM Performance With Daisy Chain**

TESTS	INPUT (V)	INPUT RANGE (V)	ADC1 CH1	ADC2 CH1
ENOB	7	±10.24	14.81	14.75
	3.45	±5.12	14.3	14.31
SNR	7	±10.24	91.011	90.963
	3.45	±5.12	89.01	89.1
THD	7	±10.24	–101.646	100.51
	3.45	±5.12	–96.3	–96.25

3.2.2.2.6 Measurement With ADC Interfaced to ISOW7841

表 25 provides performance test results for the ADS8688 with different input ranges interfaced using the ISO7841 digital isolator with integrated power.

表 **25. ADS8688A-Based, Isolated AC AIM Performance With ISOW7841**

TESTS	INPUT	INPUT RANGE (V)	CHANNEL 1	CHANNEL 7
ENOB	7	±10.24	14.9	14.9
	3.5	±5.12	14.77	14.77
	1.75	±2.56	14.51	14.51
	0.875	±1.28	13.64	13.63
	0.4375	±0.64	12.69	12.7
SNR	7	±10.24	91.47	91.51
	3.5	±5.12	90.66	90.7
	1.75	±2.56	89.11	89.12
	0.875	±1.28	83.87	83.83
	0.4375	±0.64	78.14	78.23
THD	7	±10.24	–111.02	–112.64
	3.5	±5.12	–111.06	–112.9
	1.75	±2.56	–111.26	–112.9
	0.875	±1.28	–106.44	–106.29
	0.4375	±0.64	–99.82	–101.74

3.2.2.2.7 Voltage Measurement

With the GUI, calculate RMS voltage by using the acquired samples. 表 26 shows the results.

表 **26. RMS Values for Analog Input**

INPUT (V)	ADC1 CH7	ADC2 CH7
7.0215	7.02211	7.024194
5.0149	5.017767	5.019232
2.5063	2.5134	2.5142

The RMS measurement can be improved by measuring the DC offset and compensating the DC offset from the measured samples before computing the RMS values.

3.2.2.2.8 ADC Measurement Accuracy

A performance test of the ADC inputs or measurement accuracy is performed by applying a known input voltage and capturing the AC voltage measured by the ADC on the GUI. 表 27 details the measurement errors observed with different inputs values.

表 27. ADC Measurement Accuracy for 50-Hz Voltage Input

±10.24-V RANGE	DUT A CH1		DUT B CH1	
ACTUAL INPUT (mV)	MEASURED INPUT (mV)	% ERROR	MEASURED INPUT (mV)	% ERROR
0.05015	0.0501	–0.1	0.0501	–0.1
0.10028	0.1002	–0.08	0.1003	0.02
0.2506	0.2507	0.04	0.2507	0.04
0.5015	0.5013	–0.04	0.5014	–0.02
1.003	1.0021	–0.09	1.0024	–0.06
2.007	2.006	–0.05	2.0066	–0.02
3.008	3.0079	–0.003	3.0088	0.027
5.017	5.0144	–0.052	5.0158	–0.024
7.027	7.0197	–0.104	7.0218	–0.074

The measurement error is within ±0.2% of the measured values over the entire input range. The GUI allows the user to calculate the DC offset and compensate for the DC offset during the ADC sampling and RMS calculation.

3.2.2.3 ADS8688A Synchronization Testing and Results

This section details the synchronization test procedure and results.

3.2.2.3.1 Synchronization Procedure

The synchronization procedure to correct the phase shift during multiplexed sampling is described in this section.

This section uses the following terms:

FREF— Reference frequency

FS— ADC sampling rate

TS— Sample time (1 per FS)

N— Number of samples per cycle

ΦC1— DFT on Cycle 1 data on reference channel and calculated phase angle of cycle 1

ΦC2— DFT on Cycle 2 data on reference channel and calculated phase angle of cycle 2

df— Difference in frequency between two cycles

The phase compensation algorithm consists of four steps:

1. Calculate the theoretical phase difference (ΔΦmux) introduced by the ADC as a result of multiplexing channels
2. Estimate the frequency of the power system signal using the DFT method (frequency tracking).
3. Calculate the phase angle of all the signals in the system based on the estimated frequency.
4. Compensate the phase difference for all the channels using the theoretical value calculated in Step 1.

From the captured ADC data and FS, FREF is computed using FFT analysis. If the override signal Freq is enabled from the GUI, computing FREF is skipped and the user entered value is used for further computation. N is computed using (FS / FREF). Then the phase is computed for the first two cycles of data. For computing the phase, a one-sided spectrum is computed from first cycle of data. This computed one-sided spectrum is converted into its polar form. The index of the maximum value of r gives the index of the fundamental frequency. Using fundamental frequency index and theta value, ΦC1 is computed. Similarly, ΦC2 is computed for the second cycle of data.

Frequency difference df is computed using the formula: df = (ΦC1 – ΦC2) / 2π / dtREF, where dtREF = (1 / FREF).

This computation is repeated for all channels.

Again find the phase of the reference channel (ΦREF) and other channels (ΦI) with N samples, where N is FS / FCH. DUT A Channel 0 is taken as the reference channel.

Phase difference dΦCH = ΦREF – ΦI

Now find compensation per channel using the following formula (ΦCOMP) = ((TS / Number of channels) / (TCH)) × 360 and find the phase difference with compensation dΦCHCOMP = ΦREF – ΦI – (ΦCOMP × i)

3.2.2.3.2 Synchronization of 16 Analog Input Channels

Two ADCs can be connected together to provide 16 analog input channels by following two methods:

- Two ADCs are daisy chained with only one SDO output, providing a data of 500 kSPS totally for 16 channels.
- SCLK, SDO, and /CS connected together and two SDOs are connected separately providing 500 kSPS of data for each ADC, increasing throughput.

  To compensate for the phase shift introduced by multiplexed ADC, see the Phase Compensated 8-Ch Multiplexed Data Acquisition System for Power Automation Reference Design for more details.

One degree is equal to 60 minutes. At a power factor of 0.5 Lag (inductive, 60 degrees), a 0.5-minute error contributes to 0.03% or less measurement error, which falls within the measurement uncertainty. During measurement, there is a phase shift between channels of the same ADC. To compensate for the phase shift introduced by multiplexed ADC sampling, see the Phase Compensated 8-Ch Multiplexed Data Acquisition System for Power Automation Reference Design.

3.2.2.3.3 GUI for Synchronization

A GUI has been developed for performance analysis including timer domain analysis, spectral analysis, histogram and phase analysis. 图 14 shows the phase analysis. The analysis is shown for all the analog inputs.

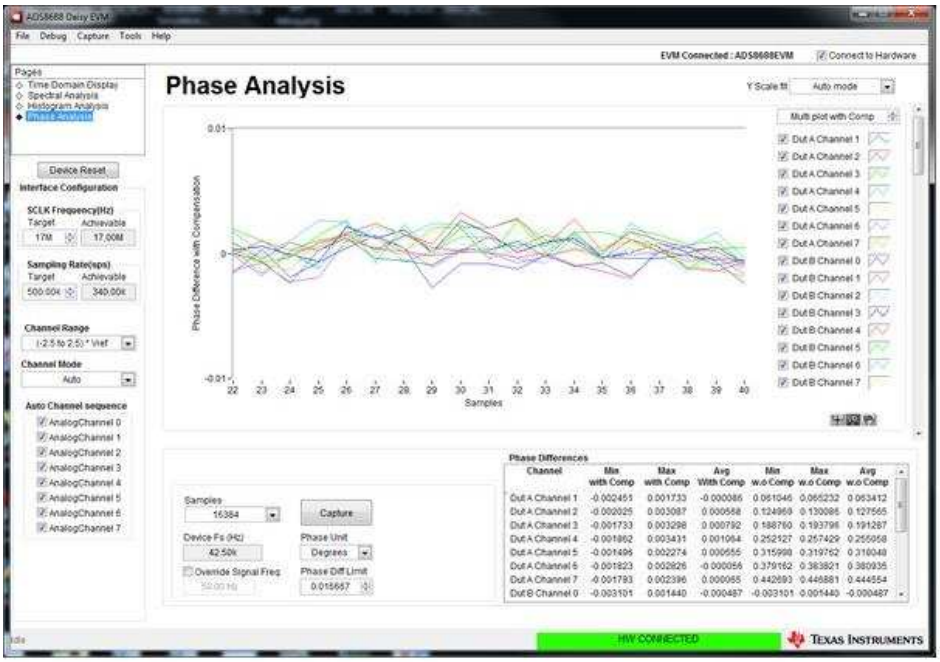

图 14. Dual ADC Synchronization Result

The phase analysis displays results with and without compensation. DUT A channel 0 is taken as the reference for phase compensation.

3.2.2.3.4 Synchronization Test Results for ADCs Connected in Daisy Chain

This section provides synchronization test results for the ADCs configured as a daisy chain. 表 28 provides the phase error with respect to DUT A channel 0.

表 **28. Synchronization Test Results of Daisy-Chained ADC**

CHANNEL	MIN WITH COMP (MINUTES)	MAX WITH COMP (MINUTES)	AVG WITH COMP (MINUTES)	MIN WITHOUT COMP (MINUTES)	MAX WITHOUT COMP (MINUTES)	AVG WITHOUT COMP (MINUTES)
DUT A Channel 1	–0.1470	0.10398	–0.00516	3.66276	3.91392	3.80472
DUT A Channel 2	–0.1215	0.18522	0.03408	7.49814	7.80516	7.6539
DUT A Channel 3	–0.1039	0.19788	0.04752	11.3256	11.62776	11.47722
DUT A Channel 4	–0.1080	0.20586	0.06384	15.12762	15.44574	15.30348
DUT A Channel 5	–0.0894	0.13644	0.0333	18.95988	19.18572	19.08288
DUT A Channel 6	–0.1093	0.16956	–0.00336	22.74972	23.02926	22.8561
DUT A Channel 7	–0.1074	0.14376	0.0039	26.56158	26.81286	26.67324
DUT B Channel 0	–0.1860	0.0864	–0.02922	–0.18606	0.0864	–0.02922
DUT B Channel 1	–0.14052	0.10032	–0.03696	3.66936	3.91026	3.77298
DUT B Channel 2	–0.15792	0.13296	0.0204	7.46178	7.75272	7.64022
DUT B Channel 3	–0.08106	0.15882	0.04302	11.34846	11.58834	11.47272
DUT B Channel 4	–0.09918	0.24066	0.06348	19.00452	15.48048	15.30312
DUT B Channel 5	–0.04488	0.23094	0.07764	19.00452	19.28076	19.12716
DUT B Channel 6	–0.1239	0.13332	0.00534	22.73508	22.9932	22.8648
DUT B Channel 7	–0.1305	0.13302	0.00888	26.5383	26.80296	26.67828

Some of the observations from the test results are:

- These is no error between DUT A channel 0 and DUT B channel 0. Similar observations are made for all the channels.
- The phase error increases with the increase in channel number for DUT A (ADC1) and DUT B (ADC2).
- The phase error between the input channels depends on the sampling rate.

When implementing this reference design hardware, series resistors, protection diodes, and filter capacitors are provided for protection and input noise filtering. Based on the phases shift requirements, these components values can change or need to be de-populated. The phase error between the ADCs can be further reduced by using a common external reference.

The phase error testing is done with the ADC samples taken at the maximum sampling rate of the device with the ADC1 and ADC2 SDO outputs interfaced to the host separately. ADCs can also be configured in daisy chain mode to expand the input channels using only one interface. The phase error depends on the ADC sampling rate.

3.2.2.3.5 Synchronization Test Results for ADCs With Dual SDO Output

This section provides synchronization test results for the ADCs configured for the dual SDO output. 表 29 provides the phase error with respect to DUT A channel 0.

表 29. Test Results for ADCs Configured for Dual SDO Output

CHANNEL	AVG WITH COMP (MINUTES)	AVG WITHOUT COMP (MINUTES)
DUT A Channel 1	–0.00588	2.15406
DUT A Channel 2	0.0252	4.34514
DUT A Channel 3	0.03216	6.51204
DUT A Channel 4	0.01722	8.65704
DUT A Channel 5	0.02178	10.8216
DUT A Channel 6	–0.00762	12.9522
DUT A Channel 7	–0.01404	15.10572
DUT B Channel 0	–0.00098	–0.48984
DUT B Channel 1	–0.00588	1.67604
DUT B Channel 2	0.0252	3.81126
DUT B Channel 3	0.03216	5.9661
DUT B Channel 4	0.01722	8.12268
DUT B Channel 5	0.02178	10.28622
DUT B Channel 6	–0.00762	12.46476
DUT B Channel 7	–0.01404	14.6331

注: The compensated value includes compensation for the gain difference between DUT A and DUT B is caused due to a change in reference and the PGA gain.

Some of the observations from the test results are:

- These is no error between DUT A channel 0 and DUT B channel 0. Similar observations are made for all the channels.
- The phase error increases with the increase in channel number for DUT A (ADC1) and DUT B (ADC2).
- The phase error between the input channels depends on the sampling rate and reduces in the dual SDO configuration due to the increased data output rate.

3.2.2.4 ISOW7841 Isolated Power Supply Testing

3.2.2.4.1 ISOW7841 Load Regulation Testing

Load regulation is tested by varying the output load from 20 to 100 mA and applying an input of 3.3 V at the input of the power connector. 表 30 provides the test results for load regulation.

表 30. ISOW7841 Load Regulation Test(1)

INPUT VOLTAGE (V)	INPUT I (SUBTRACTING NO LOAD I) (A)	POWER	OUTPUT VOLTAGE (V)	OUTPUT CURRENT (A)	POWER (W)	EFFICIENCY	OBSERVATIONS	LOAD (R)
3.3	0.057	0.188	3.340	0.022	0.073	39.064%		150
3.3	0.081	0.267	3.340	0.033	0.112	41.734%		100
3.3	0.101	0.333	3.364	0.044	0.148	44.409%		75
3.3	0.124	0.409	3.364	0.055	0.185	45.215%		150|100
3.3	0.144	0.475	3.364	0.067	0.225	47.289%		150|75
3.3	0.168	0.554	3.364	0.078	0.262	47.268%		100|75
3.3	0.184	0.607	3.364	0.085	0.285	46.876%		39
3.3	0.262	0.865	3.380	0.122	0.413	47.772%		27
3.3	0.254	0.838	3.043				Overcurrent clamp	22

(1) No load input current: 0.026 A

Observation: Load regulation observed is < ±1%.

3.2.2.4.2 ISOW7841 Line Regulation (Input versus Output Voltage Variation) Testing

Line regulation is tested by varying voltage from 3.6 to 2.3 V with an approximate 80-mA load at the output of the power connector. 表 31 provides the test results for line regulation.

表 31. Line Regulation (Input versus Output Voltage Variation) and UVLO

VOLTAGE (V)		CURRENT (A)		EFFICIENCY	LOAD in RR	SUPPLY I (A)	OBSERVATIONS
INPUT	OUTPUT	OUTPUT I	INPUT I				
3.6	3.363	0.086	0.174	49.55%	39	0.200	
3.3	3.360	0.086	0.184	46.82%	39	0.210	
3.0	3.373	0.086	0.201	43.02%	39	0.227	
2.7	3.380	0.086	0.229	37.84%	39	0.255	
2.6	3.330	0.085	0.231	36.96%	39	0.257	UVLO recover
2.5	3.200	0.082	0.222	36.96%	39	0.248	
2.4	3.000	0.076	0.214	35.94%	39	0.240	
2.3	0					0	UVLO

Observation: Line regulation observed is < ±3 mV/V.

3.2.2.4.3 ISOW7841 Ripple Measurement

图 15 shows a DC output ripple in mV on isolated supply (pkpk) with a 20-MHz bandwidth, C_{LOAD} = 20 µF, and I_{ISO} = 80 mA. The measurements are done near to the load, away from the ISOW7841 power output pins.

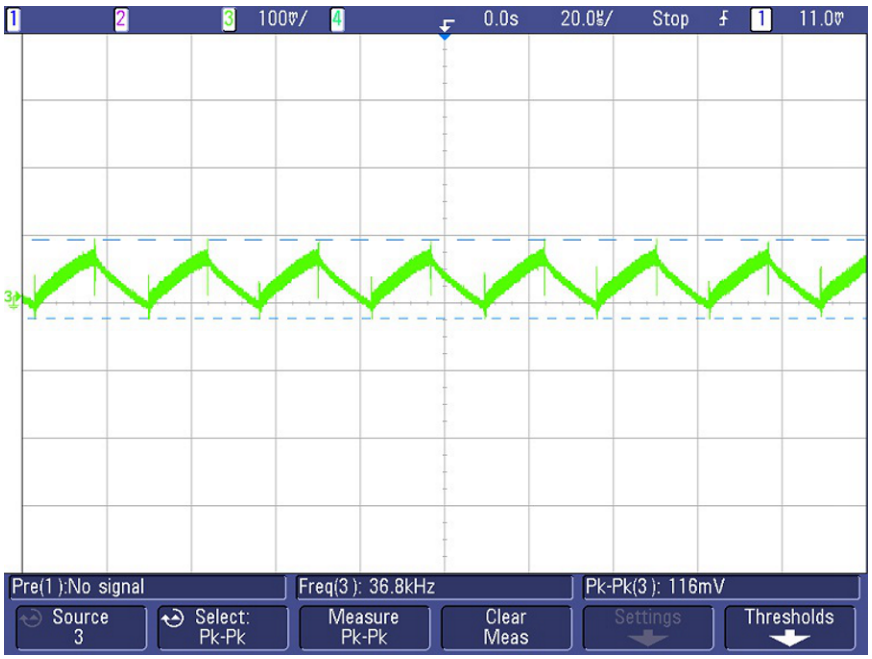

图 **15. ISOW7841 DC Output Ripple**

3.2.2.4.4 ISOW7841 Input Switching Current

图 16 shows the input switching current measured for a DC input current of 160 mA. The input voltage applied is 3.3-V DC.

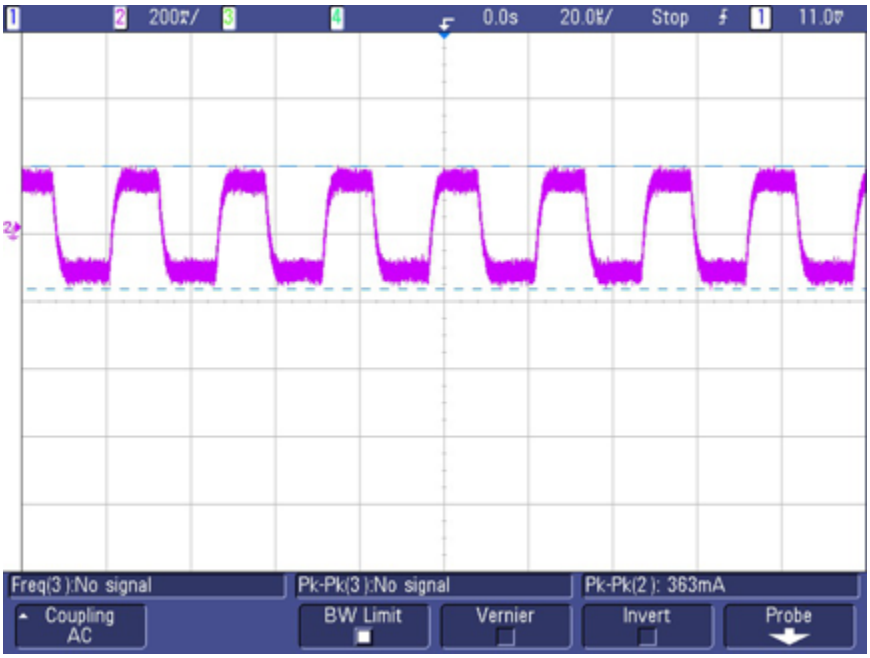

图 **16. ISOW7841 Input Switching Current for 75-mA Output Loading**

3.2.2.4.5 ISOW7841 Device Hotspot Monitoring

The output of the ISOW7841 is loaded for 80 mA, and the hotspot is monitored after 30 minutes. 图 17 shows the hotspot measurements on the ISOW784x evaluation module.

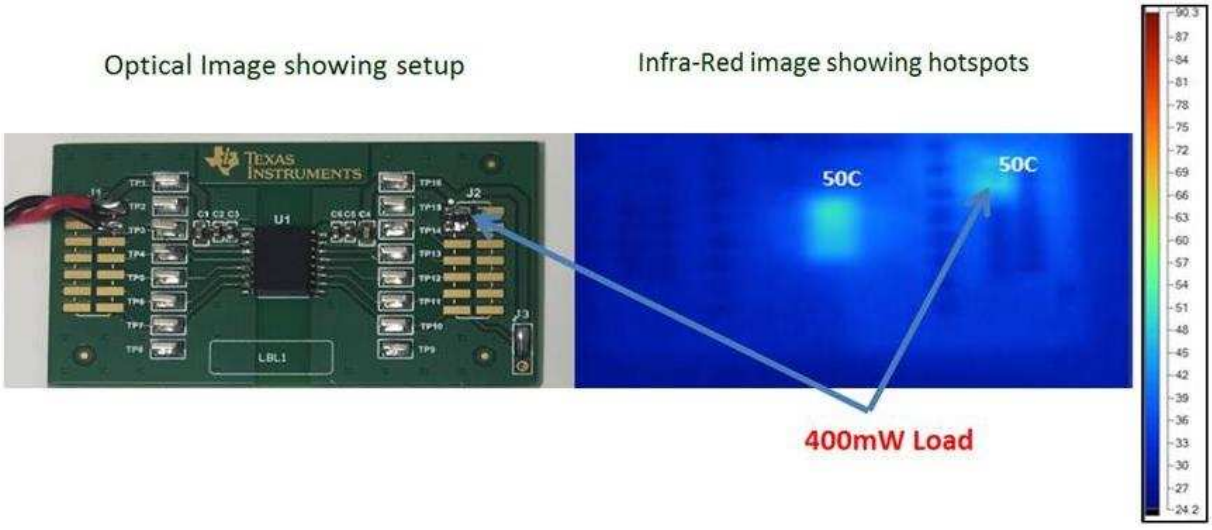

图 **17. ISOW7841 Hotspot Capture With 80-mA Load**

3.2.2.5 Test Results Summary for AC AIM

表 32 summarizes the tests and observations for the AC AIM.

表 **32. Test Results Summary**

TEST	OBSERVATION
ADC functionality	OK
ADC performance with digital isolator	OK
ADC performance with digital isolator with integrated power	OK
ADC performance in daisy chain configuration	OK
ADC performance with different input ranges	OK
ISOW7841 power output	OK
Digital isolator interface	OK
Transformer driver output	OK
DC/DC and LDO output	OK
Analog inputs phase compensation	OK
Diagnostics LEDs	OK
ADC aux channel testing	OK
Host interface with reinforced digital isolation	OK

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01576.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-0576.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01576.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01576.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01576.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01576.

5 Related Documentation

1. Texas Instruments, *16-Bit 1-MSPS Data Acquisition System With Isolated Inputs for High-Voltage Common-Mode Rejection Design Guide*
2. Texas Instruments, *20-Bit, 1-MSPS Isolator Optimized Data Acquisition Reference Design Maximizing SNR and Sample Rate Design Guide*
3. Texas Instruments, *Size and Cost-Optimized Binary Input Module Reference Design Using Digital Isolator With Integrated Power Design Guide*
4. Texas Instruments, *Low-Emission Designs With ISOW7841 Integrated Signal and Power Isolator Design Guide*
5. Texas Instruments, *Eight-Channel, Isolated, High-Voltage Analog Input Module With ISOW7841 Reference Design Guide*
6. Texas Instruments, *Isolated, High-Accuracy AIM Ref Design Using 16-Bit ADC and Digital Isolator Design Guide*

5.1 商标

6 Terminology

AC — Alternating current

AIM— Analog input module

DC — Direct current

PHI— Precision host interface

RMS — Root mean square

RTD— Resistance temperature detectors

7 About the Authors

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