STM32U5 Nucleo-144 board (MB1549)

Introduction

The STM32U5 Nucleo-144 board based on the MB1549 reference board (NUCLEO-U575ZI-Q) provides an affordable and flexible way for users to try out new concepts and build prototypes by choosing from the various combinations of performance and power consumption features, provided by the STM32U5 microcontroller.

The ST Zio connector, which extends the ARDUINO® Uno V3 connectivity, and the ST morpho headers provide easy expansion of the functionality of the STM32 Nucleo open development platform with a wide choice of specialized shields.

The STM32U5 Nucleo-144 board does not require any separate probe as it integrates the STLINK-V3E debugger/programmer.

The STM32U5 Nucleo-144 board comes with the STM32 comprehensive free software libraries and examples available with the STM32CubeU5 MCU Package.

Figure 1. STM32U5 Nucleo-144 board

Picture is not contractual.

1 Features

- STM32U5 Series microcontroller (Arm® Cortex®-M33 at 160 MHz) in an LQFP144 package
- Internal SMPS to generate V_{core} logic supply, identified by '-Q' suffixed boards(1)
- USB Type-C® sink device FS
- 3 user LEDs
- RESET and USER push-buttons
- 32.768 kHz crystal oscillator
- Board connectors:
  - USB Type-C® connector
  - ST Zio connector including ARDUINO® Uno V3
  - ST morpho extension pin headers for full access to all STM32 I/Os
- Flexible power-supply options: ST-LINK USB V_{BUS}, USB connector, or external sources
- On-board STLINK-V3E debugger/programmer with USB re-enumeration capability: mass storage, Virtual COM port, and debug port
- Comprehensive free software libraries and examples available with the STM32CubeU5 MCU Package
- Support of a wide choice of Integrated Development Environments (IDEs) including IAR Embedded Workbench®, MDK-ARM, and STM32CubeIDE

1. *SMPS significantly reduces power consumption in Run mode, by generating a V_{core} logic supply from an internal DC/DC converter.*

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Ordering information

To order the NUCLEO-U575ZI-Q Nucleo-144 board, refer to Table 1. Additional information is available from the datasheet and reference manual of the target STM32.

Table 1. Ordering information

Order code	Board reference	Target STM32
NUCLEO-U575ZI-Q	MB1549	STM32U575ZIT6Q

2.1 Products and codification

The meaning of the codification is explained in Table 1.

Table 2. Codification explanation

NUCLEO-XXYYZE-Q	Description	Example: NUCLEO-U575ZI-Q
XX	MCU series in STM32 Arm Cortex MCUs	STM32U5 Series
YY	MCU product line in the series	STM32U575/585
Z	STM32 package pin count	144 pins
E	STM32 flash memory size: • I for 2 Mbytes • J for 4 Mbytes	2 Mbytes
-Q	STM32 has an internal SMPS function	SMPS

The order code is mentioned on a sticker placed on the top or bottom side of the board.

3 Development environment

3.1 System requirements

- Multi-OS support: Windows® 10, Linux® 64-bit, or macOS®
- USB Type-A or USB Type-C® to Micro-B cable

Note: *macOS® is a trademark of Apple Inc., registered in the U.S. and other countries and regions.*
Linux® is a registered trademark of Linus Torvalds.
All other trademarks are the property of their respective owners.

3.2 Development toolchains

- IAR Systems® - IAR Embedded Workbench®(1)
- Keil® - MDK-ARM(1)
- STMicroelectronics - STM32CubeIDE

1. *On Windows® only.*

3.3 Demonstration software

The demonstration software, included in the STM32Cube MCU Package corresponding to the on-board microcontroller, is preloaded in the STM32 flash memory for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation can be downloaded from *www.st.com*.

4 Conventions

Table 3 provides the conventions used for the ON and OFF settings in the present document.

Table 3. ON/OFF convention

Convention	Definition
Jumper JPx ON	Jumper fitted
Jumper JPx OFF	Jumper not fitted
Jumper JPx [1-2]	Jumper fitted between Pin 1 and Pin 2
Solder bridge SBx ON	SBx connections closed by 0 Ω resistor
Solder bridge SBx OFF	SBx connections left open
Resistor Rx ON	Resistor soldered
Resistor Rx OFF	Resistor not soldered
Capacitor Cx ON	Capacitor soldered
Capacitor Cx OFF	Capacitor not soldered

5 Quick start

The STM32U5 Nucleo-144 board is a low-cost and easy-to-use development kit, to quickly evaluate and start development with an STM32U5 Series microcontroller in an LFQFP144-pin package. Before installing and using the product, accept the Evaluation Product License Agreement from the www.st.com/epla webpage. For more information on the STM32U5 Nucleo-144 board and demonstration software, visit the www.st.com/stm32nucleo webpage.

5.1 Getting started

Follow the sequence below to configure the STM32U5 Nucleo-144 board and launch the demonstration application (refer to Figure 4 for component location):

1. Check the jumper position on the board (refer to Default board configuration).
2. For the correct identification of the device interfaces from the host PC and before connecting the board, install the STLINK-V3E USB driver available on the *www.st.com* website.
3. Connect the STM32U5 Nucleo-144 board to a PC with a USB cable (USB Type-A or USB Type-C® to Micro-B) through the USB connector (CN1) to power the board.
4. The 5V_PWR green (LD5) and COM (LD4) LEDs light up, and the green LED (LD1) blinks.
5. Press the blue user button (B1).
6. Observe how the blinking of the LEDs (LD1, LD2, and LD3) changes, according to the clicks on the button (B1).
7. Download the demonstration software and several software examples that help to use the STM32 Nucleo features. These are available on the *www.st.com* website.
8. Develop your application using the available examples.

5.2 Default board configuration

By default, the STM32U5 Nucleo-144 board is configured with VDD_MCU@3V3. It is possible to set the board for VDD_MCU@1V8. Before switching to 1V8, check that the extension module and external shield connected to the NUCLEO board are 1.8 V compatible.

The default jumper configuration and voltage setting are shown in Table 4.

Table 4. Default jumper configuration

Jumper	Definition	Default position	Comment
JP1	STLK_NRST	OFF	STLINK-V3E MCU not under reset mode
JP2	T_NRST	ON	RST connected between MCU target and debugger
JP4	VDD	[1-2]	VDD MCU voltage selection 3V3
JP5	IDD measurement	ON	MCU VDD current measurement
JP6	5V power selection	[1-2]	5V from STLINK-V3E
JP7	UCPD_DBCC1	OFF	Refer to Section 6.11.2 UCPD.
JP8	UCPD_DBCC2	OFF	Refer to section Section 6.11.2 UCPD.

Figure 2. **Default board configuration**

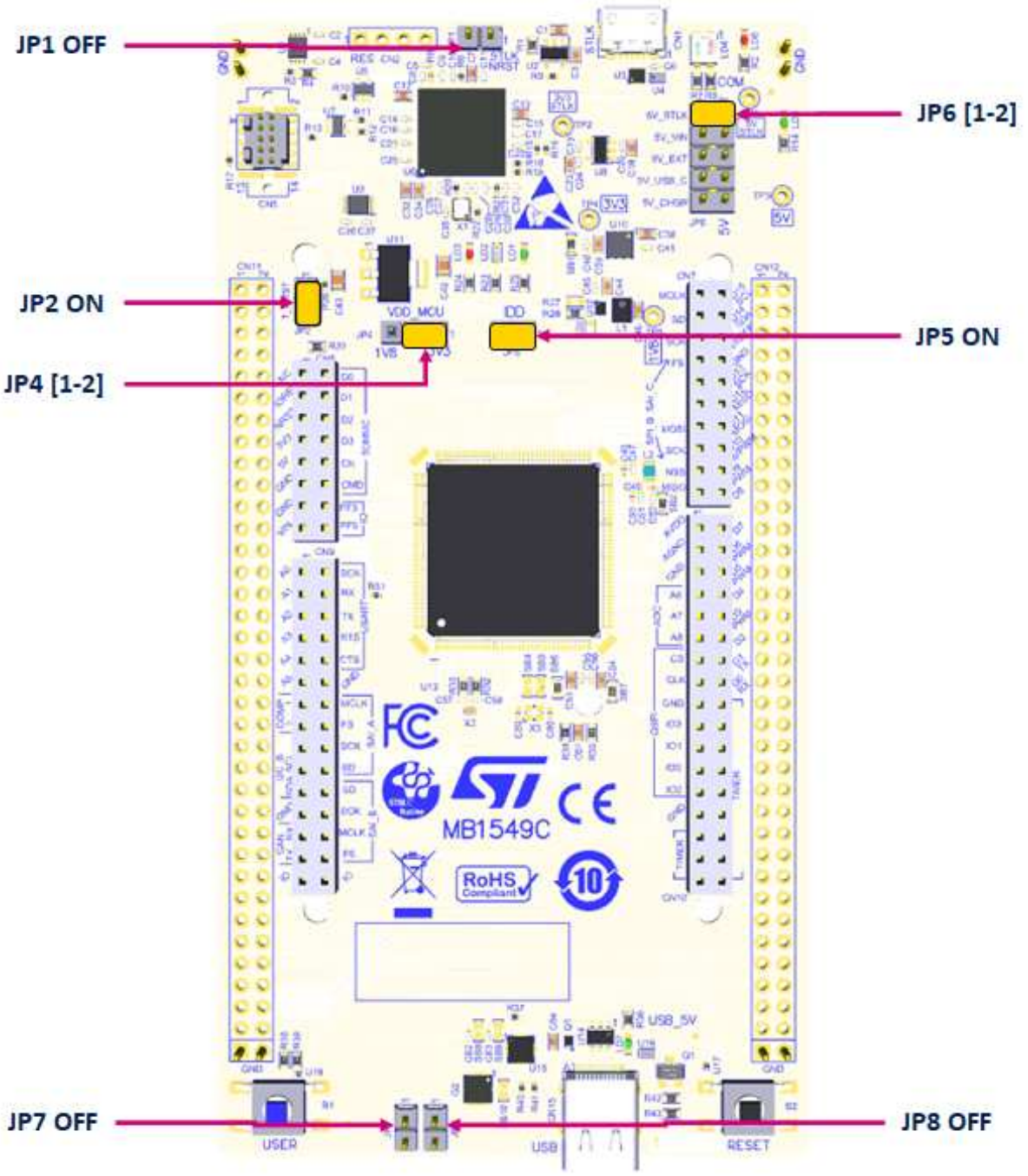


Table 5 explains the other jumper settings and configurations.

Table 5. Jumper configuration

Jumper	Definition	Setting[1]	Comment
JP1	STLK_RST	ON	Use to reset the STLINK-V3E MCU when an external debug probe is used.
		OFF	**Normal mode: use the STLINK-V3E debug probe**
JP2	T_NRST	**ON**	**STLINK-V3E can reset the target MCU.**
		OFF	STLINK-V3E cannot reset the target MCU. Configuration to use when an external debug probe is used.
JP4	VDD voltage selection	**[1-2]**	**VDD voltage selection is 3V3**
		[2-3]	VDD voltage selection is 1V8
		OFF	No internal VDD power supply (External 3V3 or 1V8 needed)
JP5	IDD measurement	**ON**	**MCU is powered by the on-board power supplies.**
		OFF	Use an ammeter to measure the MCU power consumption, or connect an external source 3V3 or 1V8 on pin 2 to supply the MCU (STLINK-PWR tools with STM32CubeMonitor-Power or ULPBench probe as exemple)
JP6	5V Power selection	**[1-2]**	**5V source from STLINK-V3E**
		[3-4]	5V source from ARDUINO® VIN 7-12V
		[5-6]	5V source from 5V_EXT
		[7-8]	5V source from USB Type-C®
		[9-10]	5V source from USB_CHGR. From STLINK-V3E USB connector (CN1) without overcurrent protection.
		OFF	NO 5V power source, configuration when external 3V3 is used.
JP7	UCPD_DBCC1	**OFF**	**UCPD_DBCC1 NOT connected to GND**
		ON	UCPD_DBCC1 connected to GND (For debug purpose)
JP8	UCPD_DBCC2	**OFF**	**UCPD_DBCC2 NOT connected to GND**
		ON	UCPD_DBCC2 connected to GND (For debug purpose)

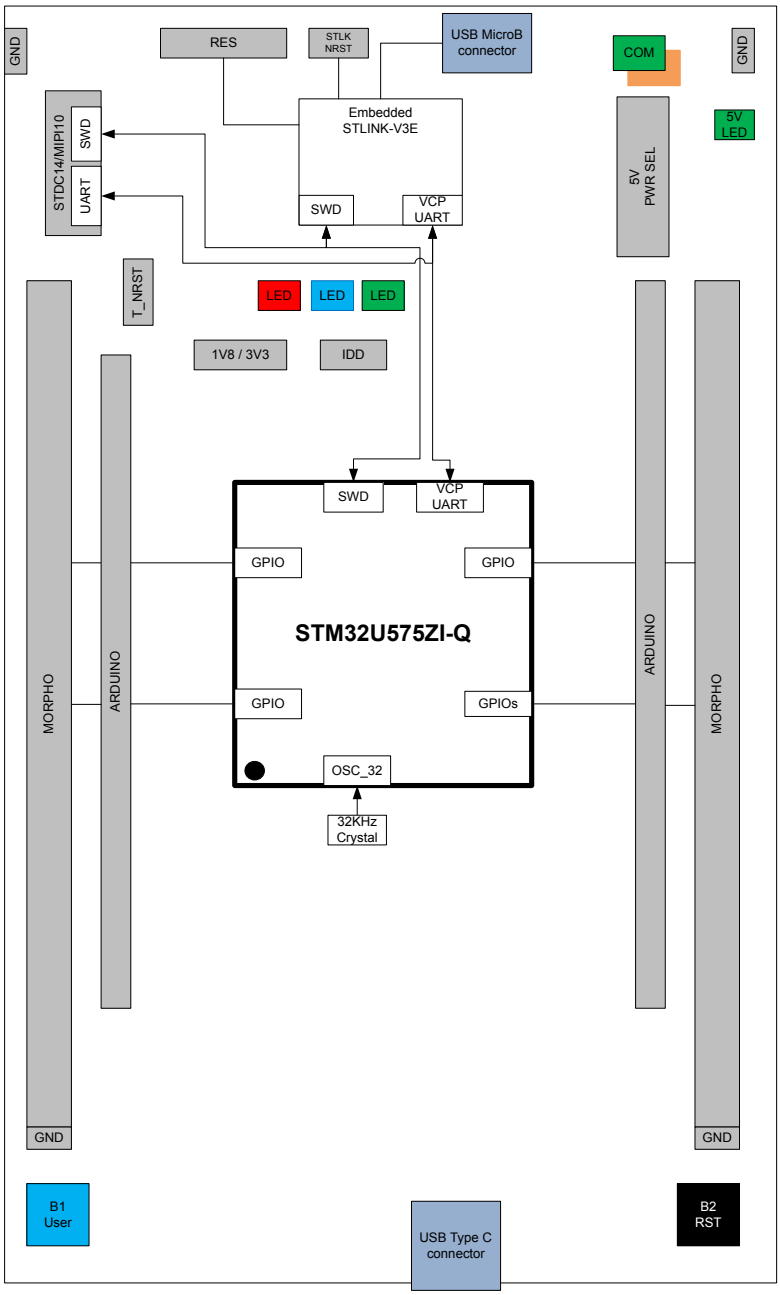
1. *The default configuration is in bold.*

6 Hardware layout and configuration

The STM32U5 Nucleo-144 board is designed around an STM32U5 microcontroller in an LFQFP 144-pin package. Figure 3 shows the connections between the STM32 and its peripherals (STLINK-V3E, push-buttons, LEDs, USB ST Zio connectors, and ST morpho headers). Figure 4 and Figure 5 show the location of these features on the STM32U5 Nucleo-144 board.

The mechanical dimensions of the board are shown in Figure 6.

Figure 3. Hardware block diagram



6.1 STM32U5 Nucleo-144 board layout

Figure 4. **STM32U5 Nucleo-144 board top layout**

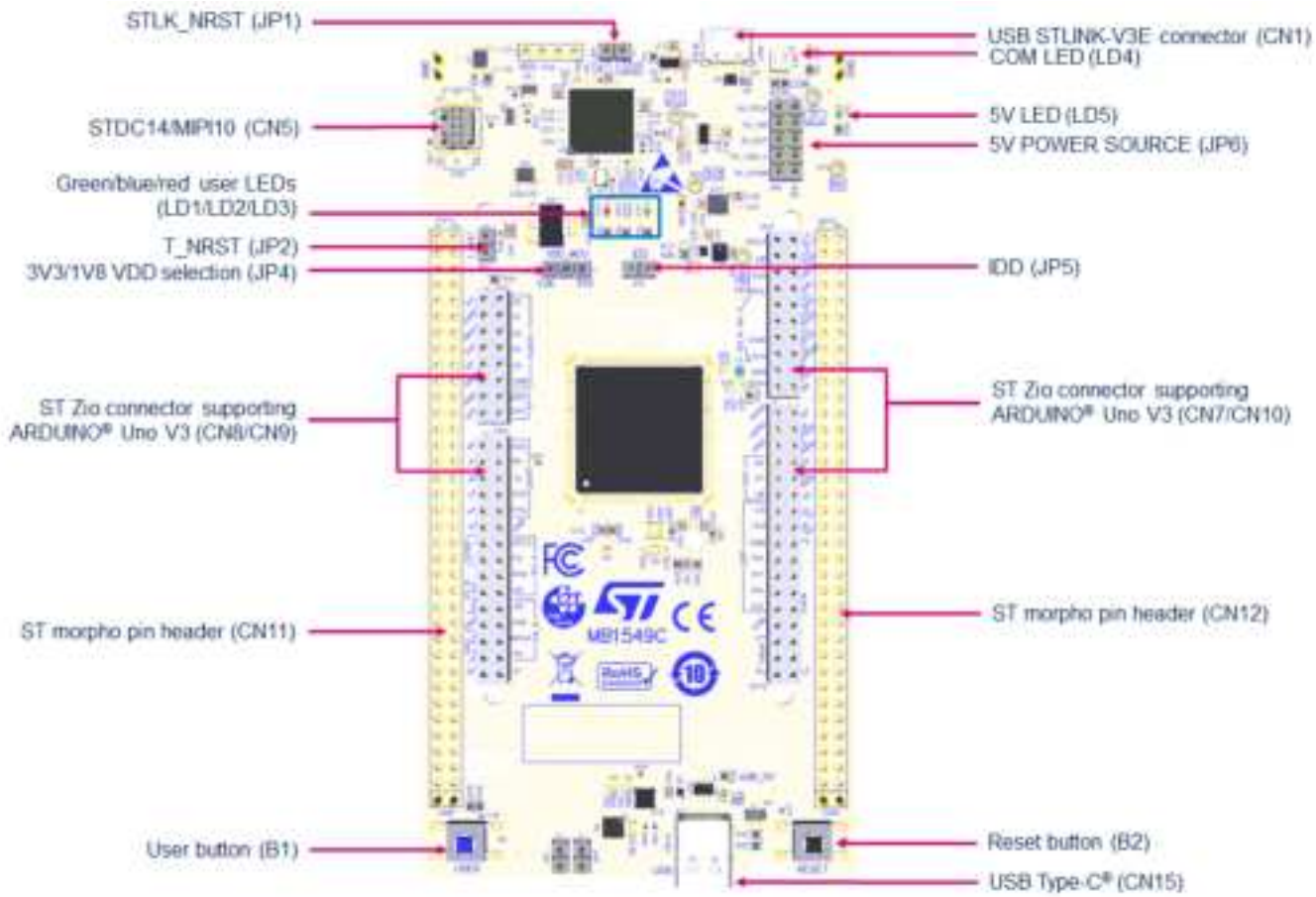
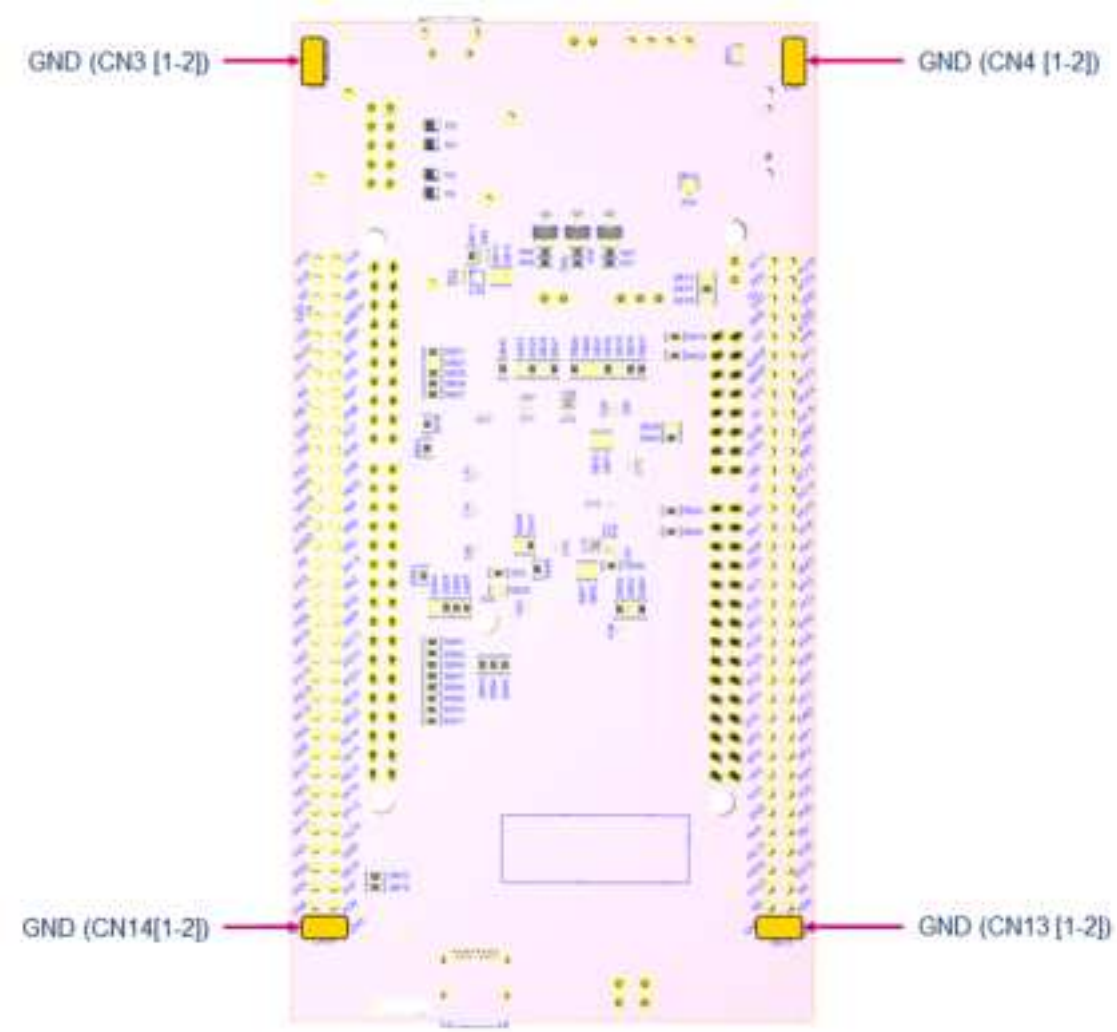
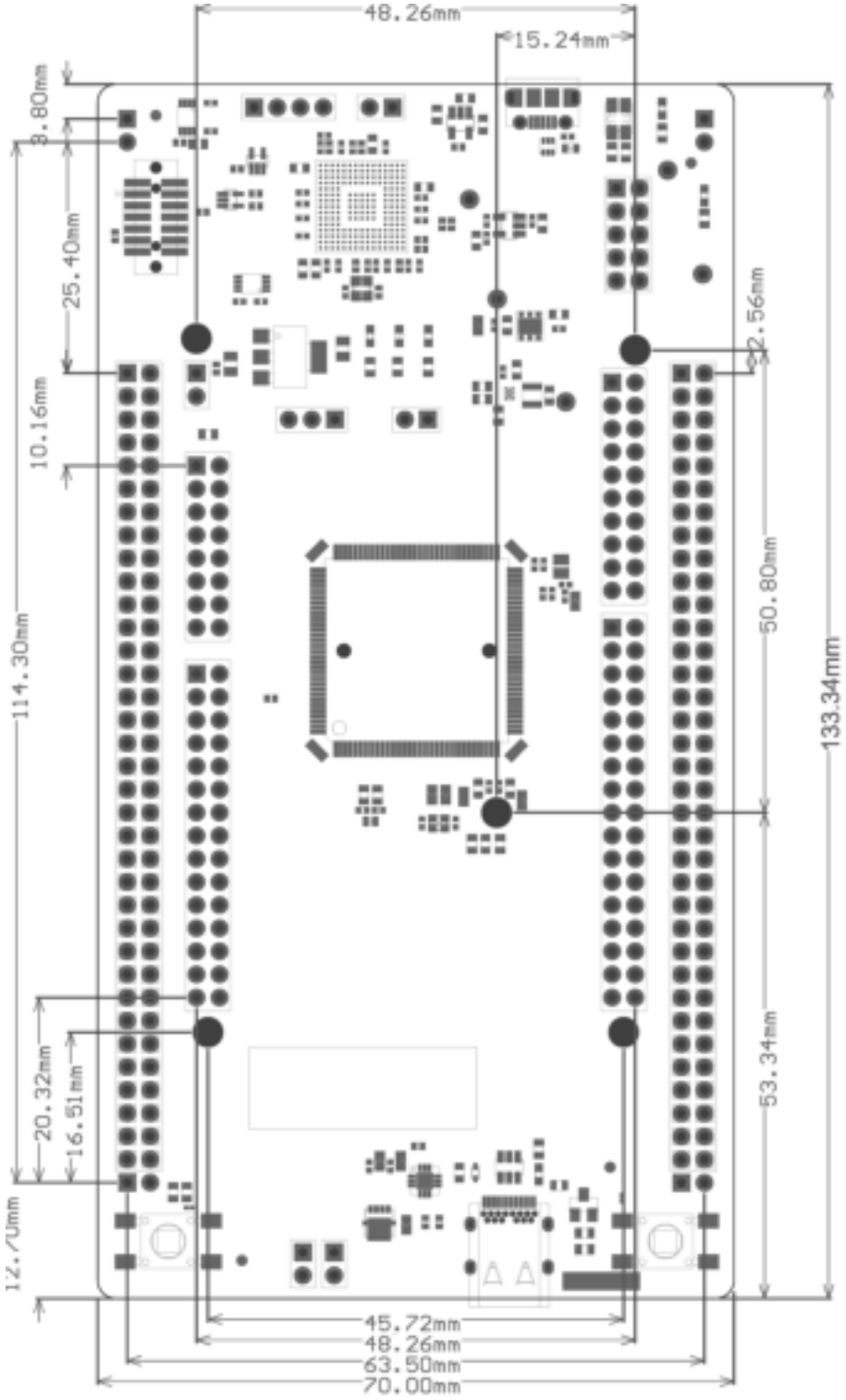


Figure 5. **STM32U5 Nucleo-144 board bottom layout**



6.2 Mechanical drawing

Figure 6. **STM32U5 Nucleo-144 board mechanical drawing (in millimeter)**



6.3 Embedded STLINK-V3E

There are two different ways to program and debug the onboard STM32 MCU:

- Using the STLINK-V3E programming and debugging tool on the STM32U5 Nucleo-144
- Using an external debug tool connected to the STDC14/MIPI-10 connector (CN5)

The STLINK-V3E makes the NUCLEO-U575ZI-Q Nucleo-144 board Arm® Mbed Enabled™.

The embedded STLINK-V3E supports only SWD and VCP for STM32 devices. For information about debugging and programming features of STLINK-V3, refer to the user manual *STLINK-V3SET debugger/programmer for STM8 and STM32* (UM2448) which describes in detail all the STLINK-V3 features.

STLINK-V3E description:

- 5V power supplied by USB connector (CN1)
- USB 2.0 high-speed compatible interface
- JTAG and SWD protocols compatible with 1.7 to 3.6 V application voltage and 5 V tolerant input I/Os
- Serial wire viewer (SWV) output
- STDC14 MIPI-10 compatible connector (CN5)
- COM status LED blinking during communication with the PC (LD4)
- 5 V/300 mA output power supply capability with current limitation (U2)
- OC fault red LED alerting on USB overcurrent request (LD6)
- 5V_PWR 5 V power green LED (LD5)

Table 6 describes the USB Micro-B connector (CN1) pinout.

Table 6. USB Micro-B connector (CN1) pinout

Pin	Pin name	Signal name	STLINK-V3E STM32 pin	Function
1	VBUS	5V_USB_CHGR	-	VBUS Power
2	DM	USB_DEV_HS_CN_N	PB14	DM
3	DP	USB_DEV_HS_CN_P	PB15	DP
4	ID	-	-	ID
5	GND	GND	GND	GND

6.3.1 Drivers

Before connecting the STM32U5 Nucleo-144 board to a Windows 7®, Windows 8®, or Windows 10® PC via USB, a driver for the STLINK-V3E (stsw-link009) must be installed (not required for Windows 10®). It is available on the *www.st.com* website.

In case the STM32U5 Nucleo-144 board is connected to the PC before the driver is installed, a peripheral may be declared as “Unknown” in the PC device manager. In this case, the user must install or update the driver files from the device manager as shown in Figure 7.

Note: Prefer using the USB Composite Device handle for a full recovery.

Figure 7. USB composite device

Note: 37xx:

- *374E for STLINK-V3E without bridge functions*
- *374F for STLINK-V3E with bridge functions*

6.3.2 STLINK-V3E firmware upgrade

The STLINK-V3E embeds a firmware upgrade mechanism through the USB port. As the firmware may evolve during the lifetime of the STLINK-V3E product, to add new functionalities, fix bugs, and support new microcontroller families, it is recommended to visit the *www.st.com* website before starting to use the STM32U5 Nucleo-144 board and periodically, to stay up-to-date with the latest firmware version.

6.3.3 Using an external debug tool to program and debug the on-board STM32

There are two basic ways to support an external debug tool:

1. Keep the embedded STLINK-V3E running. Power on the STLINK-V3E at first until the COM LED turns red. Then connect the external debug tool through the STDC14/MIPI-10 debug connector (CN5)
2. Set the embedded STLINK-V3E in a high-impedance state. When the JP1 STLK_RST jumper is ON, the embedded STLINK-V3E is in RESET state and all GPIOs are in high impedance. Remove JP2 to avoid driving MCU T_NRST. Then, connect the external debug tool to the STDC14/MIPI-10 debug connector (CN5).

Figure 8. Connecting an external debug tool to program the on-board STM32U5

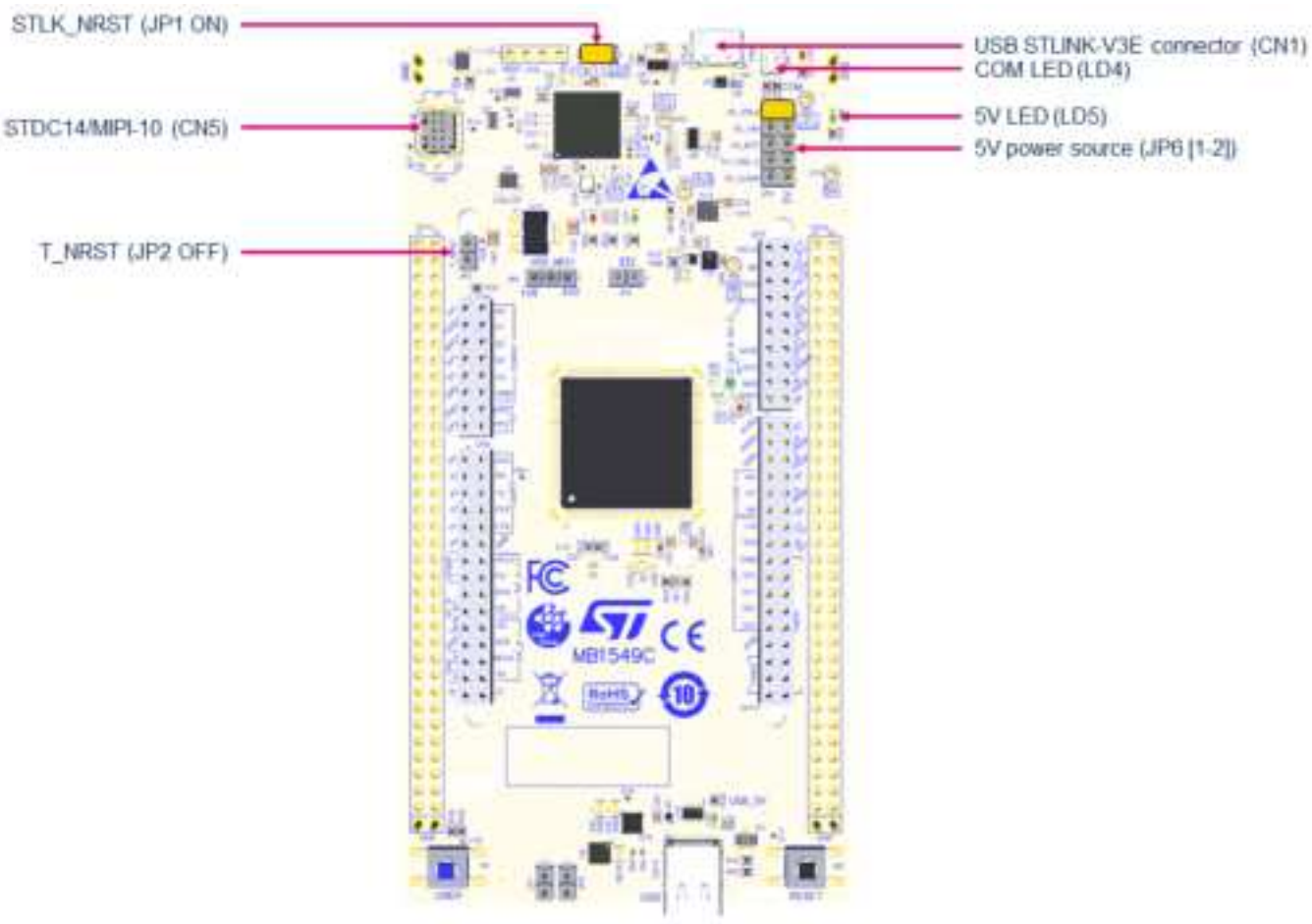


Figure 9 shows the STDC14/MIPI-10 connector (CN5).

Figure 9. STDC14/MIPI-10 debug connector (CN5)

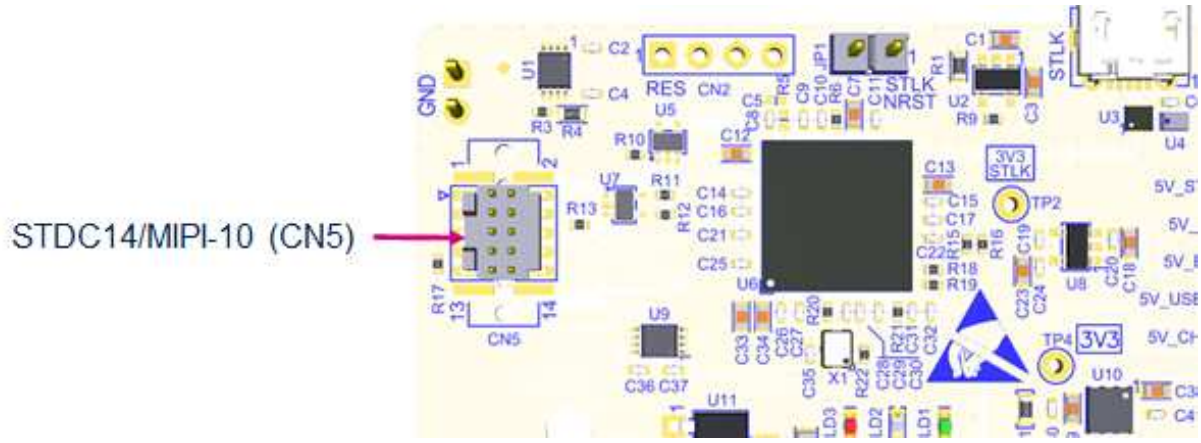


Table 7 describes the STDC14/MIPI-10 connector (CN5) pinout.

Table 7. STDC14/MIPI-10 debug connector (CN5) pinout

MIPI-10 pin	STDC14 pin	CN5	Function
-	1	NC	Reserved
-	2	NC	Reserved
1	3	VDD	Target VDD
2	4	T_SWDIO	Target SWDIO using SWD protocol or target JTMS (T_JTMS) using JTAG protocol
3	5	GND	Ground
4	6	T_SWCLK	Target SWCLK using SWD protocol or target JTCK (T_JTCK) using JTAG protocol
5	7	GND	Ground
6	8	T_SWO	Target SWO using SWD protocol or target JTDO (T_JTDO) using JTAG protocol (SB44 ON)
7	9	NC	-
8	10	T_JTDI	Not used by SWD protocol, target JTDI (T_JTDI) using JTAG protocol, only for external tools (SB39 OFF)
9	11	GNDDetect	GND detect for plug indicator
10	12	T_NRST	Target NRST using SWD protocol or target JTMS (T_JTMS) using JTAG protocol
-	13	T_VCP_RX	Target RX used for VCP (with UART supporting bootloader)
-	14	T_VCP_TX	Target TX used for VCP (with UART supporting bootloader)

Two SN74LVC2T45DCUT level shifters are used on VCP and SWD interface to offer a debug capability with 1V8 powered MCU. One level shifter is used for a signal from the MCU target (1V8) to STLINK-V3E (3V3).

- U1 used for T_VCP_TX signal
- U9 used for T_SWDIO and T_SWO signal

6.4 Power supply and power selection

6.4.1 External power supply input

The Nucleo board is designed to be powered by several DC power supplies. It is possible to configure the Nucleo board to use any of the following sources for the power supply:

- 5V_STLK from STLINK-V3E USB connector (CN1)
- VIN (7 to 12 V) from ARDUINO®-included Zio connector (CN8) or ST morpho connector (CN11)
- 5V_EXT from ST morpho connector (CN11)
- 5V_USB_C from USB Type-C® connector (CN15)
- 5V_CHGR from STLINK-V3E USB connector (CN1)
- 3V3 from ARDUINO®-included Zio connector (CN8) or ST morpho connector (CN11)

If VIN, 5V_EXT, or 3V3 is used to power a Nucleo-144 board, this power source must comply with the standard EN-60950-1: 2006+A11/2009 and must be safety extra-low voltage (SELV) with limited power capability.

The power supply capabilities are summarized in Table 8.

Table 8. Power sources capability

Input Power name	Connector pins	Voltage range	Max. current	Limitation
5V_STLK	CN1 pin 1 JP6 [1-2]	4.75 to 5.25 V	500 mA	The maximum current depends on the presence or absence of USB enumeration: • 100 mA without enumeration • 500 mA with enumeration OK
VIN / 5V_VIN	CN8 pin 15 CN11 pin 24 JP6 [3-4]	7 to 12 V	800 mA	From 7 to 12 V only and input current capability is linked to input voltage: • 800 mA input current when VIN = 7 V • 450 mA input current when 7 V < VIN < 9 V • 250 mA input current when 9 V < VIN < 12 V
5V_EXT	CN11 pin 6 JP6 [5-6]	4.75 to 5.25 V	500 mA	The maximum current depends on the power source
5V_USB_C	CN15 JP6 [7-8]	4.75 to 5.25 V	1 A	The maximum current depends on the USB host used to power the Nucleo
5V_CHGR	CN1 pin 1 JP6 [9-10]	4.75 to 5.25 V	500 mA	The maximum current depends on the USB wall charger used to power the Nucleo
3V3	CN8 pin 7 CN11 pin 16 JP5 pin 2	3.0 to 3.6 V	-	The maximum current depends on the 3V3 source. Used when the ST-LINK part of PCB is not used or removed. SB1 must be OFF to protect LDO U6.

5V_STLK is a DC power with the limitation from the STLINK-V3E USB connector (USB Type Micro-B connector of STLINK-V3E). In this case, the JP6 jumper must be on pin [1-2] to select the 5V_STLK power source. This is the default setting. If the USB enumeration succeeds, the 5V_STLK power is enabled, by asserting the T_PWR_EN signal from U6 STLINK-V3E MCU. This pin is connected to the U2 power switch, which powers the board. This power switch also features a 500 mA current limitation, to protect the PC in case of an onboard short-circuit.

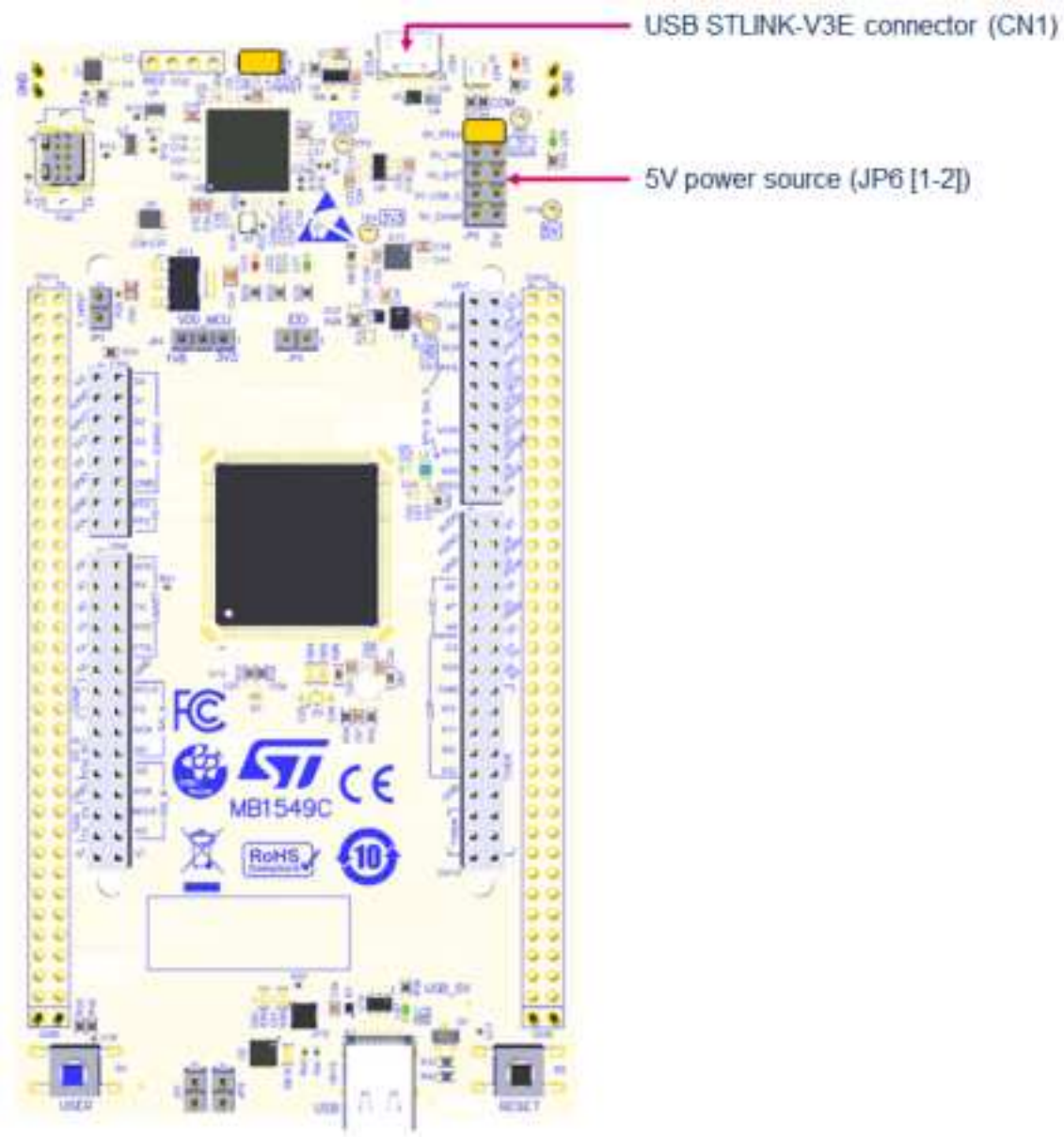
The STM32U5 Nucleo-144 board with its shield can be powered from the STLINK-V3E USB connector (CN1), but only the STLINK-V3E circuit has the power before USB enumeration because the host PC only provides 100mA to the board at that time. During the USB enumeration, the Nucleo board requires a 500mA current to the host PC.

- If the host can provide the required power, the enumeration finishes by a `SetConfiguration` command and then, the U2 power switch is switched ON, the Green LED LD5 is turned ON, thus the Nucleo board with its shield can consume 500mA current, but no more.

- If the host is not able to provide the requested current, the enumeration fails. Therefore, the U2 power switch remains OFF and the MCU part including the extension board is not powered. As a consequence, the LD5 green LED remains OFF. In this case, it is mandatory to use an external power supply.

5V_STLK configuration: The JP6 jumper is set on [1-2] as shown in Figure 10.

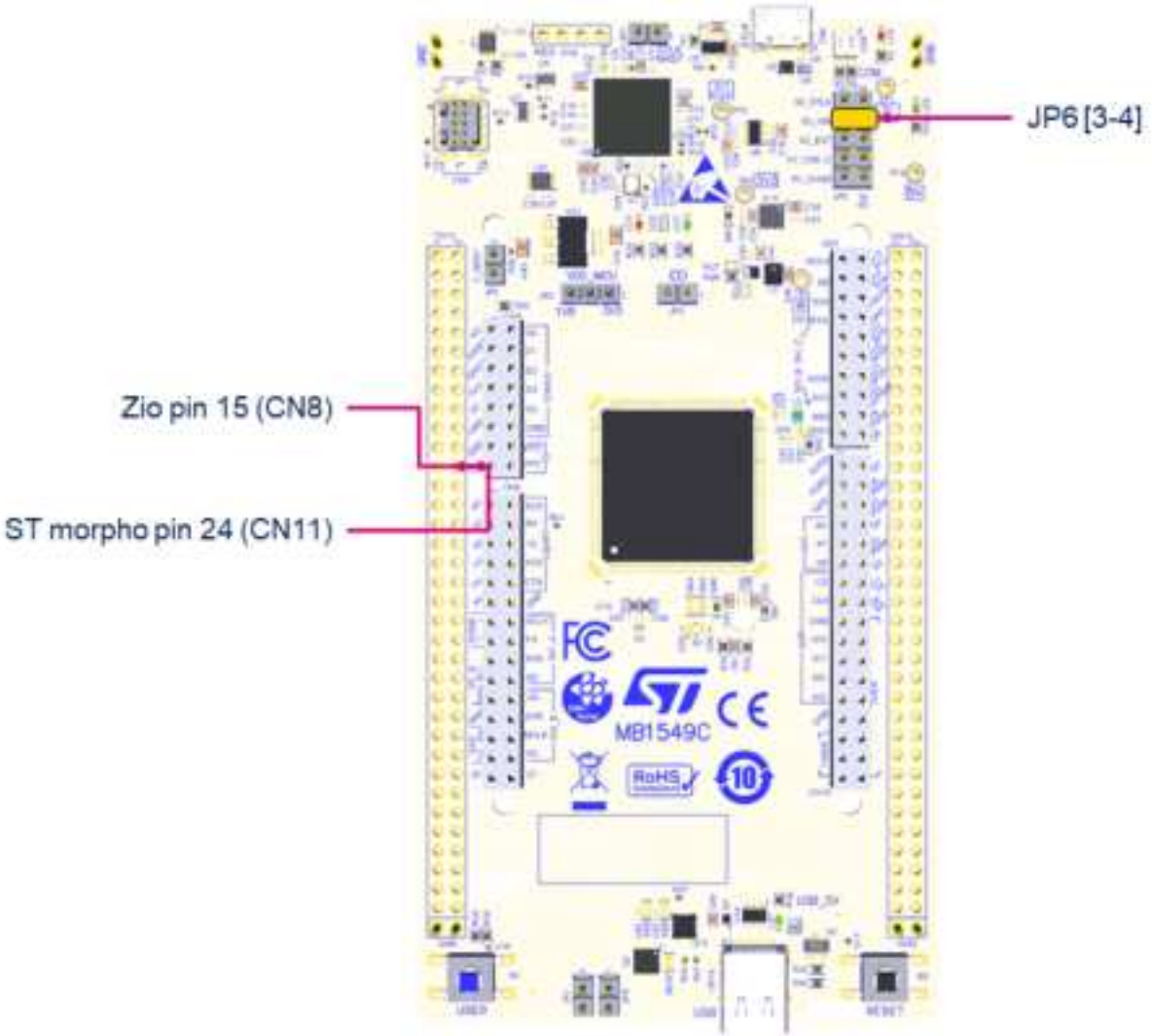
Figure 10. JP6 [1-2]: 5V_STLK power source



VIN (5V_VIN) is the 7 to 12 V DC power from the ARDUINO®-included Zio connector CN8 pin 15 named VIN on the connector silkscreen, or from the ST morpho connector CN11 pin 24. In this case, the JP6 jumper must be on pin [3-4] to select the 5V_VIN power source. In that case, the DC power comes from the power supply through the ARDUINO® Uno V3 battery shield (compatible with Adafruit PowerBoost 500 shield).

5V_VIN configuration: The JP6 jumper must be set on [3-4] as shown in Figure 11.

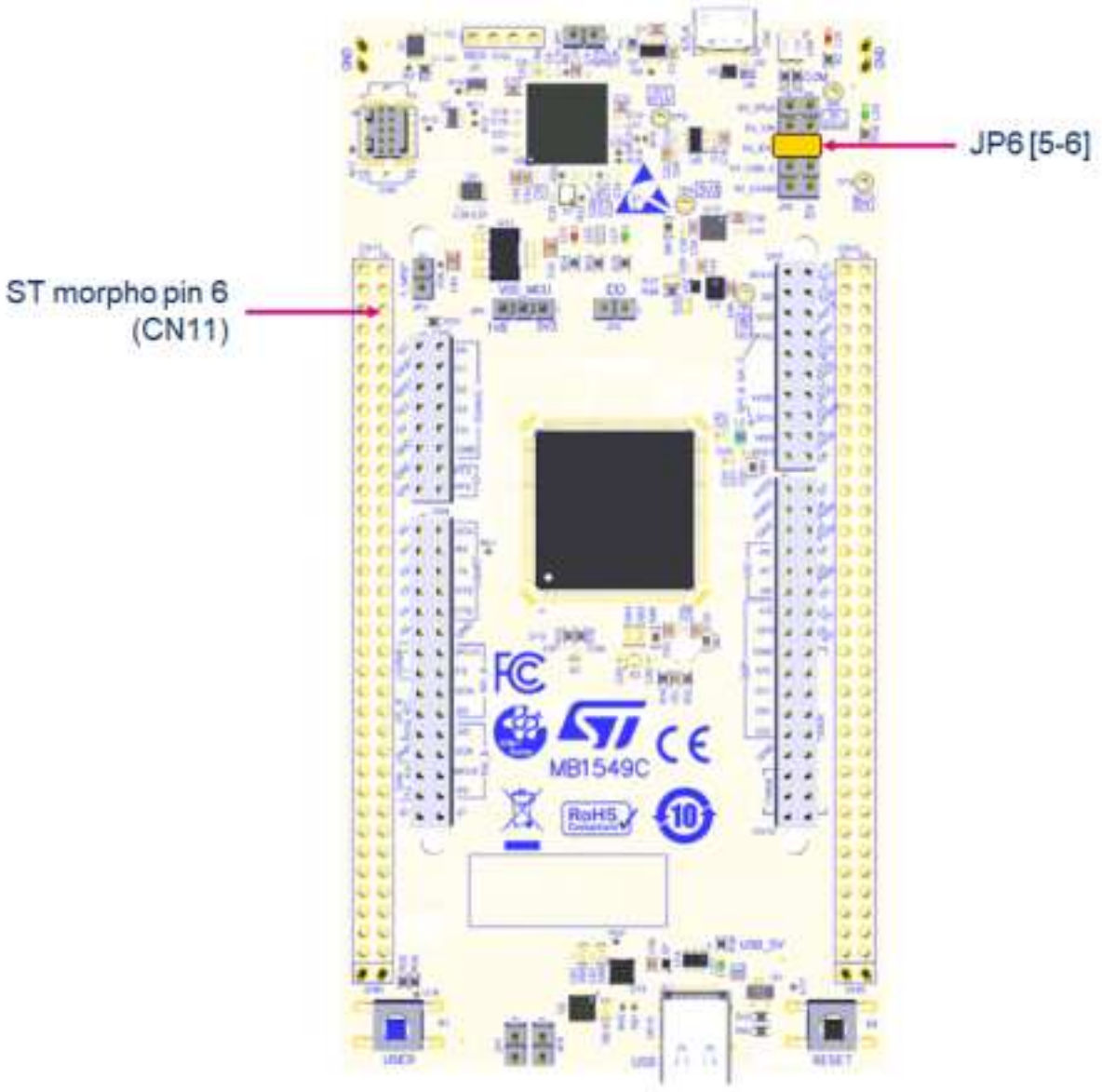
Figure 11. JP6 [3-4]: 5V_VIN power source



5V_EXT is the DC power coming from an external 5 V DC power from the ST morpho connector CN11 pin 6. In this case, the JP6 jumper must be set on [5-6] to select the 5V_EXT power source.

5V_EXT configuration: The JP6 jumper must be set on [5-6] as shown in Figure 12.

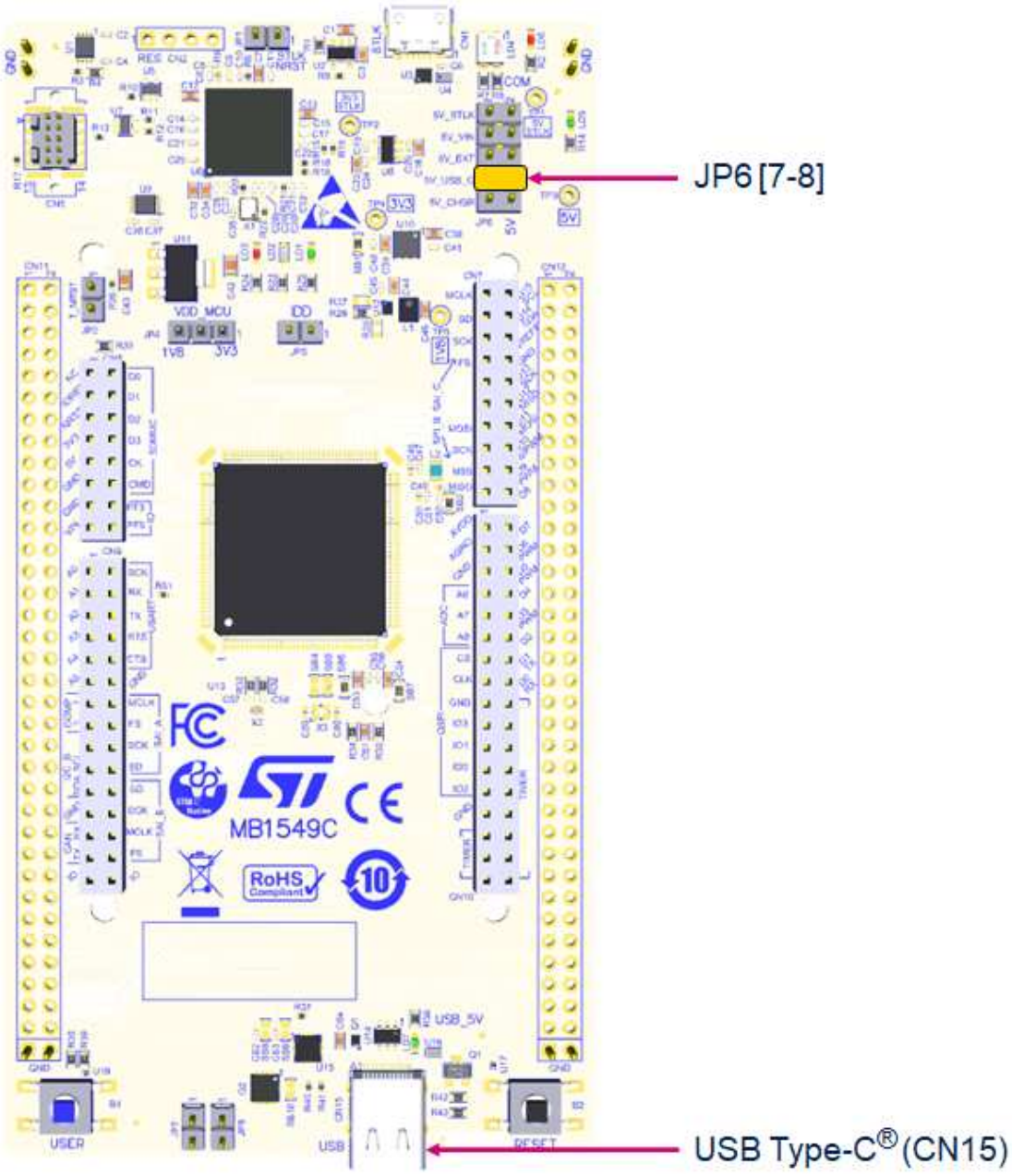
Figure 12. JP6 [5-6]: 5V_EXT power source



5V_USB_C is the DC power supply connected to the USB Type-C® user connector (CN15). In this case, the JP6 jumper must be set on [7-8] to select the 5V_USB_C power source.

5V_USB_C configuration: The JP6 jumper must be set on [7-8] as shown in Figure 13.

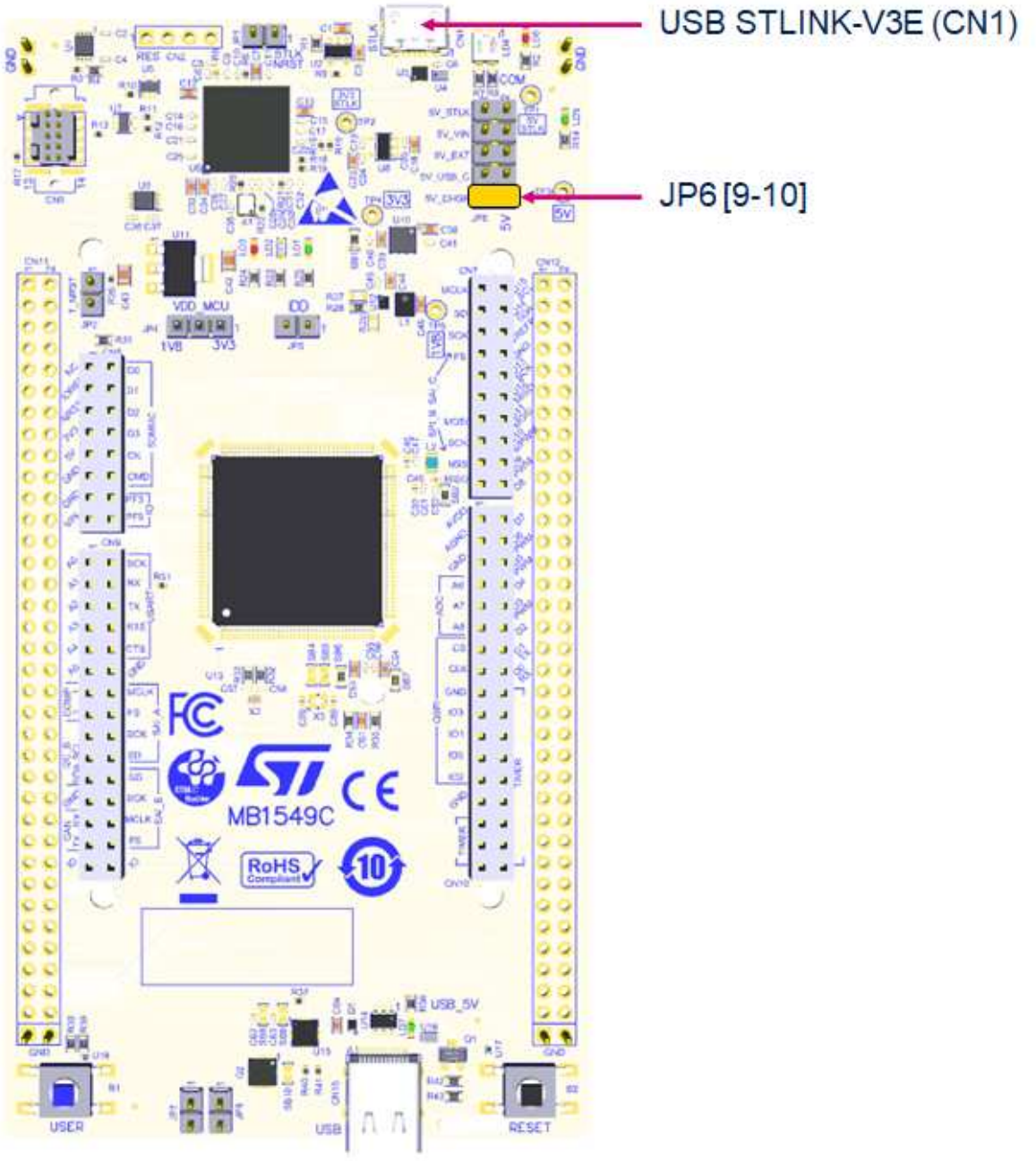
Figure 13. JP6 [7-8]: 5V_USB_C power source



5V_CHGR is the DC power charger connected to the USB STLINK-V3E connector (CN1). In this case, the JP6 jumper must be set on [9-10] to select the 5V_CHGR power source. If an external USB charger powers the Nucleo board, then the debug through CN1 is not available. If a computer is connected instead of the charger, the current limitation is no more effective. In this case, the computer can be damaged, and it is recommended to select 5V_STLK mode.

5V_CHGR configuration: The JP6 jumper must be set on [9-10] as shown in Figure 14.

Figure 14. JP6 [9-10]: 5V_CHGR power source



Note: With this 5V_CHGR JP6 configuration, the USB_PWR protection is bypassed. Never use this configuration with a computer connected instead of the charger, because as the USB_PWR protection is bypassed, the board eventually requests more than 500 mA and this can damage the computer.

External 3V3 power supply input. In certain situations, it is interesting to use an external 3V3 (CN8 pin 7, CN11 pin 16, or JP5 pin 2) directly as power input, for instance in case the 3V3 is provided by an extension board. When Nucleo is powered by 3V3, the STLINK-V3E is not powered thus programming and debug features are unavailable.

With external 3V3 the STLINK-V3E part is not supplied, so JP2 (T_NRST) must be removed to avoid keeping the target MCU in the reset state.

6.4.2 Programing/debugging when the power supply is not from STLINK-V3E (5V_STLK)

VIN, 5V_EXT, or 5V_USB_C can be used as an external power supply, in case the current consumption of the Nucleo with expansion boards exceeds the allowed current on USB. In such a condition, it is still possible to use USB for communication for programming or debugging only.

In this case, it is mandatory to power the board first using VIN, 5V_EXT, or 5V_USB_C then connect the USB cable to the PC. Proceeding this way the enumeration succeeds, thanks to the external power source.

The following power sequence procedure must be respected:

1. Connect the JP6 jumper according to the 5V selected external power source.
2. Connect the external power source according to JP6.
3. Power ON the external power supply.
4. Check that the LD5 5V green LED is turned ON.
5. Connect the PC to the USB connector (CN1).

If this sequence is not respected, the board may be powered by V_{BUS} first from STLINK-V3E, and the following risk may be encountered:

- If more than 500 mA current is needed by the board, the PC may be damaged or the current can be limited by the PC. Therefore, the board is not powered correctly.
- 500 mA is requested at enumeration so there is a risk that the request is rejected and enumeration does not succeed if PC cannot provide such current. Consequently, the board is not powered (LD5 LED remains OFF).

6.4.3 Power supply output

- **5V**: When the Nucleo board is powered by USB, VIN, or 5V_EXT, the 5V present on CN8 pin 9 or CN11 pin 18 can be used as an output power supply for an ARDUINO® shield or an extension board. In this case, the maximum current of the power source specified in Table 6 must be respected.
- **3V3**: The internal 3V3, on CN8 pin 7 or CN11 pin 16, can be used also as power supply output. The current is limited by the maximum current capability of the U10 regulator (LD39050PUR33 from STMicroelectronics: 500 mA maximum concerning Nucleo board with shield consumption).

6.4.4 Internal power supply

The Nucleo boards are designed to support two specific voltage configurations:

- 3V3 VDD configuration to reach the Nucleo low-power mode with 3.3 V
- 1V8 VDD configuration to demonstrate the MCU low-voltage capability

6.4.4.1 3V3

Regardless of the 5V power source, an LDO is used to switch from 5V to the 3V3 default power source of the VDD. The maximum current capability of this source is 500 mA. To select the 3V3 voltage for the VDD, set the JP4 jumper on [1-2].

A solder bridge (SB1) is used to disconnect the LDO output when an external 3V3 is applied to the Nucleo board.

- SB1 ON: U10 LDO output provides a 3V3 power supply (default configuration).
- SB1 OFF: U10 LDO output does not provide 3V3. An external 3V3 is needed.

6.4.4.2 1V8

An external SMPS can be used for the MCU to work at 1V8. This helps to demonstrate the 1V8 MCU capability. The external SMPS capability is 400 mA. Before using the 1V8 voltage it is necessary to check that all interfaces are 1V8 compatible and the maximum current requested does not exceed 400mA. To select the 1V8 voltage for the VDD, set the JP4 jumper on [2-3].

In this mode, it is possible to keep some MCU voltage domain on 3V3 depending on the application use case. The MCU voltage selection is done according to the solder bridge configuration. Refer to Table 9 for solder bridge configuration.

6.4.4.3 *JP4 VDD voltage selection 1V8/3V3*

The JP4 jumper selects the VDD voltage:

- Set JP4 on [1-2] to set VDD to 3V3.
- Set JP4 on [2-3] to set VDD to 1V8.

The current consumption on this jumper includes the MCU pin connected to VDD_MCU and the other features supplied by VDD, such as the U9 level shifter supply pin for 1V8 STLINK-V3E compatibility and the LEDs.

The level shifter consumption is negligible according to correct SWD I/O settings to avoid an I/O floating level.

6.4.5 MCU power supply

To supply correctly the MCU, it is mandatory to configure the solder bridges as shown in Table 9.

Table 9. MCU power supplies

Solder bridge configuration	MCU power supply
JP4 [1-2] / JP4 [2-3]	VDD selection: Jumper selection for VDD 3V3 / 1V8
JP5 [1-2] / ammeter	IDD: JP5 ON to supply the MCU or connected with an ammeter to do current measurement.
SB2 ON	SB for VDDSMPS input voltage
SB3 ON	SB for VREFP input voltage
SB30 ON	SB for VDDUSB input voltage
SB28 ON / SB29 OFF	SB for VDDIO2 PG[2-15] input voltage SB28 ON / SB29 OFF: VDDIO follows 1V8 to 3V3 VDD_MCU. SB28 OFF / SB29 ON: VDDIO fixed to 3V3 whatever the VDD-MCU voltage is.
SB50 ON	SB for VBAT input voltage
SB55 OFF / SB54 ON	SB for VDDA/VREF input voltage SB55 ON / SB54 OFF: VDDA/VREF follows 1V8 to 3V3 VDD_MCU. SB55 OFF / SB54 ON: VDDA/VREF fixed to 3V3 whatever the VDD-MCU voltage is. For more detail about VDDA/VREFP power supply, refer to the MCU datasheet.

Warning: *1V8 voltage is given as an example, but the power on sequence implementation is not respected when using 1V8 VDD. Refer to the application note STM32U5 Series hardware getting started (AN5373), and STM32U5xx products datasheets for power sequencing.*

INTERNAL VCORE SMPS power supply

Power figures in run mode are significantly improved, by generating V_{core} logic supply from the internal DC/DC converter (this function is only available on '-Q' suffixed boards).

For all general information concerning design recommendations for STM32U5 with internal SMPS and design guide for ultra-low-power applications with performance, refer to the application note *STM32U5 Series hardware getting started* (AN5373) at the *www.st.com* website.

6.4.6 VDD_MCU IDD measurement

The labeled **IDD** JP5 jumper can measure the consumption of the STM32 microcontroller by replacing the jumper with an ammeter or a current measurement tool.

- Jumper ON: STM32 Microcontroller is powered (default).
- Jumper OFF: an ammeter or an external 3V3 power source must be connected to power and measure the STM32 microcontroller consumption.

The **IDD** jumper can perform the current measurement for both 3V3 and 1V8 MCU voltage ranges.

6.5 LEDs

User green LED (LD1)

The user green LED (LD1) is connected to the PC7 STM32 I/O (SB21 ON and SB23 OFF, default configuration) or PA5 (SB21 OFF and SB23 ON, optional configuration corresponding to the D13 ST Zio connector). A transistor is used to drive the LED whatever the MCU 1V8 or 3V3 voltage range is.

User blue LED (LD2)

The user blue LED (LD2) is connected to PB7. A transistor is used to drive the LED whatever the MCU 1V8 or 3V3 voltage range is.

User red LED (LD3)

The user red LED (LD3) is connected to PG2. A transistor is used to drive the LED whatever the MCU 1V8 or 3V3 voltage range is.

These user LEDs are ON when the I/O is in the HIGH state, and are OFF when the I/O is in the LOW state.

COM tricolor LED (LD4)

The tricolor (green, orange, and red) LED (LD4) provides information about STLINK-V3E communication status. The LD4 default color is red. LD4 turns green to indicate that the communication is in progress between the PC and the STLINK-V3E, with the following setup:

- Red LED ON: when the initialization between the PC and STLINK-V3E is complete
- Green LED ON: after a successful target communication initialization
- Blinking red/green: during communication with the target
- Orange ON: communication failure

Green PWR LED (LD5)

The green LED (LD5) indicates that the STM32 part is powered by a 5 V source, and this source is available on CN8 pin 9 and CN11 pin 18.

Red STLINK-V3E USB OC power switch fault LED (LD6)

The red LED (LD6) indicates that the board power consumption on USB exceeds 500 mA.

- If 500 mA or more is expected, the board must be supplied by one of the external 5 V sources compatible with more than 500 mA capability.
- If more than 500 mA is not expected, the board must be analyzed to understand the extra consumption.

USB Type-C® green LED (LD7)

The green LED (LD7) shows the presence of the 5V_USB_C. Refer to Section 6.11 USB Type-C FS for more details.

6.6 Push-buttons

Two buttons are available on the Nucleo board.

User button (B1)

The blue button for user and wake-up functions is connected to PC13 to support the default TAMPER function or to PA0 to support the optional wake-up function of the STM32 microcontroller. When the button is pressed the logic state is HIGH, otherwise, the logic state is LOW.

- To connect the USER button to PC13, SB58 must be ON and SB59 must be OFF. This is the default configuration.
- To connect the USER button to PA0, SB58 must be OFF and SB59 must be ON. This is the optional configuration.

Reset button (B2)

The black button connected to NRST is used to reset the STM32 microcontroller. When the button is pressed the logic state is LOW, otherwise, the logic state is HIGH.

The blue and black plastic hats placed on these push-buttons can be removed if necessary when a shield or an application board is plugged into the top of the Nucleo board. This avoids pressure on the buttons and consequently a possible permanent target MCU reset.

6.7 OSC clock sources

Three clock sources are described below:

- LSE is the 32.768 kHz crystal for the STM32 embedded RTC.
- MCO is the 8 MHz clock from STLINK-V3E MCU for the STM32 microcontroller.
- HSE is the 16 MHz oscillator for the STM32 microcontroller. This clock is not implemented in a basic configuration.

6.7.1 LSE: OSC 32 KHz clock supply

There are three ways to configure the pins corresponding to the low-speed clock (LSE):

LSE on-board oscillator X2 crystal (Default configuration)

Refer to the application note *Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs* (AN2867), with the following characteristics: 32.768 kHz, 9 pF, 20 ppm. It is recommended to use NX1610SE- 32.768KHZ-EXS00A- MU01499 manufactured by NDK. The following configuration is needed:

- R32 and R33 ON
- SB51 and SB52 OFF

Oscillator from external to PC14

From external oscillator through PC14, Zio connector CN11 pin 25. The following configuration is needed:

- R32 and R33 OFF
- SB51 and SB52 ON, for connection from Zio connector CN11 pin 25

LSE not used

PC14 and PC15 are used as GPIOs instead of low-speed clocks. The following configuration is needed:

- R32 and R33 OFF
- SB51 and SB52 ON

6.7.2 OSC clock supply

There are four ways to configure the pins corresponding to the external high-speed clock (HSE):

HSE: on-board oscillator X3 crystal (Default: not connected)

For typical frequencies, capacitors, and resistors, refer to the STM32 microcontroller datasheet. Refer to the application note *Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs* (AN2867). The X3 crystal has the following characteristics: 16 MHz, 8 pF, 20 ppm. It is recommended to use NX2016SA_16MHz_EXS00A-CS07826 manufactured by NDK. The following configuration is needed:

- SB47 and SB49 OFF. PH0/PH1 is not connected to CN11 as I/O.
- SB48 (MCO) OFF
- SB4 and SB5 ON are connected to external HSE.

MCO from STLINK-V3E (Default: not connected):

MCO output of STLINK-V3E MCU is used as an input clock. This frequency cannot be changed. It is fixed at 8 MHz, and connected to PH0 OSC_IN of STM32 microcontroller. The following configuration is needed:

- SB47 OFF and SB49 ON. Only PH1 can be connected to CN11 as I/O.
- SB48 ON. MCO is connected to PH0 and R5 on the STLINK-V3E side must be connected to provide the MCO to STLINK-V3E output.
- SB4 and SB5 OFF. The external crystal is not connected to HSE.

External oscillator (Default: not connected)

The input clock comes from an external oscillator through PH0, CN11 pin 29. The following configuration is needed:

- SB47 and SB49 ON. PH0/PH1 is connected to CN11.
- SB48 OFF. MCO is not connected to PH0.
- SB4 and SB5 OFF. The external crystal is not connected to HSE.

HSE not used (Default configuration)

PH0 and PH1 are used as GPIOs instead of clocks. The following configuration is needed:

- SB47 and SB49 ON. PH0/PH1 is connected to CN11 as I/O.
- SB48 OFF. MCO is not connected to PH0.
- SB4 and SB5 OFF. The external crystal is not connected to HSE.

6.8 Reset sources

The reset signal of the Nucleo board is active LOW and the reset sources include:

- The RESET button (B2)
- The embedded STLINK-V3E
- The ARDUINO®-included Zio connector CN8 pin 5
- The ST morpho connector CN11 pin 14

6.9 Virtual COM port (VCP)

An STM32 serial interface is connected to the STLINK-V3E debug interface. The user can choose between a USART or an LPUART interface.

The selection between USART and LPUART is performed by setting related solder bridges.

Refer to the tables below to set the USART or LPUART connection to the VCP interface

Table 10. USART1 connection

Solder bridge configuration(1)	Feature
SB32, SB34 ON **SB24 SB26 SB31 SB33 OFF**	**USART1 (PA9/PA10) connected to STLINK-V3E VCP**
SB31, SB33 ON SB25 SB27 SB32 SB34 OFF	USART1 (PA9/PA10) connected to Zio, ARDUINO® Uno V3 D0/D1

1. *The default configuration is in bold.*

Table 11. LPUART1 connection

Solder bridge configuration(1)	Feature
SB25, SB27 ON **SB24 SB26 SB31 SB33 OFF**	**LPUART1 (PG7/PG8) connected to Zio, ARDUINO® Uno V3 D0/D1**
SB24, SB26 ON SB25 SB27 SB32 SB34 OFF	LPUART1 (PG7/PG8) connected to STLINK-V3E VCP.

1. *The default configuration is in bold.*

By default:

- Communication between target MCU and ST-LINK MCU is enabled on USART1 because this interface supports the bootloader mode.
- Communication between target MCU, ARDUINO® Uno V3, and ST morpho connectors is enabled on LPUART1, not to interfere with the VCP interface.

PG7 and PG8 are also connected to the ST morpho connector CN12 pins 66 (SB72) and 67 (SB73). The two solder bridges can be removed in case of conflict between ARDUINO® Uno V3 and ST morpho for PG7 or PG8.

6.10 Bootloader

The bootloader is located in the system memory, programmed by ST during production. It is used to reprogram the flash memory via USART, I^2C, SPI, CAN FD, or USB FS in device mode through the device firmware upgrade (DFU). The bootloader is available on all devices. Refer to the application note *STM32 microcontroller system memory boot mode* (AN2606) for more details.

The Root Secure Services (RSS) are embedded in a flash area named secure information block, programmed during ST production. For example, it enables secure firmware installation (SFI), thanks to the RSS extension firmware (RSSe SFI). This feature allows customers to protect the confidentiality of the firmware to be provisioned into the STM32 when production is sub-contracted to an untrusted third party. The RSS is available on all devices, after enabling the TrustZone® through the TZEN option bit.

The I/O PH3_BOOT0 gives external hardware access to the bootloader.

By default, this pin is set to level LOW by a pull-down resistor. It is possible to put this I/O to level HIGH by connecting a 2.54 mm pitch jumper between the Zio connector CN11 pin 7 and VDD pin 5.

As mentioned above, USART1 on PA9/PA10 is connected by default because this interface supports the bootloader mode.

6.11 USB Type-C® FS

The STM32 Nucleo-144 board supports USB full-speed (FS) communication. The USB connector (CN15) is a USB Type-C® connector.

The STM32 Nucleo-144 board supports USB Type-C® sink power mode only.

The LD7 green LED lights up when V_{BUS} is powered by a USB host.

6.11.1 USB FS device

With a USB stack inside the STM32 and when a USB host connection to the USB Type-C® connector (CN15) of STM32 Nucleo-144 is detected, the STM32 Nucleo-144 board can be a USB device. Depending on the powering capability of the USB host, the board can take power from the CN15 V_{BUS} terminal. In the board schematic diagrams, the corresponding power voltage line is called 5V_UCPD. The STM32 Nucleo-144 board supports a 5 V USB voltage from 4.75 to 5.25 V. MCU VDD_USB supports the 3V3 voltage only. Section 6.4 provides information on how to use the powering options. The hardware configuration for the USB FS interface is shown in Table 12. Hardware configuration for the USB interface.

Table 12. Hardware configuration for the USB interface

I/O	Solder bridge	Setting	Configuration(1)
PA11	SB40	**OFF**	**PA11 used as USB_FS_N diff pair interface** **No other muxing**
		ON	PA11 can be used as an I/O on the ST morpho connector. USB function can be used, but performances are low due to the track length to the Zio connector causing impedance mismatch.
PA12	SB41	**OFF**	**PA12 used as USB_FS_P diff pair interface** **No other muxing**
		ON	PA12 can be used as an I/O on the ST morpho connector. USB function can be used, but performances are low due to the track length to the Zio connector causing impedance mismatch.

1. *The default configuration is shown in bold.*

6.11.2 UCPD

The USB Type-C® introduces the USB Power Delivery feature. The STM32 Nucleo-144 supports the dead battery and the sink mode.

In addition to the I/O DP/DM directly connected to the USB Type-C® connector, five I/Os are also used for UCPD configuration: configuration channel (CCx), VBUS-SENSE, UCPD dead battery (DBn), and UCPD_FAULT (FLT) feature.

To protect the STM32 Nucleo-144 from USB over-voltage, a PPS-compliant USB Type-C® port protection is used: TCPP01-M12 IEC6100-4-2 level 4-compliant IC.

- Configuration Channel I/O: UCPD_CCx: These signals are connected to the associated CCx line of the USB Type-C® connector through the STM USB port Protection TCPP01-M12. These lines are used for the configuration channel lines (CCx) to select the USB Type-C® current mode. The STM32 Nucleo-144 supports only sink current mode.
- Dead Battery I/O: UCPD_DBn: This signal is connected to the associated DBn line of the TCPP01-M12. The STM USB port protection TCPP01-M12 internally manages the dead battery resistors.
- V_{BUS} fault detection: UCPD_FLT: This signal is provided by the ST USB Type-C® port protection. It is used as fault reporting to MCU after a bad V_{BUS} level detection. By design, the STM32 Nucleo-144 V_{BUS} protection is set to 6 V maximum. (R41 is set to 2K7 to select 6 V maximum). For more detail about this implementation, refer to the STM TCPP01-M12 datasheet.

Table 13 describes the hardware configuration for the UCPD feature.

Table 13. Hardware configuration for the UCPD feature

I/O	Solder bridge	Setting	Configuration(1)
PA15	SB42	OFF	PA15 Not connected to USB Type-C® port protection and used as T_JTDI (optional configuration with SB39)
		ON	**PA15 connected to USB Type-C® port protection and NOT used as T_JTDI**
	SB8	**OFF**	**PA15 connected to USB Type-C® port protection and used as UCPD_CC1**
		ON	PA15 directly connected to USB Type-C® connector. USB Type-C® port protection is bypassed.
PB15	SB9	**OFF**	**PB15 connected to USB Type-C® port protection and used as UCPD_CC2**
		ON	PB15 directly connected to USB Type-C® connector. USB Type-C® port protection is bypassed.
PC2	SB6	**ON**	**PC2 used as VBUS_SENSE**
		OFF	PC2 NOT used for UCPD. Can be used on Zio connector (SB53)
PB5	SB46	**ON**	**IO UCPD_DBn connected to USB Type-C® port protection and used as a dead battery feature**
		OFF	PB5 not used for UCPD_DBn can be used as SAI or SPI on ZIO connector
	JP8	ON	UCPD_DBCC1 connected to GND (only for internal UCPD debug purpose)
		OFF	**UCPD_DBCC1 not connected to GND, can be used for Zio connector**
PB14	SB45	**ON**	**IO UCPD_FLT connected to USB Type-C® port protection and used as over-voltage fault reporting to MCU**
		OFF	PB14 not used for UCPD_FLT can be used on the ST morpho connector
	JP7	ON	UCPD_DBCC2 connected to GND (only for internal UCPD debug purpose)
		OFF	**UCPD_DBCC2 not connected to GND, can be used for the ST morpho connector**

1. *The default configuration is shown in bold*

6.11.3 USB Type-C® connector

Figure 15 shows the pinout of the USB Type-C® connector CN15.

Figure 15. USB Type-C® connector (CN15) pinout

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	CC1	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
GND	RX1+	RX1-	VBUS	SBU2	D-	D+	CC2	VBUS	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Table 14 describes the pinout of the USB Type-C® connector (CN15).

Table 14. USB Type-C® connector (CN15) pinout

STM32 pin	Signal name	Pin name	Pin	Pin	Pin name	Signal name	STM32 pin
-	GND	GND	A1	B12	GND	GND	-
-	-	TX1+	A2	B11	RX1+	-	-
-	-	TX1-	A3	B10	RX1-	-	-
-	VBUS_C/ 5V_USB_C	VBUS	A4	B9	VBUS	VBUS_C/ 5V_USB_C	-
PA15	UCPD_CC1	CC1	A5	B8	SBU2	-	-
PA12	USB_FS_P	D+	A6	B7	D-	USB_FS_N	PA11
PA11	USB_FS_N	D-	A7	B6	D+	USB_FS_P	PA12
-	-	SBU1	A8	B5	CC2	UCPD_CC2	PB15
-	VBUS_C/ 5V_USB_C	VBUS	A9	B4	VBUS	VBUS_C/ 5V_USB_C	-
-	-	RX2-	A10	B3	TX2-	-	-
-	-	RX2+	A11	B2	TX2+	-	-
-	GND	GND	A12	B1	GND	GND	-

7 Extension connectors

Six extension connectors are implemented on the STM32U5 Nucleo-144 board:

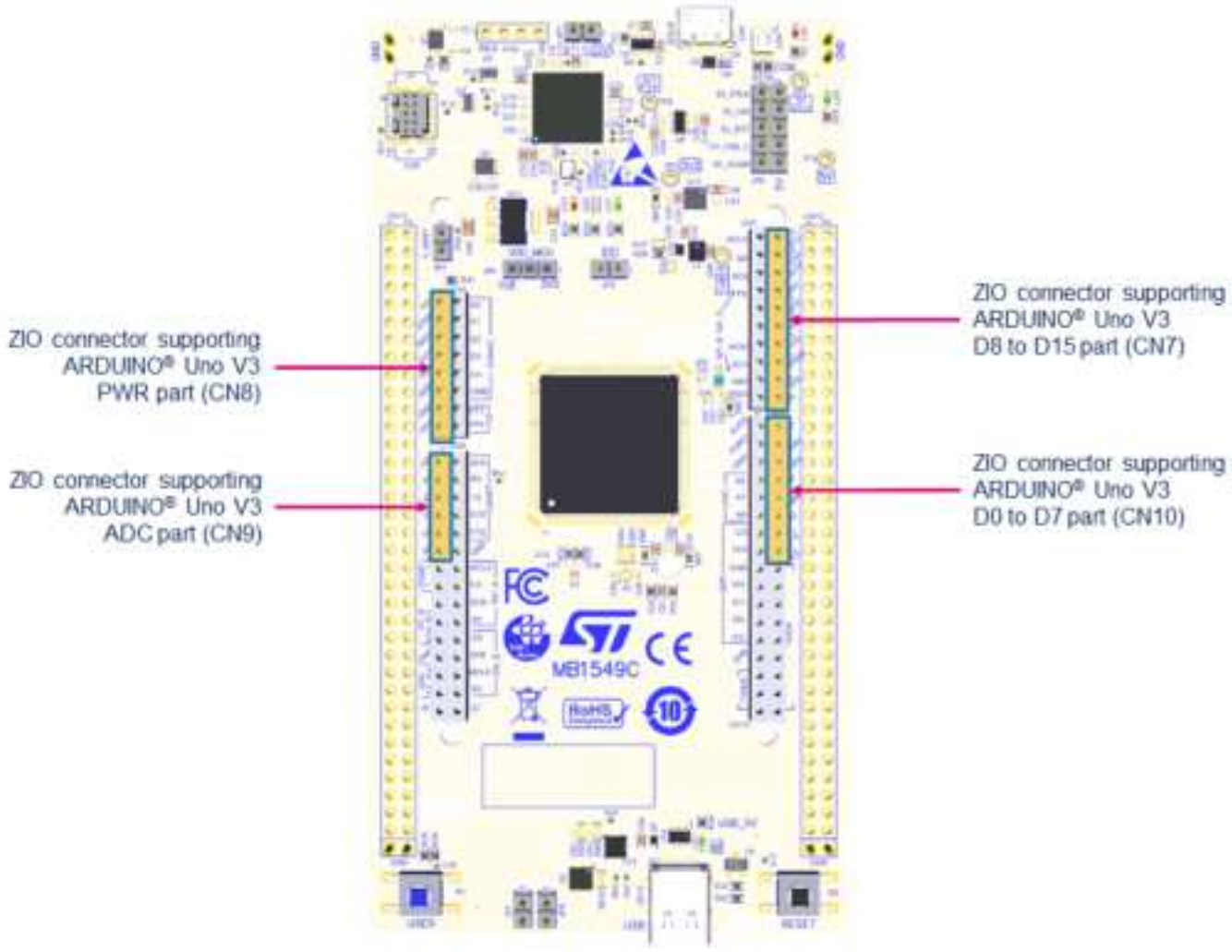
- Zio connectors (CN7, CN8, CN9, and CN10) supporting ARDUINO® Uno V3
- ST morpho connectors (CN11 and CN12)

7.1 Zio connectors supporting ARDUINO® Uno V3

The Zio connectors (CN7, CN8, CN9, and CN10) are female connectors supporting the ARDUINO® Uno V3 standard. Most shields designed for ARDUINO® can fit the Nucleo board.

Caution: Most of the STM32 microcontroller I/Os are 5 V-tolerant, but few of them are only 3V3-compatible, while ARDUINO® Uno V3 is 5 V-compatible. Refer to the STM32U5 Series data brief and STM32U5xx product datasheets for their I/O structure.

Figure 16. Zio connectors supporting ARDUINO® Uno V3



The related pinout for the ARDUINO® connector is listed in Table 15, Table 16, Table 17, and Table 18.

Table 15. ARDUINO®-included Zio connector (CN7) pinout

MCU function	STM32 pin	Signal name	Pin name	Pin	Pin	Pin name	Signal name	STM32 pin	MCU function
SAI2_A	PC6	SAI_C_MCLK	D16	1	2	D15	I2C_A_SCL	PB8	I2C1
SAI2_A	PD11	SAI_C_SD	D17	3	4	D14	I2C_A_SDA	PB9	I2C1
SAI2_A	PB13	SAI_C_SCK	D18	5	6	VREFP	-	-	-
SAI2_A	PD12	SAI_C_FS	D19	7	8	GND	-	-	-
SAI1_B/ SPI3	PA4	SAI_D_FS	D20(7)	9	10	D13	SPI_A_SCK	PA5	SPI1
SAI1_B/ SPI3	PB4	SAI_D_MCLK	D21 (7)(8)	11	12	D12	SPI_A_MISO	PA6	SPI1
SAI1_B/ SPI3	PB5	SAI_D_SD/ SPI_B_MOSI	D22 (5)(7)(8)	13	14	D11	SPI_A_MOSI / TIM_E_PWM1	PA7	SPI1
SAI1_B/ SPI3	PB3	SAI_D_SCK/ SPI_B_SCK	D23(6) (7)(8)	15	16	D10	SPI_A_CS / TIM_B_PWM3	PD14	SPI1/ TIM4_CH3
SAI1/SPI3	PA4	SPI_B_NSS	D24 (8)	17	18	D9	TIM_B_PWM2	PD15	TIM4_CH4
SAI1/SPI3	PB4	SPI_B_MISO	D25 (8)	19	20	D8	IO	PF12	-

A solder bridge (SB20) is used to disconnect the VREFP to the ARDUINO® connector CN7 pin 6.

- SB20 OFF: VREFP is not connected to the ARDUINO® connector CN7 pin 6 (Default configuration).
- SB20 ON: VREFP is connected to the ARDUINO® connector CN7 pin 6.

Table 16. ARDUINO®-included Zio connector (CN8) pinout

ARDUINO® function	Pin name	Signal name	STM32 pin	ARDUINO® function	Pin	Pin name	Signal name	STM32 pin	MCU function
RES	-	NC	NC	1	2	D43	SDMMC_D0	PC8	SDMMC1
IO REF	-	IOREF	IOREF	3	4	D44	SDMMC_D1	PC9	SDMMC1
RESET	NRST	NRST	NRST	5	6	D45	SDMMC_D2	PC10	SDMMC1
3V3 I/O	-	3V3	3V3	7	8	D46	SDMMC_D3	PC11	SDMMC1
5V output	-	5V	5V	9	10	D47	SDMMC_CK	PC12	SDMMC1
GND	-	GND	GND	11	12	D48	SDMMC_CMD	PD2	SDMMC1
GND	-	GND	GND	13	14	D49	IO	PF3	-
VIN	-	VIN	VIN	15	16	D50	IO	PF5	-

Table 17. ARDUINO®-included Zio connector (CN9) pinout

MCU function	STM32 pin	Signal name	Pin name	Pin	Pin	Pin name	Signal name	STM32 pin	MCU function
ADC1_IN8	PA3	ADC	A0	1	2	D51	USART_B_SCLK	PD7	USART2
ADC1_IN7	PA2	ADC	A1(3)	3	4	D52	USART_B_RX	PD6	USART2
ADC1_IN4	PC3	ADC	A2	5	6	D53	USART_B_TX	PD5	USART2
ADC1_IN15	PB0	ADC	A3(3)	7	8	D54	USART_B_RTS	PD4	USART2
ADC1_IN2	PC1	ADC	A4	9	10	D55	USART_B_CTS	PD3	USART2
ADC1_IN1	PC0	ADC	A5	11	12	GND	-	-	-
COMP1	PB2	COMP1_INP	D72	13	14	D56	SAI_A_MCLK	PE2	SAI1_A
COMP2	PB6	COMP2_INP	D71	15	16	D57	SAI_A_FS	PE4	SAI1_A
I2C2	PF2	I2C_B_SMBA	D70	17	18	D58	SAI_A_SCK	PE5	SAI1_A
I2C2	PF1	I2C_B_SCL	D69	19	20	D59	SAI_A_SD	PE6	SAI1_A
I2C2	PF0	I2C_B_SDA	D68	21	22	D60 (7)	SAI_B_SD	PE3	SAI1_B
-	-	-	GND	23	24	D61 (7)	SAI_B_SCK	PF8	SAI1_B
CAN1	PD0	CAN_RX	D67	25	26	D62 (7)	SAI_B_MCLK	PF7	SAI1_B
CAN1	PD1	CAN_TX	D66	27	28	D63 (7)	SAI_B_FS	PF9	SAI1_B
-	PG0	IO	D65	29	30	D64	IO	PG1	-

Table 18. ARDUINO®-included Zio connector (CN10) pinout

MCU function	STM32 pin	Signal name	Pin name	Pin	Pin	Pin name	Signal name	STM32 pin	MCU function
AVDD	-	-	AVDD	1	2	D7	IO	PF13	IO
AGND	-	-	AGND	3	4	D6	TIM_A_PWM1	PE9	TIM1_CH1
GND	-	-	GND	5	6	D5	TIM_A_PWM2	PE11	TIM1_CH2
ADC1_IN16	PB1	ADC_A_IN	A6	7	8	D4	IO	PF14	IO
ADC1_IN3	PC2	ADC_B_IN	A7	9	10	D3	TIM_A_PWM3	PE13	TIM1_CH3
ADC1_IN6	PA1	ADC_C_IN	A8	11	12	D2	IO	PF15	IO
OCTOSPI1	PA2	OCTOSPI_CS	D26(3)	13	14	D1(1)	USART_A_TX	PG7(2)	LPUART1
OCTOSPI1	PB10	OCTOSPI_CLK	D27(4)	15	16	D0(1)	USART_A_RX	PG8(2)	LPUART1
-	-	-	GND	17	18	D42	TIM_A_PWM1N	PE8	TIM1_CH1N
OCTOSPI1	PE15	OCTOSPI_IO3	D28(4)	19	20	D41	TIM_A_ETR	PE7	TIM1_ETR
OCTOSPI1	PB0	OCTOSPI_IO1	D29(3)	21	22	GND	-	-	-
OCTOSPI1	PE12	OCTOSPI_IO0	D30(4)	23	24	D40	TIM_A_PWM2N	PE10	TIM1_CH2N
OCTOSPI1	PE14	OCTOSPI_IO2	D31(4)	25	26	D39(4)	TIM_A_PWM3N	PE12	TIM1_CH3N
-	-	-	GND	27	28	D38(4)	TIM_A_BKIN2	PE14	TIM1_BKIN2
TIM2_CH1	PA0	TIM_C_PWM1	D32	29	30	D37(4)	TIM_A_BKIN1	PE15	TIM1_BKIN
TIM1_CH1	PA8	TIM_D_PWM1	D33	31	32	D36(4)	TIM_C_PWM2	PB10	TIM2_CH3
TIM4_ETR	PE0	TIM_B_ETR	D34	33	34	D35	TIM_C_PWM3	PB11	TIM2_CH4

1. *The default configuration for the D0/D1 signal is LPUART1 on PG7 and PG8, USART1 on PA9 and PA10 is connected by default on STLINK-V3E.*
2. *PG2 to PG15 can have a different I/O level to other I/Os because supplied by VDDIO.*

3. *I/O shared between ADC and OCTOSPI (exclusive)*
4. *I/O shared between OCTOSPI and motor control (exclusive)*
5. *I/O shared between SAI_D, SPI_B, and UCPD function (exclusive)*
6. *I/Os are shared between SAI and JTAG SWO (exclusive)*
7. *SAI_D and SAI_B groups are on the same SAI instance (exclusive).*
8. *SAI_D group is shared with SPI_B group, (exclusive).*

Note: The OCTOSPI interface is used in quad mode communication without DQS to support Quad-SPI memories.

7.2 ST morpho headers (CN11 and CN12)

The ST morpho consists of CN11 and CN12 male pin header footprints (not soldered by default). They can be used to connect the STM32 Nucleo-144 board to an extension board or a prototype/wrapping board placed on top of the STM32 Nucleo-144 board. All signals and power pins of the STM32 are available on the ST morpho connector. An oscilloscope, a logic analyzer, or a voltmeter can also probe this connector.

Figure 17. ST morpho connector

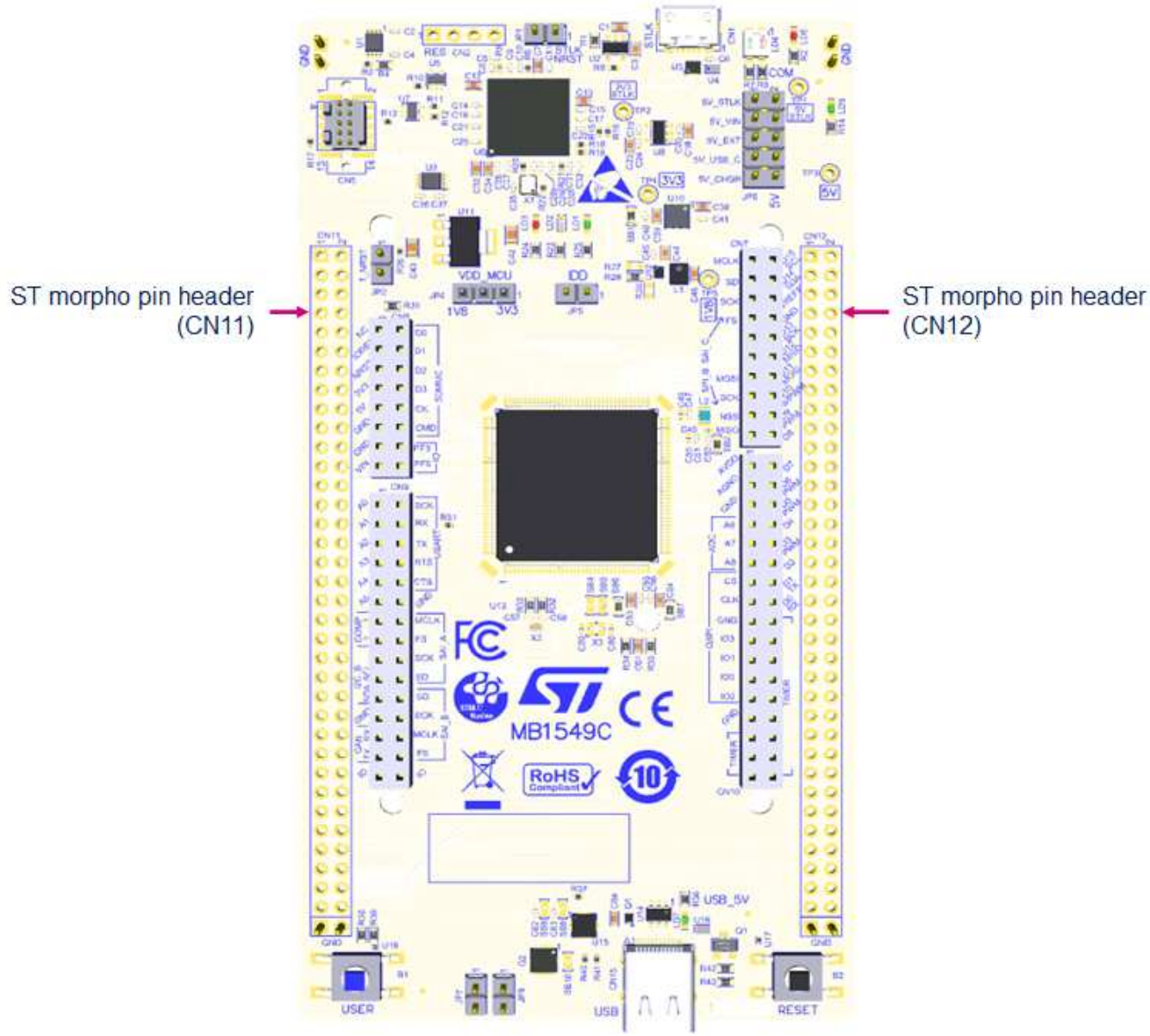


Table 19 shows the pin assignments for the STM32 on the ST morpho connector.

Table 19. ST morpho connector pin assignment

CN11 odd pins		CN11 even pins		CN12 odd pins		CN12 even pins	
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	PC10	2	PC11	1	PC9	2	PC8
3	PC12	4	PD2	3	PB8	4	PC6
5	VDD	6	5V_EXT	5	PB9	6	NC
7	PH3_BOOT0(1)	8	GND	7	VREFP(2)	8	5V_STLK(3)
9	PF6	10	NC	9	GND	10	PD8
11	PF7	12	IOREF	11	PA5	12	PA12
13	PA13(4)	14	NRST	13	PA6	14	PA11
15	PA14(4)	16	3V3	15	PA7	16	NC
17	PA15	18	5V	17	PB6	18	PB11
19	GND	20	GND	19	PC7	20	GND
21	PB7	22	GND	21	PA9	22	PB2
23	PC13	24	VIN	23	PA8	24	PB1
25	PC14	26	NC	25	PB10	26	PB15
27	PC15	28	PA0	27	PB4	28	PB14
29	PH0	30	PA1	29	PB5	30	PB13
31	PH1	32	PA4	31	PB3	32	AGND
33	VBAT	34	PB0	33	PA10	34	NC
35	PC2	36	PC1	35	PA2	36	PF5
37	PC3	38	PC0	37	PA3	38	PF4
39	PD4	40	PD3	39	GND	40	PE8
41	PD5	42	PG2(5)	41	PD13	42	PF10
43	PD6	44	PG3(5)	43	PD12	44	PE7
45	PD7	46	PE2	45	PD11	46	PD14
47	PE3	48	PE4	47	PE10	48	PD15
49	GND	50	PE5	49	PE12	50	PF14
51	PF1	52	PF2	51	PE14	52	PE9
53	PF0	54	PF8	53	PE15	54	GND
55	PD1	56	PF9	55	PE13	56	PE11
57	PD0	58	PG1	57	PF13	58	PF3
59	PG0	60	GND	59	PF12	60	PF15
61	PE1	62	PE6	61	PG14(5)	62	PF11
63	PG9(5)	64	PG15(5)	63	GND	64	PE0
65	PG12(5)	66	PG10(5)	65	PD10	66	PG8(5)
67	NC	68	PG13(5)	67	PG7(5)	68	PG5(5)
69	PD9	70	NC	69	PG4(5)	70	PG6(5)

1. *The default state of BOOT0 is 0. It can be set to 1 when a jumper is plugged on the pins 5-7 of CN11.*
2. *V_{REFP} is not connected to CN12 by default (SB20 OFF).*
3. *5V_STLK is the 5V power signal, coming from the STLINK-V3E USB connector. It rises before the 5V signal of the board.*
4. *PA13 and PA14 are shared with SWD signals connected to STLINK-V3E.*
5. *PG2 to PG15 can be set to different I/O levels, thanks to the SB to select the source for VDDIO2.*

7.3 Solder bridge configuration for the expansion connector

Table 20 details the solder bridges of the STM32U5 Nucleo-144 board for the expansion connector.

Table 20. Solder bridge configuration

Definition	Bridge	Setting(1)	Comment
IOREF selection	SB16	**OFF**	**IOREF not connected to 1V8 power supply**
		ON	IOREF connected to 1V8 power supply
	SB17	OFF	IOREF not connected to VDD power supply
		ON	**IOREF connected to VDD power supply**
	SB18	**OFF**	**IOREF not connected to 3V3 power supply**
		ON	IOREF connected to 3V3 power supply
SDMMC IO PC8/PC9	SB19	OFF	PC8 not connected to ST morpho CN12 pin 2 to avoid stub on Zio CN8 SDMMC_D0
		ON	**PC8 connected to ST morpho CN12 pin 2 and Zio CN8 pin 2: SDMMC_D0 signal quality can be impacted**
	SB22	OFF	PC9 not connected to ST morpho CN12 pin 1 to avoid stub on Zio CN8 SDMMC_D1
		ON	**PC9 connected to ST morpho CN12 pin 1 and Zio CN8 pin 4. SDMMC_D1 signal quality can be impacted**
ADC-A3 / OCTOSPI_IO1 PB0	SB63	OFF	PB0 not used as OCTOSPI_IO1
		ON	**PB0 used as OCTOSPI_IO1**
	SB64	OFF	PB0 not connected to ARDUINO® A3
		ON	**PB0 connected to ARDUINO® A3**
	SB65	OFF	PB0 not connected to ST morpho pin 34
		ON	**PB0 connected to ST morpho pin 34**
ADC_A1 / OCTOSPI_CS PA2	SB56	OFF	PA2 not connected to Zio OCTOSPI_CS
		ON	**PA2 connected to Zio OCTOSPI_CS**
	SB57	OFF	PA2 not connected to ARDUINO® A1
		ON	**PA2 connected to ARDUINO® A1**
ADC-A7 / VBUS_SENSE PC2	SB53	OFF	PC2 not connected to ADC_A7 on Zio connector and used as USB Type-C® VBUS_SENSE (SB6)
		ON	**PC2 connected to ADC_A7 on Zio connector**
Zio SAI_D / SPI_B interface	SB35	OFF	PA4 not connected to Zio CN7 pin 9 for SAI_D interface
		ON	**PA4 connected to Zio CN7 pin 9 for SAI_D interface**
	SB38	OFF	PA4 not connected to Zio CN7 pin 17 for SPI_B interface
		ON	**PA4 connected to Zio CN7 pin 17 for SPI_B interface**
	SB36	OFF	PB4 not connected to Zio (CN7) for SAI_D interface
		ON	**PB4 connected to Zio (CN7) for SAI_D interface**
	SB43	OFF	PB4 not connected to Zio (CN7) for SPI_B interface
		ON	**PB4 connected to Zio (CN7) for SPI_B interface**
	SB37	OFF	PB5 not connected to Zio (CN7) for SPI_B interface: Reserved for UCPD_DBCC1
		ON	**PB5 connected to Zio (CN7) for SPI_B interface, shared with for UCPD_DBn and UCPB_DBCC1**

Definition	Bridge	Setting(1)	Comment
OCTOSPI_CLK / TIMER_C_PWM2 PB10	SB61	OFF	PB10 not used as OCTOSPI_CLK
		ON	**PB10 used as OCTOSPI_CLK**
	SB62	OFF	PB10 not used as TIMER for motor control
		ON	**PB10 used as TIMER for motor control**
TIMER_C_PWM1 / User-Button PA0	SB60	OFF	PA0 not used as TIMER for motor control, reserved for user button
		ON	**PA0 can be used as TIMER for motor control, can't be used as user button**
OCTOSPI_IO3 / TIMER_A_BKIN1 PE15	SB66	OFF	PE15 not used as OCTOSPI_IO3
		ON	**PE15 used as OCTOSPI_IO3**
	SB67	OFF	PE15 not used as TIMER for motor control
		ON	**PE15 used as TIMER for motor control**
OCTOSPI_IO0 / TIMER_A_PWM3N PE12	SB68	OFF	PE12 not used as OCTOSPI_IO0
		ON	**PE12 used as OCTOSPI_IO0**
	SB69	OFF	PE12 not used as TIMER for motor control
		ON	**PE12 used as TIMER for motor control**
OCTOSPI_IO2 / TIMER_A_BKIN2 PE14	SB70	OFF	PE14 not used as OCTOSPI_IO2
		ON	**PE14 used as OCTOSPI_IO2**
	SB71	OFF	PE14 not used as TIMER for motor control
		ON	**PE14 used as TIMER for motor control**

1. *The default configuration is in bold.*

Note: The OCTOSPI interface is used in quad mode communication without DQS to support Quad-SPI memories.

8 NUCLEO-U575ZI-Q board information

8.1 Product marking

Evaluation tools marked as “ES” or “E” are not yet qualified and therefore not ready to be used as reference design or in production. Any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering sample tools as reference designs or in production.

“E” or “ES” marking examples of location:

- On the targeted STM32 that is soldered on the board (For an illustration of STM32 marking, refer to the STM32 datasheet “Package information” paragraph at the *www.st.com* website).
- Next to the evaluation tool ordering part number that is stuck or silk-screen printed on the board.

Some boards feature a specific STM32 device version, which allows the operation of any bundled commercial stack/library available. This STM32 device shows a "U" marking option at the end of the standard part number and is not available for sales.

To use the same commercial stack in their applications, the developers may need to purchase a part number specific to this stack/library. The price of those part numbers includes the stack/library royalties.

8.2 NUCLEO-U575ZI-Q product history

There is one generic identification associated with the Nucleo for STM32U5, PCB MB1549:

- NUU575ZIQ$xxx for products without socket and with MCU soldered

8.2.1 Product identification NUU575ZIQ$AT1

This product identification is based on the NUCLEO-U575ZI-Q revision C02.

It embeds the STM32U575ZIT6Q microcontroller with revision code "X". The limitations of this revision are detailed in the errata sheet *STM32U575xx and STM32585xx device errata* (ES0499).

8.2.2 Product identification NUU575ZIQ$AT2

This product identification is based on the NUCLEO-U575ZI-Q revision C03.

It embeds the STM32U575ZIT6Q microcontroller with revision code "X". The limitations of this revision are detailed in the errata sheet *STM32U575xx and STM32585xx device errata* (ES0499).

The bootloader revision embedded on this STM32U575ZIT6Q integrates the correction for the bootloader communication interfaces when TZEN=1.

8.3 NUCLEO-U575ZI-Q product limitations

8.3.1 Product identification NUU575ZIQ$AT1 limitations

Bootloader communication interfaces are not available if TZEN=1.

When TrustZone® is enabled and boot from system memory is selected (BOOT0 = 1) to use the bootloader, the ST embedded bootloader is blocked, thus making all the bootloader interfaces no more usable (USB-DFU, USART, SPI, I^2C, and CAN FD). As a consequence, the SFI (secure firmware install) using bootloader communication interfaces does not work, and the option bytes cannot be changed using the bootloader interface. SFI and option bytes change using JTAG/SWD interface remains functional.

There is no workaround to this limitation solved in product identification NUU575ZIQ$AT2.

8.3.2 Product identification NUU575ZIQ$AT2 limitations

No limitation identified for this product identification.

8.4 Board revision history

8.4.1 Board MB1549-C02

The revision C02 of the MB1549 board is the first official version.

8.4.2 Board MB1549-C03

The revision C03 of the MB1549 board is the second official version.

BOM improvement:

- Update C57 and C58 capacitors from 4.7 pF to 1.8 pF for 32 KHz CLOAD adaptation.
- Include STM32U575ZIT6Q with new embedded RSS.

8.5 Board known limitations

8.5.1 Board MB1549-C02 limitations

SWDIO: For the level shifter to support 1V8 MCU debug, it is recommended to set the SWDIO frequency to 8 MHz.

8.5.2 Board MB1549-C03 limitations

SWDIO: For the level shifter to support 1V8 MCU debug, it is recommended to set the SWDIO frequency to 8 MHz.

9 Federal Communications Commission (FCC) and Innovation, Science and Economic Development Canada (ISED) Compliance Statements

9.1 FCC Compliance Statement

Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

Part 15.105

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception which can be determined by turning the equipment off and on, the user is encouraged to try to correct interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Note: Use only shielded cables.

Responsible party (in the USA)

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9.2 ISED Compliance Statement

ISED Canada ICES-003 Compliance Label: *CAN ICES-3 (B) / NMB-3 (B)*.

Étiquette de conformité à la NMB-003 d'ISDE Canada: *CAN ICES-3 (B) / NMB-3 (B)*.

10 CE conformity

10.1 Warning

EN 55032 / CISPR32 (2012) Class B product

Warning: this device is compliant with Class B of EN55032 / CISPR32. In a residential environment, this equipment may cause radio interference.

Avertissement : cet équipement est conforme à la Classe B de la EN55032 / CISPR 32. Dans un environnement résidentiel, cet équipement peut créer des interférences radio.

Revision history

Table 21. **Document revision history**

Date	Version	Changes
24-Jun-2021	1	Initial release.
13-Sep-2021	2	Added *Product limitation* to *Product identification NUU575ZIQ$AT1* and *Product identification NUU575ZIQ$AT2* solving this limitation.
13-Apr-2022	3	Added Board MB1549-C03. Updated Table 18 and Table 20 for OCTOSPI interface.

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