eXecute-In-Place (XIP) with Serial Flash Memories on MPUs Using MPLAB Harmony V3

AN5218

Introduction

This document describes the eXecute-In-Place (XIP) from serial Flash memory feature on MPUs and discusses the implementation of an application using the MPLAB® Harmony v3 software framework. It explains how to generate an application binary to execute in the serial Flash memory region, and it also shows how to execute an application from the serial Flash. The purpose of this feature is to provide an option to run a DDR-less system on MPUs.

The example provided in this application note comprises the six main steps listed below. These steps are detailed in 3. Serial Flash XIP Example Using MPLAB Harmony v3:

1. SAM-BA installation on Windows host
2. Device setup to Flash using SAM-BA
3. Configure the first stage bootloader(ROMBOOT) to boot from the serial Flash memory
4. Configure the second stage bootloader(at91bootstrap) to enable XIP
5. Modification required to execute a Harmony application from QSPI
6. Debug an application on MPLAB or run an application executed from serial Flash

1. Hardware and Software Requirements

1.1 MPU Evaluation Kit

The procedure enumerated by this document is applicable to an MPU that supports XIP from serial Flash memory. The detailed steps shown here apply to SAM9X60-EK and SAMA7G54-EK evaluation kits that feature serial Flash memory on the boards.

1.1.1 SAMA7G54-EK Evaluation Kit (EV21H18A)

The SAMA7G54-EK Evaluation Kit is a development kit for evaluating the SAMA7G5 microprocessor (MPU). The SAMA7G5 is based on the Cortex®-A7 and is capable of running at 1 GHz. The evaluation kit includes an on-board embedded debugger. The SAMA7G54-EK board has Macronix Octa SPI flash MX66LM1G45GXDI00.

The SAMA7G54-EK Evaluation Kit is available at Microchip Direct.

1.1.2 SAM9X60-EK Evaluation Kit (DT100126)

The SAM9X60-EK Evaluation Kit is a development kit for evaluating the SAM9X60 microprocessor (MPU). The SAM9X60 is based on the Arm® ARM926EJ-S™ and is capable of running at 600 MHz. The evaluation kit includes an on-board embedded debugger. The SAM9X60-EK board features the Microchip QSPI module SST26VF064B.

Details of the SAM9X60-EK Evaluation Kit are available on the Microchip Website.

1.2 Windows® Host System

The eXecute-in-Place Harmony application described in this application note is tested and verified on a Windows host PC.

1.3 MPLAB X Integrated Development Environment (IDE) and MPLAB XC32 C/C++ Compiler

MPLAB X IDE is an expandable, highly configurable software program that incorporates powerful tools to help users to discover, configure, develop, debug, and qualify embedded designs for most Microchip microprocessors.

The IDE is available at the Microchip Website. This document uses MPLAB X IDE version 6.15.

The compiler is available at the Microchip Website. This document uses MPLAB XC32 version 4.35.

1.4 MPLAB Harmony v3

MPLAB Harmony v3 is a fully-integrated embedded software development framework that provides flexible and interoperable software modules that enable the user to dedicate resources to create applications for 32-bit MPUs, rather than dealing with device details, complex protocols, and library integration challenges. The Harmony framework includes MPLAB Code Configurator (MCC) , an easy-to-use development tool with a Graphical User Interface (GUI) that simplifies device set-up, library selection, configuration, and application development. MCC is available as a plug-in that directly integrates with MPLAB X IDE.

1.5 SAM-BA® In System Programmer

SAM-BA software provides an open set of tools for in-system programming of internal and external memories connected to Microchip MPUs. Devices can be programmed through the JTAG, debug UART or USB interfaces. With the SAM-BA monitor residing in on-chip non-volatile memory, SAM-BA can be used to re-program the MPU without connecting to the debugger. If using the secure boot feature of Microchip MPUs, the Secure SAM-BA edition, available under NDA, must be used.

Note: Links to download the software are given in 6. References.

2. XIP on Serial Flash Memory

The Quad Serial Peripheral Interface (QSPI) is configured to Serial Memory mode for XIP program execution. In a system that maps external Flash memory, such as ROM, SRAM, DRAM, etc., this mode allows code execution directly from Flash memory without code shadowing to RAM.

2.1 QSPI Serial Memory Mode

In Serial Memory mode, the QSPI acts as a serial Flash memory controller. The QSPI can be used to read data from the serial Flash memory, allowing the CPU to execute code from it (XIP). The QSPI can also be used to control the serial Flash memory (Program, Erase, Lock, etc.) by sending specific commands.

In this mode, the QSPI is compatible with single-bit SPI, Dual SPI, Quad and Octal SPI protocols. Refer to the device data sheet to confirm support.

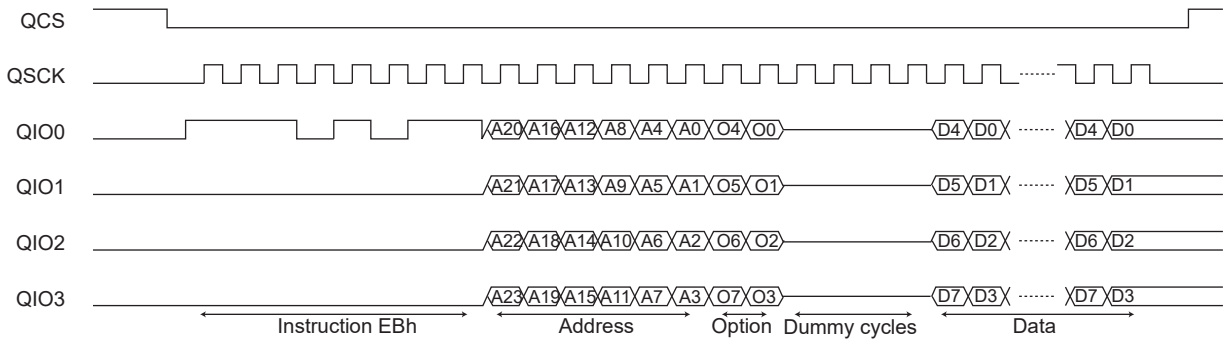
To activate this mode, QSPI_MR.SMM must be written to '1'. In Serial Memory mode, data is transferred either by QSPI_TDR and QSPI_RDR, or by writing or reading in the QSPI memory space depending on the configuration of QSPI_IFR.TFRTYP and QSPI_IFR.SMRM.

2.1.1 Instruction Frame

In order to control serial Flash memories, the QSPI sends instructions via the SPI bus (READ, PROGRAM, ERASE, LOCK, etc.). Because the instruction set implemented in serial Flash memories is memory-vendor dependent, the QSPI includes a complete Instruction Frame register (QSPI_IFR) to ensure compatibility with all serial Flash memories.

An instruction frame includes:

- (Optional) An instruction code (see Continuous Read Mode in the corresponding data sheet).
- An address (size: 8, 16, 24 or 32 bits). The address is optional but is required by instructions such as READ, PROGRAM, ERASE, LOCK. By default, the address is 8 bits long, but can be increased up to 32 bits to support serial Flash memories larger than 128 Mbits.
- An option code (size: 1/2/4/8 bits). The option code is used to activate the XIP mode or the Continuous Read mode (see Continuous Read Mode) for READ instructions, in some serial Flash memory devices. These modes improve the data read latency.
- Dummy cycles. Dummy cycles are optional but required by some READ instructions.
- Data bytes are optional. Data bytes are present for data transfer instructions such as READ or PROGRAM. The instruction code, the address/option and the data can be sent with Single-bit SPI, Dual SPI, or Quad SPI protocols.



2.1.2 Read Memory Transfer

The data of the serial memory is accessed by sending an instruction with QSPI_IFR.DATAEN = 1 and QSPI_IFR.TFRTYP = 1. In this mode, the QSPI is able to read data at random address into the serial Flash memory, allowing the CPU to execute code directly from it (XIP). In order to fetch data, the

user must first configure the instruction frame by writing the QSPI_IFR. Then data can be read at any address in the QSPI address space mapping. The address of the system bus read accesses matches the address of the data inside the serial Flash memory.

In Serial Memory mode, QSPI is compatible with four protocols:

- Single-Bit SPI: Communicate with external memory with QIO0.
- Dual SPI: Communicate with external memory with QIO0 and QIO1.
- Quad SPI: Communicate with external memory with QIO0, QIO1, QIO2 and QIO3.
- Octal SPI protocols: Communicate with external memory with QIO0 to QIO7.

When communicating with external memory, the instruction, address, and data can be set to use different modes which are configured in the Instruction Frame register (QSPI_IFR). There are ten combinations:

Value	Name	Description
0	SINGLE_BIT_SPI	Instruction: Single-bit SPI / Address-Option: Single-bit SPI / Data: Single-bit SPI
1	DUAL_OUTPUT	Instruction: Single-bit SPI / Address-Option: Single-bit SPI / Data: Dual SPI
2	QUAD_OUTPUT	Instruction: Single-bit SPI / Address-Option: Single-bit SPI / Data: Quad SPI
3	DUAL_IO	Instruction: Single-bit SPI / Address-Option: Dual SPI / Data: Dual SPI
4	QUAD_IO	Instruction: Single-bit SPI / Address-Option: Quad SPI / Data: Quad SPI
5	DUAL_CMD	Instruction: Dual SPI / Address-Option: Dual SPI / Data: Dual SPI
6	QUAD_CMD	Instruction: Quad SPI / Address-Option: Quad SPI / Data: Quad SPI
7	OCT_OUTPUT	Instruction: Single-bit SPI / Address-Option: Single-bit SPI / Data: Octal SPI
8	OCT_IO	Instruction: Single-bit SPI / Address-Option: Octal SPI / Data: Octal SPI
9	OCT_CMD	Instruction: Octal SPI / Address-Option: Octal SPI / Data: Octal SPI

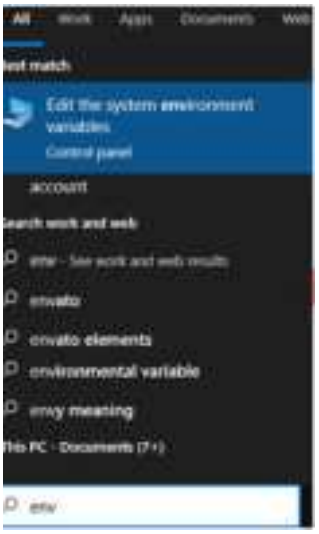
For detailed information on how to transfer instruction, address, and data with external memory, refer to the respective product data sheet.

3. Serial Flash XIP Example Using MPLAB Harmony v3

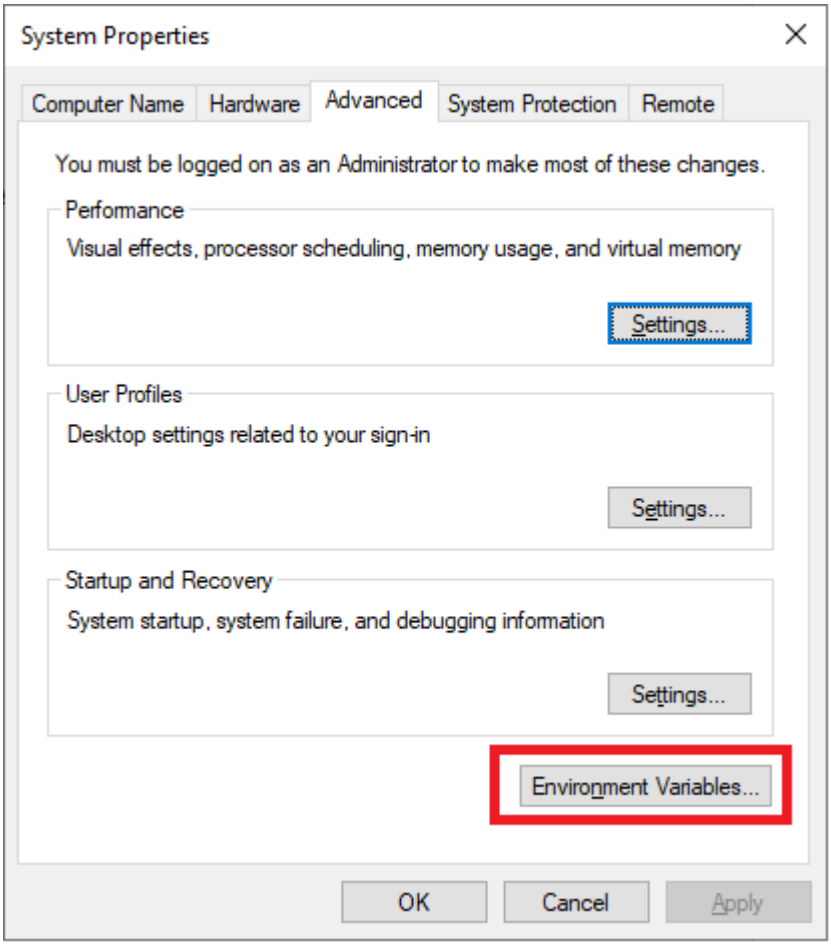
The example provided in this application note comprises the six steps detailed in the following sections.

3.1 SAM-BA Installation on Windows Host

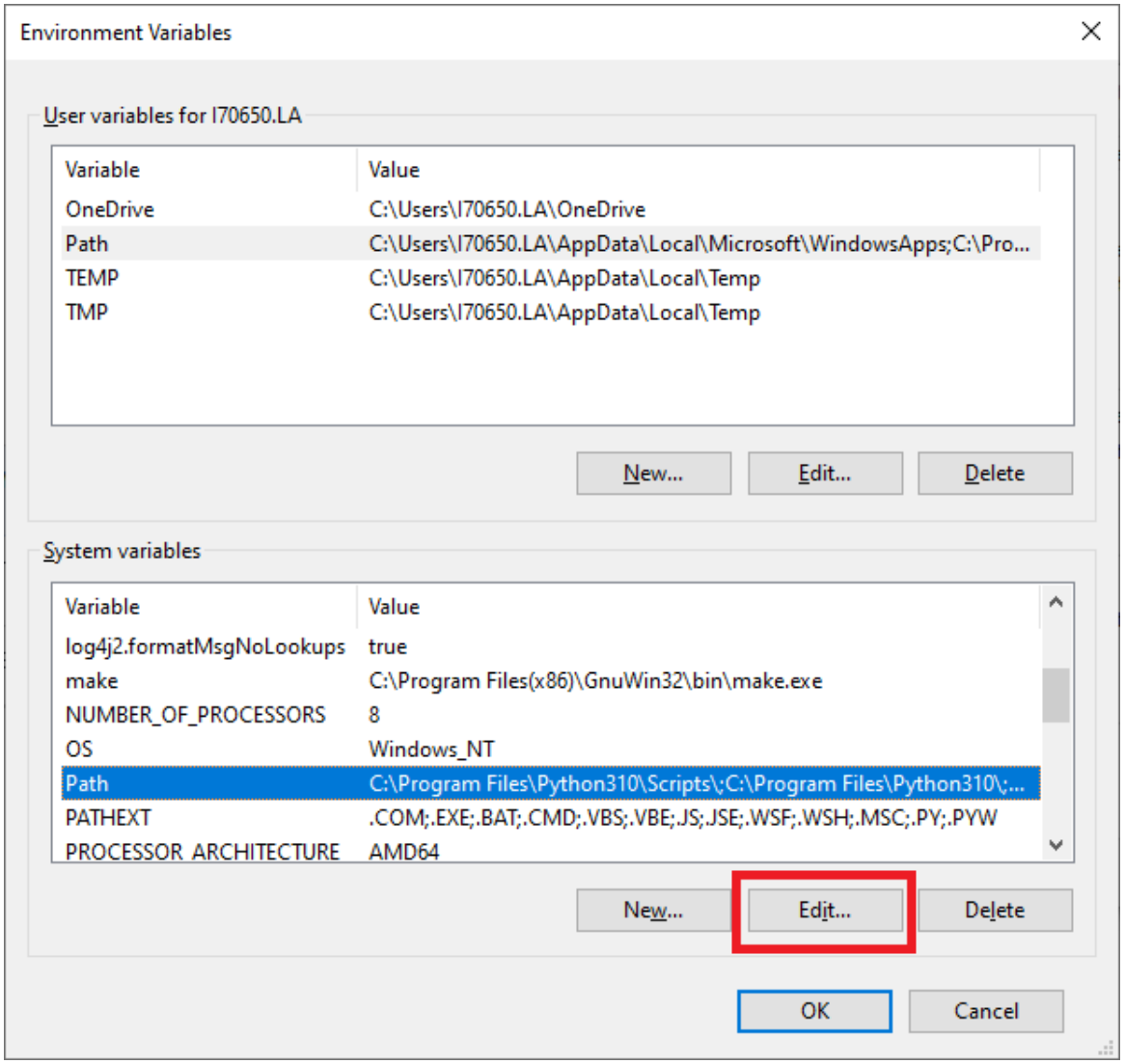
1. Download the latest version of SAM-BA tool for Windows. A link is available in 6. References.
2. Unzip the file into a working directory of your choice.
3. Add the SAM-BA directory path to the system environment variables.
   a. Select "Edit the system environment variables" in the pull-down menu.



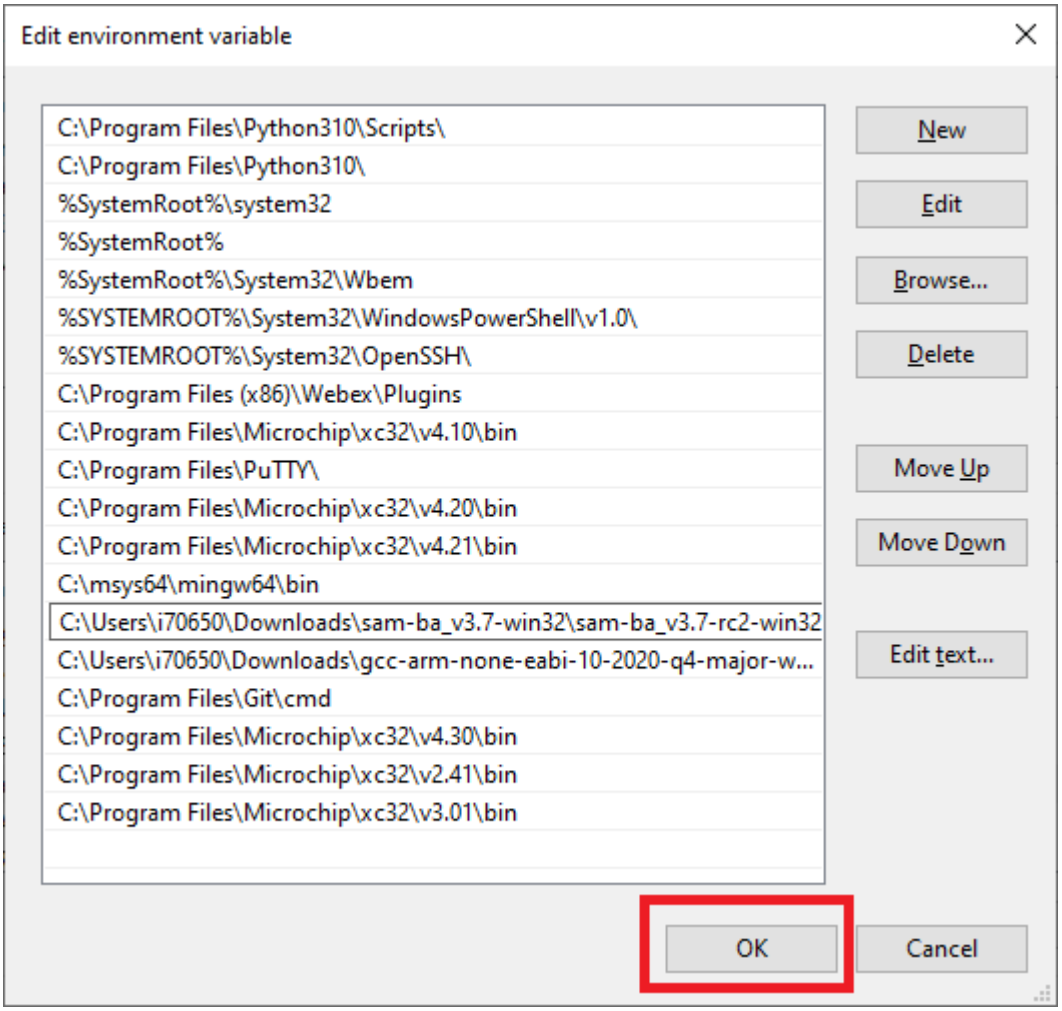
   b. In the System Properties window, click on "Environment Variables" in the Advanced tab.



c. In the Environment Variables window, double click on "Path" in the System Variables section.



d. Add the SAM-BA directory path to the path variables.



Once the SAM-BA Host program has been installed, the application is executed from the Windows command prompt using SAM-BA commands.

3.2 Device Set-Up to Flash Using SAM-BA

1. Open the Disable Boot jumper:
   a. J22 for SAMA7G54-EK Evaluation Kit
   b. J13 for SAM9X60-EK Evaluation Kit
2. Ensure there is no SD memory card inserted.
3. Press and release the start button (nSTART) on the SAMA7G54-EK. For SAM9X60-EK, this step is skipped.
4. Press and hold the "BOOT_DIS" button. This disables booting from the on-board NAND and NOR (QSPI) Flash memories,
5. While pressing the "BOOT_DIS" button, press and release the reset "nRST" button.
6. Release the "BOOT_DIS" button.
7. Confirm the MPU is set in SAM-BA monitor when `RomBOOT` appears on the console.
8. The MPU is now set in SAM-BA monitor and the device is ready to be programmed.

3.3 Configure the First Stage Bootloader to Boot from the Serial Flash Memory

The first-stage bootloader must be configured to boot from serial Flash memory. This can be done using SAM-BA commands. To information about the boot process and first-stage boot configuration, refer to the section "Boot Strategies" of the respective data sheet.

Note: This is not a mandatory step for SAM9X60-EK.

Note: A Windows command line must be open to run the SAM-BA commands.

The user accesses a list of all applets available by entering the command:

sam-ba -p <port> -b <board> -a help

Options:

1. -p, --port <port[:options:...]> where port can be **j-link** or **serial**
2. -b, --board <board[:options:...]> where board can be **sam9x60-ek** or **sama7g54-ek**

The boot configuration packet (BCP) can be written either to Emulation SRAM or to OTPC (One Time Programmable Memory Controller).

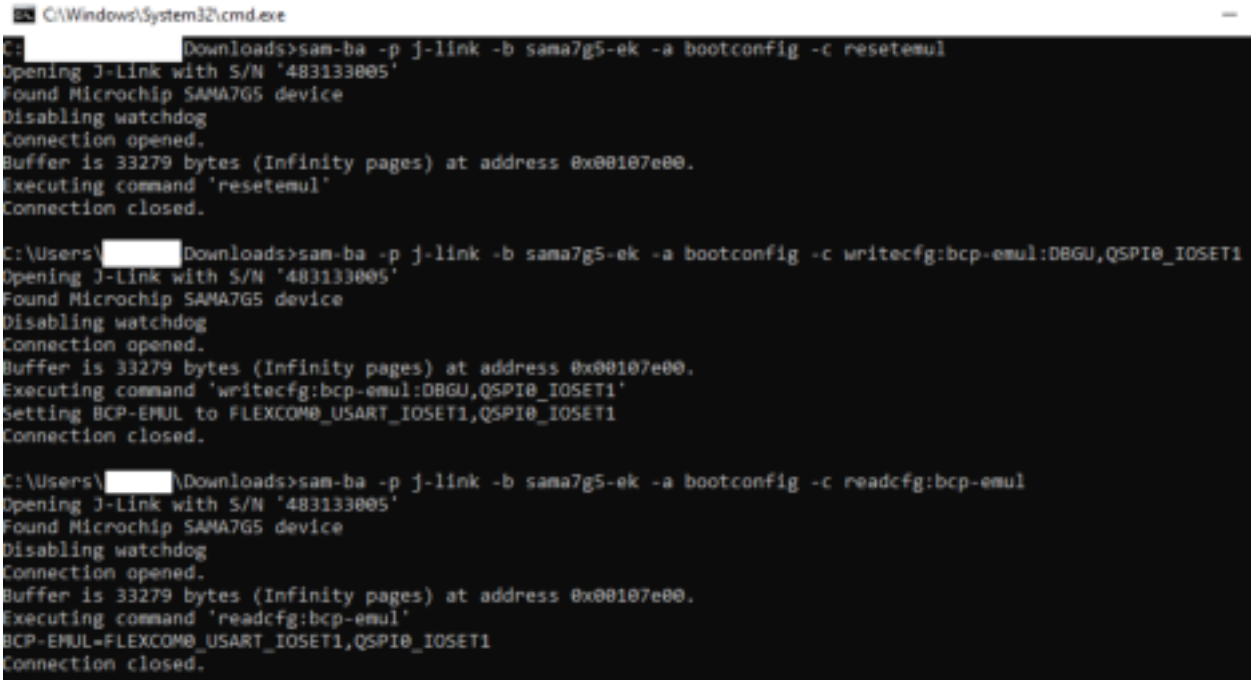
The user can program BCP to Emulation SRAM during the development phase and to OTPC during production phase.

The SAM-BA commands listed below can be used to program BCP to Emulation SRAM:

1. Enable emulation:
   sam-ba -p <port> -b <board> -a bootconfig -c writecfg:bscr:EMULATION_ENABLED
2. Read bscr and verify emulation is enabled:
   sam-ba -p <port> -b <board> -a bootconfig -c readcfg:bscr
3. Emulation SRAM reset:
   sam-ba -p <port> -b <board> -a bootconfig -c resetemul
4. Refresh Emulation SRAM:
   sam-ba -p <port> -b <board> -a bootconfig -c refreshcfg:emul
5. Enable QSPI0 as external NVM:
   sam-ba -p <port> -b <board> -a bootconfig -c writecfg:bcp-emul:QSPI0_IOSET1

6. Read bcp_emul and verify whether QSPI is set as external NVM:
   sam-ba -p <port> -b <board> -a bootconfig -c readcfg:bcp-emul
7. Reset the board by pressing and then releasing the reset button.

An example using SAMA7G54-EK is shown below:



Note: Boot configuration using Emulation SRAM must to be set up every power cycle.

WARNING Once OTPC is programmed, Emulation mode is disabled.

The steps below can be used to program BCP to OTPC:

1. Disable emulation:
   sam-ba -p <port> -b <board> -a bootconfig -c writecfg:bscr:EMULATION_DISABLED
2. Read bscr and verify emulation is disabled:
   sam-ba -p <port> -b <board> -a bootconfig -c readcfg:bscr
3. Refresh OTP:
   sam-ba -p <port>-b <board> -a bootconfig -c refreshcfg:otp
4. Enable QSPI0 as external NVM:
   sam-ba -p <port> -b <board> -a bootconfig -c writecfg:bcp-otp:QSPI0_IOSET1
5. Read bcp_otp and verify whether QSPI is set as external NVM:
   sam-ba -p <port> -b <board> -a bootconfig -c readcfg:bcp-otp
6. Reset the board by pressing and then releasing the reset button.

3.4 Configure the at91bootstrap to Enable XIP

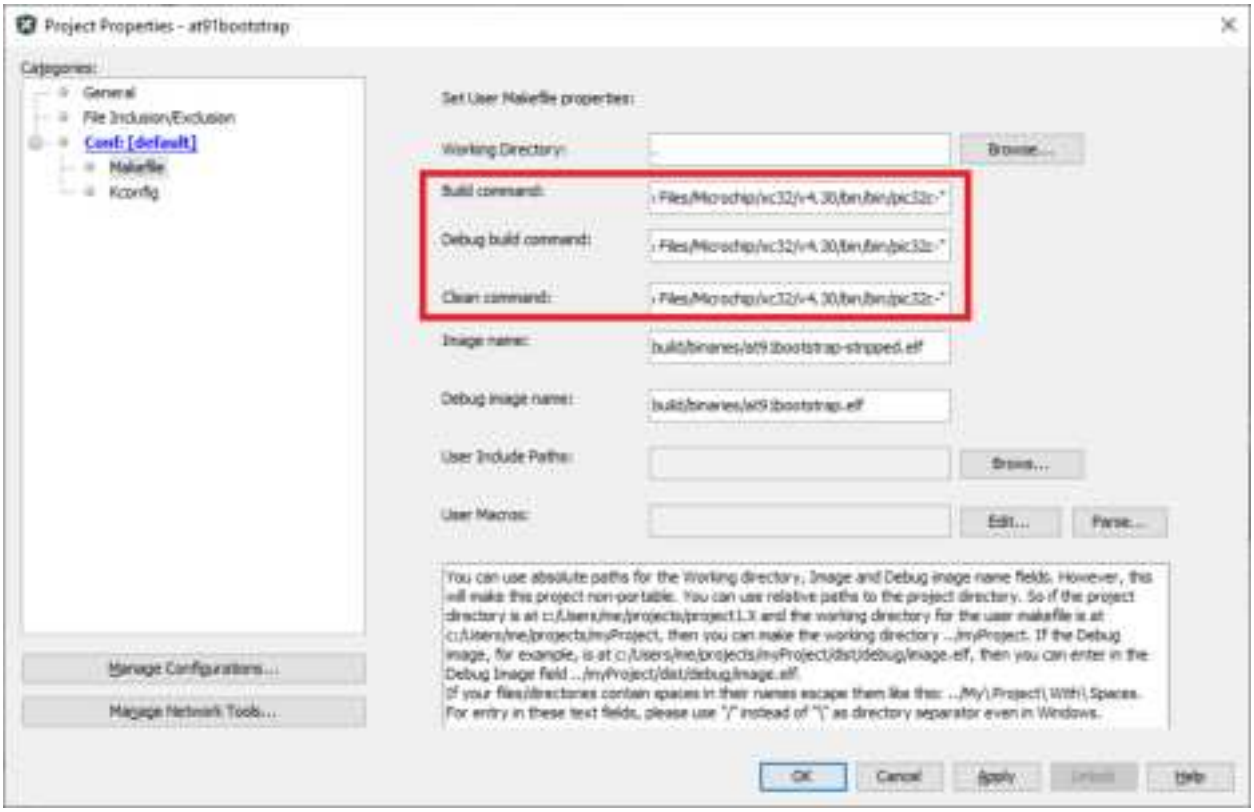
3.4.1 Preparing the Build Environment

1. The complete source code of at91bootstrap can be obtained by either of the following ways:
   - If you have Git installed, clone the repo into the project directory by using the command:
     $git clone git@https://github.com/linux4sam/at91bootstrap

- If you do not have Git installed, then download at91bootstrap from github and unzip into your project directory.

Note: Use at91bootstrap version 4.0.7 or later.

2. Open the project at91bootstrap on MPLAB X IDE and set it as the main project.
3. Use the XC32 compiler to build at91bootstrap.
   To do this:
   1. Note/Copy the XC32 installation path.
   2. Go to *Project>Properties>Makefile*.
   3. Paste the XC32 path in the Build, Debug build and Clean command fields.
      - E.g. Build/Debug command:
        make CROSS_COMPILE="C:/ProgramFiles/Microchip/xc32/v4.30/bin/bin/pic32c-"
      - Clean command:
        make mplabclean CROSS_COMPILE="C:/ProgramFiles/Microchip/xc32/v4.30/bin/bin/pic32c-"
   4. Click **Apply**.
   5. Click **OK**.



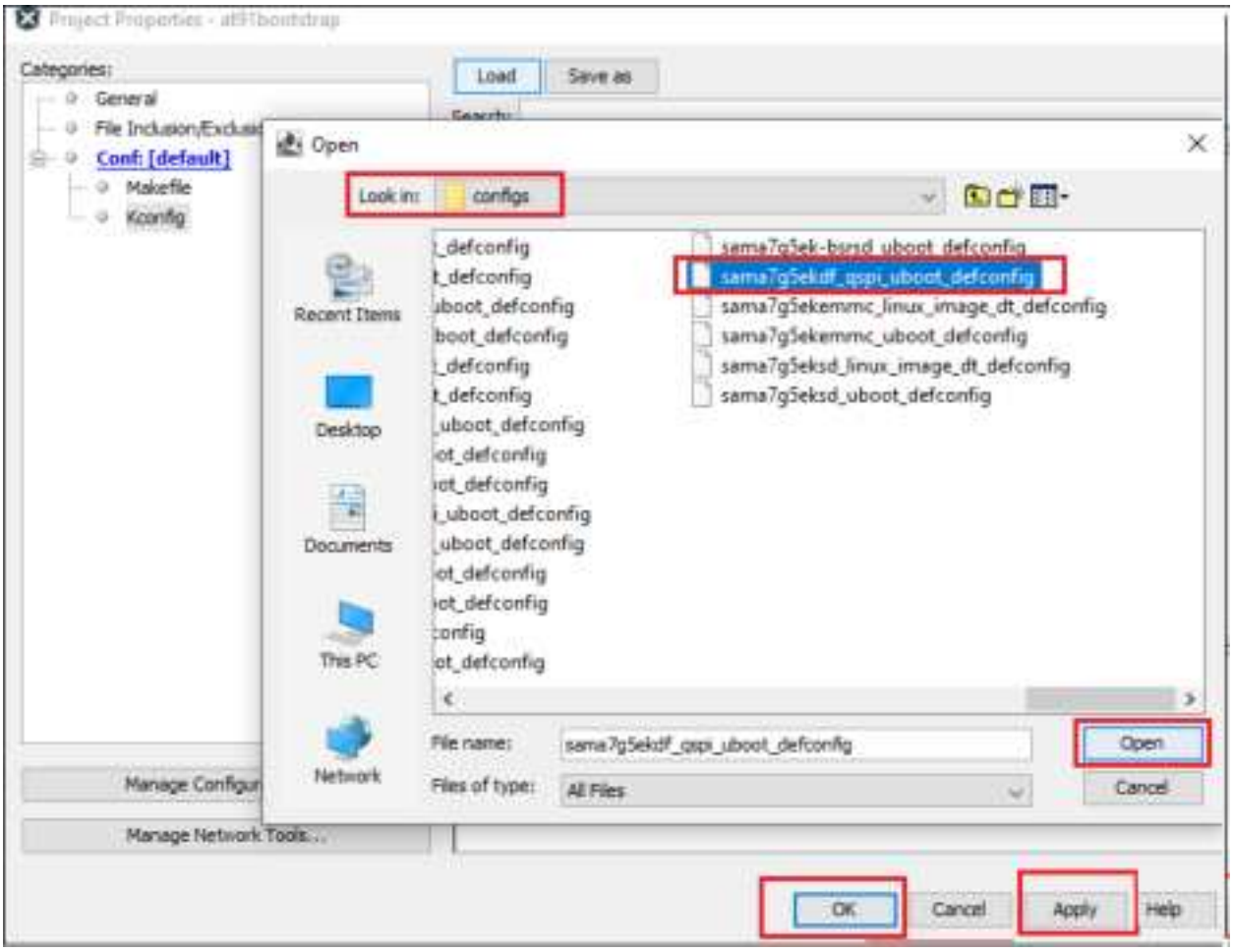
3.4.2 Configure the at91bootstrap

The at91bootstrap can be configured to either:

- debug Harmony applications executed from serial Flash on MPLAB X IDE
- run a Harmony application executed from serial Flash by using Kconfig.

3.4.2.1 Configure at91bootstrap to Debug Harmony Applications Executed from Serial Flash on MPLAB X IDE

1. Go to *Project>Properties>Kconfig>load*.
2. Select the appropriate project directory, then select configs.
3. In the configs folder, select <board>df_qspi_uboot_defconfig.
4. Click **Open**, then **Apply**, then **OK**.



Then perform the following changes:

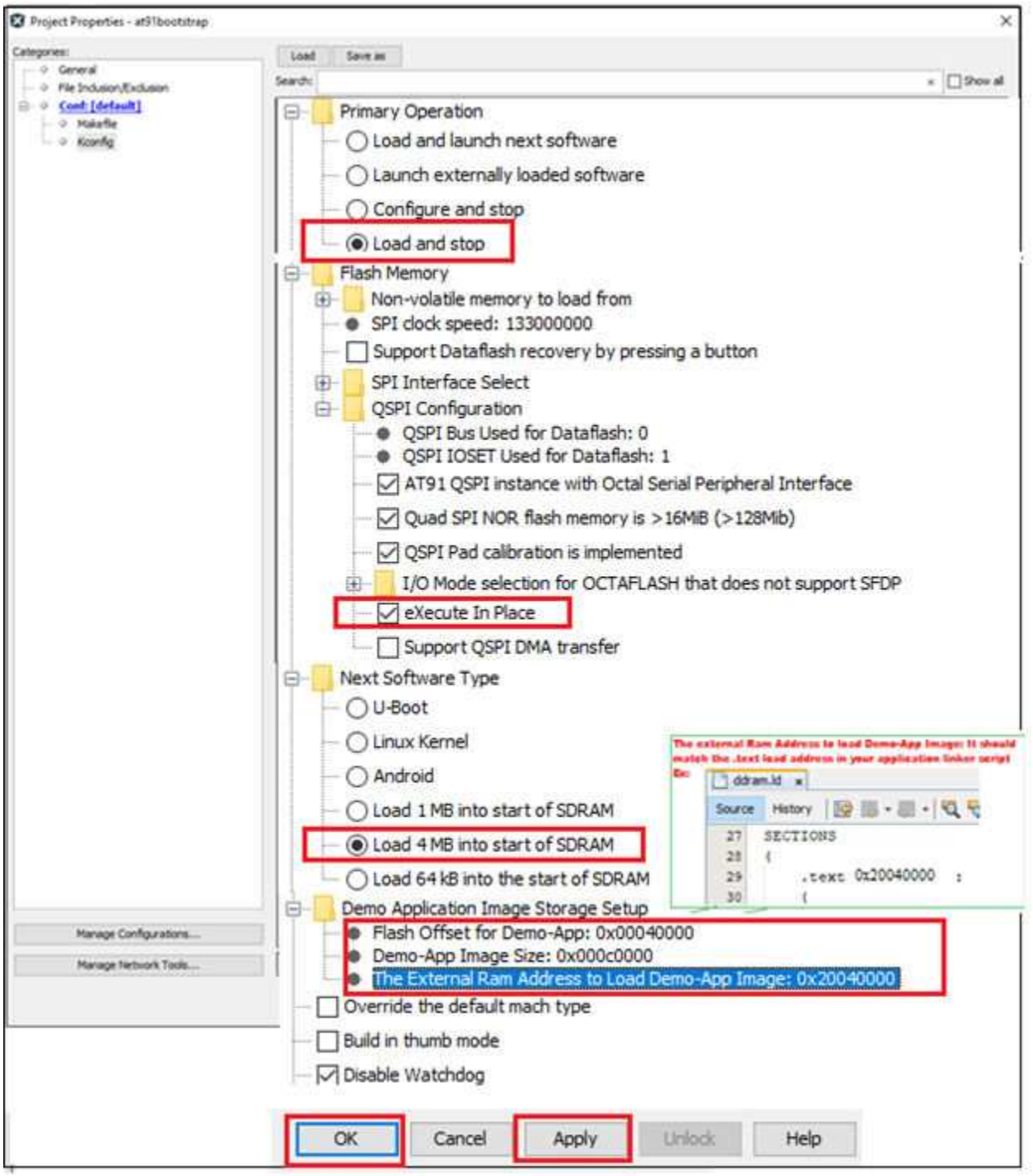
1. Under Primary Operation, select Load and Stop.
2. Under Flash Memory, expand QSPI Configuration, then select eXecute In Place.
3. Under Next software type, select Load 4 MB into the start of SDRAM.
4. Under Demo application image storage setup:
   - Flash offset is the QSPI offset where a user wants to flash the application.
   - Demo app image size is the size of the app image.
   - External RAM address to load Demo-App image is the QSPI starting address of the application. It should match the .text load address in your application linker file. The linker file can be found in the user application project folder, Eg: ddram.ld file)
5. Click **Apply**, then **OK**.

Note: The table below provides the external QSPI address for the boards. For details, refer to the product data sheet.

Table 3-1. External QSPI Address

Board Name	QSPI Start Address	QSPI End Address
SAM9X60-EK (DT100126)	0x70000000	0x708000000
SAMA7G54-EK (EV21H18A)	0x20000000	0x280000000

An example configuration for SAMA7G54-EK is shown below.



Now clean and build at91bootstrap.

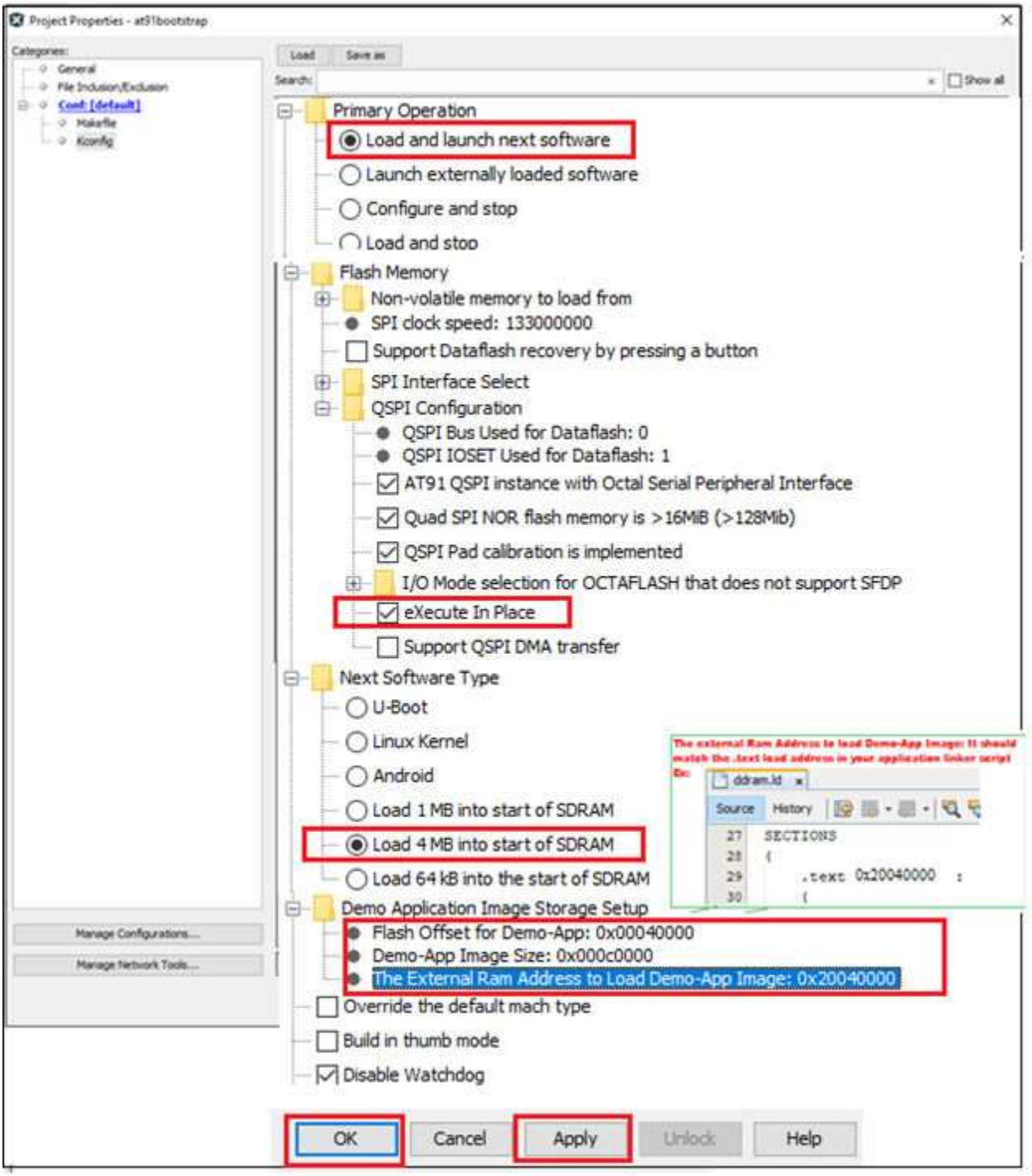
Note: The boot file (at91bootstrap.elf) generated by using this Kconfig can be used to debug the Harmony application executed from the serial Flash on MPLAB X IDE.

3.4.2.2 Configure at91bootstrap to Run Harmony Applications Executed from Serial Flash

The configuration step is the same as described in 3.4.2.2 , with a small modification:

- Under Primary Operation, select Load and launch next software.

An example configuration for SAMA7G54-EK is shown below.



Now clean and build at91bootstrap.

Note: The boot file (boot.bin) generated by using this Kconfig can be used to run Harmony applications executed from QSPI Flash.

3.5 Modifications Required to Execute a Harmony Application from Serial Flash

While creating a Harmony application on MPLAB X IDE, do the linker file modifications and serial Flash pin configuration described in the sections below. Then generate code and build the application, which is then executed from the serial Flash.

A link to create an application executed from the serial Flash on SAMA7G54-EK is given in 6. References.

3.5.1 Linker File Modifications

1. Assign a text section to serial Flash memory and a data section to the relocate section. The data section is copied from the serial Flash memory to SRAM during runtime.

   Notes:

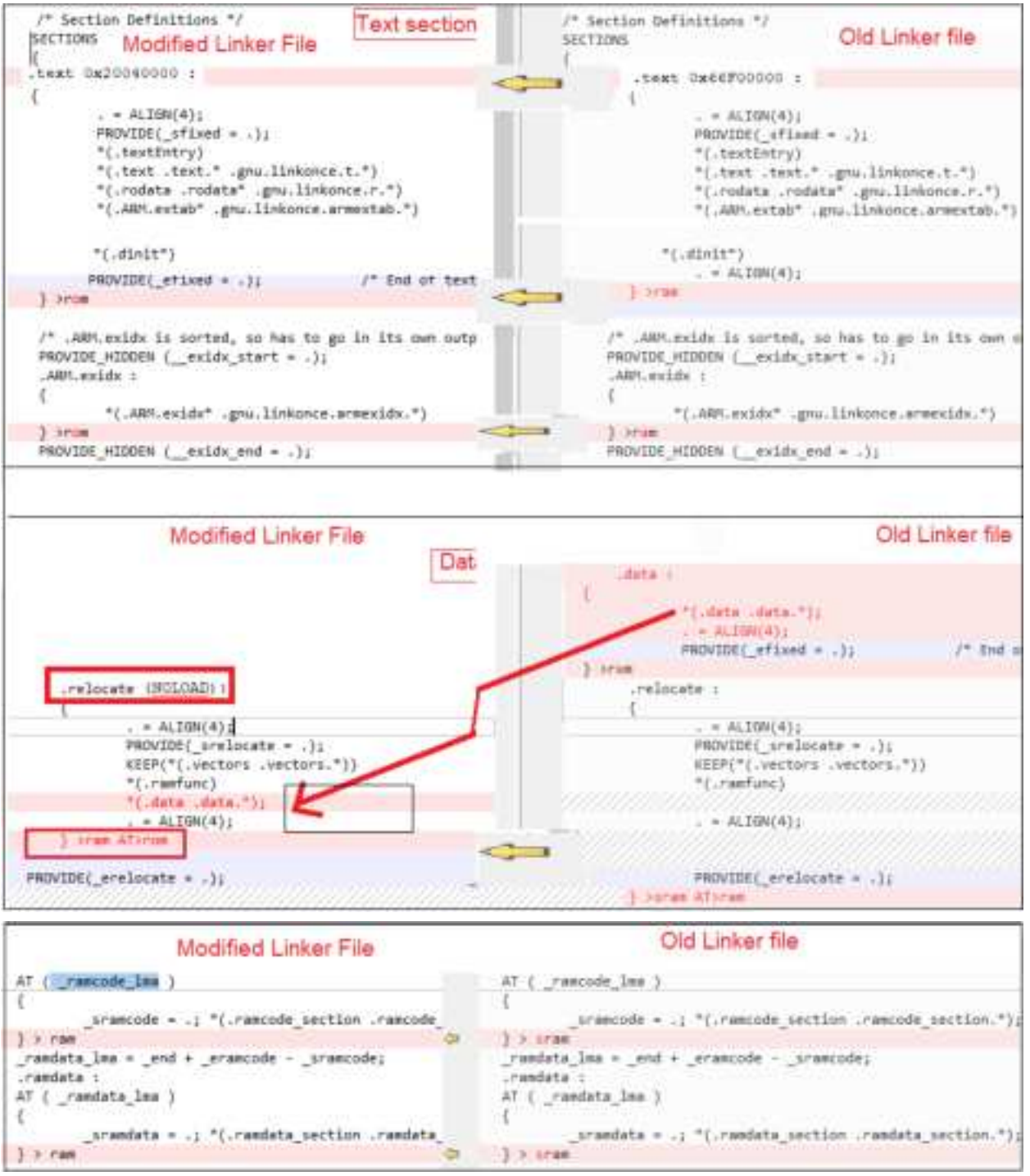
   - bss and relocate sections should be NOLOAD sections.
   - The relocate section should be loaded from serial Flash and run from SRAM.

2. Remove cache aligned sections and assign _ramcode_lma and _ramdata_lma to SRAM.

An example linker file of SAMA7G54-EK is given in the screenshots below.

Note: The text section load address should match the serial Flash jump address configured in the at91bootstrap.

```
/* Memory Spaces Definitions */
MEMORY
{
  ram         (!RWX) : ORIGIN = 0x00100000,   LENGTH = 128K /* sram */
  /* Octa SPI flash MX66LM1G45GXDI00 on SAMA7G54 is 1Gbit : 0x20000000--0x28000000
     0x20000000--0x2003FFFF is reserved for at91bootstrap */''
  rom         (LRX) : ORIGIN = 0x20040000, LENGTH = 0x7FBFFFF
}
```



3.5.2 Serial Flash Pin Configuration

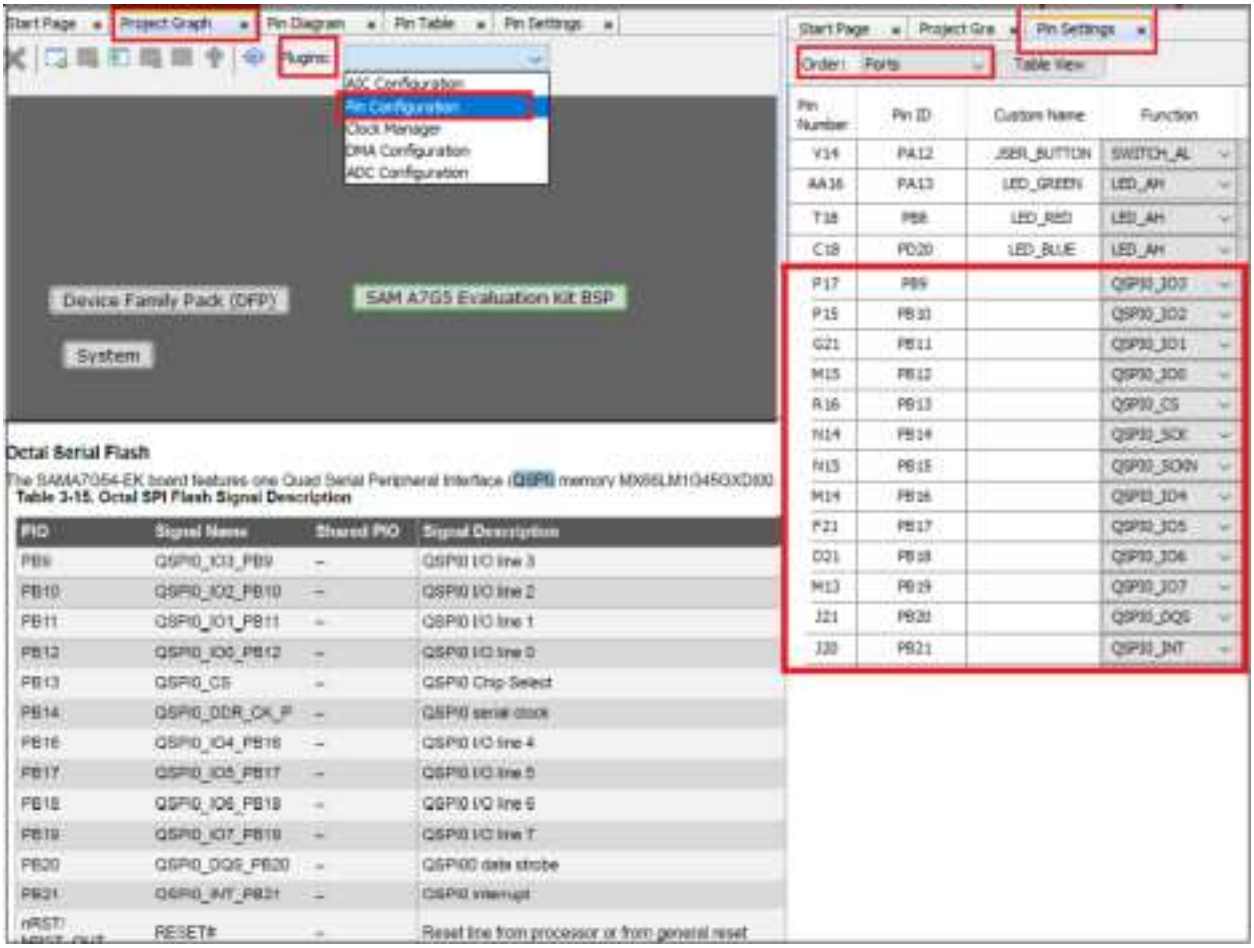
All the serial Flash pins must be configured properly to enable serial Flash support.

The table below provides the pin IDs to be used to connect to external Flash.

Table 3-2. Pin Configuration for Connection to External Flash

Board Name	Pin ID
SAM9X60-EK (DT100126)	PB19–PB24
SAMA7G54-EK (EV21H18A)	PB9–PB21

The screenshot below shows the configuration for the the SAMA7G54-EK board.



3.6 Debug an Application on MPLAB or Run an Application Executed from Serial Flash

3.6.1 Debug an Application Executed from the Serial Flash on MPLAB X IDE

Before debugging, ensure that the harmony.bin file in your project directory is flashed in the serial Flash offset. Refer to the sections 3.1 and 3.2 for initial device setup and tool installation procedure.

1. Erase the serial Flash:
   - ***sam-ba -p j-link -b <board> -a qspiflash -c erase***
2. Program the application starting from serial Flash offset of 0x40000:
   - ***sam-ba -p j-link -b <board> -a qspiflash -c write:harmony.bin:0x40000***

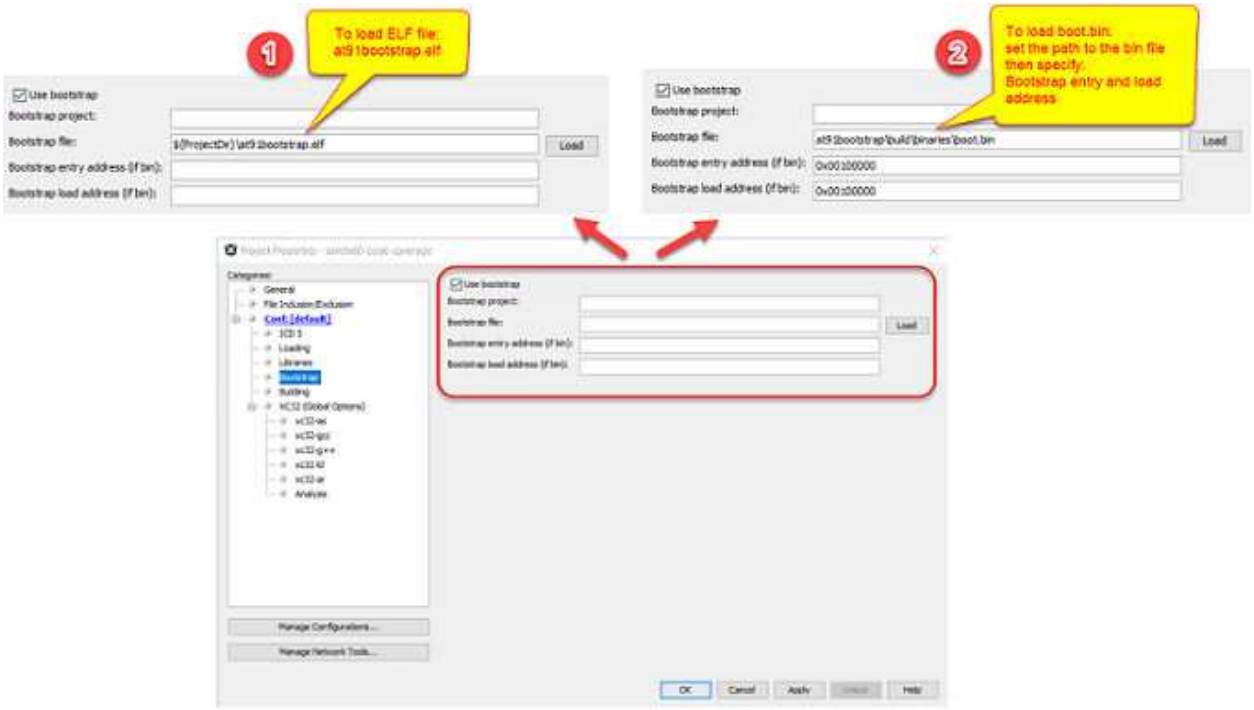
3. Reset the board.

The screenshot below illustrates step 2 performed on the SAMA9X60-EK (<board> set to sam9x60-ek).

```
C:\Users\       \sam9x60_ek_blink_led_qspi_xip\firmware\sam9x60_ek.X\dist\default\prod
uction>sam-ba -p j-link -b sam9x60-ek -a qspiflash -c write:harmony.bin:0x40000
Opening J-Link with S/N '483109897'
Found Microchip SAM9X60 device
Disabling watchdog
Connection opened.
Detected memory size is 8388608 bytes.
Page size is 256 bytes.
Buffer is 11520 bytes (45 pages) at address 0x0030a2c0.
Supported erase block sizes: 4KB
Executing command 'write:harmony.bin:0x40000'
Appending 88 bytes of padding to fill the last written page
Wrote 3584 bytes at address 0x00040000 (100.00%)
Connection closed.
```

Note: Do not flash boot.bin to serial Flash memory using SAM-BA to debug the application on MPLAB X IDE.

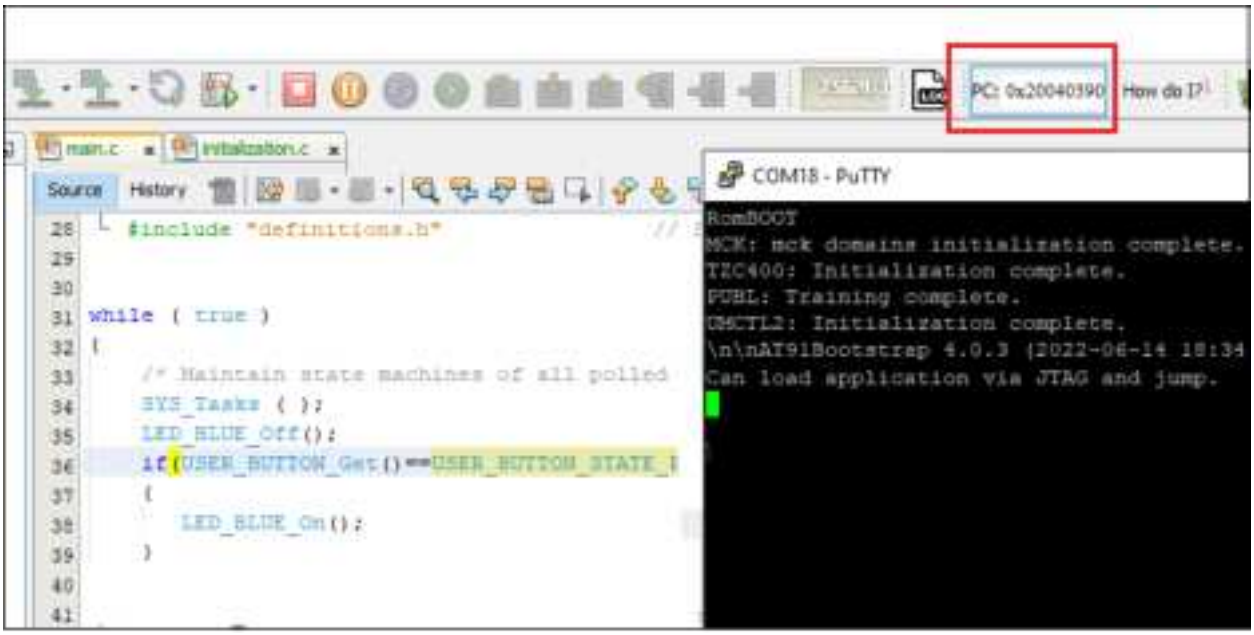
To debug the Harmony application executed from the serial Flash on MPLAB X IDE, use either at91bootstrap.elf or boot.bin file generated in 3.4.2.1 in the Harmony application project properties. If boot.bin is used, the boot entry address and boot load address must be added in the project properties as illustrated in the following screenshot.



Start debugging the application on MPLAB X IDE. The user can observe the program counter and see that the Harmony application is executed from the serial Flash memory.

With the serial connection established between the board and host PC, open the serial console to monitor debug messages.

An example screenshot is shown below:



3.6.2 Running the Harmony Application Executed from Serial Flash Memory

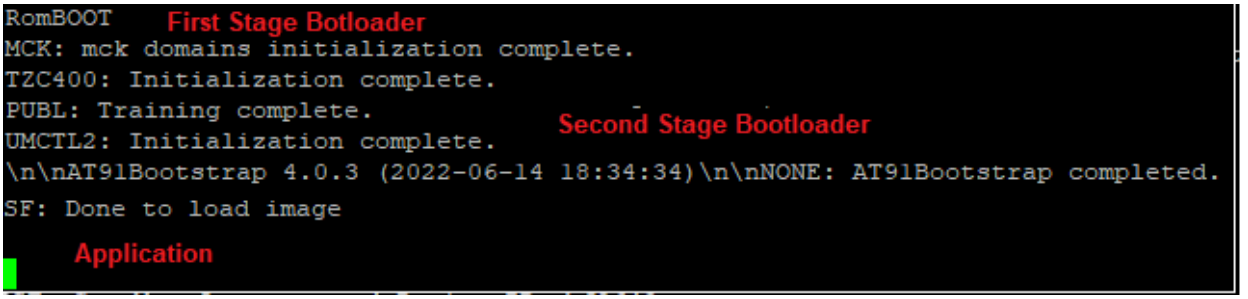
To run the Harmony application executed from serial Flash memory upon reset, flash the boot.bin and harmony.bin files to the serial Flash memory with the SAM-BA commands shown below.

Note: To run the Harmony application executed from serial Flash upon reset, use the boot.bin file generated in section 3.4.2.2

The SAM-BA commands to program the boot and application file to serial Flash are:

1. Erase the entire serial Flash:
   - ***sam-ba -p j-link -b sam9x60-ek -a qspiflash -c erase***
2. Program the at91bootstrap in the starting address of the serial Flash:
   - ***sam-ba -p j-link -b sam9x60-ek -a qspiflash -c writeboot:boot.bin***
3. Program the application starting from serial Flash offset of 0x40000
   - ***sam-ba -p j-link -b sam9x60-ek -a qspiflash -c write:harmony.bin:0x40000***

Now press the reset button and the user application is executed from serial Flash.



Note: A console serial communication can be enabled to observe the debug messages.

4. Performance

The QSPI allows the system to use high-performance serial Flash memories which are small and inexpensive, in place of larger and more expensive parallel Flash memories. Therefore, the performance of the QSPI plays an important role. The performance of the QSPI is bounded by the QSPI speed, Flash capabilities and other criteria.

Note: Refer to the application note “SAMA5D2 Quad SPI (QSPI) Performance” given in 6. References. Performance numbers in the document may vary with respect to compiler settings and optimization levels.

5. Conclusion

Developing a QSPI application in XIP requires an understanding of the QSPI protocols, at91bootstrap Kconfig settings and linker scripts. MPLAB Harmony v3 provides a flexible, abstracted and fully integrated firmware development platform for 32-bit MPUs. This document described how to use the XIP mode in the QSPI to work with external Flash memories and how to set up MPLAB X IDE to debug the application.

6. References

1. SAM-BA In-System Programmer Download
2. Application Note: SAMA5D2 Quad SPI (QSPI) Performance
3. Harmony application : Blink LED QSPI-XIP application on SAMA7G54-EK
4. Harmony application : Blink LED QSPI-XIP application on SAM9X60-EK
5. Configure and build at91bootstrap to enable QSPI-XIP on MPLAB Harmony
6. Step by Step guide to develop a Harmony application getting executed from Serial flash memory on SAM9X60-EK

7. Revision History

Revision A - 12/2023

This is the initial release of this document.

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