Description

The AL5958 is a 48-channel constant current sources matrix driver with M-PDM (Multiplex Pulse Density Modulation) control, supporting any dynamic applications from 0 scan to 32 scans. When connected to two devices, they can support up to 32 scans each device with 16 scans of integrated built-in nMOS switches. The distinctive M-PDM technology increases the refresh rate of dynamic scanning systems without increasing the frequency of grayscale clock to prevent high clock frequency causing EMI interference. And the technique of automatic black frame insertion could abate efficiently the influence of blurs caused by the scanning switch and built-in intelligent matrix display functions.

The device operates from 3V to 5V input voltage range and provides 48 constant current sourcing outputs that deliver up to 20mA of high accuracy current for each LED channel string. The current output of each color group can either be set by three different external current-sensing resistors or program a 6-bit global current control register.

The AL5958 provides a good channel to channel current accuracy and device to device current matching ±1.5% (typical).

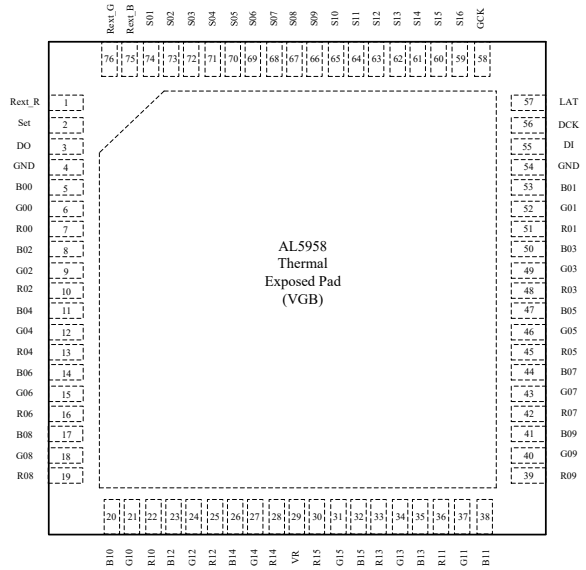
The device operates over -40°C to +85°C ambient temperature range. The AL5958 is available in wettable W-QFN9090-76/SWP (Type A1) package.

Features

- Two Separated Power Supply: VR and VGB
  - VR Supply Range 2.8V to 5V
  - VGB Supply Voltage Range 3V to 5V
- 48 Output Current Sources:
  - 0.5mA to 20mA Constant Current Output Range
  - Current Setting by 3 External Resisters
  - 6-Bit Global Current Control for Each Color Group
  - ±1.5% (typ) LED Current Accuracy Between Channels
  - ±1.5% (typ) LED Current Matching Between Devices
  - Output Staggered Delay
- Built-in 16 NMOS Scan Switches
  - For Static and Dynamic Systems from 0 Scan to 1/32 Scan
  - Flexible Scan Sequence
- Built-in 3 x 16k Bits SRAM
- Grayscale PWM Dimming
  - 16-Bit PWM Dimming Resolution
  - High Refresh Rate or Standard PWM
  - Multiplex Pulse Density Modulation Technology
  - Grayscale Clock Pin as PWM Input
  - Select Internal Grayscale PWM Clock for EMI Reduction
- Diagnosis and Protections
  - LED Open/Short
  - Grayscale Clock Watchdog
  - Undervoltage Lockout (UVLO)
- Built-in Intelligent Matrix Display Functions
  - Automatic Black Frame Insertion
  - Last Scan and Next Scan Line Ghost Image Abatement
  - Low Brightness Uniformity Compensation
  - Short LED Caterpillar & Open LED Fail Line Abatement
- Daisy-Chained up to 64 Devices
- Sleep Mode to Save Power
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Pin Assignments

(Top View – Not to Scale)



W-QFN9090-76/SWP (Type A1)

Applications

- Mini and micro-LED matrix display products
- RGB LED backlighting
- Gaming PC and keyboards
- Audio mixer indicators
- Music spectrum indicator equalizers
- LED luminous panels
- Local dimming backlights
- Film studio digital backgrounds

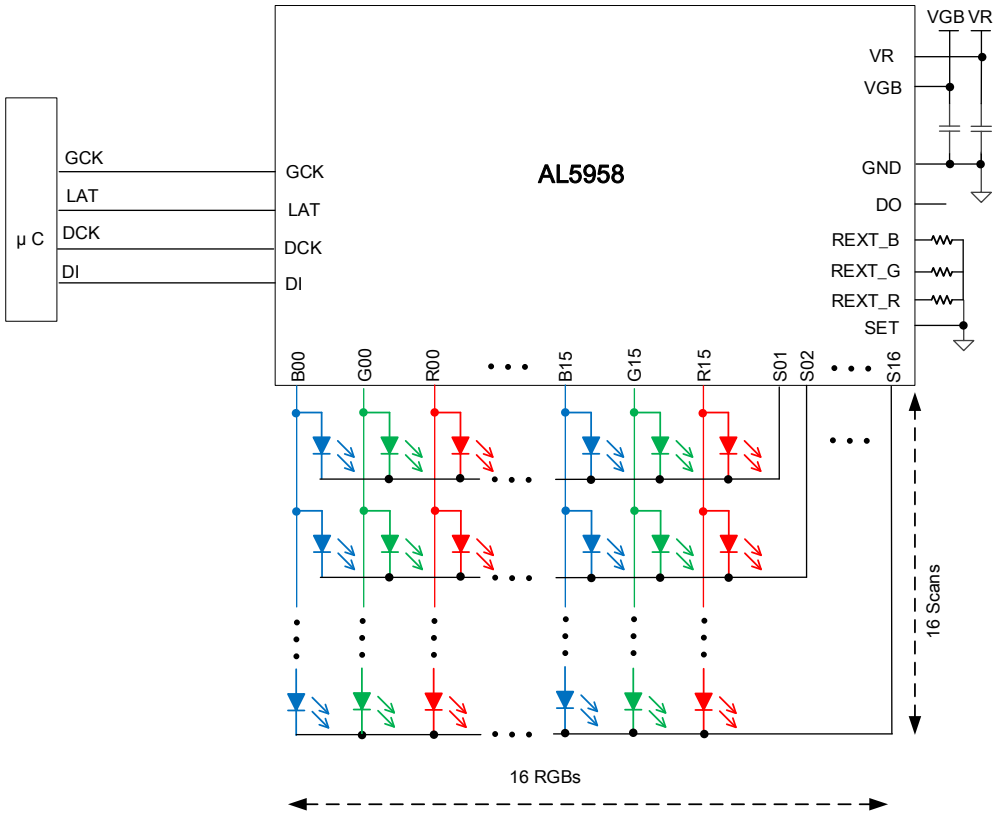
Device Information

Orderable Part Number	Package	Body Size
AL5958JCZW76-13	W-QFN9090-76/SWP (Type A1)	9mm x 9mm

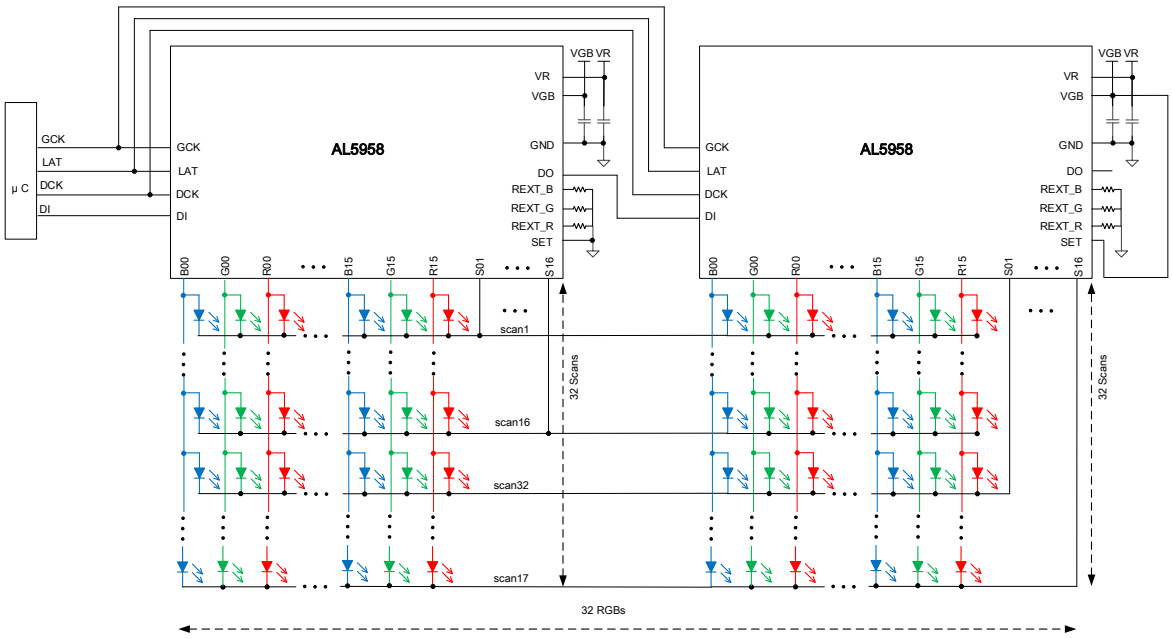
Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

1. Single device connection with 16 scans

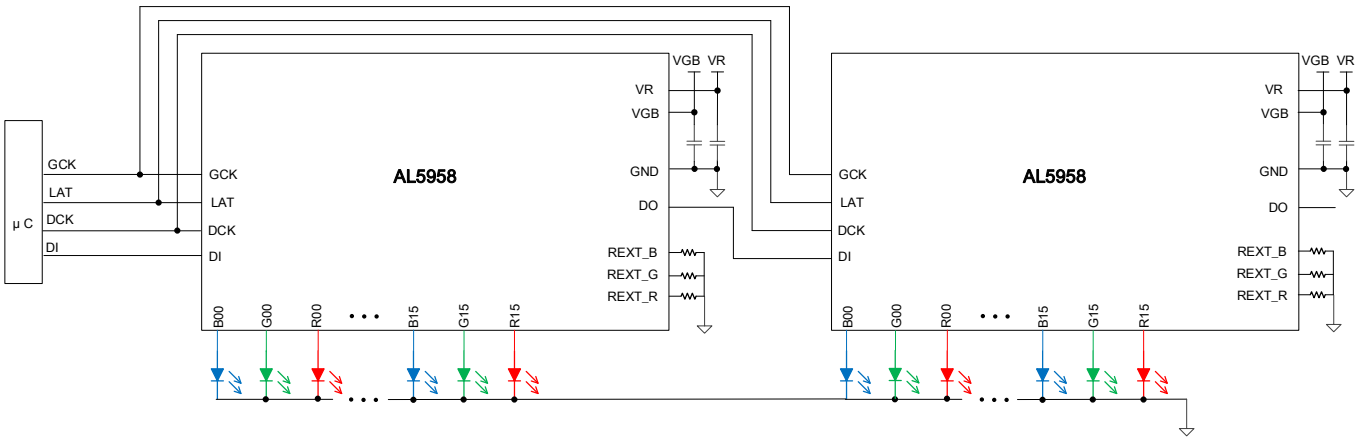


2. Dual device cascaded connection with 32 scans



Typical Applications Circuit (continued)

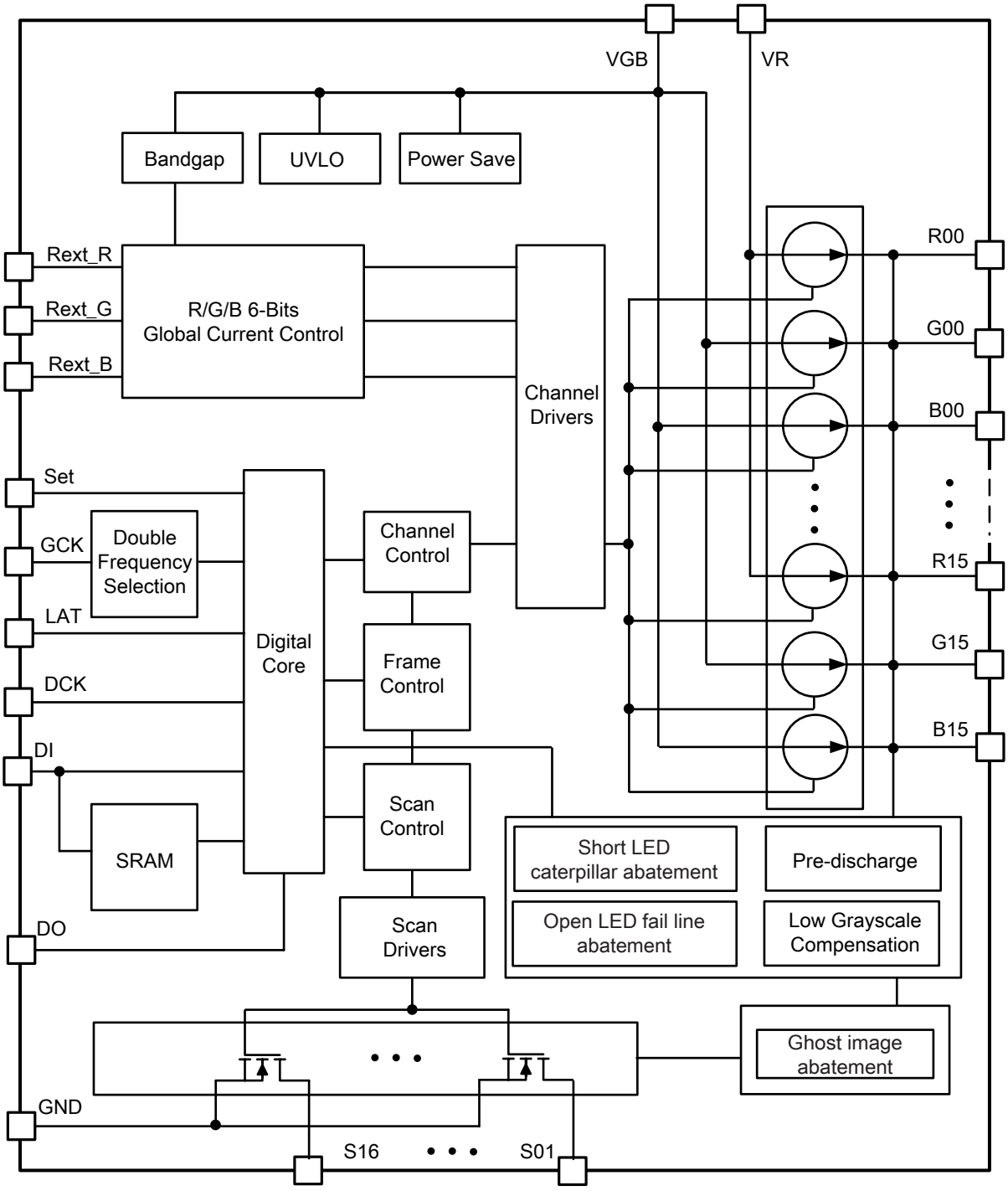
3. Dual device cascaded connection with no scans



Pin Descriptions

Pin Number	Pin Name	Function
5 to 28	B00, G00, R00 to B14, G14, R14	Source Constant-Current Outputs
29	VR	Source Supply Voltage Terminal of VLED_R (VR must ≤ VGB and cannot be floating)
30 to 53	R15, G15, B15 to R01, G01, B01	Source Constant-Current Outputs
54, 4	GND	Ground Terminal. (Both pin 54 and 4 need to connect to ground)
55	DI	Serial Data Input Terminal for All Channels.
56	DCK	Synchronous Clock Input Terminal for Serial Data Transfer. Data is sampled at the rising edge of DCK.
57	LAT	Input Terminal of Data Strobe and SCAN Mode Setting. Combine DCK with LAT to execute the frame latch and define the initial position of SCAN mode.
58	GCK	External Grayscale Clock Input for PDM Operations and Black Frame Insertion
59 to 74	S16 to S01	NMOS outputs. Set pin = 0: S01 to S16 = nMOS output of scan 1 to 16 (Nout 1 to 16) Set pin = f: S01 to S16 = nMOS output of scan 25 to 10 (Nout 25 to 10) Set pin = 1: S01 to S16 = nMOS output of scan 32 to 17 (Nout 32 to 17) *f means floating.
75, 76, 1	Rext_B / G / R	The External Resistor Connected Between REXT and GND for Output Current Value Setting. (Cannot be floating)
2	Set	Mode Selection for S01 to S16. [0, f, 1 (f means floating)]
3	DO	Serial Data Output Terminal for All Channels.
EP	VGB	Supply Voltage Terminal of Chip and Green + Blue LED. (VLED_GB) (The definition of digital input voltage level is associated with VGB.)

Functional Block Diagram



Absolute Maximum Ratings (Notes 4, 5)

Characteristic	Symbol	Rating	Unit
Supply Voltage	VLED (VR/VGB)	-0.3 to 5.5	V
Input Voltage	V_{DI}, V_{LAT}, V_{DCK}, V_{GCK}	-0.3 to VGB+0.3	V
NMOS Output Current	IOUTN	0.72	A
Output Current	IOUT	24	mA
Output Voltage	VOUT	R01 to R16: -0.3 to VR+0.3 G01 to G16, B01 to B16: -0.3 to VGB+0.3	V
Junction Temperature	T_J	-40 to +150	°C
Storage Temperature	T_{stg}	-55 to +150	°C

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
5. All voltage values are with respect to ground terminal.

Package Thermal Information (Note 6)

Symbol	Thermal Resistance	Value	Unit
$R_{\Theta JA}$	Junction-to-Ambient Thermal Resistance	20.3	°C/W
$R_{\Theta JC(top)}$	Junction-to-Case (Top) Thermal Resistance	7.2	°C/W
$R_{\Theta JB}$	Junction-to-Board Thermal Resistance	7.2	°C/W
Ψ_{JT}	Junction-to-Top Characterization Parameter	0.1	°C/W
Ψ_{JB}	Junction-to-Board Characterization Parameter	7.3	°C/W
$R_{\Theta JC(bot)}$	Junction-to-Case (Bottom) Thermal Resistance	2.8	°C/W

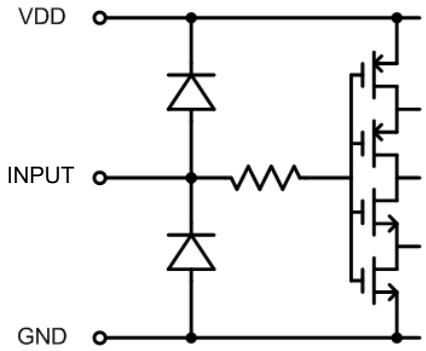
Note: 6. Test condition: device mounted on FR-4 PCB (51mm x 51mm 2oz copper, minimum recommended pad layout on top layer and thermal vias to bottom layer with maximum area ground plane. For better thermal performance, larger copper pad for heatsink is needed.

Recommended Operating Condition

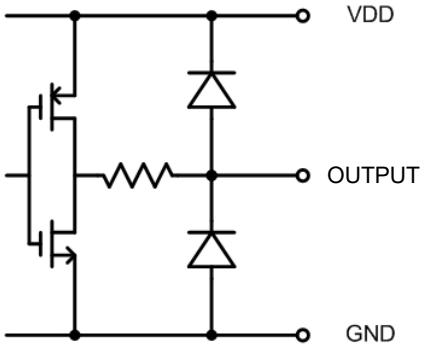
Symbol	Parameter	Min	Typ	Max	Unit
VGB	IC Operating and G/B-LED Supply Voltage	3	3.8	5	V
VR	R-LED Supply Voltage	2.8	3.0	VGB	V
IOUT	Output Current	0.5	—	20	mA
T_A	Ambient Temperature	-40	+25	+85	°C

Equivalent Circuit of Inputs and Outputs

1. DCK, DI, LAT, GCK Terminals



2. DO Terminal



Electrical Characteristics (VR = 2.8V, VGB = 3.8V, -40°C ≤ T_A ≤ +85°C, unless otherwise specified.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Input Voltage "H" Level	VIH	CMOS logic level	0.7VGB	—	VGB	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.3VGB	
NMOS Switch On-Resistance	$R_{DS(ON)}$	VGB = 3.8 V	—	450	—	mΩ
Output Leakage Current	ILK	VOUT = 0, T_A = +25°C	—	—	1	μA
Driving Current (DO)	IOL	VOL = 0.4V	1	2.35	5	mA
	IOH	VOH = VGB-0.4	-5	-2.15	-1	
Output Current Skew (Channel-to-Channel) (Note 7)	dIOUT1	VOUT_R = VR-0.7V VOUT_G/B = VGB-0.7V Rext = 1.4kΩ @10mA Gain = 100% CMD3[10:8] = 000 T_A = +25°C	—	±1.5	±5	%
Output Current Skew (Chip-to-Chip) (Note 8)	dIOUT2		—	±1.5	±5	%
Output Current Skew (Channel-to-Channel) (Note 7)	dIOUT3	VOUT_R = VR-0.7V VOUT_G/B = VGB-0.7V Rext = 7kΩ @1mA Gain = 50% CMD3[10:8] = 100 T_A = +25°C	—	±1.5	±5	%
Output Current Skew (Chip-to-Chip) (Note 8)	dIOUT4		—	±1.5	±5	%
Dropout Voltage	Vsat	Rext = 1.4kΩ IOUT @10mA	—	0.4	—	V
Output Voltage Regulation (Note 9)	% / VOUT	Rext = 1.4kΩ @10mA VOUT = 2V to 0	—	±0.1	±1	% / V
Supply Voltage Regulation (Note 10)	% / VLED	Rext = 1.4kΩ @10mA VLED = 3V to 5V	—	±0.5	±1	

Notes:

7. $$\Delta(\%) = \left[\frac{Iout_n}{\frac{(Iout_0 + Iout_1 + \ldots + Iout_{15})}{16}} - 1 \right] * 100\%$$

8. $$\Delta(\%) = \left[\frac{\frac{(Iout_0 + Iout_1 + \ldots + Iout_{15})}{16} - (Ideal\ \ Output\ \ Current)}{(Ideal\ \ Output\ \ Current)} \right] * 100\%$$

9. $$\Delta(\%/V) = \left[\frac{Iout_n(@Vout_n = 3V) - Iout_n(@Vout_n = 1V)}{Iout_n(@Vout_n = 3V)} \right] * \frac{100\%}{3V - 1V}$$

10. $$\Delta(\%/V) = \left[\frac{Iout_n(@V_{DD} = 5.5V) - Iout_n(@V_{DD} = 3V)}{Iout_n(@V_{DD} = 3V)} \right] * \frac{100\%}{5.5V - 3V}$$

(VDD = VR or VGB)

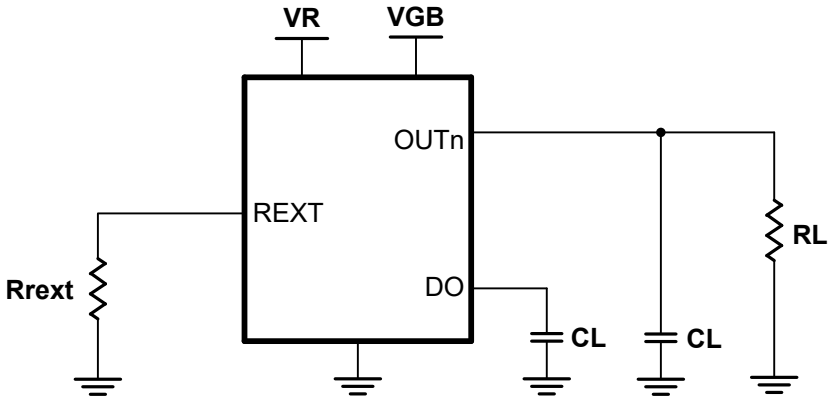
Electrical Characteristics (VR = 2.8V, VGB = 3.8V, -40°C ≤ T_A ≤ +85°C, unless otherwise specified.) (continued)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Static Supply Current (Note 11)	IVR1	Input signal is static Rext = 7kΩ @1mA All outputs turn off	1	2.4	5	mA
	IVGB1	Input signal is static Rext = 7kΩ @1mA All outputs turn off	3	6.5	16	
	IVR2	Input signal is static Rext = 1.4kΩ @10mA All outputs turn off	1.5	3.4	6	
	IVGB2	Input signal is static Rext = 1.4kΩ @10mA All outputs turn off	4	7.9	19	

Note: 11. IO excluded.

Switching Characteristics (VR = 2.8V, VGB = 3.8V, -40°C ≤ T_A ≤ +85°C, unless otherwise specified.) (Guarantee by design)

Characteristic		Symbol	Condition	Min	Typ	Max	Unit
Propagation Delay ('L to 'H')	DCK-DO	tpLH3	VIH = VGB VIL = GND Rext = 1.4kΩ @10mA Gain = 100% RL = 200Ω CL = 13pF	10	22.5	50	ns
Propagation Delay ('H' to 'L')	DCK-DO	tpHL3		10	22.5	50	
Pulse Duration	LAT	$tw_{(LAT)}$		50	—	—	
	GCK	$tw_{(GCK)}$		20	—	—	
	DCK	$tw_{(DCK)}$		20	—	—	
Setup Time	LAT	$tsu_{(LAT)}$		20	—	—	
	DI	$tsu_{(D)}$		10	—	—	
Hold Time	LAT	$th_{(LAT)}$		20	—	—	
	DI	$th_{(D)}$		10	—	—	
Hold Time of Instruction		$th_{(CM)}$		20	—	—	
DO Rise Time		$tr_{(DO)}$		6	12	30	
DO Fall Time		$tf_{(DO)}$		6	12	30	
Data Clock Frequency (Single Edge)		f_{DCK_S}		—	—	24	MHz
Data Clock Frequency (Double Edge)		f_{DCK_D}		—	—	12	
Grayscale Clock Frequency (Single Edge)		f_{GCK_S}		—	—	24	
Grayscale Clock Frequency (Double Edge)		f_{GCK_D}		—	—	12	

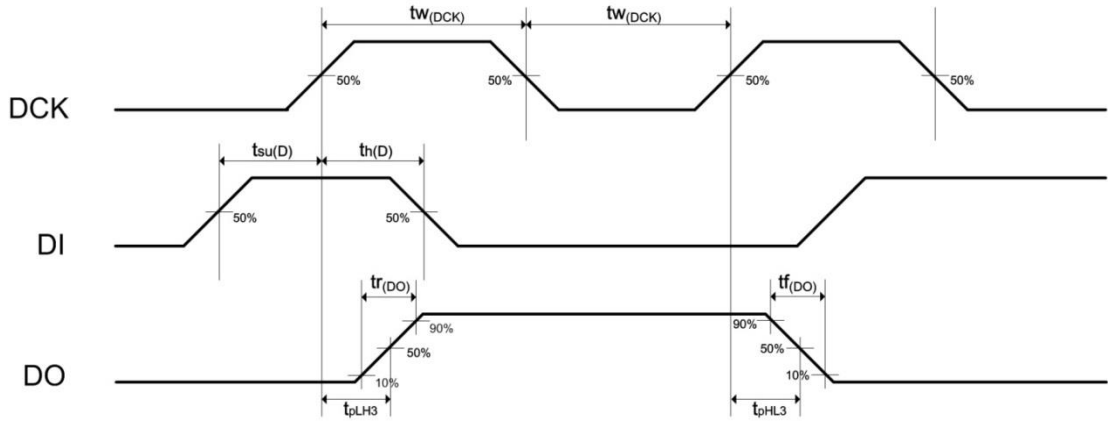


Switching Characteristics Test Circuit

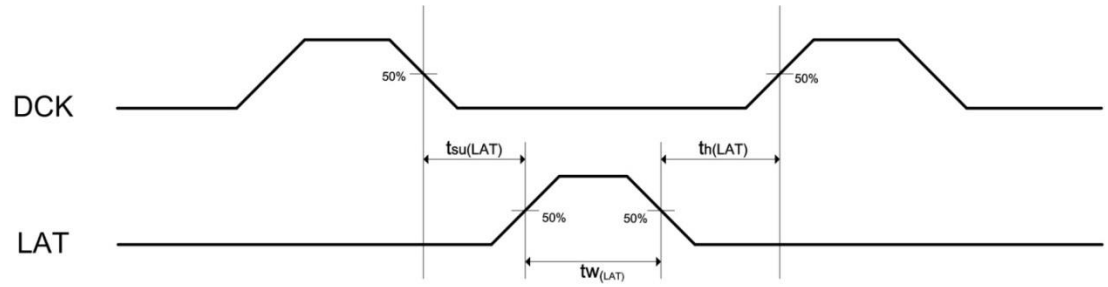
Switching Characteristics (VR = 2.8V, VGB = 3.8V, -40°C ≤ T_A ≤ +85°C, unless otherwise specified.) (continued)

Timing Diagram

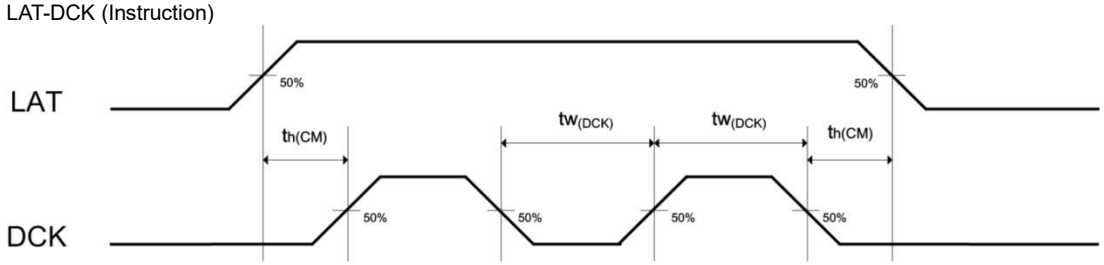
1. DCK-DI, DO



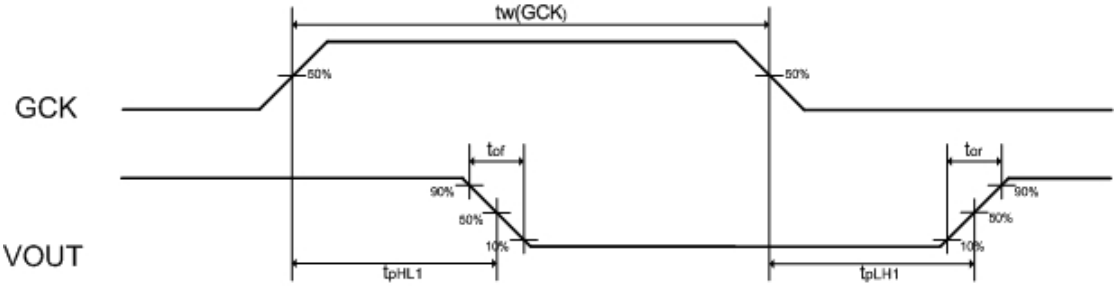
2. DCK-LAT



3. LAT-DCK (Instruction)



4. GCK-VOUT



Typical Performance Characteristics

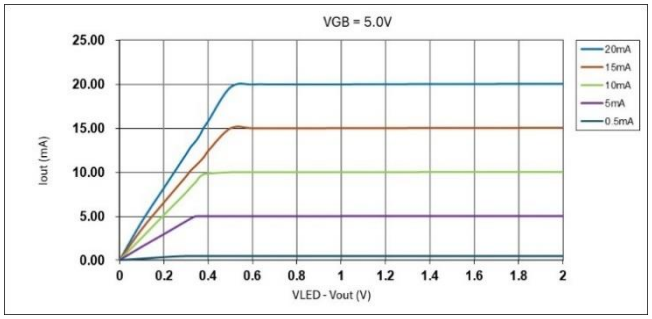


Figure 1. I-V Curve – VGB = 5.0V

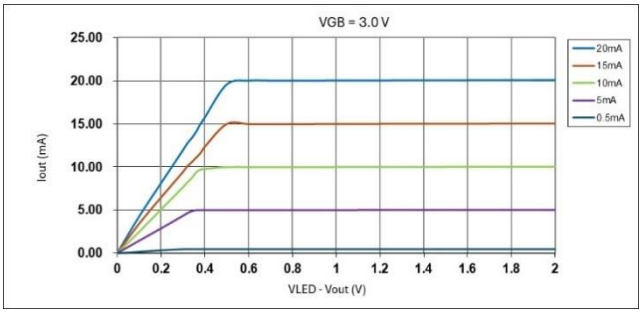


Figure 2. I-V Curve – VGB = 3.0V

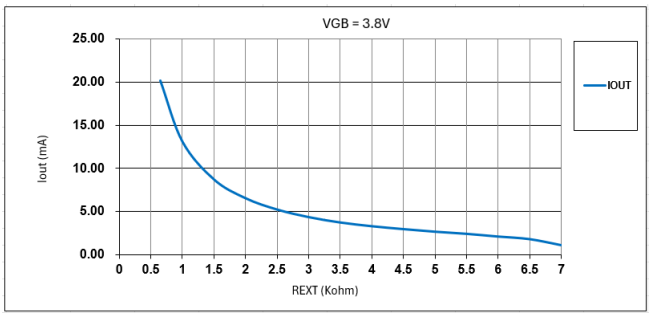


Figure 3. I-R Curve – VGB = 3.8V

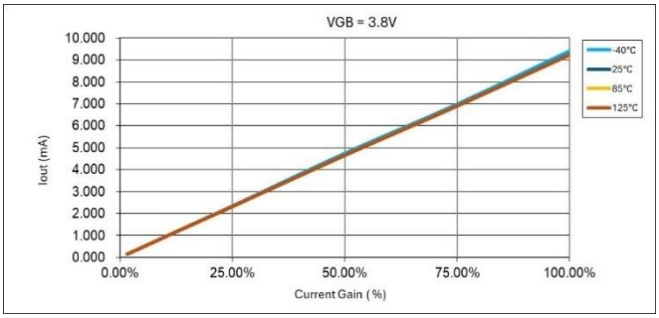


Figure 4. Current Gain Linearity – Rext = 1.4kΩ

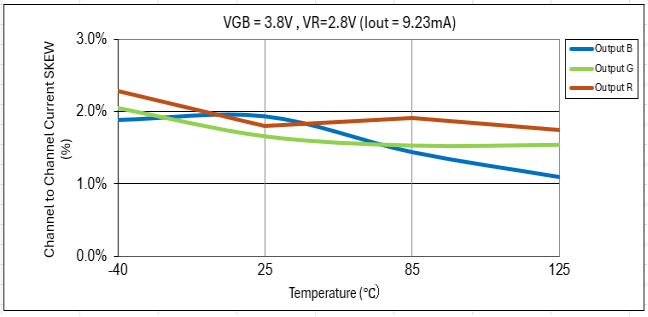


Figure 5. Channel to Channel Skew Across Temperature

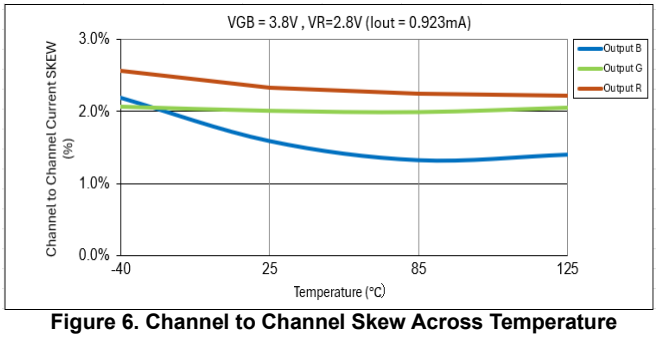


Figure 6. Channel to Channel Skew Across Temperature

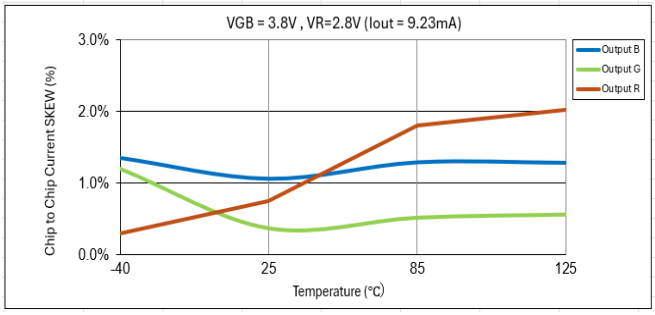


Figure 7. Chip to Chip Skew Across Temperature

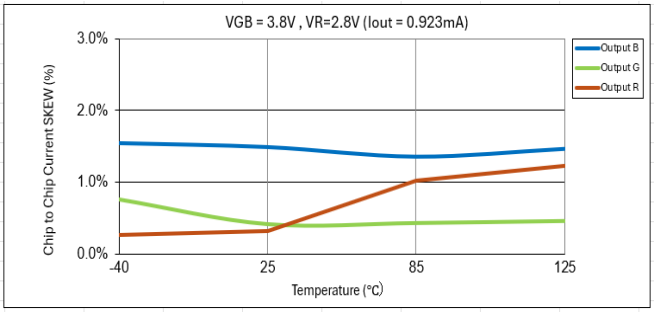


Figure 8. Chip to Chip Skew Across Temperature

Command Table Descriptions

1) R/G/B CMD1 (Command Set 1)

R/G/B CMD1 Bit	Value	Function	Description
R CMD1[14:10]	5'b00000 5'b00001 … 5'b11111	1 scan 2 scan ... 32 scan	Scan Number Selection
R CMD1[4]	1'b0 1'b1	15-bit 16-bit	Grayscale Selection – Default (16-bit)
R CMD1[0]	1'b0 1'b1	Disable Enable	Double Edge GCK Selection – Default (Enable)
G CMD1[15:12]	4'b0000 4'b0001 ... 4'b1111	Mode 0 Mode 1 ... Mode 15	Scan Mode – Default (Mode 0)
B CMD1[3:0]	4'b0000 4'b1111	Enable Disable	GCK Watchdog – Default (Enable)

2) R/G/B CMD2 (Command Set 2)

R/G/B CMD2 Bit	Value	Function	Description
R CMD2[3:2]	2'b00 2'b11	Disable Enable	Open Fail Line – Default (Disable)
R CMD2[1:0]	2'b00 ... 2'b11	0 ... 3	R Open Detection Level – Default (0)
G CMD2[1:0]	2'b00 ... 2'b11	0 ... 3	G Open Detection Level – Default (0)
B CMD2[1:0]	2'b00 ... 2'b11	0 ... 3	B Open Detection Level – Default (0)

3) R/G/B CMD3 (Command Set 3)

R/G/B CMD3 Bit	Value	Function	Description
R/G/B CMD3[13]	1'b0 1'b1	Disable Enable	Sleep Mode – Default (Disable)
R/G/B CMD3[10]	6'b000000 ... 6'b111111	1.56% ... 100%	Current Setting 1 – R/G/B Default (0)
R/G/B CMD3[9:8]	2'b00 ... 2'b11	0 ... 3	Current Setting 2 – R/G/B Default (0)
R/G/B CMD3[5:0]	6'b000000 ... 6'b111111	1.56% ... 100%	Current Gain – Default (001111)

4) R/G/B CMD4 (Command Set 4)

R/G/B CMD4 Bit	Value	Function	Description
R/G/B CMD4[13:12]	2'b00 ... 2'b11	0 ... 3	Current Setting 3 – R Default (0), G Default (1), B Default (2)
R/G/B CMD4[11]	1'b0 1'b1	0 1	Turn On Mode – R/G/B Default (0)
R/G/B CMD4[7:0]	8'b00000000 ... 8'b11111111	0 ... 255	Output Stagger Delay – R Default (6), G Default (3), B Default (0)

Functional Descriptions

Reference Resistor

The constant current values are determined by an external resistor placed between Rext pin and GND pin. The following formula is utilized to calculate the current value:

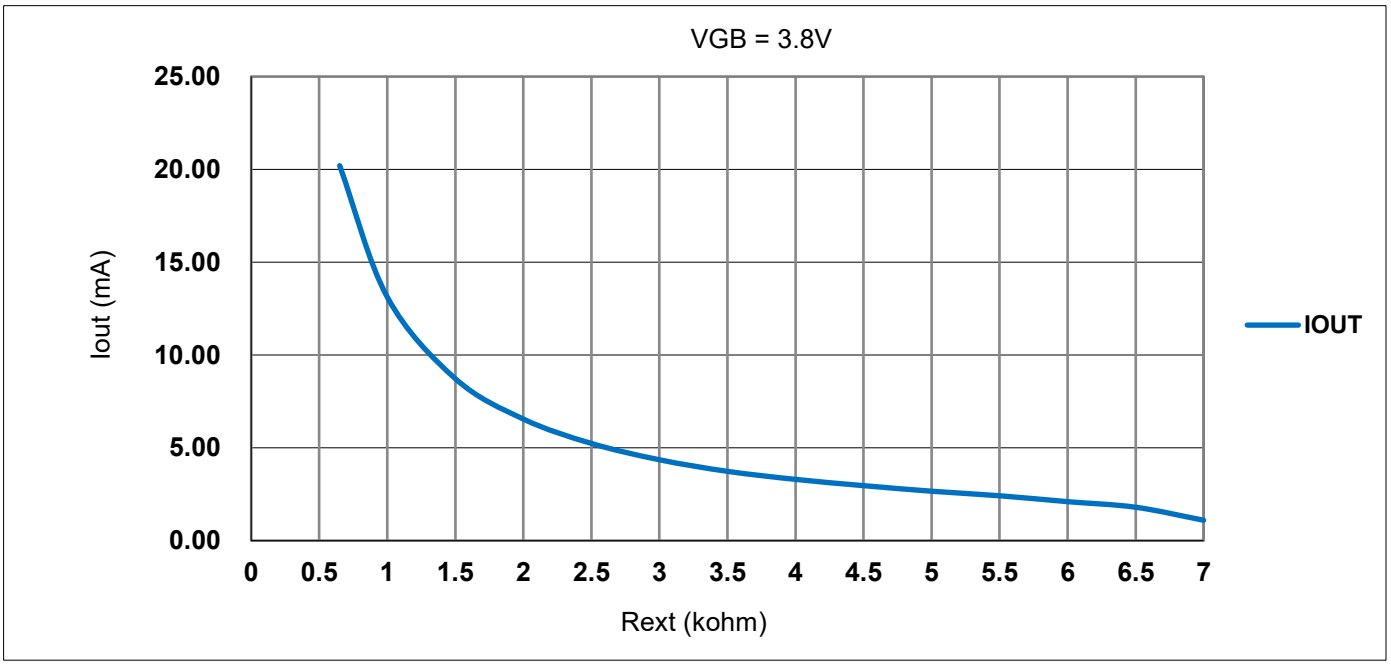
$$\text{Iout (mA)} \approx \frac{13}{\text{Rext (k}\Omega\text{)}} \text{ x Gain}$$

Where Rext is a resistor placed between Rext and GND.
And Gain is the factor of global current control (R/G/B CMD1[5:0]).

Rext range setting:

Rext Range	0.65kΩ ≤ Rext ≤ 2.6kΩ	2.6kΩ ≤ Rext ≤ 6.5kΩ
CMD3[10]	0	1

Application of Iout < 2mA, please use Rext ≤ 6.5kΩ and adjust the Gain value to set the desired output current. For example, when Rext = 6.5kΩ (CMD3[10]=1) and Gain=25%, Iout is around 0.5mA.

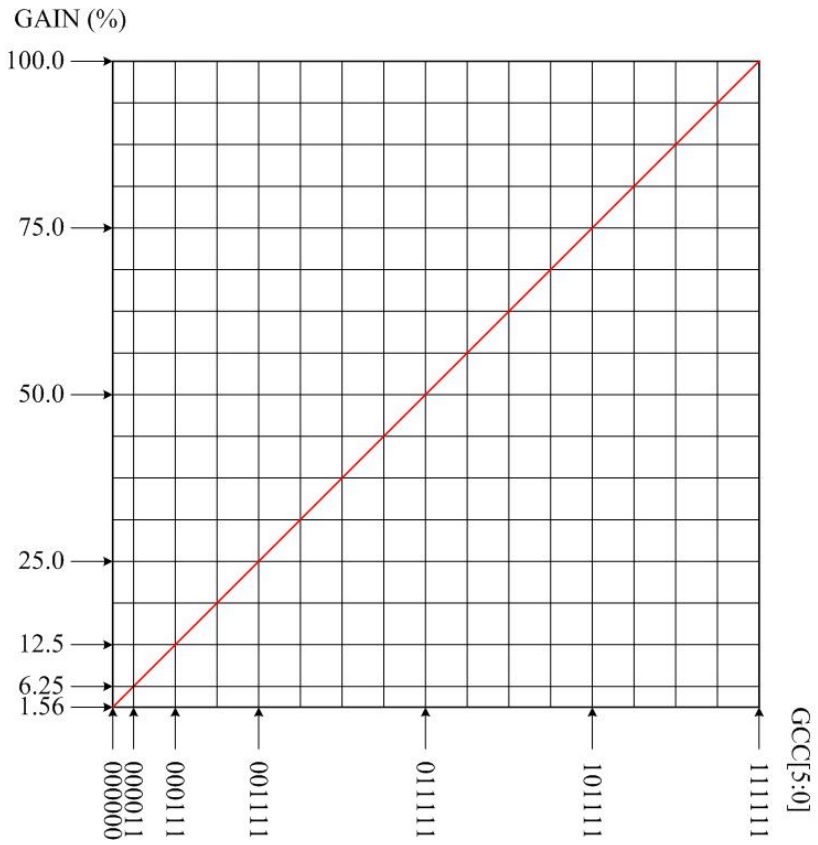


Functional Descriptions (continued)

Global Current Control (Set R/G/B CMD3[5:0])

AL5958 provides the global current control function for each color, users can use 6-bits command data CMD3[5:0] (GCC[5:0]) to adjust the output current. The following formula is utilized to calculate the current value:

GAIN = (GCC[5:0]+1) / 64 (1.56%~100%)



Functional Descriptions (continued)

Built-in Diagnosis Features

The AL5958 has four built-in diagnosis features, once any of the four errors occurred, on-board MCU needs to send command to read out the error and take any necessary action.

1) LED short detection
2) LED open detection
3) Undervoltage lockout (UVLO)
4) GCK (grayscale clock) watchdog

LED Short-Circuit Detection

The AL5958 integrates an LED Short-Circuit Detection for all independent LEDs (pixels). When any single or multiple LEDs shorted, the AL5958 triggered the error flag in the LED short detection (LSD) register. The error flag value=1 means a LED short error. Then the customer's system MCU needs to send error flag read-out command described in the waveform (Figure 10) to read the error flag from the LSD register.

LED Short Detection and Error Flag Read-Out Instruction

The system can perform LED short detection at any time by issuing the commands described in waveform diagram 1, 2, and 3 (Figure 10).

K is the number of devices cascaded, if there are 2 devices cascaded together, then K = 2 in DI and DCK waveforms. After performing LED short detection, send 8 DCKs in LAT=1 to read out the error flag of LSD register from DO-K pin. DO-K pin is the DO pin of Kth device.

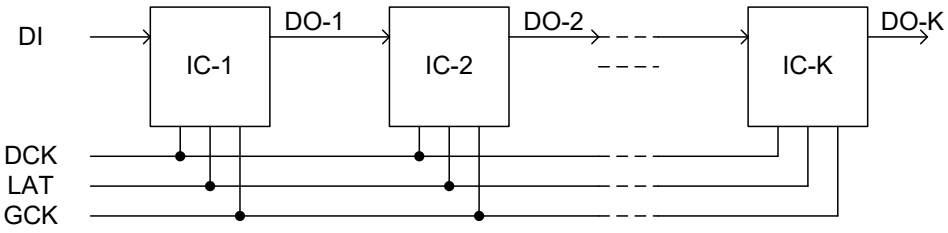


Figure 9. Multiple Devices Cascaded Together

Functional Descriptions (continued)

LED Short Detection and Error Flag Read-Out Instruction (continued)

K= Device cascade number, DCK >2.5MHz

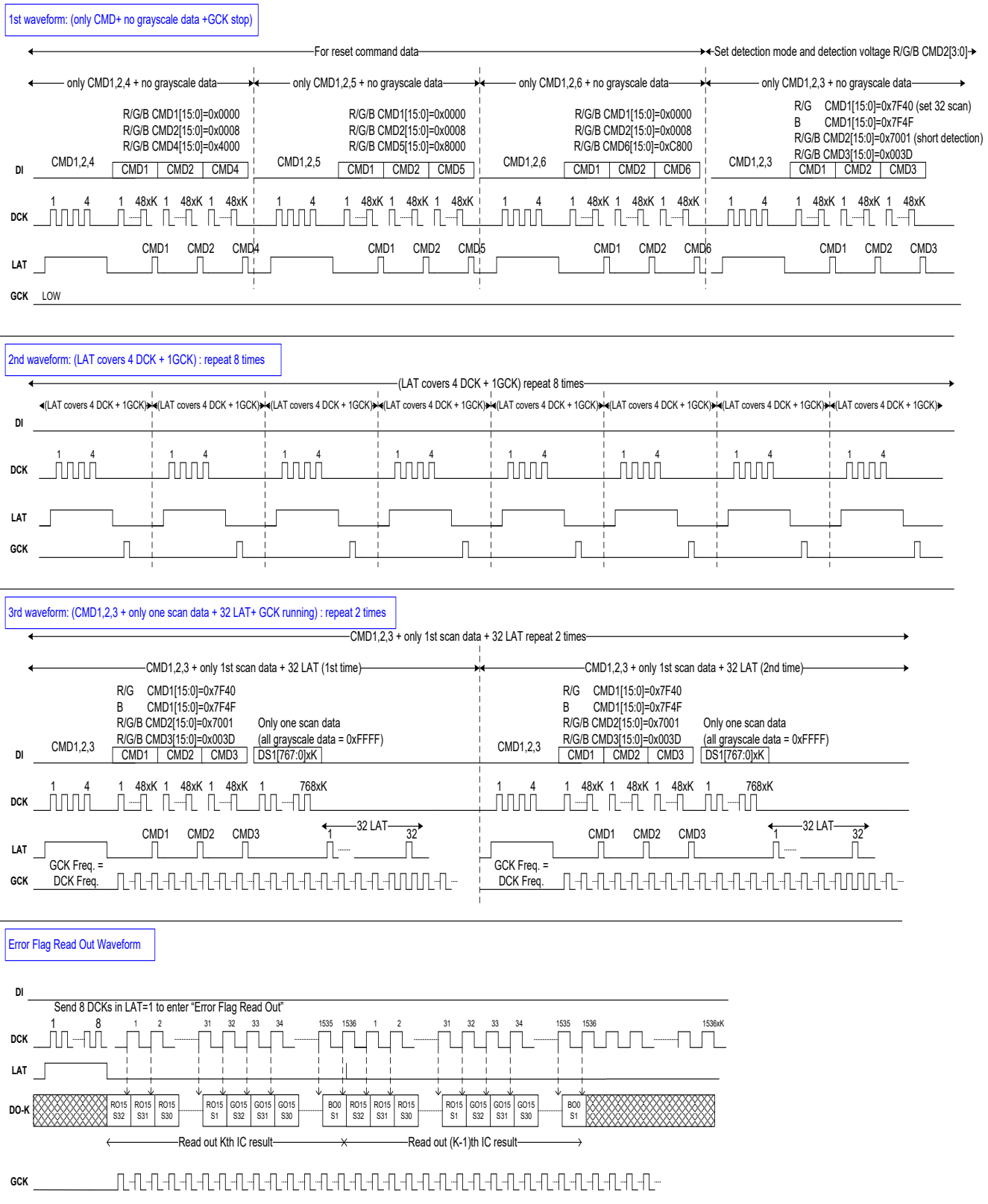


Figure 10. LED Short Detection Waveforms with Commands Instruction

Functional Descriptions (continued)

LED Short Detection and Error Flag Read-Out Instruction (continued)

Error flag read-out description in the do-k waveform above:

Example:

Bit RO15 S32 is the LED error flag of scan 32 of RO15.
Bit RO15 S31 is the LED error flag of scan 31 of RO15.

Each device needs 1536 DCKs to send out all 32 scans and 48 channels error flag, even the real application is not 32 scans. The device needs to meet the LED short detection constraints below when it performs LED short detection:

a. DCK > 2.5MHz
b. Grayscale Clock (GCK) cannot stay HIGH or LOW for more than 1ms because of AL5958's built-in GCK watchdog function.
c. 16-bit Image data must set at 100% LED brightness (D[15:0] = 0XFFFF)
d. R LED Short definition: Vout_R < Vdets_R at turn-on time. Vdets_R is adjustable by RCMD2[1:0].
e. G LED Short definition: Vout_G < Vdets_G at turn-on time. Vdets_G is adjustable by GCMD2[1:0].
f. B LED Short definition: Vout_B < Vdets_B at turn-on time. Vdets_B is adjustable by BCMD2[1:0].

R/G/B CMD2 Bit	Value	Function	Description
R CMD2[3:2]	2'b00	Perform LED **short** detection and the error report can be read out by DO pin after sending "Error Flag Read-Out Waveform".	Error detection mode selection
R CMD2[1:0]	2'b00 2'b01 2'b10 2'b11	0.6V 1.0V 1.4V 1.8V	Short detection threshold voltage of R LED (Vdets_R)
G CMD2[1:0]	2'b00 2'b01 2'b10 2'b11	0.6V 1.0V 1.4V 1.8V	Short detection threshold voltage of G LED (Vdets_G)
B CMD2[1:0]	2'b00 2'b01 2'b10 2'b11	0.6V 1.0V 1.4V 1.8V	Short detection threshold voltage of B LED (Vdets_B)

Functional Descriptions (continued)

LED Open-Circuit Detection

The AL5958 integrates an LED Open-Circuit Detection for all independent LEDs (pixels). When any single or multiple LEDs opened, the AL5958 triggered the error flag in the LED open detection (LOD) register. The error flag value=1 means an LED open error. Then the customer's system MCU needs to send error flag read-out command described in the waveform (Figure 12) to read the error flag from the LOD register.

LED Open Detection and Error Flag Read-Out Instruction

The system can perform LED open detection at any time by issuing the commands described in waveform diagram 1, 2, and 3 (Figure 12).

K is the number of devices cascaded, if there are 2 devices cascaded together, then K = 2 in DI and DCK waveforms. After performing LED open detection, send 8 DCKs in LAT=1 to read out the error flag of LOD register from DO-K pin. DO-K pin is the DO pin of Kth device.

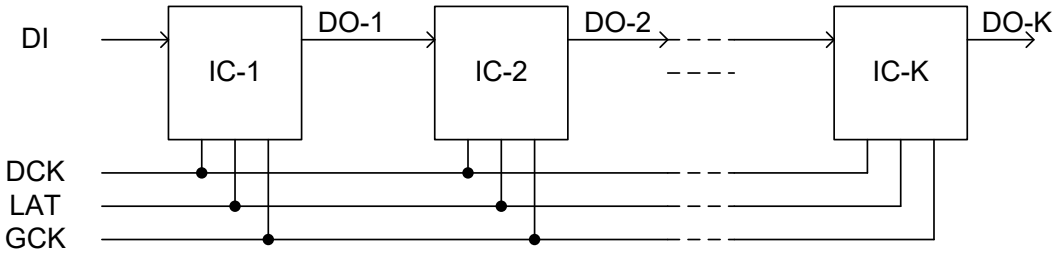


Figure 11. Multiple Devices Cascaded Together

Functional Descriptions (continued)

LED Open Detection and Error Flag Read-Out Instruction (continued)

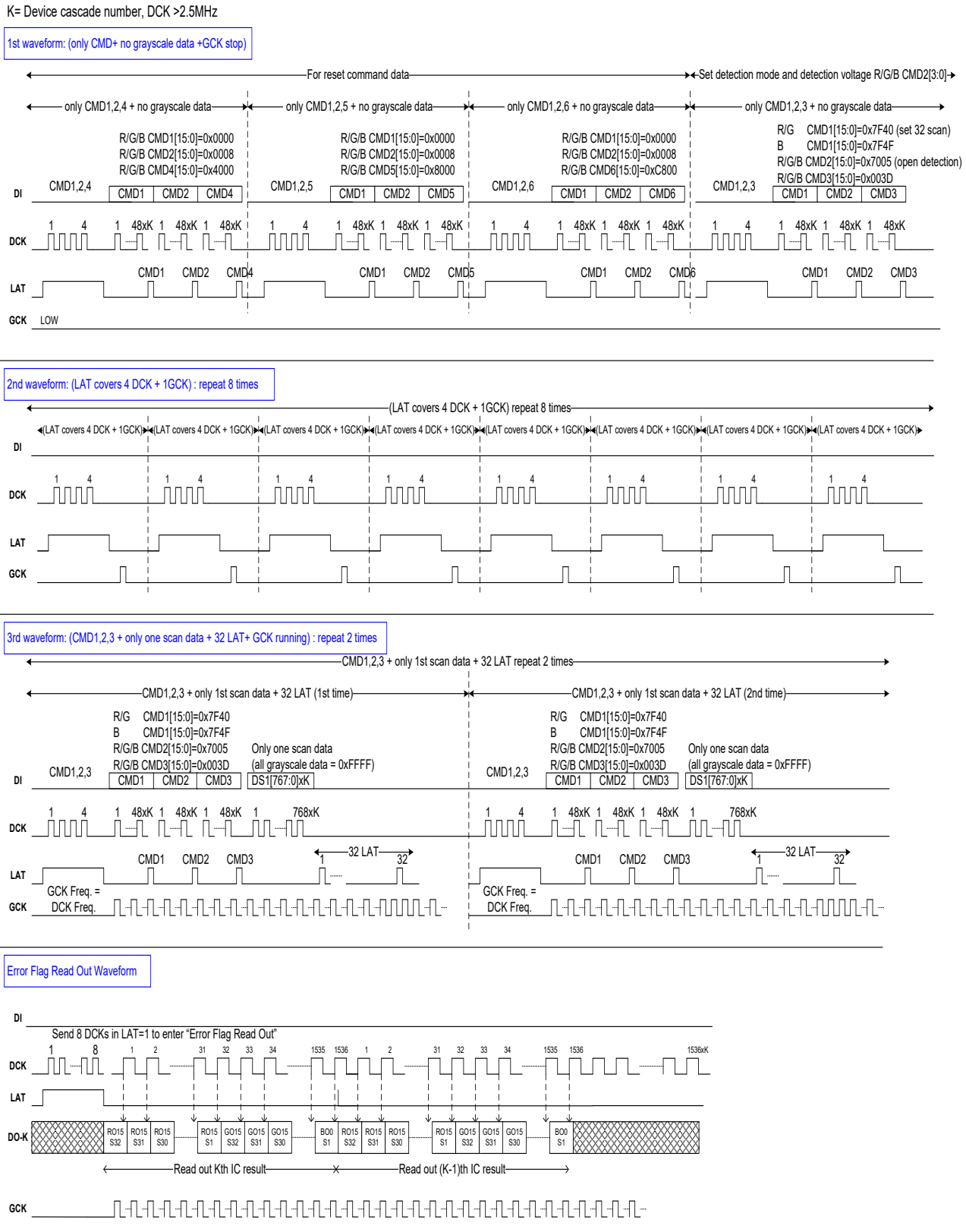


Figure 12. LED Open Detection Waveforms with Commands Instruction

Functional Descriptions (continued)

LED Open Detection and Error Flag Read-Out Instruction (continued)

Error flag read-out description in the DO-K waveform above:

Example:

RO15 and S32 are the LED error flag of scan 32 of RO15.
RO15 and S31 are the LED error flag of scan 31 of RO15.

Each device needs 1536 DCKs to send out all 32 scans and 48 channels error flag, even the real application is not 32 scans. The device needs to meet the LED open detection constraints below when it performs LED open detection:

a. DCK > 2.5MHz
b. Grayscale Clock (GCK) cannot stay HIGH or LOW for more than 1ms because of AL5958's built-in GCK watchdog function.
c. 16-bit Image data must set at 100% LED brightness (D[15:0] = 0XFFFF)
d. R LED Open definition: Vout_R > Vdeto_R at turn-on time. Vdeto_R is adjustable by RCMD2[1:0] to desired voltage level.
e. G LED Open definition: Vout_G > Vdeto_G at turn-on time. Vdeto_G is adjustable by GCMD2[1:0] to desired voltage level.
f. B LED Open definition: Vout_B > Vdeto_B at turn-on time. Vdeto_B is adjustable by BCMD2[1:0] to desired voltage level.

R/G/B CMD2 Bit	Value	Function	Description
R CMD2[3:2]	2'b01	Perform LED **open** detection and the error report can be read out by DO pin after sending "Error Flag Read-Out Waveform".	Error detection mode selection
R CMD2[1:0]	2'b00 2'b01 2'b10 2'b11	VR-0.2V VR-0.3V VR-0.4V VR-0.5V	Open detection threshold voltage of R LED (Vdeto_R)
G CMD2[1:0]	2'b00 2'b01 2'b10 2'b11	VGB-0.2V VGB-0.3V VGB-0.4V VGB-0.5V	Open detection threshold voltage of G LED (Vdeto_G)
B CMD2[1:0]	2'b00 2'b01 2'b10 2'b11	VGB-0.2V VGB-0.3V VGB-0.4V VGB-0.5V	Open detection threshold voltage of B LED (Vdeto_B)

Functional Descriptions (continued)

Undervoltage Lockout

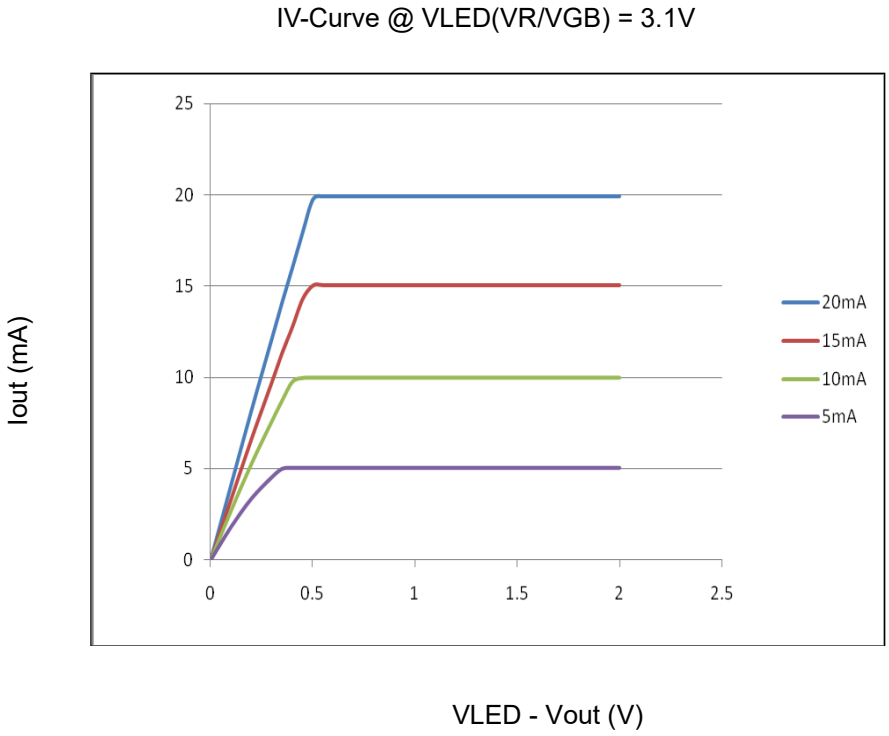
The AL5958 has two power pins VGB and VR, the power supply of digital control circuit is only connected to VGB pin; therefore, only the VGB pin has UVLO function. When VGB < 2.35V, AL5958 will automatic reset. For single color LED application, VGB and VR can be tied together.

Grayscale Clock (GCK) Watchdog Timer

The AL5958 features Grayscale Clock Watchdog Timer. If the Grayscale Clock stays HIGH or LOW for more than 1.4ms, AL5958 will automatically reset.

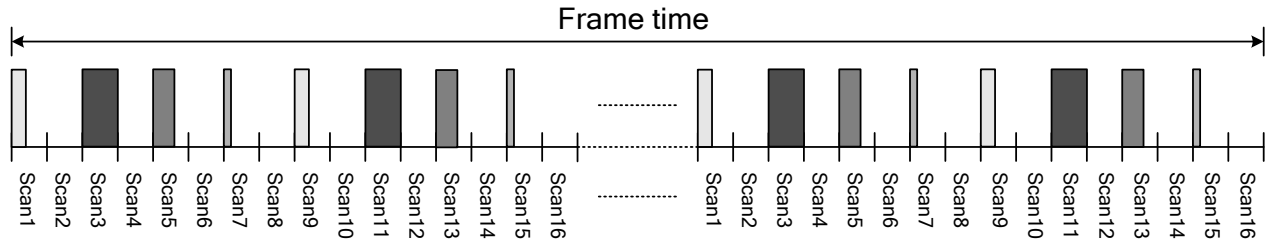
Constant-Current Output

The current characteristics could maintain invariable in the influence of loading voltage. Therefore, the AL5958 could minimize the interference of different LED forward voltages and produce the constant current. The following figures illustrate the suitable output voltage should be determined in order to keep an excellent performance.



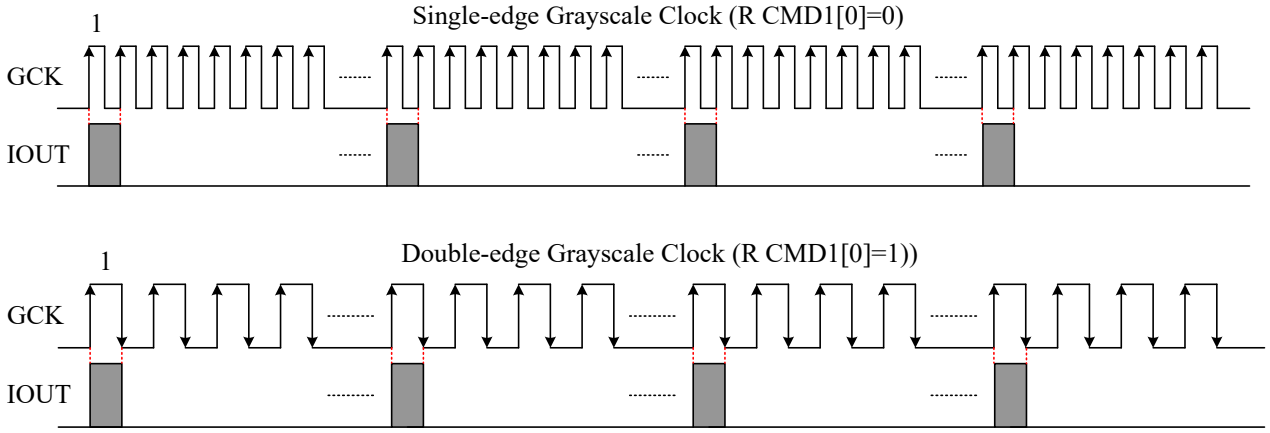
Functional Descriptions (continued)

Multiplex Pulse Density Modulation (Multiplex-PDM)



The advanced Multiplex-PDM approach divides the frame time into the designated segments and interlaces Scan images to enhance the refresh rate. By this technique, the frame refresh rate could be improved efficiently by many times without increasing the frequency of grayscale clock in order to prevent EMI interference.

Grayscale Clock (GCK) Multiplier



AL5958 provides a Grayscale Clock Multiplier function by setting RCMD1[0]. When RCMD1[0]=0, constant current outputs are triggered only at the rising edge of GCKs. When RCMD1[0]=1, constant current outputs are triggered both at the rising edge and falling edge of GCKs. By this approach, the electromagnetic interference would be decreased substantially due to slow grayscale clocks.

Automatic Black Frame Insertion

In the process of scan switching, constant current outputs have to be turned off to avoid that LEDs of the preceding and the present scanning lines are turned on simultaneously. AL5958 supports a specific technique of automatic black frame insertion to solve this problem.

Last Scan Line Ghost Image Abatement

The last scan line ghost image abatment is an optional instruction designed to eliminate ghosting of multiplexed LED modules due to parasitic capacitors on the switching MOS pins.

Functional Descriptions (continued)

Next Scan Line Ghost Image Abatement

The next scan line ghost image abatment is an optional instruction designed to eliminate ghosting of multiplexed LED modules due to parasitic capacitors on the output pins.

Power Dissipation

When one AL5958 is operating, the practical power dissipation can be determined by the following equation:

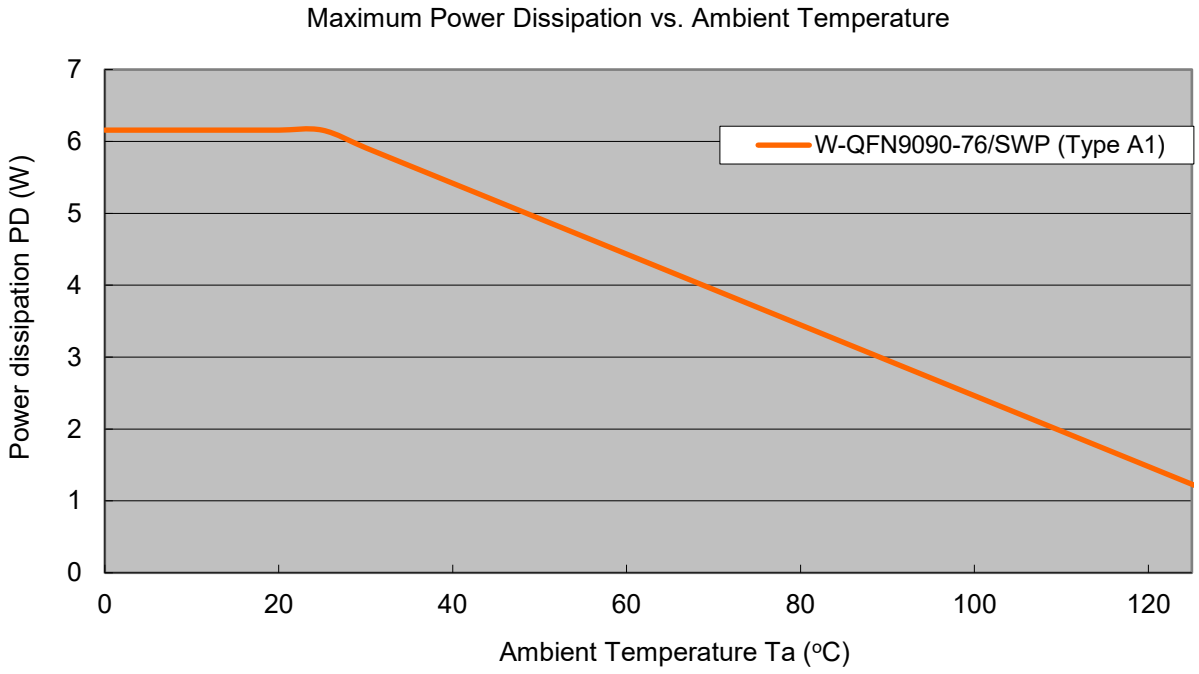
PD = (VR - Vf_RLED) * Iout_R * 16 * turn-on time efficiency
+ (VGB - Vf_GLED) * Iout_G * 16 * turn-on time efficiency
+ (VGB - Vf_BLED) * Iout_B * 16 * turn-on time efficiency
+ VR * IVR_all + VGB * IVGB_all
+ [(Iout_R + Iout_G + Iout_B) * K]^2 * 0.4 * turn-on time efficiency

(K = the RGB pixel number connected to one MOS)
(IVR_all / IVGB_all means the static + dynamic supply current of VR / VGB, not only the static supply current.)

In secure operating conditions, the power consumption of an integrated chip should be less than the maximum permissible power dissipation which is determined by the package types and ambient temperature. The formula for maximum power dissipation is described as follows:

$$PD\ (max) = \frac{Tj(max)(^{\circ}C) - Ta(^{\circ}C)}{Rth(j\text{-}a)(^{\circ}C/Watt)}$$

The PD (max) declines as the ambient temperature raises. Therefore, suitable operating conditions should be designed with caution according to the chosen package and the ambient temperature. The following figure illustrates the relation between the maximum power dissipation and the ambient temperature.

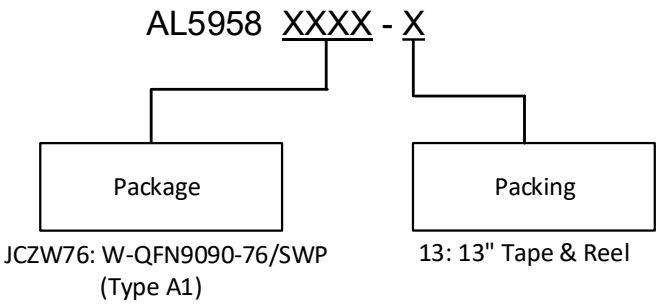


Design Tools – from Diodes Website https://www.diodes.com/design/tools/

- AL5958 Demo Board
- Demo Board Gerber File and User Guide

Evaluation Boards

Ordering Information



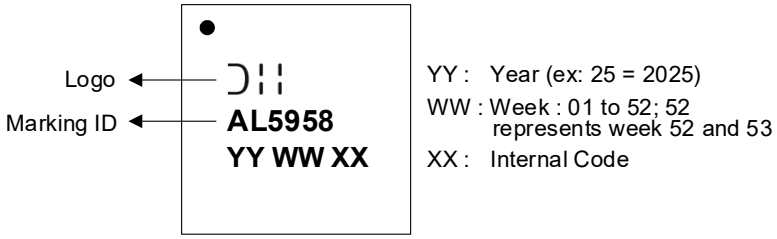
Orderable Part Number	Package Code	Package (Note 12)	Packing	
			Qty.	Carrier
AL5958JCZW76-13	JCZW76	W-QFN9090-76/SWP (Type A1)	2500	13” Tape & Reel

Note: 12. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

W-QFN9090-76/SWP (Type A1)

(Top View)



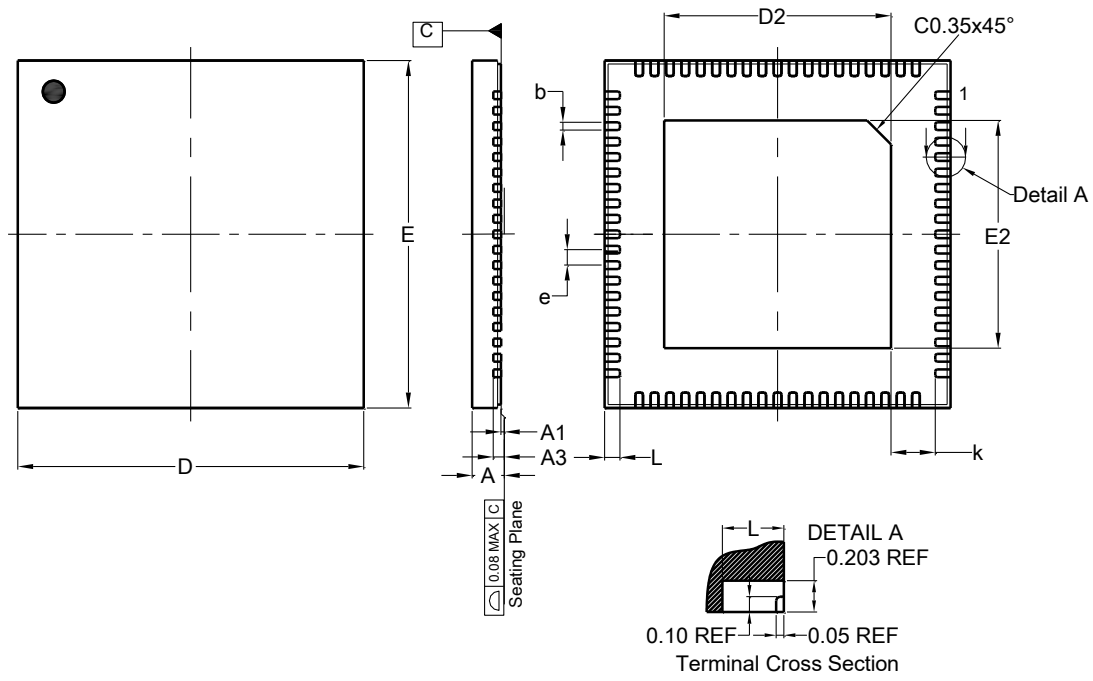
Tape and Reel Information

Please see https://www.diodes.com/assets/Packaging-Support-Docs/AP02007.pdf for tape and reel details.

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN9090-76/SWP (Type A1)

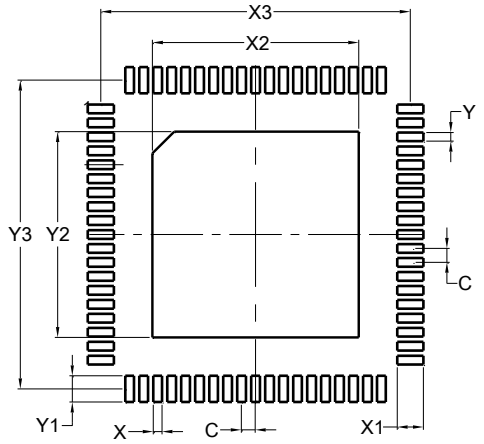


W-QFN9090-76/SWP (Type A1)			
Dim	Min	Max	Typ
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.15	0.25	0.20
D	8.90	9.10	9.00
D2	5.80	6.00	5.90
E	8.90	9.10	9.00
E2	5.80	6.00	5.90
e	0.40 BSC		
k	1.15 REF		
L	0.30	0.50	0.40
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN9090-76/SWP (Type A1)



Dimensions	Value (in mm)
C	0.400
X	0.250
X1	0.750
X2	5.900
X3	8.850
Y	0.250
Y1	0.750
Y2	5.900
Y3	8.850

Mechanical Data

- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish - Matte Tin Plated Leads, Solderable per JESD22-B102 e3
- Weight: 0.183 grams (Approximate)

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