

FIGURE LIST

INSTRUCTION

FIGURE

INSTRUCTION

FIGURE

ACIL✓	4-12	- PDX✓	33-82
ADD✓	3-80	PLT✓	31-78
ALS✓	46-108	PXA✓	34-84
ANA✓	22-60	PXD✓	34-84
ARS✓	47-110	RCT	61-130
- AXT✓	35-86	RPM	53-120
CAL✓	1-6	RQL✓	48-112
CAP✓	2-8	SAC-	21-58
CAS✓	23-62	SLP-	16-46
CCS✓	19-54	SLW	15-44
CHS✓	26-68	SPM	52-118
CLA✓	1-6	SSP✓	26-68
CLS✓	1-6	STA✓	17-48
COM✓	25-64	STD✓	17-48
DCT✓	29-14	STL✓	17-48
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DFDP	14-38	STQ-	15-44
DFMP	13-24	STR	58-126
DFSB	12-30	STZ-	15-44
DVP✓	8-20	SUB-	3-80
ENB	60-129	SWT-	30-76
ENK✓	6-18	- SXA✓	18-52
ETTA	54-22	SXD✓	18-52
FAD✓	9-22	TCOA	56-124
FDP✓	11-28	TDOA	56-124
FMP✓	10-20	TEFA	57-125
FSB✓	9-22	TIX-	37-40
HPRI✓	50-15	TMI	41-98
ICT	61-130	TMT✓	51-116
IOT	55-23	TNX✓	37-96
LAC✓	32-80	TNZ✓	40-16
LAS✓	24-104	TOV✓	42-100
LBT✓	28-72	TPL✓	41-98
- LDC	32-86	- TRA✓	43-102
LDQ✓	5-14	TRCA	57-125
LGL✓	44-104	TRP	59-128
LGR✓	45-106	TRT	59-128
LLS✓	44-104	TSL-	17-48
LRS✓	45-106	TSX✓	39-44
LXA✓	32-80	TXH✓	38-92
LXD✓	32-80	TXI✓	36-88
MIT✓	31-78	TXL✓	38-92
MPY✓	7-18	- TZE✓	40-96
MSM✓	27-76	UFA✓	9-22
MSP✓	27-76	UFM✓	10-26
ORA✓	20-56	UFS✓	9-22
PAC✓	33-82	CDP	8-20
PAX✓	33-82	VLM-	7-18
PBT✓	28-72	VMA-	7-18
PCS✓	20-56	XEC✓	49-114
PDC✓	33-82		

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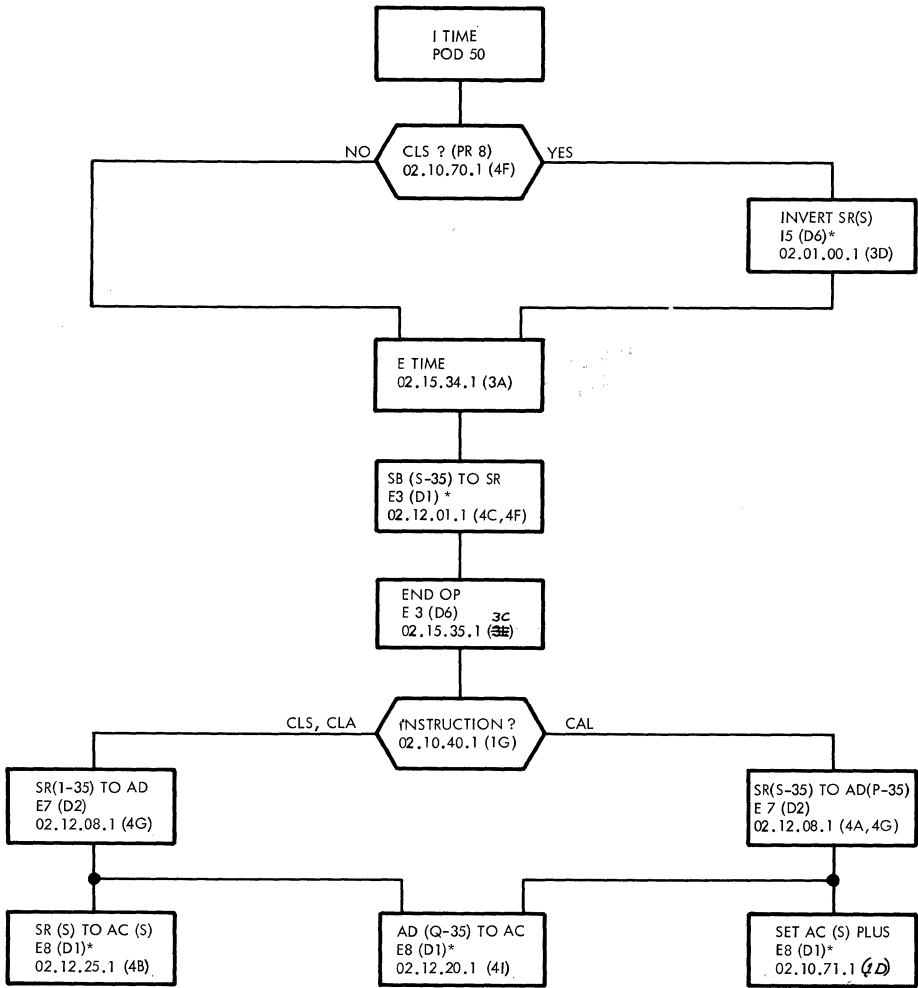
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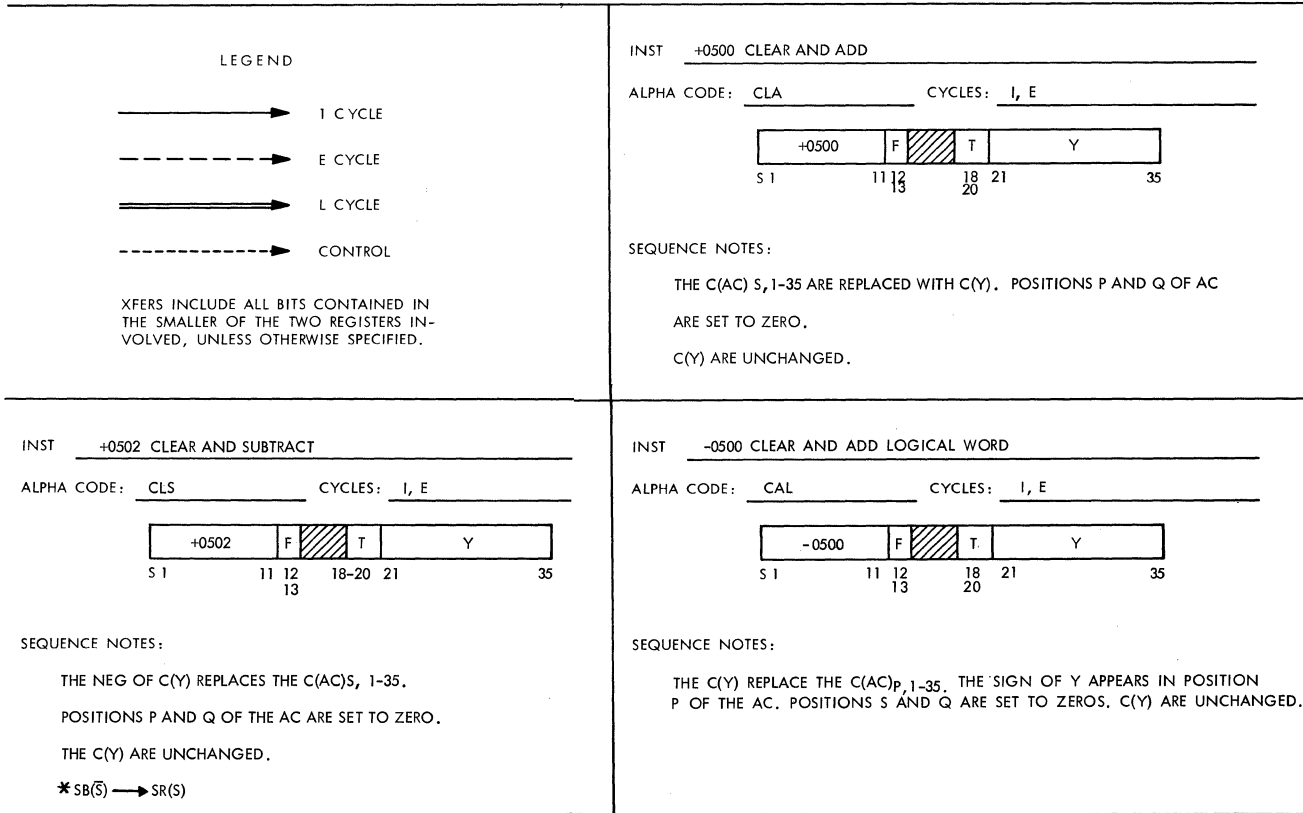
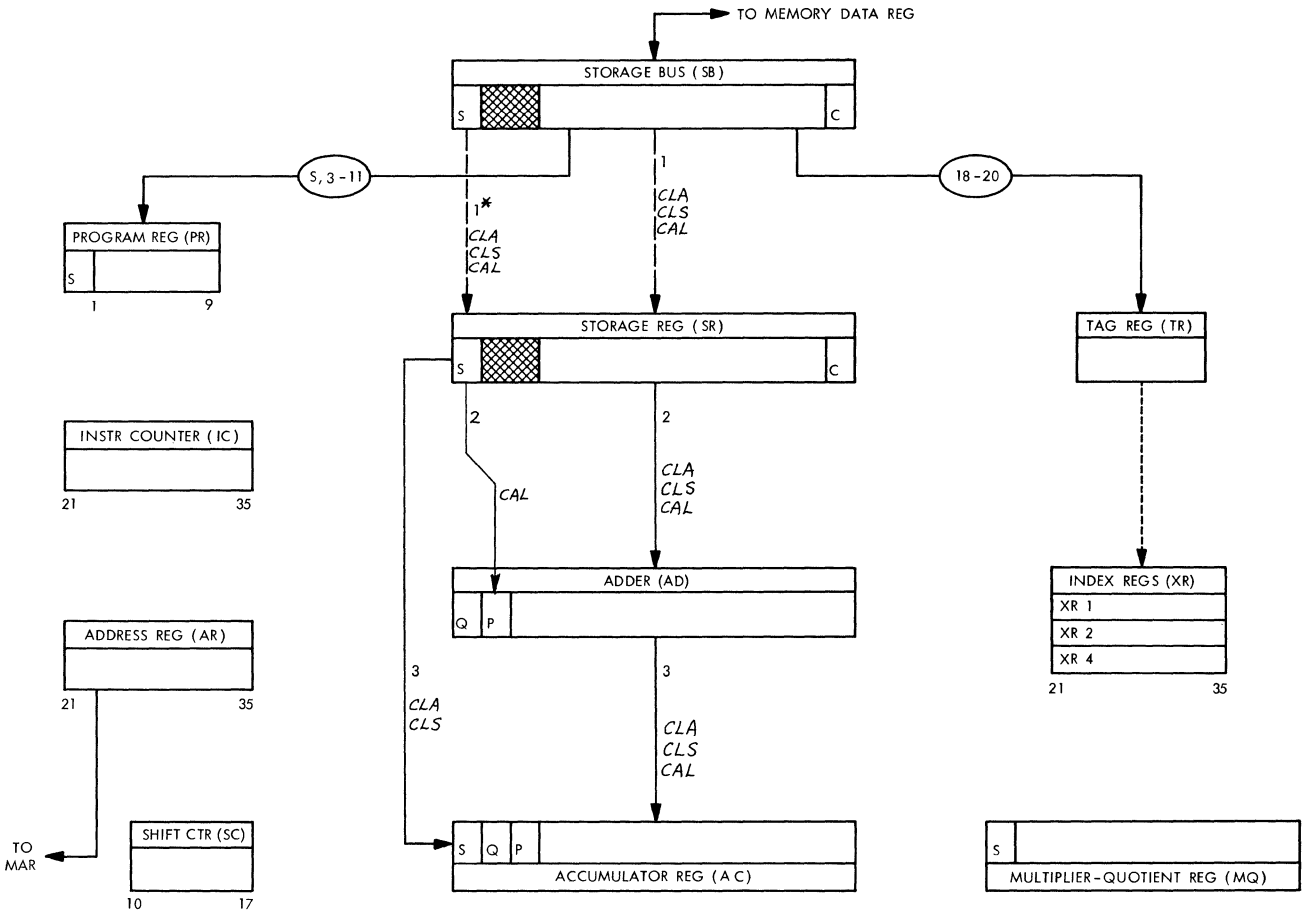
Clear and Add (CLA+0500)
Replaces the contents of the accumulator (S, 1-35) with the contents of the effective address. Bit positions P and Q of the accumulator are set to 0. The contents of memory are unchanged.

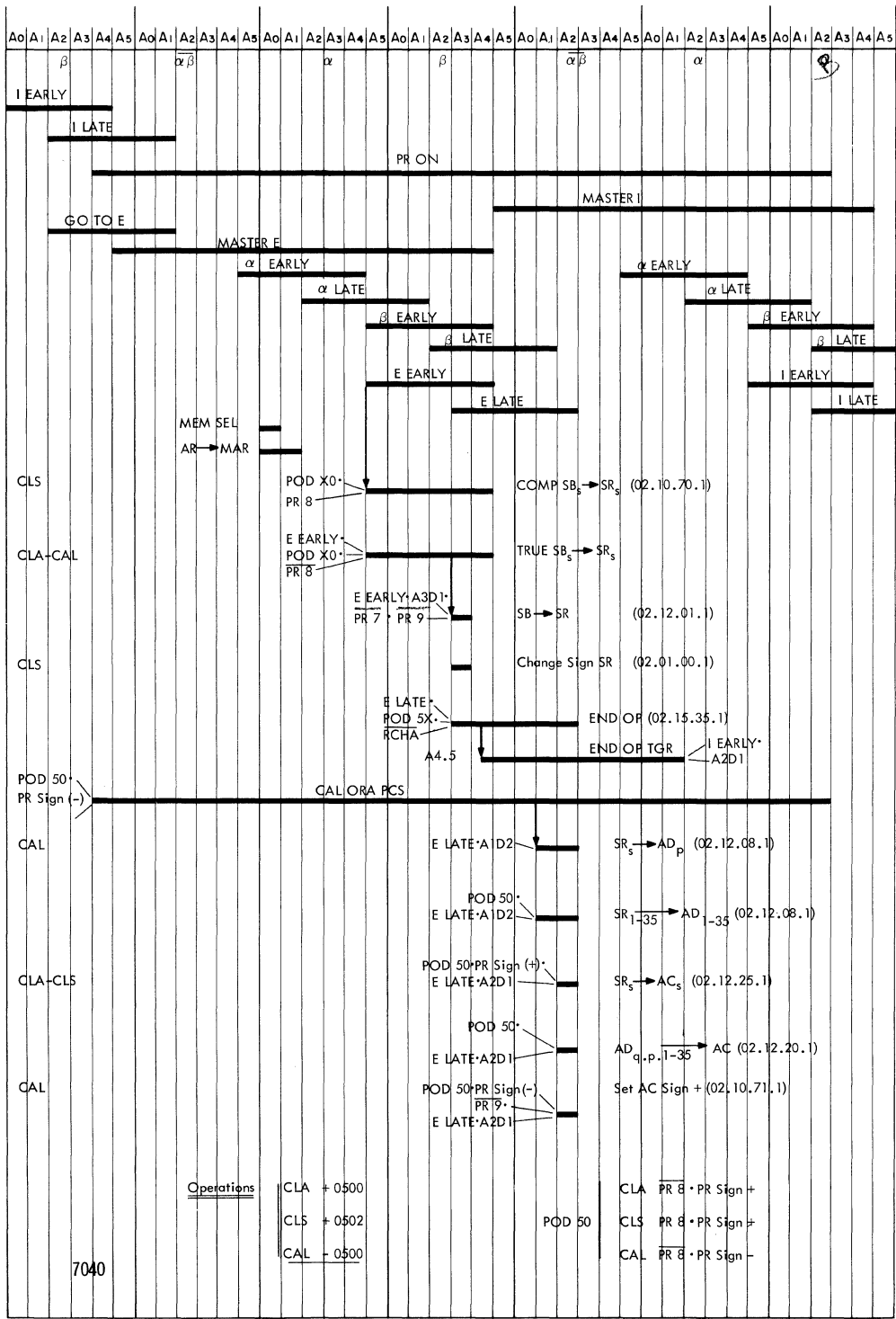
Clear and Subtract (CLS+0502)
Replaces the contents of the accumulator (S, 1-35) with the negative of the contents of the effective address. P and Q of the accumulator are set to 0. The contents of memory are unchanged.

Clear and Add Logical Word (CAL-0500)
Replaces the contents of the accumulator (P, 1-35) with the contents of the effective address. The sign of the memory word goes to bit P of the accumulator. Bits S and Q of the accumulator are set to 0's. The contents of memory are unchanged.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER.





Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	CLA		00006	050000 000006
00002	TRA		00000	002000 000000
00003	Pattern			777777 777777
00004	Pattern			000000 000000
00005				
00006				

Location Switches	Inst	Tag	Address	Octal Equiv.
00000	CLS		00005	050200 000005
00001	CLS		00006	050200 000006
00002	TRA		00000	002000 000000
00003	Pattern			777777 777777
00004	Pattern			000000 000000
00005				
00006				

Location Switches	Inst	Tag	Address	Octal Equiv.
00000	CAL		00005	450000 000005
00001	CAL		00006	450000 000006
00002	TRA		00000	002000 000000
00003	Pattern			070707 070707
00004	Pattern			707070 707070
00005				
00006				

Clear and Add (CLA)										
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	ACCUMULATOR (Q, P)	TALLY COUNTER
I	E	00001	+500	000	0	00005	0500000000005	0000000000000	00	
E	I	00001	+500	000	0	00001	7777777777777	7777777777777	00	
I	E	00002	+500	000	0	00006	0500000000006	7777777777777	00	
E	I	00002	+500	000	0	00002	0000000000000	0000000000000	00	
I	I	00003	+020	000	0	00000	0020000000000	0000000000000	00	

Clear and Subtract (CLS)										
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	ACCUMULATOR (Q, P)	TALLY COUNTER
I	E	00001	+502	000	0	00005	0502000000005	0000000000000	00	
E	I	00001	+502	000	0	00001	3777777777777	3777777777777	00	
I	E	00002	+502	000	0	00006	0502000000006	3777777777777	00	
E	I	00002	+502	000	0	00002	4000000000000	4000000000000	00	
I	I	00003	+020	000	0	00000	0020000000000	4000000000000	00	
I	E	00001	+502	000	0	00005	0502000000005	4000000000000	00	

Clear and Add Logical Word (CAL)										
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	ACCUMULATOR (Q, P)	TALLY COUNTER
I	E	00001	-500	000	0	00005	4500000000005	0000000000000	00	
E	I	00001	-500	000	0	00001	0707070707070	0707070707070	00	
I	E	00002	-500	000	0	00006	4500000000006	0707070707070	00	
E	I	00002	-500	000	0	00002	7070707070707	3070707070707	01	
I	I	00003	+020	000	0	00000	0020000000000	3070707070707	01	
I	E	00001	-500	000	0	00005	4500000000005	3070707070707	01	

Clear and Add Logical Word with Parity (CAP -1510)
Replaces the contents of bits S, P, 1-35 of the accumulator with bits C, S, 1-35 of the effective address. The sign of the memory location and the parity bit go to bits P and S, respectively, of the accumulator. Accumulator Q is reset to 0. The contents of the effective address are not checked for parity and do not cause a parity trap request. The contents of memory are unchanged.

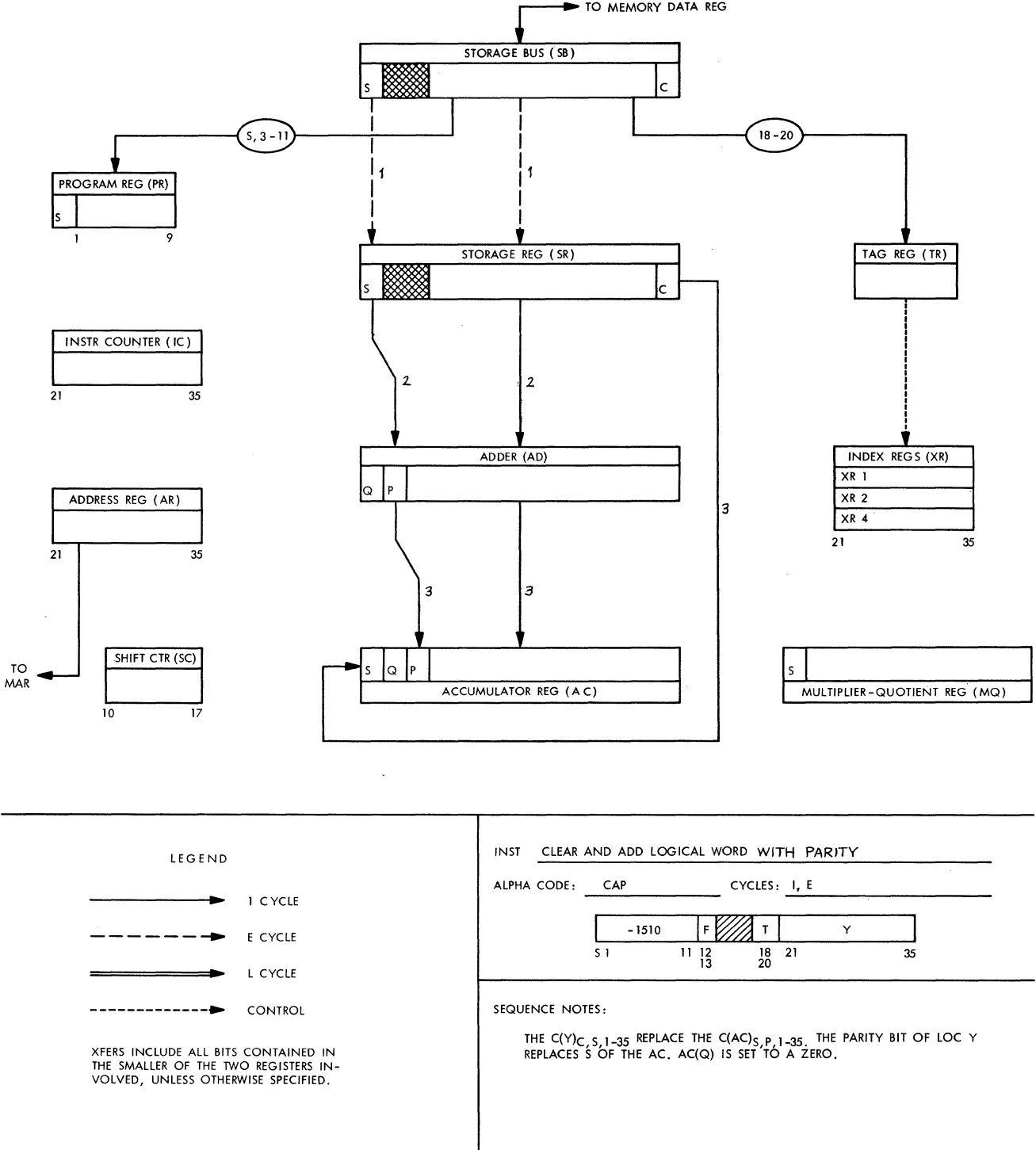
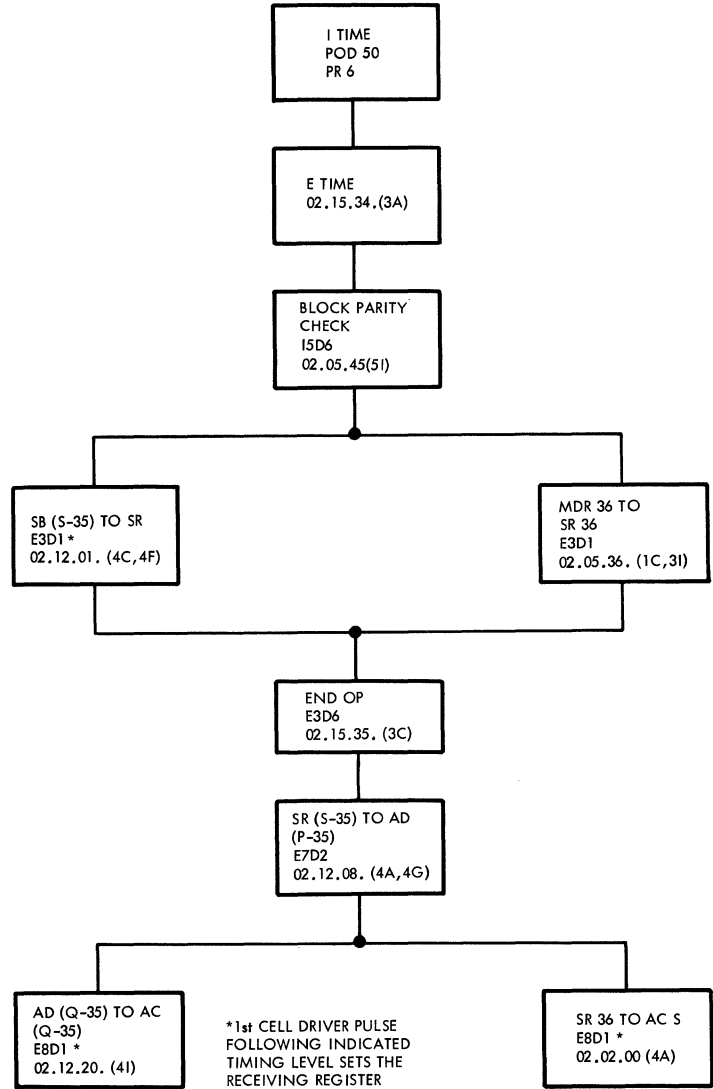
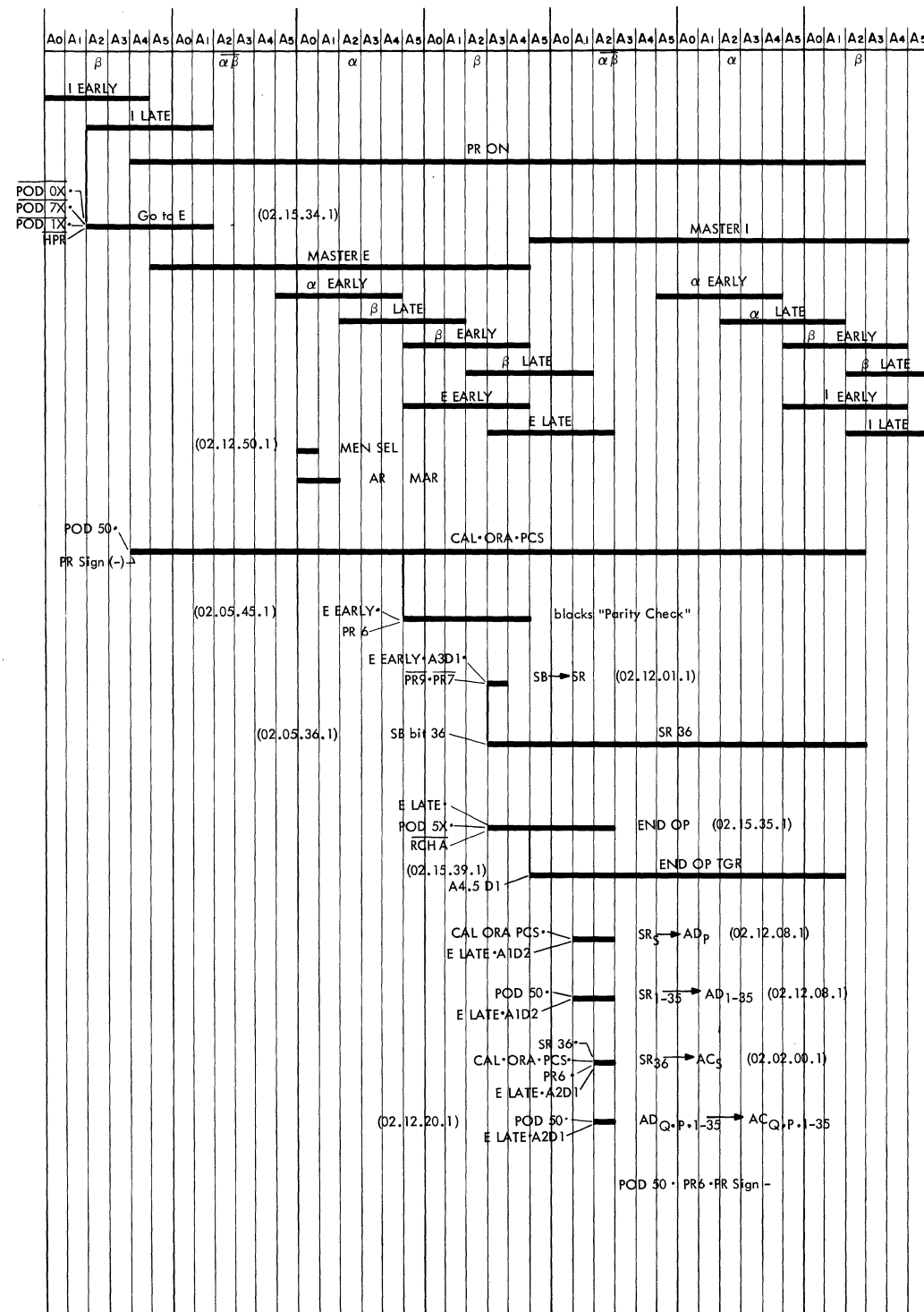
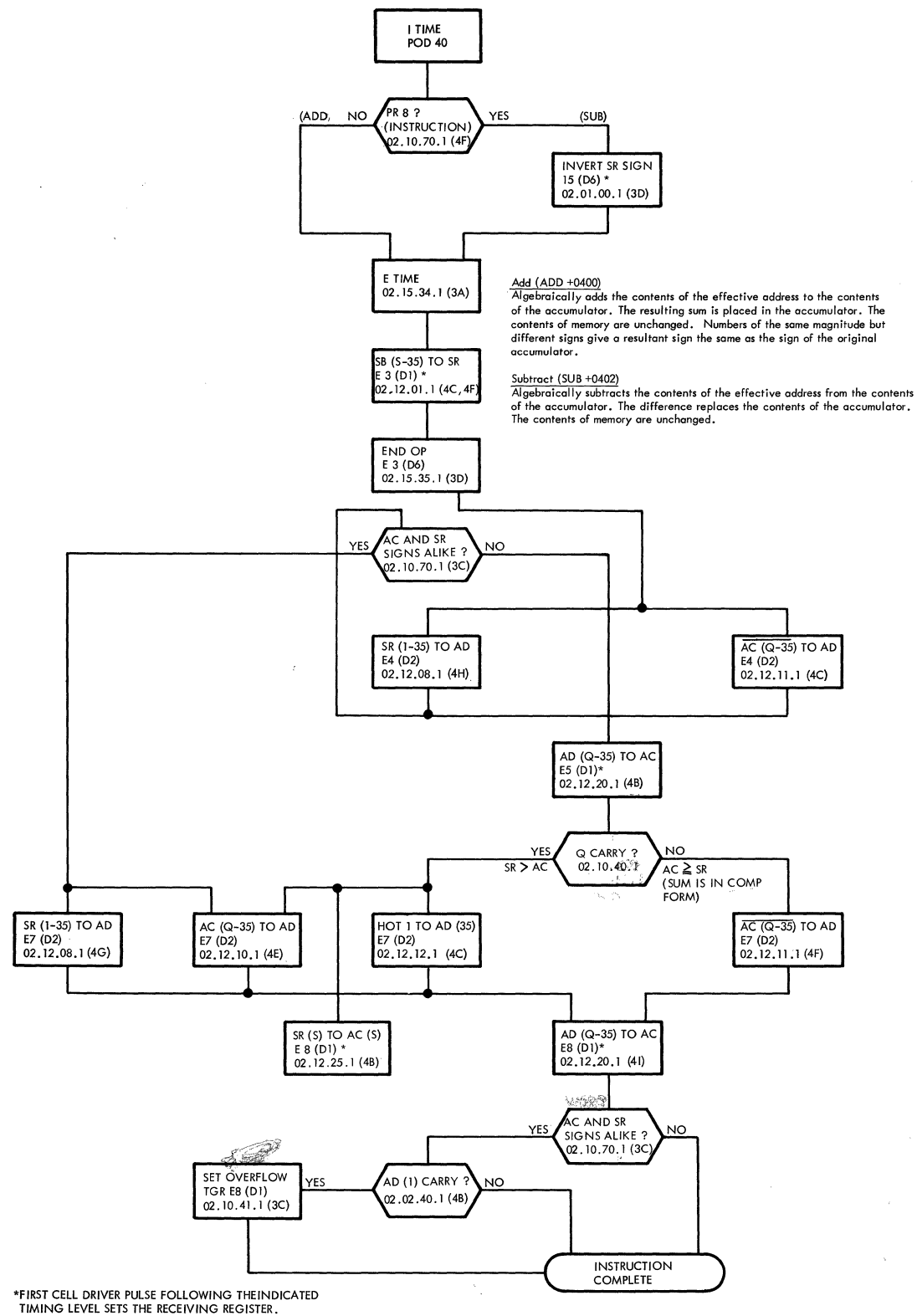


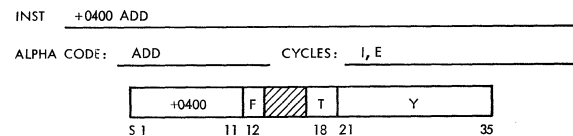
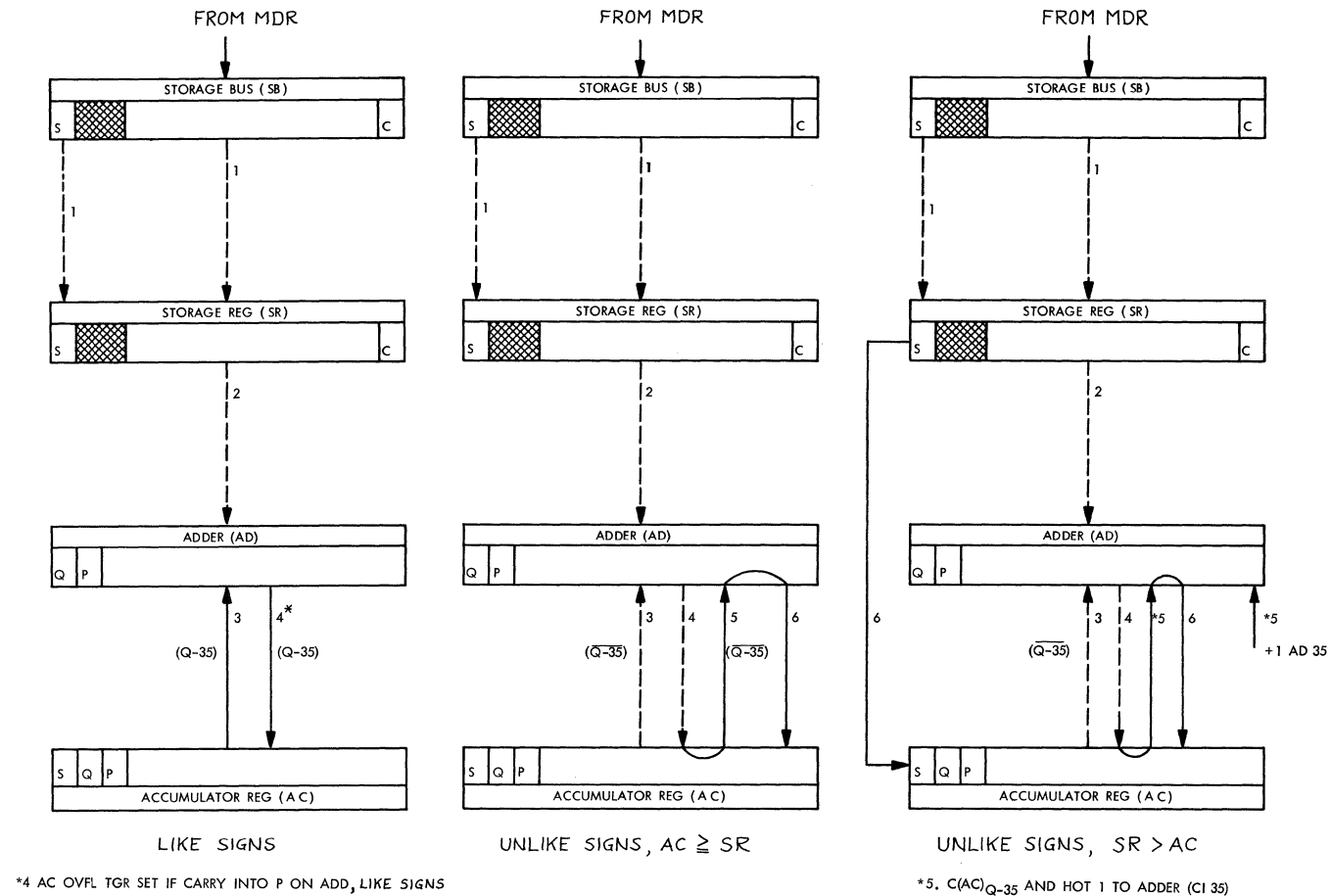
FIGURE 2. CAP





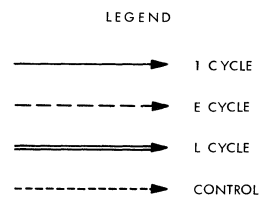
*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER.

FIGURE 3. ADD, SUB

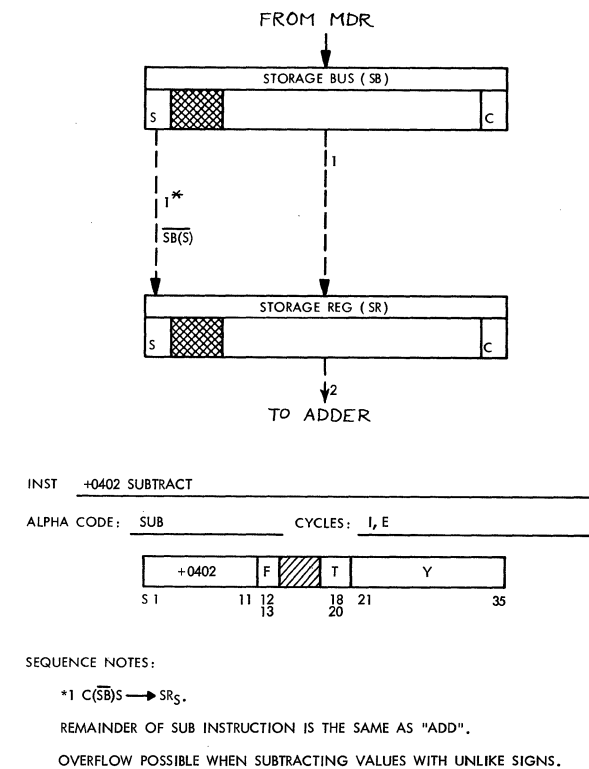


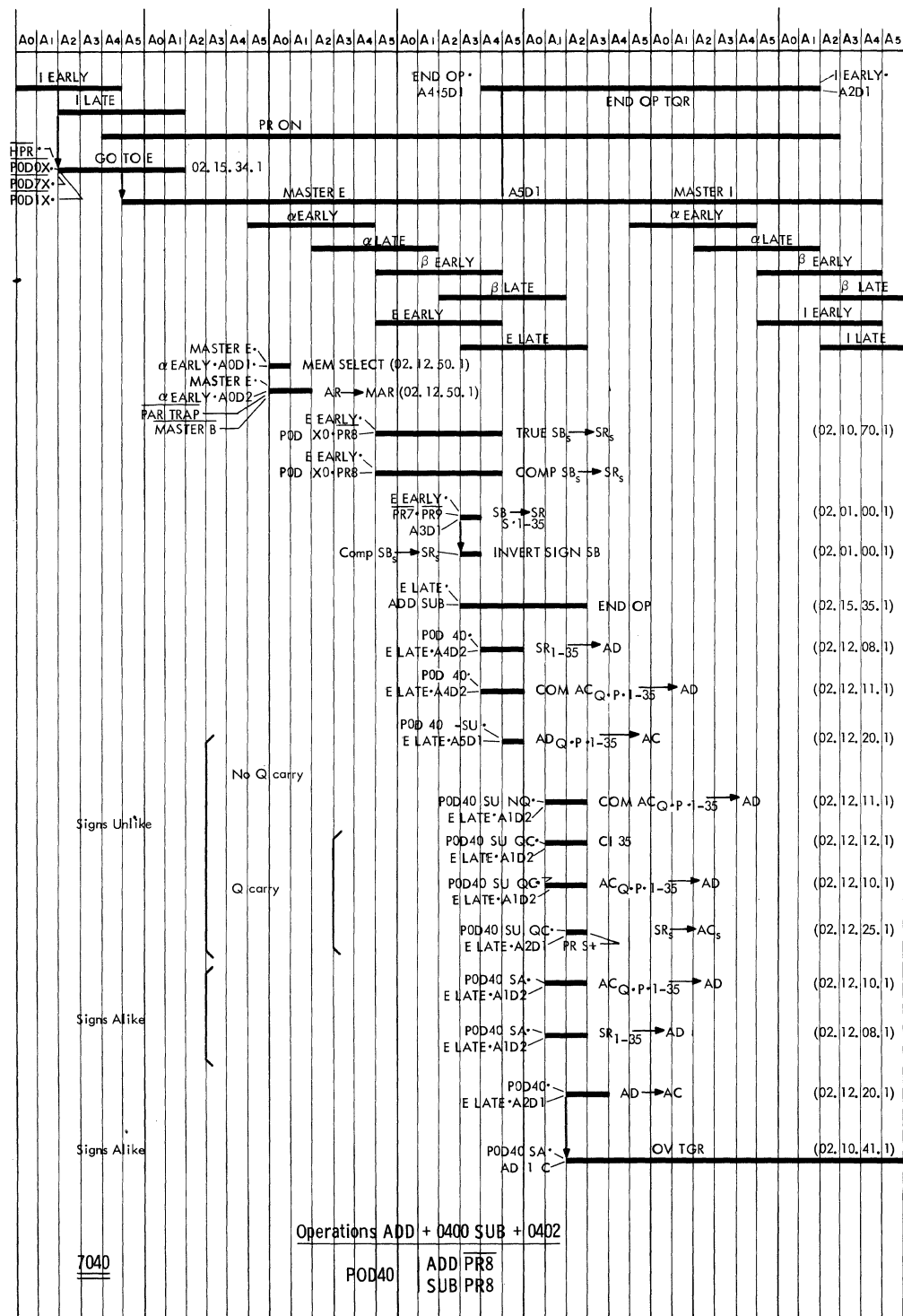
SEQUENCE NOTES:

THE C(Y) ARE ALGEBRAICALLY ADDED TO C(AC). THE RESULTING SUM IS PLACED IN THE AC. C(Y) ARE UNCHANGED. NUMBERS OF THE SAME MAGNITUDE BUT DIFFERENT SIGNS GIVE RESULTANT SIGN OF THE ORIGINAL AC.



XFRS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.





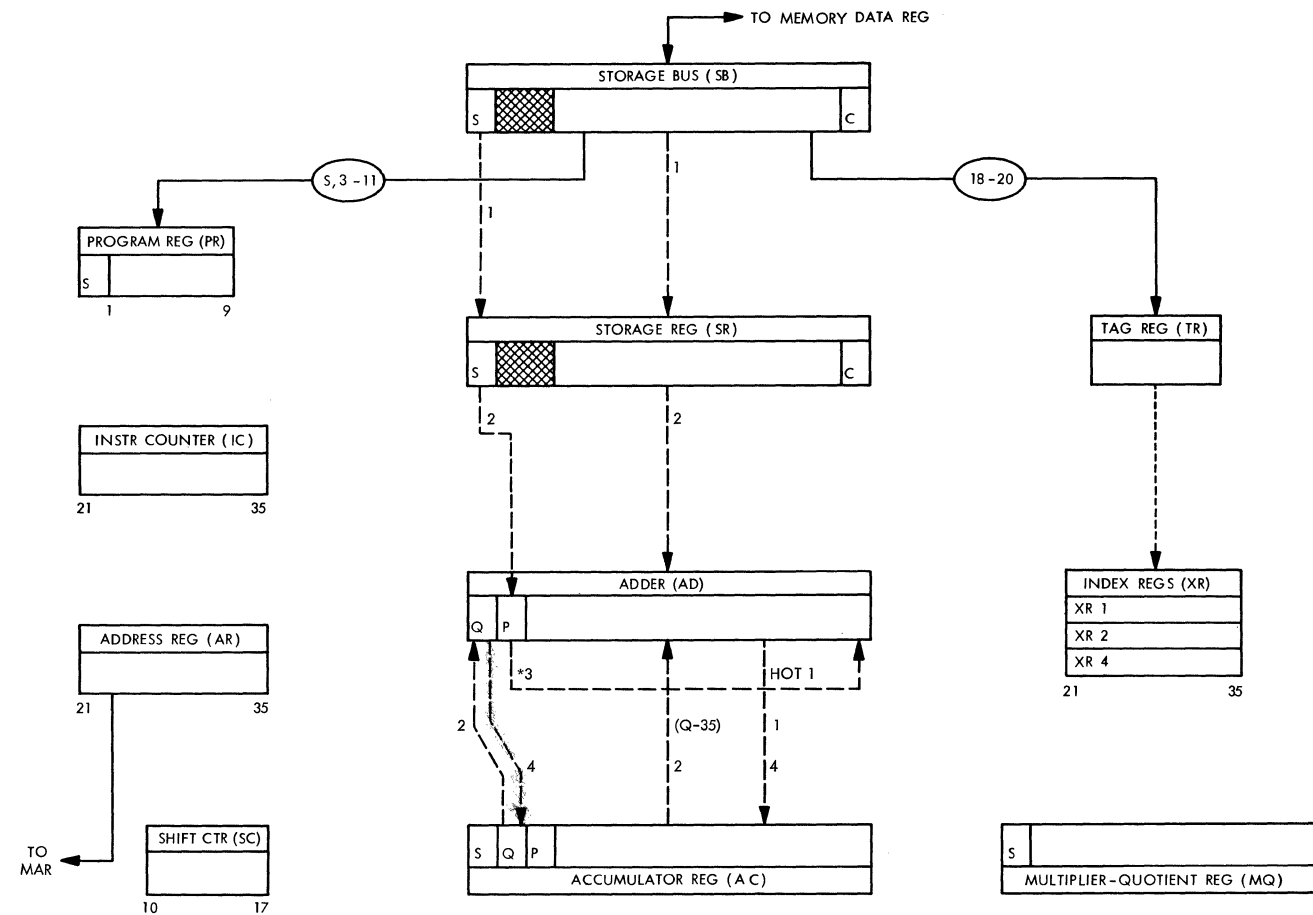
Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	ADD		00006	040000 000006
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			000000 000001
00006	Pattern			377777 777777

Add (ADD)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY
I	E	00001	+500	000	0	00005	0500000000005	0000000000000	00						
E	I	00001	+500	000	0	00001	0000000000001	0000000000001	00						
I	E	00002	+400	000	0	00006	0400000000006	0000000000001	00						
E	I	00002	+400	000	0	00002	3777777777777	0000000000000	01				1	1	1
I	I	00003	+020	000	0	00000	0020000000000	0000000000000	01				1	0	0
I	E	00001	+500	000	0	00005	0500000000005	0000000000000	01				1		
E	I	00001	+500	000	0	00001	0000000000001	0000000000000	00				1		
I	E	00002	+400	000	0	00006	0400000000006	0000000000000	00				1		

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	SUB		00006	040200 000006
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			000000 000001
00006	Pattern			377777 777777

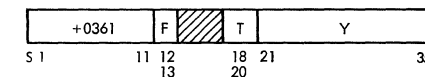
Subtract (SUB)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY
I	E	00001	+500	000	0	00005	0500000000005	0000000000000	00						
E	I	00001	+500	000	0	00001	0000000000001	0000000000001	00						
I	E	00002	+402	000	0	00006	0402000000006	0000000000001	00						
E	I	00002	+402	000	0	00002	7777777777777	7777777777776	00				1	1	1
I	I	00003	+020	000	0	00000	0020000000000	7777777777776	00				0	0	0
I	E	00001	+500	000	0	00005	0500000000005	7777777777776	00				0	0	0

* FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER.



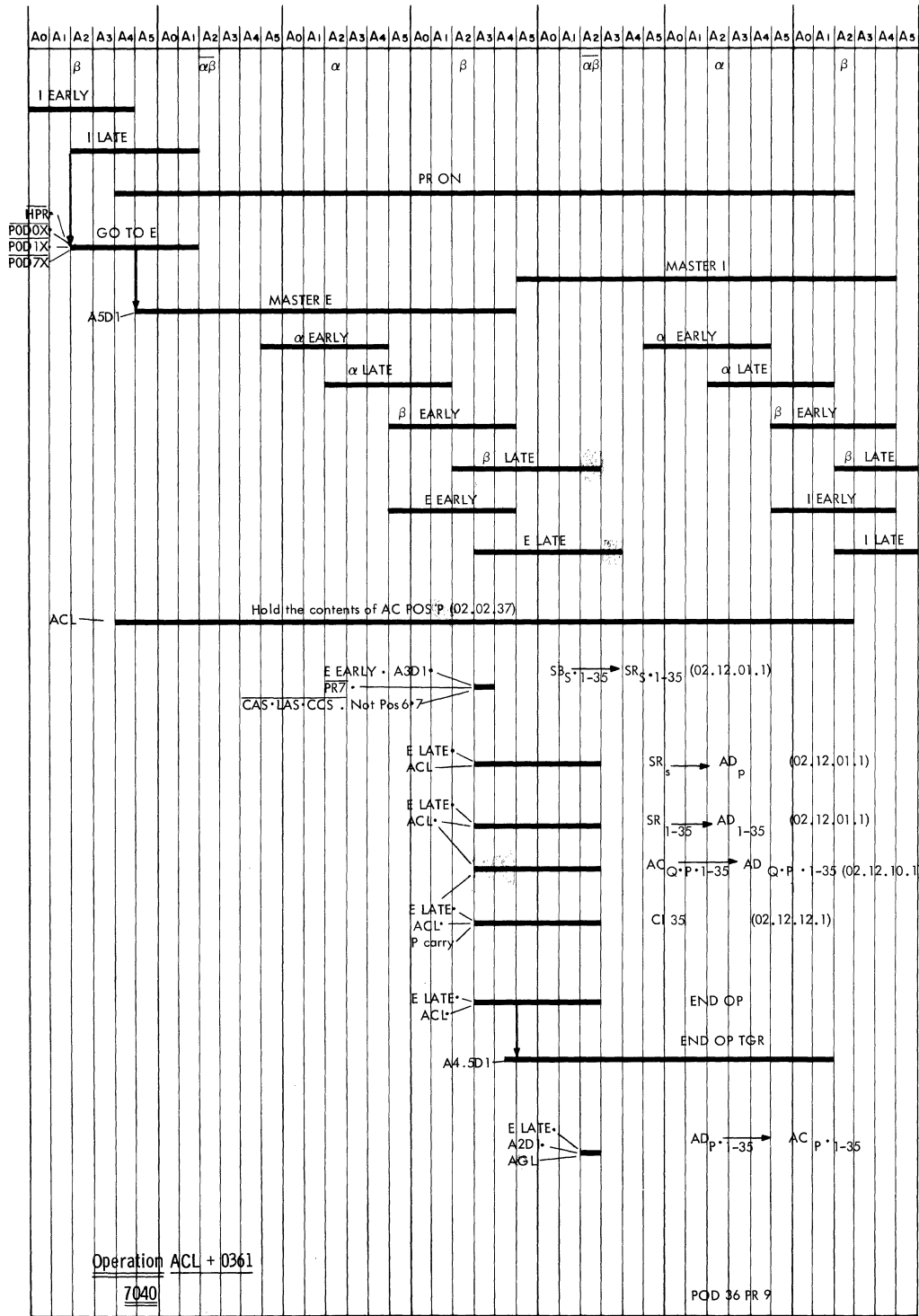
 1 CYCLE
 E CYCLE
 L CYCLE
 CONTROL

ALPHA CODE: ACL CYCLES:



* 3 P CARRY $\rightarrow$ CI 35.

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Location Switches	Inst	Tag	Address	Octal Equiv.
00000	CAL		00005	450000 000005
00001	ACL		00006	036100 000006
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			525252 525252
00006	Pattern			252525 252525

Add and Carry Logical Word (ACL)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, L, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK
I	E	00001	-500	000	0	00005	4500000000005	0000000000000	00						
E	I	00001	-500	000	0	00001	52525252525252	12525252525252	01						
I	E	00002	+361	000	0	00006	0361000000006	12525252525252	01						
E	I	00002	+361	000	0	00002	25252525252525	37777777777777	01						
I	I	00003	+020	000	0	00000	0020000000000	37777777777777	01						
I	E	00001	-500	000	0	00005	4500000000005	37777777777777	01						

Load MQ (LDQ +0560)
The contents of the specified memory location to the MQ register (S,1-35).
The contents of memory are unchanged.

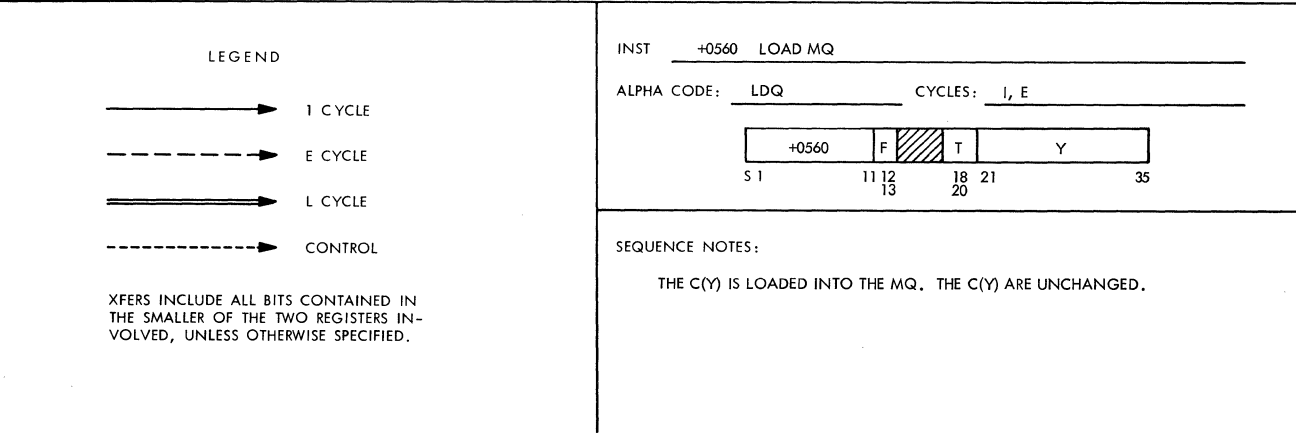
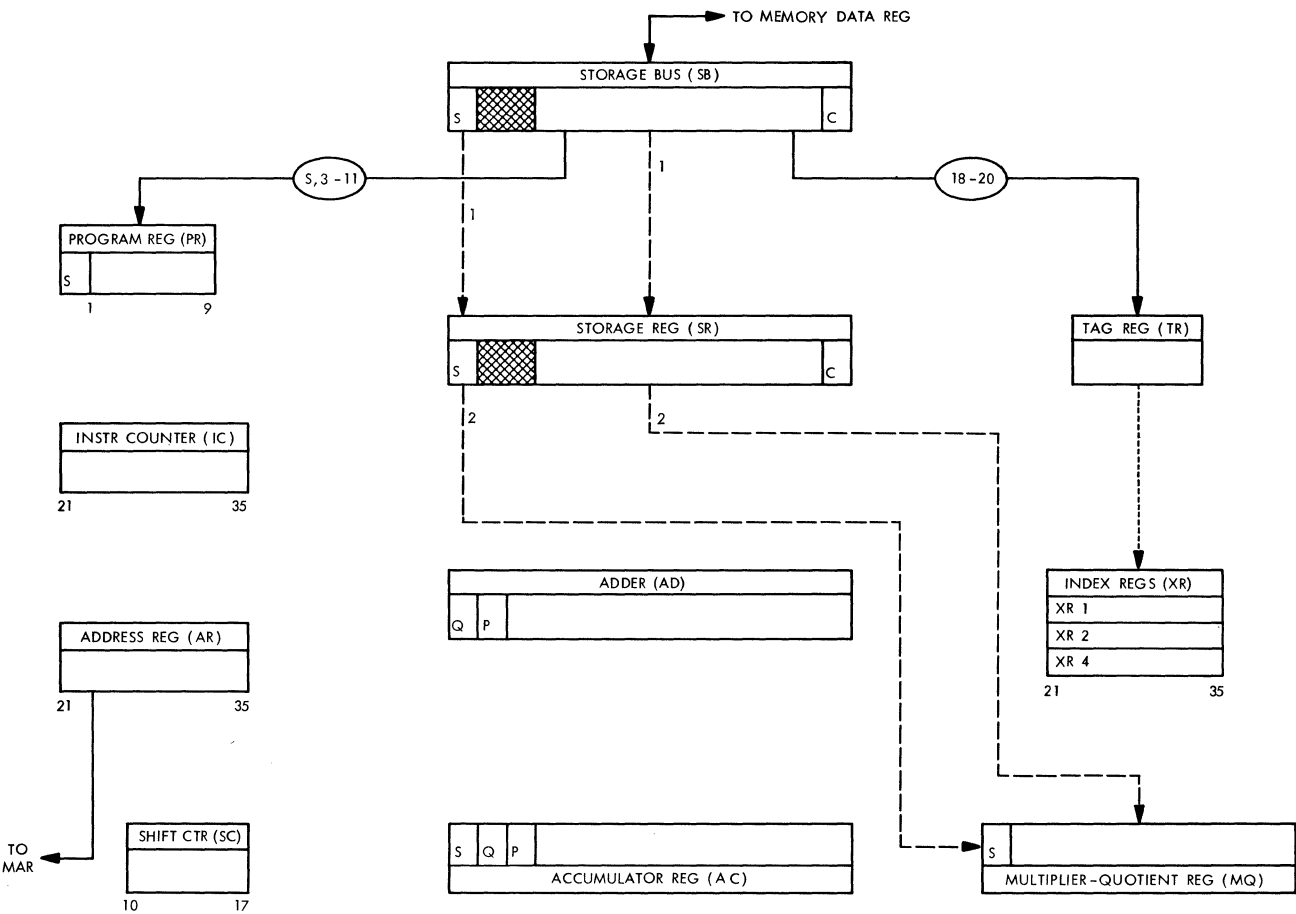
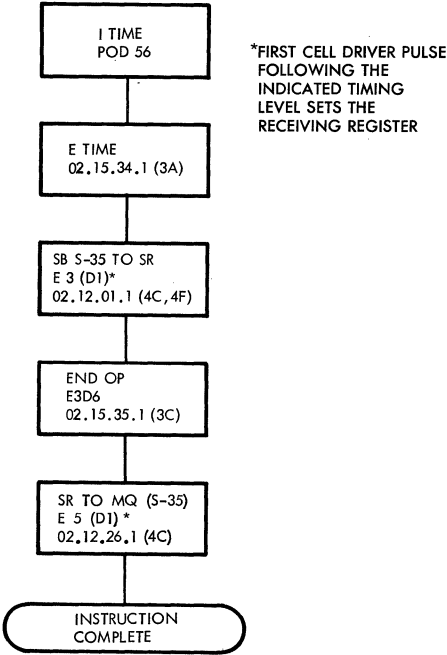


FIGURE 5. LDQ

Enter Keys (ENK +0760...0004)
Places the contents of the console word bank keys into the MQ register.
Address modification may change the operation.

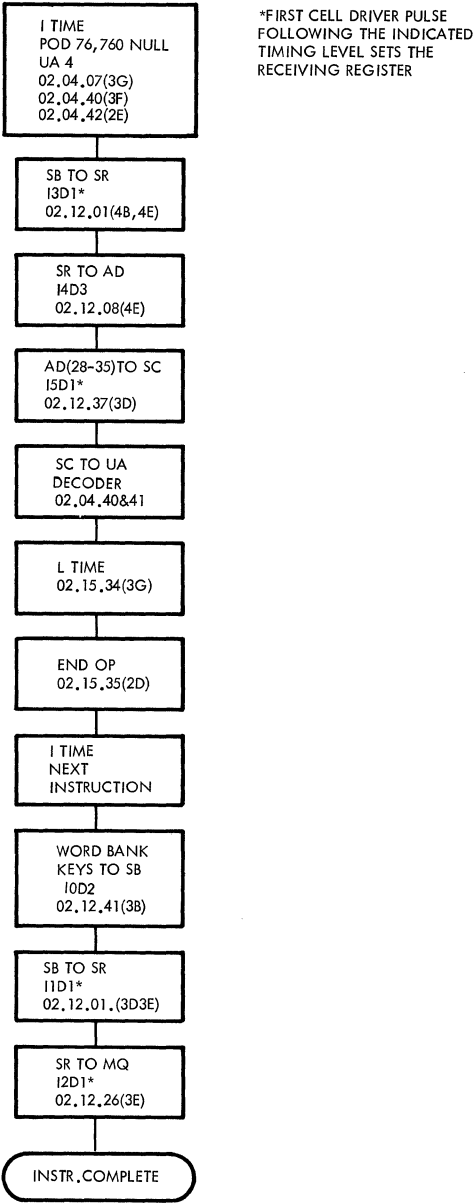
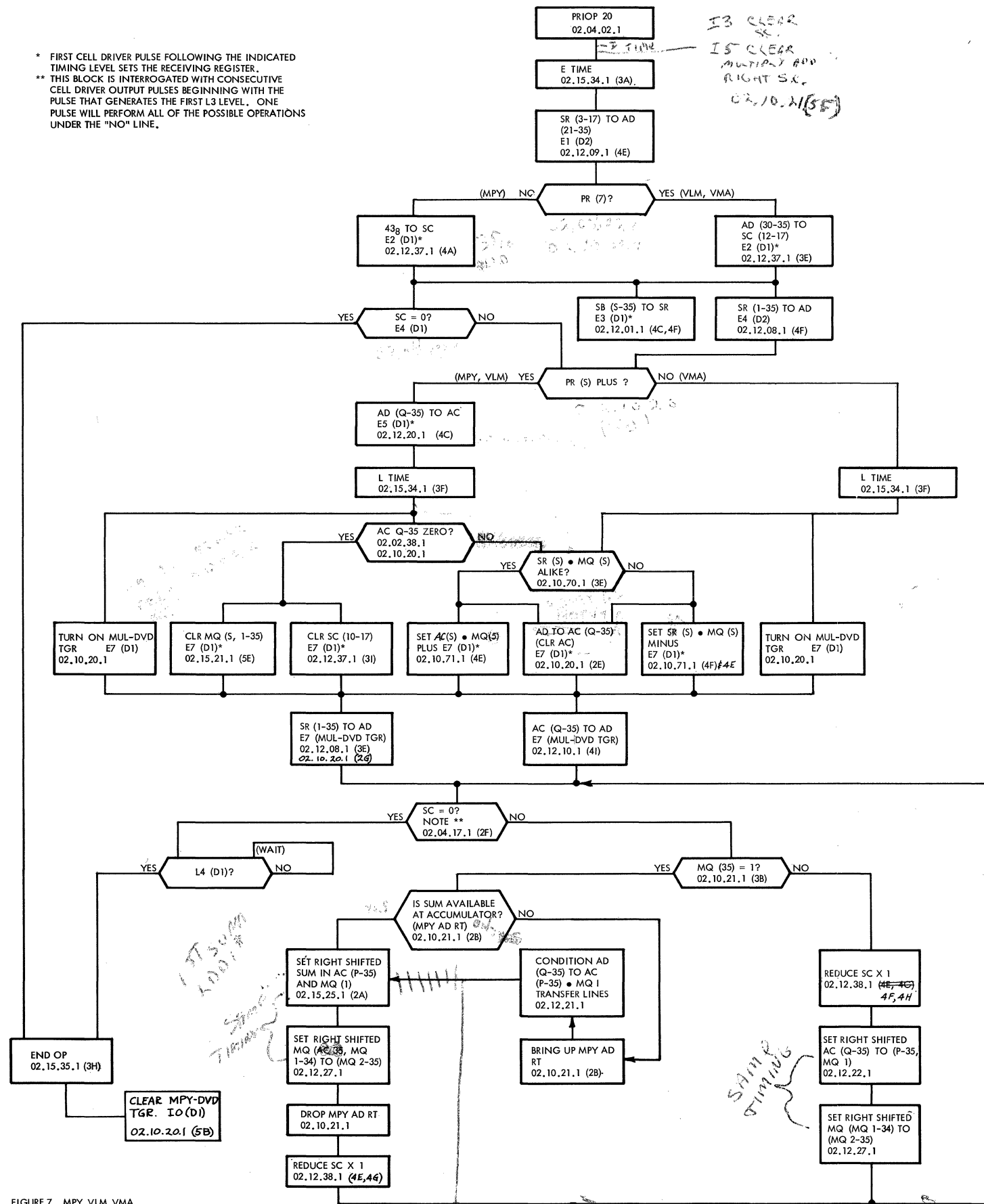


FIGURE 6. ENK

* FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER.
 ** THIS BLOCK IS INTERROGATED WITH CONSECUTIVE CELL DRIVER OUTPUT PULSES BEGINNING WITH THE PULSE THAT GENERATES THE FIRST L3 LEVEL. ONE PULSE WILL PERFORM ALL OF THE POSSIBLE OPERATIONS UNDER THE "NO" LINE.



Multiply (MPY +0200)

Multiplies the contents of the specified memory location (multiplicand) by the contents of the MQ register (multiplier). The result is a 70-bit product that appears in the combined accumulator-MQ. The 35 most significant bits of the product replace the contents of the accumulator (1-35), and the least significant bits replace the contents of the MQ register (1-35). Accumulator P and Q are cleared. The signs of both the accumulator and the MQ register are set to the algebraic sign of the product. The number of bits to the right of the binary point of the first factor added to the number of bits to the right of the binary point of the second factor gives the total number of bits to the right of the binary point in the product.

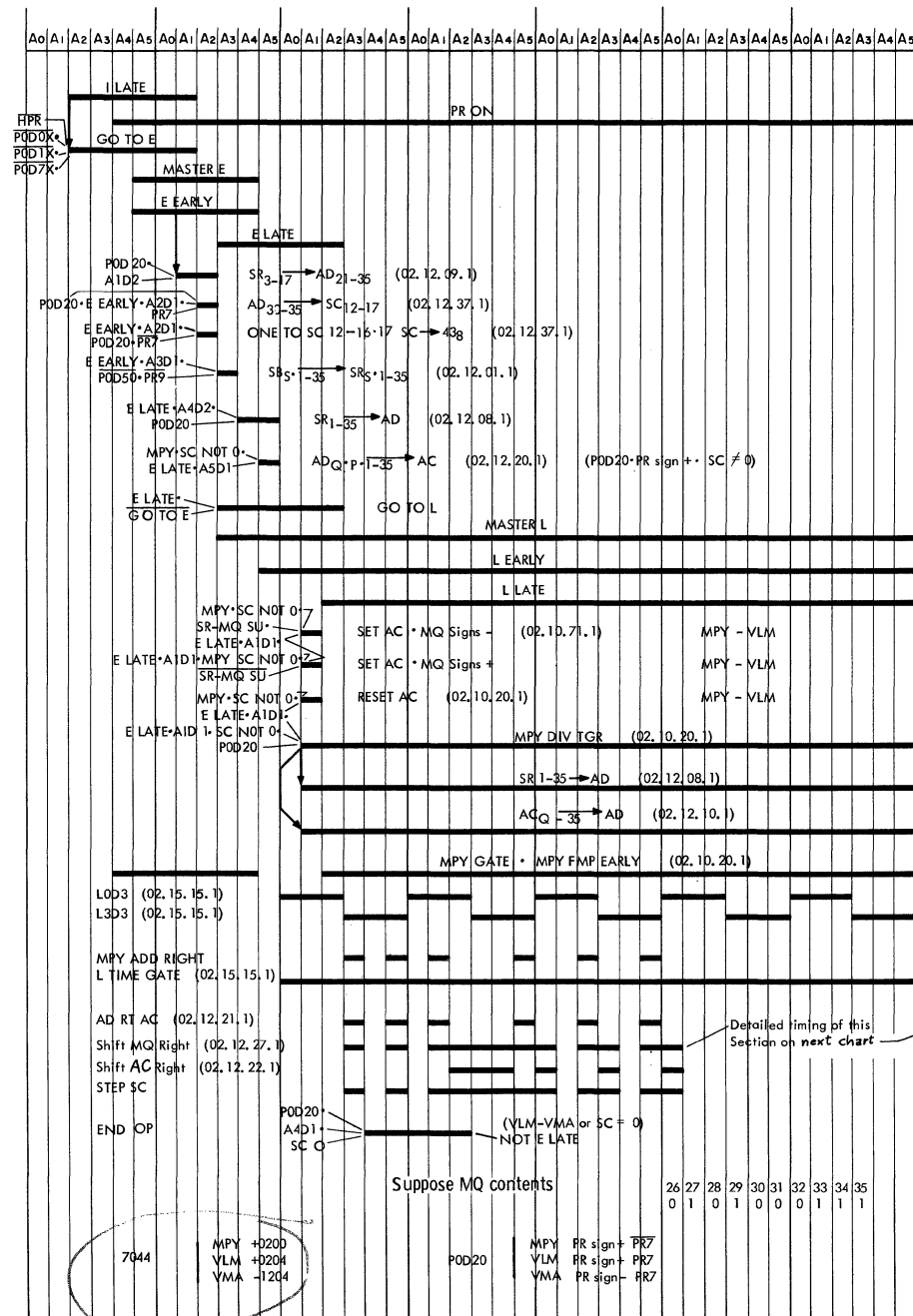
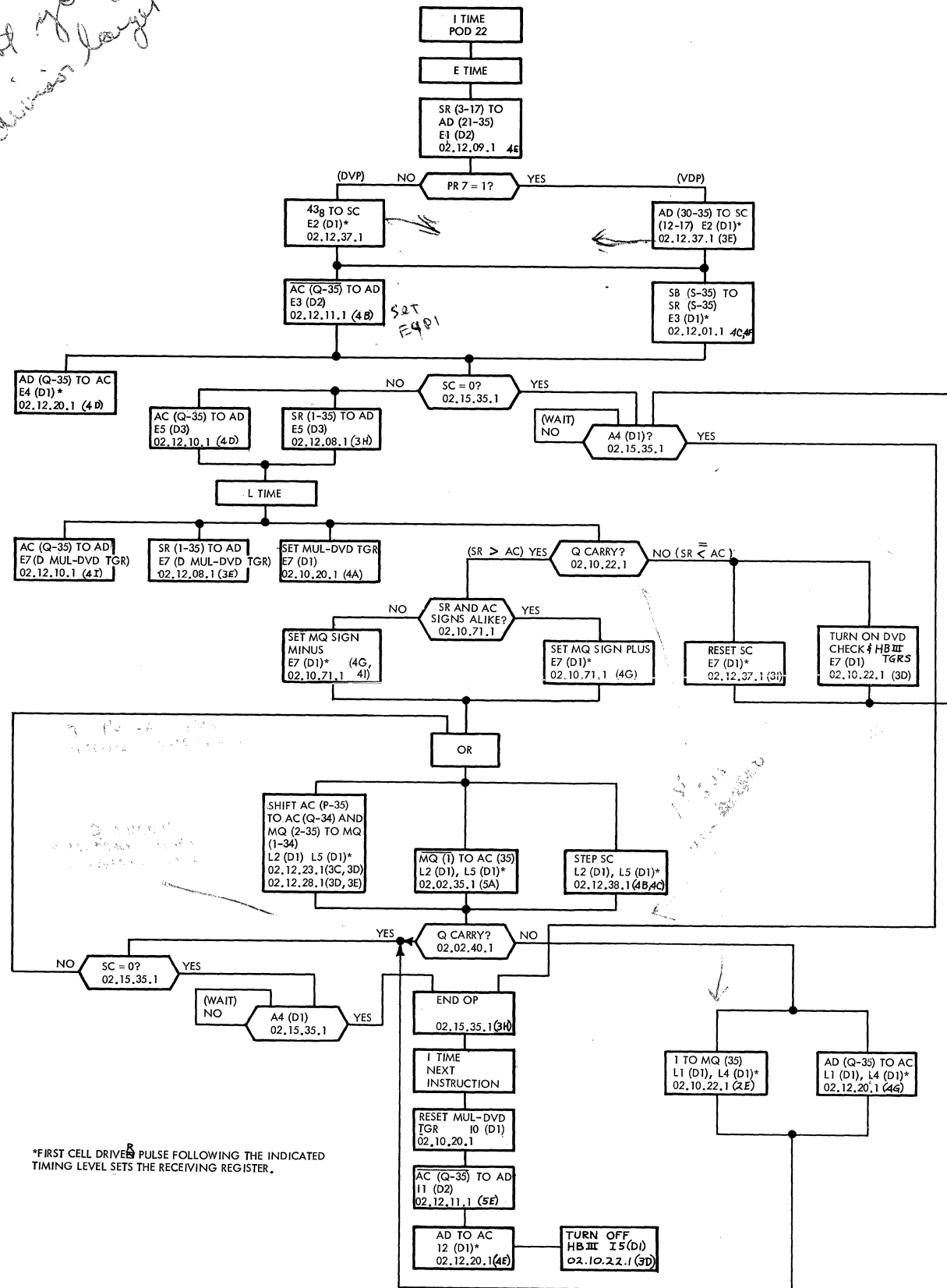


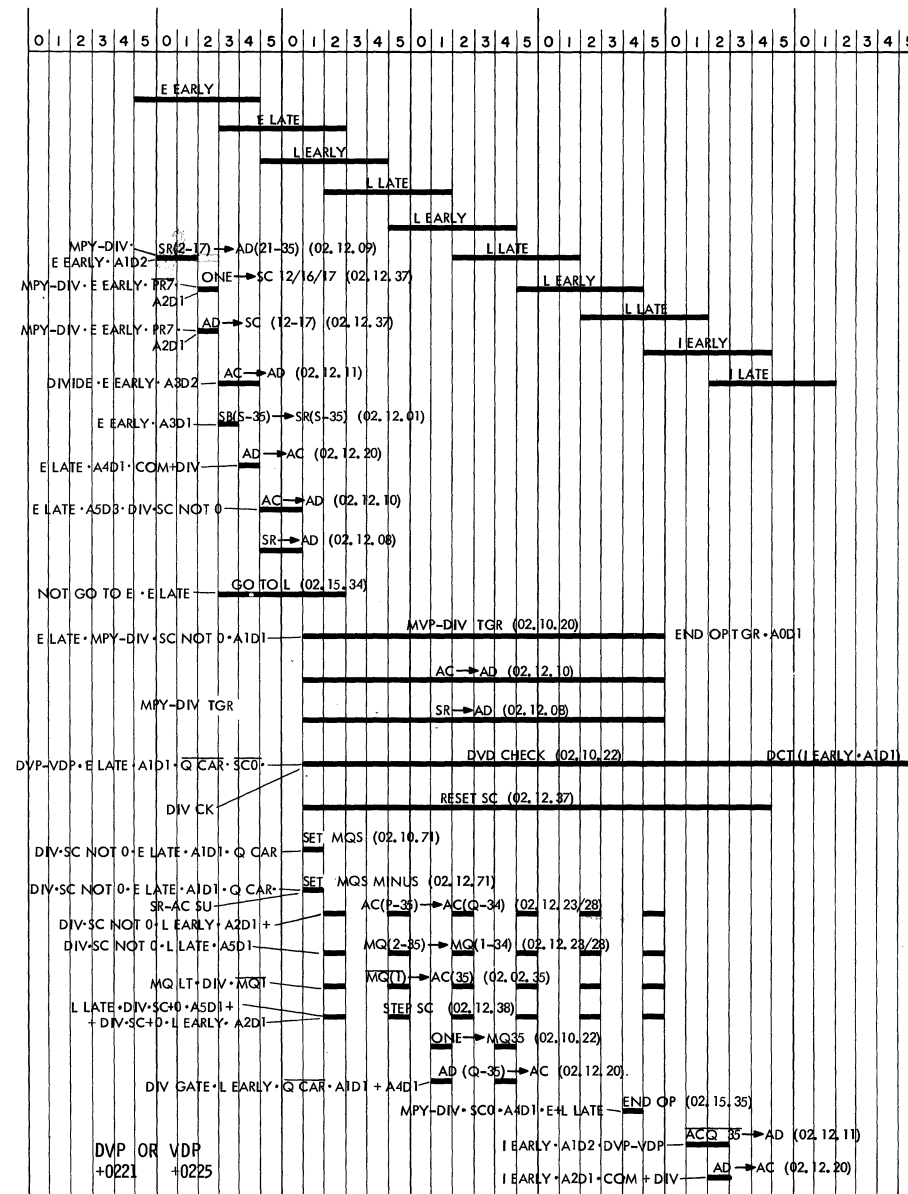
FIGURE 7. MPY, VLM, VMA

SR must be 7 AC
if not you get divide
division larger than dividend



*FIRST CELL DRIVES PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER.

FIGURE 8. DVP, VDP



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00004	050000 000004
00001	LDQ		00005	056000 000005
00002	DVP		00006	022100 000006
00003	TRA		00000	002000 000000
00004	Pattern			000000 000000
00005	Pattern			007777 600001
00006	Pattern			000000 077777

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00004	050000 000000
00001	LDQ		00005	056000 000005
00002	VDP		00006	022524 000006
	(C=24)			
00003	TRA		00000	002000 000000
00004	Pattern			000000 000000
00005	Pattern			007777 600001
00006	Pattern			400000 077777

Divide or Proceed (DVP)																			
CONSOLE INDICATORS																			
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	P CARRY	P OVERFLOW	FP 1
I	E	00001	+500	000	0	00004	050000000004	000000000000	00	000000000000									
E	I	00001	+500	000	0	00001	000000000000	000000000000	00	000000000000									
I	E	00002	+560	000	0	00005	056000000005	000000000000	00	000000000000									
E	I	00002	+560	000	0	00002	007777600001	000000000000	00	007777600001									
I	E	00003	+221	000	0	00006	022100000006	000000000000	00	007777600001									
E	L (1)	00003	+221	043	0	00006	000000077777	377777777777	11	007777600001							1	0	
L (1)	L (2)	00003	+221	041	0	00006	000000077777	377777777777	11	037777000004							1	1	
L (2)	L (3)	00003	+221	037		00006	000000077777	377777777777	11	177774000020							1	1	
L (3)	L (4)	00003	+221	035	0	00006	000000077777	377777777776	11	377760000100							1	1	
L (4)	L (5)	00003	+221	033		00006	000000077777	377777777770	11	377700000400							1	1	
L (5)	L (6)	00003	+221	031		00006	000000077777	377777777774	11	377400002000							1	1	
L (6)	L (7)	00003	+221	027		00006	000000077777	377777777600	11	376000010000							1	1	
L (7)	L (8)	00003	+221	025		00006	000000077777	377777777000	11	370000040000							1	1	
L (8)	L (9)	00003	+221	023		00006	000000077777	377777774000	11	340000200000							1	1	
L (9)	L (10)	00003	+221	021		00006	000000077777	377777600000	11	200001000000							1	1	
L (10)	L (11)	00003	+221	017		00006	000000077777	377777700001	11	000004000000							1	1	
L (11)	L (12)	00003	+221	015		00006	000000077777	377777600005	11	000020000002							1	1	
L (12)	L (13)	00003	+221	013		00006	000000077777	377777600021	11	000100000016							1	1	
L (13)	L (14)	00003	+221	011		00006	000000077777	377777600101	11	000400000076							1	1	
L (14)	L (15)	00003	+221	007		00006	000000077777	377777600401	11	002000000376							1	1	
L (15)	L (16)	00003	+221	005		00006	000000077777	377777602001	11	010000001776							1	1	
L (16)	L (17)	00003	+221	003		00006	000000077777	377777610001	11	040000007776							1	1	
L (17)	L (18)	00003	+221	001		00006	000000077777	377777640001	11	200000037776							1	1	
L (18)	I	00003	+221	000	0	00003	000000077777	377777777777	11	000000077777							1	0	
I	I	00004	+020	000	0	00000	002000000000	000000000000	00	000000077777							0	0	
I	E	00001	+500	000	0	00004	050000000004	000000000000	00	000000077777							0	0	
E	I	00001	+500	000	0	00001	000000000000	000000000000	00	000000077777							0	0	
I	E	00002	+560	000	0	00005	056000000005	000000000000	00	000000077777							0	0	

Variable Length Divide or Proceed (VDP)																			
CONSOLE INDICATORS																			
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	P CARRY	P OVERFLOW	FP 1
I	E	00001	+500	000	0	00004	050000000004	000000000000	00	000000000000									
E	I	00001	+500	000	0	00001	000000000000	000000000000	00	000000000000									
I	E	00002	+560	000	0	00005	056000000005	000000000000	00	000000000000									
E	I	00002	+560	000	0	00002	007777600001	000000000000	00	007777600001									
I	E	00003	+225	000	0	00006	022524000006	000000000000	00	007777600001									
E	L (1)	00003	+225	024	0	00006	400000077777	377777777777	11	407777600001							1		
L (1)	L (2)	00003	+225	022	0	00006	400000077777	377777777777	11	437777000004							1	1	
L (2)	L (3)	00003	+225	020	0	00006	400000077777	377777777777	11	577774000020							1	1	
L (3)	L (4)	00003	+225	016	0	00006	400000077777	377777777776	11	777760000100							1	1	
L (4)	L (5)	00003	+225	014	0	00006	400000077777	377777777770	10	777700000400							1	1	
L (5)	L (6)	00003	+225	012	0	00006	400000077777	377777777774	10	777400002000							1	1	
L (6)	L (7)	00003	+225	010	0	00006	400000077777	377777777600	10	776000010000							1	1	
L (7)	L (8)	00003	+225	006	0	00006	400000077777	377777777000	10	770000040000							1	1	
L (8)	L (9)	00003	+225	004	0	00006	400000077777	377777774000	10	740000200000							1	1	
L (9)	L (10)	00003	+225	002	0	00006	400000077777	377777600000	10	600001000000							1	1	
L (10)	L (11)	00003	+225	000	0	00006	400000077777	377777700001	10	400004000000							1	1	
L (11)	I	00003	+225	000	0	00003	400000077777	377777700001	10	400004000000							1	1	
I	I	00004	+020	000	0	00000	002000000000	000000077776	00	400004000000									
I	E	00001	+500	000	0	00004	050000000004	000000077776	00	400004000000									
E	I	00001	+500	000	0	00001	000000000000	000000000000	00	400004000000									
I	E	00002	+560	000	0	00005	056000000005	000000000000	00	400004000000									
E	I																		

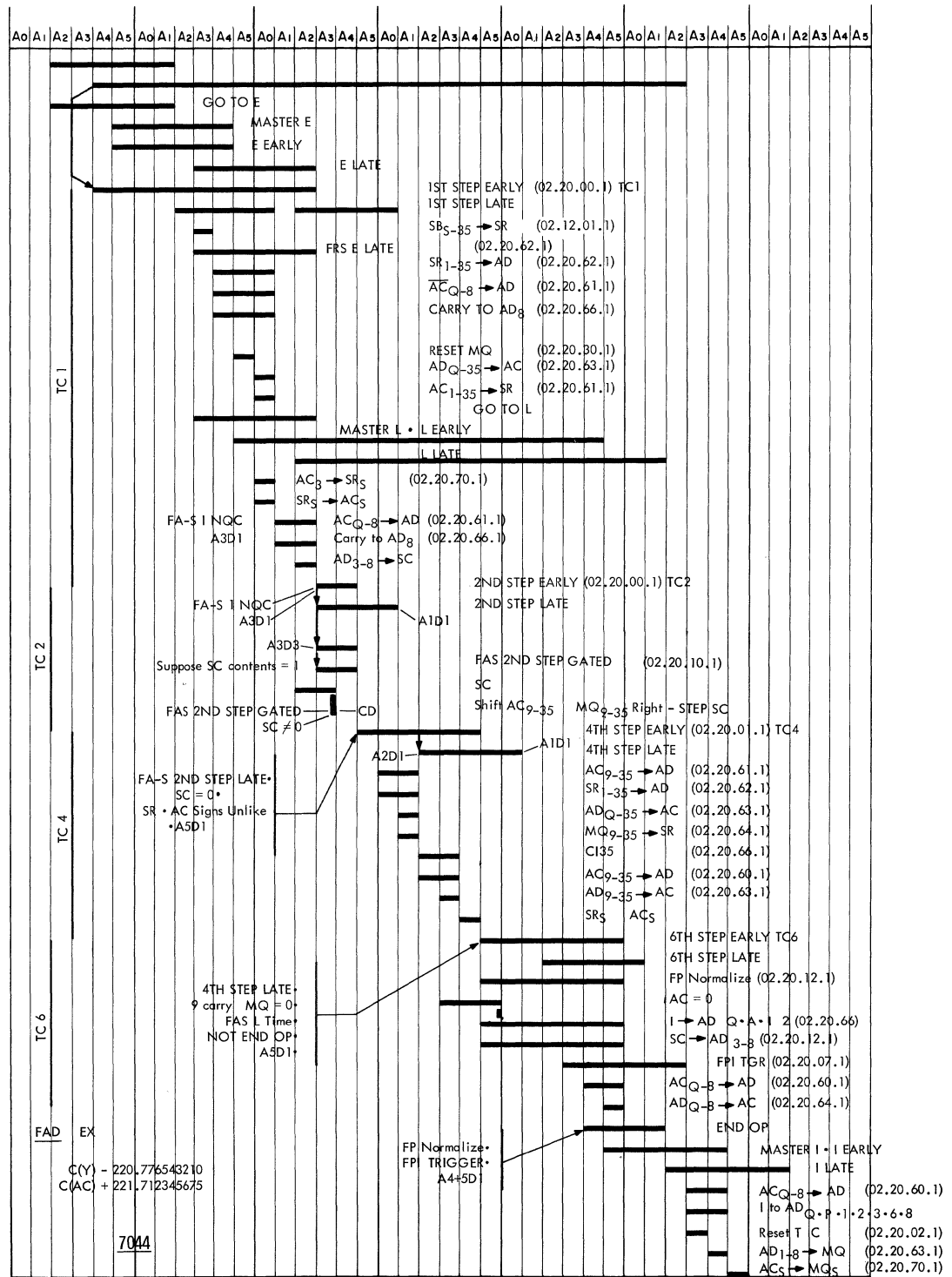
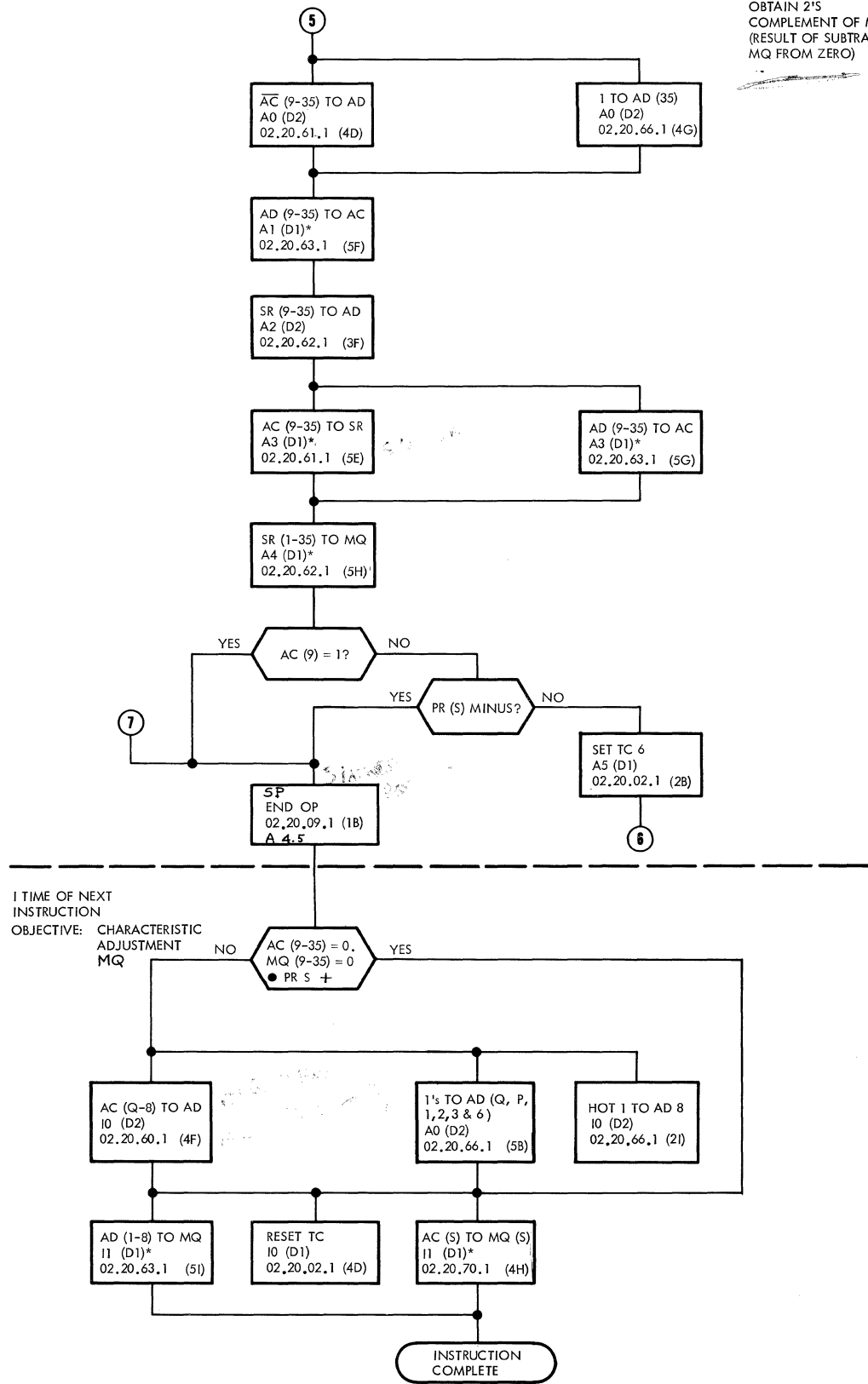
Adds the floating-point number in the specified memory location to the accumulator. The most significant portions of the result appear as a normalized floating-point number in the accumulator. The least significant portion of the result appears in the MQ register as a floating-point number with a characteristic 33g less than the accumulator characteristic. The signs of the accumulator and the MQ are set to the sign of the larger factor. The sum in the accumulator and MQ is always normalized whether the original factors are normalized or not. If the contents of the accumulator (1-35) contain 0's, the FAD instruction may be used to normalize an unnormalized floating-point number.

Unnormalized Floating Add (UFA -0300)
Same as FAD except that the sum is not normalized.

Floating Subtract (FSB -0302)
Algebraically subtracts the floating-point number in the specified memory location from the floating-point number in the accumulator. The results are normalized.

Same as FSB except that the difference is not normalized.





Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	FAD		00006	030000 000006
00002	TRA		00000	002000 000000
00003				
00004	Pattern			600012 334567
00005	Pattern			606065 443210
00006				

Floating Add(FAD)																					
CONSOLE INDICATORS																					
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	P CARRY	P OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00005	050000000005	000000000000	00	000000000000											
E	I	00001	+500	000	0	00001	600012334567	600012334567	00	000000000000											
I	E	00002	+300	000	0	00006	030000000006	600012334567	00	000000000000	1 & 10										
E	L(1)	00002	+300	006	0	00006	606065443210	600012334567	00	000000000000	1 & 10			1							
L(1)	L(2)	00002	+300	001	0	00006	606065443210	600000246713	00	000560000000	2 & 10			1							
L(2)	L(3)	00002	+300	000	0	00006	606065443210	600000123345	00	000670000000	3 & 10			1							
L(3)	L(4)	00002	+300	377	0	00006	606065443210	606153355333	00	000560000000	6 & 10			1							
L(4)	I	00002	+300	375	0	00002	606065443210	603655665556	00	000700000000	6 & 10			1						1	
I	I	00003	+020	000	0	00000	002000000000	603655665556	00	550700000000											
I	E	00001	+500	000	0	00005	050000000005	603655665556	00	550700000000											
E	I	00001	+500	000	0	00001	600012334567	600012334567	00	550700000000											
I	E	00002	+300	000	0	00006	030000000006	600012334567	00	550700000000											

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	UFA		00006	430000 000006
00002	TRA		00000	002000 000000
00003				
00004	Pattern			377777 777777
00005	Pattern			200000 000000
00006				

		Unnormalized Floating Add (UFA)																			
		CONSOLE INDICATORS																			
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S 1-35)	ACCUMULATOR (Q P)	MQ REGISTER (S 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	P CARRY	P OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00005	050000000005	000000000000	00	000000000000											
E	I	00001	+500	000	0	00001	377777777777	377777777777	00	000000000000											
I	E	00002	-300	000	0	00006	430000000006	377777777777	00	000000000000	1 & 10										
E	L(1)	00002	-300	000	0	00006	377777777777	201000000000	11	000000000000	1 & 10										
L(1)	L(2)	00002	-300	000	0	00006	377777777777	201000000000	11	000000000000	3 & 10										
L(2)	I	00002	-300	000	0	00002	377777777777	377777777777	00	000000000000	3 & 10										
I	I	00003	+020	000	0	00000	002000000000	377777777777	00	344000000000											
I	E	00002	+500	000	0	00005	050000000005	377777777777	00	344000000000											
E	I	00002	+500	000	0	00001	377777777777	377777777777	00	344000000000											
I	E	00002	-300	000	0	00006	430000000006	377777777777	00	344000000000											

FIGURE 9. FAD, UFA, FSB, UFS
(CONTINUED)

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00004	050000 000004
00001	FSB		00005	030200 000005
00002	TRA		00000	002000 000000
00003				
00004	Pattern			606065 443210
00005	Pattern			600012 334567
00006				

Floating Subtract (FSB)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S 1-35)	ACCUMULATOR (Q P)	MQ REGISTER (S 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK
I	E	00001	+500	000	0	00004	050000000004	000000000000	00	000000000000					
E	I	00001	+500	000	0	00001	606065443210	606065443210	00	000000000000					
I	E	00002	+302	000	0	00005	030200000005	606065443210	00	000000000000	1 & 10				
E	L(1)	00002	+302	000	0	00005	606065443210	372012334567	11	000000000000	1 & 10				
L(1)	L(2)	00002	+302	003	0	00005	606065443210	372001233456	11	000700000000	2 & 10				
L(2)	L(3)	00002	+302	000	0	00005	606065443210	372000123345	11	000670000000	4 & 10				
L(3)	L(4)	00002	+302	000	0	00005	606065443210	606670000000	00	000670000000	5 & 10				
L(4)	L(5)	00002	+302	377	0	00005	606110000000	606152637504	00	206220000000	6 & 10				
L(5)	I	00002	+302	375	0	00002	606110000000	603653176421	00	206100000000	6 & 10				
I	I	00003	+020	000	0	00000	002000000000	603653176421	00	550100000000					
I	E	00001	+500	000	0	00004	050000000004	603653176421	00	550100000000					
E	I	00001	+500	000	0	00001	606065443210	606065443210	00	550100000000					
I	E	00002	+302	000	0	00005	030200000005	506065443210	00	550100000000	1 & 10				

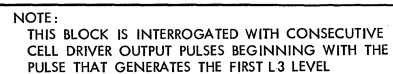
Location Switches	Inst	Tag	Address	Octal Equiv
00000	LDQ		00004	056000 000004
00001	CLA		00005	050000 000005
00002	UFS		00006	430200 000006
00003	TRA		00000	002000 000000
00004	Pattern			777777 777777
00005	Pattern			200012 334567
00006	Pattern			206065 443210

Unnormalized Floating Subtract (UFS)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S 1-35)	ACCUMULATOR (Q P)	MQ REGISTER (S 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK
I	E	00001	+560	000	0	00004	056000000004	000000000000	00	000000000000					
E	I	00001	+560	000	0	00001	777777777777	000000000000	00	777777777777					
I	E	00002	+500	000	0	00005	050000000005	000000000000	00	777777777777					
E	I	00002	+500	000	0	00002	200012334567	200012334567	00	777777777777					
I	E	00003	-302	000	0	00006	430200000006	200012334567	00	777777777777	1 & 10				
E	L(1)	00003	-302	006	0	00006	606065443210	200012334567	00	000000000000	1 & 10				
L(1)	L(2)	00003	-302	001	0	00006	606065443210	200000246713	00	000560000000	2 & 10				
L(2)	L(3)	00003	-302	000	0	00006	606065443210	200000123345	00	000670000000	4 & 10				
L(3)	L(4)	00003	-302	000	0	00006	606065443210	606670000000	00	000670000000	5 & 10				
L(4)	I	00003	-302	000	0	00003	606110000000	606065317642	00	206110000000	5 & 10				
I	I	00004	+020	000	0	00000	002000000000	606065317642	00	553110000000					
I	E	00001	+560	000	0	00004	056000000004	606065317642	00	553100000000					
E	I	00001	+560	000	0	00001	777777777777	606065317642	00	777777777777					
I	E	00002	+500	000	0	00005	050000000005	606065317642	00	777777777777					

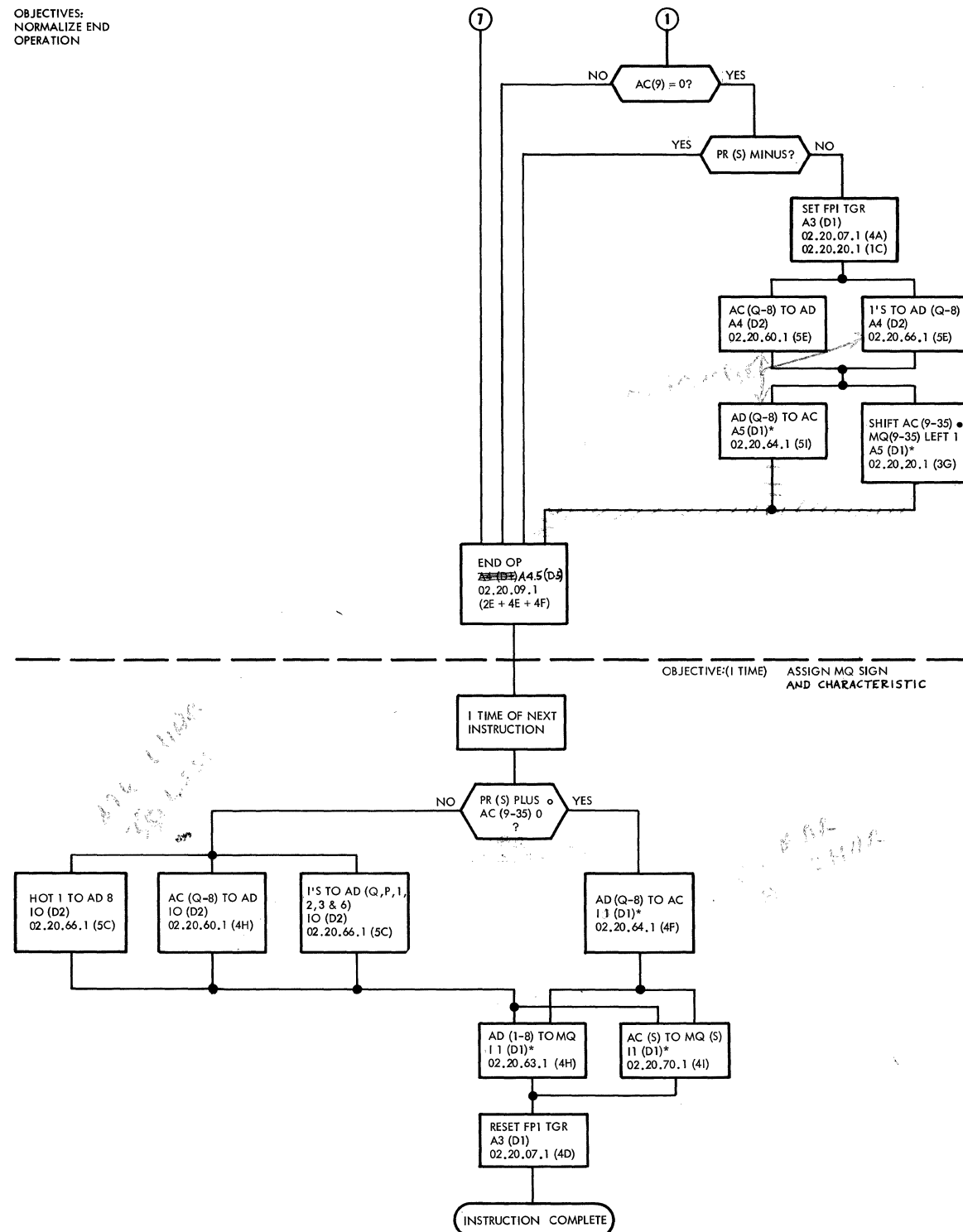
Multiplies the contents of the specified memory location by the contents of the MQ register. The most significant part of the product appears in the accumulator, and the least significant part appears in the MQ register. The product of two normalized numbers is in normalized form. If either number is not normalized, the product may or may not be in normalized form.

Multiplies the contents of the specified memory location by the contents of the MQ register. The result is not normalized.

1. ZERO TEST MULTIPLIER IF AC FR IS CLEARED
2. ASSIGN PRODUCT SIGN
3. ENSURE NORMAL ZERO PRODUCT IF UFM WITH NORMALIZED ZERO MULTIPLICAND



	OBJECTIVE:(1 TIME)	ASSIGN MQ SIGN AND CHARACTERISTIC
--	--------------------	-----------------------------------

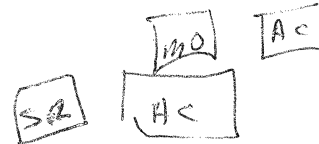


26

Floating Divide or Proceed (FDP+0241)

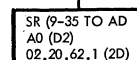
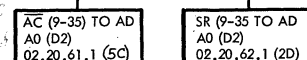
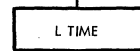
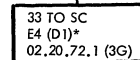
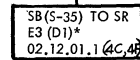
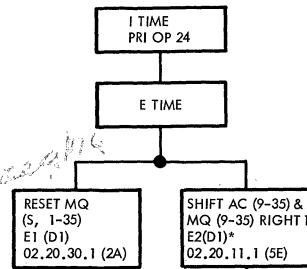
Divides the contents of the accumulator (dividend) by the contents of the specified memory location (divisor). The quotient appears in the MQ register, and the remainder appears in the accumulator. If the dividend fraction is greater than or equal to twice that of the divisor fraction, or if the divisor fraction is 0, division does not occur and the computer takes the next instruction in sequence. The quotient is in normal form if both the dividend and the divisor are in normal form. The sign of the MQ is the algebraic sign of the quotient. If the dividend fraction is 0, the contents of the accumulator (Q, P, 1-35) are cleared and the sign is set plus.

Remainder
char = 33, less
char dividend char



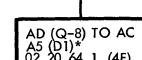
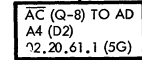
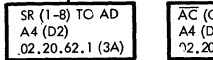
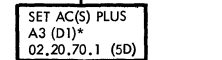
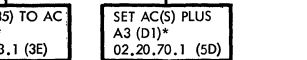
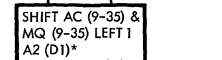
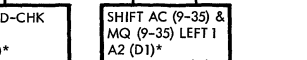
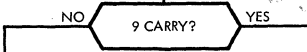
always 2 bits
to direct with
normalized re

OBJECTIVE: RESET MQ REGISTER
PREPARE FOR DIVIDE CHECK TEST



OBJECTIVES:
STEP 1 (TC11)
1. CHECK FOR LEGAL DIVIDE
2. DIVIDEND ZERO TEST
3. OBTAIN CHARACTERISTIC DIFFERENCE IN COMPLEMENT FORM

DIVIDEND $\geq$
TWICE THE
DIVISOR



1 END OP

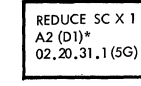
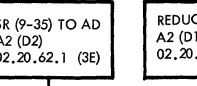
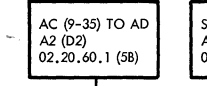
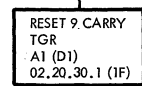
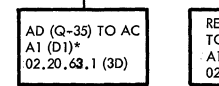
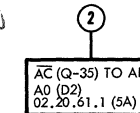
2

* FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER.

CHAR - either
true difference or
2's complement difference

OBJECTIVES: TC 2
OBTAIN TRUE CHARACTERISTIC DIFFERENCE
PERFORM 1ST OF 27 10 DIVIDE CYCLE STEPS.

implement dividend for Subt.



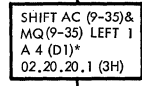
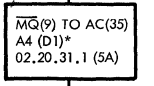
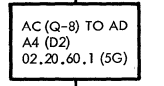
(DIVIDEND $\geq$
DIVISOR)

NO

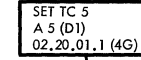
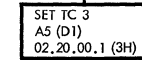
9 CARRY?

YES

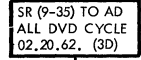
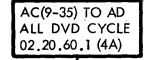
(DIVIDEND <
DIVISOR)



OR



OBJECTIVE: TC13
REMAINDER OF
DIVIDE CYCLE



NO

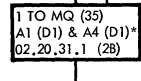
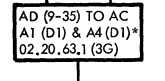
AD 9 CARRY?

YES

NO

AC 9 OVERFLOW?

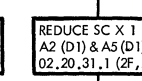
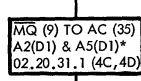
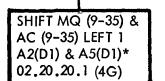
YES



YES

SC = 0?

NO



7

OBJECTIVES:
TC13 AND TC15:
1. 200 PLUS CHARACTER DIFFERENCE TO MQ
2. OBTAIN ORIGINAL CHARACTERISTIC OF DIVIDEND

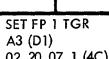
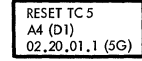
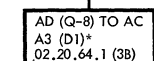
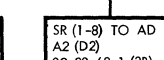
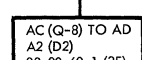
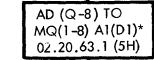
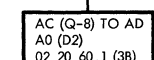
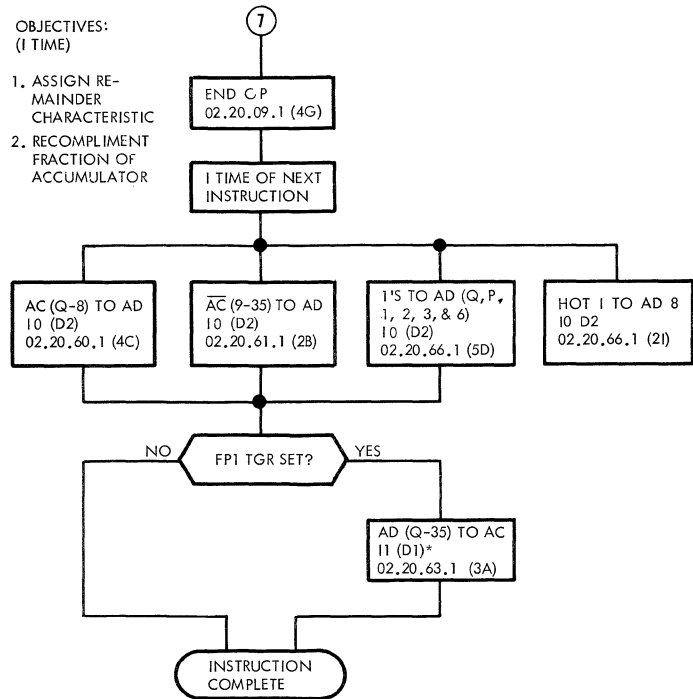


FIGURE 11. FDP



* FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

Location Switches	Inst	Tag	Address	Octal Equiv
00000	LDQ		00007	056000 000007
00001	CLA		00005	050000 000005
00002	FDP		00006	024100 000006
00003	TRA		00000	002000 000000
00004				
00005	Pattern			173516 274051
00006	Pattern			176444 444445
00007	Live Reg			000000 000000

Floating Divide or Proceed (FDP)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (A, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (M, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK
I	E	00001	+560	000	0	00007	056000000007								
E	I	00001	+560	000	0	00001	000000000000								
I	E	00002	+500	000	0	00005	050000000005								
E	I	00002	+500	000	0	00002	173516274051	173516274051	00						
I	E	00003	+241	000	0	00006	024100000006	173516274051	00		1&10				
E	L (1)	00003	+241	033	0	00006	176444444445	173247136024	00	000400000000	1&10				
L (1)	L (2)	00003	+241	033	0	00006	176444444445	002516274051	00	000000000000	2&10				1
L (2)	L (3)	00003	+241	032	0	00006	176444444445	376261503726	11	000000000000	3,5,10				
L (3)	L (4)	00003	+241	030	0	00006	176444444445	174530641757	00	176000000004	3&10				1 1 1
L (4)	L (5)	00003	+241	026	0	00006	176444444445	174654327011	00	176000000022	3&10				1 1 1
L (5)	L (6)	00003	+241	024	0	00006	176444444445	174261504047	00	176000000110	3&10				1 1 1
L (6)	L (7)	00003	+241	022	0	00006	176444444445	174560642463	00	176000000444	3&10				1 1 1
L (7)	L (8)	00003	+241	020	0	00006	176444444445	174654323431	00	176000002222	3&10				1 1 1
L (8)	L (9)	00003	+241	016	0	00006	176444444445	174261516147	00	176000011110	3&10				1 1 1
L (9)	L (10)	00003	+241	014	0	00006	176444444445	174530713063	00	176000044444	3&10				1 1 1
L (10)	L (11)	00003	+241	012	0	00006	176444444445	174654565431	00	176000222222	3&10				1 1 1
L (11)	L (12)	00003	+241	010	0	00006	176444444445	174262726147	00	176001111110	3&10				1 1 1
L (12)	L (13)	00003	+241	006	0	00006	176444444445	174535753063	00	176004444444	3&10				1 1 1
L (13)	L (14)	00003	+241	004	0	00006	176444444445	174700765431	00	176022222222	3&10				1 1 1
L (14)	L (15)	00003	+241	002	0	00006	176444444445	174403726147	00	176111111110	3&10				1 1 1
L (15)	L (16)	00003	+241	000	0	00006	176444444445	174130641751	00	176444444442	3&10				1 1 1
L (16)	I	00003	+241	000	0	00003	176444444445	174575306416	00	176444444443	3&10				1
I	I	00004	+020	000	0	00000	002000000000	141202471361	00	176444444443					
I	E	00001	+560	000	0	00007	056000000007	141202471361	00	176444444443					
E	I	00001	+560	000	0	00001	000000000000	141202471361	00	000000000000					
I	E	00002	+500	000	0	00005	050000000005	141202471361	00	000000000000					

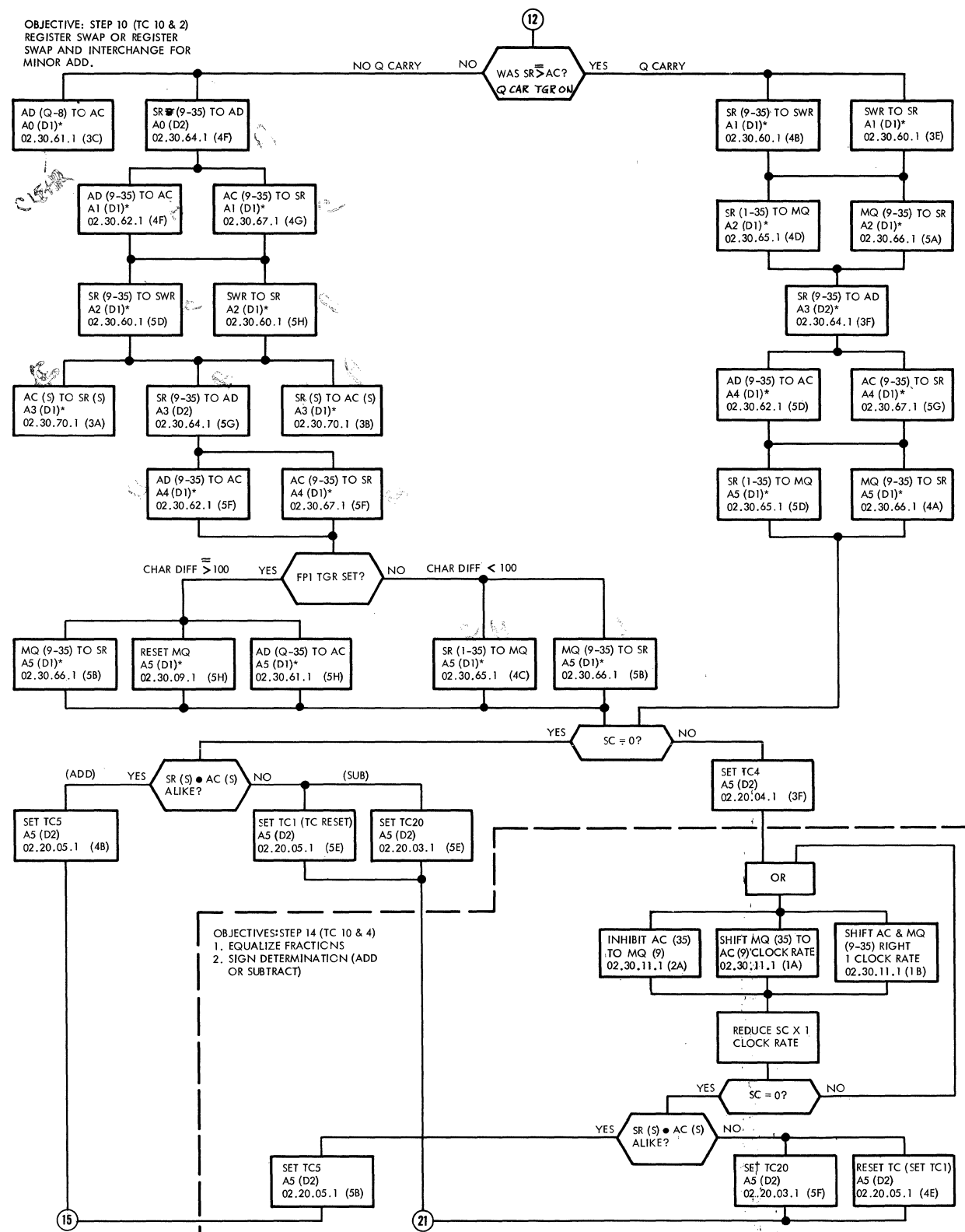
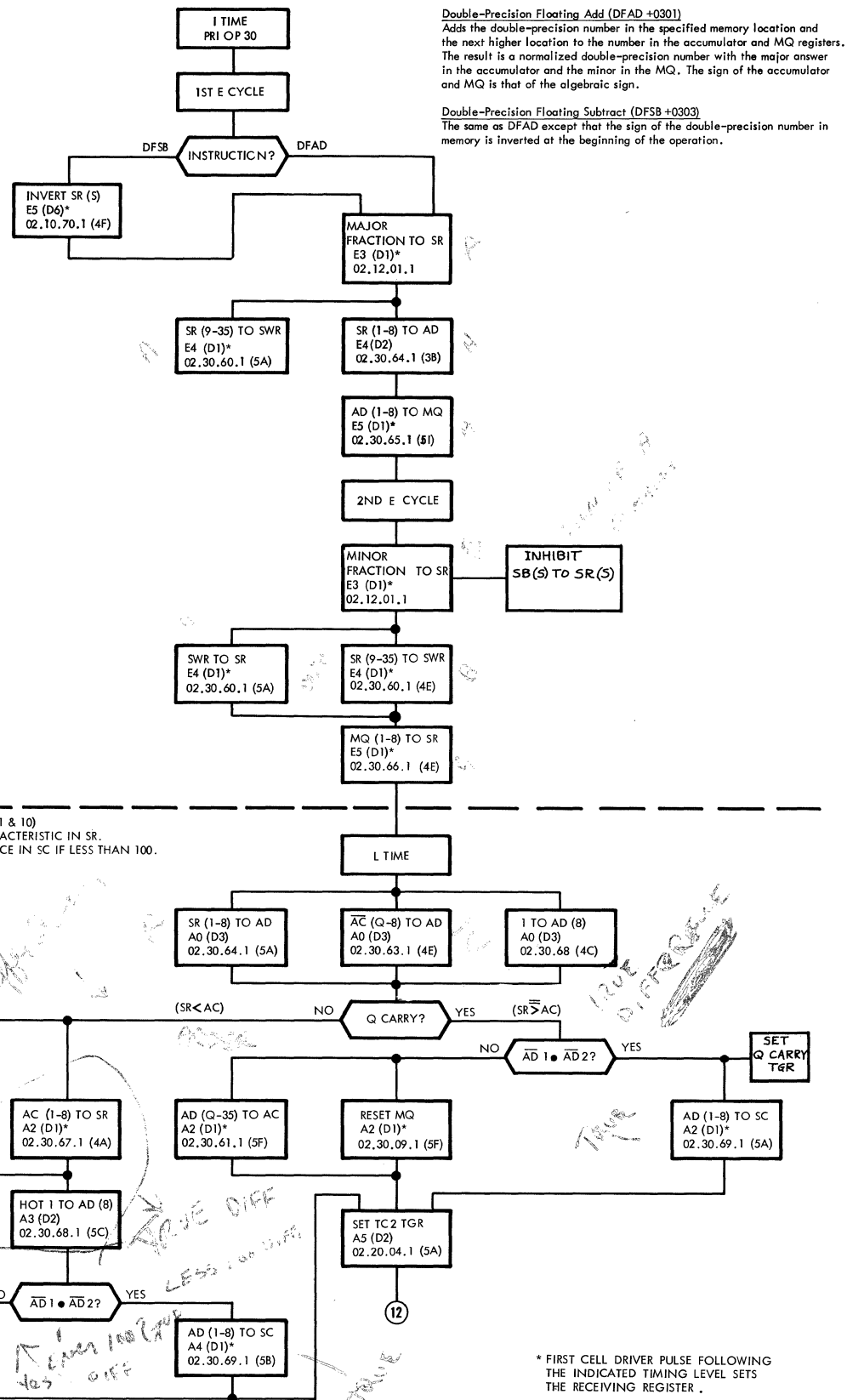
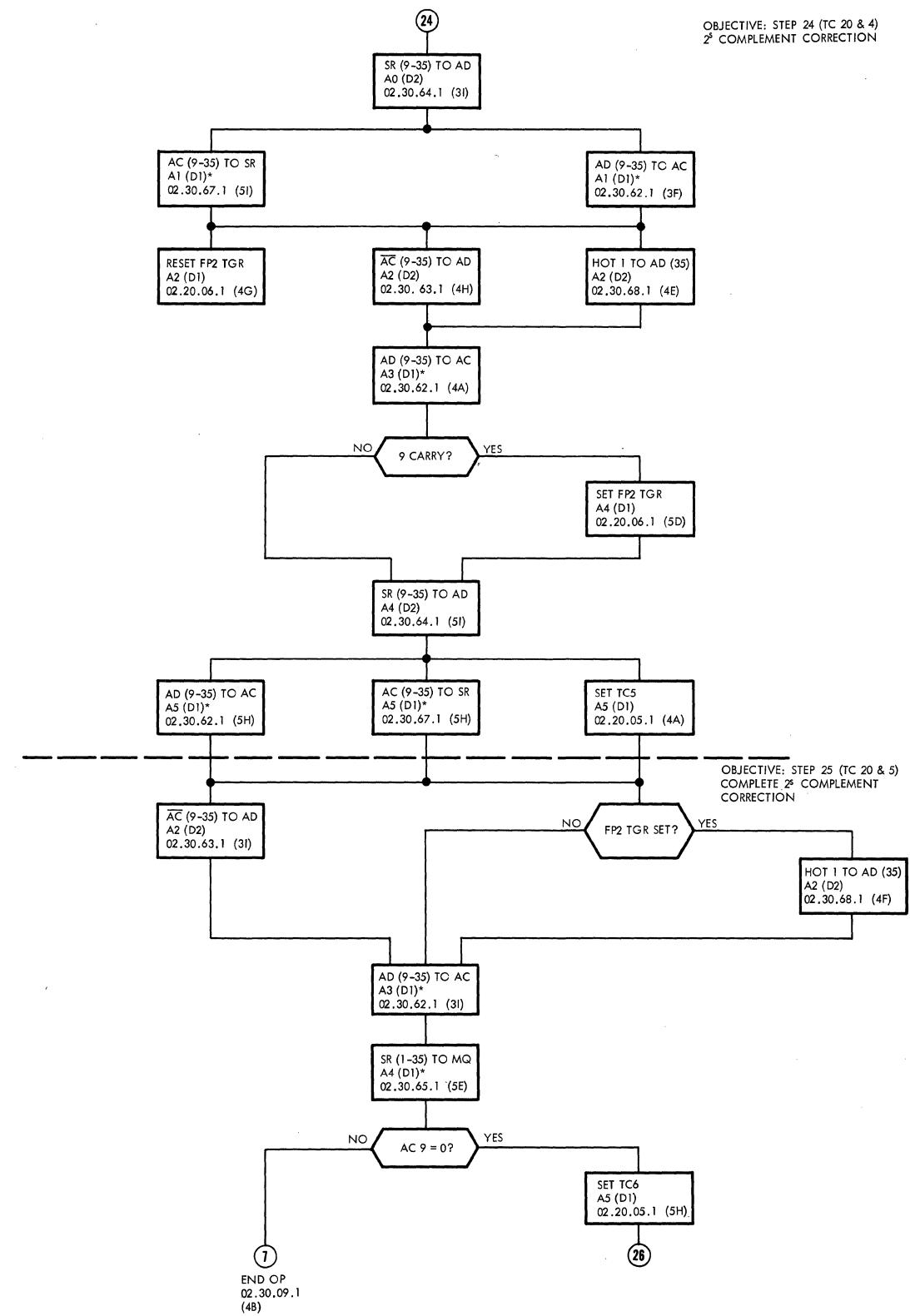
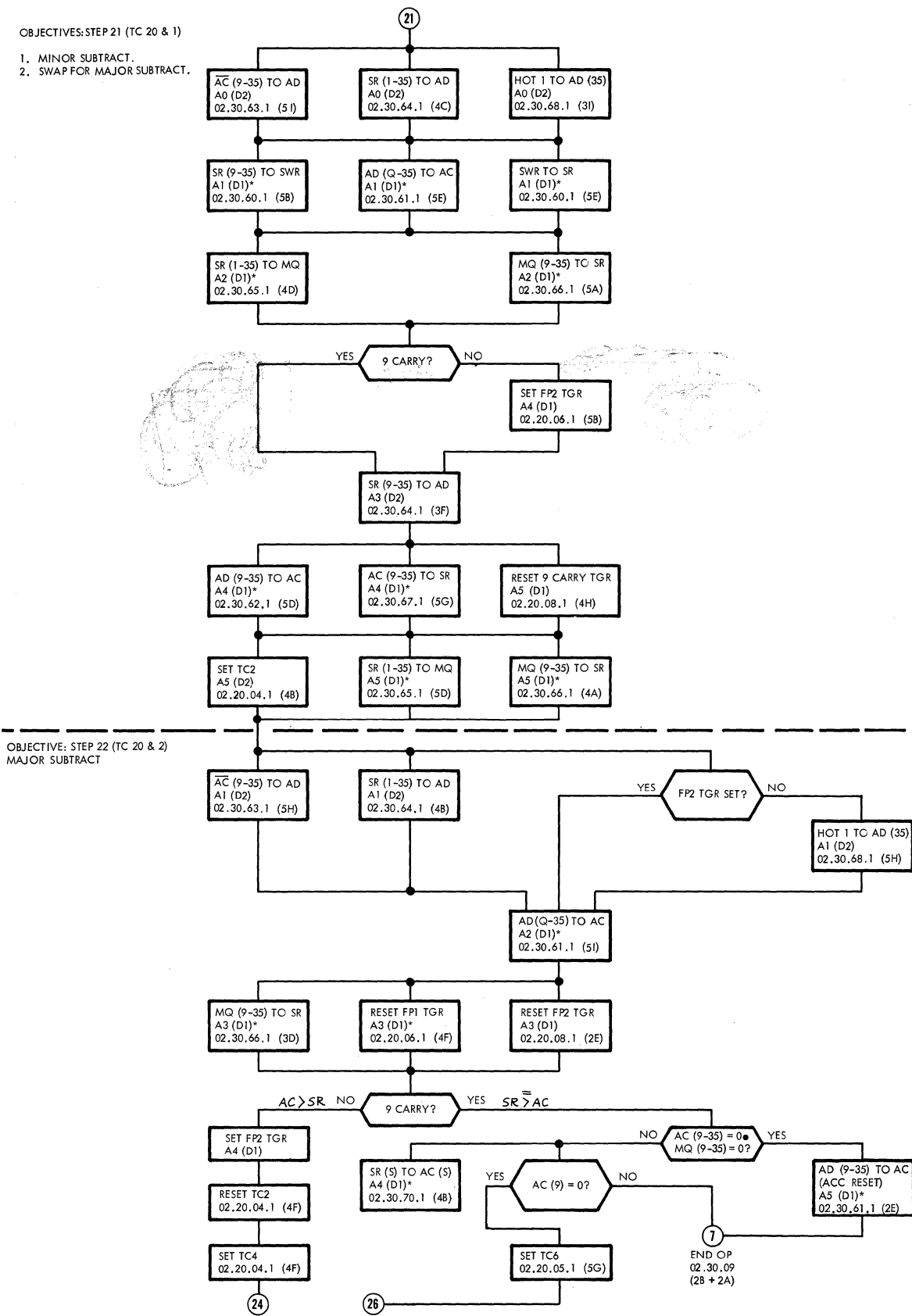
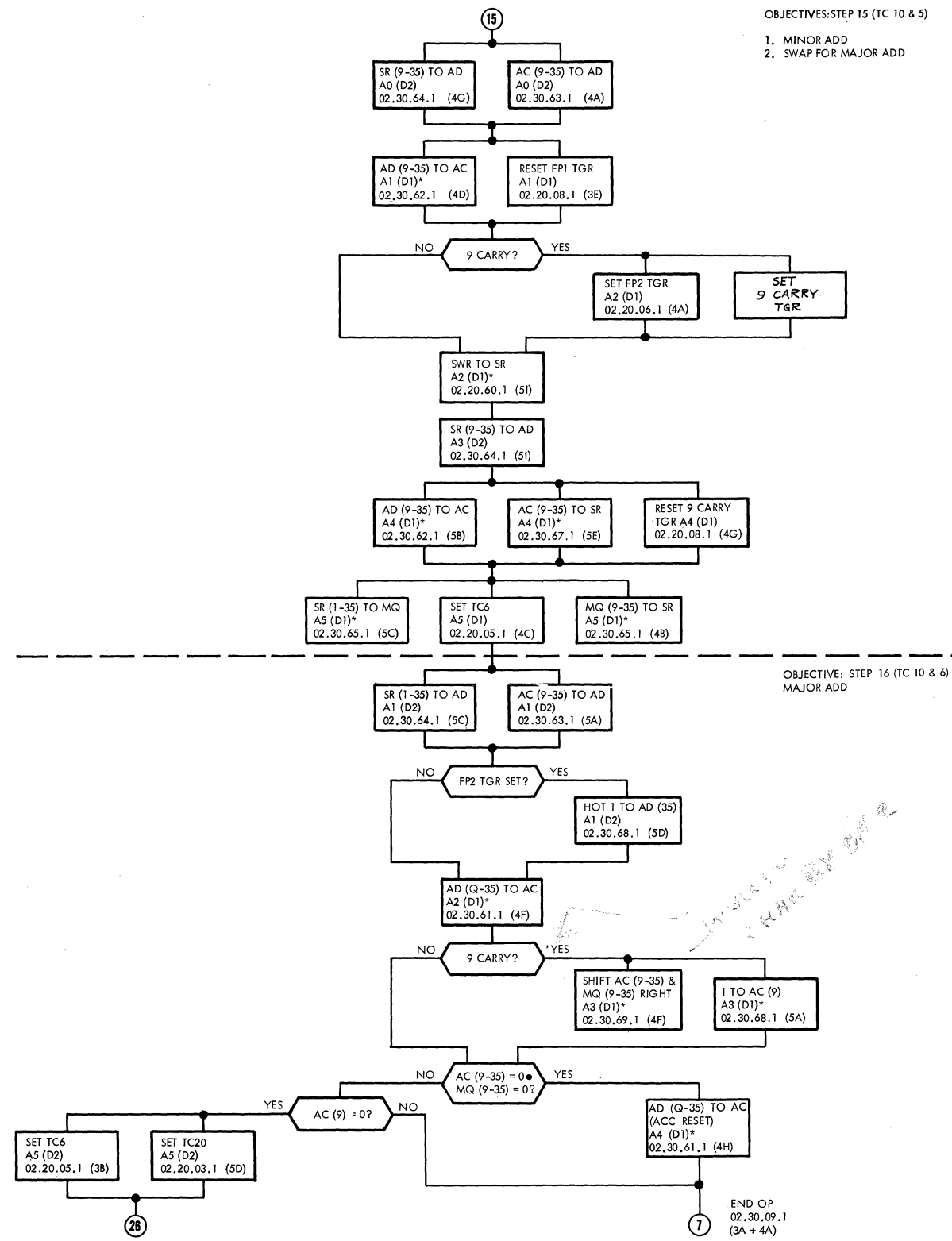
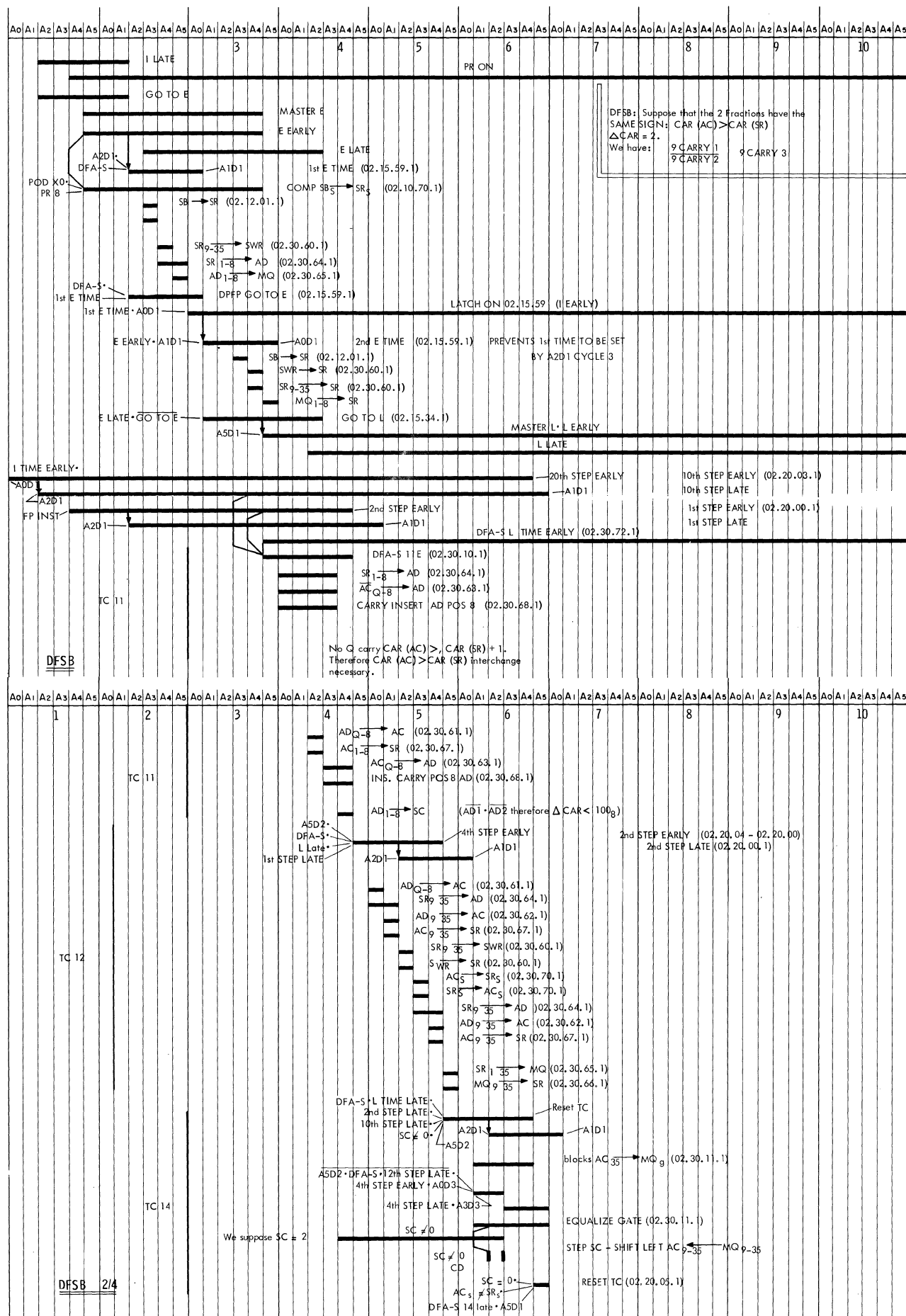
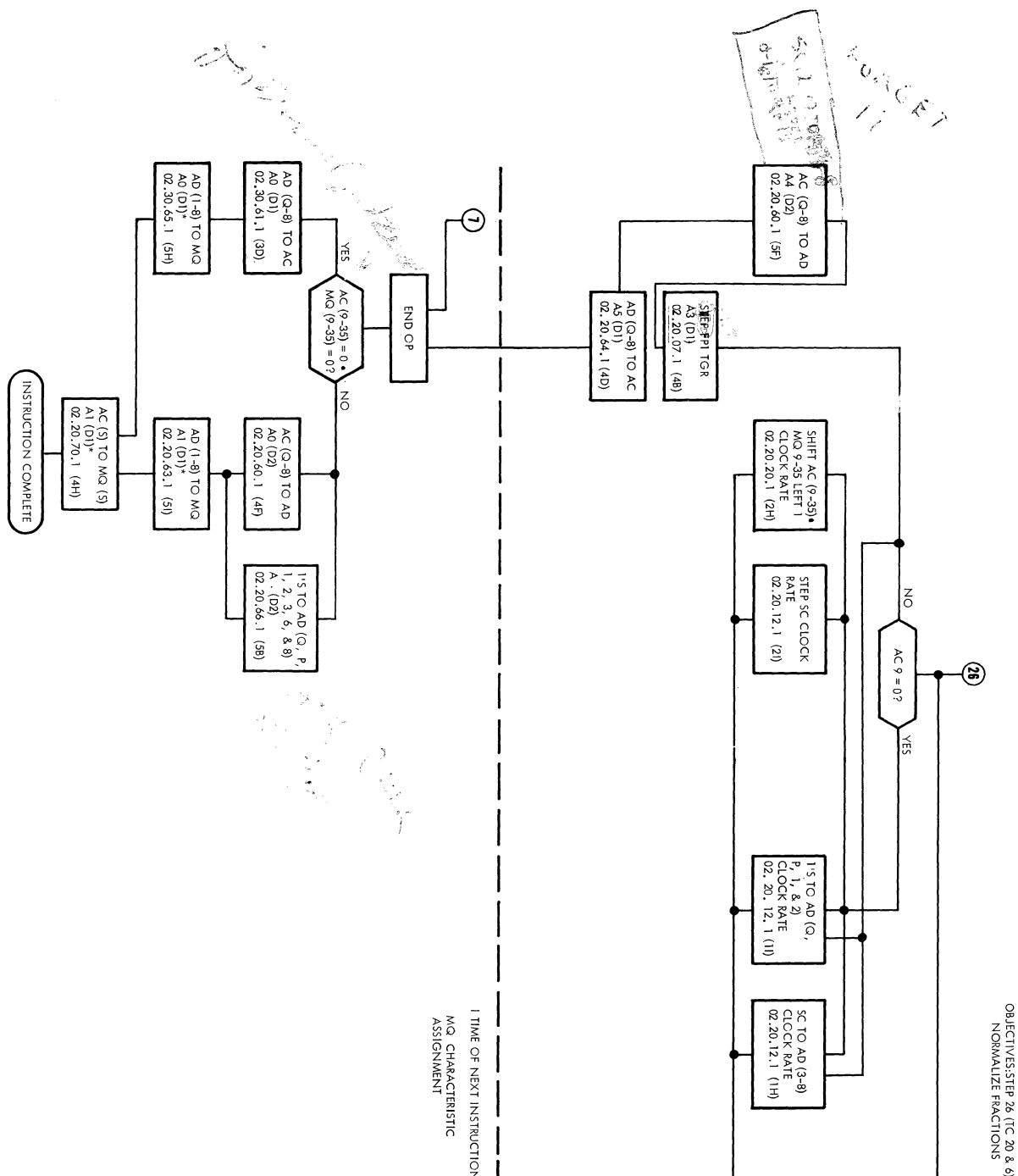
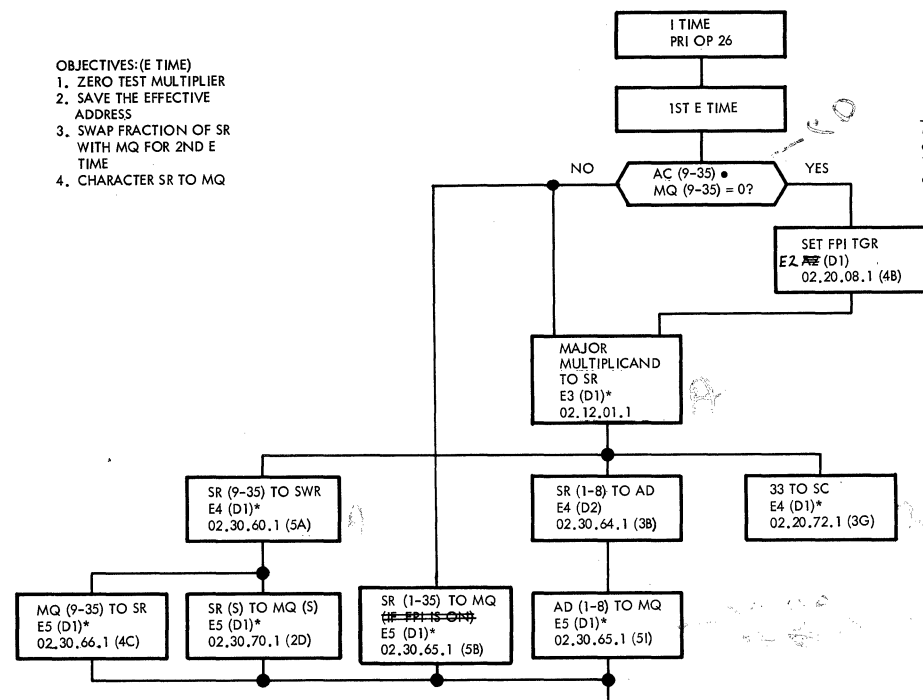


FIGURE 12. DFAD, DFSB

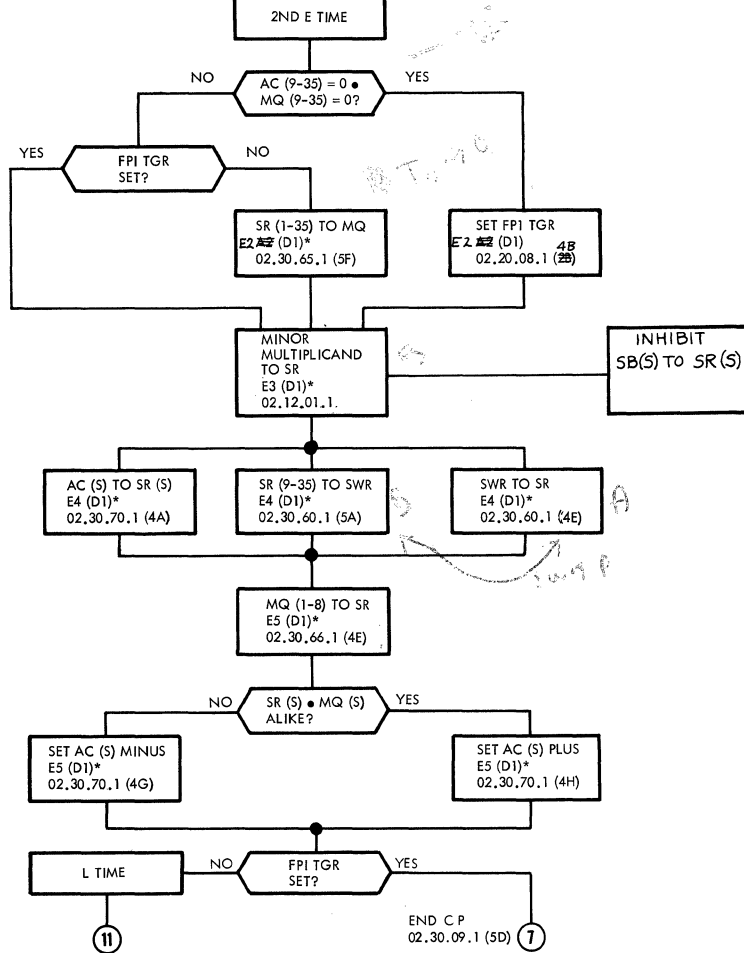




OBJECTIVES: (E TIME)
1. ZERO TEST MULTIPLIER
2. SAVE THE EFFECTIVE ADDRESS
3. SWAP FRACTION OF SR WITH MQ FOR 2ND E TIME
4. CHARACTER SR TO MQ



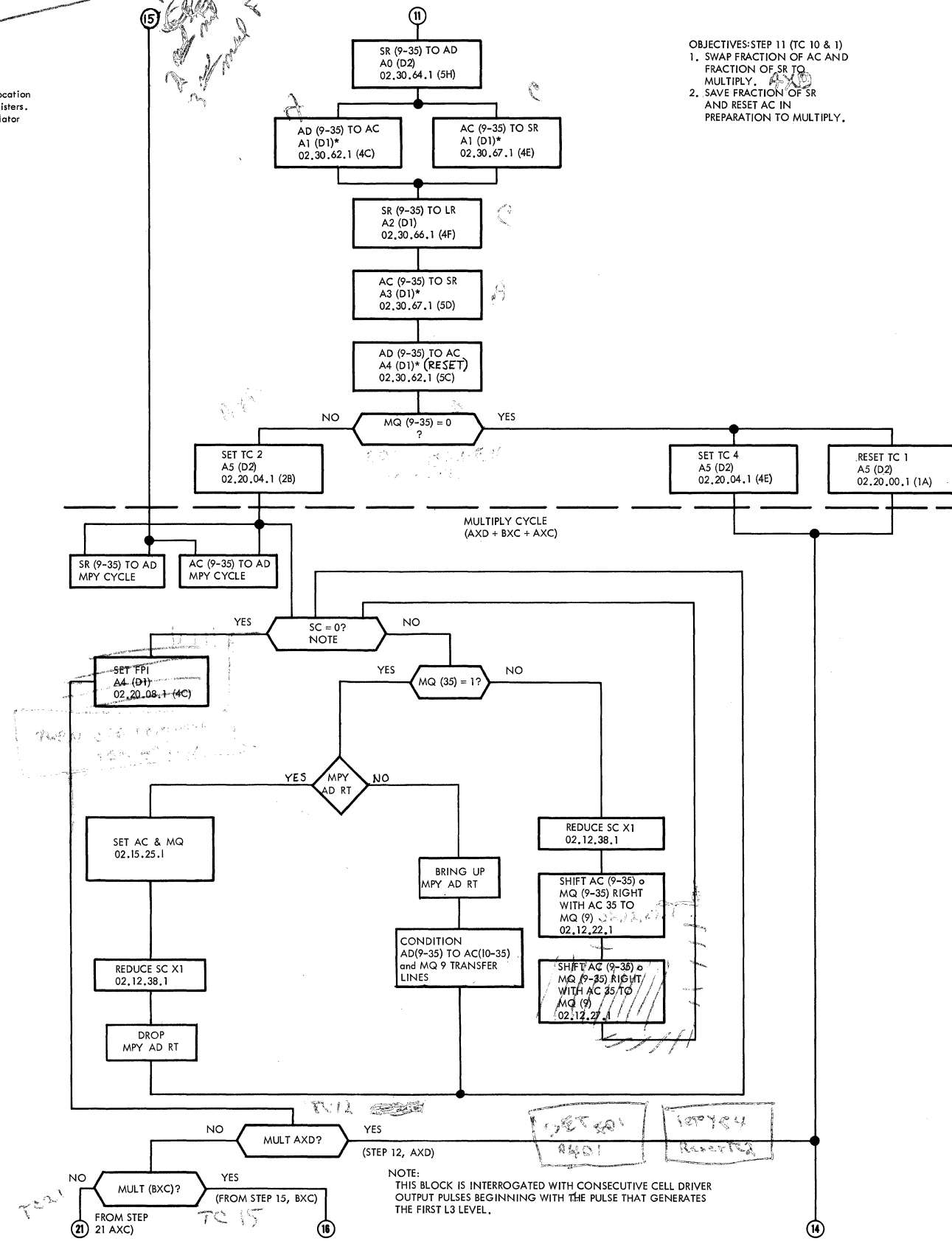
OBJECTIVES: (2ND E TIME)
1. ZERO TEST HIGH ORDER MULTIPLIER AND MULTIPLICAND
2. ORIGINAL FRACTION OF MQ BACK TO MQ
3. SWAP THE FRACTIONS OF THE EFFECTIVE ADDRESS AND EFFECTIVE ADDRESS + 1.
4. RESTORE SR CHARACTERISTIC
5. DETERMINE PRODUCT SIGN



* FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

FIGURE 13. DFMP

Double-Precision Floating Multiply (DFMP) (0261)
Multiplies the double-precision number in the specified memory location and location plus 1 by the number in the accumulator and MQ registers. The result is a normalized double-precision number in the accumulator and MQ registers with an associated algebraic sign.

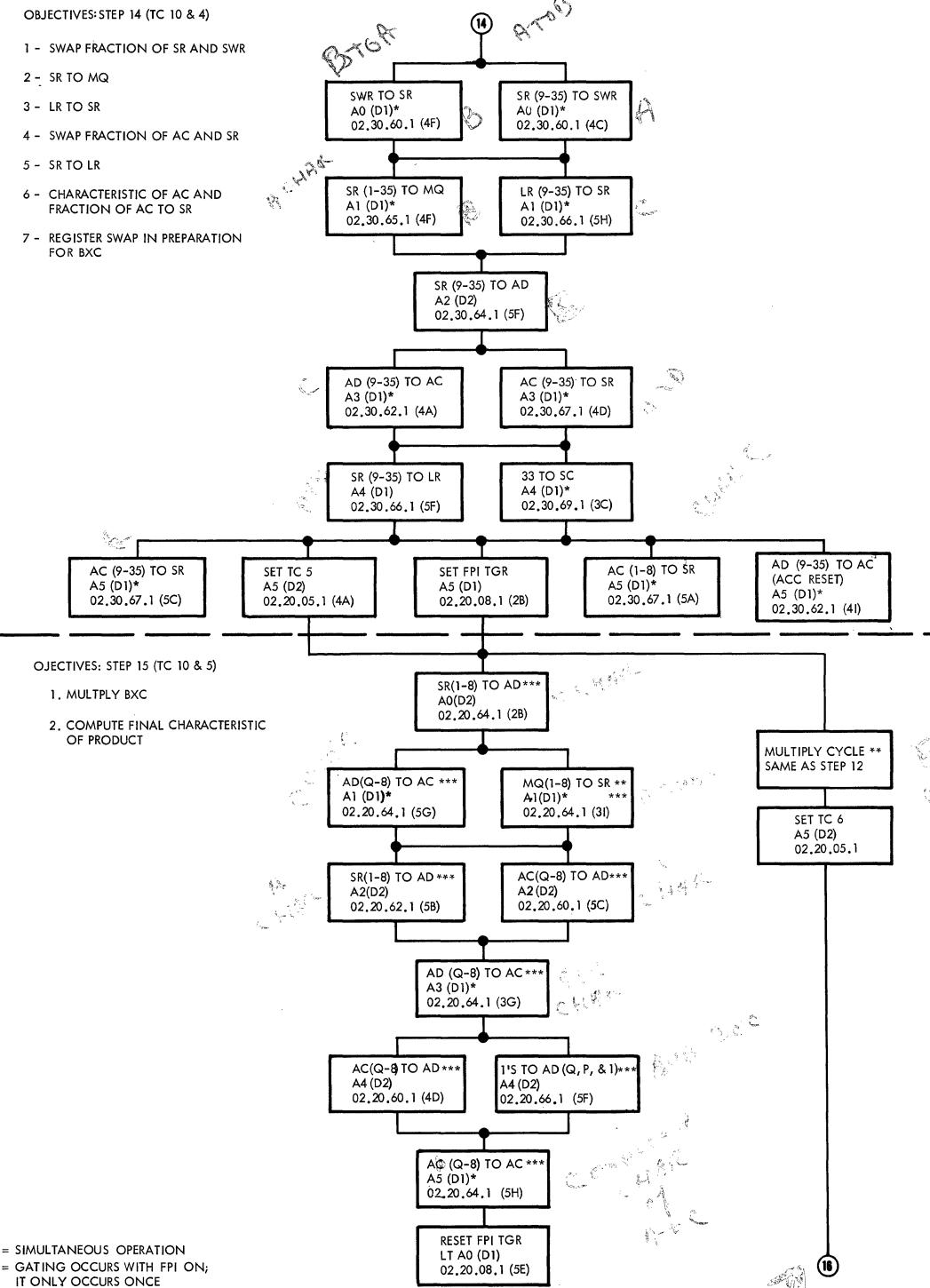


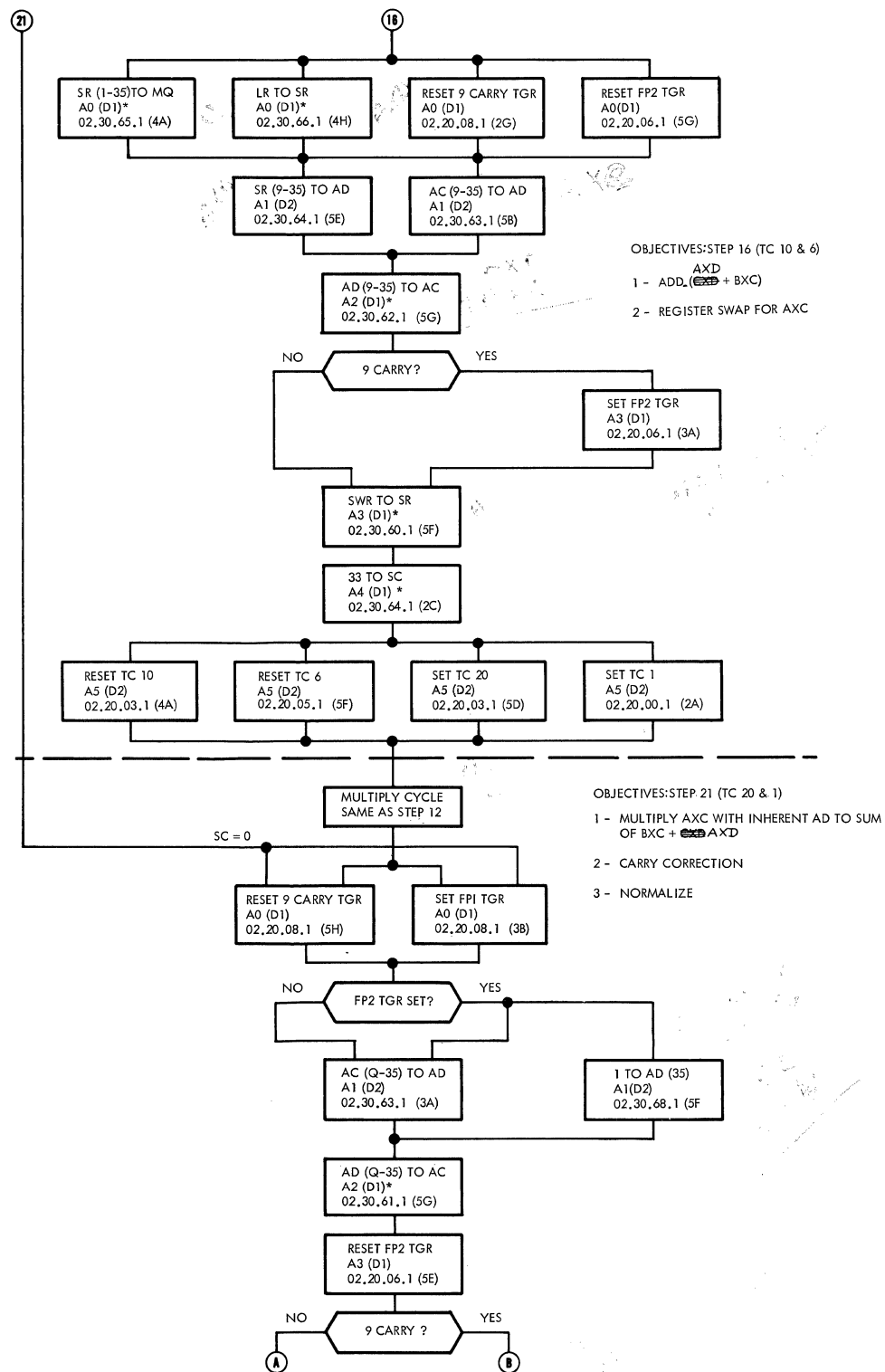
OBJECTIVES: STEP 11 (TC 10 & 1)
1. SWAP FRACTION OF AC AND FRACTION OF SR TO MULTIPLY.
2. SAVE FRACTION OF SR AND RESET AC IN PREPARATION TO MULTIPLY.

OBJECTIVES: STEP 14 (TC 10 & 4)
1 - SWAP FRACTION OF SR AND SWR
2 - SR TO MQ
3 - LR TO SR
4 - SWAP FRACTION OF AC AND SR
5 - SR TO LR
6 - CHARACTERISTIC OF AC AND FRACTION OF AC TO SR
7 - REGISTER SWAP IN PREPARATION FOR BXC

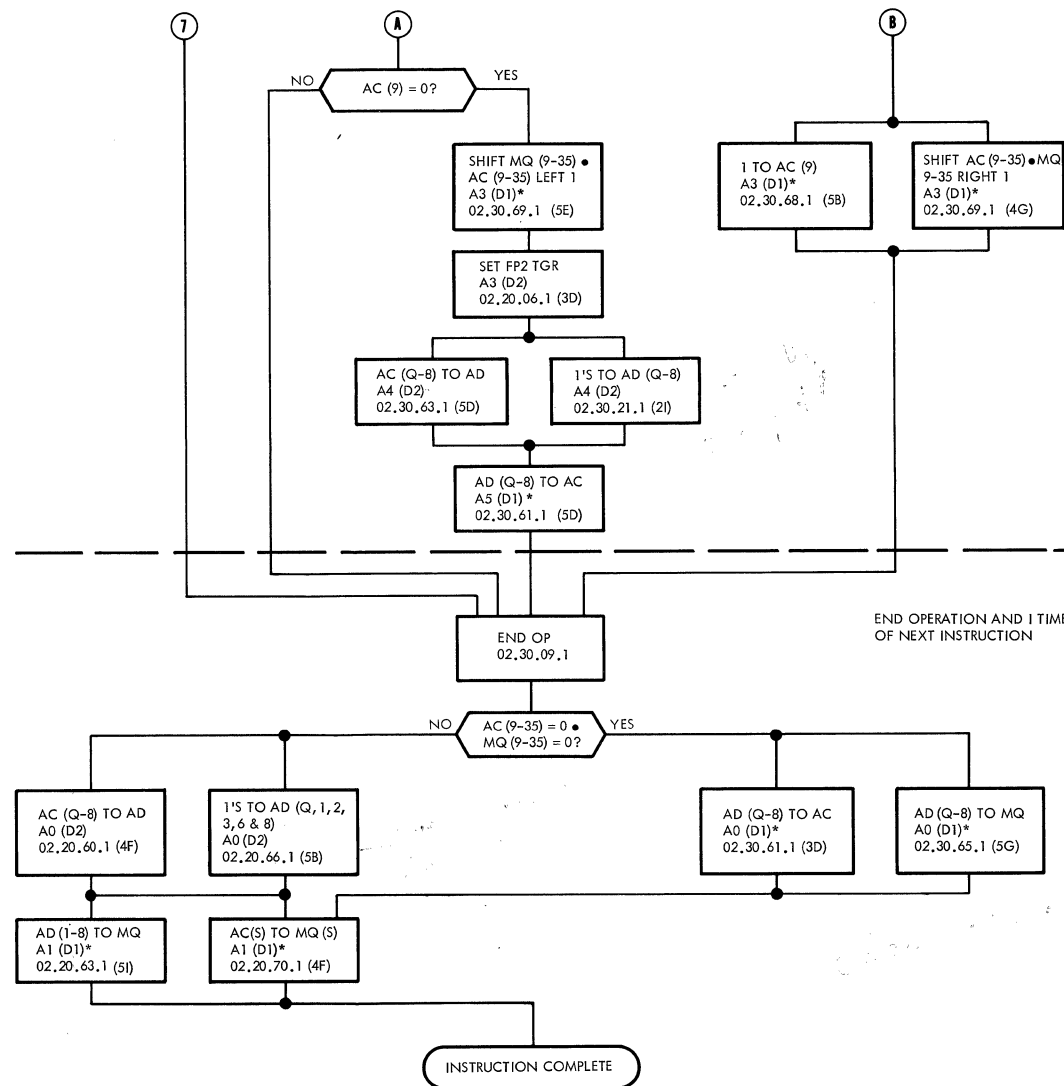
OBJECTIVES: STEP 15 (TC 10 & 5)
1. MULTIPLY BXC
2. COMPUTE FINAL CHARACTERISTIC OF PRODUCT

** = SIMULTANEOUS OPERATION
*** = GATING OCCURS WITH FPI ON; IT ONLY OCCURS ONCE



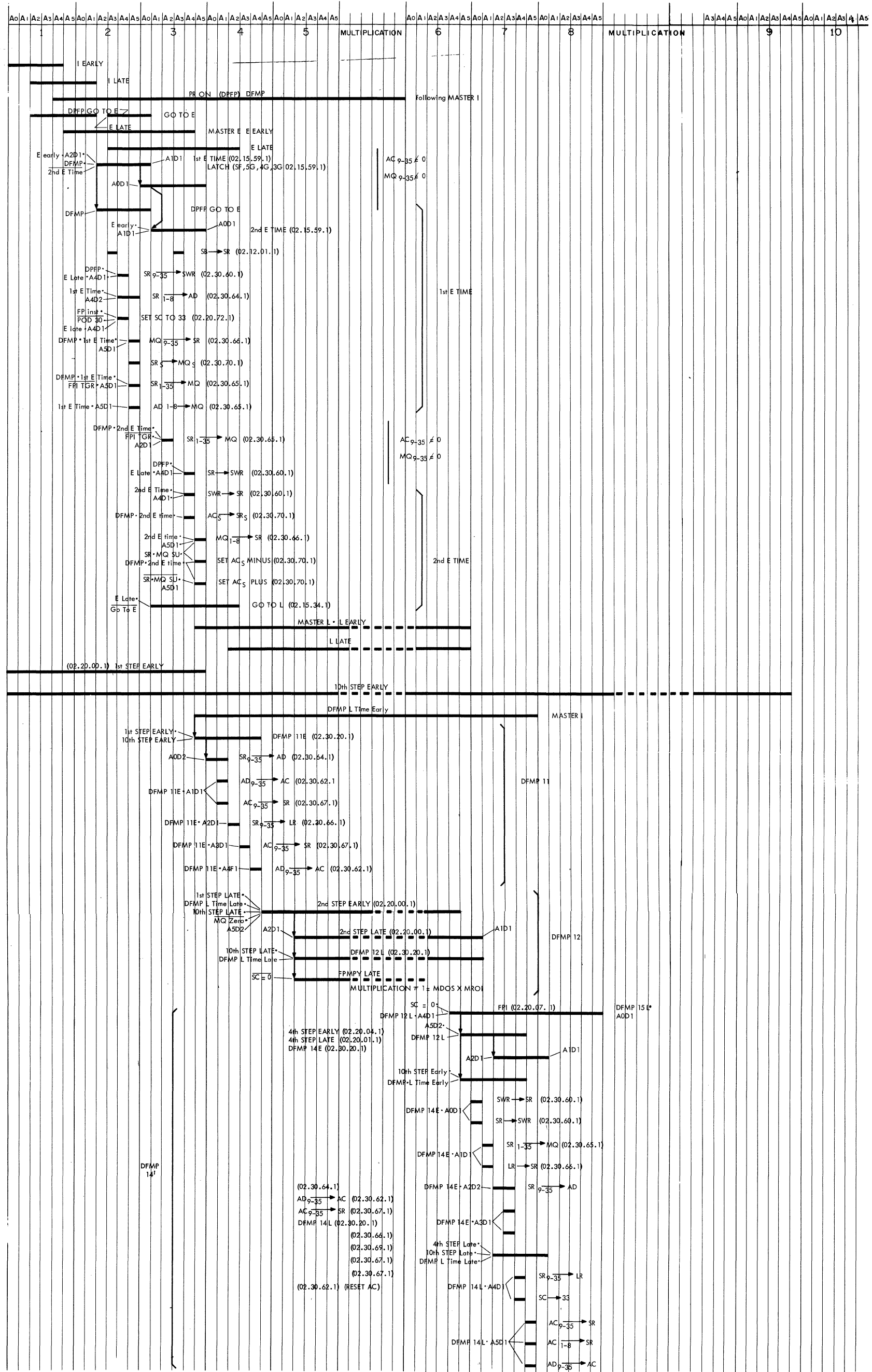


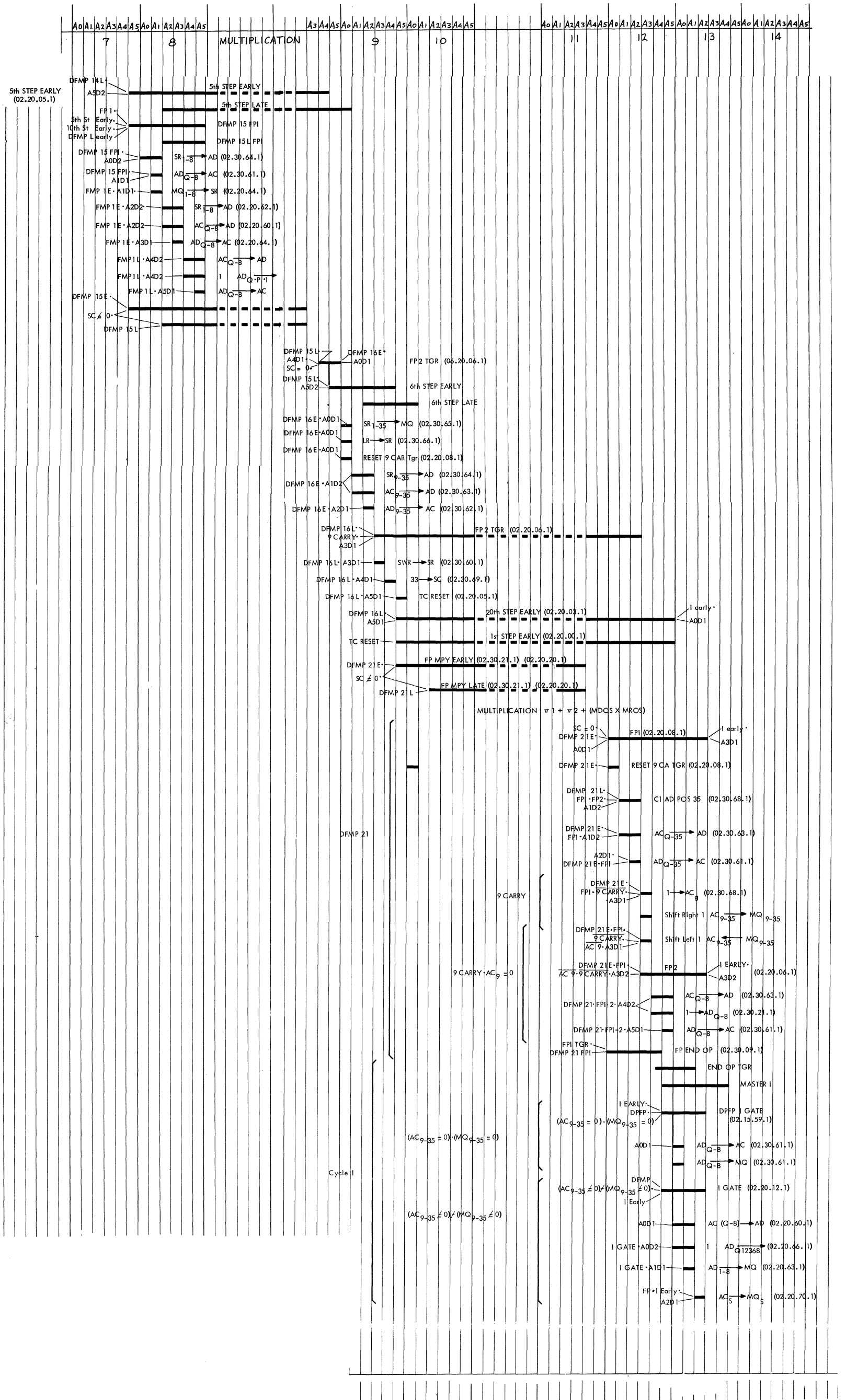
Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00004	050000 000004
00001	LDQ		00005	056000 000005
00002	DFMP		00004	026100 000004
00003	TRA		00000	002000 000000
00004	Pattern		211777	777777
00005	Pattern		200777	777777



Double Precision Floating Multiply (DFMP)														
CONSOLE INDICATORS														
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (A 1-35)	ACCUMULATOR (Q 1-35)	MQ REGISTER (M 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	X CARRY
I	E	00001	+500	000	0	00004	05000000000004	00000000000000	00	00000000000000				
E	I	00001	+500	000	0	00001	211777777777	211777777777	00	00000000000000				
I	E	00002	+560	000	0	00005	05600000000005	211777777777	00	00000000000000				
E	I	00002	+560	000	0	00002	200777777777	211777777777	00	200777777777				
I	E (1)	00003	+261	000	0	00004	02610000000004	211777777777	00	200777777777				
E (1)	E (2)	00003	+261	033	0	00005	211777777777	211777777777	00	211777777777				
E (2)	L (1)	00003	+261	033	0	00005	211777777777	211777777777	00	211777777777				
L (1)	L (2)	00003	+261	033	0	00005	211777777777	21100000000000	00	211777777777				
L (2)	L (3)	00003	+261	030	0	00005	211777777777	211677777777	00	211777777777				
L (3)	L (4)	00003	+261	025	0	00005	211777777777	211767777777	00	211017777777				
L (4)	L (5)	00003	+261	022	0	00005	211777777777	211767777777	00	211001777777				
L (5)	L (6)	00003	+261	017	0	00005	211777777777	211776777777	00	211000177777				
L (6)	L (7)	00003	+261	014	0	00005	211777777777	211777677777	00	211000017777				
L (7)	L (8)	00003	+261	011	0	00005	211777777777	211777767777	00	211000001777				
L (8)	L (9)	00003	+261	006	0	00005	211777777777	211777776777	00	211000000177				
L (9)	L (10)	00003	+261	003	0	00005	211777777777	211777777677	00	211000000017				
L (10)	L (11)	00003	+261	000	0	00005	211777777777	211777777776	00	211000000001				
L (11)	L (12)	00003	+261	000	0	00005	211777777777	211777777776	00	211000000001				
L (12)	L (13)	00003	+261	033	0	00005	211777777777	211000000000	00	211777777777				
L (13)	L (14)	00003	+261	030	0	00005	211777777777	222677777777	00	211777777777				
L (14)	L (15)	00003	+261	025	0	00005	211777777777	222767777777	00	211017777777				
L (15)	L (16)	00003	+261	022	0	00005	211777777777	222767777777	00	211001777777				
L (16)	L (17)	00003	+261	017	0	00005	211777777777	222767777777	00	211000177777				
L (17)	L (18)	00003	+261	014	0	00005	211777777777	222777677777	00	211000017777				
L (18)	L (19)	00003	+261	011	0	00005	211777777777	222777767777	00	211000001777				
L (19)	L (20)	00003	+261	006	0	00005	211777777777	222777776777	00	211000000177				
L (20)	L (21)	00003	+261	003	0	00005	211777777777	222777777677	00	211000000017				
L (21)	L (22)	00003	+261	000	0	00005	211777777777	222777777776	00	211000000001				
L (22)	L (23)	00003	+261	000	0	00005	211777777777	222777777776	00	211000000001				
L (23)	L (24)	00003	+261	033	0	00005	211777777777	222777777774	00	211777777777				
L (24)	L (25)	00003	+261	030	0	00005	211777777777	222777777776	00	211577777777				
L (25)	L (26)	00003	+261	025	0	00005	211777777777	222777777776	00	211757777777				
L (26)	L (27)	00003	+261	022	0	00005	211777777777	222777777776	00	211757777777				
L (27)	L (28)	00003	+261	017	0	00005	211777777777	222777777776	00	211775777777				
L (28)	L (29)	00003	+261	014	0	00005	211777777777	222777777776	00	211777577777				
L (29)	L (30)	00003	+261	011	0	00005	211777777777	222777777776	00	211777757777				
L (30)	L (31)	00003	+261	006	0	00005	211777777777	222777777776	00	211777757777				
L (31)	L (32)	00003	+261	003	0	00005	211777777777	222777777776	00	211777757777				
L (32)	L (33)	00003	+261	000	0	00005	211777777777	222777777776	00	211777757777				
L (33)	I	00003	+261	000	0	00003	211777777777	222777777776	00	211777757777				
I	I	00004	+020	000	0	00000	00200000000000	222777777777	00	167777777775				
E	E	00001	+500	000	0	00004	05000000000004	222777777777	00	167777777775				
E	I	00001	+500	000	0	00001	211777777777	211777777777	00	167777777775				
I	E	00002	+560	000	0	00005	05600000000005	211777777777	00	167777777775				
E	I	00002	+560	000	0	00002	200777777777	211777777777	00	200777777777				

FIGURE 13. DFMP
(CONTINUED)





Double-Precision Floating Divide or Proceed (DFPD -0241)
Divides the double-precision number in the accumulator and MQ (dividend)
by the double-precision number in the specified memory location and loca-
tion plus 1 (divisor). The result is a double quotient in the accumulator and
MQ registers with an associated algebraic sign.

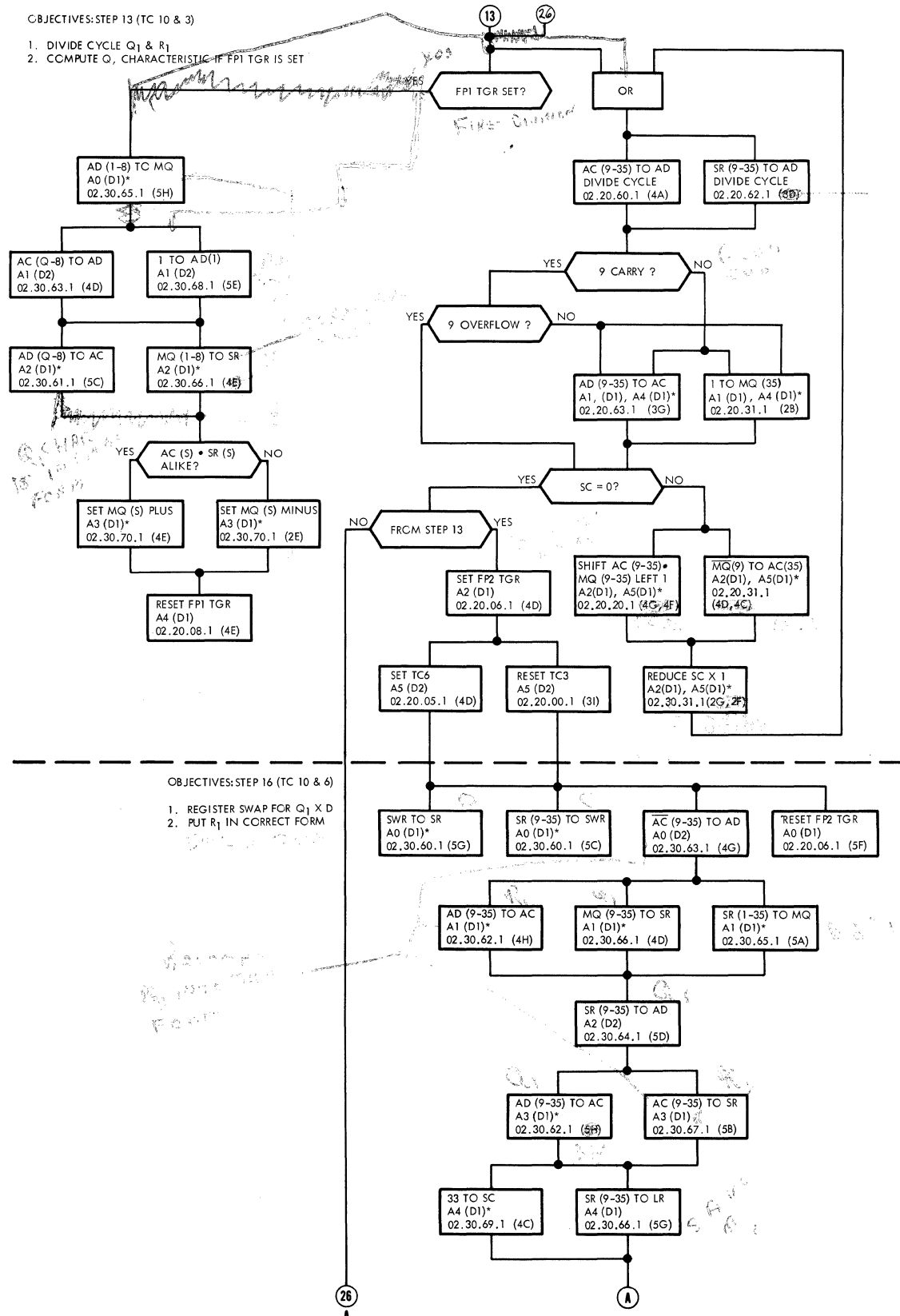
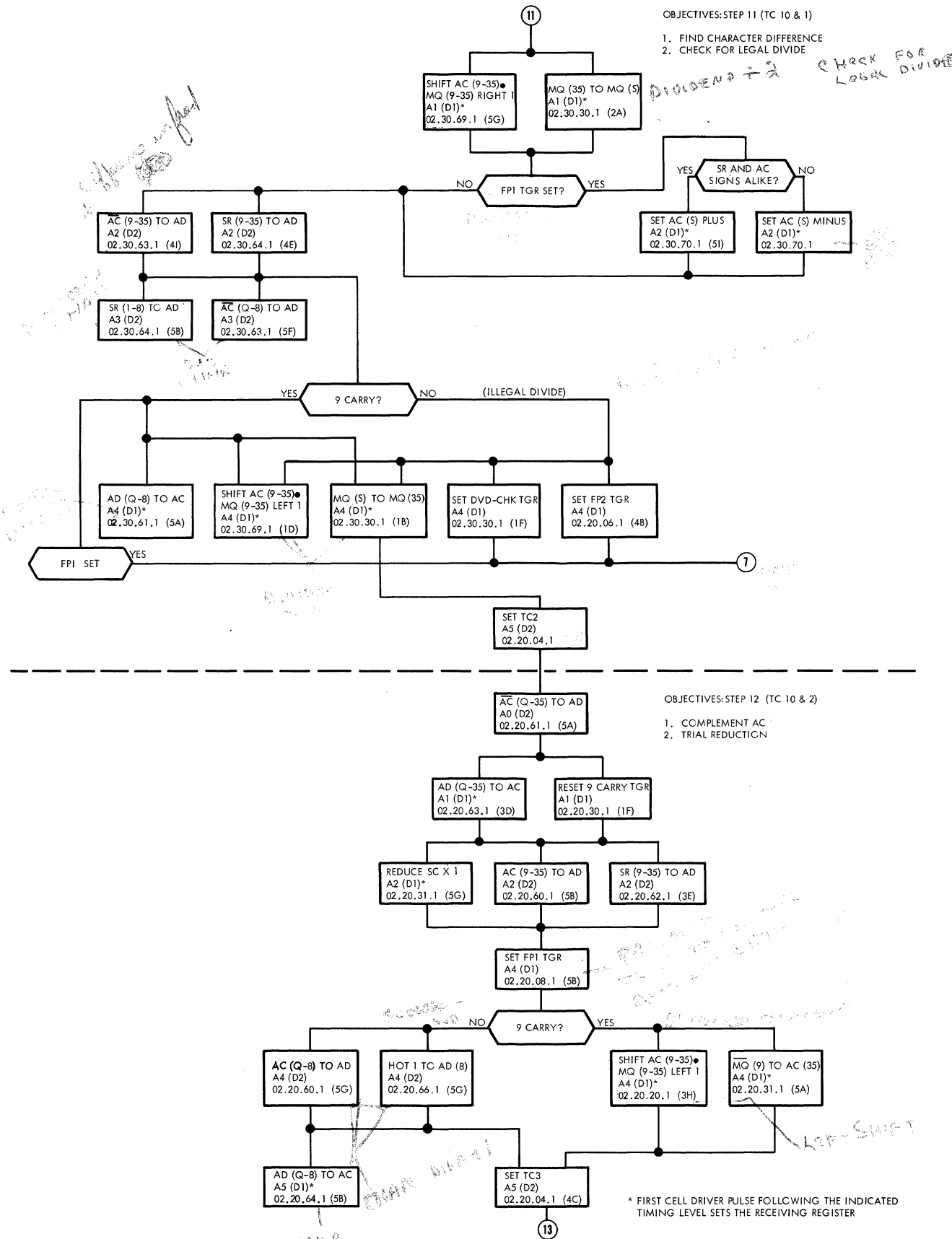
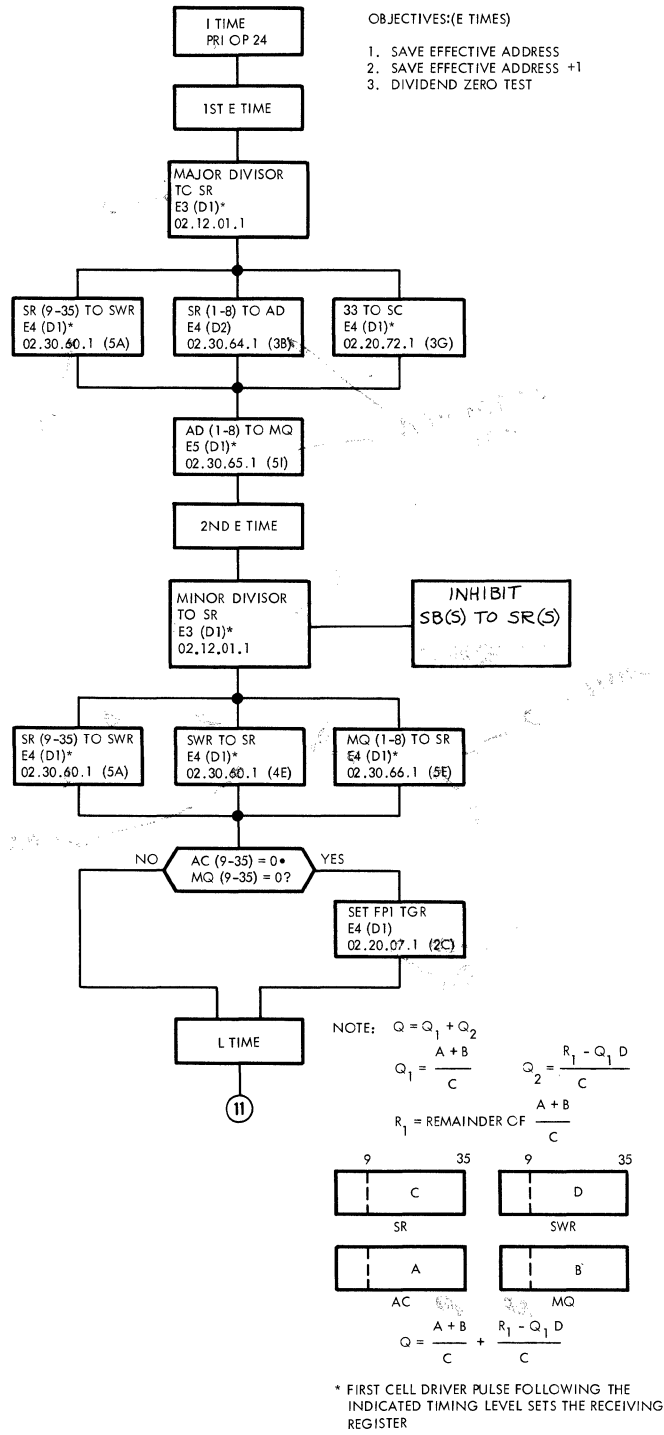
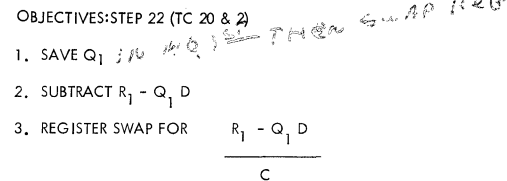
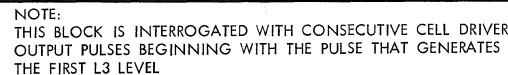
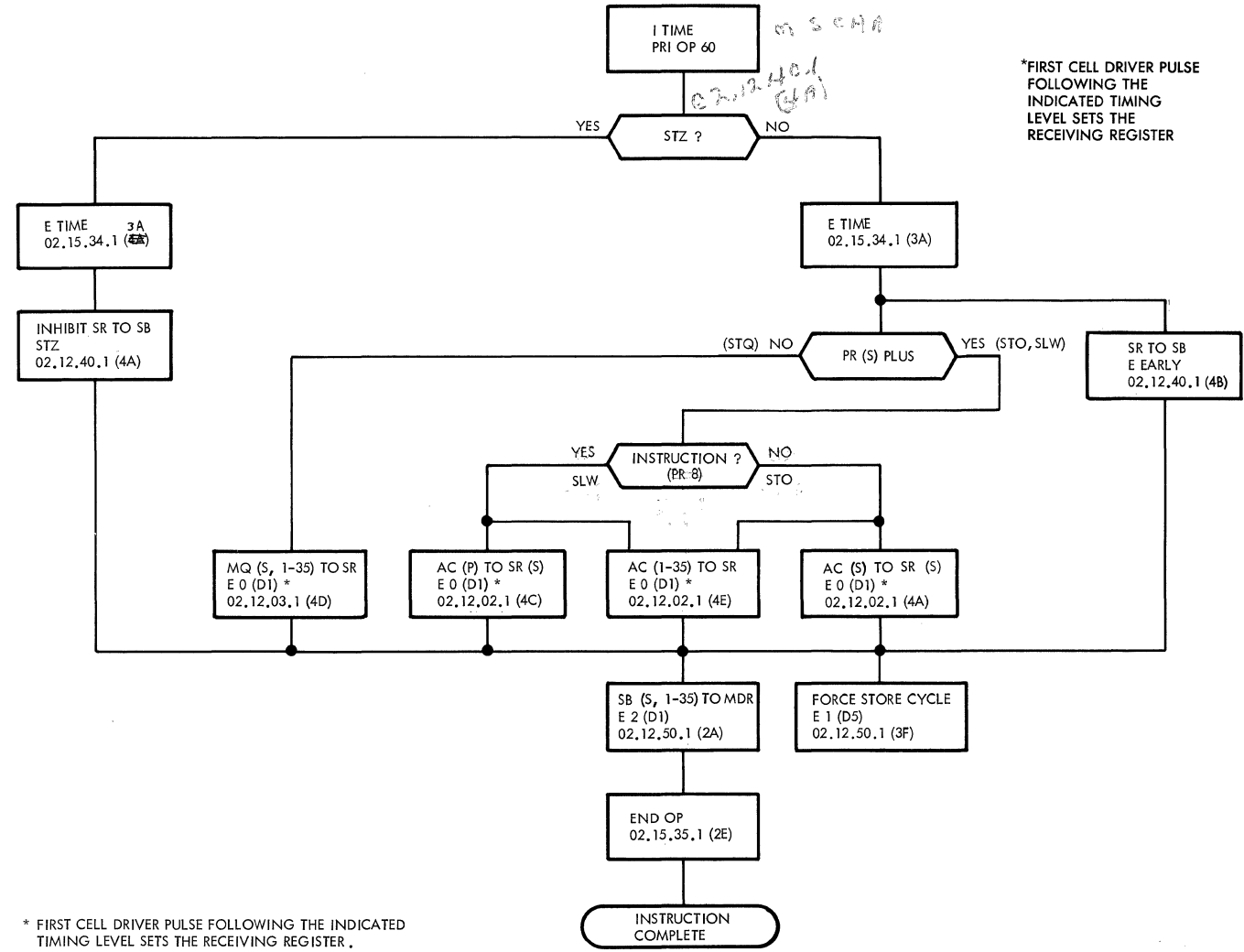
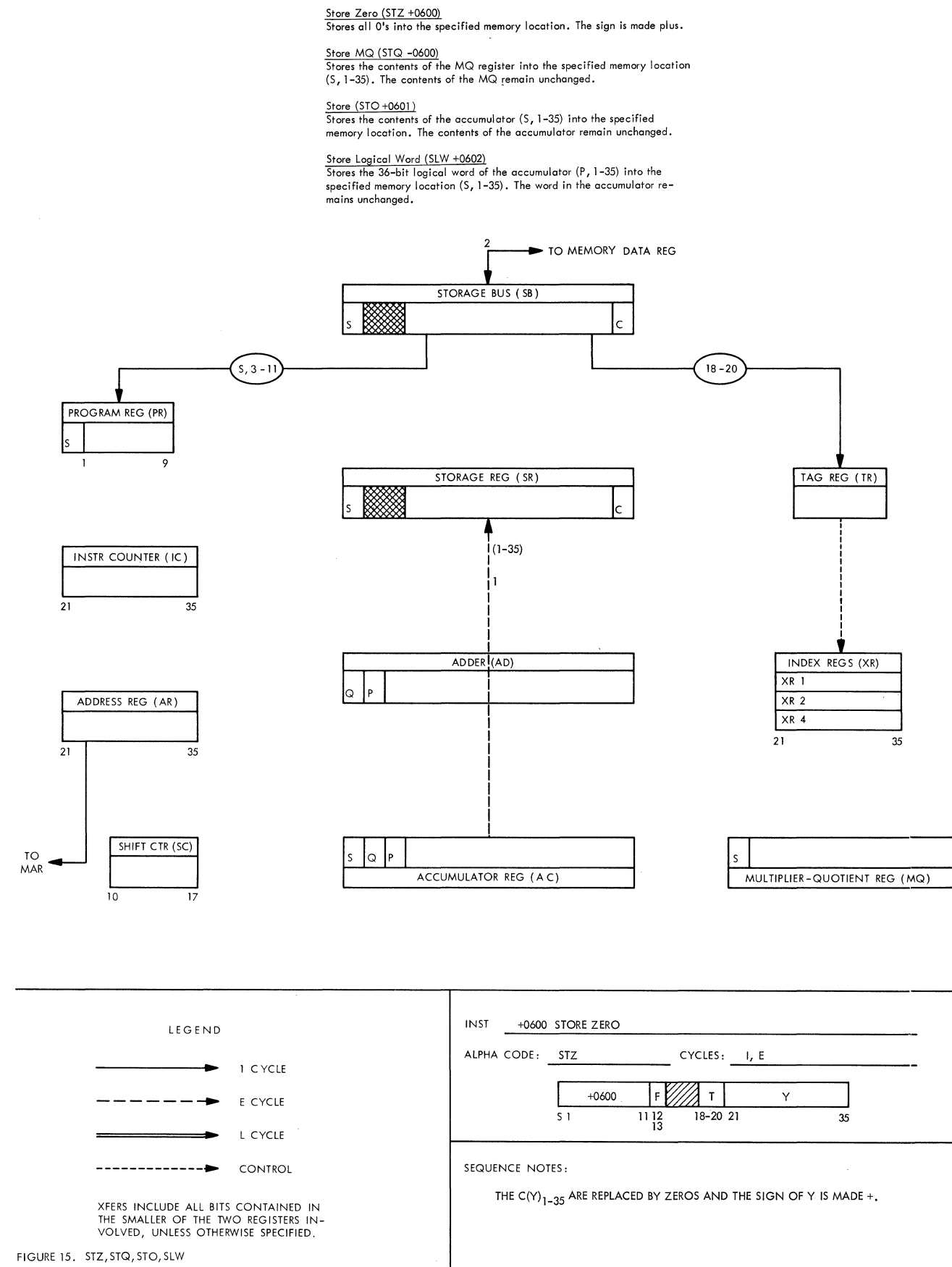


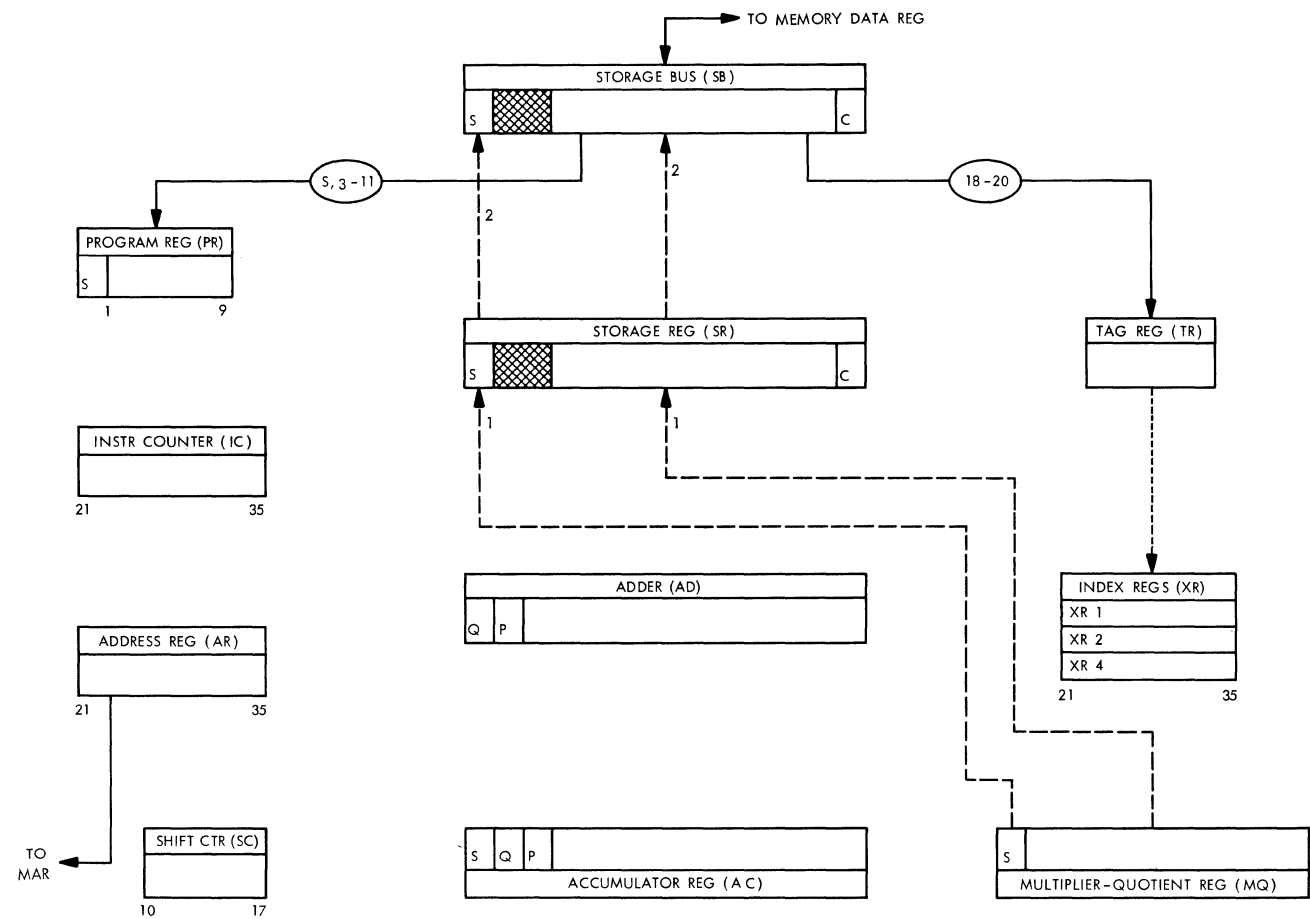
FIGURE 14. DFPD



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	LDQ		00006	056000 000006
00002	DFDP		00004	424100 000004
00003	TRA		00000	002000 000000
00004	Pattern			176777 777777
00005	Pattern			173777 777777
00006	Pattern			173777 777776

Double Precision Divide and Proceed (DFDP)																
CONSOLE INDICATORS																
Cycle Executed	Cycle Time	Instruction Counter	Instruction Shift Counter	Tag	Address	Storage Register (5 1-35)	Accumulator (5 1-35)	Accumulator (Q, P)	MO Register (5 1-35)	Tally Counter	Index Register	Position Register	Accu Overflow	Divide Check	X Carry	P Carry
I	E	00001	+500	000	0	00005	050000000005	000000000000	00	000000000000						
E	I	00001	+500	000	0	00001	173777777777	173777777777	00	000000000000						
I	E	00002	+560	000	0	00006	056000000006	173777777777	00	000000000000						
E	I	00002	+560	000	0	00002	173777777776	173777777777	00	173777777776						
I	E(1)	00003	-241	000	0	00004	424100000004	173777777777	00	173777777776	1 & 10					
E(1)	E(2)	00003	-241	033	0	00005	176777777777	173777777777	00	176777777776	1 & 10					
E(2)	L(1)	00003	-241	033	0	00005	176777777777	173777777777	00	176777777776	1 & 10					
L(1)	L(2)	00003	-241	033	0	00005	176777777777	002777777777	00	176777777776	2 & 10				1	
L(2)	L(3)	00003	-241	032	0	00005	176777777777	376000000000	11	176777777776	3 & 10				0	1
L(3)	L(4)	00003	-241	030	0	00005	000777777777	176777777774	00	000777777774	3 & 10				1	1
L(4)	L(5)	00003	-241	026	0	00005	000777777777	176777777760	00	000777777760	3 & 10				1	1
L(5)	L(6)	00003	-241	024	0	00005	000777777777	176777777700	00	000777777700	3 & 10				1	1
L(6)	L(7)	00003	-241	022	0	00005	000777777777	176777777400	00	000777777400	3 & 10				1	1
L(7)	L(8)	00003	-241	020	0	00005	000777777777	176777776000	00	000777776000	3 & 10				1	1
L(8)	L(9)	00003	-241	016	0	00005	000777777777	176777770000	00	000777770000	3 & 10				1	1
L(9)	L(10)	00003	-241	014	0	00005	000777777777	176777740000	00	000777740000	3 & 10				1	1
L(10)	L(11)	00003	-241	012	0	00005	000777777777	176777600000	00	000777600000	3 & 10				1	1
L(11)	L(12)	00003	-241	010	0	00005	000777777777	176777000000	00	000777000000	3 & 10				1	1
L(12)	L(13)	00003	-241	006	0	00005	000777777777	176774000000	00	000774000000	3 & 10				1	1
L(13)	L(14)	00003	-241	004	0	00005	000777777777	176760000000	00	000760000000	3 & 10				1	1
L(14)	L(15)	00003	-241	002	0	00005	000777777777	176700000000	00	000700000000	3 & 10				1	1
L(15)	L(16)	00003	-241	000	0	00005	000777777777	176400000000	00	000400000000	3 & 10				1	1
L(16)	L(17)	00003	-241	000	0	00005	000777777777	176400000000	00	000400000000	6 & 10				1	1
L(17)	L(18)	00003	-241	033	0	00005	000400000000	176000000000	00	000777777777	1 & 20				1	
L(18)	L(19)	00003	-241	030	0	00005	000400000000	176340000000	00	000077777777	1 & 20				1	
L(19)	L(20)	00003	-241	025	0	00005	000400000000	176340000000	00	000007777777	1 & 20				1	
L(20)	L(21)	00003	-241	022	0	00005	000400000000	176377400000	00	000000777777	1 & 20				1	
L(21)	L(22)	00003	-241	017	0	00005	000400000000	176377740000	00	000000077777	1 & 20				1	
L(22)	L(23)	00003	-241	014	0	00005	000400000000	17637774000	00	000000007777	1 & 20				1	
L(23)	L(24)	00003	-241	011	0	00005	000400000000	17637777400	00	000000000777	1 & 20				1	
L(24)	L(25)	00003	-241	006	0	00005	000400000000	17637777740	00	000000000077	1 & 20				1	
L(25)	L(26)	00003	-241	003	0	00005	000400000000	17637777774	00	000000000007	1 & 20				1	
L(26)	L(27)	00003	-241	000	0	00005	000400000000	176377777777	00	000000000000	1 & 20				1	
L(27)	L(28)	00003	-241	000	0	00005	000400000000	176377777777	00	000400000000	2 & 20					1
L(28)	L(29)	00003	-241	000	0	00005	000777777777	176000000000	00	000000000000	4 & 20					
L(29)	L(30)	00003	-241	033	0	00005	000777777777	201000000000	11	000000000000	5 & 20				1	
L(30)	L(31)	00003	-241	032	0	00005	000777777777	176777777777	00	000000000000	6 & 20				1	1
L(31)	L(32)	00003	-241	030	0	00005	000777777777	176777777777	00	000000000000	6 & 20				1	1
L(32)	L(33)	00003	-241	026	0	00005	000777777777	176777777777	00	000000000000	6 & 20				1	1
L(33)	L(34)	00003	-241	024	0	00005	000777777777	176777777777	00	000000000000	6 & 20				1	1
L(34)	L(35)	00003	-241	022	0	00005	000777777777	176777777777	00	000000000000	6 & 20				1	1
L(35)	L(36)	00003	-241	020	0	00005	000777777777	176777777777	00	000000000000	6 & 20				1	1
L(36)	L(37)	00003	-241	016	0	00005	000777777777	176777777777	00	000000000000	6 & 20				1	1
L(37)	L(38)	00003	-241	014	0	00005	000777777777	176777777777	00	000000000000	6 & 20				1	1
L(38)	L(39)	00003	-241	012	0	00005	000777777777	176777777777	00	000000000000	6 & 20				1	1
L(39)	L(40)	00003	-241	010	0	00005	000777777777	176777777777	00	000000000000	6 & 20				1	1
L(40)	L(41)	00003	-241	006	0	00005	000777777777	176777777777	00	000000000000	6 & 20				1	1
L(41)	L(42)	00003	-241	004	0	00005	000777777777	176777777777	00	000000000000	6 & 20				1	1
L(42)	L(43)	00003	-241	002	0	00005	000777777777	176777777777	00	000000000000	6 & 20				1	1
L(43)	L(44)	00003	-241	000	0	00005	000777777777	176777777777	00	000000000000	6 & 20				1	1
L(44)	L(45)	00003	-241	000	0	00005	000400000000	176000000000	00	000000000000	3 & 30				1	1
L(45)	I	00003	-241	000	0	00003	000400000000	176400000000	00	000000000000	3 & 30					
I	I	00004	+020	000	0	00000	002000000000	176400000000	00	143000000000						
I	E	00001	+500	000	0	00005	050000000005	176400000000	00	143000000000						
E	I	00001	+500	000	0	00001	173777777777	173777777777	00	143000000000						
I	E	00002	+560	000	0	00006	056000000006	173777777777	00	143000000000						





LEGEND

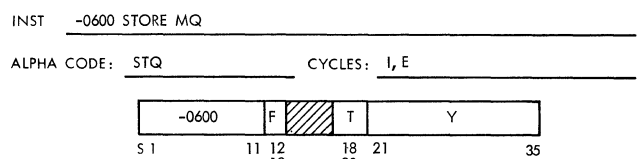
→ 1 CYCLE

--- E CYCLE

== L CYCLE

----- CONTROL

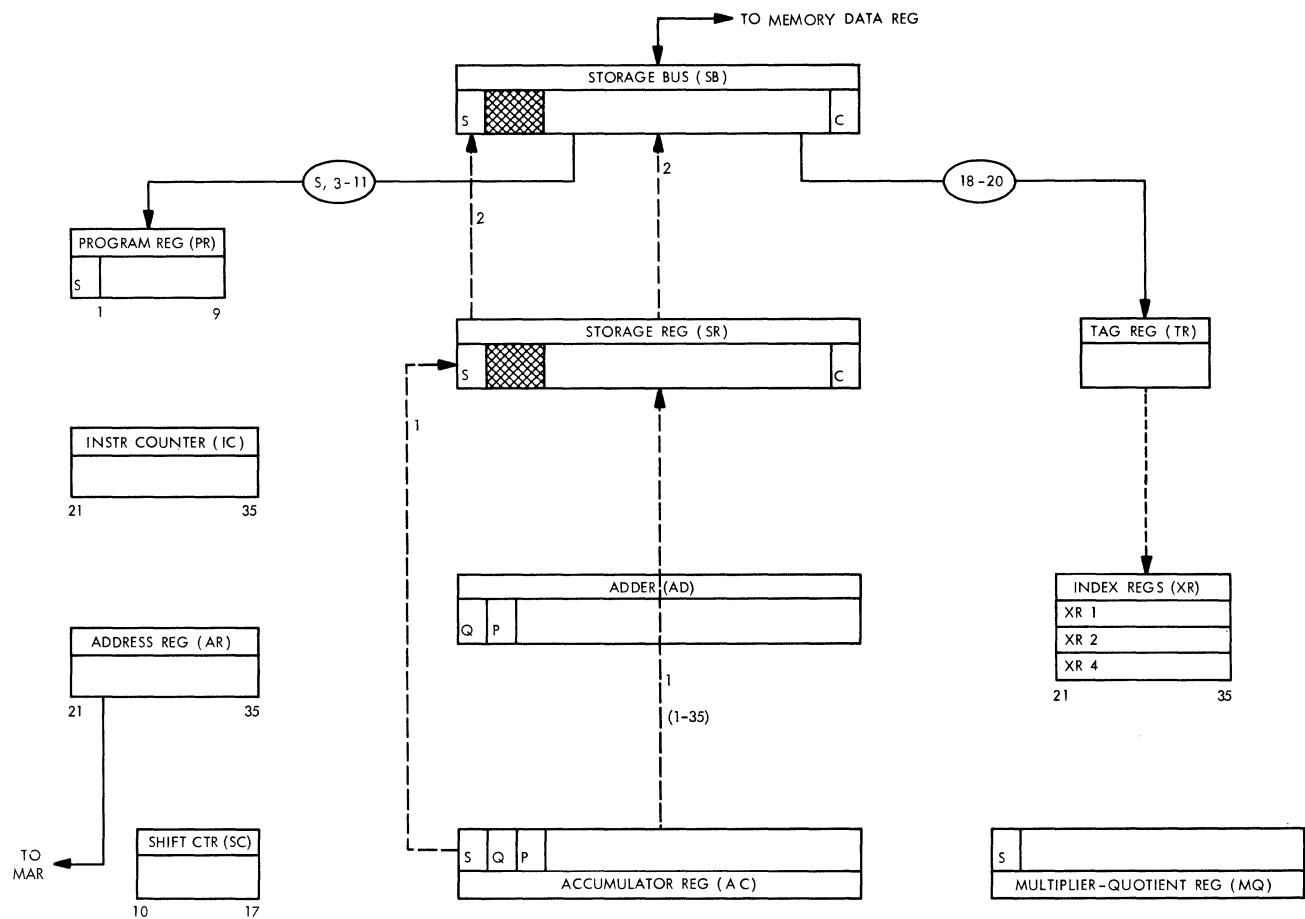
XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.



SEQUENCE NOTES:

THE C(MQ)_{S-35} ARE PLACED INTO THE SPECIFIED Y LOCATION.

THE C(MQ) REMAIN UNCHANGED.



LEGEND

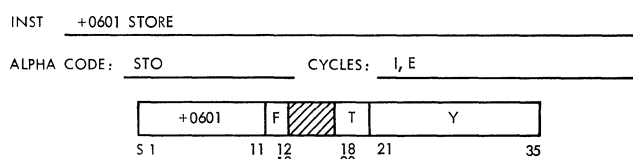
→ 1 CYCLE

--- E CYCLE

== L CYCLE

----- CONTROL

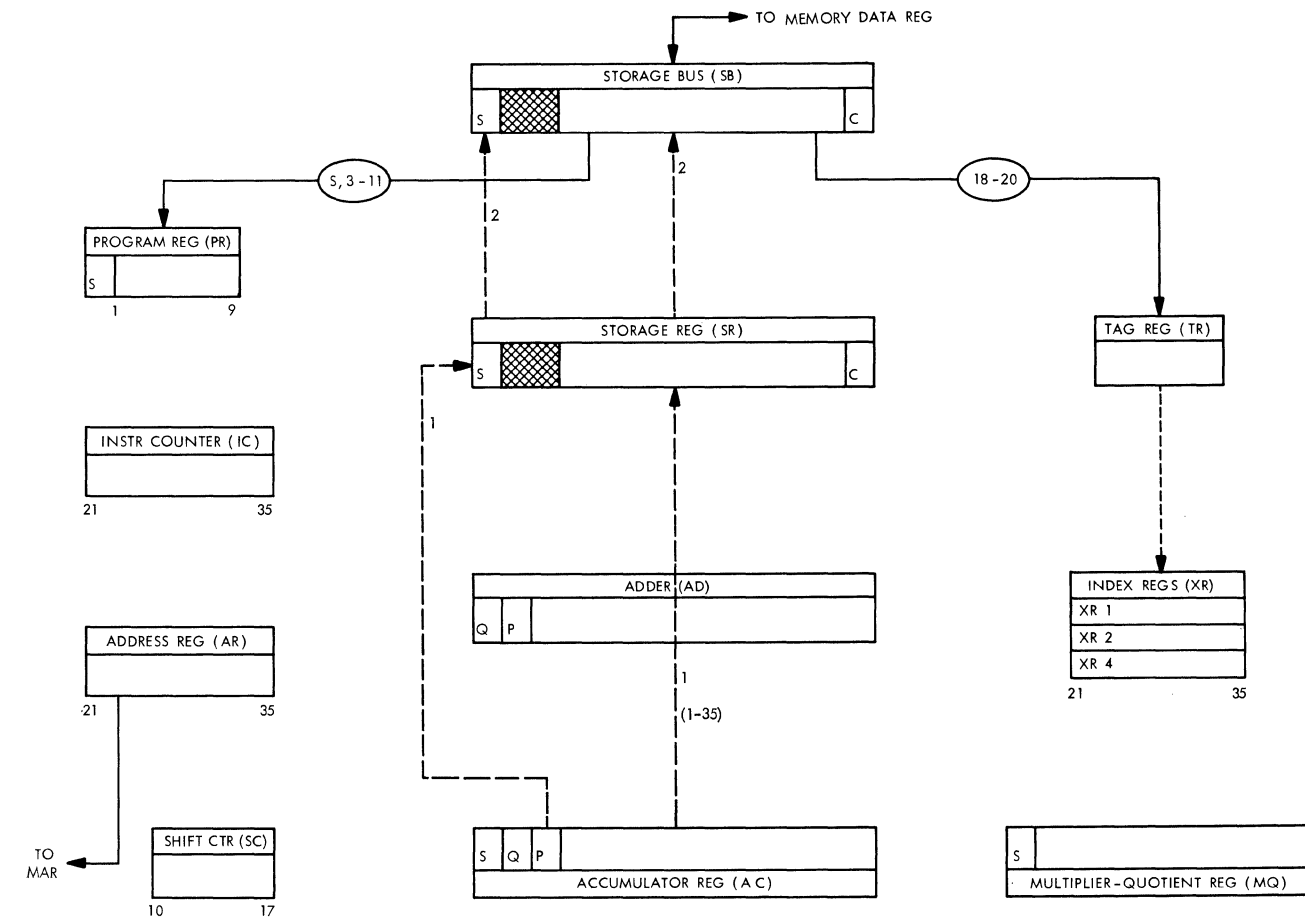
XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.



SEQUENCE NOTES:

THE C(AC)_{S, 1-35} ARE PLACED INTO LOCATION Y.

THE C(AC) ARE UNCHANGED.



LEGEND

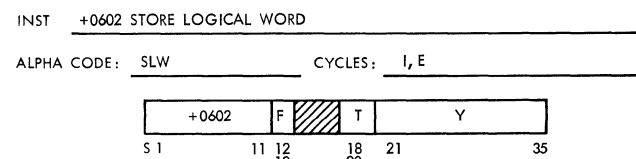
→ 1 CYCLE

--- E CYCLE

== L CYCLE

----- CONTROL

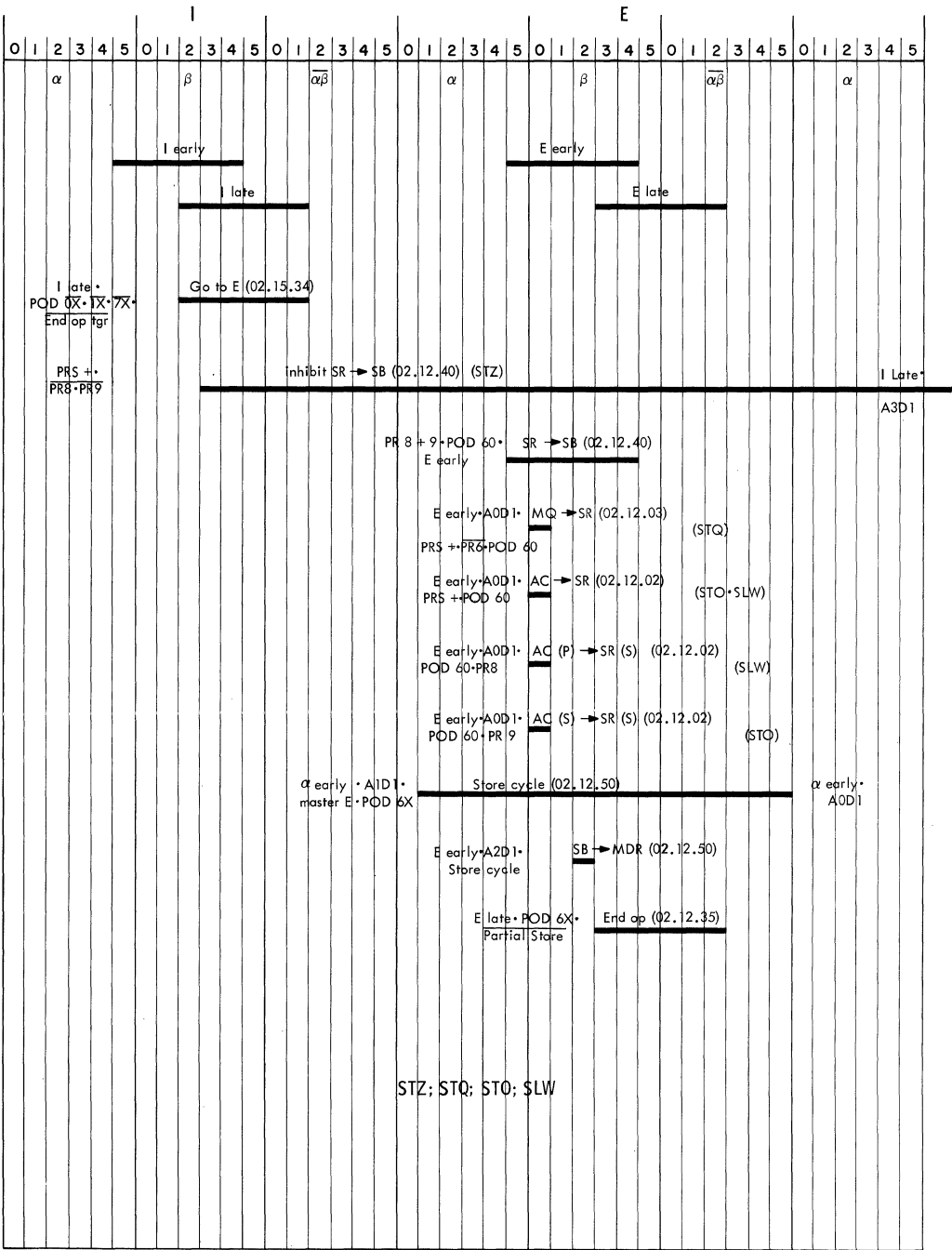
XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.



SEQUENCE NOTES:

THE C(AC)_{P, 1-35} ARE PLACED INTO LOCATION Y.

THE C(AC) ARE UNCHANGED.



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STO		00007	060100 000007
00002	LDQ		00007	056000 000007
00003	STZ		00007	060000 000007
00004	LDQ		00007	056000 000007
00005	TRA		00007	002000 000000
00006	Pattern Live Reg			777777 777777
00007				

Location Switches	Inst	Tag	Address	Octal Equiv
00000	LDQ		00006	056000 000006
00001	STQ		00007	460000 000007
00002	CLA		00007	050000 000007
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern Live Reg			777777 777777
00007				

Store Zeros (STZ)									
CONSOLE INDICATORS									
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	Address	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	MQ REGISTER (M, 1-35)	TALLY COUNTER
I	E	00001	+500	000	0	00006	0500000000006	0000000000000	00
E	I	00001	+500	000	0	00001	7777777777777	7777777777777	00
I	E	00002	+601	000	0	00007	0601000000000	7777777777777	00
E	I	00002	+601	000	0	00002	7777777777777	7777777777777	00
I	E	00003	+560	000	0	00007	0560000000007	7777777777777	00
E	I	00003	+560	000	0	00003	7777777777777	7777777777777	00
I	E	00004	+600	000	0	00007	0600000000007	7777777777777	00
E	I	00004	+600	000	0	00004	0000000000000	7777777777777	00
I	E	00005	+560	000	0	00007	0560000000007	7777777777777	00
E	I	00005	+560	000	0	00005	0000000000000	7777777777777	00
I	I	00006	+020	000	0	00000	0020000000000	7777777777777	00
I	E	00001	+500	000	0	00006	0500000000006	7777777777777	00

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STO		00007	060100 000007
00002	LDQ		00007	056000 000007
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern Live Reg			777777 777777
00007				

Store MQ (STQ)									
CONSOLE INDICATORS									
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	Address	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	MQ REGISTER (M, 1-35)	TALLY COUNTER
I	E	00001	+560	000	0	00006	0560000000006	0000000000000	00
E	I	00001	+560	000	0	00001	7777777777777	0000000000000	00
I	E	00002	-600	000	0	00007	4600000000007	0000000000000	00
E	I	00002	-600	000	0	00002	7777777777777	0000000000000	00
I	E	00003	+500	000	0	00007	0500000000007	0000000000000	00
E	I	00003	+500	000	0	00003	7777777777777	7777777777777	00
I	I	00004	+020	000	0	00000	0020000000000	7777777777777	00
I	E	00001	+560	000	0	00006	0560000000006	7777777777777	00
E	I	00001	+560	000	0	00001	7777777777777	7777777777777	00
I	E	00002	-600	000	0	00007	4600000000007	7777777777777	00
E	I	00002	-600	000	0	00002	7777777777777	7777777777777	00
I	E	00003	+500	000	0	00007	0500000000007	7777777777777	00

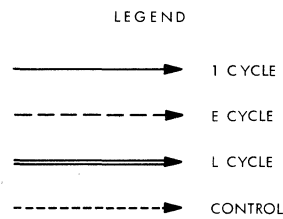
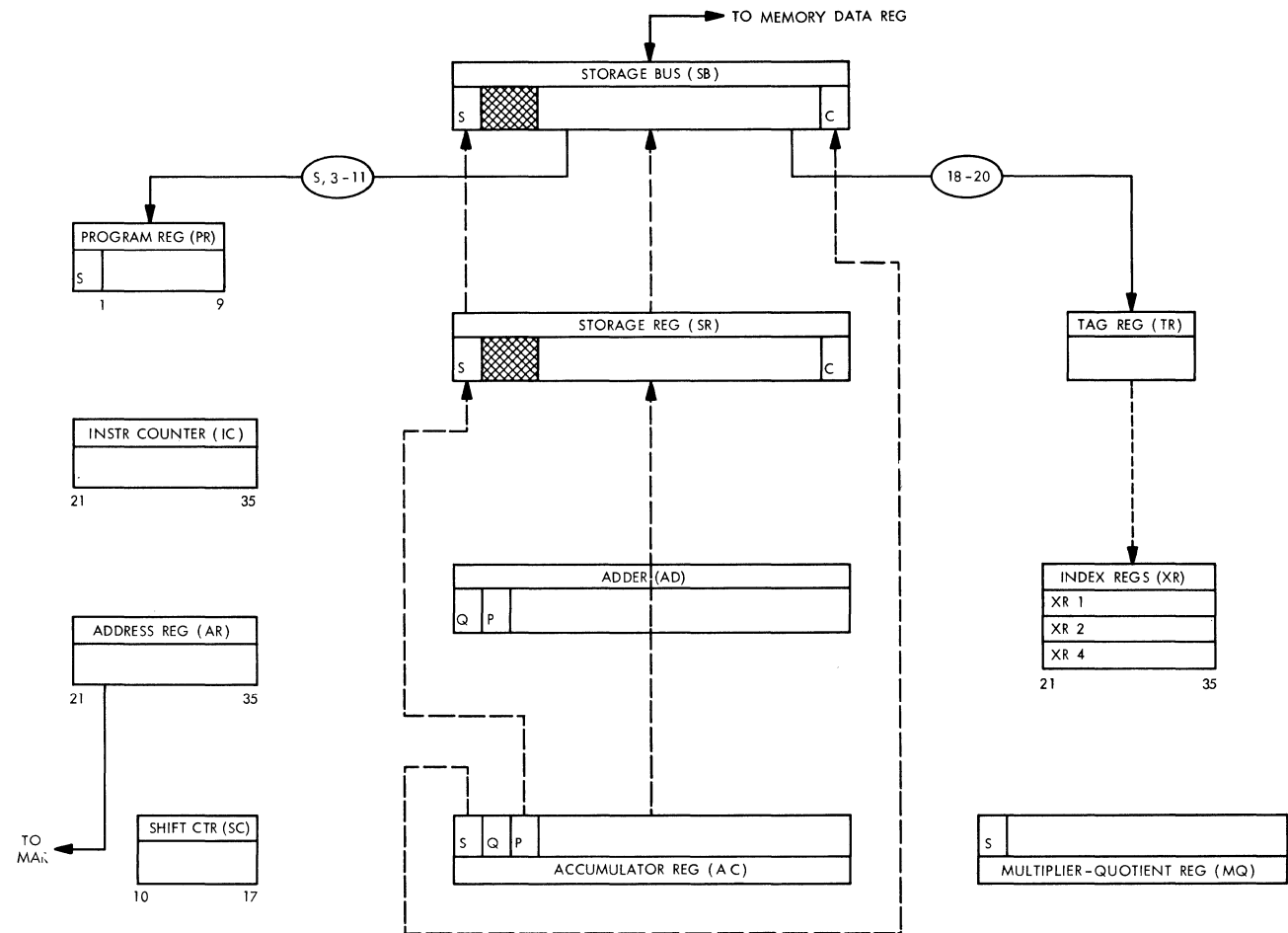
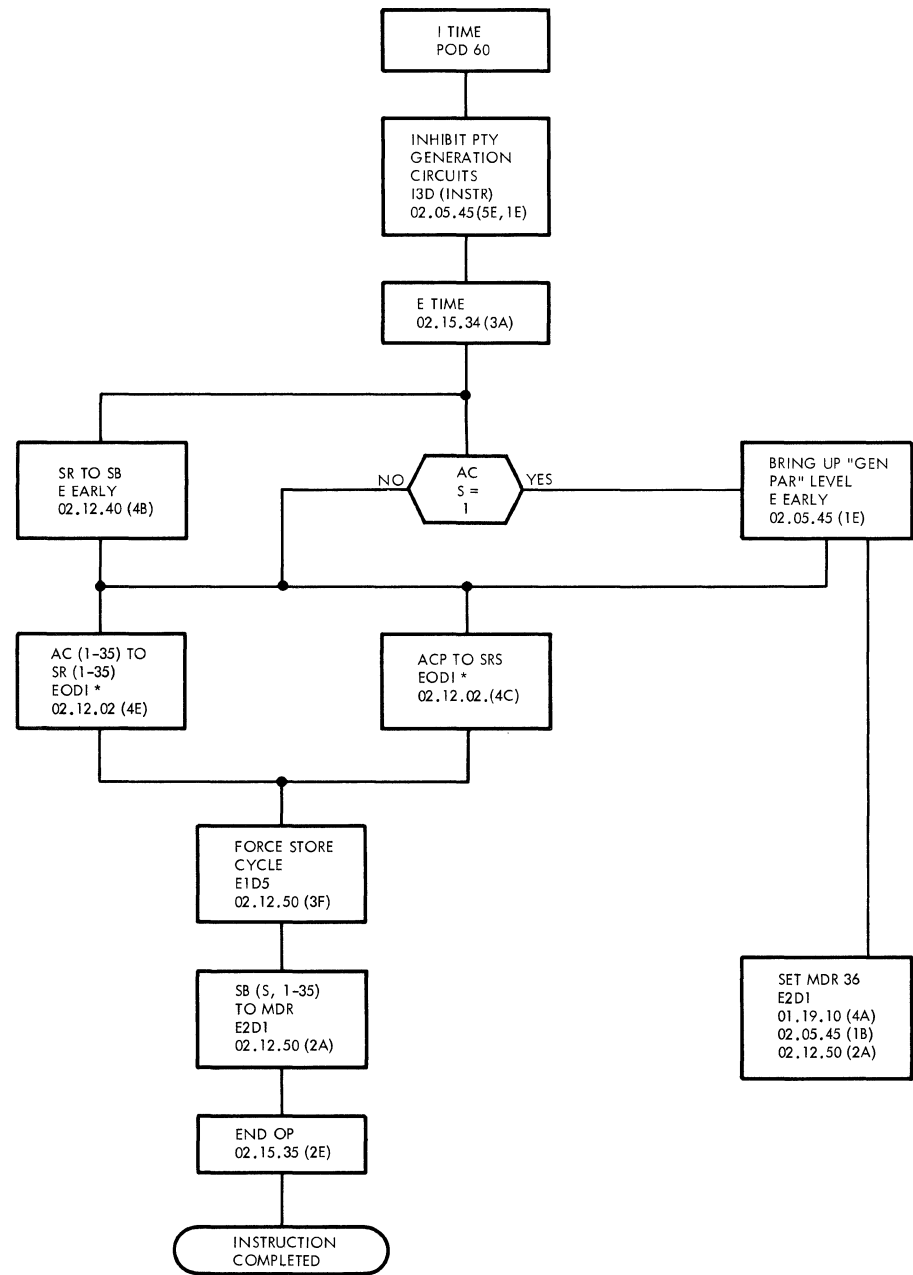
Location Switches	Inst	Tag	Address	Octal Equiv
00000	CAL		00006	450000 000006
00001	SLW		00007	060200 000007
00002	LDQ		00007	056000 000007
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern Live Reg			631463 146314
00007				

Store Accumulator (STO)									
CONSOLE INDICATORS									
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	Address	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	MQ REGISTER (M, 1-35)	TALLY COUNTER
I	E	00001	+500	000	0	00006	0500000000006	0000000000000	00
E	I	00001	+500	000	0	00001	7777777777777	7777777777777	00
I	E	00002	+601	000	0	00007	0601000000007	7777777777777	00
E	I	00002	+601	000	0	00002	7777777777777	7777777777777	00
I	E	00003	+560	000	0	00007	0560000000007	7777777777777	00
E	I	00003	+560	000	0	00003	7777777777777	7777777777777	00
I	I	00004	+020	000	0	00000	0020000000000	7777777777777	00
I	E	00001	+500	000	0	00006	0500000000006	7777777777777	00
E	I	00001	+500	000	0	00001	7777777777777	7777777777777	00
I	E	00002	+601	000	0	00007	0601000000007	7777777777777	00
E	I	00002	+601	000	0	00002	7777777777777	7777777777777	00
I	E	00003	+560	000	0	00007	0560000000007	7777777777777	00

Store Logical Word (SLW)									
CONSOLE INDICATORS									
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	Address	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	MQ REGISTER (M, 1-35)	TALLY COUNTER
I	E	00001	-500	000	0	00006	4500000000006	0000000000000	00
E	I	00001	-500	000	0	00001	631463146314	231463146314	01
I	E	00002	+602	000	0	00007	0602000000007	231463146314	01
E	I	00002	+602	000	0	00002	231463146314	231463146314	01
I	E	00003	+560	000	0	00007	0560000000007	231463146314	01
E	I	00003	+560	000	0	00003	631463146314	231463146314	01
I	I	00004	+020	000	0	00000	0020000000000	231463146314	01
I	E	00001	-500	000	0	00006	4500000000006	231463146314	01
E	I	00001	-500	000	0	00001	631463146314	231463146314	01
I	E	00002	+602	000	0	00007	0602000000007	231463146314	01
E	I	00002	+602	000	0	00002	231463146314	231463146314	01
I	E	00003	+560	000	0	00007	0560000000007	231463146314	01

FIGURE 15. STZ, STQ, STO, SLW (CONTINUED)

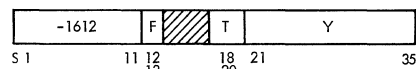
Store Logical Word with Parity (SLP -1612)
Stores the 36-bit logical word of the accumulator (P, 1-35) into the specified memory location (S, 1-35). In addition, the sign bit of the accumulator is stored into the C bit position of the memory location. Unlike other store operations, parity is not generated on SLP.



XFRS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST STORE LOGICAL WORD WITH PARITY

ALPHA CODE: SLP CYCLES: I, E



SEQUENCE NOTES:

THE C(AC), S, P, 1-35 ARE STORED INTO THE C(Y)C, S, 1-35.

AC(P) → Y(S).

AC IS UNCHANGED AND PARITY IS NOT CHECKED.

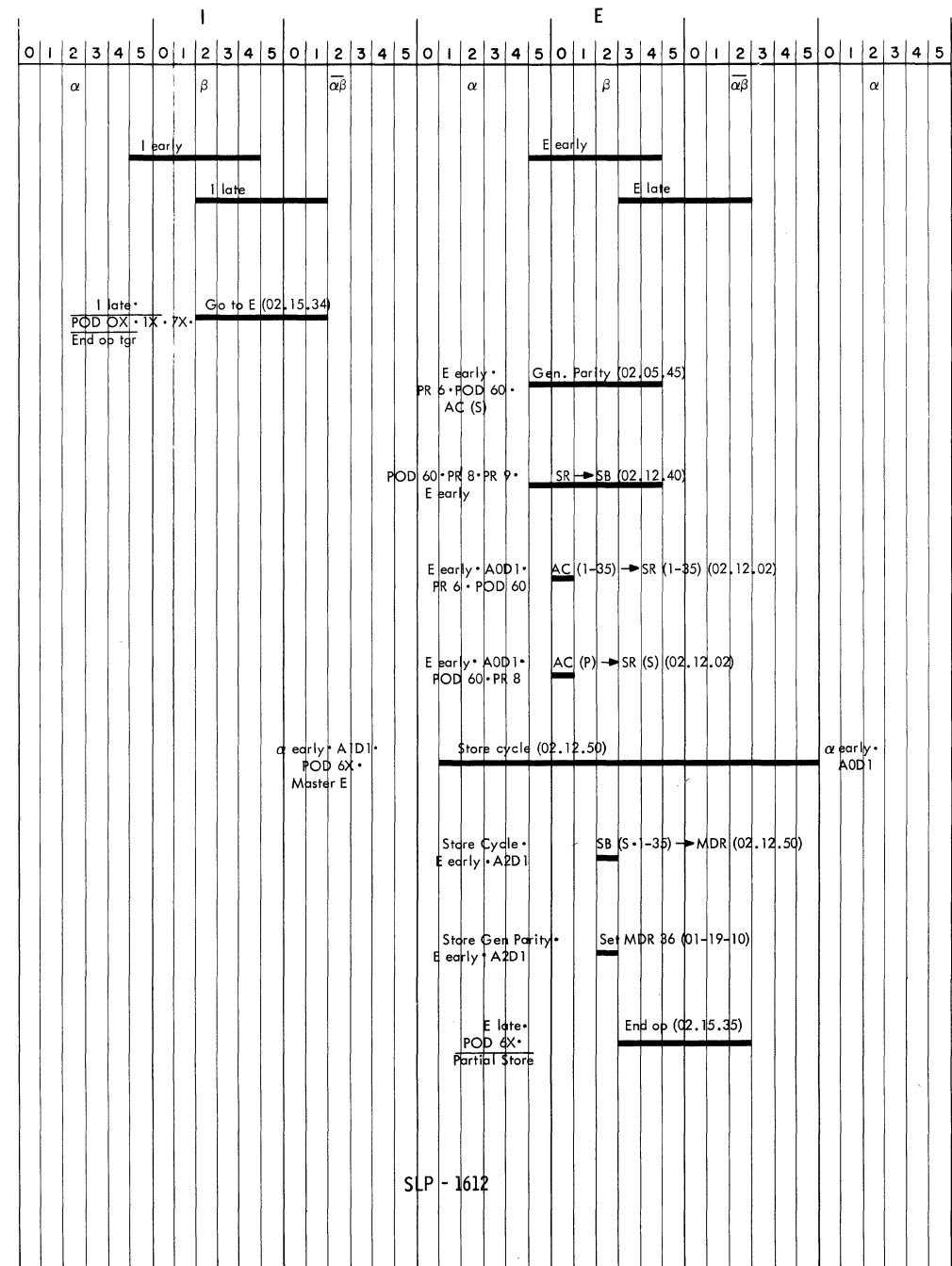


FIGURE 16. SLP

Store Address (STA+0621)
Stores the address portion of the accumulator (21-35) into positions 21-35 of the specified memory location. The rest of the memory word and the accumulator are unchanged.

Store Decrement (STD+0622)
Stores the decrement portion of the accumulator (3-17) into positions 3-17 of the specified memory location. The rest of the memory word and the accumulator are unchanged.

Store Instruction Location Counter (STL+0625)
Stores the contents of the instruction counter (the location of the STL instruction plus 1) into positions 21-35 of the specified memory location. The rest of the memory word is unchanged.

Transfer and Store Instruction Counter (TSL+0627)
Stores the contents of the instruction counter (the location of the TSL instruction plus 1) into positions 21-35 of the specified memory location. The rest of the memory word is unchanged. The computer takes its next instruction from the specified memory location plus 1.

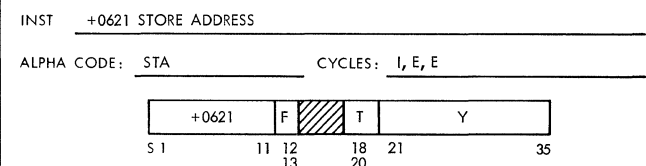
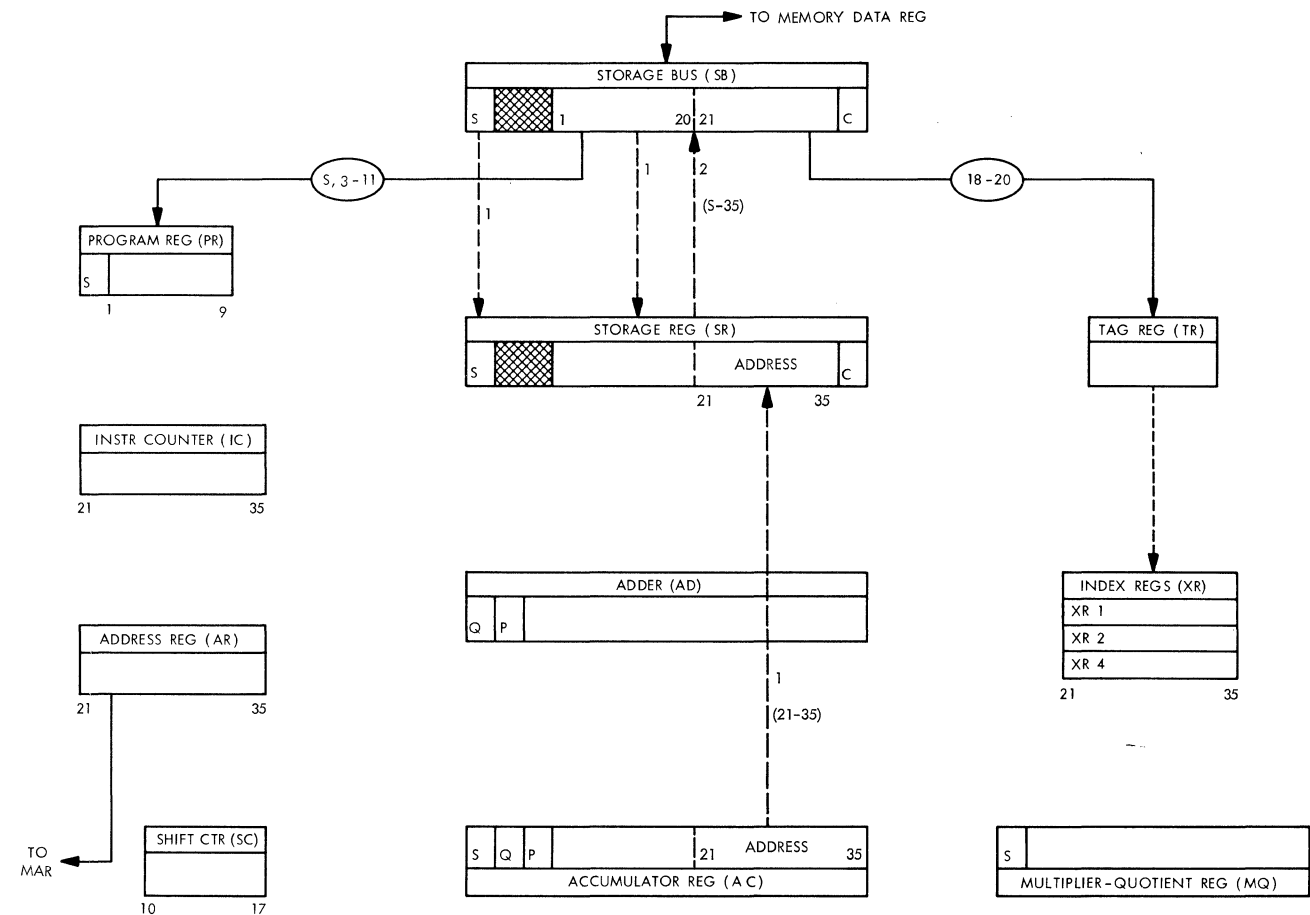
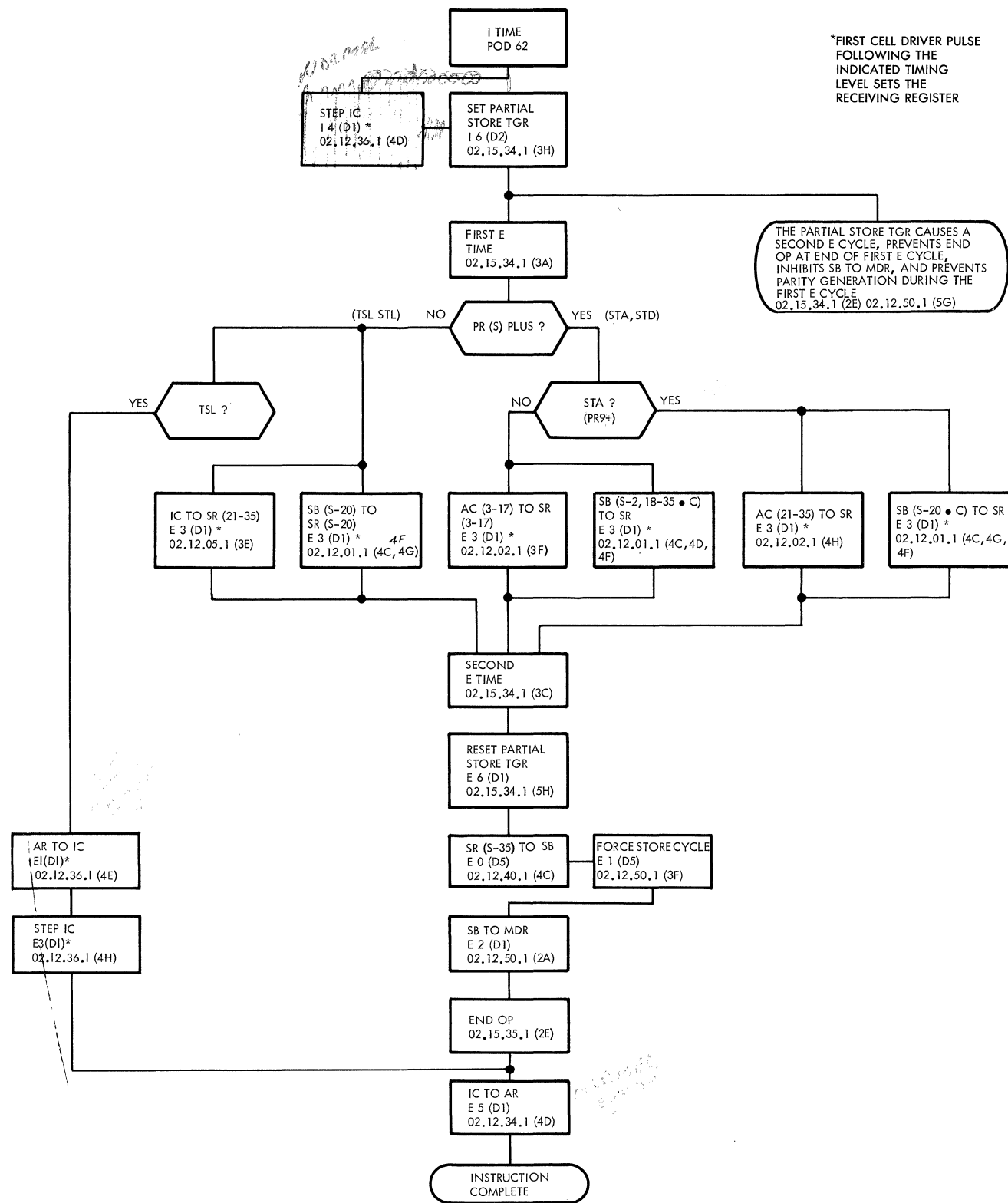
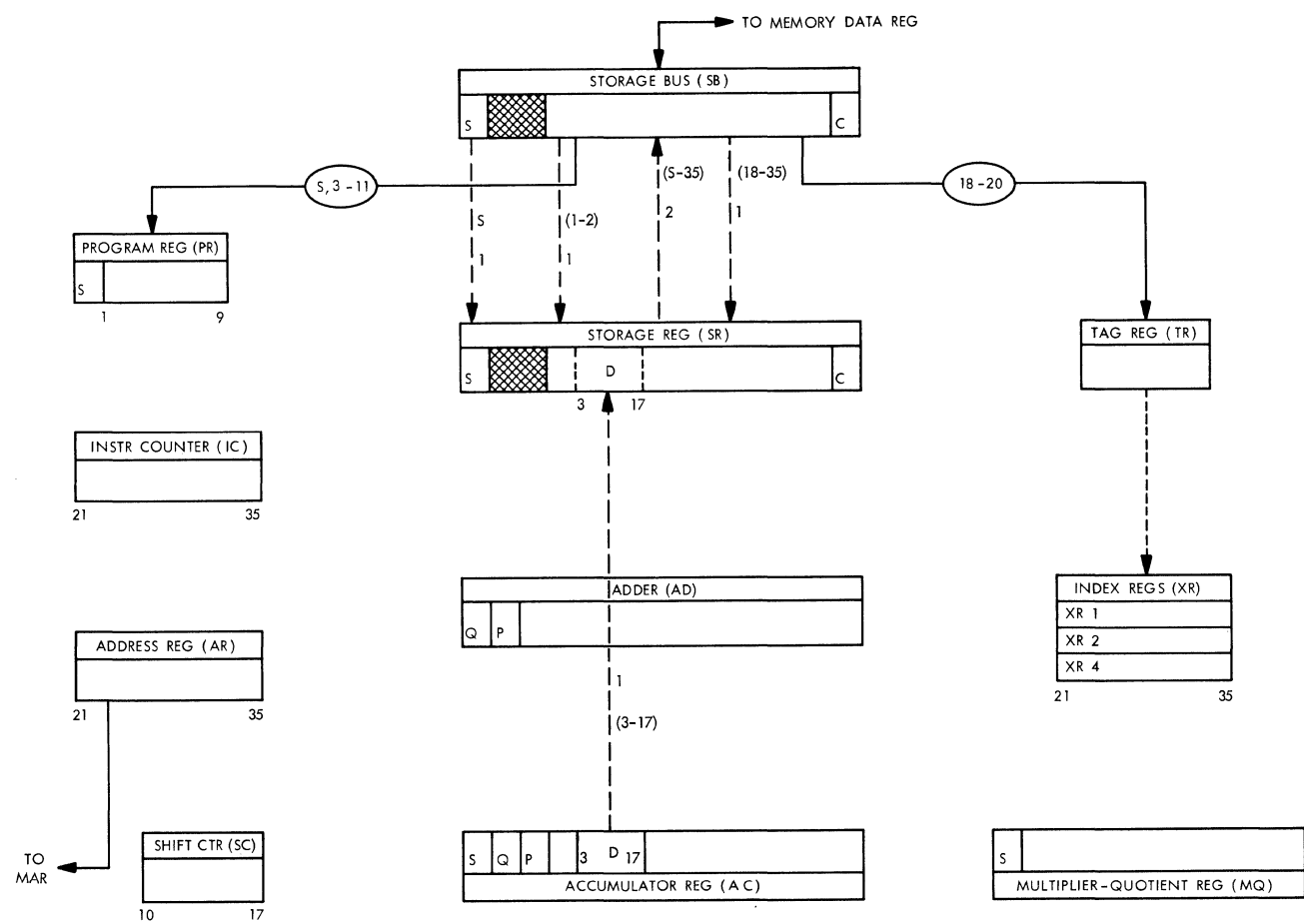


FIGURE 17. STA, STD, STL, TSL



LEGEND

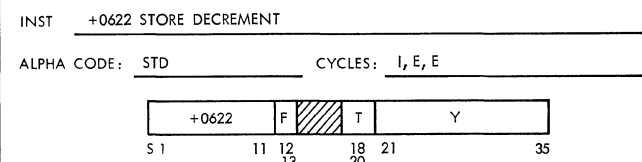
1 CYCLE

E CYCLE

L CYCLE

CONTROL

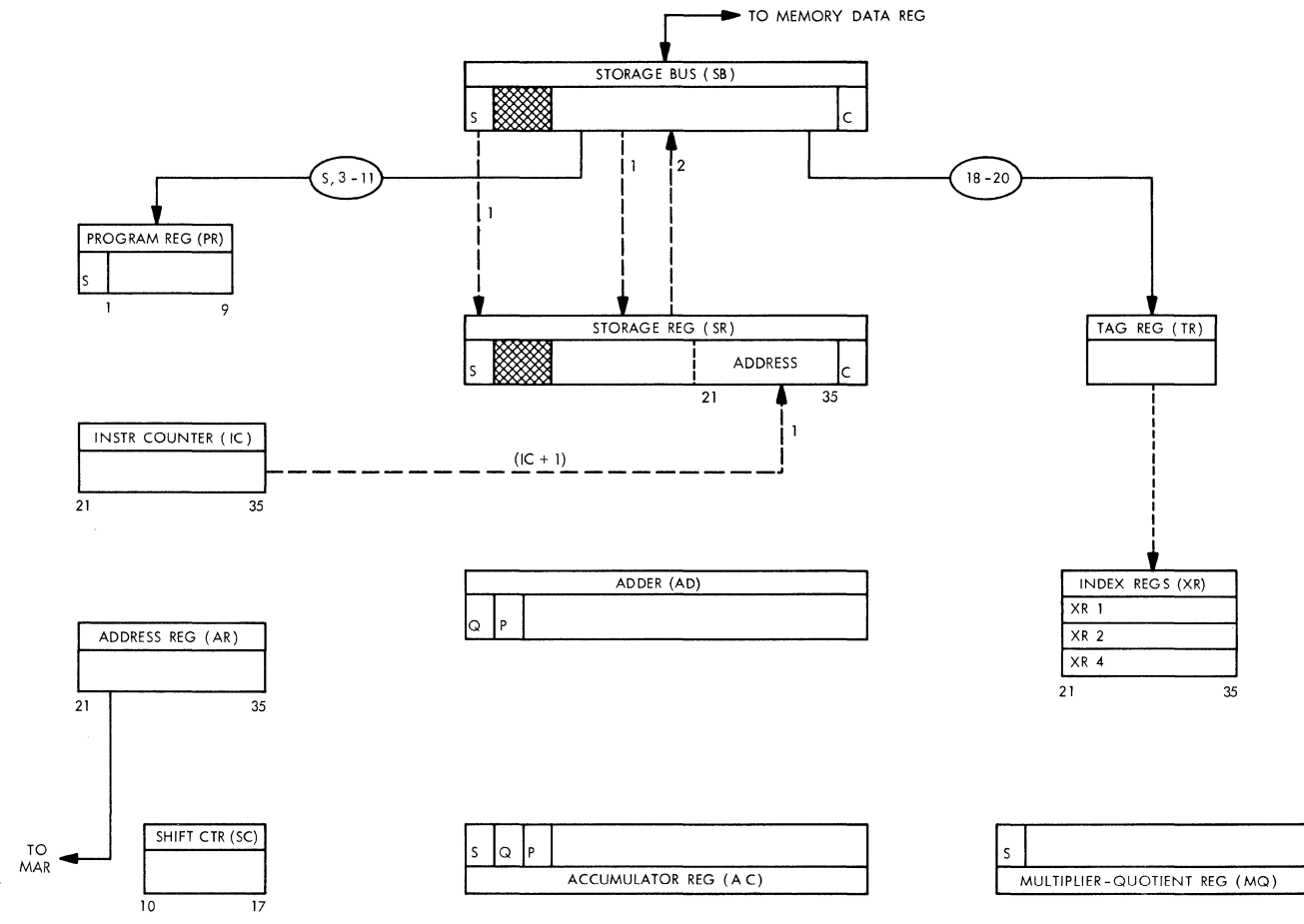
XFRS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.



SEQUENCE NOTES:

THE C(AC)₃₋₁₇ ARE PLACED INTO C(Y)₃₋₁₇.

THE C(Y)_{5-2, 18-35} AND THE C(AC) ARE UNCHANGED.



LEGEND

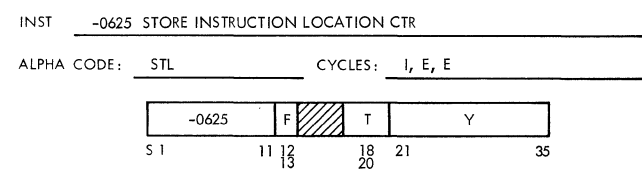
1 CYCLE

E CYCLE

L CYCLE

CONTROL

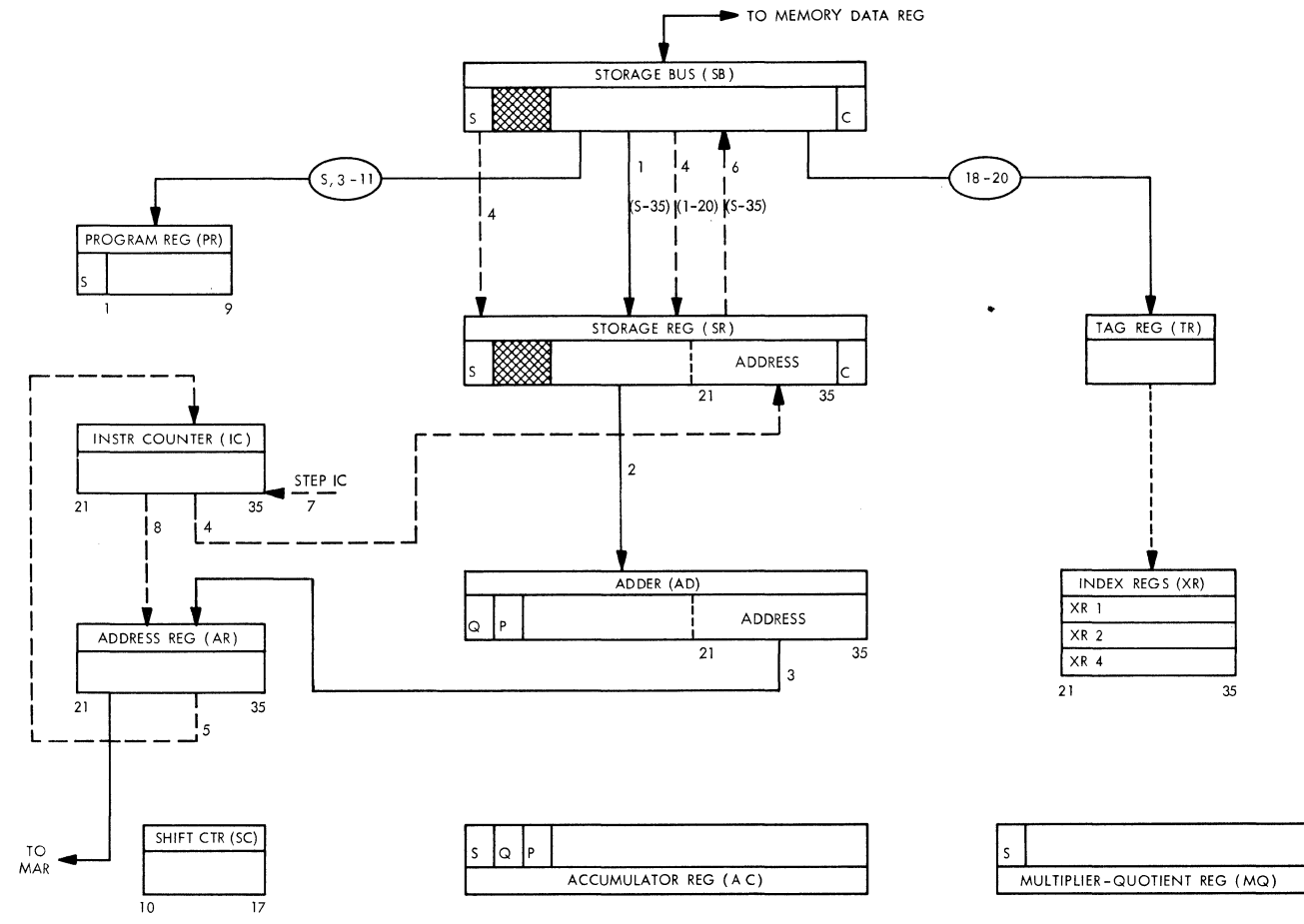
XFRS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.



SEQUENCE NOTES:

THE LOCATION OF THE STL INSTRUCTION +1 IS PLACED IN C(Y)₂₁₋₃₅.

THE C(Y)_{5, 1-20} ARE UNCHANGED.



LEGEND

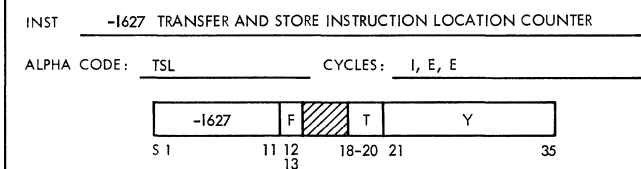
1 CYCLE

E CYCLE

L CYCLE

CONTROL

XFRS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.



SEQUENCE NOTES:

THE LOCATION OF THE TSL +1 IS STORED IN C(Y)₂₁₋₃₅.

POSITIONS 5, 1-20 OF Y ARE UNCHANGED.

THE COMPUTER TAKES ITS NEXT INSTRUCTION FROM Y+1.

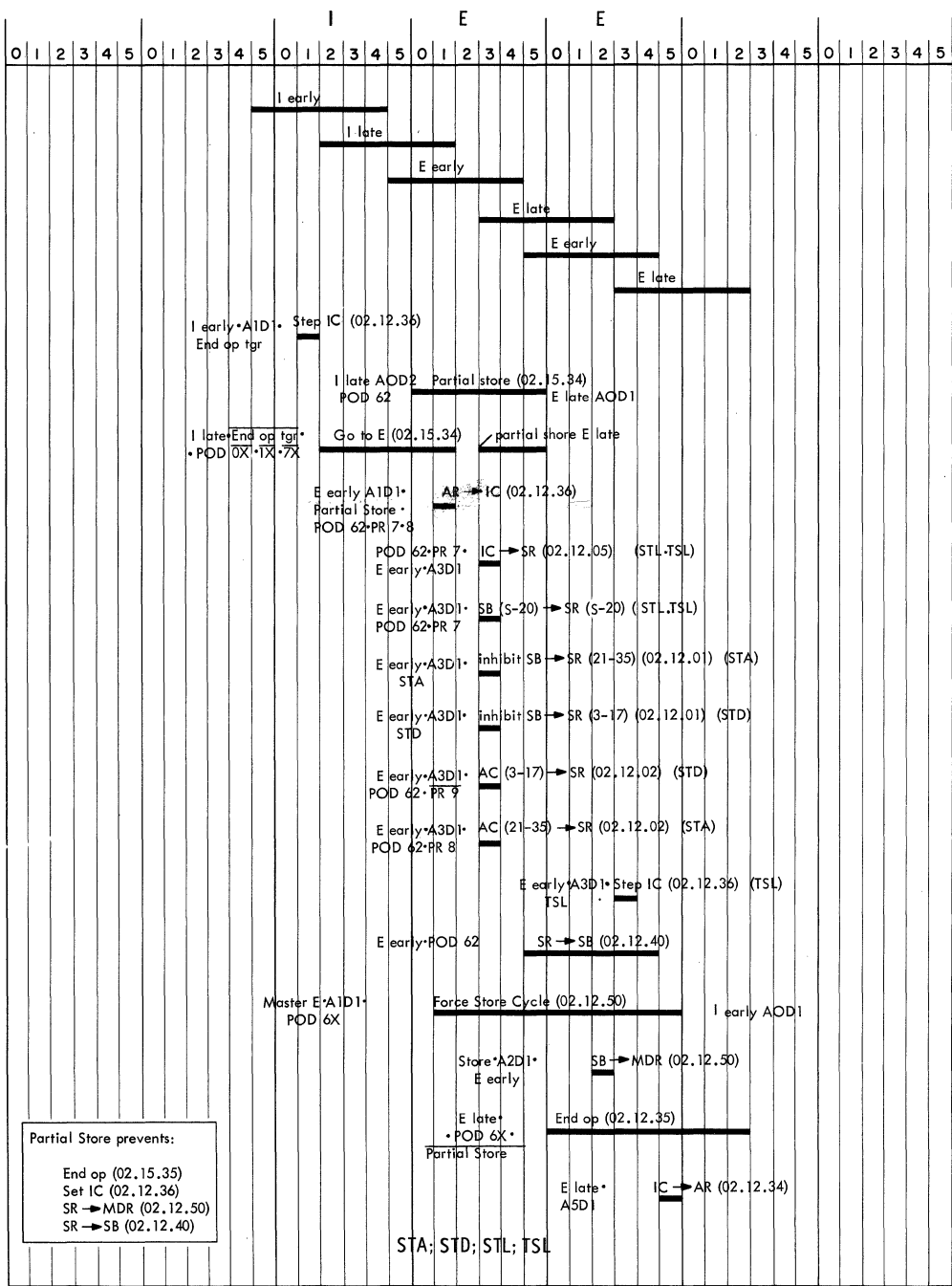


FIGURE 17. STA, STD, STL, TSL
(CONTINUED)

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STA		00007	062100 000007
00002	LDQ		00007	056000 000007
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern Live Reg			377777 777777
00007				

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STD		00007	062200 000007
00002	LDQ		00007	056000 000007
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern Live Reg			377777 777777
00007				

Store Address (STA)										CONSOLE INDICATORS		
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORE REGISTER (S 1-35)	ACCUMULATOR (S 1-35)	ACCUMULATOR (Q P)	MQ REGISTER (S 1-35)	TALLY COUNTER	
I	E	00001	+500	000	0	00006	0500000000006	0000000000000	00	0000000000000		
E	I	00001	+500	000	0	00001	3777777777777	3777777777777	00	0000000000000		
I	E(1)	00002	+621	000	0	00007	0621000000007	3777777777777	00	0000000000000		
E(1)	E(2)	00002	+621	000	0	00007	0000000777777	3777777777777	00	0000000000000		
E(2)	I	00002	+621	000	0	00002	0000000777777	3777777777777	00	0000000000000		
I	E	00003	+560	000	0	00007	0560000000007	3777777777777	00	0000000000000		
E	I	00003	+560	000	0	00003	0000000777777	3777777777777	00	0000000777777		
I	I	00004	+020	000	0	00000	0020000000000	3777777777777	00	0000000777777		
I	E	00001	+500	000	0	00006	0500000000006	3777777777777	00	0000000777777		
E	I	00001	+500	000	0	00001	3777777777777	3777777777777	00	0000000777777		
I	E(1)	00002	+621	000	0	00007	0621000000007	3777777777777	00	0000000777777		
E(1)	E(2)	00002	+621	000	0	00007	0000000777777	3777777777777	00	0000000777777		
E(2)	I	00002	+621	000	0	00002	0000000777777	3777777777777	00	0000000777777		
I	E	00003	+560	000	0	00007	0560000000007	3777777777777	00	0000000777777		

Store Decrement (STD)										CONSOLE INDICATORS		
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORE REGISTER (S 1-35)	ACCUMULATOR (S 1-35)	ACCUMULATOR (Q P)	MQ REGISTER (S 1-35)	TALLY COUNTER	
I	E	00001	+500	000	0	00006	0500000000006	0000000000000	00	0000000000000		
E	I	00001	+500	000	0	00001	3777777777777	3777777777777	00	0000000000000		
I	E(1)	00002	+622	000	0	00007	0622000000007	3777777777777	00	0000000000000		
E(1)	E(2)	00002	+622	000	0	00007	0777770000000	3777777777777	00	0000000000000		
E(2)	I	00002	+622	000	0	00002	0777770000000	3777777777777	00	0000000000000		
I	E	00003	+560	000	0	00007	0560000000007	3777777777777	00	0000000000000		
E	I	00003	+560	000	0	00003	0777770000000	3777777777777	00	0777770000000		
I	I	00004	+020	000	0	00000	0020000000000	3777777777777	00	0777770000000		
I	E	00001	+500	000	0	00006	0500000000006	3777777777777	00	0777770000000		
E	I	00001	+500	000	0	00001	3777777777777	3777777777777	00	0777770000000		
I	E(1)	00002	+622	000	0	00007	0622000000007	3777777777777	00	0777770000000		
E(1)	E(2)	00002	+622	000	0	00007	0777770000000	3777777777777	00	0777770000000		
E(2)	I	00002	+622	000	0	00002	0777770000000	3777777777777	00	0777770000000		
I	E	00003	+560	000	0	00007	0560000000007	3777777777777	00	0777770000000		

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CL A		00006	050000 000006
00001	STL		00007	462500 000007
00002	CL A		00007	050000 000007
00003	TRA		00000	002000 000000
00004				
00005	Pattern			377777 777777
00006	Live Reg			
00007				

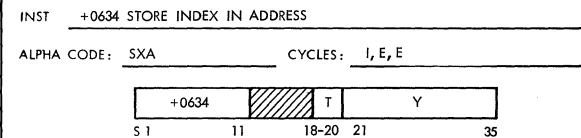
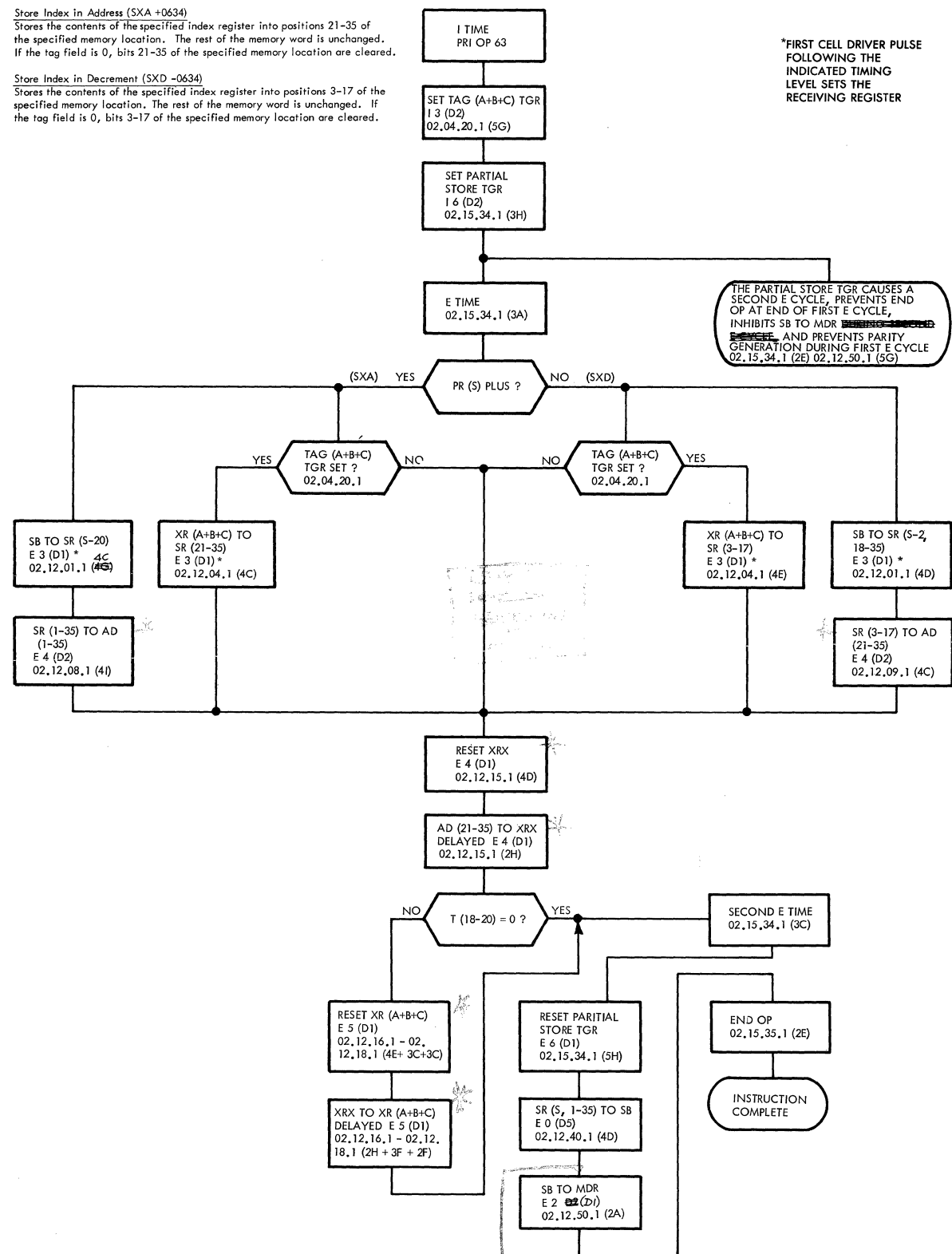
Location Switches	Inst	Tag	Address	Octal Equiv
00000	CL A		00006	050000 000006
00001	TSL		00003	562700 000003
00002	TRA		00001	002000 000001
00003	TRA		00000	002000 000000
00004	ADD		00006	040000 000006
00005	TRA		00003	002000 000003
00006	Pattern			000000 000001

Store Instruction Location Counter (STL)											
CONSOLE INDICATORS											
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	
I	E	00001	+500	000	0	00006	050000000006	000000000000	00		
E	I	00001	+500	000	0	00001	377777777777	377777777777	00		
I	E(1)	00002	-625	000	0	00007	462500000007	377777777777	00		
E(1)	E(2)	00002	-625	000	0	00007	000000000002	377777777777	00		
E(2)	I	00002	-625	000	0	00002	000000000002	377777777777	00		
I	E	00003	+500	000	0	00007	050000000007	377777777777	00		
E	I	00003	+500	000	0	00003	000000000002	000000000002	00		
I	I	00004	+020	000	0	00000	002000000000	000000000002	00		
I	E	00001	+500	000	0	00006	050000000006	000000000002	00		

TRANSFER AND STORE INSTRUCTION COUNTER (TSL)											
CONSOLE INDICATORS											
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER
I	E	00001	+500	000	0	00006	050000000006	000000000000	00		
E	I	00001	+500	000	0	00001	000000000001	000000000001	00		
I	E(1)	00002	-627	000	0	00003	562700000003	000000000001	00		
E(1)	E(2)	00002	-627	000	0	00003	002000000002	000000000001	00		
E(2)	I	00004	-627	000	0	00004	002000000002	000000000001	00		
I	E	00005	+400	000	0	00006	040000000006	000000000001	00		
E	I	00005	+400	000	0	00005	000000000001	000000000002	00	*	
I	I	00006	+020	000	0	00003	002000000003	000000000002	00		
I	I	00004	+020	000	0	00002	002000000002	000000000002	00		
I	I	00003	+020	000	0	00001	002000000001	000000000002	00		
I	E(1)	00002	-627	000	0	00003	562700000003	000000000002	00		
E(1)	E(2)	00003	-627	000	0	00003	002000000002	000000000002	00		
E(2)	I	00004	-627	000	0	00004	002000000003	000000000002	00		
I	E	00005	+400	000	0	00006	050000000006	000000000002	00		
E	I	00005	+400	000	0	00005	000000000001	000000000003	00	*	
Note	*Increase accumulator by one for each program pass.										

Store Index in Address (SXA +0634)
Stores the contents of the specified index register into positions 21-35 of the specified memory location. The rest of the memory word is unchanged. If the tag field is 0, bits 21-35 of the specified memory location are cleared.

Store Index in Decrement (SXD -0634)
Stores the contents of the specified index register into positions 3-17 of the specified memory location. The rest of the memory word is unchanged. If the tag field is 0, bits 3-17 of the specified memory location are cleared.

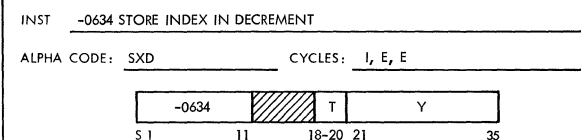
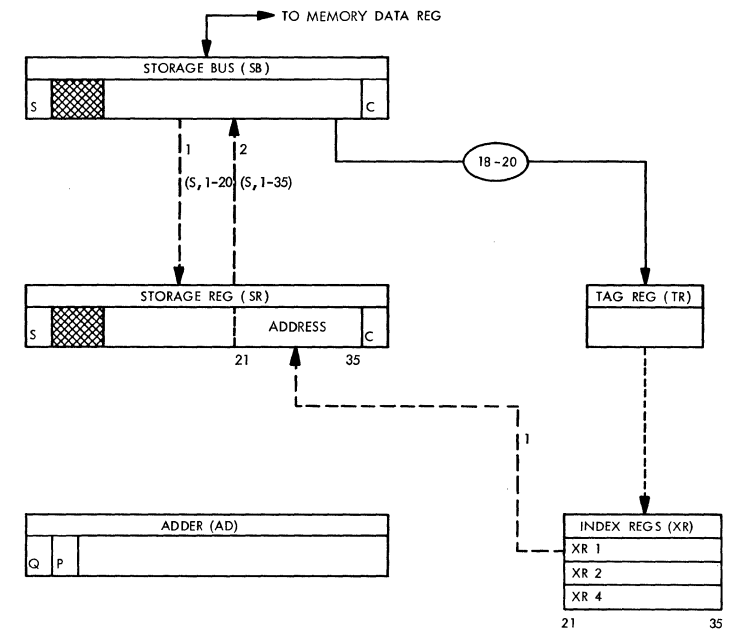


SEQUENCE NOTES:

THE CONTENTS OF THE SPECIFIED INDEX REGISTER(S) ARE STORED IN C(Y)₂₁₋₃₅.

THE C(Y)_{S, 1-20} ARE UNCHANGED.

WITH A TAG OF ZERO, THE C(Y)₂₁₋₃₅ ARE CLEARED TO ZEROS.



SEQUENCE NOTES:

THE CONTENTS OF THE SPECIFIED INDEX REGISTER(S) ARE STORED IN C(Y)₃₋₁₇.

THE C(Y)_{S-2, 18-35} ARE UNCHANGED.

WITH A TAG OF ZERO, THE C(Y)₃₋₁₇ ARE CLEARED TO ZEROS.

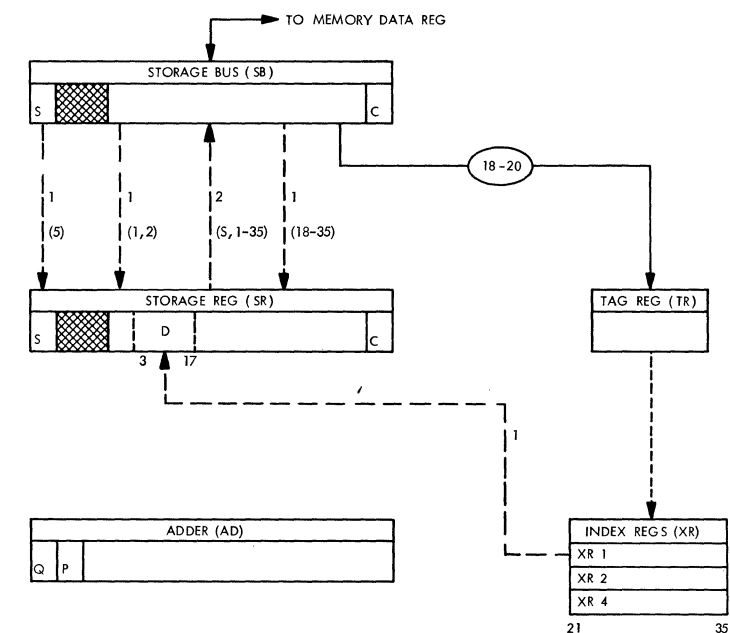
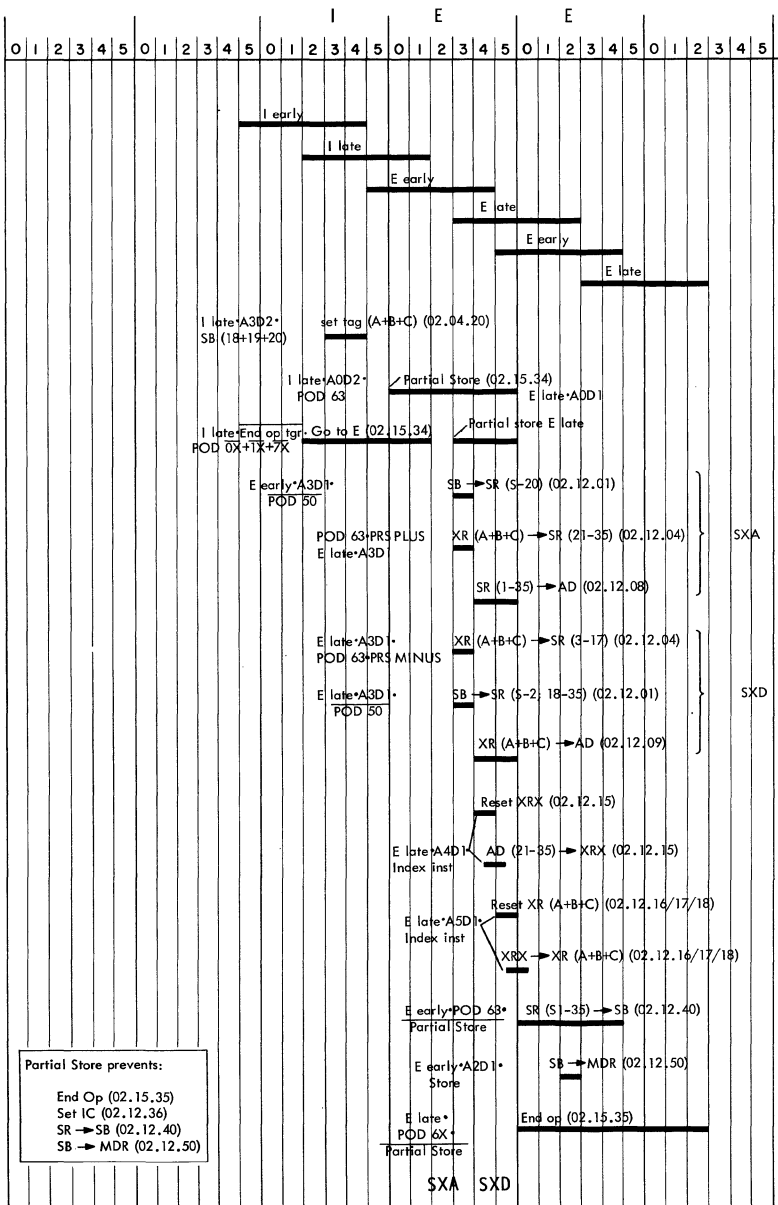


FIGURE 18. SXA, SXD

**Compatibility*

FORCE STORE CYCLE



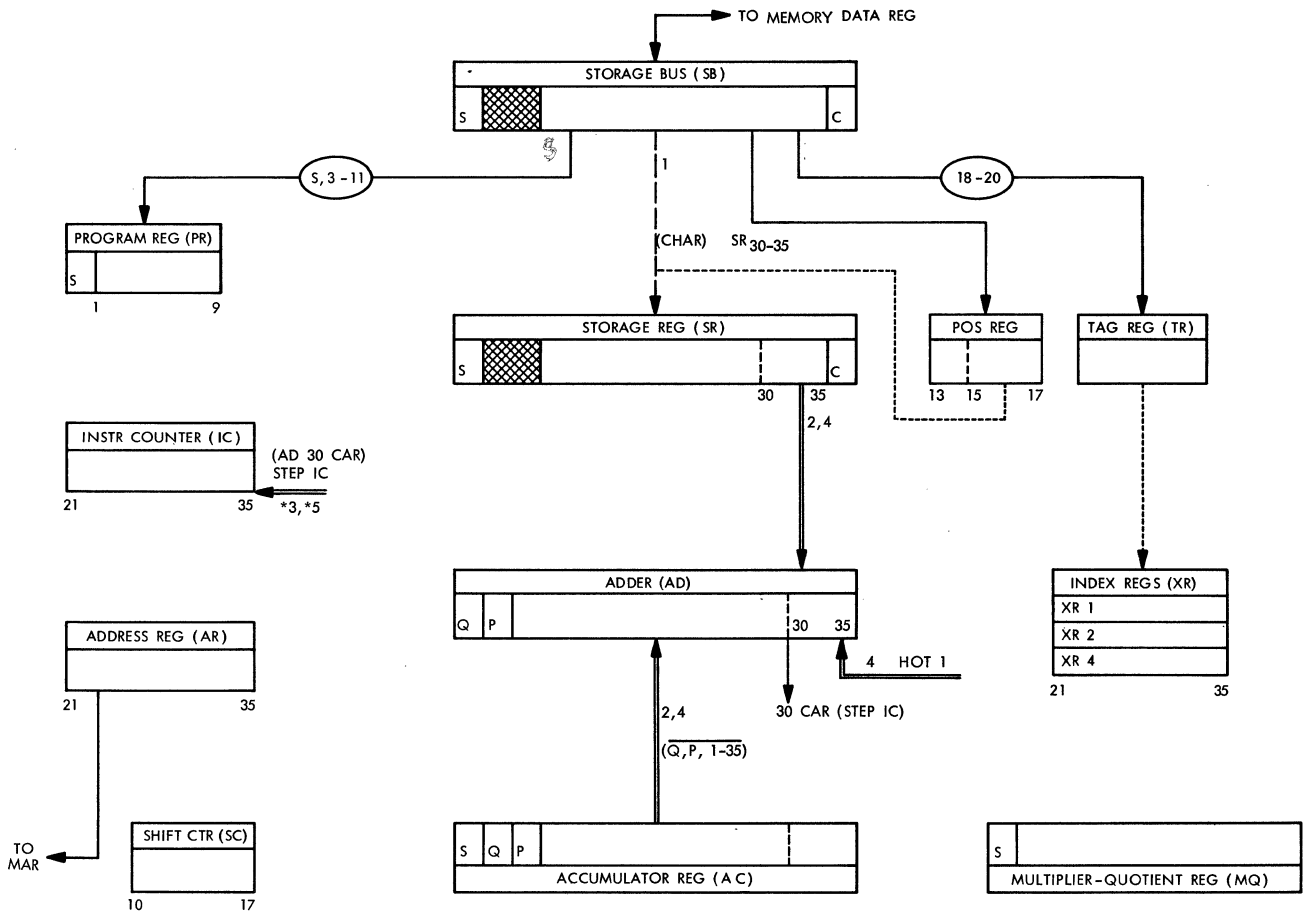
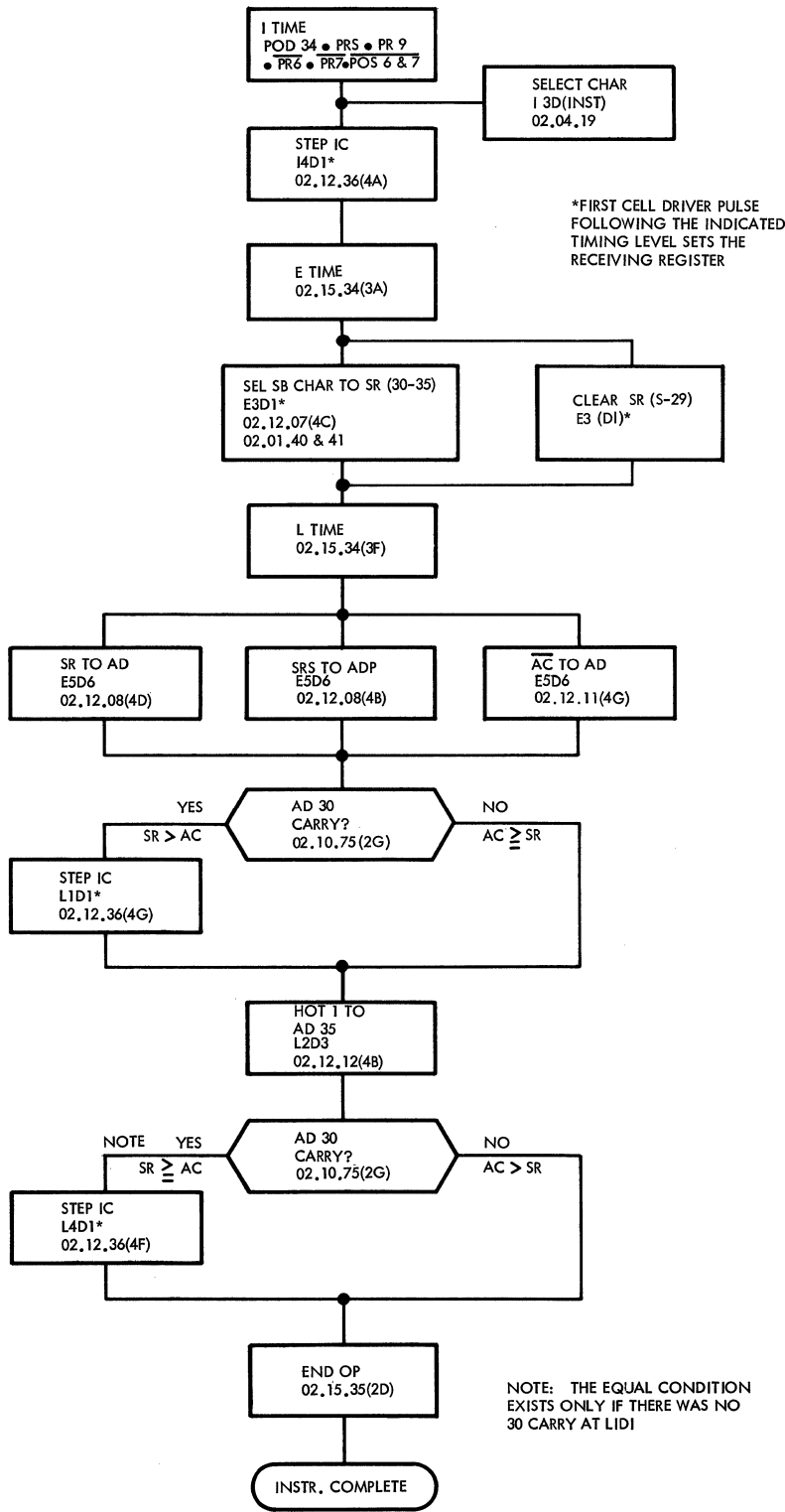
Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STO		00007	060100 000007
00002	AXT	7	77777	077400 777777
00003	SKA	7	00007	063400 700007
00004	LDQ		00007	056000 000007
00005	TRA		00000	002000 000000
00006	Pattern Live Reg			042077 700000
00007				

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STO		00007	060100 000007
00002	AXT	7	77777	077400 777777
00003	SKD	7	00007	463400 700007
00004	LDQ		00007	056000 000007
00005	TRA		00000	002000 000000
00006	Pattern Live Reg			042000 777777
00007				

Store Index in Address (SXA)										CONSOLE INDICATORS											
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (A 1-35)	ACCUMULATOR (Q, P)	MIO REGISTER (M 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	P CARRY	P OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00006	0500000000006	0000000000000	00	0000000000000		00000									
E	I	00001	+500	000	0	00001	0420777000000	0420777000000	00	0000000000000		00000									
I	E	00002	+601	000	0	00007	0601000000007	0420777000000	00	0000000000000		00000									
E	I	00002	+601	000	0	00002	0420777000000	0420777000000	00	0000000000000		00000									
I	I	00003	+774	377	7	00003	0774007777777	0420777000000	00	0000000000000		77777									
I	E(1)	00004	+634	000	7	00007	0634007000007	0420777000000	00	0000000000000		77777									
E(1)	E(2)	00004	+634	000	7	00007	0420777777777	0420777000000	00	0000000000000		77777									
E(2)	I	00004	+634	000	7	00004	0420777777777	0420777000000	00	0000000000000		77777									
I	E	00005	+560	000	0	00007	0560000000007	0420777000000	00	0000000000000		77777									
E	I	00005	+560	000	0	00005	0420777777777	0420777000000	00	0420777777777		77777									
I	I	00006	+020	000	0	00000	0020000000000	0420777000000	00	0420777777777		77777									
I	E	00001	+500	000	0	00006	0500000000006	0420777000000	00	0420777777777		77777									
E	I	00001	+500	000	0	00001	0420777000000	0420777000000	00	0420777777777		77777									
I	E	00002	+601	000	0	00007	0601000000007	0420777000000	00	0420777777777		77777									
E	I	00002	+601	000	0	00002	0420777000000	0420777000000	00	0420777777777		77777									
I	I	00003	+774	377	7	00003	0774007777777	0420777000000	00	0420777777777		77777									
I	E(1)	00004	+634	000	7	00007	0634007000007	0420777000000	00	0420777777777		77777									
E(1)	E(2)	00004	+634	000	7	00007	0420777777777	0420777000000	00	0420777777777		77777									
E(2)	I	00004	+634	000	7	00004	0420777777777	0420777000000	00	0420777777777		77777									
I	E	00005	+560	000	0	00007	0560000000007	0420777000000	00	0420777777777		77777									

Store Index in Decrement (SKD)										CONSOLE INDICATORS										
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (A 1-35)	ACCUMULATOR (Q, P)	MIO REGISTER (M 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	P CARRY	P OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00006	0500000000006	0000000000000	00	0000000000000	00000									
E	I	00001	+500	000	0	00001	0420007777777	0420007777777	00	0000000000000	00000									
I	E	00002	+601	000	0	00007	0601000000007	0420007777777	00	0000000000000	00000									
E	I	00002	+601	000	0	00002	0420007777777	0420007777777	00	0000000000000	00000									
I	I	00003	+774	377	7	00003	0774007777777	0420007777777	00	0000000000000	77777									
I	E(1)	00004	-634	000	7	00007	4634007000007	0420007777777	00	0000000000000	77777									
E(1)	E(2)	00004	-634	000	7	00007	0777777777777	0420007777777	00	0000000000000	77777									
E(2)	I	00004	-634	000	7	00004	0777777777777	0420007777777	00	0000000000000	77777									
I	E	00005	+560	000	0	00007	0560000000007	0420007777777	00	0000000000000	77777									
E	I	00005	+560	000	0	00005	0777777777777	0420007777777	00	0777777777777	77777									
I	I	00006	+020	000	0	00000	0020000000000	0420007777777	00	0777777777777	77777									
I	E	00001	+500	000	0	00006	0500000000006	0420007777777	00	0777777777777	77777									
E	I	00001	+500	000	0	00001	0420007777777	0420007777777	00	0777777777777	77777									
I	E	00002	+601	000	0	00007	0601000000007	0420007777777	00	0777777777777	77777									
E	I	00002	+601	000	0	00002	0420007777777	0420007777777	00	0777777777777	77777									
I	I	00003	+774	377	7	00003	0774007777777	0420007777777	00	0777777777777	77777									
I	E(1)	00004	-634	000	7	00007	4634007000007	0420007777777	00	0777777777777	77777									
E(1)	E(2)	00004	-634	000	7	00007	0777777777777	0420007777777	00	0777777777777	77777									
E(2)	I	00004	-634	000	7	00004	0777777777777	0420007777777	00	0777777777777	77777									
I	E	00005	+560	000	0	00007	0560000000007	0420007777777	00	0777777777777	77777									

Compare Character with Storage (CCS -1341)
Compares the character in positions 30-35 of the accumulator with the character (specified by bits 15-17 of the instruction word) in the specified memory location. If the accumulator character bits are greater than the character in memory, the computer takes the next sequential instruction; if these bits are equal to the specified character, the computer skips the next instruction and proceeds from there; if they are less than the specified character, the computer skips the next two instructions. The contents of the accumulator and memory are unchanged.



LEGEND

- 1 CYCLE
- - - - -→ E CYCLE
- =====→ L CYCLE
- - - - -→ CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -1341 -- C COMPARE CHARACTER WITH STORAGE

ALPHA CODE: CCS CYCLES: I, E, (L)

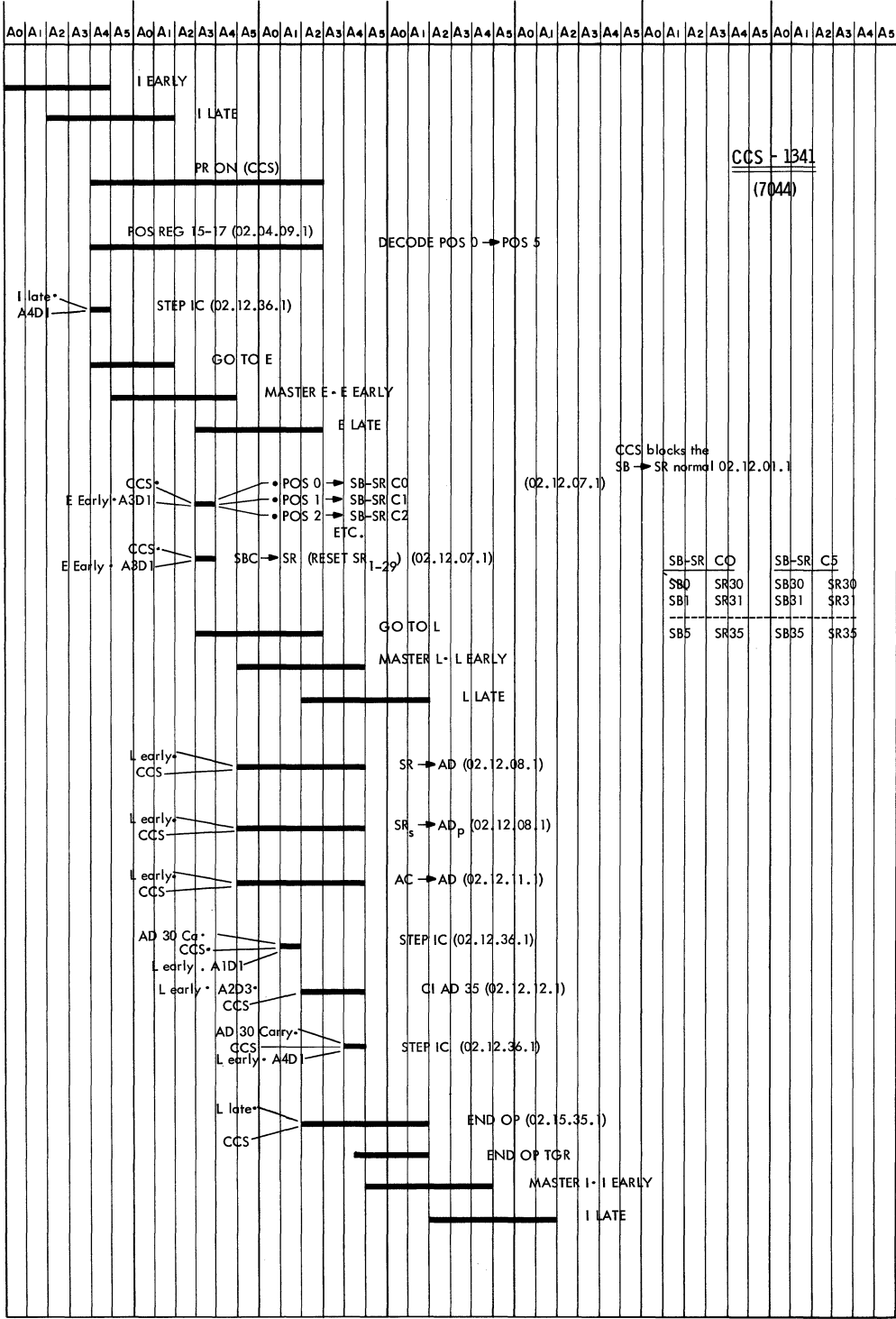
-1341	F	C	T	Y
S 1	11 12 13	15 17	18 20	21 35

SEQUENCE NOTES:

THE CHARACTER IN LOCATION Y SPECIFIED BY THE "C" FIELD IS COMPARED WITH THE C(AC)₃₀₋₃₅. IF C(AC)₃₀₋₃₅ > CHARACTER IN Y, TAKE THE NEXT INSTRUCTION. IF C(AC)₃₀₋₃₅ = TO THE SPECIFIED CHAR, SKIP 1 INSTRUCTION. IF THE C(AC)₃₀₋₃₅ < CHAR, SKIP 2 INSTRUCTIONS.

CYCLES REQUIRED 7040: I, E
7044: I, E, L

FIGURE 19. CCS



CCS - 1341
(7044)

CCS blocks the
SB → SR normal D2.D2.01.1

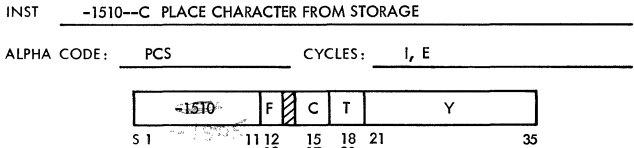
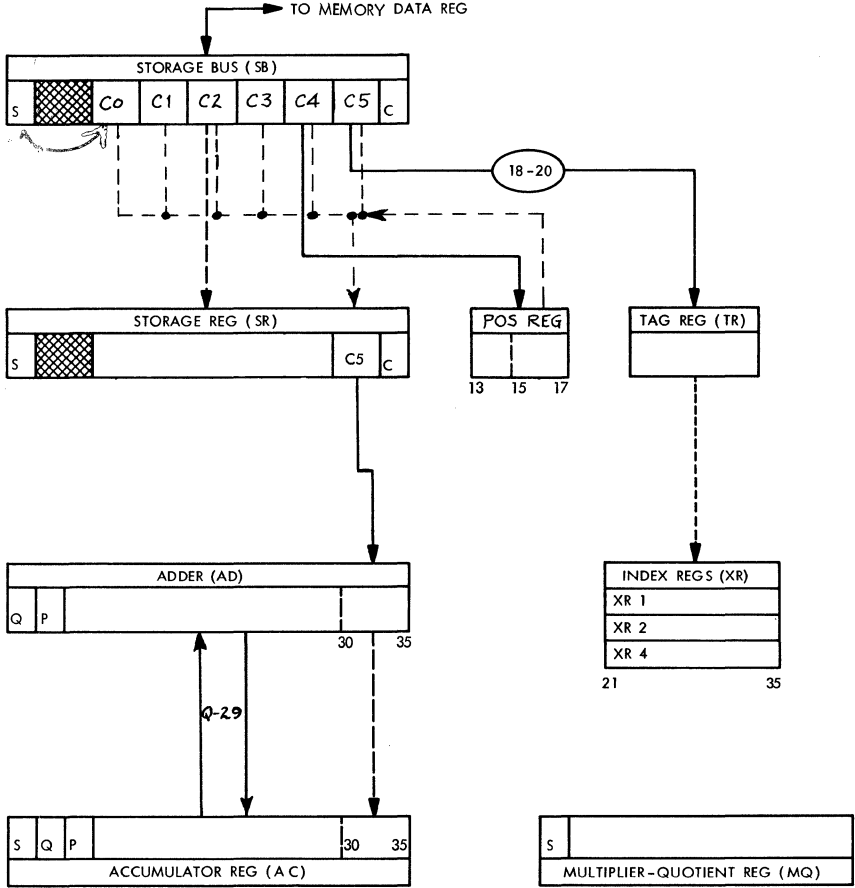
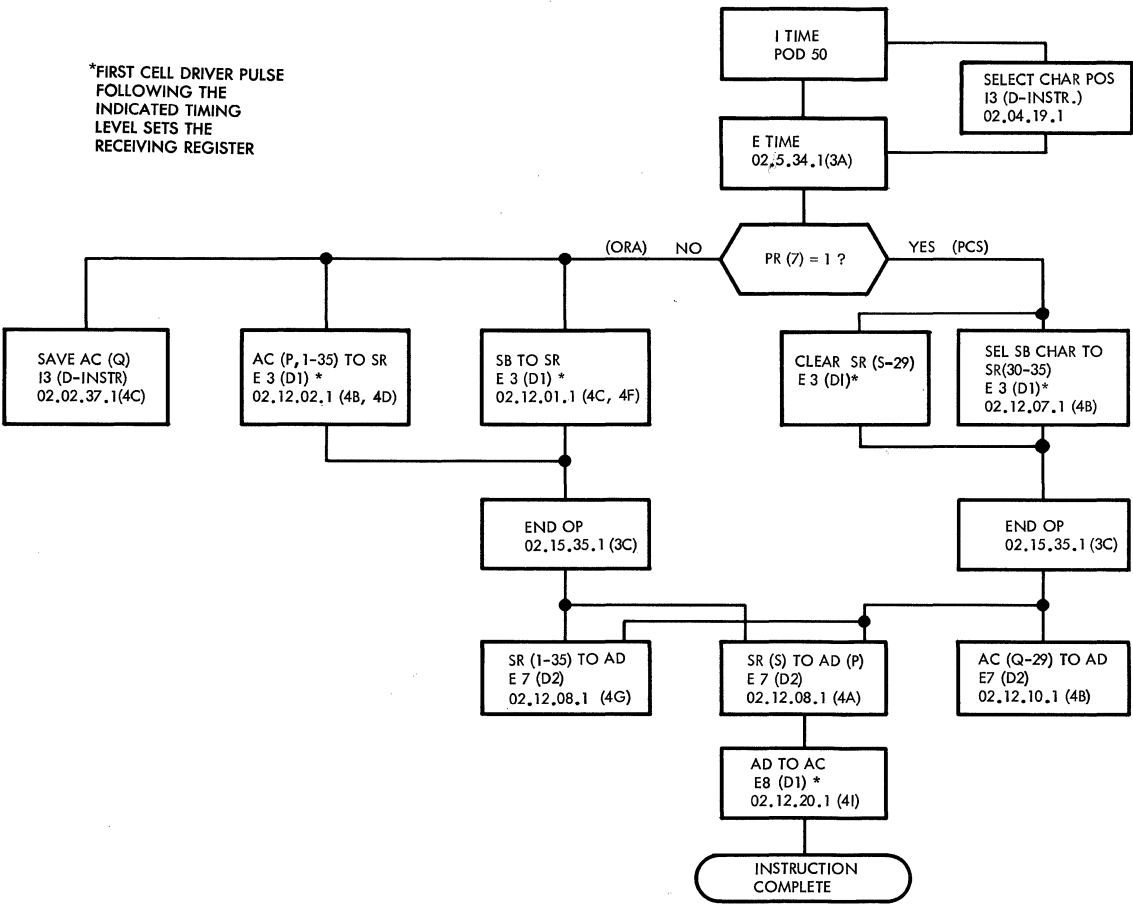
SB-SR	CO	SB-SR	C5
SB0	SR30	SB30	SR30
SB1	SR31	SB31	SR31
SB5	SR35	SB35	SR35

Compare Character with Storage (CCS)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY
I	E	00001	+500	000	0	00006	050000000006	000000000000	00						
E	I	00001	+500	000	0	00001	042000000076	042000000076	00						
I	E	00002	-341	000	0	00003	534105000003	042000000076	00			17			
E	L	00002	-341	000	0	00003	000000000075	042000000076	00			15			
I	E	00002	-341	000	0	00002	000000000075	042000000076	00			17			
E	L	00002	-341	000	0	00002	000000000075	042000000076	00			15			
I	I	00003	+020	000	0	00000	002000000000	042000000076	00						
E	E	00001	+500	000	0	00006	050000000006	042000000076	00						

Place Character from Storage (PCS -1505)
Places the character (specified by bits 15-17 of the instruction word) of the specified memory location into positions 30-35 of the accumulator. The memory word and the rest of the accumulator are unchanged.

OR to Accumulator (ORA -0501)
Logically OR's each bit of the specified memory location with the corresponding bits of the accumulator. The result is placed in the accumulator. The sign bit of the memory word is OR'ed with the P bit of the accumulator. The contents of memory and bits S and Q of the accumulator are unchanged.

Logical OR'ing is as follows:
1,1 = 1
1,0 = 1
0,1 = 1
0,0 = 0

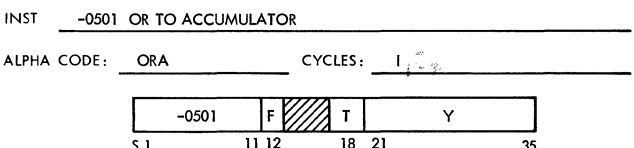
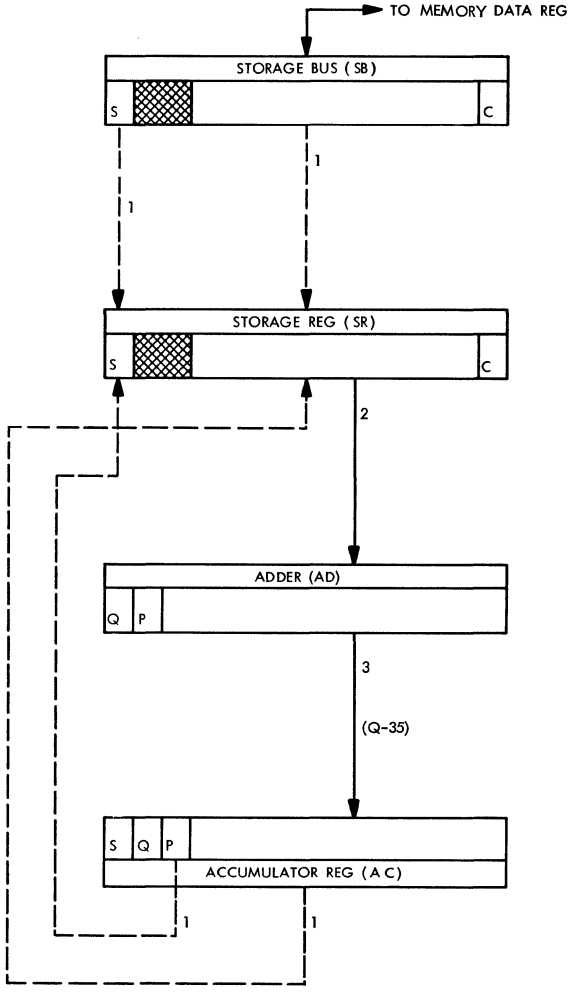


SEQUENCE NOTES:

THE CHARACTER IN LOCATION Y SPECIFIED BY THE "C" FIELD OF THE INSTRUCTION REPLACES THE C(AC)₃₀₋₃₅.

THE C(AC)_{S, Q, P, 1-29} ARE UNCHANGED.

THE C(Y) ARE UNCHANGED.

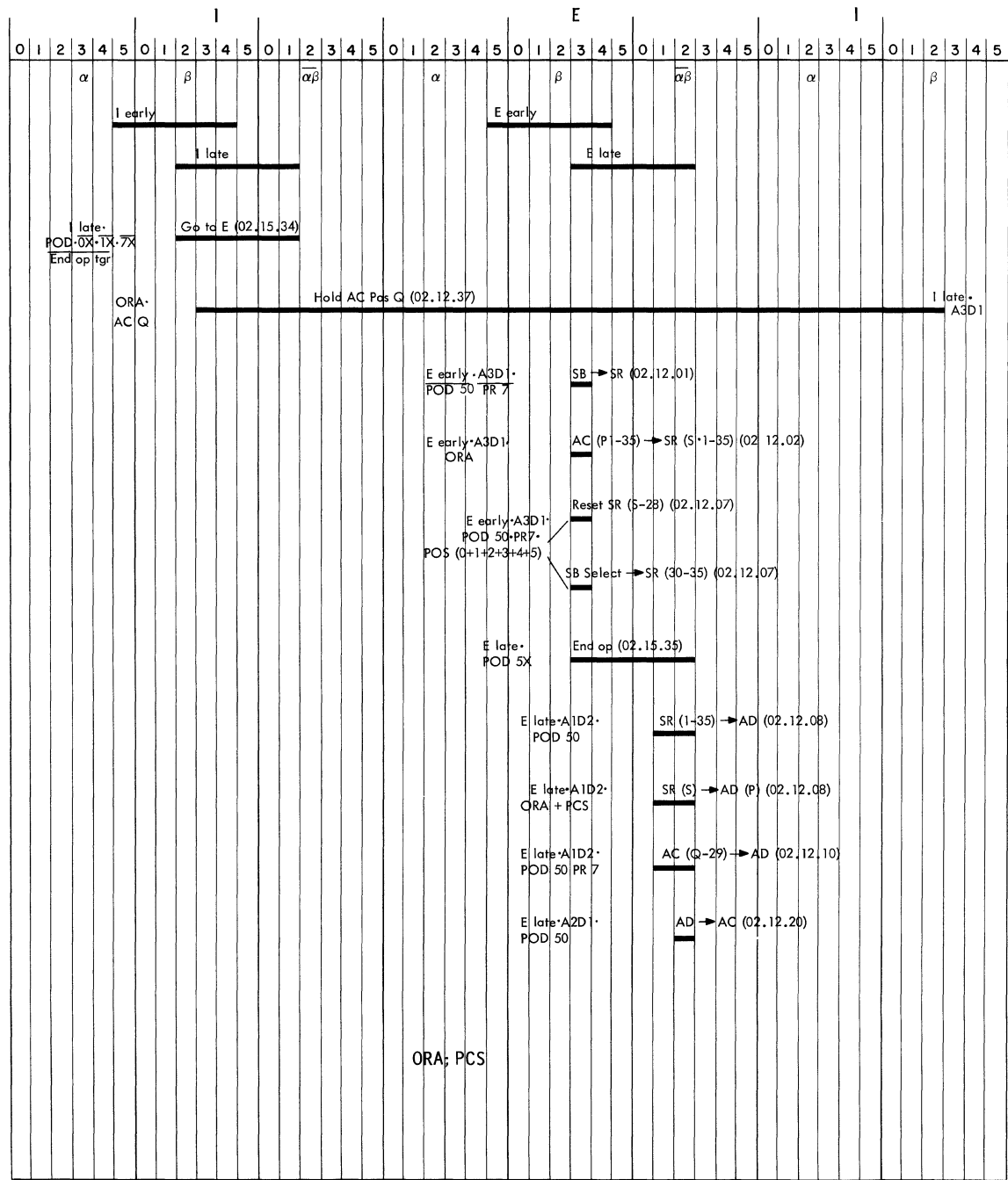


SEQUENCE NOTES:

LOGICAL ADDITION OF C(AC)_{P-35} AND C(Y)_{S-35}.

THE AC(Q) AND AC(S) ARE UNCHANGED.

FIGURE 20. PCS, ORA



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	STO		00007	060100 000007
00002	CAL		00006	450000 000006
00003	ORA		00007	450100 000007
00004	TRA		00000	002000 000000
00005	Pattern			252525 252525
00006	Pattern			252525 525252

OR to Accumulator (ORA)														
CONSOLE INDICATORS														
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (M, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW
I	E	00001	+500	000	0	00005	0500000000005	0000000000000	00					
E	I	00001	+500	000	0	00001	2525252525252	2525252525252	00					
I	E	00002	+601	000	0	00007	0601000000007	2525252525252	00					
E	I	00002	+601	000	0	00002	2525252525252	2525252525252	00					
I	E	00003	-500	000	0	00006	4500000000006	2525252525252	00					
E	I	00003	-500	000	0	00003	2525252525252	2525252525252	00					
I	E	00004	-501	000	0	00007	4501000000007	2525252525252	00					
E	I	00004	-501	000	0	00004	2525257777777	2525257777777	00					
I	I	00005	+020	000	0	00000	0020000000000	2525257777777	00					
I	E	00001	+500	000	0	00005	0500000000005	2525257777777	00					

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STO		00007	060100 000007
00002	PCS		00007	550500 000007
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			172737 475767
00007	Live Reg			

Place Character from Storage (PCS)														
CONSOLE INDICATORS														
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (M, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW
I	E	00001	+500	000	0	00006	0500000000006	0000000000000	00					
E	I	00001	+500	000	0	00001	172737475767	172737475767	00					
I	E	00002	+601	000	0	00007	0601000000007	172737475767	00					
E	I	00002	+601	000	0	00002	172737475767	172737475767	00					
I	E	00003	-505	000	0	00007	5505000000007	172737475767	00					
E	I	00003	-505	000	0	00003	0000000000017	172737475767	00					
I	I	00004	+020	000	0	00000	0020000000000	172737475767	00					
I	E	00001	+500	000	0	00006	0500000000006	172737475767	00					

Store Accumulator Character (SAC -1623)
Stores the character in accumulator positions 30-35 into the specified memory location character position (specified by bits 15-17 of the instruction word). The contents of the accumulator and the rest of the memory word are unchanged.

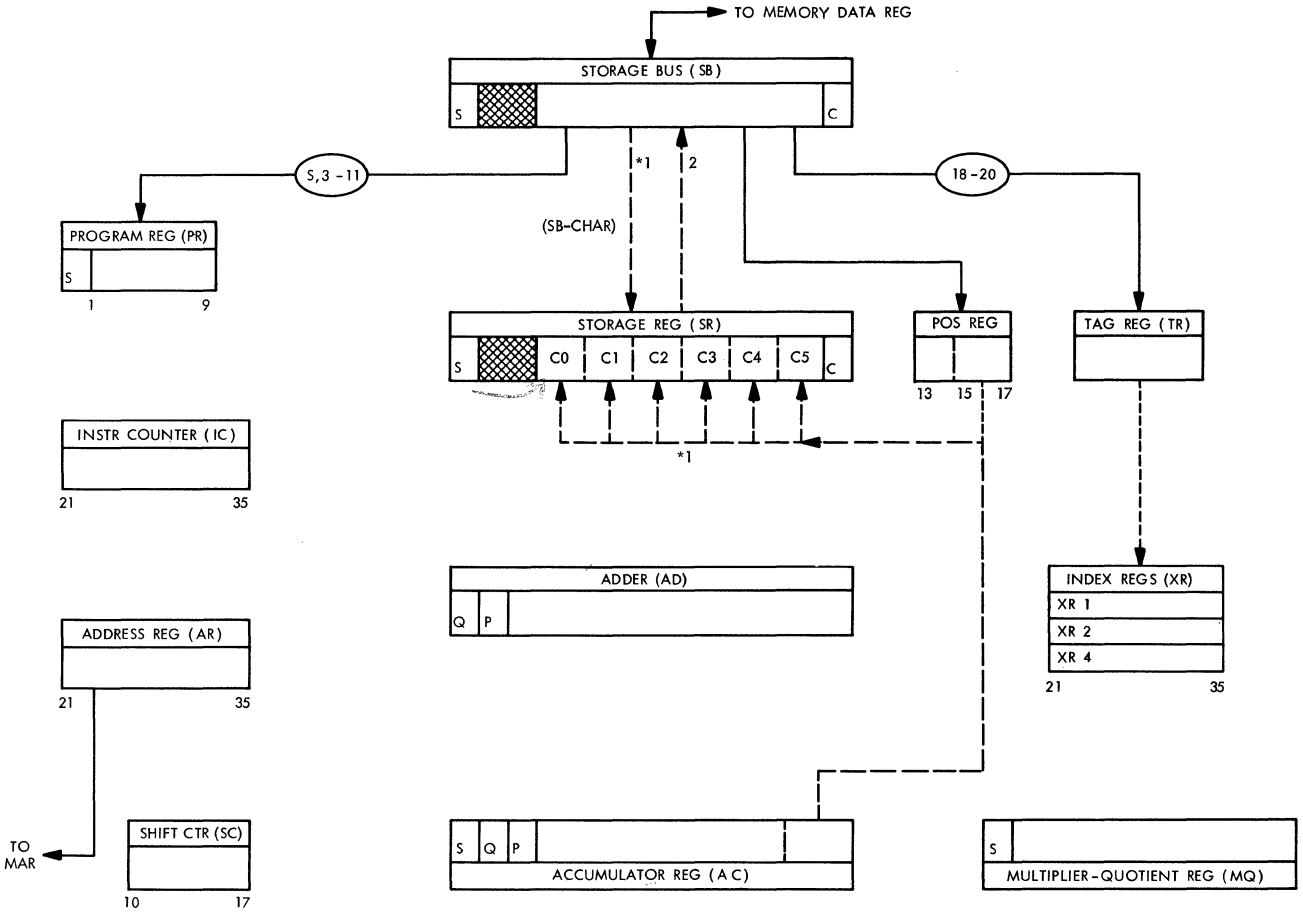
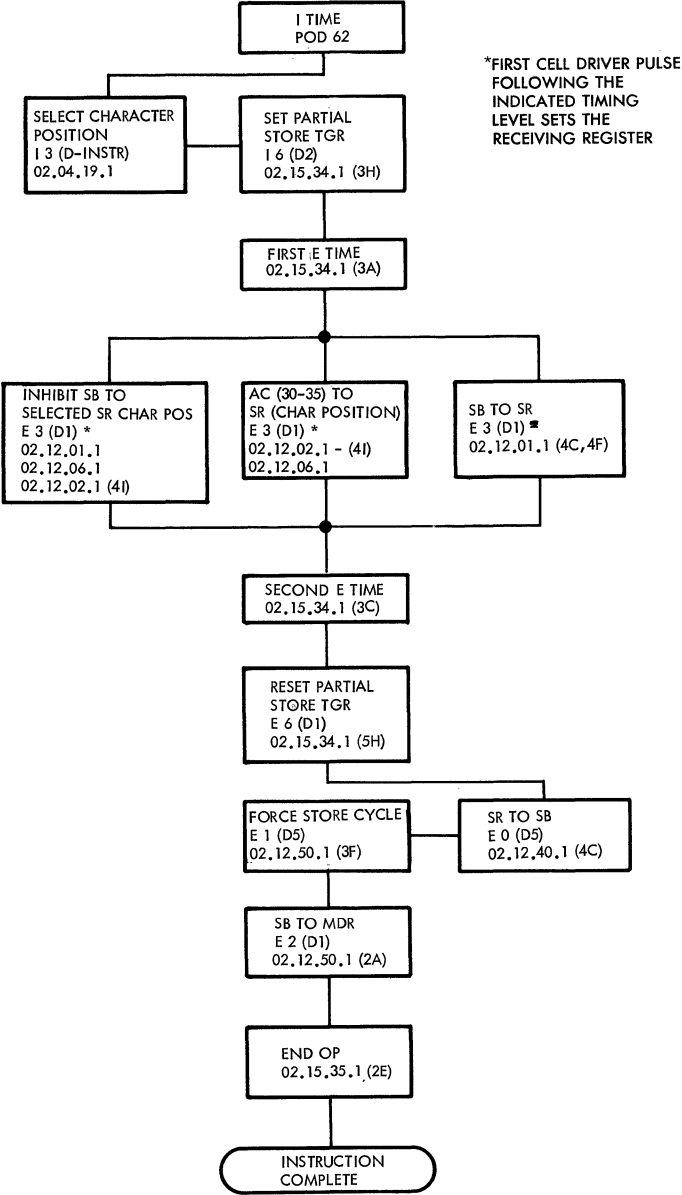


FIGURE 21. SAC

AND to Accumulator (ANA -0320)
Logically AND's each bit of the specified memory location with the corresponding bits of the accumulator. The memory word sign bit is AND'ed with the accumulator P bit. The AND'ed result of the two words appears in the accumulator. Bits S and Q of the accumulator are cleared, and the contents of the memory word are unchanged. Logical AND'ing is as follows:
1,1 = 1
1,0 = 0
0,1 = 0
0,0 = 0

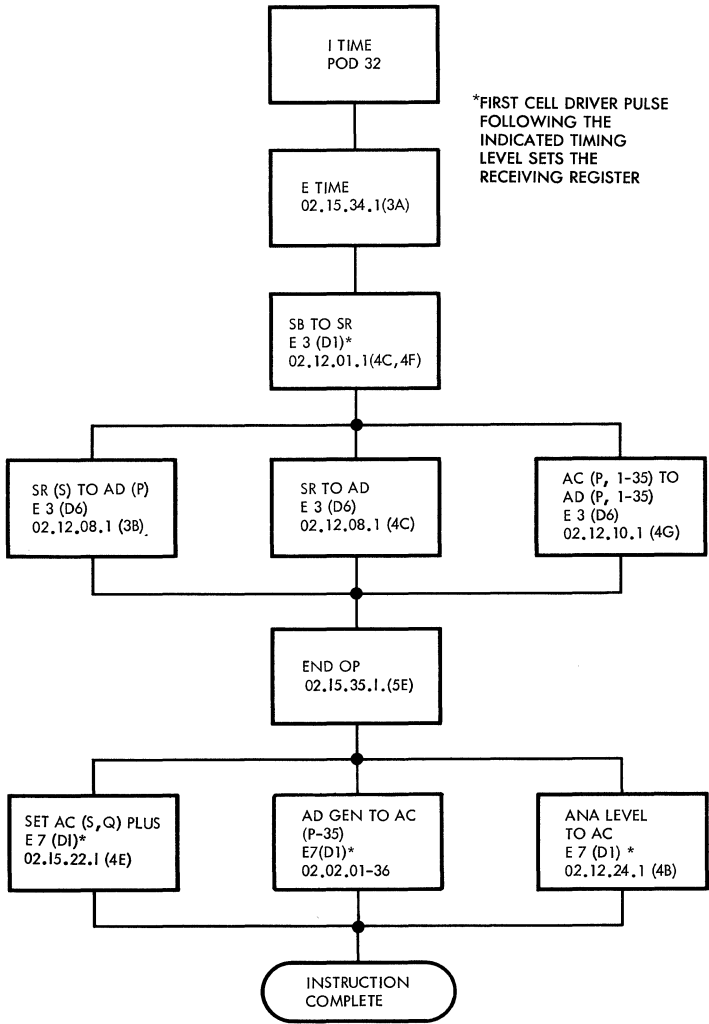
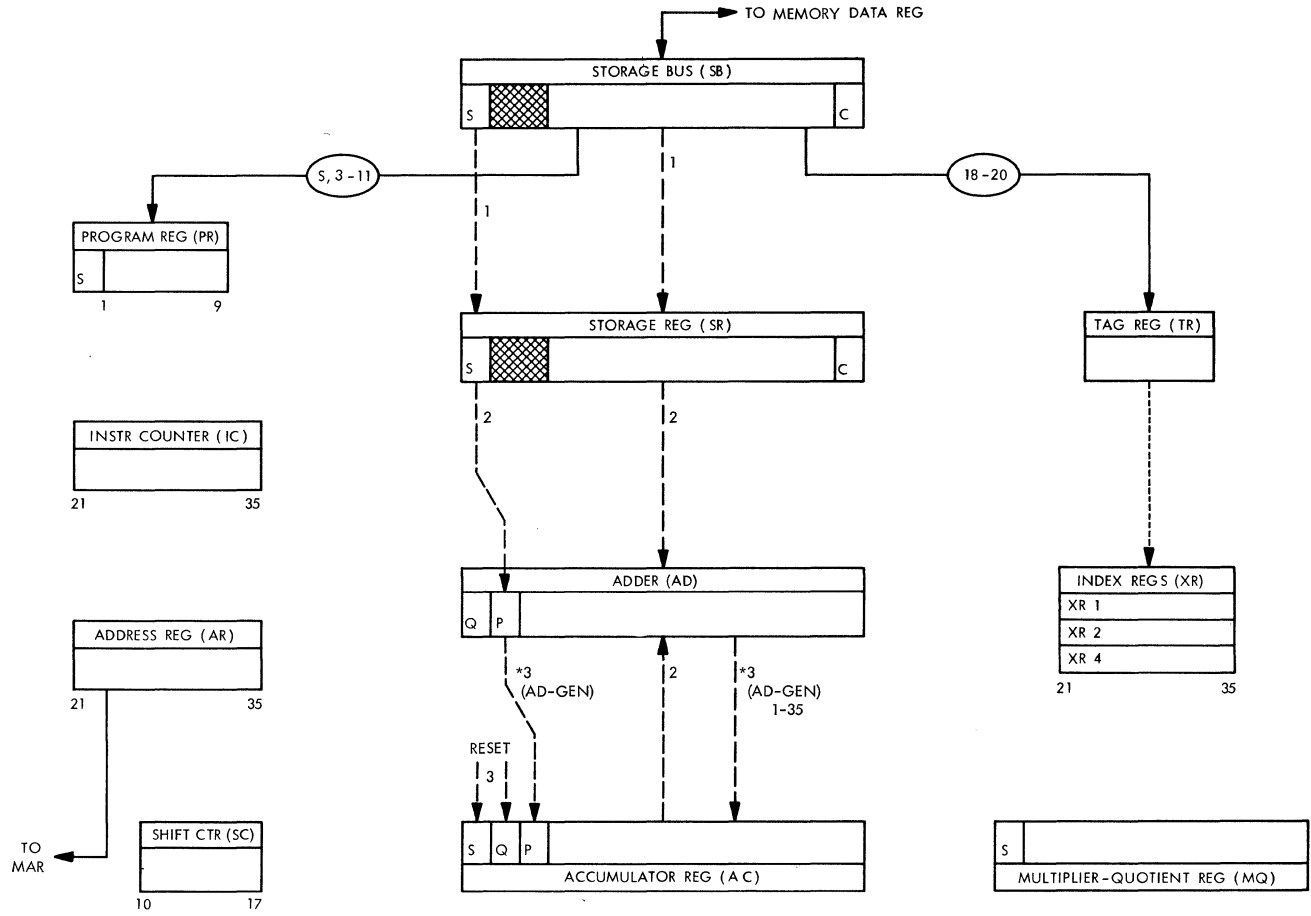
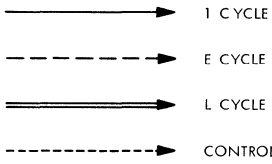


FIGURE 22. ANA



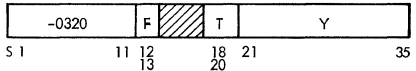
LEGEND



Xfers include all bits contained in the smaller of the two registers involved, unless otherwise specified.

INST -0320 AND TO ACCUMULATOR

ALPHA CODE: ANA CYCLES: I, E

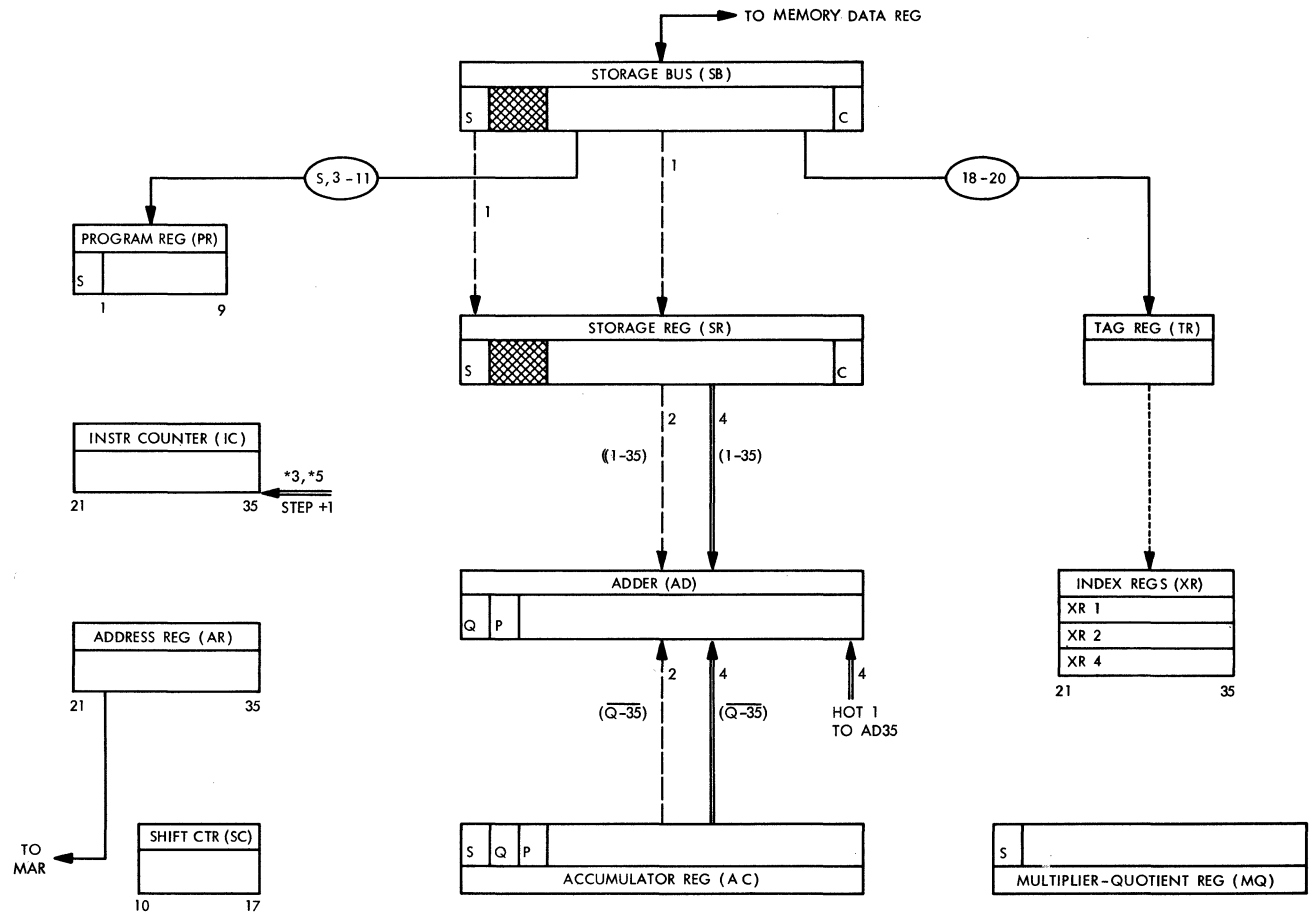
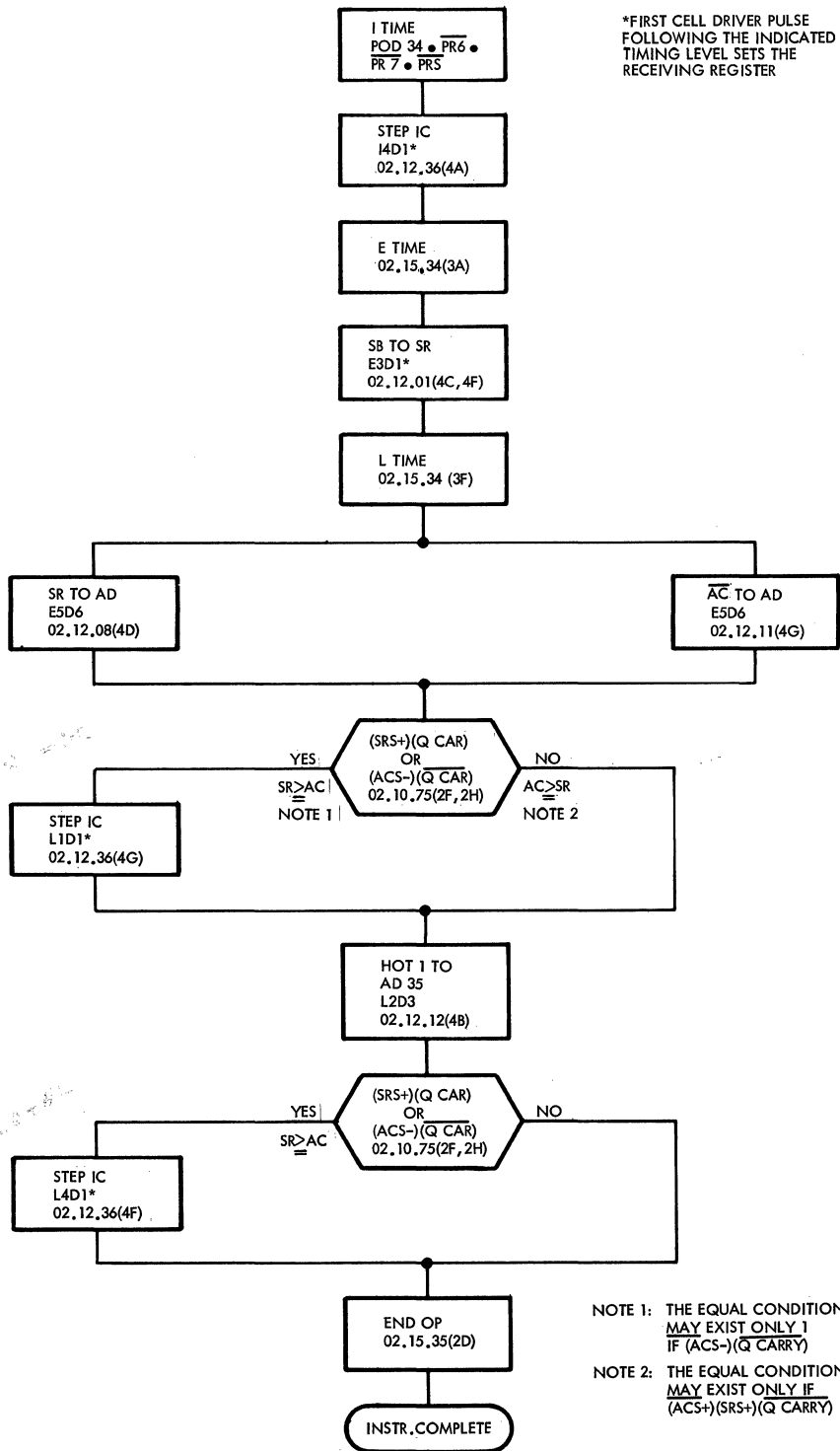


SEQUENCE NOTES:

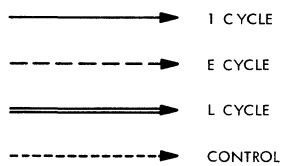
LOGICAL MULTIPLICATION OF AC_P, 1-35 AND C(Y)_S, 1-35.
AC(S) AND AC(Q) ARE CLEARED. THE C(Y) ARE UNCHANGED.

Compare Accumulator with Storage (CAS +0340)
Compares algebraically the contents of the accumulator and the specified memory location. If the accumulator is the greater, the computer takes the next sequential instruction. If the accumulator and memory are equal, the computer skips the next instruction and proceeds from there. If the accumulator is less than memory, the computer skips the next two instructions.

A +0 is considered greater than a -0



LEGEND



Xfers include all bits contained in the smaller of the two registers involved, unless otherwise specified.

INST +0340 COMPARE ACCUMULATOR WITH STORAGE

ALPHA CODE: CAS CYCLES: I, E, L



SEQUENCE NOTES:

IF: C(AC) > C(Y), THE COMPUTER TAKES NEXT INSTRUCTION.

C(AC) = C(Y), THE COMPUTER SKIPS 1 INSTRUCTION.

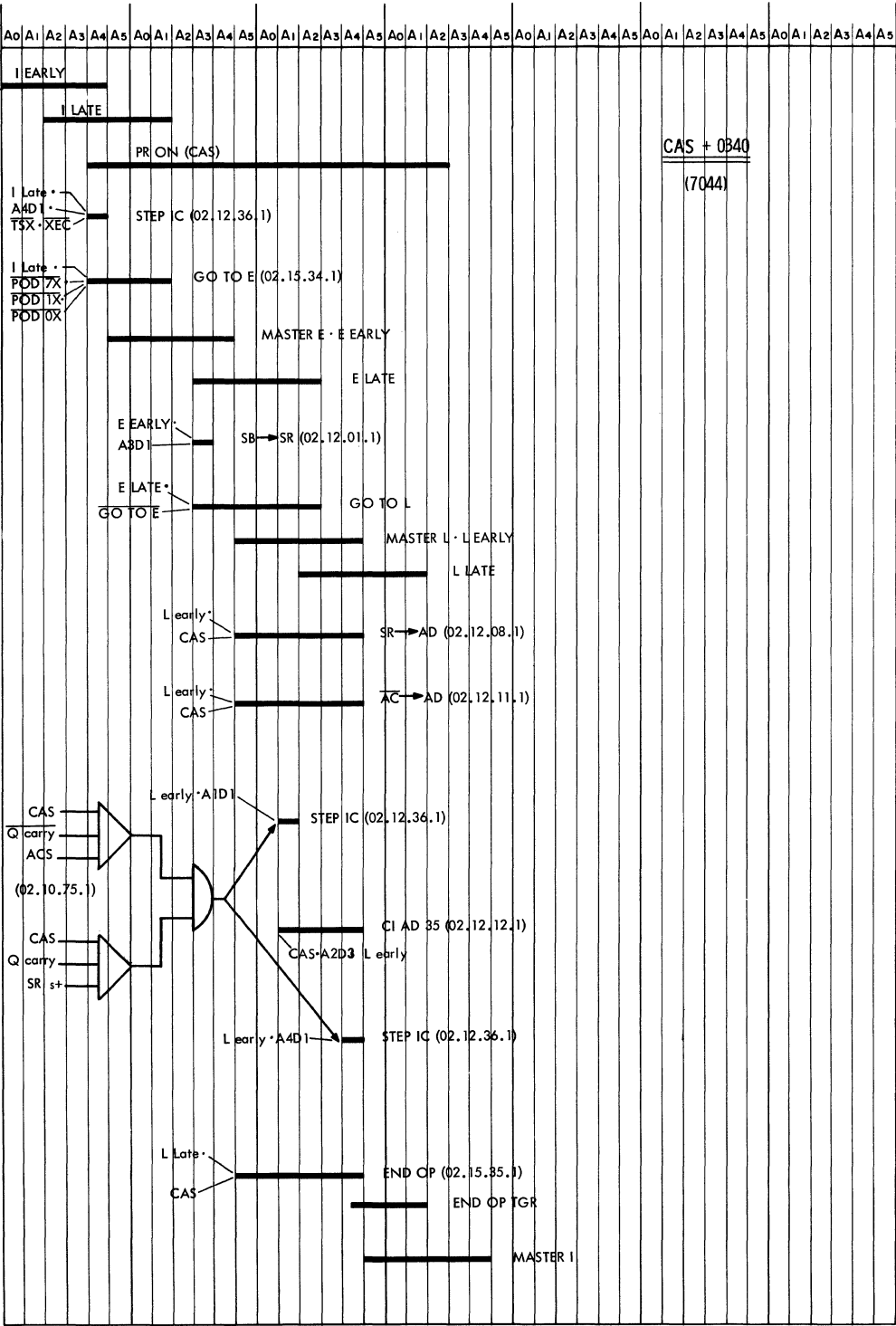
C(AC) < C(Y), THE COMPUTER SKIPS 2 INSTRUCTIONS.

A PLUS ZERO (+0) IS CONSIDERED GREATER THAN A MINUS ZERO (-0).

CYCLES REQUIRED: 7040: I, E
7044: I, E, L

*3, *5 AC(S)-, Q CAR
SR(S)+, Q CAR

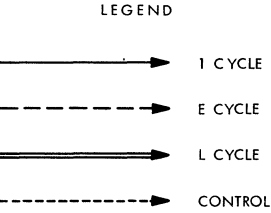
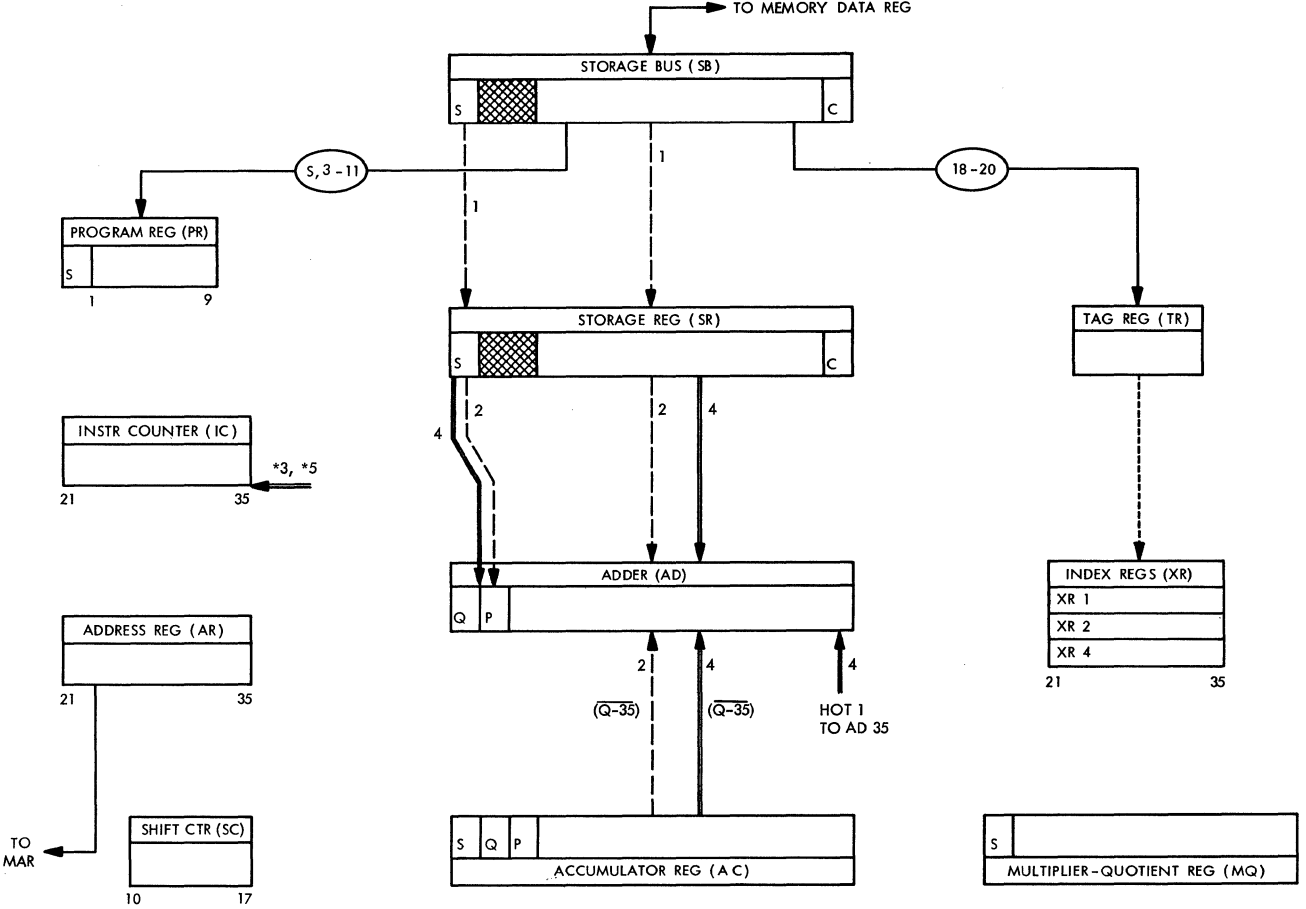
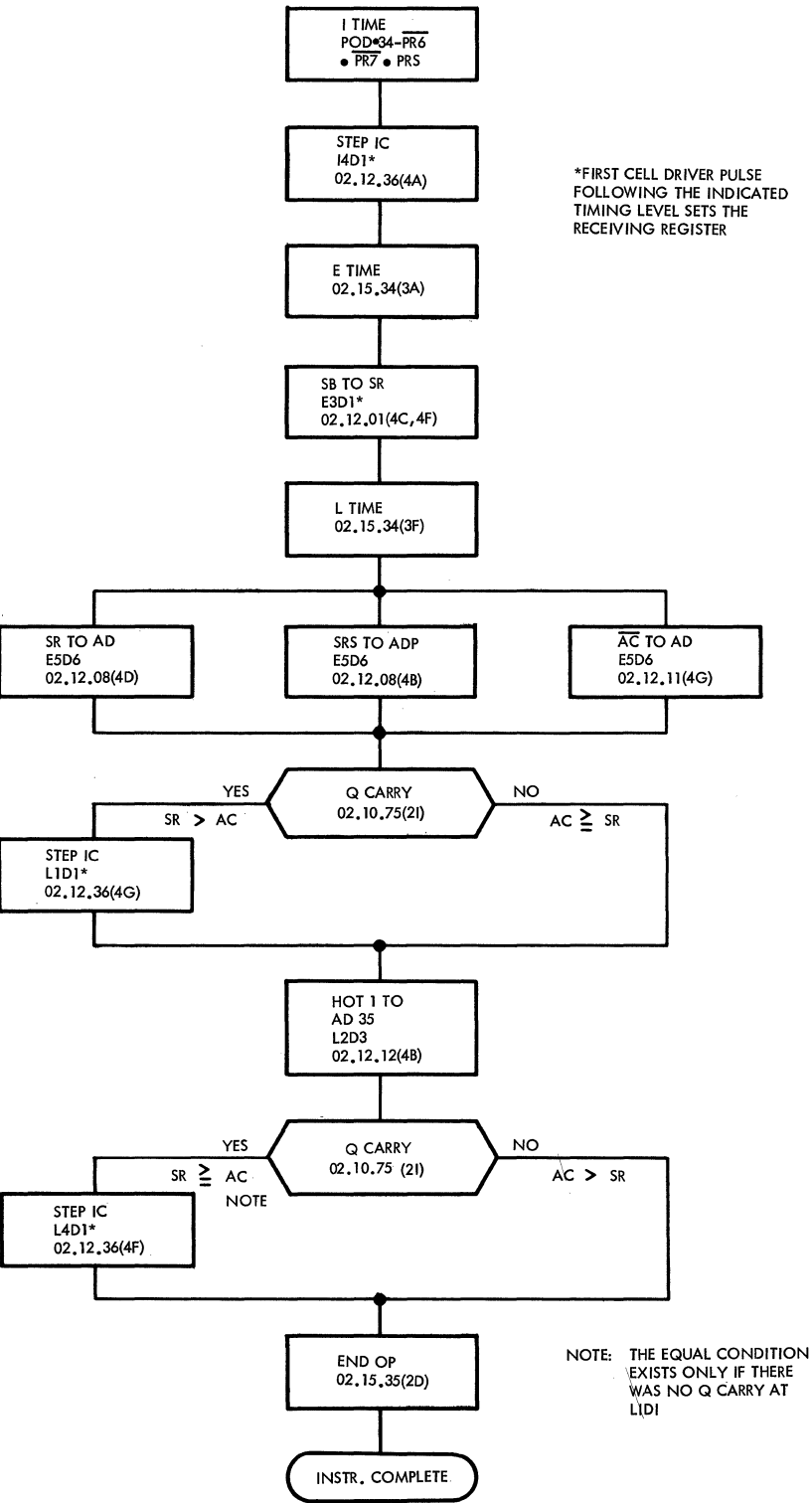
FIGURE 23. CAS



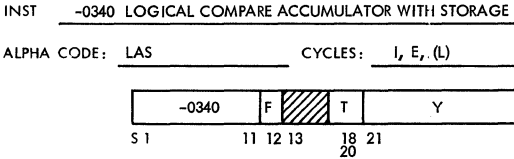
Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	CAS		00006	034000 000006
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			177777 777777
00006	Pattern			777777 777777

Compare Accumulator to Storage (CAS)																	
CONSOLE INDICATORS																	
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY
I	E	00001	+500	000	0	00005	050000000005	000000000000									0
E	I	00001	+500	000	0	00001	177777777777	177777777777									0
I	E	00002	+340	000	0	00006	034000000006	177777777777									0
E	L	00002	+340	000	0	00006	777777777777	177777777777									0
L	I	00002	+340	000	0	00002	777777777777	177777777777									1
I	I	00003	+020	000	0	00000	002000000000	177777777777									0
I	E	00001	+500	000	0	00005	050000000005	177777777777									0

Logical Compare Accumulator with Storage (LAS -0340)
Compares the contents of the accumulator (Q,P,1-35) with the contents of the specified memory location (S,1-35). The accumulator is treated as an unsigned 37-bit number and the memory word is treated as an unsigned 36-bit number. If the accumulator is the greater, the computer takes the next sequential instruction. If the accumulator equals memory, the computer skips the next instruction and proceeds from there. If the accumulator is less than memory, the computer skips the next two instructions and proceeds from there.



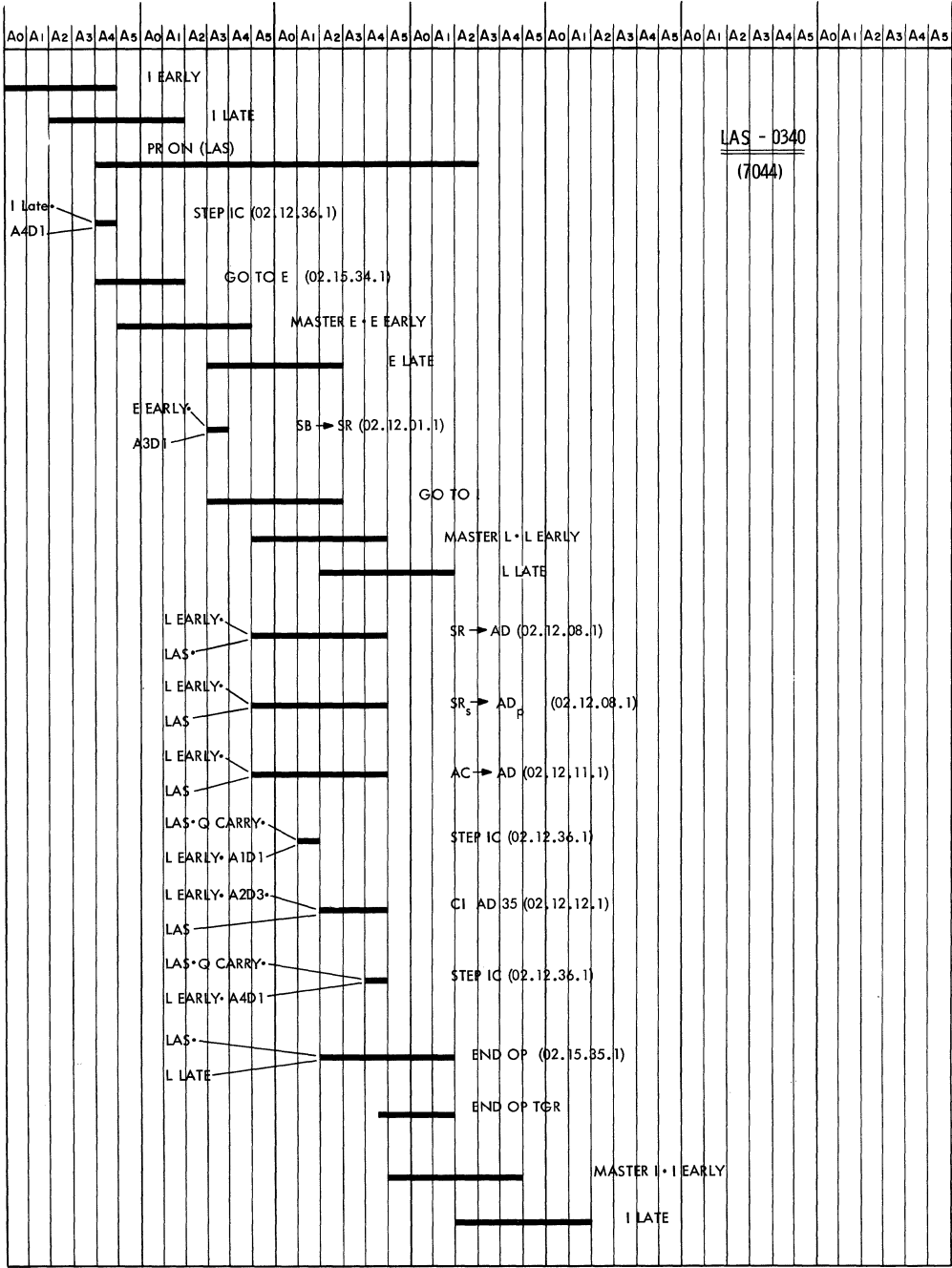
XFRS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.



SEQUENCE NOTES:

- IF: $C(AC)_{Q,P,1-35} > C(Y)_{S,1-35}$ THE COMPUTER TAKES NEXT INSTRUCTION.
- $C(AC)_{Q,P,1-35} = C(Y)_{S,1-35}$ THE COMPUTER SKIPS 1 INSTRUCTION.
- $C(AC)_{Q,P,1-35} < C(Y)_{S,1-35}$ THE COMPUTER SKIPS 2 INSTRUCTIONS.
- THE AC IS TREATED AS AN UNSIGNED 37-BIT REGISTER.
- THE C(Y) IS TREATED AS AN UNSIGNED 36-BIT REGISTER.
- CYCLES REQUIRED: 7040: I, E
7044: I, E, L
- *3, *5 (Q CAR)

FIGURE 24. LAS



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	LAS		00006	434000 000006
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			377777 777777
00006	Pattern			377777 777776

Logical Compare Accumulator to Storage (LAS)																			
CONSOLE INDICATORS																			
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	P CARRY	P OVERFLOW	FP 1
I	E	00001	+500	000	0	00005	0500000000005	0000000000000	00										
E	I	00001	+500	000	0	00001	3777777777777	3777777777777	00										
I	E	00002	-340	000	0	00006	4340000000006	3777777777777	00										
E	L	00002	-340	000	0	00006	3777777777776	3777777777777	00										
L	I	00002	-340	000	0	00002	3777777777776	3777777777777	00										
I	I	00003	+020	000	0	00000	0020000000000	3777777777777	00										
I	E	00001	+500	000	0	00005	0500000000005	3777777777777	00										

Complement Magnitude (COM+0760...0006)
Replaces all 1's with 0's, and all 0's with 1's, in the accumulator
Q,P,1-35 positions. Accumulator sign is unchanged.

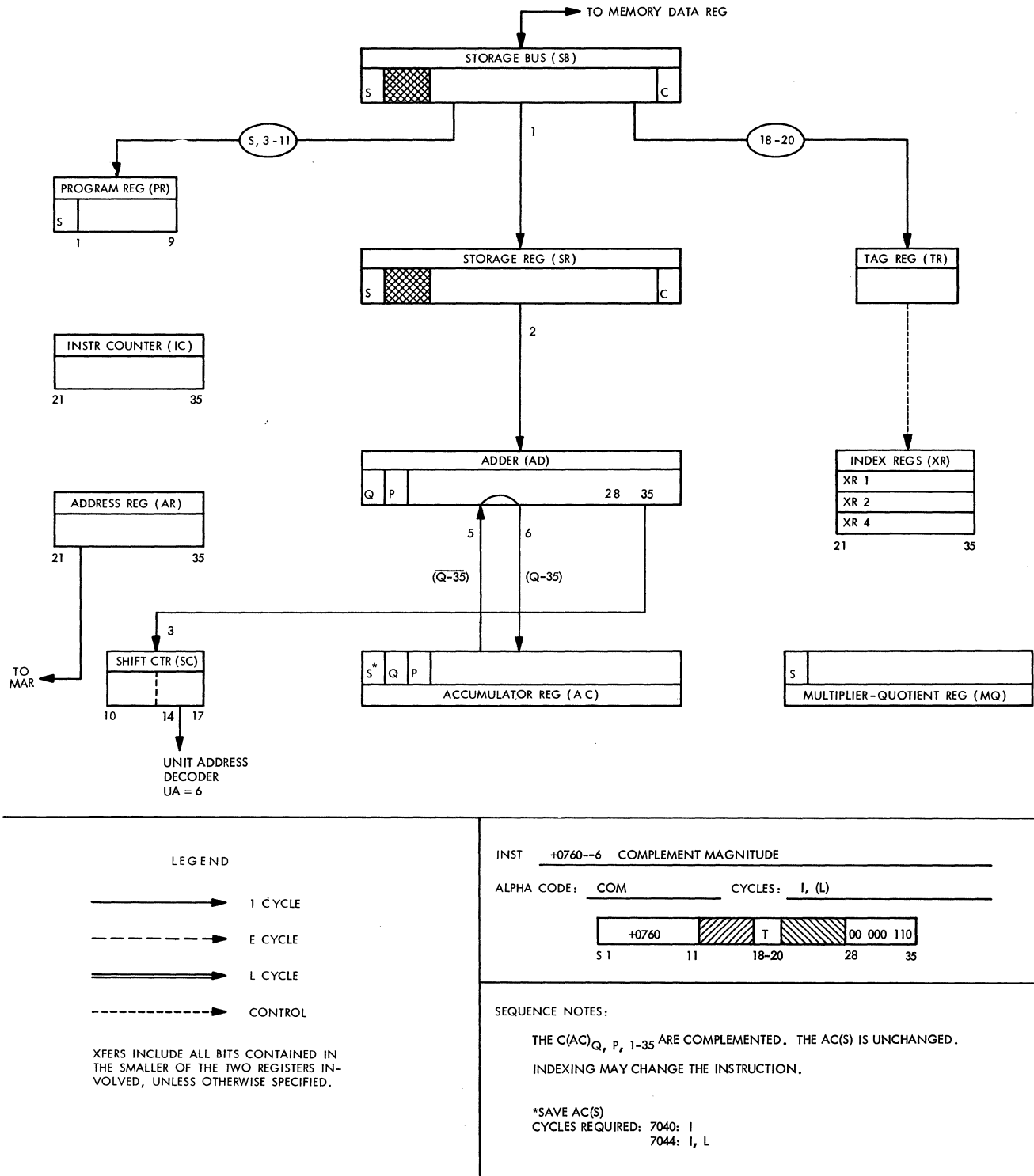
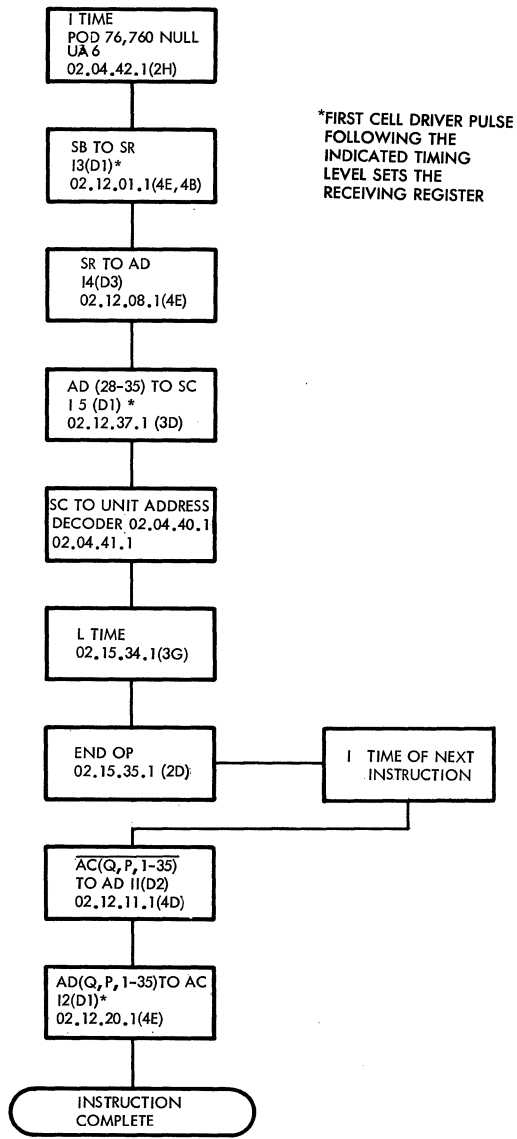
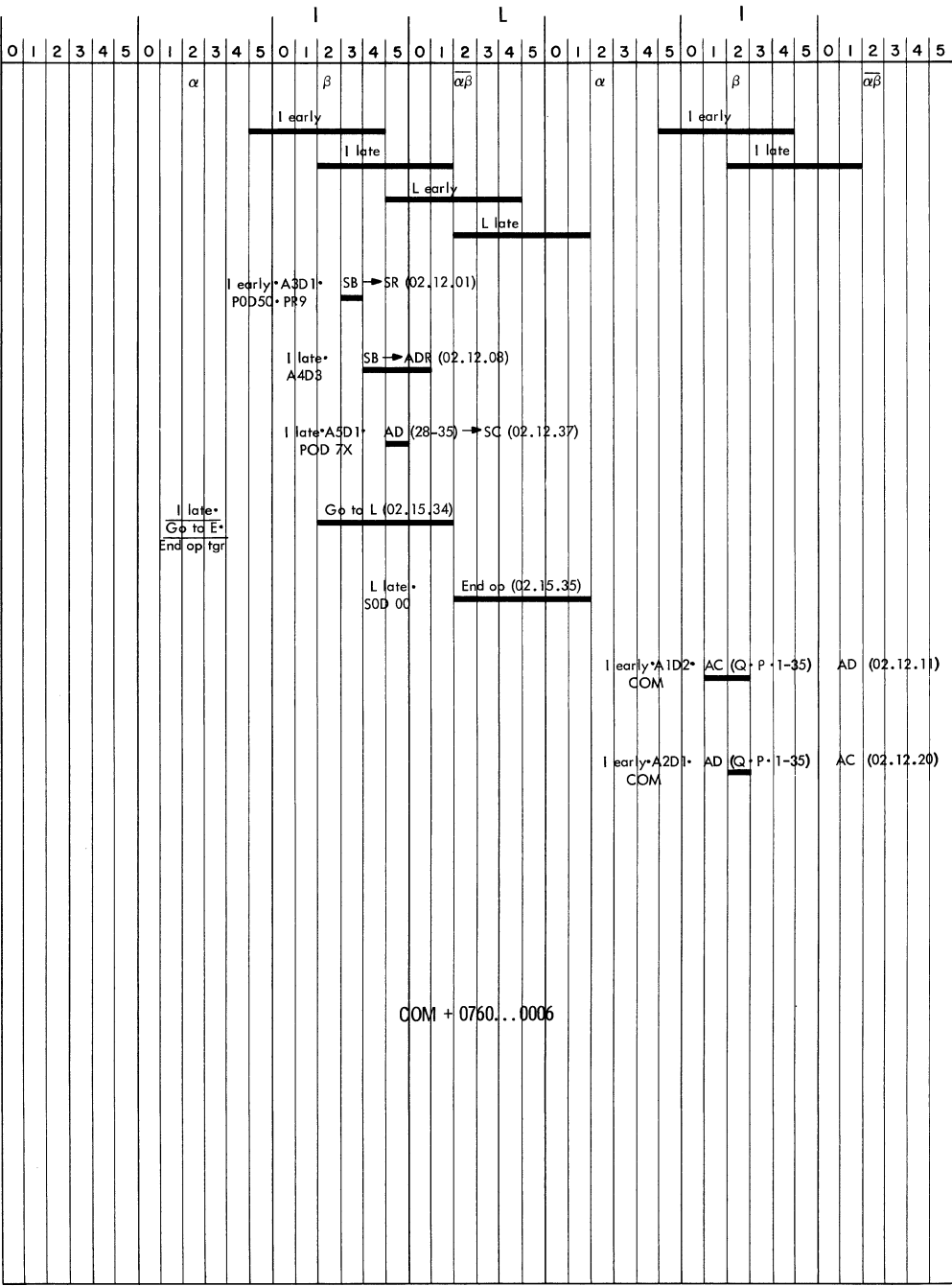


FIGURE 25. COM

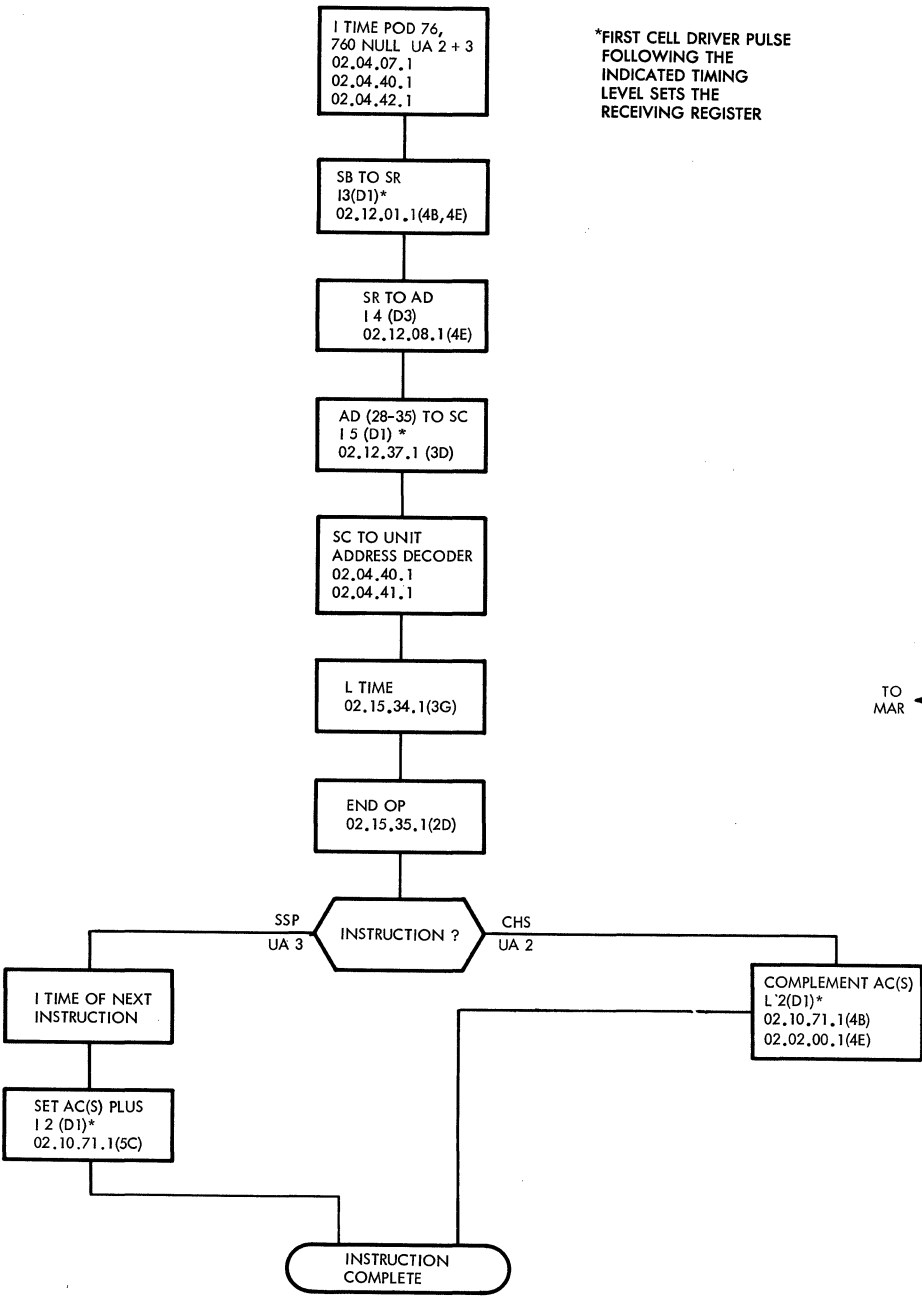


Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	COM		00006	076000 000006
00002	TRA		00001	002000 000001
00003				
00004				
00005				
00006	Pattern			777777 777777

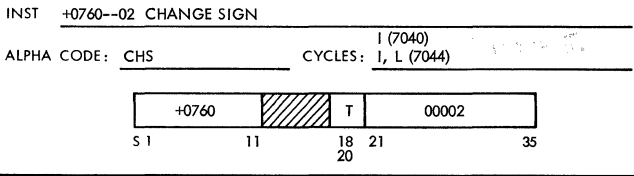
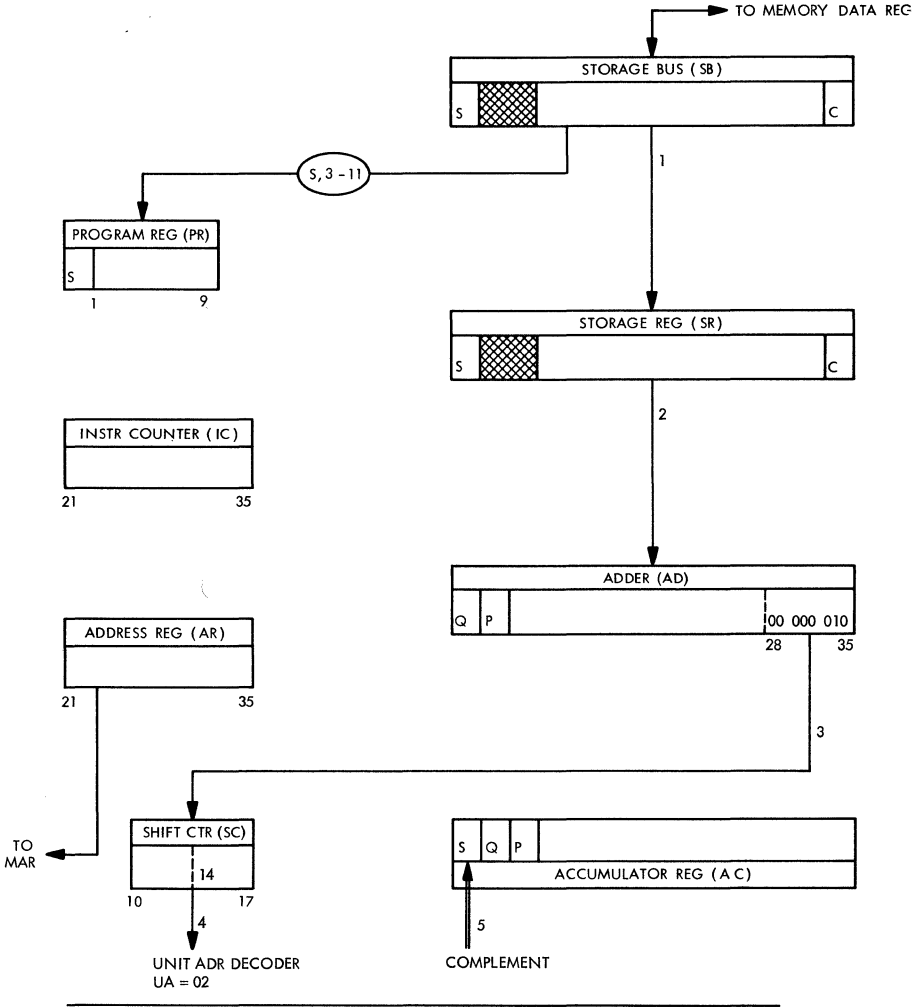
Complement Magnitude (COM)																	
CONSOLE INDICATORS																	
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (A 1-35)	ACCUMULATOR (Q P)	MQ REGISTER (S 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	P CARRY
I	E	00001	+500	000	0	00006	050000000000	000000000000	00								
E	I	00001	+500	000	0	00001	777777777777	777777777777	00								
I	L	00002	+760	006	0	00006	076000000006	777777777777	00								
L	I	00002	+760	006	0	00002	076000000006	777777777777	00								
I	I	00003	+020	000	0	00001	002000000001	400000000000	11								
I	L	00002	+760	006	0	00006	076000000006	400000000000	11								
L	I	00002	+760	006	0	00002	076000000006	400000000000	11								
I	I	00003	+020	000	0	00001	002000000001	777777777777	00								
I	L	00002	+760	006	0	00006	076000000006	777777777777	00								
L	I	00002	+760	006	0	00002	076000000006	777777777777	00								

Change Sign (CHS +0760 ... 0002)
Makes the accumulator sign negative if it is plus, and plus if it is negative.
The rest of the accumulator is unchanged.

Set Sign Plus (SSP +0760 ... 0003)
Sets the accumulator sign to plus.

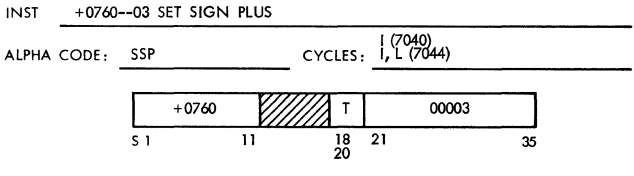
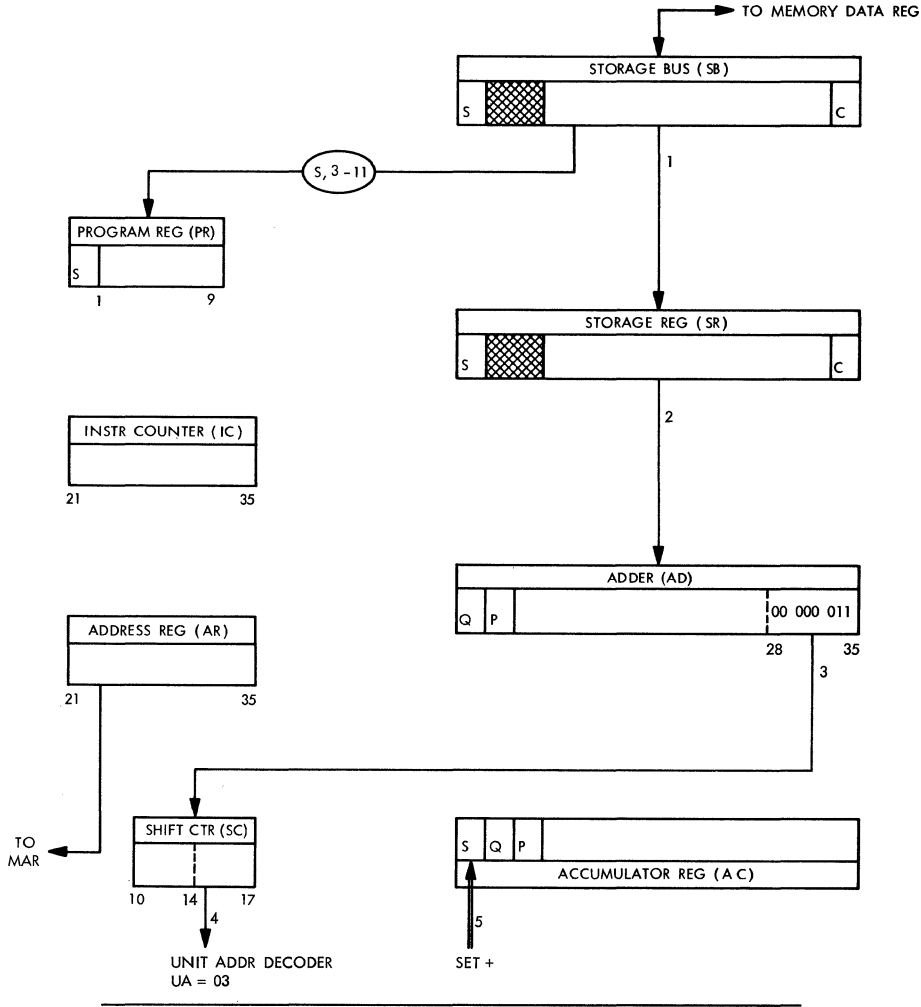


*FIRST CELL DRIVER PULSE
FOLLOWING THE
INDICATED TIMING
LEVEL SETS THE
RECEIVING REGISTER



SEQUENCE NOTES:

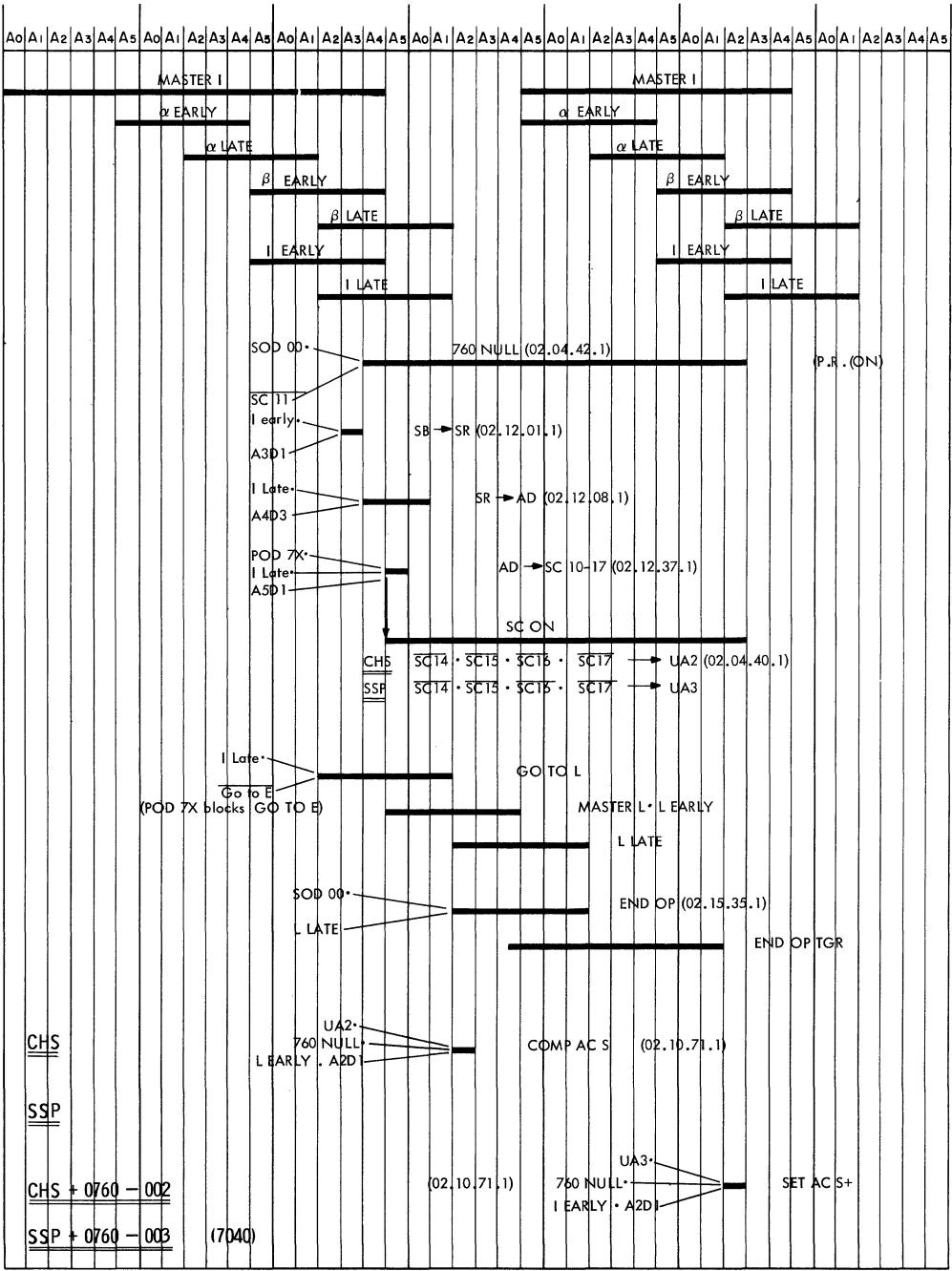
CHANGE THE SIGN OF THE ACCUMULATOR. INDEXING MAY CHANGE
THE OPERATION. THE C(AC)_{Q, P, 1-35} ARE UNCHANGED.



SEQUENCE NOTES:

THE SIGN OF THE AC IS SET TO PLUS (0).
INDEXING MAY CHANGE THE OPERATION.
THE C(AC)_{Q, P, 1-35} ARE UNCHANGED.

FIGURE 26. CHS, SSP



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	CHS		00002	076000 000002
00002	CHS		00002	076000 000002
00003	TRA		00000	002000 000000
00004	Pattern			377777 777777
00005				
00006				

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	SSP		00003	076000 000003
00002	SSP		00003	076000 000003
00003	TRA		00000	002000 000000
00004	Pattern			777777 777777
00005				
00006				

Change Sign (CHS)											
CONSOLE INDICATORS											
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER
I	E	00001	+500	000	0	00006	0500000000006	0000000000000	00		
E	I	00001	+500	000	0	00001	3777777777777	3777777777777	00		
I	L	00002	+760	002	0	00002	0760000000002	3777777777777	00		
L	I	00002	+760	002	0	00002	0760000000002	7777777777777	00		
I	L	00003	+760	002	0	00002	0760000000002	7777777777777	00		
L	I	00003	+760	002	0	00003	0760000000002	3777777777777	00		
I	I	00004	+020	000	0	00000	0020000000000	3777777777777	00		
I	E	00001	+500	000	0	00006	0500000000006	3777777777777	00		

Set Sign Plus (SSP)											
CONSOLE INDICATORS											
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (A, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER
I	E	00001	+500	000	0	00006	050000000006	000000000000	00		
E	I	00001	+500	000	0	00001	777777777777	777777777777	00		
I	L	00002	+760	003	0	00003	076000000003	777777777777	00		
L	I	00002	+760	003	0	00002	076000000003	777777777777	00		
I	L	00003	+760	003	0	00003	076000000003	377777777777	00		
L	I	00003	+760	003	0	00003	076000000003	377777777777	00		
I	I	00004	+020	000	0	00000	002000000000	377777777777	00		
I	E	00001	+500	000	0	00006	050000000006	377777777777	00		

Make Storage Sign Minus (MSM -1623.6)
Makes the specified memory location sign minus. The rest of the memory word is unchanged.

Make Storage Sign Plus (MSP -1623.7)
Makes the specified memory location sign plus. The rest of the memory word is unchanged.

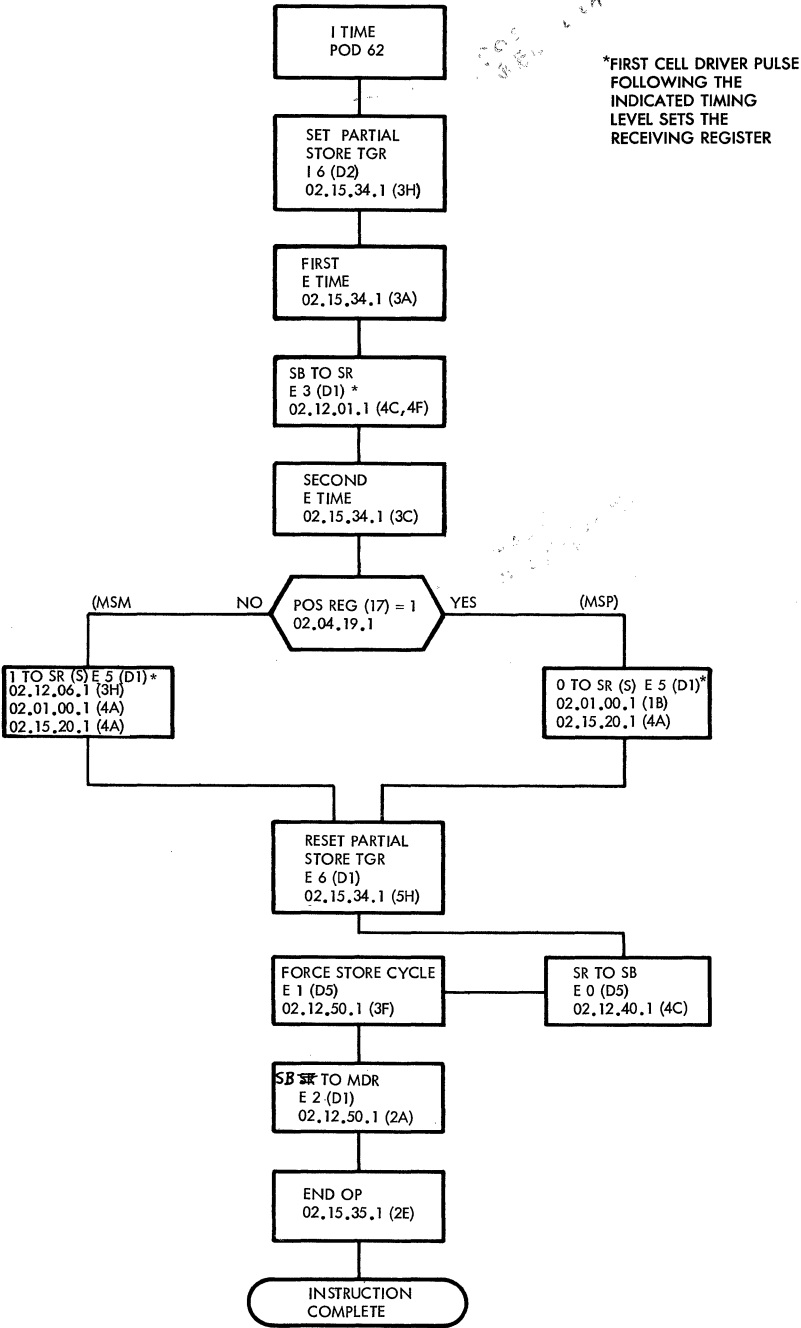
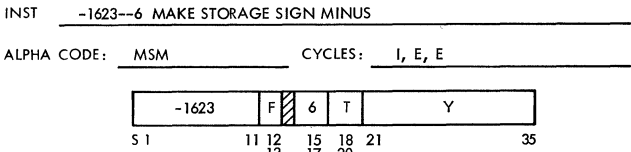
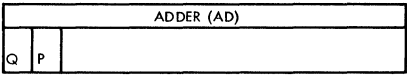
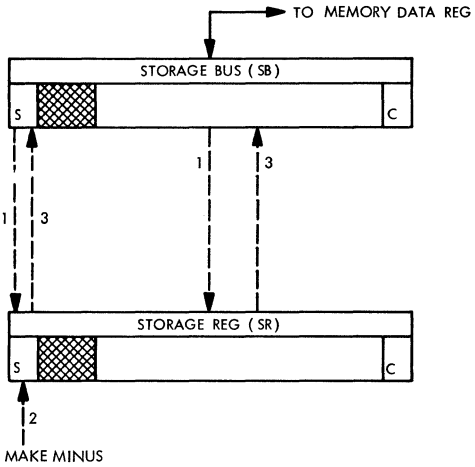


FIGURE 27. MSM,MSP

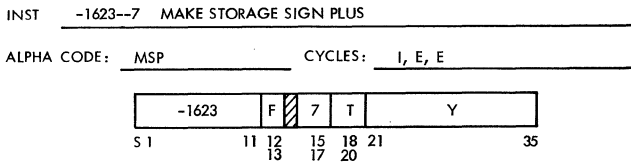
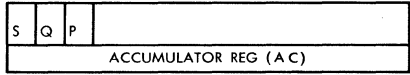
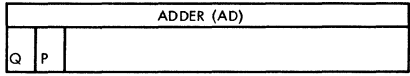
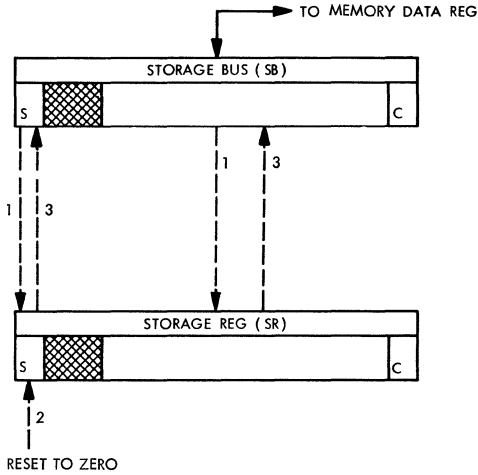


SEQUENCE NOTES:

THE SIGN BIT OF C(Y) IS REPLACED BY A 1 BIT (MINUS).

THE REMAINDER OF Y IS UNCHANGED.

POSITIONS 15-17 MUST CONTAIN 6g.

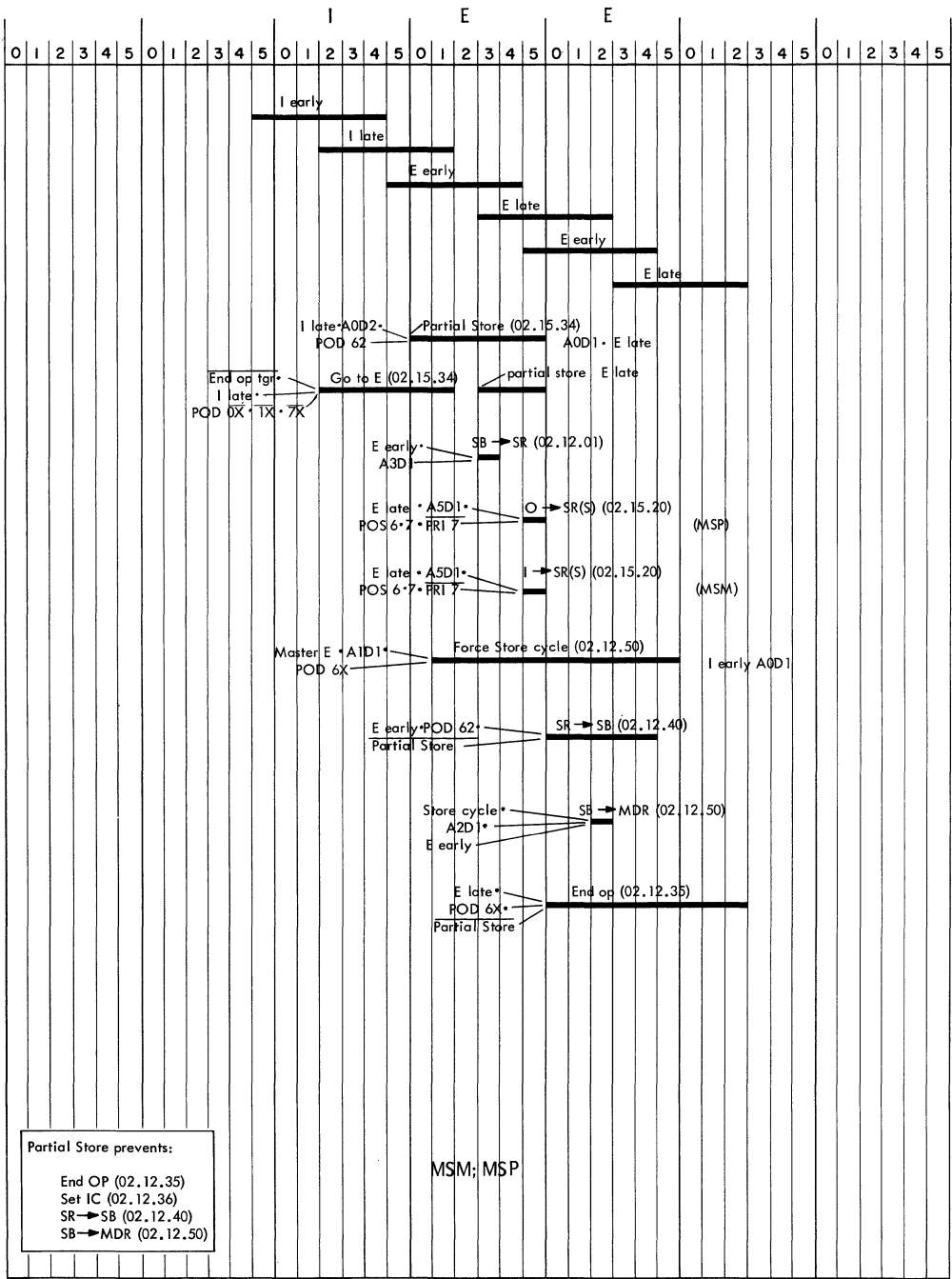


SEQUENCE NOTES:

THE SIGN BIT OF C(Y) IS REPLACED BY A ZERO BIT (PLUS).

THE REMAINDER OF Y IS UNCHANGED.

POSITIONS 15-17 MUST CONTAIN



Location Switches	Inst	Tag	Address	Octal Equiv
00000	MSM, 6		00007	562306 000007
00001	MIT, 6		00007	534106 000007
00002	HPR			042000 000000
00003	TRA		00000	002000 000000

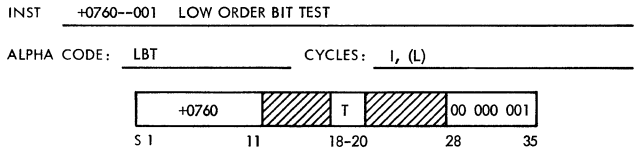
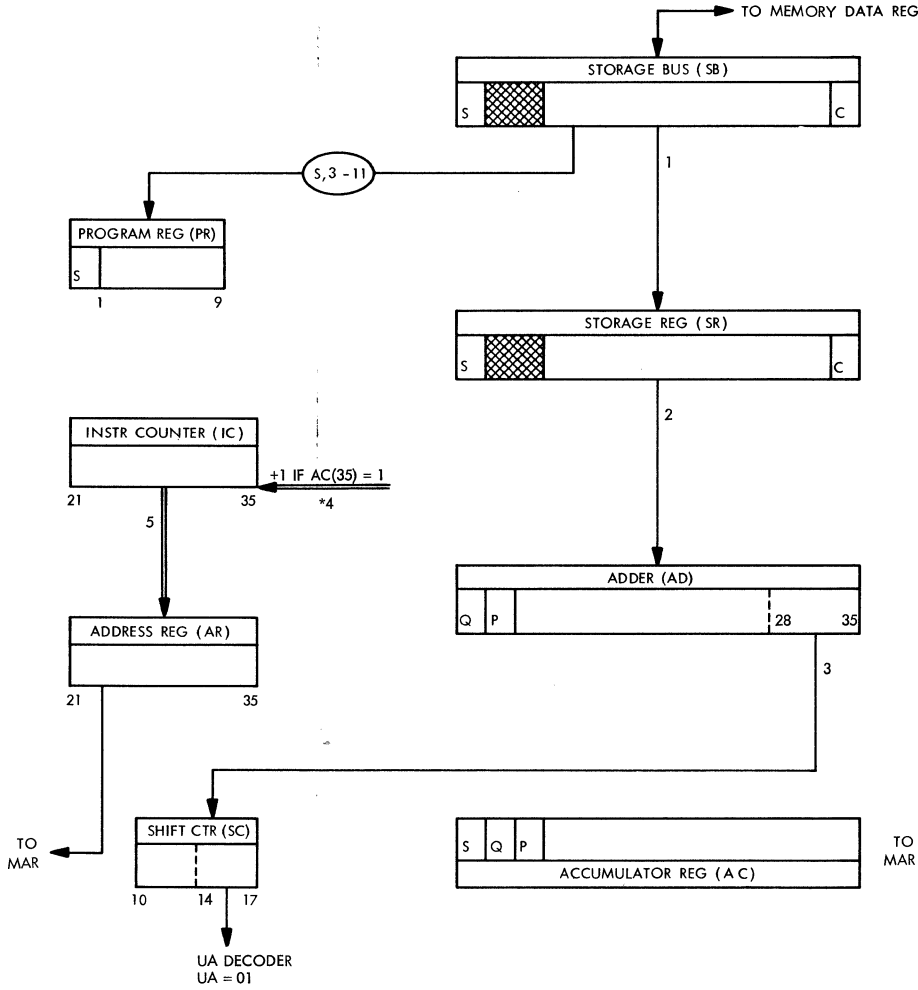
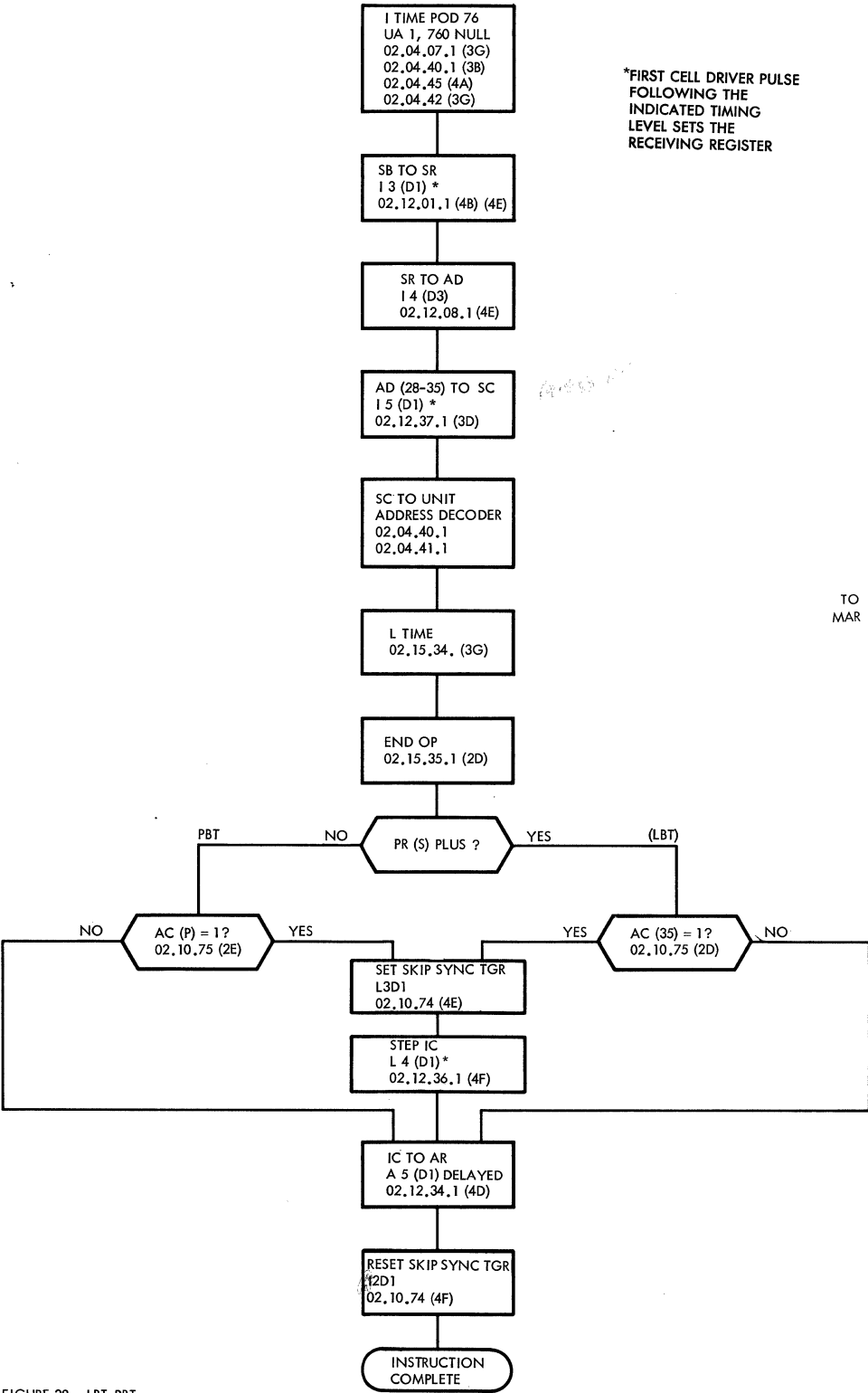
Make Storage Sign Minus (MSM)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY
I	E(1)	00001	-623	000	0	00007	562306000007								
E(1)	E(2)	00001	-623	000	0	00007	400000000000								
E(2)	I	00001	-623	000	0	00001	400000000000								
I	E	00002	-341	000	0	00007	543106000007								
E	L	00002	-341	000	0	00007	400000000000								
L	I	00003	-341	000	0	00003	400000000000								
I	I	00004	+020	000	0	00000	002000000000								

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STO		00007	060100 000007
00002	MSP, 7		00007	562307 000007
00003	PLT, 7		00007	534107 000007
00004	HPR			042000 000000
00005	TRA		00000	002000 000000
00006	Pattern			400000 000000

Make Storage Sign Plus (MSP)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY
I	E	00001	+500	000	0	00006	050000000006	000000000000	00						
E	I	00001	+500	000	0	00001	400000000000	400000000000	00						
I	E	00002	+601	000	0	00007	060100000007	400000000000	00						
E	I	00002	+601	000	0	00002	400000000000	400000000000	00						
I	E(1)	00003	-623	000	0	00007	562307000007	400000000000	00						
E(1)	E(2)	00003	-623	000	0	00007	000000000000	400000000000	00						
E(2)	I	00003	-623	000	0	00003	000000000000	400000000000	00						
I	E	00004	-341	000	0	00007	534107000007	400000000000	00						
E	L	00004	-341	000	0	00007	000000000000	400000000000	00						
L	I	00005	-341	000	0	00005	000000000000	400000000000	00						
I	I	00006	+020	000	0	00000	002000000000	400000000000	00						
E	E	00001	+500	0000	0	00006	050000000006	400000000000	00						

Low-Order Bit Test (LBT +0760 ... 0001)
If accumulator bit 35 is a 1, the computer skips the next instruction. If bit 35 is a 0, the computer takes the next sequential instruction.

P-Bit Test (PBT -0760 ... 0001)
If accumulator P-bit is a 1, the computer skips the next instruction. If the P-bit is a zero, the computer takes the next sequential instruction.



SEQUENCE NOTES:

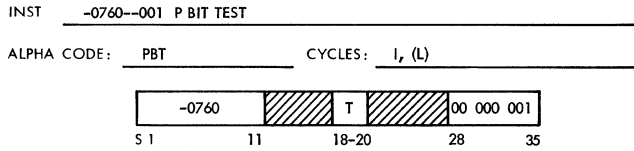
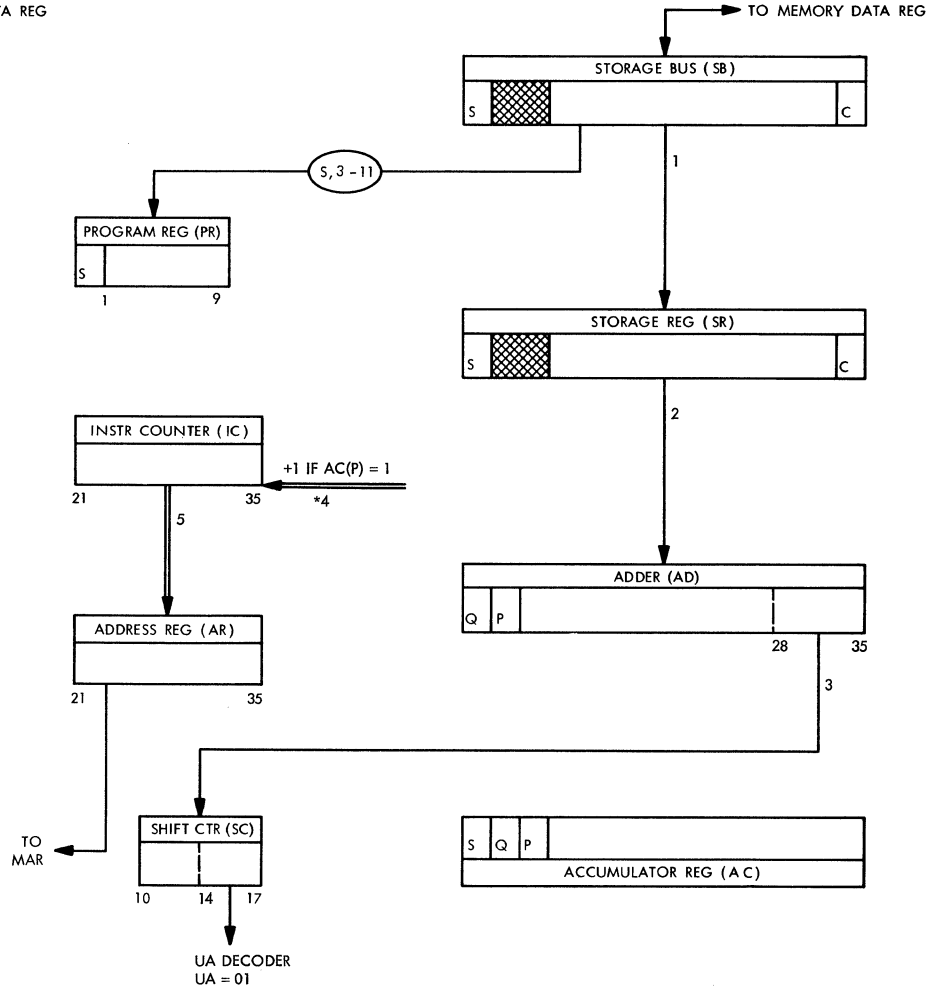
IF AC(35) = 1, THE COMPUTER SKIPS THE NEXT INSTRUCTION AND CONTINUES.

IF AC(35) = 0, THE COMPUTER TAKES THE NEXT SEQUENTIAL INSTRUCTION.

INDEXING MAY CHANGE THE INSTRUCTION.

*4 STEP I. C. BY 1 IF AC(35) = 1.

CYCLES REQUIRED: 7040: I
7044: I, L



SEQUENCE NOTES:

IF AC(P) = 1, THE COMPUTER SKIPS THE NEXT INSTRUCTION AND CONTINUES.

IF AC(P) = 0, THE COMPUTER TAKES THE NEXT SEQUENTIAL INSTRUCTION.

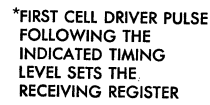
INDEXING MAY CHANGE THE INSTRUCTION.

*4 STEP I. C. BY 1 IF AC(P) = 1.

CYCLES REQUIRED: 7040: I
7044: I, L

FIGURE 28. LBT,PBT

If the divide check indicator is on, it is turned off and the computer takes the next sequential instruction. If the divide check indicator is off, the computer skips the next instruction.



1 CYCLE

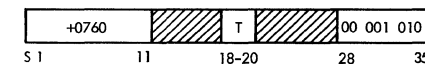
E CYCLE

L CYCLE

CONTROL

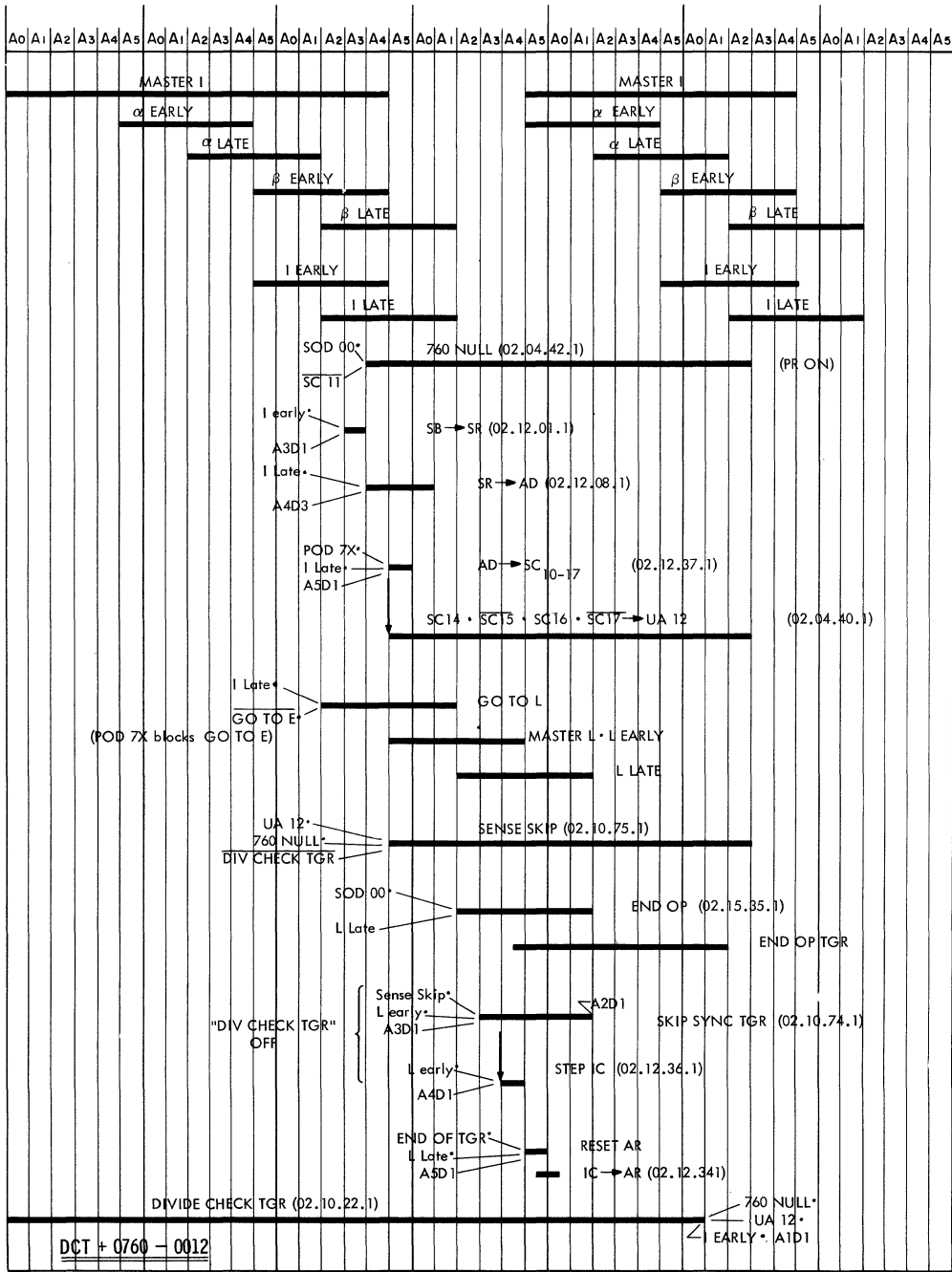
INST +0760--012 DIVIDE CHECK TEST

ALPHA CODE: DCT CYCLES: 1, (L)



IF THE DVD CHK INDICATOR IS ON, THE INDICATOR IS TURNED OFF AND THE COMPUTER TAKES THE NEXT SEQUENTIAL INSTRUCTION. IF THE INDICATOR IS OFF, THE COMPUTER SKIPS THE NEXT INSTRUCTION AND CONTINUES. INDEXING MAY CHANGE THE INSTRUCTION.

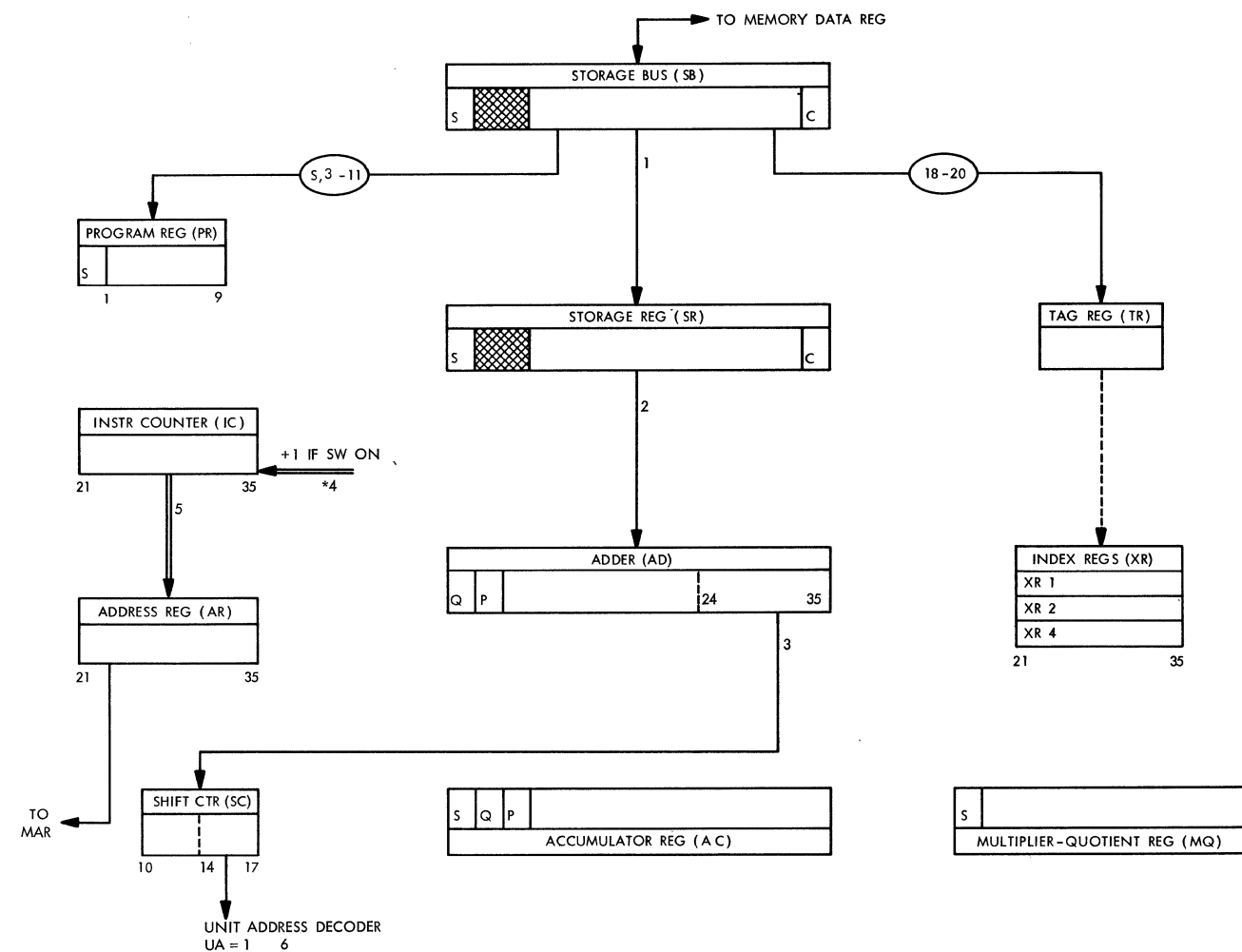
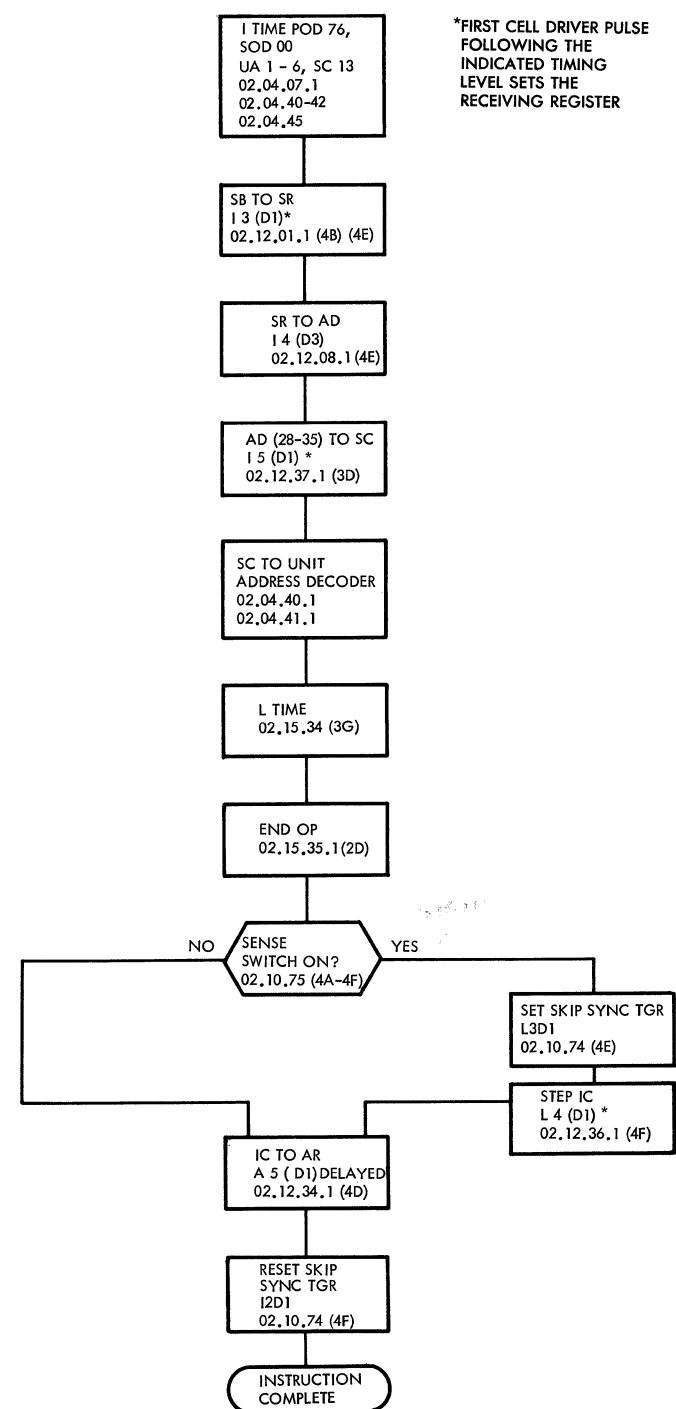
CYCLES REQUIRED: 7040: I
7044: I, L



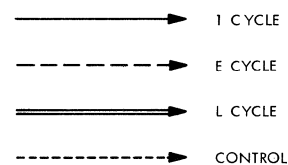
Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	DVP		00006	022100 000006
00002	DCT		00012	076000 000012
00003	TRA		00000	002000 000000
00004	HPR		00000	042000 000000
00005	Pattern			200000 000000
00006	Pattern			100000 000000

Divide Check Test (DCT)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK
I	E	00001	+500	000	0	00005	0500000000005	0000000000000	00	0000000000000					
E	I	00001	+500	000	0	00001	2000000000000	2000000000000	00	0000000000000					
I	E	00002	+221	000	0	00006	0221000000006	2000000000000	00	0000000000000					
E	L	00002	+221	000	0	00006	1000000000000	1777777777777	11	0000000000000				1	
L	I	00002	+221	000	0	00002	1000000000000	1777777777777	11	0000000000000				1	
I	L	00003	+760	012	0	00012	0760000000012	2000000000000	00	0000000000000				1	
L	I	00003	+760	012	0	00003	0760000000012	2000000000000	00	0000000000000				1	
I	I	00004	+020	000	0	00000	0020000000000	2000000000000	00	0000000000000				0	
I	E	00001	+500	000	0	00005	0500000000005	2000000000000	00	0000000000000				0	

Sense Switch Test (SWT+0760 ... 0161 to 0166)
If the switch tested is off, the computer takes the next sequential instruction.
If the switch is on, the computer skips the next instruction.



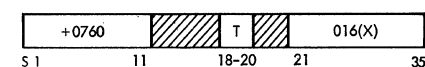
LEGEND



XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0760--0166 SENSE SWITCH TEST

ALPHA CODE: SWT CYCLES: 1, (L)



SEQUENCE NOTES:

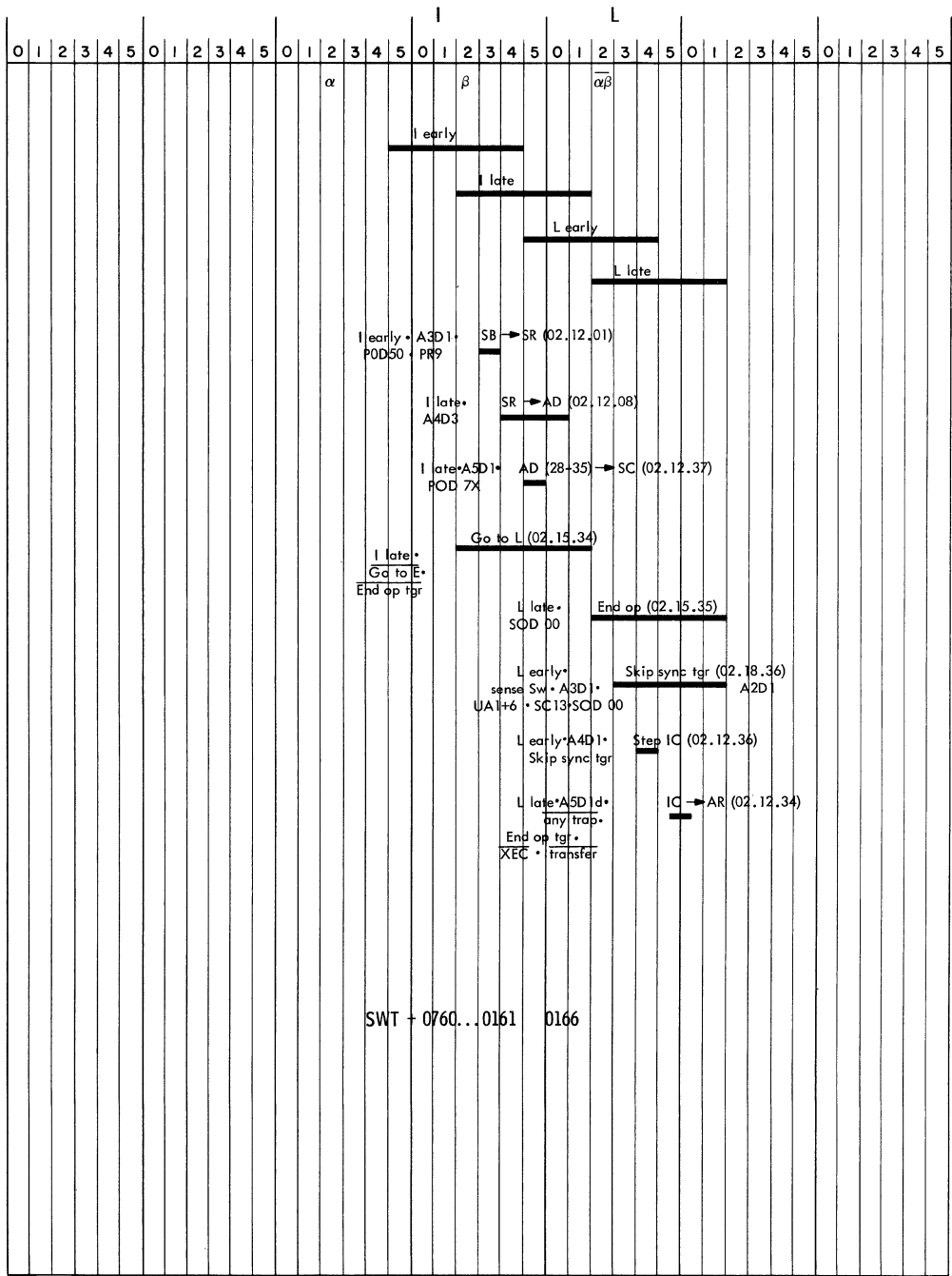
IF SENSE SWITCH IS ON (1-6), THE COMPUTER SKIPS THE NEXT INSTRUCTION AND CONTINUES.

IF THE SWITCH IS OFF, THE COMPUTER TAKES THE NEXT SEQUENTIAL INSTRUCTION.

INDEXING MAY CHANGE THE INSTRUCTION.

CYCLES REQUIRED: 7040: I
7044: I, L

FIGURE 30. SWT



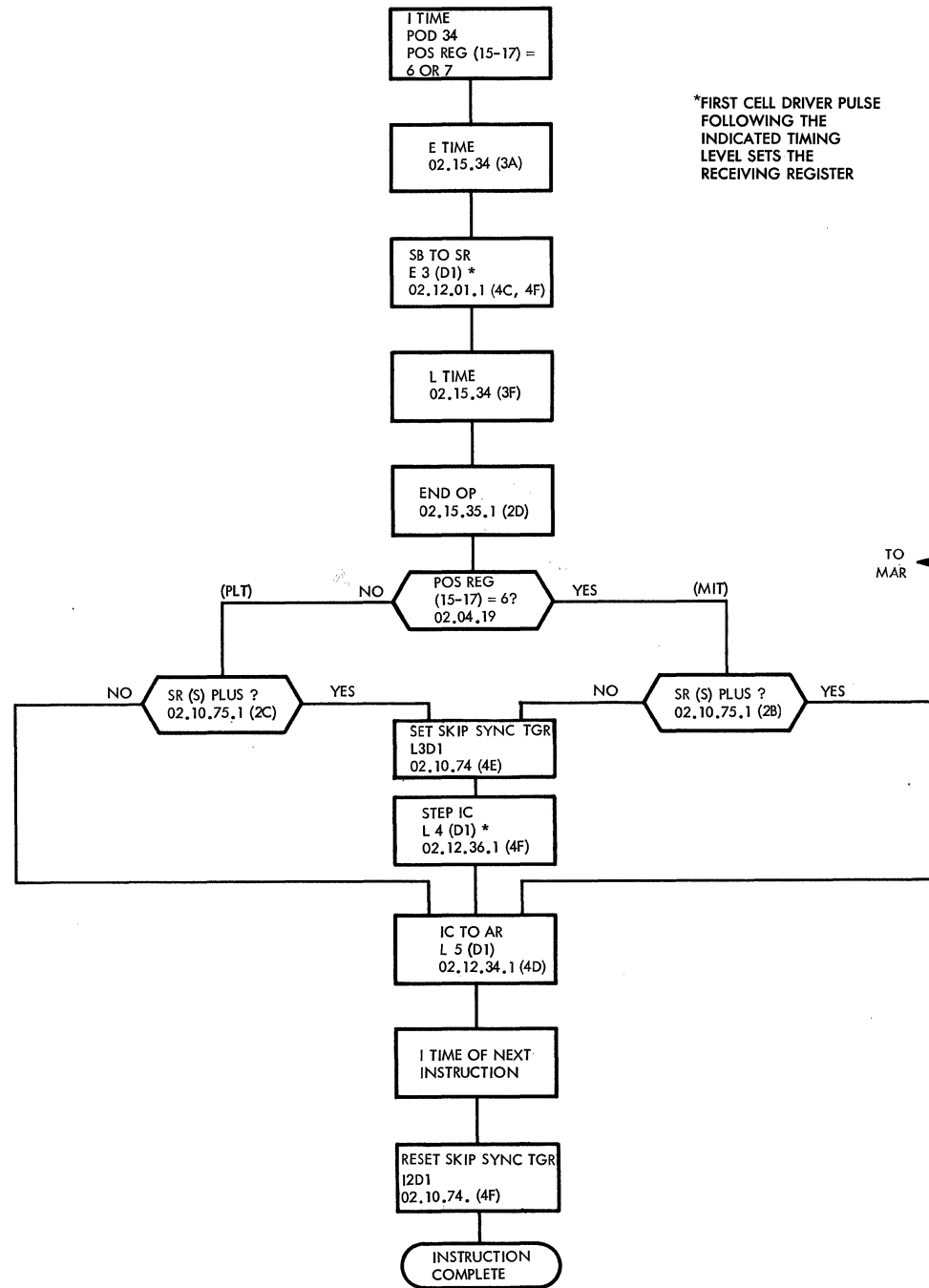
Location Switches	Inst	Tag	Address	Octal Equiv
00000	SWT		00161	076000 000161
00001	TRA		00000	002000 000000
00002	ADD		00004	040000 000004
00003	TRA		00000	002000 000000
00004	Pattern			000000 000001

Sense Switch Test (SWT)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S 1-35)	ACCUMULATOR (Q P)	MQ REGISTER (S 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK
I	L	00001	+760	161	0	00161	0760000000161		←						
L	I	00001	+760	161	0	00001	0760000000161		SS#1 OFF						
I	I	00002	+020	000	0	00000	0020000000000								
I	L	00001	+760	161	0	00161	0760000000161	0000000000000	*	←					
L	I	00002	+760	161	0	00002	0760000000161	0000000000000							
I	E	00003	+400	000	0	00004	0400000000004	0000000000000		SS#1 ON					
E	I	00003	+400	000	0	00003	0000000000001	0000000000001	*						
I	I	00004	+020	000	0	00000	0020000000000	0000000000000	*						
*Accumulator is increased by one for each pass.															

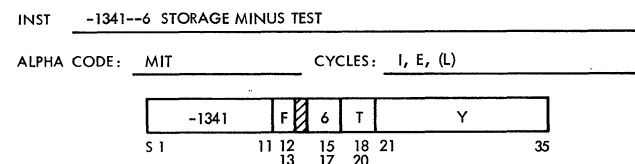
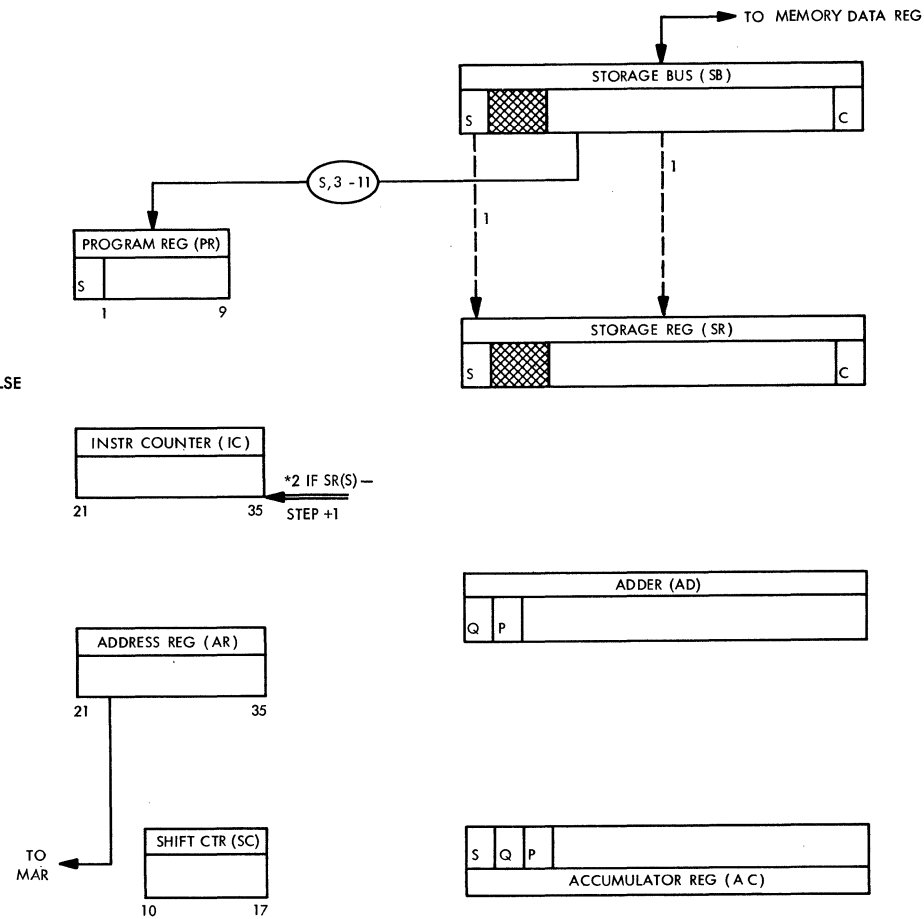
Storage Minus Test (MIT -1341.6)
If the sign of the specified memory location is minus, the computer skips the next instruction. If the sign is plus, the computer takes the next instruction.

Storage Plus Test (PLT -1341.7)
If the sign of the specified memory location is plus, the computer skips the next instruction. If the sign is minus, the computer takes the next instruction.

CCS
1341.0-5



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

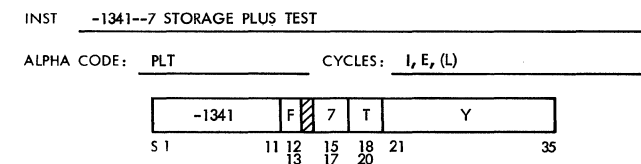
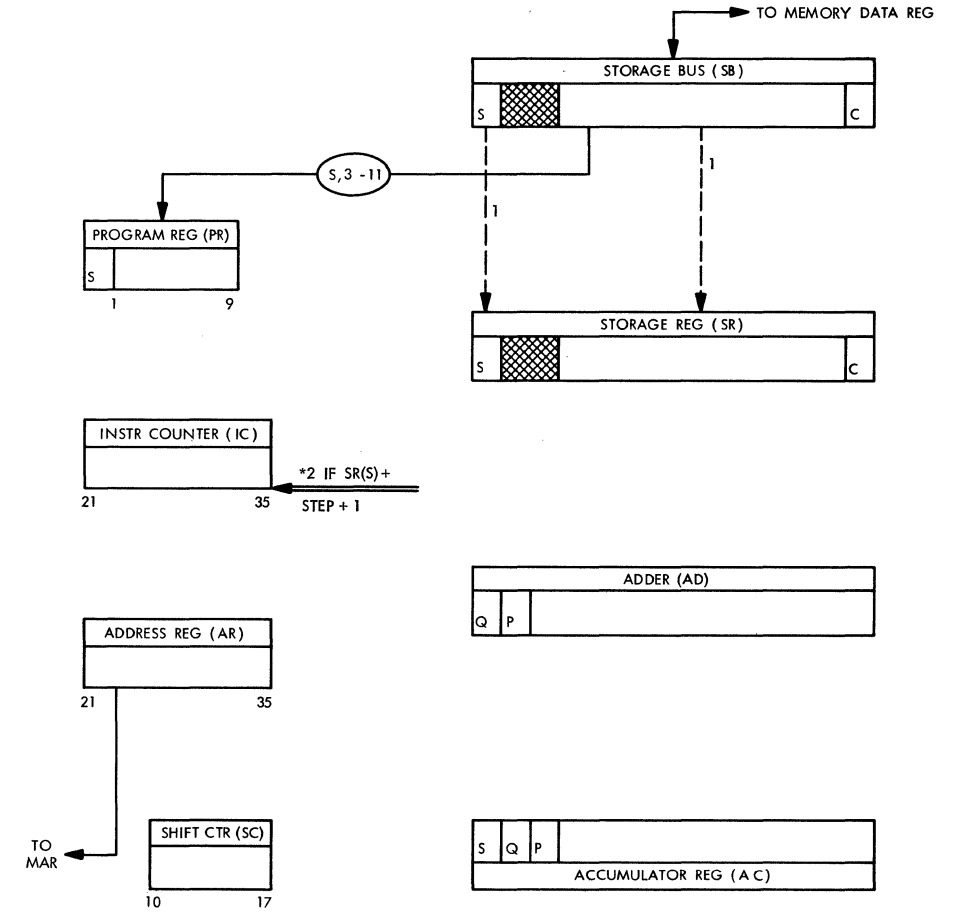


SEQUENCE NOTES:

IF THE SIGN OF LOCATION Y IS MINUS, THE COMPUTER SKIPS THE NEXT INSTRUCTION.

IF THE SIGN IS PLUS, TAKE THE NEXT INSTRUCTION.

CYCLES REQUIRED: 7040: I, E
7044: I, E, L



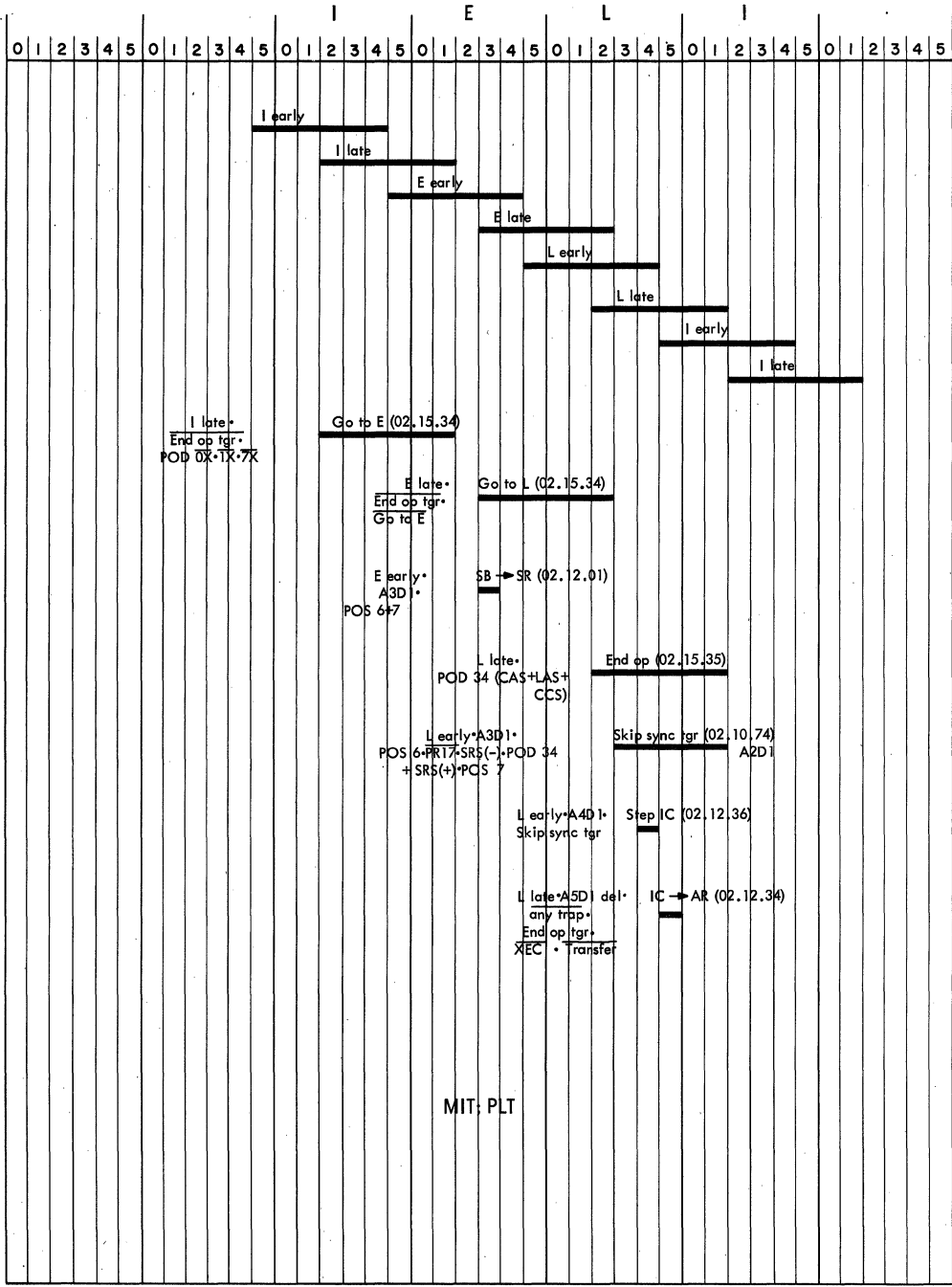
SEQUENCE NOTES:

IF THE SIGN OF LOCATION Y IS PLUS, THE COMPUTER SKIPS THE NEXT INSTRUCTION.

IF THE SIGN IS MINUS, TAKE THE NEXT INSTRUCTION.

CYCLES REQUIRED: 7040: I, E
7044: I, E, L

FIGURE 31. MIT, PLT



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STO		00007	060100 000007
00002	MIT		00007	534106 000007
00003	HPR			042000 000000
00004	TRA		00000	002000 000000
00005				
00006	Pattern			400000 000000

Storage Minus Test (MIT)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	ACCUMULATOR (Q, P)	MO REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK
E	E	00001	+500	000	0	00006	0500000000006	0000000000000	00						
E	I	00001	+500	000	0	00001	4000000000000	4000000000000	00						
I	E	00002	+601	000	0	00007	0601000000007	4000000000000	00						
E	I	00002	+601	000	0	00002	4000000000000	4000000000000	00						
I	E	00003	-341	000	0	00007	5341060000007	4000000000000	00						
E	L	00003	-341	000	0	00007	4000000000000	4000000000000	00						
L	I	00004	-341	000	0	00004	4000000000000	4000000000000	00						
I	I	00005	+020	000	0	00000	0020000000000	4000000000000	00						
I	E	00001	+500	000	0	00006	0506000000006	4000000000000	00						

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STO		00007	060100 000007
00002	PLT		00007	534107 000007
00003	HPR			042000 000000
00004	TRA		00000	002000 000000
00005	TRA		00000	002000 000000
00006	Pattern			000000 000000

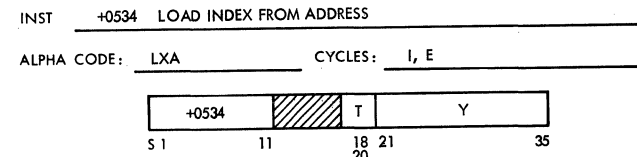
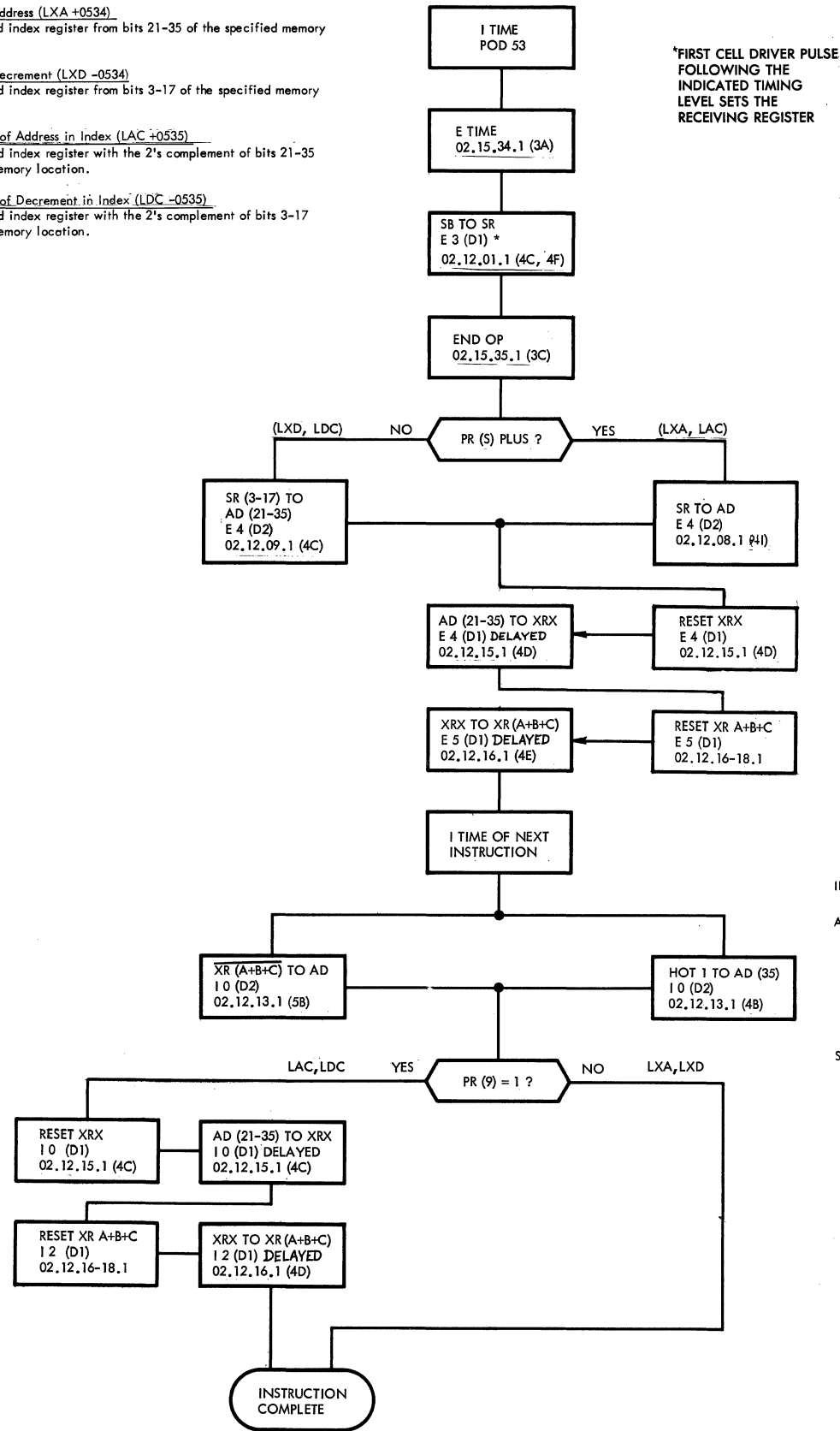
Storage Plus Test (PLT)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	ACCUMULATOR (Q, P)	MO REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK
I	E	00001	+500	000	0	00006	0500000000006	0000000000000	00						
E	I	00001	+500	000	0	00001	0000000000000	0000000000000	00						
I	E	00002	+601	000	0	00007	0601000000007	0000000000000	00						
E	I	00002	+601	000	0	00002	0000000000000	0000000000000	00						
I	E	00003	-341	000	0	00007	5341070000007	0000000000000	00						
E	L	00003	-341	000	0	00007	0000000000000	0000000000000	00						
L	I	00004	-341	000	0	00004	0000000000000	0000000000000	00						
I	I	00005	+020	000	0	00000	0020000000000	0000000000000	00						

Load Index from Address (LXA +0534)
Loads the specified index register from bits 21-35 of the specified memory location.

Load Index from Decrement (LXD -0534)
Loads the specified index register from bits 3-17 of the specified memory location.

Load Complement of Address in Index (LAC +0535)
Loads the specified index register with the 2's complement of bits 21-35 of the specified memory location.

Load Complement of Decrement in Index (LDC -0535)
Loads the specified index register with the 2's complement of bits 3-17 of the specified memory location.

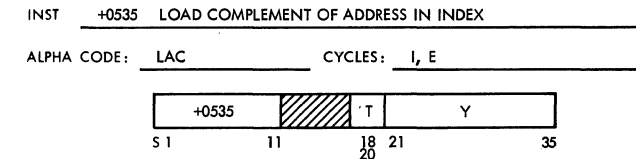
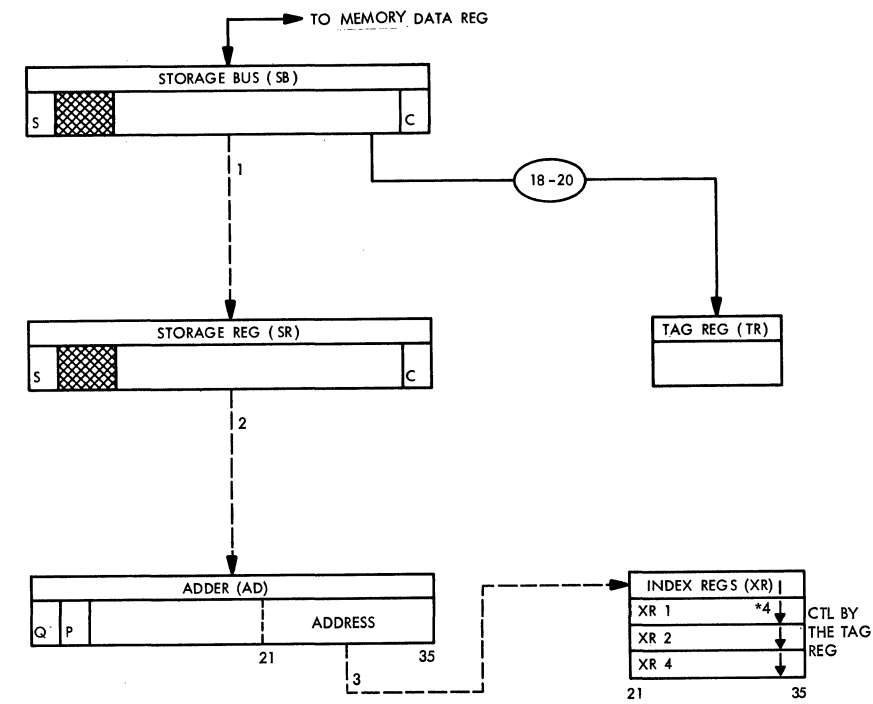


SEQUENCE NOTES:

THE SPECIFIED IX REGISTER(S) IS LOADED WITH THE C(Y)₂₁₋₃₅.

THE C(Y) ARE UNCHANGED.

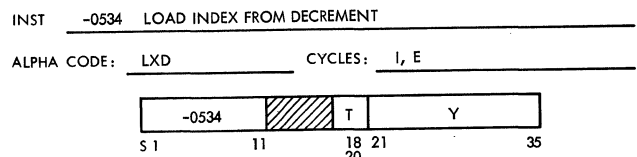
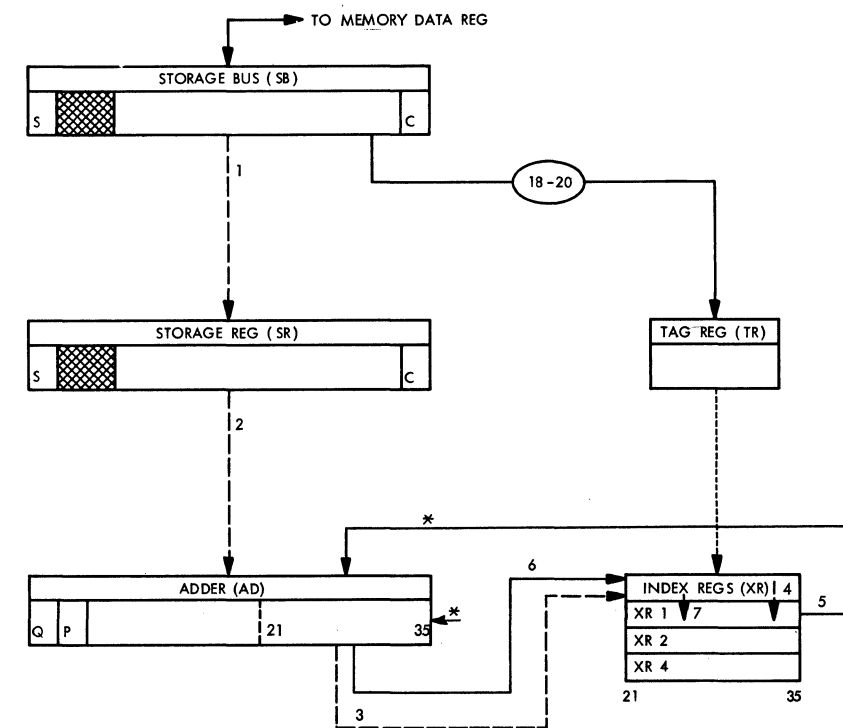
A TAG OF ZERO RESULTS IN A NO-OP.



SEQUENCE NOTES:

THE SPECIFIED INDEX REGISTER(S) IS LOADED WITH THE 2'S COMPLEMENT OF C(Y)₂₁₋₃₅. THE C(Y) ARE UNCHANGED. A TAG OF ZERO RESULTS IN A NO-OP.

* COMPLEMENT TRANSFER PLUS "HOT I" TO ADDER CAUSES 2'S COMPLEMENT

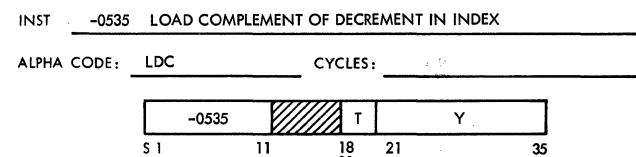
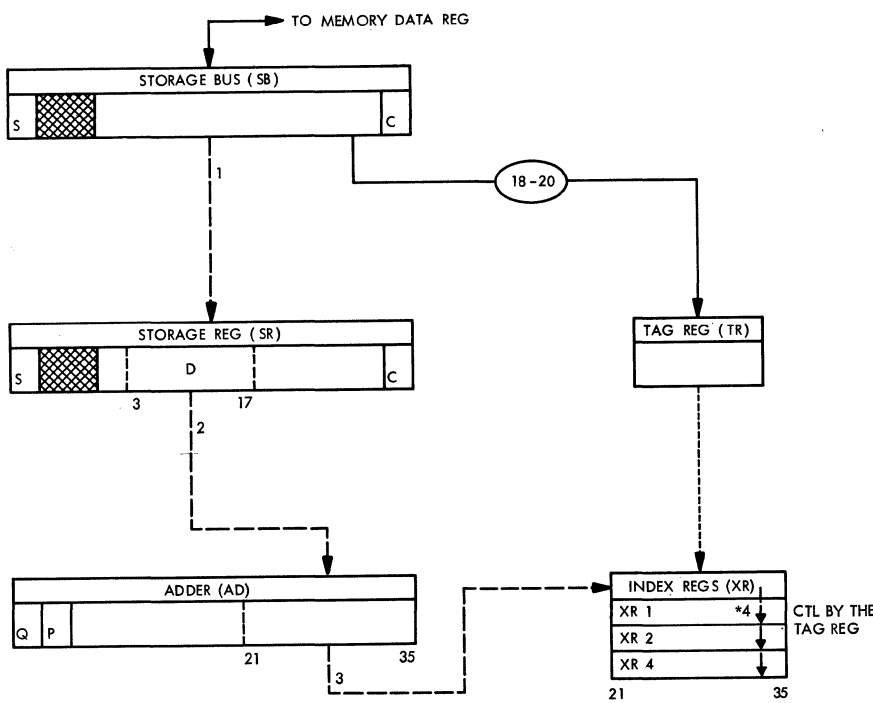


SEQUENCE NOTES:

THE SPECIFIED IX REGISTER(S) IS LOADED WITH THE C(Y)₃₋₁₇.

THE C(Y) ARE UNCHANGED.

A TAG OF ZERO RESULTS IN A NO-OP.



SEQUENCE NOTES:

THE SPECIFIED INDEX REGISTER(S) IS LOADED WITH THE 2'S COMPLEMENT OF C(Y)₃₋₁₇. THE C(Y) ARE UNCHANGED. A TAG OF ZERO RESULTS IN A NO-OP.

* COMPLEMENT TRANSFER PLUS "HOT I" TO ADDER CAUSES 2'S COMPLEMENT

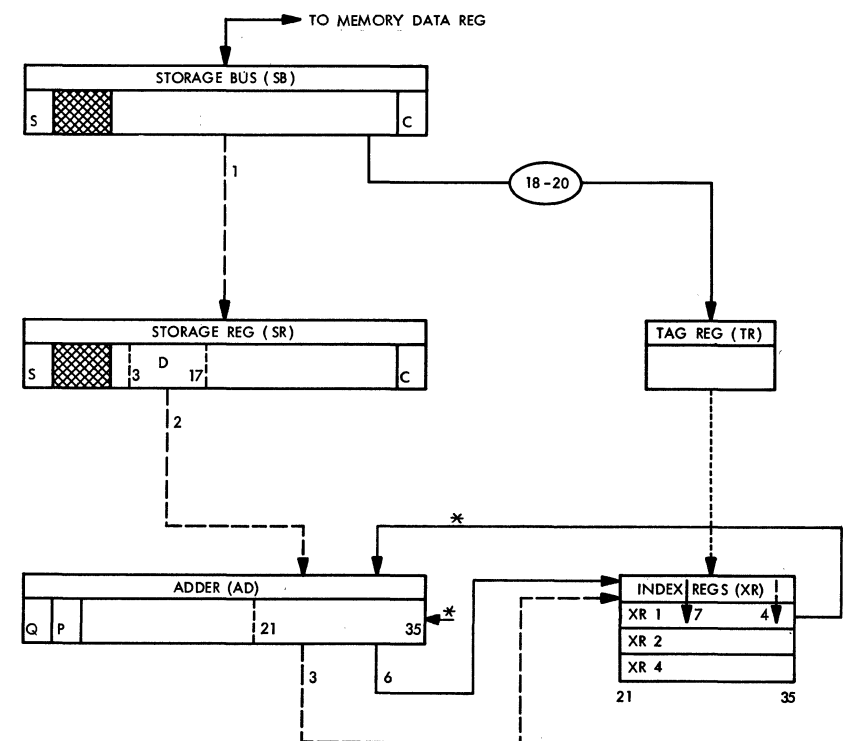
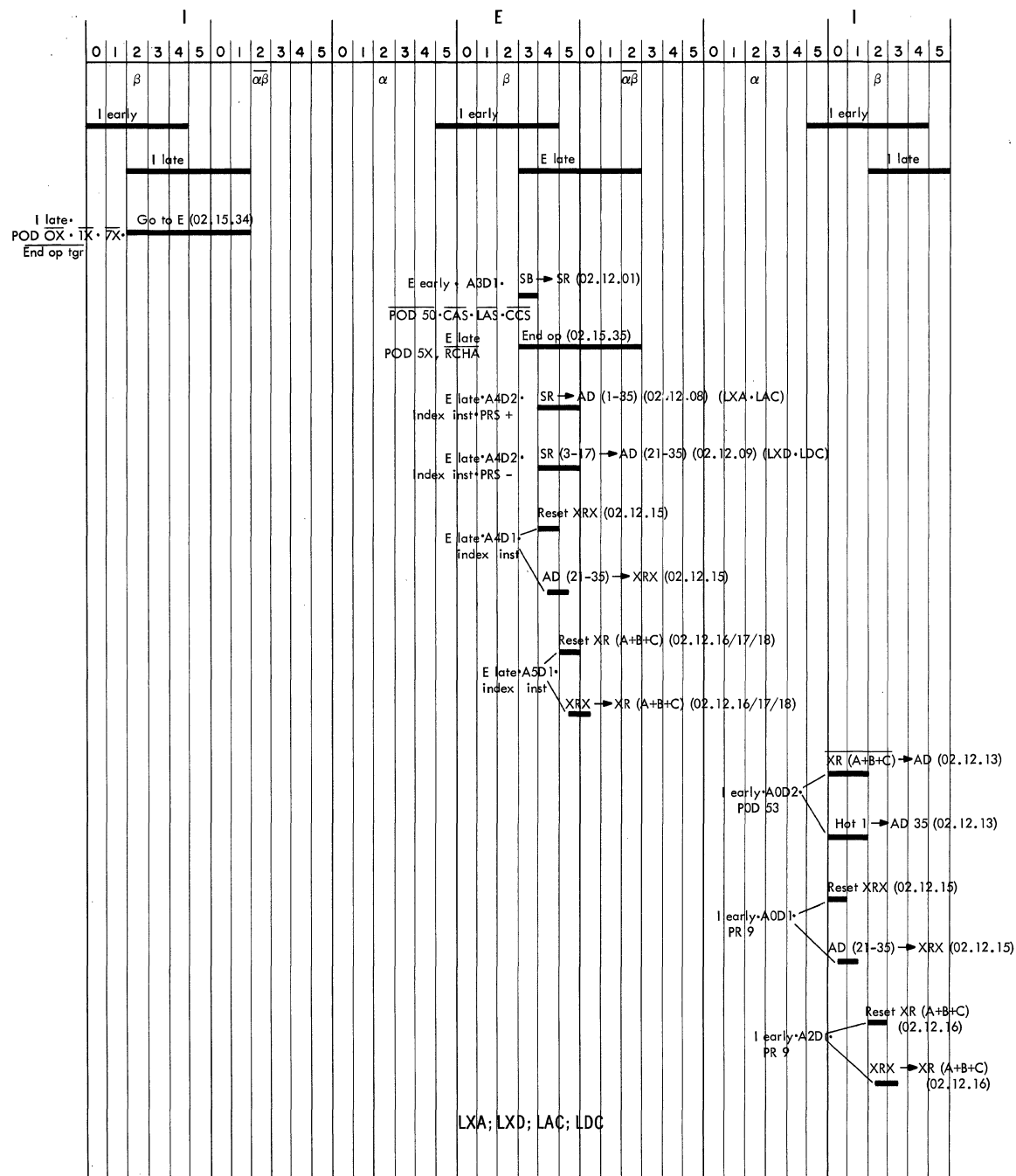


FIGURE 32. LXA, LXD, LAC, LDC



Location Switches	Inst	Tag	Address	Octal Equiv
00000	LXA	4*	00006	053400 400006
00001	LXA	4*	00007	053400 400007
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			000000 077777
00006	Pattern			000000 000000
00007				

* Change tag to test remaining index registers.

Load Index from Address (LXA)														
CONSOLE INDICATORS														
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (A 1-35)	ACCUMULATOR (Q 1-35)	MQ REGISTER (M 1-35)	TALLY COUNTER	INDEX REGISTER C	POSITION REGISTER	ACCU OVERFLOW
I	E	00001	+534	000	4	00006	053400400006					00000		
E	I	00001	+534	000	4	00001	000000077777					77777		
I	E	00002	+534	000	4	00007	053400400007					77777		
E	I	00002	+534	000	4	00002	000000000000					00000		
I	I	00003	+020	000	0	00000	002000000000					00000		

Location Switches	Inst	Tag	Address	Octal Equiv
00000	LXD	3*	00006	453400 300006
00001	LXD	3*	00007	453400 300007
00002	TRA		00000	002000 000000
00003				
00004				
00005				
00006				077777 000000
00007				000000 000000

* Change tag to test remaining index register.

Load Index from Decrement (LXD)														
CONSOLE INDICATORS														
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (A 1-35)	ACCUMULATOR (Q 1-35)	MQ REGISTER (M 1-35)	TALLY COUNTER	INDEX REGISTER A & B	POSITION REGISTER	ACCU OVERFLOW
I	E	00001	-534	000	3	00006	453400300006					00000		
E	I	00001	-534	000	3	00001	077777000000					77777		
I	E	00002	-534	000	3	00007	453400300007					77777		
E	I	00002	-534	000	3	00002	000000000000					00000		
I	I	00003	+020	000	0	00000	002000000000					00000		

Location Switches	Inst	Tag	Address	Octal Equiv
00000	LAC	6*	00006	053500 600006
00001	TRA	0	00000	002000 000000
00002				
00003				
00004				
00005				
00006	Pattern			000000 000001

* Change tag to test remaining index register.

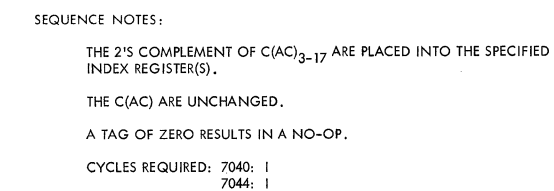
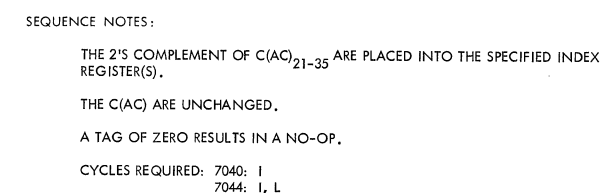
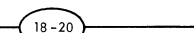
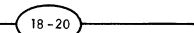
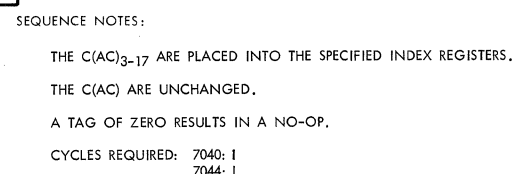
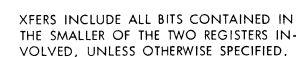
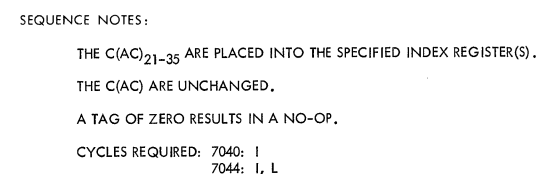
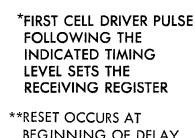
Load Complement of Address in Index (LAC)														
CONSOLE INDICATORS														
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (A 1-35)	ACCUMULATOR (Q 1-35)	MQ REGISTER (M 1-35)	TALLY COUNTER	INDEX REGISTER B & C	POSITION REGISTER	ACCU OVERFLOW
I	E	00001	+535	000	6	00006	053500600006					00000		
E	I	00001	+535	000	6	00001	000000000001					00001		
I	I	00002	+020	000	0	00000	002000000000					77777		
I	E	00001	+535	000	6	00006	053500600006					77777		

Location Switches	Inst	Tag	Address	Octal Equiv
00000	LDC	5*	00006	453500 000006
00001	TRA		00000	002000 000000
00002				
00003				
00004				
00005				
00006	Pattern			000001 000000

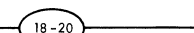
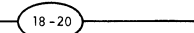
* Change tag to test remaining index register.

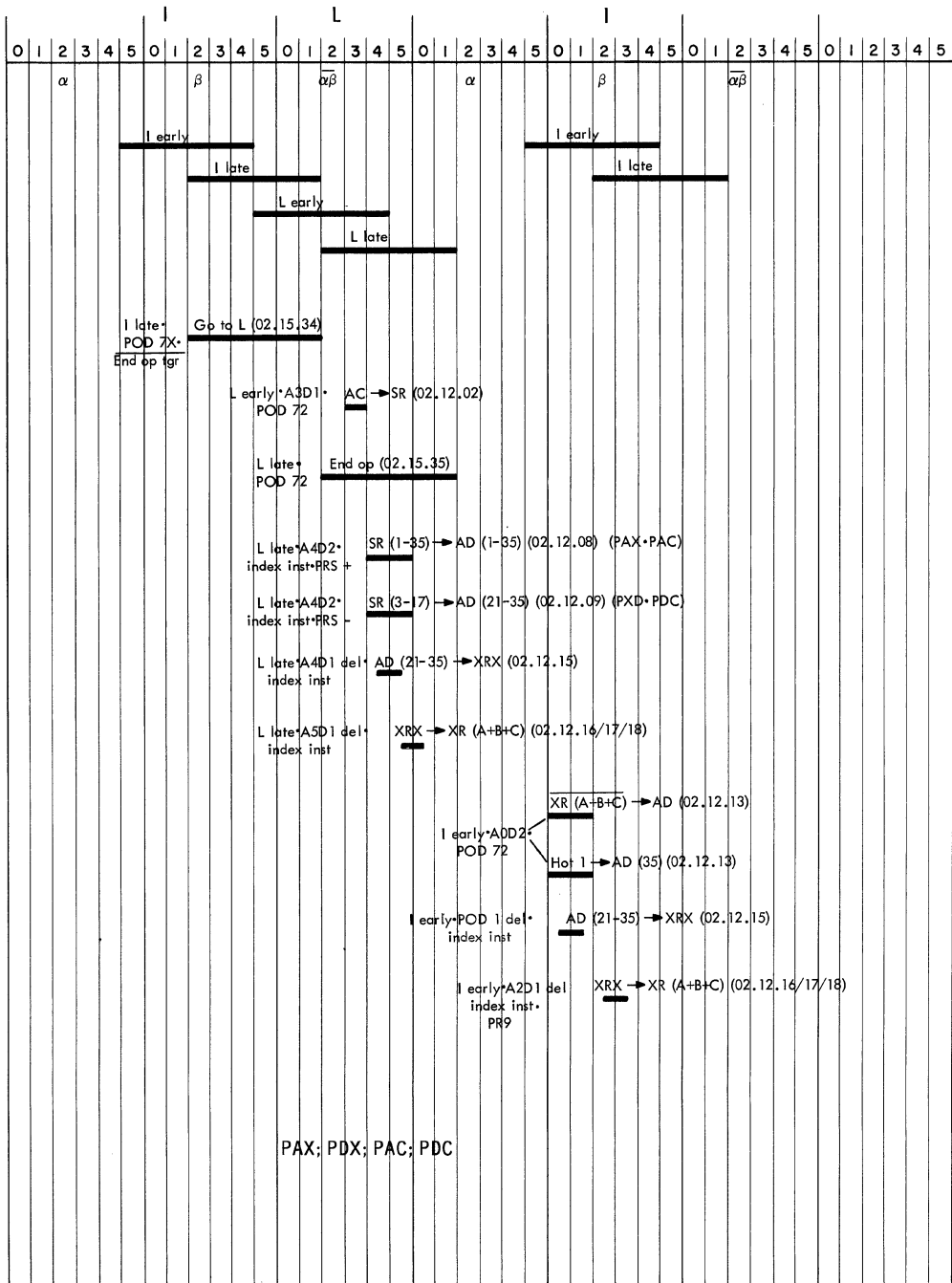
Load Complement of Decrement in Index (LDC)														
CONSOLE INDICATORS														
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (A 1-35)	ACCUMULATOR (Q 1-35)	MQ REGISTER (M 1-35)	TALLY COUNTER	INDEX REGISTER A & C	POSITION REGISTER	ACCU OVERFLOW
I	E	00001	-535	000	5	00006	453500500006					00000		
E	I	00001	-535	000	5	00001	000001000000					00001		
I	I	00002	+020	000	0	00000	002000000000					77777		
I	E	00001	-535	000	5	00006	453500500006					77777		

Place Complement of Decrement in Index (PDC -0737)
Places the 2's complement of accumulator bits 3-17 into the specified index register. The accumulator is unchanged.



* COMPLEMENT TRANSFER PLUS "HOT 1" TO ADDER
CAUSES 2'S COMPLEMENT.





Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA	1*	00006	050000 000006
00001	PAX		00000	073400 100000
00002	CLA		00007	050000 000007
00003	PAX		00000	073400 100000
00004	TRA	1*	00000	002000 000000
00005	TRA		00000	002000 000000
00006	Pattern	Pattern		000000 052525
00007	Pattern			000000 000000

* Change tag to test remaining index registers.

Place Address in Index (PAX)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER A	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK
I	E	00001	+500	000	0	00006	0500000000006	0000000000000	00			00000			
E	I	00001	+500	000	0	00001	000000052525	000000052525	00			00000			
I	L	00002	+734	000	1	00000	073400100000	000000052525	00			00000			
L	I	00002	+734	000	1	00002	000000052525	000000052525	00			52525			
I	E	00003	+500	000	0	00007	0500000000007	000000052525	00			52525			
E	I	00003	+500	000	0	00003	0000000000000	000000000000	00			52525			
I	L	00004	+734	000	1	00000	073400100000	000000000000	00			52525			
L	I	00004	+734	000	1	00004	0000000000000	000000000000	00			00000			
I	I	00005	+020	000	0	00000	0020000000000	000000000000	00			00000			

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA	7	00006	050000 000006
00001	PDX		00000	473400 700000
00002	CLA		00007	050000 000007
00003	PDX		00000	473400 700000
00004	TRA	7	00000	002000 000000
00005	TRA		00000	002000 000000
00006	Pattern	Pattern		025252 000000
00007	Pattern			700000 000000

Place Decrement in Index (PDX)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER A, B, & C	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK
I	E	00001	+500	000	0	00006	0500000000006	0000000000000	00			00000			
E	I	00001	+500	000	0	00001	0252520000000	0252520000000	00			00000			
I	L	00002	-734	000	7	00000	473400700000	0252520000000	00			00000			
L	I	00002	-734	000	7	00002	4252520000000	0252520000000	00			25252			
I	E	00003	+500	000	0	00007	0500000000007	0252520000000	00			25252			
E	I	00003	+500	000	0	00003	0000000000000	0000000000000	00			25252			
I	L	00004	-734	000	7	00000	473400700000	0000000000000	00			25252			
L	I	00004	-734	000	7	00000	4000000000000	0000000000000	00			00000			
I	I	00005	+020	000	0	00000	0020000000000	0000000000000	00			00000			

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA	2*	00006	050000 000006
00001	PAC		00000	073700 200000
00002	TRA		00000	002000 000000
00003	TRA		00000	002000 000000
00004	Pattern	Pattern		000000 025253
00005	Pattern			000000 025253
00006	Pattern	Pattern		000000 025253
00007	Pattern			000000 025253

* Change tag to test remaining index registers.

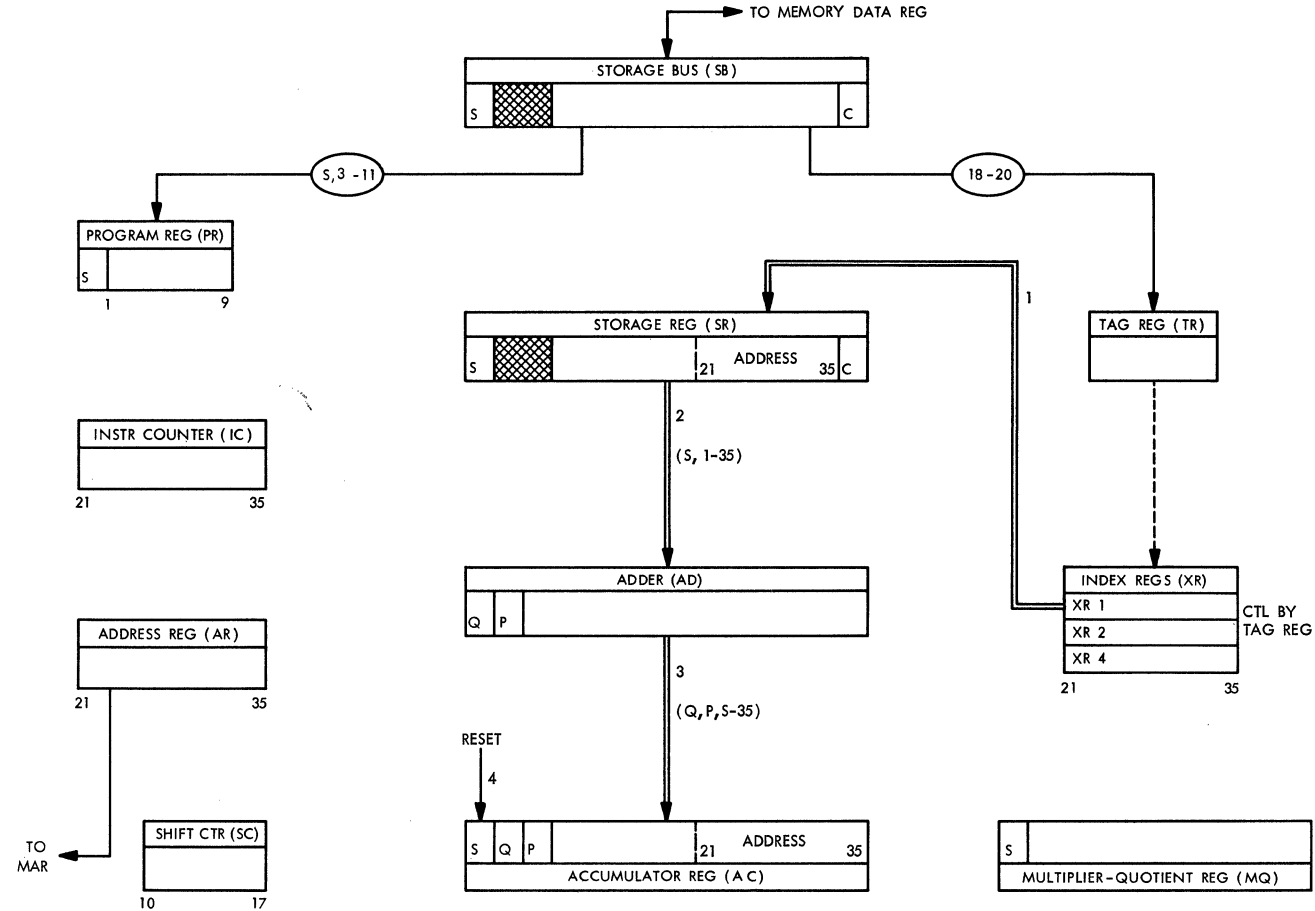
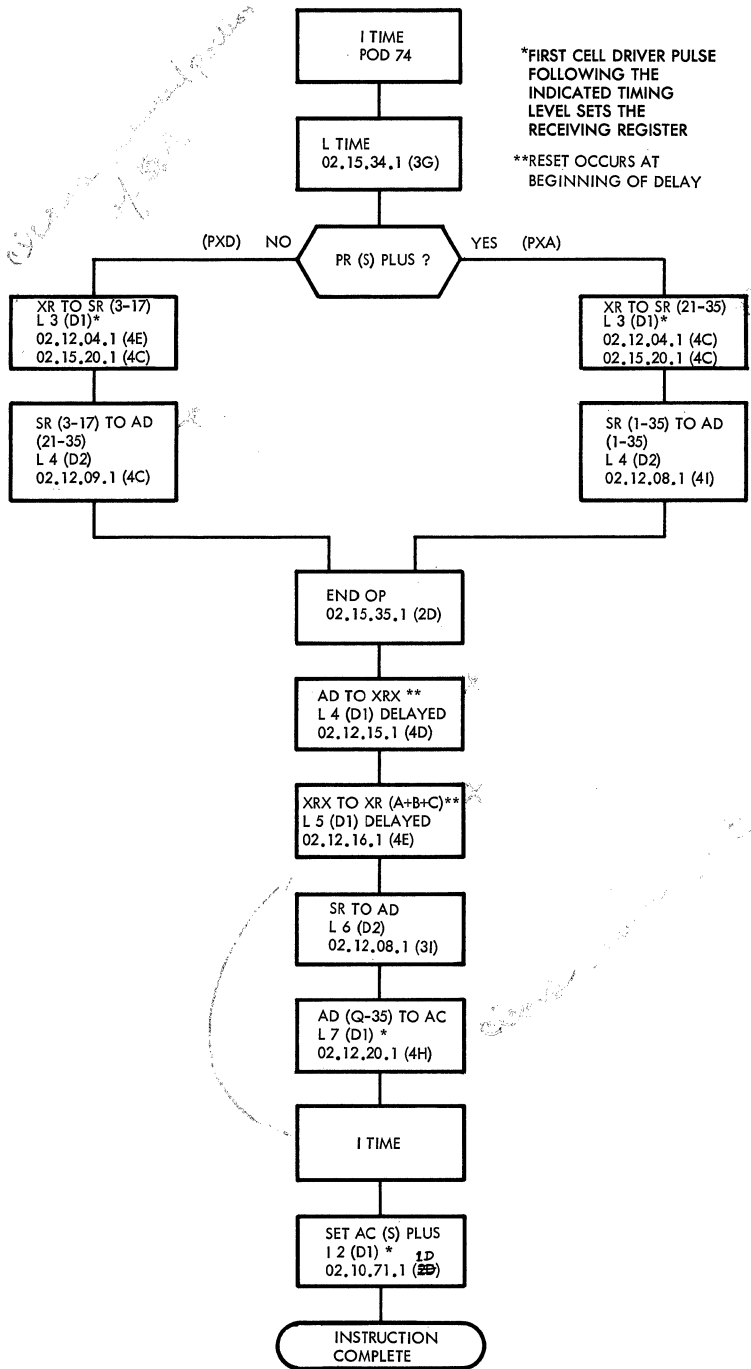
Place Complement of Address in Index (PAC)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER B	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK
I	E	00001	+500	000	0	00006	0500000000006	0000000000000	00			00000			
E	I	00001	+500	000	0	00001	000000025253	000000025253	00			00000			
I	L	00002	+737	000	2	00000	073700200000	000000025253	00			00000			
L	I	00002	+737	000	2	00002	000000025253	000000025253	00			25253			
I	I	00003	+020	000	0	00000	0020000000000	000000025253	00			52525			
I	E	00001	+500	000	0	00006	0500000000006	000000025253	00			52525			
E	I	00001	+500	000	0	00001	000000025253	000000025253	00			52525			
I	L	00002	+737	000	2	00000	073700200000	000000025253	00			52525			

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA	7	00006	050000 000006
00001	PDC		00000	473700 700000
00002	TRA		00000	002000 000000
00003	TRA		00000	002000 000000
00004	Pattern	Pattern		052526 000000
00005	Pattern			000000 000000
00006	Pattern	Pattern		052526 000000
00007	Pattern			000000 000000

Place Complement of Decrement in Index (PDC)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER A, B, & C	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK
I	E	00001	+500	000	0	00006	0500000000006	0000000000000	00			00000			
E	I	00001	+500	000	0	00001	0525260000000	0525260000000	00			00000			
I	L	00002	-737	000	7	00000	473700700000	0525260000000	00			00000			
L	I	00002	-737	000	7	00002	4525260000000	0525260000000	00			52526			
I	I	00003	+020	000	0	00000	0020000000000	0525260000000	00			25252			
I	E	00001	+500	000	0	00006	0500000000006	0525260000000	00			25252			
E	I	00001	+500	000	0	00001	0525260000000	0525260000000	00			25252			
I	L	00002	-737	000	7	00000	473700700000	0525260000000	00			25252			

Place Index in Address (PXA +0754)
Places the contents of the specified index register into accumulator 21-35.
The rest of the accumulator is cleared. The index register is unchanged.

Place Index in Decrement (PXD -0754)
Places the contents of the specified index register into accumulator 3-17.
The rest of the accumulator is cleared. The index register is unchanged.



LEGEND

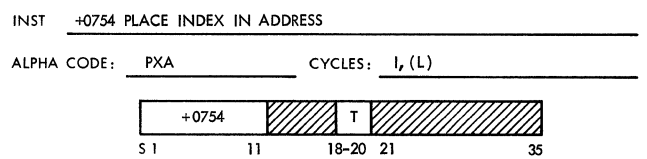
1 CYCLE

E CYCLE

L CYCLE

CONTROL

XFRS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.



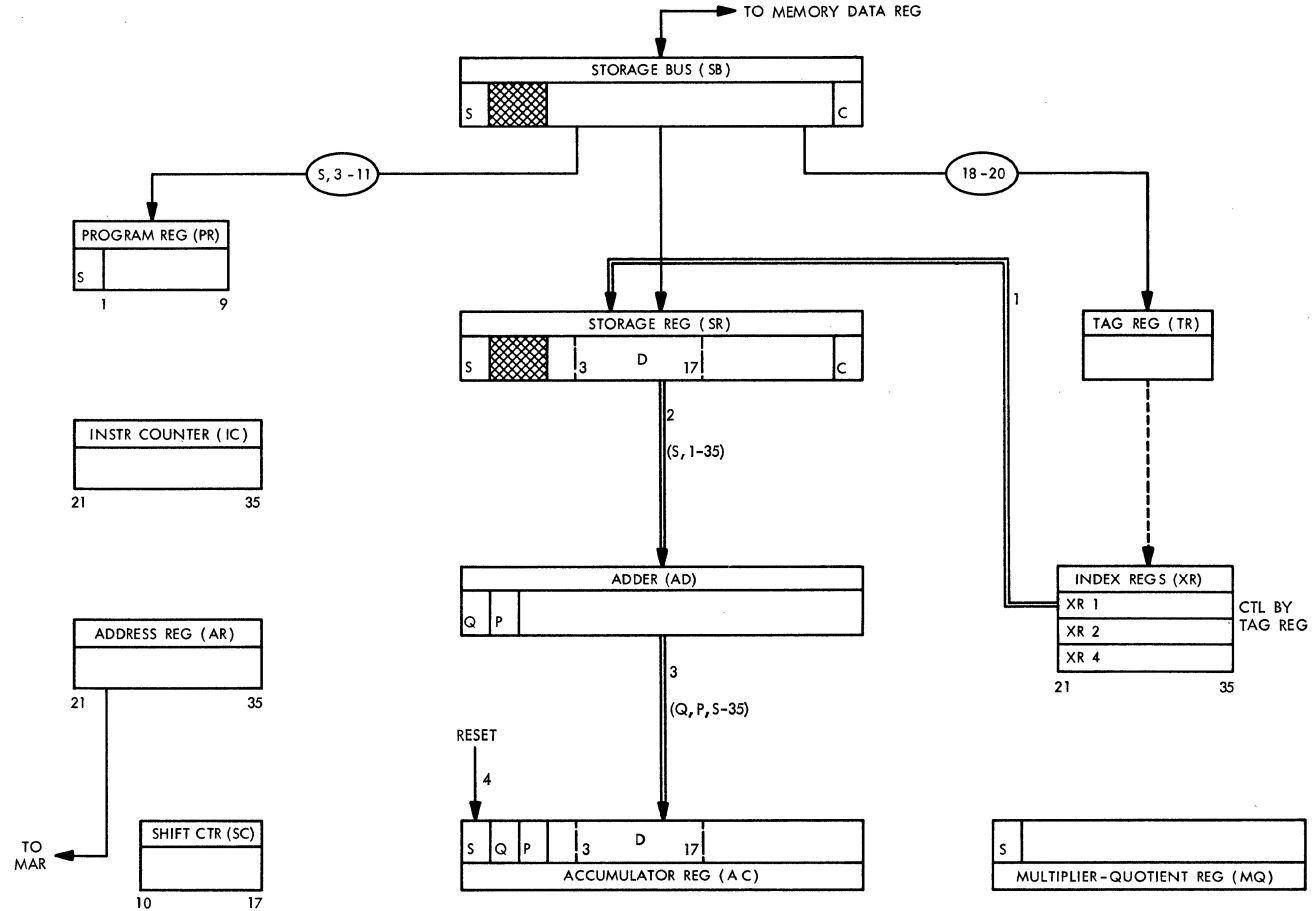
SEQUENCE NOTES:

THE ENTIRE ACCUMULATOR IS CLEARED AND THE CONTENTS OF THE SPECIFIED INDEX REGISTER(S) ARE PLACED IN THE C(AC)21-35.

WITH A TAG OF ZERO, THE C(AC) ARE CLEARED.

THE INDEX REGISTER(S) IS UNCHANGED.

CYCLES REQUIRED: 7040: 1
7044: I, L



LEGEND

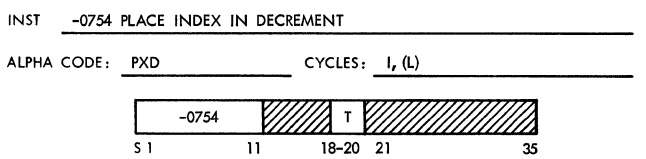
1 CYCLE

E CYCLE

L CYCLE

CONTROL

XFRS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.



SEQUENCE NOTES:

THE ENTIRE ACCUMULATOR IS CLEARED AND THE CONTENTS OF THE SPECIFIED INDEX REGISTER(S) ARE PLACED IN THE C(AC)3-17.

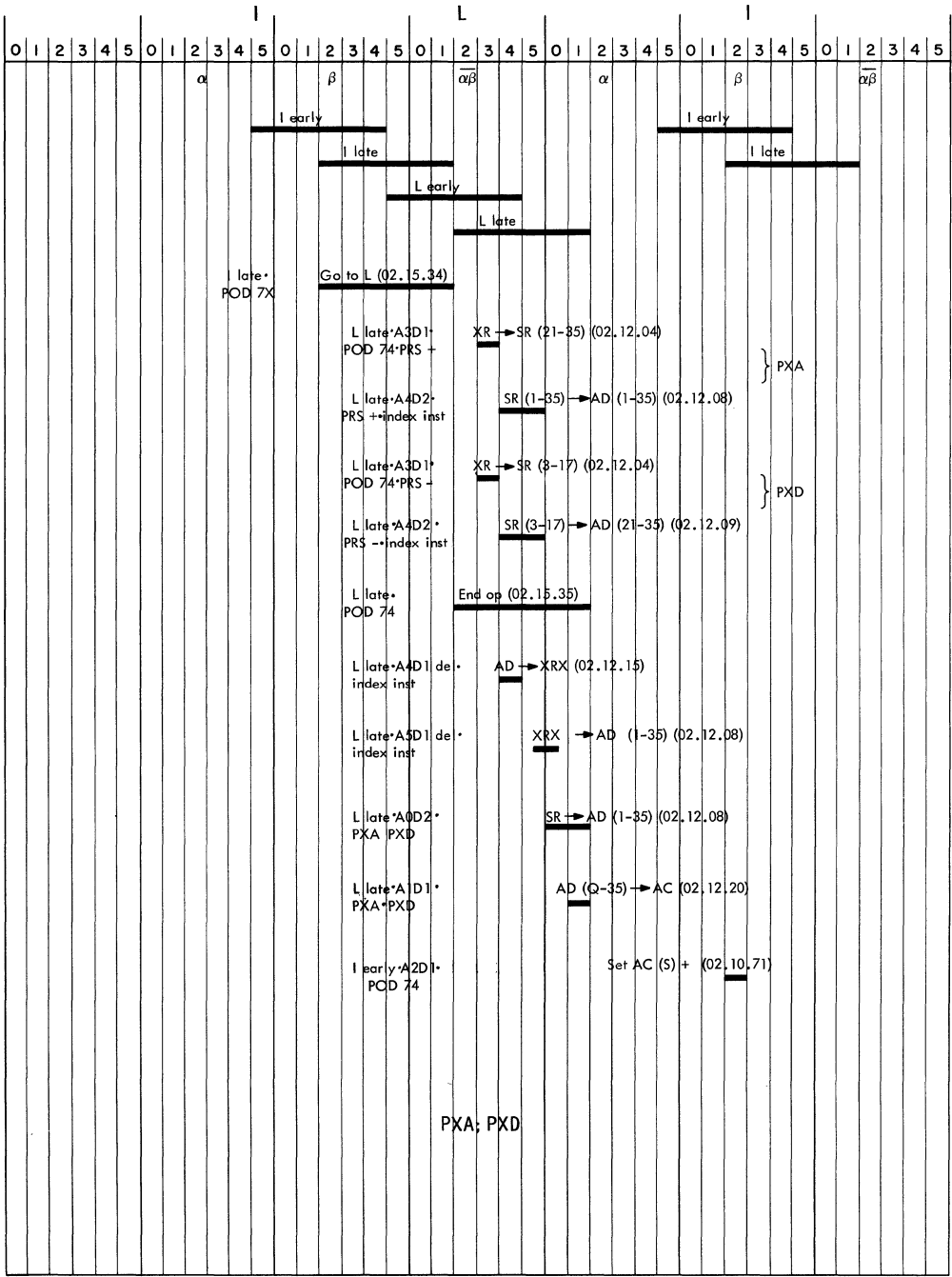
WITH A TAG OF ZERO, THE C(AC) ARE CLEARED.

THE INDEX REGISTER(S) IS UNCHANGED.

CYCLES REQUIRED: 7040: 1
7044: I, L

FIGURE 34. PXA, PXD

2 Providing no effect for compatibility with previous machines.



Location Switches	Inst	Tag	Address	Octal Equiv
00000	AXT	1*	77777	077400 177777
00001	CLA		00006	050000 000006
00002	PXA	1*	00000	075400 100000
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			777777 700000

*Change tag to test remaining index registers.

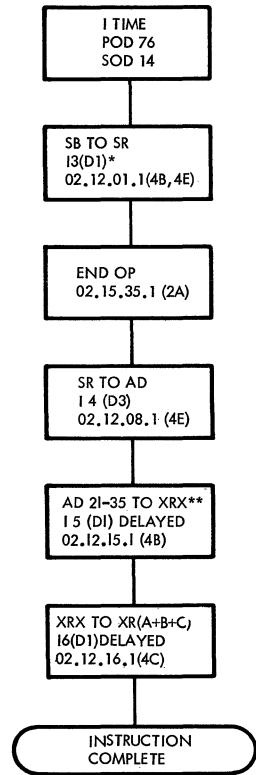
Place Index in Address (PXA)																					
CONSOLE INDICATORS																					
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER A	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	P CARRY	P OVERFLOW	FP 1	FP 2
I	I	00001	+774	377	1	00001	077400177777	000000000000	00			77777									
I	E	00002	+500	000	0	00006	050000000006	000000000000	00			77777									
E	I	00002	+500	000	0	00002	777777700000	777777700000	00			77777									
I	L	00003	+754	000	1	00000	075400100000	777777700000	00			77777									
L	I	00003	+754	000	1	00003	000000077777	000000077777	00			77777									
I	I	00004	+020	000	0	00000	002000000000	000000077777	00			77777									
I	I	00001	+774	377	1	00001	077400177777	000000077777	00			77777									
I	E	00001	+500	000	0	00006	050000000006	000000077777	00			77777									

Location Switches	Inst	Tag	Address	Octal Equiv
00000	AXT	1*	77777	077400 177777
00001	CLA		00006	050000 000006
00002	PXD	1*	00000	475400 100000
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			777777 777777

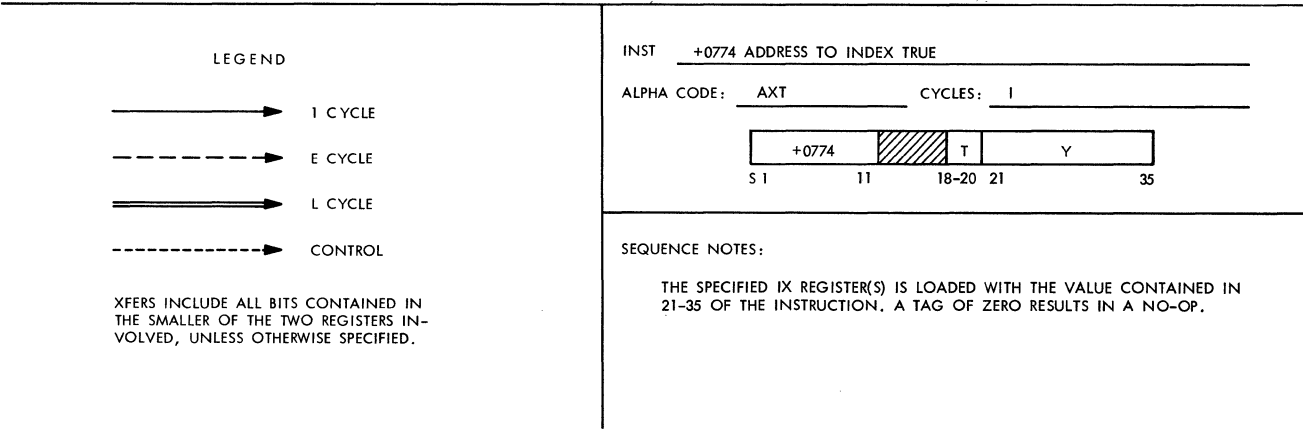
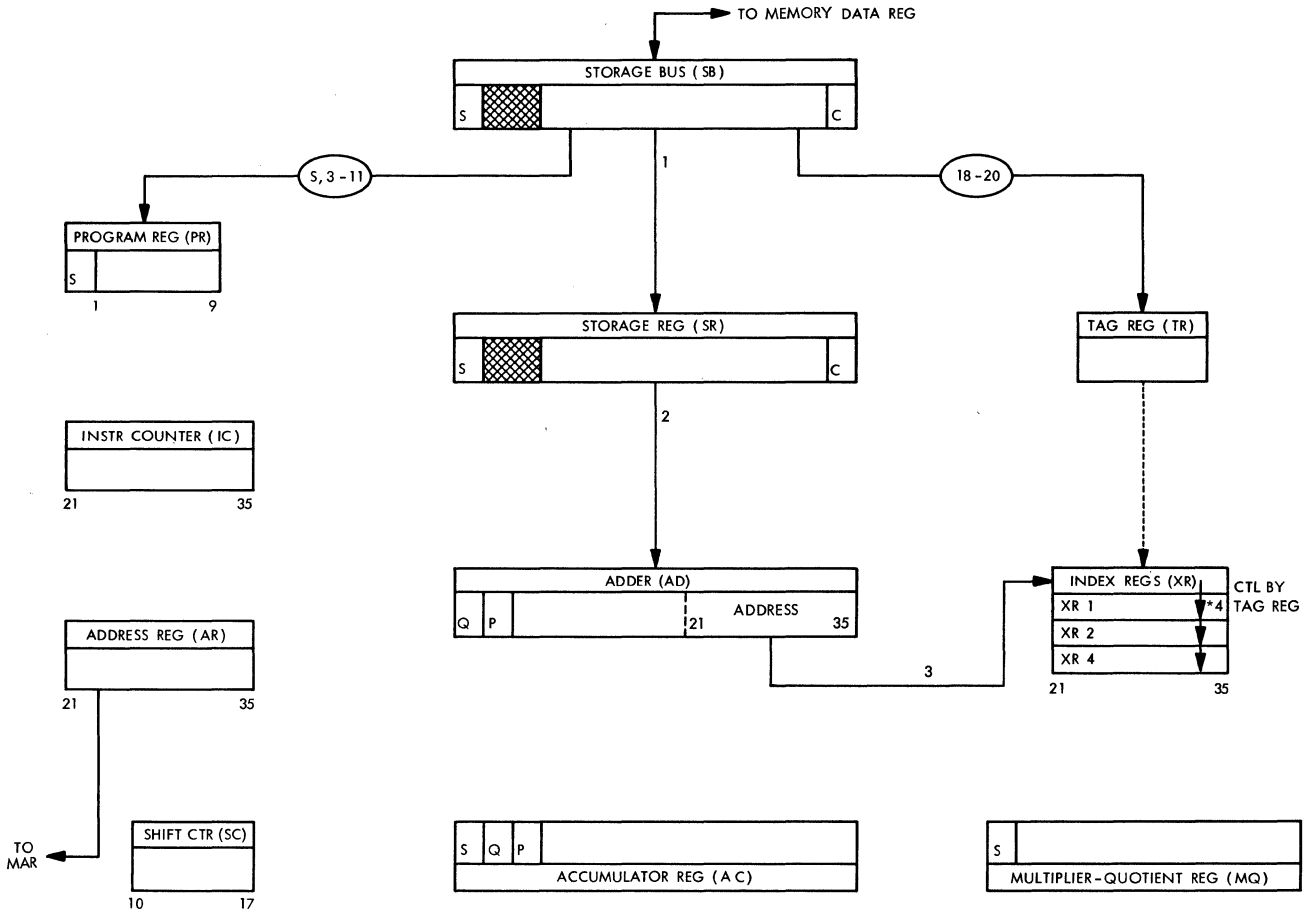
*Change tag to test remaining index registers.

Place Index in Decrement (PXD)																					CONSOLE INDICATORS									
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER 4	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2											
I	I	00001	+774	377	1	00001	077400177777	000000000000	00		77777																			
I	E	00002	+500	000	0	00006	050000000006	000000000000	00		77777																			
E	I	00002	+500	000	0	00002	777777777777	777777777777	00		77777																			
I	L	00003	-754	000	1	00000	475400100000	777777777777	00		77777																			
L	I	00003	-754	000	1	00003	077777000000	477777000000	00		77777																			
I	I	00004	+020	000	0	00000	002000000000	077777000000	00		77777																			
I	I	00001	+774	377	1	00001	077100177777	077777000000	00		77777																			
I	E	00002	+500	000	0	00006	050000000006	077777000000	00		77777																			

Address to Index True (AXT+0774)
Loads the specified index register from positions 21-35 of the instruction word.
The instruction is unchanged.

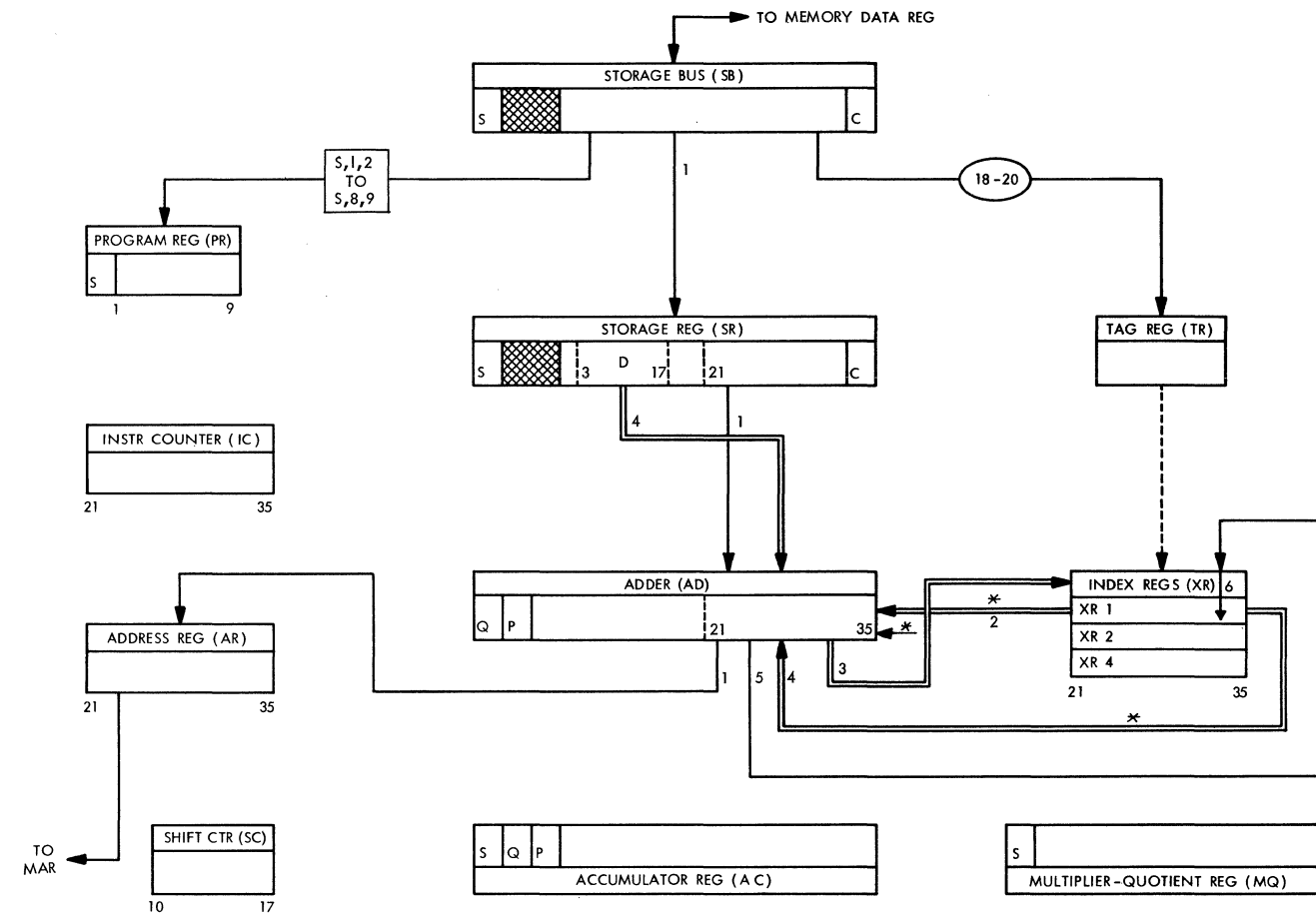
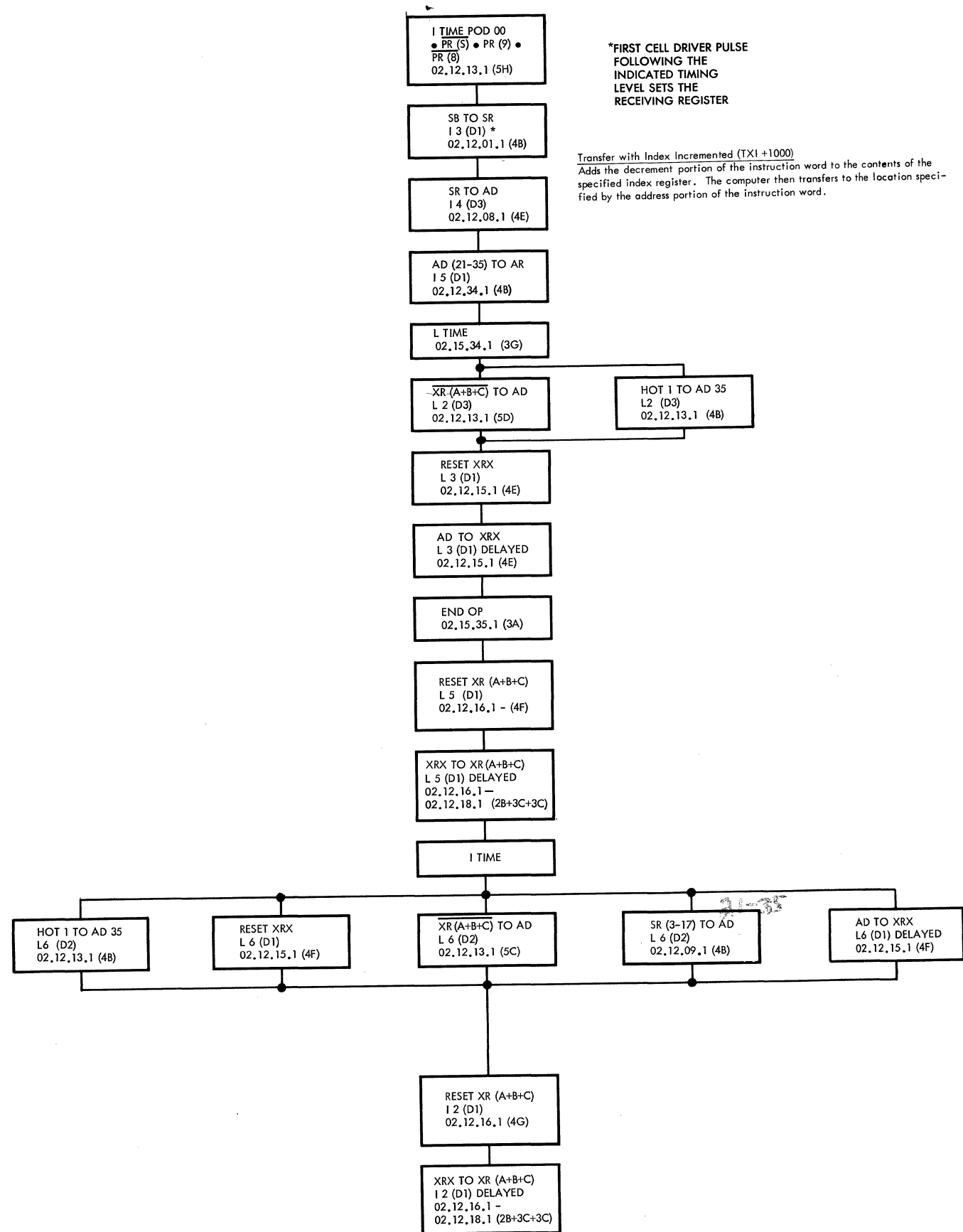


*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER
**RESET OCCURS AT START OF DELAY

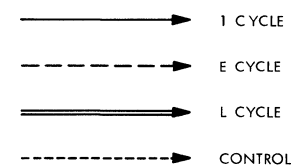




Address to Index True (AXT)



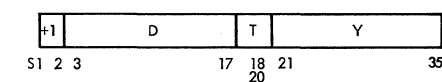
LEGEND



XFRS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +1 000 TRANSFER WITH INDEX INCREMENTED

ALPHA CODE: TXI CYCLES: I, (L)



SEQUENCE NOTES:

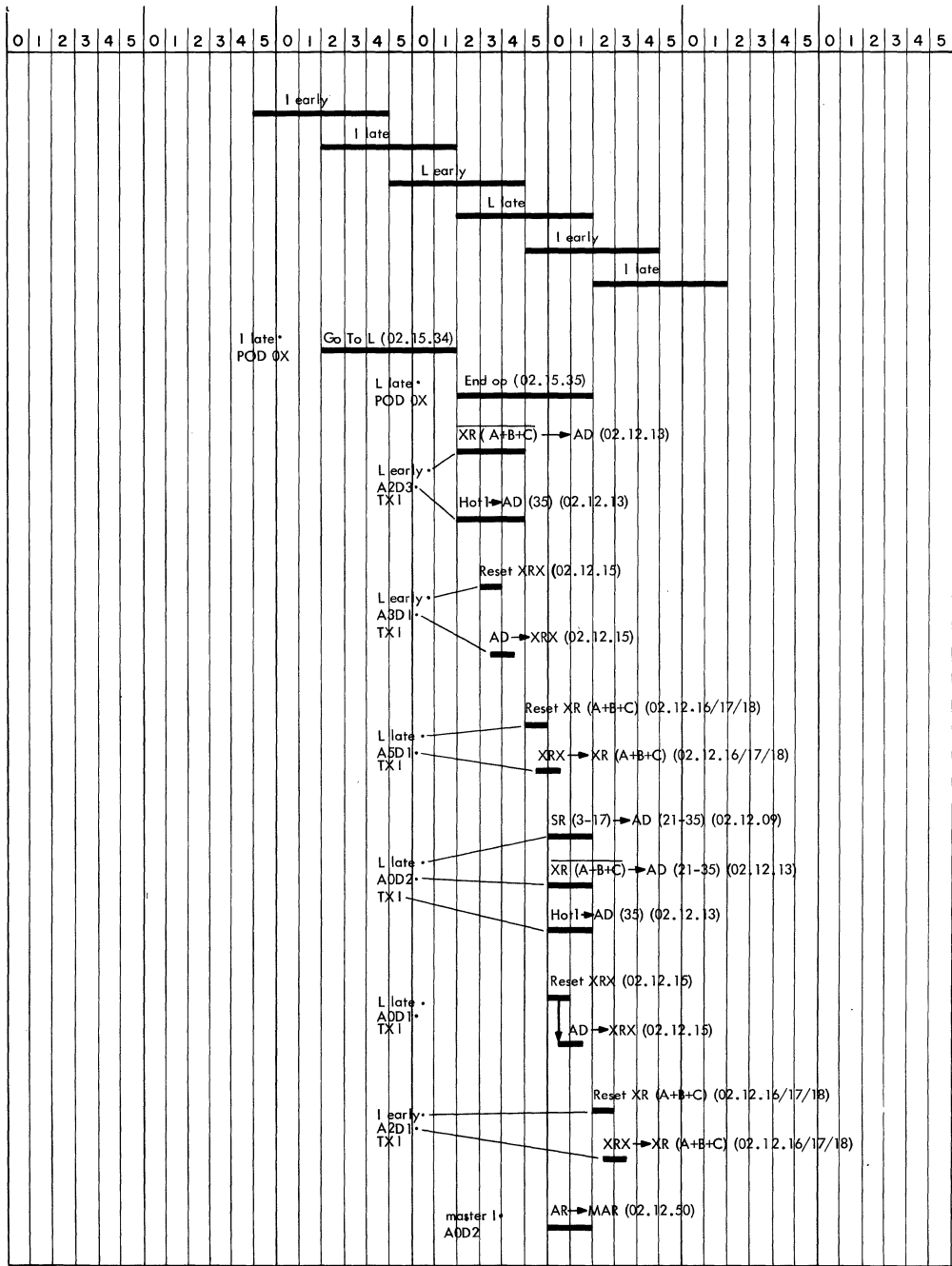
THE DECREMENT PORTION OF THE INSTRUCTION WORD IS ADDED TO THE CONTENTS OF THE SPECIFIED XR(S).

THE COMPUTER TAKES ITS NEXT INSTRUCTION FROM LOCATION Y.

CYCLES REQUIRED: 7040: I
7044: I L

* COMPLEMENT TRANSFER PLUS "HOT I" TO ADDER CAUSES 2'S COMPLEMENT.

FIGURE 36. TXI



Location Switches	Inst	Tag	Address	Octal Equiv
00000	TXI (D=7)	7	00002	100007 700002
00001	HPR			042000 000000
00002	TXI (D=70)	7		100070 700004
00003	HPR			042000 000000
00004	TXI (D=700)	7	00005	100700 700005
00005	AXT	7	00000	077400 700000
00006	TRA		00000	002000 000000

Transfer with Index Decrement (TXI)																
CONSOLE INDICATORS																
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S 1-35)	ACCUMULATOR (Q P)	MQ REGISTER (S 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY
I	L	00001	+001	000	1	00002	100007700002					00000				
L	I	00001	+001	000	1	00002	100007700002					00000				
I	L	00003	+001	000	1	00004	100070700004					00007				
L	I	00003	+001	000	1	00004	100070700004					77771				
I	L	00005	+001	000	1	00005	100700700005					00077				
L	I	00005	+001	000	1	00005	100700700005					77701				
I	I	00006	+774	000	1	00006	077400700000					00000				
I	I	00007	+020	000	0	00000	002000000000					00000				

Transfer on Index (TIX +2000)

If the contents of the specified index register are greater than the decrement field of the instruction word, the decrement is subtracted from the index register and the computer takes the next instruction from the location specified by the address field of the instruction word. If the contents of the specified index register are equal to or less than the decrement, the index register is not decremented and the computer takes the next sequential instruction.

Transfer on No Index (TNX -2000)

If the contents of the specified index register are greater than the decrement field of the instruction word, the decrement is subtracted from the index register and the computer takes the next sequential instruction. If the contents of the specified index register are equal to or less than the decrement, the index register is not decremented and the computer takes the next instruction from the location specified by the address field of the instruction word.

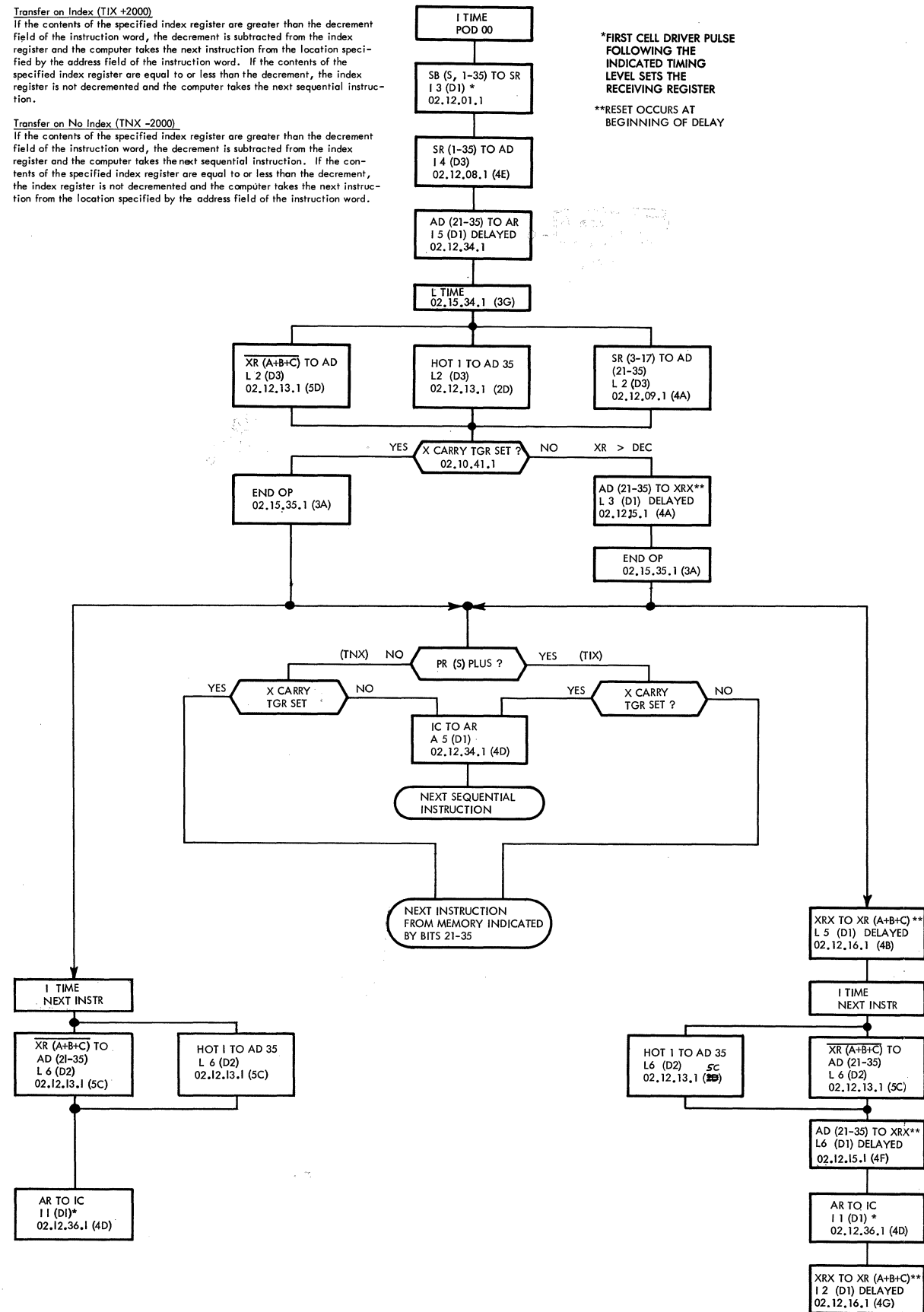
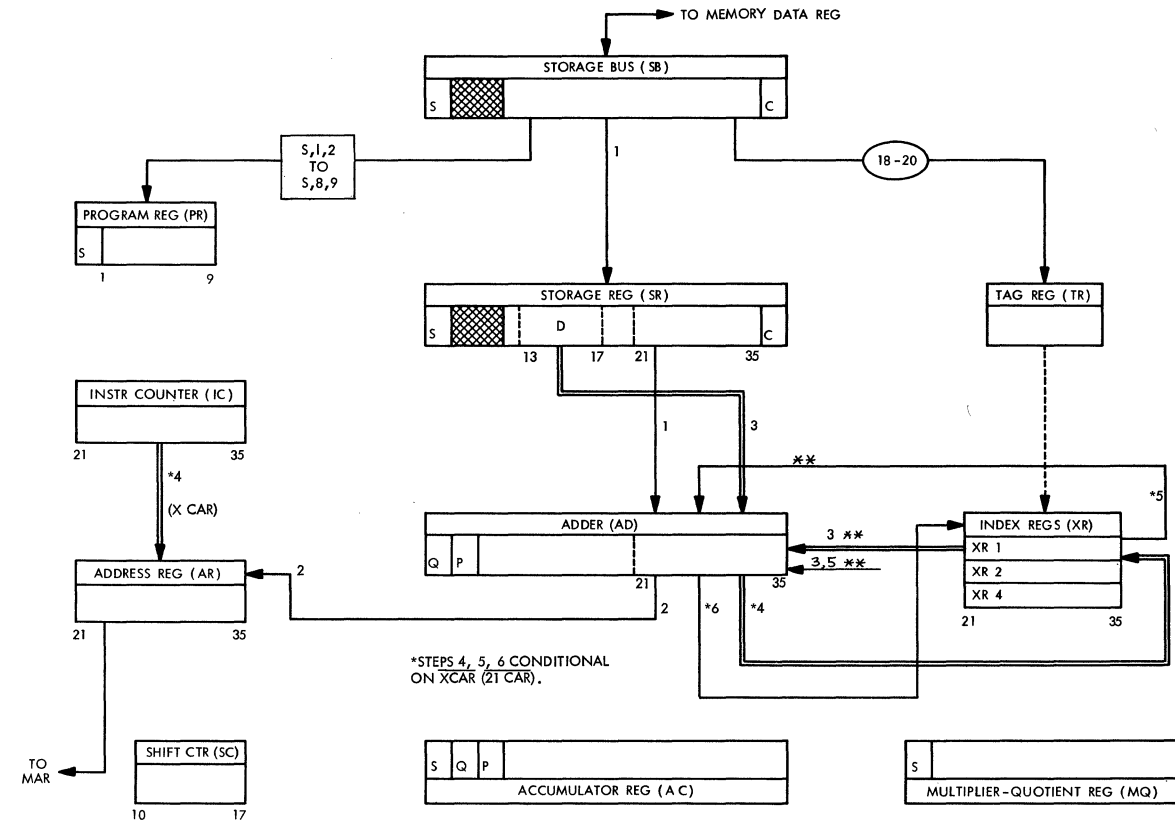


FIGURE 37. TIX, TNX



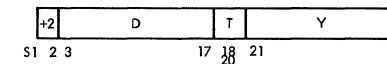
LEGEND

- Solid line: 1 CYCLE
- Dashed line: E CYCLE
- Thick solid line: L CYCLE
- Thin dashed line: CONTROL

XFRS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +2 000 TRANSFER ON INDEX

ALPHA CODE: TIX CYCLES: 1, L



SEQUENCE NOTES:

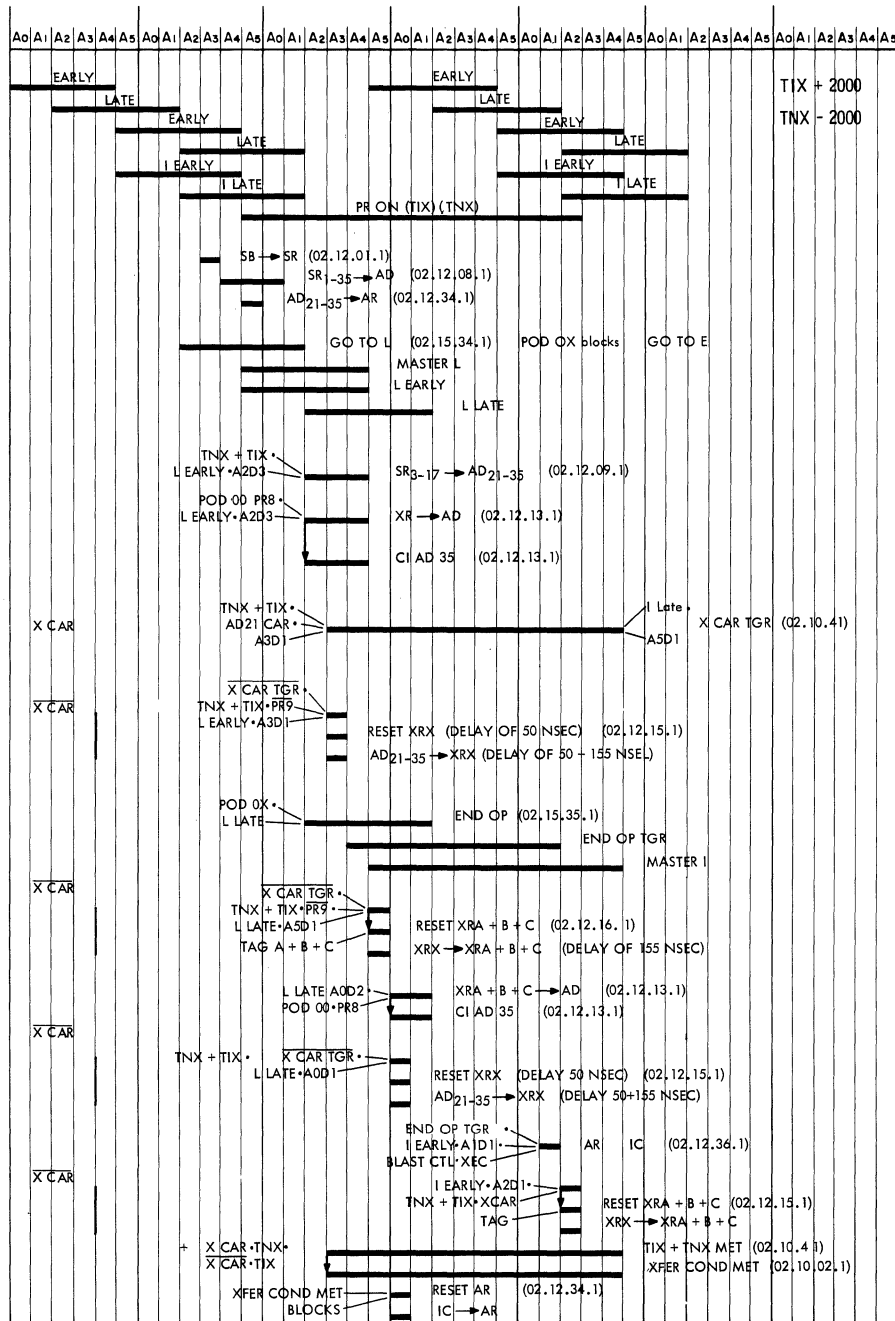
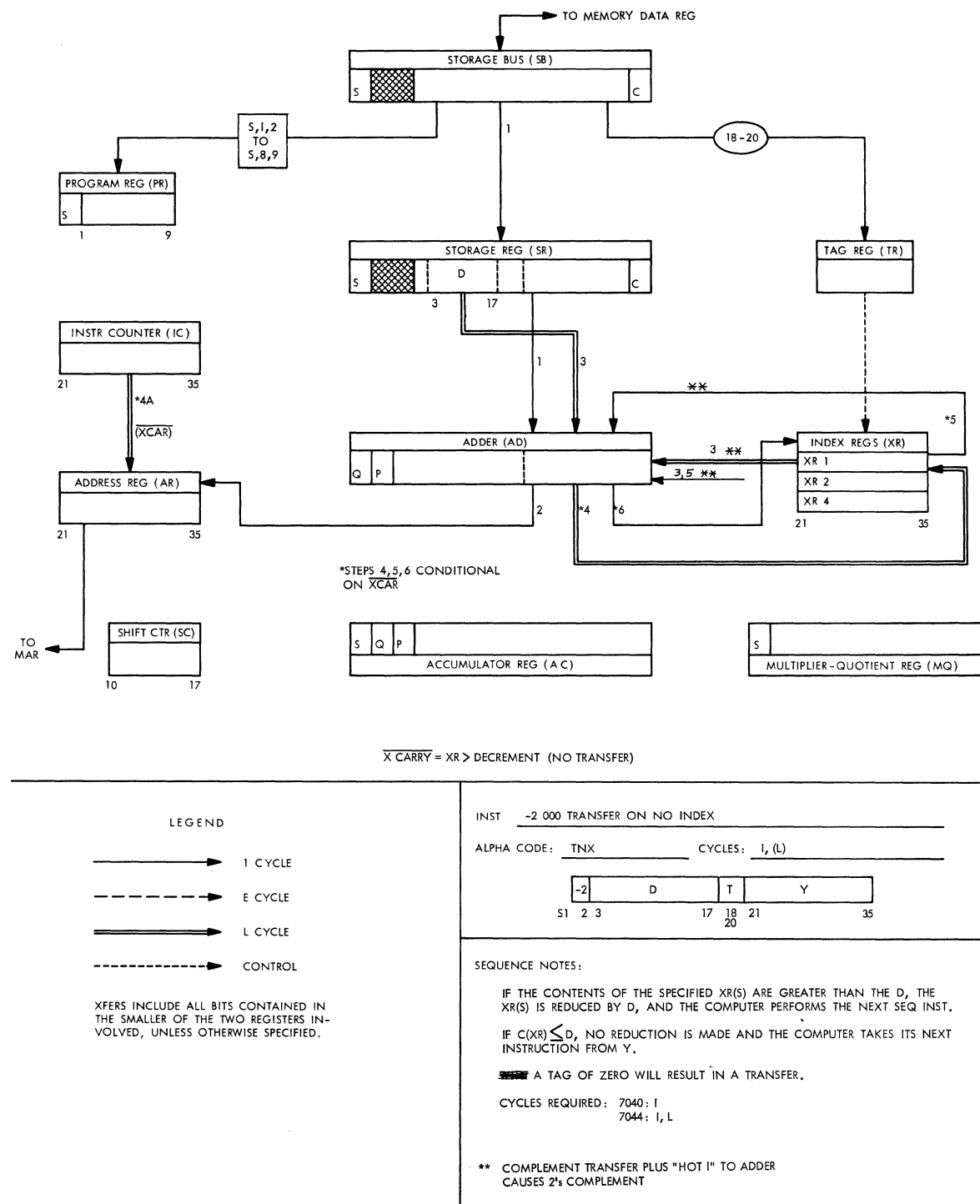
IF THE CONTENTS OF THE SPECIFIED XR(S) ARE GREATER THAN THE D, THE INDEX REGISTER(S) IS REDUCED BY D AND THE COMPUTER TAKES ITS NEXT INSTRUCTION FROM Y.

IF $C(XR) \leq D$, NO REDUCTION IS MADE AND THE COMPUTER TAKES THE NEXT SEQUENTIAL INST. WITH A TAG OF ZERO, NO TRANSFER

CYCLES REQUIRED: 7040: 1, 7040: 1, L

IF TAG = 0, TRANSFER 2's COMPLEMENT OF ZERO TO AD FROM XR. X CARRY WILL ALWAYS OCCUR

** COMPLEMENT TRANSFER PLUS "HOT 1" TO ADDER CAUSES 2's COMPLEMENT



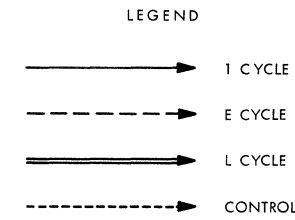
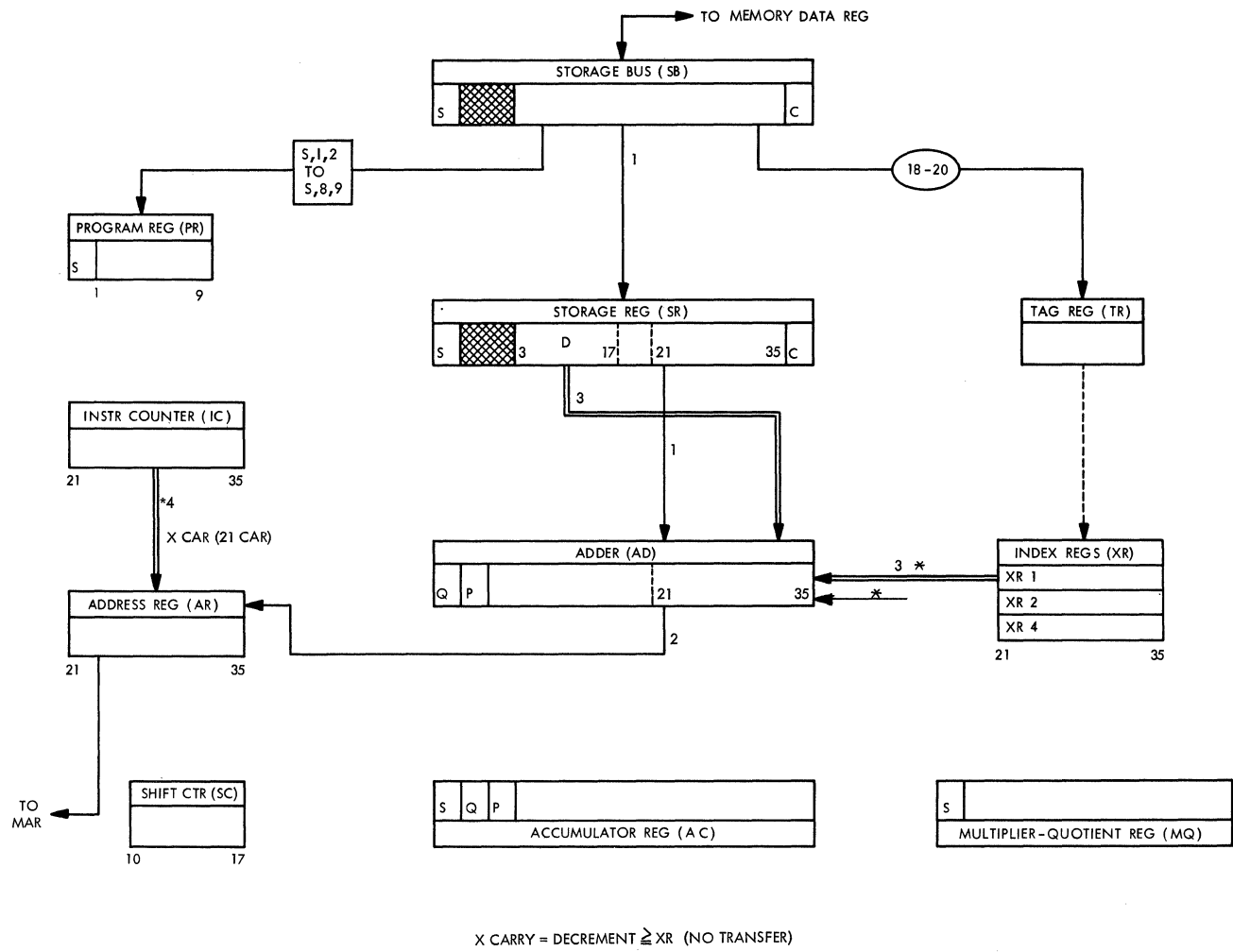
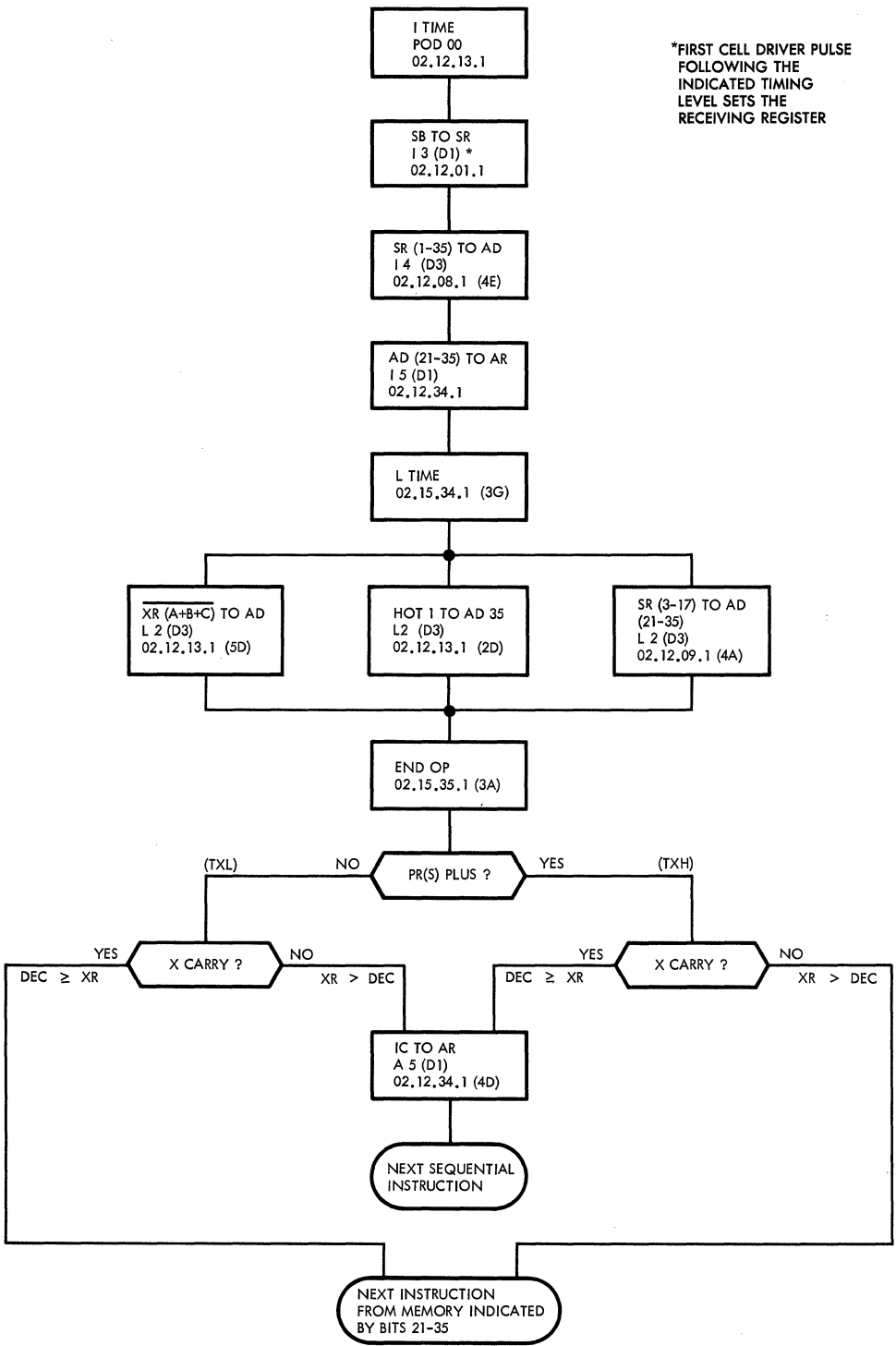
Location Switches	Inst	Tag	Address	Octal Equiv
00000	AXT	7	00003	077400 000003
00001	TIX (D=1)	7	00001	200001 700001
00002	TRA		00000	002000 000000
00003				
00004				
00005				
00006				

Transfer on Index (TIX)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	INDEX REGISTER (I, 1-35)	MG REGISTER (M, 1-35)	TALLY COUNTER	INDEX REGISTER (A, B, C)	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	FP2
I	I	00001	+774	003	7	00001	077400700003				00003			0	
I	L	00002	+002	000	7	00001	200001700001				00003			0	
L	I	00002	+002	000	7	00001	200001700001				77776			0	
I	I	00002	+002	000	7	00001	200001700001				00002			0	
L	I	00002	+002	000	7	00001	200001700001				77777			0	
I	L	00002	+002	000	7	00001	200001700001				00001			0	
L	I	00002	+002	000	7	00002	200001700001				00001			1	
I	I	00003	+020	000	0	00000	002000000000				00001			0	

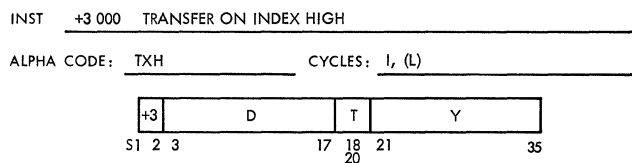
Location Switches	Inst	Tag	Address	Octal Equiv
00000	AXT	7	00003	077400 700003
00001	TIX (D=1)	7	00000	600001 700000
00002	TRA	1	00001	002000 000001
00003				
00004				
00005				
00006				

Transfer on No Index (TNX)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	INDEX REGISTER (I, 1-35)	MG REGISTER (M, 1-35)	TALLY COUNTER	INDEX REGISTER (A, B, C)	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	FP2
I	I	00001	+774	003	7	00001	077400700003				00003			0	
I	L	00002	-002	000	7	00000	600001700000				00003			0	
L	I	00002	-002	000	7	00002	600001700000				77776			0	
I	I	00003	+020	000	0	00001	002000000001				00002			0	
I	L	00002	-002	000	7	00000	600001700000				00002			0	
L	I	00002	-002	000	7	00002	600001700000				77777			0	
I	I	00003	+020	000	0	00001	002000000001				00001			0	
I	L	00002	-002	000	7	00000	600001700000				00001			0	
L	I	00002	-002	000	7	00000	600001700000				00001			1	

Transfer on Index Low or Equal (TXL -3000)
If the contents of the specified index register are less than or equal to the decrement field of the instruction word, the computer takes its next instruction from the location specified by the address field of the instruction. If the index register is greater than the decrement, the computer takes the next sequential instruction.



XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.



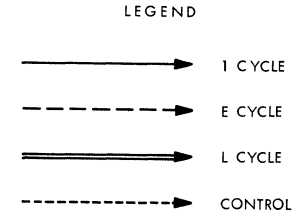
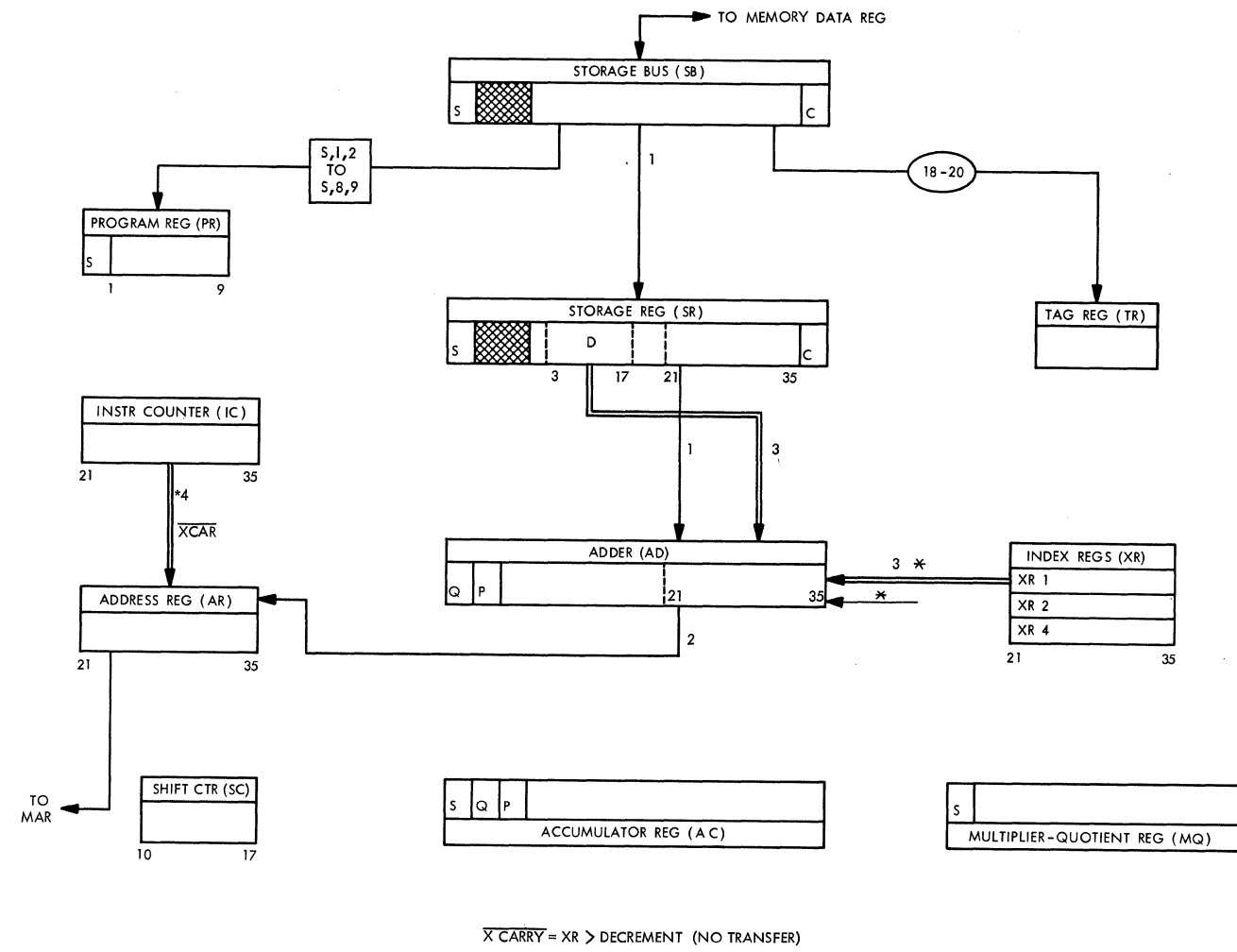
SEQUENCE NOTES:

IF THE CONTENTS OF THE SPECIFIED XR(S) ARE GREATER THAN D, THE COMPUTER TAKES ITS NEXT INSTRUCTION FROM LOCATION Y.

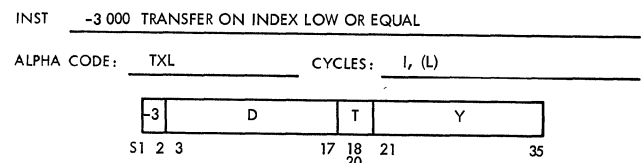
IF C(XR) IS $\leq$ D, THE COMPUTER TAKES ITS NEXT SEQUENTIAL INSTRUCTION. WITH A TAG OF ZERO, NO TRANSFER OCCURS.

CYCLES REQUIRED: 7040: I
7044: I, L

* COMPLEMENT TRANSFER PLUS "HOT I" TO ADDER CAUSES 2's COMPLEMENT



XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.



SEQUENCE NOTES:

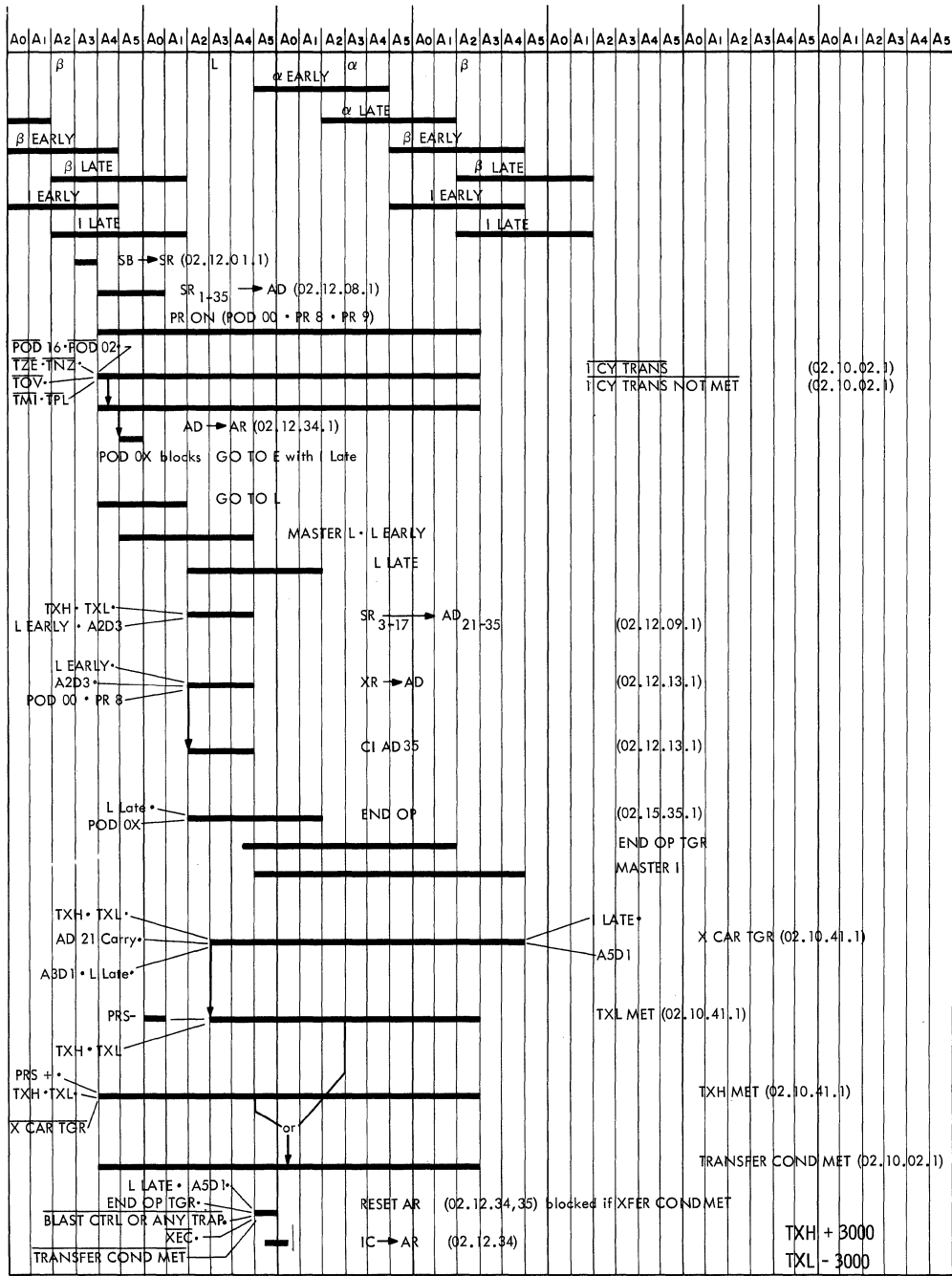
IF THE CONTENTS OF THE SPECIFIED XR(S) ARE LESS THAN OR EQUAL TO D, THE COMPUTER TAKES ITS NEXT INSTRUCTION FROM LOCATION Y.

IF C(XR) $>$ D, THE COMPUTER TAKES ITS NEXT SEQUENTIAL INSTRUCTION. WITH A TAG OF ZERO, A TRANSFER OCCURS.

CYCLES REQUIRED: 7040: I
7044: I, L

* COMPLEMENT TRANSFER PLUS "HOT I" TO ADDER CAUSES 2's COMPLEMENT

FIGURE 38. TXH, TXL



Location Switches	Inst	Tag	Address	Octal Equiv
00000	AXT	7	00077	077400 700077
00001	TXH	7	00004	300076 700004
00002	HPR			042000 000000
00003	HPR			042000 000000
00004	AXT	7	00000	077400 700000
00005	TXH	7	00004	300000 700002
00006	TRA		00000	002000 000000

Transfer on Index High (TXH)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTERS A, B, & C	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK
I	I	00001	+774	077	7	00001	077400700077					00077			0
I	L	00002	+003	000	7	00004	300076700004					00077			0
L	I	00002	+003	000	7	00004	300076700004					00077			0
I	I	00005	+774	000	7	00005	077400700000					00000			0
I	L	00006	+003	000	7	00002	300000700002					00000			0
L	I	00006	+003	000	7	00006	300000700002					00000			1
I	I	00007	+020	000	0	00000	002000000000					00000			0

Location Switches	Inst	Tag	Address	Octal Equiv
00000	AXT	7	00077	077400 700077
00001	TXL	7	00005	700076 700005
00002	TXL	7	00006	700076 700006
00003	AXT	7	00000	077400 700000
00004	TXL	7	00006	700000 700006
00005	HPR		00000	042000 000000
00006	TRA		00000	002000 000000

Transfer on Index Low or Equal (TXL)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTERS A, B, & C	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK
I	I	00001	+774	077	7	00001	077400700077					00077			0
I	L	00002	-003	000	7	00005	700076700005					00077			0
L	I	00002	-003	000	7	00002	700076700005					00077			0
I	L	00003	-003	000	7	00006	700076700006					00077			0
L	I	00003	-003	000	7	00003	700076700006					00077			0
I	I	00004	+774	000	7	00004	077400700000					00000			0
I	L	00005	-003	000	7	00006	700000700006					00000			0
L	I	00005	-003	000	7	00006	700000700006					00000			1
I	I	00007	+020	000	0	00000	002000000000					00000			0

Transfer and Set Index (TSX +0074)
Places the 2's complement of the location of the instruction in the specified index register. The computer takes the next instruction from the location specified by the address field of the instruction word.

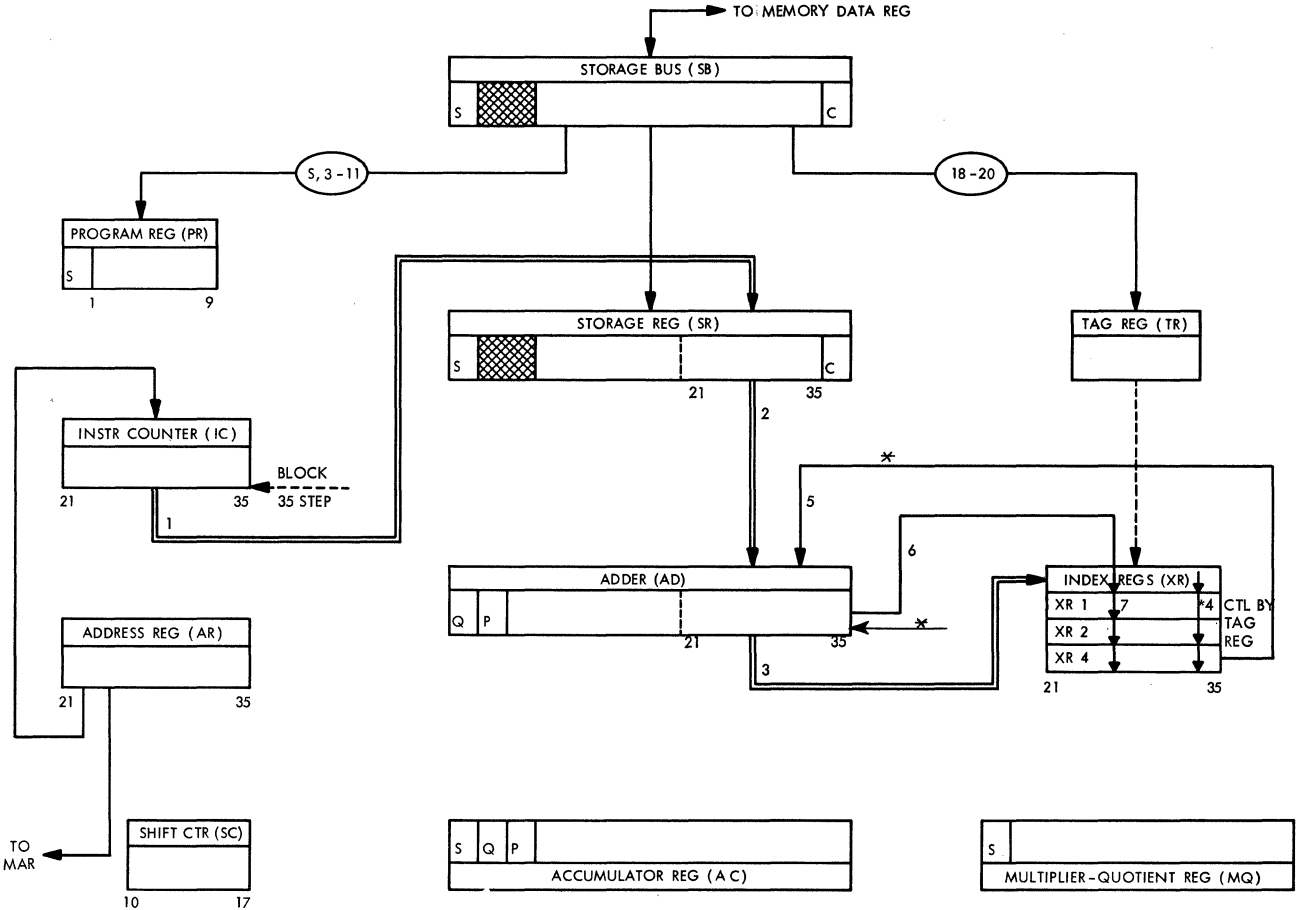
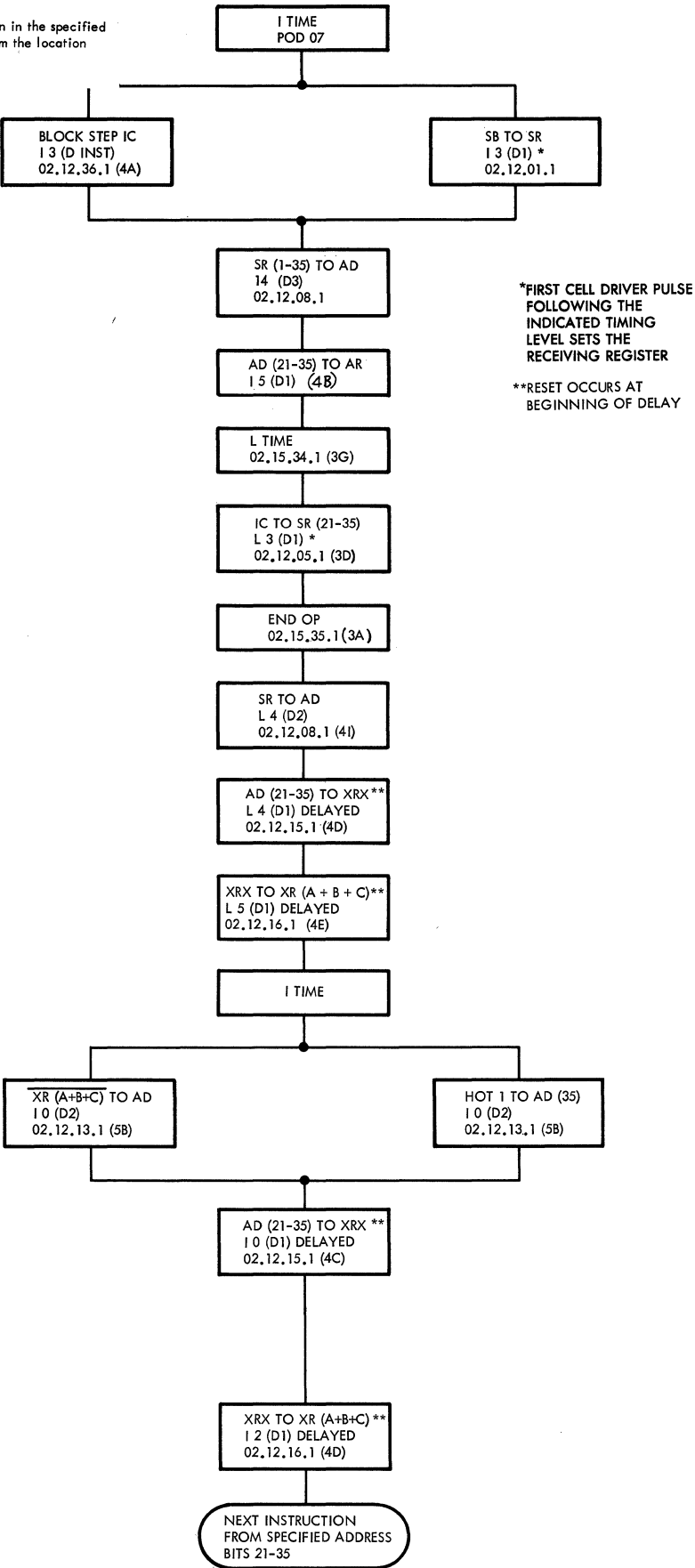
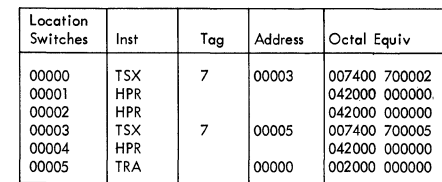


FIGURE 39. TSX

95

Transfer on Zero (TZE +0100)
If the accumulator is zero ($Q, P, 1-35$), the computer takes its next instruction from the location specified by the address field of the instruction word. If the accumulator is not zero, the computer takes the next sequential instruction.

Transfer on No Zero (TNZ -0100)
If the accumulator is not zero ($Q, P, 1-35$), the computer takes its next instruction from the location specified by the address field of the instruction word. If the accumulator is zero, the computer takes the next sequential instructions.

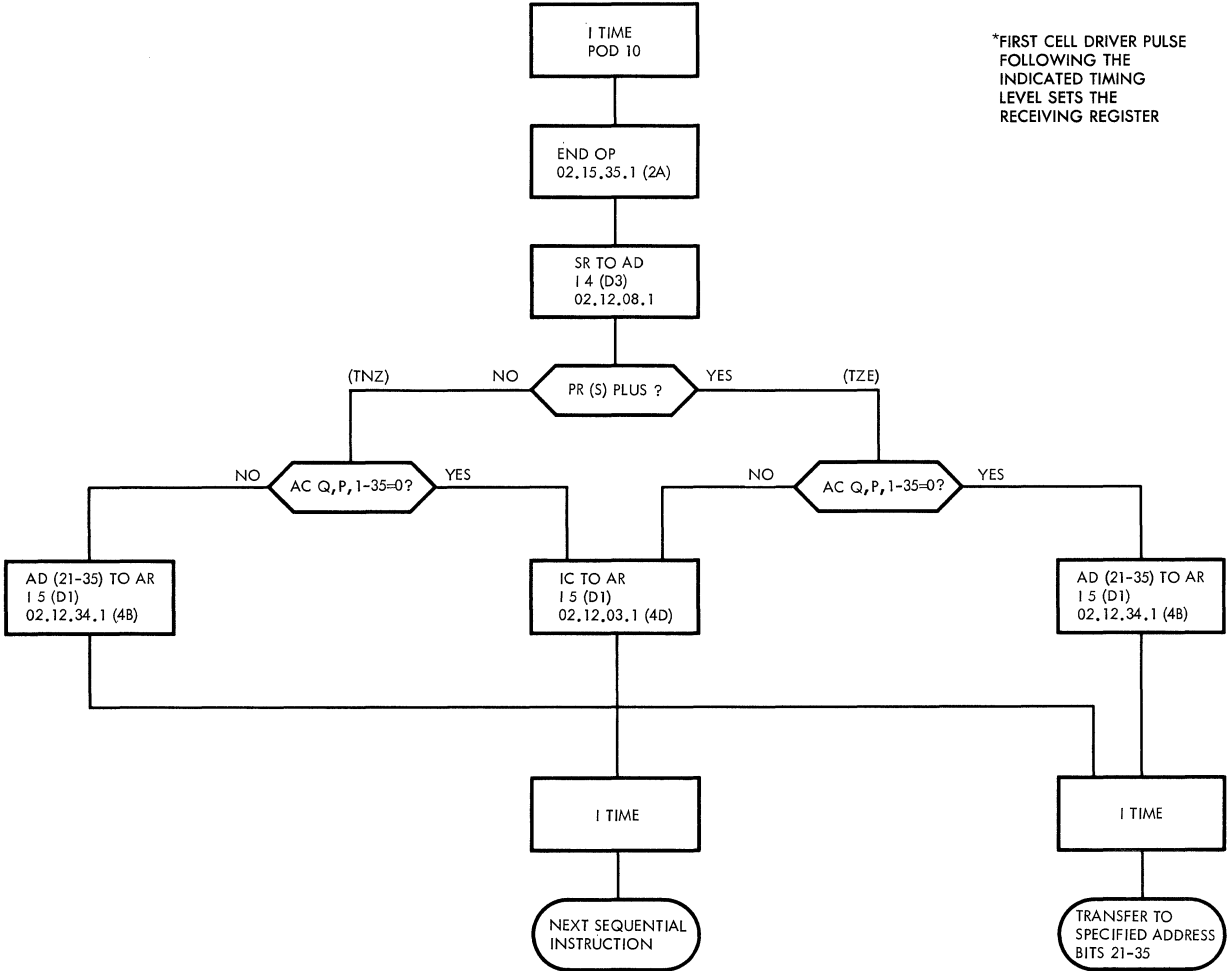
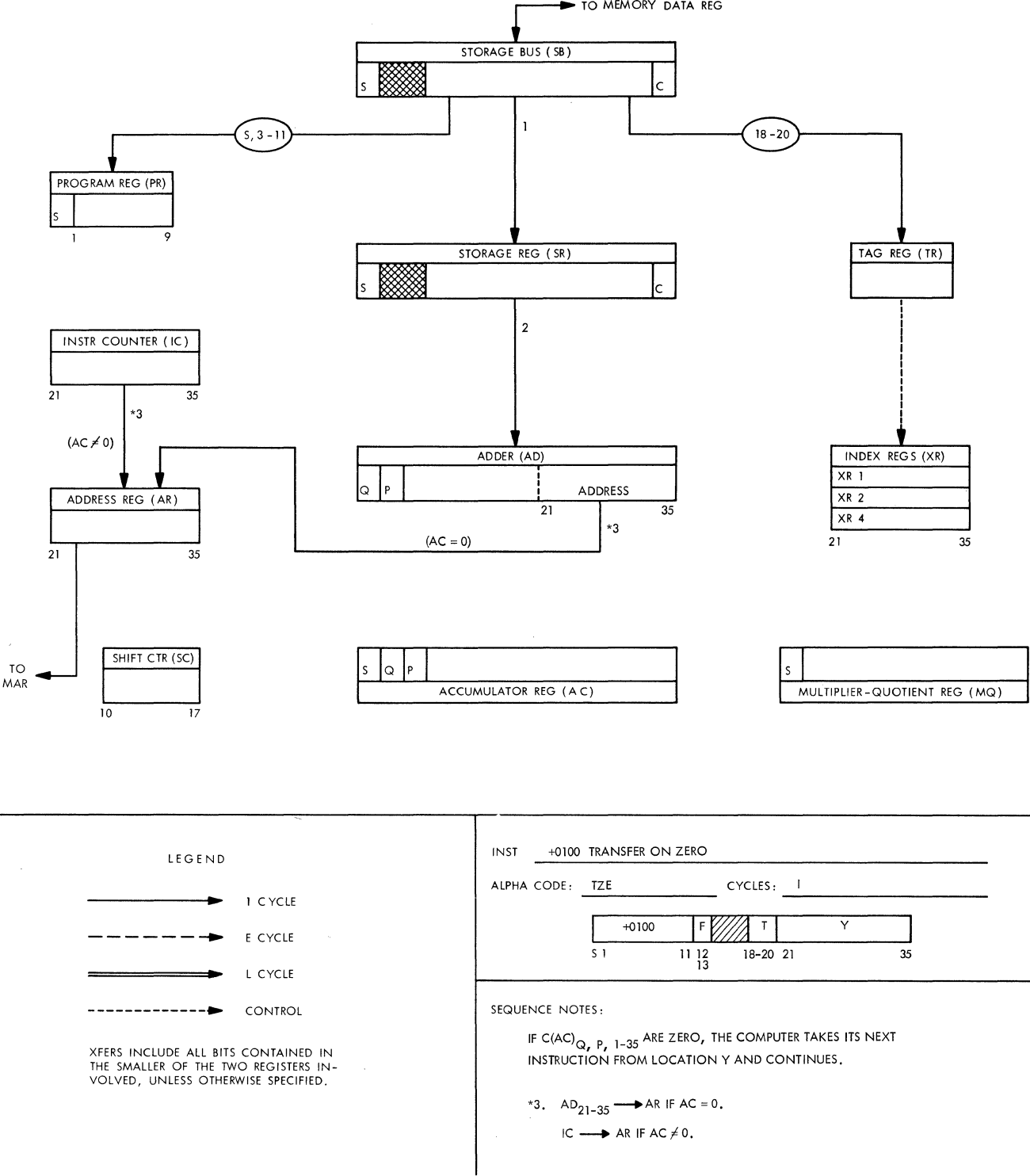
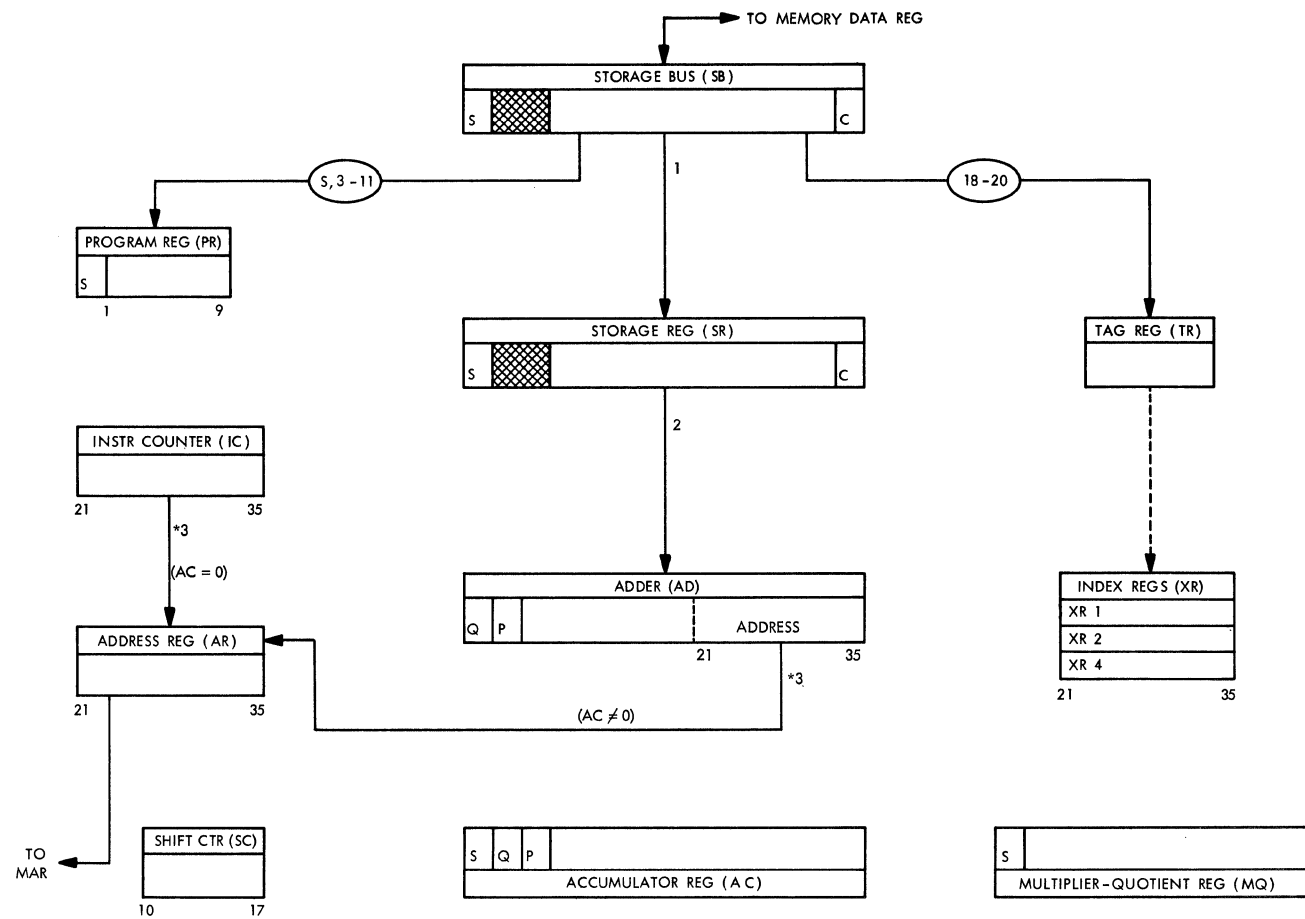


FIGURE 40. TZE, TNZ





LEGEND

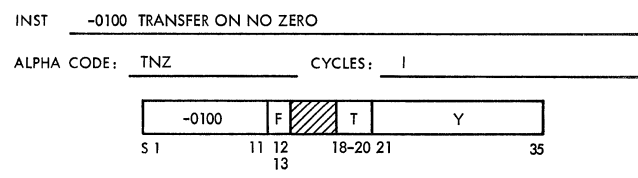
→ 1 CYCLE

--- E CYCLE

== L CYCLE

----- CONTROL

XFER INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

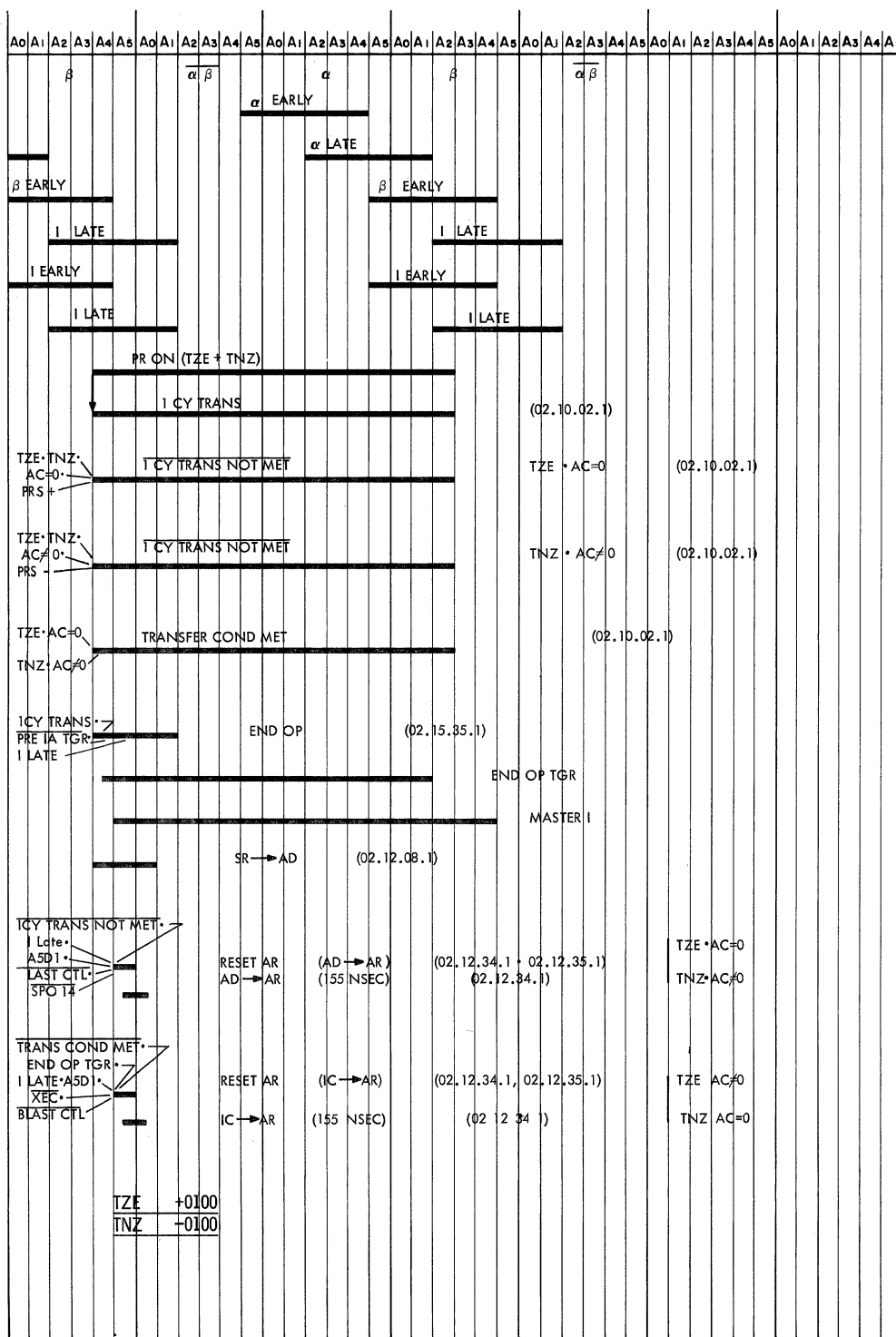


SEQUENCE NOTES:

IF C(AC)_{Q, P, 1-35} ARE NOT ZERO, THE COMPUTER TAKES ITS NEXT INSTRUCTION FROM LOCATION Y AND CONTINUES.

*3 AD₂₁₋₃₅ → AR IF AC ≠ 0.

IC → AR IF AC = 0.



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	TZE		00003	010000 000003
00002	HPR		00000	042000 000000
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			000000 000000

Transfer on Zero (TZE)																						CONSOLE INDICATORS									
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (A 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (M 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	P CARRY	FP OVERFLOW	FP 1	FP 2										
I	E	00001	+500	000	0	00006	050000000006	000000000000	00																						
E	I	00001	+500	000	0	00001	000000000000	000000000000	00																						
I	I	00002	+100	000	0	00003	010000000003	000000000000	00																						
I	I	00004	+020	000	0	00000	002000000000	000000000000	00																						

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	TNZ		00003	410000 000003
00002	HPR		00000	042000 000000
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			377777 777777

Transfer on No Zero (TNZ)																					
CONSOLE INDICATORS																					
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (A 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (M 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	P CARRY	OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00												
E	I	00001	+500	000	0	00001	377777777777	377777777777	00												
I	I	00002	-100	000	0	00003	410000000003	377777777777	00												
I	I	00004	+020	000	0	00000	002000000000	377777777777	00												
I	E	00001	+500	000	0	00006	050000000006	377777777777	00												

Transfer on Plus (TPL+0120)
If the sign of the accumulator is plus, the computer takes its next instruction from the location specified by the address field of the instruction word. If the sign is minus, the computer takes the next sequential instruction.

Transfer on Minus (TMI-0120)
If the sign of the accumulator is minus, the computer takes its next instruction from the location specified by the address field of the instruction word. If the sign is plus, the computer takes the next sequential instruction.

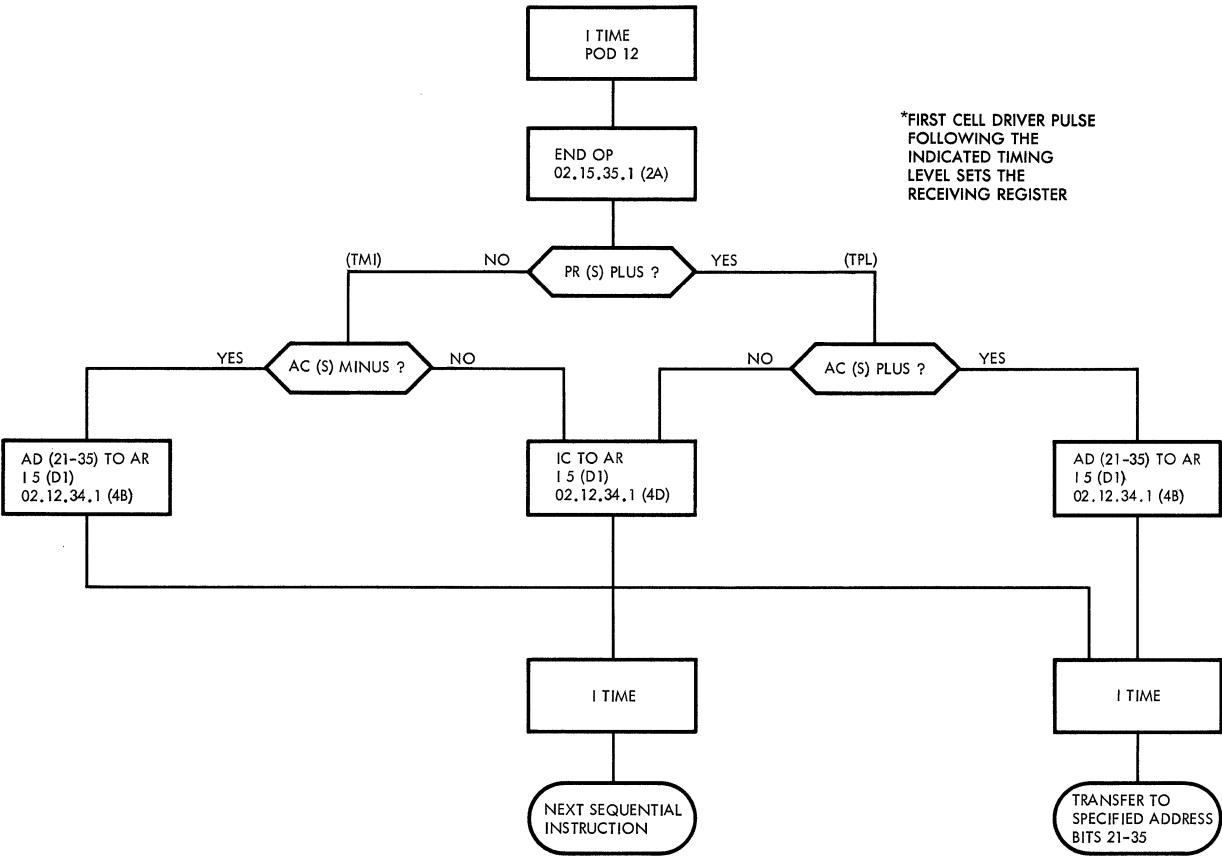
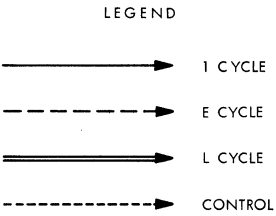
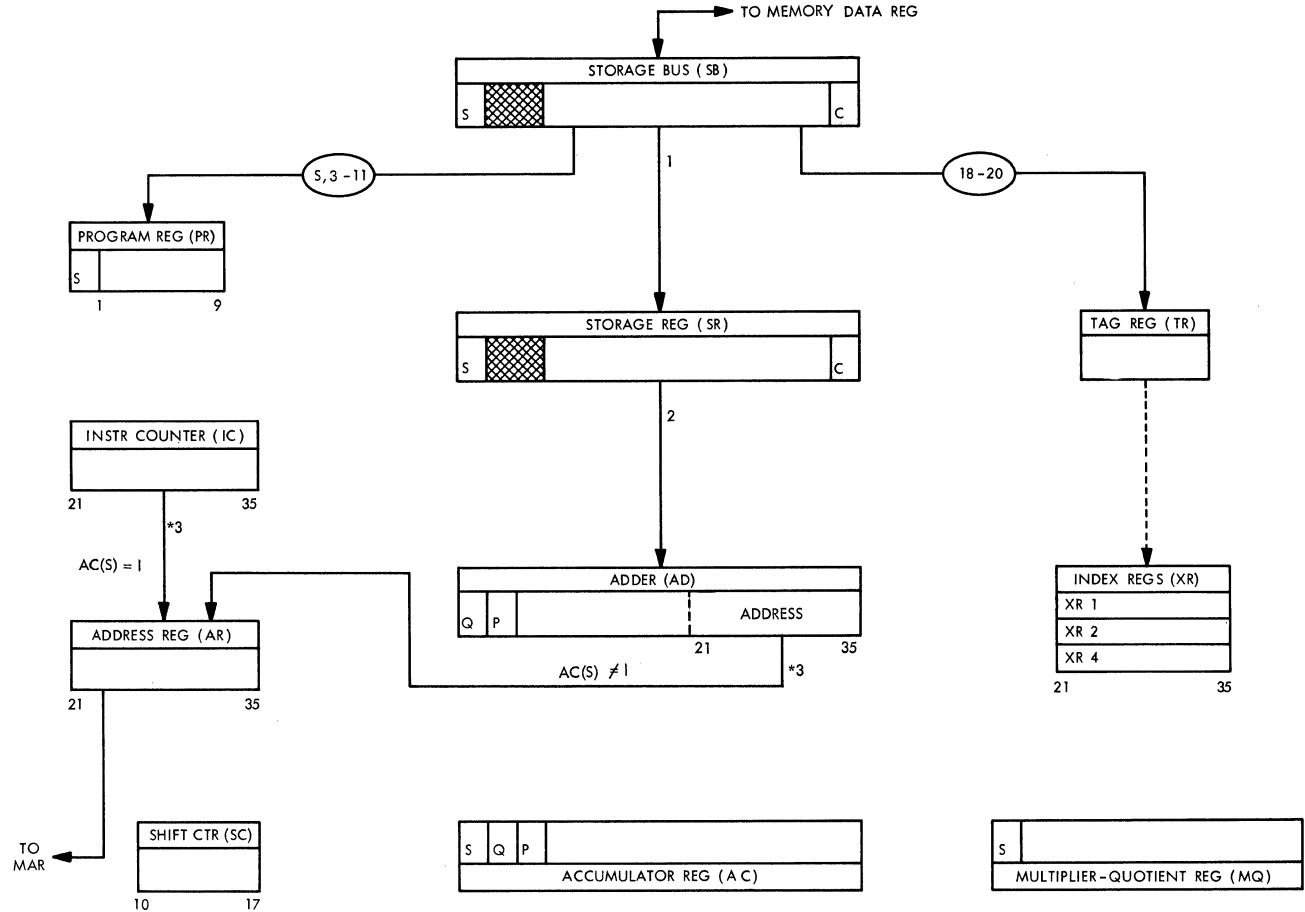
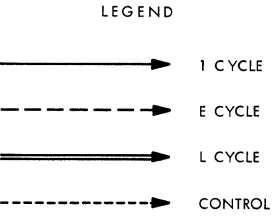
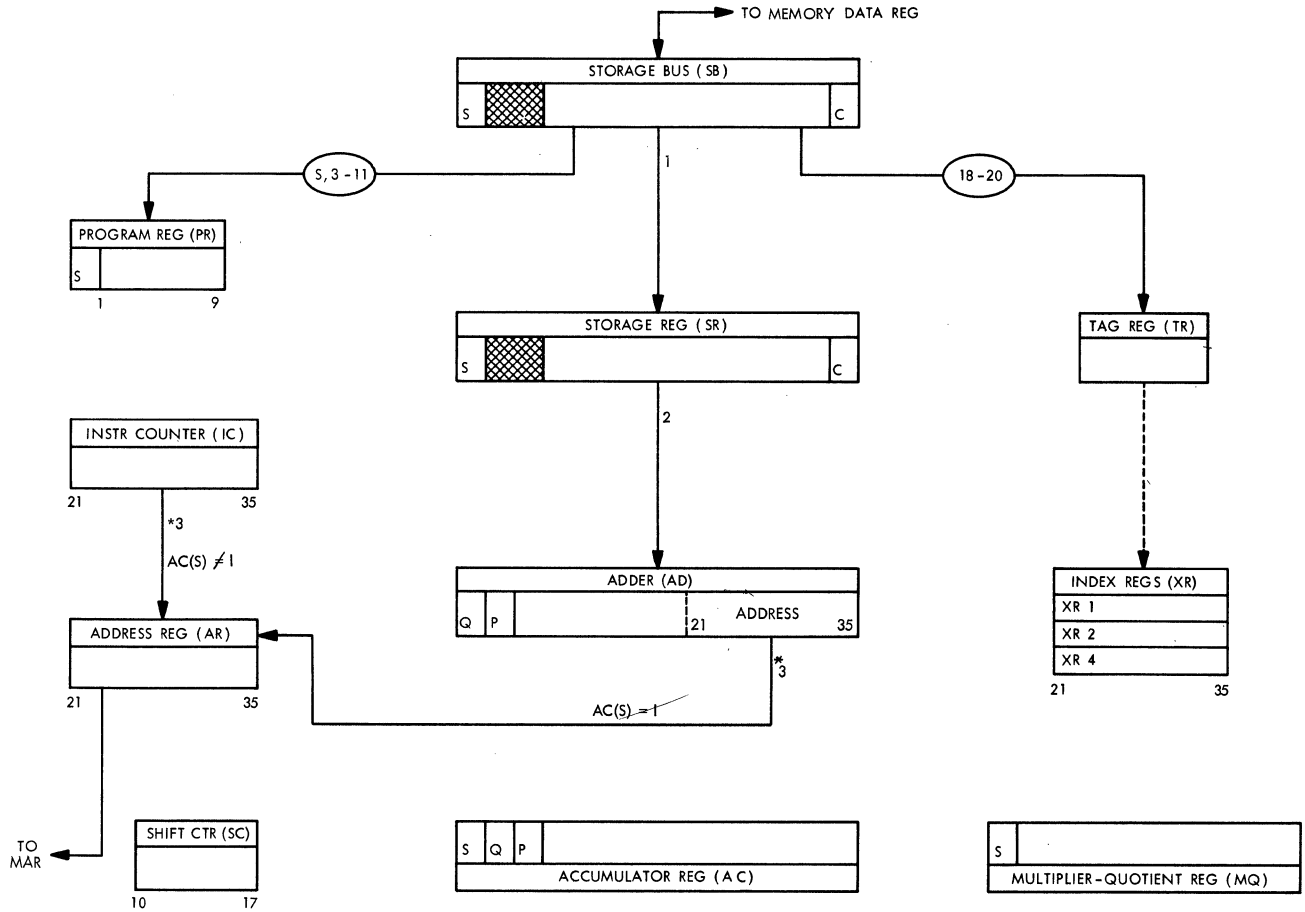
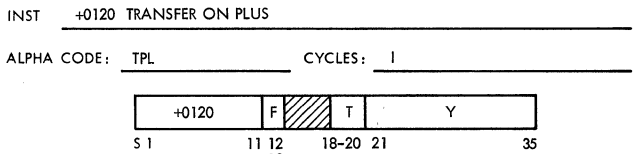


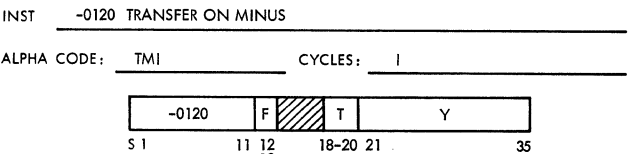
FIGURE 41. TPL,TMI

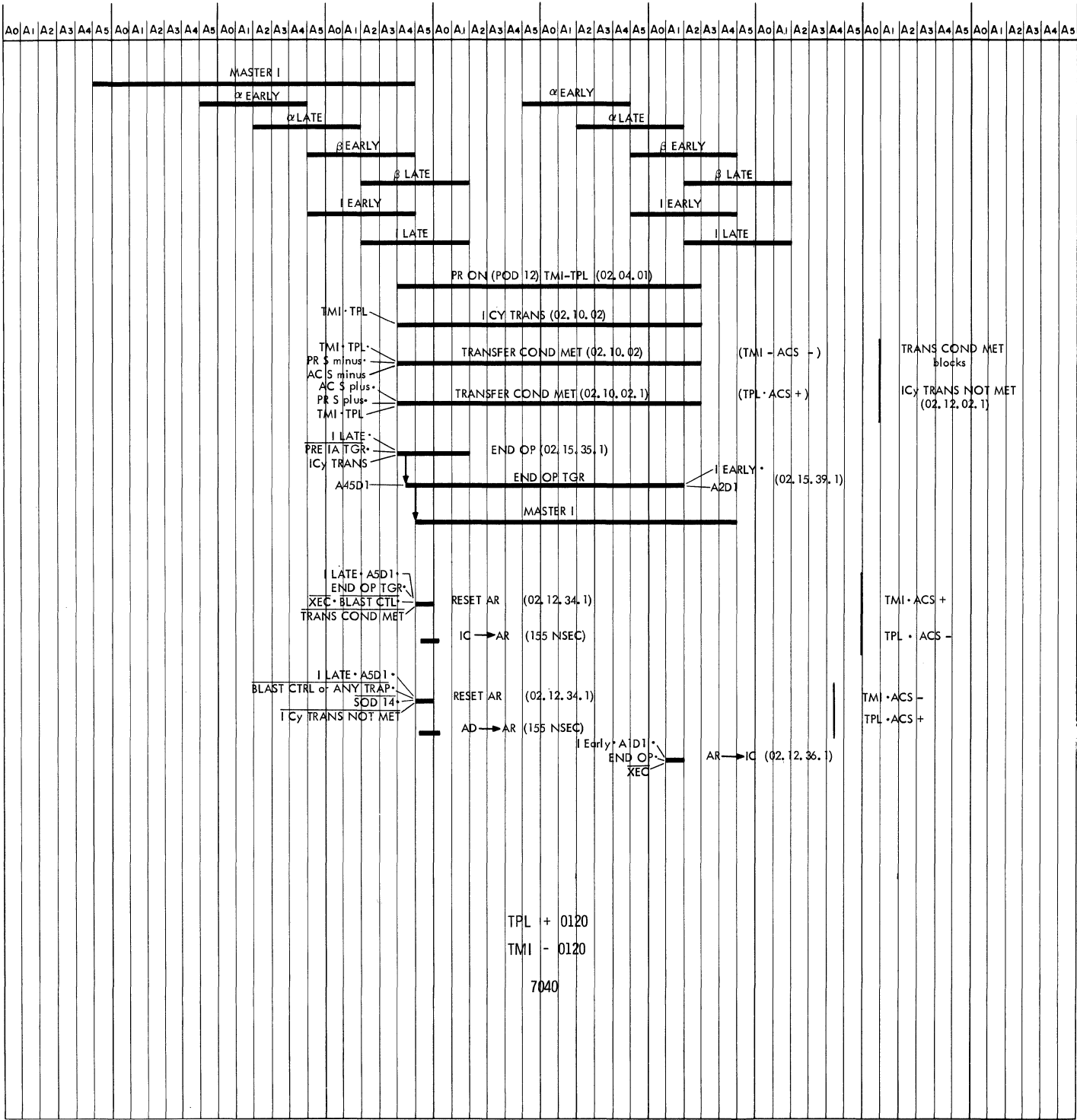


XFRS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.



XFRS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.





Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	TPL		00003	012000 000003
00002	HPR		00000	042000 000000
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			377777 777777

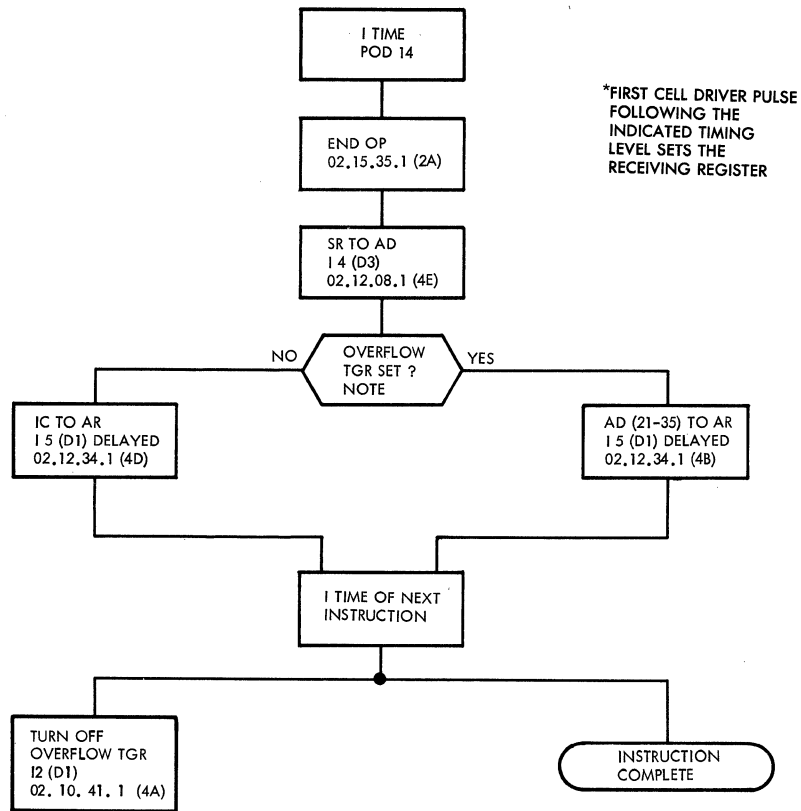
Transfer on Plus (TPL)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S 1-35)	ACCUMULATOR (Q P)	MQ REGISTER (S 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK
I	E	00001	+500	000	0	00006	050000000006	000000000000	00						
E	I	00001	+500	000	0	00001	377777777777	377777777777	00						
I	I	00002	+120	000	0	00003	012000000003	377777777777	00						
I	I	00004	+020	000	0	00000	002000000000	377777777777	00						
I	E	00001	+500	000	0	00006	050000000006	377777777777	00						

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	TMI		00003	412000 000003
00002	HPR		00000	042000 000000
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			400000 000000

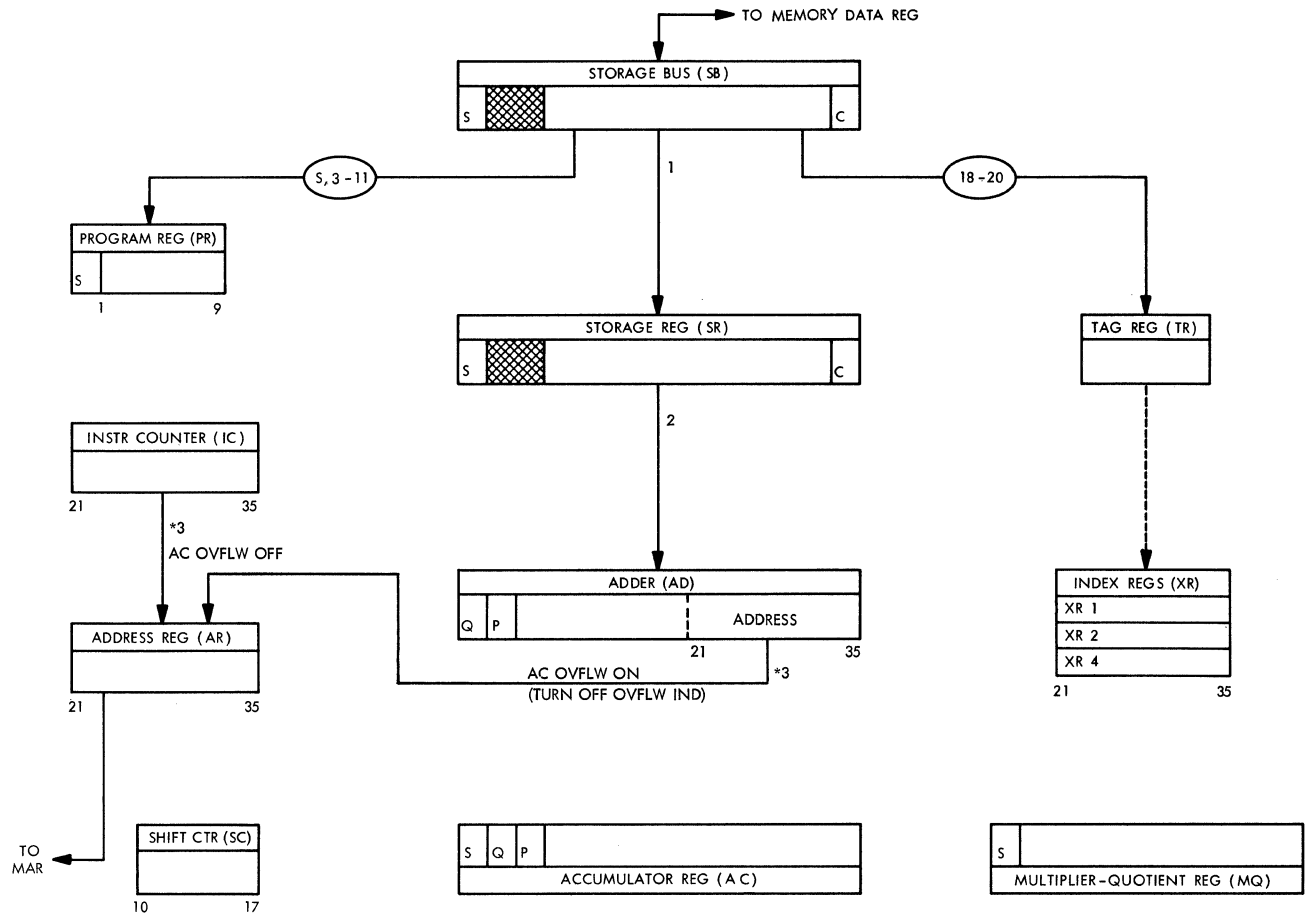
Transfer on Minus (TMI)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S 1-35)	ACCUMULATOR (Q P)	MQ REGISTER (S 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK
I	E	00001	+500	000	0	00006	050000000006	000000000000	00						
E	I	00001	+500	000	0	00001	400000000000	400000000000	00						
I	I	00002	-120	000	0	00003	412000000003	400000000000	00						
I	I	00004	+020	000	0	00000	002000000000	400000000000	00						
I	E	00001	+500	000	0	00006	050000000006	400000000000	00						

NOTE: If the Sign of the accumulator is plus, this routine hangs up with the cycle Time L indicator on.

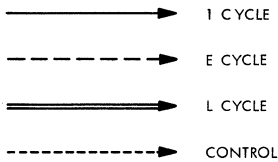
Transfer on Overflow (TOV +0140)
If the overflow indicator is on, it is turned off and the computer takes its next instruction from the location specified by the address field of the instruction word. If the indicator is off, the computer takes the next sequential instruction.



NOTE:
THE OVERFLOW TRIGGER IS SET BY :
1. AD-AC AND POD 40 AND SIGNS ALIKE AND AD 1 CARRY.
2. AC LEFT INSTRUCTION AND AC (1) = 1 AND SC ≠ 0 .



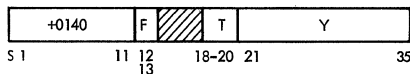
LEGEND



XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0140 TRANSFER ON OVERFLOW

ALPHA CODE: TOV CYCLES: 1

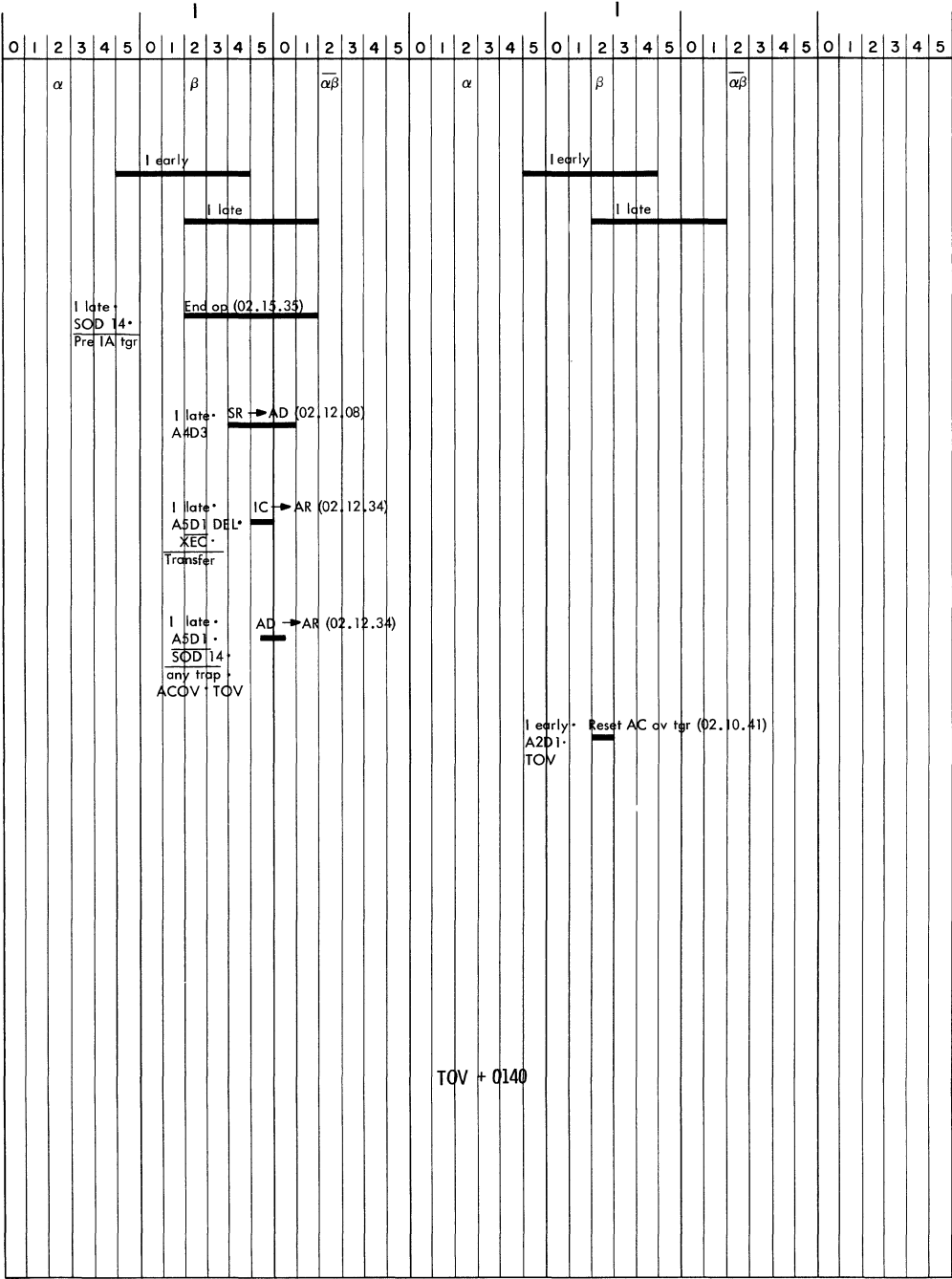


SEQUENCE NOTES:

IF AC OVERFLOW INDICATOR IS ON, THE COMPUTER TURNS OFF THE INDICATOR AND TAKES ITS NEXT INSTRUCTION FROM Y.

*3 AD₂₁₋₃₅ → AR IF AC OVERFLOW ON. (TURN OFF INDICATORS)

IC → AR IF AC OVERFLOW NOT ON.

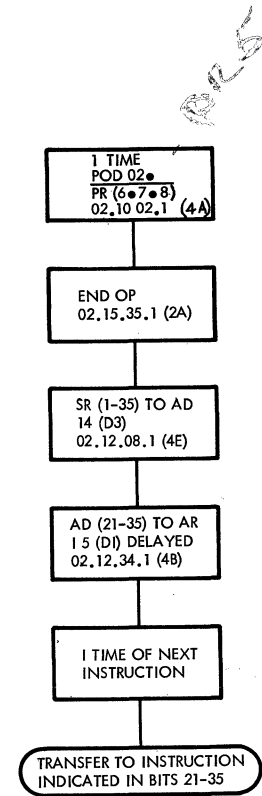


Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	ADD		00006	040000 000006
00002	TOV		00004	014000 000004
00003	HPR		00000	042000 000000
00004	TRA		00000	002000 000000
00005	Pattern		00000	000000 000001
00006	Pattern		00000	377777 777777

Transfer on Overflow (TOV)																
CONSOLE INDICATORS																
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (A, 1-35)	ACCUMULATOR (Q, 1-35)	MQ REGISTER (M, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	X CARRY	P CARRY
I	E	00001	+500	000	0	00005	0500000000005	0000000000000	00							
E	I	00001	+500	000	0	00001	0000000000001	0000000000001	00							
I	E	00002	+400	000	0	00006	0400000000006	0000000000001	00							
E	I	00002	+400	000	0	00002	3777777777777	0000000000000	01				1	1	1	
I	I	00003	+140	000	0	00004	0140000000004	0000000000000	01				1	0	0	
I	I	00005	+020	000	0	00000	0020000000000	0000000000000	01				0	0	0	
I	E	00001	+500	000	0	00005	0500000000005	0000000000000	01				0	0	0	

FIGURE 42. TOV

Transfer (TRA +0020)
Causes the computer to take its next instruction from the location specified by the address field of the instruction word.



*FIRST CELL DRIVER PULSE
FOLLOWING THE
INDICATED TIMING
LEVEL SETS THE
RECEIVING REGISTER

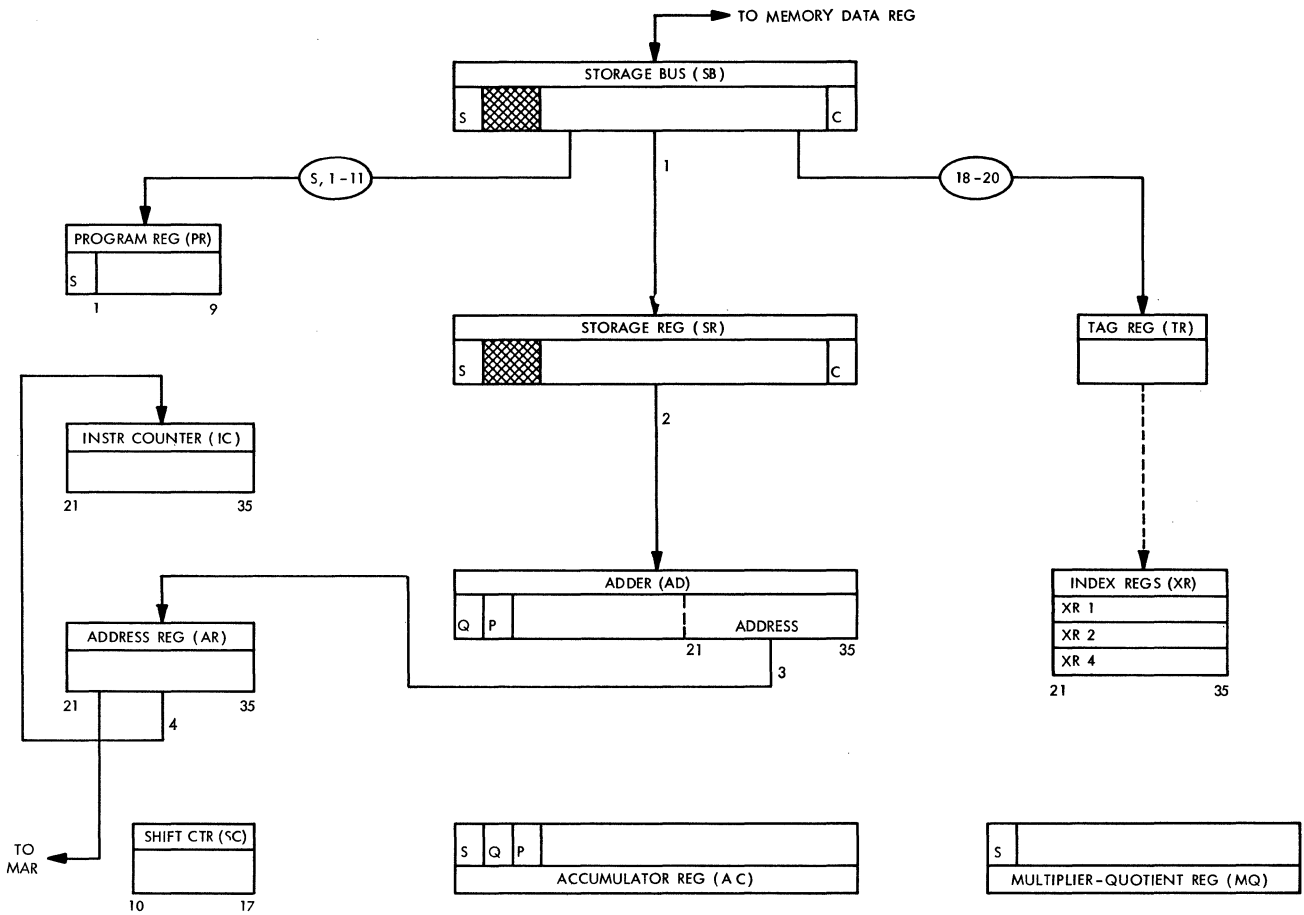


FIGURE 43. TRA

LEGEND

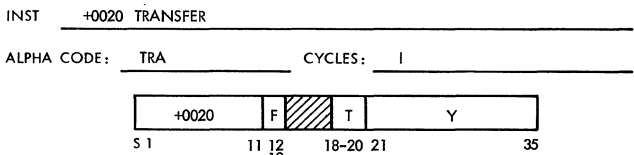
1 CYCLE

E CYCLE

L CYCLE

CONTROL

XFRS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.



SEQUENCE NOTES:

CAUSES THE COMPUTER TO TAKE ITS NEXT INSTRUCTION FROM LOCATION Y AND CONTINUE FROM THERE.

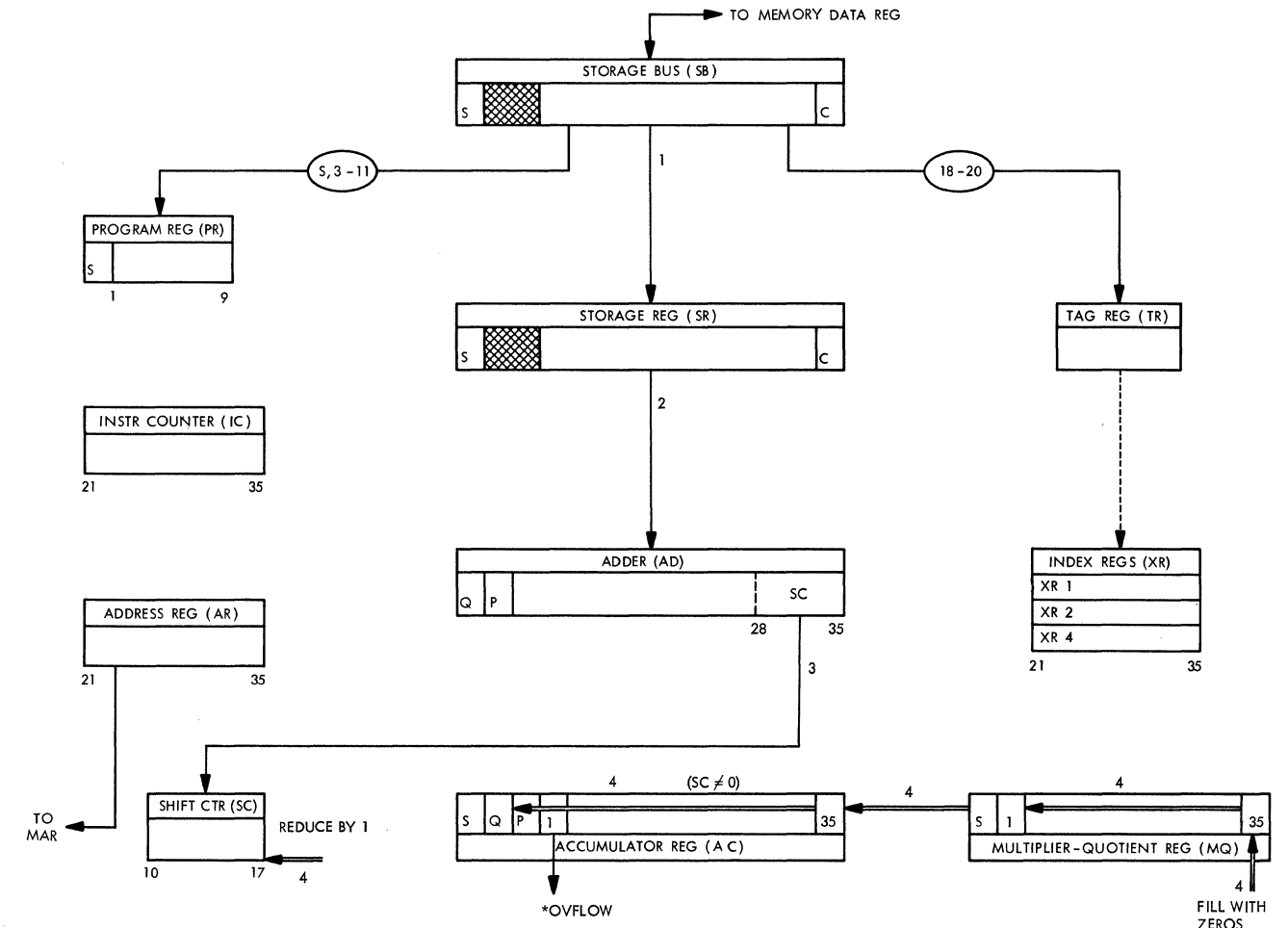
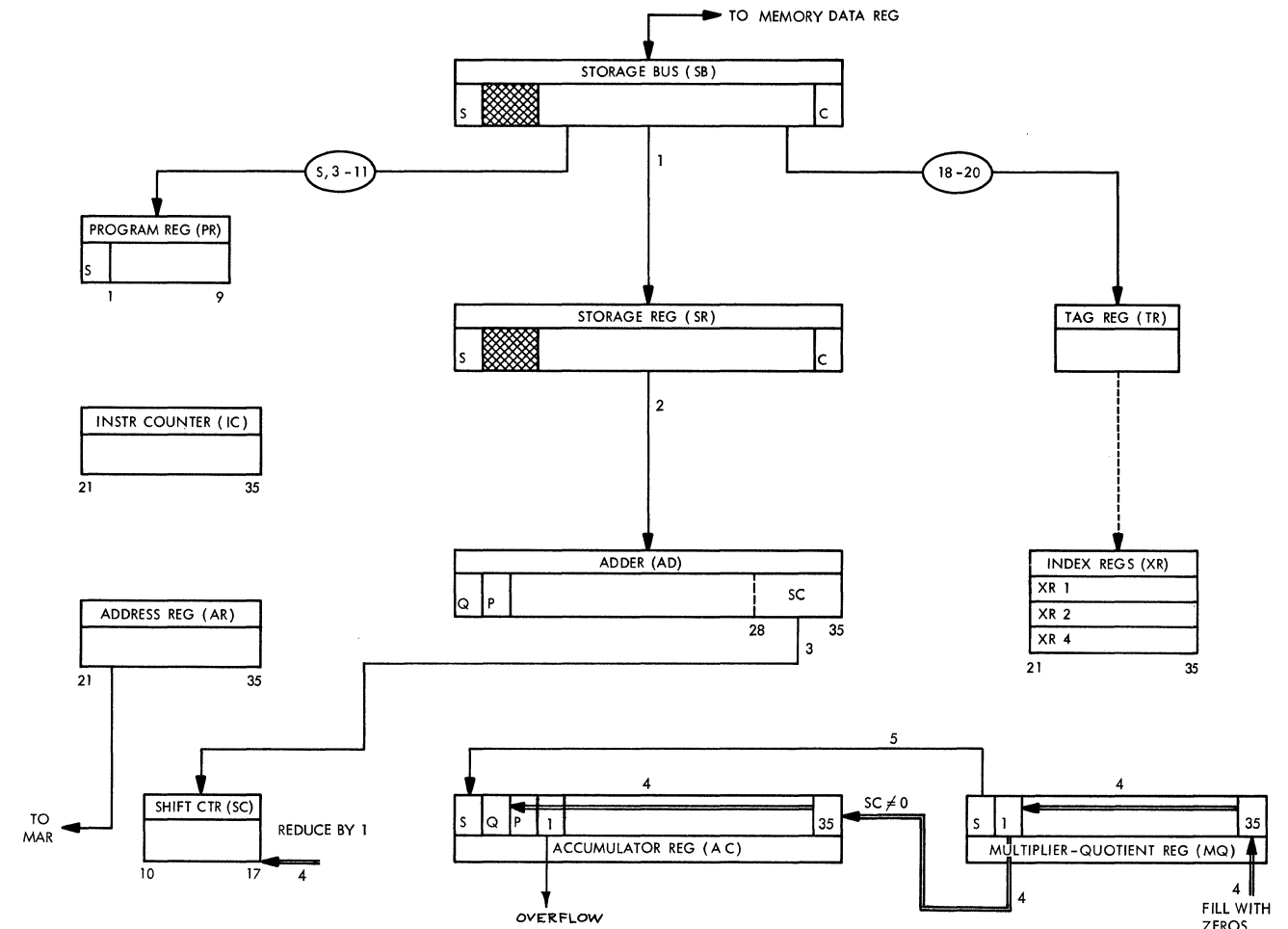
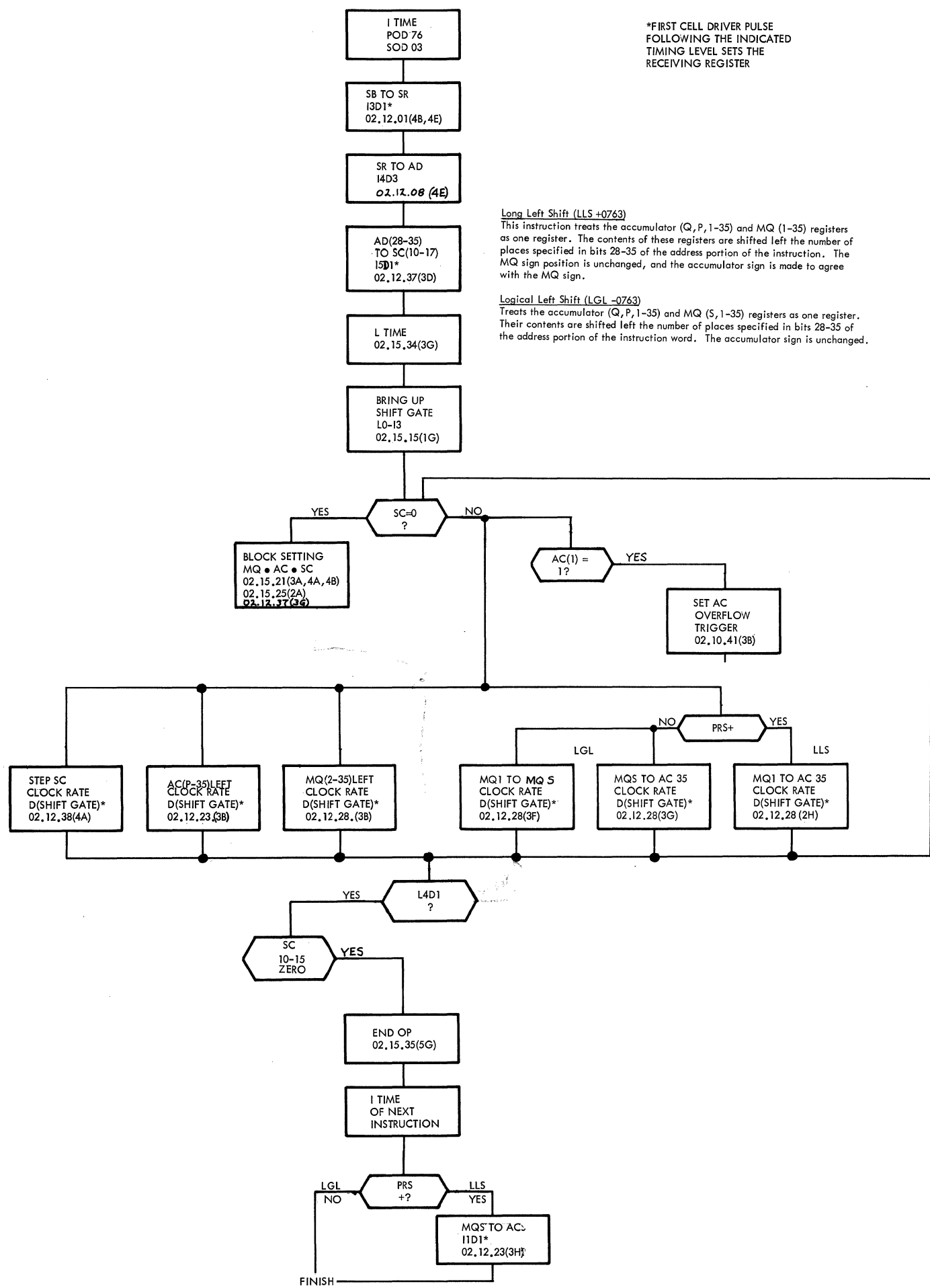


FIGURE 44. LLS,LGL



Long Left Shift (LLS)

CONSOLE INDICATORS

Logical Left Shift (LGL)

CONSOLE INDICATORS

Long Right Shift (LRS +0765)

This instruction treats the accumulator (Q,P,1-35) and the MQ (1-35) registers as one register. The contents of these registers are shifted right the number of places specified in positions 28-35 of the address portion of the instruction word. The accumulator sign is unchanged, and the MQ sign is made to agree with the accumulator sign.

Logical Right Shift (LGR -0765)

Treats the accumulator (Q,P,1-35) and the MQ (S,1-35) registers as one register. The contents of these registers are shifted right the number of places specified in bits 28-35 of the address portion of the instruction word. The accumulator sign is unchanged.

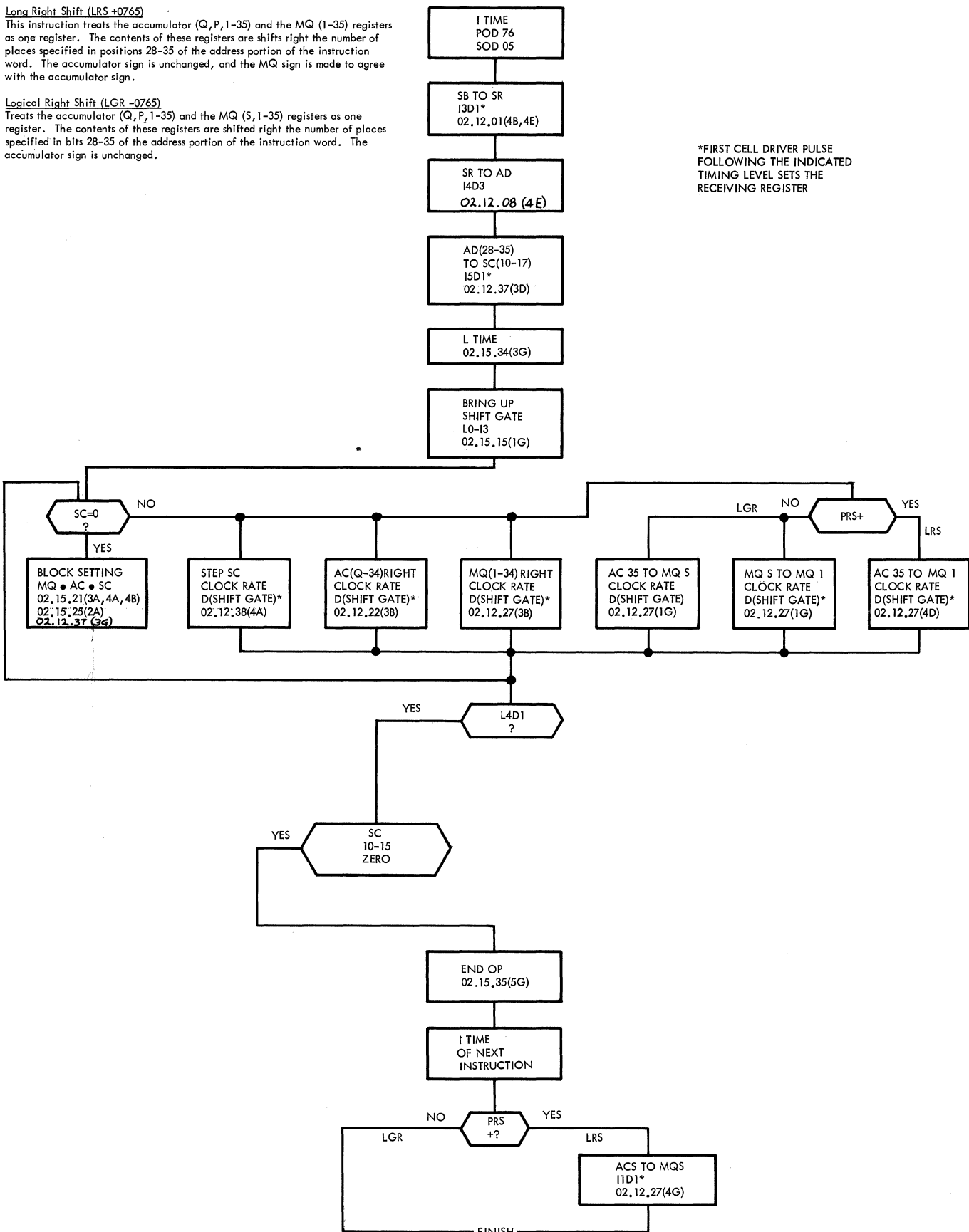
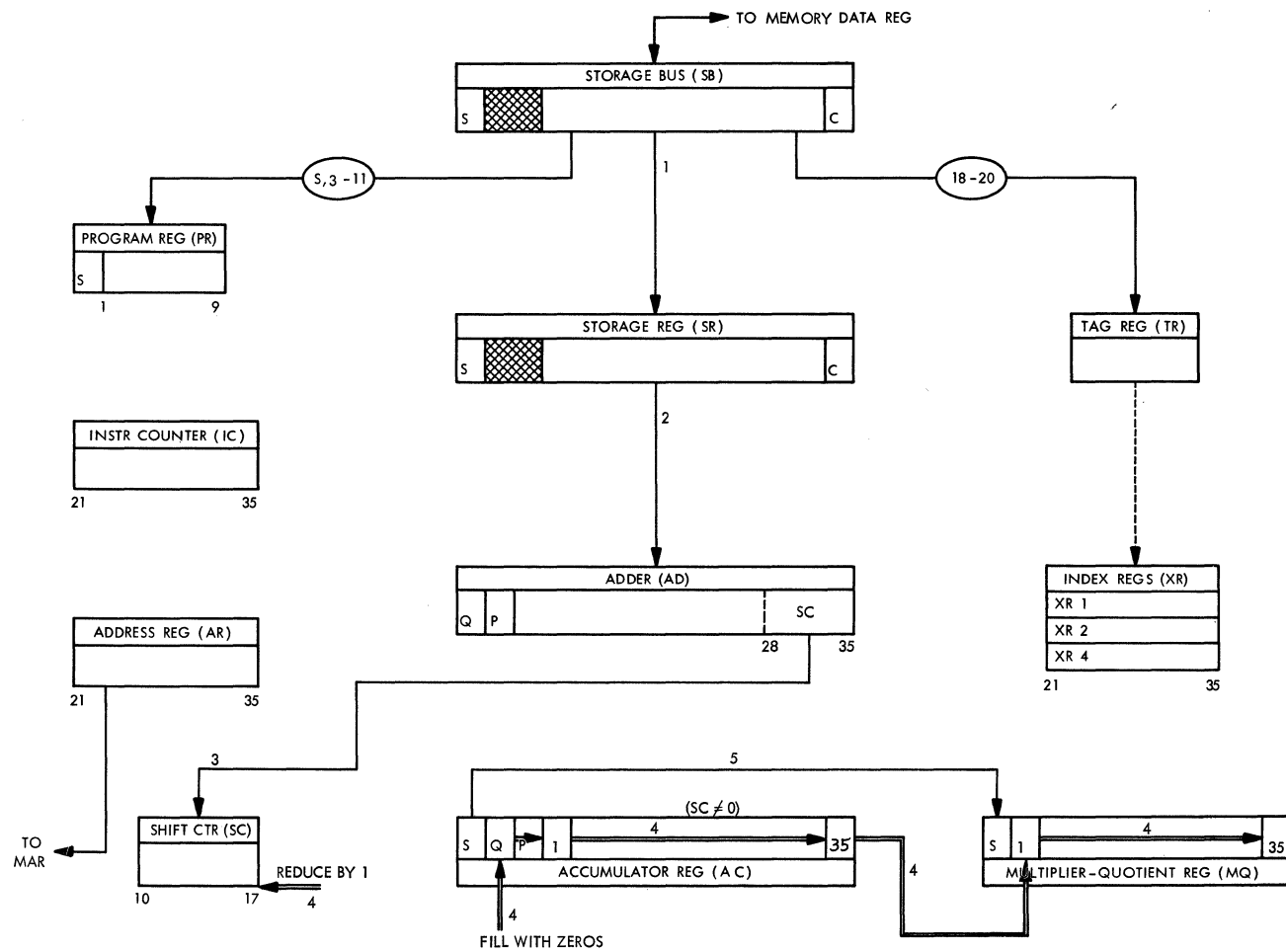
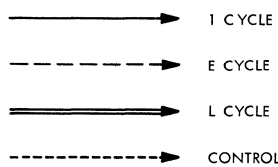


FIGURE 45. LRS,LGR



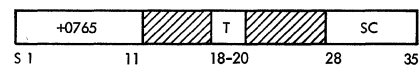
LEGEND



XFRS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0765 LONG RIGHT SHIFT

ALPHA CODE: LRS CYCLES: 1, L, ---



SEQUENCE NOTES:

THE C(AC)_{Q, P, 1-35} AND C(MQ)₁₋₃₅ ARE TREATED AS ONE REGISTER.

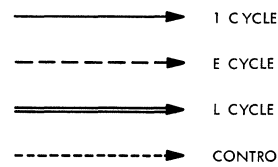
THEIR CONTENTS ARE SHIFTED RIGHT THE NUMBER OF PLACES INDICATED IN 28-35.

THE MQ SIGN IS SET EQUAL TO THE AC SIGN.

VACATED BITS ARE FILLED WITH ZEROS.

CYCLES REQUIRED: 7040: 1-4 2/3
7044: 2-13

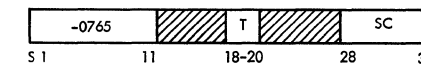
LEGEND



XFRS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -0765 LOGICAL RIGHT SHIFT

ALPHA CODE: LGR CYCLES: 1, L, ---



SEQUENCE NOTES:

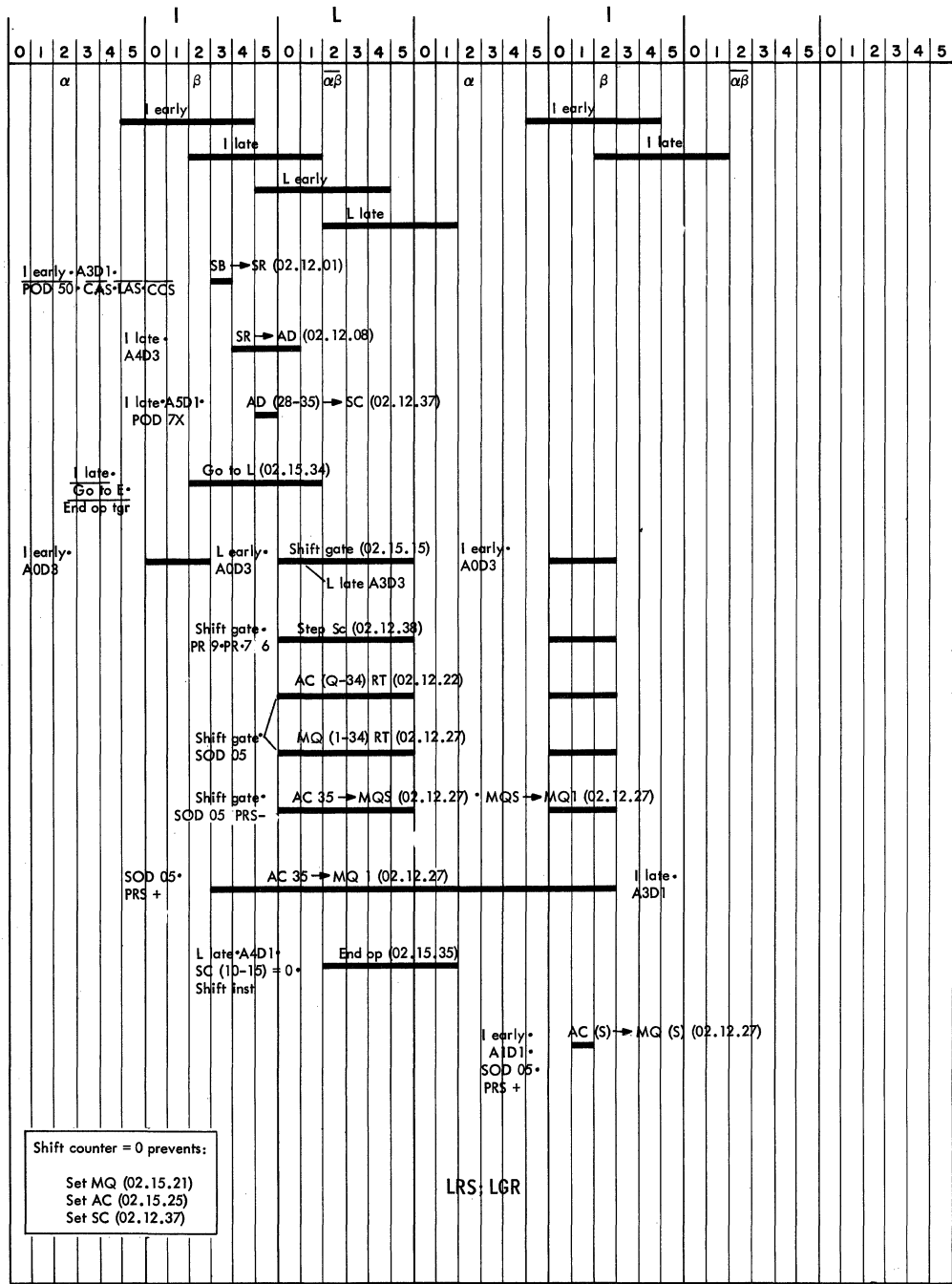
THE C(AC)_{Q, P, 1-35} AND C(MQ)_{S, 1-35} ARE TREATED AS ONE REGISTER.

THEIR CONTENTS ARE SHIFTED RIGHT THE NUMBER OF PLACES INDICATED IN 28-35.

THE SIGN OF THE AC IS UNCHANGED.

VACATED BITS ARE FILLED WITH ZEROS.

CYCLES REQUIRED: 7040: 1-4 2/3
7044: 2-13



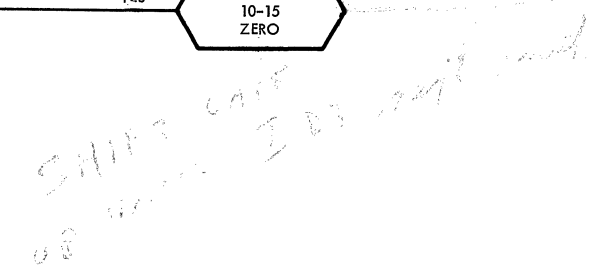
Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	LRS		00043	076500 000043
00002	TRA		00000	002000 000000
00003				
00004				
00005				
00006	Pattern			377777 777777

Long Right Shift (LRS)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	Address	STORAGE REGISTER (S 1-35)	ACCUMULATOR (A 1-35)	ACCUMULATOR (Q P)	MQ REGISTER (S 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	X CARRY
I	E	00001	+500	000	0	00006	0500000000006	0000000000000	00	0000000000000					
E	I	00001	+500	000	0	00001	3777777777777	3777777777777	00	0000000000000					
I	L(1)	00002	+765	043	0	00043	0765000000043	3777777777777	00	0000000000000					
L(1)	L(2)	00002	+765	035	0	00043	0765000000043	0037777777777	00	3740000000000					
L(2)	L(3)	00002	+765	027	0	00043	0765000000043	0000377777777	00	3777400000000					
L(3)	L(4)	00002	+765	021	0	00043	0765000000043	0000003777777	00	3777774000000					
L(4)	L(5)	00002	+765	013	0	00043	0765000000043	0000000037777	00	3777777400000					
L(5)	L(6)	00002	+765	005	0	00043	0765000000064	0000000000037	00	3777777777400					
L(6)	I	00002	+765	000	0	00002	0765000000043	0000000000000	00	3777777777777					
I	I	00003	+020	000	0	00000	0020000000000	0000000000000	00	3777777777777					
I	E	00001	+500	000	0	00006	0500000000006	0000000000000	00	3777777777777					
E	I	00001	+500	000	0	00001	3777777777777	3777777777777	00	3777777777777					
I	L(1)	00002	+765	043	0	00043	0765000000043	3777777777777	00	3777777777777					
L(1)	L(2)	00002	+765	035	0	00043	0765000000043	0037777777777	00	3777777777777					
L(2)	L(3)	00002	+765	027	0	00043	0765000000043	0000377777777	00	3777777777777					
L(3)	L(4)	00002	+765	021	0	00043	0765000000043	0000003777777	00	3777777777777					
L(4)	L(5)	00002	+765	013	0	00043	0765000000043	0000000037777	00	3777777777777					
L(5)	L(6)	00002	+765	005	0	00043	0765000000043	0000000000037	00	3777777777777					
L(6)	I	00002	+765	000	0	00002	0765000000043	0000000000000	00	3777777777777					
I	I	00003	+020	000	0	00000	0020000000000	0000000000000	00	3777777777777					
I	E	00001	+500	000	0	00006	0500000000006	0000000000000	00	3777777777777					

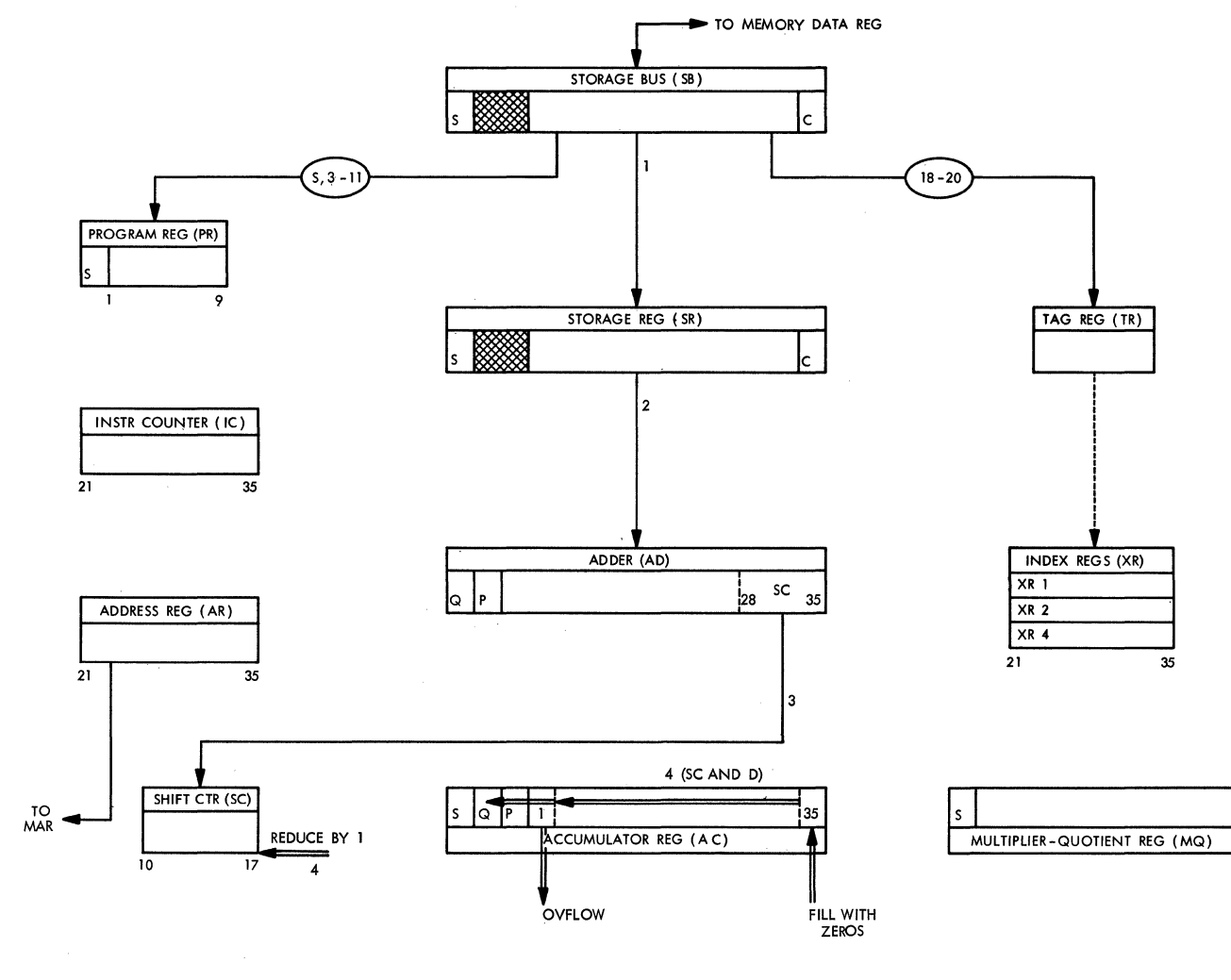
Location Switches	Inst	Tag	Address	Octal Equiv
00000	CAL		00006	450000 000006
00001	LGR		00044	476500 000044
00002	TRA		00000	002000 000000
00003				
00004				
00005				
00006	Pattern			777777 777777

Logical Right Shift (LGR)															
CONSOLE INDICATORS															
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION SHIFT COUNTER	TAG	Address	STORAGE REGISTER (S 1-35)	ACCUMULATOR (A 1-35)	ACCUMULATOR (Q P)	MQ REGISTER (S 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	X CARRY
I	E	00001	-500	000	0	00006	4500000000006	0000000000000	00	0000000000000					
E	I	00001	-500	000	0	00001	7777777777777	3777777777777	01	0000000000000					
I	L(1)	00002	-765	044	0	00044	4765000000044	3777777777777	01	0000000000000					
L(1)	L(2)	00002	-765	036	0	00044	4765000000044	0077777777777	00	7700000000000					
L(2)	L(3)	00002	-765	030	0	00044	4765000000044	0000777777777	00	7777000000000					
L(3)	L(4)	00002	-765	022	0	00044	4765000000044	0000007777777	00	7777770000000					
L(4)	L(5)	00002	-765	014	0	00044	4765000000044	0000000077777	00	7777777000000					
L(5)	L(6)	00002	-765	006	0	00044	4765000000044	0000000000777	00	7777777777000					
L(6)	I	00002	-765	000	0	00002	4765000000044	0000000000000	00	7777777777777					
I	I	00003	+020	000	0	00000	0020000000000	0000000000000	00	7777777777777					
I	E	00001	-500	000	0	00006	4500000000006	0000000000000	00	7777777777777					
E	I	00001	-500	000	0	00001	7777777777777	3777777777777	01	7777777777777					
I	L(1)	00002	-765	044	0	00044	4765000000044	3777777777777	01	7777777777777					
L(1)	L(2)	00002	-765	036	0	00044	4765000000044	0077777777777	00	7777777777777					
L(2)	L(3)	00002	-765	030	0	00044	4765000000044	0000777777777	00	7777777777777					
L(3)	L(4)	00002	-765	022	0	00044	4765000000044	0000007777777	00	7777777777777					
L(4)	L(5)	00002	-765	014	0	00044	4765000000044	0000000077777	00	7777777777777					
L(5)	L(6)	00002	-765	006	0	00044	4765000000044	0000000000777	00	7777777777777					

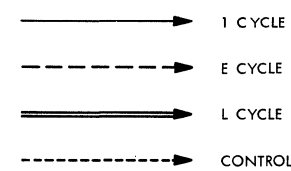
Causes the contents of the accumulator (Q,P,1-35) to be shifted left the number of places specified in bits 28-35 of the address portion of the instruction word. The sign position is unchanged.



*FIRST CELL DRIVER PULSE
FOLLOWING THE INDICATED
TIMING LEVEL SETS THE
RECEIVING REGISTER



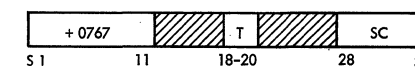
LEGEND



XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST	+0767 ACCUMULATOR LEFT SHIFT
------	------------------------------

ALPHA CODE:



SEQUENCE NOTES:

THE C(AC)_{Q,P}, 1-35 ARE SHIFTED LEFT THE NUMBER OF PLACES INDICATED IN 28-35. SIGN POSITION IS UNCHANGED, VACATED BITS FILLED WITH ZEROS. A "1" SHIFTED OUT OF POS 1 TURNS ON AC OVFLOW.

CYCLES REQUIRED: 7040 1-2 2/3
7044 2-7

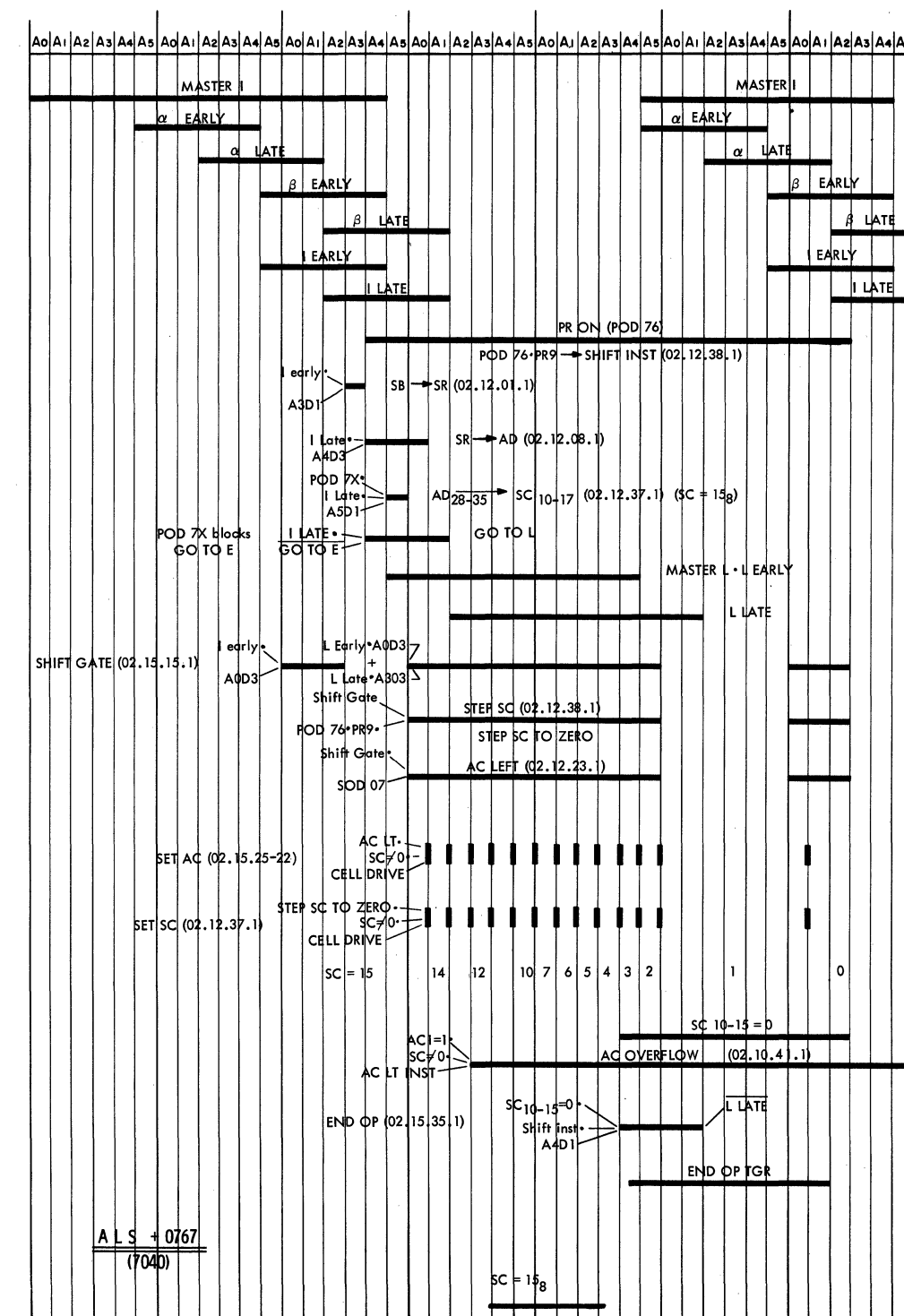


FIGURE 46. ALS

Accumulator Right Shift (ARS-0077)
Causes the contents of the accumulator (Q,P,1-35) to be shifted right the number of places specified in bits 28-35 of the address portion of the instruction word. The sign position is unchanged.

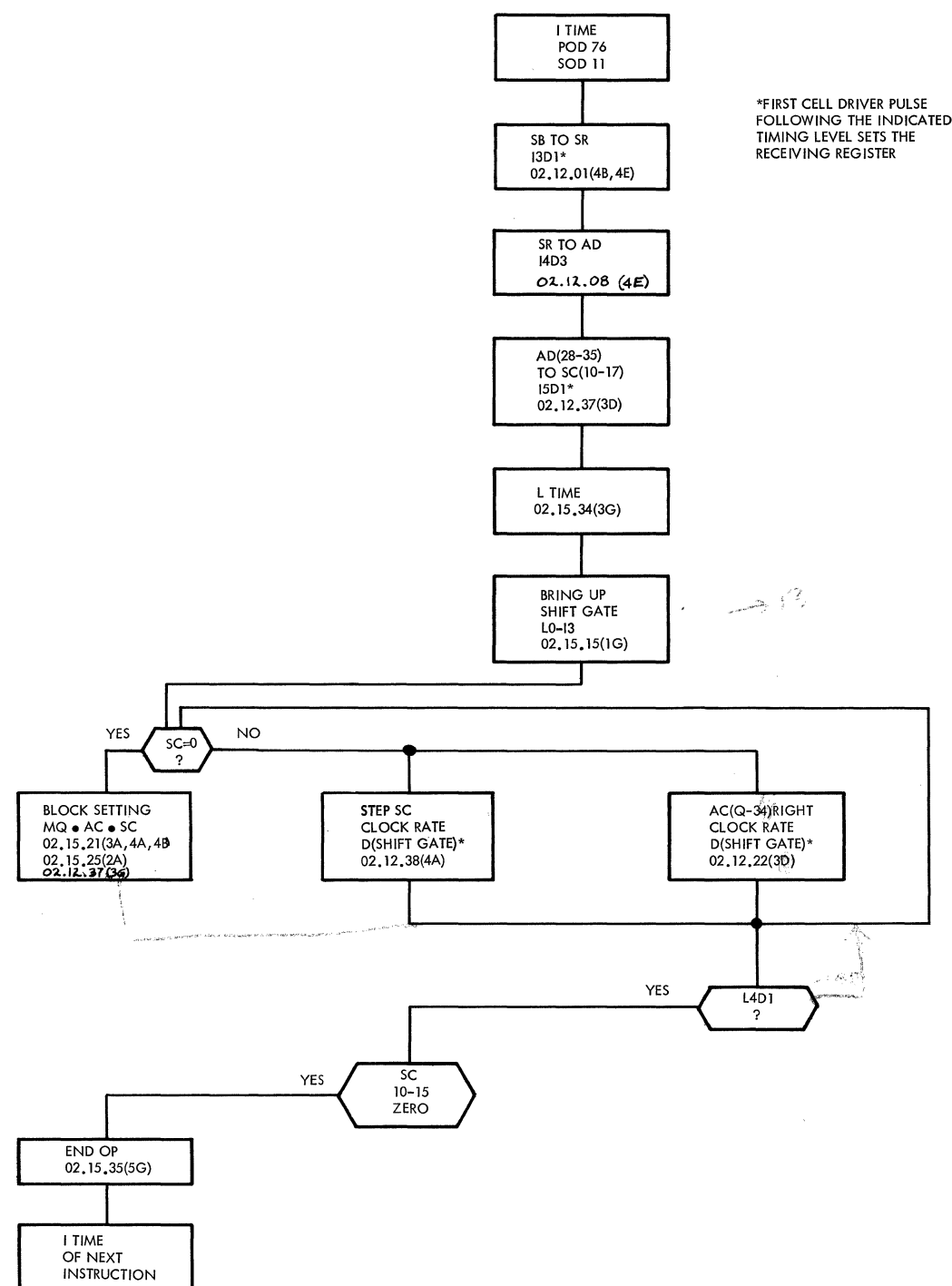
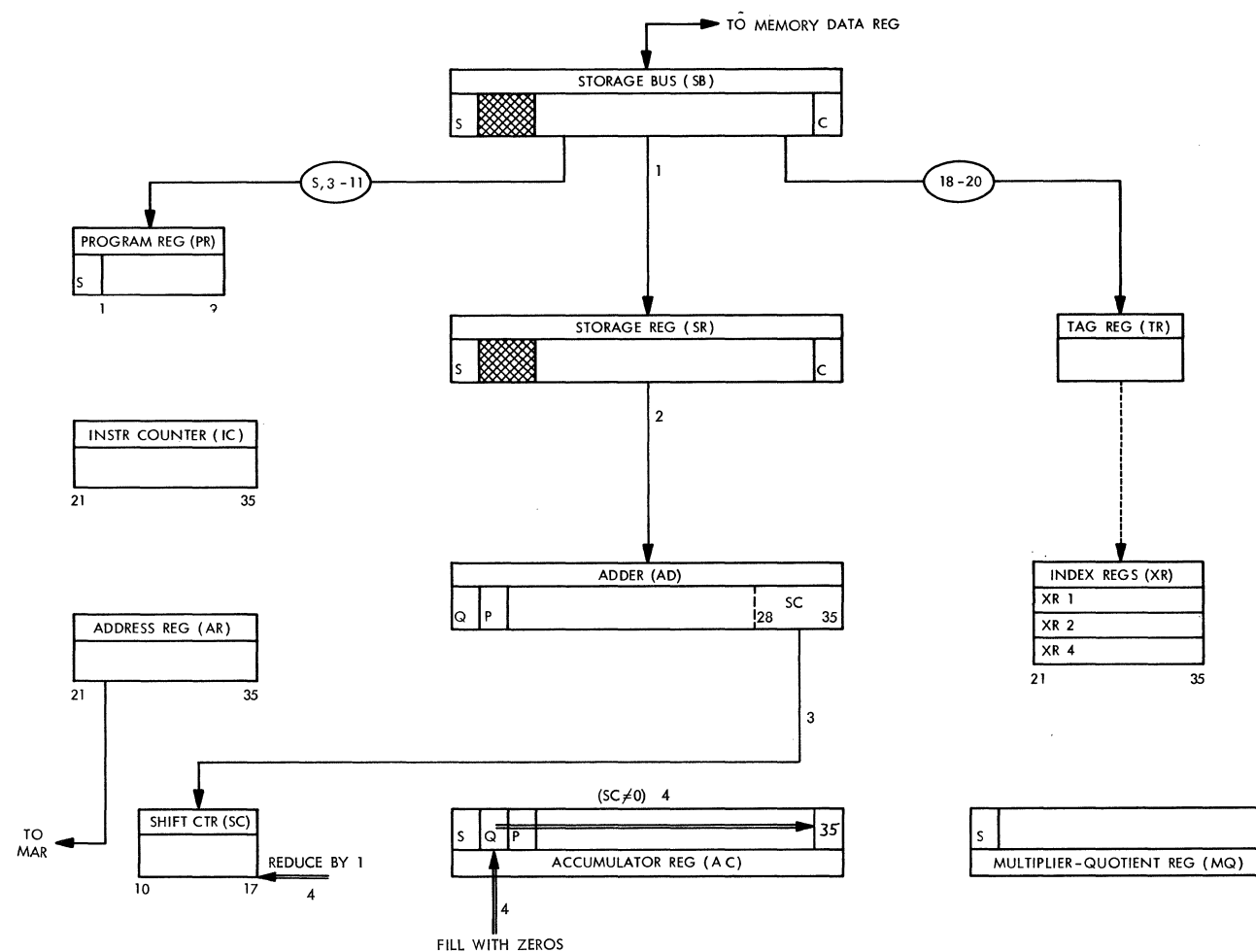


FIGURE 47. ARS



LEGEND

1 CYCLE
E CYCLE
L CYCLE
CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0771 ACCUMULATOR RIGHT SHIFT

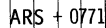
ALPHA CODE: ARS CYCLES: I, L,----



SEQUENCE NOTES:

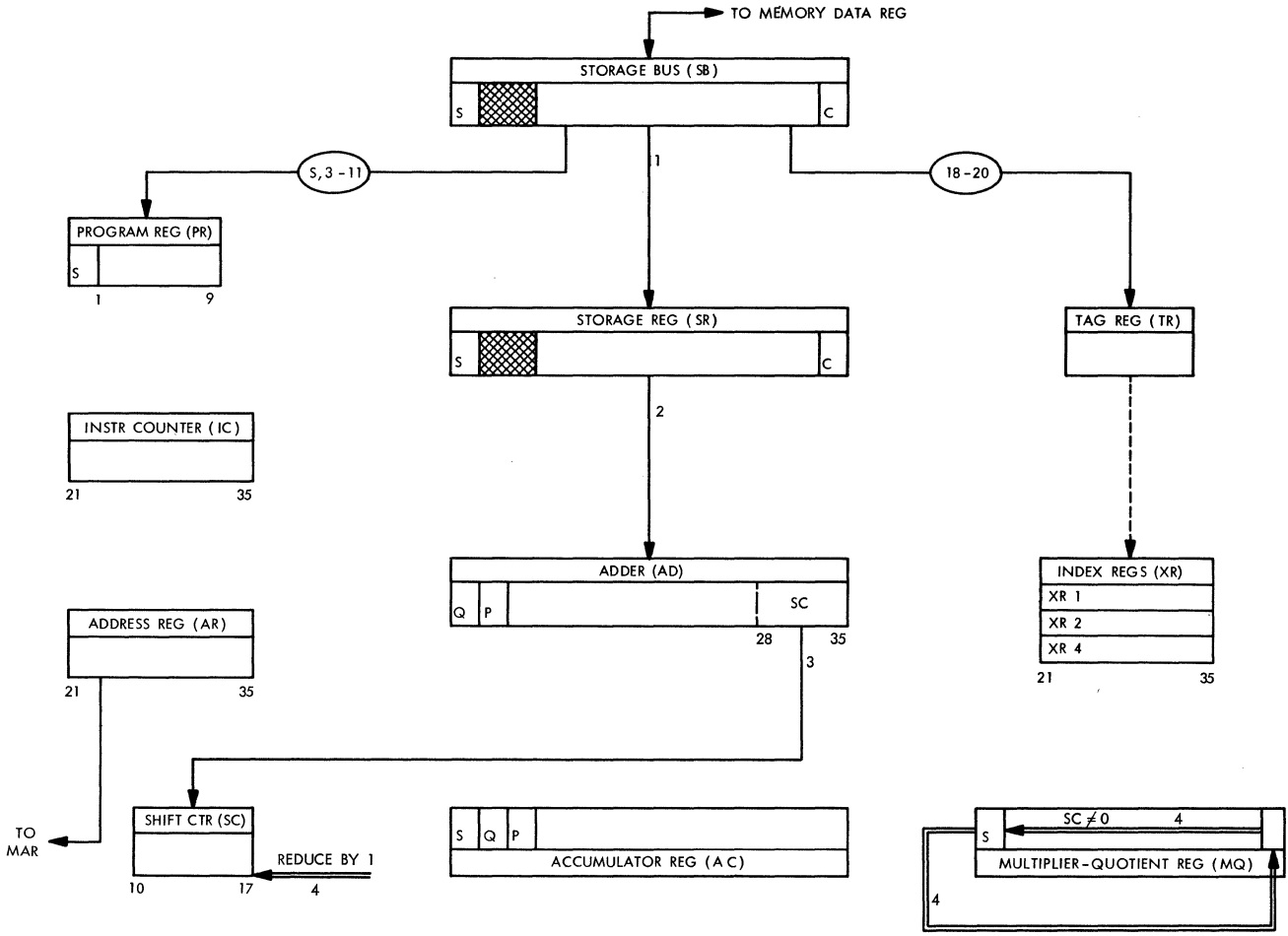
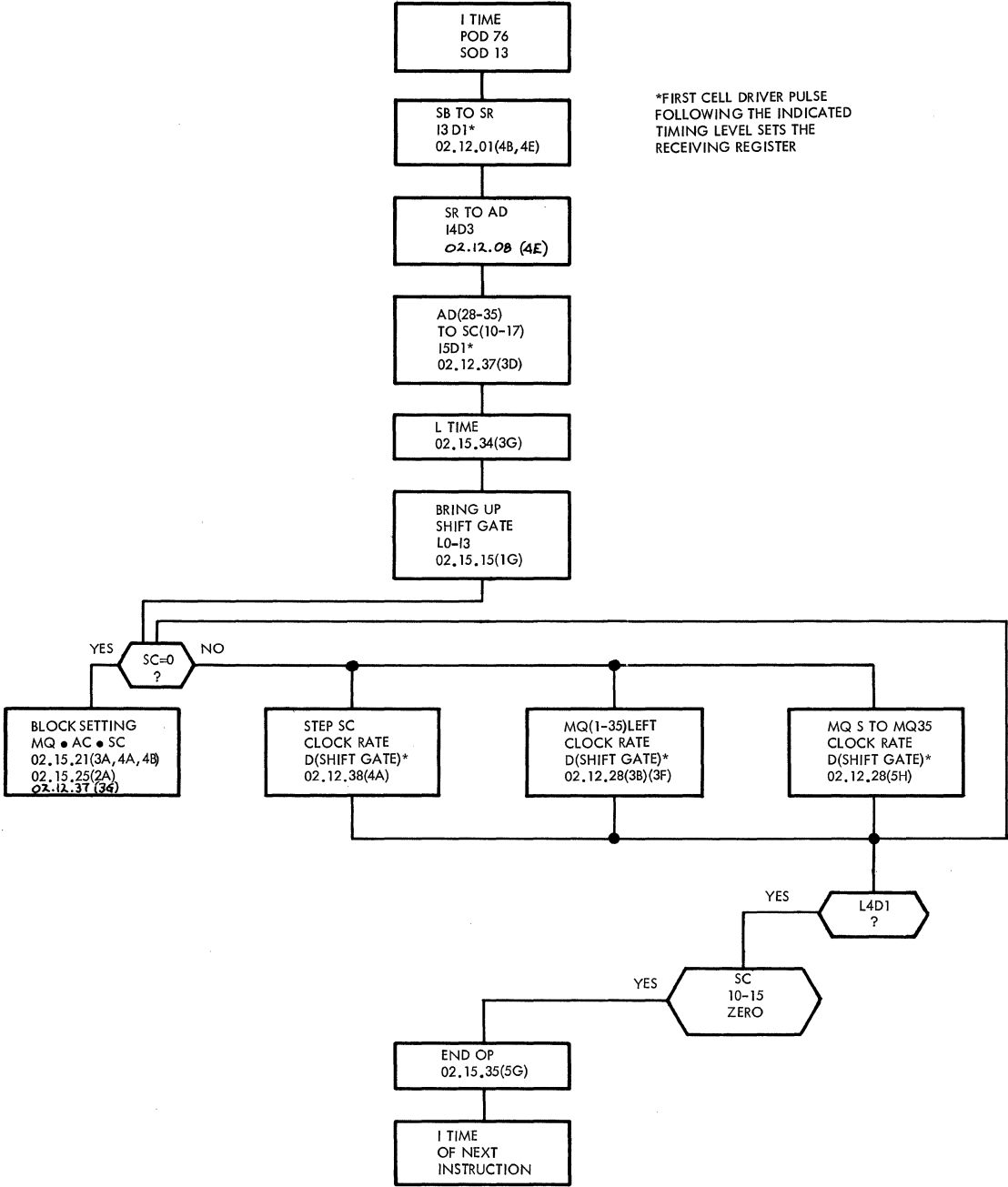
THE C(AC)_{Q,P,1-35} ARE SHIFTED RIGHT THE NUMBER OF PLACES INDICATED IN 28-35. THE SIGN POSITION IS UNCHANGED. VACATED BITS ARE FILLED WITH ZEROS.

CYCLES REQUIRED: 7040 1-2 2/3
7044 2-7



Accumulator Right Shift (ARS)

Rotate MQ Left (RQL -0773)
The contents of the MQ register (S,1-35) are shifted left the number of places specified by the address portion of the instruction word. The sign position shifts into position 35; thus, the register becomes a closed loop.



LEGEND

1 CYCLE

E CYCLE

L CYCLE

CONTROL

XFRS INCLUDE ALL BITS CONTAINED IN
THE SMALLER OF THE TWO REGISTERS IN-
VOLVED, UNLESS OTHERWISE SPECIFIED.

INST -0773 ROTATE MQ LEFT

ALPHA CODE: RQL CYCLES: I, L, ---

SEQUENCE NOTES:

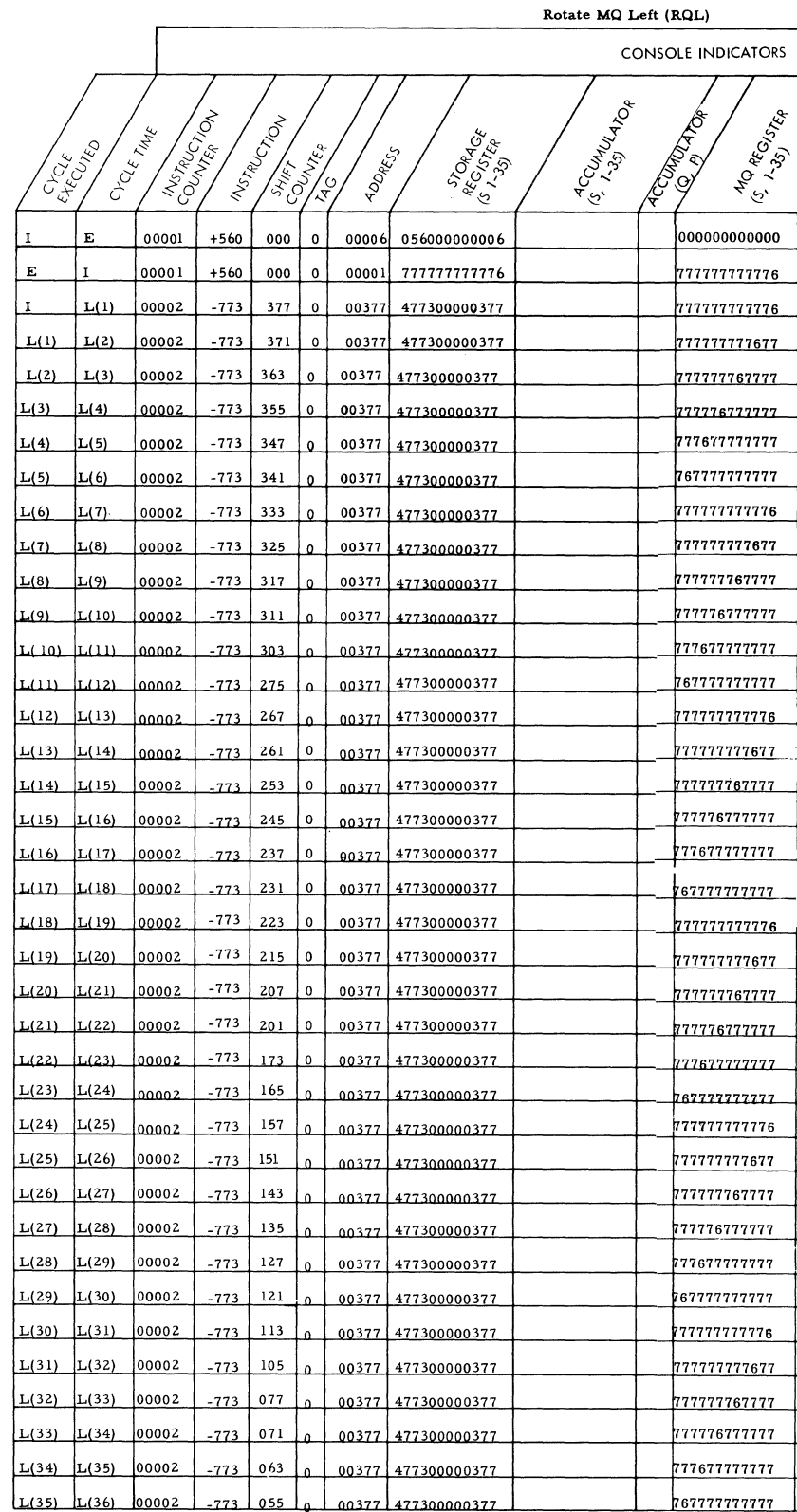
THE C(MQ)_{S,1-35} ARE SHIFTED LEFT THE NUMBER OF PLACES INDICATED IN 28-35.

THE SIGN BIT IS CONNECTED TO THE 35 BIT FORMING A CLOSED SHIFTING LOOP.

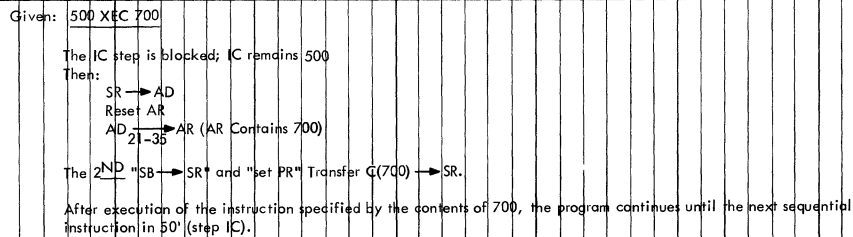
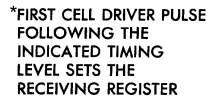
NO BITS ARE LOST.

CYCLES REQUIRED: 7040: 1 - 2 2/3
7044: 2 - 7

FIGURE 48. RQL

[illegible]

Causes the computer to execute the instruction at the location specified by the address portion of the instruction word. The computer then returns to the location plus 1 of the Execute instruction.

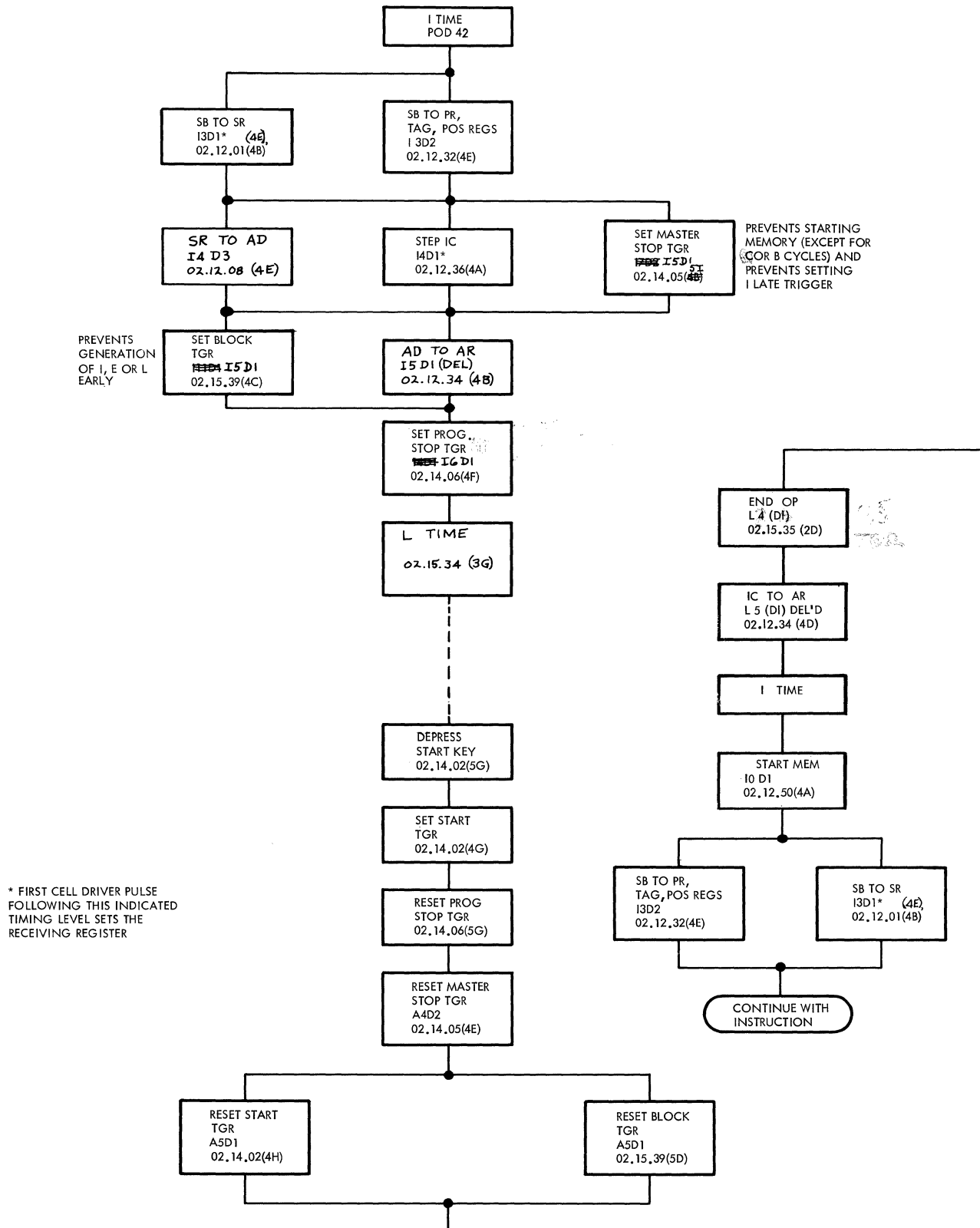


Execute (XEC)											CONSOLE INDICATORS	
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (A 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TAI	
I	E	00001	+500	000	0	00006	050000000006	000000000000	00			
F	I	00001	+500	000	0	00001	042000000000	042000000000	00		←	
I	I	00001	+522	000	0	00005	052200000005	042000000000	00			
I	E	00002	+400	000	0	00006	040000000006	042000000000	00			
E	I	00002	+400	000	0	00002	042000000000	104000000000	00			
I	I	00002	+522	000	0	00005	052200000005	104000000000	00			
I	E	00003	+400	000	0	00006	040000000006	104000000000	00			
E	I	00003	+400	000	0	00003	042000000000	146000000000	00			
I	I	00003	+522	000	0	00004	052200000004	146000000000	00			
I	I	00004	+020	000	0	00000	002000000000	146000000000	00			
I	E	00001	+500	000	0	00006	050000000006	146000000000	00		←	

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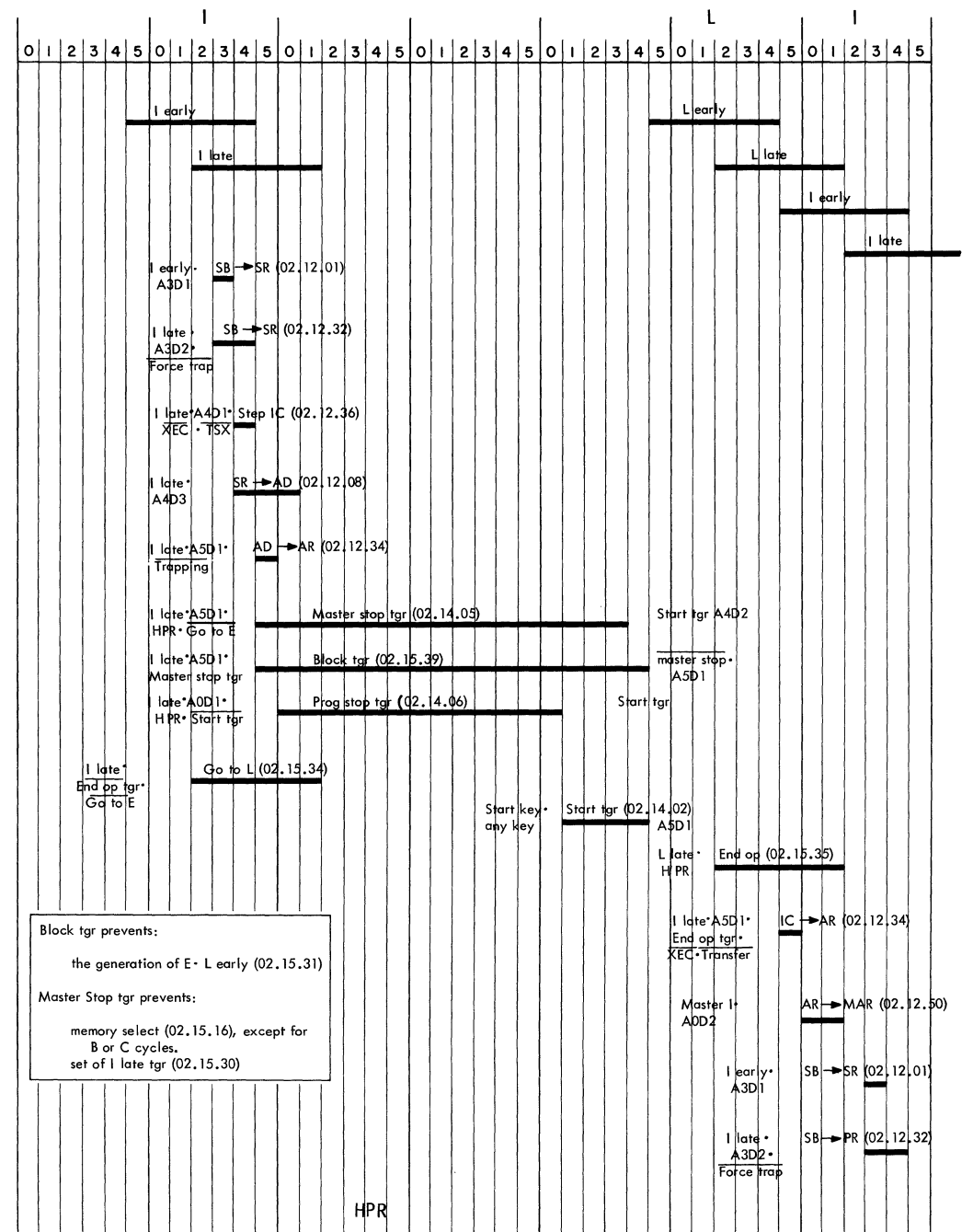
Halt and Proceed (HPR +0420)

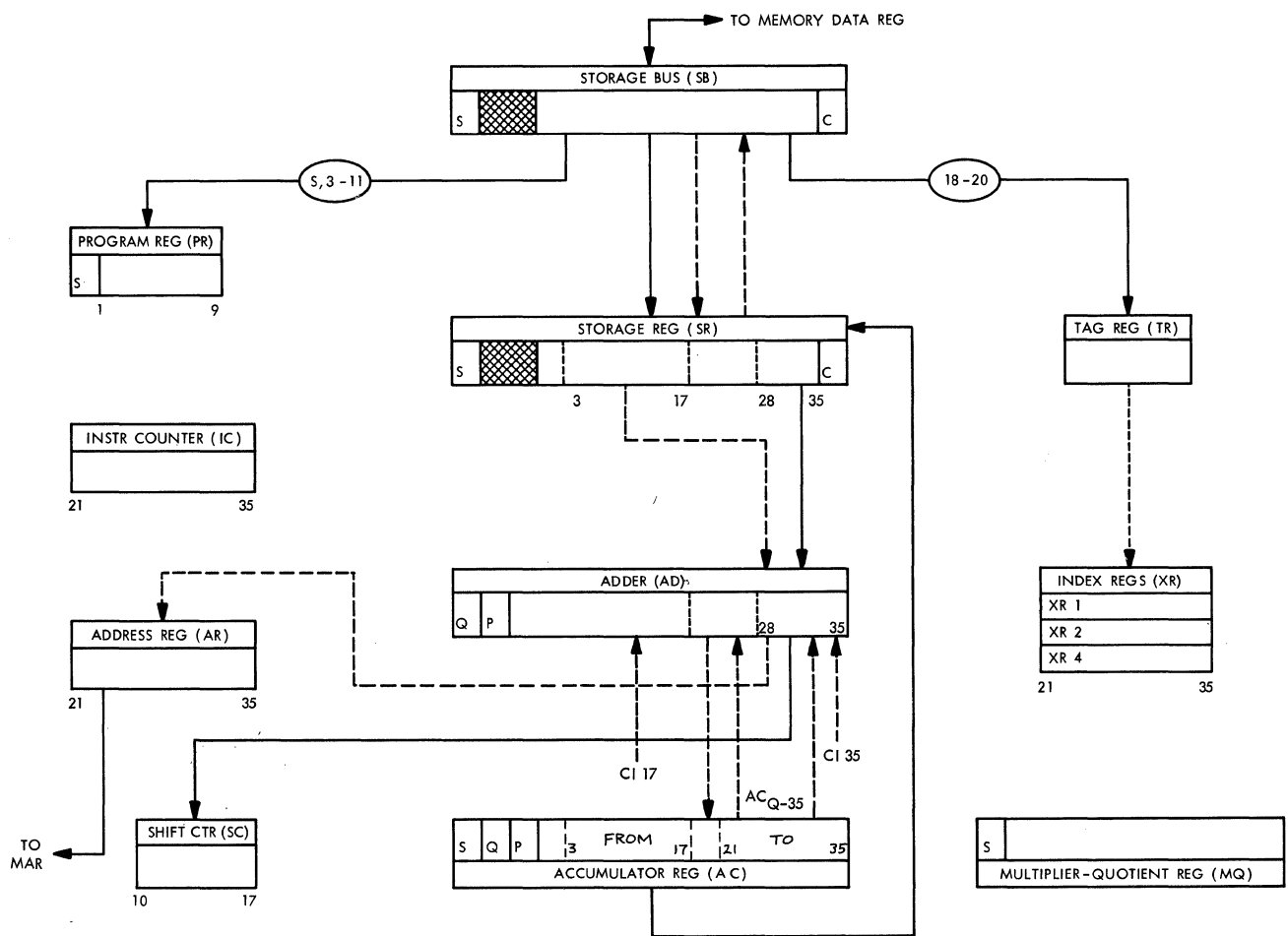
This instruction stops the computer. The instruction counter contains the location of the next instruction. When the start key is pressed, the computer proceeds with the next instruction.



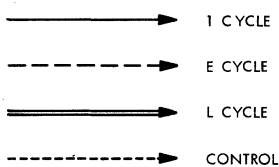
* FIRST CELL DRIVER PULSE FOLLOWING THIS INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

FIGURE 50. HPR





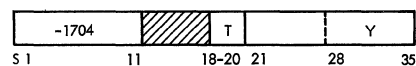
LEGEND



XFRS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -1704--C TRANSMIT

ALPHA CODE: TMT CYCLES: I, (L) + 2N



SEQUENCE NOTES:

Set Protect Mode (SPM -1160)

Causes the field register to be set to the high-order seven positions of instruction word 21-35, and the count register to be set to instruction word 32-35. Count register position 32 determines the mode of protection (1 for trap on equal, 0 for trap on unequal). Count register positions 33-35 determine the number of high-order positions of the field register that are to be compared with any store address. An attempt to store into a protected area of memory results in a memory protect trap.

If the computer is already in the memory-protect mode when the SPM instruction is given, an instruction trap results, placing the location of the SPM instruction plus 1 in the address part of location 32. Bit 16 is set on (indicating a violation), protect-mode is turned off, and the computer takes its next instruction from location 33.

If SPM is given on a machine that does not have the memory-protect option, a no-operation results and the computer takes its next instruction from the next sequential location.

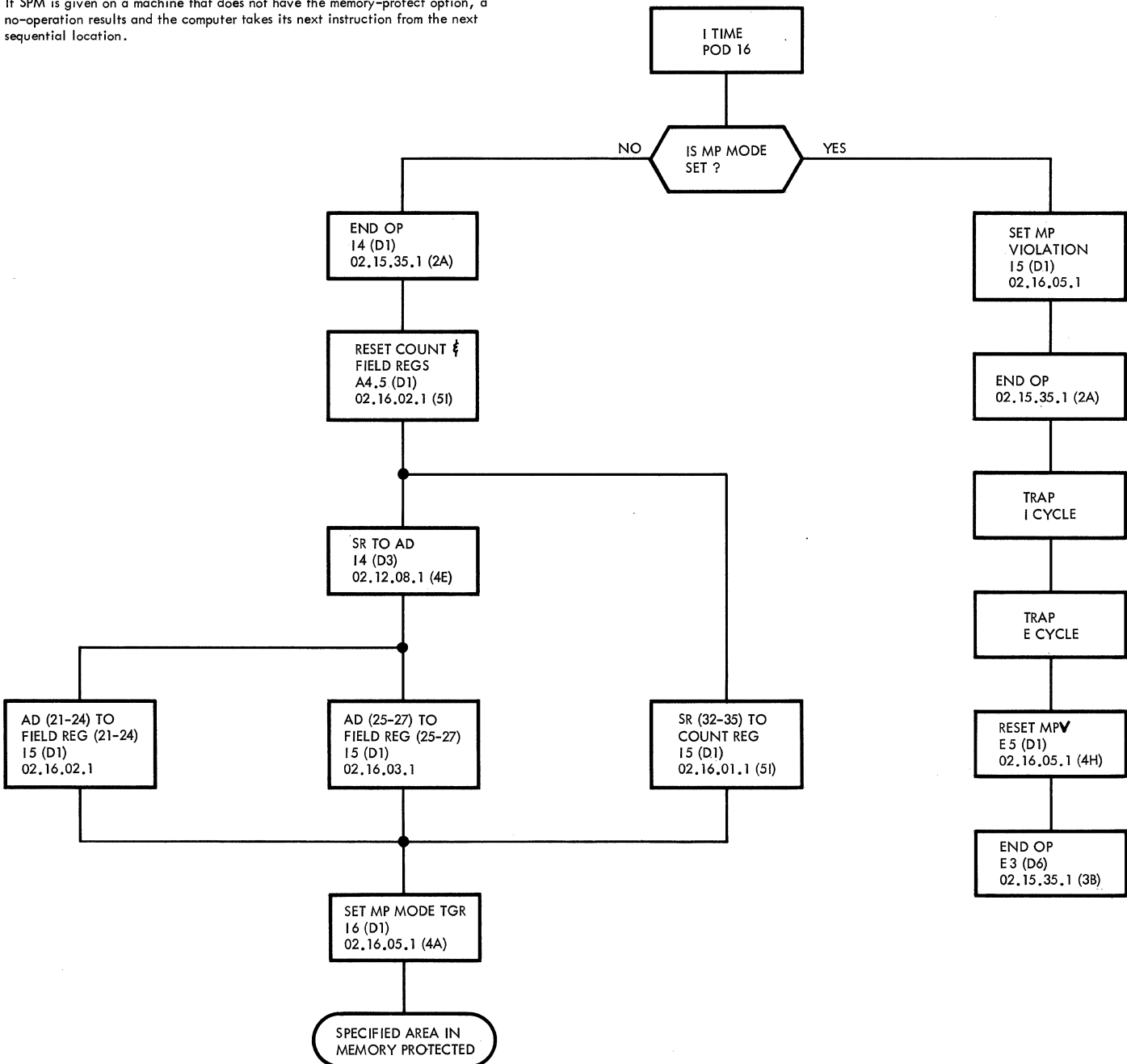
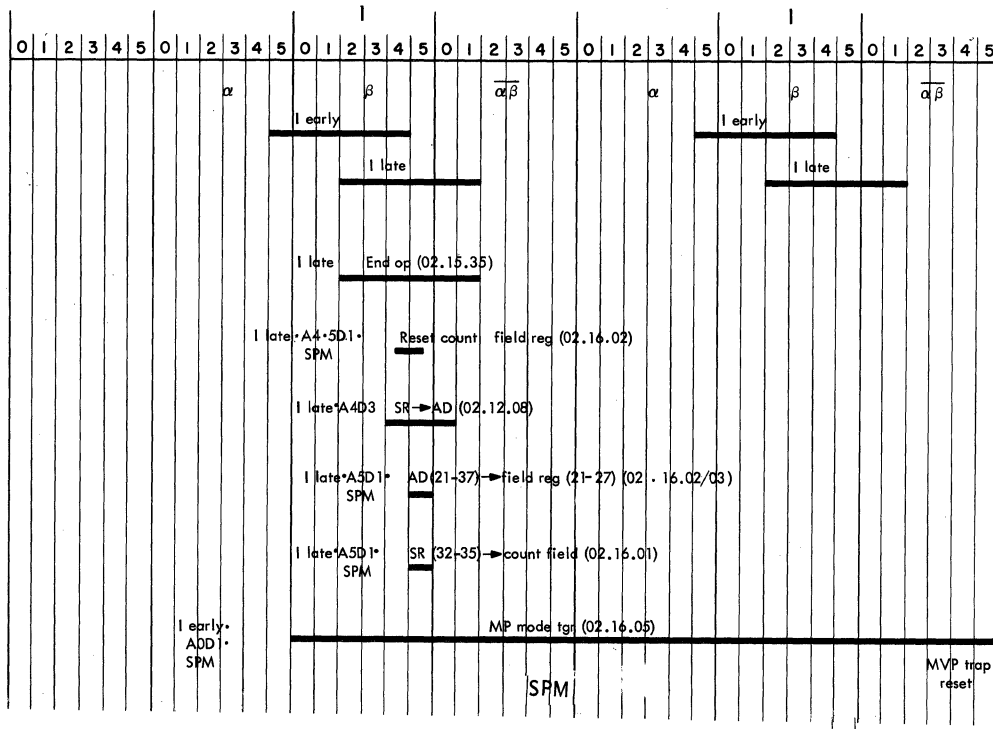


FIGURE 52. SPM



Location Switches	Inst	Tag	Address	Octal Equiv
00100	SPM		00000	516000 000000
00101	TRA		00104	002000 000104
00102				000000 000000
00103	TRA		00106	002000 000106
00104	SPM		00000	516000 000000
00105	HPR			042000 000000
00106	TRA		00100	002000 000100
00032				
00033	TRA		00106	002000 000106

CONSOLE INDICATORS																						
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S' 1-35)	ACCUMULATOR (S' 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S' 1-35)	TALLY COUNTER	MEMORY PROTECT	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	P CARRY	P OVERFLOW	FP 1	FP 2
I	I	00100	+020	000	0	00100	002000000100															
I	I	00101	-160	000	0	00101	516000000000				0											
I	I	00102	+020	000	0	00104	002000000104				1											
I	I	00105	-160	000	0	00105	516000000000				1											
I	E	00105	000	000	0	00032	042000000000				1											
E	I	00105	000	000	0	00033	000002000105				0											
I	I	00034	+020	000	0	00106	002000000106				0											
I	I	00107	+020	000	0	00100	002000000100				0											

Release Protect Mode (RPM -1004)

If the computer is in memory-protect mode, this instruction turns the memory-protect mode off and traps to location 32 (sets bit 15). If the computer is not in memory-protect mode, this instruction traps to location 32 and sets bit 14. In either case, the computer takes its next instruction from location 33.

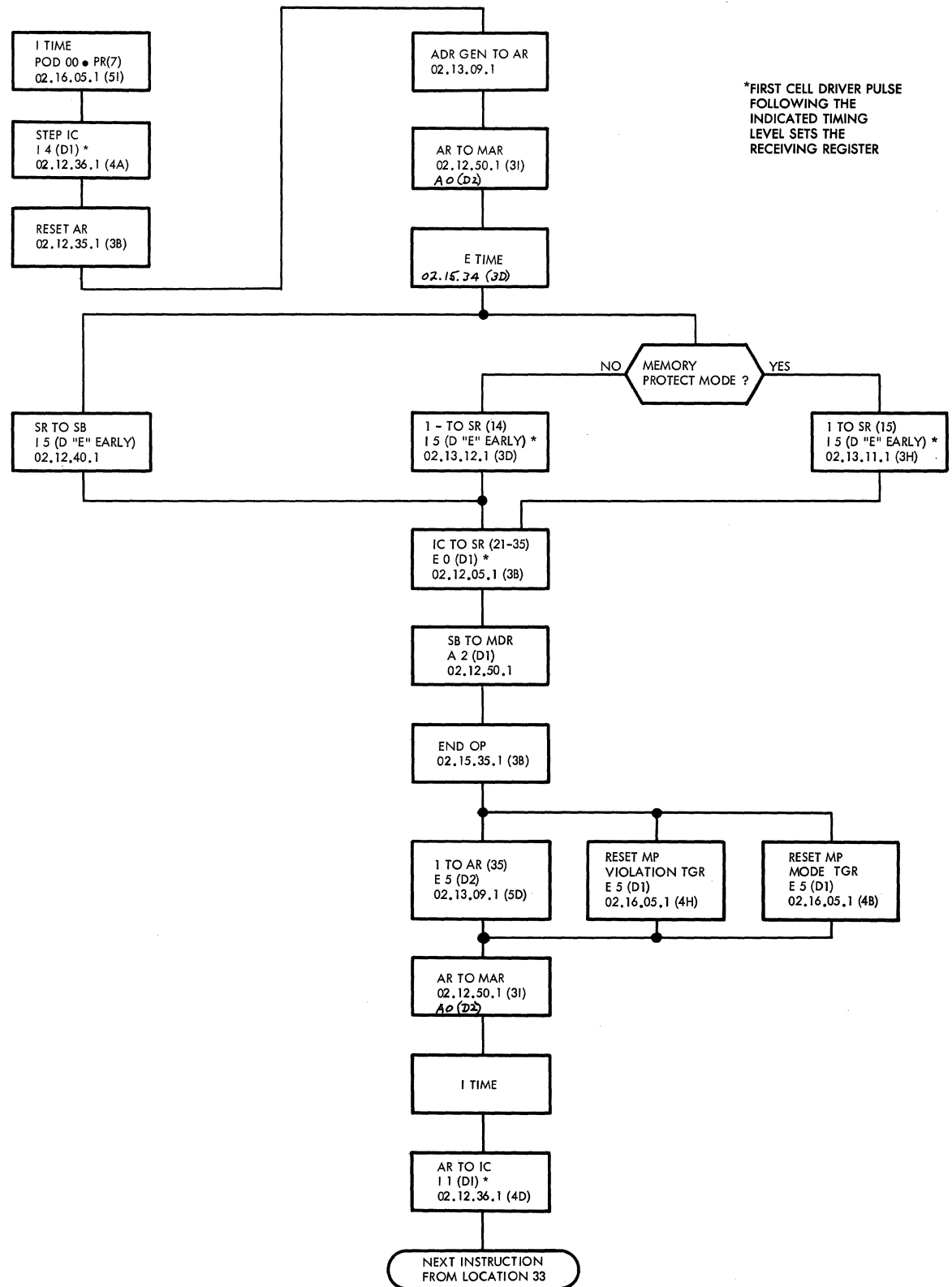
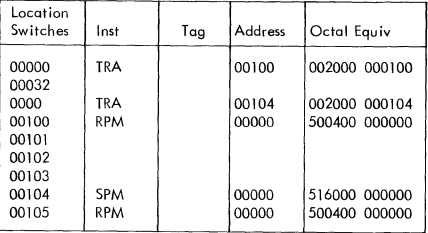


FIGURE 53. RPM

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This instruction is used to test the status of the end-of-tape trigger in Channel A. If the trigger is on, the computer resets the trigger and takes the next sequential instruction. If the EOT trigger is off, the computer skips the next instruction. The end-of-tape trigger is turned on when a write select, write end of file, or write blank tape causes the end-of-tape marker to be sensed.

An end-of-tape condition on any of the channels B-E can be tested by executing ETT (-0760) with the proper channel selected.

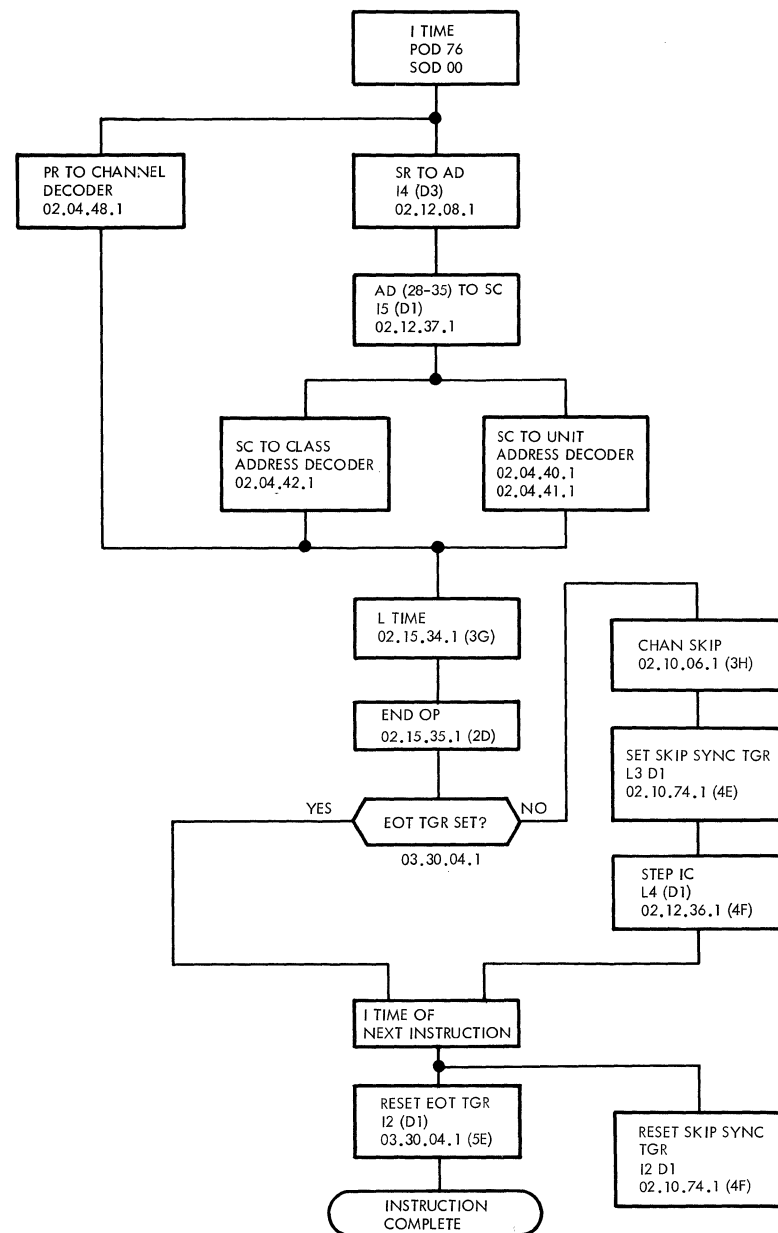
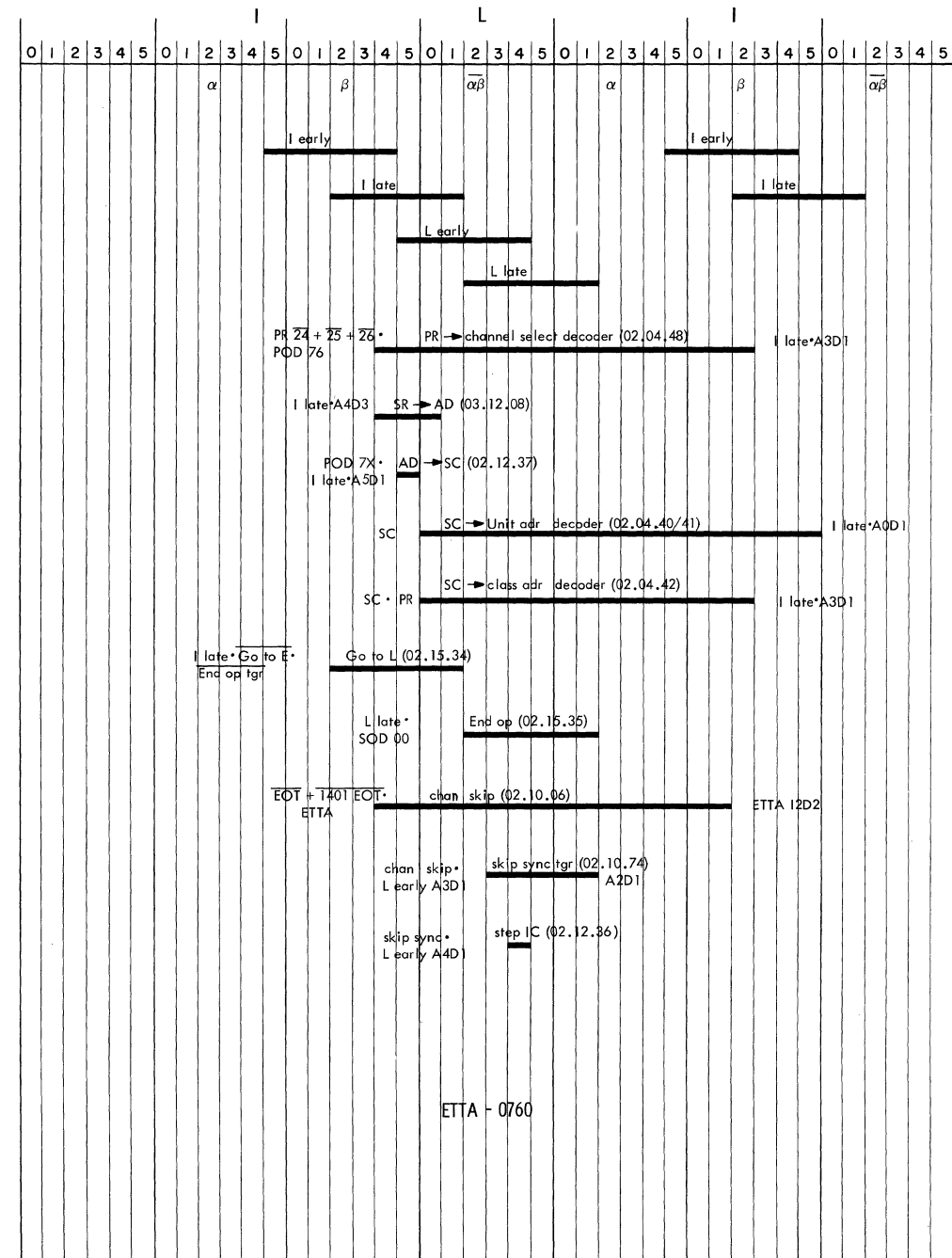


FIGURE 54. ETTA



Input-Output Check Test (IOT +0760 ... 0005)
If the I/O check indicator is on, the indicator is turned off and the computer takes the next sequential instruction. If the indicator is off, the computer skips the next instruction.

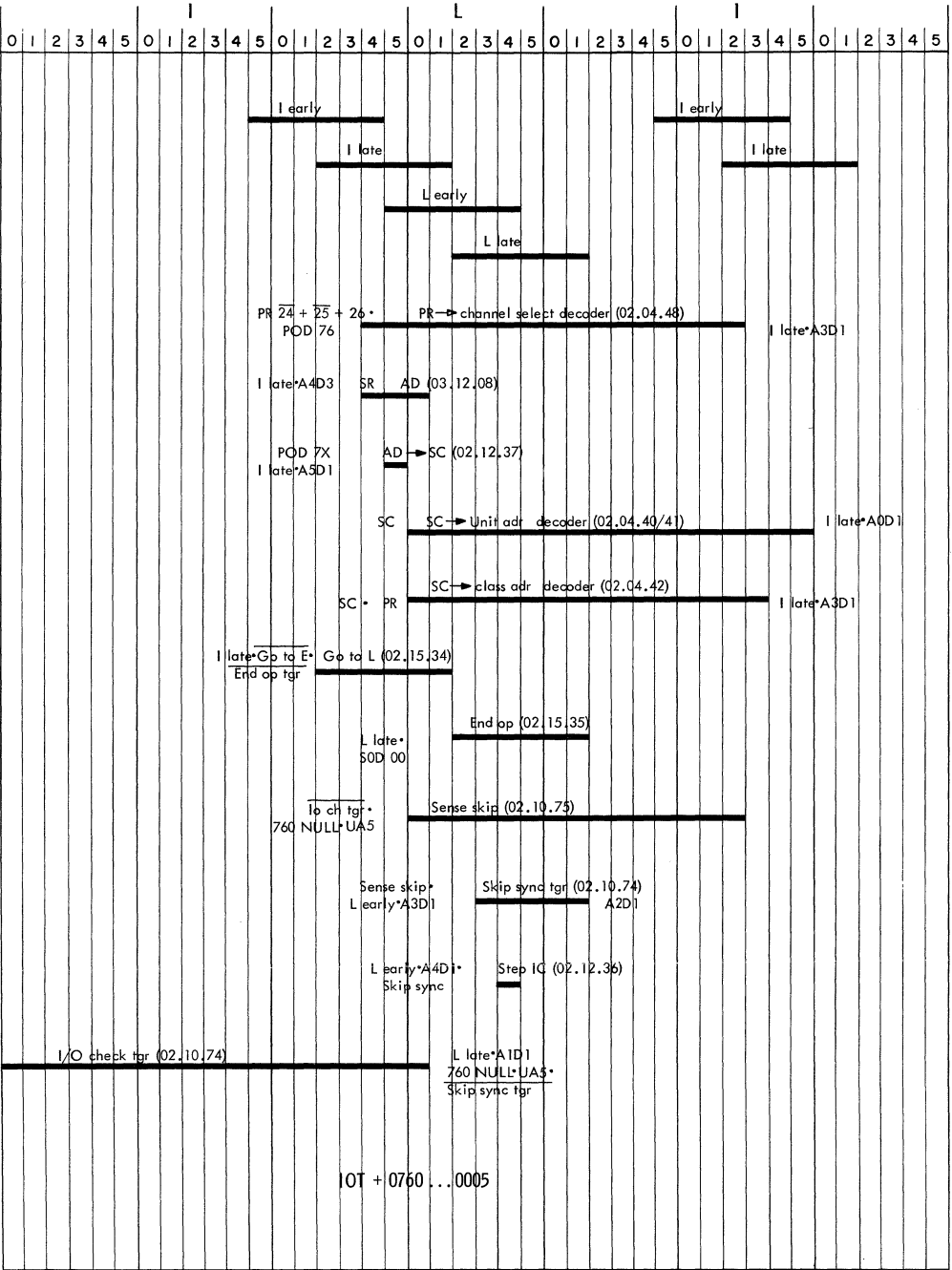
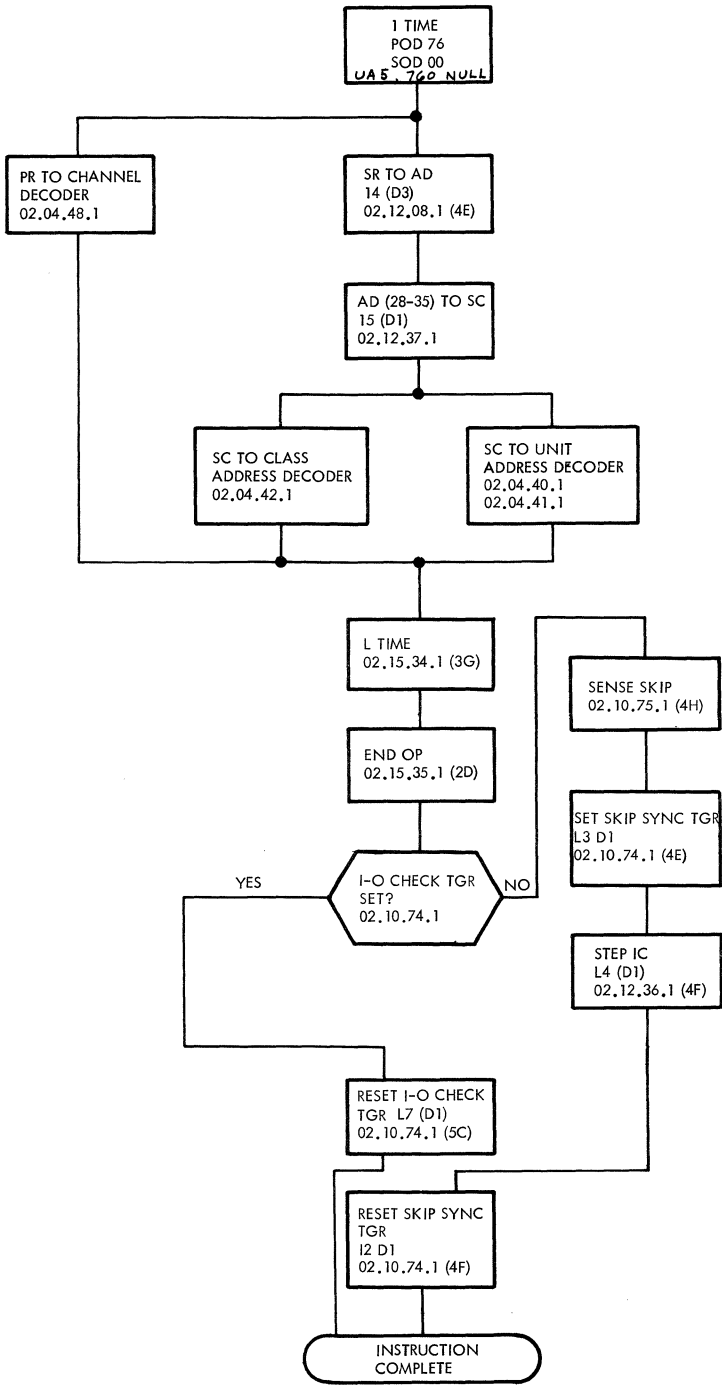


FIGURE 55. IOT

If the channel-in-use indicator is on for the specified channel, the computer takes its next instruction from the location specified by the address portion of the instruction word. If the channel-in-use indicator is off, the computer takes the next sequential instruction.

001	Reader
010	Punch
011	Printer
100	Typewriter
101	1401

The TDOA instruction will always transfer if channel A is in use, regardless of the status of the device specified.

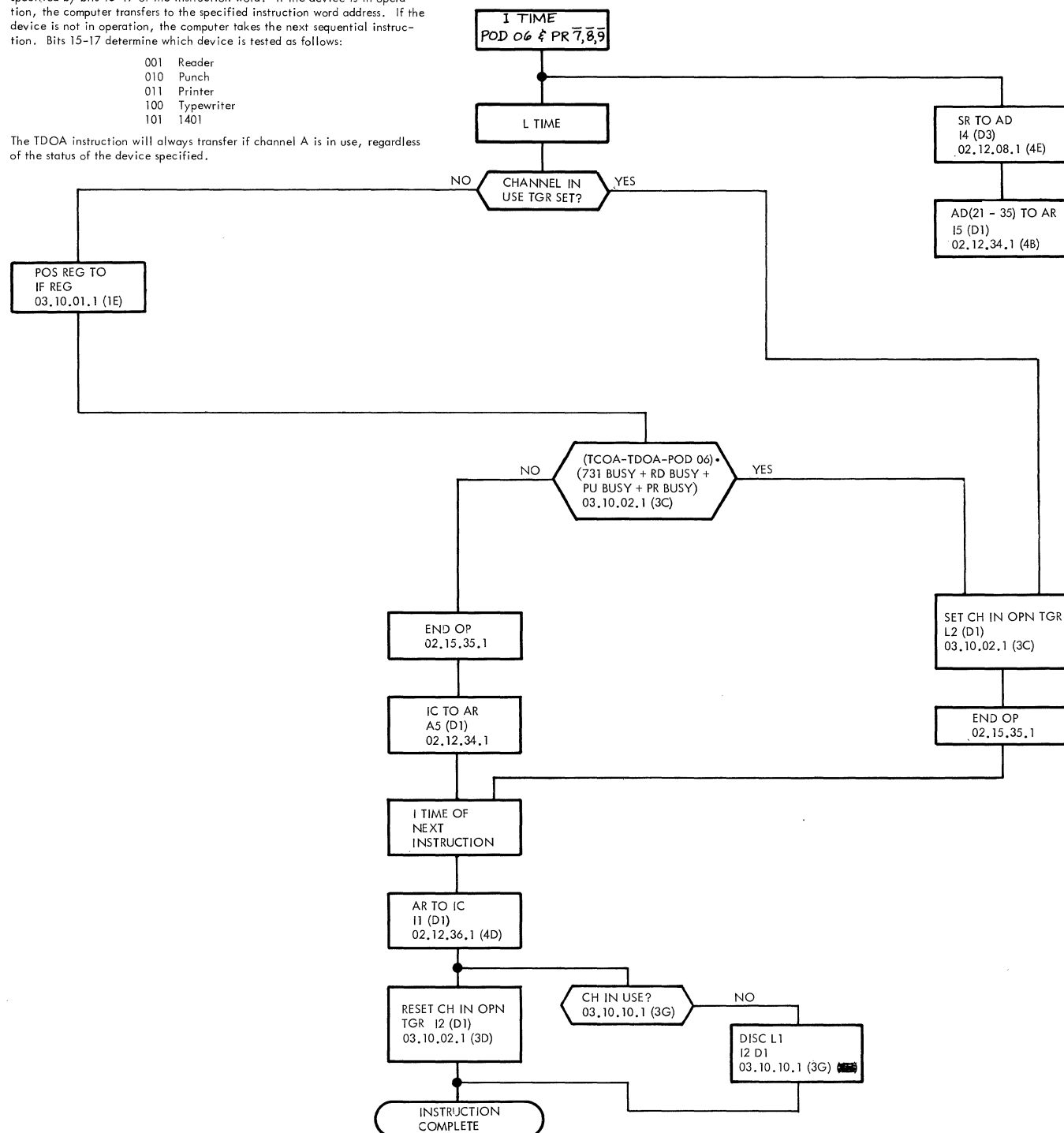
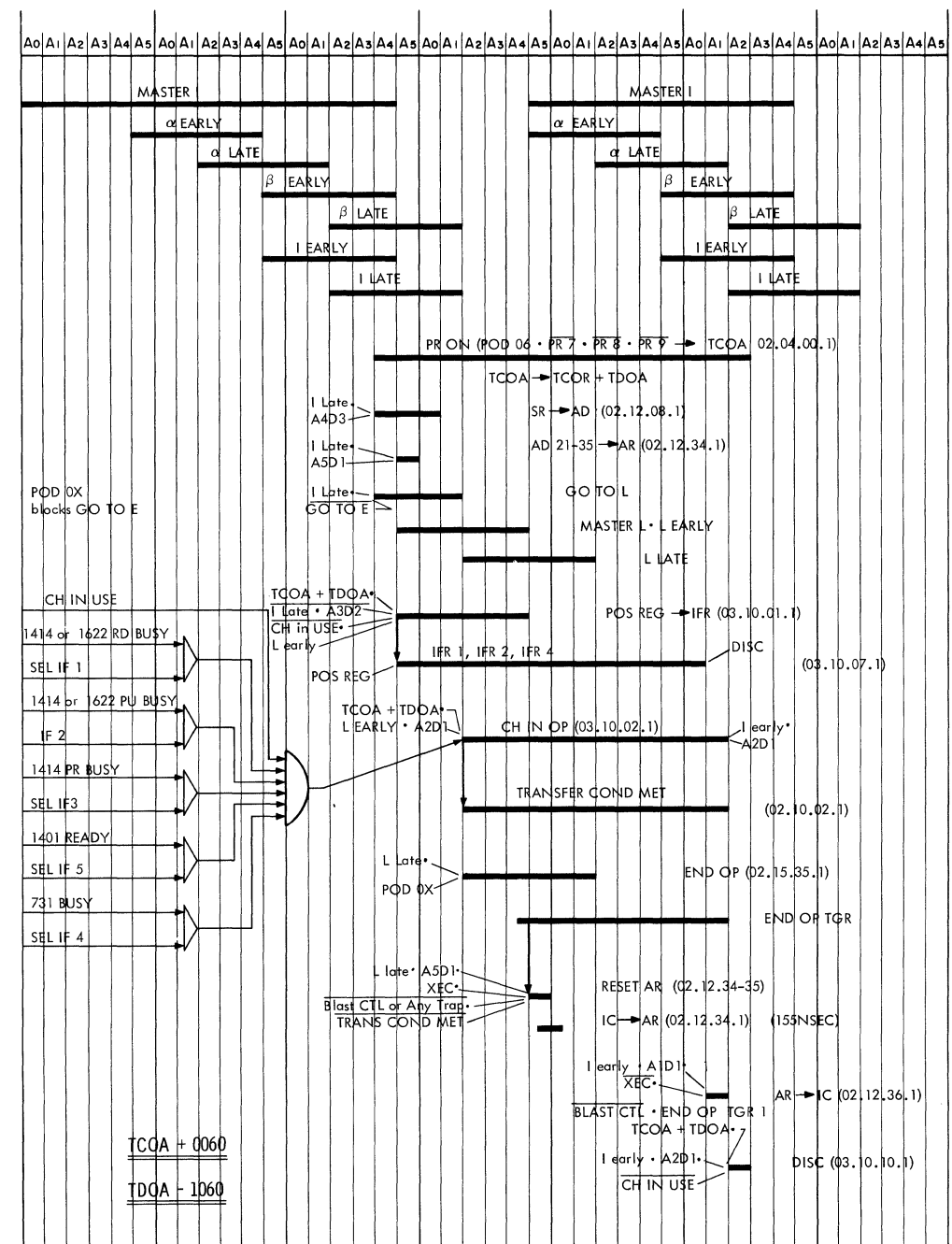


FIGURE 56. TCOA,TDOA



Transfer on Redundancy Check (TRCA +0022)
(TRCB -0022)
(TRCC +0024)
(TRCD -0024)
(TRCE +0026)

If the redundancy-check indicator for the specified channel is on, it is turned off and the computer takes its next instruction from the address portion of the instruction word. If the indicator is off, the computer takes the next sequential instruction.

If channel parity is enabled, the TRC will not transfer and will not turn the redundancy-check indicator off.

Transfer on End of File (TEFA +0030)
(TEFB -0030)
(TEFC +0031)
(TEFD -0031)
(TEFE +0032)

If the end-of-file indicator for the specified channel is on, it is turned off and the computer takes its next instruction from the address portion of the instruction word. If the indicator is off, the computer takes the next sequential instruction.

If channel end is enabled, the TEF will not transfer and will not turn off the end-of-file indicator.

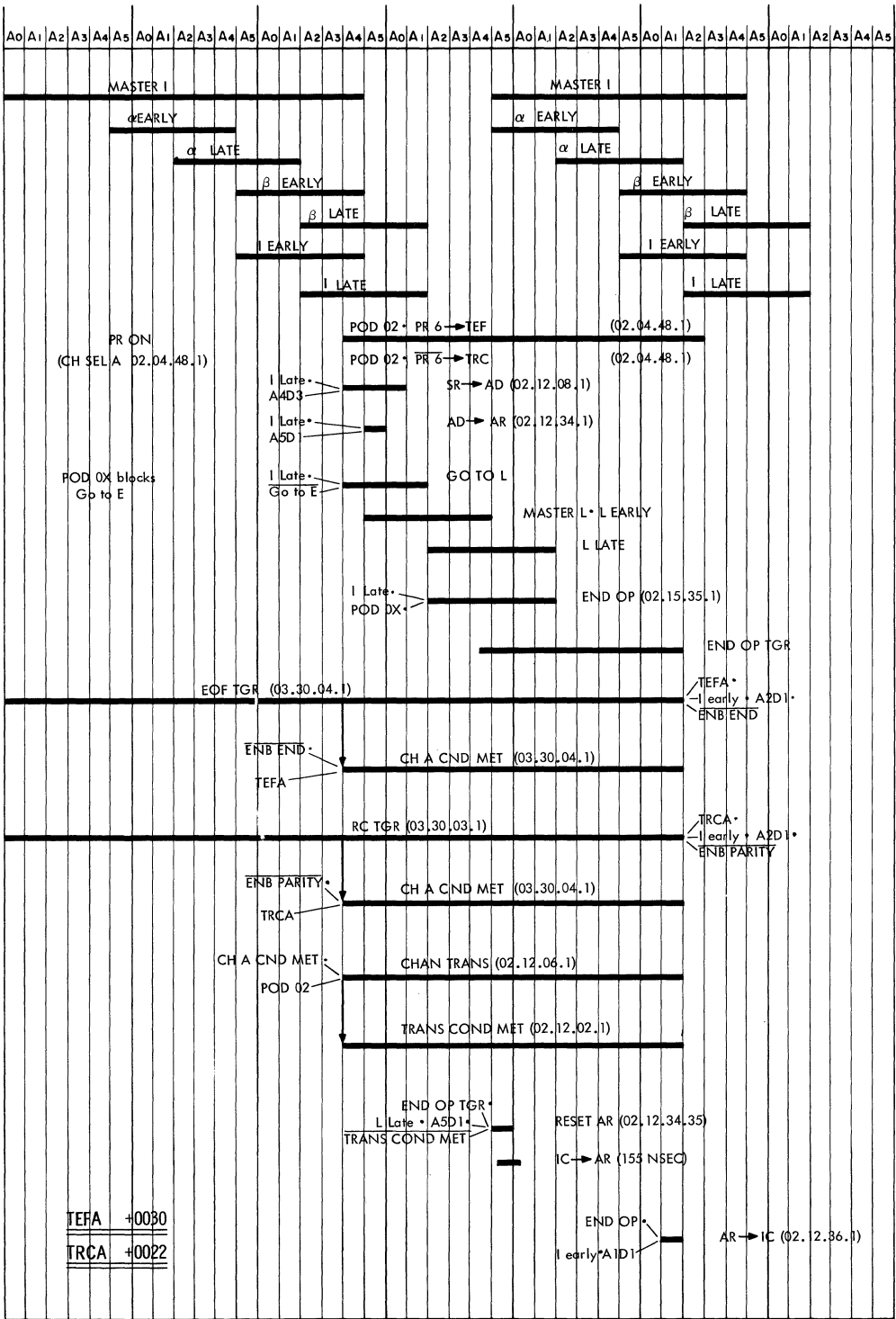
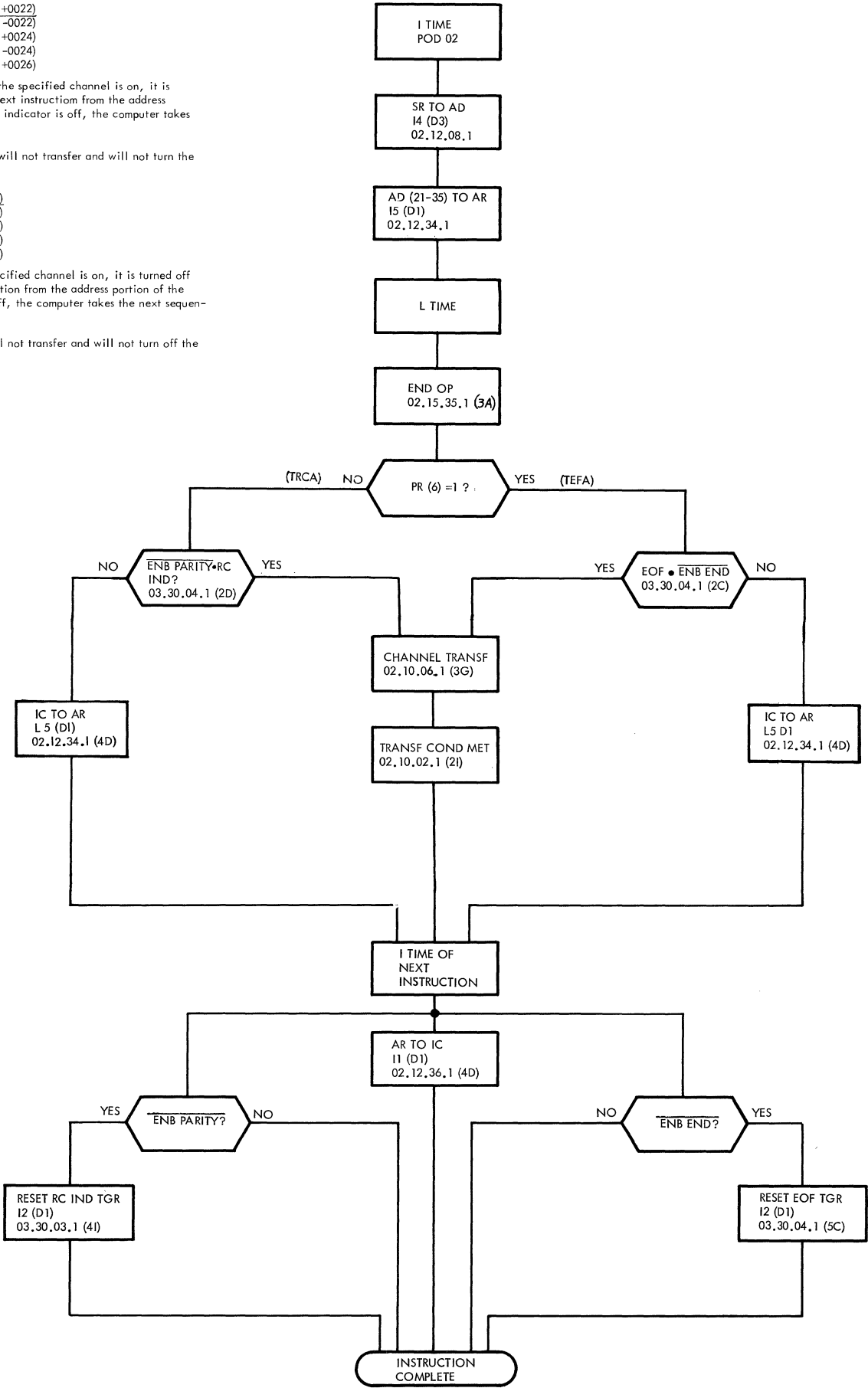
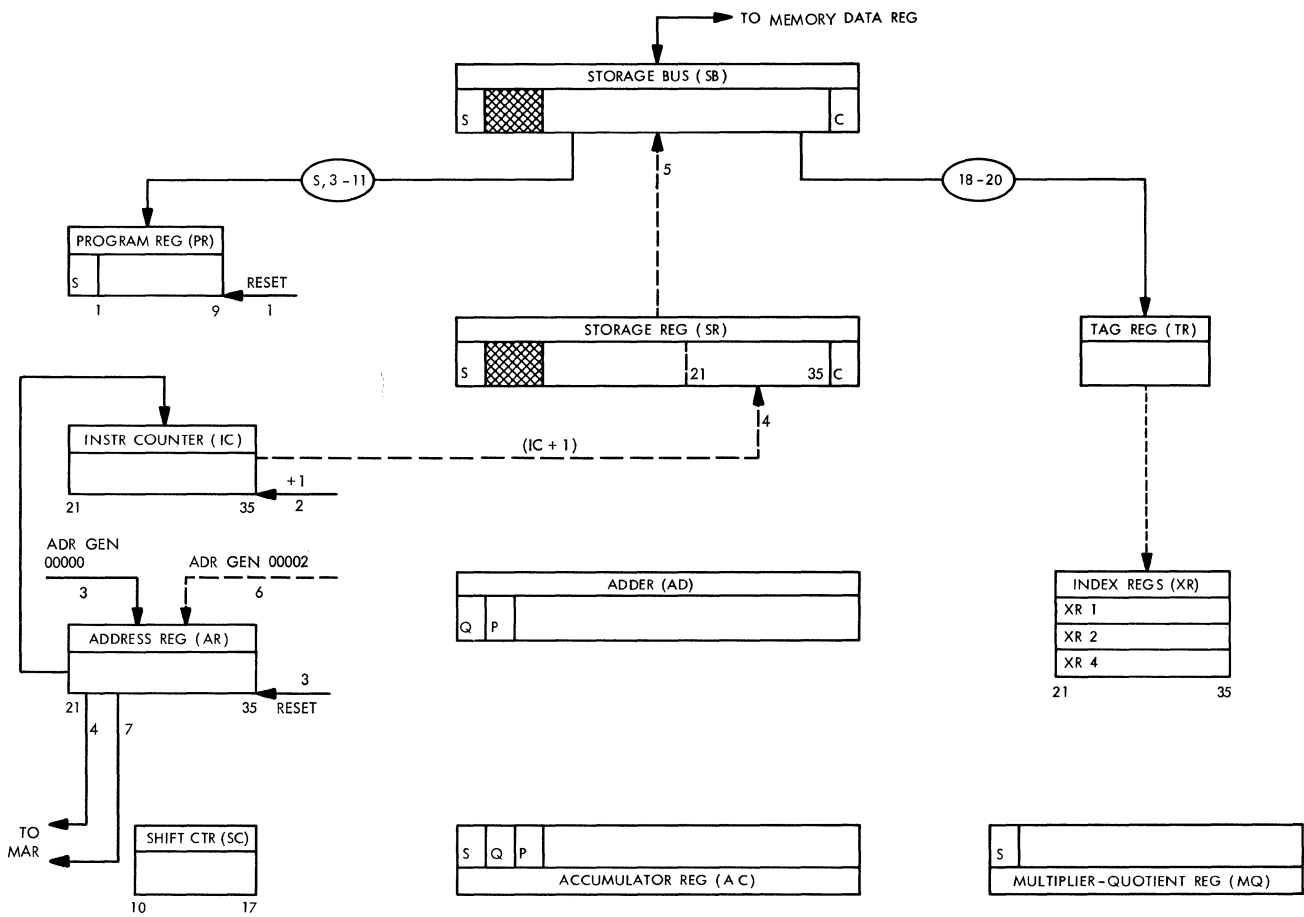
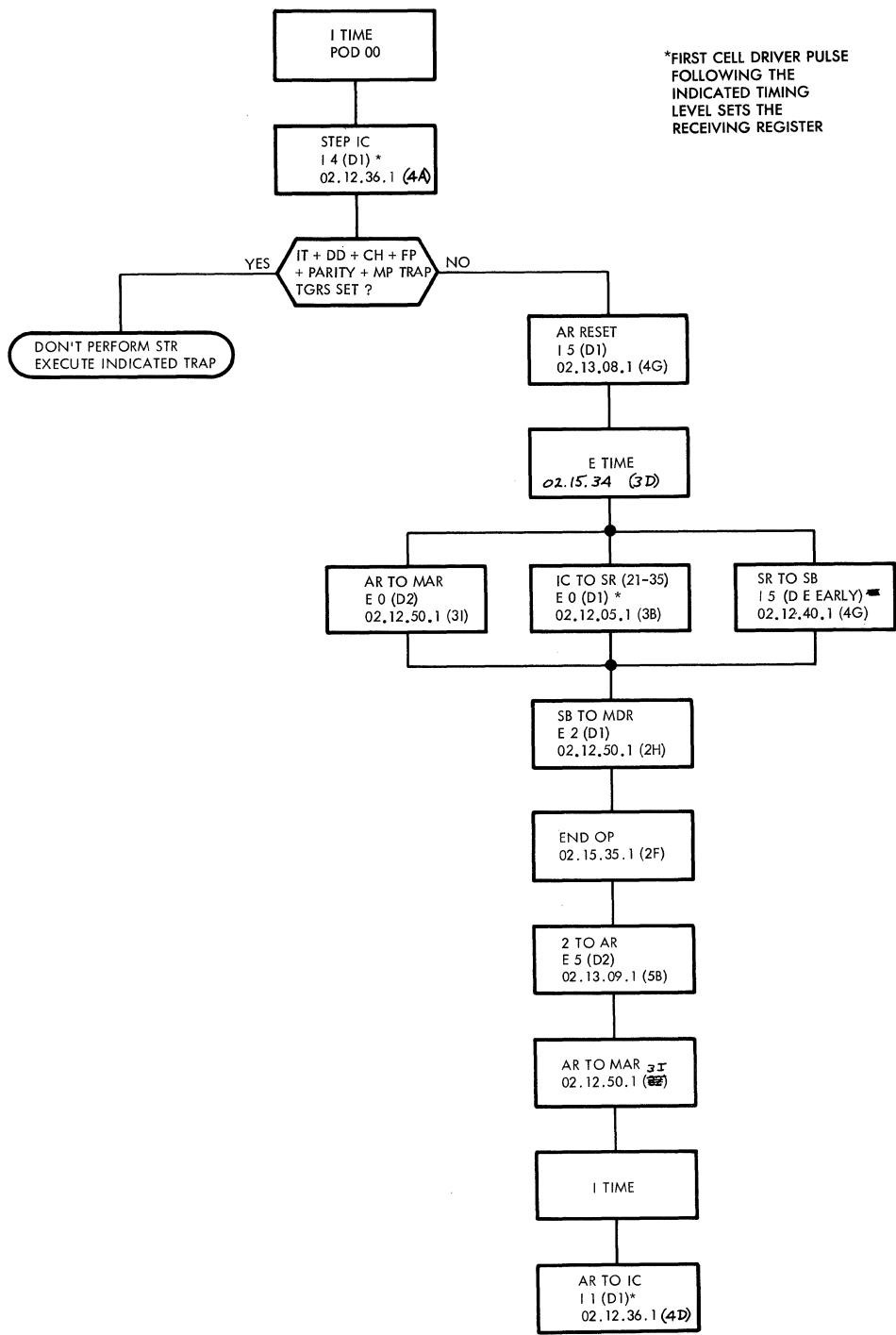


FIGURE 57. TRCA,TEFA

Store Location and Trap (STR -1000)
Execution of this instruction causes trapping to location 00000, where the instruction counter count (location of the STR plus 1) is stored in positions 21-35. The computer then transfers to location 00002. Bits 12-35 of the instruction word are not interpreted by the computer.



LEGEND

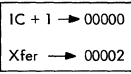
- I CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFRS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -1000 (+0000) STORE LOCATION AND TRAP
ALPHA CODE: STR CYCLES: I, E

SEQUENCE NOTES:
THE LOCATION OF THE STR INSTRUCTION + 1 IS PLACED IN C(00000)21-35.
C(00000)5-20 ARE CLEARED.
THE COMPUTER TRANSFERS TO LOC 00002.

FIGURE 58. STR

[illegible]

Transfer and Restore Traps (TRT -1164)
Turns on the trap-control trigger. The computer transfers to the location specified by the address portion of the instruction word.

Transfer and Restore Parity and Traps (TRP -1165)
Turns on the trap-control and parity-mode triggers. The computer transfers to the location specified by the address portion of the instruction word.

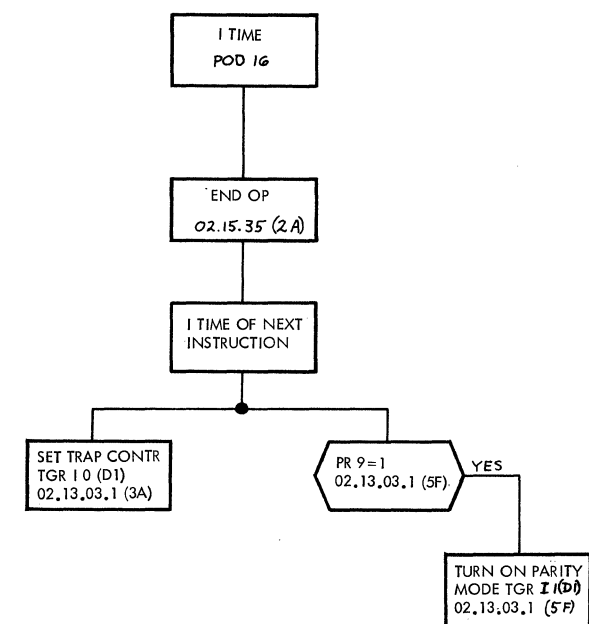


FIGURE 59. TRT,TRP

Enable from Y (ENB +0564)
The contents of Y (location specified by address portion of instruction word) are used to set the channel mask bits to 1 or 0. Execution of each enable instruction cancels the effect of previous enable instructions. The enable instruction turns on channel trap control.

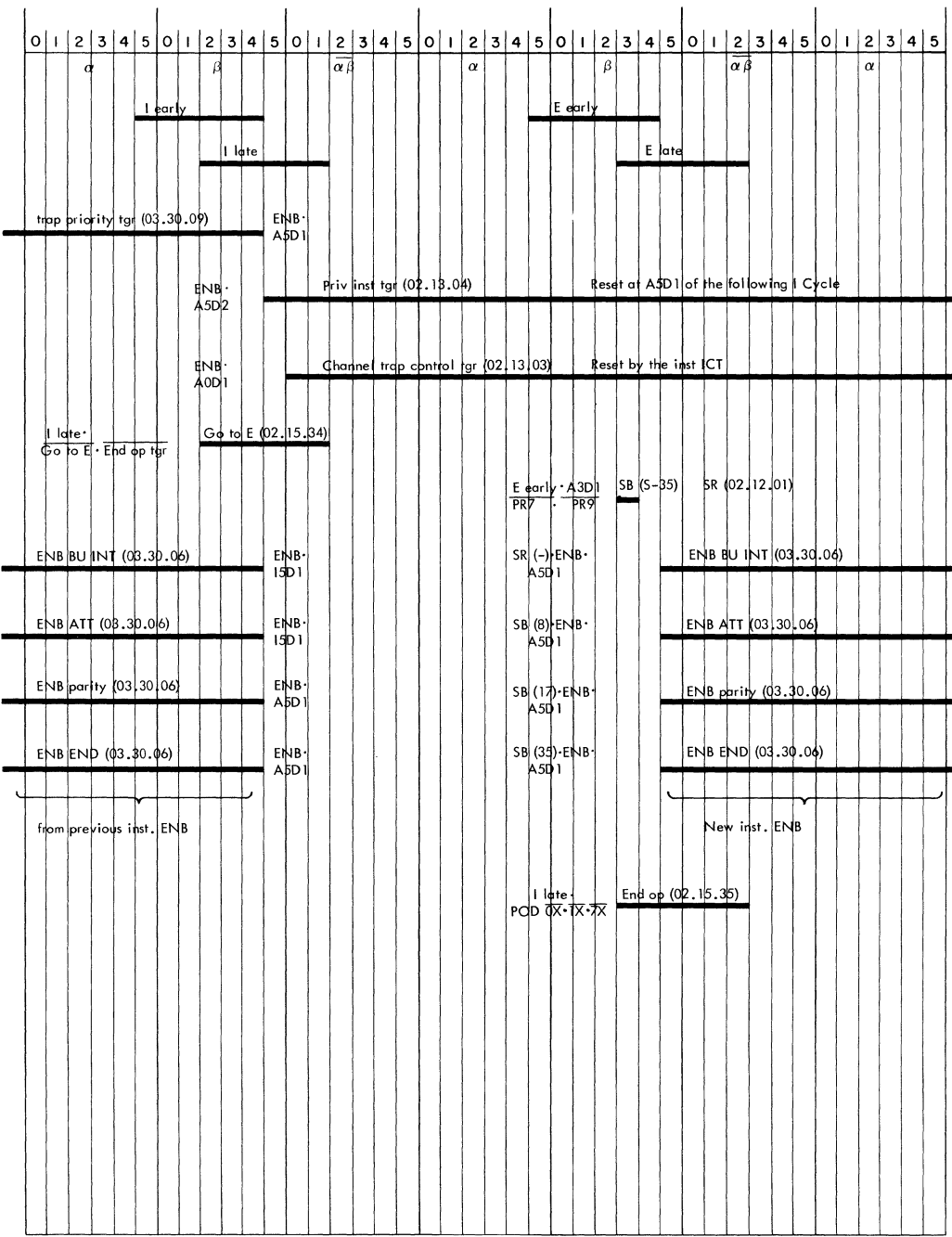
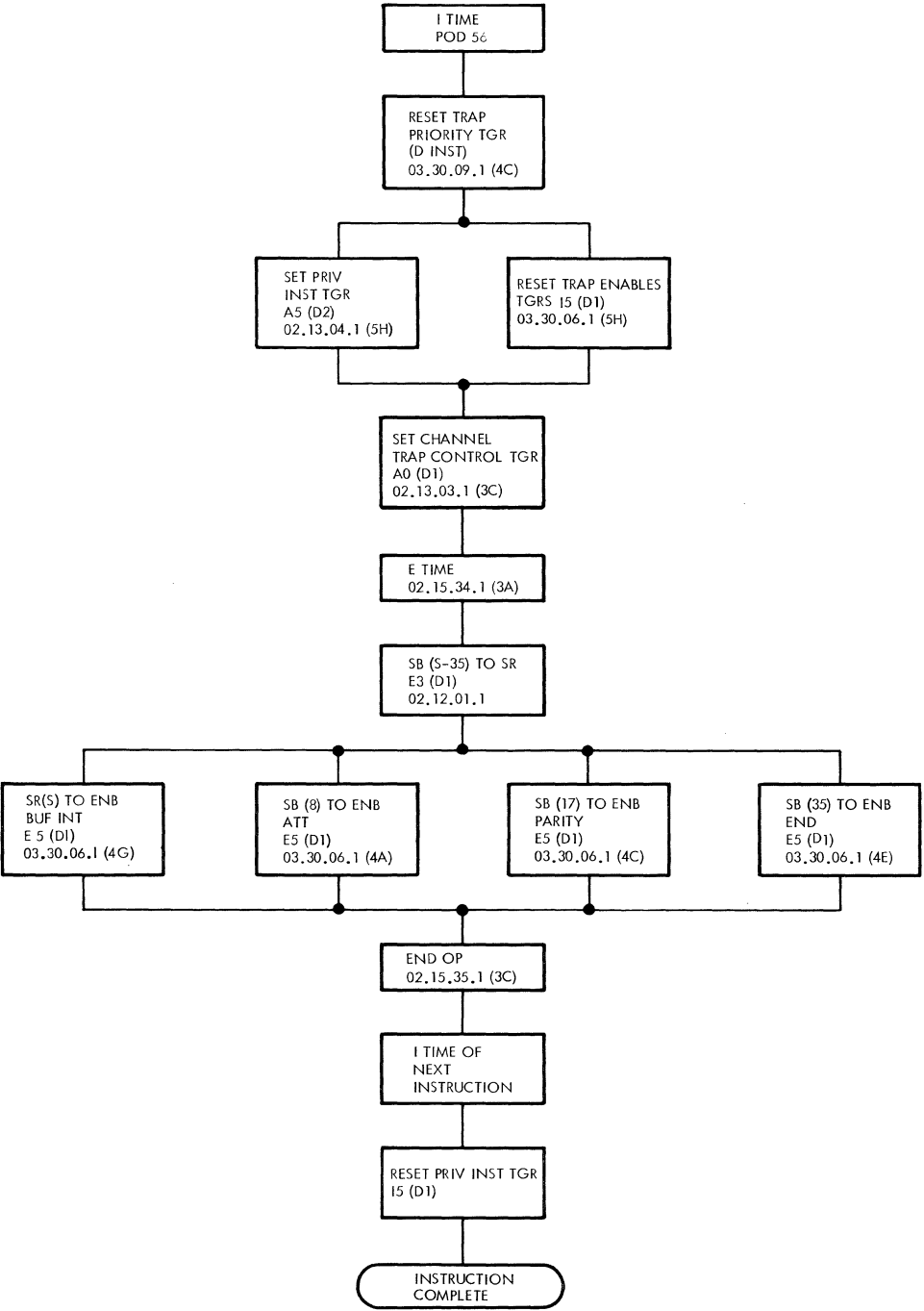


FIGURE 60. ENB

Restore Channel Traps (RCT +0760 ... 0014)
Turns on channel trap control. This allows traps to occur as specified by the previous enable instruction. It cancels the inhibiting effect of an executed trap or an ICT instruction.

Inhibit Channel traps (ICT +1760 ... 0014)
Turns off channel trap control. This inhibits all channel traps and direct data traps until an RCT instruction or a new ENR instruction is given.

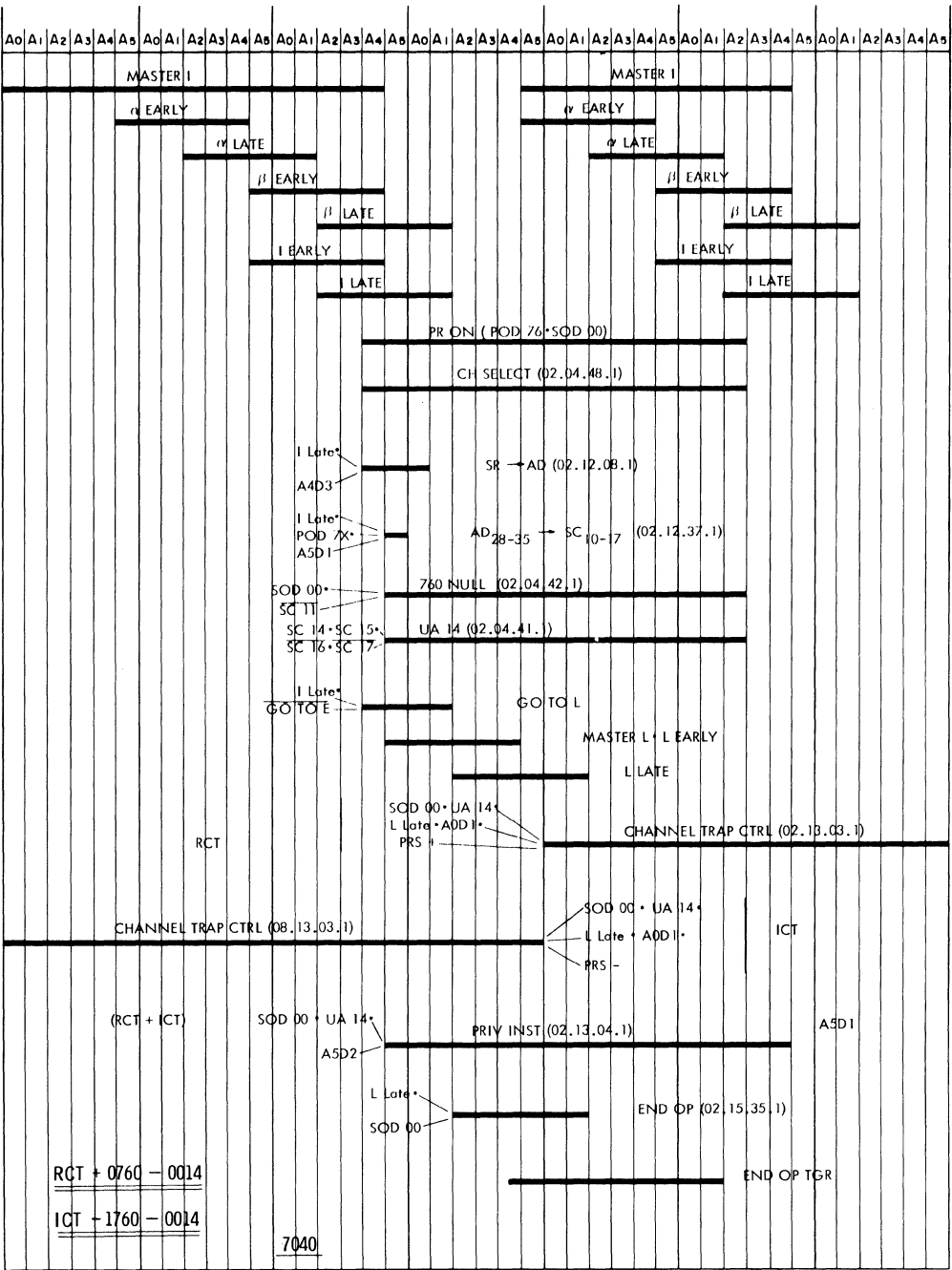
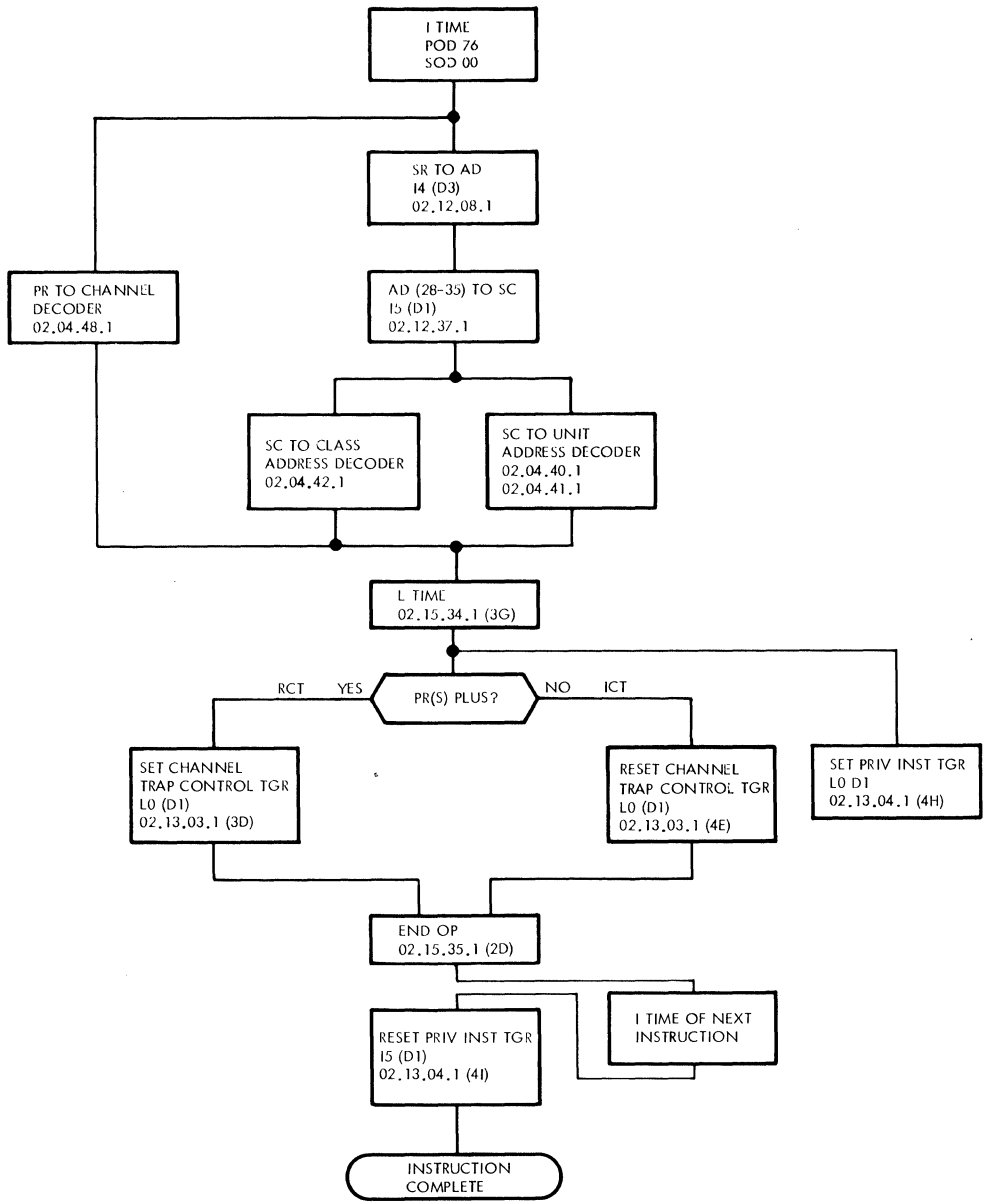


FIGURE 61. RCT,ICT

COMMENT SHEET

IBM 7040-44 CENTRAL PROCESSING UNIT

PRELIMINARY CUSTOMER ENGINEERING REFERENCE MANUAL, FORM R23-2659

FROM

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Your comments regarding this manual will help Product Publications increase the value of future reference manuals. Please consider the following questions and mail this form.*

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If not, why?
2. Have the programs and their associated indicator charts helped you fix any troubles?
3. Have the timing charts helped you fix any troubles?
4. General comments:

FOLD

FOLD

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