INFORMATION NOTE

N° 10204AERRA

Dear Customer,

With this INFINEON Technologies Information Note we would like to inform you about the following

MC-ISAR_AS422 Release Notes Addendum V4.0 affecting products TC3xx

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INFORMATION NOTE

N° 10204AERRA

MC-ISAR_AS422 Release Notes Addendum V4.0 affecting products TC3xx

- **Products affected:** Please refer to attached affected product list 1_cip10204.

- **Detailed Change Information:**

Subject: MC-ISAR_AS422 Release Notes Addendum V4.0 affecting products TC3xx.

Reason: Update of the Release Note Addendum due to new known issues.

Description:

Old	New
■ Release Notes Addendum **Version 3.0**	■ Release Notes Addendum **Version 4.0** (for details please refer to 4_cip10204 attached).

- **Product Identification:** Not applicable (no change of product)

- **Impact of Change:** Assessment in Application required !

- **Attachments:**

Affected product list	1_cip10204
Release Notes Addendum Version 4.0	4_cip10204

- **Intended start of delivery:** Not applicable

If you have any questions, please do not hesitate to contact your local Sales office.

MC-ISAR_AS422_TC3xx

Release Notes Addendum

Version: v4.0 Released

Date: 2020-08-06

About this document

Scope and purpose

This release notes addendum (RNA) document lists all the issues identified in productive releases of the MC-ISAR_AS422_TC3xx product. Issues reported on or before 2020-07-16 are considered in this version, including safety topics / anomalies.

Note: Issues and safety anomalies known at the time of release are documented in release notes and safety case. Integrators are required to take them into consideration in addition to the issues listed in this document.

Table 1 Production Releases (PR) covered

HW Devices	SW Package names	Release Date	Release quality	Release number
TC39xB TC38x	MC-ISAR_AS42x_AURIX2G_TC38xA_TC39xB_BASIC_1.10.0.zip MC-ISAR_AS42x_AURIX2G_TC38xA_TC39xB_CD_1.10.0.zip MC-ISAR_AS42x_AURIX2G_TC38xA_TC39xB_COM-E_1.10.0.zip MC-ISAR_AS42x_AURIX2G_TC38xA_TC39xB_DEMO_1.10.0.zip	2019-03-27	PR	1.10.0
TC39xB TC38x TC37xEXT TC37xPD TC35x	MC-ISAR_AS42x_TC3xx_BASIC_1.30.0.zip MC-ISAR_AS42x_TC3xx_CD_1.30.0.zip MC-ISAR_AS42x_TC3xx_COM-E_1.30.0.zip MC-ISAR_AS42x_TC3xx_DEMO_1.30.0.zip	2019-10-24	PR	1.30.0
TC39x TC38x TC37x TC37XEXT TC35x TC36x TC33XEXT TC33x TC32x	MC-ISAR_AS42x_TC3xx_BASIC_1.40.0.zip MC-ISAR_AS42x_TC3xx_CD_1.40.0.zip MC-ISAR_AS42x_TC3xx_COM-E_1.40.0.zip MC-ISAR_AS42x_TC3xx_DEMO_1.40.0.zip	2020-05-29	PR	1.40.0

Intended audience

This document is intended for anyone using the MC-ISAR_AS422_TC3xx, also referred as MCAL SW.

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1 Known issues v4.0

1.1 Can_17_McmCan

1.1.1 0000053912-11728

Issue description: Each CAN kernel has a dedicated message RAM shared between the controllers associated with the kernel. The message RAM associated with each kernel has a start and end boundary. The RX and TX hardware object configuration associated with the hardware objects should take care that this message RAM boundary is not exceeded. However in case the message RAM end address of one kernel overlaps with that of another, there is no error message flagged during generation of code. Hence the configuration errors result in an overlap of message RAM boundaries leading to mismatched hardware object configuration.

Impact: The user shall not know that an incorrect configuration has been made and the message RAM boundaries have overlapped.

Work around: The user shall ensure by checking the generated files the start and end addresses of the message RAM for each kernel.

Impacted Release(s): 1.30.0

1.1.2 0000053912-10616

Issue description: In CAN driver uses references of MCU parameters. The DESTINATION-REF path has an incorrect reference of AUTOSAR for IFX specific parameters. This reference should be AURIX2G.

Impact: Incorrect BMD reference path leading to schema violations.

Work around: No workaround.

Impacted Release(s): 1.30.0

1.2 CanTrcv_17_V9251

1.2.1 0000053912-12336

Issue description: In tresos, option to add new element is not available in CanTrcvWaitTime and CanTrcvTimerType containers.

Impact: User is not able to add the elements in CanTrcvWaitTime and CanTrcvTimerType containers.

Work around:
While creating tresos project, if the option "Automatically add the minimum number of child elements in lists" is enabled, issue is resolved.

Impacted Release(s): 1.40.0

1.3 Crc

1.3.1 0000053912-8823

Issue description: SMC[SW]:FCE:CRC_CFG safety measure to be handled by integrator.

Impact: No impact to CRC driver. User shall implement the safety measure described in SMC[SW]:FCE:CRC_CFG.

Work around:
Integrator/User shall compare the expected CRC and the calculated CRC provided by CRC driver. If mismatch in CRC results, integrator/user shall take appropriate actions.

Impacted Release(s): 1.10.0, 1.30.0, 1.40.0

1.4 Dma

1.4.1 0000053912-12349

Issue description: Incorrect documentation of ASIL level for Dma_ChInterruptHandler() and Dma_MEInterruptDispatcher().

Impact: No functional impact. ASIL level for Dma_ChInterruptHandler() and Dma_MEInterruptDispatcher() should be ASIL B, instead of QM.

Work around:
Customer shall treat the ASIL level of Dma_ChInterruptHandler() and Dma_MEInterruptDispatcher() as ASIL B.

Impacted Release(s): 1.10.0, 1.30.0, 1.40.0

1.5 Eth_17_GEthMac

1.5.1 0000053912-11663

Issue description:

As per GETH_TC.P001, Ethernet frequency operating range changed to 100 - 150 MHz from 150 - 200 MHz.

Impact: User can configure wrong operation conditions for Ethernet frequency if > 150 MHz and may impact the Ethernet IP functionality.

Work around:

User shall configure Ethernet Frequency only as 150MHz.

Impacted Release(s): 1.10.0, 1.30.0

1.6 Fee

1.6.1 0000053912-12347

Issue description:

When NVM block read request is made while QS block erase is ongoing in the hardware and if suspending the ongoing erase fails, then the NVM block read request will be rejected with E_NOT_OK along with DET error FEE_E_BUSY or Safety error FEE_SE_BUSY.

Impact: Unintended DET or safety error (FEE_E_BUSY\FEE_SE_BUSY) is reported.

Work around:

Do not use following combination of features together:

1. Both NVM and QS blocks are configured

2. Erase suspend feature is enabled

3. Safety errors or DETs are enabled

OR

Ignore FEE_E_BUSY or FEE_SE_BUSY in the above scenario based on E_NOT_OK returned by Fee_Read() API.

Impacted Release(s): 1.10.0, 1.30.0, 1.40.0

1.7 Fls_17_Dmu

1.7.1 0000053912-12506

Issue description: In the Example code presented in the user manual, the call to Fls_17_Dmu_Write () function is incorrect. The parameter pass to this function are not in the correct order.

Impact:

If the customer uses the same example mentioned in the user manual, then

1. If DET/Safety is enabled, FLS_17_DMU_E_PARAM_ADDRESS DET will be raised.

2. If DET/Safety is disabled then incorrect behavior will occur and may lead to trap.

Work around:

Refer to the prototype of API Fls_17_Dmu Write() as describe in user manual and pass the parameters in the order described.

Impacted Release(s): 1.10.0, 1.30.0, 1.40.0

1.7.2 0000053912-12152

Issue description:

Due to improper handling of OPER error in interrupt mode , driver may get stuck in busy state.

Pre-condition: FLS is configured in Interrupt mode and DET/Safety is disabled.

Impact: Driver will get stuck in busy state.

Work around:

User can use one of the following workaround.

Workaround 1: Enable DET/Safety , this will give the timeout DET notification. When user receive timeout notification, he can use Fls_17_Dmu_GetOperStatus to determine if an OPER has occurred. If OPER error has occurred, then user should initiate a system reset to clear the OPER error.

Workaround 2: User should implement a timeout mechanism. When timeout occurs, application should call Fls_17_Dmu_GetOperStatus to determine if an OPER has occurred. If OPER error has occurred, then user should initiate a system reset to clear the OPER error.

Impacted Release(s): 1.30.0

1.7.3 0000053912-12507

Issue description: FLS_E_PARAM_DATA is also reported when the SourceAddressPtr is not word aligned (4 byte aligned). This information is missing in the error handling description of Fls_17_Dmu_Write API.

Impact: User may not be able to find out the reason why FLS_E_PARAM_DATA DET is reported even when the SourceAddressPtr passed is not NULL.

Work around:

If FLS_E_PARAM_DATA DET is reported, user has to check whether the SourceAddressPtr passed is word-aligned and not NULL.

Impacted Release(s): 1.10.0, 1.30.0, 1.40.0

1.7.4 0000053912-12365

Issue description: When configuration parameter FlsIfxFeeUse is not enabled and if erase operation fails due to EVER error, runtime error FLS_17_DMU_E_ERASE_FAILED is not reported.

Impact: Run time error FLS_17_DMU_E_ERASE_FAILED is not reported.

Work around: User should use the job error notification to mean that erase failed.

Impacted Release(s): 1.10.0, 1.30.0, 1.40.0

1.8 General

1.8.1 0000053912-8815

Issue description: SMC[SW]:SCU:ERU_CONFIG ESM is not supported by MCAL.

Impact:

SMC[SW]:SCU:ERU_CONFIG ESM is not supported by MCAL and wrongly documented in MCAL User manual. This may cause confusion to integrator.

Work around:

Customer shall implement the SMC[SW]:SCU:ERU_CONFIG ESM if required for their use case.

Impacted Release(s): 1.10.0, 1.30.0

1.8.2 0000053912-12030

Issue description: IRQ configuration not supported for Can_17_McmCan, Eth_17_GEthMac, I2c, Sent, Adc, Lin_17_AscLin and Uart modules.

Impact:

1) User cannot configure IRQ configurations for modules like Ethernet, CAN, VADC, I2C and ASCLIN.

Impacted devices are :

TC356_ADAS - ETH, ASCLIN, I2C, VADC, CAN

TC357_ADAS - ETH,ASCLIN,I2C,VADC,CAN

TC364_LQFP - ETH,ASCLIN,I2C,VADC,CAN

TC364_TQFP - ETH,ASCLIN,I2C,VADC,CAN

TC365 - ETH,ASCLIN,I2C,VADC,CAN

TC366 - ETH,ASCLIN,I2C,VADC,CAN

TC367 - ETH,ASCLIN,I2C,VADC,CAN

TC375 - ETH,ASCLIN,VADC,CAN

TC377 - ETH,ASCLIN,VADC,CAN

TC375_ED - ETH,ASCLIN,VADC,CAN

TC377_ED - ETH,ASCLIN,VADC,CAN

TC377_ED_EX - ETH,ASCLIN,VADC,CAN

TC387 - ETH,ASCLIN,I2C,VADC,CAN

TC389 - ETH,ASCLIN,I2C,VADC,CAN

TC397 - ETH,ASCLIN,I2C,VADC,CAN

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TC397_ADAS - ETH,ASCLIN,I2C,VADC,CAN

TC399 - ETH,ASCLIN,I2C,VADC,CAN

2) For TC374_ED, additional SENT IRQ connections provided which do not exist in the device.

3) For TC32x and TC33x devices, SENT IRQ connections increased to support 0 - 9 available SRNs.

Work around:

1) User cannot use interrupt modes for missing modules.

2) User shall not configure Sent interrupt connections > 9

3) User can only use the SRNs as provided in the configuration.

Impacted Release(s): 1.10.0, 1.30.0

1.9 Icu_17_TimerIp

1.9.1 0000053912-12024

Issue description: Configuration missing for Tim Channels in TC375, TC375_ED and TC374_ED variants.

Impact:

User cannot configure the below TIM channels :

1) TIM4_CH1 and TIM4_CH7 for TC374_ED variant

2) TIM5_CH0, TIM5_CH1, TIM5_CH2, TIM5_CH3 for TC375, TC375_ED and TC374_ED variants.

User also cannot configure the above missing TIM channels input as previous TIM channel's input.

Work around:

User shall ensure to achieve ICU driver functionality with the TIM channels as provided/available in the configuration.

Impacted Release(s): 1.30.0

1.10 Mcu

1.10.1 0000053912-12344

Issue description: Incorrect Tresos description for McuClockReferencePointFrequency2

Impact:

No functional impact.
Tresos description for McuClockReferencePointFrequency2 (fPLL2) should be calculated as :
fPLL2 = ((N+1)* fOSC)/((P+1) * (K3 + 1)* 1, 6) if McuPll2DivSelect= MCU_K3_DIV_FACTOR_NOT_BYPASSED_SEL0
OR
fPLL2 = ((N+1)* fOSC) / ((P+1) * (K3 + 1)) if McuPll2DivSelect= MCU_K3_DIV_FACTOR_BYPASSED_SEL1

Work around:

User shall configure the McuClockReferencePointFrequency2 as per the above equation.

Impacted Release(s): 1.10.0, 1.30.0, 1.40.0

1.10.2 0000053912-11679

Issue description: Mcu plugin issue for TC375, TC375_ED and TC374_ED derivatives.

Impact:

Code generation failure occurs since error is reported for MCU plugin. This applies for TC375, TC375_ED and TC374_ED derivatives.

Work around:

Customer cannot use Mcu plugin configuration for TC375, TC375_ED and TC374_ED derivatives.

Impacted Release(s): 1.30.0

1.10.3 0000053912-11550

Issue description: DCO Input frequency range increased to 10 - 40 MHz from 16 - 40 MHz.

Impact:

For all A2G variants, DCO Input frequency range increased from 16 - 40 MHz to 10 - 40 MHz . But MCU code generation plugin only supports in the range of 16 - 40 MHz.

Work around:

User needs to configure DCO Input frequency in the provided range of 16 - 40 MHz only.

Impacted Release(s): 1.10.0, 1.30.0

1.10.4 0000053912-11663

Issue description: As per GETH_TC.P001, Ethernet frequency operating range changed to 100 - 150 MHz from 150 - 200 MHz.

Impact:

User can configure wrong operation conditions for Ethernet frequency if > 150 MHz and may impact the Ethernet IP functionality.

Work around:

User shall configure Ethernet Frequency only as 150MHz.

Impacted Release(s): 1.10.0, 1.30.0

1.11 Sent

1.11.1 0000053912-12426

Issue description: In TC387, 20 SENT channels are bonded out(0-14, 17/18, 20-22).However in TC387 properties file, SENT Channels 0 to 19 are considered.

Holes present in sent channels are not considered in TC387 properties file.

Impact:

In TC387, few SENT channels (20,21,22) are not selectable in MCAL though provided in the hardware. SENT channels (15,16,19) are listed as configurable channels which should not be selected by the user.

Work around:

Use only the SENT channels (0-14, 17/18).

Impacted Release(s): 1.40.0

1.12 Smu

1.12.1 0000053912-12189

Issue description: Smu_SetAlarmAction() does not support disable of FSP action.

Impact:

User cannot disable FSP action at runtime using Smu_SetAlarmAction() API.

Work around:

Users shall configure the FSP action during SMU initialization and not change the FSP action at runtime.

Impacted Release(s): 1.10.0, 1.30.0, 1.40.0

1.13 Spi

1.13.1 0000053912-10645

Issue description: Calling Spi_Cancel() cancels the successive job of ongoing sequence being transmitted and updates the sequence status to cancelled. However updating the QSPI HW unit status to IDLE only happens once the ongoing job transmission is completed. So calling Spi_GetHwUnitStatus or Spi_GetStatus immediately after Spi_Cancel will return SPI_BUSY due to ongoing job.

Impact:

Calling Spi_GetHwUnitStatus or Spi_GetStatus immediately after Spi_Cancel in case of only single sequence/last sequence will return SPI_BUSY.

Work around:

User must call Spi_GetHwUnitStatus or Spi_GetStatus and wait untill the API returns SPI_IDLE.

Impacted Release(s): 1.10.0,1.30.0

1.13.2 0000053912-12064

Issue description: Trap occurs in SPI when DMA error interrupts occur on multiple channels across cores.

Impact:

If DMA move engine error occurs simultaneously on multiple SPI channels, a trap would occur in SPI driver if DMA interrupt error is less than any of the SPI interrupts.

Work around:

Interrupt priority of DMA and SPI shall be of order : DmaError > QspiError > Tx > Rx > PT2.

Impacted Release(s): 1.10.0, 1.30.0

1.13.3 0000053912-12218

Issue description: SPI_E_UNINIT DET reported from Spi_MainFunction_Handling.

Impact:

DET reported when Spi_MainFunction_Handling is called when SPI module is not initialized.

Work around:

SPI_E_UNIT DET when reported from Spi_MainFunction_Handling to be ignored by the application software.

Impacted Release(s): 1.10.0, 1.30.0, 1.40.0

1.14 Uart

1.14.1 0000053912-12037

Issue description: If CTS pin is not used for handshaking in UART, NONE option is missed in BMD files.

Impact:

User need to select one of the pin from the list.

Work around:

If UartCTSEnable option is disabled, any pin selected will not have impact on the generated code.

Impacted Release(s): 1.10.0,1.30.0

1.15 Wdg_17_Scu

1.15.1 0000053912-12307

Issue description: Incorrect information provided in WDG UM.

Impact:

In WDG UM, "system WDT" is mentioned in Hardware-software mapping chapter. The "system WDT" peripheral does not exist and should be renamed as "Safety WDT".

Work around: User shall interpret "system WDT" as "Safety WDT".

Impacted Release(s): 1.10.0, 1.30.0, 1.40.0

2 Safety topics v4.0

2.1.1 0000053912-8814

Issue description: ESM[SW]:DMA:ERROR_HANDLING description insufficient.

Impact:

User manual information is incomplete.

Work around:

Customer to use the workaround as mentioned below:

About handling DMA errors when using of SPI and DMA drivers together (Ref:ESM[SW]:DMA:ERROR_HANDLING):

Limitation:

The below limitation is applicable if SPI uses the DMA driver for asynchronous transmission:

Whenever the DMA channel used by SPI driver encounters an error, the DMA driver notifies the error along with the channel information to the SPI driver. However, due to the limitation in the error notification interface from SPI to the application, the SPI driver notifies the same error to the application without the DMA channel information.

Workaround:

The application shall supervise the DMA RP Error Interrupt Service Request. The application shall read the DMA move engine error registers ERRSR0 and ERRSR1 before invoking the interrupt handler provided by DMA. This is to determine the error cause and the DMA channel number which caused the RP error. The sequence is as below:

- Move engine error occurs in hardware

- RP ISR is triggered

- Application reads the error flags in ERRSRm for determining the error cause and ERRSRm.LEC for determining the DMA channel number that caused the error.

- Call Dma_MEInterruptDispatcher

- On return from Dma_MEInterruptDispatcher, Application shall take necessary action.

Impacted Release(s): 1.10.0, 1.30.0

2.1.2 0000053912-8816

Issue description: Clarity to achieve SMC[SW]:SMU:CONFIG is incomplete in SW User Manual.

Impact:

In SW User Manual, documentation clarity to achieve SMC[SW]:SMU:CONFIG is incomplete. AoU to be added, see AoU text in Workaround.

Work around:

AoU: Customer shall ensure to enable 'SmuStdbyEnable' in SMU driver configuration to achieve SMC[SW]:SMU:CONFIG ESM.

Impacted Release(s): 1.10.0, 1.30.0, 1.40.0

3 Known issues v3.0

3.1 ADC

3.1.1 0000053912-9946

Issue description: HSPDM Input Trigger configuration support given for unsupported devices in ADC.

Impact: HSPDM module is not available in the following devices i.e. TC38x devices, TC37x devices and TC36x devices, hence trigger of HSPDM is not possible from the unsupported devices if configured.

Work around:

User should not configure the HSPDM as a trigger source from the following HSPDM unsupported devices. i.e. TC38x devices, TC37x devices and TC36x devices.

Impacted Release(s): 1.10.0, 1.30.0

3.2 CAN

3.2.1 0000053912-10694

Issue description: When Can module is initialized again from the same core, the DET CAN_17_MCMCAN_E_TRANSITION is not reported.

Impact: Unnecessary re-initialization sequence retriggered.

Work around:

The user shall ensure that Can_17_McmCan_Init is called only once from the same core.

Impacted Release(s): 1.10.0, 1.30.0

3.2.2 0000053912-10858

Issue description: CAN11 RX selection value is missed in AURIX2G_TC366.properties file.

Impact: There is an additional option of CAN11_RXDA which is made unavailable in the current configuration. Hence the user is able to use only CAN11_RXDB.

Work around:

The user shall use the CAN11_RXDB when using controller 1 of kernel 1.

Impacted Release(s): 1.30.0

3.2.3 0000053912-10749

Issue description: Main Function Period is generated incorrectly in bswmd arxml file.

Impact: In case of polling function the period configured is not generated in the bswmd arxml as configured and only the default value of 5ms.

Work around:

In case polling is used and the user shall not be able to configure any value other than 5ms. The user shall use the default value of 5ms for polling functions.

Impacted Release(s): 1.10.0, 1.30.0

3.2.4 0000053912-9738

Issue description: In the Can_17_McmCan_SetControllerMode API, the return value of the API is determined based on whether the transition to a requested state occurs or not. When a request is made for a state transition to CANIF_CS_STARTED and the transition does not take place succesfully due to a timeout condition, the global state variable still gets updated to STARTED. Hence in the next call when the system tries to recover by calling the API again, it triggers a DET to indicate that the CanSM is already in STARTED state.

Impact: The subsequent attempts to transition to the STARTED state by calling the API returns CAN_NOT_OK and DET.

Work around:

No workaround.
Hint: Timeout event should be avoided. One possible way to achieve this is to configure a high value for the parameter CanTimeoutDuration.

Impacted Release(s): 1.10.0, 1.30.0

3.3 CanTrcv_17_V9251

3.3.1.1 0000053912-10559

Issue description: CanTrcv module multiplicity was 0-1. According to the AUTOSAR requirement , the module multiplicity value should be 0-*.

Impact: Multiple CanTrcv modules cannot be added in the configuration.

Work around: Multiple CanTrcv modules should not be in the configuration.

Impacted Release(s): 1.30.0

3.4 CanTrcv_17_W9255

3.4.1 0000053912-10560

Issue description: CanTrcv module multiplicity was 0-1. According to the AUTOSAR requirement, the module multiplicity value should be 0-*.

Impact: Multiple CanTrcv modules cannot be added in the configuration.

Work around:

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Multiple CanTrcv modules should not be in the configuration.

Impacted Release(s): 1.30.0

3.5 DIO

3.5.1 0000053912-10461

Issue description: Plausibility check for input parameter "Level" is not done for Dio_WriteChannel() API.

Impact: For Dio_WriteChannel(), a wrong "Level" value will always result in setting the port pin as STD_HIGH.

Work around:

For Dio_WriteChannel(), user shall pass only as STD_LOW or STD_HIGH as the input parameter for "Level".

Impacted Release(s): 1.10.0, 1.30.0

3.6 DMA

3.6.1 0000053912-9369

Issue description: Mismatches in parameters in their names and dependencies.

Impact: The names and dependency mismatches can result in incorrect interpretation of parameters.

Work around:

The following parameter names are mentioned incorrectly in User Manual: DmaInitDeInitApiMode, DmaChDeInitApiConfiguration, DmaGetVersionInfoApiConfiguration and DmaResourcePartitionErrorNotifRoutine. They are to be read as DmaInitApiMode, DmaDeinitApiConfiguration, DmaVersionInfoApi and DmaMoveEngineErrorNotifRoutine respectively.

Impacted Release(s): 1.30.0

3.6.2 0000053912-10804

Issue description: Trap will occur if DMA clock is not enabled and Dma_MEStatusClear() is invoked before Dma_Init().

Impact: Invoking Dma_MEStatusClear() API before Dma_Init() will result in a trap if the DMA clock is not enabled.

Work around:

Dma_MEStatusClear() shall be invoked after Dma_Init() is done for the respective cores.

Impacted Release(s): 1.10.0, 1.30.0

3.6.3 0000053912-9819

Issue description: Dma_ChInit() has a wrong error DET DMA_E_DATA_TRANSFER_IN_PROGRESS indicated in UM.

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Impact: No functional impact. Customer may mistakenly consider DET DMA_E_DATA_TRANSFER_IN_PROGRESS to be raised by Dma_ChInit() API.

Work around:

The user shall ignore the error DET DMA_E_DATA_TRANSFER_IN_PROGRESS for Dma_ChInit() API.

Impacted Release(s): 1.10.0, 1.30.0

3.7 DSADC

3.7.1 0000053912-9745

Issue description: Mismatch in Property file variables for the XDM and BMD.

Impact: When user uses the BMD for configuration and XDM for generation then Generator will raise an Error for the variable mismatch.

The following parameters cannot be configured only for non-tresos tool user:-

DsadcComModeVoltNegAEnable, DsadcComModeVoltNegBEnable, DsadcComModeVoltNegCEnable, DsadcComModeVoltNegDEnable, DsadcComModeVoltPosAEnable,DsadcComModeVoltPosBEnable,DsadcComModeVoltPosCEnable,DsadcComModeVoltPosDEnable,DsadcInputPinSelection

DsadcTriggerSelect.

Work around:

Limitation:

Users who do not use Tresos tool, should avoid configuring following parameters:

DsadcComModeVoltNegAEnable, DsadcComModeVoltNegBEnable, DsadcComModeVoltNegCEnable, DsadcComModeVoltNegDEnable, DsadcComModeVoltPosAEnable,DsadcComModeVoltPosBEnable,DsadcComModeVoltPosCEnable,DsadcComModeVoltPosDEnable,DsadcInputPinSelection

DsadcTriggerSelect.

Impacted Release(s): 1.30.0

3.7.2 0000053912-10628

Issue description: Comparator event selection for lower and upper boundary is not working.

Impact: Comparator event will be generated for all the events even though user wants the events only for inside boundary or outside boundary.

Work around:

Based on the converted results, user has to identify whether the result is inside the boundary or outside the boundary in every comparator event.

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Impacted Release(s): 1.30.0

3.8 FEE

3.8.1 0000053912-10899

Issue description: Un-configured blocks management while handling word-line failures during write operation may result in out of bound array access.

Impact: During the mentioned scenario, if out of bound array access happens to be in a reserved memory area, it results in a trap.

Work around:

Use same block configuration for both boot and run time application configurations. This ensures that there are no un-configured blocks.

Impacted Release(s): 1.10.0, 1.30.0

3.8.2 0000053912-10903

Issue description: Occurrence of Program verify error during QS hardening results in a word-line skip for the write operation of the block, which triggered GC.

Impact: Unintended word-line skips resulting in unusable word-lines until next GC happens.

Work around:

No workaround required as driver recovers during next GC cycle.

Impacted Release(s): 1.10.0, 1.30.0

3.8.3 0000053912-10284

Issue description: As part of FEE double sector algorithm garbage collection (GC) happens. During GC, erase operation could weaken the data in QS region because of the ‘erase disturbs’. In order to secure the QS data, FEE driver performs check and hardening periodically. Due to an error in the software implementation of FEE driver, hardening check is not performed for all pages. This issue is observed only when user configures both NVM and QS data blocks.

Impact: This may result in not performing the hardening operation for a page where hardening is actually required and thereby leading to data loss in the QS region.

Work around:

Avoid using configuration where both NVM and QS data blocks are configured.

Impacted Release(s): 1.10.0, 1.30.0

3.8.4 0000053912-10964

Issue description: Possibilities of Data blocks corruption leading to trap under certain scenarios while handling word-line failures during write operation.

Impact: Data flash content may be corrupted leading to data loss of user blocks and may result in a trap.

Work around: None.

Customers are requested to contact Field Application Engineers for support in case this issue impacts their use case. Field application engineers can support customer to analyse and understand the impact in customer specific environment.

Impacted Release(s): 1.10.0, 1.30.0

3.8.5 0000053912-10661

Issue description: Due to an error in the software implementation of FEE driver, when a pending user write request is cancelled by Fee_Cancel()/ Fee_17_CancelAll() API, followed by either user write request or user read request and then followed by user write request, driver may write unintended data.

API call sequences:

Fee_Write() → Fee_Cancel() → Fee_Read() → Fee_Write() or Fee_Write() → Fee_Cancel() → Fee_Write()

Impact: In the scenario mentioned in the description, the data flash content may be corrupted leading to

• Data loss of user blocks and/or

• Trap (DAE/DSE)

Work around:

Do not use Fee_Cancel()/ Fee_17_CancelAll() API for canceling pending write operation.

Impacted Release(s): 1.10.0, 1.30.0

3.8.6 0000053912-11133

Issue description: Multiple instances of QS cannot be erased by single call to Fee_17_EraseQuasiStaticData API when 256 QS instances are requested for erasure or if the QS block instances order is not maintained as specified in the user manual even after export and import of the configuration in Tresos.

Impact: Multiple instances of QS cannot be erased by single call to Fee_17_EraseQuasiStaticData API when 256 QS instances are requested for erasure or if the QS block instances order is not maintained as specified in the user manual even after export and import of the configuration in Tresos.

In the scenario mentioned above, the driver state will be stuck in 'busy' or incorrect QS block state may be reported by Fee_17_GetQuasiStaticBlockInfo respectively.

Work around:

Known issues v3.0

In this scenario, Fee_17_EraseQuasiStaticData API shall be called for each instance rather than the total number of instances.

Impacted Release(s): 1.10.0, 1.30.0

3.9 Flexray

3.9.1 0000053912-9999

Issue description: The Fr_17_Eray_ReconfigLPdu() API does not report the development error FR_E_INV_CHNL_IDX for negative values of the input parameter Fr_ChnlIdx.

Impact: When negative values of Fr_ChnlIdx parameter are passed to the Fr_17_Eray_ReconfigLPdu() API, the API does not report the development error FR_E_INV_CHNL_IDX and results in incorrect configuration of the channel index value for the LPdu.

Work around:

The application should use the defined enum literals of type Fr_ChannelType for the input parameter Fr_ChnlIdx, or use positive values.

Impacted Release(s): 1.10.0, 1.30.0

3.9.2 0000053912-9310

Issue description: During the execution of Fr_17_Eray_SetWakeupChannel() API, if there is a hardware error detected during the change of controller's POCState to POC:ready, the API returns E_OK (irrespective of the DEM configuration) instead of E_NOT_OK.

Impact: In case an hardware error is detected by Fr_17_Eray_SetWakeupChannel() API during the change of controller's POCState to POC:ready, this error condition is not recognized by the upper layer SW by checking the return value because E_OK is returned.

Work around:
The DEM event for FR controller hardware error needs to be configured and a check whether this production error is reported needs to be performed in order to examine the hardware error detected by Fr_17_Eray_SetWakeupChannel() API.

Impacted Release(s): 1.10.0, 1.30.0

3.10 FLS

3.10.1 0000053912-10907

Issue description: FSI in the NVM subsystem executes erase, program and verify operations on all flash memories. The FSI performs flash commands by the CPU (Host command sequence interpreter) and HSM (HSM command sequence interpreter- Only for DFLASH1) in time slices. Time out values in Flash drivers are calculated for the case that only one operation is executed uninterrupted by the time slicing (Issue applicable for both FLS and FlsLoader).

Impact: Unintended time out DET may be raised when operations on DFLASH0 and DFLASH1 are performed in parallel.

Work around:

Ensure operations on DFLASH0 and DFLASH1 are not happening in parallel.

Impacted Release(s): 1.10.0, 1.30.0

3.10.2 0000053912-7586

Issue description: Reporting of unintended timeouts may be observed for the lower range of supported values of FlsCallCycle parameter.

Impact: Reporting of unintended timeouts by the FLS driver will be observed while the actual write/erase operation is still going on in the hardware.

Work around:

It is to be ensured that the scheduling frequency of FLS operations using the Fls_17_Dmu_MainFunction() API is done at a rate greater than or equal to 200us. This can be done by configuring the parameter 'FlsCallcycle' to a value greater than or equal to 200. Timeouts may be observed for the values less than 200, if configured for FlsCallCycle.

Impacted Release(s): 1.10.0, 1.30.0

3.10.3 0000053912-10182

Issue description: Operation Error(OPER) will be notified as sequence error(SQER) for erase resume(Fls_17_Dmu_ResumeErase()) and hardening(Fls_17_Dmu_IsHardening()) operations.

Impact: 1) Hardening: There will not be any impact from the user perspective for the hardening operation(Fls_17_Dmu_IsHardeningRequired()) as this API is used only by Infineon FEE, so this will be taken care by Infineon FEE.

2) Resume Erase(Fls_17_Dmu_ResumeErase()): Resume erase will be impacted and an OPER(operation error) will be notified as SQER(sequence error).

Work around:

Known issues v3.0

If a user repeatedly gets a sequence error(SQER) while resuming an erase using the Fls_17_Dmu_ResumeErase() API, then a system reset is recommended.

Impacted Release(s): 1.10.0, 1.30.0

3.11 FLSLoader

3.11.1 0000053912-10907

Issue description: FSI in the NVM subsystem executes erase, program and verify operations on all flash memories. The FSI performs flash commands by the CPU (Host command sequence interpreter) and HSM (HSM command sequence interpreter- Only for DFLASH1) in time slices. Time out values in Flash drivers are calculated for the case that only one operation is executed uninterrupted by the time slicing (Issue applicable for both FLS and FlsLoader).

Impact: Unintended time out DET may be raised when operations on DFLASH0 and DFLASH1 are performed in parallel.

Work around:

Ensure operations on DFLASH0 and DFLASH1 are not happening in parallel.

Impacted Release(s): 1.10.0, 1.30.0

3.11.2 0000053912-10733

Issue description: If there are interrupts during PFLASH write operation or if the Safety watchdog counter frequency divider is not set to 16384, then the Safety watchdog timeout may happen.

Impact: Safety alarms may be triggered during PFLASH write operation if the Safety ENDINIT is disabled more than the Safety watchdog timeout period. This may happen if there are interrupts during PFLASH write operation or if the Safety watchdog counter frequency divider is not set to 16384.

Work around:

Application shall ensure PFLASH write operation is not interrupted and the Safety watchdog counter frequency divider is set to 16384.

Impacted Release(s): 1.10.0, 1.30.0

3.12 General

3.12.1 0000053912-10718

Issue description: OS wrapper calls made for register writes in CAT1 interrupt context.

Impact: In CAT1 interrupt context, call to OS wrapper for register writes are made (e.g: ADC, SPI). It is inconsistent across MCAL modules.

Known issues v3.0

Work around:

At integration level, user shall take care of handling OS wrappers being called in CAT1 interrupt context.

Impacted Release(s): 1.10.0, 1.30.0

3.12.2 0000053912-9253

Issue description: Impact on MCAL for Errata CPU_TC.H019.

Impact: If the lock (like Semaphore or Spinlock) and resource being protected are placed in different memory modules (e.g: DSPR, PSPR, LMU), correct sequence of execution (read and write instruction sequence) to the lock and resource is not ensured and leads to inconsistent data. being read/written to the lock and resource.

Work around:

User shall ensure that:
- The lock (address of which is passed to the Mcal_GetSpinlock() API) and the resource to be protected shall be placed in the same memory module.
- The lock used shall be placed in the non-cached memory section.

Impacted Release(s): 1.10.0, 1.30.0

3.13 HSSL

3.13.1 0000053912-10086

Issue description: Structures/Unions are not recommended to be passed directly as function arguments. This will occupy lot of space on stack and inefficient. This is a violation of ECR_206.

Impact: Windriver compiler bug TCDIAB-14541 (structure members are incorrectly accessed) has an impact.

Work around:

HSSL is a demo module. If customer see an impact due to this, then required code changes can be made to fix the issue.

Impacted Release(s): 1.30.0

3.13.2 0000053912-10882

Issue description: Running HSSL module in user mode results in trap as registers with SV-write are written directly.

Impact: HSSL module cannot be run in user mode.

Work around:

As HSSL is demo code, customer can update the code to support user mode.

Impacted Release(s): 1.30.0

3.14 I2C

3.14.1 0000053912-10934

Issue description: Running I2C module in user mode results in trap as GPCTL(Write-SV mode) register is written directly.

Impact: I2C module cannot be run in user mode.

Work around:
As I2C is demo code, customer can update the code to support user mode.

Impacted Release(s): 1.30.0

3.15 ICU

3.15.1 0000053912-10719

Issue description: Unavailable port pin PORT23_PIN0 in TC377_ED_EX used for TIM channel configuration.

Impact: Customer may select PORT23_PIN0 for TIM channel configuration which does not exist and ICU functionality will not work for that pin.

Work around:
Customer shall not select PORT23_PIN0 TIM channel in ICU configuration.

Impacted Release(s): 1.30.0

3.16 LIN

3.16.1 0000053912-10001

Issue description: Wakeup related call back LinIf_WakeupConfirmation to be guarded with Wakeup Enable is ON else implicit declaration of call back function warning is reported.

Impact: Compiler warning is reported.

Work around:
A dummy declaration of LinIf_WakeupConfirmation must be defined in LinIf when LIN_GLOBAL_CHANNEL_WAKEUP_SUPPORT is STD_OFF.

Impacted Release(s): 1.10.0, 1.30.0

3.16.2 0000053912-10316

Issue description: When DET is OFF and channel state is not in LIN_CH_SLEEP, if Lin_17_AscLin_Wakeup and Lin_17_AscLin_WakeupInternal APIs are called the return value will be E_OK indicating the wakeup has occurred.

Impact: Upper layer assumes that the wakeup has occurred successfully and may process channel accordingly though actual wakeup has not occurred on the bus.

Known issues v3.0

Work around:

All sequences should be tested with DET ON.

Impacted Release(s): 1.10.0, 1.30.0

3.16.3 0000053912-10315

Issue description: When LIN_17_ASCLIN_GLOBAL_CHANNEL_WAKEUP_SUPPORT is ON and channel wakeup is enabled or disabled, EcuM_CheckWakeup is been called in both cases. EcuM_CheckWakeup should not be called when channel wakeup is disabled.

Impact: If false or unintended wakeup is detected for a LIN channel for which wakeup is disable during configuration, the LIN driver will not validate this scenario and the LIN driver will invoke EcuM_CheckWakeup().

Note: if this error scenario happens, application will get a wrong information from driver instead of error notification.

Work around: No workaround for the issue. Users to ensure that the false wakeup or unintended wakeup is not happening in the system.

Impacted Release(s): 1.10.0, 1.30.0

3.17 MCALLIB

3.17.1 0000053912-10568

Issue description: Wrong STM tick used for delay operations if SYSCLK is selected as the clock source.

Impact: Mcal_DelayTickResolution() API will provide a higher STM tick resolution, and result in slower timeout than desired. Below are the impacted MCAL drivers using Mcal_DelayTickResolution() API:
- CanTrcv_17_V9251
- CanTrcv_17_W9255
- Can_17_McmCan
- Eth_17_GEthMac
- FlsLoader
- Fls_17_Dmu
- Fr_17_Eray
- Lin_17_AscLin
- McalLib
- Mcu
- Uart
- Wdg_17_Scu

Work around:

User shall not use SYSCLK as the input clock source. They shall use the back-up clock or oscillator as the clock sources.

Known issues v3.0

Impacted Release(s): 1.30.0

3.18 MCU

3.18.1 0000053912-9801

Issue description: Mcu code generation fails when default Tresos naming convention is not followed for configuration containers and parameters.

Impact: If the name of configuration containers and parameters listed below are changed from default Tresos names, Mcu code generation will fail.
McuEruAllocationConf
McuGtmAllocationConf
McuCcu6ModuleAllocationConf
McuGpt12ModuleAllocationConf
GtmTomGlobalConf
GtmTomChannelConf
GtmAtomGlobalConf
GtmAtomChannelConf

Work around:
The short name for following containers and their respective sub-containers shall follow the syntax <Container_Name>_<i> where <i> is an integer:
McuEruAllocationConf
McuGtmAllocationConf
McuCcu6ModuleAllocationConf
McuGpt12ModuleAllocationConf
GtmTomGlobalConf
GtmTomChannelConf
GtmAtomGlobalConf
GtmAtomChannelConf
Note: The above naming convention is by default followed in Tresos, when new containers are added or when project is created.

Impacted Release(s): 1.10.0, 1.30.0

3.18.2 0000053912-10172

Issue description: RAM redundancy handling may result in trap during standby entry of Mcu_SetMode() API.

Impact: If Standby mode is used and customer has application data in the first 64 bytes of configured Standby RAM, a trap may occur. The driver assumes valid RAM addresses are present in the first 64 bytes and tries to de-reference these addresses.

Known issues v3.0

Work around:
If Standby mode shall be used, customer shall reserve the first 64 bytes of the configured Standby RAM and not use it.

Impacted Release(s): 1.10.0, 1.30.0

3.18.3 0000053912-9132

Issue description: Mcu_SetMode() activates the Standby mode even when a write to PMSWCR3 register fails (DEM failure reported).

Impact: If wake-up timer is used as a wake-up sourceand during execution of Mcu_SetMode() to Standby mode, if PMSWCR3 write fails because of a hardware failure, the system may not wake-up from Standby at all even when wake-up timer has triggered the system for wake-up.

Work around:
The user shall not use wake-up timer as the only wake-up source.

Impacted Release(s): 1.10.0, 1.30.0

3.18.4 0000053912-9412

Issue description: A compilation error is reported when McuInitClockApi configuration parameter is set FALSE.

Impact: A compilation error will be reported when the configuration parameter McuInitClockApi is switched OFF.

Work around:
The user shall not set the McuInitClockApi configuration parameter to False.

Impacted Release(s): 1.30.0

3.19 OCU

3.19.1 0000053912-6153

Issue description: Data Inconsistency when Ocu_Init is called by multiple cores with different configuration pointer.

Impact: The operation of the Ocu driver cannot be guaranteed, if Ocu_Init is invoked concurrently from multiple cores with different configuration pointer, it leads to data inconsistency.

Work around:
User shall ensure the configuration pointer passed for Ocu initialization(Ocu_Init() API) should be the same across all the configured cores.

Impacted Release(s): 1.30.0

3.20 PORT

3.20.1 0000053912-9809

Issue description: Variation point for certain Autosar and IFX parameters not configurable.

Impact: The following parameters can not be configured:

PortPinDirectionChangeable

PortPinInputPullResistor

PortPinOutputPadDriveStrength

PortPinOutputPinDriveMode

PortPinInputPadLevel

PortPinEnableAnalogInputOnly

PortPinEmergencyStop

PortPinControllerSelect

PortLVDSRxEnController

PortLVDSRxPathEnable

PortLVDSRxTerminationMode

PortLVDSMode

PortLVDSPadSupply

PortLVDSTxEnController

PortLVDSTxPathEnable

Known issues v3.0

PortLVDSTxPowerDownPullDown.

Work around:
Customer should not configure certain parameters for variation point support.

Impacted Release(s): 1.10.0

3.21 PWM

3.21.1 0000053912-10918

Issue description: GHS Compiler warning in PWM for following configurations:

PWM_17_GTMCCU6_DE_INIT_API = STD_ON, PWM_17_GTMCCU6_SET_OUTPUT_TO_IDLE_API = STD_OFF and PWM_17_GTMCCU6_DUTY_SHIFT_IN_TICKS = STD_OFF.

Impact: Compiler warning in GHS will occur when PWM_17_GTMCCU6_DE_INIT_API = STD_ON, PWM_17_GTMCCU6_SET_OUTPUT_TO_IDLE_API = STD_OFF and PWM_17_GTMCCU6_DUTY_SHIFT_IN_TICKS = STD_OFF.

Work around:
To avoid the compiler warning, customer can use any one of the below workarounds:
1) Enable PWM_17_GTMCCU6_SET_OUTPUT_TO_IDLE_API = STD_ON and PWM_17_GTMCCU6_DUTY_SHIFT_IN_TICKS = STD_ON

2) Customer shall configure at-least 1 CCU6 channel if PWM_17_GTMCCU6_DE_INIT_API = STD_ON, PWM_17_GTMCCU6_SET_OUTPUT_TO_IDLE_API = STD_OFF and PWM_17_GTMCCU6_DUTY_SHIFT_IN_TICKS = STD_OFF.

Impacted Release(s): 1.30.0

3.21.2 0000053912-11145

Issue description: For PWM shifted channels when PwmHandleShiftByOffset is TRUE, the configuration error check unnecessarily restricts the user to configure the channels in the order and also the channels to be configured in the same module(TGC/AGC) eventhough check is not required.

Impact: User is unnecessarily forced to order the PWM TOM/ATOM channels only within a TOM/ATOM module when PwmHandleShiftByOffset=TRUE.

Work around:
User shall ensure PWM TOM/ATOM channels are ordered in the same respective TOM/ATOM module when PwmHandleShiftByOffset=TRUE.

Impacted Release(s): 1.30.0

3.22 SENT

3.22.1 0000053912-10695

Issue description: Deinit API throws compilation error when SentDevErrorDetect is off and SentMulticoreErrorDetect is ON.

Impact: DET off configuration gives compilation error.

Work around:
SentDevErrorDetect and SentMultiCoreErrorDetect should be ON.

Impacted Release(s): 1.30.0

3.23 SMU

3.23.1 0000053912-8818

Issue description: 'A2GT-REQ_AoU_SW-15' in MCAL user manual is not inline with 'ESM[SW]:SMU:ALIVE_ALARM_TEST' AoU in safety manual.

Impact: Information related to frequency of the "SMU Alive Test" execution is not mentioned. This may lead to incorrect deployment of the safety measure.

Work around:
A2GT-REQ_AoU_SW-15 to be read as "The integrated system shall execute the "SMU Alive Test" provided in MCAL software at least once per driving cycle and take the appropriate actions depending on the result."

Impacted Release(s): 1.10.0, 1.30.0

3.23.2 0000053912-10578

Issue description: The Smu_LockConfigRegs() API is non-reentrant and can be invoked from only one core at a time but it is incorrectly documented to be Re-entrant in both SAS and User Manual.

Impact: The Smu_LockConfigRegs() API does not support reentrancy. Treating the API as reentrant or calling it simultaneously from multiple cores can lead to inconsistent results. In some cases, second invocation may return E_OK but in others, it may return with E_NOT_OK and DET or Safety error, if enabled.

Work around:
User shall treat the Smu_LockConfigRegs() API in a non-reentrant manner.

Impacted Release(s): 1.10.0, 1.30.0

3.24 SPI

3.24.1 0000053912-9099

Issue description: Spi_Deinit not resetting all the registers which are initialized as part of Spi_Init.

Known issues v3.0

Impact: Impact analysis done and no functional impact.

Work around: No work around required as there is no functional impact.

Impacted Release(s): 1.10.0, 1.30.0

3.24.2 0000053912-8936

Issue description: In Multicore scenario, few SPI hardware channels mapped to Core 0 which are using only synchronous and few other hardware channels mapped to Core 1 which are always asynchronous. Calling any runtime API results in FALSE UNINIT DET.

Impact: The mentioned DET will be observed for all the runtime API until all cores are successfully initialized.

Work around:

User must ensure that all cores initializations are done before invoking any runtime API from any core.

Impacted Release(s): 1.10.0, 1.30.0

3.24.3 0000053912-9102

Issue description: Multiple DEMs are reported on any HW error occurred during asynchronous transmission.

Impact: To handle each DEM, repetitive corrective actions may be triggered by application in quick successions.

Work around:

Ignore the successive DEM which are reported with the same EVENT ID: SPI_E_HARDWARE_ERROR.

Note: Applicable only for Asynchronous Transmission.

Impacted Release(s): 1.10.0, 1.30.0

3.24.4 0000053912-9108

Issue description: While Spi_Controlloopback API is executing and second thread invokes the Spi_Asynctransmit API then there is a possibility of data getting corrupted since the loopback will be enabled/disabled when data transfer is in progress.

Impact: Data transmission over the SPI interface to the other end may not be guaranteed.

Work around:

When Spi_ControlLoopBack API is invoked, upper layer must ensure that no other thread is allowed to start a new sequence on the same HW until Spi_ControlLoopBack API has completed its execution.

Impacted Release(s): 1.30.0

3.24.5 0000053912-8951

Issue description: Clearing of PT2F is missing when interrupts are enabled.

Impact: Trap observed while switching from interrupt mode to polling mode in LEVEL-2 configuration.

Work around:

At runtime, user must avoid switching between interrupt to polling mode.

Impacted Release(s): 1.10.0, 1.30.0

3.24.6 0000053912-9831

Issue description: Issue with 8-bit IB channel buffer access for Synchronous configuration, resulting in invalid generation of SPI_SYNC_IB_BUFFER_SIZE_COREx macro size.

Impact: IB transmission (TX) and Reception (RX) buffers will be corrupted. Functionality cannot be guaranteed.

Work around:

1. Ensure that the number of IB buffers are multiple of 4 bytes in case of 8-bit channel data width.
2. Use asynchronous transmission mode instead of synchronous if #1 is not feasible.

Impacted Release(s): 1.10.0, 1.30.0

3.24.7 0000053912-9901

Issue description: SpiMaxChannel, SpiMaxJob, SpiMaxSequence Post-build variant value should be set to false.

Impact: Values for these configuration parameters are not allowed to change across variants.

Work around:
Customers to ensure that value of these configuration parameters (i.e. SpiMaxChannel, SpiMaxJob, SpiMaxSequence) can not be changed.

Impacted Release(s): 1.10.0, 1.30.0

3.24.8 0000053912-9100

Issue description: CS_VIA_GPIO is not de-asserted when error occurs during synchronous transmission.

Impact: Slave will not be de-asserted and successive communication to different slave devices will also be impacted.

Work around:

1. DEM is reported when there any error during transmission. Use must de-assert the CS line while handling the DEM.
2. Use HW driven CS instead of GPIO.

Known issues v3.0

Impacted Release(s): 1.10.0, 1.30.0

3.24.9 0000053912-9371

Issue description: Spi_SyncTransmit() API is exiting before Trailing Delay is over and updating the state as IDLE even though Hardware is busy.

Impact: 1. API Spi_GetHWUnitStatus() will return SPI_BUSY
2. API Spi_ControlLoopBack() will return E_NOT_OK
though Spi_SyncTransmit() API returns E_OK indicating the transmission completion.

Work around:

After Spi_SyncTransmit() API returns E_OK, user must call Spi_GetHWUnitStatus() API and wait untill it returns SPI_IDLE.

Impacted Release(s): 1.10.0, 1.30.0

3.24.10 0000053912-9720

Issue description: Spi_Cancel API should cancel the sequence only if the sequence is in pending state.

Impact: Updates the sequence status to SPI_SEQ_CANCELED even though the sequence transmission is not on-going.

Work around:

User must invoke Spi_Cancel() only when Spi_GetSequenceResult() API returns SPI_SEQ_PENDING.

Impacted Release(s): 1.10.0, 1.30.0

3.24.11 0000053912-9087

Issue description: Spi_SyncTransmit() is returning E_OK if HW error is encountered by reporting a DEM.

Impact: If DEM reporting is disabled, User assumes that the transmission is successful since the API returns E_OK.

Work around:

User can call Spi_GetSequenceResult() API to get the sequence status though Spi_SyncTransmit() API returns E_OK.

Impacted Release(s): 1.10.0, 1.30.0

3.24.12 0000053912-9890

Issue description: IB channel offset overflows when more than one channel configured with 65535 data elements.

Impact: IB buffer is corrupted.

Work around:

Known issues v3.0

User must ensure the sum of all IB channel buffers size allocated for a core must not cross 65535 bytes.

Impacted Release(s): 1.10.0, 1.30.0

3.24.13 0000053912-10039

Issue description: Incorrect EB, IB channel validation with respect to 8190(max data elements allowed per asynchronous job) during configuration code generation.

Impact: Incorrect errors will be reported.

Work around:

User must ensure the number of data elements per asynchronous job must not cross 8190 data elements.

Impacted Release(s): 1.10.0, 1.30.0

3.24.14 0000053912-10068

Issue description: SPI_E_PARAM_SEQ DET/SE not raised if Spi_AsyncTransmit() is called for a Synchronous sequence.

Impact: Functional behavior is not guaranteed.

Work around:

User must have a configuration where configuration parameters both SpiDevErrorDetect and SpiMulticoreCheckEnable must be set to TRUE.

Impacted Release(s): 1.10.0, 1.30.0

3.24.15 0000053912-10935

Issue description: Spi_GetJobResult doesn't report DET when called with a Job not allocated to that CPU core.

Impact: Incorrect job result will be returned even though Job is not configured for the core.

Work around:

User must ensure that the JobID passed to the Spi_GetJobResult() API is assigned to core on which the Spi_GetJobResult() API is invoked.

Impacted Release(s): 1.10.0, 1.30.0

3.24.16 0000053912-9101

Issue description: Incorrect behavior of Spi_GetHwUnitStatus() API.

Impact: Spi_GetHwUnitStatus() may return SPI_IDLE intermittently, even though HW unit is in busy state.

Work around:

Avoid using this API.

Known issues v3.0

Note: This is an optional API.

Impacted Release(s): 1.10.0, 1.30.0

3.24.17 0000053912-9103

Issue description: Spi_SyncTransmit and Spi_AsyncTransmit behave different if error is encountered during transmission. If an error occurs during Sync transmission, all the jobs related to same sequence is marked as SPI_JOB_FAILED. In case of AsyncTransmit all the jobs apart from the one failed is marked as SPI_JOB_OK, only job that failed is marked as SPI_JOB_FAILED. Status of the jobs to be retained as Queued / pending.

Impact: Calling Spi_GetJobResult on a Job(not actually transmitted but belongs to failed sequence) returns SPI_JOB_OK in case of Asynchronous communication where as it returns SPI_JOB_FAILED incase of synchronous communication.

Work around:
If the Spi_GetJobResult API returns SPI_JOB_FAILED, user must ignore the status of successive jobs.

Impacted Release(s): 1.10.0, 1.30.0

3.24.18 0000053912-10645

Issue description: Calling Spi_Cancel() cancels the successive job of ongoing sequence being transmitted and updates the sequence status to cancelled. However updating the QSPI HW unit status to IDLE only happens once the ongoing job transmission is completed. So calling Spi_GetHwUnitStatus or Spi_GetStatus immediately after Spi_Cancel will return SPI_BUSY due to ongoing job.

Impact: Calling Spi_GetHwUnitStatus or Spi_GetStatus immediately after Spi_Cancel in case of only single sequence/last sequence will return SPI_BUSY.

Work around:
User must call Spi_GetHwUnitStatus or Spi_GetStatus and wait untill the API returns SPI_IDLE.

Impacted Release(s): 1.0.0, 1.10.0, 1.20.0, 1.30.0, 1.40.0

3.25 UART

3.25.1 0000053912-10629

Issue description: UART driver does not support fast frequencies.

Impact: Clock mismatch possible in baud rate regeneration for fast frequencies. This will lead to incorrect data communication.

Work around:

The user should always select UartCsrClksel as ASLINS in tresos to take reference for the baud rate generation.

Known issues v3.0

Impacted Release(s): 1.30.0

3.25.2 0000053912-10808

Issue description: Incorrect CTS select line SELECT_CTS_A_PORT14_PIN9 is given for ASCLIN0 Kernel it should be None.

Impact: If SELECT_CTS_A_PORT14_PIN9 used for ASCLIN0 then Handshaking mechanism may not work .

Work around:

a) ASCLIN0: Avoid using this configuration.

b) For the rest: User can choose different AscLin kernal(ASCLIN1/ASCLIN2/ASCLIN3) to enable Handshaking mechanism.

Impacted Release(s): 1.30.0

3.26 WDG

3.26.1 0000053912-9891

Issue description: Wrong maximum limit for WDG Slow Refresh time configuration parameters, when STM timer is selected.

Impact: The WDG Slow refresh time configuration for STM timer can only be a maximum of 4.294 seconds. For Slow refresh times > 4.294 secs for STM timer, arithmetic overflow will occur and incorrect timer values would be configured.

Work around:

Customer can use one of the workarounds:

- Configure GTM timer instead of STM timer

- If STM timer is used, maximum refresh time for SLOW mode shall be 4.294 seconds.

Impacted Release(s): 1.10.0, 1.30.0

4 Safety topics v3.0

This section lists safety anomalies and safety related updates related to production releases and maintenance releases.

4.1 HW safety manual

4.1.1 0000053912-9009

Issue description: Impact analysis of AURIX TC3xx Safety Manual 1.05 to existing production releases.

Impact: Additional information related to AoU is documented in 0000053912-8818. No other impacts.

Work around: See issue description of 0000053912-8818.

Impacted Release(s): 1.10.0, 1.30.0.

5 Known issues v2.0

5.1 ADC

5.1.1 0000053912-7242

Issue description: AdcChannelLowLimit description in MCAL UM is confusing.

Impact: UM description for AdcChannelLowLimit parameter is wrong. I.e. Value has to be greater than or equal to AdcChannelLowLimit. However no functional impact.

Work around:

UM description for AdcChannelLowLimit parameter should be read as follows:

Parameter defines the lower limit used for limit checking.

1. This parameter is configurable only if AdcChannelLimitCheck is set to TRUE, and AdcChannelRangeSelect is not equal to 'ADC_RANGE_OVER_HIGH'.

2. AdcChannelLowLimit value has to be less than or equal to AdcChannelHighLimit.

The default and maximum value of this parameter is added based on the 12-bit ADC converters value supported by the hardware.

Impacted Release(s): Impacted Release(s): Impacted Release(s): 1.10.0.

5.1.2 0000053912-7580

Issue description: Config pointer passed in Adc_InitCheck API is not used for checking the correct initialization of ADC driver.

Impact: Validation of the input Config pointer isn't considered and Adc_InitCheck API will return E_OK incorrectly.

Work around: None.

Impacted Release(s): Impacted Release(s): Impacted Release(s): 1.10.0.

5.2 All Modules

5.2.1 0000053912-7100

Issue description: In <Mod>_Bswmd.arxml signed values are not supported for enum data types.

Impact: Signed values can’t be used for enum data type.

Work around: Customer to use only unsigned values for enum data types.

Impacted Release(s): Impacted Release(s): Impacted Release(s): 1.10.0.

5.2.2 0000053912-8516

Issue description: RTE generation issues possible due to invalid / missing information in BswMD ARXML.

Impact: Customer cannot generate RTE with Mentor RTE tool because of the invalid/missing information used in BSWMD ARXML. Impacted drivers are DSADC, MCU, ADC, PWM, ICU, WDG, GPT, OCU, HSSL, I2C, SPI, CanTrcv_17_V9251 and CanTrcv_17_W9255.

Work around: No workaround available.

Impacted Release(s): 1.10.0.

5.3 CAN

5.3.1 0000053912-7284

Issue description: Duplication of SWPDU ID on triggering CAN_Write() from same dedicated HTH (INTERRUPT and POLLING).

Impact: When Can_Write is triggered at the end of transmission, a notification is provided to upper layer for successful transmission. In this scenario where message is successfully transmitted on bus and notification is delayed due to other higher priority interrupts and in mean time a Can_Write request is provided on the same HTH, previous PDU id will be overwritten by the new request due to which two notifications will be obtained for last message being transmitted.

Work around: Successive Can_Write on a same dedicated HTH has to trigger only after successful notification is obtained to upper layer.

Impacted Release(s): 1.10.0.

5.3.2 0000053912-7285

Issue description: Unexpected acceptance of Can_17_McmCan_Write during execution of Can_17_McmCan_lActivateIcom.

Impact: When Icom is enabled / disabled using the API Can_17_McmCan_SetIcomConfiguration, controller is initialized and filters are re-configured during which messages should not be accepted for transmission. Since the controller is re-initialized, behavior of the hardware will not be predictable and is undefined in this state, so possibility of message not getting transmitted is high.

Work around: Controller needs to be in stopped state by using Can_17_McmCan_SetControllerMode API and Can_17_McmCan_SetIcomConfiguration API to be used for enabling / disabling Icom. Application to make sure that messages are requested to be transmitted only after successful Icom enable / disable.

Impacted Release(s): 1.10.0.

5.3.3 0000053912-7295

Issue description: Clearing of Busoff interrupt flag is missed in certain conditions.

Known issues v2.0

Impact: In Case of Icom feature is enabled through configuration, Icom(Can_17_McmCan_SetIcomConfiguration) is not enabled and busoff reporting is disabled (CanIcomWakeOnBusOff), bus-off interrupt flag (IR.BO) will not be cleared leading to not getting successive bus-off interrupt.

Work around: Disable complete Icom feature by setting the value of CanPublicIcomSupport to FALSE.

Impacted Release(s): 1.10.0.

5.3.4 0000053912-7299

Issue description: Unintended bitwise access, missing timeout monitoring and global variable update sequence is not as expected in CAN Driver.

Impact:

#a. Can_Write API: BAR register updated bit-wise, we have a remote chance to update rest of the bits though transmission is completed in background if we do a bit-wise update. This may lead to a retransmission of same message twice. However this is a very remote possibility.

#b. Can_17_McmCan_SetIcomConfiguration: It has been observed that in this function when clearing / setting INIT, CCE bits timeout is not implemented. These needs to be added to make sure that the bits are SET / clear as intended and then proceed with functionality. No Impact to user is observed but this is the recommended practice.

#c, #d. Can_17_McmCan_SetIcomConfiguration: Certain global variables / update of global variables sequences were not proper due to which Can_Write and Can_17_McmCan_SetIcomConfiguration API had certain race around condition leading to un-predictable software behavior.

Work around:

- None for impact #a
- None for impact #b

• Workaround for #c & #d. Controller needs to be in stopped state by using Can_17_McmCan_SetControllerMode API and Can_17_McmCan_SetIcomConfiguration API to be used for enabling / disabling Icom. Application to make sure that messages are requested to be transmitted only after successful Icom enable / disable.

Impacted Release(s): 1.10.0.

5.3.5 0000053912-7620

Issue description: CAN RX message indications not received after resuming from RXfull and CAN controller mode put to stop.

Impact: If interrupts are disabled and more and more messages are received setting the FIFO to full, however in this case, watermark / full interrupt bits would be SET in interrupt register. When CAN controller is put to STOP and then to START mode though CAN controller as such is reset, IR bits would remain SET and is not cleared by ISR due to watermark check in ISR code. In this condition user will experience that no further RX ISR will be triggered and controller will be held in stand-still state.

Known issues v2.0

Work around: Can_17_McmCan_SetControllerMode API to move to STOP / START state to be performed only when no pending interrupts are to be processed.

Impacted Release(s): 1.0.0.

5.3.6 0000053912-7535

Issue description: A2GT-PRQ-4559 deviated for mixed mode implementation.

Impact: If watermark interrupt is missed due to messages getting received when processing the RX interrupt, upper layer may be notified with callback on reception of message.

Work around: When polling mode / Mixed mode is not used Can_17_McmCan_MainFunction_Read should not be called from the scheduler.

Impacted Release(s): 1.10.0, 1.30.0.

5.4 DIO

5.4.1 0000053912-8827

Issue description: P22.6 and P22.7 cannot be configured in TC37x and TC35x devices.

Impact: For DIO module, customer will not be able to configure the available port pins 22.6 and 22.7.

Work around: No workaround available. Customer can use the patch: "MC-ISAR_AS42x_TC3xx_1.30.0_Patch_1.zip".

Impacted Release(s): 1.30.0

5.5 Ethernet

5.5.1 0000053912-4810

Issue description: Transmission is failing intermittently in 10Mbps mode.

Impact: Ethernet packet transmission fails in RGMII/10 Mbps mode intermittently. This behavior is observed only when the global time stamp through the parameter 'EthGlobalTimeSupport ' is enabled.

Hint - If the time stamp feature in not enabled or the RGMII is not configured in 10 Mbps, then this issue is not observed.

Work around: Disable time stamp feature through the parameter 'EthGlobalTimeSupport '.

Impacted Release(s): 1.10.0, 1.30.0.

5.5.2 0000053912-8281

Issue description: VLAN packet transmission with data size of 1500 is not supported.

Impact: VLAN tagged packet with data size of 1500 cannot be transmitted using ETHERNET driver.

Known issues v2.0

Work around: No workaround available.

Impacted Release(s): 1.10.0, 1.30.0.

5.5.1 0000053912-7079

Issue description: Variation Point not supported.

Impact: Variation point support is not available for customers to use.

Work around: None

Impacted Release(s): 1.10.0.

5.6 FLS

5.6.1 0000053912-7407

Issue description: FLS driver status and Job Result not set when FLS_17_DMU_E_TIMEOUT DET/SE is raised by Fls_17_Dmu_MainFunction.

Impact: Unintended timeout DET may be reported.

Work around: To avoid unintended timeout DET, the user has to ensure that calling frequency of Fls_17_Dmu_MainFunction is greater than or equal to 200 us. (Configuration parameter - FlsCallCycle).

Impacted Release(s): Impacted Release(s): Impacted Release(s): 1.10.0.

5.6.2 0000053912-8037

Issue description: During Flash prog/erase operation, if the flash hardware remains busy, operation error is not handled.

Impact: Operation error is not detected and reported, but the timeout DET is reported.

Work around: During runtime the timeout DET will be reported, in which case a system reset must be applied.

Impacted Release(s): 1.10.0.

5.6.3 0000053912-8330

Issue description: Compile time error name if FLs_InitCheck not selected is not named correctly.

Impact: Compilation / linker error may occur when FlsInitCheck parameter in configuration is enabled.

Work around: User has to ensure that the configuration parameter FlsInitCheck is enabled if an Fls_17_Dmu_InitCheck call is being made in the code.

Impacted Release(s): 1.10.0, 1.30.0.

5.7 FLS loader

5.7.1 0000053912-7697

Issue description: FlsLoader_Write() is failing for DFlash when Executed with McuFSIFrequency at 20MHz.

Impact: For FSI frequencies other than 100 MHz, unintended timeout for write or erase operation may occur.

Work around: To avoid unintended timeouts, FSI frequency shall be configured at 100MHz.

Impacted Release(s): 1.10.0.

5.7.2 0000053912-8081

Issue description: Possibility of incorrect program flow while checking busy status.

Impact: Checking of the busy status, if done too early might reflect a wrong status and cause incorrect program flow.

Work around: Delay to be added after program and erase command sequence as per HW UM (v1.2.0 onwards).

Impacted Release(s): 1.10.0.

5.7.3 0000053912-8089

Issue description: During Flash prog/erase operation, if the flash hardware remains busy, operation error is not handled.

Impact: Operation error is not detected and reported, but the timeout DET is reported.

Work around: During runtime the timeout DET will be reported, in which case a system reset must be applied.

Impacted Release(s): 1.10.0.

5.8 Flexray

5.8.1 0000053912-8320

Issue description: Potential issue in macro "FR_17_ERAY_MSG_BUFF_COUNT_MAX_0".

Impact: The pre-compile macro FR_17_ERAY_MSG_BUFF_COUNT_MAX_0/

FR_17_ERAY_MSG_BUFF_COUNT_MAX_1 generated in Fr_17_Eray_Cfg.h considers the LPdu count only in the present configuration and not the maximum value across all post-build configurations.

Work around: By configuring the variant which is having maximum number of configured LPdus as the last one, the macro FR_17_ERAY_MSG_BUFF_COUNT_MAX_0/FR_17_ERAY_MSG_BUFF_COUNT_MAX_1 will be generated with max number of LPdu count. However user has to verify this manually by checking the macro value.

Impacted Release(s): Impacted Release(s): Impacted Release(s): 1.10.0, 1.30.0.

5.9 General

5.9.1 0000053912-7985

Issue description: RSM tool not reporting all functions for a module.

Impact: Functions with higher complexity may exist, higher than the release criteria.

Work around: User can run code complexity tool, other than RSM tool for recheck.

Impacted Release(s): 1.10.0

5.9.2 0000053912-8948

Issue description: Resource properties issues in TC37x.

Impact:

Impact on PWM or OCU modules:

TC375 device: Customer is not allowed to configure GTM TOUT configurations for port pins PORT21_PIN6, PORT21_PIN7 and PORT11_PIN6.

TC377 device: Customer is not allowed to configure GTM TOUT configurations for port pins PORT21_PIN6 and PORT21_PIN7.

TC377_ED device: Customer is not allowed to configure GTM TOUT configurations for port pins PORT21_PIN6 and PORT21_PIN7.

TC377_ED_EX device: Customer is not allowed to configure GTM TOUT configurations for port pins ORT21_PIN6 and PORT21_PIN7. Customer should not configure the PORT23_PIN0 TOUT as this pin does not exist on this device.

TC375_ED device: Customer is not allowed to configure GTM TOUT configurations for port pins PORT21_PIN6, PORT11_PIN6 and PORT21_PIN7.

Impact on LIN and UART module:

TC377_ED_EX: Customer cannot configure the ASCLIN RX line for any of the following pins:

SELECT_C_PORT1_PIN8, SELECT_E_PORT13_PIN11, SELECT_E_PORT33_PIN6, SELECT_H_PORT13_PIN12, SELECT_B_PORT34_PIN02, SELECT_D_PORT14_PIN15, SELECT_B_PORT01_PIN0, SELECT_D_PORT10_PIN9, SELECT_A_PORT14_PIN15, SELECT_B_PORT01_PIN8, SELECT_D_PORT13_PIN11

Impact on PORT module:

TC377_ED:

- P22.6 and P22.7 cannot be used

- P40.10 PCSR feature cannot be used

Known issues v2.0

- Port22 and Port23 PCSR pins cannot be configured

- User will not be able to use PDISC support for P40.4, P40.10, P40.11, P40.12

- User will not be able to select Port23 pin 5 fast pin

TC377_ED_EX:

- The complete functionality of P23.0 pin cannot be used.

TC377_ED_EX:

- User will not be able to use Pin channel support for P22.6 and P22.7

- User will not be able to use the P22.6 and P22.7 pin for PCSR functionality

- Analog pin support for Port40 pin 4,10,11,12 added, user will not be able use this pins for DISC configuration

TC375_ED:

- P23.2, 23.3, 23.4 PCSR feature cannot be used

Impact on Dio Module:

TC377_ED_EX: The complete functionality of P23.0 pin cannot be used.

T356_ADAS: P14.6 and P15.6 cannot be used

TC377_ED, TC377, TC377_ED_EX: P22.6 and P22.7 cannot be used

Impact on Eth Module:

TC375, TC375_ED: User will not be able to configure 10 Mbps speed in RMII mode.

Impact on SENT module:

TC375 and TC375_ED: P32.5 and P32.7 pins cannot be configured

Impact on CAN module:

TC377_ED_EX: selects the incorrectly mapped CANxx_RXDC pin for the controller with address 0xF0218100, the CAN controller receive functionality will not work as expected. For this device and controller any of the other available options must be used.

Work around: No workaround available.

Customer can use the patch: "MC-ISAR_AS42x_TC3xx_1.30.0_Patch_1.zip" available in MyInfineon.

Impacted Release(s): 1.30.0

5.10 HSSL

5.10.1 0000053912-8559

Issue description: Wrong Memmap section used.

Impact: No functional impact is seen, however there are two behaviors as captured below

1. Instead of storing the initialized const variable in flash it utilizes the RAM space to store.

2. Single RAM variable is initialized though it can be kept as cleared RAM variable.

Work around: No workaround available.

Impacted Release(s): 1.30.0.

5.11 I2C

5.11.1 0000053912-7409

Issue description: Async Read/Write operation is not working after I2c_AsyncRead API is called with data size more than 4 bytes.

Impact: I2C_AsyncRead() service cannot be used to read more than 4 bytes of data from the slave device.

Work around: For reading the data from the slave, application shall use API I2c_SyncRead().

Impacted Release(s): 1.10.0.

5.11.2 0000053912-9027

Issue description: I2C configure parameter "I2cFastModeSclLowLength" is incorrectly generated.

Impact: I2C configure parameter "I2cFastModeSclLowLength" is generated as bit21~bit28, but according to the user manual it should be in bit24~bit31.

Work around: No workaround. As I2C is demo code, customer to configure the parameter as per hardware user manual.

Impacted Release(s): 1.10.0, 1.30.0.

5.11.3 0000053912-7801

Issue description: Memory mapping naming for configuration is incorrect.

Impact: Since I2C is not multicore, all memory sections names should be defined with core scope as LOCAL. But I2C implementation violates this rule.

Work around: Memory mapping for configuration data has to be changed in files(I2c_PBcfg.c and I2c_PBcfg.h) as follows:

Known issues v2.0

1. From "I2C_START_SEC_CONFIG_DATA_QM_GLOBAL_UNSPECIFIED" to "I2C_START_SEC_CONFIG_DATA_QM_LOCAL_UNSPECIFIED".

2. From "I2C_STOP_SEC_CONFIG_DATA_QM_GLOBAL_UNSPECIFIED" to "I2C_STOP_SEC_CONFIG_DATA_QM_LOCAL_UNSPECIFIED".

Impacted Release(s): 1.10.0.

5.12 ICU

5.12.1 0000053912-8327

Issue description: Invalid configuration check if variation point is enabled.

Impact: The configuration tool may wrongly restrict configuration across variation point configurations for below pre-compile configuration parameters:

- IcuGetInputStateApi

- IcuGetDutyCycleValuesApi

- IcuGetTimeElapsedApi

- IcuEnableWakeupApi

- IcuEdgeDetectApi

Below error may be thrown due to difference of ICU modes across valid variation point configurations:

- For edge detect/signal measurement:

-- IcuGetInputStateApi will be forced to be set to false in a variation where no channels are associated but is required to be set to true for another variant where channels are associated.

- For duty cycle measurement:

-- IcuGetDutyCycleValuesApi will be forced to be set to false in a variation where no channels are associated but is required to be set to true for another variant where channels are associated.

- For signal measurement (non dutycycle):

-- IcuGetTimeElapsedApi will be forced to be set to false in a variation where no channels are associated but is required to be set to true for another variant where channels are associated.

- For edge detection only:

-- IcuEnableWakeupApi and IcuEdgeDetectApi will be forced to be set to false in a variation where no channels are associated but is required to be set to true for another variant where channels are associated.

Known issues v2.0

Work around: For variation point configuration, if any of the below configuration parameters is set to True, then at least one ICU channel must be associated for that ICU mode across variation point configurations :

- IcuGetInputStateApi

- IcuGetDutyCycleValuesApi

- IcuGetTimeElapsedApi

- IcuEnableWakeupApi

- IcuEdgeDetectApi

Impacted Release(s): 1.10.0, 1.30.0.

5.12.2 0000053912-8361

Issue description: Post-Build Variant Multiplicity needs to be changed to TRUE for Edge Detect, Signal Measurement and Time Stamp Containers.

Impact: Below ICU configuration containers do not support variation point:

- IcuSignalEdgeDetection

- IcuSignalMeasurement

- IcuTimestampMeasurement

- IcuWakeup.

Work around: No workaround available.

Impacted Release(s): 1.10.0, 1.30.0.

5.13 MCALLIB

5.13.1 0000053912-8083

Issue description: McalLib ARXML file issue results in RTE generation issue with Mentor RTE tool..

Impact: Customer cannot generate RTE with Mentor RTE tool because of the invalid reference types used in BSWMD ARXML.

Work around: None.

Impacted Release(s): 1.10.0.

5.14 MCU

5.14.1 0000053912-7423

Issue description: Tresos allows invalid FSI2 Div Update in CCUCON0 Register.

Known issues v2.0

Impact: Incorrect divider values generated in Mcu_PBCfg.c for FSI and FSI2 clocks if SRI frequency is less than PLL0 frequency.

Work around: SRI frequency should be equal to PLL0 frequency.

Note: No workaround possible if SRI frequency is less than PLL0 frequency.

Impacted Release(s): 1.10.0.

5.14.2 0000053912-7774

Issue description: Code Sequence issue in Mcu_17_Gtm_AtomChannelShadowTransfer.

Impact:

From MCAL perspective,

- No impact during driver initialization, only for runtime APIs

- Only ADC driver calls Mcu_17_Gtm_AtomChannelShadowTransfer() in Adc_EnableHardwareTrigger() and Adc_StartGroupConversion() at runtime. If User calls the above mentioned ADC APIs in a re-entrant manner, deadlock may occur and Spinlock might never be acquired by the re-entrant API.

From MCU GTM library's perspective, if Mcu_17_Gtm_AtomChannelShadowTransfer() is called in a re-entrant manner, deadlock may occur and Spinlock might never be acquired by the re-entrant API.

Work around: User can use any one of the workarounds:

1. The APIs Adc_EnableHardwareTrigger(), Adc_StartGroupConversion() or Mcu_17_Gtm_AtomChannelShadowTransfer() should be treated as non-re-entrant APIs.

2. User shall disable interrupts before invoking APIs Adc_EnableHardwareTrigger(), Adc_StartGroupConversion() or Mcu_17_Gtm_AtomChannelShadowTransfer().

Impacted Release(s): 1.10.0.

5.14.3 0000053912-8072

Issue description: Selecting external input for oscillator source will generate wrong OSCVAL value.

Impact: To detect malfunction of oscillator, oscillator watchdog monitors the actual incoming clock frequency Fosc. The expected input frequency of Fosc is selected through OSCCON.OSCVAL. If the Oscillator mode is selected as External Input Clock mode, OSCVAL is wrongly configured as 0. This may cause SMU Oscillator watchdog alarms even though there is no malfunction of oscillator.

Work around: SMU Oscillator watchdog alarms should not be enabled if Oscillator mode is selected as External Input Clock mode. If customer needs this safety measure, there are no other workarounds.

Impacted Release(s): 1.10.0.

5.14.4 0000053912-7108

Issue description: fSource2 is mapped to wrong Tresos Parameter in User manual.

Impact: The configuration parameter McuClockReferencePointFrequency2 has a typo error in the UM description and may lead to confusion for customer.

Work around: McuClockReferencePointFrequency2 to be treated as fSOURCE2.

Impacted Release(s): 1.10.0, 1.30.0

5.14.5 0000053912-8800

Issue description: Generation error when MSC frequency is set to 0 while source frequency is not disabled.

Impact: Configuration generation error will occur when McuMscClockSourceSelection != MSC_CLOCK_SOURCE_DISABLED_SEL0 and McuMscFrequency = 0.

Work around: Customer shall configure one of the workarounds:
1) If MSC clock is used, then McuMscFrequency shall be > 0 if McuMscClockSourceSelection != MSC_CLOCK_SOURCE_DISABLED_SEL0
2) If MSC clock is not used, McuMscClockSourceSelection shall be set to MSC_CLOCK_SOURCE_DISABLED_SEL0.

Impacted Release(s): 1.10.0, 1.30.0

5.15 OCU

5.15.1 0000053912-9015

Issue description: BSWMD - Module Dependency Section is incorrect.

Impact: The BSW-MODULE-DEPENDENCY for Mcu interfaces are missing in the BSWMD file. The missing interfaces are:
Mcu_17_Gtm_AtomChEndisCtrlUpdate
Mcu_17_Gtm_AtomChEndisStatUpdate
Mcu_17_Gtm_AtomChInitCheck
Mcu_17_Gtm_AtomChOutEnCtrlUpdate
Mcu_17_Gtm_AtomChOutEnStatUpdate
Mcu_17_Gtm_AtomChUpdateEnDis
Mcu_17_Gtm_AtomChannelDeInit
Mcu_17_Gtm_AtomChannelDisable
Mcu_17_Gtm_AtomChannelShadowTransfer
Mcu_17_Gtm_TomChInitCheck
Mcu_17_Gtm_TomChUpdateEnDis
Mcu_17_Gtm_TomChannelDisable
Mcu_17_Gtm_TomChannelShadowTransfer.

Work around: User shall modify the generated ARXML file by adding the following missed sections:

1) Under <SHORT-NAME>McuDependency</SHORT-NAME> tag, add missed Mcu Timer APIs entries under <REQUIRED-ENTRYS> tag:

Known issues v2.0

<BSW-MODULE-ENTRY-REF-CONDITIONAL>

<BSW-MODULE-ENTRY-REF DEST="BSW-MODULE-ENTRY">/AUTOSAR_Mcu/BswModuleEntrys/Mcu_17_Gtm_AtomChEndisCtrlUpdate</BSW-MODULE-ENTRY-REF>

</BSW-MODULE-ENTRY-REF-CONDITIONAL>

<BSW-MODULE-ENTRY-REF-CONDITIONAL>

<BSW-MODULE-ENTRY-REF DEST="BSW-MODULE-ENTRY">/AUTOSAR_Mcu/BswModuleEntrys/Mcu_17_Gtm_AtomChEndisStatUpdate</BSW-MODULE-ENTRY-REF>

</BSW-MODULE-ENTRY-REF-CONDITIONAL>

<BSW-MODULE-ENTRY-REF-CONDITIONAL>

<BSW-MODULE-ENTRY-REF DEST="BSW-MODULE-ENTRY">/AUTOSAR_Mcu/BswModuleEntrys/Mcu_17_Gtm_AtomChInitCheck</BSW-MODULE-ENTRY-REF>

</BSW-MODULE-ENTRY-REF-CONDITIONAL>

<BSW-MODULE-ENTRY-REF-CONDITIONAL>

<BSW-MODULE-ENTRY-REF DEST="BSW-MODULE-ENTRY">/AUTOSAR_Mcu/BswModuleEntrys/Mcu_17_Gtm_AtomChOutEnCtrlUpdate</BSW-MODULE-ENTRY-REF>

</BSW-MODULE-ENTRY-REF-CONDITIONAL>

<BSW-MODULE-ENTRY-REF-CONDITIONAL>

<BSW-MODULE-ENTRY-REF DEST="BSW-MODULE-ENTRY">/AUTOSAR_Mcu/BswModuleEntrys/Mcu_17_Gtm_AtomChOutEnStatUpdate</BSW-MODULE-ENTRY-REF>

</BSW-MODULE-ENTRY-REF-CONDITIONAL>

<BSW-MODULE-ENTRY-REF-CONDITIONAL>

<BSW-MODULE-ENTRY-REF DEST="BSW-MODULE-ENTRY">/AUTOSAR_Mcu/BswModuleEntrys/Mcu_17_Gtm_AtomChUpdateEnDis</BSW-MODULE-ENTRY-REF>

</BSW-MODULE-ENTRY-REF-CONDITIONAL>

<BSW-MODULE-ENTRY-REF-CONDITIONAL>

<BSW-MODULE-ENTRY-REF DEST="BSW-MODULE-ENTRY">/AUTOSAR_Mcu/BswModuleEntrys/Mcu_17_Gtm_AtomChannelDeInit</BSW-MODULE-ENTRY-REF>

Known issues v2.0

```
            </BSW-MODULE-ENTRY-REF-CONDITIONAL>

            <BSW-MODULE-ENTRY-REF-CONDITIONAL>

             <BSW-MODULE-ENTRY-REF DEST="BSW-MODULE-
ENTRY">/AUTOSAR_Mcu/BswModuleEntrys/Mcu_17_Gtm_AtomChannelDisable</BSW-MODULE-ENTRY-REF>

            </BSW-MODULE-ENTRY-REF-CONDITIONAL>

             <BSW-MODULE-ENTRY-REF-CONDITIONAL>

            <BSW-MODULE-ENTRY-REF DEST="BSW-MODULE-
ENTRY">/AUTOSAR_Mcu/BswModuleEntrys/Mcu_17_Gtm_AtomChannelShadowTransfer</BSW-MODULE-
ENTRY-REF>

             </BSW-MODULE-ENTRY-REF-CONDITIONAL>

            <BSW-MODULE-ENTRY-REF-CONDITIONAL>

             <BSW-MODULE-ENTRY-REF DEST="BSW-MODULE-
ENTRY">/AUTOSAR_Mcu/BswModuleEntrys/Mcu_17_Gtm_TomChInitCheck</BSW-MODULE-ENTRY-REF>

            </BSW-MODULE-ENTRY-REF-CONDITIONAL>

            <BSW-MODULE-ENTRY-REF-CONDITIONAL>

             <BSW-MODULE-ENTRY-REF DEST="BSW-MODULE-
ENTRY">/AUTOSAR_Mcu/BswModuleEntrys/Mcu_17_Gtm_TomChUpdateEnDis</BSW-MODULE-ENTRY-REF>

            </BSW-MODULE-ENTRY-REF-CONDITIONAL>

            <BSW-MODULE-ENTRY-REF-CONDITIONAL>

             <BSW-MODULE-ENTRY-REF DEST="BSW-MODULE-
ENTRY">/AUTOSAR_Mcu/BswModuleEntrys/Mcu_17_Gtm_TomChannelDisable</BSW-MODULE-ENTRY-REF>

            </BSW-MODULE-ENTRY-REF-CONDITIONAL>

            <BSW-MODULE-ENTRY-REF-CONDITIONAL>

             <BSW-MODULE-ENTRY-REF DEST="BSW-MODULE-
ENTRY">/AUTOSAR_Mcu/BswModuleEntrys/Mcu_17_Gtm_TomChannelShadowTransfer</BSW-MODULE-
ENTRY-REF>

            </BSW-MODULE-ENTRY-REF-CONDITIONAL>
```

2) Under <SHORT-NAME>McalLibDependency</SHORT-NAME> tag, add below entry:

```
          <BSW-MODULE-DEPENDENCY>

           <SHORT-NAME>McalSafetyErrorDependency</SHORT-NAME>
```

```
        <TARGET-MODULE-ID>255</TARGET-MODULE-ID>

        <REQUIRED-ENTRYS>

         <BSW-MODULE-ENTRY-REF-CONDITIONAL>

          <BSW-MODULE-ENTRY-REF DEST="BSW-MODULE-
ENTRY">/AUTOSAR_Stub/BswModuleEntrys/Mcal_ReportSafetyError</BSW-MODULE-ENTRY-REF>

         </BSW-MODULE-ENTRY-REF-CONDITIONAL>

        </REQUIRED-ENTRYS>

       </BSW-MODULE-DEPENDENCY>
```

Impacted Release(s): 1.30.0.

5.16 PORT

5.16.1 0000053912-7526

Issue description: PortPinMode configuration for Port 40 and Port41 is not available for customers who do not use Tresos as the configuration tool.

Impact: Tresos tool does not export the PortPinMode container information in the AUTOSAR format arxml file for Ports 40 and 41 only. Customers who are using any other configuration tool apart from Tresos, this information will be missing.

Work around: After importing the generated arxml file, customer shall manually add the Port 40 and Port 41 configurations in the AUTOSAR configuration tool.

Impacted Release(s): 1.10.0.

5.16.2 0000053912-7344

Issue description: Port_SetPinDirection range check is missing for Direction input parameter.

Impact: Range check is not done for input parameter Direction and no error shall be reported if wrong values are passed. If wrong value is passed, the direction will made as Input.

Work around: User shall ensure PORT_PIN_IN (0) or PORT_PIN_OUT (0x80) is passed for the input parameter Direction in Port_SetPinDirection API.

Note: for 1.30.0, this limitation is documented in UM.

Impacted Release(s): 1.10.0.

5.17 PWM

5.17.1 0000053912-7131

Issue description: TOM_CH_IRQ_NOTIFY Register is not cleared after Pwm_DeInit.

Known issues v2.0

Impact: Spurious Interrupt might occur while Pwm_17_GtmCcu6_Deinit for the active PWM channels, before they are de-initialized. However no functional impact.

Work around: User should ignore the spurious PWM interrupts after invocation of Pwm_17_GtmCcu6_Deinit.

Impacted Release(s): 1.10.0.

5.17.2 0000053912-8454

Issue description: Glitch in Pwm_Init if default TOUT is used for other TOM/ATOM channels.

Impact: Initialization of one of the GTM PWM channels may trigger a glitch on the output pins of other TOUTSEL/S. The scenario occurs when the affected TOUTSEL/s holds a default value (HW reset value) such that the channel under initialization is driving the affected TOUTSEL (in turn the port pin also). Hence, during the initialization phase a glitch is observed on such channels.

Work around: In order to avoid such a glitch on the port pins, the user may follow one of the following workarounds:
• To set the port pins used by the PWM channels as input during the initialization phase of the PWM driver. After completion of the initialization, the port pin's ALT mode can be restored to PWM.
• To set the port pins used for PWM channels as "Output Low" or "Output High" during the initialization phase of the PWM driver. After completion of the initialization, the port pin's ALT mode can be restored to PWM.

Impacted Release(s): 1.10.0, 1.30.0.

5.18 SMU

5.18.1 0000053912-7759

Issue description: Smu_RegisterMonitor() returns E_OK even when fault is detected in a safety flip-flop protected register.

Impact: UM Description of Smu_RegisterMonitor() API is ambiguous with respect to return value and output parameter RegMonResult. However no functional impact.

Work around: Description of Smu_RegisterMonitor() API should be read as follows:

The purpose of the Smu_RegisterMonitor() API is to provide the initialization, execution and termination of the Safety Flip Flop tests to be executed for different modules as enabled in input parameter RegMonPtr.

The prerequisites for Register monitor test shall be taken care by the user as mentioned in the HW UM before invoking the Smu_RegisterMonitor() API.

The API returns E_OK only if the test execution was completed successfully irrespective of SFF failures.

The parameter RegMonResult is populated based on the result of SFF tests run for the enabled modules after checking the RMEF.

RegMonResult needs to be checked only when Smu_RegisterMonitor() returns E_OK.

Known issues v2.0

Impacted Release(s): 1.10.0.

5.18.2 0000053912-8463

Issue description: Register Monitor Test Timeout for different IOM frequency.

Impact: For IOM Frequency < 1MHz, Smu_RegisterMonitor() API may report a DEM failure because the IOM register monitor test status has not completed within the desired time. The timeout value was derived based on Safety Manual 1.04.

Work around: Customer shall ensure IOM frequency >= 1MHz if IOM Functional block is configured for Register monitoring test in Smu_RegisterMonitor() API.

Impacted Release(s): 1.10.0, 1.30.0.

5.19 SPI

5.19.1 0000053912-7235

Issue description: Implementation of Spi_ControlLoopBack is not robust.

Impact:

a. Spi_kernelLoopBackState variable is not partitioned across cores, so if ASIL partition is done for variables allocated to cores this variable cannot be partitioned since it is allocated to single core.

b. Loopback mode can be enabled / disabled when transmission is in progress.

Work around:

a. None

b. Spi_ControlLoopBack API shall not be invoked while transmission is in progress.

Note: Application to make sure that the Spi_ControlLoopBack API to be called for enabling / disabling the loopback on 'sequence end notification', when complete transmission of sequence is done.

Impacted Release(s): 1.10.0.

5.19.2 0000053912-7669

Issue description: Calling SchM_Exit_Spi_Queue_Update() twice when SPI_SEQ_PENDING in Async_Transmit causing error in OS.

Impact: Un-predictable behavior. However this can be observed when DET is enabled and DET will be reported if such scenario occurs.

Work around: Spi_GetSequenceResult API to be used to check the status of sequence 'is not in SPI_SEQ_PENDING' before calling successive transmit of same sequence.

Impacted Release(s): 1.10.0.

5.19.3 0000053912-9038

Issue description: For GetStatus() API, SPI_E_UNINIT DET reporting is not documented in User manual.

Impact: If customers enable the DET and call GetStatus() API, then SPI_E_UNINIT DET will be reported, though it is not documented in the user manual.

Work around: Customers to note that SPI_E_UNINIT DET will be reported in the scenario mentioned. No action is required to be taken as its expected behaviour.

Impacted Release(s): 1.10.0, 1.30.0.

5.19.4 0000053912-8519

Issue description: Parameter SPI_INIT_CHECK_API in Tresos does not influence the code.

Impact: Spi_Initcheck() API is always enabled irrespective of corresponding APIs on-off configuration. However no functional impact.

Work around: No workaround available.

Impacted Release(s): 1.10.0, 1.30.0.

5.19.5 0000053912-9020

Issue description: Reserved bit DMA ADICR is written with 1 instead of 0. This is not as per HW User manual recommendation.

Impact: Reserved bit23 of DMA ADICR register is written with value "1". No impact is seen in MCAL.

Work around: None.

Impacted Release(s): 1.10.0, 1.30.0.

5.20 WDG

5.20.1 0000053912-7168

Issue description: No “DISABLE” action in "Mcu_17_Gtm_TomChannelDeInit."

Impact: The impact is only if Wdg is configured with the GTM timer. The impacted APIs are Wdg_17_Scu_Init(), Wdg_17_Scu_SetMode() and Wdg_17_Scu_SetTriggerCondition(). The first interrupt of the window period will be serviced earlier than the configured interval. The subsequent GTM interrupts for the window shall be serviced within the proper configured interval. However no functional impact foreseen but timing violations can be seen for the first window period.

Work around: No workaround for Wdg_17_Scu_Init(). User shall disable the GTM timer by calling Mcu_17_Gtm_TomChannelDisable() before invoking Wdg_17_Scu_SetTriggerCondition() or Wdg_17_Scu_SetMode() API.

Impacted Release(s): 1.10.0.

5.20.2 0000053912-8790

Issue description: Issue in Wdg driver leading to safety error.

Impact: Undesired Safety error shall be reported with Error Id WDG_17_SCU_E_DRIVER_STATE in the WDG ISR if Wdg_17_Scu_SetTriggerCondition() API is pre-empted by the ISR after Wdg_17_Scu_DriverState is set to BUSY in the Wdg_17_Scu_SetTriggerCondition() API.

Work around: Customer shall disable WDG trigger interrupts before calling Wdg_17_Scu_SetTriggerCondition() API.

Impacted Release(s): 1.10.0, 1.30.0.

6 Safety topics v2.0

This section lists safety anomalies and safety related updates related to production releases and maintenance releases.

6.1 HW safety manual

6.1.1 0000053912-8506

Issue description: Impact analysis of AURIX TC3xx Safety Manual 1.02/1.03 to MCAL 1.10.0 production release.

Impact: No functional or safety impact to product 1.10.0.

Work around: None.

Impacted Release(s): 1.10.0.

7 Known issues v1.0

7.1 ADC

7.1.1 0000053912-6063

Issue description: Safety Error ADC_SE_PARAM_KERNEL is not reported when non available kernel (Within 0-11) is passed as parameter for interrupt handlers.
Impact: No safety error is reported if non-existent kernel ID is passed to ADC ISR routines. ISR exits without any adverse effect.
Work around: User shall ensure that plausible values are passed to the ADC ISR routines.
Impacted Release(s): 1.10.0

7.2 CAN

7.2.1 0000053912-7064

Issue description: CAN messages are lost if Can_17_McmCan_Write() API is invoked for a HTH in re-entrant mode.
Impact: Can_17_McmCan_Write() API behaves as non-reentrant for the re-entrant HTH.
Work around: Can_17_McmCan_Write() shall not be invoked for a HTH in the re-entrant mode.
Impacted Release(s): 1.10.0

7.2.2 0000053912-6838

Issue description: CAN driver provides wrong transmit confirmation to CanIf module.
Impact: If the Can_17_McmCan_Write() API is invoked for a HTH before receiving the transmit confirmation of the previous pending transmit request for the same HTH, the CAN driver may give incorrect transmit notifications.
Work around: Invoke Can_17_McmCan_Write() for a HTH only after receiving the transmit confirmation for the pending request for a HTH.
Impacted Release(s): 1.10.0

7.2.3 0000053912-6701

Issue description: CAN-FD controller cannot use external oscillator as the clock source.
Impact: If the CAN-FD controller is configured to use external oscillator as clock source, then code generator gives an error. Hence CAN-FD controllers cannot use external oscillator as the clock source.
Work around: The CAN-FD controller shall be configured to a clock source other than external oscillator.
Impacted Release(s): 1.10.0

7.3 DIO

7.3.1 0000053912-6170

Issue description: Dio_FlipChannel() API may return incorrect pin level.
Impact: Based on the strength of the pin driver and load capacitance, there may be a delay in flipping the channel. Hence, a wrong pin level may be returned by Dio_FlipChannel().

Known issues v1.0

Work around: After Dio_FlipChannel(), user should call Dio_ReadChannel() API to ensure that the flipping of channel was successful.

Note: Time required to flip the channel is based on the high output load.

Impacted Release(s): 1.10.0

7.4 FLS

7.4.1 0000053912-6598

Issue description: Fls_17_Dmu_Cancel function should reset the internal variables when a job is cancelled. But, currently Fls_17_Dmu_Cancel API does not reset the internal variables when the ongoing job is either an erase or a blank check.

Impact: There is no functional impact. The next request that follows the cancel will set the variables according to the requested job.

Work around: None.

Impacted Release(s): 1.10.0

7.4.2 0000053912-7034

Issue description: FLS status gets set to the initialized in Fls_17_Dmu_Init() even if an operational error (OPER) is present.

Impact: FLS status is set to initialized even if an operational error (OPER) is present when Fls_17_Dmu_Init() executes.

Work around: If during FLS initialization (Fls_17_Dmu_Init) an illegal state notification is received, then the user should perform a system reset.

Impacted Release(s): 1.10.0

7.4.3 0000053912-6912

Issue description: Runtime Errors for timeout are not reported in Fls_17_Dmu_Erase() and Fls_17_Dmu_Write().

Impact: User is not notified of a run time error.

Work around: As the run time error is not reported, the user has to check the return value of the called function. If a run time error occurs, then the return value of the called function will be E_NOT_OK.

Impacted Release(s): 1.10.0

7.4.4 0000053912-6993

Issue description: In FLS standalone mode (without Infineon FEE), ECC errors are not cleared before triggering the write operations on DFLASH (in erase check).

Impact: ECC error is not detected in such a scenario but, PVER error will be detected in case the write/program operation fails. Additionally, if SAFETY or DET is enabled, the above mentioned write will be verified by matching the written data with the data in the source buffer and in case a difference is detected, the write operation fails with FLS_17_DMU_E_VERIFY_WRITE_FAILED DET/SAFETY error.

Work around: Not required.

Impacted Release(s): 1.10.0

7.4.5 0000053912-6543

Issue description: Range for the parameter FlsWaitStateRead is incorrectly documented in the user manual due to a typographical error.
Impact: Wrong information in the user manual. Code is correct.
Work around: Correct range for the parameter FlsWaitStateRead is FLS_17_DMU_WAIT_STATE_READACCESS0 - FLS_17_DMU_WAIT_STATE_READACCESS255.
Impacted Release(s): 1.10.0

7.5 General

7.5.1 0000053912-6784

Issue description: ARXML file cannot be used with Mentor RTE generator.
Impact: Customer cannot generate RTE with Mentor RTE tool because of the invalid reference type used in BSWMD ARXML for 'void' datatype. Impacted drivers are MCU, MCALLIB, FLSLOADER, HSSL, CanTrcv_17_V9251 and CanTrcv_17_W9255.
Work around: User shall modify the generated ARXML file by replacing the following <BASE-TYPE-REF DEST="SW-BASE-TYPE">/AUTOSAR_Platform/ImplementationDataTypes/BaseTypes/void</BASE-TYPE-REF> with <IMPLEMENTATION-DATA-TYPE-REF DEST="IMPLEMENTATION-DATA-TYPE">/AUTOSAR_Platform/ImplementationDataTypes/BaseTypes/void</IMPLEMENTATION-DATA-TYPE-REF>.
Impacted Release(s): 1.10.0

7.5.2 0000053912-7071

Issue description: Negative value check of Enum parameters is missing.
Impact: The driver does comparison checks against enum values considering it as a 32-bit unsigned integer. If user passes a negative value, the comparison fails and results in a wrong control flow. The impacted MCAL drivers are MCU, ICU, OCU and DMA.
Work around: Customer shall pass enum values as 32-bit unsigned integer.
Impacted Release(s): 1.10.0

7.6 Ethernet

7.6.1 0000053912-6166

Issue description: If a frame exceeding the configured buffer size is received further frames cannot be received.
Impact: Ethernet driver stops receiving the frames.
Work around: User of the ETH driver must ensure that the EthCtrlRxBufLenByte parameter is configured with maximum packet size, including the header, as expected in the ETH bus. While configuring EthCtrlRxBufLenByte, the user shall consider broadcast frames also. If the maximum receive packet length is not known during the configuration, user shall configure the EthCtrlRxBufLenByte parameter to 1522.
Impacted Release(s): 1.10.0

7.7 ICU

7.7.1 0000053912-6486

Issue description: GPT12 getinput state for multi-edge detection returning incorrect value. Input state for a GPT12 multi-edge detection channel returns incorrect value.
Impact: Icu_17_TimerIp_GetInputState()provides an invalid input state for multi-edge detection channel if notification is not enabled for the respective channel.
Work around: Channel notification shall be enabled for multi-edge detection channels to ensure that the channel status is read correctly.
Impacted Release(s): 1.10.0

7.7.2 0000053912-6189

Issue description: Icu_17_TimerIP_SetActivationCondition is not setting the detect condition correctly (for ERU), when pre-empted by Enable Edge Detection API.
Impact: Icu_17_TimerIp_SetActivationCondition will have a corrupted active edge configuration if pre-empted by Icu_17_TimerIp_EnableEdgeDetection for that channel. This is applicable only if ERU is configured for that channel in edge detection mode.
Work around: User shall ensure Icu_17_TimerIp_SetActivationCondition is executed in critical section.
Impacted Release(s): 1.10.0

7.7.3 0000053912-6173

Issue description: Icu_17_TimerIp_SetActivationCondition not clearing the channel status (for CCU6 and GPT12), if notification is not enabled.
Impact: Icu_17_TimerIp_SetActivationCondition returns a wrong channel status if invoked with disabled notifications for that channel. This applies only to GPT12 and CCU6.
Work around: Ensure Icu_17_TimerIp_EnableNotification is called before Icu_17_TimerIp_SetActivationCondition for channels associated with GPT12 and CCU6.
Impacted Release(s): 1.10.0

7.8 LIN

7.8.1 0000053912-6547

Issue description: Incorrect reference path to McuClockReferencePointConfig in LIN BMD file.
Impact: Code generation for LIN module fails due to error in reference path to MCU module.
Work around: User has to manually update the LIN BMD file and correct the path as "/AURIX2G/EcucDefs/Mcu/McuModuleConfiguration/McuClockSettingConfig/McuClockReferencePointConfig" for the parameter "LinSysClockRef".
Impacted Release(s): 1.10.0

7.9 MCALLIB

7.9.1 0000053912-7192

Issue description: Incoherent memory read across cores.

Known issues v1.0

Impact: If the LockAddress parameter passed to Mcal_ReleaseSpinlock() is placed in DLMU/DSPR, the value may not be written into the memory but stored in store buffer. Hence, reading from other cores will read the incoherent memory and may timeout to acquire the spinlock even though the acquired core has released it.

Work around:

User can choose one of the below:

- Place the variable in LMU
- Invoke DSYNC() after calling Mcal_ReleaseSpinlock().

Impacted Release(s): 1.10.0

7.10 MCU

7.10.1 0000053912-6712

Issue description: Divider for EXTCLK1 is not generated correctly in Mcu_PBCfg.c.

Impact: Correct frequency for EXTCLK1 is not generated.

Work around: fOut should not be selected for EXTCLK1 in the configuration tool.

Impacted Release(s): 1.10.0

7.10.2 0000053912-6737

Issue description: Wrong ERU EIFR mask generation.

Impact: ERU HW is paired with two ERU channels. If customer selects only one of the ERU pair, a spurious interrupt is issued if an interrupt occurs on the other channel.

Work around: Always ensure both the channels of pairs are allocated/used. Currently only ICU driver uses ERU unit for interrupts.

Impacted Release(s): 1.10.0

7.10.3 0000053912-7108

Issue description: fSource2 is mapped to the wrong Tresos Parameter in MCAL UM.

Impact: The configuration parameter McuClockReferencePointFrequency2 has a typographical error in the basic UM description for MCU driver and may confuse customers. No functional impact.

Work around: Customer should treat McuClockReferencePointFrequency2 as fSource2.

Impacted Release(s): 1.10.0

7.10.4 0000053912-6028

Issue description: InitCheck() for ICU or GPT returns E_NOT_OK if GPT Timer3 and Timer6 have different pre-scalar values.

Impact: Gpt_InitCheck() API or Icu_17_TimerIp_InitCheck() API fails if customer configures GPT Timer3 and Timer6 with different pre-scalar values.

Work around: User can choose one of the below:

- Customer shall configure GPT Timer3 and Timer6 to have the same pre-scalar value.
- Customer shall configure any one of the GPT timers - either Timer3 or Timer6.

Impacted Release(s): 1.10.0

7.11 PORT

7.11.1 0000053912-6762

Issue description: Variation option missing for AUTOSAR parameters.
Impact: Customer cannot configure the AUTOSAR Port parameters PortPinDirectionChangeable as Post Build Variation point.
Work around: No workaround available.
Impacted Release(s): 1.10.0

7.11.2 0000053912-7344

Issue description: Range check missing for parameter Direction in Port_SetPinDirection().
Impact: Range check is not done for input parameter Direction and no error is reported if wrong values are passed. If a wrong value is passed, the pin Direction will be wrongly configured as Input.
Work around: User shall ensure that 0 or 0x80 is passed as the input parameter Direction for Port_SetPinDirection() API.
Impacted Release(s): 1.10.0

7.12 PWM

7.12.1 0000053912-6549

Issue description: Link error when compiling the MCAL in Pwm_17_GtmCcu6.
Impact: Linker error for Pwm_lPolarity could occur for certain combinations of PWM configurations.
Work around: To avoid linker error, enable configuration for any one of the following features:
- PwmDeInitApi
- PwmNotificationSupported
- PwmSetOutputToIdle

Impacted Release(s): 1.10.0

7.12.2 0000053912-6387

Issue description: Pwm_InitCheck() may incorrectly return E_NOT_OK for some CCU6 channel combinations.

Impact: Pwm_InitCheck() incorrectly returns E_NOT_OK if T13 for CCU60 or T12 for CCU61 is configured.

Work around: User shall not configure T13 for CCU60 or T12 for CCU61.

Impacted Release(s): 1.10.0

7.13 SPI

7.13.1 0000053912-6783

Issue description: The SPI driver does not consider the interrupt enable status for spurious interrupt check.
Impact: If any SPI spurious interrupts are triggered in the controller, then the SPI driver will not report safety error SPI_E_SAFETY_SPURIOUS_INTERRUPT and behavior from SPI driver will be undefined.
Work around: User shall ensure that SPI interrupts are checked to be enabled before invoking the SPI interrupt handler.

Known issues v1.0

Impacted Release(s): 1.10.0

7.14 UART

7.14.1 0000053912-6703

Issue description: Over Sampling parameter (UartChanBaudOverSampling) does not cover the complete range supported by the HW.

Impact: Though the possible range for oversampling field in BITCON register is 3 to 15, the values allowed to be configured in the UART driver configuration tool is 8 to 16. Hence, user cannot configure the oversampling values in the range 3 to 7 and also the value 16 is invalid.

Work around:

1. User shall not configure value 16 for UartChanBaudOverSampling.
2. There is no work around to configure the range from 3 to 7.

Impacted Release(s): 1.10.0

7.15 WDG

7.15.1 0000053912-6684

Issue description: DET major version check has an incorrect dependency on "WdgSafetyEnable" parameter.

Impact: Unintended DET check for AUTOSAR major version happens if configuration parameter WdgDevErrorDetect is OFF but WdgSafetyEnable is ON. It should be dependent only when WdgDevErrorDetect is ON.

Work around: If DET is not used in the user environment, user shall include dummy Det.h file with the macro DET_AR_RELEASE_MAJOR_VERSION defined as 4.

Impacted Release(s): 1.10.0

8 Safety topics v1.0

This section lists safety anomalies related to production releases and maintenance releases.

8.1 Safety case

8.1.1 0000053912-7283

Issue description: Incorrect ISO 26262 part number mentioned in 1.10.0 safety case, section 5.3.3.
Impact: It's a typographical error. No functional or safety impact.
Work around: Name of the figure 6 in section 5.3.3 is mentioned as 'Goal: fulfillment of system development requirements according to ISO 26262 Part 6'. Integrators to consider it as 'Goal: fulfillment of system development requirements according to ISO 26262 Part 4'.
Impacted Release(s): 1.10.0

8.2 ISO 26262 Argumentation Sheet

8.2.1 0000053912-7228

Issue description: Method 'error guessing' was incorrectly marked as 'applicable' for unit testing in ISO26262 clauses argumentation sheet (Part 6, Table 11, method 1d).
Impact: Error guessing is not mandatory for ASIL B. In addition, unit test cases for boundary value and equivalence class cover all necessary test cases in the context of unit testing. Hence, there is no functional or safety impact.
Work around: In safety case for 1.10.0, in 'TC3xx_SW_MCAL_ISO26262_Argumentation.xlsx' document, Part 6, Table 11, Method 1d is marked as 'YES'. It must be treated as 'NO'.
Impacted Release(s): 1.10.0

9 HW Derivative specification

This section explains the hardware derivatives supported and their respective property files. Customers must ensure that relevant range checks are implemented and tested as per applicable HW documentation.

9.1 Device support details:

Table 1 Umbrella Device Support TC35xAB/TC37xAA/TC37xED AB/TC38x AD and AE/TC39x BC and BD

AURIX Umbrella device	Name displayed in Tresos Tool	Tresos Property File
SAK-TC356TA-64F300S	TC356_ADAS	AURIX2G_TC356_ADAS.properties
SAK-TC357TT-64F300S	TC357_ADAS	AURIX2G_TC357_ADAS.properties
SAL-TC370TP-96F300	TC377	AURIX2G_TC377.properties
SAL-TC375TP-96F300W	TC375	AURIX2G_TC375.properties
SAL-TC377TP-96F300S	TC377	AURIX2G_TC377.properties
SAL-TC377DP-96F300S	TC377	AURIX2G_TC377.properties
SAL-TC375TE-96F300W	TC375_ED	AURIX2G_TC375_ED.properties
SAL-TC377TX-96F300S	TC377_ED_EX	AURIX2G_TC377_ED.properties
SAL-TC377TE-96F300S	TC377_ED	AURIX2G_TC377_ED.properties
SAL-TC387QP-160F300S	TC387	AURIX2G_TC387.properties
SAK-TC389QP-160F300S	TC389	AURIX2G_TC389.properties
SAK-TC397XE-256F300S	TC397	AURIX2G_TC397.properties
SAK-TC397XT-256F300S[3)]	TC397_ADAS	AURIX2G_TC397_ADAS.properties
SAK-TC399XE-256F300S	TC399	AURIX2G_TC399.properties

Table 2 Marking option device Support for TC35xAB/TC37xAA/TC37xED AA/TC38x AD and AE/TC39x BC and BD[1)]

AURIX Marking option device	Name displayed in Tresos Tool	Tresos Property File
SAK-TC356TH-64F300S	TC356_ADAS	AURIX2G_TC356_ADAS.properties
SAK-TC357TA-64F300S	TC357_ADAS	AURIX2G_TC357_ADAS.properties
SAK-TC357TH-64F300S	TC357_ADAS	AURIX2G_TC357_ADAS.properties
SAK-TC375TP-96F300W	TC375	AURIX2G_TC375.properties
SAK-TC377TP-96F300S	TC377	AURIX2G_TC377.properties
SAK-TC377DP-96F300S	TC377	AURIX2G_TC377.properties
SAK-TC375TE-96F300W	TC375_ED	AURIX2G_TC375_ED.properties
SAK-TC375DP-96F300W	TC375	AURIX2G_TC375.properties
SAL-TC375DP-96F300W	TC375	AURIX2G_TC375.properties
SAK-TC377TX-96F300S	TC377_ED_EX	AURIX2G_TC377_ED.properties
SAK-TC377TX-64F300S	TC377_ED_EX	AURIX2G_TC377_ED.properties
SAL-TC380QP-160F300	TC389	AURIX2G_TC389.properties
SAK-TC387QP-160F300S	TC387	AURIX2G_TC387.properties
SAL-TC387TP-128F300S	TC387	AURIX2G_TC387.properties
SAK-TC387TP-128F300S	TC387	AURIX2G_TC387.properties
SAL-TC387TP-160F300S	TC387	AURIX2G_TC387.properties
SAK-TC387TP-160F300S	TC387	AURIX2G_TC387.properties
SAK-TC387QN-160F300S	TC387	AURIX2G_TC387.properties
SAL-TC389QP-160F300S	TC389	AURIX2G_TC389.properties

SAK-TC389QN-160F300S	TC389	AURIX2G_TC389.properties
SAL-TC397XP-256F300S	TC397	AURIX2G_TC397.properties
SAK-TC397XP-256F300S	TC397	AURIX2G_TC397.properties
SAK-TC397XX-256F300S	TC397	AURIX2G_TC397.properties
SAK-TC397QP-192F300S	TC397	AURIX2G_TC397.properties
SAK-TC397QP-256F300S	TC397	AURIX2G_TC397.properties
SAK-TC397XZ-256F300S	TC397	AURIX2G_TC397.properties
SAL-TC397XE-256F300S	TC397	AURIX2G_TC397.properties
SAK-TC397XM-256F300S	TC397	AURIX2G_TC397.properties
SAL-TC397QP-192F300S	TC397	AURIX2G_TC397.properties
SAL-TC397QP-256F300S	TC397	AURIX2G_TC397.properties
SAL-TC397XZ-256F300S	TC397	AURIX2G_TC397.properties
SAL-TC397XX-256F300S	TC397	AURIX2G_TC397.properties
SAK-TC397XA-256F300S	TC397_ADAS	AURIX2G_TC397_ADAS.properties
SAK-TC397QA-160F300S	TC397_ADAS	AURIX2G_TC397_ADAS.properties
SAL-TC399XX-256F300S	TC399	AURIX2G_TC399.properties
SAL-TC399XP-256F300S	TC399	AURIX2G_TC399.properties
SAK-TC399XP-256F300S	TC399	AURIX2G_TC399.properties
SAK-TC399XX-256F300S	TC399	AURIX2G_TC399.properties
SAL-TC399XE-256F300S	TC399	AURIX2G_TC399.properties

Note:

[1)] For TC38x, TC39x, TC37x, TC37xEXT, TC35x marking option device support, range check has to be imposed by user, and not in the MCAL code.

10 Acronyms, abbreviations and integration support

Please refer to AURIX 2G HW user manual and MC-ISAR_AS422_TC3xx user manual. In case of any queries or support required to implement the work around, contact field application engineers.

Revision History

Date	Version	Description
2019-07-22	v1.0	Reviewed and released for issues reported post first production release until Jun. 21st 2019.
2020-01-21	v2.0	• Updated for issues reported from 22nd Jun. 2019 to 20th Nov. 2019. • Chapter 'HW Derivative specification' updated as per latest HW documentation. • Updated the file name in line with product name. • Issue from RNA v1.0, 0000053912-7344 was updated to enhance the descriptions. Issue 0000053912-7530 was deleted as it had same information as in 0000053912-7697. • Chapter name for JIRA 0000053912-6166 changed from GETH to Ethernet to ensure consistency of driver names.
2020-04-30	v3.0	• Updated for issues reported until 9th Apr. 2020. • Chapter 'HW Derivative specification' updated as per latest HW documentation.
2020-08-06	v4.0	• Updated for issues reported until 16th Jul. 2020. • Issue from RNA v3.0, 0000053912-10645 was updated and added to RNA v4.0 to correct the 'Impacted Releases'.

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AFFECTED MPNS

SAK-TC356TA-64F300S AB
SAK-TC356TD-48F300S AB
SAK-TC356TH-64F300S AB
SAK-TC357TA-64F300S AB
SAK-TC357TC-64F300S AB
SAK-TC357TH-64F300S AB
SAK-TC367DP-48F200S AA
SAK-TC367DP-48F300S AA
SAK-TC367DP-64F300S AA
SAK-TC367V0-64F300S AA
SAK-TC367VB-32F200S AA
SAK-TC375TI-96F300W AA
SAK-TC375TP-96F300W AA
SAK-TC377DP-96F300S AA
SAK-TC377TP-96F300S AA
SAK-TC377TX-64F300S AB
SAK-TC377TX-96F300S AB
SAK-TC387QP-160F300S AD
SAK-TC387QP-160F300S AE
SAK-TC387TP-128F300S AD
SAK-TC387TP-128F300S AE
SAK-TC387TP-128F300S AE
SAK-TC387TP-160F300S AD
SAK-TC387TP-160F300S AE
SAK-TC389QP-160F300S AD
SAK-TC389QP-160F300S AE
SAK-TC397QA-160F300S BC
SAK-TC397QA-160F300S BD
SAK-TC397QP-192F300S BC
SAK-TC397QP-192F300S BD
SAK-TC397QP-256F300S BC
SAK-TC397QP-256F300S BD
SAK-TC397TT-256F300S BC
SAK-TC397XA-256F300S BC
SAK-TC397XA-256F300S BD
SAK-TC397XP-256F300S BC
SAK-TC397XP-256F300S BD
SAK-TC397XX-256F300S BC
SAK-TC397XX-256F300S BD
SAK-TC397XZ-256F300S BC
SAK-TC397XZ-256F300S BD
SAK-TC399XP-256F300S BC
SAK-TC399XX-256F300S BC
SAK-TC399XX-256F300S BD
SAL-TC367DP-64F300S AA
SAL-TC375TI-96F300W AA

SAL-TC375TP-96F300W AA
SAL-TC377DP-96F300S AA
SAL-TC377TP-96F300S AA
SAL-TC377TX-96F300S AB
SAL-TC387QP-160F300S AD
SAL-TC387QP-160F300S AE
SAL-TC387TP-128F300S AD
SAL-TC387TP-128F300S AE
SAL-TC387TP-160F300S AD
SAL-TC387TP-160F300S AE
SAL-TC389QP-160F300S AD
SAL-TC389QP-160F300S AE
SAL-TC397XP-256F300S BC
SAL-TC397XP-256F300S BD
SAL-TC399XP-256F300S BC
SAL-TC399XP-256F300S BD
SAL-TC399XX-256F300S BC
SAL-TC399XX-256F300S BD
SP003833202
SP005424938
SP004818890
SP003803252
SP003803256
SP003803258
SP005351244
SP004577246
SP001694656
SP005411327
SP005411324
SP005428961
SP001724106
SP004987108
SP001694648
SP005353025
SP004950416
SP002921224
SP005351247
SP002921230
SP005351248
SP005425390
SP002921232
SP005351249
SP002921222
SP005351252
SP002739588
SP005351257
SP002739602

SP005351258
SP002739604
SP005351259
SP002739608
SP002739594
SP005351382
SP002739600
SP005351385
SP002725526
SP005351387
SP002739606
SP005351388
SP002725524
SP002725518
SP005351395
SP001724120
SP005428963
SP001724110
SP004987116
SP001724092
SP004950414
SP002921220
SP005351250
SP003021930
SP005398494
SP002921234
SP005411061
SP002921216
SP005351253
SP002725522
SP005351392
SP002725520
SP005351397
SP002725508
SP005351398
TC356TA64F300SABKXUMA1
TC356TD48F300SABKXUMA1
TC356TH64F300SABKXUMA1
TC357TA64F300SABKXUMA1
TC357TC64F300SABKXUMA1
TC357TH64F300SABKXUMA1
TC367DP48F200SAAKXUMA1
TC367DP48F300SAAKXUMA1
TC367DP64F300SAAKXUMA1
TC367V064F300SAAKXUMA1
TC367VB32F200SAAKXUMA1
TC375TI96F300WAAKXUMA1

TC375TP96F300WAAKXUMA1
TC377DP96F300SAAKXUMA1
TC377TP96F300SAAKXUMA1
TC377TX64F300SABKXUMA1
TC377TX96F300SABKXUMA1
TC387QP160F300SADKXUMA1
TC387QP160F300SAEKXUMA1
TC387TP128F300SADKXUMA1
TC387TP128F300SAEKXUMA1
TC387TP128F300SAEKXQMA1
TC387TP160F300SADKXUMA1
TC387TP160F300SAEKXUMA1
TC389QP160F300SADKXUMA1
TC389QP160F300SAEKXUMA1
TC397QA160F300SBCKXUMA1
TC397QA160F300SBDKXUMA1
TC397QP192F300SBCKXUMA1
TC397QP192F300SBDKXUMA1
TC397QP256F300SBCKXUMA1
TC397QP256F300SBDKXUMA1
TC397TT256F300SBCKXUMA1
TC397XA256F300SBCKXUMA1
TC397XA256F300SBDKXUMA1
TC397XP256F300SBCKXUMA1
TC397XP256F300SBDKXUMA1
TC397XX256F300SBCKXUMA1
TC397XX256F300SBDKXUMA1
TC397XZ256F300SBCKXUMA1
TC397XZ256F300SBDKXUMA1
TC399XP256F300SBCKXUMA1
TC399XX256F300SBCKXUMA1
TC399XX256F300SBDKXUMA1
TC367DP64F300SAALXUMA1
TC375TI96F300WAALXUMA1
TC375TP96F300WAALXUMA1
TC377DP96F300SAALXUMA1
TC377TP96F300SAALXUMA1
TC377TX96F300SABLXUMA1
TC387QP160F300SADLXUMA1
TC387QP160F300SAELXUMA1
TC387TP128F300SADLXUMA1
TC387TP128F300SAELXUMA1
TC387TP160F300SADLXUMA1
TC387TP160F300SAELXUMA1
TC389QP160F300SADLXUMA1
TC389QP160F300SAELXUMA1
TC397XP256F300SBCLXUMA1

TC397XP256F300SBDLXUMA1
TC399XP256F300SBCLXUMA1
TC399XP256F300SBDLXUMA1
TC399XX256F300SBCLXUMA1
TC399XX256F300SBDLXUMA1