

### Description

The AL58812 is comprised of 12 programmable LED current channels, each with an internal 12-bit PWM for color and brightness control through an I2C or SPI digital interface. The AL58812 is ideal for up to 4 RGB LED module lighting applications, with 3 programmable banks (A, B, C) for software control of each color. An external resistor can set the global output current of all 12 channels. Each channel current can digitally be configured up to 70mA under the thermal limitation of the package.

Features of the AL58812 are controlled via an I2C/SPI digital interface, which is selectable by the INT\_SEL pin. The AL58812 has a 30kHz, 12-bit PWM generator for each channel, as well as channel/module independent color mixing and brightness control registers to enable vivid LED effects with zero audible noise. Users can benefit from the device's ultra-low shutdown Iq Power-Saving Mode and easy software programming.

The device operates over -40°C to +85°C ambient temperature range. The AL58812 is available in W-QFN5050-40/SWP (Type A1) MSL level 1 package.

## Features

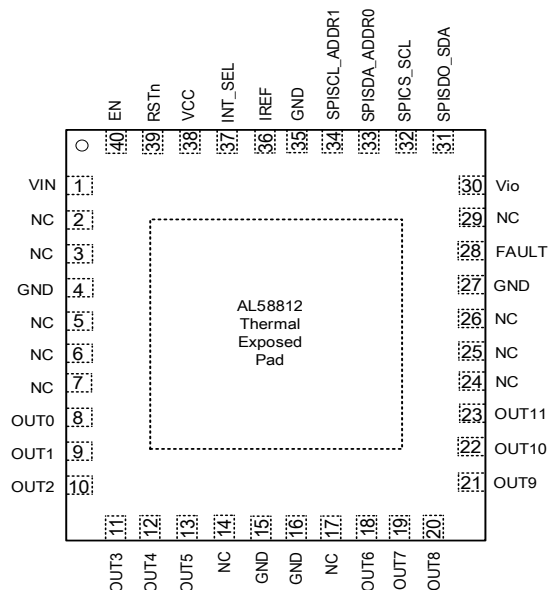
- Input Voltage 2.7V to 5.5V
- 12 Precision LED Current Sinks
  - OUT Pins Voltage max 5.5V
  - 70mA per Channel Current
  - 12-Bit PWM Register with 30kHz PWM Generator
  - PWM Phase Shifting
  - 6-Bit Global Current Dimming
  - Independent Color-Mixing Register
  - Independent Brightness Control Registers
  - Logarithmic or Linear-Scale Brightness Control
  - Three Programmable Banks (A, B, C)
  - Low-Dropout VSAT 200mV Typical at 70mA
- Hardware-Selectable I2C or SPI Digital Interface
  - Support 400kHz I2C Interface and 4MHz SPI
- Diagnosis and Protections
  - Open-Drain Fault Indication Pin and Registers
  - Individual Fault Mask Registers for Each Channel
  - Overtemperature Protection (OTP) with Pre-OTP Warning
  - LED Open/Short, Undervoltage
- Ultra-Low Quiescent Shutdown 1µA:
  - Power-Saving Mode: 15µA (max)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](#) or your local Diodes representative.**  
<https://www.diodes.com/quality/product-definitions/>

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Assignments

(Top View – Not to Scale)



W-QFN5050-40/SWP (Type A1)

## Applications

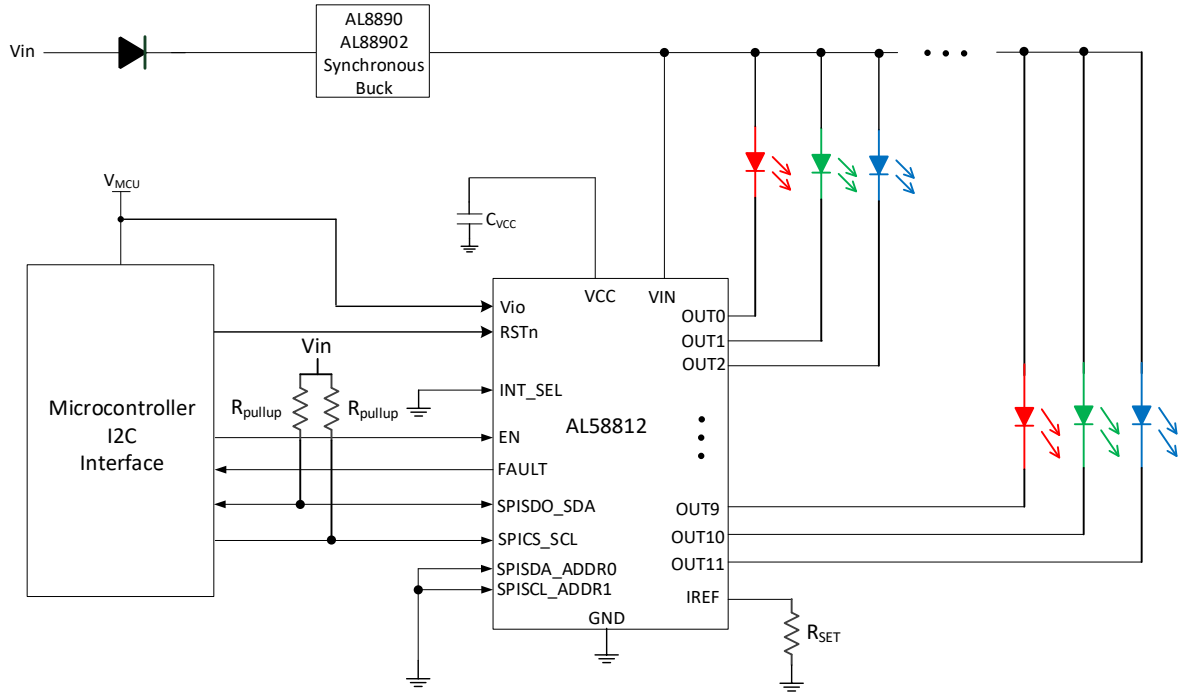
- Smart home appliances
- Electric vehicle charging stations
- Infotainment displays
- IoT information indicators
- Computing hardware

## Device Information

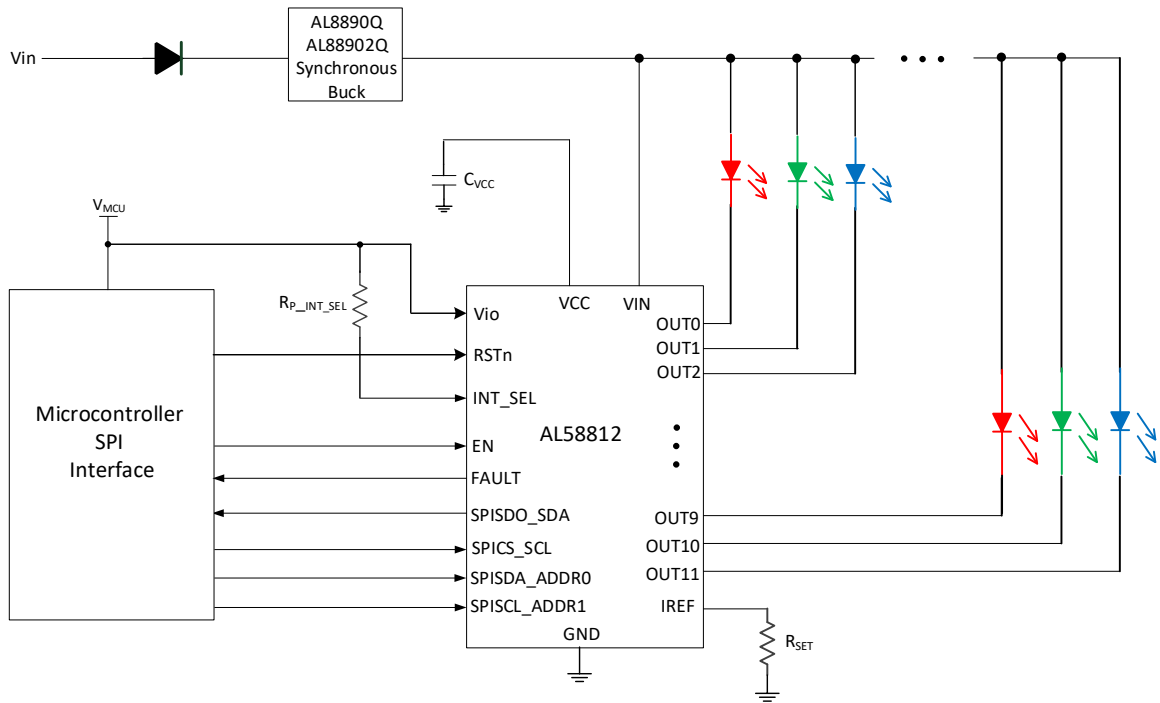
Orderable Part Number	Package	Body Size
AL58812FRZW40-13	W-QFN5050-40/SWP (Type A1)	5mm x 5mm

## Typical Applications Circuit

### 1) For I2C Interface

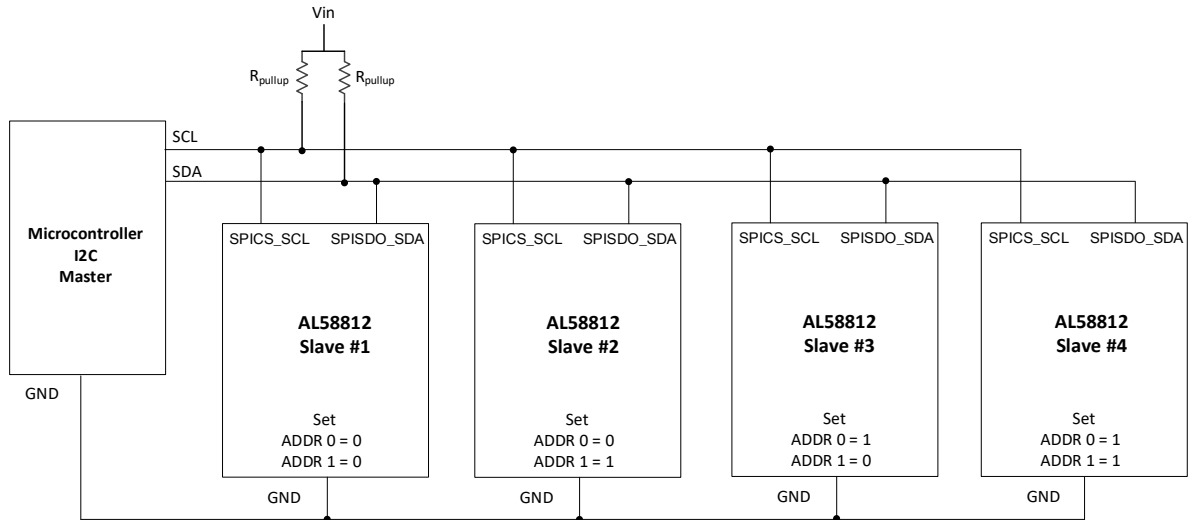


### 2) For SPI Interface

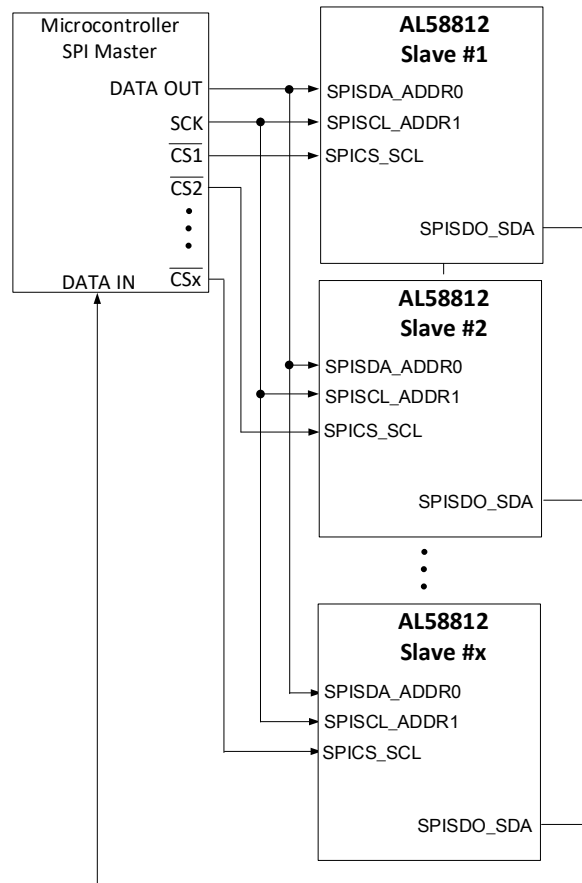


## Typical Applications Circuit (continued)

3) Four AL58812 connected together with external hardware pins setup



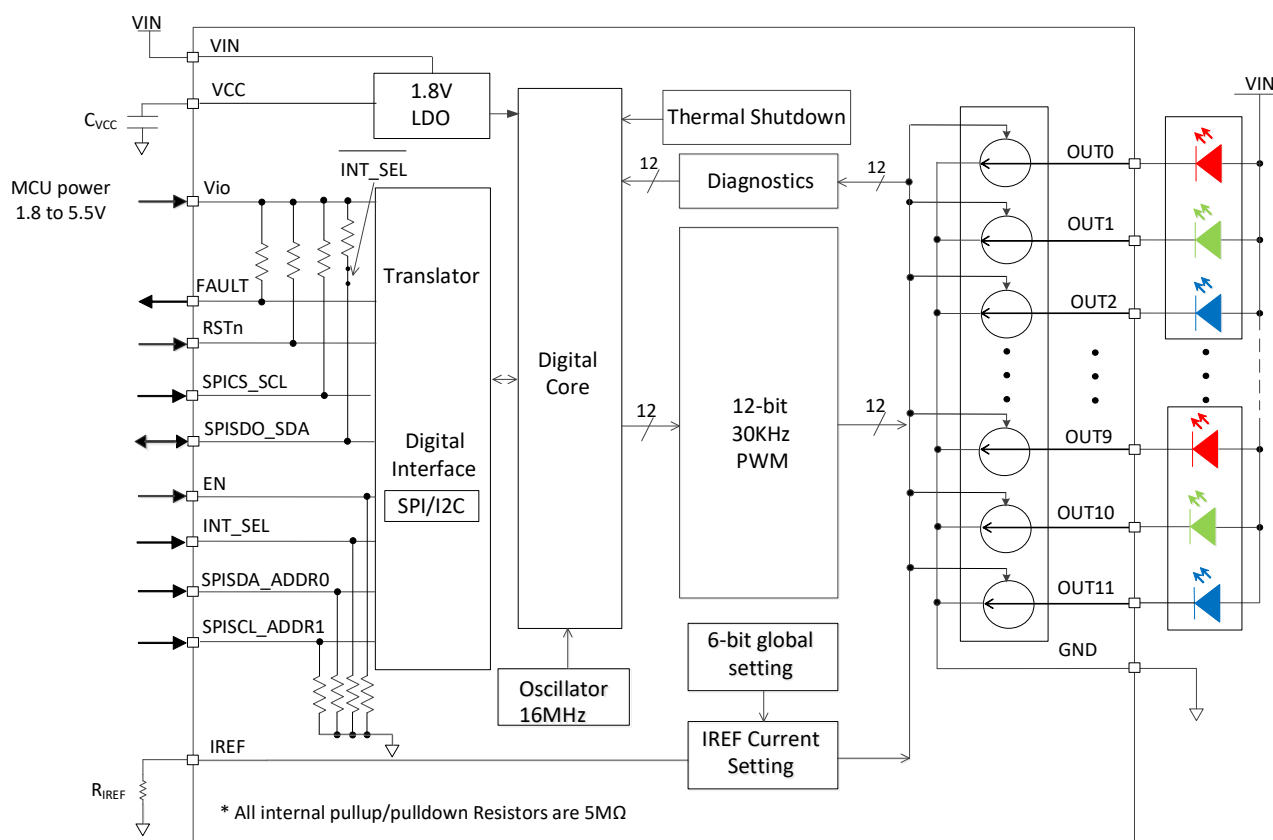
4) AL58812 (SPI interface) connected in parallel



## Pin Descriptions

Pin Name	Pin Number	Type	Function
VIN	1	Power	Power Supply
NC	2, 3, 5, 6, 7, 14, 17, 24, 25, 26, 29	—	No Connect
GND	4, 15, 16, 27, 35	GND	Ground
OUT0 to OUT5	8 to 13	O	Current Sink Output for LED 0 to LED 5
OUT6 to OUT11	18 to 23	O	Current Sink Output for LED 6 to LED 11
FAULT	28	O	Analog Output with Open-Drain Internal Pullup 5MΩ Resistor to VLDO for Fault Indication.
Vio	30	I	Input Power from MCU Power Rail
SPISDO_SDA	31	I/O	INT_SEL = HIGH, SPI Master Input Slave Output, Serial Data Line. INT_SEL = LOW, I2C Data Line. If not used, this pin must be connected to GND or VIN. (Default HIGH with an internal pullup when I2C mode selected from INT_SEL pin)
SPICS_SCL	32	I	INT_SEL = HIGH, SPI Active Low Chip Select. INT_SEL = LOW, I2C Bus Clock Line. If not used, this pin must be connected to GND or VIN. (Default HIGH with an internal pullup)
SPISDA_ADDR0	33	I	INT_SEL = HIGH, SPI Master Output Slave Input, Serial Data Line. INT_SEL = LOW, I2C Slave-Address Selection Pin. This pin must not be left floating. (Default LOW with an internal pulldown)
SPISCL_ADDR1	34	I	INT_SEL = HIGH, SPI Serial Clock Line from SPI Master (FPGA). INT_SEL = LOW, I2C Slave-Address Selection Pin. This pin must not be left floating. (Default LOW with an internal pulldown)
IREF	36	O	Connect an external resistor to regulate all channel output current.
INT_SEL	37	I	Selects the required communication interface. INT_SEL = LOW selects I2C and INT_SEL = HIGH selects SPI. This pin must not be left floating. (Default LOW with an internal pulldown)
VCC	38	O	Internal LDO 1.8V output pin, this pin must be connected to a 1μF capacitor to GND.
RSTn	39	I	Resets digital interface only but retains other register values if pulled down for time between 1ms to 20ms. Resets all register values if pulled down for time more than 20ms. Needs to be pulled high for powering up the internal digital block. (Default HIGH with an internal pullup)
EN	40	I	Active low to shut down the chip. (Default LOW with an internal pulldown)
—	Thermal Exposed Pad	GND	Thermal exposed pad also serves as a ground for the device.

### Functional Block Diagram



## Absolute Maximum Ratings (@T<sub>A</sub> = +25°C, unless otherwise specified.) (Note 4)

Symbol	Parameter	Rating	Unit
V <sub>IN</sub>	Input Voltage, Voltage Relative to GND	-0.3 to 6	V
I <sub>OUTx</sub>	OUTx Output Current	160	mA
V <sub>OUTx</sub> , EN, FAULT, RSTn, V <sub>io</sub> , INT_SEL, SPICS_SCL, SPISDO_SDA, SPISDA_ADDR0, SPISCL_ADDR1, IREF	High-Voltage Pins	-0.3 to 6V	V
VCC	Low-Voltage Output Pin	-0.3 to 2V	V
T <sub>J</sub>	Junction Temperature	-40 to +150	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
ESD	HBM	2000	V
	CDM	1000	V

Note: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

## Package Thermal Information (Note 5)

Symbol	Thermal Resistance	Value	Unit
R <sub>θJA</sub>	Junction-to-Ambient Thermal Resistance	36.0	°C/W
R <sub>θJC(top)</sub>	Junction-to-Case (Top) Thermal Resistance	18.7	°C/W
R <sub>θJB</sub>	Junction-to-Board Thermal Resistance	6.4	°C/W
Ψ <sub>JT</sub>	Junction-to-Top Characterization Parameter	0.2	°C/W
Ψ <sub>JB</sub>	Junction-to-Board Characterization Parameter	6.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-Case (Bottom) Thermal Resistance	1.1	°C/W

Note: 5. Test condition: device mounted on FR-4 PCB (51mm x 51mm 2oz copper, minimum recommended pad layout on top layer and thermal vias to bottom layer with maximum area ground plane. For better thermal performance, larger copper pad for heatsink is needed

## Recommended Operating Conditions (@T<sub>A</sub> = -40°C to +85°C, unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>IN</sub>	Device Supply Voltage	2.7	—	5.5	V
V <sub>io</sub>	Input Power from MCU Rail	1.8	3.3	5.5	V
I <sub>OUTx</sub>	OUTx Output Current (Note 6)	—	70	—	mA
T <sub>A</sub>	Ambient Temperature (Note 6)	-40	—	+85	°C

Note: 6. Dependent on ambient temperature, LED voltage, package thermal limitation, and PCB layout. Set Max\_Current\_Option = 1 for 70mA.

# Electrical Characteristics (V<sub>IN</sub> = 3.3V, -40°C < T<sub>A</sub> < +85°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>POWER SUPPLY</b>						
VCC	Internal 1.8V LDO Output	—	1.74	1.8	1.86	V
I <sub>VIN</sub>	Shutdown Supply Current	V <sub>EN</sub> = 0V	—	0.2	6	μA
	Standby Supply Current	V <sub>EN</sub> = 3.3V, Chip_EN = 0 (bit)	—	12	33	μA
	Normal-Mode Supply Current	With 39mA LED current per OUTx	—	7	9	mA
	Power-Save Mode Supply Current	V <sub>EN</sub> = 3.3V, Chip_EN = 1 (bit) Power_Save_EN = 1 (Bit) All LEDs turned off for time > 30ms	—	12	33	μA
UVLO+	V <sub>IN</sub> UVLO Rising	—	2	2.36	2.5	V
UVLO-	V <sub>IN</sub> UVLO Falling	—	1.8	2.16	2.4	V
UVLO_Hys	—	—	—	0.2	—	V
V <sub>IREF</sub>	Output Voltage of IREF Pin	—	0.68	0.7	0.72	V
<b>CURRENT SINK</b> (Note 7), Max_Current_Option set in Device Config 1 Register, G5:G0 set in LED Global Dimming Register (See page 24)						
I <sub>MAX</sub>	Maximum Global Output Current (Channel Average Current, Color Register = FF, Brightness Register = FF)	V <sub>IN</sub> in full range, R <sub>IREF</sub> = 2.1kΩ Max_Current_Option = 0, G5:G0 = 000000	—	29.25	—	mA
		V <sub>IN</sub> in full range, R <sub>IREF</sub> = 2.1kΩ Max_Current_Option = 1, G5:G0 = 100000 (Note 10)	—	7	—	mA
		V <sub>IN</sub> in full range, R <sub>IREF</sub> = 2.1kΩ Max_Current_Option = 1 G5:G0 = 000000	—	39	—	mA
		V <sub>IN</sub> in full range, R <sub>IREF</sub> = 2.1kΩ Max_Current_Option = 1 G5:G0 = 011111 (Note 10)	—	70	—	mA
I <sub>LIM</sub>	Internal Current Limit	V <sub>IN</sub> = 3.3V Max_Current_Option = 1, V <sub>IREF</sub> = 0V G5:G0 = 011111	—	75	155	mA
I <sub>D2D</sub> (Note 8)	Device to Device (I <sub>avg</sub> -I <sub>set</sub> )/I <sub>set</sub> x 100	V <sub>IN</sub> = 2.7V to 5.5V, R <sub>IREF</sub> = 2.1kΩ All channels' current set to 10mA. PWM = 100%. G5:G0 = 100011 (I <sub>MAX</sub> = 10mA)	—	±3	—	%
I <sub>C2C</sub> (Note 9)	Channel to Channel (I <sub>outx</sub> -I <sub>avg</sub> )/I <sub>avg</sub> x 100	V <sub>IN</sub> = 2.7V to 5.5V, R <sub>IREF</sub> = 2.1kΩ All channels' current set to 10mA. PWM = 100%. G5:G0 = 100011 (I <sub>MAX</sub> = 10mA)	—	±3	—	%
I <sub>lkg</sub>	LEDx Leakage Current	PWM = 0%	—	0.01	2.2	μA
VSAT	Output Saturation Voltage	V <sub>IN</sub> in full range, Max_Current_Option = 1 (bit), R <sub>IREF</sub> = 2.1kΩ, PWM = 100%, the voltage when the LED current has dropped 5%, G5:G0 = 000000	—	0.2	0.6	V
V <sub>OPEN_th_rising</sub>	LED Open Threshold	V <sub>IN</sub> = 3.3V, V <sub>OUTx</sub> < V <sub>OPEN_th_rising</sub>	0.10	0.2	0.35	V
V <sub>SC_th_rising</sub>	LED Short Threshold (V <sub>IN</sub> - V <sub>OUTx</sub> )	V <sub>IN</sub> = 3.3V, V <sub>IN</sub> - V <sub>OUTx</sub> < V <sub>SC_th_rising</sub>	0.31	0.62	0.9	V

- Notes:
- For understanding of PWM generation process, please refer to [Section 2.1.3](#).
  - I<sub>D2D</sub>: accuracy of average of all 12 channels current with respect to design target.
  - I<sub>C2C</sub>: accuracy of individual channel current with respect to the average of all 12 channels current within a device. Channel current: average, or mean current (not RMS current) on a channel. Not production tested, guaranteed by design.
  - Not production tested, guaranteed by design.

# Electrical Characteristics (V<sub>IN</sub> = 3.3V, -40°C < T<sub>A</sub> < +85°C, unless otherwise specified.) (continued)

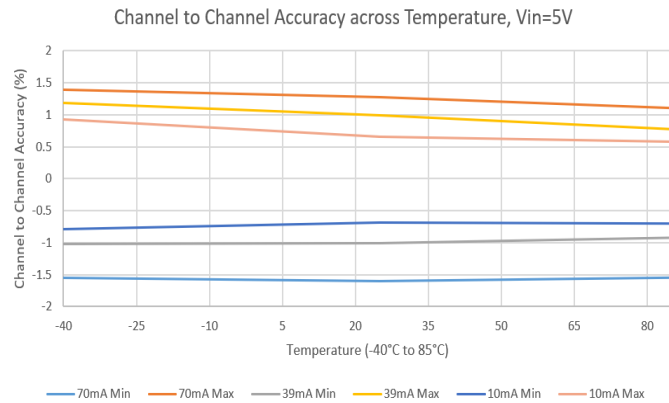
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>PWM GROUP DIMMING</b>						
f <sub>PWM</sub>	PWM Frequency	—	25	30	36	kHz
f <sub>OSC</sub>	Internal Oscillator Frequency (Note 10)	—	—	15.5	—	MHz
t <sub>IOUTx_rise</sub>	IOUTx Rise Time (Note 10)	Time for 0% to 90% rise of IOUTx	—	8	—	ns
<b>PROTECTION (Note 10)</b>						
T <sub>(PRETSD)</sub>	Pre-Thermal Warning Threshold	—	—	+145	—	°C
T <sub>(PRETSD_HYS)</sub>	Pre-Thermal Warning Hysteresis	—	—	+20	—	°C
T <sub>SD</sub>	Thermal Shutdown Temperature	—	—	+165	—	°C
T <sub>HYS</sub>	Thermal Shutdown Temperature Hysteresis	—	—	+20	—	°C

Note: 10. Not production tested, guaranteed by design.



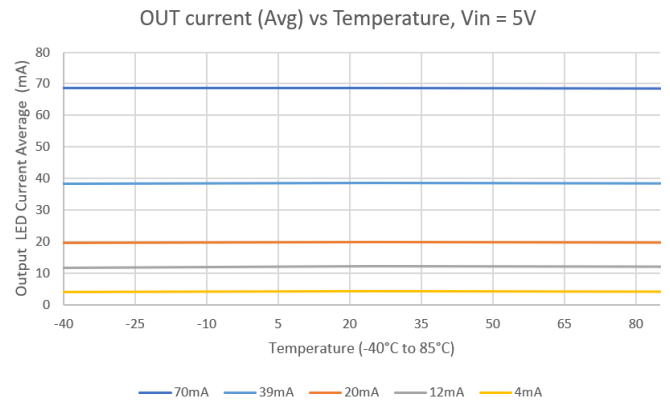
## Typical Performance Characteristics

( $V_{IN} = 5V$ ,  $-40^{\circ}C < T_A < +85^{\circ}C$ . Max\_Current\_Option = 1 for 70mA, unless otherwise specified.)



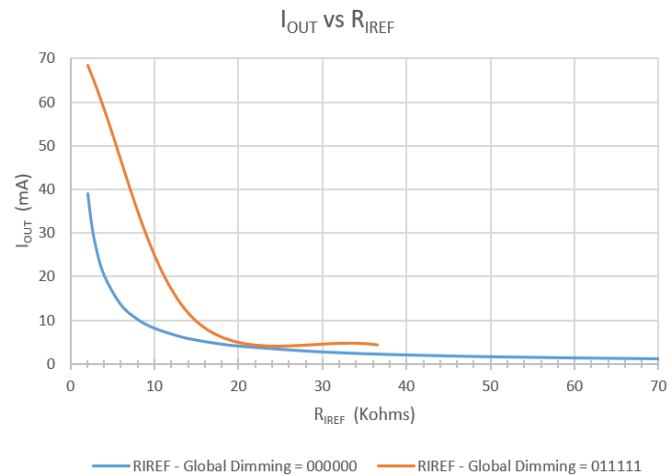
$V_{IN} = 5V$ ,  $I_{OUT} = 70mA$ ,  $39mA$ ,  $10mA$

**Figure 1. Channel to Channel Accuracy vs. Temperature**

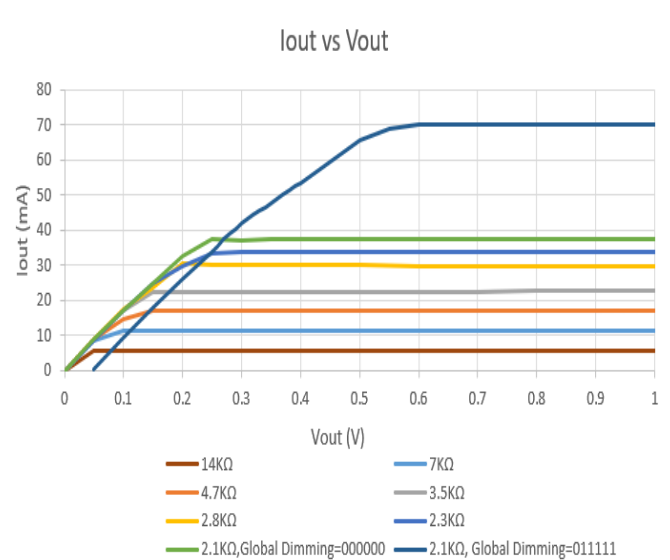


$V_{IN} = 5V$ ,  $I_{OUT} = 70mA$ ,  $39mA$ ,  $20mA$ ,  $12mA$ ,  $4mA$

**Figure 2. OUT Current vs. Temperature**



**Figure 3.  $I_{OUT}$  vs.  $R_{IREF}$**



$V_{IN} = 5V$ ,  $R_{IREF} = 2.1k\Omega$  to  $14k\Omega$

**Figure 4.  $I_{OUT}$  vs.  $V_{OUT}$**

## Functional Descriptions

### 1. General Operation

One of the I2C or SPI protocols can be selected using INT\_SEL pin. Using I2C/SPI interface, AL58812 controls LED's color and brightness through 4 primary mechanisms:

1. Use R<sub>REF</sub> to set full range for LED current I<sub>MAX</sub> (up to 70mA).
2. Set I<sub>MAX</sub> by using 6-bit global dimming register, which is termed as LED GLOBAL DIMMING in the registers map.
3. Set color/brightness registers for LED color and brightness (see *Registers Map Description*).
4. Further select various dimming and protection features described in *Registers Map Description*.

### 2. Feature Description

#### 2.1 Each Channel PWM Control

The AL58812 device is designed with independent color mixing and brightness control, which makes it easier to achieve the RGB LED color effects needed. With the inputs of the color-mixing register and the brightness-control register, the final PWM generator output for each channel is 12-bit resolution and 30kHz dimming frequency, which helps achieve a smooth dimming effect and eliminates audible noise. See Figure 5.

For example, yellow color has the red, green and blue components as 255, 255 and 0 respectively. So to get the color yellow for the first RGB LED module, the color registers at the addresses 14h, 15h and 16h need to be configured with the values 255, 255 and 0 respectively. And then the brightness register for first RGB LED module at the address 8h can be configured based on the amount of brightness needed, 255 being the maximum brightness.

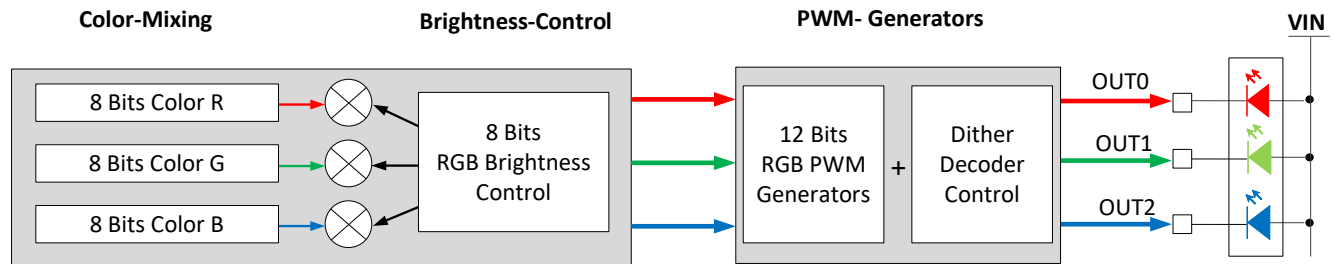


Figure 5. PWM Control Scheme for Each Channel

#### 2.1.1 Independent Color Mixing per RGB LED Module

Each output channel has its own individual 8-bit color-setting register (OUT<sub>x</sub>\_COLOR). The device allows every RGB LED module to achieve > 16 million (256 × 256 × 256) color-mixing.

#### 2.1.2 Independent Brightness Control per RGB LED Module

When color is fixed, the independent brightness-control is used to achieve accurate and flexible dimming control for every RGB LED module.

##### 2.1.2.1 Brightness-Control Register Configuration

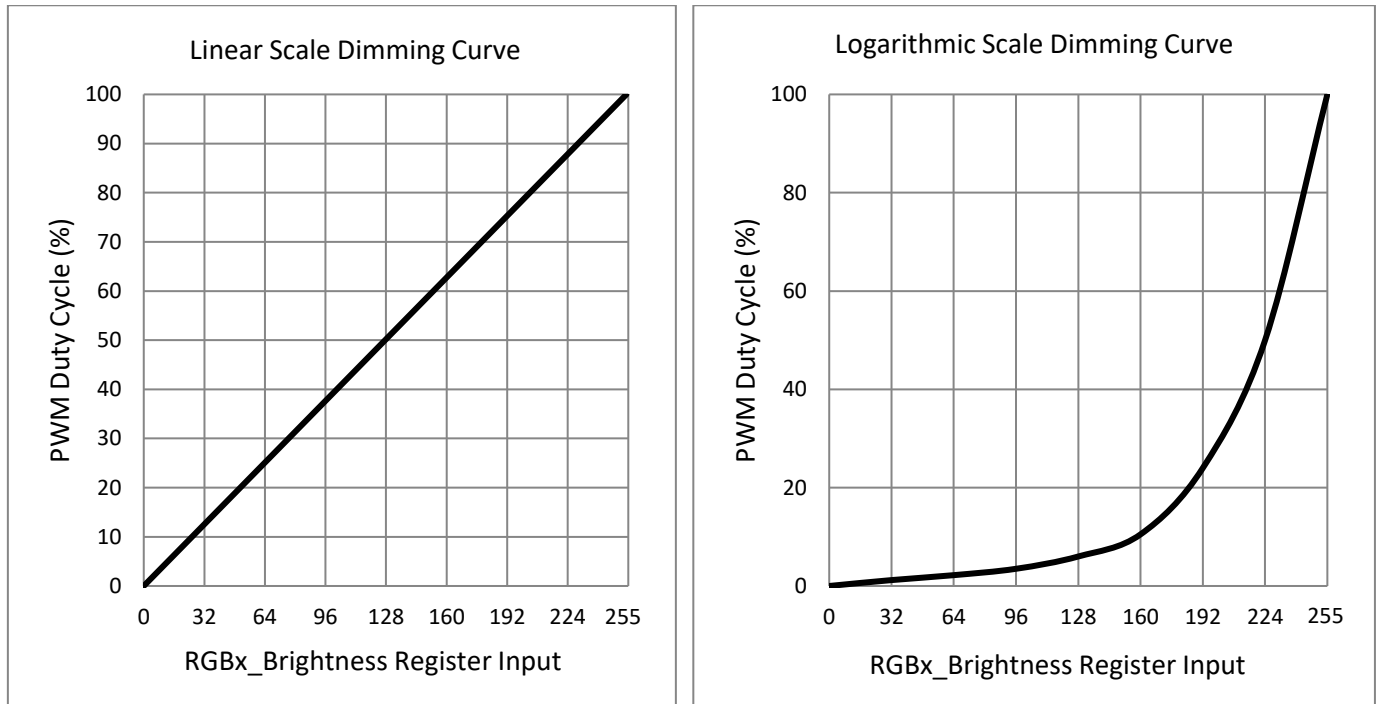
Every three consecutive output channels are assigned to their respective brightness-control register (RGB<sub>x</sub>\_BRIGHTNESS). For example, LED0, LED1, and LED2 are assigned to RGB0\_BRIGHTNESS, so it is recommended to connect the RGB LEDs in the sequence as shown in Table 1. The AL58812 device allows 256-step brightness control for each RGB LED module, which helps achieve a smooth dimming effect.

Keeping FFh (default value) in the RGB0\_BRIGHTNESS register results in 100% dimming brightness. With this setting, the users can just configure the color mixing register by channel to achieve the target dimming effect in a single-color LED application.

## Functional Descriptions (continued)

### 2.1.2.2 Logarithmic- or Linear-Scale Brightness Control

For human-eye-friendly visual performance, a logarithmic-scale dimming curve is usually implemented in LED drivers. However, for RGB LEDs, if using a single register to achieve both color mixing and brightness control, color distortion can be observed easily when using a logarithmic scale. The AL58812 device, with independent color-mixing and brightness-control registers, implements the logarithmic scale dimming control inside the brightness control function, which solves the color distortion issue effectively (See Figure 6). Also, the AL58812 device allows users to configure the dimming scale either logarithmically or linearly through the global Log\_Scale\_EN register bit. If a special dimming curve is desired, using the linear scale with software correction is the most flexible approach.



**Figure 6. Logarithmic vs Linear Dimming Curve**

### 2.1.3 12-Bit, 30kHz PWM Generator per Channel

With the inputs of the color mixing and the brightness control, the final output PWM duty cycle is defined as the product obtained by multiplying the color-mixing register value by the related brightness-control register value. The final output PWM duty cycle has 12 bits of control resolution, which is achieved by 9 bits of pure PWM resolution and 3 bits of dithering digital control. The AL58812 device allows the users to enable or disable the dithering function through the PWM\_Dithering\_EN register. When enabled (default), the output PWM duty-cycle resolution is 12 bits. When disabled, the output PWM duty-cycle resolution is 9 bits. More details about dithering are mentioned in the following paragraph.

When 3-bit dithering is enabled, dither effect is generated with  $8 (2^3 = 8)$  possible dither values: "0", "1", "2",... "7", where 0 means no dithering; "1" means every 8<sup>th</sup> PWM pulse is made 1 LSB longer to increase the final average duty cycle by 1 LSB/8 (duty cycle is termed as DT); "2" means in every group of 8 PWM pulses, the 7<sup>th</sup> and 8<sup>th</sup> PWM pulses are both made 1 LSB longer to increase DT by 2 LSB/8, etc. AL58812 uses 512 clocks in a 100% PWM DT period to achieve 9-bit pure PWM resolution ( $2^9 = 512$ ), thus 1 LSB PWM DT is 1/512. Therefore dither value "1" adds  $1/(8 \times 512) = 0.0244\%$  additional DT to pure PWM DT. For example, combining with dither value "1", the pure PWM DT of 25% will actually generate DT = 25.0244% for LED current regulation; while with dither value "2", pure PWM DT of 25% will actually generate DT = 25.05%. Though AL58812 pure PWM resolution is  $1/512 = 0.195\%$ , the 3-bit dither scheme enhances PWM resolution to 0.0244%.

## Functional Description (continued)

### 2.1.4 PWM Phase-Shifting

A PWM phase-shifting scheme allows delaying the time when each LED driver is active. When the LED drivers are not activated simultaneously, the peak load current from the pre-stage power supply is significantly decreased. The scheme also reduces input-current ripple and ceramic-capacitor audible ringing. LED drivers are grouped into three different phases.

- Phase 1 - The rising edge of the PWM pulse is fixed. The falling edge of the pulse is changed when the duty cycle changes. Phase 1 is applied to LED0, LED3, ..., LED[3 × (n - 1)].
- Phase 2 - The middle point of the PWM pulse is fixed. The pulse spreads in both directions when the PWM duty cycle is increased. Phase 2 is applied to LED1, LED4, ..., LED[3 × (n - 1) + 1].
- Phase 3 - The falling edge of the PWM pulse is fixed. The rising edge of the pulse is changed when the duty cycle changes. Phase 3 is applied to LED2, LED5, ..., LED[3 × (n - 1) + 2].

### 2.2 LED Bank Control

For most LED-animation effects, like blinking and breathing, all the RGB LEDs have the same lighting pattern. Instead of controlling the individual LED separately, which occupies the microcontroller resources heavily, the AL58812 device provides an easy coding approach, the LED bank control. Each channel can be configured as either independent control or bank control through the RGBx\_Bank\_EN register. When RGBx\_Bank\_EN = 0 (default), the LED is controlled independently by the related color-mixing and brightness-control registers. When RGBx\_Bank\_EN = 1, the AL58812 device drives the LED in LED bank-control mode. The LED bank has its own independent PWM control scheme, which is the same structure as the PWM scheme of each channel. When a channel configured as LED bank-control mode, the related color mixing and brightness control is governed by the bank control registers (BANK\_A\_COLOR, BANK\_B\_COLOR, BANK\_C\_COLOR, and BANK\_BRIGHTNESS) regardless of the inputs on its own color-mixing and brightness-control registers.

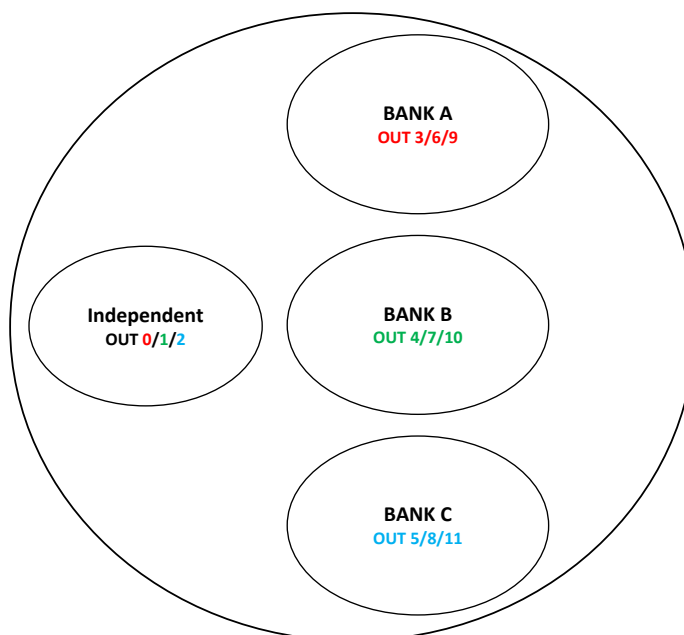
**Table 1. Bank Number and RGB Number Assignment**

Out Number	Bank Number	RGB Module Number	Register
OUT0	Bank A	RGB0	RGB0_Bank_EN
OUT1	Bank B		
OUT2	Bank C		
OUT3	Bank A	RGB1	RGB1_Bank_EN
OUT4	Bank B		
OUT5	Bank C		
OUT6	Bank A	RGB2	RGB2_Bank_EN
OUT7	Bank B		
OUT8	Bank C		
OUT9	Bank A	RGB3	RGB3_Bank_EN
OUT10	Bank B		
OUT11	Bank C		

With the bank control configuration, the AL58812 device enables users to achieve smooth and live LED effects globally with an ultra-simple software effort.

For example (as shown in Figure 7), say if we want to configure RGB0 in independent mode and rest of RGB1 to RGB5 in BANK mode, we can do that by configuring LED\_CONFIG0 register to FEh and LED\_CONFIG1 register to 0Fh. By doing this, the RGB0 module operating in independent mode will be using RGB0\_BRIGHTNESS for brightness and R0\_COLOR, G0\_COLOR and B0\_COLOR for R, G and B colors respectively, while the other RGB modules in bank mode would use BANK\_BRIGHTNESS for brightness and BANK A, BANK B and BANKC for R, G and B colors respectively.

## Functional Description (continued)



(RGB0 is independent, RGB1 to RGB3 is bank mode)

**Figure 7. Bank PWM Control Example**

### 2.3 Automatic Power-Save Mode

When all the LED outputs are inactive, the AL58812 device is able to enter power-save mode automatically, thus lowering idle-current consumption down to 25µA (maximum). Automatic power-save mode is enabled when register bit Power\_Save\_EN = 1 (default) and all the LEDs are off (both color and brightness registers = 00H) for a duration of > 30ms. Almost all analog blocks are powered down in power-save mode. If any I2C/SPI command to the device occurs, the AL58812 device returns to NORMAL mode.

### 2.4 Protection Features

#### 2.4.1 LED Open-Circuit Diagnostics

The AL58812 integrates LED open-circuit diagnostics to allow users to monitor LED status real time. The device monitors OUTx voltage to determine if there is any open-circuit failure.

If the voltage  $V_{OUTx}$  for any of the channels goes below threshold  $V_{OPEN\_th\_rising}$  and if the open persists for more than  $t_{FAULT\_WAIT}$ , the AL58812 pulls the FAULT pin low to report fault and also sets flag register Open\_Fault\_CHx and FLAG\_OPEN to 1. Once the open-circuit failure is removed, the controller needs to send CLR\_FAULT to clear the FLAG\_OPEN after fault removal. The fault delay is decided based on below table.

**Table 2. Fault Wait Time**

FW1	FW0	$t_{FAULT\_WAIT}$
0	0	8 PWM clock count
0	1	16 PWM clock count
1	0	24 PWM clock count
1	1	32 PWM clock count

#### 2.4.2 LED Short-Circuit Diagnostics

AL58812 monitors voltage difference between SUPPLY ( $V_{IN}$ ) and OUTx to determine if there is any short-circuit failure. If the difference voltage ( $V_{IN} - V_{OUTx}$ ) for any of the channel falls below threshold ( $V_{SC\_th\_rising}$ ) and if the short persists for more than  $t_{FAULT\_WAIT}$ , the AL58812 pulls the FAULT pin low to report fault and also sets flag register Short\_Fault\_CHx and FLAG\_SHORT to 1. The MCU should turn off the channel that detects a short fault to avoid overstressing device. Once the short-circuit failure is removed, the controller needs to send CLR\_FAULT to clear the FLAG\_SHORT after fault removal.

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## Functional Description (continued)

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### 2.4.3 Pre-OTP Warning & Thermal Shutdown

The AL58812 has pre-thermal warning threshold of +145°C (typical) and thermal shutdown threshold of +165°C (typical). When the AL58812 junction temperature rises above the pre-thermal warning threshold of +145°C (typical) and if it persists for more than 33μs, the device reports pre-thermal warning by pulling FAULT pin low and sets the flag register FLAG\_PREOTP to 1. The device releases pre-OTP warning once the temperature goes below +125°C. Once the fault is removed, the controller needs to send CLR\_FAULT to clear the flag register after fault removal.

The AL58812 device also implements a thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature further rises to +165°C (typical), the device shuts down all output drivers and pulls the FAULT pin low. The AL58812 device releases thermal shutdown when the junction temperature of the device is reduced to +145°C (typical).

### 2.4.4 Pre-UVLO Warning

The AL58812 provides Pre-UVLO feature that warns the MCU about supply (VIN) being low and soon UVLO might be triggered. When VIN goes below Pre-UVLO- threshold and if it persists for more than 33μs, FAULT pin is pulled low and the flag register FLAG\_PREUVLO is set to 1. The device releases Pre-UVLO warning once the VIN goes above Pre-UVLO+ threshold. Once the fault is cleared, the controller needs to send CLR\_FAULT to clear the flag register after fault removal.

### 2.4.5 UVLO

The AL58812 device has an internal comparator that monitors the voltage at VIN. When VIN is below UVLO-, reset is active and the AL58812 device is in the INITIALIZATION state. When VIN supply goes below the UVLO- threshold, FAULT pin is pulled low to indicate the fault.

### 2.4.6 Digital POR Indicator

The AL58812 device has a digital bit FLAG\_POR to indicate the power-on reset. The default value of this bit is high to indicate the power-on reset of digital block. The controller can set CLR\_POR during the start of the operation to reset FLAG\_POR so that the next power-on reset to digital block can be captured.

## 2.5 Interface Selection

Interface selection between I2C or SPI is done using an external pin INT\_SEL. When tied low, I2C is selected while when connected to high, SPI is selected.

## 2.6 Digital Communication Enhancements

Pulling the external pin RSTn high enables the internal digital block. Pulling down for time duration between 1ms to 20ms resets only the digital interface and would keep other register values unaltered. Pulling down for time duration more than 20ms would reset all the registers. There is an internal pullup resistor that would by default pull up this pin to HIGH.

## Functional Description (continued)

### 2.7 Current Setting for All Channels

The maximum global output current for all 12 channels can be adjusted by the external resistor,  $R_{REF}$ , as described below.

$$I_{MAX} = K_{REF} \times V_{REF} / R_{REF} \times [ (Max\_Current\_Option/4) + (3/4) ] \quad \dots\dots\dots(1)$$

where,

$I_{MAX}$  = Channel average current, Color Register = FF, Brightness Register = FF

$V_{REF} = 0.7V$

$R_{REF}$  = External dimming resistor (2.1kΩ recommended)

Max\_Current\_Option = 1 (default) or 0, see Register Map

$K_{REF} = 21 + (N \times 3)$ , is the current multiplication factor which can be programmed using 6-bit global dimming register G5:G0 (Address = 66H), which is analog dimming register and N is the decimal equivalent of  $\overline{G5} \overline{G4} \overline{G3} \overline{G2} \overline{G1} \overline{G0}$ .

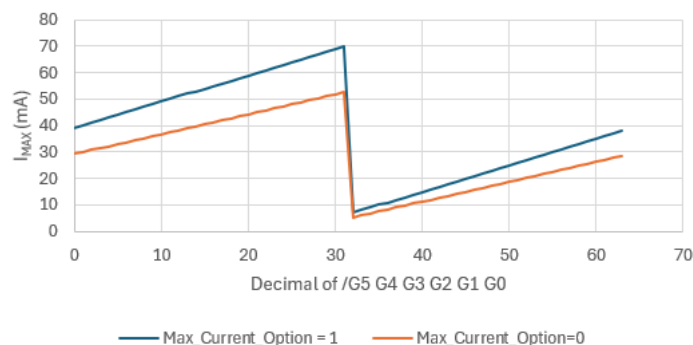
For example, if all global dimming register bits are 0, the N will be decimal equivalent of 100000 which is 32. Hence,  $K_{REF} = 21 + (32 \times 3) = 117$ .

Using equation (1) above, for  $R_{REF} = 2.1k\Omega$  and Max\_Current\_Option = 1, below is the table that shows  $I_{MAX}$  variation with respect to the global dimming register bits. From Table 3, we can see that the default value = 39mA, minimum value = 7mA and maximum value = 70mA.

**Table 3.  $I_{MAX}$  vs. Global Dimming @  $R_{REF} = 2.1k\Omega$**

G5	G4	G3	G2	G1	G0	$I_{MAX}$ (mA) Max_Current_Option = 1	$I_{MAX}$ (mA) Max_Current_Option = 0	N	$K_{REF}$
1	0	0	0	0	0	39 (Default)	29.25	32	117 (Default)
1	0	0	0	0	1	40	30	33	120
1	0	0	0	1	0	41	30.75	34	123
1	0	0	0	1	1	42	31.5	35	126
⋮						⋮	⋮	⋮	⋮
1	1	1	1	0	0	67	50.25	60	201
1	1	1	1	0	1	68	51	61	204
1	1	1	1	1	0	69	51.75	62	207
1	1	1	1	1	1	70 (max)	52.5 (max)	63	210 (max)
0	0	0	0	0	0	7 (min)	5.25 (min)	0	21 (min)
0	0	0	0	0	1	8	6	1	24
0	0	0	0	1	0	9	6.75	2	27
0	0	0	0	1	1	10	7.5	3	30
⋮						⋮	⋮	⋮	⋮
0	1	1	1	0	1	36	27	29	108
0	1	1	1	1	0	37	27.75	30	111
0	1	1	1	1	1	38	28.5	31	114

**$I_{MAX}$  (mA) vs. Global Dimming @  $R_{REF} = 2.1k\Omega$**



## Functional Description (continued)

Similarly, using equation (1) above, for global dimming register setting of 000000H and Max\_Current\_Option = 1, below is the table that shows  $I_{MAX}$  variation with respect to the  $R_{REF}$ .

**Table 4.  $I_{MAX}$  vs.  $R_{REF}$  @ G5:G0 = 000000**

$R_{REF}$ (k $\Omega$ )	$I_{MAX}$ (mA)	$K_{REF}$
2.1 (Recommended)	39	117
14.7	5.57	117
36.5	2.24	117

Table 5 shows  $I_{MAX}$  range using global dimming at different  $R_{REF}$  values.

**Table 5.  $I_{MAX}$  vs. Global Dimming Bits @ Various  $R_{REF}$**

$R_{REF}$ (k $\Omega$ )	$I_{MAX}$ (mA)		
	Min	Default	Max
2.1 (Recommended)	7	39	70
14.7	1	5.57	10
36.5	0.4	2.24	4

### 2.7.1 Thermal Considerations

As  $V_{INMAX}$  increases to 5.5V, the voltage on OUTx nodes can go as high as 3V for RED LEDs and 2V for GREEN and BLUE LEDs. In such situation if the user configures G0:G5 or Rext for higher currents, the device will get overheated and might hit the thermal shutdown voltage.

Hence the  $V_{IN}$  and  $I_{OUTx}$  for the channels should be chosen in such a way that the device junction temperature does not exceed its thermal shutdown temperature. Below is the formula relating the power dissipation and  $\theta_{JA}$  that can be used to avoid device thermal shutdown.

$$T_J = T_A + (\theta_{JA} \times P_{TOTAL})$$

Where,

- $T_J$  is the junction temperature.
- $T_A$  is the ambient temperature.
- $\theta_{JA}$  is the junction to ambient thermal resistance.
- $P_{TOTAL}$  is the device's total power dissipation.

Example: if all the 12 channels are turned on and carry the same current  $I_{MAX}$ , then the device total power dissipation is given by,

$$P_{TOTAL} = (4 \times V_{(OUT0)} \times I_{MAX}) + (4 \times V_{(OUT1)} \times I_{MAX}) + (4 \times V_{(OUT2)} \times I_{MAX})$$

### 2.8 Microcontroller (MCU) Supply

AL58812 can recognize interface logic levels from 1.8V to 5.5V. So MCU interacting with AL58812 can operate in the range 1.8V to 5.5V. However, the information of the supply used by MCU is required to be shared with AL58812 by connecting the MCU supply to Vio pin of AL58812.



## Functional Description (continued)

### 2.9 Device Functional Modes

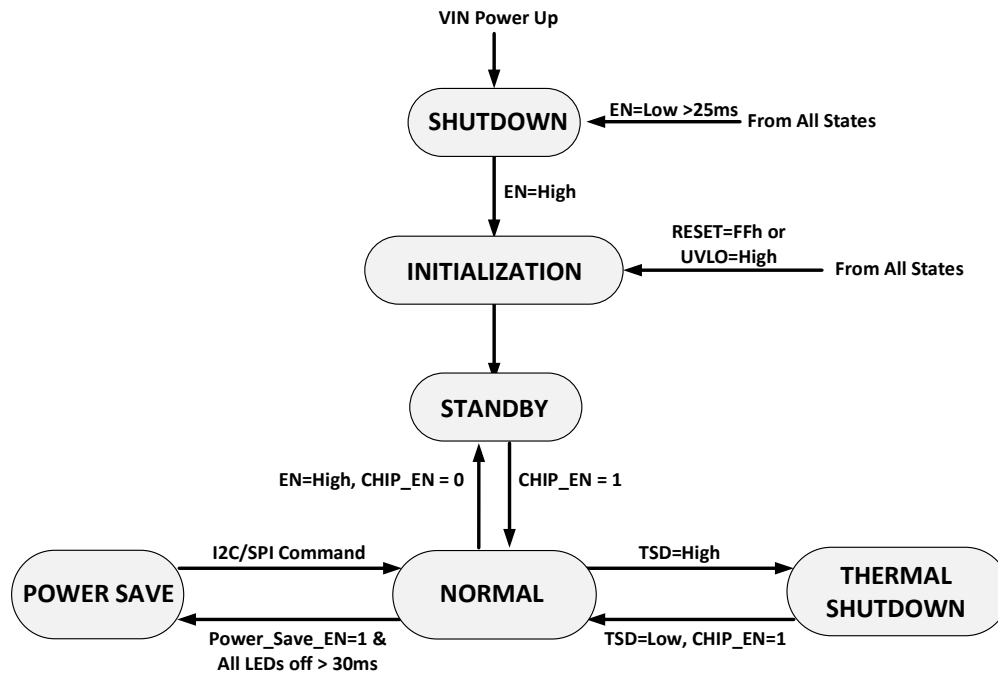


Figure 8. Functional Mode

- **INITIALIZATION:** The device enters INITIALIZATION mode when EN = High. In this mode, all the registers are reset. Entry can also be from any state, if the RESET (register) = FFh or UVLO is active.
- **NORMAL:** The device enters the NORMAL mode when Chip\_EN (register) = 1.  $I_{VIN}$  is 7mA (typical).
- **POWER SAVE:** The device automatically enters the POWER SAVE mode when Power\_Save\_EN (register) = 1 and all the LEDs are off for a duration of > 30ms. In POWER SAVE mode, analog blocks are disabled to minimize power consumption, but the registers retain the data and keep it available via I2C/SPI.  $I_{VIN}$  is 25 $\mu$ A (max). In case of any I2C/SPI command to this device, it goes back to the NORMAL mode.
- **SHUTDOWN:** The device enters SHUTDOWN mode from all states on VIN power down or when EN = Low > 25ms.  $I_{VIN}$  is < 6 $\mu$ A (max).
- **STANDBY:** The device enters the STANDBY mode when Chip\_EN (register bit) = 0. In this mode, all the OUTx are shut down, but the registers retain the data and keep it available via I2C/SPI. STANDBY is the low-power-consumption mode, when all circuit functions are disabled.  $I_{VIN}$  is 25 $\mu$ A (max).
- **THERMAL SHUTDOWN:** The device automatically enters THERMAL SHUTDOWN mode when the junction temperature exceeds +160°C (typical). In this mode, the FAULT pin state will change to LOW, Flag register (65h), and the default value 10h will change to 14h. All OUTx outputs will shut down.

Addr.	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	FDV
65h	FLAG	Reserved			FLAG_POR	FLAG_PREUVLO	FLAG_PREOTP	FLAG_SHORT	FLAG_OPEN	10h

- **RETURN TO NORMAL MODE:** Write 02h to Mask and CLR register (68h) to clear the Fault bit.

Addr.	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	FDV
68h	MASK and CLR	Reserved	POR_Mask	PreUVLO_Mask	PreOTP_Mask	Short_Mask	Open_Mask	CLR_Fault	CLR_POR	00h

Write 40h to DEVICE\_CONFIG0 register (00h) to enable the device back to normal mode, then decrease the junction temperature below +150°C (typical). FAULT pin state will change to HIGH, then the device returns to NORMAL mode.

Addr.	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	FDV
00h	DEVICE_CONFIG0	Reserved	CHIP_EN	Reserved						00h

## Functional Description (continued)

### 3. Programming (SPI)

#### 3.1 SPI-Compatible Interface

The AL58812 is compatible with SPI serial-bus specification, and it operates as a slave.

##### 3.1.1 SPI Initialization

Upon the release of power-on-reset (POR), the SPI peripheral in Digital Block waits for the chip selection signal (SPICS\_SCL) from the SPI Controller. The output SPISDA\_ADDR0 of the AL58812 is at high impedance until the reception of an active low on the select line.

The duration of the select line (SPICS\_SCL) should be compliant with the lead and lag time requirements.

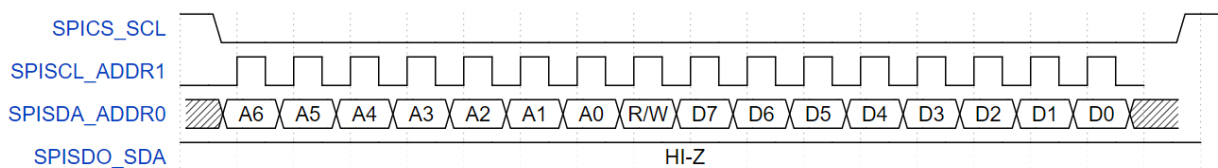
Lead time: 1) The time from SPICS\_SCL low to SPISCL\_ADDR1 high.  
2) Least lead time is half clock period.

Lag time: 1) The time from SPISCL\_ADDR1 low to SPICS\_SCL high.  
2) Least lag time is one clock period.

AL58812 is configured to communicate in Mode 0. Data read on rising edge. Clock Polarity in Idle State is Logic Low.

##### 3.1.2 Write Operation

A '1' on bit (R/W) of the SPI request frame indicates a write request from the SPI Controller. Bits A6 to A0 provide the address of the register to which the data is to be written. The contents of the frame from bit D7 to D0 is written into the respective register with last positive edge of the SPISCL\_ADDR1 in the current SPI frame.

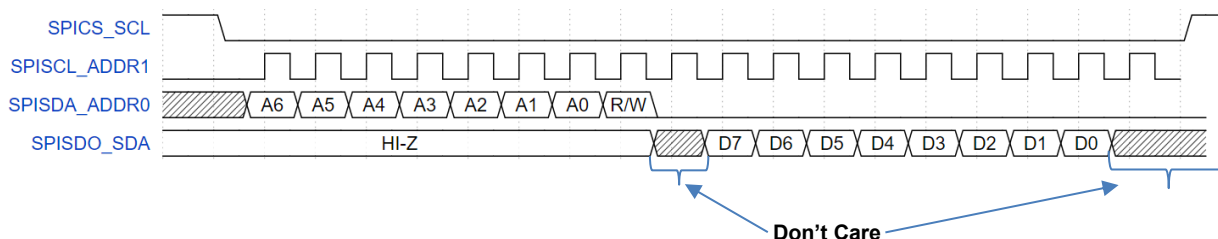


**Figure 9. SPI Write Transaction**

##### 3.1.3 Read Operation

A read request from the SPI Controller is decoded with the read/write enable bit (R/W). A '0' on bit (R/W) of the frame indicates a read request from the Controller.

Bits A6 to A0 provide the address of the register. For a valid address, the 8-bit contents of the respective register are read out. For invalid addresses (out-of range/unused addresses) the response will be a default value (zero). The peripheral responds to the read request one clock cycle later by setting up data on falling edge and Controller reads data on rising edge. The peripheral responds to the read request one clock cycle later by setting up data on falling edge and Controller reads data on rising edge.



**Figure 10. SPI Read Transaction**

## Functional Description (continued)

### 4. Programming (I2C)

#### 4.1 I2C Interface

The I2C-compatible two-wire serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bi-directional communications between the devices connected to the bus. The two interface lines are the serial data line (SDA) and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a master or a slave depending on whether it generates or receives the serial clock, SCL. The SCL and SDA lines should each have a pullup resistor placed somewhere on the line and remain HIGH even when the bus is idle.

##### 4.1.1 Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when the clock signal is LOW.

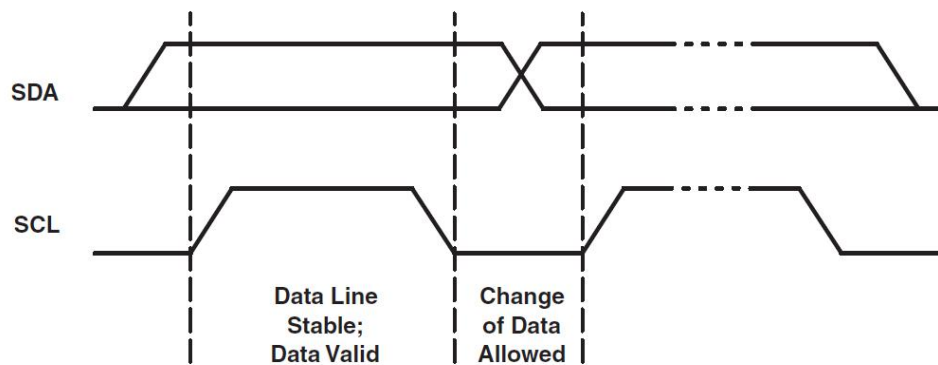


Figure 11. Data Validity

##### 4.1.2 Start and Stop Conditions

START and STOP conditions classify the beginning and the end of the data transfer session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while the SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The bus master always generates START and STOP conditions. The bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the bus master can generate repeated START conditions. First START and repeated START conditions are functionally equivalent.

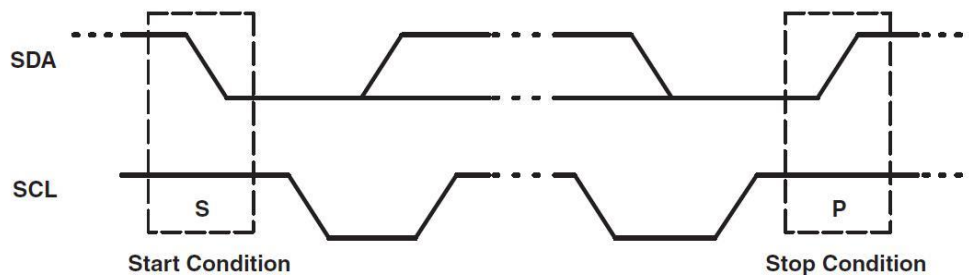


Figure 12. Start and Stop Conditions

## Functional Description (continued)

### 4.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most-significant bit (MSB) being transferred first. Each byte of data must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

There is one exception to the acknowledge-after-every-byte rule. When the master is the receiver, it must indicate to the transmitter an end of data by not acknowledging (negative acknowledge) the last byte clocked out of the slave. This negative acknowledge still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

After the START condition, the bus master sends a chip address. This address is seven bits long followed by an eighth bit, which is a data direction bit (READ or WRITE). For the eighth bit, a 0 indicates a WRITE, and a 1 indicates a READ. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register.

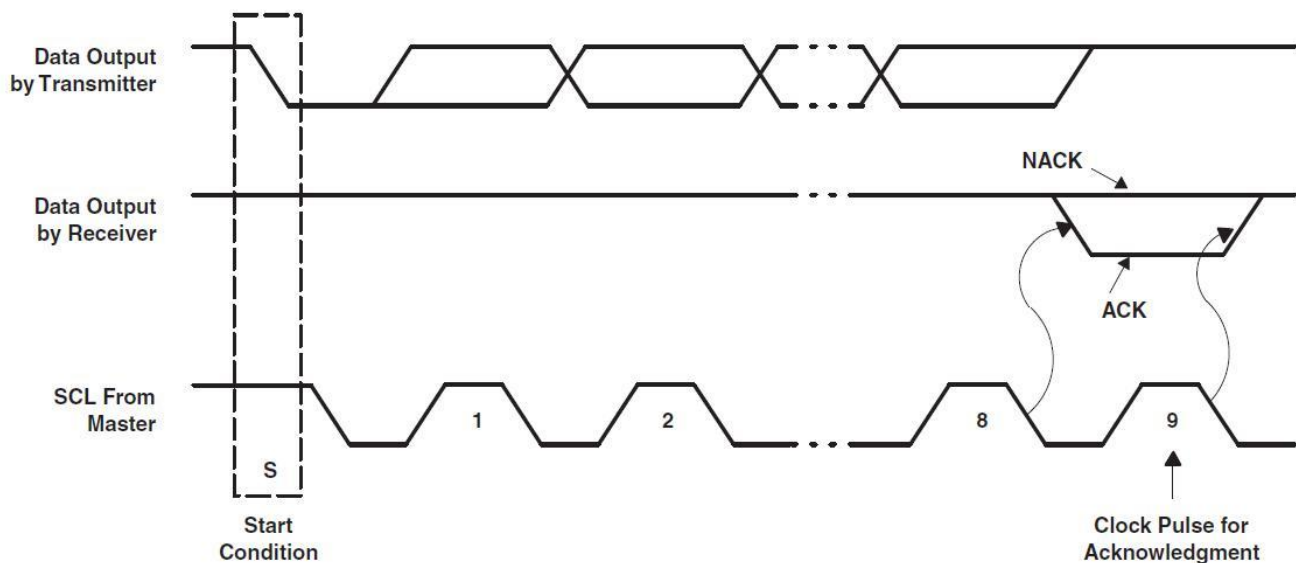


Figure 13. Acknowledge and Not Acknowledge on I2C Bus

## Functional Description (continued)

### 4.1.4 I2C Slave Addressing

The device slave address is defined by connecting GND or Vio to the SPISDA\_ADDR0 and SPISCL\_ADDR1 pins. A total of 4 independent slave addresses can be realized by combinations when GND or Vio is connected to the SPISDA\_ADDR0 and SPISCL\_ADDR1 pins (see Table 6 and Table 7).

The device responds to a broadcast slave address regardless of the setting of the SPISDA\_ADDR0 and SPISCL\_ADDR1 pins. Global writes to the broadcast address can be used for configuring all devices simultaneously. The device supports global read using a broadcast address; however, the data read is only valid if all devices on the I2C bus contain the same value in the addressed register.

**Table 6. Slave-Address Combinations**

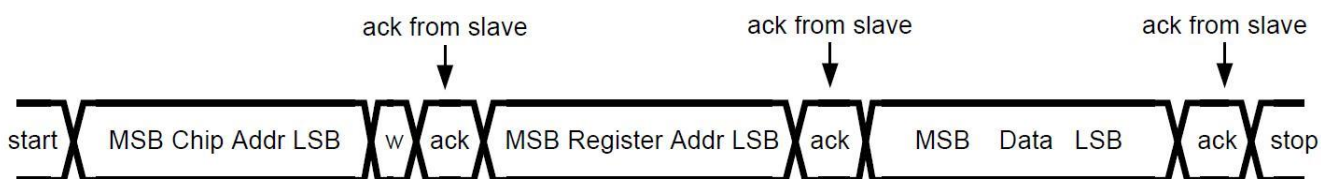
SPISCL_ADDR1	SPISDA_ADDR0	Slave Address	
		Independent	Broadcast
GND	GND	011 0000	001 1100
GND	Vio	011 0001	
Vio	GND	011 0010	
Vio	Vio	011 0011	

**Table 7. Chip Address**

	Slave Address							R/W
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	Bit 0
<b>Independent</b>	0	1	1	0	0	SPISCL_ADDR1	SPISDA_ADDR0	1 or 0
<b>Broadcast</b>	0	0	1	1	1	0	0	1 or 0

### 4.1.5 Control-Register Write Cycle

- The master device generates a start condition.
- The master device sends the slave address (7 bits) and the data direction bit (R/W = 0).
- The slave device sends an acknowledge signal if the slave address is correct.
- The master device sends the control register address (8 bits).
- The slave device sends an acknowledge signal.
- The master device sends the data byte to be written to the addressed register.
- The slave device sends an acknowledge signal.
- If the master device sends further data bytes, the control register address of the slave is incremented by 1 after the acknowledge signal. To reduce program load time, the device supports address auto incrementation. The register address is incremented after each 8 data bits.
- The write cycle ends when the master device creates a stop condition.



**Figure 14. Write Cycle**

## Functional Description (continued)

### 4.1.6 Control-Register Read Cycle

- The master device generates a start condition.
- The master device sends the slave address (7 bits) and the data direction bit (R/W = 0).
- The slave device sends an acknowledge signal if the slave address is correct.
- The master device sends the control register address (8 bits).
- The slave device sends an acknowledge signal.
- The master device generates a repeated-start condition.
- The master device sends the slave address (7 bits) and the data direction bit (R/W = 1).
- The slave device sends an acknowledge signal if the slave address is correct.
- The slave device sends the data byte from the addressed register.
- If the master device sends an acknowledge signal, the control-register address is incremented by 1. The slave device sends the data byte from the addressed register. To reduce program load time, the device supports address auto incrementation. The register address is incremented after each 8 data bits.
- The read cycle ends when the master device does not generate an acknowledge signal after a data byte and generates a stop condition.

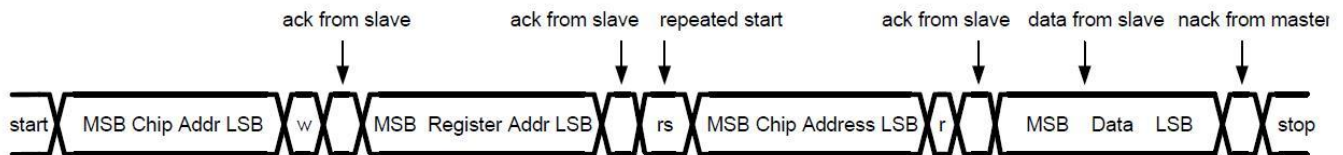


Figure 15. Read Cycle

### 4.2 FAULT Output

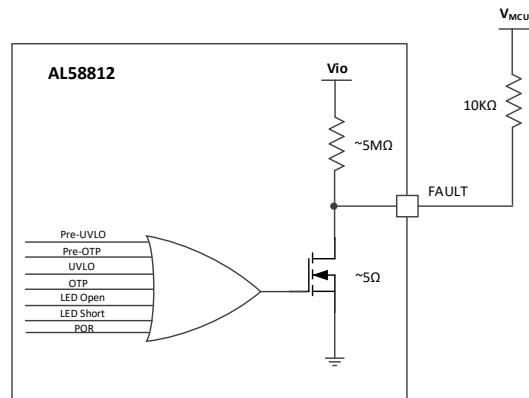


Figure 16. FAULT Internal Block Diagram

The FAULT pin is a fault indicator pin. It can be used as an interrupt output to master controller in case of any fault. The FAULT pin is an nMOS open-drain output with an internal 5MΩ pullup resistor, pulled to Vio and if additionally, this pin can also be pulled up externally to MCU supply using a smaller resistor like 10kΩ, as shown in figure above. When one or any of the faults are triggered such as UVLO, OTP, pre-UVLO, pre-OTP, LED open, LED short is detected, FAULT pin is pulled low continuously. Once the FAULT pin output is triggered, the controller needs to take necessary action and to deal with the fault and reset the fault flag. AL58812 takes action only for UVLO and OTP faults. For any other fault, AL58812 only reports the fault and the controller needs to take the action.

## Functional Description (continued)

Protection	Detection	FAULT Pin	Action
Pre-UVLO	$V_{IN} < 2.5V$	Low	When $V_{IN}$ goes below Pre-UVLO- threshold and if it persists for more than 33 $\mu$ s, FAULT pin is pulled low and sets the flag register FLAG_PREUVLO to 1. Once the $V_{IN}$ goes above Pre-UVLO+ threshold, the fault is cleared. The controller needs to send CLR_FAULT to clear the flag register after fault removal.
Pre-OTP	$T_J > +145^{\circ}C$	Low	When the junction temperature $> +145^{\circ}C$ (typical) and if it persists for more than 33 $\mu$ s, the device pulls FAULT pin low and sets the flag register FLAG_PREOTP to 1. Once the temperature $< +125^{\circ}C$ , the fault is removed. The controller needs to send CLR_FAULT to clear the flag register after fault removal.
UVLO	$V_{IN} < 1.8V$	Low	When $V_{IN}$ is below UVLO-, reset is active and the device is in the INITIALIZATION state. When $V_{IN}$ supply goes below the UVLO- threshold, FAULT pin is pulled low to indicate the fault.
OTP - Thermal Protection	$T_J > +165^{\circ}C$	Low	When the junction temperature $> +165^{\circ}C$ (typical), the device shuts down all output drivers and pulls the FAULT pin low. The AL58812 device releases thermal shutdown when the junction temperature $< +145^{\circ}C$ (typical).
LED Open	$V_{OUTx} < V_{OPEN\_th\_rising}$	Low	If the voltage $V_{OUTx}$ for any of the channels goes below threshold $V_{OPEN\_th\_rising}$ and if the open persists for more than $t_{FAULT\_WAIT}$ , the FAULT pin is pulled low and sets flag register Open_Fault_CHx and FLAG_OPEN to 1. Once the open-circuit failure is removed, the controller needs to send CLR_FAULT to clear the FLAG_OPEN after fault removal.
LED Short	$V_{IN} - V_{OUTx} < V_{SC\_th\_rising}$	Low	If the difference voltage ( $V_{IN} - V_{OUTx}$ ) for any of the channel falls below threshold ( $V_{SC\_th\_rising}$ ) and if the short persists for more than $t_{FAULT\_WAIT}$ , the FAULT pin is pulled low and sets flag register Short_Fault_CHx and FLAG_SHORT to 1. The MCU should turn off the channel that detects a short fault to avoid overstressing the device. Once the short-circuit failure is removed, the controller needs to send CLR_FAULT to clear the FLAG_SHORT after fault removal.
POR	Software Reset	Low	The default value of this bit is high to indicate the power-on reset of digital block. The controller can set CLR_POR during the start of the operation to reset FLAG_POR so that the next power-on reset to digital block can be captured.

### 4.3 Unused Channel Masking

Write a "1" to all the reserved bits in the Open Mask registers located in addresses 6Ah/6Bh/6Ch/6Dh/6Eh.

Any unused channels from the 12 channels need the fault masked so it will not be reported to FAULT pin. OUTx pins of those unused channels can be left floating or grounded.

### 4.4 Fault Masking

Open\_Mask\_CHx prevents the output open-circuit fault of individual channels from being reported to FAULT pin while Open\_Mask prevents any of the channels open fault from being reported to FAULT pin.

Short\_Mask\_CHx prevents the output short-circuit fault of individual channels from being reported to FAULT pin while Short\_Mask prevents any of the channels short fault from being reported to FAULT pin.

Pre\_OTP\_Mask prevents the Pre\_OTP fault from being reported to FAULT pin.

Pre\_UVLOMask prevents the Pre\_UVLO fault from being reported to FAULT pin.

POR\_Mask prevents the POR event from being reported to FAULT pin.

## Registers Map Description

### 5. Registers Map

Addr.	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	FDV
00h	DEVICE_CONFIG0	Reserved	CHIP_EN	Reserved						00h
01h	DEVICE_CONFIG1	Phase_Shift_EN	Reserved	Log_Scale_EN	Power_Save_EN	Reserved	Dither_EN	Max_Current_Option	LED_Global_Off	AEh
02h	LED_CONFIG0	RGB2_Bank_EN	Reserved		RGB1_Bank_EN	RGB0_Bank_EN	Reserved	Reserved	Reserved	00h
03h	LED_CONFIG1	Reserved							RGB3_Bank_EN	00h
04h	BANK_BRIGHTNESS	Bank_Brightness								FFh
05h	BANK_A_COLOR	Bank_A_Color								00h
06h	BANK_B_COLOR	Bank_B_Color								00h
07h	BANK_C_COLOR	Bank_C_Color								00h
08h to 0Ah	Reserved	Reserved								00h
0Bh	RGB0_BRIGHTNESS	RGB0_Brightness								FFh
0Ch	RGB1_BRIGHTNESS	RGB1_Brightness								FFh
0Dh to 0Eh	Reserved	Reserved								00h
0Fh	RGB2_BRIGHTNESS	RGB2_Brightness								FFh
10h	RGB3_BRIGHTNESS	RGB3_Brightness								FFh
11h to 1Ch	Reserved	Reserved								00h
1Dh	R0_COLOR	R0_Color								00h
1Eh	G0_COLOR	G0_Color								00h
1Fh	B0_COLOR	B0_Color								00h
20h	R1_COLOR	R1_Color								00h
21h	G1_COLOR	G1_Color								00h
22h	B1_COLOR	B1_Color								00h
23h to 28h	Reserved	Reserved								00h
29h	R2_COLOR	R2_Color								00h
2Ah	G2_COLOR	G2_Color								00h
2Bh	B2_COLOR	B2_Color								00h
2Ch	R3_COLOR	R3_Color								00h
2Dh	G3_COLOR	G3_Color								00h
2Eh	B3_COLOR	B3_Color								00h
2Fh to 37h	Reserved	Reserved								00h
38h	RESET	RESET								00h
65h	FLAG	Reserved			FLAG_POR	FLAG_PREUVLO	FLAG_PREOTP	FLAG_SHORT	FLAG_OPEN	10h
66h	LED_GLOBAL_DIMMING	Reserved		G5	G4	G3	G2	G1	G0	00h
67h	FAULT WAIT	Reserved						FW1	FW0	00h
68h	MASK and CLR	Reserved	POR_Mask	PreUVLO_Mask	PreOTP_Mask	Short_Mask	Open_Mask	CLR_Fault	CLR_POR	00h

\* FDV = Factory Default Value



## Register Maps Description (continued)

### 5. Registers Map (continued)

Addr.	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	FDV
6Ah	Reserved	Reserved								00h
6Bh	OM0	Reserved	OM_OUT5	OM_OUT4	OM_OUT3	OM_OUT2	OM_OUT1	OM_OUT0	Reserved	00h
6Ch	OM1	OM_OUT8	OM_OUT7	OM_OUT6	Reserved					00h
6Dh	OM2	Reserved					OM_OUT11	OM_OUT10	OM_OUT9	00h
6Eh to 6Fh	Reserved	Reserved								00h
70h	SM0	Reserved	SM_OUT5	SM_OUT4	SM_OUT3	SM_OUT2	SM_OUT1	SM_OUT0	Reserved	00h
71h	SM1	SM_OUT8	SM_OUT7	SM_OUT6	Reserved					00h
74h	SM2	Reserved					SM_OUT11	SM_OUT10	SM_OUT9	00h
75h to 76h	Reserved	Reserved								00h
77h	OF0	Reserved	OF_OUT5	OF_OUT4	OF_OUT3	OF_OUT2	OF_OUT1	OF_OUT0	Reserved	00h
78h	OF1	OF_OUT8	OF_OUT7	OF_OUT6	Reserved					00h
79h	OF2	Reserved					OF_OUT11	OF_OUT10	OF_OUT9	00h
7Ah to 7Bh	Reserved	Reserved								00h
7Ch	SF0	Reserved	SF_OUT5	SF_OUT4	SF_OUT3	SF_OUT2	SF_OUT1	SF_OUT0	Reserved	00h
7Dh	SF1	SF_OUT8	SF_OUT7	SF_OUT6	Reserved					00h
7Eh	SF2	Reserved					SF_OUT11	SF_OUT10	SF_OUT9	00h
7Fh	Reserved	Reserved								00h

\* OMx = Open\_Maskx

\* SMx = Short\_Maskx

\* OFx = Open Faultx

\* SFx = Short Faultx

\* FDV = Factory Default Value

**Register Maps Description** (continued)

**Table 8. Access Type Codes**

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
<b>Write Type</b>		
$\bar{W}$	$\bar{W}$	Write
<b>Power-On Reset or Default Value</b>		
(xxh)	(xxh)	Value after POR or default value

**5.1 DEVICE\_CONFIG0 (Address = 00h) [default = 00h]**
**Table 9. DEVICE\_CONFIG0 Register**

7	6	5	4	3	2	1	0
Reserved	Chip_EN	Reserved					
Reserved	R/ $\bar{W}$ -(00h)	Reserved					
Reserved	0 = Disabled 1 = Enabled	Reserved					

**5.2 DEVICE\_CONFIG1 (Address = 01h) [default = AEh]**
**Table 10. DEVICE\_CONFIG1 Register**

7	6	5	4	3	2	1	0
Phase_Shift_EN	Reserved	Log_Scale_EN	Power_Save_EN	Reserved	Dither_EN	Max_Current Option	LED_Global_Off
R/ $\bar{W}$ -(01h)	R/ $\bar{W}$ -(00h)	R/ $\bar{W}$ -(01h)	R/ $\bar{W}$ -(00h)	R/ $\bar{W}$ -(01h)	R/ $\bar{W}$ -(01h)	R/ $\bar{W}$ -(01h)	R/ $\bar{W}$ -(00h)
0 = Disabled 1 = Enabled	—	0 = Linear curve Enabled 1 = Logarithmic curve Enabled	0 = Power Save Mode Disabled 1 = Power Save Mode Enabled	—	0 = Disabled 1 = Enabled	0 = 29.25mA 1 = 39mA	0 = Normal Operation 1 = Shutdown all LEDs

**5.3 LED\_CONFIG0 (Address = 02h) [default = 00h]**
**Table 11. LED\_CONFIG0 Register**

7	6	5	4	3	2	1	0
RGB2_Bank_EN	Reserved		RGB1_Bank_EN	RGB0_Bank_EN	Reserved	Reserved	Reserved
R/W-(00h)							
0 = Disabled 1 = Enabled	—		0 = Disabled 1 = Enabled	0 = Disabled 1 = Enabled	—	—	—

\* 0 = Independent Mode Enabled

\* 1 = Bank Mode Enabled

**5.4 LED\_CONFIG1 (Address = 03h) [default = 00h]**
**Table 12. LED\_CONFIG1 Register**

7	6	5	4	3	2	1	0
Reserved							RGB3_Bank_EN
R/ $\bar{W}$ -(00h)							
—							0 = Disabled 1 = Enabled

## Register Maps Description (continued)

### 5.5 BANK\_BRIGHTNESS (Address = 04h) [default = FFh]

Table 13. BANK\_BRIGHTNESS Register

7	6	5	4	3	2	1	0
BANK_BRIGHTNESS							
R/W-(FFh)							
00h = 0% of full brightness							
...							
80h = 50% of full brightness							
...							
FFh = 100 % of full brightness							

### 5.6 BANK\_A\_COLOR (Address = 05h) [default = 00h]

Table 14. BANK\_A\_COLOR Register

7	6	5	4	3	2	1	0
BANK_A_COLOR							
R/W-(00h)							
00h = The color mixing percentage is 0%							
...							
80h = The color mixing percentage is 50%							
...							
FFh = The color mixing percentage is 100%							

### 5.7 BANK\_B\_COLOR (Address = 06h) [default = 00h]

Table 15. BANK\_B\_COLOR Register

7	6	5	4	3	2	1	0
BANK_B_COLOR							
R/W-(00h)							
00h = The color mixing percentage is 0%							
...							
80h = The color mixing percentage is 50%							
...							
FFh = The color mixing percentage is 100%							

### 5.8 BANK\_C\_COLOR (Address = 07h) [default = 00h]

Table 16. BANK\_C\_COLOR Register

7	6	5	4	3	2	1	0
BANK_C_COLOR							
R/W-(00h)							
00h = The color mixing percentage is 0%							
...							
80h = The color mixing percentage is 50%							
...							
FFh = The color mixing percentage is 100%							

### 5.9 RGB0 to RGB3\_BRIGHTNESS (Address = 0Bh, 0Ch, 0Fh, and 10h) [default = FFh]

Table 17. RGB0 to RGB3\_BRIGHTNESS Register

7	6	5	4	3	2	1	0
RGB0 to RGB3_BRIGHTNESS							
R/W-(FFh)							
00h = 0% of full brightness							
...							
80h = 50% of full brightness							
...							
FFh = 100 % of full brightness							

## Register Maps Description (continued)

### 5.10 Rx\_COLORx = 0 to 3 (Address = 1Dh, 20h, 29h, and 2Ch) [default = 00h]

**Table 18. Rx\_COLOR Register**

7	6	5	4	3	2	1	0
Rx_COLOR							
R/W-(00h)							
00h = The color mixing percentage is 0%							
...							
80h = The color mixing percentage is 50%							
...							
FFh = The color mixing percentage is 100%							

### 5.11 Gx\_COLORx = 0 to 3 (Address = 1Eh, 21h, 2Ah, and 2Dh) [default = 00h]

**Table 19. Gx\_COLOR Register**

7	6	5	4	3	2	1	0
Gx_COLOR							
R/W-(00h)							
00h = The color mixing percentage is 0%							
...							
80h = The color mixing percentage is 50%							
...							
FFh = The color mixing percentage is 100%							

### 5.12 Bx\_COLORx = 0 to 3 (Address = 1Fh, 22h, 2Bh, and 2Eh) [default = 00h]

**Table 20. Bx\_COLOR Register**

7	6	5	4	3	2	1	0
Bx_COLOR							
R/W-(00h)							
00h = The color mixing percentage is 0%							
...							
80h = The color mixing percentage is 50%							
...							
FFh = The color mixing percentage is 100%							

### 5.13 RESET (Address = 38h) [default = 00h]

**Table 21. RESET Register**

7	6	5	4	3	2	1	0
RESET							
W-(00h)							
FFh = Resets all the registers to default value.							

### 5.14 FLAG (Address = 65h) [default = 00h]

**Table 22. FLAG Register**

7	6	5	4	3	2	1	0
Reserved			FLAG_POR	FLAG_PREUVLO	FLAG_PREOTP	FLAG_SHORT	FLAG_OPEN
R/W-(00h)							
Reserved			0 = No POR fault reported. 1 = POR fault reported.	0 = No Pre_UVLO fault reported. 1 = Pre_UVLO fault reported.	0 = No Pre_OTP fault reported. 1 = Pre_OTP fault reported.	0 = No short fault reported on any channel. 1 = Short fault reported on any of the channels.	0 = No open fault reported on any channel. 1 = Open fault reported on any of the channels.

## Register Maps Description (continued)

### 5.15 LED\_GLOBAL\_DIMMING (Address = 66h) [default = 00h]

**Table 23. LED\_GLOBAL\_DIMMING Register**

7	6	5	4	3	2	1	0
Reserved		G5	G4	G3	G2	G1	G0
R/W-(00h)							
Reserved	6-bit LED Global current setting. See <a href="#">Table 3</a> for details.						

### 5.16 FAULT\_WAIT (Address = 67h) [default = 00h]

**Table 24. FAULT\_WAIT Register**

7	6	5	4	3	2	1	0
Reserved						FW1	FW0
R/W-(00h)							
Reserved						0 = as per <a href="#">Table 2</a> 1 = as per <a href="#">Table 2</a>	0 = as per <a href="#">Table 2</a> 1 = as per <a href="#">Table 2</a>

### 5.17 MASK and CLR (Address = 68h) [default = 00h]

**Table 25. MASK and CLR Register**

7	6	5	4	3	2	1	0
Reserved	POR_Mask	PreUVLOMask	PreOTP_Mask	Short_Mask	Open_Mask	CLR_Fault	CLR_POR
R/W-(00h)							
Reserved	0 = POR mask turned off 1 = POR mask turned on	0 = Pre-UVLO mask turned off 1 = Pre-UVLO mask turned on	0 = Pre-OTP mask turned off 1 = Pre-OTP mask turned on	0 = Short Detection Mask off 1 = Short Detection Mask on	0 = Open Detection Mask off 1 = Open Detection Mask on	0 = Clearing faults turned off 1 = Clears the faults	0 = Clearing POR turned off 1 = Clears the POR faults

### 5.18 OM0 (Address = 6Bh) [default = 00h]

**Table 26. OM0 Register**

7	6	5	4	3	2	1	0
Reserved	OM_OUT5	OM_OUT4	OM_OUT3	OM_OUT2	OM_OUT1	OM_OUT0	Reserved
R/W-(00h)							
—	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	—

OM = Open\_Maskx

### 5.19 OM1 (Address = 6Ch) [default = 00h]

**Table 27. OM1 Register**

7	6	5	4	3	2	1	0
OM_OUT8	OM_OUT7	OM_OUT6	Reserved				
R/W-(00h)							
0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	—				

OM = Open\_Maskx

## Register Maps Description (continued)

### 5.20 OM2 (Address = 6Dh) [default = 00h]

**Table 28. OM2 Register**

7	6	5	4	3	2	1	0
Reserved					OM_OUT11	OM_OUT10	OM_OUT9
R/W-(00h)							
—					0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

OM = Open\_Maskx

### 5.21 SM0 (Address = 70h) [default = 00h]

**Table 29. SM0 Register**

7	6	5	4	3	2	1	0
Reserved	SM_OUT5	SM_OUT4	SM_OUT3	SM_OUT2	SM_OUT1	SM_OUT0	Reserved
R/W-(00h)							
—	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	—

SM = Short\_Maskx

### 5.22 SM1 (Address = 71h) [default = 00h]

**Table 30. SM1 Register**

7	6	5	4	3	2	1	0
SM_OUT8	SM_OUT7	SM_OUT6	Reserved				
R/W-(00h)							
0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	—				

SM = Short\_Maskx

### 5.23 SM2 (Address = 74h) [default = 00h]

**Table 31. SM2 Register**

7	6	5	4	3	2	1	0
Reserved					SM_OUT11	SM_OUT10	SM_OUT9
R/W-(00h)							
—					0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

SM = Short\_Maskx

### 5.24 OF0 (Address = 77h) [default = 00h]

**Table 32. OF0 Register**

7	6	5	4	3	2	1	0
Reserved	OF_OUT5	OF_OUT4	OF_OUT3	OF_OUT2	OF_OUT1	OF_OUT0	Reserved
R/W-(00h)							
—	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	—

OFx = Open\_Faultx

## Register Maps Description (continued)

### 5.25 OF1 (Address = 78h) [default = 00h]

**Table 33. OF1 Register**

7	6	5	4	3	2	1	0
OF_OUT8	OF_OUT7	OF_OUT6	Reserved				
R/W-(00h)							
0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	—				

OFx = Open\_Faultx

### 5.26 OF2 (Address = 79h) [default = 00h]

**Table 34. OF2 Register**

7	6	5	4	3	2	1	0
Reserved					OF_OUT11	OF_OUT10	OF_OUT9
R/W-(00h)							
—					0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

OFx = Open\_Faultx

### 5.27 SF0 (Address = 7Ch) [default = 00h]

**Table 35. SF0 Register**

7	6	5	4	3	2	1	0
Reserved	SF_OUT5	SF_OUT4	SF_OUT3	SF_OUT2	SF_OUT1	SF_OUT0	Reserved
R/W-(00h)							
—	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	—

SFx = Short\_Faultx

### 5.28 SF1 (Address = 7Dh) [default = 00h]

**Table 36. SF1 Register**

7	6	5	4	3	2	1	0
SF_OUT8	SF_OUT7	SF_OUT6	Reserved				
R/W-(00h)							
0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	—				

SFx = Short\_Faultx

### 5.29 SF2 (Address = 7Eh) [default = 00h]

**Table 37. SF2 Register**

7	6	5	4	3	2	1	0
Reserved					SF_OUT11	SF_OUT10	SF_OUT9
R/W-(00h)							
—					0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

SFx = Short\_Faultx

## Application Information

### Timing Requirements for I2C Interface (Note 11)

Symbol	Parameter	Min	Typ	Max	Unit
f <sub>SCL</sub>	I2C Clock Frequency	—	—	400	kHz
t <sub>EN_H</sub>	EN First Rising Edge Until First I2C Access	—	—	500	μs
t <sub>EN_L</sub>	EN First Falling Edge Until First I2C Reset	—	—	3	μs
1	Hold Time (Repeated) START Condition	0.6	—	—	μs
2	Clock Low Time	1.3	—	—	μs
3	Clock High Time	600	—	—	ns
4	Setup Time for A Repeated START Condition	600	—	—	ns
5	Data Hold Time	0	—	—	ns
6	Data Setup Time	100	—	—	ns
7	Rise Time of SDA and SCL	20 + 0.1 C <sub>b</sub>	—	300	ns
8	Fall Time of SDA and SCL	15 + 0.1 C <sub>b</sub>	—	300	ns
9	Setup Time for STOP Condition	600	—	—	ns
10	Bus Free Time Between a STOP and a START Condition	1.3	—	—	ns
C <sub>b</sub>	Capacitive Load Parameter for Each Bus Line. Load of 1pF corresponds to one nanosecond.	—	—	200	pF

Note: 11. Specified by design & ATE characterized.

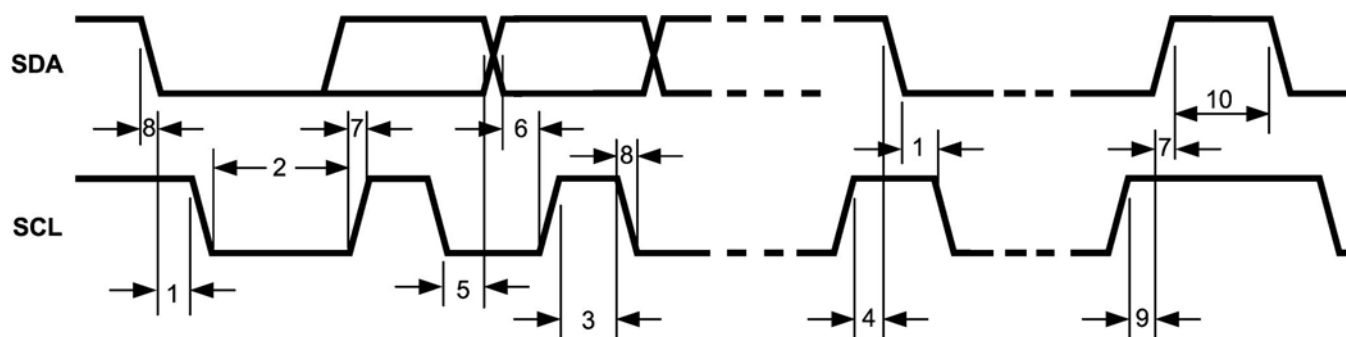


Figure 17. I2C Timing Parameters

Table 38. Input and Output Logic Levels

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL INPUT LOGIC LEVELS (EN, RSTn, INT_SEL)						
V <sub>IL</sub>	Input Logic Low	V <sub>IO</sub> = 1.8V	—	—	0.35	V
V <sub>IH</sub>	Input Logic High		1.4	—	—	V
DIGITAL INTERFACE LOGIC LEVELS (SPICS_SCL, SPISDO_SDA, SPISDA_ADDR0, SPISCL_ADDR1)						
V <sub>IL</sub>	Input Logic Low	V <sub>IO</sub> = 1.8V	—	—	0.4	V
V <sub>IH</sub>	Input Logic High		1.4	—	—	V
V <sub>SDA</sub>	SDA Output Low Level	IPULLUP = 5mA	—	—	0.4	V



## Application Information (continued)

### Timing Requirements for SPI Interface (Note 11)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{SCLK}$	SPI Clock Frequency	—	—	—	4	MHz
$t_{CSS}$	The Time from SPICS_SCL Low to SPISCL_ADDR1 High	—	250	—	—	ns
$t_{CSH}$	The Time from SPISCL_ADDR1 Low to SPICS_SCL High	—	250	—	—	ns
$t_{DS}$	Data Setup Time	—	10	—	—	ns
$t_{DH}$	Data Hold Time	—	0	—	—	ns
$t_{CS\_HI}$	Minimum Chip Select Deasserted HIGH Time	—	250	—	—	ns
$t_{D(SDO)}$	SDO Delay Time	$C_L = 50pF$	—	—	20	ns
$t_{LOW}$	LOW Period of SCLK Clock	—	125	—	—	ns
$t_{HIGH}$	HIGH Period of SCLK Clock	—	125	—	—	ns

Note: 11. Specified by design & ATE characterized.

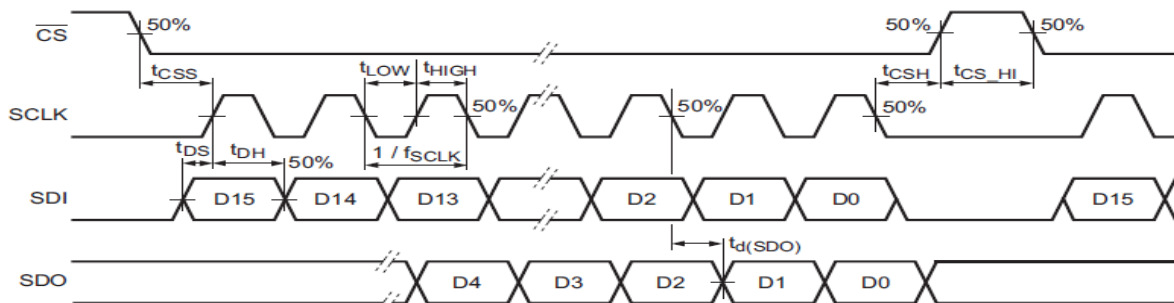
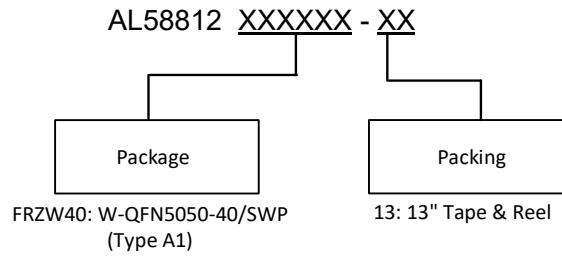


Figure 18. SPI Timing Parameters

## Design Tools – from Diodes Incorporated's Website <https://www.diodes.com/design/tools/>

- RGB 3 in 1 Deno Board - AL58812EV1
- Arduino Sample Code
- Demo Board Gerber File for PCB Layout Reference

## Ordering Information

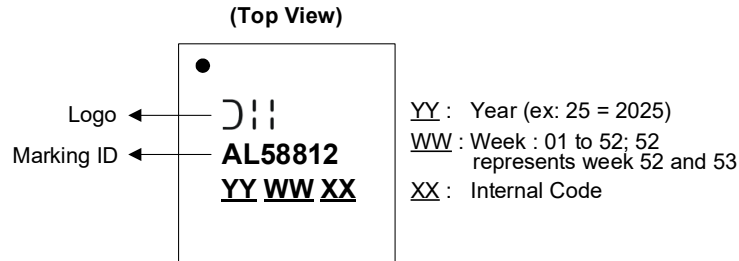


Orderable Part Number	Part Number Suffix	Package Code	Package (Note 12)	Packing	
				Qty.	Carrier
AL58812FRZW40-13	-13	FRZW40	W-QFN5050-40/SWP (Type A1)	5000	Tape & Reel

Note: 12. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information

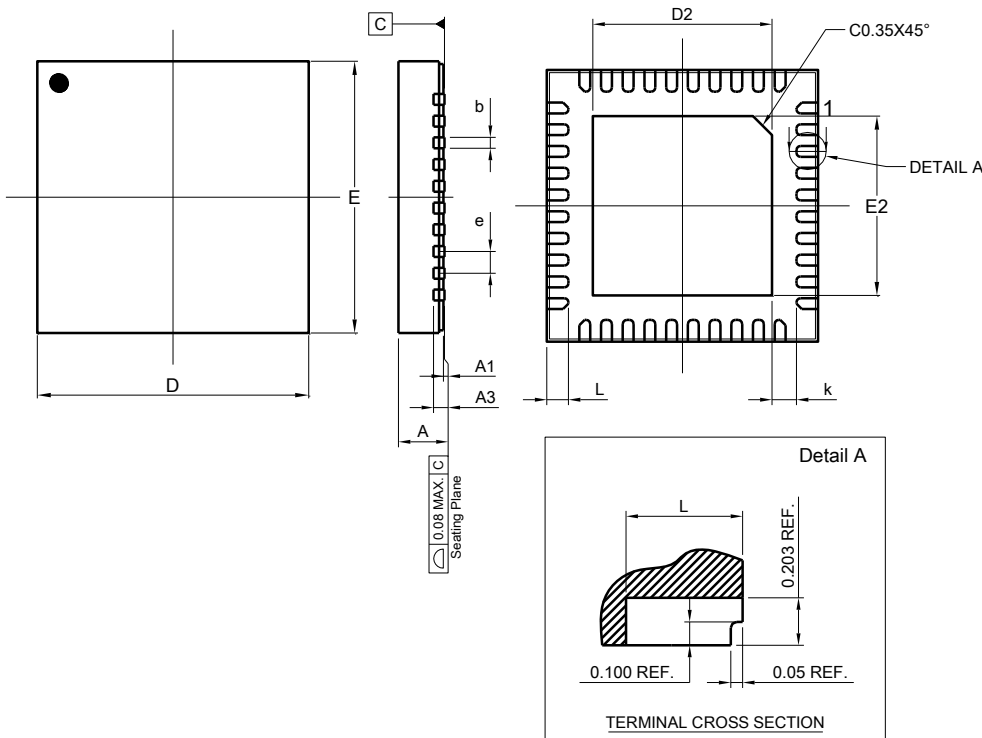
### W-QFN5050-40/SWP (Type A1)



## Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**W-QFN5050-40/SWP (Type A1)**

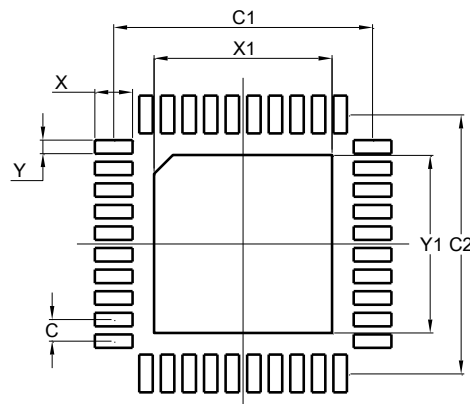


W-QFN5050-40/SWP (Type A1)			
Dim	Min	Max	Typ
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.15	0.25	0.20
D	4.90	5.10	5.00
D2	3.25	3.35	3.30
E	4.90	5.10	5.00
E2	3.25	3.35	3.30
e	0.40 BSC		
k	0.20	--	--
L	0.35	0.45	0.40
All Dimensions in mm			

## Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**W-QFN5050-40/SWP (Type A1)**



Dimensions	Value (in mm)
C	0.400
C1	4.800
C2	4.800
X	0.700
X1	3.300
Y	0.250
Y1	3.300

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## Tape and Reel Information

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Please see <https://www.diodes.com/assets/Packaging-Support-Docs/AP02007.pdf> for tape and reel details.

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## Mechanical Data

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### Package W-QFN5050-40/SWP (Type A1)

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per JESD22-B102 (e3)
- Weight: 0.0091 grams (Approximate)

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