Running CoreTSE_AHB IP based Webserver on SmartFusion2 using lwIP and FreeRTOS – Libero SoC v11.7

DG0634 Demo Guide

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1 Preface

1.1 Purpose

This demo is for SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) devices. It provides instructions on how to use the Webserver reference design using lwIP and FreeRTOS.

1.2 Intended Audience

This demo guide is intended for:

- FPGA designers
- Embedded designers
- System-level designers

1.3 References

The following references are used in this document:

1.3.1 Microsemi Publications

- *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*
- *UG0447: SmartFusion2 and IGLOO2 High Speed Serial Interfaces User Guide*
- *Libero SoC User Guide*
- *UG0541: SmartFusion2 Evaluation Kit User Guide*

Refer to the following web page for a complete and up-to-date listing of SmartFusion2 device documentation: *www.microsemi.com/soc/products/smartfusion2/docs.aspx*.

1.3.2 Others

- lwIP TCP/IP stack: http://download.savannah.gnu.org/releases/lwip/
- FreeRTOS stack: *www.freeRTOS.org*

2 Running CoreTSE_AHB IP based Webserver on SmartFusion2 using lwIP and FreeRTOS

2.1 Introduction

This demo design explains the CoreTSE_AHB IP based implementation of the webserver application on the SmartFusion2 Security Evaluation Kit. SmartFusion2 devices have built-in microcontroller subsystem (MSS) media access controller (MAC) for Ethernet solutions. This demo guide describes how to use the CoreTSE_AHB intellectual property (IP) core and not MSS Ethernet MAC for running the Webserver application. The soft IP CoreTSE_AHB is useful when a solution demands more than one Ethernet interface. Microsemi Core Triple-Speed (CoreTSE) Ethernet IP is a configurable soft IP core that complies with the IEEE 802.3 standard.

The CoreTSE IP core enables system designers to implement a broad range of Ethernet designs, from low cost 10/100 Ethernet to higher performance 1 gigabit ports. The CoreTSE IP core is suited for use in networking equipment such as switches, routers, and data acquisition systems.

The CoreTSE IP has the following major interfaces:

- 10/100/1000 Mbps Ethernet MAC with a gigabit media independent interface (GMII) and ten bit interface (TBI) to support serial gigabit media independent interface (SGMII), 1000BASE-T, and 1000BASE-X.
- GMII or TBI physical layer interface connects to Ethernet PHY
- MAC data path interface

The CoreTSE IP Ethernet MAC can be configured as GMII or TBI for Ethernet network at 10/100/1000 Mbps data transfer rates (line speeds).

The CoreTSE IP core is available in two different versions:

- CoreTSE_AHB: Uses AHB interface for both the transmit and receive paths. This IP works for SmartFusion2 SoC FPGA.
- CoreTSE (Non-AMBA): Uses direct access to the MAC with a streaming packet interface. This IP works for IGLOO®2 FPGA.

For more information about CoreTSE_AHB IP, refer to the *CoreTSE_AHB Handbook*.

Note: CoreTSE_AHB IP core requires license for using in Libero® SoC design. For license request, contact soc_marketing@microsemi.com.

This demo describes the following:

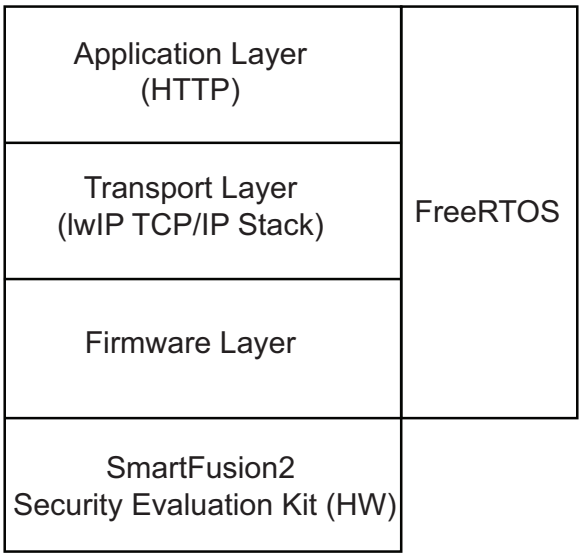
- Use of CoreTSE_AHB IP-based Ethernet MAC connection to an SGMII PHY
- Integration of CoreTSE_AHB driver with the lwIP TCP/IP stack and the FreeRTOS operating system
- Implementation of Webserver on the SmartFusion2 Security Evaluation Kit board
- Procedure to run the Webserver design on the SmartFusion2 Security Evaluation Kit board

The Webserver demo design has the following software layers:

- Application Layer
- Transport Layer (lwIP TCP/IP Stack)
- RTOS and Firmware Layer

Figure 1 shows the block diagram of the webserver application on the SmartFusion2 device.

Figure 1 • **Block Diagram of Webserver Application on SmartFusion2**



2.1.1 Application Layer

The webserver application is implemented on the SmartFusion2 Security Evaluation Kit board.

Webserver handles the HTTP request from the client browser and transfers the static pages to the client in response to their request. These pages run on the client (host PC) browser. When the URL with IP address (for example, http://10.60.3.25) is typed in the browser, the HTTP request is sent to the port on the webserver. The webserver interprets the request and responds to the client with the requested page or resource.

2.1.2 Transport Layer (lwIP TCP/IP Stack)

The lwIP TCP/IP stack was developed by Adam Dunkels at the swedish institute of computer science (SICS). The lwIP stack is suitable for the embedded systems because of the less resource usage. It can be used with or without the operating system. lwIP consists of the actual implementations of the IP, ICMP, UDP, and TCP protocols, as well as the support functions such as buffer and memory management.

The lwIP is available (under a BSD license) in C source-code format for download from the following path: http://download.savannah.gnu.org/releases/lwip/

2.1.3 RTOS and Firmware Layer

FreeRTOS is an open source real time operating system kernel. FreeRTOS is used in this demo to prioritize and schedule the tasks. Refer to http://www.freertos.org for more information and the latest source code.

The firmware provides the software driver implementation to configure and control the following MSS components:

- Multi-mode universal asynchronous receiver/transmitter (MMUART)
- General purpose input and output (GPIO)
- Real-time clock (RTC)

2.2 Design Requirements

Table 1 lists the hardware and software design requirements.

Table 1 • **Design Requirements**

Design Requirements	Description
Hardware Requirements	
SmartFusion2 Security Evaluation Kit: • 12 V adapter • FlashPro4 • USB A to Mini-B cable	Rev D or later
RJ45 cable	–
Host PC or Laptop	Windows 64-bit Operating System
Software Requirements	
Libero System-on-Chip (SoC)	v11.7
FlashPro Programming Software	v11.7
SoftConsole	v3.4 SP1*
Host PC Drivers	USB to UART drivers
Browser	Mozilla Firefox or Internet Explorer
IP Requirements	
CoreTSE_AHB IP	License provided on request
Note: *For this tutorial, SoftConsole v3.4 SP1 is used. For using SoftConsole v4.0, see the *TU0546: SoftConsole v4.0 and Libero SoC v11.7 Tutorial*.	

2.3 Demo Design

2.3.1 Introduction

The demo design files are available for download from the following path in the Microsemi website:
http://soc.microsemi.com/download/rsc/?f=m2s_dg0634_liberov11p7_df

The demo design files include:

- Libero SoC hardware project with SoftConsole firmware project
- Sample files
- Programming files
- `Readme.txt` file

Figure 2 shows the top-level structure of the design files. For more information, refer to the `Readme.txt` file.

Figure 2 • **Demo Design Files Top-Level Structure**

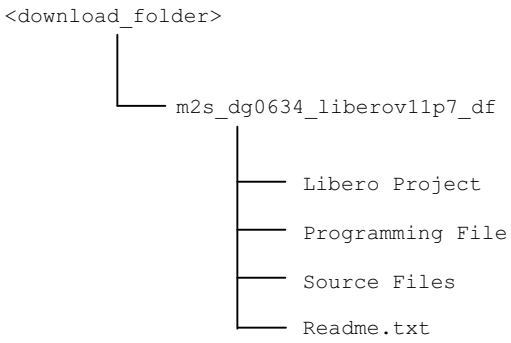
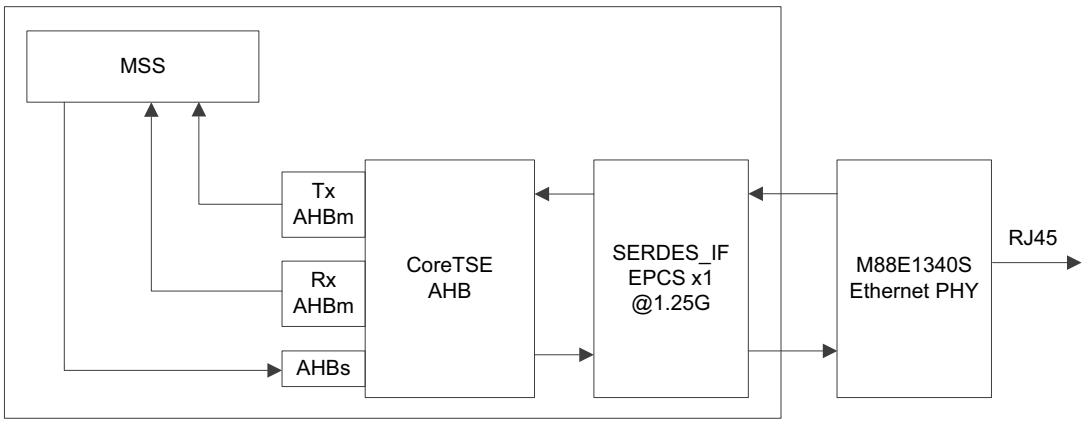


Figure 3 shows the demo design block diagram.

Figure 3 • **Block Diagram of CoreTSE_AHB Webserver Demo**



In the webserver demo design, CoreTSE_AHB IP is instantiated in the FPGA fabric and connected to the on-board Ethernet Marvell PHY using the high-speed serial interface (SERDES_IF).

The following sections explain the initialization and configuration of CoreTSE_AHB, SERDES_IF and the Ethernet packet transmission and reception.

2.3.1.1 CoreTSE_AHB IP MAC Initialization

The CoreTSE_AHB IP MAC is configured in the TBI mode. The ARM® Cortex®-M3 (micro controller subsystem) is used to initialize the CoreTSE_AHB IP MAC in 1000 Base-T and the on-board Ethernet PHY.

2.3.1.2 SERDES_IF Configuration

The high-speed SERDES_IF is configured in the external physical coding sub layer (EPCS) mode lane 3 and is connected between the CoreTSE_AHB IP MAC and the on-board Ethernet PHY.

2.3.1.3 Ethernet Packet Reception

The CoreTSE_AHB IP MAC receives the Ethernet packet from the on-board Ethernet PHY through high-speed SERDES_IF using the built-in DMA controller.

2.3.1.4 Ethernet Packet Transmission

CoreTSE_AHB MAC transmits the Ethernet packet from the built-in DMA controller to the on-board Ethernet PHY through high-speed SERDES_IF.

The Security Evaluation Kit acts a webserver and the host PC acts as a web client that accesses the webserver features through the RJ45 interface.

2.3.2 Demo Design Features

The demo has the following options:

- Webserver
  - RTC and Ethernet interface data display
  - Blinking LEDs
  - HyperTerminal display
  - SmartFusion2 Google search

2.3.3 Demo Design Description

The demo design is implemented using an SGMII PHY interface by configuring the CoreTSE_AHB IP MAC for the ten-bit interface (TBI) operation.

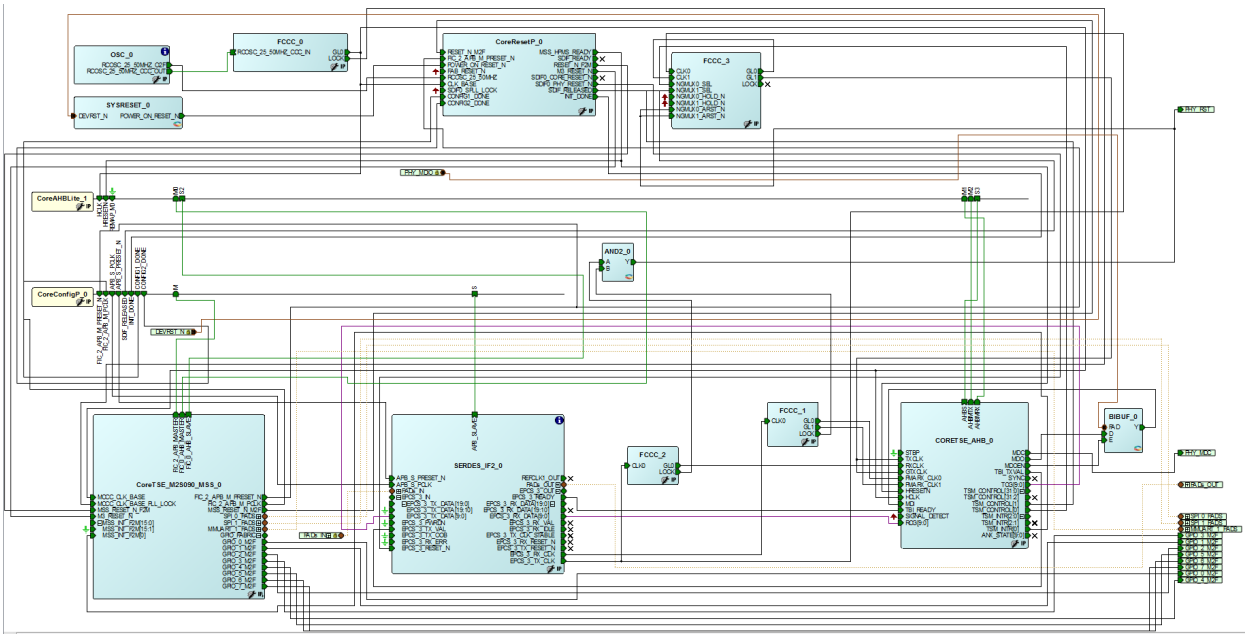
The demo design comprises of:

- Libero SoC Hardware Project
- SoftConsole Firmware Project

2.3.3.1 Libero SoC Hardware Project

Figure 4 shows the Libero SoC hardware design implementation for this demo design.

Figure 4 • **Libero Top-Level Design**

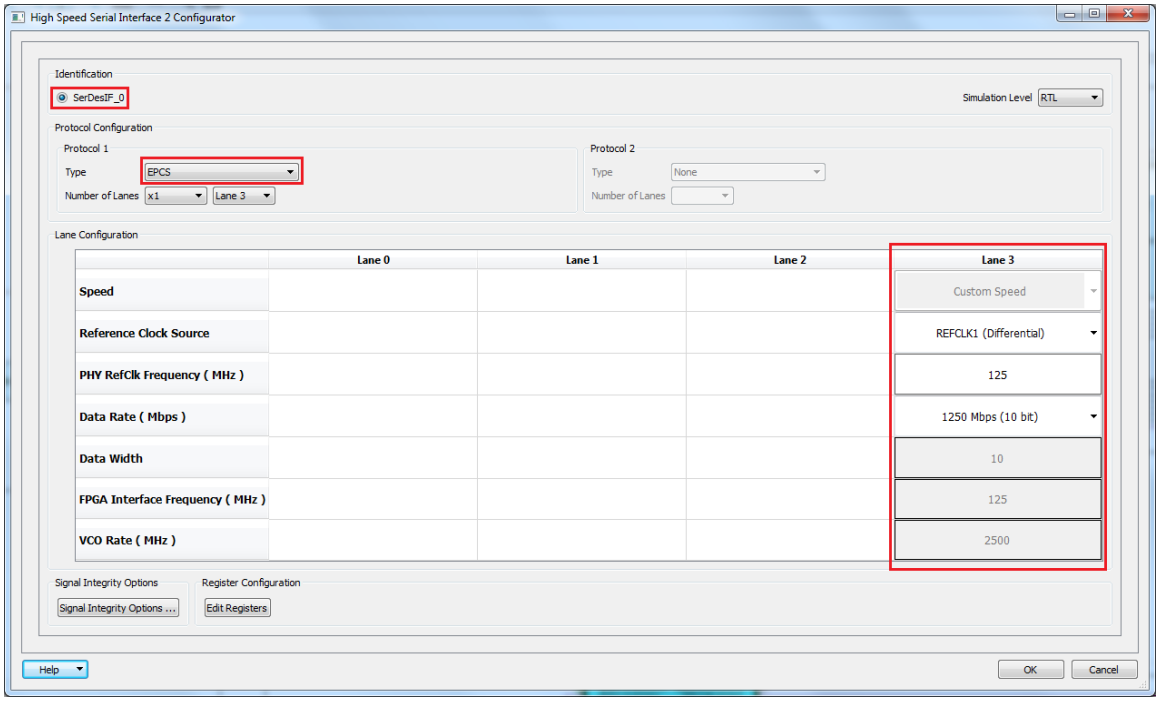


Libero hardware project uses the following SmartFusion2 MSS resources and IPs:

- **MMUART_1** for RS-232 communications on the Security Evaluation Kit
- **GPIO**: Interfaces the light emitting diodes (LEDs)
- **CoreTSE_AHB IP** core
- SERDES_IF and **SERDES_IF_2** configured for **SERDESIF_0 EPCS Lane 3**, as shown in Figure 5.

For more information on SERDES_IF, refer to the *UG0447: SmartFusion2 and IGLOO2 High Speed Serial Interfaces User Guide.*

Figure 5 • **High Speed Serial Interface Configurator Window**



2.3.3.1.1 Package Pin Assignments

Package pin assignments for LEDs and PHY interface signals are shown in Table 2 and Table 3 on page 12.

Table 2 shows the port names for the package pins.

Table 2 • **LED to Package Pins Assignments**

Port Name	Package Pin
LED_1	E1
LED_2	F4
LED_3	F3
LED_4	G7
LED_5	H7
LED_6	J6
LED_7	H6
LED_8	H5

Table 3 shows the port names and directions for the package pins.

Table 3 • **PHY Interface Signals to Package Pins Assignments**

Port Name	Direction	Package Pin
PHY_MDC	Output	J3
PHY_MDIO	Input	J4
PHY_RST	Output	K6

2.3.3.2 SoftConsole Firmware Project

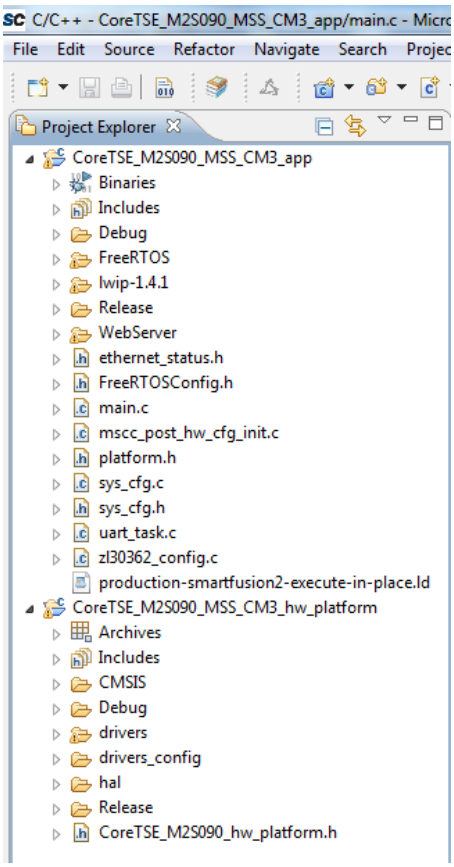
Open the CoreTSE_AHB webserver SoftConsole project using the standalone SoftConsole IDE.

The following stacks are used for this demo design:

- **lwIP TCP/IP** stack version 1.4.1
- **FreeRTOS** (www.freertos.org)

Figure 6 shows the SoftConsole software directory structure of the demo design.

Figure 6 • **SoftConsole Project Explorer Window**



The SoftConsole workspace has the following projects:

- CoreTSE_M2S090_MSS_CM3_app: Contains webserver application implementation using lwIP and FreeRTOS.
- CoreTSE_M2S090_MSS_CM_hw_platform: Contains all the firmware and hardware abstraction layers of the hardware design. This project is configured as a library and is referenced by the CoreTSE_M2S090_MSS_CM3_app project. The contents of this folder get overwritten every time the root design is regenerated in the Libero SoC software.

Note: To run the SoftConsole project in debug mode refer to "Appendix: Running the SoftConsole Project in Debug Mode" on page 27.

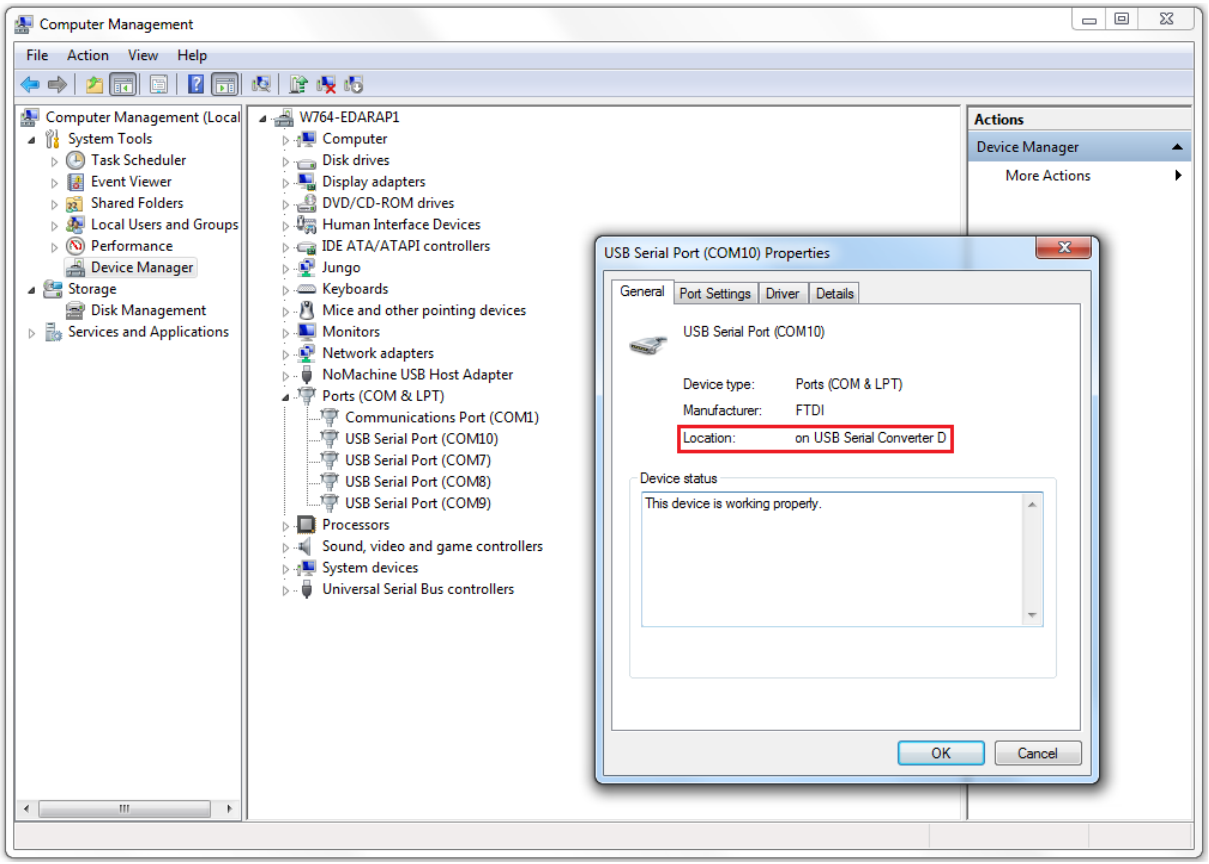
2.4 Setting Up the Demo Design

The following steps describe how to setup the demo for the SmartFusion2 Security Evaluation Kit board:

1. Connect the host PC to the J18 connector using the USB A to Mini-B cable. The USB to UART bridge drivers are automatically detected.
2. From the detected four COM ports, right-click any one of the COM ports and select Properties. The selected COM port properties window is displayed, as shown in Figure 7.
3. Ensure to have the **Location** as **on USB Serial Converter D** in the Properties window, as shown in Figure 7.

Note: Make a note of the COM port number for serial port configuration and ensure that the COM port location is specified as **on USB Serial Converter D**.

Figure 7 • **Device Manager Window**



4. Install the USB driver, if it is not detected automatically.
5. Install the FTDI D2XX driver for serial terminal communication through the FTDI Mini USB cable. Download the drivers and installation guide from: www.microsemi.com/soc/documents/CDM_2.08.24_WHQL_Certified.zip

6. Connect the jumpers on the SmartFusion2 Security Evaluation Kit board, as shown in Table 4. For information on jumper locations, refer to "Appendix: Jumper Locations" on page 23.

CAUTION: Switch **OFF** the power supply switch, **SW7**, before making the jumper connections.

Table 4 • **SmartFusion2 FPGA Security Evaluation Kit Jumper Settings**

Jumper	Pin (From)	Pin (To)	Comments
J22, J23, J24, J8, J3	1	2	These are the default jumper settings of the SmartFusion2 Security Evaluation Kit board. Ensure that jumpers are set accordingly.

7. Connect the power supply to the J6 connector in the SmartFusion2 Security Evaluation Kit.
8. This design example can run in both static IP and dynamic IP modes. By default, the programming files are provided for dynamic IP mode.
    - For static IP, connect the host PC to the J13 connector on the SmartFusion2 Security Evaluation Kit board using an RJ45 cable.
    - For dynamic IP, connect any one of the open network ports to the J13 connector of the SmartFusion2 Security Evaluation Kit board using an RJ45 cable.

2.4.1 Board Setup Snapshot

Snapshots of the SmartFusion2 Security Evaluation Kit board with the setup is given in "Appendix: Board Setup for Running the Demo" on page 22.

2.5 Running the Demo Design

1. Download the demo design from:
   http://soc.microsemi.com/download/rsc/?f=m2s_dg0634_liberov11p7_df
2. Switch **ON** the SW7 power supply switch.
3. Start any of the serial terminal emulation programs such as:
    - HyperTerminal
    - PuTTY
    - TeraTerm

Note: In this demo, HyperTerminal is used.

The configuration for the program is:

- Baud Rate: 115200
- Eight data bits
- One stop bit
- No parity
- No flow control

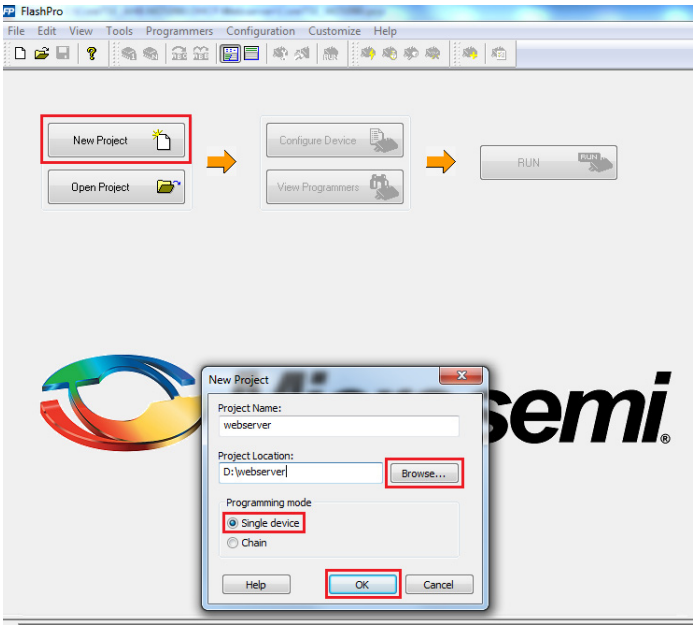
For information on configuring the serial terminal emulation programs, refer to the *Configuring Serial Terminal Emulation Programs Tutorial*.

2.5.1 Running the Webserver Demo

The following steps describe how to run the webserver demo:

1. Launch the **FlashPro** software.
2. Click **New Project**.
3. In the **New Project** window, enter the project name.

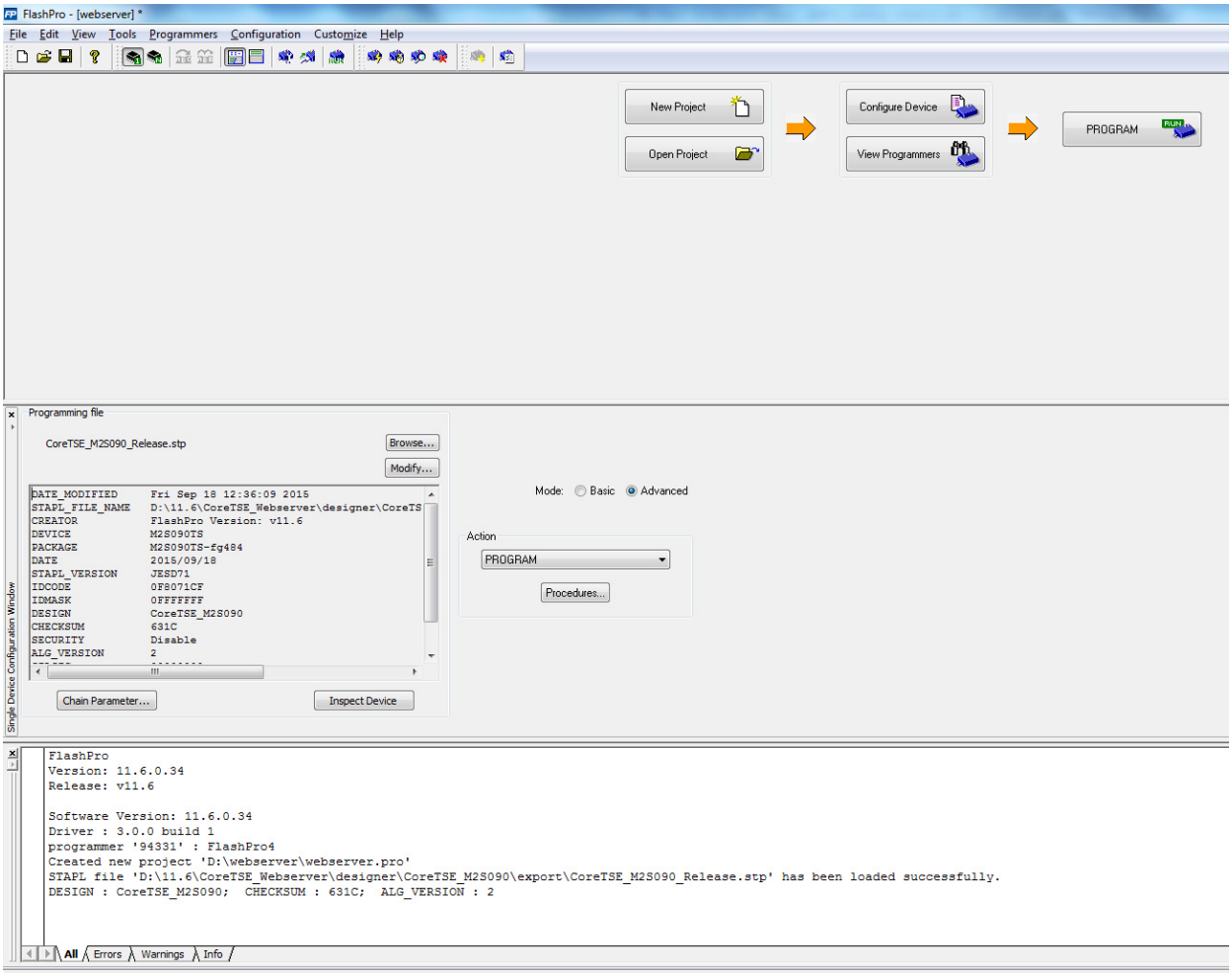
Figure 8 • **FlashPro New Project**



4. Click **Browse** and navigate to the location where the project is required to be saved.
5. Select **Single device** as the **Programming mode**.
6. Click **OK** to save the project.

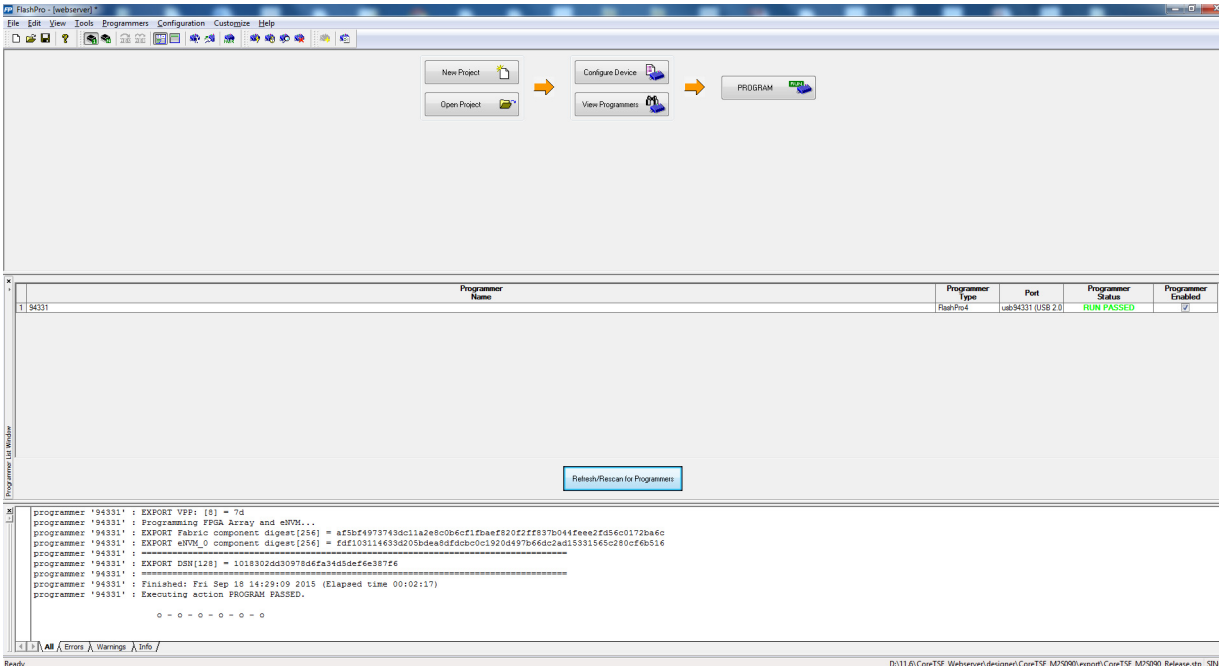
7. Click **Configure Device,** as shown in Figure 9.
8. Click **Browse** and navigate to the location where the file is located and select the file. The default location is: *<download_folder>\ProgrammingFiles\webserver.* The required programming file is selected and is ready to be programmed in the device.

Figure 9 • **FlashPro Project Configured**



9. Click **PROGRAM** to start programming the device. Wait until a message is displayed indicating that the program has passed.

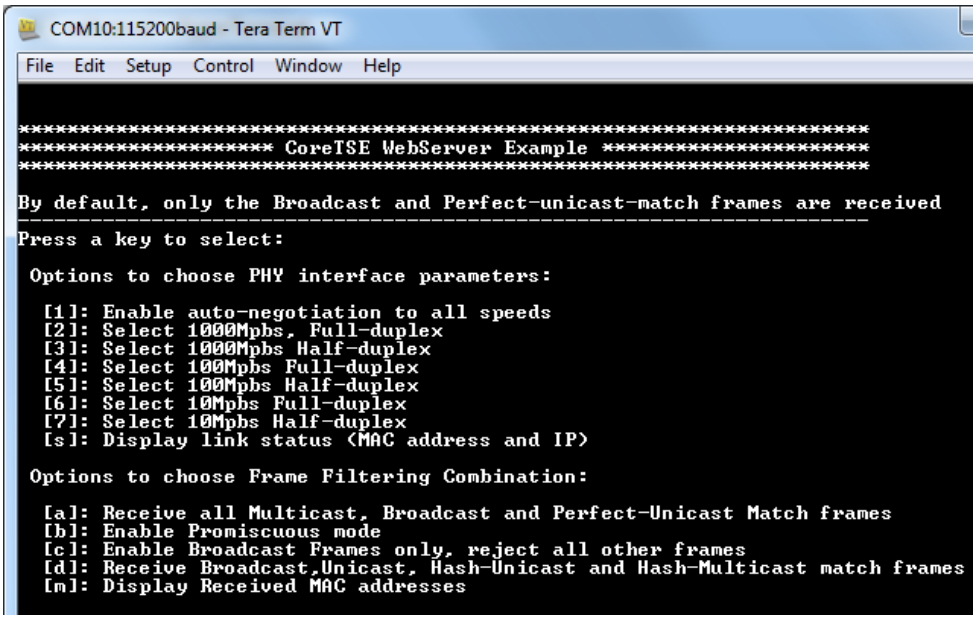
Figure 10 • **FlashPro Program Passed**



Note: The demo can be run in static and dynamic modes. To run the design in static IP mode, follow the steps mentioned in the "Appendix: Running the Design in Static IP Mode" on page 24.

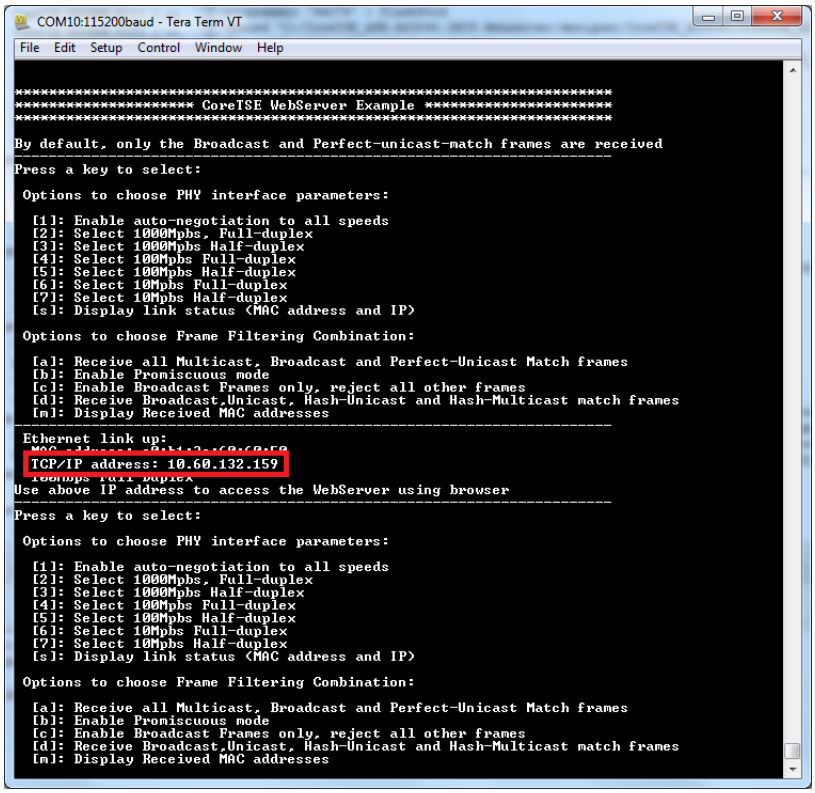
10. Power cycle the SmartFusion2 Security Evaluation Kit board.
    A welcome message is displayed in the HyperTerminal window, as shown in Figure 11.

Figure 11 • **HyperTerminal with Welcome Message**



11. Press **S** on the keyboard till the IP address is displayed, as shown in Figure 12.

Figure 12 • **HyperTerminal with IP Address**

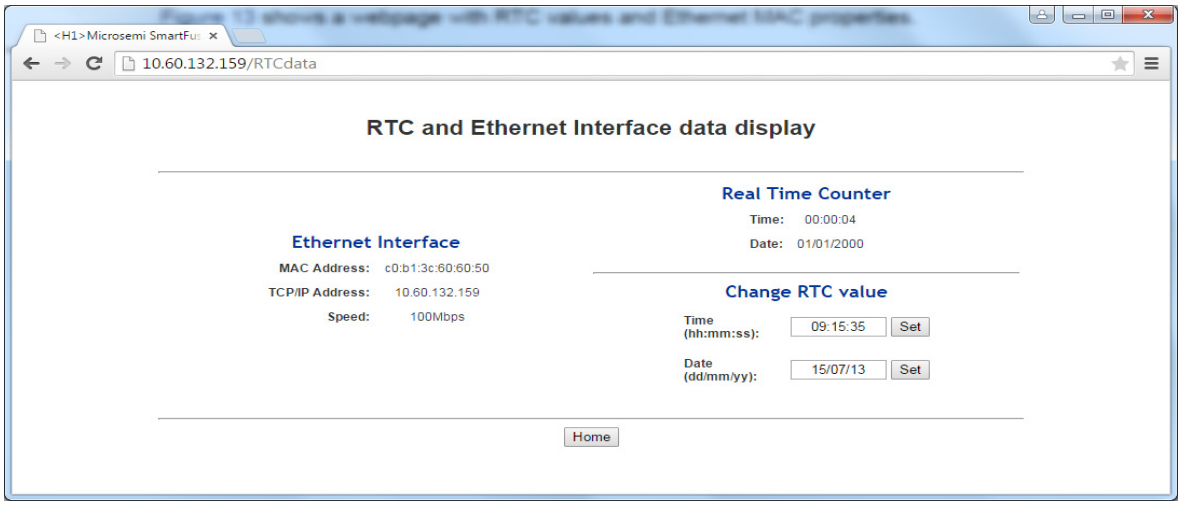


12. Enter the IP address displayed on the HyperTerminal in the address bar of the browser (Mozilla Firefox) to run the webserver. The main menu of the webserver is shown in Figure 13.
13. Click **RTC and Ethernet Interface data display** on the main menu of webserver demo.

Figure 13 • **Main Menu of Webserver**

Figure 14 shows the webpage with RTC values and Ethernet MAC properties.

Figure 14 • **Webserver RTC and Ethernet Interface Data Display**



14. Click **Home** to go back to the main menu.
15. Click **Blinking LED's** on the main menu.

Figure 15 • **Selecting Blinking LEDs**

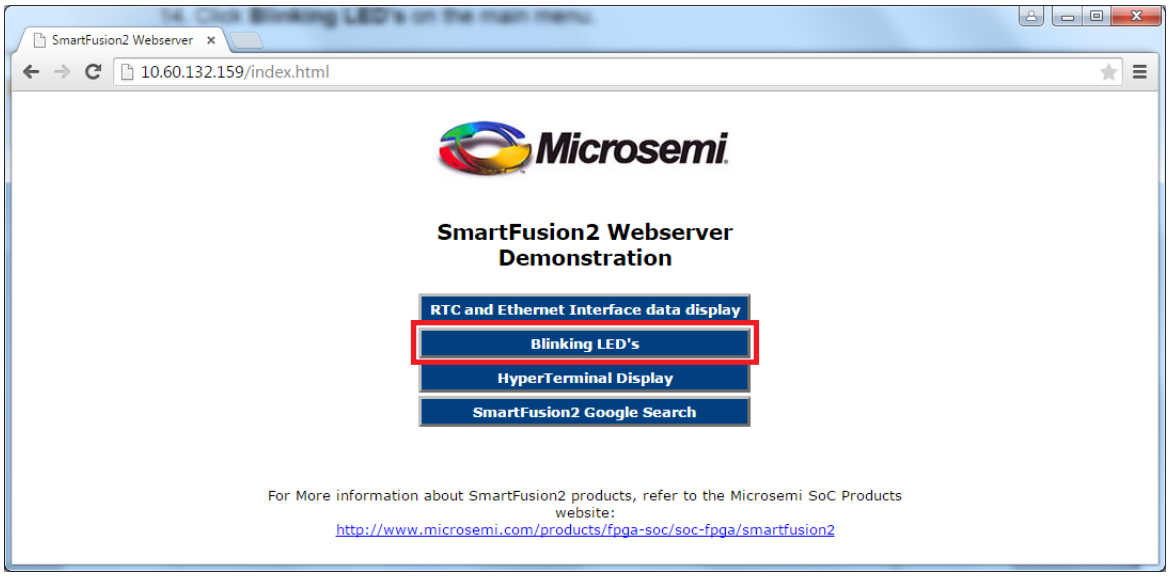
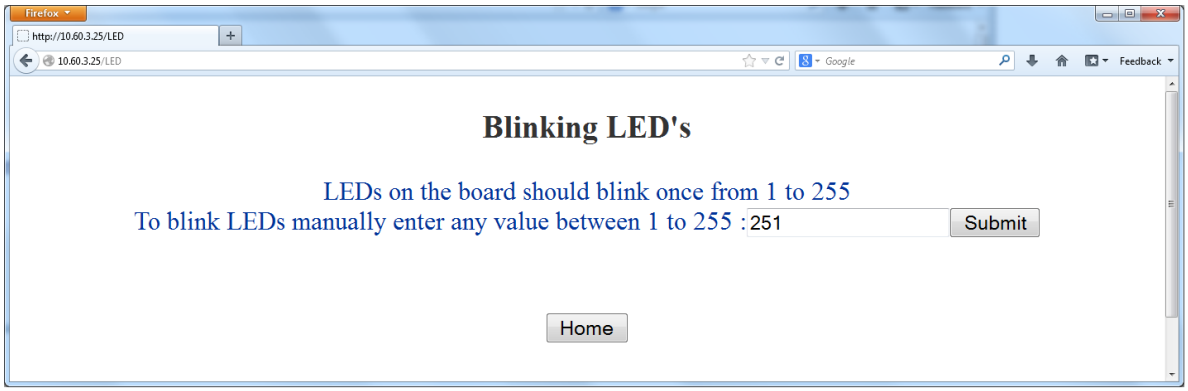


Figure 16 shows a running LED pattern on the board. The webpage displays an option to enter the values to blink the LEDs manually.

16. Enter any number between 1 to 255, to toggle the LEDs manually and click **Submit**. For example, if 1 is entered, LED1 goes OFF. If 255 is entered, all the eight LEDs go OFF.

Note: The SmartFusion2 Security Evaluation Kit has Active Low LEDs.

Figure 16 • **Blinking LEDs**



17. Click **Home** to go back to the main menu.
18. Click **HyperTerminal Display** on the main menu.

Figure 17 • **Selecting HyperTerminal Display**

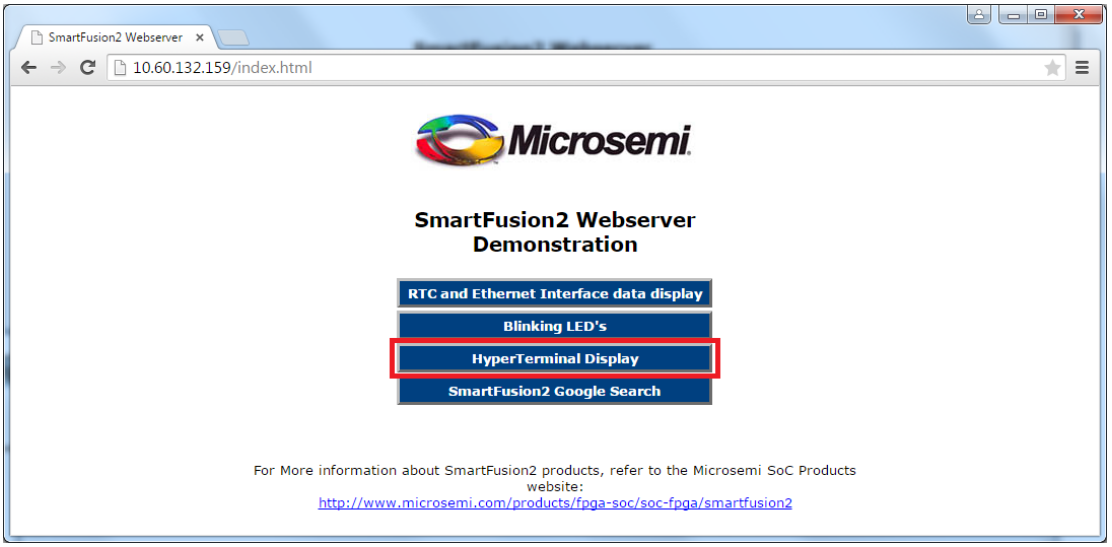
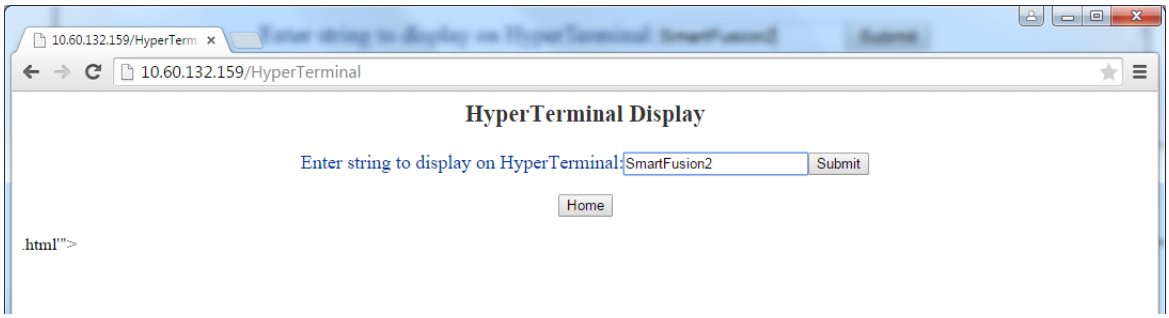


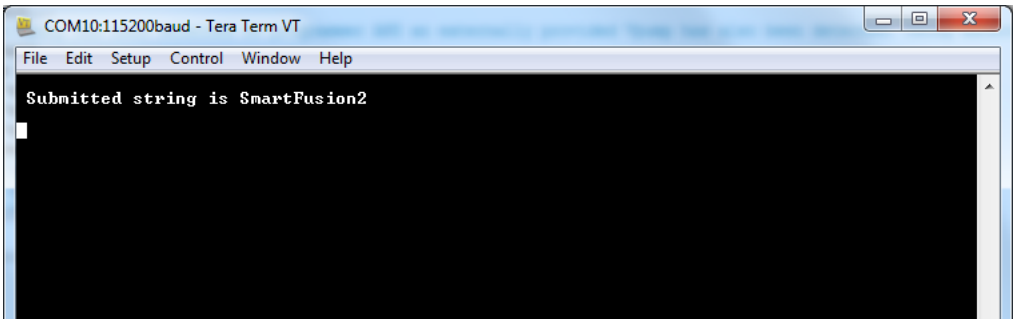
Figure 18 shows the webpage that displays an option to enter a string value.

Figure 18 • **Webserver HyperTerminal Display**



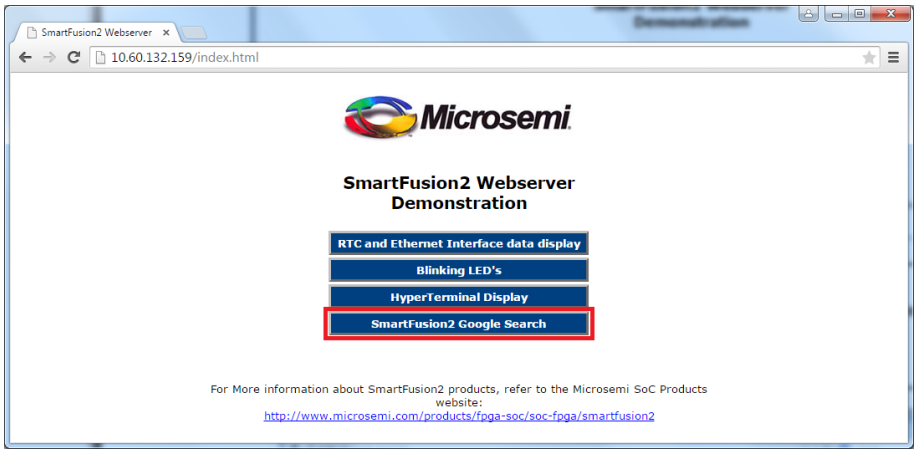
The entered string is displayed on HyperTerminal, as shown in Figure 19.

Figure 19 • **String Display on HyperTerminal**



19. Click **Home** to go back to the main menu.
20. Click **SmartFusion2 Google Search** on the main menu.

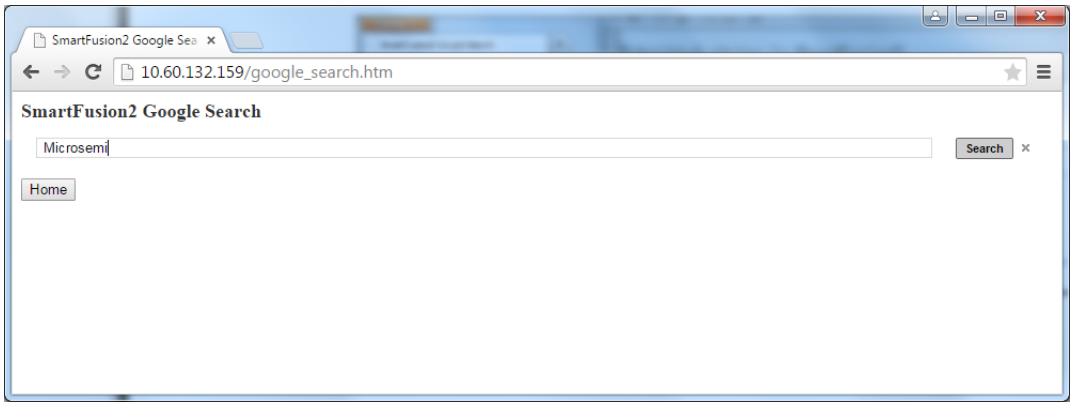
Figure 20 • **Selecting SmartFusion2 Google Search**



Note: Internet connection with proper access rights is required to get to the SmartFusion2 Google search page.

Figure 21 shows the webpage with Google search option.

Figure 21 • **Webserver SmartFusion2 Google Search**

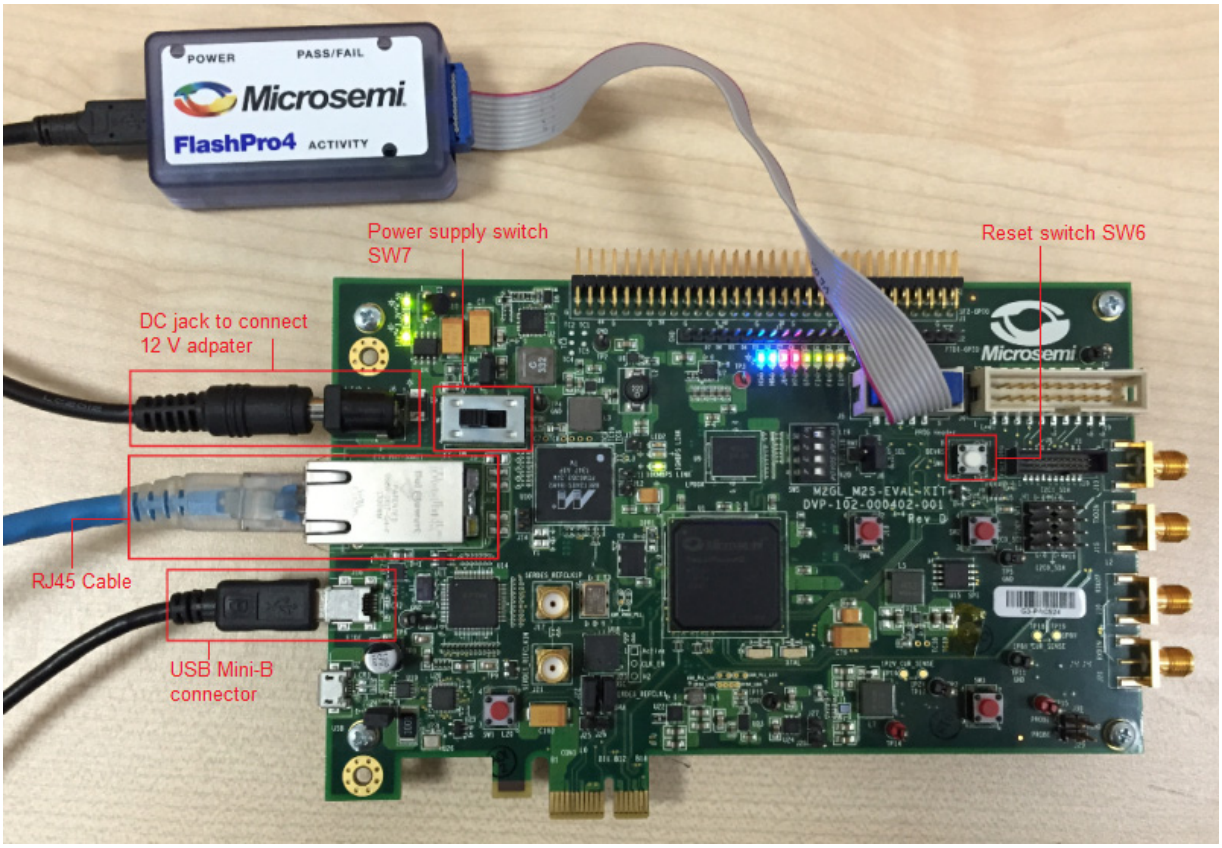


21. Click **Home** to go back to the main menu.

3 Appendix: Board Setup for Running the Demo

Figure 22 shows the board setup for running the demo on the SmartFusion2 Security Evaluation Kit board.

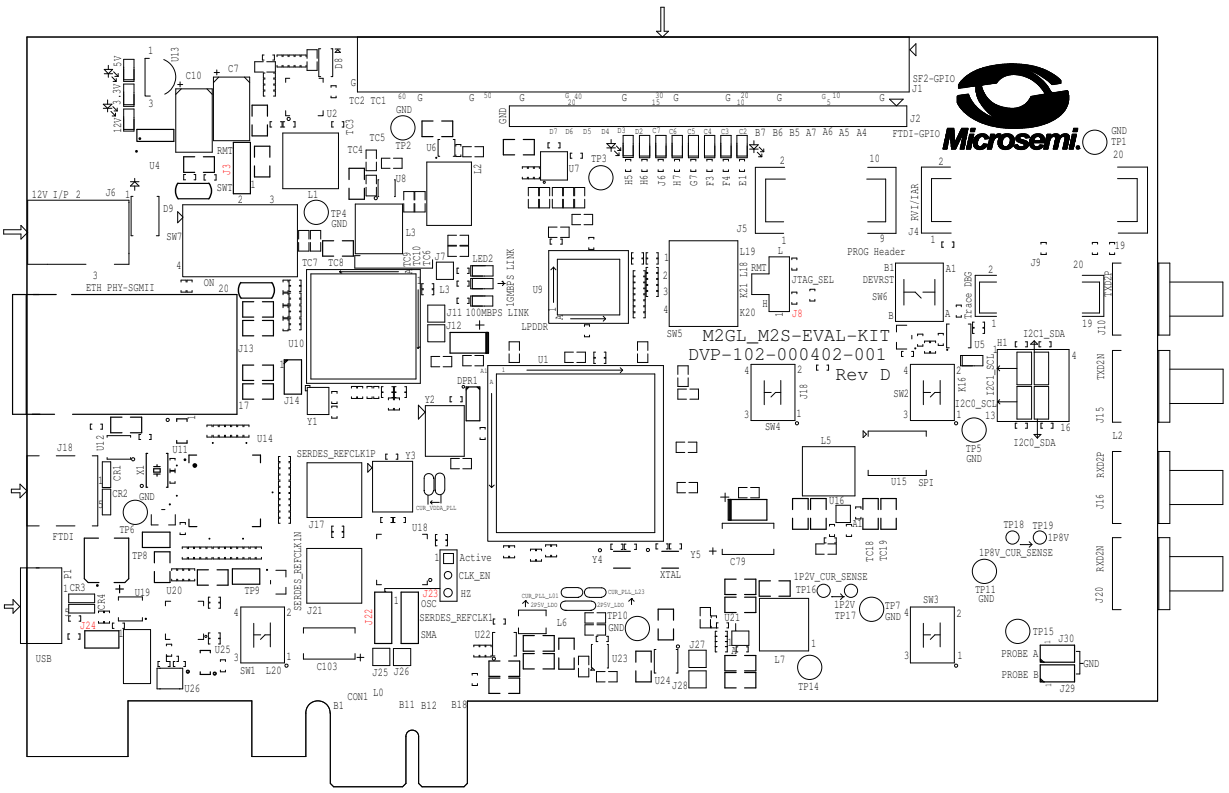
Figure 22 • **SmartFusion2 Security Evaluation Kit Setup**



4 Appendix: Jumper Locations

Figure 23 shows the jumper locations in the SmartFusion2 Security Evaluation Kit board.

Figure 23 • **SmartFusion2 Security Evaluation Kit Silkscreen Top View**



Notes:

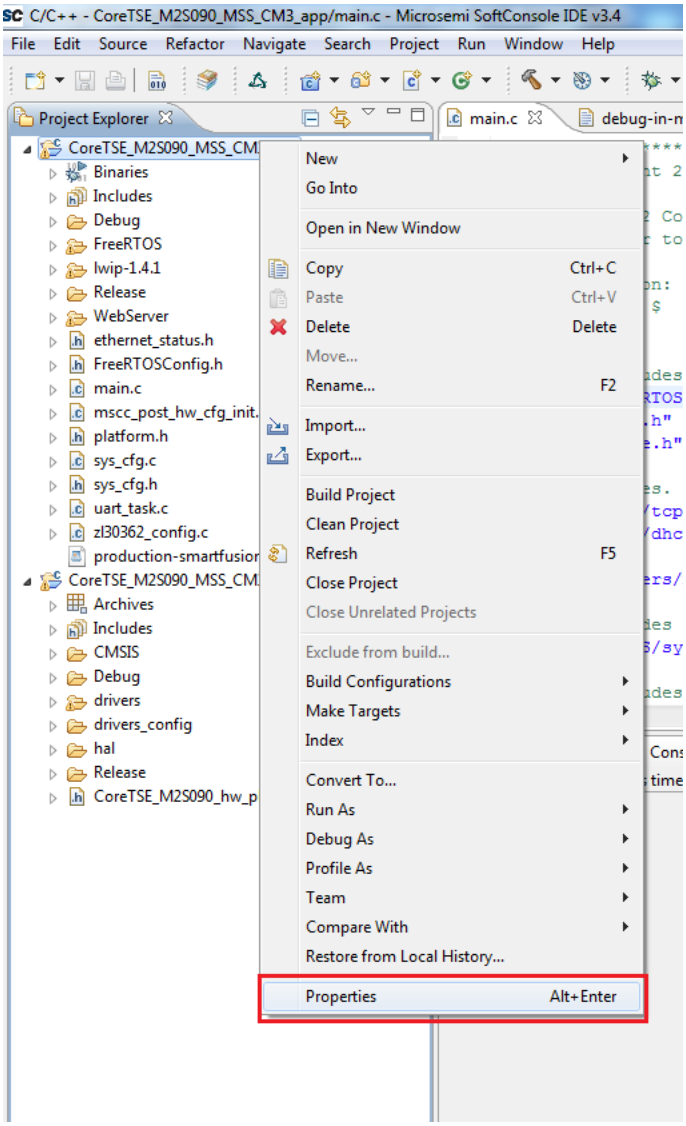
- Jumpers highlighted in red are set by default.
- The location of the jumpers in Figure 23 are searchable.

5 Appendix: Running the Design in Static IP Mode

The following steps describe how to run the design in static IP mode:

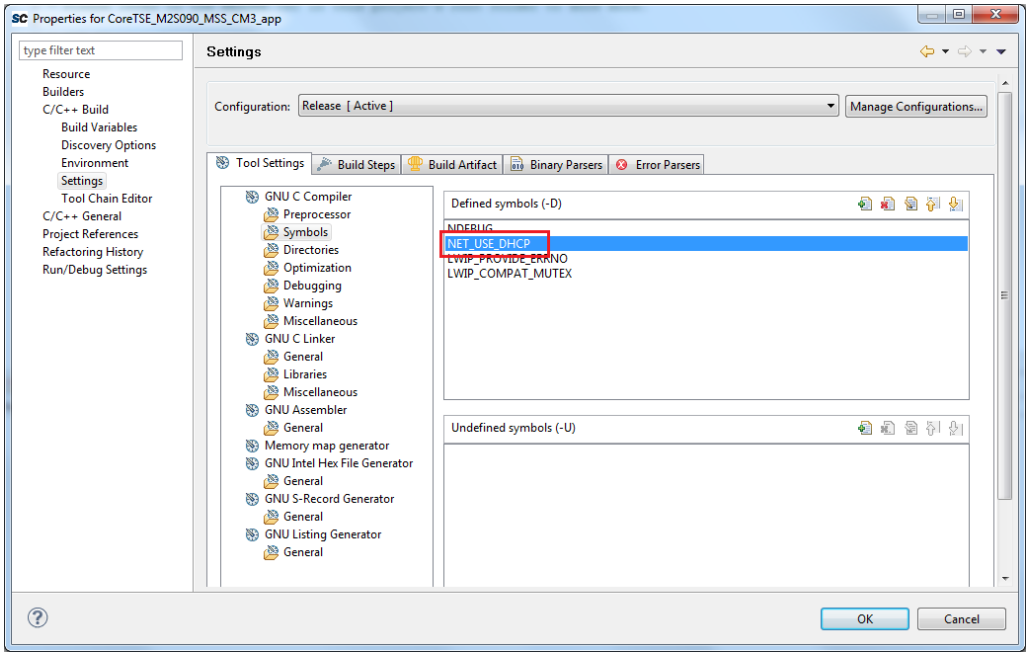
1. To run the webserver design in static IP mode, right-click the **CoreTSE_M2S090_MSS_CM3_app project** and select **Properties,** as shown in Figure 24.

Figure 24 • **Project Explorer Window of SoftConsole Project**



2. Remove the symbol **NET_USE_DHCP** in **Tool Settings** of the **Properties** for **CoreTSE_M2S090_MSS_CM3_app** window, as shown in Figure 25.

Figure 25 • **CoreTSE_M2S090_MSS_CM3_app Properties Window**



3. If the device is connected in static IP mode and the board static IP address is 169.254.1.23, change the host TCP/IP settings to reflect the IP address. Figure 26 shows the host PC TCP/IP settings.

Figure 26 • **Host PC TCP/IP Settings**

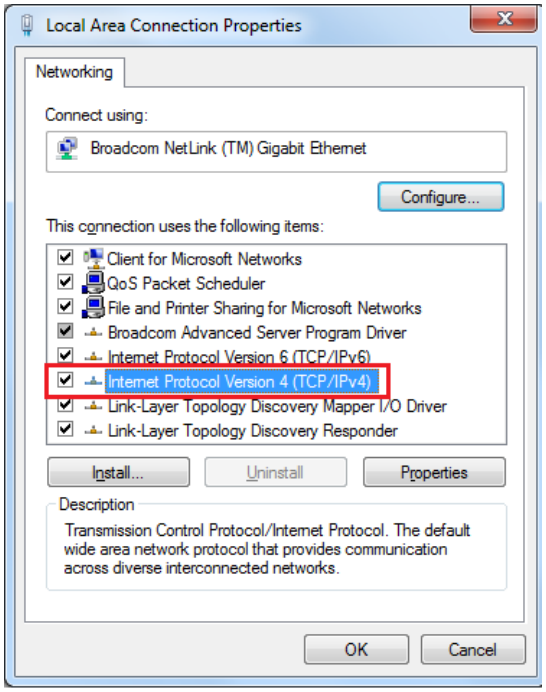
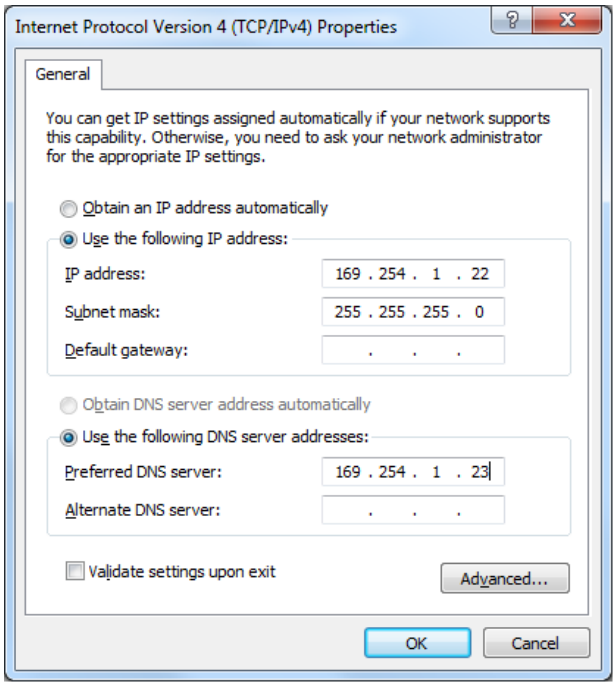


Figure 27 shows the static IP address settings.

Figure 27 • **Static IP Address Settings**



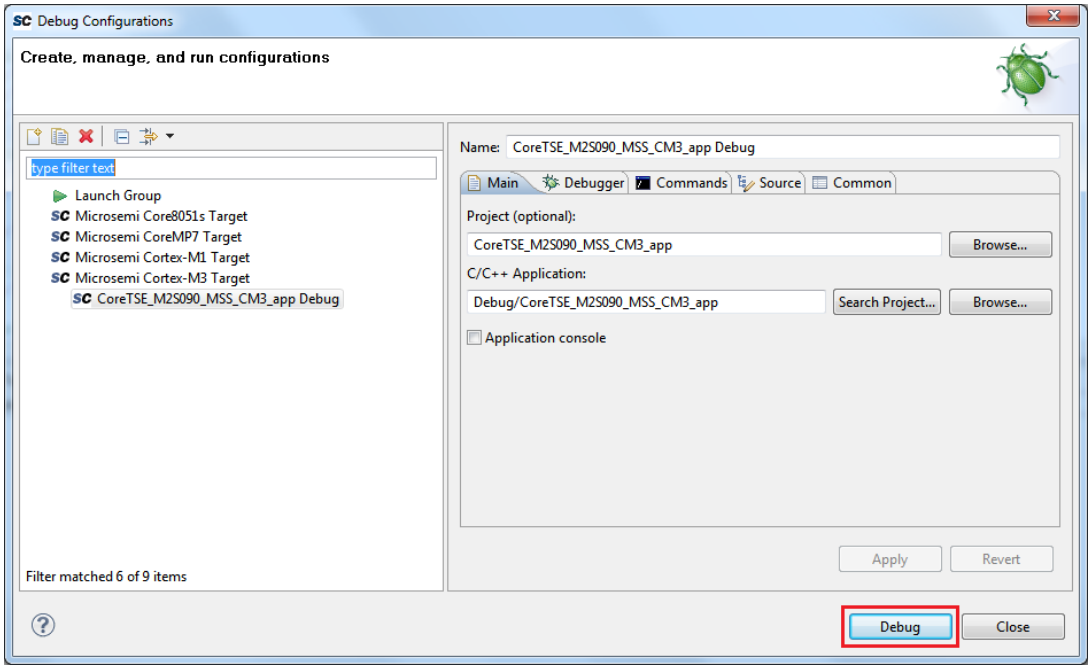
4. After these settings are made, compile the design, load the design into memory, and run the design using the SoftConsole.

6 Appendix: Running the SoftConsole Project in Debug Mode

The following steps describe how to run the SoftConsole project in Debug mode:

1. Select **Debug Configurations** from the **Run** menu of the SoftConsole. The **Debug Configurations** dialog box is displayed, as shown in Figure 28.

Figure 28 • **Debug Configurations**



2. Select the target and click **Debug**.

Note: To run the application in debug mode, FlashPro4 JTAG programmer is required.

7 Revision History

The following table shows important changes made in this document for each revision.

Revision*	Changes
Revision 2 (March 2016)	Updated the document for Libero v11.7 software release (SAR 77067).
Revision 1 (September 2015)	Initial release.
Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.	

8 Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

8.1 Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

8.2 Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

8.3 Technical Support

For Microsemi SoC Products Support, visit
http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

8.4 Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/products/fpga-soc/fpga-and-soc.

8.5 Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

8.5.1 Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

8.5.2 My Cases

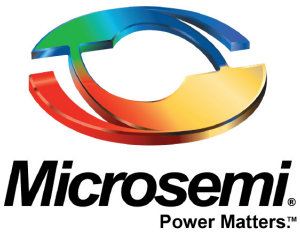
Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

8.5.3 Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Visit About Us for sales office listings and corporate contacts.

8.6 ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.



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