AF31G

Hardware Design

Wi-Fi&Bluetooth Module Series

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The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergent help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or

	metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-06-23	Barret XIONG/Logan ZHANG	Creation of the document
1.0.0	2022-06-23	Barret XIONG/Logan ZHANG	Preliminary
1.0.1	2022-07-19	Barret XIONG	Preliminary： 1. Updated the pin names: 20, 21, 24, 25, 27, 28, 58, 59, 60, 61, 62, 63 2. Updated the Pin Assignment (Figure 2) 3. Updated the weight of AF31G (Table 2) 4. Updated the SDIO routing requirements (Chapter 4.1.1.2) 5. Updated the packaging information (Chapter 8.3) 6. Updated the Absolute Maximum Ratings of VDD_IO (Table 23)

Contents

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1 Introduction

This document, describing AF31G and its air interface and hardware interfaces connected to your applications, informs you of the interface and RF specifications, electrical and mechanical details, as well as other related information of the module.

With the application notes and user guides provided separately, you can easily use the module to design and set up mobile applications.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

AF31G is an automotive grade Wi-Fi and Bluetooth module with low power consumption. It is complying with IEEE 802.11a/b/g/n/ac 2.4 GHz & 5 GHz WLAN standards and Bluetooth 5.0 standard, which enables seamless integration of WLAN and Bluetooth Low Energy technologies.

It supports a low-power PCIe Gen2 interface for Wi-Fi and a UART/PCM interface for Bluetooth, and it also supports LTE & Wi-Fi/Bluetooth coexistence interface.

Table 2: Brief Introduction of the Module

AF31G	
Footprint	LGA
Pin numbers	112
Size	(23 ±0.2) mm × (23 ±0.2) mm × (3 ±0.2) mm
Weight	3.11 g
Wireless network functions	Wi-Fi and Bluetooth 5.0

2.1. Key Features

Table 3: Key Features

Parameter	Details
Power Supply	**VDD_PA:** ● 3.14–3.46 V ● Typical: 3.3 V **VDD_IO:** ● 1.71–1.89 V ● Typical: 1.8 V
Frequency Range	**Wi-Fi:** ● 2.4 GHz: 2.400–2.4835 GHz ● 5 GHz: 5.150–5.850 GHz **Bluetooth:** ● 2.4 GHz: 2.402–2.480 GHz
Wi-Fi Transmission Data Rates	**802.11b:** ● 1 Mbps, 2 Mbps, 5.5 Mbps, 11 Mbps **802.11g:** ● 6 Mbps, 9 Mbps, 12 Mbps, 18 Mbps, 24 Mbps, 36 Mbps, 48 Mbps, 54 Mbps **802.11n:** ● HT20 (MCS 0-7), HT40 (MCS 0-7) **802.11a:** ● 6 Mbps, 9 Mbps, 12 Mbps, 18 Mbps, 24 Mbps, 36 Mbps, 48 Mbps, 54 Mbps **802.11ac:** ● VHT20 (MCS 0-8), VHT40 (MCS 0-9), VHT80 (MCS 0-9)
Protocol Features	● IEEE 802.11a/b/g/n/ac ● Bluetooth 5.0
Wi-Fi Modulation	BPSK, QPSK, CCK, 16QAM, 64QAM and 256QAM
Bluetooth Modulation	GFSK, 8-DPSK and π/4-DQPSK
Wi-Fi Operating Modes	● AP ● STA
Wireless Connection Interface	● Wi-Fi: PCIe Gen2 interface used for Wi-Fi function ● Bluetooth: UART and PCM interfaces used for Bluetooth function
WLAN_SLP_CLK	32 kHz clock interface, provide clock function when the module is under low power consumption mode
Antenna Interfaces	● Wi-Fi & Bluetooth antenna interfaces ● 50 Ω characteristic impedance

Operating Temperature	● Operating Temperature Range: -40 °C to +85 °C [1] ● Storage temperature range: -40 °C to +95 °C
RoHS	All hardware components are fully compliant with EU RoHS directive.

2.2. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- Radio frequency
- Peripheral interfaces

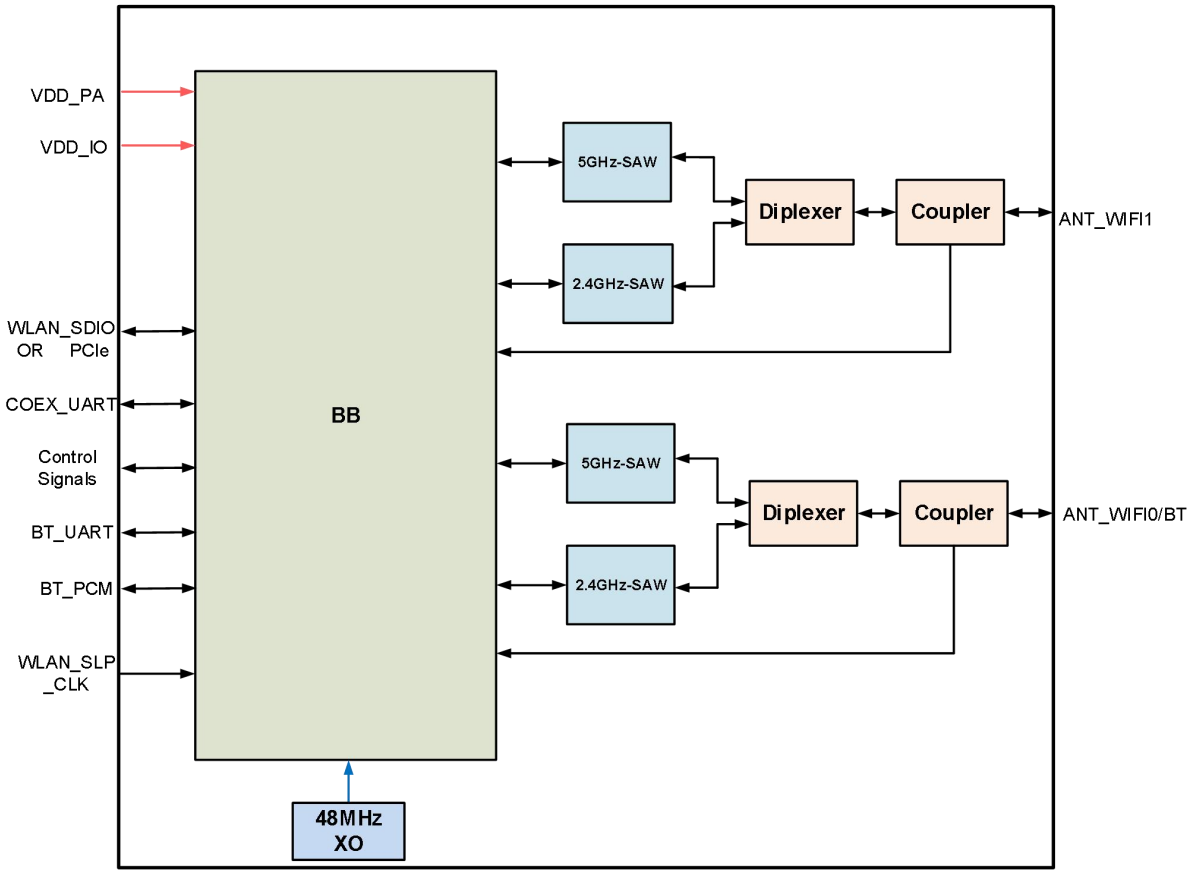


Figure 1: Functional Diagram

[1] To meet normal operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this temperature range, the module's related indicators can meet IEEE and Bluetooth specifications.

2.3. Pin Assignment

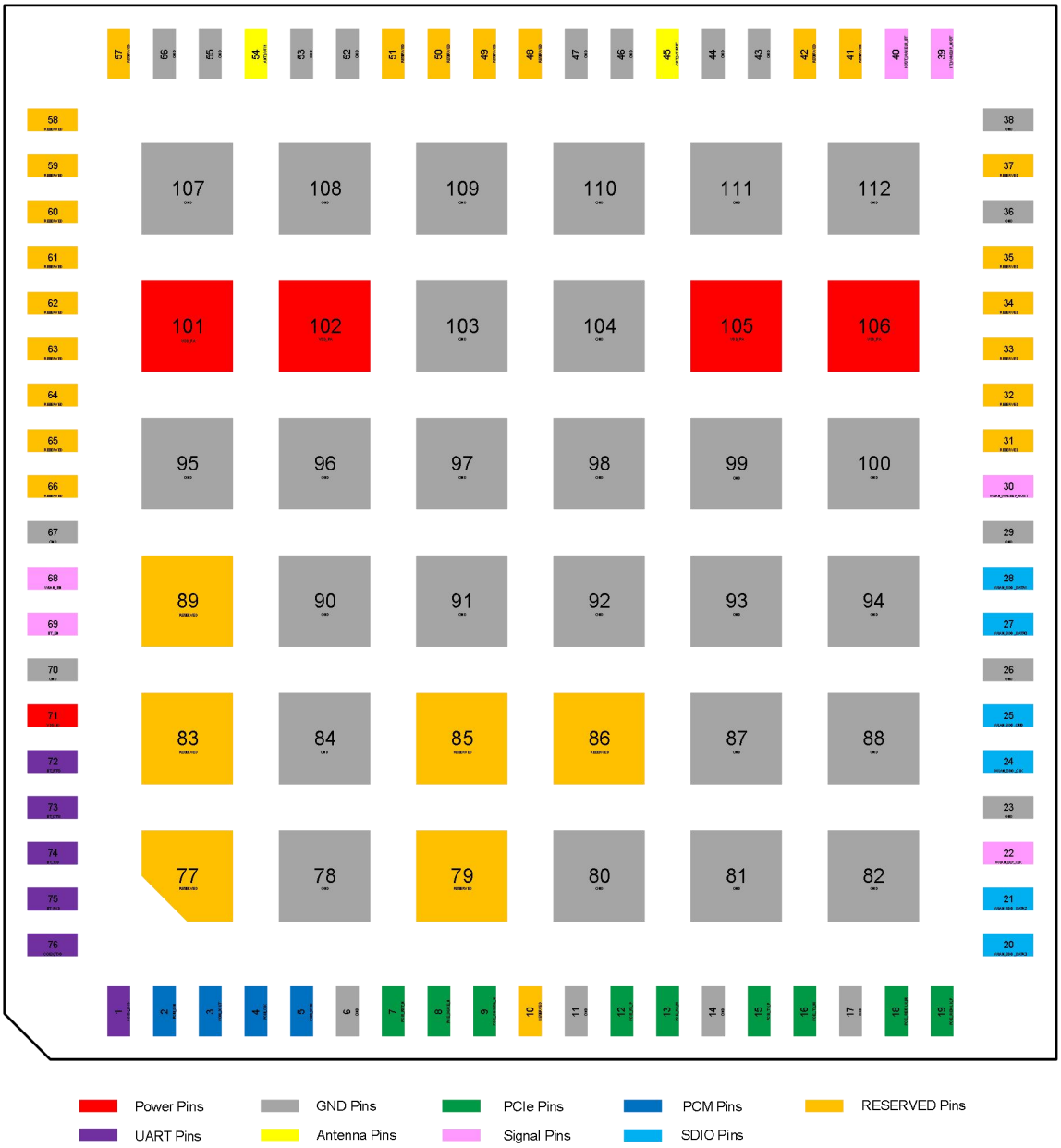


Figure 2: Pin Assignment (Top View)

NOTE

1. Please keep all RESERVED pins open.
2. SDIO interface and PCIe interface exist in different hardware modules respectively. Modules supporting PCIe interface do not support SDIO interface. At this time, it is necessary to suspend the pins of all SDIO interfaces, and vice versa.

2.4. Pin Description

Table 4: Parameters Definition

Parameter	Description
AI	Analog input
AO	Analog output
DI	Digital Input
DO	Digital output
OD	Open drain
PI	Power input
PO	Power output

Table 5: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comments**
VDD_PA	101, 102, 105, 106	PI	Main Power supply for module	3.3 V	It must be provided with sufficient current up to 1.5 A.
VDD_IO	71	PI	Voltage supply for I/O	1.8 V	It must be provided with sufficient current up to 300 mA.
GND	6, 11, 14, 17, 23, 26, 29, 36, 38, 43, 44, 46, 47, 52, 53, 55, 56, 67, 70, 78, 80, 81, 82, 84, 87, 88, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 103, 104, 107, 108, 109, 110, 111, 112				
Bluetooth Application Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comments**
BT_WAKEUP_HOST	39	DO	Bluetooth Wakeup Host	1.8 V	VDD_IO power domain.
HOST_WAKEUP_BT	40	DI	Host Wakeup Bluetooth		

BT_EN	69	DI	Bluetooth enable control		VDD_IO power domain. Active high.
PCM_DIN	2	DI	PCM data input		VDD_IO power domain.
PCM_SYNC	5	DI	PCM data frame sync		
PCM_CLK	4	DI	PCM clock		
PCM_DOUT	3	DO	PCM data output		
BT_TXD	74	DO	Bluetooth UART transmit		
BT_RXD	75	DI	Bluetooth UART receive		
BT_RTS	72	DO	Request To Send		
BT_CTS	73	DI	Clear To Send		
SDIO Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comments**
WLAN_WAKEUP_HOST	30	DO	SDIO wake up Host	1.8 V	VDD_IO power domain. Active low.
WLAN_SDIO_CLK	24	DI	WLAN SDIO bus clock		VDD_IO power domain.
WLAN_SDIO_CMD	25	DIO	WLAN SDIO bus command		
WLAN_SDIO_DATA0	27	DIO	WLAN SDIO data bus D0		
WLAN_SDIO_DATA1	28	DIO	WLAN SDIO data bus D1		
WLAN_SDIO_DATA2	21	DIO	WLAN SDIO data bus D2		
WLAN_SDIO_DATA3	20	DIO	WLAN SDIO data bus D3		
PCIe Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comments**
WLAN_EN	68	DI	Wi-Fi enable control	1.8 V	VDD_IO power domain.
PCIE_CLK_P	19	AI	PCIe reference		Require

			clock (+)		differential impedance of 85 Ω.
PCIE_CLK_M	18	AI	PCIe reference clock (-)		
PCIE_TX_P	15	AO	PCIe transmit (+)		
PCIE_TX_M	16	AO	PCIe transmit (-)		
PCIE_RX_P	12	AI	PCIe receive (+)		
PCIE_RX_M	13	AI	PCIe receive (-)		
PCIE_CLKREQ_N	9	OD	PCIe clock request	1.8 V	VDD_IO power domain.
PCIE_WAKE_N	8	OD	PCIe wakes up host		
PCIE_RST_N	7	DI	PCIe reset		
Coexistence UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comments**
COEX_TXD	76	DO	LTE/WLAN & Bluetooth coexistence transmit	1.8 V	VDD_IO power domain. If unused, keep this pin open.
COEX_RXD	1	DI	LTE/WLAN & Bluetooth coexistence receive		
Sleep Clock Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comments**
WLAN_SLP_CLK	22	DI	External 32.768 kHz sleep clock input	1.8 V	VDD_IO power domain.
RF Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comments**
ANT_WIFI0/BT	45	IO	2.4/5 GHz Wi-Fi antenna interface 0 and Bluetooth antenna		50 Ω characteristic impedance.

			interface
ANT_WIFI1	54	IO	2.4/5 GHz Wi-Fi antenna interface 1

Reserved Interface		
Pin Name	**Pin No.**	**Comments**
RESERVED	10, 31, 32, 33, 34, 37, 41, 42, 48, 49, 50, 51, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 77, 79, 83, 85, 86, 89	

3 Operating Characteristics

3.1. Power Supply

3.1.1. Power Supply Pins

The following table shows the power supply pins and the ground pins of AF31G.

Table 6: Pin Definition of Power Supply

Pin Name	Pin No.	I/O	Description	Comments
VDD_PA	101, 102, 105, 106	PI	Main power supply for module	It must be provided with sufficient current up to 1.5 A.
VDD_IO	71	PI	Voltage supply for I/O	It must be provided with sufficient current up to 300 mA.
GND	6, 11, 14, 17, 23, 26, 29, 36, 38, 43, 44, 46, 47, 52, 53, 55, 56, 67, 70, 78, 80, 81, 82, 84, 87, 88, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 103, 104, 107, 108, 109, 110, 111, 112			

3.1.2. Reference Design for Power Supply

AF31G is powered by VDD_PA, and it is recommended to use a power supply chip with maximum output current exceeding 1.5 A. The following figure shows a reference design for VDD_PA is controlled by WLAN_PWR_EN1.

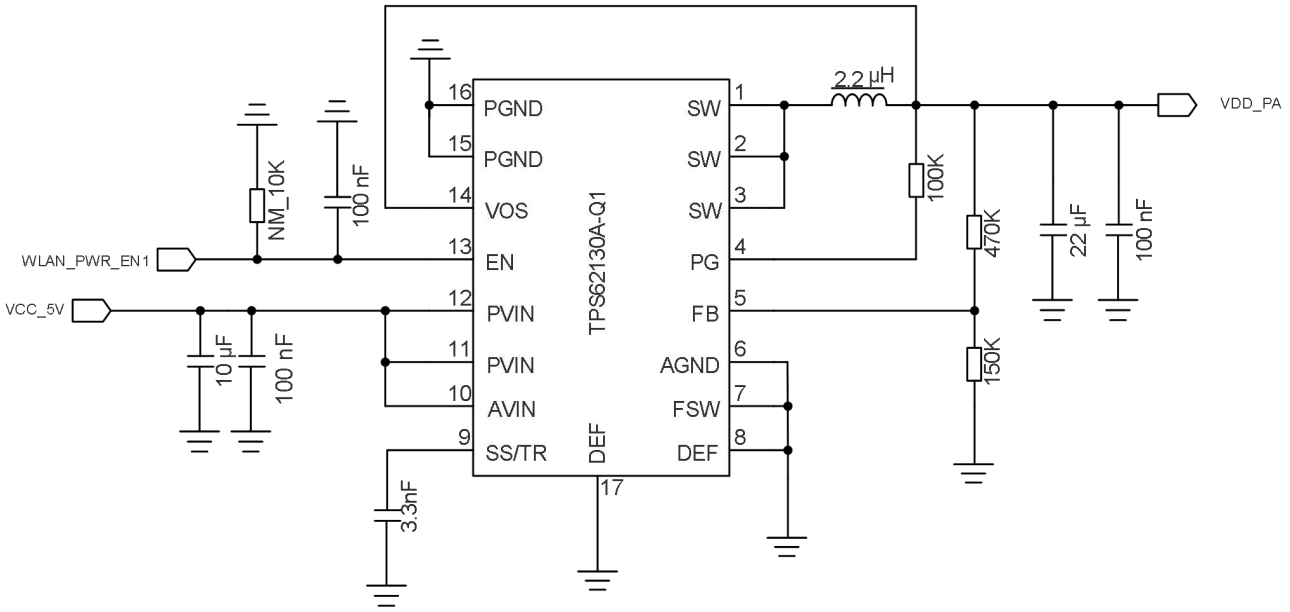


Figure 3: Reference Circuit for VDD_PA

The power supply for I/O in AF31G is from VDD_IO, and it is recommended to use a power supply chip with maximum output current exceeding 300 mA. The following figure shows a reference design for VDD_IO is controlled by WLAN_PWR_EN2.

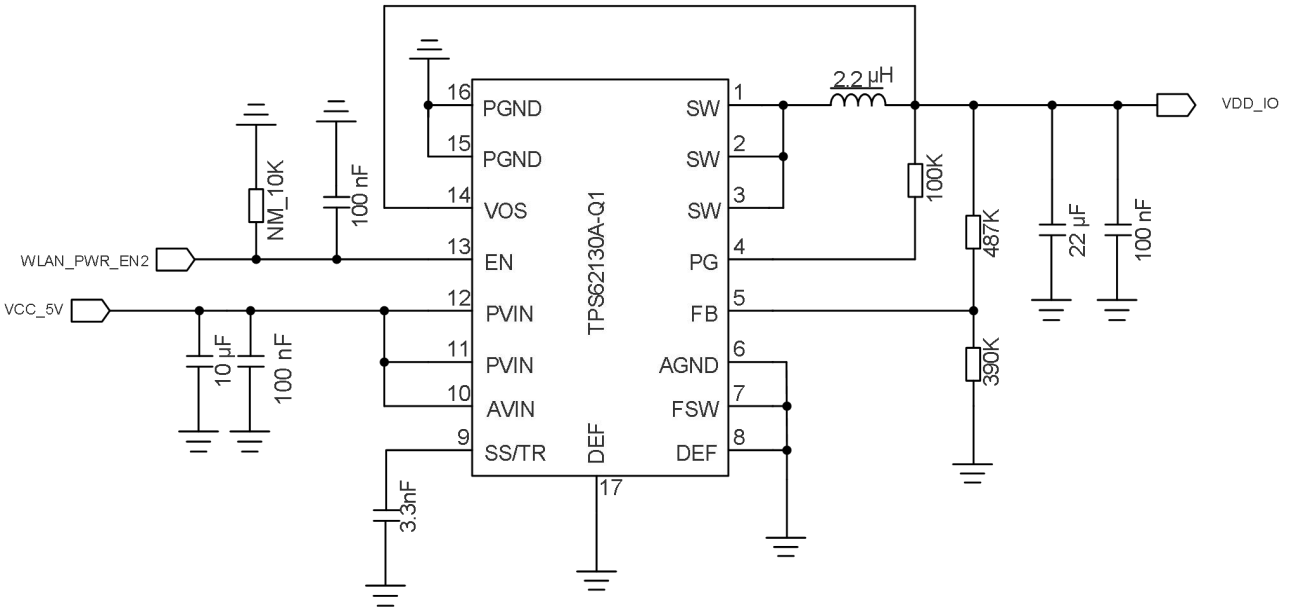


Figure 4: Reference Circuit for VDD_IO

3.1.3. Timing of Turning on the Module

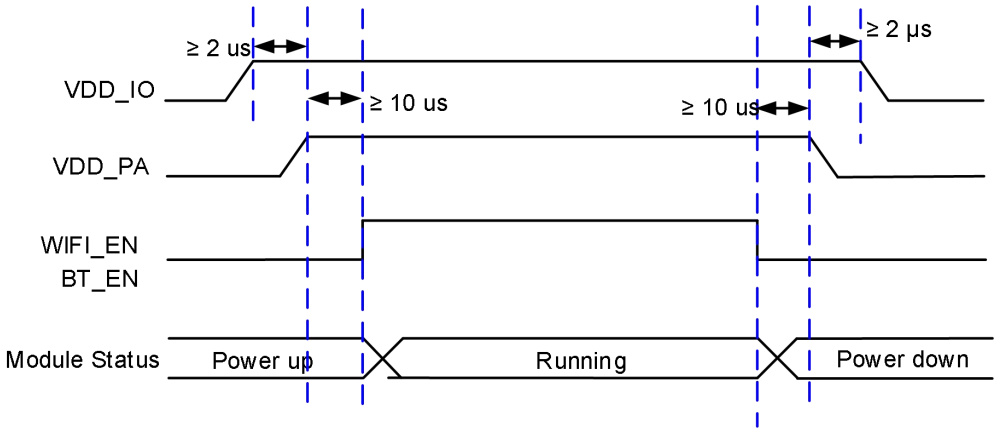


Figure 5: Power-up Timing

4 Application Interfaces

4.1. Wireless Connection Interface

AF31G supports low power PCIe Gen2 interface or SDIO 3.0 for Wi-Fi function and UART as well as PCM interfaces for Bluetooth function.

4.1.1. Wi-Fi Application Interface

The following figure shows the Wi-Fi application interface connection between AF31G and AG52x series modules. SDIO interface and PCIe interface exist in different hardware modules respectively. Please make sure witch AF31G module used.

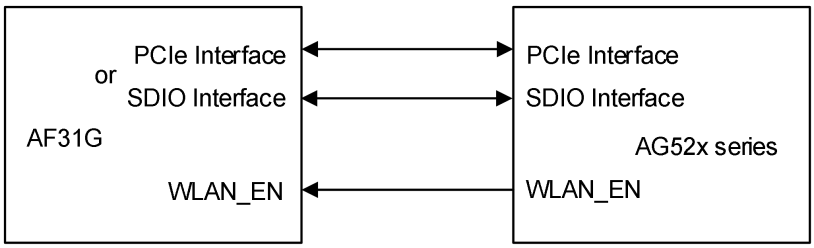


Figure 6: Wi-Fi Application Interface Connection

4.1.1.1. PCIe Interface

Table 7: Pin Definition of PCIe Interface

Pin Name	Pin No.	I/O	Description	Comments
PCIE_REFCLK_P	19	AI	PCIe reference clock (+)	Require differential impedance of 85 Ω.
PCIE_REFCLK_M	18	AI	PCIe reference clock (-)	
PCIE_TX_P	15	AO	PCIe transmit (+)	
PCIE_TX_M	16	AO	PCIe transmit (-)	

PCIE_RX_P	12	AI	PCIe receive (+)	
PCIE_RX_M	13	AI	PCIe receive (-)	
PCIE_CLKREQ_N	9	OD	PCIe clock request	
PCIE_WAKE_N	8	OD	PCIe wakes up host	VDD_IO power domain
PCIE_RST_N	7	DI	PCIe reset	

The following figure shows the PCIe interface connection between AF31G and AG52x series modules.

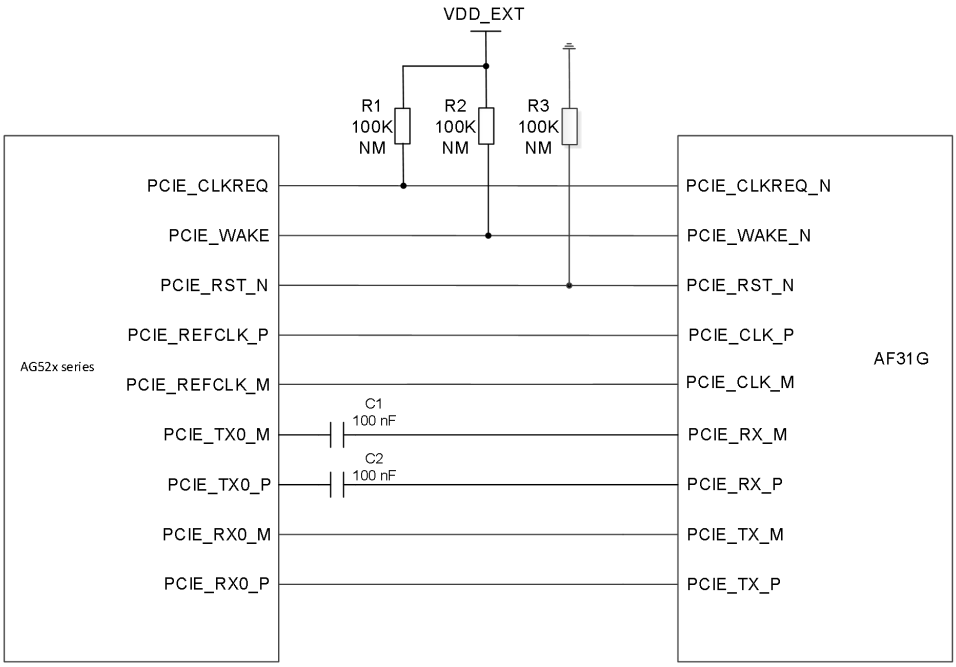


Figure 7: PCIe Interface Connection

In order to ensure the integrity of PCIe signal, C1 and C2 components must be placed close to AG52x series modules. The extra stubs of traces must be as short as possible.

The following principles of PCIe interface design should be complied with, to meet PCIe Gen2 specifications.

- It is important to route the PCIe signal traces (PCIE_TX/PCIE_RX/PCIE_REFCLK) as differential pairs with total grounding. And the differential impedance is 85 Ω ±10%.
- For PCIe signal traces, the maximum length of each differential data pair (PCIE_TX/PCIE_RX/ PCIE_REFCLK) is recommended to be less than 300 mm, and each differential data pair mat ching should be less than 0.7 mm (5 ps).
- The trace space between TX differential data pair and RX differential data pair should be three times wider than PCIe trace width.

- The trace space between PCIe signals and the other signals should be four times wider than PCIe trace width.
- Do not route signal traces under crystals, oscillators, magnetic devices, or RF signal traces. It is important to route the PCIe differential traces in inner-layer of the PCB and surround the traces with ground on that layer and with ground planes above and below.

4.1.1.2. SDIO Interface

Table 8: Pin Definition of SDIO Interface

Pin Name	Pin No.	I/O	Description	Comments
WLAN_WAKEUP_HOST	30	DO	SDIO wake up Host	VDD_IO power domain. Active low.
WLAN_SDIO_CLK	24	DI	WLAN SDIO bus clock	VDD_IO power domain.
WLAN_SDIO_CMD	25	DIO	WLAN SDIO bus command	
WLAN_SDIO_DATA0	27	DIO	WLAN SDIO data bus D0	
WLAN_SDIO_DATA1	28	DIO	WLAN SDIO data bus D1	
WLAN_SDIO_DATA2	21	DIO	WLAN SDIO data bus D2	
WLAN_SDIO_DATA3	20	DIO	WLAN SDIO data bus D3	

The following figure shows the SDIO interface connection between AF31G and AG52x series modules.

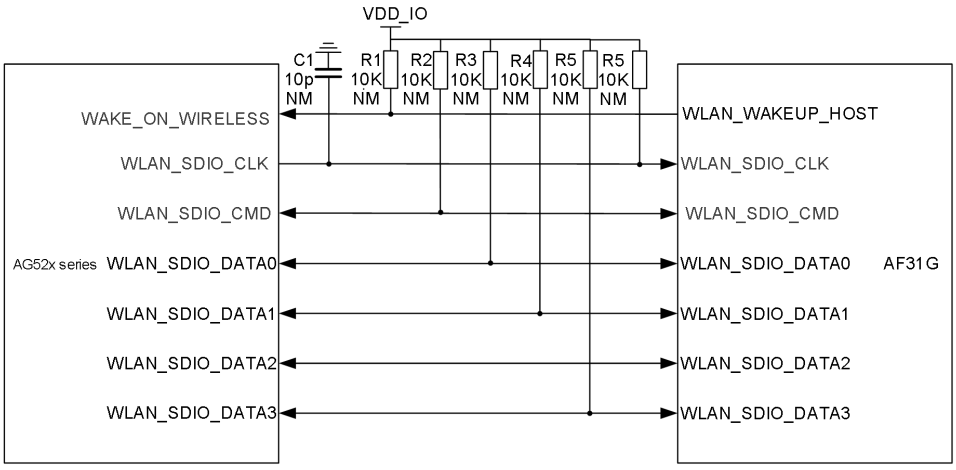


Figure 8: SDIO Interface Connection

As SDIO signals are very high-speed, in order to ensure the SDIO interface design corresponds with the SDIO 3.0 specification, please comply with the following principles:

- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO signal trace is 50 Ω ±10%.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is recommended to keep matching length between WLAN_SDIO_CLK and WLAN_SDIO_DATA[0:3]/WLAN_SDIO_CMD less than 1 mm and total routing length less than 50 mm. AF31G has 14 mm of internal tracing and 36 mm of external tracing.
- It is recommended that keep termination resistors within 15–24 Ω on clock lines near the module and keep the route distance from the module clock pins to termination resistors less than 5 mm.
- Make sure the adjacent trace spacing is 2 times of the trace width and bus capacitance is less than 15 pF.

4.1.1.3. WLAN_EN

WLAN_EN is used to control the Wi-Fi function of AF31G. Wi-Fi function will be enabled when WLAN_EN is at high level.

Table 9: Pin Definition of WLAN_EN

Pin Name	Pin No.	I/O	Description	Comments
WLAN_EN	68	DI	Wi-Fi enable control	VDD_IO power domain.

NOTE

WLAN_EN is a sensitive signal, and it should be ground shielded and routed as close as possible to AF31G.

4.1.2. Bluetooth Application Interface

The following figure shows the block diagram of Bluetooth application interface connection between AF31G and AG52x series modules:

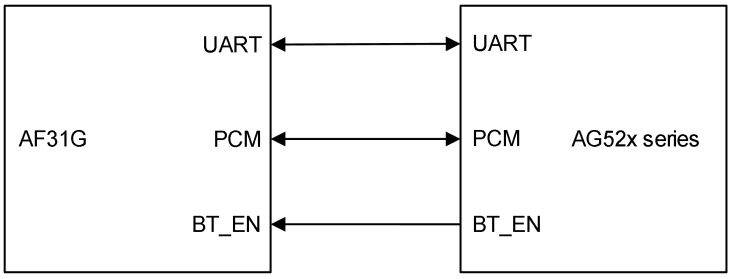


Figure 9: Block Diagram of Bluetooth Application Interface Connection

4.1.2.1. PCM Interface

AF31G provides PCM interface for Bluetooth voice application.

Table 10: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comments
PCM_DIN	2	DI	PCM data input	VDD_IO power domain.
PCM_SYNC	5	DI	PCM data frame sync	
PCM_CLK	4	DI	PCM clock	
PCM_DOUT	3	DO	PCM data output	

The following figure shows the PCM interface connection between AF31G and AG52x series modules.

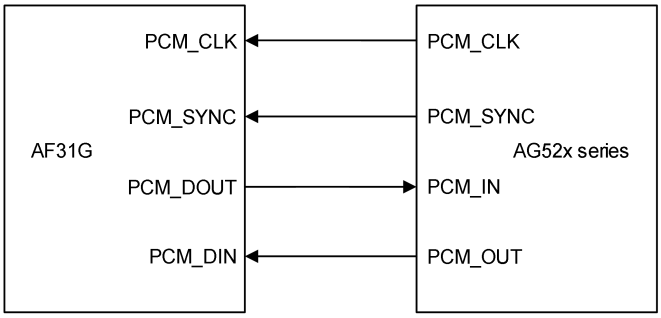


Figure 10: Block Diagram of PCM Interface Connection

4.1.2.2. BT_EN

BT_EN is used to control the Bluetooth function of AF31G. Bluetooth function will be enabled when BT_EN is at high level.

Table 11: Pin Definition of BT_EN

Pin Name	Pin No.	I/O	Description	Comments
BT_EN	69	DI	Bluetooth enable control	VDD_IO power domain. Active high.

4.1.2.3. BT_UART

Table 12: Pin Definition of BT_UART

Pin Name	Pin No.	I/O	Description	Comments
BT_TXD	74	DO	Bluetooth UART transmit	VDD_IO power domain.
BT_RXD	75	DI	Bluetooth UART receive	
BT_RTS	72	DO	Request To Send	
BT_CTS	73	DI	Clear To Send	

The following figure shows the reference design for BT_UART connection between AF31G and AG52x series modules.

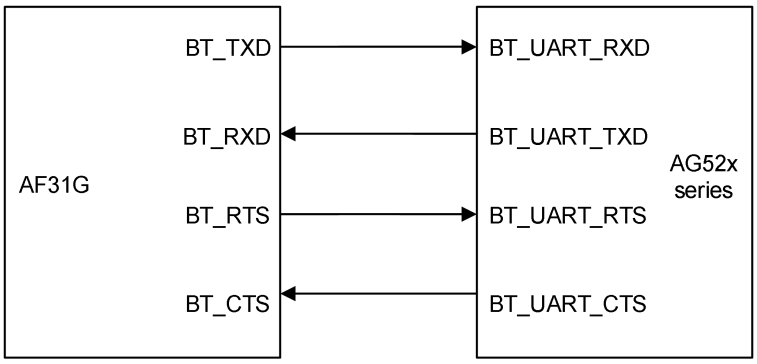


Figure 11: BT_UART Interface Connection

4.2. Coexistence UART

Table 13: Pin Definition of Coexistence UART

Pin Name	Pin No.	I/O	Description	Comments
COEX_TXD	76	DO	LTE/WLAN & Bluetooth coexistence transmit	VDD_IO power domain. If unused, keep this pin open.
COEX_RXD	1	DI	LTE/WLAN & Bluetooth coexistence receive	

The following figure shows the reference design for coexistence UART interface connection between AF31G and AG52x series modules.

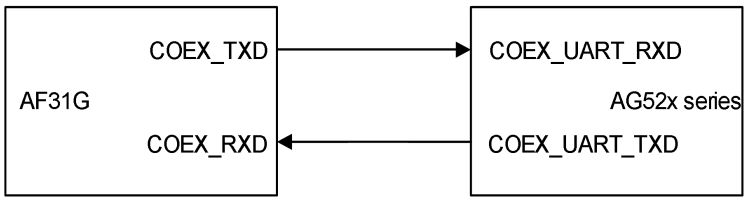


Figure 12: Coexistence UART Interface Connection

4.3. WLAN_SLP_CLK

The 32.768 kHz clock can be used in low power consumption mode, such as power saving mode and sleep mode, in which basic logic operations can be maintained.

Table 14: Pin Definition of WLAN_SLP_CLK

Pin Name	Pin No.	I/O	Description	Comments
WLAN_SLP_CLK	22	DI	External 32.768 kHz sleep clock input	VDD_IO power domain.

5 RF Specifications

5.1. RF Antenna

The characteristic impedance of the antenna ports should be controlled to 50 Ω.

5.1.1. Antenna Interface & Frequency Bands

Table 15: Pin Definition of RF Antenna Interface

Pin Name	Pin No.	I/O	Description	NOTE
ANT_WIFI0/BT	45	IO	2.4/5 GHz Wi-Fi antenna interface 0 and Bluetooth antenna interface	50 Ω characteristic impedance.
ANT_WIFI1	54	IO	2.4/5 GHz Wi-Fi antenna interface 1	

Table 16: Operating Frequency of AF31G (Unit: GHz)

Parameter	Frequency Bands
2.4 GHz Wi-Fi	2.400–2.4835
5 GHz Wi-Fi	5.150–5.850
Bluetooth	2.402–2.480

5.1.2. Reference Design

AF31G provides an RF antenna pin for Wi-Fi/Bluetooth antenna connection. The RF trace in host PCB connected to the module's RF antenna pin should be microstrip line or other types of RF trace, with characteristic impendence close to 50 Ω. This module comes with grounding pins which are next to the antenna pin in order to give a better grounding.

It is recommended to reserve a π-type and LCs matching circuit for better RF performance, and add a TVS for ESD protection. The π-type matching components (C3, C4, R1), the LCs (L1, C1, L2, C2) and

TVS (D1) should be placed as close to the antenna as possible. The capacitors and inductors are not mounted by default. The parasitic capacitance of TVS should be less than 0.05 pF.

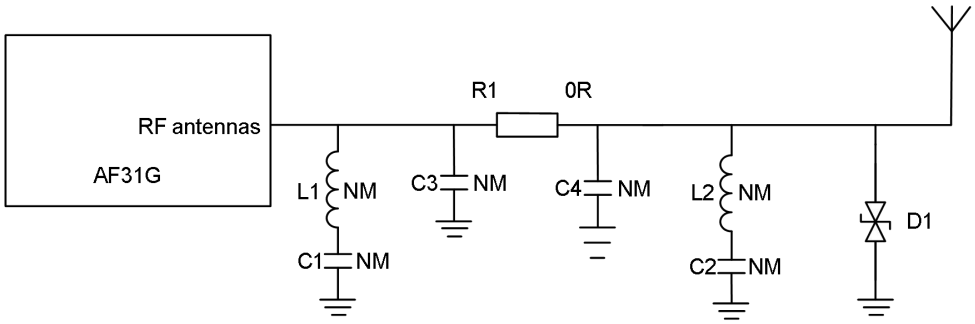


Figure 13: Reference Design for RF Antenna Interface

5.2. RF Performances

5.2.1. Conducted RF Performance of Wi-Fi

Table 17: Conducted RF Output Power at 2.4 GHz (Unit: dBm)

Standard	Data Rate	Typ.
802.11b	1 Mbps	TBD
802.11b	11 Mbps	TBD
802.11g	6 Mbps	TBD
802.11g	54 Mbps	TBD
802.11n, HT20	MCS 0	TBD
802.11n, HT20	MCS 7	TBD
802.11n, HT40	MCS 0	TBD
802.11n, HT40	MCS 7	TBD

Table 18: Conducted RF Output Power at 5 GHz (Unit: dBm)

Standard	Data Rate	Typ.
802.11a	6 Mbps	TBD
802.11a	54 Mbps	TBD
802.11n, HT20	MCS 0	TBD
802.11n, HT20	MCS 7	TBD
802.11n, HT40	MCS 0	TBD
802.11n, HT40	MCS 7	TBD
802.11ac, VHT20	MCS 0	TBD
802.11ac, VHT20	MCS 8	TBD
802.11ac, VHT40	MCS 0	TBD
802.11ac, VHT40	MCS 9	TBD
802.11ac, VHT80	MCS 0	TBD
802.11ac, VHT80	MCS 9	TBD

Table 19: Conducted RF Receiving Sensitivity at 2.4 GHz (Unit: dBm)

Standard	Data Rate	Typ.
802.11b	1 Mbps	TBD
802.11b	11 Mbps	TBD
802.11g	6 Mbps	TBD
802.11g	54 Mbps	TBD
802.11n, HT20	MCS 0	TBD
802.11n, HT20	MCS 7	TBD
802.11n, HT40	MCS 0	TBD
802.11n, HT40	MCS 7	TBD

Table 20: Conducted RF Receiving Sensitivity at 5 GHz (Unit: dBm)

Standard	Data Rate	Typ.
802.11a	6 Mbps	TBD
802.11a	54 Mbps	TBD
802.11n, HT20	MCS 0	TBD
802.11n, HT20	MCS 7	TBD
802.11n, HT40	MCS 0	TBD
802.11n, HT40	MCS 7	TBD
802.11ac, VHT20	MCS 0	TBD
802.11ac, VHT20	MCS 8	TBD
802.11ac, VHT40	MCS 0	TBD
802.11ac, VHT40	MCS 9	TBD
802.11ac, VHT80	MCS 0	TBD
802.11ac, VHT80	MCS 9	TBD

5.2.2. Conducted RF Performance of BLE

Table 21: Conducted RF Performance of BLE (Unit: dBm)

Frequency	Transmitting Power (Typ.)	Receiving Sensitivity (Typ.)
0	TBD	TBD
19	TBD	TBD
39	TBD	TBD

5.3. Reference Design of RF Routing

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

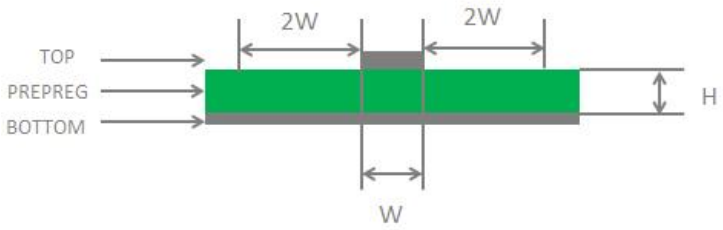


Figure 14: Microstrip Design on a 2-layer PCB

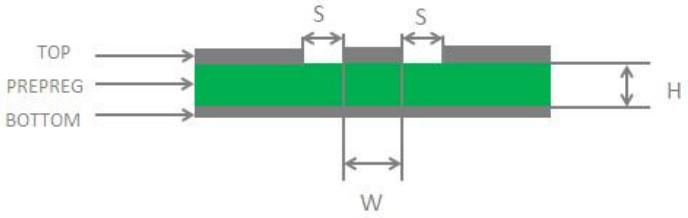


Figure 15: Coplanar Waveguide Design on a 2-layer PCB

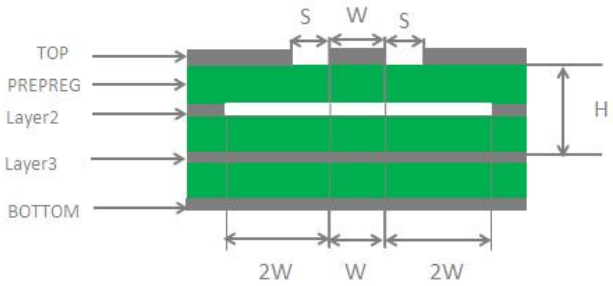


Figure 16: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

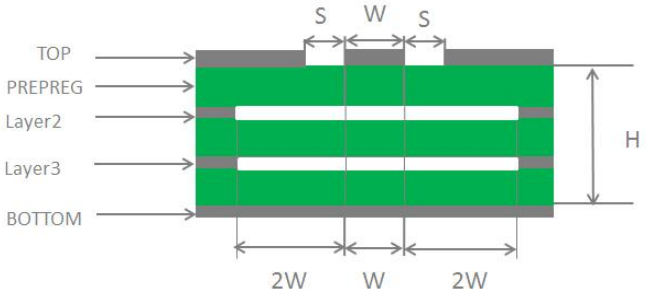


Figure 17: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- Design the GND pins adjacent to RF pins as thermal relief pads, and fully connect them to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- Reserve clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, please refer to ***document [2]***.

5.4. Antenna Requirements

Table 22: Antenna Requirements

Parameter	Requirements
Frequency range:	● 2.400–2.4835 GHz (Cable Insertion Loss: < 1 dB) ● 5.150–5.850 GHz (Cable insertion loss: <1 dB)
VSWR	< 2
Gain:	≥ 1 dBi
Max Input Power:	50 W
Input Impedance:	50 Ω

Polarization Type	Vertical

5.5. RF Connector Recommendation

If the RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connectors provided by Hirose.

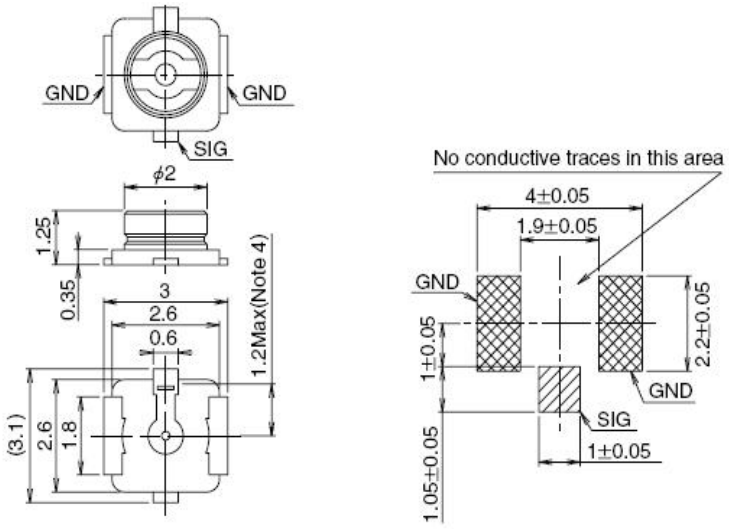


Figure 18: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series connectors listed in the following figure can be used to match the U.FL-R-SMT.

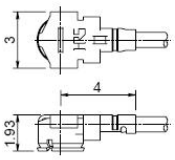
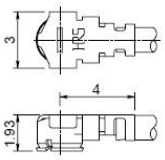
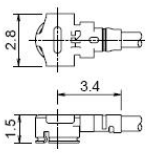
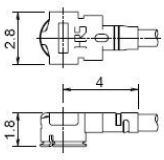
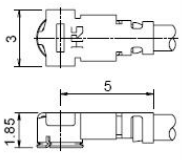
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 19: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of the mated connector.

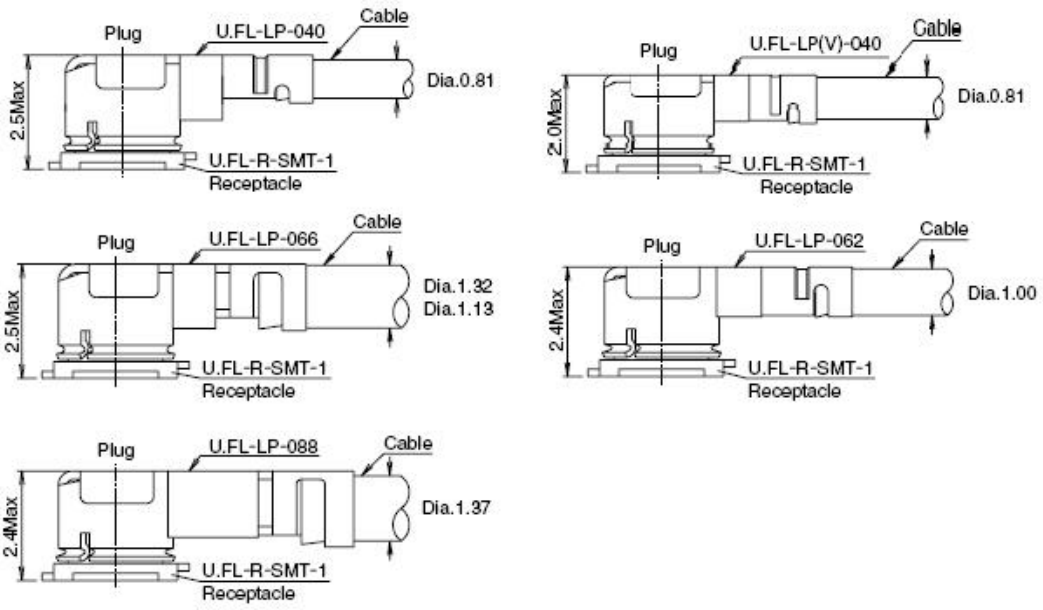


Figure 20: Space Factor of the Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics &

7 Reliability

7.1. Absolute Maximum Ratings

Table 23: Absolute Maximum Ratings (Unit: V)

Parameter	Min.	Max.
VDD_IO	-0.3	3.6
VDD_PA	-0.3	3.6
Digital I/O Input Voltage	-0.3	V_{DDIO} + 0.2

NOTE

V_{DDIO} is the supply voltage associated with the input pin to which the test voltage is applied.

The following table shows the recommended operating conditions of AF31G.

Table 24: Recommended Operating Conditions (Unit: V)

Parameter	Min.	Typ.	Max.
VDD_IO	1.71	1.8	1.89
VDD_PA	3.14	3.3	3.46

7.2. Digital I/O Characteristic

Table 25: General DC Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V_{IH}	High Level Input Voltage	0.7 × VDD_IO	VDD_IO + 0.2	V
V_{IL}	Low Level Input Voltage	-0.3	0.3 × VDD_IO	V
V_{OH}	High Level Output Voltage	0.9 × VDD_IO	VDD_IO	V
V_{OL}	Low Level Output Voltage	0	0.3 × VDD_IO	V
I_{iL}	Input Leakage Current	-5.0	5.0	μA
I_{oL}	Input Leakage Current		-11	mA

7.3. Power Consumption

7.3.1. Wi-Fi Power Consumption

Under the maximum transmit power, the Wi-Fi power consumption test results are as follows:

Table 26: Power Consumption of the Module (Normal Operation; Unit: mA)

Description	Conditions	$I_{VDD\_CORE\_VL}$	$I_{VDD\_CORE\_VM}$	$I_{VDD\_CORE\_VH}$	I_{VDD_IO}	$I_{VDD\_PA\_A}$	$I_{VDD\_PA\_B}$
802.11b	TX 1 Mbps @ TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD
	TX 11 Mbps @ TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD
802.11g	TX 6 Mbps @ TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD
	TX 54 Mbps @ TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD
802.11n (2.4 GHz)	TX HT20 MCS 0 @TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD
	TX HT20 MCS 7 @TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD
	TX HT40 MCS 0 @ TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD
	TX HT40 MCS 7 @ TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD
802.11a	TX 6 Mbps @ TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD

(5 GHz)	TX 54 Mbps @ TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD
802.11n (5 GHz)	TX HT20 MCS 0 @ TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD
	TX HT20 MCS 7 @ TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD
	TX HT40 MCS 0 @ TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD
	TX HT40 MCS 7 @ TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD
802.11ac (5 GHz)	TX VHT20 MCS 0 @ TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD
	TX VHT20 MCS 8 @ TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD
	TX VHT40 MCS 0 @ TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD
	TX VHT40 MCS 9 @ TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD
	TX VHT80 MCS 0 @ TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD
	TX VHT80 MCS 9 @ TBD dBm	TBD	TBD	TBD	TBD	TBD	TBD

7.3.2. BLE Power Consumption

BLE power consumption during non-signaling is here as follows:

Table 27: BLE Power Consumption During Non-signaling

Description	Power	Power Supply	Consumed Current
Non-signaling	TBD dBm	3.3 V	TBD
		1.8 V	TBD

NOTE

For more details about current consumption, please contact Quectel Technical Supports for the power consumption test report of the module.

7.4. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 28: Electrostatics Discharge Characteristics (25 °C, 45 % Relative Humidity; Unit: kV)

Tested Interfaces	Contact Discharge	Air Discharge
VDD	TBD	TBD
GND	TBD	TBD
Antenna Interfaces	TBD	TBD

7.5. Thermal Dissipation

The module offers the best performance when all internal IC chips are working within their operating temperatures. When the IC chip reaches or exceeds the maximum junction temperature, the module may still work but the performance and function (such as RF output power, data rate, etc.) will be affected to a certain extent. Therefore, the thermal design should be maximally optimized to ensure all internal IC chips always work within the recommended operating temperature range.

The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on your PCB, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Follow the principles below when the heatsink is necessary:
  - Do not place large size components in the area where the module is mounted on your PCB to reserve enough place for heatsink installation.
  - Attach the heatsink to the shielding cover of the module; In general, the base plate area of the heatsink should be larger than the module area to cover the module completely;
  - Choose the heatsink with adequate fins to dissipate heat;
  - Choose a TIM (Thermal Interface Material) with high thermal conductivity, good softness and good wettability and place it between the heatsink and the module;

- Fasten the heatsink with four screws to ensure that it is in close contact with the module to prevent the heatsink from falling off during the drop, vibration test, or transportation.

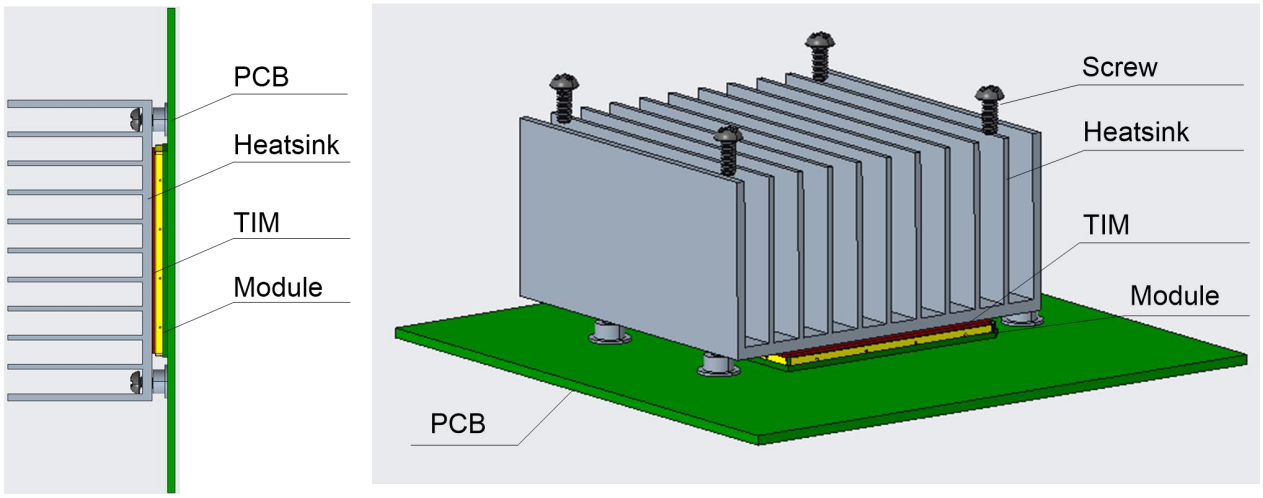


Figure 21: Placement and Fixing of the Heatsink

7.6. Operating and Storage Temperatures

Table 29: Operating and Storage Temperatures (Unit: °C)

Parameter	Min.	Typ.	Max.
Operating temperature range [2]	-40	+25	+85
Storage temperature range	-40		+95

[2] To meet normal operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this temperature range, the module's related indicators can meet IEEE and Bluetooth specifications.

8 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

8.1. Mechanical Dimensions

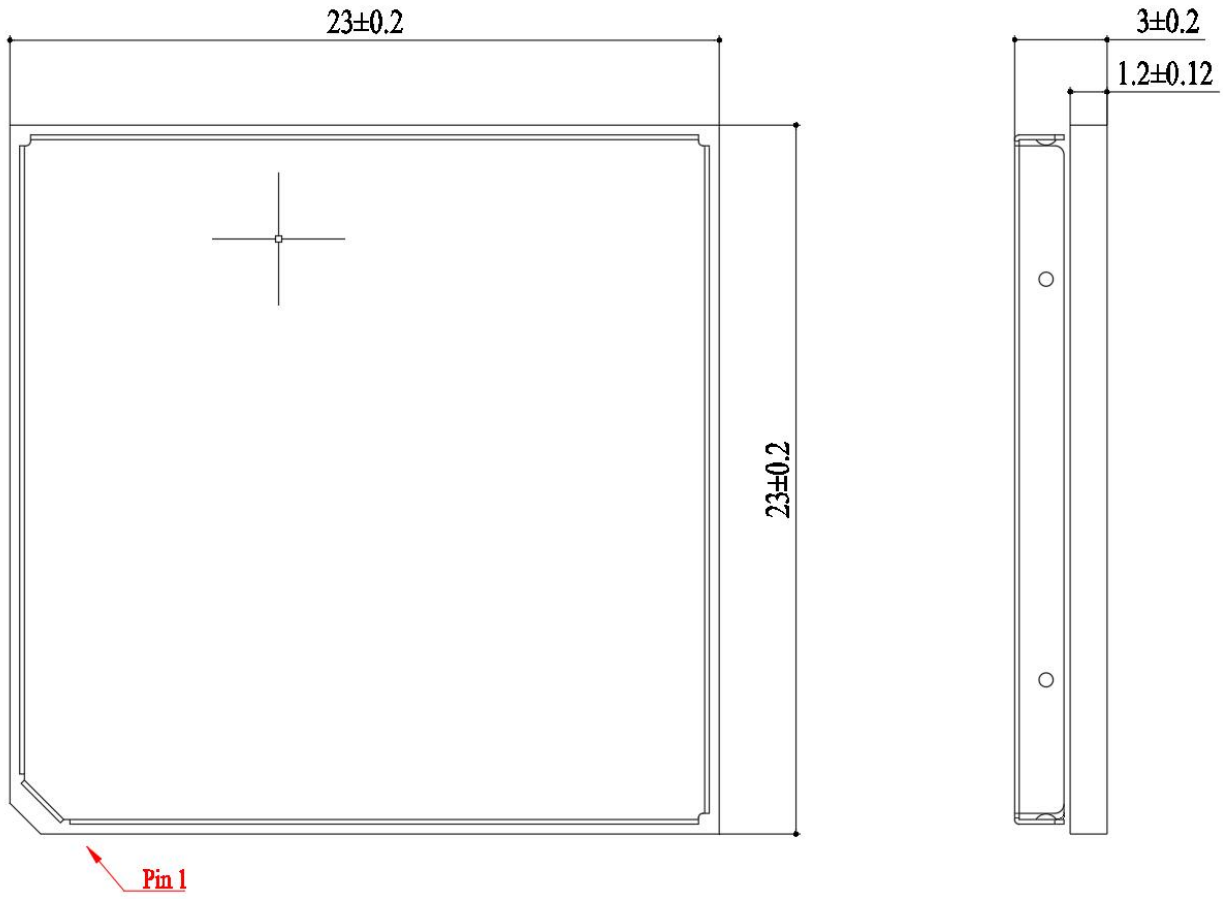


Figure 22: Module Top and Side Dimensions

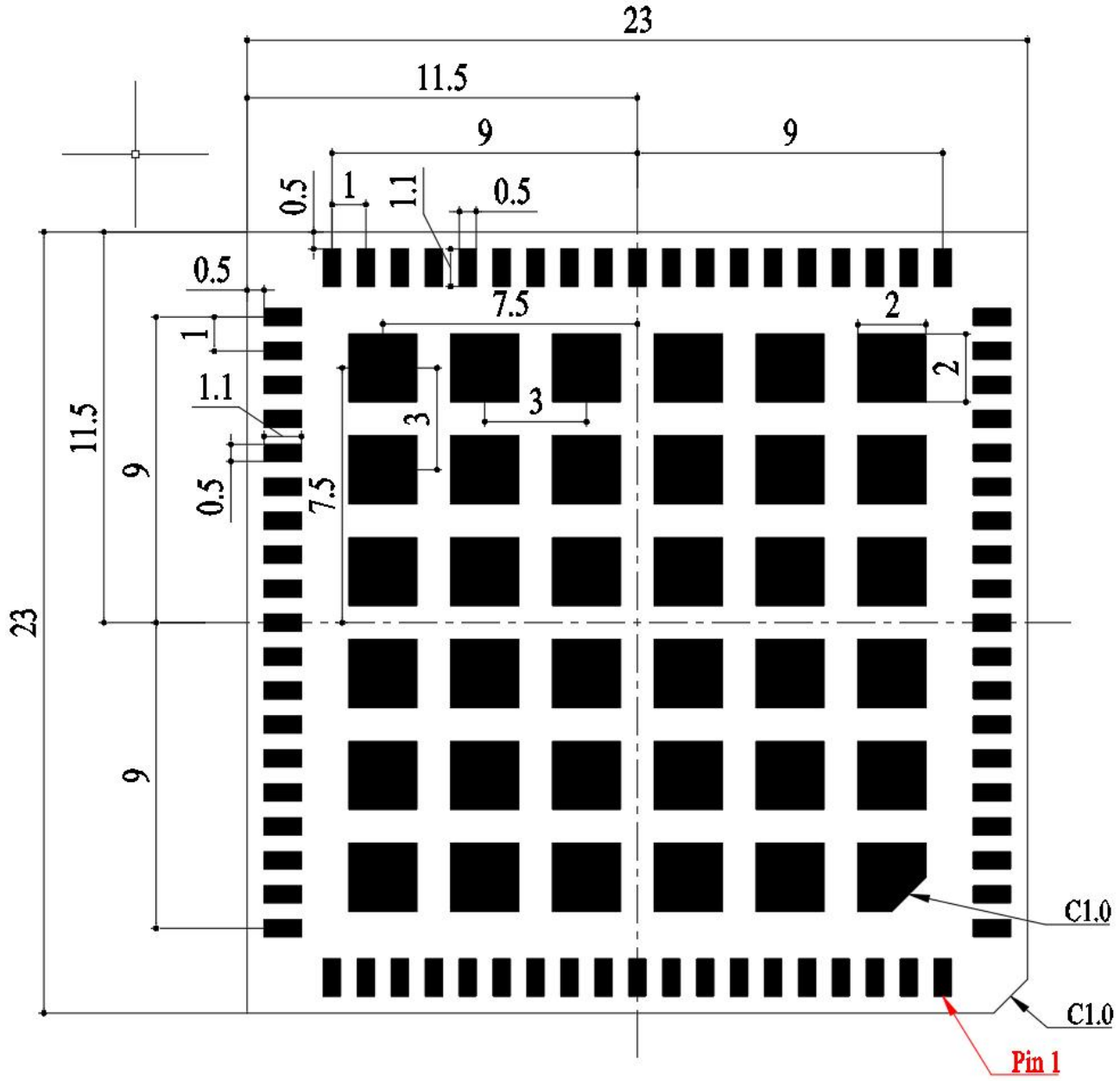


Figure 23: Module Bottom Dimension (Bottom View)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

8.2. Recommended Footprint

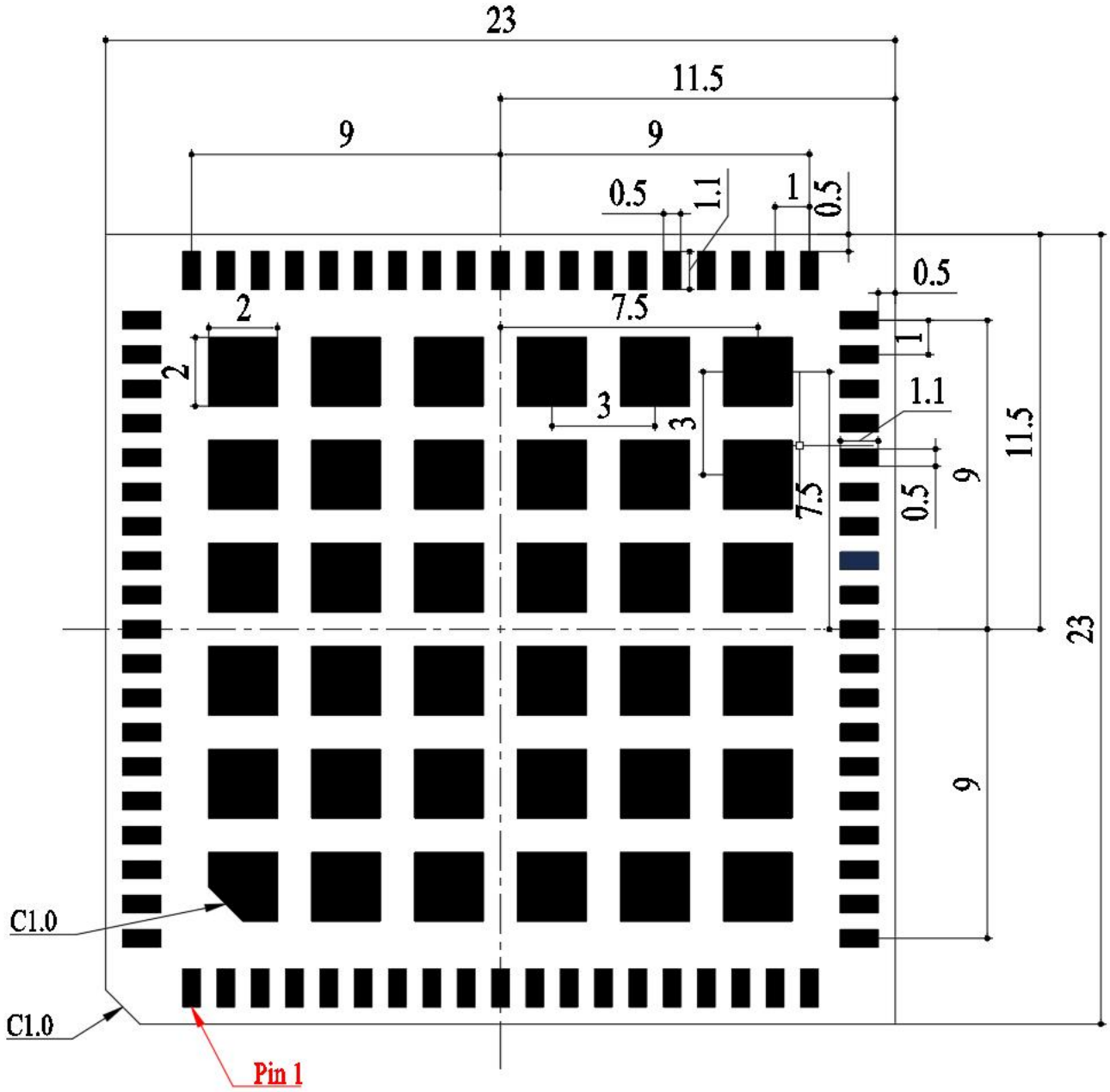


Figure 24: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

8.3. Top and Bottom Views

Figure 25: Top View of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

9 Storage, Manufacturing and Packaging

9.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [3] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[3] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

9.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be TBD mm. For more details, please refer to ***document [1]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

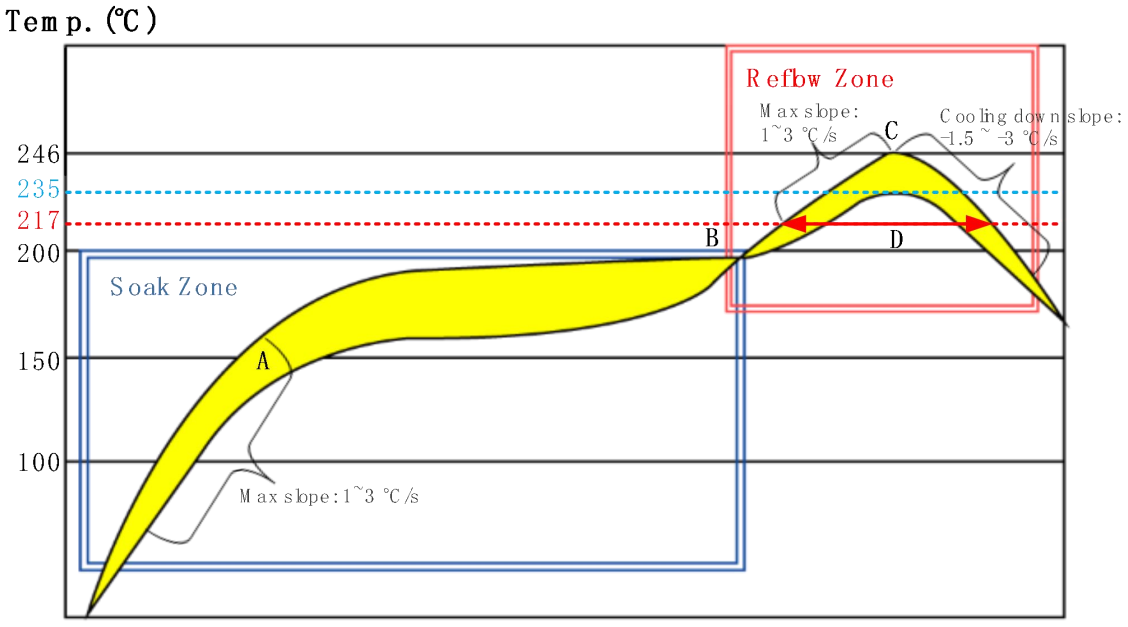


Figure 26: Recommended Reflow Soldering Thermal Profile

Table 30: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1 to 3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70 to 120 s
Reflow Zone	
Max slope	1 to 3 °C/s
Reflow time (D: over 217 °C)	40 to 70 s
Max temperature	235 to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
2. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
3. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [1][2]***.

9.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

9.3.1. Carrier Tape

Dimension details are as follow:

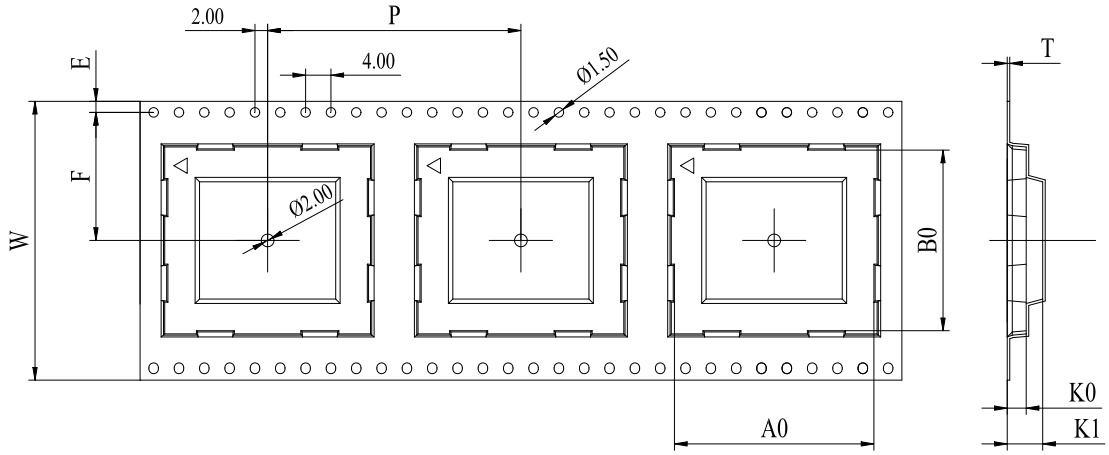


Figure 22: Carrier Tape Dimension Drawing

Table 31: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.4	23.5	23.5	3.5	6.8	20.2	1.75

9.3.2. Plastic Reel

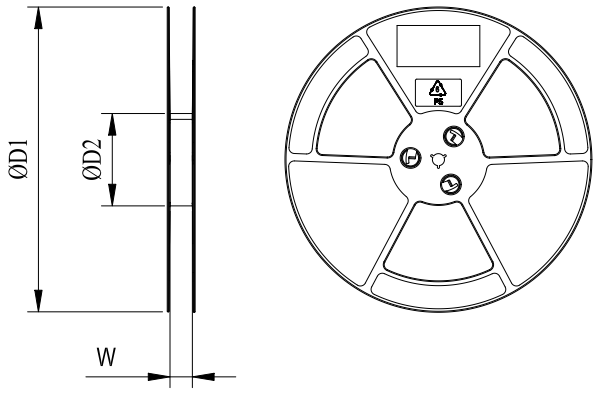
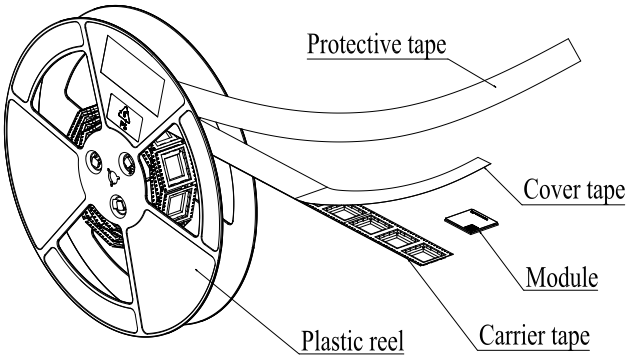


Figure 23: Plastic Reel Dimension Drawing

Table 32: Plastic Reel Dimension Table (Unit: mm)

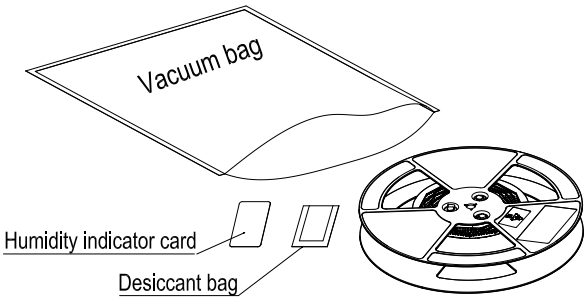
øD1	øD2	W
330	100	44.5

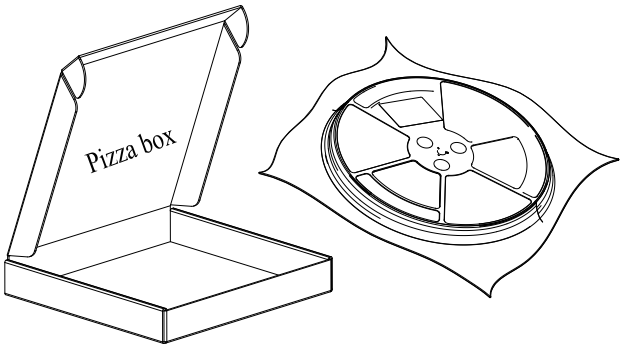
9.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 cartoon box and seal it. 1 cartoon box can pack 1000 modules.

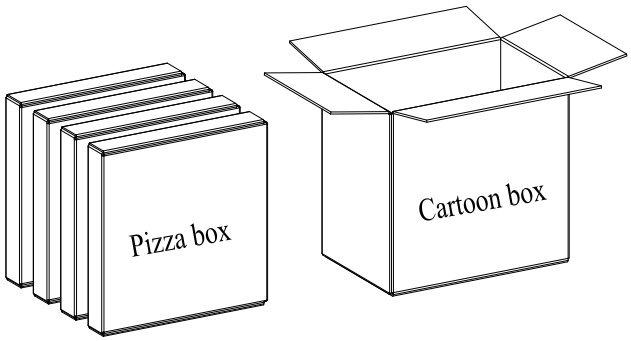


Figure 24: Packaging Process

10 Appendix References

Table 33: Related Documents

Document Name
[1] Quectel_Module_Secondary_SMT_Application_Note
[2] Quectel_RF_Layout_Application_Note

Table 34: Terms and Abbreviations

Abbreviation	Description
bps	Bytes per second
CDMA	Code Division Multiple Access
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear To Send
ESD	Electrostatic Discharge
GND	Ground
HSIC	High Speed Inter Chip
IEEE	Institute of Electrical and Electronics Engineers
LGA	Land Grid Array
LTE	Long Term Evolution
MCS	Modulation and Coding Scheme
PCB	Printed Circuit Board
PCM	Pulse Code Modulation

PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTS	Request To Send
SMS	Short Message Service
UART	Universal Asynchronous Receiver/Transmitter
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WLAN	Wireless Local Area Network

FCC Certification Requirements.

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.

And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based time- averaging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.

2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

3.A label with the following statements must be attached to the host end product: This device contains **FCC ID: XMR202302AF31G.**

4.To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

- ❒ Buletooth:≤3.67dBi
- ❒ Buletooth(LE):≤3.67dBi
- ❒ Wi-Fi 2.4G:≤4.35dBi
- ❒ Wi-Fi 5G:≤5.4dBi

5. This module must not transmit simultaneously with any other antenna or transmitter

6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

For this device, OEM integrators must be provided with labeling instructions of finished products. Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module:"Contains Transmitter Module FCC ID: **XMR202302AF31G.**" or "Contains FCC ID: **XMR202302AF31G.**" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party

responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user’s authority to operate the equipment.