

Jumpers and Headers Setting Guide

IMB-1245P-WV

IMB-1245M-WV

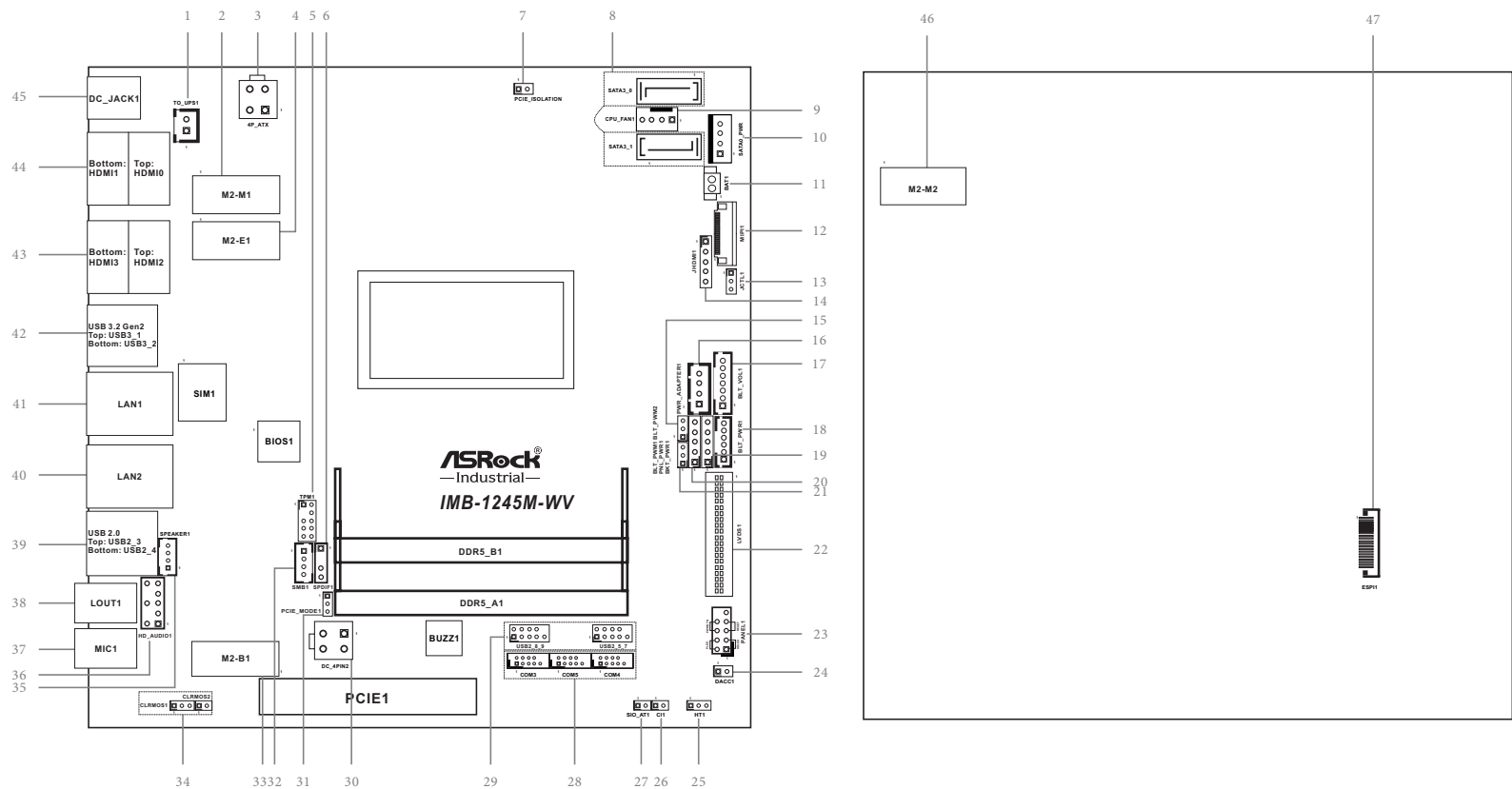
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Revision History

Date	Description
April 26, 2024	Sixth Release
May 29, 2024	Seventh Release
July 16, 2024	Eighth Release
November 12, 2024	Ninth Release
April 25, 2025	Tenth Release
May 6, 2025	Eleventh Release

For earlier revisions, please contact technical support.



1 : 2-pin UPS Module Power Input Connector (TO_UPS1)

Pin	Signal Name
1	GND
2	DC Input



2 : M.2 Key-M Socket (M2_M1)

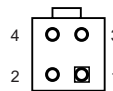
Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	GND	+3.3V	4
5	PERn3	NA	6
7	PERp3	NA	8
9	GND	SATA_LED	10
11	PETn3	+3.3V	12
13	PETp3	+3.3V	14
15	GND	+3.3V	16
17	PERn2	+3.3V	18
19	PERp2	NA	20
21	GND	NA	22
23	PETn2	NA	24
25	PETp2	NA	26
27	GND	NA	28
29	PERn1	NA	30
31	PERp1	NA	32
33	GND	NA	34
35	PETn1	NA	36
37	PETp1	NA	38
39	GND	NA	40
41	PERn0	NA	42
43	PERp0	NA	44
45	GND	NA	46
47	PETn0	NA	48
49	PETp0	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
67	NA	NA	68
69	PEDET	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	GND		

4 : M.2 Key-E Socket (M2_E1)

Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	USB D+	+3.3V	4
5	USB D-	NA	6
7	GND	NA	8
9	CNV_WGR_D1-	CNV_RF_RESET	10
11	CNV_WGR_D1+	NA	12
13	GND	MODEM_CLKREQ	14
15	CNV_WGR_D0-	NA	16
17	CNV_WGR_D0+	GND	18
19	GND	NA	20
21	CNV_WGR_CLK-	CNV_BRI_RSP	22
23	CNV_WGR_CLK+		
33	GND	CNV_BGI_DT	32
35	PETp	CNV_RGI_RSP	34
37	PETn	CNV_BRI_DT	36
39	GND	NA	38
41	PERp	NA	40
43	PERn	NA	42
45	GND	NA	44
47	PEFCLKp	NA	46
49	PEFCLKn	NA	48
51	GND	SUSCLK	50
53	CLKREQ#	PERST0#	52
55	NA	W_DISABLE1#	54
57	GND	W_DISABLE2#	56
59	CNV_WT_D1-	NA	58
61	CNV_WT_D1+	NA	60
63	GND	NA	62
65	CNV_WT_D0-	NA	64
67	CNV_WT_D0+	NA	66
69	GND	NA	68
71	CNV_WT_CLK-	NA	70
73	CNV_WT_CLK+	+3.3V	72
75	GND	+3.3V	74

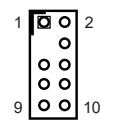
3 : 4-pin ATX PWR Connector (4P_ATX)

Pin	Signal Name
1	GND
2	GND
3	DC Input
4	DC Input



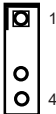
5 : TPM Header (TPM1)

Pin	Signal Name	Signal Name	Pin
1	TPM PWR	RST#	2
3		CS#	4
5	IRA	MOSI	6
7	MISO	GND	8
9	CLK	GND	10



6 : SPDIF Header (SPDIF1)

Pin	Signal Name
1	+5V
2	
3	SPDIF OUT
4	GND



7 : PCIE_ISOLATION1

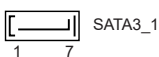
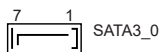
Pin	Signal Name
1	PSON#
2	GND



* Connect to PCIE_ISOLATION_1 header on VGA-PWR card.

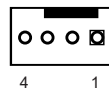
8 : SATA3 Connectors (SATA3_0, SATA3_1)

Pin	Signal Name
1	GND
2	SATA-A+
3	SATA-A-
4	GND
5	SATA-B+
6	SATA-B-
7	GND



9 : CPU FAN Connector (+12V) (CPU_FAN1)

Pin	Signal Name
1	GND
2	+12V
3	CPU_FAN_SPEED
4	FAN_SPEED_CONTROL



10 : SATA Power Output Connector (SATA0_PWR1)

Pin	Signal Name
1	+5V
2	GND
3	GND
4	+12V



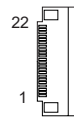
11 : Battery Connector (BAT1)

Pin	Signal Name
1	BAT+
2	GND



12 : MIPI Connector (MIPI1)

Pin	Signal Name
1	+3V
2	I2C0_SDA
3	I2C0_SCL
4	GND
5	N/A
6	N/A
7	GND
8	CSI_E_D3_DP
9	CSI_E_D3_DN
10	GND
11	CSI_E_D2_DP
12	CSI_E_D2_DN
13	GND
14	CSI_E_CK_DP
15	CSI_E_CK_DN
16	GND
17	CSI_E_D1_DP
18	CSI_E_D1_DN
19	GND
20	CSI_E_D0_DP
21	CSI_E_D0_DN
22	GND



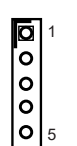
13 : JCTL1 (Default 1-2)

Pin	Signal Name
1	REMOTE_CTL_ATX
2	REMOTE_CTL
3	REMOTE_CTL_SP
1&2	ATX_PWR
2&3	Special_PWR



14 : JHDMI1

Pin	Signal Name
1	+5V
2	GND
3	GPP_V23
4	GPP_V22
5	GPP_C8



* Only used by ASRockInd design card HDMI-MIPI.

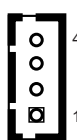
15 : CON_LBKLT_CTL Voltage Level (BLT_PWM2)

1-2 : 3V Level (Default)
2-3 : 5V Level



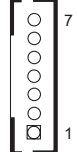
16 : Power Adapter (PWR_ADAPTER1)

Pin	Signal Name
1	GND
2	5VA_CONTROL
3	5VA
4	GND



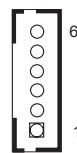
17 : Backlight Volume Control (BLT_VOL1)

Pin	Signal Name
1	GPIO_VOL_UP
2	GPIO_VOL_DW
3	PWRDN
4	BLT_UP
5	BLT_DW
6	GND
7	GND



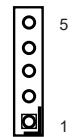
18 : Inverter Power Control Wafer (BLT_PWR1)

Pin	Signal Name
1	GND
2	GND
3	CON_LBKLT_CTL
4	CON_LBKLT_EN
5	LCD_BLT_VCC
6	LCD_BLT_VCC



19 : Backlight Power Select (LCD_BLT_VCC) (BKT_PWR1)

1-2: LCD_BLT_VCC: +5V (Default)
2-3: LCD_BLT_VCC: +12V
4-5: LCD_BLT_VCC: DC_IN



20 : Panel Power Select (LCD_VCC) (PNL_PWR1)

1-2: LCD_VCC : +3V (Default)
2-3: LCD_VCC : +5V
4-5: LCD_VCC : +12V



21 : Brightness Control Mode (BLT_PWM1)

1-2 : From eDP PWM to CON_LBKLT_CTL
2-3 : From LVDS PWM to CON_LBKLT_CTL (Default)

* Please set to 1-2 when adjusting brightness by Brightness Control bar under OS.

* Please set to 2-3 when adjusting brightness by BLT_VOL1.



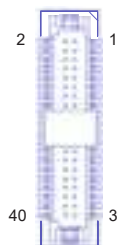
22* : LVDS Panel Connector (LVDS1)

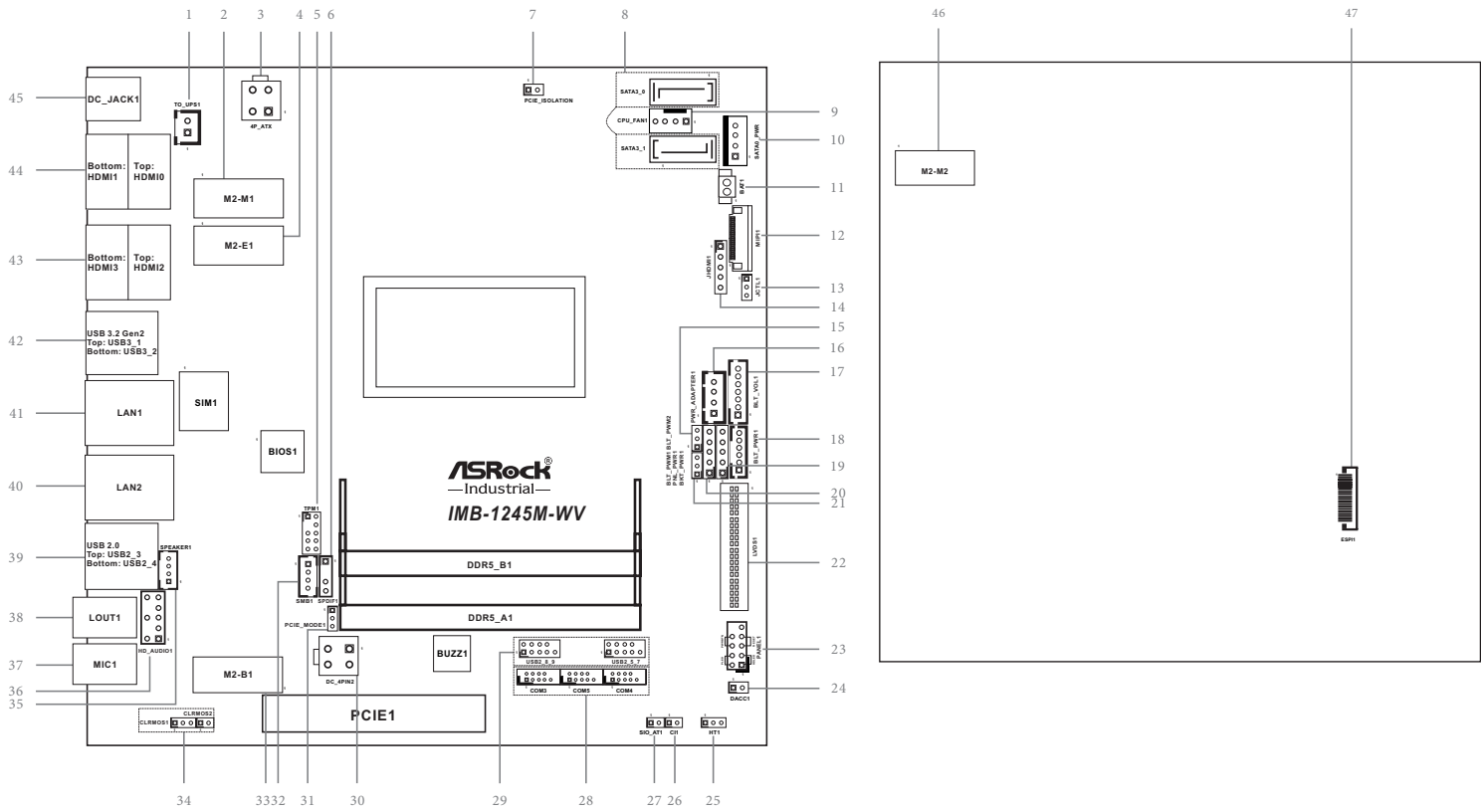
Pin	Signal Name	Signal Name	Pin
1	LCD_VCC	LCD_VCC	2
3	+3.3V	N/A	4
5	N/A	LVDS_A_DATA0#	6
7	LVDS_A_DATA0	PD (Panel Detection)	8
9	LVDS_A_DATA1#	LVDS_A_DATA1	10
11	GND	LVDS_A_DATA2#	12
13	LVDS_A_DATA2	GND	14
15	LVDS_A_DATA3#	LVDS_A_DATA3	16
17	GND	LVDS_A_CLK#	18
19	LVDS_A_CLK	GND	20
21	LVDS_B_DATA0#	LVDS_B_DATA0	22
23	GND	LVDS_B_DATA1#	24
25	LVDS_B_DATA1	GND	26
27	LVDS_B_DATA2#	LVDS_B_DATA2	28
29	DPLVDD_EN	LVDS_B_DATA3#	30
31	LVDS_B_DATA3	GND	32
33	LVDS_B_CLK#	LVDS_B_CLK	34
35	GND	CON_LBKLT_EN	36
37	CON_LBKLT_CTL	LCD_BLT_VCC	38
39	LCD_BLT_VCC	LCD_BLT_VCC	40

*eDP by pass mode (switch by BIOS)

Pin	Signal Name	Signal Name	Pin
1	LCD_VCC	LCD_VCC	2
3	+3V	N/A	4
5	N/A	N/A	6
7	eDP_HP	GND	8
9	eDP_TX1-	eDP_TX1+	10
11	GND	eDP_TX0-	12
13	eDP_TX0+	GND	14
15	N/A	N/A	16
17	GND	eDP_AUX-	18
19	eDP_AUX+	GND	20
21	N/A	N/A	22
23	GND	N/A	24
25	N/A	GND	26
27	N/A	N/A	28
29	LVDD_EN	N/A	30
31	N/A	GND	32
33	N/A	N/A	34
35	GND	CON_LBKLT_EN	36
37	CON_LBKLT_CTL	+LCD_BLT_VCC	38
39	+LCD_BLT_VCC	+LCD_BLT_VCC	40

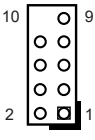
* PD (Panel Detection):
Connect this pin to LVDS Panel's Ground pin to detect Panel detection.





23 : System Panel Header (PANEL1)

Pin	Signal Name	Signal Name	Pin
1	HDLED+	PLED+	2
3	HDLED-	PLED-	4
5	GND	PWRBTN#	6
7	RESET#	GND	8
9	GND		10



24 : DACC1

Open: no ACC
Short: ACC (Default)

* Auto clear CMOS when system boot improperly.



25 : Heater header (HT1)

Pin	Signal Name
1	Heater_PWR (5V/1A)
2	GND
3	NTC (Negative Temperature Coefficient) thermistors



* The 10k Ohm NTC thermistors is suggested.

* Deep mode is not supported when the preheat function is enabled.

26 : Chassis Intrusion Header (CI1)

CI1
Open : Normal (Default)
Short : Active Case Open



27 : ATX/AT Mode Jumper (SIO_AT1)

Open: ATX Mode (Default)
Short: AT Mode



28 : COM Port Headers (COM3~5)
(RS232/422/485) *



* This motherboard supports RS232/422/485 on COM3, 4 and 5 ports. Please refer to the table below for the pin definition. In addition, COM3, 4 and 5 ports (RS232/422/485) can be adjusted in BIOS setup utility > Advanced Screen > Super IO Configuration. You may refer to our user manual for details.

COM3, 4 and 5 Ports Pin Definition

Pin	RS232	RS422	RS485
1	DCD	TX-	RTX-
2	RXD	TX+	RTX+
3	TXD	RX+	N/A
4	DTR	RX-	N/A
5	GND	GND	GND
6	DSR	N/A	N/A
7	RTS	N/A	N/A
8	CTS	N/A	N/A
9	PWR	PWR	PWR

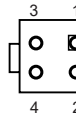
29 : USB 2.0 Headers (USB2_5_7, USB2_8_9)

Pin	Signal Name	Signal Name	Pin
1	USB_PWR	USB_PWR	2
3	P-	P-	4
5	P+	P+	6
7	GND	GND	8
9	DUMMY		10



30 : 4-pin ATX PWR Connector (DC_4PIN2)

Pin	Signal Name
1	GND
2	GND
3	PCIE_EXT +12V
4	PCIE_EXT +12V



* Only use with VGA-PWR card

31 : PCIE_PWR_MODE (PCIE_MODE1)

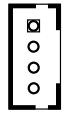
1-2: LOW_PWR_MODE (Default)
2-3: HIGH_PWR_MODE

* Only set to HIGH_PWR_Mode (pin 2-3) when using VGA-PWR CARD..



32 : SMB1

Pin	Signal Name
1	GPP_D03
2	SMB_CLK_MAIIN
3	SMB_DATA_MAIN
4	GND



33 : M.2 Key-B Socket (M2_B1)

Pin	Signal Name	Signal Name	Pin
1	NA	+3.3V	2
3	GND	+3.3V	4
5	GND	FULL_Card_Power off	6
7	USB_D+	DISABLE1_N	8
9	USB_D-	N/A	10
11	GND		
		NA	20
21	GND	NA	22
23	NA	NA	24
25	NA	DISABLE2_N	26
27	GND	NA	28
29	USB3_RX_N	UIM_RESET	30
31	USB3_RX_P	UIM_CLK	32
33	GND	UIM_DATA	34
35	USB3_TX_N	UIM_PWR	36
37	USB3_TX_P	NA	38
39	GND	NA	40
41	PERn0	NA	42
43	PERp0	NA	44
45	GND	NA	46
47	PETn0	NA	48
49	PETp0	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
59	NA	NA	60
61	NA	NA	62
63	NA	NA	64
65	NA	SIM_DETECT	66
67	NA	NA	68
69	PEDET	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	NA		

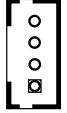
34 : Clear CMOS Headers

CLRMOS1
1-2 : Normal (Default)
2-3 : Clear CMOS
CLRMOS2
Open : Normal (Default)
Short : Auto Clear CMOS
When AC Power On



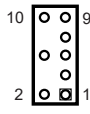
35 : 3W Audio AMP Output Wafer (SPEAKER1)

Pin	Signal Name
1	OUTLN
2	OUTLP
3	OUTRP
4	OUTRN

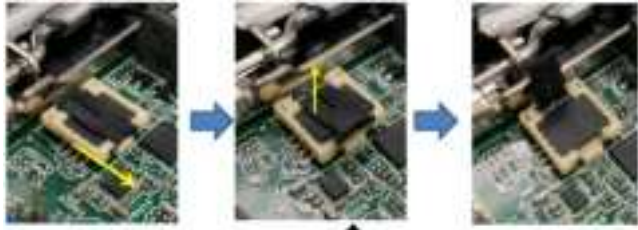


36 : Front Panel Audio Header (HD_AUDIO1)

Pin	Signal Name	Signal Name	Pin
1	MIC2_L	GND	2
3	MIC2_R		4
5	OUT2_R	MIC_RET	6
7	J_SENSE		8
9	OUT2_L	OUT_RET	10



Installation of ROM Socket



- Do not apply force to the actuator cover after ic is inserted.
- Do not apply force to actuator cover when it is opening over 120 degree, Otherwise, the actuator cover may be broken.



- The yellow dot (Pin1) on the ROM must be installed at pin1 position of the socket (white arrow area).
 - Make sure the white dot on the ROM is installed outwards of the socket.
 - For further details of how to install ROM, please refer to ASRI website.
- Warning: If the installation does not follow as the picture, then it may cause severe damage to chipset & MB.**

37 : Mic In (MIC1)

38 : Line Out (LOUT1)

39 : USB 2.0 Ports (USB2_3_4)

40 : RJ45 LAN Port (LAN2)

41 : RJ45 LAN Port (LAN1)

42 : USB 3.2 Gen2 Ports (USB3_1_2)

43 : HDMI Ports (HDMI2_3)

44 : HDMI Ports (HDMI0_1)

45 : DC_JACK1

Back Side :

46 : ESPI Header (ESPI1)

Pin	Signal Name
1	GND
2	ESPI_CLK
3	GND
4	ESPI_CS0#
5	ESPI_RESET#
6	GND
7	+3V
8	ESPI_CS1#
9	SMBus_CLK
10	SMBus_DATA
11	ESPI_IO0
12	ESPI_IO1
13	ESPI_IO2
14	ESPI_IO3
15	ESPI_ALERT1#
16	+3VSB
17	Internal Use
18	+5VSB
19	ESPI_ALERT0#
20	GND



47 : M.2 Key-M Socket (M2_M2)

Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	GND	+3.3V	4
5	PERn3	NA	6
7	PERp3	NA	8
9	GND	SATA_LED	10
11	PETn3	+3.3V	12
13	PETp3	+3.3V	14
15	GND	+3.3V	16
17	PERn2	+3.3V	18
19	PERp2	NA	20
21	GND	NA	22
23	PETn2	NA	24
25	PETp2	NA	26
27	GND	NA	28
29	PERn1	NA	30
31	PERp1	NA	32
33	GND	NA	34
35	PETn1	NA	36
37	PETp1	NA	38
39	GND	NA	40
41	PERn0	NA	42
43	PERp0	NA	44
45	GND	NA	46
47	PETn0	NA	48
49	PETp0	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
		NA	68
69	PEDET	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	GND		