Jetson Thor Series Modules

Design Guide

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Document History

DG-12084-001_v1.2

Version	Date	Description of Change
1.0	June 18, 2025	Initial release
1.1	July 3, 2025	Updated the following: > Removed DMIC5 > Figure 5-2, Figure 5-8 > Note under Figure 5-3 and Figure 5-5 > Section 5.1.1 > Added section 5.1.3
1.2	July 31, 2025	Updated the following: > Figure 5-1, Figure 5-3, Figure 5-5, Figure 15-1 > Table 5-1, Table 5-4, Table 9-6, Table 15-1 (and note), Table 15-2 > Sections 5.1.1, 5.1.3

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Chapter 1. Introduction

This design guide contains recommendations and guidelines for engineers to follow and create a product that is optimized to achieve the best performance from the interfaces supported by the NVIDIA® Jetson™ Thor series module, hereafter referred to as “Thor Module.”

This design guide provides detailed information on the capabilities of the hardware module, which may differ from supported configurations by provided software. Refer to the software release documentation for information on supported capabilities.

1.1 References

Refer to the following documents or models listed for more information. Always use the latest revision of all documents.

- *Jetson T5000 Modules Data Sheet (DS-11945-001)*
- *Jetson Thor Developer Kit Carrier Board Specification (SP-12334-001)*
- *Jetson Thor Series Pinmux Configuration Template*
- *Jetson Thor Series Modules Thermal Design Guide (TDG-12271-001)*
- *Jetson Thor Developer Kit Carrier Board Reference Design Files*
- *Jetson Thor Series Supported Component List (DA-12429-001)*

1.2 Attachments

The following files are attached to this design guide.

- Jetson_Thor_Series_Pin_Descriptions_v1.0.nvxlsx
- Jetson_Thor_Series_Schematic_Checklist_v1.1.nvxlsx
- Jetson_Thor_Series_Layout_Checklist_v1.0.nvxlsx
- Jetson_Thor_Series_Bringup_Checklist_v1.1.nvxlsx

To access the attached files, click the **Attachment** icon on the toolbar on this PDF (using Adobe Acrobat Reader or Adobe Acrobat). Select the file and use the Tool Bar options (**Open, Save**) to retrieve the documents.

Note that Excel files with the .nvxlsx extension will need to be saved as .xlsx.

1.3 Abbreviations and Definitions

Table 1-1 lists abbreviations that may be used throughout this design guide and their definitions.

Table 1-1. Abbreviations and Definitions

Abbreviation	Definition
CEC	Consumer Electronic Control
CAN	Controller Area Network
DP	VESA® DisplayPort® (output)
GPIO	General Purpose Input Output
HDI	High-Density Interconnect
HDMI™	High-Definition Multimedia Interface
I2C	Inter IC
I2S	Inter IC Sound Interface
LDO	Low Dropout (voltage regulator)
LPDDR5X	Low Power Double Data Rate DRAM, Fifth generation, extended
MGBE	Multi-Gigabit Ethernet
MTS	Multi-Stream Transport
NVMe	Non-Volatile Memory Express
PCIe (PEX)	Peripheral Component Interconnect Express Interface
PDM	Pulse-Density Modulation
PHY	Physical Layer
PMIC	Power Management Integrated Circuit
RTC	Real Time Clock
SC7	System Core State 7 (Sleep)

Abbreviation	Definition
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus

Table 1-2. Industry Standards

Interface	Specification
CAN	Version 2.0/ISO11898
DP	Version 1.4a
ETHER_QOS	RGMII Version 2.0
HDMI	Version 2.1
I2C	NXP 3.0
MGBE	IEEE 802.3-2015
MIPI CSI	C-PHY Revision 2.0 / D-PHY 2.1
PCI Express	PCI Express Base Specification Revision 5.0, Version 1.0
USB	Universal Serial Bus Specification Revision 2.0, 3.2; Gen1 and Gen2
XFI	SFF INF-8077i, Revision 4.5, 2005

Note: All occurrences of USB 3.2 refer to "USB 3.2 Gen 1x1: SuperSpeed USB 5 Gbps" and "USB 3.2 Gen 2x1: SuperSpeed USB 10 Gbps" only. Also note that Gen 1x1 and Gen 2x1 are referred to simply as Gen1 and Gen2 in this design guide.

Chapter 2. Introduction

The NVIDIA Jetson Thor series modules reside at the center of the embedded system solution and Jetson Thor SoC:

- Power (Power Sequencer, Regulators)
- DRAM (LPDDR5X)
- QSPI NOR
- Power Monitors
- Thermal Sensor

Table 2-1. Jetson Thor Features

Category	Function	Category	Function
USB	USB 2.0 USB 3.2 Gen2x1 (10 Gbps)	Display	HDMI / DP (4x– see note). DP supports multi-head operation through Multi-Stream Transport (MST).
PCIe	Root Port and Endpoint supported up to Gen5	SPI	Initiator and Target
Camera	CSI (6x2 or 4x4) D-PHY and C-PHY	Fan	PWM and TACH
LAN	5 Gigabit Ethernet: PCIe MGBE Ethernet: XFI	Debug	JTAG and UART
Audio	I2S, Digital Mic	System	Power control, Reset, Alerts
Miscellaneous	CAN, I2C, UART	Power	Main Inputs (HV, MV, and SV)

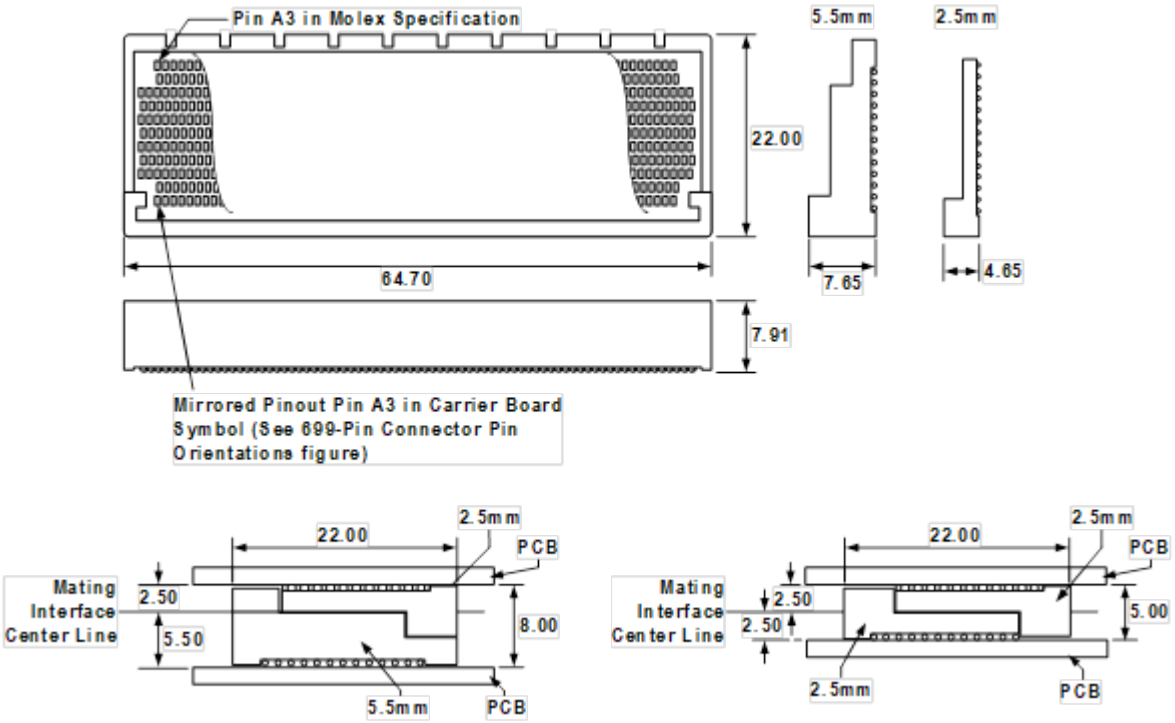
Note: HDMI and DP share the same pins. See Chapter 9 for display details.

Chapter 3. Main Connector Details

The main 699-pin connector on the Jetson Thor is from the Molex Mirror Mezz family. See the *Jetson Thor Series Supported Components List (DA-12429-001)* for compatible module connectors to use on the carrier board. Refer to the Molex Mirror Mezz connector specification for details.

Refer to the *Jetson_Thor_Series_Pin_Descriptions* in the attachment for the 699-pin map.

Figure 3-1. 699-pin Connector Dimensions



Note: Various documents related to the Molex Mirror Mezz connector can be found at: Mirror Mezz Connectors - Molex

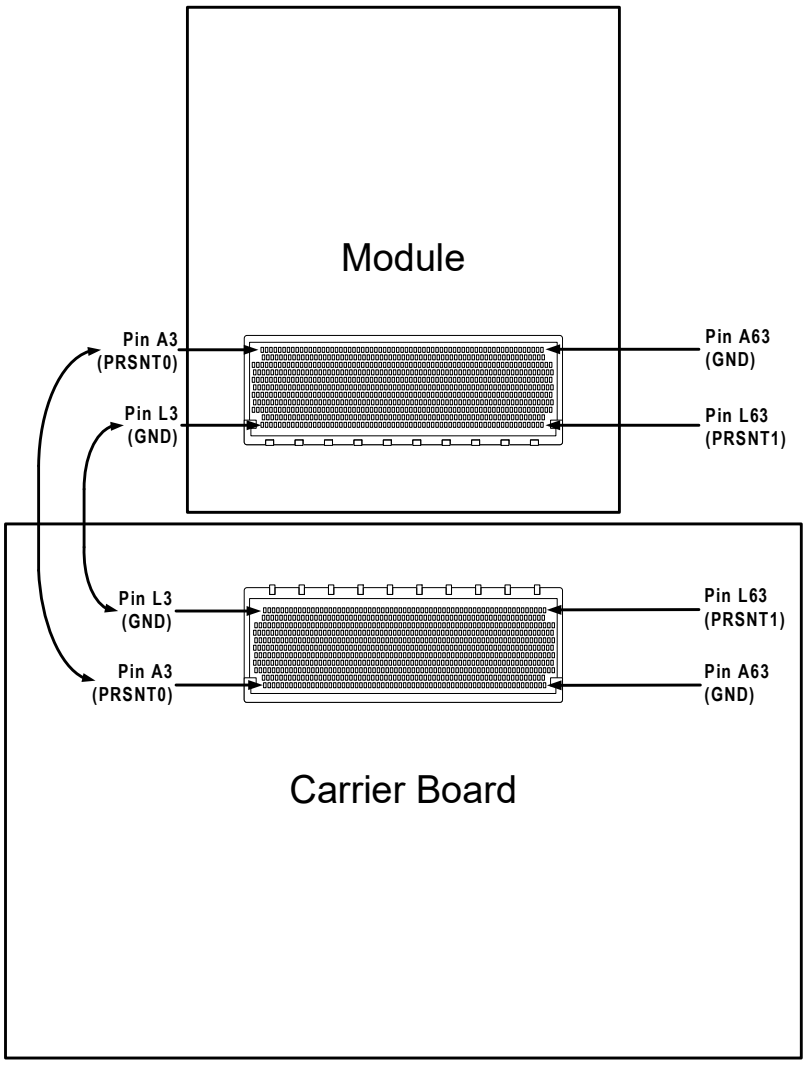
The *Molex Application Guide* for Mirror Mezz™, which includes details for connector mounting can be found at: https://www.molex.com/pdm_docs/as/2028280001-AS-000.pdf

3.1 Connector Pin Orientations

The symbol pinout for the 699-pin connector on the carrier board is mirrored such that the pin numbers match when the module and carrier board connectors are mated (see Figure 3-2). The orientation shown matches the carrier board in the upright position as well as the layout file.

ⓘ	Caution**:** Note that the 699-pin connector pinout on the carrier board is a mirror image of the Molex pinout. Designers should verify the pinout of their designs against the Jetson Thor reference layout.

Figure 3-2. 699-pin Connector Pin Orientation



3.2 Module to Carrier Board Standoff

The spacing between the module PCB and the carrier board PCB are shown in Figure 3-3 and Figure 3-4 to illustrate the following two cases:

- 5.5 mm connector on the carrier board (8 mm nominal spacing).
- 2.5 mm connector (5 mm nominal spacing).

The standoffs to support the module are located between the carrier board and the bottom plate.

Figure 3-3. 5.5 mm Height on Carrier Board

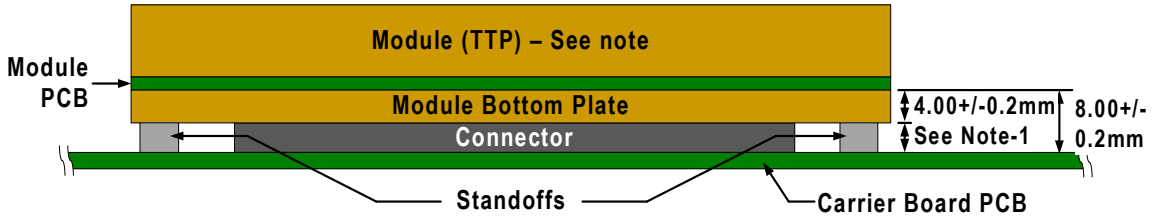
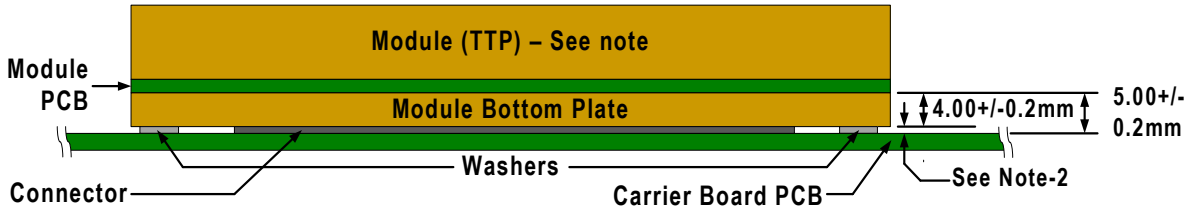


Figure 3-4. 2.5 mm Height on Carrier Board



Notes:

1. See Section 3.3 for standoff heights recommendations.
2. If the 2.5 mm height connector is used, there can be no components under the module on the carrier board due to the extremely limited clearance.

3.3 Module to Carrier Board Standoff Height Recommendations

Standoffs and spacers are required between the module bottom plate and the carrier board. The height should be chosen to meet the connector board-to-board spacing requirements and accommodate the tolerances in the bottom plate and the standoff itself. If the standoff is too short, the carrier board PCB may warp as the mounting screws are tightened. If too tall, the connectors will not mate fully. The two cases (5.5 mm and 2.5 mm connector on the carrier board) are described in this section and are accompanied by tables that show the possible permutations of tolerances of the bottom plate and spacers. The platform designer can determine if a different height would be more appropriate but should consider both the PCB warpage (standoff height too short) and connector contact overlap length to find the best balance.

The following examples are based on Molex parts using spacer heights and spacer tolerances to produce a workable solution.

5.5 mm height – 8.00+/-0.15 mm board to board spacing case

For this case, a standoff height of 4.2 mm is used. This is based on a standoff with ±0.13 mm height tolerance. The tolerance for the bottom plate is ±0.1 mm and ±0.1 mm for the solder balls between the bottom plate and the module PCB. The following table shows example calculations using the connector board spacing, module bottom plate height, and example standoff height with tolerances mentioned.

Table 3-1. Standoff Height Calculations for 5.5 mm Height Connector Case

Board to Board Spacing (mm)	Bottom Plate Height (mm)	Board to Bottom Plate Gap (mm)	Standoff Height (mm)	Space Beyond Ideal Mating Spec. (mm)
8	3.8	4.2	4.07	-0.13
8	3.8	4.2	4.33	0.13
8	4.2	3.8	4.07	0.27
8	4.2	3.8	4.33	0.53
Margin to -0.15 mm Conn. Spec.				0.02
Nominal connector sweep range				1.5
Worst case remaining sweep/contact (mm)				0.97

Notes:

1. Positive values mean no PCB warpage but less sweep. Negative values can result in PCB warpage.
2. The mating connector height tolerance comes from the Molex connector specification.
3. The connector contact sweep range can be found on the Molex website in the Mirror Mezz area.
4. The module bottom plate height/tolerance can be found in the Jetson Thor Data Sheet.

2.5 mm height – 5.00+/-0.15 mm board to board spacing case

For this case, a standoff height of 1.2 mm is used. This is based on a standoff with ±0.13 mm height tolerance. The tolerance for the bottom plate is ±0.1 mm and ±0.1 mm for the solder balls between the bottom plate and the module PCB. The following table shows example calculations using the connector board spacing, module bottom plate height, and example standoff height with tolerances mentioned.

Table 3-2. Standoff Height Calculations for 2.5 mm Height Connector Case

Board to Board Spacing (mm)	Bottom Plate Height (mm)	Board to Bottom Plate Gap (mm)	Standoff Height (mm)	Space Beyond Ideal Mating Spec. (mm)
5	3.8	1.2	1.07	-0.13
5	3.8	1.2	1.33	0.13
5	4.2	0.8	1.07	0.27
5	4.2	0.8	1.33	0.53
Margin to -0.15mm Conn. Spec.				0.02
Nominal connector sweep range				1.5
Worst case remaining sweep/contact (mm)				0.97

Notes:

1. Positive values mean no PCB warpage but less sweep. Negative values can result in PCB warpage.
2. See additional notes in the “Notes” section of Table 3-1.

3.4 Module Installation and Removal

To install the Jetson Thor correctly, follow the sequence and mounting hardware instructions below:

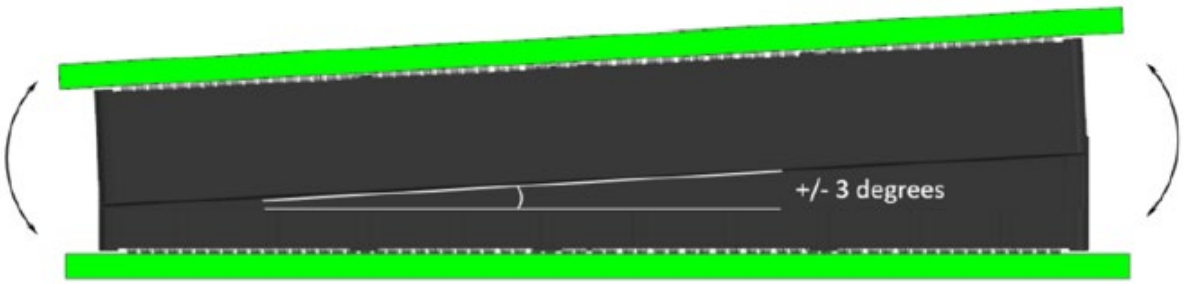
1. Connectors should be parallel with respect to each other during mating.
2. Use a smooth motion during mating (no mechanical shock, knocking, hammering).
3. The top and bottom PCB are to be bolted to enhance reliability.
4. Secure with M3 screws (4x) from the top of the module. Torque the screws to 4.5 in-lbf.

If a fixture is used to do the mating, then that fixture should hold the mating connectors parallel to within ± 2 degrees. Also, the fixture should allow the connectors to become parallel as the mating process progresses.

To remove the Jetson Thor correctly, follow the sequence and mounting hardware instructions below:

1. The PCB design needs to have enough finger reachability and space required to hold the board for un-mating.
2. Remove mounting screws (4x) from the top of the module.
3. Rock the top board a few times, no more than ± 3 degrees, to gradually disengage the connectors.

Figure 3-5. Module Removal



Chapter 4. Reference Design Considerations

The Jetson Thor Developer Kit Carrier Board Reference design files are provided as a reference design. This chapter provides the necessary details for designers to replicate certain features if desired. In addition, aspects of the design that are specific to the NVIDIA developer kit usage, but not useful or supported on a custom carrier board, are identified.

Most of the features implemented on the Jetson Thor Developer Kit can be duplicated by copying the connections from the Jetson Thor Carrier Board Reference Design Files. These listed features have aspects that would require additional information.

- **Button Power MCU:** The developer kit carrier board implements a button power MCU (EFM8SB10F2G – U79). This device is programmed with firmware that is available on the Jetson Download Center. The posting is titled *NVIDIA Jetson Carrier Board Power Button Supervisor Firmware*. The connections used on the reference design must be followed exactly and the firmware provided must be used to ensure correct functionality.
- **USB Type-C® (USB-C®) PD Controller:** Designs that intend to follow the NVIDIA carrier board design and include the USB-C PD Controller (CYPD8225 – U237) must replicate the circuitry on the latest carrier board exactly. The firmware binary is used to program the Cypress CYPD8225 controller and is available on the Jetson Download Center. The posting is titled *Cypress Firmware Binary for USB Type-C PD controller (CYPD8225)*. The customer should get the flashing instructions from Cypress. No support or source code is provided for this firmware. If modifications or source code is required, contact Cypress directly for support. This firmware binary is released under the L4T firmware EULA.
- **Power Monitoring:** There is a power monitoring IC (INA238 – U280) that monitors the input power to trigger throttling when the power consumption exceeds the power supply capacity.

The following list is the Jetson Thor Developer Kit carrier board features that should not be copied as they are not required or useful for a custom carrier board design. They will not be supported by NVIDIA.

- **The ID EEPROM (AT24C02D – U501)** is a feature that is used for NVIDIA internal purposes, but not useful on a custom design. A similar function may be desired for a custom design, but the NVIDIA software will not interact with these devices and the I2C address used by the developer kit carrier board ID EEPROM on the I2C1 interface (7'h56) should be avoided.
- **Debug MCU (ATSAMD21G16B-AU – U136), circuit, and associated USB connector (J90):** These features are used at NVIDIA for internal debugging and development purposes. These are not required, and support will not be provided if implemented. Designers have the option to implement something similar on their custom carrier boards but should develop their own circuit to meet their needs.

Chapter 5. Power

This chapter describes the power specifications for the Jetson Thor.

> **Caution:** The Jetson Thor module is not hot-pluggable. Before installing or removing the module, the main power supplies (SYS_VIN_SV , SYS_VIN_HV and SYS_VIN_MV) must be disconnected and the power rails allowed to discharge to <0.6V.

Table 5-1. Power and System Pin Descriptions

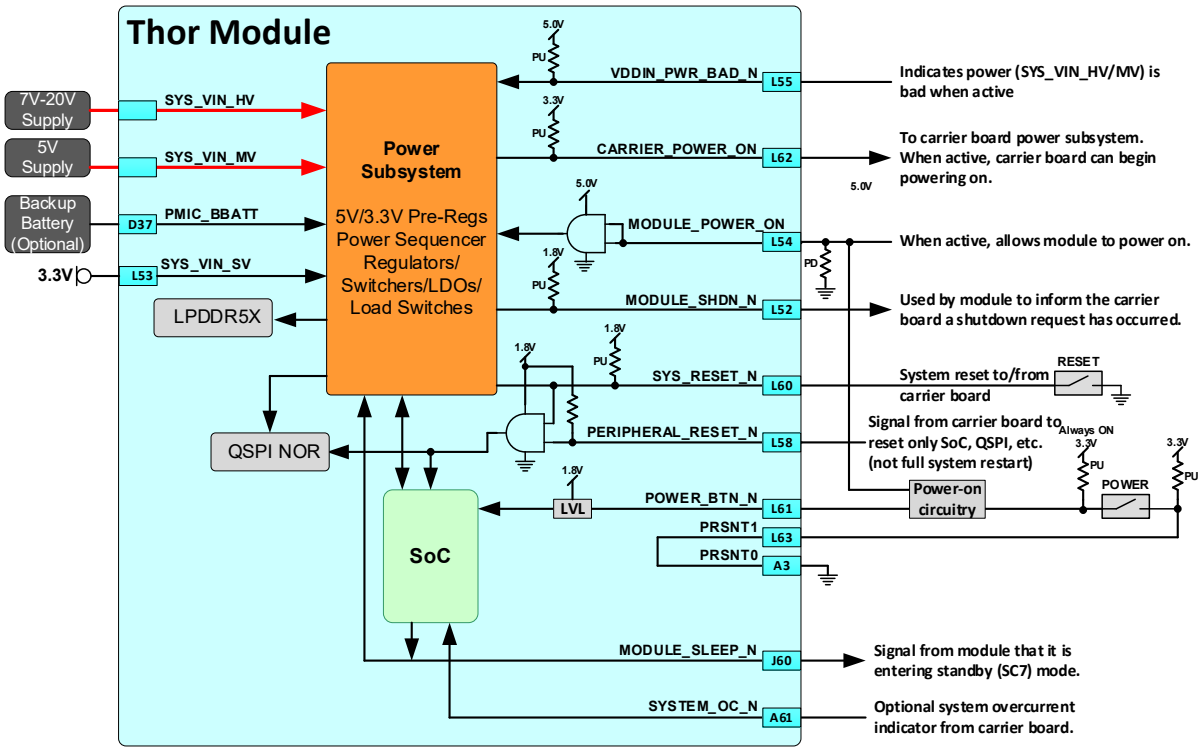
Pin #	Module Pin Name	Usage/Description	Direction	Pin Type
See note below	SYS_VIN_HV	**System Voltage Input – High**	Input	Power: 7V to 20V
	SYS_VIN_MV	**System Voltage Input – Medium**	Input	Power: 5.0V
L53	SYS_VIN_SV	**Safety Logics Voltage Input**: Must be tied to 3.3V. See power sequencing for timing.	Input	Power: 3.3V
D37	PMIC_BBATT	**Real-Time Clock**: Optionally used to provide back-up power for RTC in the Power Sequencer. Connects to Lithium Cell or similar power source, which provides power to RTC when the system is disconnected from power. Rechargeable cells or super capacitors are not supported.	Input	Power: 1.85V to 5.5V
L60	SYS_RESET_N	**System Reset:** Asserted by power sequencer in the module during power-on. Can be asserted by the carrier board to reset the SoC, Boot devices, etc., but not the power sequencer. A 10kΩ pull-up to 1.8V is on the module.	Bidir	Open Drain, 1.8V
L55	VDDIN_PWR_BAD_N	**VDD_IN Power Bad**: Carrier board asserts low when SYS_VIN_HV and SYS_VIN_MV are not valid. Carrier board should stop asserting this signal and allow the signal to be pulled high by the internal pull-up on the module when SYS_VIN_HV and SYS_VIN_MV are stable and have reached required voltage levels. This prevents the SoC from powering up until the main input supply voltages are stable. A 10kΩ pull-up to 5V is on the module.	Input	Open-drain, 5.0V

Pin #	Module Pin Name	Usage/Description	Direction	Pin Type
L54	MODULE_ POWER_ON	**Module Power On**: Signal asserted to the module to start power-on sequence. This signal should be driven low by the carrier board initially and then driven high when the module is to be powered on.	Input	CMOS, 5.0V
L62	CARRIER_ POWER_ON	**Carrier Power On**: Asserted by the module when module power up sequence is complete. This signal high indicates that it is safe for the carrier board to power up. A 10kΩ pull-up to 3.3V is on module.	Output	Open-drain, 3.3V
L61	POWER_BTN_N	**Power Button**: Can be configured by software to be used to power system off or enter and exit sleep mode (SC7). Level shifter between module pin (3.3V) and SoC pin (1.8V) on module.	Bidir	Open-drain, 3.3V
L58	PERIPHERAL_ RESET_N	**Peripheral Reset**: Driven from carrier board and AND'd with SYS_RESET_N to drive the Thor SF_SYS_RST_N pin. When PERIPHERAL_RESET_N is asserted, the SoC and QSPI are reset (not Power Sequencer). A 10kΩ pull-up to 1.8V is on the module.	Input	CMOS – 1.8V
L10	FORCE_ RECOVERY_N	**Force Recovery strap pin**: Held low when SYS_RESET_N goes inactive (power-on or reset button press) to enter force recovery mode.	Input	CMOS – 1.8V
J60	MODULE_SLEEP_N	**Sleep Acknowledge**: Indicates module is in sleep mode (SC7 state).	Output	CMOS – 1.8V
L56	THERM_ALERT_N	**Thermal Alert**: Thermal alert assertion. System needs to actively cool down the module once the signal is asserted low.	Output	Open-drain, 3.3V
A61	SYSTEM_OC_N	**System Over-current Thermal warning**: Optionally, the signal can be asserted by external events (e.g., low battery) to trigger hardware clock throttling.	Input	CMOS, 1.8V
L52	MODULE_SHDN_N	**Module Shutdown indicator**: Used to inform carrier board that a shutdown request has occurred on-module (thermal shutdown). A 10kΩ pull-up to 1.8V is on the module.	Output	CMOS – 1.8V
A3	PRSNT0	**Present 0**: Tied with PRSNT1 on module. Used to detect when the module is connected to the carrier board. Can be used to keep the carrier board from powering the module until the module is installed fully in the carrier board. Tied to GND on the carrier board if implemented to match reference design.	N/A	N/A
L63	PRSNT1	**Present 1**: Tied to one side of the power button on the carrier board. Refer to the Jetson Thor Carrier Board Reference Design files for the detailed connection.		
K40	MID0	**Module ID** #0	Not connected	N/A

Pin #	Module Pin Name	Usage/Description	Direction	Pin Type
H40	MID1	**Module ID** #1	Tied to GND	N/A

Note: Refer to the Jetson_Thor_Series_Pin_Descriptions in the attachment.

Figure 5-1. Power Block Diagram



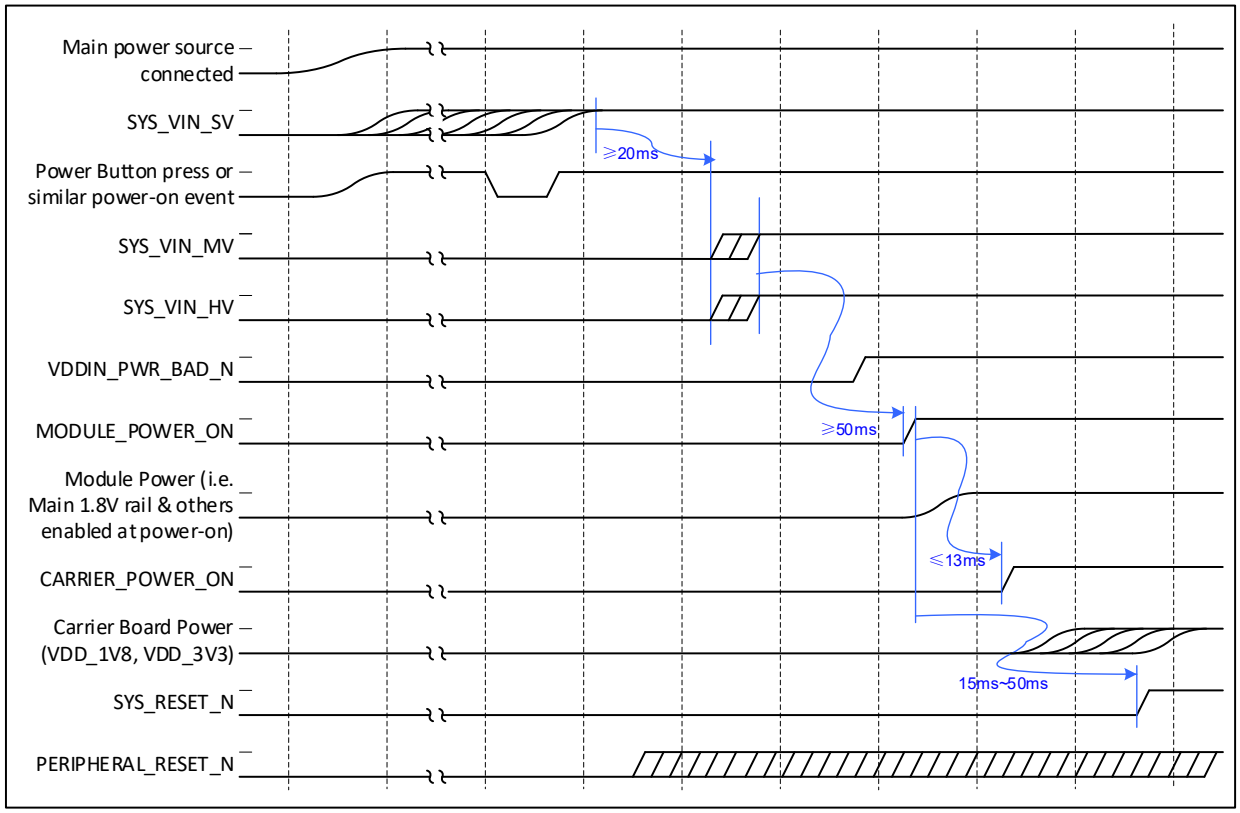
5.1 Power Sequencing

5.1.1 Power-On Sequence

The basic power-ON sequencing requirements is as follows:

- The main power source for the system is applied. The **SYS_VIN_SV, SYS_VIN_HV,** and **SYS_VIN_MV** are derived from this power source. **SYS_VIN_SV** must be powered up first or it may have remained powered from the previous power cycle. Optionally, **SYS_VIN_SV, SYS_VIN_HV,** and **SYS_VIN_MV** supplies can be gated and only enabled to the module when a signal (such as **VIN_PWR_ON**) is enabled. This can help avoid damage if the module is inserted when main power is on.
- **VDDIN_PWR_BAD_N** will stay active (low) until **SYS_VIN_HV** is valid (and not gated).
- **MODULE_POWER_ON** can be set active (high) once **VDDIN_PWR_BAD_N** is inactive (high).
- As the module powers on, one of the last supplies is the 3.3V supply. **CARRIER_POWER_ON** is pulled up to the powergood pin of the 3.3V supply on the module. Once this signal is active (high), the carrier board supplies associated with the module (1.8V, 3.3V) can power on.
- **SYS_RESET_N** is driven by the power sequencer on the module during power-on. It does not need to be controlled by the carrier board. If the carrier board supplies required for powering on require additional time, the **PERIPHERAL_RESET_N** signal can be held low. This will keep the SoC and other boot devices in reset.

Figure 5-2. Power-On Sequence (Power Button Case)



Notes:

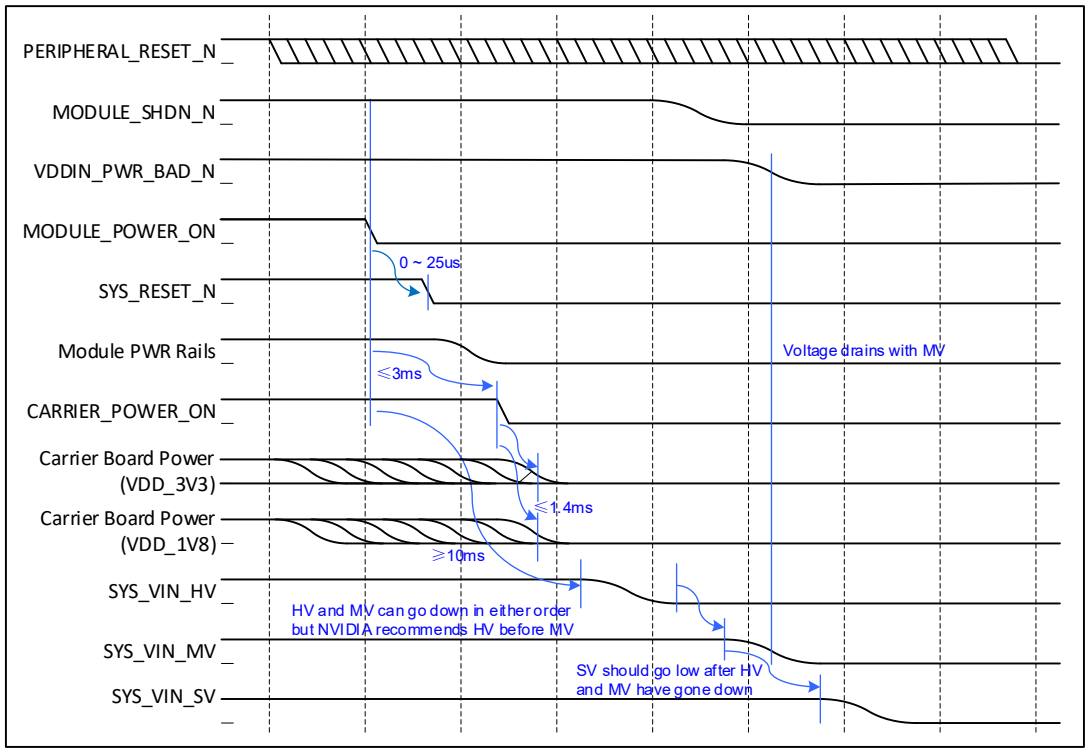
1. PERIPHERAL_RESET_N is optionally kept High during the power-up sequence. If Carrier Board Power is not up yet by the time SYS_RESET_N is de-asserted, PERIPHERAL_RESET_N must be held Low until the carrier board is ready to bring Thor out of RESET.
2. MODULE_POWER_ON must be driven low by the carrier board initially before driving it high to power on the module during the power-on sequence.

5.1.2 Power Down Sequence by Power Button Press

1. MODULE_SHDN_N and VDDIN_PWR_BAD_N do not play a role in this power down sequence; they drain with the MV rail going down at the end.
2. User presses a button that causes MODULE_POWER_ON to go low.

   If a button MCU is being used, the user holds the Power Button for X-amount of time (see the 5.3.2 Power Button Supervisor MCU section).
3. The power sequencer on the module starts the power down sequence from the moment MODULE_POWER_ON goes low.

Figure 5-3. Power Down Sequence – Button Press Shutdown Case



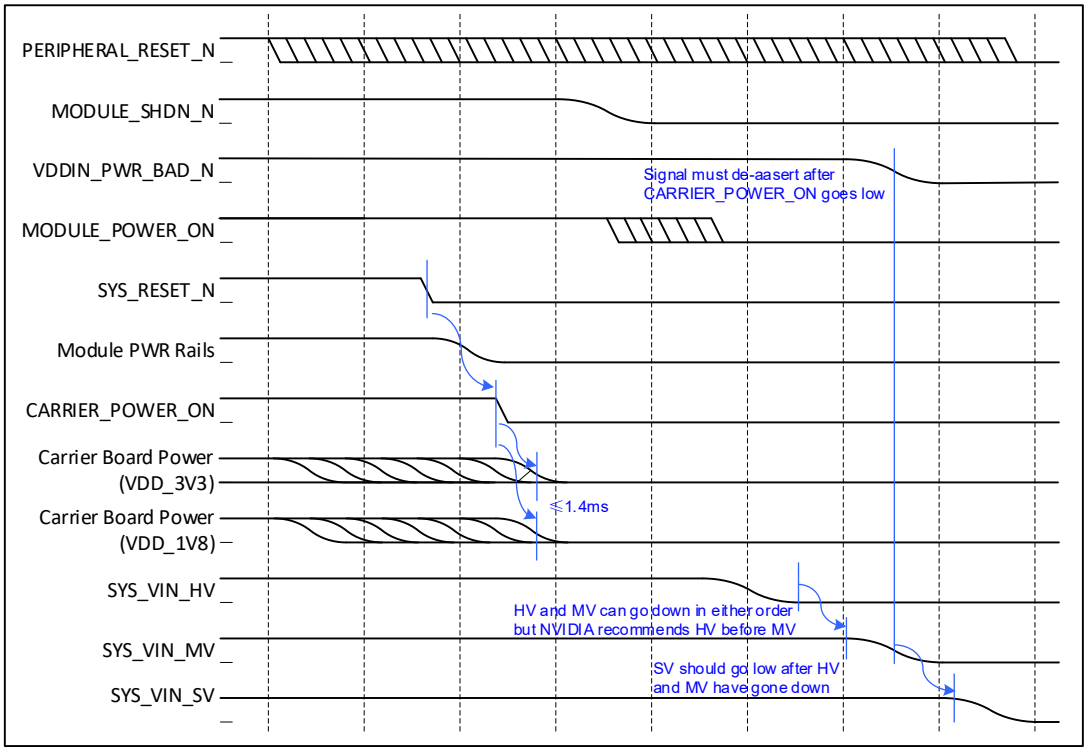
Notes:

1. Once CARRIER_POWER_ON is de-asserted by the module, backdrive into Thor I/O from the carrier board must be eliminated by this point.
2. VDD_3V3 and VDD_1V8 on the carrier board should be discharged earlier than the module power. Refer to section 5.4 Power Discharge for discharging.
3. SYS_VIN_MV must go below 100 mV before the system can be powered on again. Any undefined low voltage is considered as 0V.

5.1.3 Power Down Sequence by Software Shutdown

1. MODULE_SHDN_N and VDDIN_PWR_BAD_N do not play a role in this power down sequence.
2. SYS_RESET_N is the first signal to assert low.
3. MODULE_POWER_ON signal should go low after CARRIER_POWER_ON goes low. With the button MCU solution used on the reference design, MODULE_POWER_ON will go low after a propagation delay/MCU response time as CARRIER_POWER_ON notifies the Button MCU to go to shutdown state.

Figure 5-4. Power Down Sequence – User Initiated – SW Shutdown Case



Notes (see Figure 5-4):

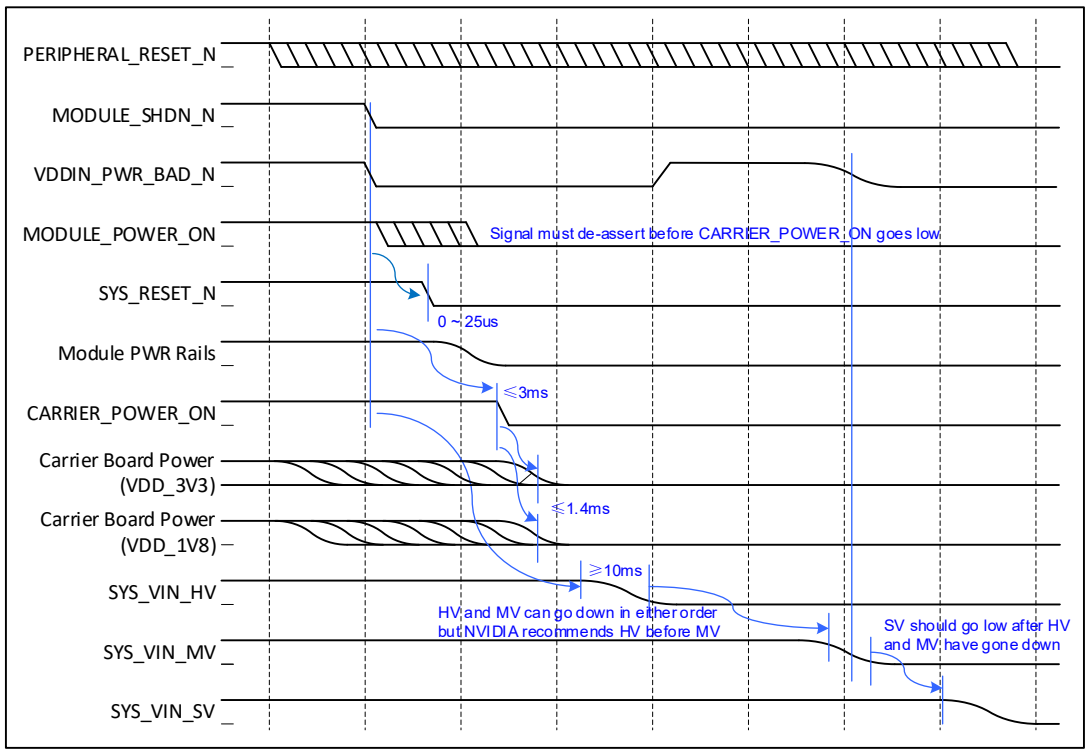
1. Once CARRIER_POWER_ON is de-asserted by the module, backdrive into Thor I/O from the carrier board must be eliminated by this point.
2. VDD_3V3 and VDD_1V8 on the carrier board should be discharged earlier than the module power. Refer to 5.4 Power Discharge for discharging.
3. SYS_VIN_MV must go below 100 mV before the system can be powered on again. Any undefined low voltage is considered as 0V.

5.1.4 Power Down Sequence by an Event

MODULE_SHDN_N and VDDIN_PWR_BAD_N signals are essentially all tied together.

- MODULE_SHDN_N is a signal to the carrier board indicating the module is shutting down, primarily due to a thermal event.
- VDDIN_PWR_BAD_N is a signal from the carrier board. If the monitored voltage drops below a threshold, this signal is pulled low, initiating a shutdown. It should connect to a circuit on the carrier board that also pulls MODULE_POWER_ON low, ensuring both the module and carrier board recognize the shutdown state). This is implemented in the Power Button MCU circuit in the reference design.

Figure 5-5. Power Down Sequence – Shutdown Due to an Event Case



Notes (see Figure 5-4):

1. Once CARRIER_POWER_ON is de-asserted by the module, backdrive into Thor I/O from the carrier board must be eliminated by this point.
2. VDD_3V3 and VDD_1V8 on the carrier board should be discharged earlier than the module power. Refer to section 5.4 Power Discharge for discharging.
3. SYS_VIN_MV must go below 100 mV before the system can be powered on again. Any undefined low voltage is considered as 0V.
4. If the main power rails (**SYS_VIN_HV/MV**) are not powered off, it is possible for the system to power on again depending on the state of the signals. If the system was powered down due to a shutdown condition that is cleared, the system may power back on. Unless this is desired, a means of keeping the module powered off should be provided. One way is to latch the state of **CARRIER_POWER_ON** when it goes from high to low (module powered off) and using this to keep **MODULE_POWER_ON** inactive (low).

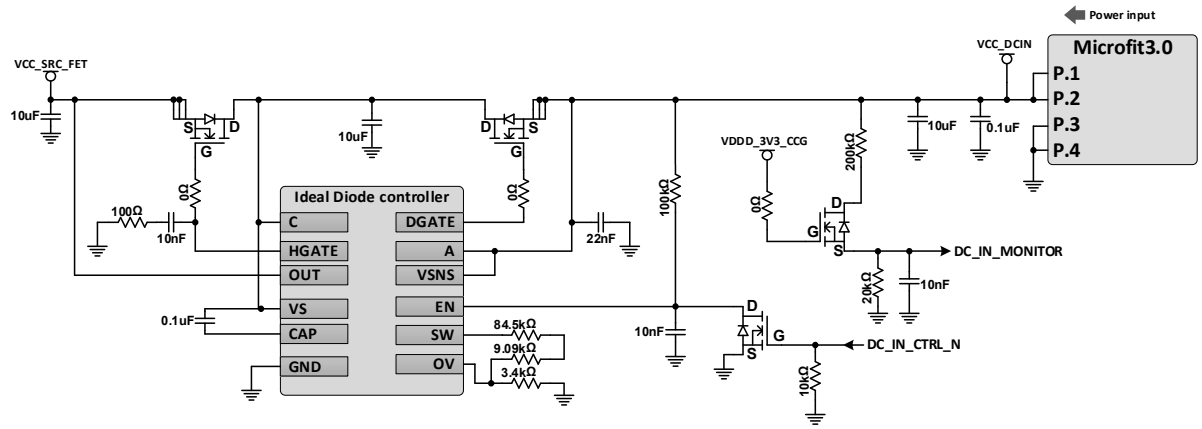
5.2 SYS_VIN_HV Input

The Jetson Thor Developer Kit carrier board allows the main system power to be supplied either by one of the USB Type-C connectors or a Microfit connector. The details for implementing USB-C for power can be found in the Jetson Thor Carrier Board Reference Design Files. If a design only requires a simple Microfit connector, the circuit in Figure 5-5 can be used.

Note: Designs that intend to follow the NVIDIA carrier board design and include the USB-C PD Controller (CYPD8225 – U237) must replicate the circuitry on the latest Jetson Thor Carrier Board exactly. NVIDIA will provide the binary and the customer should get the flashing instructions from Cypress. Make sure the system gets more than 45W during flashing.

The example shown in Figure 5-5 shows the main system power being supplied to the carrier board by a Microfit connector. This circuit is a simplified example based on the carrier board reference design.

Figure 5-6. Simplified Microfit Connector Connections



Note: Designs with a single MOSFET should select a part that DOES NOT limit reverse current.

5.3 Power-On

This section provides examples for powering on the Jetson Thor.

- Auto Power-ON requirements
- Power button supervisor MCU circuit

5.3.1 Auto Power-on

If the system does not require a power button or equivalent, and should power on when the main power source is connected, the following requirements should be met:

- **SYS_VIN_SV, SYS_VIN_HV,** and **SYS_VIN_MV** should be powered on. **SYS_VIN_SV** must be powered up first or it may have remained powered from the previous power cycle. These can be optionally gated and a signal used to enable them when the module is detected mounted correctly using PRSNT[1:0].
- **VDDIN_PWR_BAD_N** should be de-asserted (high) once the **SYS_VIN_HV** and **SYS_VIN_MV** supplies are enabled and stable.
- **MODULE_POWER_ON** should be asserted (high)

Note: The design should de-assert (low) **MODULE_POWER_ON** if **VDDIN_PWR_BAD_N** is asserted (low), **CARRIER_POWER_ON** is de-asserted (low), or **MODULE_SHDN_N** is asserted (low).

5.3.2 Power Button Supervisor MCU Circuit

The Jetson Thor Developer Kit carrier board implements a power button supervisor (or Button MCU for short). This supervisor is a low power device meant to intercept push-button (momentary) switches to control ON or Enable signals to the module Power Sequencer and main processor. This supervisor is always powered and allows close to complete system Power-OFF while providing proper timing for ON and OFF signals to the system. The selected Button MCU to perform this function is the EFM8SB10F2G-QFN20 from Silicon Labs.

Note: Designs that intend to follow the NVIDIA carrier board design and include the EFM8SB10F2G-QFN20 MPU for Button Power Button control need to replicate the circuitry on the latest Jetson Thor Carrier Board. NVIDIA will provide the binary and the customer should get the flashing instructions from Silicon Labs.

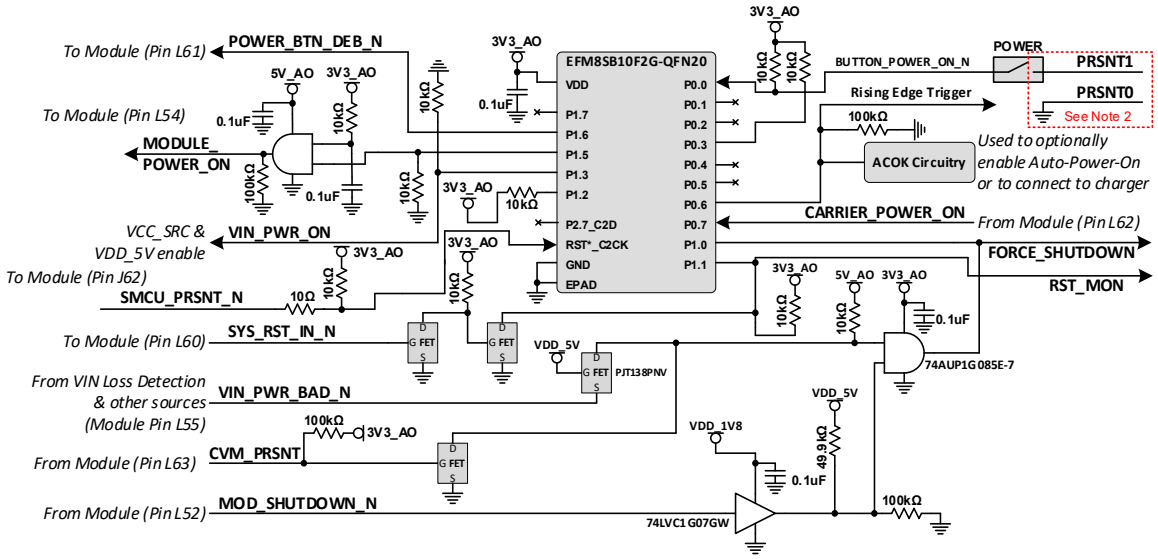
Table 5-2. Power Button Supervisor Control Signals

Signal Name	Associated Module Pin #	I/O Type	Trigger Level	Drive Mode	Description	MCU Pin
BUTTON_POWER_ON_N		Input (debounced)	Level	OD (HiZ)	Power Button	P0.0
EFM8_ACOK		Input (debounced)	Edge	OD (HiZ)	Determine when power is supplied	P0.6
CARRIER_POWER_ON	L62	Input	Level	OD (HiZ)	Closed loop on power output	P0.7
SYS_RESET_N	L60	Input	Edge	OD (HiZ)	Monitor / Power Good mask	P1.1

Signal Name	Associated Module Pin #	I/O Type	Trigger Level	Drive Mode	Description	MCU Pin
MODULE_SHDN_N	L52	Input	Level	OD (HiZ)	Triggers shutdown sequence	P1.0
BRD_SEL		Input		OD (HiZ)	Strap pin for board selection	P1.2
VIN_PWR_ON		Output		PP	Enable power to module	P1.3
MODULE_POWER_ON	L54	Output		PP	Enable input to PMIC	P1.5
POWER_BTN_DEB_N	L61	Output		OD	Buffered output of power button signal	P1.6

Note: OD = Open-drain. PP = Push-pull.

Figure 5-7. Power-On Button Circuit



Notes:

1. Refer to the carrier board reference design for the latest connection details including different sources for ACOK.
2. Optional use of Present pins on module to ensure the power button will only initiate power-on if the module is mounted correctly. The PRSNT[1:0] pins are on opposing corners of the module connector.

5.3.2.1 Defined Behaviors

For all actions triggered by **BUTTON_POWER_ON*** or **ACOK**, there will be a de-bounce time before triggering any output signal. The minimum I/O delay for these signals is therefore the de-bounce time. De-bounce time is 20 ms. If both signals are triggered within the 20 ms de-bounce time started by the first detected signal, then the de-bounce time for the subsequent signals might extend up to 25 ms.

> **Note**: The time values in the following timing diagrams have an accuracy of ± 10%.

5.3.2.2 Power-OFF -> Power-ON (Power Button Case)

Power button press use case: User presses the power button briefly, and the Button MCU sends the power enable signals to the module (**VIN_PWR_ON**) and to the Power Sequencer on the module (**MODULE_POWER_ON**). The signal representing the power button to the Jetson Thor (**POWER_BTN_N**), will have the same (brief) duration of the power button input to the Button MCU. Once the power button is pressed, the power OK input (ACOK) is ignored, as the power-ON sequence is already initiated by the power button.

If power-ON is successful, `FORCE_SHUTDOWN_N` goes high as well as `CARRIER_POWER_ON`.

Figure 5-8. Power-OFF to On Sequence Power Button Case

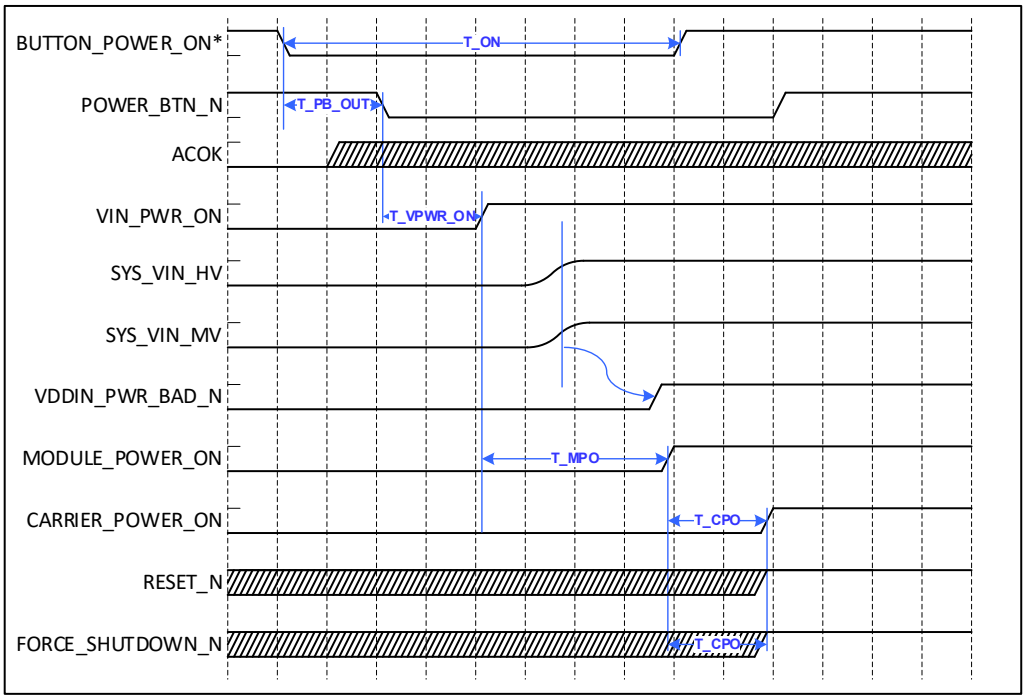


Table 5-3. Power-OFF to On Timing Power Button Case

Timing	Parameter	Min	Typical	Units
T_ON	BUTTON_POWER_ON*	20		ms
T_PB_OUT	Delay from BUTTON_POWER_ON to POWER_BTN_N		20	ms
T_VPWR_ON	Delay to first rail ON		0	ms

Timing	Parameter	Min	Typical	Units
T_SV	Time delay required after SYS_VIN_SV is up and stable before SYS_VIN_MV and SYS_VIN_HV begin to power up.	20		ms
T_MPO	MODULE_POWER_ON (module PMIC enable) delay from power VIN_PWR_ON rising edge		80	ms
T_CPO	Maximum allocated delay to CARRIER_POWER_ON assertion		100	ms

5.3.2.3 Power-OFF -> Power-ON (Auto-Power-On Case)

When the user connects the main power source, the Button MCU sends the power enable signals to the module (**VIN_PWR_ON**) and enables **MODULE_POWER_ON**. This is accomplished by having the ACOK signal driven high instead of pulled to **GND**.

The signal representing the power button to the Jetson Thor (**POWER_BTN_N**) will continue following the power button (**BUTTON_POWER_ON***) behavior. However, once the power-ON sequence is initiated by the connection of the main power source, and **ACOK** is driven high (by push-pull driver powered from 3V3_AO), the power button signals will not affect the Button MCU behavior until the **PWR_GOOD** signal verification is complete.

Figure 5-9. Power-OFF to On Sequence Auto Power-On Case

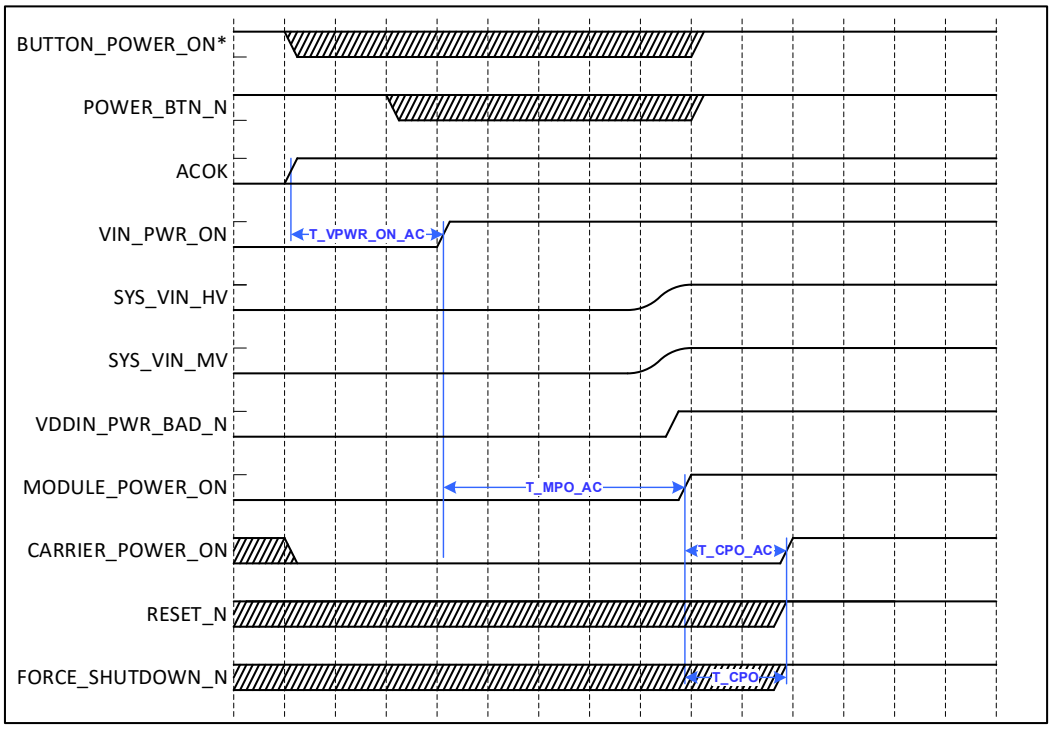


Table 5-4. Power-OFF to On Timing Auto Power-On Case

Timing	Parameter	Typical	Units
T_VPWR_ON_AC	Delay from ACOK detected high with main power source applied to first rail ON (de-bounce only)	20	ms
T_SV	Time delay required after SYS_VIN_SV is up and stable before SYS_VIN_HV and SYS_VIN_MV begin to power up	20 (min)	ms
T_MPO_AC	MODULE_POWER_ON active delay from VIN_PWR_ON rising edge	80	ms
T_CPO_AC	Maximum allocated delay to CARRIER_POWER_ON active	100	ms

5.3.2.4 Power-ON -> Power-OFF (Power Button Held Low > 10 Seconds)

With the system in power-ON state, the user holds the power button for more than 10 seconds. The same button signal is relayed to the Jetson Thor through the buffered signal **POWER_BTN_N**. The system is forced to shut down at the 10 second mark. **ACOK** is ignored as the sequence is initiated by the power button.

Figure 5-10. Power-ON to OFF Power Button Held Low > 10 Seconds

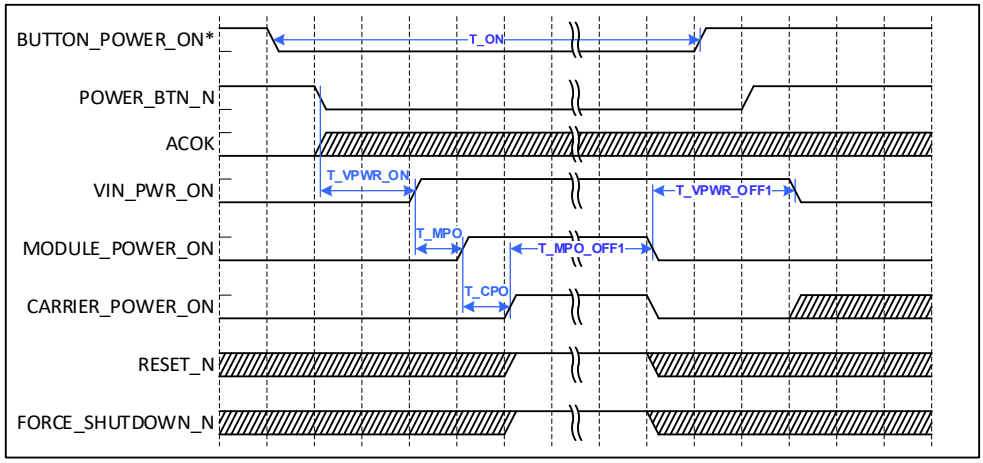


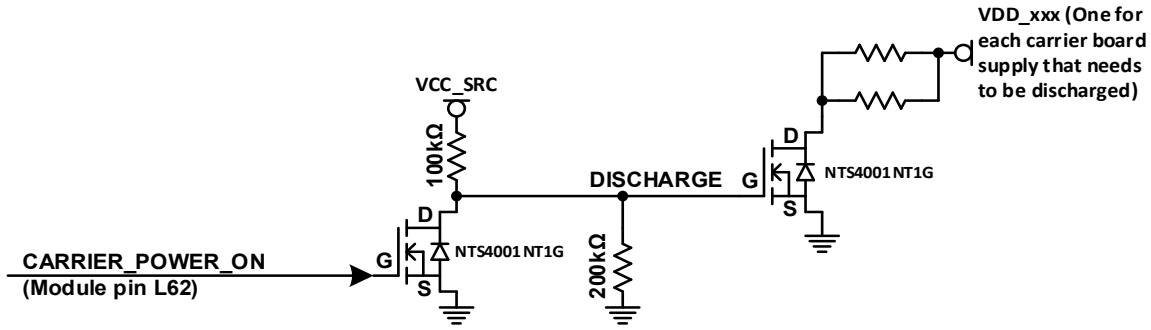
Table 5-5. Power-ON to OFF Timing Power Button Held Low > 10 Seconds

Timing	Parameter	Typical	Units
T_ON	Power button active duration for forced OFF (T_PWR_ON + T_MPO_ON + T_CPO + T_MPO_OFF1)	> 10	s
T_VPWR_ON	Delay to first rail ON (de-bounce only)	20	ms
T_MPO_OFF1	Wait time to force MODULE_POWER_ON OFF	10	s
T_MPO	Enable delay from VIN_PWR_ON rising edge	80	ms
T_CPO	Maximum allocated delay to detect CARRIER_POWER_ON	100	ms
T_VPWR_OFF1	Delay to first rail OFF	10	ms

5.4 Power Discharge

To meet the power down requirements, discharge circuitry may be required. Figure 5-10 shows an example of a simplified discharge circuit. The **DISCHARGE** signal is generated, based on a transition of the **CARRIER_POWER_ON** signal or the removal of the main supply (**VDD_SRC**). When **DISCHARGE** is asserted, the various carrier board rails that need to be discharged are pulled to GND.

Figure 5-11. Power Discharge

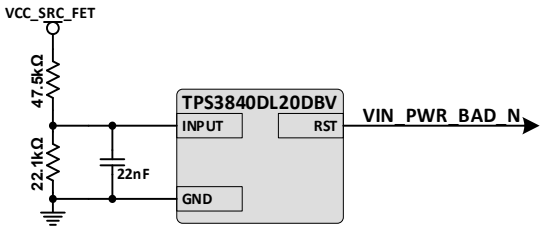


Note: The resistor values in the discharge circuit for each rail should be tuned to bring the rail down in the proper timeframe.

5.5 Power Loss Detection

The circuit in Figure 5-11 is implemented on the Jetson Thor carrier board to detect a loss or unacceptable droop on the main power input (**VCC_SRC**).

Figure 5-12. VIN Loss Detection Circuit



5.6 Deep Sleep or SC7

Jetson Thor supports a low power state called Deep Sleep or SC7. This can be entered under software control, and exited using various mechanisms, including wake capable pins that are listed in the pin mux. More details related to SC7 can be found in the module data sheet and developer guide.

Chapter 6. General Routing Guidelines

6.1 Signal Name Conventions

The following conventions are used in describing the signals for Jetson Thor:

- Signal names use a mnemonic to represent the function of the signal. For example, Serial Peripheral Interface Chip Select signal is represented as **SPI_CS**, with a different font to distinguish it from other text. All active low signals are identified by an underscore followed by capital N (_N) after the signal name. For example, **SYS_RESET_N** indicates an active low signal. Active high signals do not have the underscore-N (_N) after the signal names. For example, **CARRIER_POWER_ON** indicates an active high signal. Differential signals are identified as a pair with the same names that end with _P and _N, just P and N or + and - (for positive and negative, respectively). For example, **USB1_P** and **USB1_N** indicate a differential signal pair.
- I/O Type: The signal I/O type is represented as a code to indicate the operational characteristics of the signal.

The following table lists the I/O codes used in the signal description tables.

Table 6-1. Signal Type Codes

Code	Definition
A	Analog
DIFF I/O	Bidirectional Differential Input/Output
DIFF IN	Differential Input
DIFF OUT	Differential Output
I/O	Bidirectional Input/Output
I	Input
O	Output
OD	Open Drain Output
I/OD	Bidirectional Input / Open Drain Output
P	Power

6.2 Routing Guideline Format

The routing guidelines have the following format to specify how a signal should be routed.

- Breakout traces are traces routed from a BGA or other pin array, either to a point beyond the array, or to another layer where full normal spacing guidelines can be met. Breakout trace delay is limited to 12.5 mm unless otherwise specified.
- After breakout, signals should be routed according to specified impedance for differential, single-ended, or both (for example: HDMI). Trace spacing to other signals also specified.
- Follow maximum and minimum trace delays where specified. Trace delays are typically shown in mm or in terms of signal delay in pico-seconds (ps) or both.
  - For differential signals, trace spacing to other signals must be larger of specified × dielectric height or inter-pair spacing.
  - Spacing to other signals or pairs cannot be smaller than spacing between complementary signals (intra-pair).
  - Total trace delay depends on signal velocity, which is different between outer (microstrip) and inner (stripline) layers of a PCB.

6.3 Signal Routing Conventions

Throughout this design guide, the following signal routing conventions are used:

SE Impedance (/ Diff Impedance) at x Dielectric Height Spacing

- Single-ended (SE) impedance of trace (along with differential impedance for diff pairs) is achieved by spacing requirement. Spacing requirements are specified as a multiple of dielectric height. Dielectric height is typically different for microstrip and stripline.

Note: Trace spacing requirement applies to SE traces or differential pairs to other SE traces or differential pairs. It does not apply to traces making up a differential pair. For this case, spacing/trace widths are chosen to meet differential impedance requirement.

6.4 Routing Guidelines

Pay close attention when routing high-speed interfaces, such as HDMI, DP, USB 3.2, MGBE, PCIe, or CSI. Each of these interfaces has strict routing rules for the trace impedance, width, spacing, total delay, and delay or flight time matching. The following guidelines provide an overview of the routing guidelines and notations used in this design guide.

- **Controlled Impedance**
  Each interface has different trace impedance requirements and spacing to other traces. It is up to the designer to calculate trace width and spacing required to

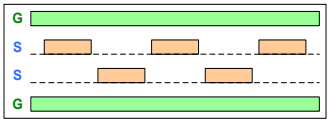
achieve specified single-ended (SE) and differential (Diff) impedances. Unless otherwise noted, trace impedance values are ±15%.

- **Max Trace Lengths and Delays**
  Trace lengths and delays should include main PCB routing and any additional routing on a flex or secondary PCB segment connected to main PCB. The maximum length or delay should be from the Jetson Thor to the actual connector (i.e., USB, HDMI and so on) or device (i.e., onboard USB device, Display driver IC, camera imager IC, and so on).
- **Trace Delay or Flight Time Matching**
  Signal flight time is the time it takes for a signal to propagate from one end (driver) to the other end (receiver). One way to get the same flight time for a signal within a signal group is to match trace lengths or delays within the specified delay in the signal group.
  - Total trace delay = Carrier PCB trace delay only. Do not exceed maximum trace delay specified.
  - It is recommended to match trace delays based on flight time of signals. For example, outer-layer signal velocity could be 5.9 ps/mm and inner-layer 6.9 ps/mm. If one signal is routed 250 mm on the outer layer and second signal is routed 250 mm in the inner layer, the difference in flight time between two signals will be 250 ps! That is a big difference if required matching is 15 ps (trace delay matching). To fix this, inner trace needs to be 36 mm shorter or outer trace needs to be 42 mm longer.
  - In this design guide, terms such as intra-pair and inter-pair are used when describing differential pair delay. Intra-pair refers to matching traces within differential pair (for example, true to complement trace matching). Inter-pair matching refers to matching differential pairs average delays to other differential pairs average delays. For CSI CPHY, Intra-trio and inter-trio describe relative trio delays. Intra-trio refers to matching traces within the CPHY trios. Inter-trio matching refers to matching trio average delays to other trio average delays.

6.5 General PCB Routing Guidelines

For GSSG stack-up to minimize crosstalk, signals should be routed in such a way that they are not on top of each other in two routing layers, as shown in the following figure.

Figure 6-1. Signal Routing Example



Do not route other signals or power traces and areas directly under or over critical high-speed interface signals.

Note: The requirements detailed in the interface signal routing requirements tables must be met for all interfaces implemented or proper operation cannot be guaranteed.

Chapter 7. USB, PCIe, and MGBE

The Jetson Thor facilitates multiple high-speed interfaces to be brought out on the module in different configurations. The tables in this chapter show basic generic usage and descriptions of the UPHY lanes.

Table 7-1. SoC UPHY0 Data Lane Pin Descriptions (USB 3.2 and PCIe)

Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type
C35	UPHY_RX0_N	HS_UPHY0_L0_RX_N	UPHY block 0, Receive Lane 0	Input	UPHY Diff Pair
C34	UPHY_RX0_P	HS_UPHY0_L0_RX_P		Input	UPHY Diff Pair
A23	UPHY_RX1_N	HS_UPHY0_L1_RX_N	UPHY block 0, Receive Lane 1	Input	UPHY Diff Pair
A22	UPHY_RX1_P	HS_UPHY0_L1_RX_P		Input	UPHY Diff Pair
C22	UPHY_RX2_N	HS_UPHY0_L2_RX_N	UPHY block 0, Receive Lane 2	Input	UPHY Diff Pair
C23	UPHY_RX2_P	HS_UPHY0_L2_RX_P		Input	UPHY Diff Pair
B32	UPHY_RX3_N	HS_UPHY0_L3_RX_N	UPHY block 0, Receive Lane 3	Input	UPHY Diff Pair
B33	UPHY_RX3_P	HS_UPHY0_L3_RX_P		Input	UPHY Diff Pair
B20	UPHY_RX4_N	HS_UPHY0_L4_RX_N	UPHY block 0, Receive Lane 4	Input	UPHY Diff Pair
B21	UPHY_RX4_P	HS_UPHY0_L4_RX_P		Input	UPHY Diff Pair
D21	UPHY_RX5_N	HS_UPHY0_L5_RX_N	UPHY block 0, Receive Lane 5	Input	UPHY Diff Pair
D20	UPHY_RX5_P	HS_UPHY0_L5_RX_P		Input	UPHY Diff Pair
B13	UPHY_RX6_N	HS_UPHY0_L6_RX_N	UPHY block 0, Receive Lane 6	Input	UPHY Diff Pair
B12	UPHY_RX6_P	HS_UPHY0_L6_RX_P		Input	UPHY Diff Pair
D13	UPHY_RX7_N	HS_UPHY0_L7_RX_N	UPHY block 0, Receive Lane 7	Input	UPHY Diff Pair
D12	UPHY_RX7_P	HS_UPHY0_L7_RX_P		Input	UPHY Diff Pair
K33	UPHY_TX0_N	HS_UPHY0_L0_TX_N	UPHY block 0, Transmit Lane 0	Output	UPHY Diff Pair
K32	UPHY_TX0_P	HS_UPHY0_L0_TX_P		Output	UPHY Diff Pair
J23	UPHY_TX1_N	HS_UPHY0_L1_TX_N	UPHY block 0, Transmit Lane 1	Output	UPHY Diff Pair
J22	UPHY_TX1_P	HS_UPHY0_L1_TX_P		Output	UPHY Diff Pair
G22	UPHY_TX2_N	HS_UPHY0_L2_TX_N	UPHY block 0, Transmit Lane 2	Output	UPHY Diff Pair
G23	UPHY_TX2_P	HS_UPHY0_L2_TX_P		Output	UPHY Diff Pair
G34	UPHY_TX3_N	HS_UPHY0_L3_TX_N	UPHY block 0, Transmit Lane 3	Output	UPHY Diff Pair
G35	UPHY_TX3_P	HS_UPHY0_L3_TX_P		Output	UPHY Diff Pair
K20	UPHY_TX4_N	HS_UPHY0_L4_TX_N	UPHY block 0, Transmit Lane 4	Output	UPHY Diff Pair
K21	UPHY_TX4_P	HS_UPHY0_L4_TX_P		Output	UPHY Diff Pair
H21	UPHY_TX5_N	HS_UPHY0_L5_TX_N	UPHY block 0, Transmit Lane 5	Output	UPHY Diff Pair
H20	UPHY_TX5_P	HS_UPHY0_L5_TX_P		Output	UPHY Diff Pair
K12	UPHY_TX6_N	HS_UPHY0_L6_TX_N	UPHY block 0, Transmit Lane 6	Output	UPHY Diff Pair
K13	UPHY_TX6_P	HS_UPHY0_L6_TX_P		Output	UPHY Diff Pair
H13	UPHY_TX7_N	HS_UPHY0_L7_TX_N	UPHY block 0, Transmit Lane 7	Output	UPHY Diff Pair

Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type
H12	UPHY_TX7_P	HS_UPHY0_L7_TX_P		Output	UPHY Diff Pair

Notes:

In the Direction column, Output is from the Jetson Thor; Input is to the Jetson Thor. Bidir is for Bidirectional signals.

AC coupling capacitors are required for PCIe TX signals from both the Thor SoC and the connected PCIe device. If the connected PCIe device is on the other side of a connector, the AC capacitors should be located on the same side of the connector as the PCIe device.

Table 7-2. SoC UPHY1 Data Lane Pin Descriptions (PCIe and MGBE (XFI))

Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type
D25	UPHY_RX8_N	HS_UPHY1_L0_RX_N	UPHY block 1, Receive Lane 0	Input	UPHY Diff Pair
D24	UPHY_RX8_P	HS_UPHY1_L0_RX_P		Input	UPHY Diff Pair
B24	UPHY_RX9_N	HS_UPHY1_L1_RX_N	UPHY block 1, Receive Lane 1	Input	UPHY Diff Pair
B25	UPHY_RX9_P	HS_UPHY1_L1_RX_P		Input	UPHY Diff Pair
C26	UPHY_RX10_N	HS_UPHY1_L2_RX_N	UPHY block 1, Receive Lane 2	Input	UPHY Diff Pair
C27	UPHY_RX10_P	HS_UPHY1_L2_RX_P		Input	UPHY Diff Pair
A27	UPHY_RX11_N	HS_UPHY1_L3_RX_N	UPHY block 1, Receive Lane 3	Input	UPHY Diff Pair
A26	UPHY_RX11_P	HS_UPHY1_L3_RX_P		Input	UPHY Diff Pair
D29	UPHY_RX12_N	HS_UPHY1_L4_RX_N	UPHY block 1, Receive Lane 4	Input	UPHY Diff Pair
D28	UPHY_RX12_P	HS_UPHY1_L4_RX_P		Input	UPHY Diff Pair
B28	UPHY_RX13_N	HS_UPHY1_L5_RX_N	UPHY block 1, Receive Lane 5	Input	UPHY Diff Pair
B29	UPHY_RX13_P	HS_UPHY1_L5_RX_P		Input	UPHY Diff Pair
C30	UPHY_RX14_N	HS_UPHY1_L6_RX_N	UPHY block 1, Receive Lane 6	Input	UPHY Diff Pair
C31	UPHY_RX14_P	HS_UPHY1_L6_RX_P		Input	UPHY Diff Pair
A31	UPHY_RX15_N	HS_UPHY1_L7_RX_N	UPHY block 1, Receive Lane 7	Input	UPHY Diff Pair
A30	UPHY_RX15_P	HS_UPHY1_L7_RX_P		Input	UPHY Diff Pair
H25	UPHY_TX8_N	HS_UPHY1_L0_TX_N	UPHY block 1, Transmit Lane 0	Output	UPHY Diff Pair
H24	UPHY_TX8_P	HS_UPHY1_L0_TX_P		Output	UPHY Diff Pair
K24	UPHY_TX9_N	HS_UPHY1_L1_TX_N	UPHY block 1, Transmit Lane 1	Output	UPHY Diff Pair
K25	UPHY_TX9_P	HS_UPHY1_L1_TX_P		Output	UPHY Diff Pair
G26	UPHY_TX10_N	HS_UPHY1_L2_TX_N	UPHY block 1, Transmit Lane 2	Output	UPHY Diff Pair
G27	UPHY_TX10_P	HS_UPHY1_L2_TX_P		Output	UPHY Diff Pair
J27	UPHY_TX11_N	HS_UPHY1_L3_TX_N	UPHY block 1, Transmit Lane 3	Output	UPHY Diff Pair
J26	UPHY_TX11_P	HS_UPHY1_L3_TX_P		Output	UPHY Diff Pair
H29	UPHY_TX12_N	HS_UPHY1_L4_TX_N	UPHY block 1, Transmit Lane 4	Output	UPHY Diff Pair
H28	UPHY_TX12_P	HS_UPHY1_L4_TX_P		Output	UPHY Diff Pair
K28	UPHY_TX13_N	HS_UPHY1_L5_TX_N	UPHY block 1, Transmit Lane 5	Output	UPHY Diff Pair
K29	UPHY_TX13_P	HS_UPHY1_L5_TX_P		Output	UPHY Diff Pair
G30	UPHY_TX14_N	HS_UPHY1_L6_TX_N	UPHY block 1, Transmit Lane 6	Output	UPHY Diff Pair
G31	UPHY_TX14_P	HS_UPHY1_L6_TX_P		Output	UPHY Diff Pair
J31	UPHY_TX15_N	HS_UPHY1_L7_TX_N	UPHY block 1, Transmit Lane 7	Output	UPHY Diff Pair
J30	UPHY_TX15_P	HS_UPHY1_L7_TX_P		Output	UPHY Diff Pair

Notes:

In the Direction column, Output is from Jetson Thor; Input is to Jetson Thor. Bidir is for Bidirectional signals.

AC coupling capacitors are required for PCIe TX signals from both the Thor SoC and the connected PCIe device. If the connected PCIe device is on the other side of a connector, the AC capacitors should be located on the same side of the connector as the PCIe device.

The following tables show the supported UPHY mapping for the UPHY blocks [1:0]. The mapping tables indicate which lanes of each UPHY block can be assigned for USB, PCIe, or MGBE. Only one of the supported configurations per UPHY block can be used in a design. Each UPHY block is programmed independently. It is not required to select the same configuration on all two UPHY blocks.

Table 7-3. UPHY0 Mapping Options (USB and PCIe)

Module Pin Names	UPHY0 Lanes	Jetson Thor Functions	
		Configuration #1	Configuration #2
UPHY_RX0/TX0	Lane 0	USB 3.2 (P0)	
UPHY_RX1/TX1	Lane 1	USB 3.2 (P1)	
UPHY_RX2/TX2	Lane 2	USB 3.2 (P2)	
UPHY_RX3/TX3	Lane 3	PCIe x1 (C1), RP	
UPHY_RX4/TX4	Lane 4	PCIe x1 (C2), RP or EP	
UPHY_RX5/TX5	Lane 5	Reserved	
UPHY_RX6/TX6	Lane 6	PCIe x2 (C3), RP	
UPHY_RX7/TX7	Lane 7		

Table 7-4. UPHY1 Mapping Options (PCIe and MGBE (XFI))

Module Pin Names	UPHY1 Lanes	Jetson Thor Functions	
		Configuration #1	Configuration #2
UPHY_RX8/TX8	Lane 0	PCIe x8 (C4), RP or EP	PCIe x4 (C5), RP or EP
UPHY_RX9/TX9	Lane 1		
UPHY_RX10/TX10	Lane 2		
UPHY_RX11/TX11	Lane 3		
UPHY_RX12/TX12	Lane 4		MGBE C0 (XFI)
UPHY_RX13/TX13	Lane 5		MGBE C1 (XFI)
UPHY_RX14/TX14	Lane 6		MGBE C2 (XFI)
UPHY_RX15/TX15	Lane 7		MGBE C3 (XFI)

Note: MGBE full speed at 25GbE per port and C4 EP are being validated. Refer to the *Jetson Linux Developer Guide* (when it is available) for the latest on support.

7.1 USB

Jetson Thor supports multiple USB 2.0 and USB 3.2 ports. Each of the USB 2.0 or USB 3.2 ports can support either host or device modes. Only one USB 2.0 or USB 3.2 port can be a device at a time. Polarity inversion (P/N swapping) is supported on the USB 3.2 interfaces. There are connection examples in this section to implement either a simple USB 3.2/2.0 connection to a USB 3.2 Type A connector or to a USB-C connector (based on the NVIDIA developer kit carrier board reference design).

Notes:
1. Some non-compliant USB 3.0 devices may fail unless USB 3.2 Gen2 is disabled.
2. See Section 17.1 “USB Recovery Mode” for requirements for USB recovery mode.

USB 3.2 high-speed interface pins share UPHY lanes with PCIe.

Table 7-5. USB 2.0 Pin Descriptions

Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type
F13	USB0_N	HS_USB2_P0_N	USB 2.0 Port 0 Data	Bidir	USB2 Diff pair
F12	USB0_P	HS_USB2_P0_P			
C10	USB1_N	HS_USB2_P1_N	USB 2.0, Port 1 Data	Bidir	USB2 Diff pair
C11	USB1_P	HS_USB2_P1_P			
A11	USB2_N	HS_USB2_P2_N	USB 2.0, Port 2 Data	Bidir	USB2 Diff pair
A10	USB2_P	HS_USB2_P2_P			
G10	USB3_N	HS_USB2_P3_N	USB 2.0, Port 3 Data	Bidir	USB2 Diff pair
G11	USB3_P	HS_USB2_P3_P			

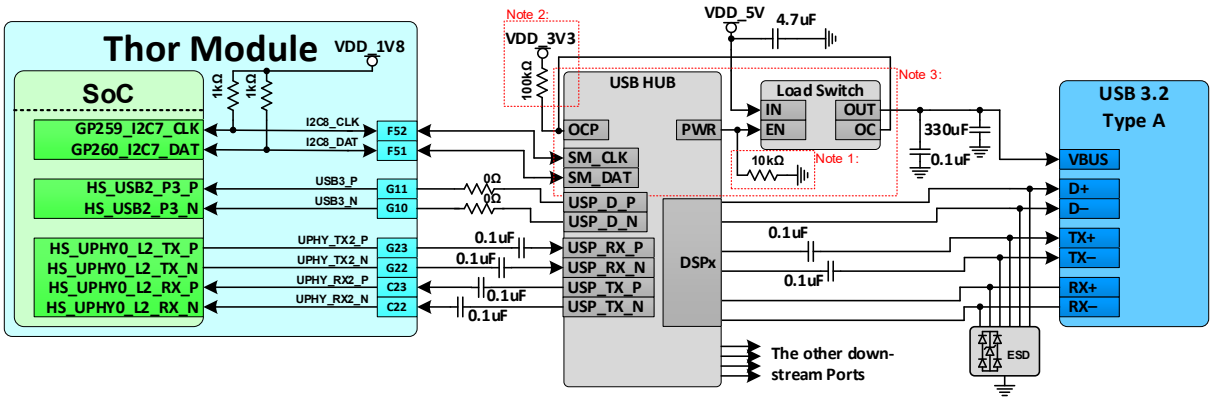
Note: In the Direction column, Output is from Jetson Thor; Input is to Jetson Thor. Bidir is for Bidirectional signals.

Table 7-6. USB Control Pin Descriptions

Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type
F54	GPIO22	GP113_USB_VBUS_EN0	USB Power enable #0 or GPIO #22	Bidir	Open-Drain, 1.8V
G55	GPIO23	GP114_USB_VBUS_EN1	USB Power enable #1 or GPIO #23	Bidir	

Note: In the Direction column, Output is from Jetson Thor; Input is to Jetson Thor. Bidir is for Bidirectional signals.

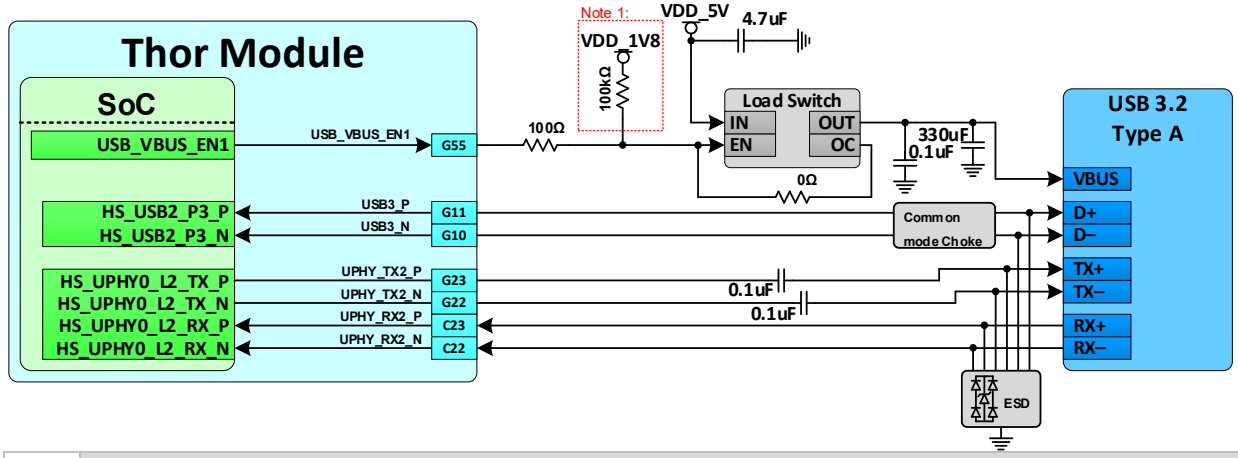
Figure 7-1. Simple USB Type A Connection Example with HUB



Notes:

1. A weak pull-down is required on the load switch enable.
2. A weak pull-up is required on Over-Current Protection (OCP).
3. A load switch is required between the carrier board supplies and the USB VBUS supply. The load switch should have over-current protection. In Figure 7-1 this is supported by routing the over current (OC) pin of the load switch to the same pin used for the over-current protection on the USB HUB pin.

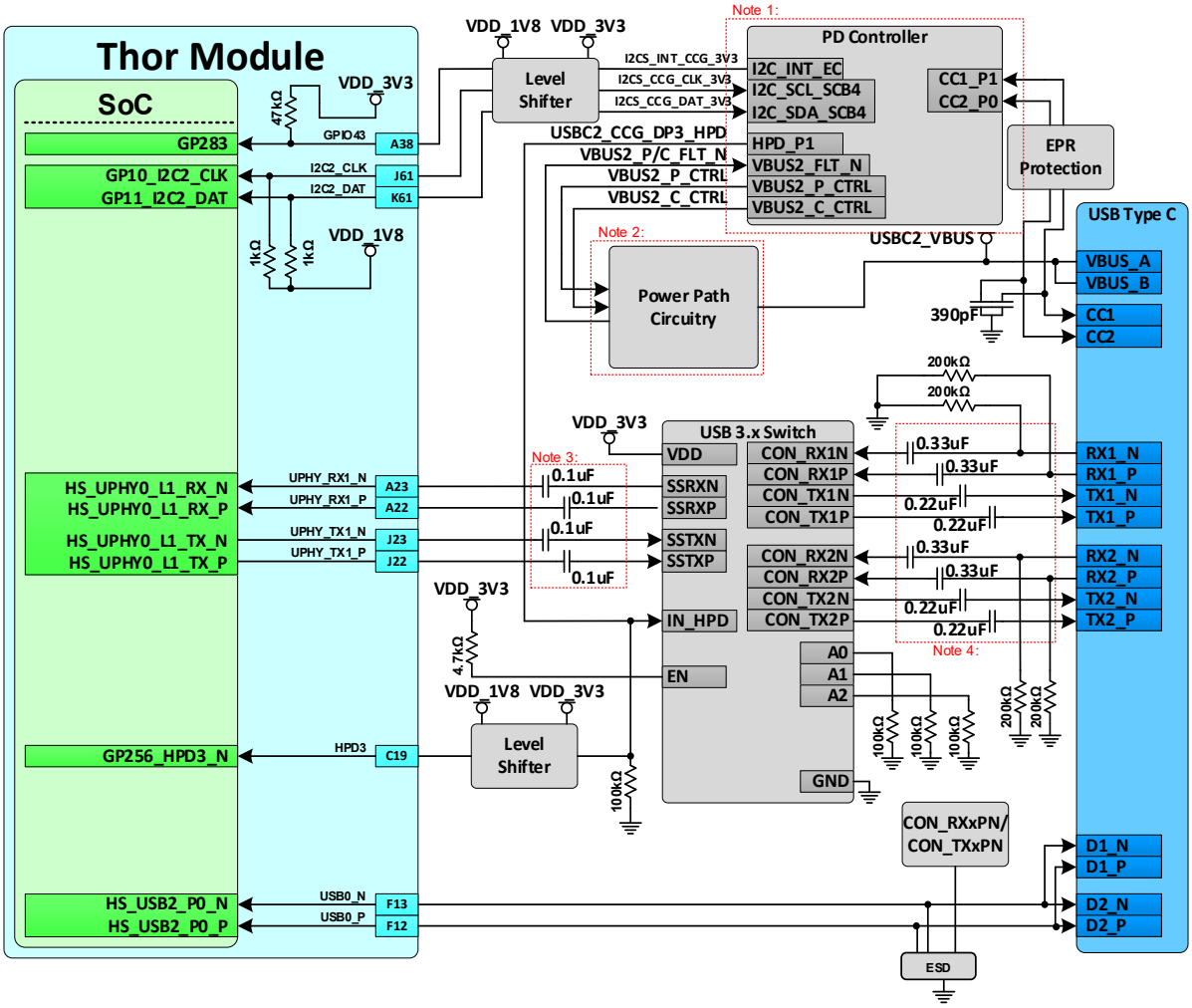
Figure 7-2. Simple USB Type A Connection Example without HUB



Notes:

1. A weak pull-up is required on the load switch enable and over-current connection.
2. A load switch is required between the carrier board supplies and the USB VBUS supply. The load switch should have over-current protection. In Figure 7-2, this is supported by routing the over current (OC) pin of the load switch to the same pin used for the enable (USB_VBUS_EN1) pin, which is bidirectional and can be used to detect an over current condition.

Figure 7-3. USB Type-C Connection Example



Notes:

1. PD controller has internal pull-up on VBUS2_FLT_N.
2. See Figure 7-4 for Dual Mode Circuitry.
3. Cap values are 0.22uF or 0.1uF. Values depend on USB 3.x Switch recommendations.
4. Caps on RX & TX depend on USB 3.x Switch used.

Figure 7-4. USB Type-C Dual Mode Circuitry Sample Connections

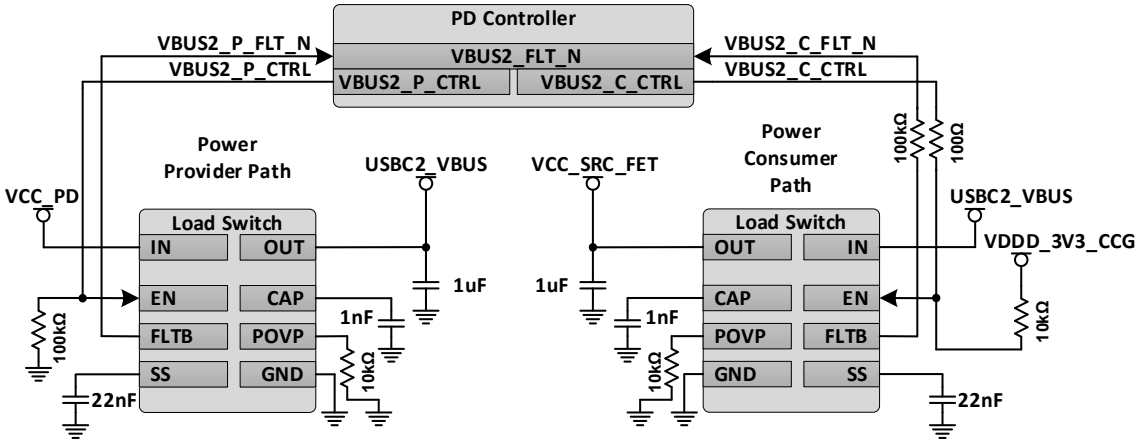


Table 7-7. USB 2.0 Signal Connections

Module Pin Name	Type	Termination	Description
USB[3:0]_N/P	DIFF I/O	90Ω common-mode chokes close to connector. ESD Protection between choke and connector on each line to GND.	USB Differential Data Pair: Connect to USB connector, Mini-Card Socket, Hub, or another device on the PCB.

Table 7-8. USB 3.2 Signal Connections

Module Pin Name	Type	Termination	Description
UPHY_TX[2:0]_N/P (USB 3.2 Port #[2:0]	DIFF Out	Series 0.1uF AC caps. See note 1.	USB 3.2 Differential Transmit Data Pairs: Connect to USB connectors, hubs, or other devices on the PCB.
UPHY_RX[2:0]_N/P (USB 3.2 Port #[2:0]	DIFF In	Series 0.1uF AC caps. See notes 1 and 2.	USB 3.2 Differential Receive Data Pairs: Connect to USB connectors, hubs, or other devices on the PCB.

Notes:

1. Common-mode chokes (not recommended) and ESD protection if required.
2. AC caps are required on both TX and RX traces. If routing to a USB connector, AC caps should be placed on the SoC TX traces only. The AC caps for the SoC RX traces will be on the peripheral side.

7.1.1 USB 2.0 Design Guidelines

These requirements apply to the USB 2.0 controller PHY interfaces: USB[3:0].

Table 7-9. USB 2.0 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency (High Speed): Bit Rate/UI period/Freq.	480/2.083/240	Mbps/ns/MHz	
Max Loading: High Speed / Full Speed / Low Speed	10 / 150 / 600	pF	Max loading should include any passive and active components on the trace such as CMC, Switch, ESD etc.
Reference plane	GND		
Trace Impedance: Diff pair / Single Ended	90 / 50	Ω	±15%
Max Via proximity (Signal via to GND return via)	24 (3.8)	ps (mm)	
Min Pair to Pair spacing Microstrip Stripline	 4x 3x	Dielectric height	
Max Trace Delay With CMC or SW (Microstrip / Stripline) Without CMC or SW (Microstrip / Stripline)	 825/965 (140) 1415/16550 (240)	ps (mm)	Prop delay assumption: 6.9/mm for stripline, 5.9ps/mm. for microstrip. See Note 3
Max Intra-Pair Skew between USBx_P and USBx_N	7.5	ps	

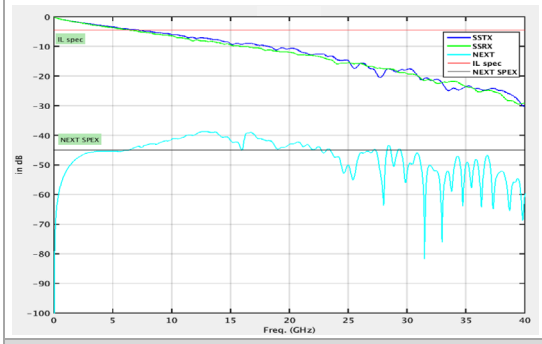
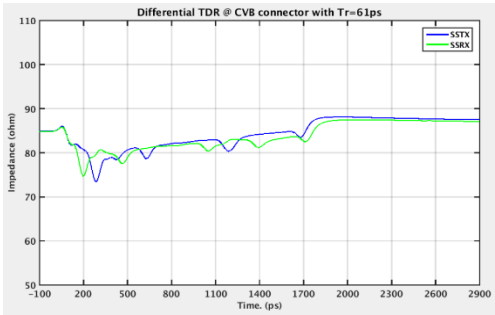
Notes:

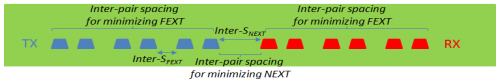
1. If a portion of route is over a flex cable this length should be included in the Max Trace Length/Delay calculation and 85Ω Differential pair trace impedance is recommended.
2. Up to four signal Vias can share a single GND return Via.
3. CMC = Common-Mode-Choke. SW = Analog Switch
4. Adjustments to the USB drive strength, slew rate, termination value settings should not be necessary, but if any are made, they MUST be done as an offset to default values instead of overwriting those values.
5. Void the ground under/below the USB connector pad for USB_DP/DN signals.
6. Keep critical USB related traces such as USBx DP/DN & USB_REXT away from other signal traces or unrelated power traces/areas or power supply components.
7. If additional connector is between module and the USB connector or other device on the PCB, routing on both sides of that connector should be included for max length and max length may have to be reduced.

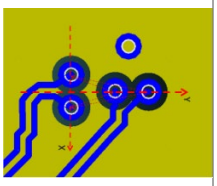
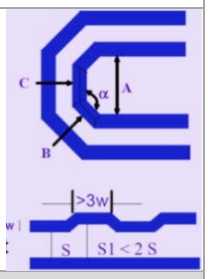
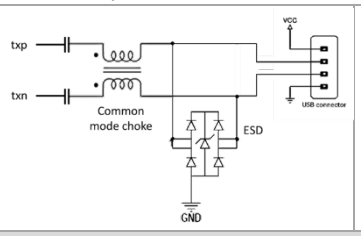
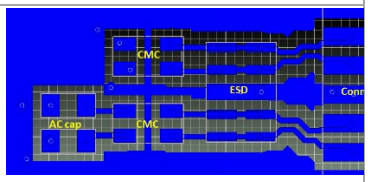
7.1.2 USB 3.2 Design Guidelines

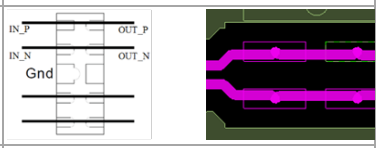
The following requirements apply to the USB 3.2 PHY interfaces. Jetson Thor supports up to USB Gen2x1 (10 Gbps).

Table 7-10. USB 3.2 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI period GEN1 GEN2	 5.0 / 200 10.0 / 100	 Gbps / ps	Device mode supports GEN1 speed only.
Max Number of Loads	1	load	
Termination	90 differential	Ω	On-die termination at TX and RX
Insertion Loss (IL) GEN1 Host (Type C) GEN1 Host (Type A) GEN1 Device (Type C) GEN1 Device (Micro AB) GEN2 Dual role mode) Resonance Dip Frequency GEN1 GEN2	 ≥ -3.8 ≥ -7.3 ≥ -3.8 ≥ -2.5 [*] ≥ -4.5 > 8 > 20	 dB @ 2.5GHz dB @ 2.5GHz dB @ 2,5GHz dB @ 2.5GHz dB @ 5GHz GHz GHz	Only the PCB (and connector) without added-on components such as CMC, ESD, and Mux, is considered. The connector is included. For Gen2, the loss budget is the same for all connector types. For dual role mode, host and device have the same loss budget [*] the consideration of Gen1 fixture loss See Note 6 The resonance dip could be caused by a via stub for layer transition or trace stub for co-layout.
Time-domain Reflectometer (TDR) Dip GEN1 GEN2	 75 75	 Ω	 @ Tr = 200ps (10%-90%) @ Tr = 61ps (10%-90%)
Near End Crosstalk (NEXT)	≤ −45	dB	DC – 5GHz per each TX-RX NEXT
IL/NEXT Plot 		TDR Plot 	
Impedance			
Trace Impedance: Diff pair / Single Ended	85 / 43	Ω	±15%. Intrinsic differential impedance, does not account for coupling from other trace pairs
Reference plane	GND		

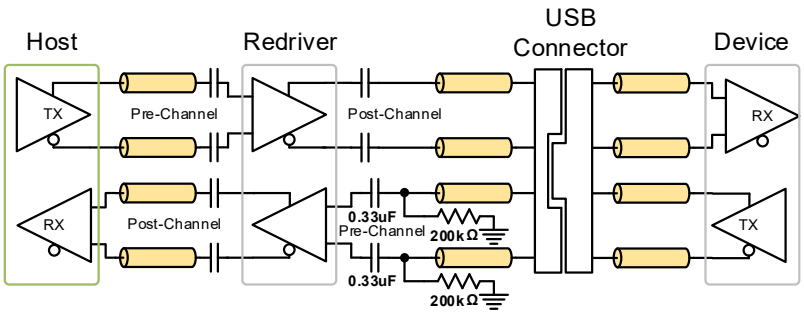
Parameter	Requirement	Units	Notes
Trace Length (delay)/Skew			
Trace loss characteristic: GEN1 GEN2	 < 0.6 < 1	 dB/in @ 2.5 GHz dB/in @ 5G Hz	Based on the dielectric material EM370(Z). The following max length is derived based on this characteristic. The length constraint must be re-defined if the loss characteristic is changed. Note that microstrip loss could be similar to stripline due to humidity effect.
The following max length (delay) is derived based on the trace loss characteristic above. The length (delay) constraint must be re-defined if loss characteristic is changed. The trace loss profile for Gen2 support is based on the dielectric material EM370(Z). See the loss plots in the sheet "USB3 LOSS BUDGET". Note that microstrip loss could be similar to stripline due to humidity effect			
Breakout Region – Max length	11	mm	Minimum trace width and spacing
Max Trace Length (delay) GEN1 Host GEN1 Device GEN2 Host or Device	 160 (1071) 107 (714) 114 (765)	 mm (ps)	Stripline (6.7ps/mm) assumed. CMC use length reduction = 30mm (GEN1/2) ESD use length reduction = 10mm (GEN1), 12.5mm (GEN2).
Max Intra-Pair Skew (RX/TX_N to RX/TX_P)	0.15 (1)	mm (ps)	Do not perform length matching within breakout region. Trace length (delay) matching should be done before discontinuities. See Note 2
Differential pair uncoupled length (delay)	6.29 (41.9)	mm (ps)	
Trace Spacing for TX/RX Non-interleaving			
TX-RX Xtalk is very critical in PCB trace routing. The ideal solution is to route TX and RX on different layers.			
If routing on the same layer, it is strongly recommended not interleaving TX and RX lanes			
If interleaving is required in breakout, all the inter-pair spacing should follow the rule of inter-S_{NEXT} (between TX/RX pair spacing)			
The breakout trace width is suggested to be the minimum to increase inter-pair spacing			
Do not perform serpentine routing for intra-pair skew compensation in the breakout region			
			
Min Inter-SNEXT (between TX/RX) Breakout Main-route	 4.85x 3x	 Dielectric height	These are the recommended dimensions for meeting the NEXT requirement. Stripline structure in a GSSG structure is assumed (holds in broadside-coupled stripline structure)
Max length Breakout (L_{BRK}) GEN1 GEN2 Main-route	 11 3 Max trace length - L_{BRK}	 mm mm	
Trace Spacing for TX/RX Interleaving			
Max Pair-pair spacing, Spacing to plane and SMT pad, and Spacing to unrelated high-speed signals Microstrip / Stripline	 4x / 3x	 Dielectric height	

Parameter	Requirement	Units	Notes
Via			
Topology	Y-pattern is recommended. Keep symmetry		Y-pattern helps with Xtalk suppression. It can also reduce the limit of the pair-pair distance. Review needed (NEXT/FEXT check) if via placement does not use Y-pattern. 
GND via	Place GND via as symmetrically as possible to data pair vias. Up to four signal vias (two diff pairs) can share a single GND return via		GND via is used to maintain return path, while its Xtalk suppression is limited
Max # of Vias PTH vias Micro Vias	4 if all vias are PTH via Not limited		As long as total channel loss meets IL specification
Max Via Stub Length	0.4	mm	Long via stub requires review (IL and resonance dip check)
Max Via proximity (Signal via to GND return via)	24 (3.8)	ps (mm)	
Serpentine			
Min bend angle	135	deg (a)	
Dimension Min A Spacing Min B, C Length Min Jog Width	 4x 1.5x 3x	Trace width	S1 must be taken care in order to consider Xtalk to adjacent pair. 
Add-on Components			
Placement order	SoC – AC capacitor – Common mode choke – ESD – Device/Connector		
			
AC Cap			
Value on TX – Min/Max	100/265	nF	100nF recommended. Only required for TX pair when routed to connector.
Value on RX (connector case) – Min/Max	297/363	nF	Optional. 330nF recommended if placed.
Location (max length to adjacent discontinuity)	8	mm	Discontinuity is connector, via, or component pad
Voiding	GND/PWR void under/above cap is required.		

Parameter	Requirement	Units	Notes
ESD			
Max Junction capacitance (IO to GND) GEN1 GEN2	 0.8 0.35	pF	GEN1: e.g., SEMTECH RClamp0524p GEN2: e.g., TPD4E02B04DQA
Footprint	Pad should be on the net – not trace stub		
Location (max length to adjacent discontinuity)	8	mm	Discontinuity is connector, via, or component pad
Common-Mode Choke			
Common-mode impedance @ 100 MHz (Min/Max) GEN1 GEN2	 65/90 5/35	Ω	• Gen1: NFG0QHB542HS2 or others having less Sdd21 • Gen2: the selection priority from the min Sdd21 to the max Sdd21 NFG0QHB542HS2 -> NFG0QHB372HS2 -> NFG0QHB242HS2 -> TCM0605S_120 -> TCM0605S_350 • add CMC for fixing Wi-Fi desense problem - Wi-Fi/BT 2.4G: NFG0QHB242HS2 - Wi-Fi 5.0G: NFG0QHB542HS2 - if issue at both 2.4G and 5G, try NFG0QHB372HS2
Max Rdc	0.3	Ω	
Differential TDR impedance	85 ±15%	Ω @TR-200 ps (10%-90%)	
Min Sdd21 GEN1 GEN2	 ≥ -0.7 @2.5GHz ≥ -1.15 @2.5GHz	 dB @2.5GHz dB @5.0GHz	
Max Scc21 GEN1 GEN2	 ≥ -9.1 @2.5GHz ≥ -29.3 @2.5GHz	 dB @2.5GHz dB @5.0GHz	
Location (close to any adjacent discontinuity)	8	mm	Discontinuity: Connector, via, or other add-on components.
FPC (Additional length of Flexible Printed Circuit Board)			
The FPC routing should be included for PCB trace calculations (max length/delay, etc.)			
Characteristic Impedance	Same as PCB		
Loss characteristic	Strongly recommend being the same as PCB or better		If worse than PCB, the PCB and FPC length (delay) must be re-estimated
Connector			
SMT Connector GND Voiding			GND plane under signal pad should be voided. Size of void should be the same size as the pad.
Connector type			Connector used must be USB-IF certified

Parameter	Requirement	Units	Notes
Notes: 1. Up to four signal Vias can share a single GND return Via 2. Recommend trace length/delay matching to <1ps before Vias or any discontinuity to minimize common mode conversion. 3. Place GND Vias as symmetrically as possible to data pair Vias. 4. Keep critical USB 3.2 traces away from other signals or unrelated power traces/areas or power supply components. 5. If an additional connector is between module and USB connector or other device on the PCB, routing on both sides of that connector should be included for max length and the max length may have to be reduced. 6. If USB3.x path includes a redriver with minimum EQ gain equalizing to 8.1dB, the insertion loss should meet the following requirements to avoid over-equalization and minimum CVM Module loss, which is roughly -2.6dB@5G including on-die; PKG, CVM PCB, and Board-to-Board connector loss is already considered. • -8.4dB@5GHz <TX path pre-channel loss <-6.4dB@5GHz (refer to Figure 7-5 for the path model) • Suggested by redriver suppliers reserving 0.33uF AC cap on RX lanes and 200k PD resistor on RX lanes.			

Figure 7-5. USB3.x Path Model With Redriver



7.1.3 Common USB Routing Guidelines

If routing to USB device or USB connector includes a flex or 2nd PCB, the total routing including all PCBs and flexes must be used for the maximum trace and skew calculations.

Keep critical USB related traces away from other signal traces or unrelated power traces and areas or power supply components.

Table 7-11. Recommended USB Observation Test Points for Initial Boards

Test Points Recommended	Location
One for each of the USB 2.0 data lines (USBx_N/P)	Near Jetson Thor connector and USB device. USB connector pins can serve as test points.
One for each of the USB 3.2 output lines used (TXn_N/P)	Near USB device. USB connector pins can serve as test points.
One for each of the USB 3.2 input lines (RXn_N/P)	Near Jetson Thor connector.

7.2 PCI Express

Jetson Thor provides 12 lanes that can be used for PCIe. Root port is supported on all PCIe interfaces. Endpoint mode is supported on Interfaces C2, C4 and C5 only. For pin descriptions of the RX/TX lanes, see Table 7-1 and Table 7-2. Lane reversal and polarity inversion (P/N swapping) is supported.

Table 7-12. PCIe Clock Pin Descriptions

Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type
F33	UPHY_REFCLK3_N	HS_UPHY1_REFCLK1_N	PCIe output Reference Clock for controller #5.	Bidir	PCIe Diff pair
F32	UPHY_REFCLK3_P	HS_UPHY1_REFCLK1_P			
F25	UPHY_REFCLK1_N	HS_UPHY1_REFCLK2_N	PCIe output Reference Clock for controller #4.	Bidir	PCIe Diff pair
F24	UPHY_REFCLK1_P	HS_UPHY1_REFCLK2_P			
E22	UPHY_REFCLK4_N	HS_UPHY0_REFCLK4_N	PCIe output Reference Clock for controller #3.	Output	PCIe Diff pair
E23	UPHY_REFCLK4_P	HS_UPHY0_REFCLK4_P			
E14	UPHY_REFCLK5_N	HS_UPHY0_REFCLK3_N	PCIe output Reference Clock for controller #2.	Bidir	PCIe Diff pair
F15	UPHY_REFCLK5_P	HS_UPHY0_REFCLK3_P			
D48	UPHY_REFCLK6_N	HS_UPHY0_REFCLK2_N	PCIe Output Reference Clock for controller #1.	Output	PCIe Diff pair
D49	UPHY_REFCLK6_P	HS_UPHY0_REFCLK2_P			

Note: In the Direction column, Output is from Jetson Thor; Input is to Jetson Thor. Bidir is for Bidirectional signals.

Table 7-13. PCIe Control Pin Descriptions

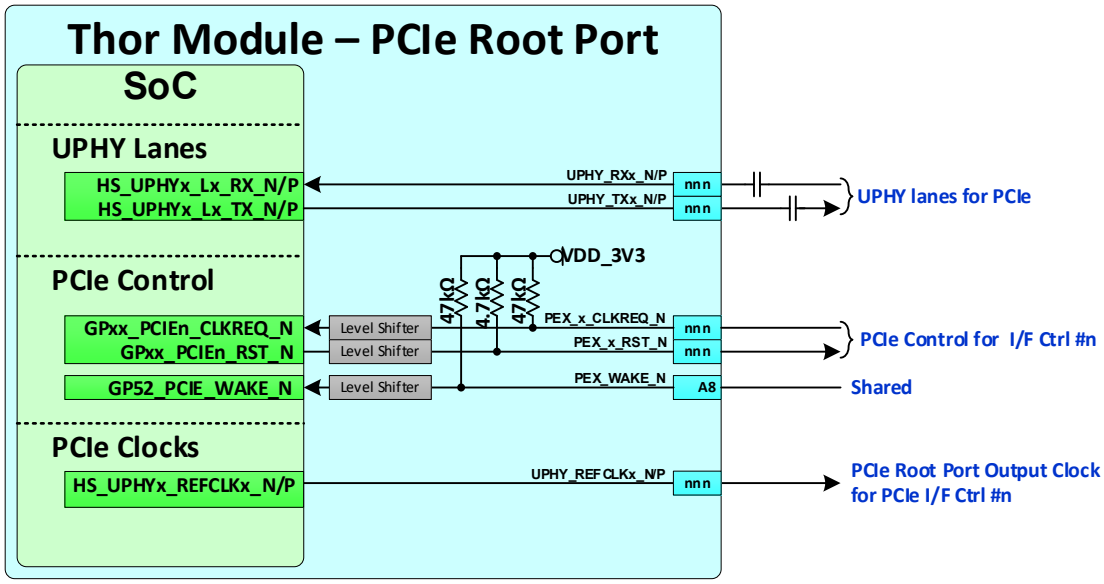
Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type
B37	PEX_C1_CLKREQ_N	GP42_PCIE1_CLKREQ_N	PCIe Clock Request for controller #1. 47KΩ pull-up to 3.3V on module.	Bidir	Open-Drain, 3.3V
E11	PEX_C2_CLKREQ_N	GP44_PCIE2_CLKREQ_N	PCIe Clock Request for controller #2. 47KΩ pull-up to 3.3V on module.	Bidir	
G8	PEX_C3_CLKREQ_N	GP46_PCIE3_CLKREQ_N	PCIe Clock Request for controller #3. 47KΩ pull-up to 3.3V on module.	Bidir	
C8	PEX_C4_CLKREQ_N	GP60_PCIE4_CLKREQ_N	PCIe Clock Request for controller #4. 47KΩ pull-up to 3.3V on module.	Bidir	
L19	PEX_C5_CLKREQ_N	GP62_PCIE5_CLKREQ_N	PCIe Clock Request for controller #5. 47KΩ pull-up to 3.3V on module	Bidir	
B36	PEX_C1_RST_N	GP43_PCIE1_RST_N	PCIe Reset for controller #1. 4.7KΩ pull-up to 3.3V on module.	Output	
D10	PEX_C2_RST_N	GP45_PCIE2_RST_N	PCIe Reset for controller #2. 4.7KΩ pull-up to 3.3V on module.	Output	
J9	PEX_C3_RST_N	GP47_PCIE3_RST_N	PCIe Reset for controller #3. 4.7KΩ pull-up to 3.3V on module.	Output	
H10	PEX_C4_RST_N	GP61_PCIE4_RST_N	PCIe Reset for controller #4. 4.7KΩ pull-up to 3.3V on module.	Output	
L18	PEX_C5_RST_N	GP63_PCIE5_RST_N	PCIe Reset for controller #5. 4.7KΩ pull-up to 3.3V on module.	Output	
A8	PEX_WAKE_N	GP52_PCIE_WAKE_N	PCIe Wake. Wake signal shared by all PCIe interfaces. 47KΩ pull-up to 3.3V on module.	Input	

Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type

Notes:

1. In the Direction column, Output is from Jetson Thor; Input is to Jetson Thor. Bidir is for Bidirectional signals.
2. The direction shown in this table for PEX_Cx_RST_N and PCIE_WAKE_N signals is true when used for those PCIe functions. Otherwise, if used as GPIOs, the direction is bidirectional.

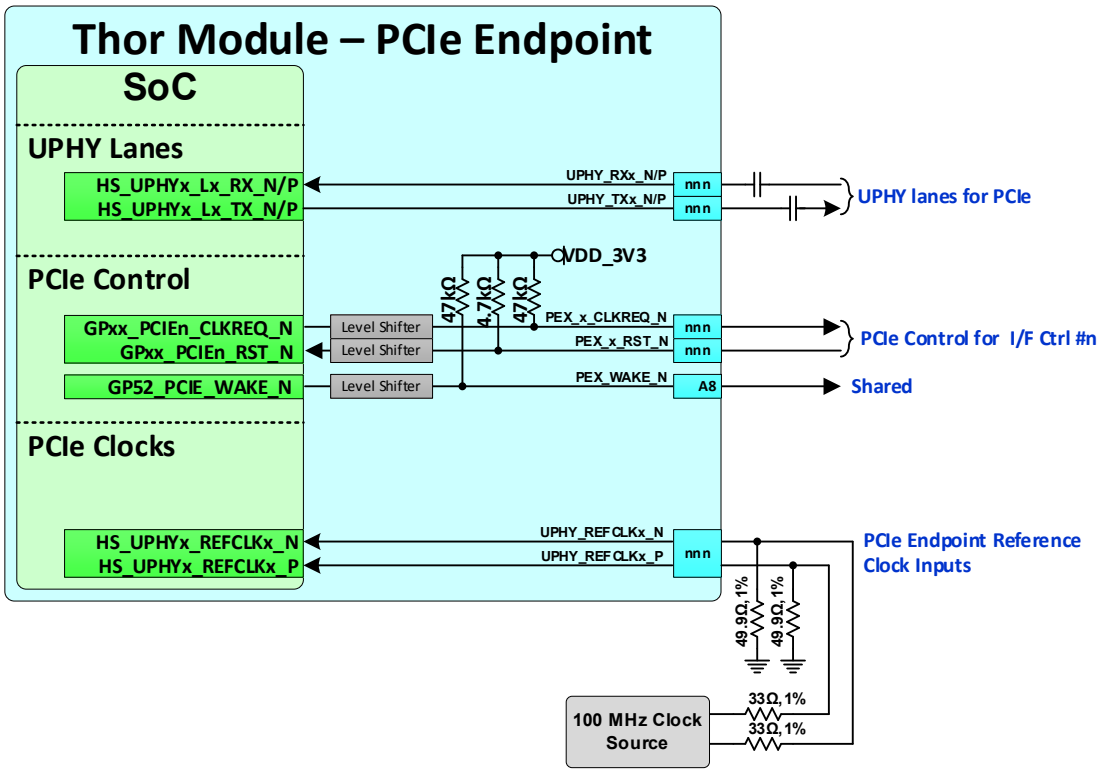
Figure 7-6. PCIe Signal Connections (Root Port)



Notes:

- AC Capacitors required on SoC RX lines (Device TX lines) on carrier board if connected directly to device. They are not placed on the carrier board if connected to a PCIe or M.2 connector. In those cases, the AC caps are on the adapter board plugged into those connectors.
- See design guidelines for correct AC capacitor values.
- The PCIe RX/TX signals comply to the PCIe SIG requirements and are HCSL compatible.
- The PCIe REFCLK inputs and PCIEx_CLK clock outputs comply to the PCIe CEM specification “REFCLK DC Specifications and AC Timing Requirements.” The clocks are HCSL compatible.

Figure 7-7. PCIe Signal Connections (Endpoint)



Notes:

- AC Capacitors required on SoC RX lines (Device TX lines) on carrier board if connected directly to device. They are not placed on the carrier board if connected to a PCIe or M.2 connector. In those cases, the AC caps are on the adapter board plugged into those connectors.
- See design guidelines for correct AC capacitor values.
- The PCIe RX/TX signals comply to the PCIe SIG requirements and are HCSL compatible.
- The PCIe REFCLK inputs and PCIEx_CLK clock outputs comply to the PCIe CEM specification “REFCLK DC Specifications and AC Timing Requirements.” The clocks are HCSL compatible.

Table 7-14. PCIe Signal Connections Module I/Fs Configured as Root Ports

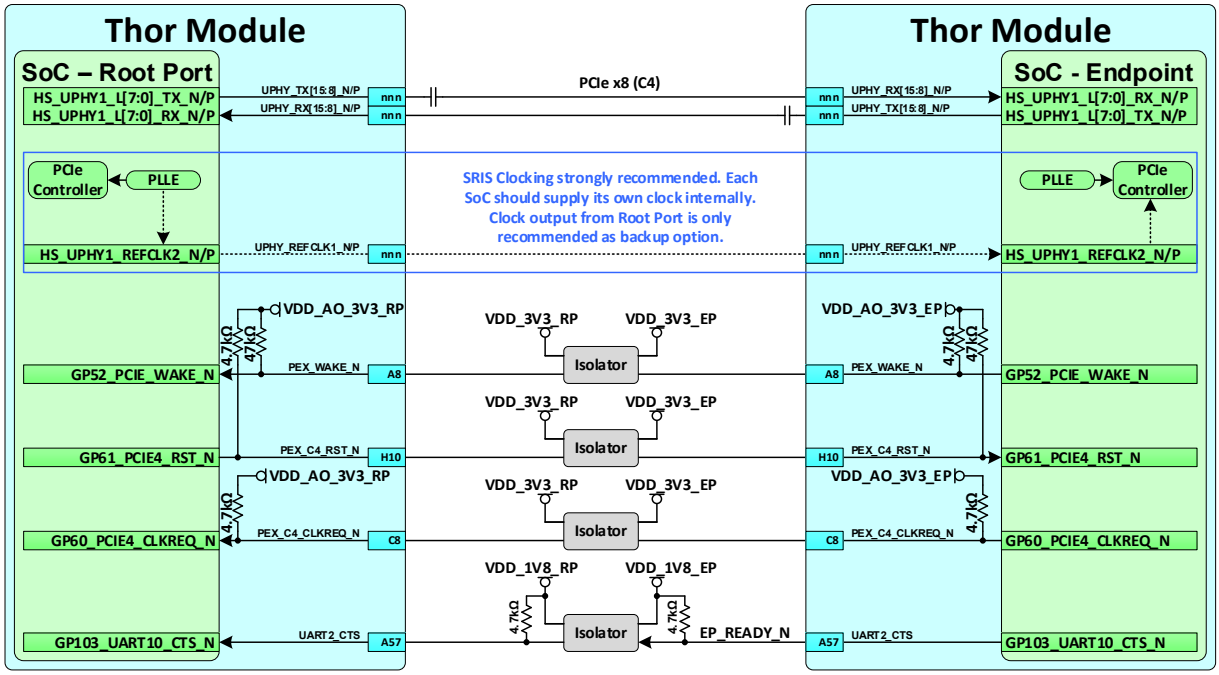
Module Pin Name	Type	Termination	Description
PCIe Interface C1 (x1) – As Root Port (only Root Port Supported)			
UPHY_TX3_P/N (SoC UPHY0 Lane 3)	DIFF OUT	Series Capacitor (see Design Guideline for value)	Differential Transmit Data Pair: Connect to TX_+/– pins of PCIe connector or RX_+/– pins of PCIe device through AC caps.
UPHY_RX3_P/N (SoC UPHY0 Lane 3)	DIFF IN	Series Capacitor (see Design Guideline for value) if device on main PCB.	Differential Receive Data Pair: Connect to RX_+/– pins of PCIe connector or TX_+/– pin of PCIe device through AC caps.
UPHY_REFCLK6_P/N	DIFF OUT	Series capacitors are typically not required. Check Endpoint device requirement.	Differential Reference Clock Output: Connect to REFCLK_+/– pins of PCIe device/connector.
PEX_C1_CLKREQ_N	I	47 kΩ pullup on module to VDD_3V3.	PEX Clock Request for UPHY_REFCLKx: Connect to CLKREQ pin on device/connector(s)
PEX_C1_RST_N	O	4.7 kΩ pullup on module to VDD_3V3.	PEX Reset: Connect to PERST pin on device/connector.
PCIe Interface C2 (Up to x1) – As Root Port			
UPHY_TX4_P/N (SoC UPHY0 Lane 4)	DIFF OUT	Series Capacitor (see Design Guideline for value)	Differential Transmit Data Pair: Connect to TX_+/– pins of PCIe connector or RX_+/– pins of PCIe device through AC caps.
UPHY_RX4_P/N (SoC UPHY0 Lane 4)	DIFF IN	Series Capacitor (see Design Guideline for value) if device on main PCB.	Differential Receive Data Pair: Connect to RX_+/– pins of PCIe connector or TX_+/– pin of PCIe device through AC caps.
UPHY_REFCLK5_P/N	DIFF OUT		Differential Reference Clock Output: Connect to REFCLK_+/– pins of PCIe device/connector.
PEX_C2_CLKREQ_N	I	47 kΩ pullup on module to VDD_3V3.	PEX Clock Request for UPHY_REFCLKx: Connect to CLKREQ pin on device/connector(s)
PEX_C2_RST_N	O	4.7 kΩ pullup on module to VDD_3V3.	PEX Reset: Connect to PERST pin on device/connector.
PCIe Interface C3 (Up to x2) – As Root Port			
UPHY_TX[7:6]_P/N (SoC UPHY0 Lane [7:6])	DIFF OUT	Series Capacitor (see Design Guideline for value)	Differential Transmit Data Pair: Connect to TX_+/– pins of PCIe connector or RX_+/– pins of PCIe device through AC caps.
UPHY_RX[7:6]_P/N (SoC UPHY0 Lane [7:6])	DIFF IN	Series Capacitor (see Design Guideline for value) if device on main PCB.	Differential Receive Data Pair: Connect to RX_+/– pins of PCIe connector or TX_+/– pin of PCIe device through AC caps.
UPHY_REFCLK4_P/N	DIFF OUT		Differential Reference Clock Output: Connect to REFCLK_+/– pins of PCIe device/connector.
PEX_C3_CLKREQ_N	I	47 kΩ pullup on module to VDD_3V3.	PEX Clock Request for UPHY_REFCLKx: Connect to CLKREQ pin on device/connector(s)
PEX_C3_RST_N	O	4.7 kΩ pullup on module to VDD_3V3.	PEX Reset: Connect to PERST pin on device/connector.
PCIe Interface C4 (Up to x8) – As Root Port			
UPHY_TX[15:8]_P/N (SoC UPHY1 Lanes [7:0])	DIFF OUT	Series Capacitor (see Design Guideline for value)	Differential Transmit Data Pair: Connect to TX_+/– pins of PCIe connector or RX_+/– pins of PCIe device through AC caps.
UPHY_RX[15:8]_P/N (SoC UPHY1 Lanes [7:0])	DIFF IN	Series Capacitor (see Design Guideline for value) if device on main PCB.	Differential Receive Data Pair: Connect to RX_+/– pins of PCIe connector or TX_+/– pin of PCIe device through AC caps.

Module Pin Name	Type	Termination	Description
UPHY_REFCLK1_P/N	DIFF OUT		Differential Reference Clock Output: Connect to REFCLK_+/– pins of PCIe device/connector.
PEX_C4_CLKREQ_N	I	47 kΩ pullup on module to VDD_3V3.	PEX Clock Request for UPHY_REFCLKx: Connect to CLKREQ pin on device/connector(s)
PEX_C4_RST_N	O	4.7 kΩ pullup on module to VDD_3V3.	PEX Reset: Connect to PERST pin on device/connector.
PCIe Interface C5 (Up to x4) – As Root Port			
UPHY_TX[11:8]_P/N (SoC UPHY1 Lanes [3:0])	DIFF OUT	Series Capacitor (see Design Guideline for value)	Differential Transmit Data Pair: Connect to TX_+/– pins of PCIe connector or RX_+/– pins of PCIe device through AC caps.
UPHY_RX[11:8]_P/N (SoC UPHY1 Lanes [3:0])	DIFF IN	Series Capacitor (see Design Guideline for value) if device on main PCB.	Differential Receive Data Pair: Connect to RX_+/– pins of PCIe connector or TX_+/– pin of PCIe device through AC caps.
UPHY_REFCLK3_P/N	DIFF OUT		Differential Reference Clock Output: Connect to REFCLK_+/– pins of PCIe device/connector.
PEX_C5_CLKREQ_N	I	47 kΩ pullup on module to VDD_3V3.	PEX Clock Request for UPHY_REFCLKx: Connect to CLKREQ pin on device/connector(s)
PEX_C5_RST_N	O	4.7 kΩ pullup on module to VDD_3V3.	PEX Reset: Connect to PERST pin on device/connector.
Common			
PEX_WAKE_N	I	47 KΩ pullup to VDD_3V3 on Module.	PEX Wake: Connect to WAKE pins on devices or connectors

Table 7-15. PCIe Signal Connections Module I/F Configured as Endpoint

Module Pin Name	Type	Termination	Description
PCIe Interface C2 (Up to x1) – As Endpoint			
UPHY_TX4_P/N (SoC UPHY0 Lanes 4)	DIFF OUT	Series Capacitor (see Design Guideline for value)	Differential Transmit Data Pairs: Connect to TX_+/– pins of PCIe connector or RX_+/– pin of PCIe device through AC caps.
UPHY_RX4_P/N (SoC UPHY0 Lanes 4)	DIFF IN	Series Capacitor (see Design Guideline for value) if device on main PCB.	Differential Receive Data Pairs: Connect to RX_+/– pins of PCIe connector or TX_+/– pin of PCIe device through AC caps.
UPHY_REFCLK5_P/N	DIFF IN	33 Ω series resistors near clock source. 49.9Ω resistors to GND on each line near Endpoint device. AC caps if required by clock source device.	Differential Reference Clock Input: Connect to 100 MHz clock source or REFCLK_+/– pins of PCIe connector.
PEX_C2_CLKREQ_N	O	47 kΩ pullup on module to VDD_3V3.	PEX Clock Request: Connect to CLKREQ pin on device/connector.
PEX_C2_RST_N	I	4.7 kΩ pullup on module to VDD_3V3.	PEX Reset: Connect to PERST pin on device/connector.
PCIe Interface C4 (Up to x8) – As Endpoint			
UPHY_TX[15:8]_P/N (SoC UPHY1 Lanes [7:0])	DIFF OUT	Series Capacitor (see Design Guideline for value)	Differential Transmit Data Pairs: Connect to TX_+/– pins of PCIe connector or RX_+/– pin of PCIe device through AC caps.
UPHY_RX[15:8]_P/N (SoC UPHY1 Lanes [7:0])	DIFF IN	Series Capacitor (see Design Guideline for value) if device on main PCB.	Differential Receive Data Pairs: Connect to RX_+/– pins of PCIe connector or TX_+/– pin of PCIe device through AC caps.
UPHY_REFCLK1_P/N	DIFF IN	33 Ω series resistors near clock source. 49.9Ω resistors to GND on each line near Endpoint device. AC caps if required by clock source device.	Differential Reference Clock Input: Connect to 100 MHz clock source or REFCLK_+/– pins of PCIe connector.
PEX_C4_CLKREQ_N	O	47 kΩ pullup on module to VDD_3V3.	PEX Clock Request: Connect to CLKREQ pin on device/connector.
PEX_C4_RST	I	4.7 kΩ pullup on module to VDD_3V3.	PEX Reset: Connect to PERST pin on device/connector.
PCIe Interface C5 (Up to x4) – As Endpoint			
UPHY_TX[11:8]_P/N (SoC UPHY1 Lanes [3:0])	DIFF OUT	Series Capacitor (see Design Guideline for value)	Differential Transmit Data Pair: Connect to TX_+/– pins of PCIe connector or RX_+/– pins of PCIe device through AC caps.
UPHY_RX[11:8]_P/N (SoC UPHY1 Lanes [3:0])	DIFF IN	Series Capacitor (see Design Guideline for value) if device on main PCB.	Differential Receive Data Pair: Connect to RX_+/– pins of PCIe connector or TX_+/– pin of PCIe device through AC caps.
UPHY_REFCLK3_P/N	DIFF IN		Differential Reference Clock Output: Connect to REFCLK_+/– pins of PCIe device/connector.
PEX_C5_CLKREQ_N	O	47 kΩ pullup on module to VDD_3V3.	PEX Clock Request for UPHY_REFCLKx: Connect to CLKREQ pin on device/connector(s)
PEX_C5_RST_N	I	4.7 kΩ pullup on module to VDD_3V3.	PEX Reset: Connect to PERST pin on device/connector.
Common			
PEX_WAKE_N	O	47 kΩ pullup to VDD_3V3 on Module.	PEX Wake: Unused for interfaces configured as Endpoint

Figure 7-8. PCIe Jetson Thor RP to Jetson Thor EP connection Example



Notes:

- Figure 7-8 is an example showing PCI controller #4 (C4) for both Root Port and Endpoint. Other configurations are possible using PCI controller #2 (C2), or controller #5 (C5) for either the Root Port or Endpoint.
- Recommended Clocking [validation in progress]: SRIS and SRNS
- Using Separate Reference No Spread (SRNS) disables Spread Spectrum Clocking (SSC); thus, the EMI effect with SSC disabled must be considered.
- All side band signals have a level shifter in the module.

Table 7-16. PCIe Signal Connections Jetson Thor RP to Jetson Thor EP

Module Pin Name	Type	Termination	Description
UPHY_TX[15:8]_P/N UPHY_RX[15:8]_P/N (SoC UPHY1 Lanes [7:0])	DIFF OUT	Series Capacitor (see Design Guideline for value)	Differential Transmit/Receive Data Pairs: Connect Jetson Thor Root Port TX pins to Jetson Thor Endpoint RX pins through AC caps. Connect Jetson Thor Endpoint TX pins to Jetson Thor Root Port RX pins through AC caps.
UPHY_REFCLK1_P/N	DIFF OUT		PCIe Reference Clocks (ctrl C4). Connect UPHY_REFCLK1_P/N from Root Port Jetson Thor to UPHY_REFCLK1_P/N of Endpoint Jetson Thor. Back-up if SRIS or SRNS option is used.
UPHY_REFCLK1_P/N	DIFF IN		

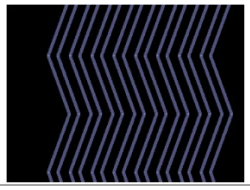
Module Pin Name	Type	Termination	Description
PEX_C4_CLKREQ_N (ctrl C4) Root Port Endpoint	 I O	Isolation between RP and EP (see Figure 7-5).	PCIe Clock Request for PEX_CLK4_P/N (ctrl). Connect to CLKREQ_N pin on each Thor device connected (RP to EP).
PEX_C4_RST_N (ctrl C4) Root Port Endpoint	 O I	Isolation between RP and EP (see Figure 7-5).	PCIe Reset: Connect to RST_N pin on each Thor device connected (RP to EP).
PEX_WAKE_N Root Port Endpoint	 I O	Isolation between RP and EP (see Figure 7-5).	PCIe Wake: Connect to WAKE pin on each THOR device connected (RP to EP).

Note: The table includes mention of only C4. C2 and C5 can also be an Endpoint. If used, the CLKREQ and RST pins associated with that controller would be used. The Endpoint Ready signal can be the one shown for C4 if that controller is not used in this configuration. Alternately, another GPIO (or GPIOs) can be chosen. Any GPIO used should be DD type and tristate at power-on.

7.2.1 PCIe Design Guidelines up to Gen5

The following table details the PCIe design guidelines up to Gen5.

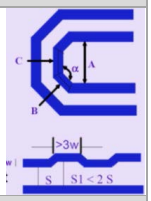
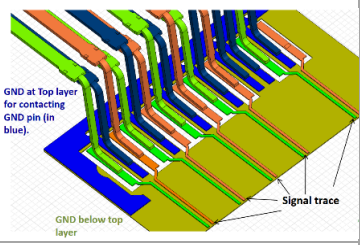
Table 7-17. PCIe Interface Signal Routing Requirements up to Gen5

Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI Period Gen5 Gen4 Gen3	 32.0 / 31.25 16.0 / 62.50 8.0 / 125.00	 Gbps / ps Gbps / ps Gbps / ps	
Topology	Point-point		Unidirectional, differential. Driven by 100MHz common reference clock
Termination	43	Ω	To **GND** Single Ended for P and N
Impedance			
Trace Impedance Differential / Single Ended	 85 / 50	 Ω	±15%
Reference plane	GND		
Fiber-weave effect (Only required for GEN4)	> Use spread-glass (denser weave) instead of regular-glass (sparse weave) to minimize intra-pair skew > Use zig-zag route instead of straight to minimize skew, this is a mandatory for PCIe gen4 design		Example of zig-zag routing 

Parameter	Requirement	Units	Notes
Spacing and IOSI Requirement			
Gen5 and Gen4			
P/N within pair (i.e. intra-pair) skew.	< 0.15 [1]	mm [ps]	Using PCB propagation delay = 160ps/in ~ 0.0062inch guidance. Between P-to-N trace skew.
P/N within pair (i.e. intra-pair) skew between subsequent discontinuities.	< 0.15 [1]	mm [ps]	Using PCB propagation delay = 160ps/in ~ 0.00625inch guidance. Between P-to-N of subsequent discontinuities.
Lane-to-Lane Skew RX-to-RX, TX-to-TX within same Partition (i.e. inter-pair) skew.	< 79.375 [500]	mm [ps]	Using PCB propagation delay = 160ps/in ~ 3.125inch guidance. Between Lane-to-lane within same partition skew.
P/N uncoupled length within pair (i.e. intra-pair).	< 6.5 [40]	mm [ps]	Using PCB propagation delay = 160ps/in ~ 0.25inch guidance. Between P-to-N PCB discontinuities (i.e. via/pad/BGA transitions).
PCB Trace Spacing (Stripline Required).	4x	x dielectric height	Lane-to-Lane (i.e. coplanar)
PCB Noise Coupling Avoidance (Stripline Required).	4x	x dielectric height	To plane/unrelated high-speed signals.
RX-to-TX of same Partition if routed on same layer (Stripline Required).	9x	x dielectric height	Lane-to-Lane (i.e. coplanar)
RX-to-RX, TX-to-TX, RX-to-TX of different Partition if routed on same layer (Stripline Required).	9x	x dielectric height	Lane-to-Lane (i.e. coplanar)
PCB Max BGA Breakout Length	< 6.5 [40]	mm [ps]	Maximum PCB trace length. Using 160ps/in ~ 0.25inch guidance.
PCB Signal Via from BGA	< 6.5 [40]	mm [ps]	Maximum between BGA ball to 1st VIA transition.
Max trace route over VIODS	< 1.27 [8]	mm [ps]	Maximum PCB trace length. Using 160ps/in ~ 0.05inch guidance.
PCB Return Via Proximity (S:G)	< 1x	P/N via pitch	GND via placed < 1x P/N differential pair pitch.
Max VIA Transitions	2	N/A	Use of micro or back-drilled VIA. Do not double-count stacked micro-to-micro or micro-to-core vias.
Max VIA Stub	< 0.38 [15]	mm [mils]	Maximum PTH via stub < 0.015inch with back-drill.
AC Capacitor (i.e. 0402 cap)	0.22	uF	Only required for TX pairs routed to connector. Boards plugging into the connector must implement AC caps on its TX signals.
Max location of AC Capacitor (i.e., 0402 cap) from adjacent discontinuity.	< 8.0 [50]	mm [ps]	Maximum AC cap placement to adjacent discontinuity. Using 160ps/in ~ 0.3125inch guidance.

Parameter	Requirement	Units	Notes
VOID AC capacitor pad discontinuity.	0.1 [4]	mm [mils]	VOID under pad from edge of pad.
Up to Gen3			
P/N within pair (i.e. intra-pair) skew.	< 0.15 [1]	mm [ps]	Using PCB propagation delay = 160ps/in ~ 0.00625inch guidance. Between P-to-N trace skew.
P/N within pair (i.e. intra-pair) skew between subsequent discontinuities.	< 0.15 [1]	mm [ps]	Using PCB propagation delay = 160ps/in ~ 0.00625inch guidance. Between P-to-N of subsequent discontinuities.
Lane-to-Lane Skew RX-to-RX, TX-to-TX within same Partition (i.e. inter-pair) skew.	< 79.375 [500]	mm [ps]	Using PCB propagation delay = 160ps/in ~ 3.125inch guidance. Between Lane-to-lane within same partition skew.
P/N uncoupled length within pair (i.e. intra-pair).	< 6.5 [40]	mm [ps]	Using PCB propagation delay = 160ps/in ~ 0.25inch guidance. Between P-to-N PCB discontinuities (i.e. via/pad/BGA transitions).
PCB Trace Spacing (Stripline/Microstrip).	3x/4x	x dielectric height	Lane-to-Lane (i.e. coplanar)
PCB Noise Coupling Avoidance (Stripline/Microstrip).	3x/4x	x dielectric height	To plane/unrelated high-speed signals.
RX-to-TX of same Partition if routed on same layer (Stripline/Microstrip).	9x/12x	x dielectric height	Lane-to-Lane (i.e. coplanar)
RX-to-RX, TX-to-TX, RX-to-TX of different Partition if routed on same layer (Stripline/Microstrip).	9x/12x	x dielectric height	Lane-to-Lane (i.e. coplanar)
PCB Max BGA Breakout Length	< 6.5 [40]	mm [ps]	Maximum PCB trace length. Using 160ps/in ~ 0.25inch guidance.
PCB Signal Via from BGA	< 6.5 [40]	mm [ps]	Maximum between BGA ball to 1st VIA transition.
Max trace route over VIODS	< 1.27 [8]	mm [ps]	Maximum PCB trace length. Using 160ps/in ~ 0.05inch guidance.
PCB Return Via Proximity (S:G)	< 1x	P/N via pitch	GND via placed < 1x P/N differential pair pitch.
Max VIA Transitions	2	N/A	Use of micro or back-drilled VIA. Do not double-count stacked micro-to-micro or micro-to-core vias.
Max VIA Stub	< 0.38 [15]	mm [mils]	Maximum PTH via stub < 0.015inch with back-drill.
AC Capacitor (i.e. 0402 cap)	0.22	uF	Only required for TX pairs routed to connector. Boards plugging into the connector must implement AC caps on its TX signals.
Max location of AC Capacitor (i.e. 0402 cap) from adjacent discontinuity.	< 8.0 [50]	mm [ps]	Maximum AC cap placement to adjacent discontinuity. Using 160ps/in ~ 0.3125inch guidance.

Parameter	Requirement	Units	Notes
VOID AC capacitor pad discontinuity.	0.1 [4]	mm [mils]	VOID under pad from edge of pad.
Insertion Loss and Max Length			
Gen5			
Total Loss Budget	36	dB	End to End
Thor Module to Thor Module Remaining Budget for Carrier B'd Max Length Thor Module to Direct Devices Remaining Budget for Carrier B'd Max Length Thor Module to Connector Remaining Budget for Carrier B'd Max Length	 21.8 221 (1395) 27.8 282 (1779) 17.9 181 (1145)	 dB mm (ps) dB mm (ps) dB mm (ps)	Insertion Loss: - Thor module: -7.1 dB - CEM connector: -1.5 dB - Add-in Card: -9.5 dB - Direct Device: -1.1 dB (using Thor SoC for reference) Max Length: Using estimated dB/in model (i.e. EM370(Z) = -2.5 dB/in @ 16 GHz parameter.
Gen4			
Total Loss Budget	28	dB	End to End
Thor Module to Thor Module Remaining Budget for Carrier B'd Max Length Thor Module to Direct Devices Remaining Budget for Carrier B'd Max Length Thor Module to Connector Remaining Budget for Carrier B'd Max Length	 20.4 370 (2331) 23.5 426 (2685) 14.7 266 (1680)	 dB mm (ps) dB mm (ps) dB mm (ps)	Insertion Loss: - Thor module: -3.8 dB - CEM connector: -1.5 dB - Add-in Card: -8.0 dB - Direct Device: -0.7 dB (using Thor SoC for reference) Max Length: Using estimated dB/in model (i.e. EM370(Z) = -1.4 dB/in @ 16 GHz parameter.
Gen3			
Total Loss Budget	20	dB	End to End
Thor Module to Thor Module Remaining Budget for Carrier B'd Max Length Thor Module to Direct Devices Remaining Budget for Carrier B'd Max Length Thor Module to Connector Remaining Budget for Carrier B'd Max Length	 15.2 429 (2702) 17.1 482 (3040) 9.4 265 (1670)	 dB mm (ps) dB mm (ps) dB mm (ps)	Insertion Loss: - Thor module: -2.4 dB - CEM connector: -1.7 dB - Add-in Card: -6.5 dB - Direct Device: -0.5 dB (using Thor SoC for reference) Max Length : Using estimated dB/in model (i.e. EM370(Z) = -0.9 dB/in @ 16 GHz parameter.

Parameter	Requirement	Units	Notes
Serpentine (See USB 3.2 Guidelines)			
Min bend angle	135	deg (a)	S1 must be taken care in order to consider Xtalk to adjacent pair 
Dimension Min A Spacing Min B, C Length Min Jog Width	 4x 1.5x 3x	Trace width	
Miscellaneous			
GND fill rule	Remove unwanted GND fill that is either floating or act like antenna		
Connector			
Voiding	Void all layers of golden finger area under the pad ~0.15mm larger than the pad size is recommended.		
Keep critical PCIe traces such as PEX_TX/RX, etc. away from other signal traces or unrelated power traces/areas or power supply components			

Note: The trace length/delay for "Direct to device" does not account for the losses of the end device loss and any connectors involved. The loss should first be adjusted by subtracting the end device/connector losses. The length/delay may also need to be adjusted if the PCB material loss is different than the EM-370(Z) PCB material assumed.

Figure 7-9. Insertion Loss S-Parameter Plot (DES21)

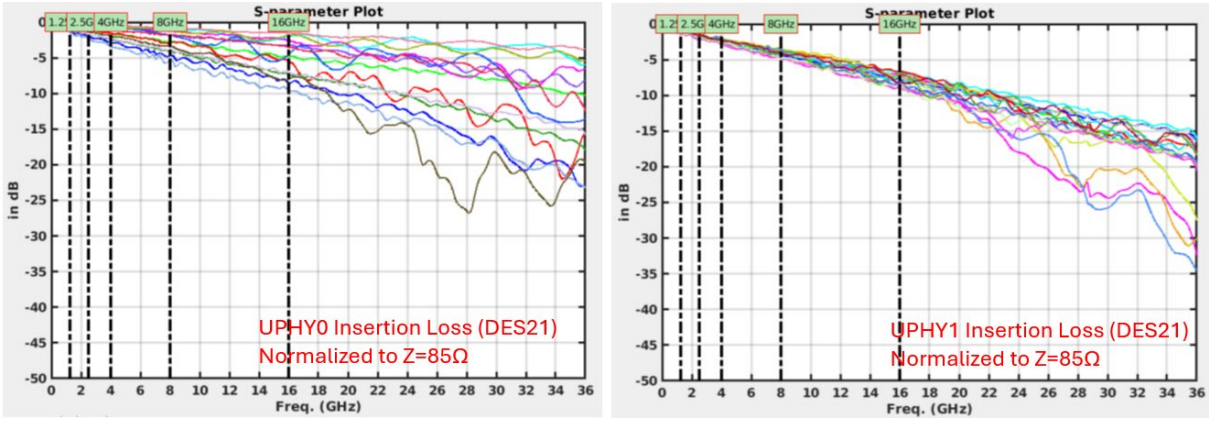


Table 7-18. Recommended PCIe Observation Test Points for Initial Boards

Test Points Recommended	Location
One for each of the PCIe TX_+/– output lines used.	Near PCIe device. Connector pins may serve as test points if accessible.
One for each of the PCIe RX_+/– input lines used.	Near Jetson Thor connector.

7.2.2 Ethernet via PCIe

The Jetson Thor provides an Ethernet interface to support 5 Gigabit Ethernet functionality via PCIe Network Interface Controller (NIC). As shown in Figure 8-1 and Figure 8-2, the Ethernet PHY, magnetics, and RJ45 connector are not included on the module and must be implemented externally to the module.

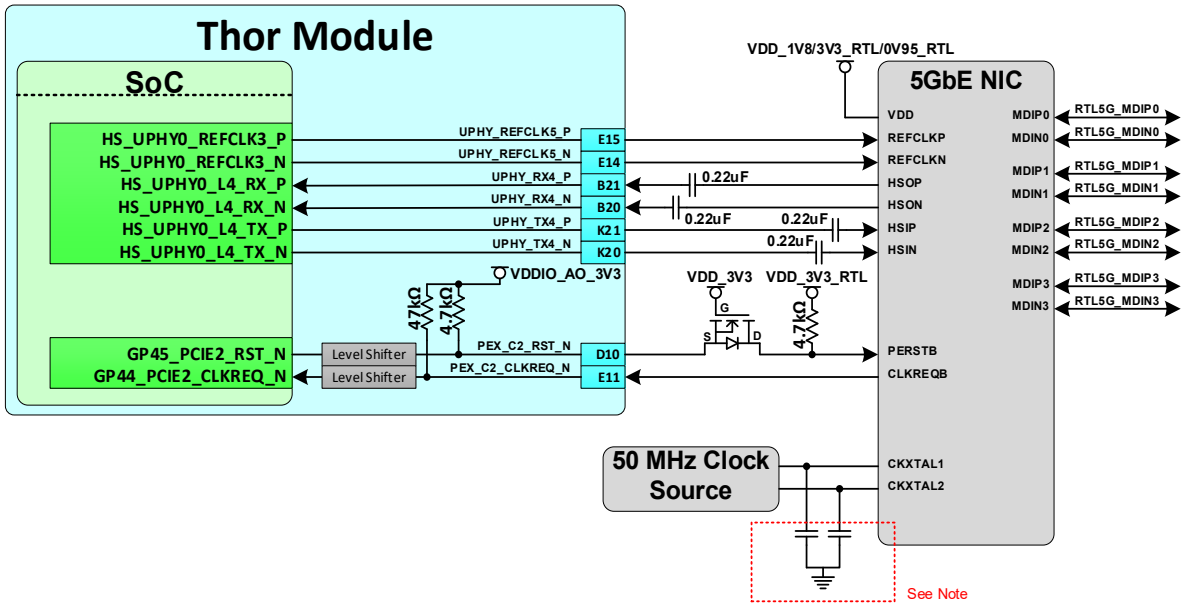
Note: This Chapter uses PCIe Controller 2 (C2) as a reference, however, using a different port is acceptable.

Table 7-19. Jetson Thor Module Gigabit Ethernet Pin Descriptions

Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type
E15	UPHY_REFCLK5_P	HS_UPHY0_REFCLK3_P	PCIe output Reference Clock for controller #2	Output	PCIe Diff Pair
E14	UPHY_REFCLK5_N	HS_UPHY0_REFCLK3_N	PCIe output Reference Clock for controller #2	Output	PCIe Diff Pair
B21	UPHY_RX4_P	HS_UPHY0_L4_RX_P	Differential Receive Data Pair: Connect to RX_+/– pins of PCIe connector or TX_+/– pin of PCIe device through AC caps.	Input	PCIe Diff Pair
B20	UPHY_RX4_N	HS_UPHY0_L4_RX_N	Differential Receive Data Pair: Connect to RX_+/– pins of PCIe connector or TX_+/– pin of PCIe device through AC caps.	Input	PCIe Diff Pair
K21	UPHY_TX4_P	HS_UPHY0_L4_TX_P	Differential Transmit Data Pair: Connect to TX_+/– pins of PCIe connector or RX_+/– pins of PCIe device through AC caps.	Output	PCIe Diff Pair
K20	UPHY_TX4_N	HS_UPHY0_L4_TX_N	Differential Transmit Data Pair: Connect to TX_+/– pins of PCIe connector or RX_+/– pins of PCIe device through AC caps.	Output	PCIe Diff Pair
D10	PEX_C2_RST_N	GP45_PCIE2_RST_N	PCIe Reset for controller #2. 4.7KΩ pull-up to 3.3V on module.	Output	Open-Drain, 3.3V
E11	PEX_C2_CLKREQ_N	GP44_PCIE2_CLKREQ_N	PCIe Clock Request for controller #2. 47KΩ pull-up to 3.3V on module.	Input	Open-Drain, 3.3V

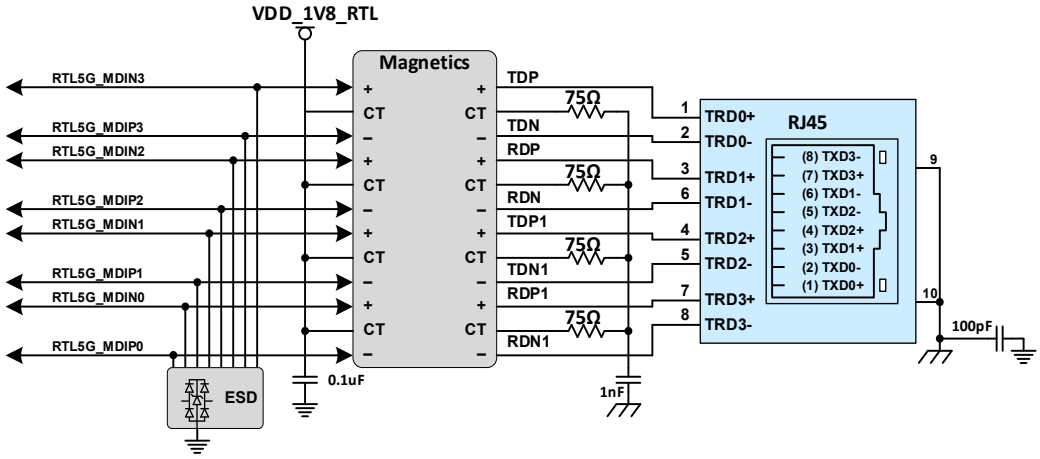
Note: In the Direction column, Output is from Jetson Thor; Input is to Jetson Thor. Bidir is for Bidirectional signals.

Figure 7-10. Ethernet Connections



Note: The load capacitance should be decided considering the actual crystal characteristics and layout parasitic capacitance.

Figure 7-11. Ethernet Magnetics and RJ45 Connections



Notes:

- The connections in Figure 7-11 match those used on the carrier board and are shown for reference only.
- Refer to the *Jetson Thor Developer Kit Carrier Board Reference Design Files* for linked status LED connection.

Table 7-20. Ethernet Signal Connections

Module Pin Name	Type	Termination	Description
UPHY_REFCLK5_P/N	O		Ethernet Reference Clock: Connect to REFCLKP/N pins on GbE Transceiver.
UPHY_RX4_P/N	I	Series Capacitor (see Design Guideline for value) if device on main PCB.	Ethernet Data Receiver: Connect, through AC caps, to HSOP/N pins on GbE Transceiver.
UPHY_TX4_P/N	O	Series Capacitor (see Design Guideline for value).	Ethernet Data Transmitter: Connect, through AC caps, to HSIP/N pins on GbE Transceiver.
PEX_C2_RST_N	I	4.7 kΩ pullup on module to VDDIO_AO_3V3	Ethernet Reset: Connect, through FET and pull-up, to PERSTB pin on GbE Transceiver.
PEX_C2_CLKREQ_N	I	47 kΩ pullup on module to VDDIO_AO_3V3	Ethernet Clock Request: Connect to CLKREQB pin on GbE Transceiver.

Note: Refer to the relevant device manufacturer guidelines for correct connections from the SoC input and output clock, data, control to device.

7.3 MGBE

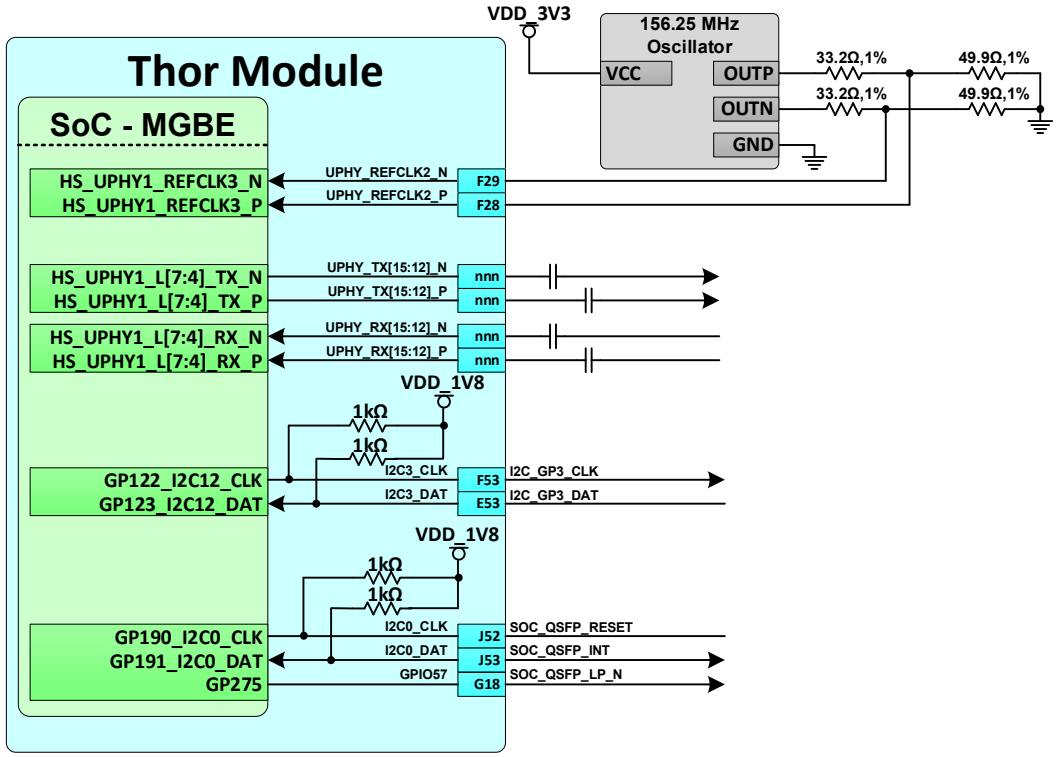
The Jetson Thor integrates advanced Multi-Gigabit Ethernet (MGBE) controllers, which support high-speed communication with external devices such as Ethernet PHYs and switches. These connections can be established via XFI differential lines, enabling line rate of 2.5 Gbps, 5 Gbps and 10 Gbps, or through 25GAUI differential lanes for up to 4x 25 Gbps performance. The MGBE controllers are designed to deliver robust and scalable networking capabilities, making them ideal for high-bandwidth applications.

The figure below shows an example of an MGBE connection.

Notes:

- The MGBE controller may be referred to as 10-Gigabit Ethernet (10GbE) or 25-Gigabit Ethernet (25GbE). Contact your NVIDIA Applications Engineering team for further details.
- Four MGBE can run at 2.5/5/10 Gbps or 25 Gbps [validation in progress]. Note that MGBE at 25 Gbps requires all controllers to be at the same speed. If MGBE is not at 25 Gbps, controllers can be a combination of 2.5/5/10 Gbps.

Figure 7-12. QSFP Connection Example



Note: See Table 7-21 for correct AC capacitor values.

Table 7-21. MGBE Signal Connections

Pin #	Module Pin Name	Type	Termination	Description
D28/D29	UPHY_RX12_P/N	DIFF IN	100nF	MGBE0 RX differential signal: Connect to TX_P/N of external PHY/Switch device through AC caps
H28/H29	UPHY_TX12_P/N	DIFF OUT	100nF	MGBE0 TX differential signal: Connect to RX_P/N of external PHY/Switch device through AC caps
B29/B28	UPHY_RX13_P/N	DIFF IN	100nF	MGBE1 RX differential signal: Connect to TX_P/N of external PHY/Switch device through AC caps
K29/K28	UPHY_TX13_P/N	DIFF OUT	100nF	MGBE1 TX differential signal: Connect to RX_P/N of external PHY/Switch device through AC caps
C31/C30	UPHY_RX14_P/N	DIFF IN	100nF	MGBE2 RX differential signal: Connect to TX_P/N of external PHY/Switch device through AC caps

Pin #	Module Pin Name	Type	Termination	Description
G31/G30	UPHY_TX14_P/N	DIFF OUT	100nF	MGBE2 TX differential signal: Connect to RX_P/N of external PHY/Switch device through AC caps
A30/A31	UPHY_RX15_P/N	DIFF IN	100nF	MGBE3 RX differential signal: Connect to TX_P/N of external PHY/Switch device through AC caps
J30/J31	UPHY_TX15_P/N	DIFF OUT	100nF	MGBE3 TX differential signal: Connect to RX_P/N of external PHY/Switch device through AC caps
F28/F29	UPHY_REFCLK2_P/N	DIFF IN		MGBE Reference Clock: Connect to external 156.25 MHz oscillator specified in Table 7-22. Refer to Figure 7-12 for connection details.

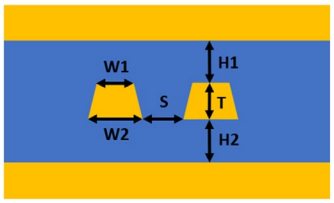
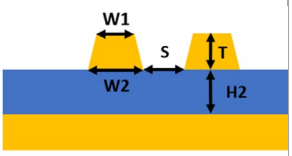
Table 7-22. MGBE Interface Reference Clock Oscillator Requirements

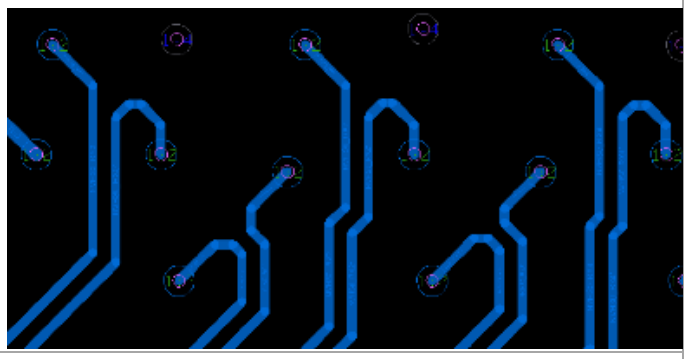
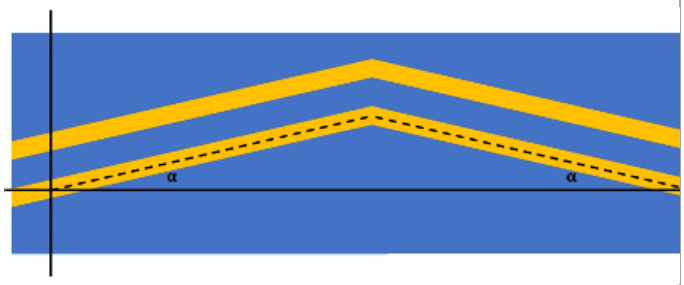
Parameter	Min	Typ	Max	Unit	Condition
Output Frequency		156.250000		MHz	
Output Driver Type		HCSL			
Frequency Stability	-100	–	+100	ppm	Inclusive of initial tolerance, aging, operating temperature, rated power supply voltage and load variations.
L_100k		-120		dBc/Hz	Phase noise at 100 kHz (typical value given for reference)
Duty Cycle	45	–	55	%	
JITrefclk	–	0.5	1.2	ps	Integrate from 12 kHz to 20 MHz
AMPrefclk	0.3	-	1.8	Vppd	Differential Voltage Swing
VCMrefclk	0.25		0.55	Vcm	Common mode
TRrefclk	0.2	1	2	ns	Rise/Fall time, 10 to 90%
Zdiff_reclk	78	85	105	Ohm	Differential trace impedance
Zcm_refclk	22.5	25	27.5	Ohm	CM trace impedance

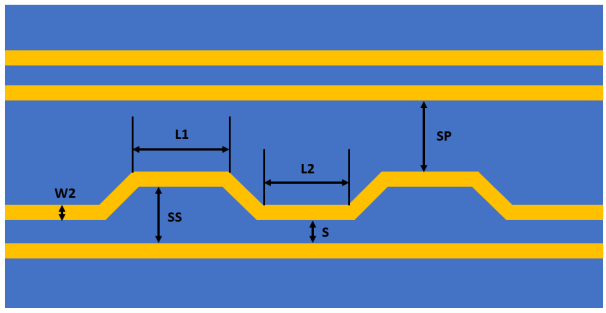
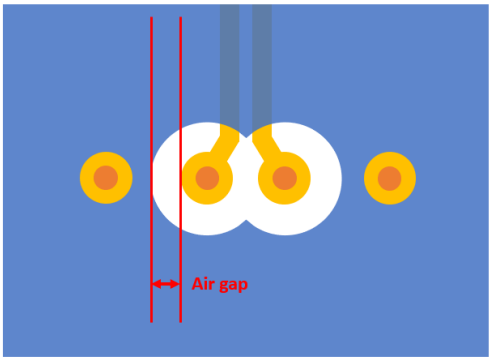
7.3.1 10 GbE MGBE Design Guidelines

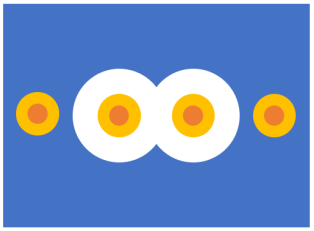
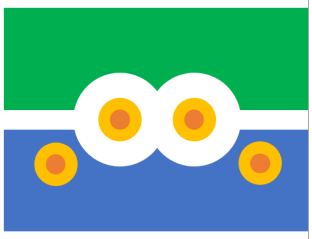
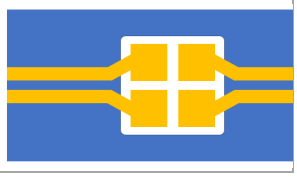
Table 7-23. MGBE 10GbE Interface Signal Routing Requirements

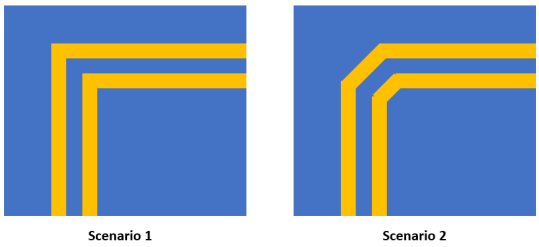
Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI Period	10 / 100	Gbps / ps	Exact baud rate 10.3125GBd NRZ
Configuration / Device Organization	1	Load	

Parameter	Requirement	Units	Notes
Topology	Point-point		Unidirectional, differential
Termination	85 differential	Ω	On-die termination at TX
Transmission line	Stripline		See note 1
Impedance Control			
Trace Impedance (differential)	85	Ω	See note 2
Reference plane	GND		Ground reference should be solid. Referencing to power plane or partial ground plane (some portion is power plane and some portion is ground plane) is not allowed under any circumstance.
Spacing			
Minimum Trace Spacing (Stripline/MS) between: TX and RX pairs TX/RX. Pairs and unrelated High-Speed structures TX/RX pairs and other Low-Seed structures TX/RX pairs and edge of reference plane TX/RX pairs and power structures (plane, via or traces)	7x / 10x 9x / 12x 7x / 10x 4x / 8x 7x / 10x	Equivalent Dielectric Height (see below)	Route TX and RX on separate layers whenever possible. See note 3 and note 4. For spacing between TX and RX pairs, refer to note 8 when using 2.5Gpbs and/or 5Gbps speeds only.
Equivalent Dielectric Height (HE) is to be used in case of asymmetric stripline, having heights H1 and H2, where H1 > H2	$HE = \left(0.0041\left(\frac{H1}{H2}\right)^3 - 0.1306\left(\frac{H1}{H2}\right)^2 + 1.4397\frac{H1}{H2} + 1.6583\right) \times \frac{H2}{3}$		
Trace coupling ratio CR	$CR = \frac{S}{min(H1,H2)}$ for stripline $CR = \frac{S}{H2}$ for microstrip		Main route should comply to CR > 1.5. This is a general good practice to avoid very thin trace.
	 *Stripline*		 *Microstrip*
Length and Skew			
Breakout region (Maximum Length)	41.9	ps	
Max trace length	150	mm	See note 5
Channel loss (not including SoC package loss)	6.0	dB @5.5GHz	See note 6
Max PCB via distance from the BGA	41.9	ps	Maximum distance from BGA ball to first PCB via.

Parameter	Requirement	Units	Notes
PCB within pair (intra-pair) skew	≤ 0.13 (1)	mm (ps)	Do trace length matching before hitting discontinuities. See note 7.
Differential pair uncoupled total length	10	mm	
	Form a differential pair as soon as possible when the route starts. Below is an illustration: 		
Fiber-weave compensation	To minimize intra-pair skew, the following is recommended: • Use spread-glass (denser weave) PCB material instead of regular-glass (sparse weave). • Zig-zag should be used instead of straight routing. The angle (α) of the zig-zag routing should be higher than or equal to 10 degrees.		
	Example of zig-zag routing: 		
Serpentine geometry	The serpentine geometry is shown on the right-side figure and must satisfy the following: $L1 \geq 3 \times W2$ $L2 \geq 1.5 \times L1$ $SS \leq 2 \times S$ SP should comply to the main routing spacing rule.		

Parameter	Requirement	Units	Notes
	Example of serpentine geometry: 		
Via			
GND vias placement	Place **GND** vias as symmetrically as possible to data pair vias. There should be at least one GND via associated with one signal via of a differential pair. **GND** via should be placed less than 1x the diff pair via pitch.		
Max # of layer transitions for TX/RX	4		Do not count connection between micro-vias or micro-vias and core vias in High-Density Interconnect (HDI) designs as layer transition.
Max via stub length	0.3	mm	• Longer via stubs would require review. • Backdrill recommended for PTH stack-up, unless the impedance target can be satisfied without it.
Via void	• For Plated Through Hole (PTH) design: void all layers in the stack-up. • For HDI design: void all signaling layers, including area under (or above) the transition layer via pad.		
Via air gap	As good practice, the air gap (distance between the edge of the pad and the boundary of the void as is shown below) can be around 0.25mm (it may be adjusted based on the stack-up and impedance simulation results). 		

Parameter	Requirement	Units	Notes
Via pad	Only on component layer (top or bottom) and signal layer. Pad on other layers are considered as non-functional pad (NFP) and should be avoided.		
Via reference plane	Vias should only reference to one type of plane, e.g., GND plane (or power plane, which is not recommended) as shown in Scenario 1 below. Referencing vias to partial plane or multiple planes (see Scenario 2) is not recommended.  Scenario 1  Scenario 2		
Stitching vias (via fence)	Recommended for better isolation in case main route of TX/RX pair is close to other signals and signal to signal spacing is marginal.		
AC Capacitor			
Value	100	nF	AC coupling capacitors should be placed close to either the receiving or transmitting device.
Maximum distance from RX/TX BGA pad (discontinuity)	6.5	mm	
Voiding	Voiding the plane directly under the pad 3-4 mils larger than the pad size is recommended.		Example of void under the capacitor pad: 

Parameter	Requirement	Units	Notes
Miscellaneous			
Conductor bends	The bending corner should be either rounded or bevel, as shown in Scenario 2 below. Routing with 90 degrees (Scenario 1) is not accepted. 		
Routing signals over void, pad, and antipads	Not allowed under any circumstance		

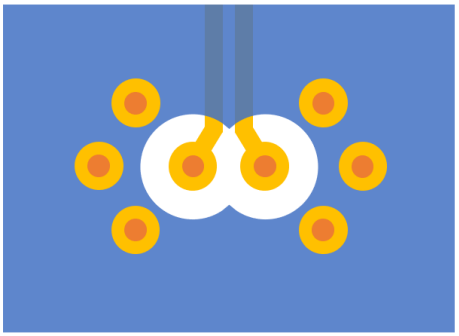
Notes:

1. Stripline routing is strongly recommended for better crosstalk performance. The two reference planes of the stripline should be solid ground layer. Microstrip routing is to be used for breakout region (usually connecting AC cap). If microstrip is needed for the entire channel, tighter trace-to-trace spacing spec should be applied. Work with your NVIDIA Applications Engineer for further details.
2. For the main route, if 100Ω is not achievable due to stack-up limitation, the target impedance can be relaxed to 95Ω or 85Ω. This is possible because NVIDIA UPHY pads are 85Ω. Remaining routing such as breakdown and connector areas can be relaxed to 85Ω~110Ω.
3. If routing on different layers are not applicable due to other routing constraints, routing TX and RX pairs on the same layer is acceptable if the separation between these pairs are at least 7x and 10x for stripline and microstrip respectively.
4. If components at both ends of the channel are placed on the same layer (e.g., all on top layer or all on bottom layer), RX routing layer should be the layer closer to component placement layer while TX routing layer can be further from the component placement layer (e.g., components all on top layer, RX on L3, TX on L5).
5. The maximum Trace Length has been defined by considering a maximum PCB loss budget of 6dB @ 5.5GHz (including vias and connector loss) and typical PCB material having a trace loss of less than 1.0dB/in @ 5.5GHz. If traces with higher loss and/or connectors are used, the maximum trace length may have to be adjusted accordingly to ensure that maximum PCB loss budget is not exceeded. Moreover, if a connector is used, the routing on both sides of that connector should be included for the maximum Trace Length calculation.
6. Channel loss (including connector – if any) should comply with INF-8077i – 2005 from SFF Committee – i.e., 6.0dB@5.5GHz. Contact your NVIDIA Applications Engineering Team for further details.
7. Include only PCB trace lengths/delays for Differential P/N matching. The SoC package delays for differential signal pairs are adequately matched. Do length matching before via transitions to different layers or any discontinuity to minimize common mode conversion.
8. In case recommended spacing between TX and RX pairs cannot be met for designs that do not require 10Gbps speeds, that spacing could be relaxed to 6x/7x for stripline/microstrip routing cases, respectively.

7.3.2 25 GbE MGBE Design Guidelines

Most of the routing requirements for MGBE 10GbE Interface Signals listed in Table 7-23 are also applicable to MGBE 25GbE routing. The only differences to be considered are listed in Table 7-24 below.

Table 7-24. MGBE 25GbE Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Data rate / UI period	25 / 40	Gbps / ps	Exact baud rate 25.78125GBd NRZ
Impedance Control			
Trace impedance (differential)	85	Ω	Intrinsic Zdiff, does not account for coupling from other trace pairs and Etch angle = 80°
Spacing			
Minimum trace spacing (Stripline) between: TX and RX pairs TX/RX pairs and unrelated High-Speed structures TX/RX pairs and other Low-Speed structures TX/RX pairs and edge of reference plane TX/RX pairs and power structures (plane, via or traces)	 16x 16x 16x 7x 7x	 Equivalent Dielectric Height (see definition in Table 1-4)	TX and RX must be routed on separate layers.
Length and Skew			
Maximum PCB loss budget	11.6	dB @12.5GHz	See Note 1
Maximum trace length	128	mm	Just for reference. See Note 2.
Differential pair uncoupled total length	41.9	ps	
Via			
GND vias placement	Place **GND** vias as symmetrically as possible to data pair vias. There should be at least three GND via associated with one signal via of a differential pair. **GND** via should be placed less than 1x the diff pair via pitch. 		

Parameter	Requirement	Units	Notes
Maximum via stub Length	0	mm	No via stub allowed
Maximum # of layer transitions for TX/RX	2		Do not count connection between stacked micro-vias or micro-vias and core vias (vertically aligned) in HDI designs as layer transition.

Notes:

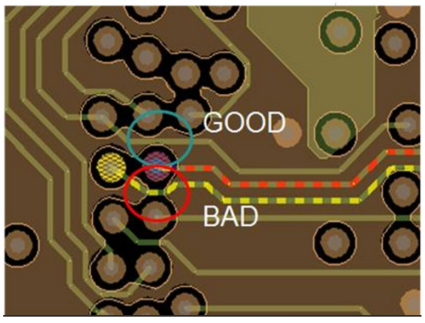
1. **The maximum PCB loss is the net loss budget left for the PCB traces routing. It does not account for losses created by connectors or additional elements along the PCB traces. If such elements are added to the PCB traces, the PCB loss budget must be adjusted accordingly. Contact your NVIDIA Applications Engineering team for further details.**
2. **The given maximum trace length is defined based on the maximum PCB loss budget while considering a PCB material EM370z(FR4) with 2.3dB/in losses at 12.5GHz. If PCB material with different losses is used, maximum trace length shall be adjusted accordingly. Contact your NVIDIA Applications Engineering team for further details.**

7.3.3 Reference Clock Oscillator Requirements

This section describes the design guidelines for MGBE Reference Clock, including routing requirements, as well as guidelines for supporting the oscillator selection.

Most of the routing requirements for MGBE Interface Signals listed in Table 7-23 and Table 7-24 are also applicable to MGBE Reference Clock routing. The only differences to be considered are listed in Table 7-25 below.

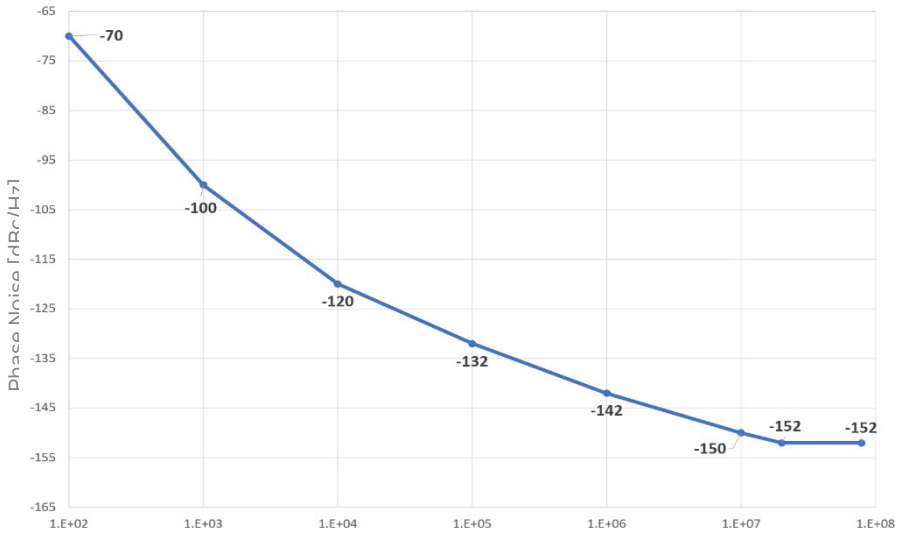
Table 7-25. MGBE Reference Clock Routing Requirements

Parameter	Requirement	Units	Notes
Trace impedance: Zcm (Common mode) Zdiff (Differential)	 25 100	 Ω	 ± 10%
Avoid routing over voids in the GND reference in the ball-out area. The figure to the right shows a “GOOD” example, where the GND continues between the BGA balls with the Reference Clock routing staying over the GND. Avoid the “BAD” example, where the GND has a break and the signal passes over this break (or void).			

Note: Reference Clock routing as microstrip carries EMI risk, which can be mitigated with suitable enclosure design.

The requirements for selecting MGBE Reference Clock Oscillator are listed in Table 7-26. They apply for all speeds supported by NVIDIA's Thor MGBE Interface.

Table 7-26. MGBE Interface Reference Clock Oscillator Requirements

Parameter	Min	Typ	Max	Unit	Condition
Output frequency		156.250000		MHz	
Output driver type		HCSL			
Frequency stability	-100	–	+100	ppm	Including initial tolerance, aging, operating temperature, rated power supply voltage and load variations.
Duty cycle	45	–	55	%	
Phase noise mask (See Notes 1 and 2)					
Integrated jitter mask (See Note 3)	–	-	622.2	fs	Integrated from 1kHz to 78MHz
	–	-	254.7	fs	Integrated from 12kHz to 1MHz
	–	-	345.6	fs	Integrated from 12kHz to 20MHz
	–	-	442.2	fs	Integrated from 12kHz to 78MHz
	–	-	275.9	fs	Integrated from 20MHz to 78MHz
AMPrefclk	0.3	-	1.6	Vppd	Differential voltage swing
VCMrefclk	0.25		0.55	Vcm	Common mode
TRrefclk	0.2	1	2	ns	Rise/Fall time, 10 to 90%

Notes:

1. **The phase noise may be relaxed in case only 10G (or lower speeds) are used by MGBE. Contact your NVIDIA Applications Engineering team for further details.**
2. **The phase noise mask does not include the spurs. The power sum of all spurs should not be more than -67dBc.**
3. **The integrated jitter (including spur) of the select crystal/oscillator shall not exceed the given integrated jitter mask.**

7.3.4 Camera Over Ethernet

Camera over Ethernet (CoE) is a protocol that encapsulates raw camera pixel data into Ethernet packets. When combined with the Multi GigaBit Ethernet (MGBE) engine, it provides a high bandwidth transport media that allows sensor data to bypass the CPU and be directly transferred into GPU memory. NVIDIA's Holoscan Sensor Bridge (HSB) leverages the CoE protocol to offer a highly configurable and user-friendly solution for sensor data transmission. For more details, refer to the HSB User Guide.

Chapter 8. Storage

Jetson Thor supports external storage for OS and user data.

- NVMe through PCIe
  - PCIE C1, x1 (UPHY0 Lane [3])
  - PCIE C2, x1 (UPHY0 Lane [4])
  - PCIE C3, x2 (UPHY0 Lanes [7:6]) or x1 (UPHY Lane [6])
  - PCIe C4, x4 (UPHY1 Lanes [3:0]) or x2 (UPHY1 Lanes [1:0]) or x1 (UPHY1 Lane [0])
  - PCIE C5, x4 (UPHY1 Lanes [3:0]) or x2 (UPHY1 Lanes [1:0]) or x1 (UPHY1 Lane [0])
- SSD through USB 3.2
  - USB 3.2 Port 0, 1, or 2

Chapter 9. Display

Jetson Thor supports a standard DP 1.4 or HDMI™ v2.1 interface. They share the same set of interface pins, so either DisplayPort or HDMI can be supported natively. Multi-head support through MST is included. Refer to the *NVIDIA Jetson Thor Module Data Sheet* for the maximum resolutions supported.

Notes:
1. MST is only supported on DisplayPort.
2. Embedded DisplayPort (eDP) support is removed starting in v0.9.

Table 9-1. Jetson Thor HDMI and DP Pin Description

Module Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type
Display 0					
D52	DP0_D0_HDMI_D2_N	HS_DISP0_HDMI_D2_DP0_N	Display Port 0: HDMI Lane 2 or DP lane 0. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
D51	DP0_D0_HDMI_D2_P	HS_DISP0_HDMI_D2_DP0_P			
B52	DP0_D1_HDMI_D1_N	HS_DISP0_HDMI_D1_DP1_N	Display Port 0: HDMI Lane 1 or DP lane 1. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
B51	DP0_D1_HDMI_D1_P	HS_DISP0_HDMI_D1_DP1_P			
A50	DP0_D2_HDMI_D0_N	HS_DISP0_HDMI_D0_DP2_N	Display Port 0: HDMI Lane 0 or DP lane 2. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
A51	DP0_D2_HDMI_D0_P	HS_DISP0_HDMI_D0_DP2_P			
C50	DP0_D3_HDMI_CK_N	HS_DISP0_HDMI_CK_DP3_N	Display Port 0: HDMI CK or DP lane 3. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
C51	DP0_D3_HDMI_CLK_P	HS_DISP0_HDMI_CK_DP3_P			
K50	HPD0	GP253_HPD0_N	Display Port 0: Hot Plug Detect (HPD)	Bidir	CMOS – 1.8V
J50	HDMI_CEC	GP06_HDMI_CEC	HDMI CEC	Bidir	Open Drain, 1.8V

Module Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type
G53	DP_AUX_CH0_P	SF_DPAUX0_P	Display Port 0 Aux+ or HDMI DDC SCL. AC-Coupled on Carrier Board for DP AUX (DP) or pulled high for DDC/I2C.	Bidir	Open-Drain, 1.8V
G54	DP_AUX_CH0_N	SF_DPAUX0_N		Bidir	Open-Drain, 1.8V
Display 1					
H48	DP1_D0_HDMI_D2_N	HS_DISP1_HDMI_D2_DP0_N	Display Port 1: HDMI Lane 2 or DP lane 0. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
H49	DP1_D0_HDMI_D2_P	HS_DISP1_HDMI_D2_DP0_P			
G50	DP1_D1_HDMI_D1_N	HS_DISP1_HDMI_D1_DP1_N	Display Port 1: HDMI Lane 1 or DP lane 1. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
G51	DP1_D1_HDMI_D1_P	HS_DISP1_HDMI_D1_DP1_P			
J48	DP1_D2_HDMI_D0_N	HS_DISP1_HDMI_D0_DP2_N	Display Port 1: HDMI Lane 0 or DP lane 2. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
J47	DP1_D2_HDMI_D0_P	HS_DISP1_HDMI_D0_DP2_P			
K47	DP1_D3_HDMI_CK_N	HS_DISP1_HDMI_CK_DP3_N	Display Port 1: HDMI CK or DP lane 3. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
K46	DP1_D3_HDMI_CK_P	HS_DISP1_HDMI_CK_DP3_P			
C18	HPD1	GP254_HPD1_N	Display Port 1: Hot Plug Detect	Bidir	CMOS – 1.8V
D16	DP_AUX_CH1_P	SF_DPAUX1_P	Display Port 1 Aux+/- or HDMI DDC SCL/DAT. AC-Coupled on Carrier Board for DP AUX (DP) or pulled high for DDC/I2C.	Bidir	Open-Drain, 1.8V
D17	DP_AUX_CH1_N	SF_DPAUX1_N			
Display 2					
A14	DP2_D0_HDMI_D2_N	HS_DISP2_HDMI_D2_DP0_N	Display Port 2: HDMI Lane 2 or DP lane 0. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
A15	DP2_D0_HDMI_D2_P	HS_DISP2_HDMI_D2_DP0_P			
J15	DP2_D1_HDMI_D1_N	HS_DISP2_HDMI_D1_DP1_N	Display Port 2: HDMI Lane 1 or DP lane 1. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
J14	DP2_D1_HDMI_D1_P	HS_DISP2_HDMI_D1_DP1_P			
C14	DP2_D2_HDMI_D0_N	HS_DISP2_HDMI_D0_DP2_N	Display Port 2: HDMI Lane 0 or DP lane 2. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
C15	DP2_D2_HDMI_D0_P	HS_DISP2_HDMI_D0_DP2_P			
G14	DP2_D3_HDMI_CK_N	HS_DISP2_HDMI_CK_DP3_N	Display Port 2: HDMI CK or DP lane 3. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair

Module Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type
G15	DP2_D3_HDMI_CK_P	HS_DISP2_HDMI_CK_DP3_P			
A19	HPD2	GP255_HPD2_N	Display Port 2: Hot Plug Detect	Bidir	CMOS – 1.8V
E19	DP_AUX_CH2_P	SF_DPAUX2_P	Display Port 2 Aux+ or HDMI DDC SCL. AC-Coupled on Carrier Board for DP AUX (DP) or pulled high for DDC/I2C.	Bidir	Open-Drain, 1.8V
E18	DP_AUX_CH2_N	SF_DPAUX2_N			
Display 3					
D32	DP3_D0_HDMI_D2_N	HS_DISP3_HDMI_D2_DP0_N	Display Port 3: HDMI Lane 2 or DP lane 0. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
D33	DP3_D0_HDMI_D2_P	HS_DISP3_HDMI_D2_DP0_P			
J34	DP3_D1_HDMI_D1_N	HS_DISP3_HDMI_D1_DP1_N	Display Port 3: HDMI Lane 1 or DP lane 1. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
J35	DP3_D1_HDMI_D1_P	HS_DISP3_HDMI_D1_DP1_P			
A35	DP3_D2_HDMI_D0_N	HS_DISP3_HDMI_D0_DP2_N	Display Port 3: HDMI Lane 0 or DP lane 2. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
A34	DP3_D2_HDMI_D0_P	HS_DISP3_HDMI_D0_DP2_P			
H33	DP3_D3_HDMI_CK_N	HS_DISP3_HDMI_CK_DP3_N	Display Port 3: HDMI CK or DP lane 3. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
H32	DP3_D3_HDMI_CK_P	HS_DISP3_HDMI_CK_DP3_P			
C19	HPD3	GP256_HPD3_N	Display Port 3: Hot Plug Detect	Bidir	CMOS – 1.8V
F20	DP_AUX_CH3_P	SF_DPAUX3_P	Display Port 3 Aux+ or HDMI DDC SCL. AC-Coupled on Carrier Board for DP AUX (DP) or pulled high for DDC/I2C.	Bidir	Open-Drain, 1.8V
F21	DP_AUX_CH3_N	SF_DPAUX3_N			

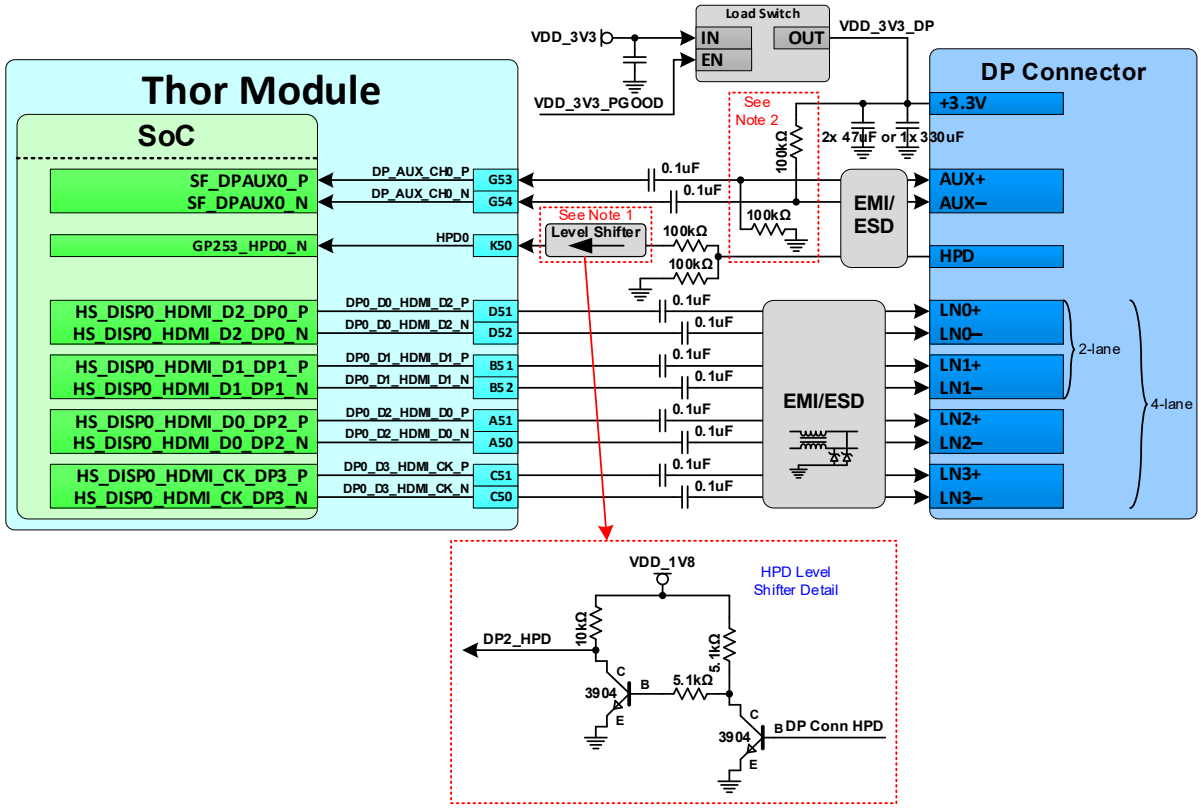
Notes:

1. In the Direction column, Output is from Jetson Thor; Input is to Jetson Thor. Bidir is for Bidirectional signals.
2. The direction shown in this table for DPx_HPD is true when used for Hot Plug Detect. Otherwise, if used as GPIOs, the direction is bidirectional.

9.1 DP

The following figure shows a basic connection example to DP connectors.

Figure 9-1. DP Connection Example

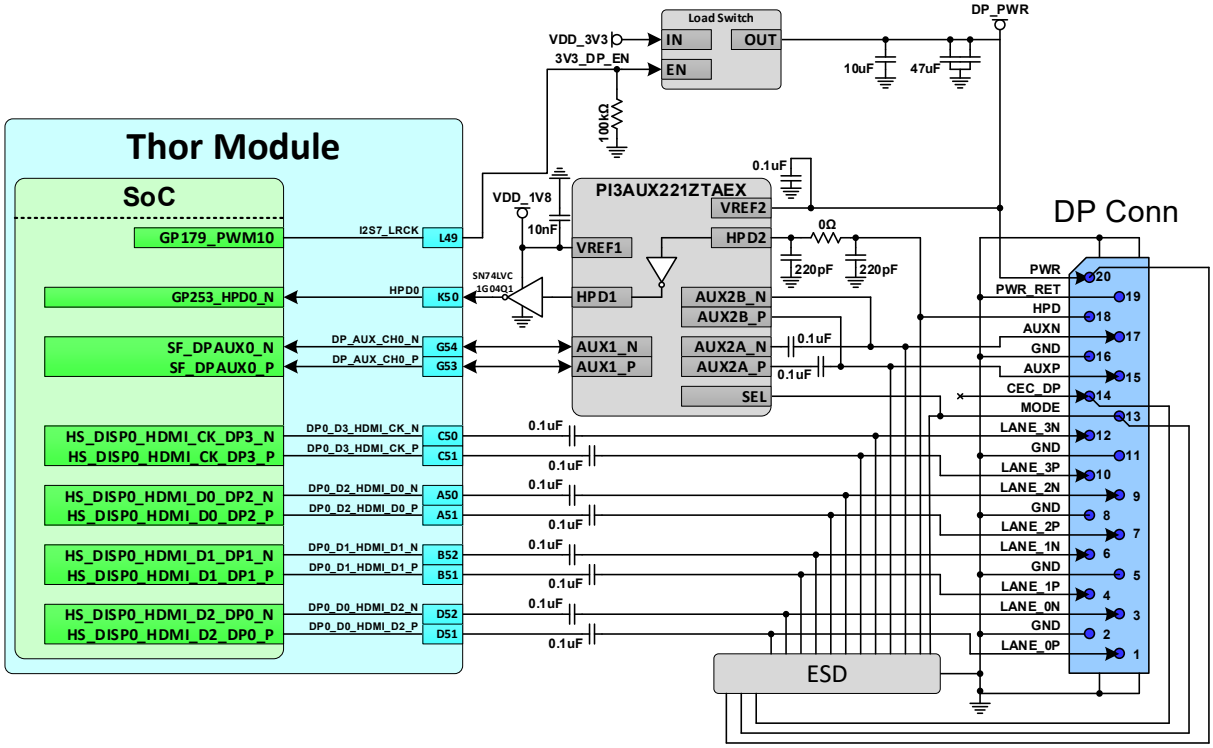


Notes:

1. A Level shifter is required on HPD to avoid the pin from being driven when the module is off. The level shifter must be non-inverting (preserve polarity of the signal from the display). See level shifter detail below main figure.
2. Pull-up/down only required for DP.
3. If EMI devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing and electrical requirements of the DisplayPort specification for the modes to be supported. Any ESD solution must also maintain signal integrity and meet the DisplayPort requirements for the modes to be supported.

The following figure shows an example connection to a DP connector using an integrated PI3AUX221 device to reduce the components required for level shifting and pull-up resistors. This design also supports DP++.

Figure 9-2. DP Connection Example with Integrated PI3AUX221 Device



Notes:

1. CEC is optional. If not required, the CEC_DP pin on the DP connector (Pin 14) left open.
2. If EMI devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing and electrical requirements of the DisplayPort specification for the modes to be supported. Any ESD solution must also maintain signal integrity and meet the DisplayPort requirements for the modes to be supported.

Table 9-2. Basic DP Signal Connections

Pin #	Module Pin Name	Type	Termination	Description
D51	DP0_D0_HDMI_D2_P	O	Series 0.1uF capacitors on all lines	DP Differential Data Lanes: Connect to matching pins on display connector. See DP/HDMI Pin Descriptions and connection diagram for details.
D52	DP0_D0_HDMI_D2_N			
B51	DP0_D1_HDMI_D1_P			
B52	DP0_D1_HDMI_D1_N			
A51	DP0_D2_HDMI_D0_P			
A50	DP0_D2_HDMI_D0_N			
C51	DP0_D3_HDMI_CK_P			
C50	DP0_D3_HDMI_CK_N			
G53	DP_AUX_CH0_P	I/OD	Series 0.1uF capacitors DP_AUX_CH0_P pulled to GND through 100kΩ resistor. DP_AUX_CH0_N pulled to VDD_3V3_DP through 100kΩ resistor.	DP: Auxiliary Channels: Connect to AUX_CH+/– on display connector.
G54	DP_AUX_CH0_N			
K50	HPD0_N	I	100kΩ series resistor and 100kΩ resistor to GND then Level shifter (non-inverting) between connector and module pin.	DP: Hot Plug Detect: Connect to HPD pin on display connector. See Connections Example figure for details.
	VDD_3V3_EDP	P	From level shifter	DP 3.3V supply: Connect output of load switch to DP connector +3.3V pin. Connect input of load switch to VDD_3V3. Connect enable of load switch to VDD_3V3_PGOOD.

Table 9-3. DP Signal Connections for Integrated PI3AUX221 Solution

Module Pin Name	Type	Termination	Description
DP0_D0_HDMI_D[2:0]_P/N	O	Series 0.1uF capacitors on all lines. Optional ESD to GND.	DP Differential Data Lanes: Connect to matching pins on display connector.
DP_AUX_CH0_P/N	I/OD	To PI3AUX221 with 0.1uF series capacitors on AUX2A_N/P path to connector.	DP Auxiliary Channel: Connect to PI3AUX221 device to AUX1_N/P pins. Connect PI3xxx device AUX2B_N/P pins to AUX_CH–/P pins on DP connector. Connect PI3xxx device AUX2A_N/P pins through series AC capacitors to AUX_CH–/P pins on DP connector.
HDP0	I	To PI3AUX221 through inverter then to DP connector HPD pin.	DP Hot Plug Detect: Connect to inverter output then HPD1 pin of PI3AUX221 device. Connect PI3xxx HPD2 pin to HPD pin on display connector.
HDMI_CEC	I/OD	Refer to Figure 9-4 for gating circuitry details.	Consumer Electronics Control (optional): Connect to CEC_DP pin on DP Connector through circuitry. See details under connection figure or reference design for details.

Module Pin Name	Type	Termination	Description
VDD_3V3_EDP	P	From level shifter	DP 3.3V supply: Connect output of load switch to DP connector +3.3V pin. Connect input of load switch to VDD_3V3. Connect enable of load switch to VDD_3V3_PGOOD.
(PI3AUX221 VREF1)	P		PI3AUX221 Voltage Reference 1: Connect to VDD_1V8.
(PI3AUX221 VREF2)	P		PI3AUX221 Voltage Reference 2: Connect to VDD_3V3_DP.
(PI3AUX221 SEL)	I		PI3AUX221 Mode Select: Connect to MODE pin of DP connector.

9.1.1 DP Routing Guidelines

The following figure shows the topology for DisplayPort. The table below shows the signal routing requirements including **DP_AUX**.

Figure 9-3. DP Differential Main Link Topology

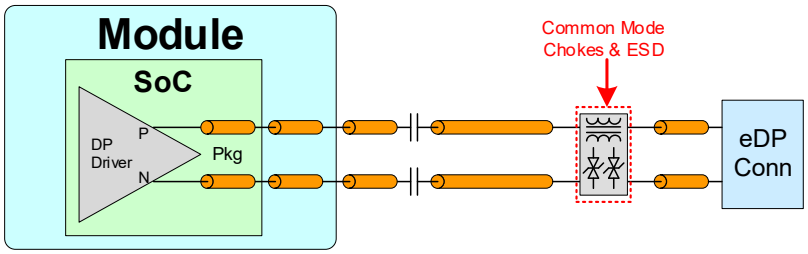
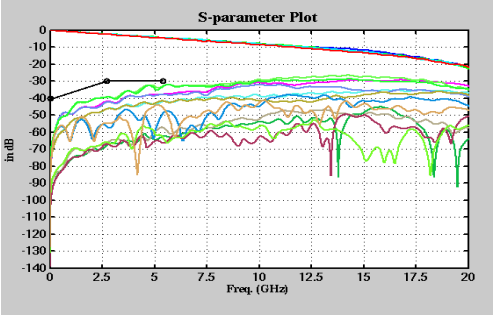
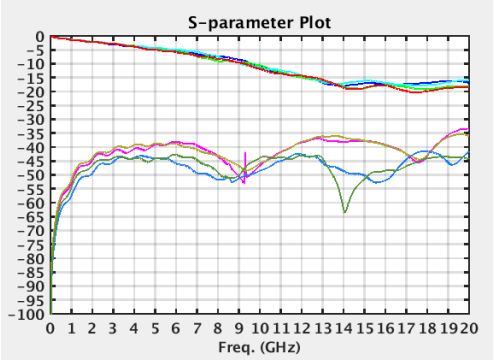
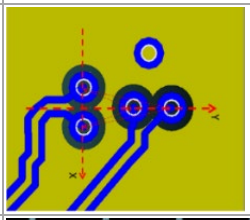
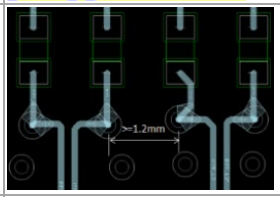


Table 9-4. DP Main Link Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Max Data Rate / Min UI HBR3 HBR2 HBR RBR	 8.1 / 123 5.4 / 185 2.7 / 370 1.62 / 617	Gbps / ps	Per data lane
Number of Loads / Topology	1	load	Point-Point, Differential, Unidirectional
Termination	100	Ω	On die at TX/RX
Electrical Specification			
Insertion Loss E-HBR @ 0.675GHz PBR 0.68GHz HBR 1.35GHz HBR2 @ 2.7GHz HBR3 @ 4.05GHz	 <=0.7 <=0.7 <=1.2 <=4.5 <=5.5	dB	
Resonance dip frequency HBR2 HBR3	 >8 >12	GHz	

Parameter	Requirement	Units	Notes
TDR dip	>85	Ω	@ Tr-200ps (10%-90%)
FEXT @ DC @ 2.7GHz @ 5.4GHz	 <= -40dB <= -30dB <= -30dB	IL/FEXT plot – up to HBR2  IL/FEXT plot – HBR3  	
Impedance			
Trace Impedance (Diff pair)	100 90 85	Ω (±10%)	100Ω is the specification target. 95/85Ω are implementation options (Zdiff does not account for trace coupling) 95Ω should be used to support DP-HDMI co-layout as HDMI 2.0 requires 100Ω impedance (see HDMI section for addition of series resistor R_S). 85Ω can be used if DP only and is preferable as it provides better trace loss characteristic performance. See Note 1.
Reference Plane	**GND**		
Trace Length (delay), Spacing and Skew			
Trace loss characteristic HBR2 or lower (@ 2.7GHz) HBR3 (@405GHz)	 < 0.64 <=0.9	dB/in	The following max length (delay) is derived based on this characteristic. The length (delay) constraint must be re-defined if loss characteristic is changed.
Max PCB Via dist. from module conn. **RBR/HBR** **HBR2 and HBR3**	 No requirement 7.62	mm	

Parameter	Requirement	Units	Notes
Max trace length (delay) from module to connector **RBR/HBR** Stripline Microstrip **HBR2** Stripline Microstrip **HBR3** Stripline Microstrip	 215 (1137.5) 215 (975) 184 (1260) 178 (1050) 162 (1120) 155 (900)	mm (ps)	6.9ps/mm assumption for Stripline, 5.9ps/mm for Microstrip.
Trace spacing (Pair-Pair) Stripline Microstrip (**HBR/RBR**) Microstrip (**HBR2/HBR3**)	 3x 4x 5x to 7x	dielectric height	
Trace spacing (Main Link to AUX): Stripline/Microstrip	3x / 5x	dielectric height	
Max Intra-pair (within pair) Skew	0.15 (1)	mm (ps)	Do not perform length (delay) matching within breakout region. Do trace length (delay) matching before hitting discontinuity (i.e. matching to <1ps before the vias or any discontinuity to minimize common mode conversion).
Max Inter-pair (pair-pair) Skew	150	ps	
Via			
Max GND transition Via distance	< 1x	diff pair pitch	For signals switching reference layers, add symmetrical GND stitching Via near signal Vias.
Impedance dip Recommended via dimension for impedance control Drill/Pad Antipad Via pitch	≥97 ≥92 200/400 >840 ≥880	Ω @ 200ps Ω @ 35ps um um um	The via dimension must be required for the HDMI-DP co-layout condition.
Topology	Y-pattern is recommended keep symmetry Xtalk suppression is best using the Y-pattern. It can also reduce the limit of pair-pair distance.		
	For in-line via, the distance from a via of one lane to the adjacent via from another lane >= 1.2 mm center-center.		
GND via	Place GND via as symmetrically as possible to data pair vias. Up to four signal vias (two diff pairs) can share a single GND return via		GND via is used to maintain return path, while its Xtalk suppression is limited

Parameter	Requirement	Units	Notes
Max # of Vias PTH vias Micro Vias	 Four if all vias are PTH via Not limited as long as total channel loss meets IL specification		
Max Via Stub Length	0.4	mm	
AC Cap			
Value	0.1	uF	Discrete 0402
Max Dist. from AC cap to connector RBR/HBR HBR2/HBR3	 No requirement 0.5	in	
Voiding RBR/HBR HBR2/HBR3	 No requirement Voiding required		**HBR2**: Voiding the plane directly under the pad ~0.1mm larger than the pad size is recommended.
Serpentine (See USB 3.2 Guidelines)			
Connector			
Voiding RBR/HBR HBR2/HBR3	 No requirement Voiding required		**HBR2**: Standard DP Connector: Voiding requirement is stack-up dependent. For typical stack-ups, voiding on the layer under the connector pad is required to be 5.7mil larger than the connector pad.
General			
Keep critical PCIe traces away from other signal traces or unrelated power traces/areas or power supply components			

Notes:

1. For DP, the specification puts a higher priority on the trace loss characteristic than on the impedance. However, before selecting 85Ω for impedance, it is important to make sure the selected stack-up, material and trace dimension can achieve the needed low loss characteristic.
2. The average of the differential signals is used for length/delay matching.
3. Do not perform length/delay matching within breakout region. Recommend doing trace length/delay matching to <1ps before vias or any discontinuity to minimize common mode conversion

Table 9-5. Recommended DP Test Points for Initial Boards

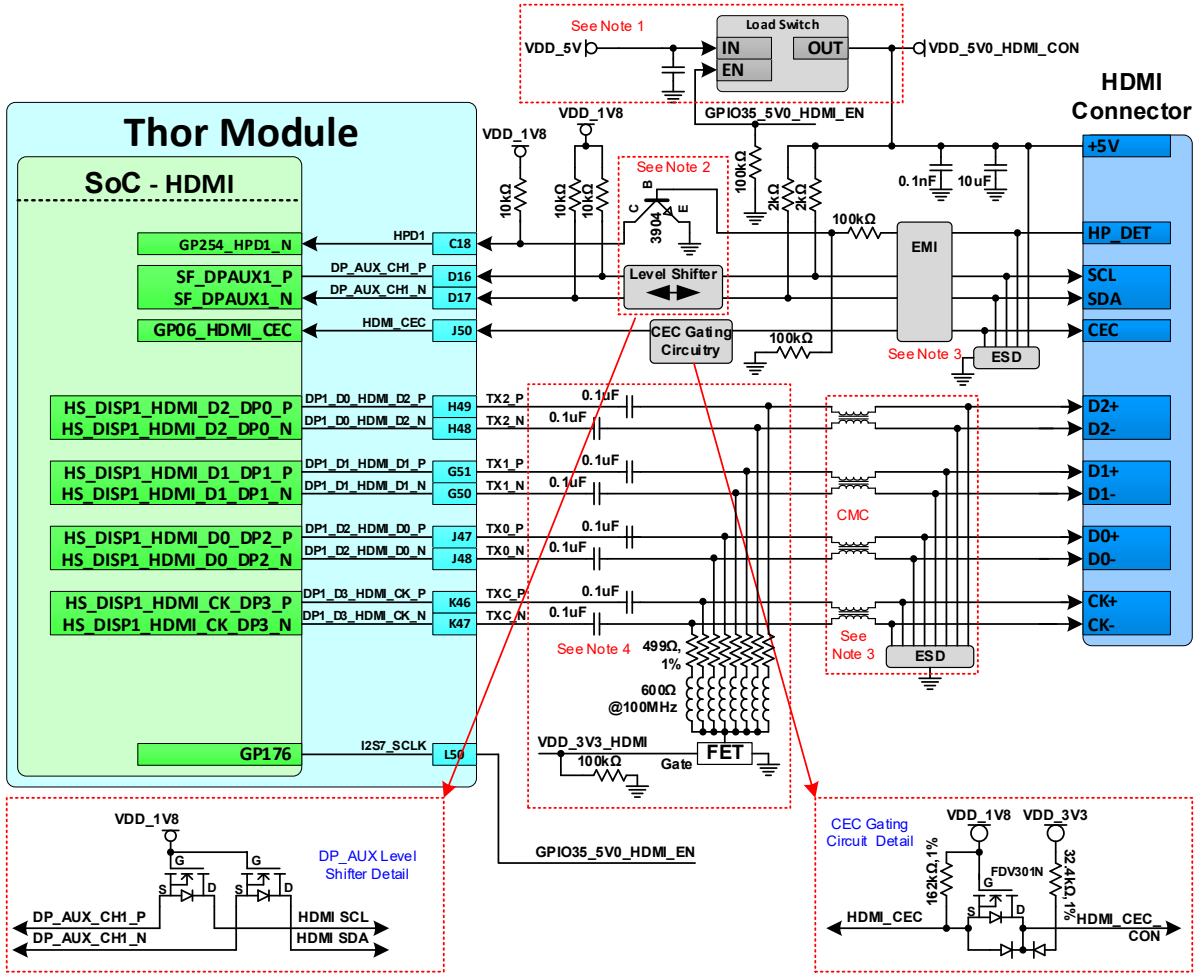
Test Points Recommended	Location
One for each signal line.	Near display connector. Connector pins can be used if accessible.

Note: Test points must be done carefully to minimize signal integrity impact. Avoid stubs and keep pads small and near signal traces

9.2 HDMI

The following figure shows the connection example for an HDMI connector.

Figure 9-4. HDMI Connection Example



Notes:

1. Load switch circuit is intended to remove power to the HDMI connector, etc., to avoid backdrive on signals to the module. Other mechanisms may be used but must prevent module pins being driven when the module is off.
2. Level shifters required on DDC/HPD. Jetson Thor pads are not 5V tolerant and cannot directly meet HDMI VIL/VIH requirements. HPD level shifter can be non-inverting or inverting.
3. If EMI/ESD devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing and electrical requirements of the HDMI specification for the modes to be supported. See requirements and recommendations in the related sections of Table 9-7.
4. HDMI_DP2_TXx pads are native DP pads and require series AC capacitors and pull-downs (RPDs) to be HDMI compliant. The 499Ω, 1% pull-downs must be disabled when

	SoC is off to meet the HDMI VOFF requirement. The FET enables the pull-downs when the HDMI interface is to be used. Chokes between pull-downs and FET are required for Standard Technology designs and recommended for HDI designs.

Table 9-6. HDMI Signal Connections

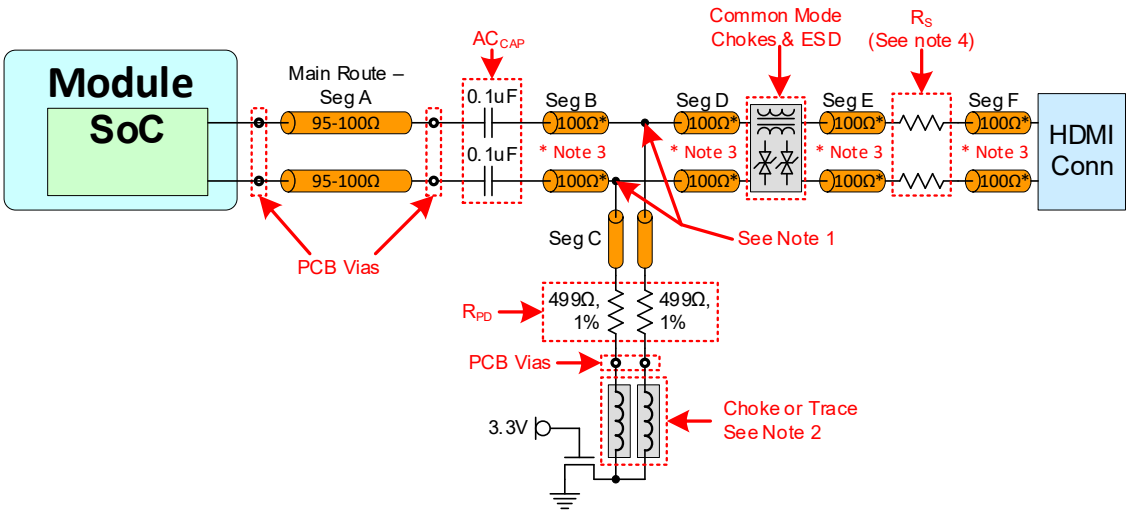
Pin #	Module Pin Name	Type	Termination (See Note on ESD)	Description
K47	DP1_D3_HDMI_CK_N	DIFF OUT	0.1uF series AC_{CAP} → 499Ω to GND (R_{PD}) -> EMI/ESD (if required), then ≤6Ω series register (R_S if required).	HDMI Differential Clock: Connect to C–/C+ and pins on HDMI connector
K46	DP1_D3_HDMI_CK_P			
J47	DP1_D2_HDMI_D0_N	DIFF OUT		HDMI Differential Data: Connect to D[2:0]+/– pins. See Table 9-1 and connection diagram.
J48	DP1_D2_HDMI_D0_P			
G51	DP1_D1_HDMI_D1_N			
G50	DP1_D1_HDMI_D1_P			
H49	DP1_D0_HDMI_D2_N			
H48	DP1_D0_HDMI_D2_P			
C18	HPD1	I	Thor module to Connector: 10kΩ PU to 1.8V → level shifter → 100kΩ series resistor. 100kΩ to GND on connector side.	HDMI Hot Plug Detect: Connect to HPD pin on HDMI Connector
J50	HDMI_CEC	I/OD	Gating circuitry. See details under connection figure or reference design for details.	HDMI Consumer Electronics Control: Connect to CEC on HDMI Connector through circuitry.
D17	DP_AUX_CH1_N	I/OD	From Thor module to Connector: 10kΩ PU to 3.3V → level shifter → 1.8kΩ PU to 5V → connector pin. See details under connection figure for recommended level shifter circuit.	HDMI: DDC Interface – Clock and Data: Connect DPx_AUX_CH+ to SCL and DPx_AUX_CH– to SDA on HDMI connector
D16	DP_AUX_CH1_P			
	HDMI 5V Supply	P	Adequate decoupling (0.1uF and 10uF recommended) on supply near connector.	HDMI 5V supply to connector: Connect to +5V on HDMI connector.

Note: Any ESD and/or EMI solutions must support targeted modes (frequencies).

9.2.1 HDMI Design Guidelines

The following figure illustrates the HDMI clock and data topology.

Figure 9-5. HDMI CLK and Data Topology

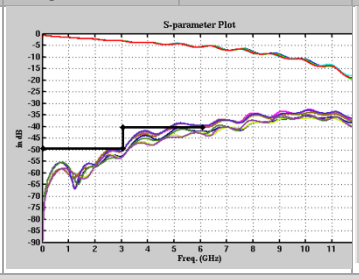
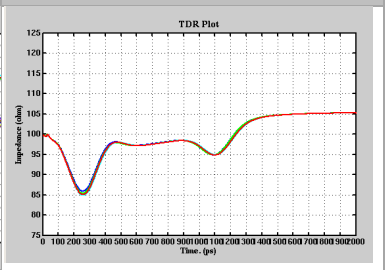
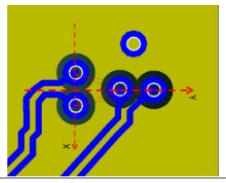


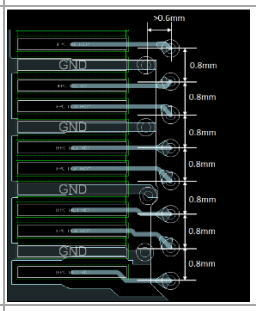
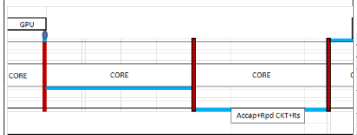
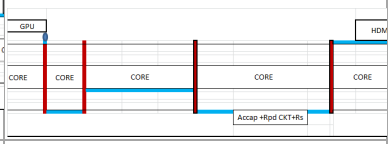
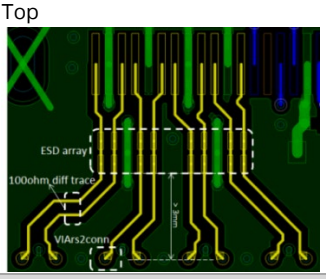
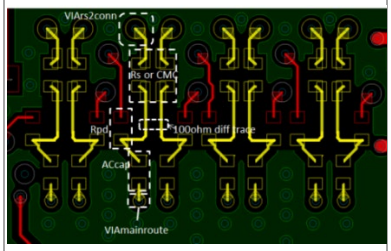
Notes:

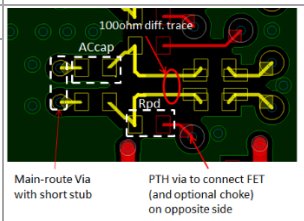
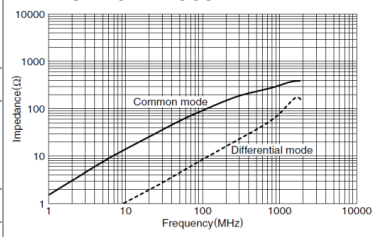
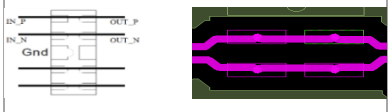
1. RPD pad must be on the main trace. RPD and ACCAP must be on same layer.
2. Chokes (600 Ω @ 100 MHz) or narrow traces (1 uH@DC-100 MHz) between pull-downs and FET are required for Standard Technology (through-hole) designs and recommended for HDI designs.
3. The trace after the main route via should be routed on the top or bottom layer of the PCB, and either with 100 Ω (for HDMI 2.0 HF 1-9 test) differential impedance, or as uncoupled 50 Ω Single Ended traces.

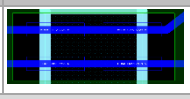
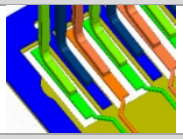
Table 9-7. HDMI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Electrical Specification			
IL resonance dip frequency	<= 1.7 <= 2 <= 3 < 4.3 > 12	dB @ 1GHz dB @ 1.5GHz dB @ 3GHz dB @ 6GHz GHz	For HDMI 2.0, 6dB and 6GHz is supported.
TDR dip	>= 85	Ω @ Tr=200ps	10%-90%. If TDR dip is 75~85ohm that dip width should be < 250ps
FEXT	<= -50 <= -40 <= -40	dB at DC dB at 3GHz dB at 6GHz	
	IL/FEXT plot		TDR plot

Parameter	Requirement	Units	Notes
			
Impedance			
Trace Impedance Diff pair	100	Ω	±10%. Target is 100Ω. 95Ω for the breakout and main route is an implementation option.
Reference plane	GND		
Trace Length (delay), Spacing and Skew			
Trace loss characteristic:	< 1.1 < 0.8 < 0.4	dB/in. @ 6GHz dB/in. @ 3GHz dB/in. @ 1.5GHz	The max length (delay) is derived based on this characteristic. The length (delay) constraint must be re-defined if the loss characteristic is changed.
Min Trace spacing (Pair-Pair) Stripline: 2.1 Stripline: 1.4b/2.0 Microstrip: 2.1 Microstrip: 1.4b/2.0	 4x 3x 7x 5x to 7x	dielectric height	For Stripline, this is 3x of the thinner of above and below.
Min Trace spacing (Main Link to DDC) Stripline Microstrip	 3x 5x	dielectric height	For Stripline, this is 3x of the thinner of above and below.
Max Total Delay (2.1) Stripline (4x spacing) Microstrip (7x spacing)	 76 (535) 63.5 (375)	mm (ps)	Propagation delay: 6.9ps/mm assumption for Stripline, 5.9ps/mm for Microstrip.
Max Total Delay (1.4b/2.0) Stripline Microstrip (5x spacing) Microstrip (7x spacing)	 101 (700) 88.5 (525) 101 (600)	mm (ps)	Propagation delay: 6.9ps/mm assumption for Stripline, 5.9ps/mm for Microstrip.
Max Intra-Pair (within pair) Skew	0.15 (1)	mm (ps)	See Notes 1, 2, and 3
Max Inter-Pair (pair to pair) Skew	150	ps	See Notes 1, 2, and 3
Max **GND** transition Via distance	1x	Diff pair via pitch	For signals switching reference layers, add one or two ground stitching vias. It is recommended they be symmetrical to signal vias.
Via			
Topology	Y-pattern is recommended keep symmetry		Xtalk suppression is the best by Y-pattern. Also, it can reduce the limit of pair-pair distance. Need review (NEXT/FEXT check) if via placement is not Y-pattern.
Minimum Impedance dip Recommended via dimension for impedance control Drill/Pad Antipad Via pitch	≥97 ≥92 200/400 >840 ≥880	Ω @ 200ps Ω @ 35ps um um um	

Parameter	Requirement	Units	Notes
GND via	Place GND via as symmetrically as possible to data pair vias. Up to four signal vias (two diff pairs) can share a single GND return via		GND via is used to maintain return path, while its Xtalk suppression is limited
Connector pin via	The break-in trace to the connector pin via should be routed on the BOTTOM in order to avoid via stub effect. Equal spacing (0.8mm) between adjacent signal vias. The x-axis distance between signal and GND via should be > 0.6mm		
Max # of Vias PTH vias Micro Vias	Four if all vias are PTH via Not limited as long as total channel loss meets IL specification		
	No breakout: ≤ 3 vias 		Breakout on the same layer as main trunk: ≤ 4 vias 
Max Via Stub Length	0.4	mm	Long via stub requires review (IL and resonance dip check)
Serpentine (refer to the USB 3.2 Guidelines) **Topology (Figure 9-5)**			
The main-route via dimensions should comply with the via structure rules (See Via section)			
For the connector pin vias, follow the rules for the connector pin vias (See Via section)			
The traces after main-route via should be routed as 100Ω differential or as uncoupled 50ohm Single-ended traces on PCB Top or Bottom.			
Maximum distance from RPD to main trace (seg B)	1	mm	
Maximum distance from AC cap to RPD stubbing point (seg A)	~0	mm	
Pull-down Register (RPD). Choke/FET			
Series Resistor (RS) Series resistor on P/N path for HDMI 2.0 but not required for HDMI 2.1 (Mandatory to meet HDMI2.0 Compliance)			
Maximum distance between ESD and signal via	3	mm	
Add-on Components			
Example of a case where space is limited for placing components.	Top 		Bottom 
AC CAP			
Value	0.1	uF	

Parameter	Requirement	Units	Notes
Max via distance from BGA	7.62 (52.5)	mm (ps)	
Location	Must be placed before pull-down resistor		The distance between the AC cap and the HDMI connector is not restricted.
Placement PTH design Micro-Via design	Place cap on bottom layer if main-route above core Place cap on top layer if main-route below core Not Restricted		
Void	GND (or PWR) void under/above the cap is needed. Void size = SMT area + 1x dielectric height keepout distance		
Pull-down Resistor (RPD), choke/FET			
Value	499	Ω	
Location	Must be placed after AC cap		
Layer of placement	Same layer as AC cap. The FET and choke can be placed on the opposite layer through a PTH via		
Choke between RPD and FET Choke Max Trace Rdc Max Trace length	 600 or 1 ≤20 4	 Ω@100MHz uH@DC-100MHz mΩ mm	Can be choke or Trace. Recommended option for HDMI2.0 HF1-9 improvement.
Void	GND/PWR void under/above cap is preferred		
Common-Mode Choke (Stuffing option – not added unless EMI issue is seen)			
Common-mode impedance @ 100MHz Min Max	 65 90	 Ω	TDK ACM2012D-900-2P 
RDC	<=0.3ohm		
Differential TDR impedance	90ohm +/-15% @ Tr=200ps (10%-90%)		
Min Sdd21 @ 2.5GHz	2.22	dB	
Max Scc21 @ 2.5GHz	19.2	dB	
Location	Close to any adjacent discontinuity (< 8mm) – such as connector, via, etc.		
ESD (On-chip protection diode is able to withstand 2kV HMM. External ESD is optional. Designs should include ESD footprint as a stuffing option)			
Max junction capacitance (IO to GND)	0.35	pF	e.g., ON-semiconductor ESD8040
Footprint	Pad right on the net instead of trace stub		
Location	After pull-down resistor/CMC and before RS		

Parameter	Requirement	Units	Notes
Void	GND/PWR void under/above the cap is needed. Void size = 1mm x 2mm for 1 pair		
Connector			
Connector Voiding	Voiding the ground below the signal lanes 0.1448(5.7mil) larger than the pin itself		
General			
Routing over Voids	Routing over voids is not allowed except void around device ball/pin the signal is routed to.		
Noise Coupling	Keep critical HDMI related traces including differential clock/data traces and RSET trace away from other signal traces or unrelated power traces/areas or power supply components		

Notes:

1. **The average of the differential signals is used for length/delay matching.**
2. **Do not perform length/delay matching within breakout region. Recommend doing trace length/delay matching to <1ps before vias or any discontinuity to minimize common mode conversion**
3. **If routing includes a flex or 2nd PCB, the maximum trace delay and skew calculations must include all the PCBs/flex routing. Solutions with flex/2nd PCB may not achieve maximum frequency operation.**

Table 9-8. Recommended HDMI and DP Test Points for Initial Boards

Test Points Recommended	Location
One for each signal line.	Near display connector. Connector pins can be used if accessible.

Note: Test points must be done carefully to maximize integrity. Avoid stubs and keep pads small and near signal traces.

Chapter 10. Video Input

The Jetson Thor supports four MIPI CSI x4 bricks, allowing a variety of device types and combinations to be supported. Up to four quad lane cameras or four dual lane cameras plus two quad lane cameras or six dual lane cameras (total of six in any configuration) are available. Both MIPI D-PHY and C-PHY mode are supported. In D-PHY mode, each data channel has peak bandwidth of up to 2.5 Gbps. For C-PHY, each lane (Trio) supports up to 4.5 Gsps.

Note: Maximum data rate may be limited by use case and memory bandwidth.

Table 10-1. Jetson Thor CSI Pin Description

Pin #	Module Pin Name	SoC Ball Name	Usage/Description (See Note 2)	Direction	Pin Type
E42	CSI0_D0_P	HS_CSI0_D0_P	Camera, CSI 0: DPHY Data 0+, CPHY Lane 0:A	Input	MIPI D-PHY/ C-PHY
E41	CSI0_D0_N	HS_CSI0_D0_N	Camera, CSI 0: DPHY Data 0–, CPHY Lane 0:B		
F43	CSI0_CLK_P	HS_CSI0_CLK_P	Camera, CSI 0: DPHY Clock+, CPHY Lane 0:C		
F42	CSI0_CLK_N	HS_CSI0_CLK_N	Camera, CSI 0: DPHY Clock–, CPHY Lane 1:C		
E39	CSI0_D1_P	HS_CSI0_D1_P	Camera, CSI 0: DPHY Data 1+, CPHY Lane 1:A		
E38	CSI0_D1_N	HS_CSI0_D1_N	Camera, CSI 0: DPHY Data 1–, CPHY Lane 1:B		
G41	CSI1_D0_P	HS_CSI1_D0_P	Camera, CSI 1: DPHY Data 0+, CPHY Lane 0:A	Input	MIPI D-PHY/ C-PHY
G42	CSI1_D0_N	HS_CSI1_D0_N	Camera, CSI 1: DPHY Data 0–, CPHY Lane 0:B		
H43	CSI1_CLK_P	HS_CSI1_CLK_P	Camera, CSI 1: DPHY Clock+, CPHY Lane 0:C		
H42	CSI1_CLK_N	HS_CSI1_CLK_N	Camera, CSI 1: DPHY Clock–, CPHY Lane 1:C		
J41	CSI1_D1_P	HS_CSI1_D1_P	Camera, CSI 1: DPHY Data 1+, CPHY Lane 1:A		
J42	CSI1_D1_N	HS_CSI1_D1_N	Camera, CSI 1: DPHY Data 1–, CPHY Lane 1:B		
A41	CSI2_D0_P	HS_CSI2_D0_P	Camera, CSI 2: DPHY Data 0+, CPHY Lane 0:A	Input	MIPI D-PHY/ C-PHY
A42	CSI2_D0_N	HS_CSI2_D0_N	Camera, CSI 2: DPHY Data 0–, CPHY Lane 0:B		
B43	CSI2_CLK_P	HS_CSI2_CLK_P	Camera, CSI 2: DPHY Clock+, CPHY Lane 0:C		
B42	CSI2_CLK_N	HS_CSI2_CLK_N	Camera, CSI 2: DPHY Clock–, CPHY Lane 1:C		
C42	CSI2_D1_P	HS_CSI2_D1_P	Camera, CSI 2: DPHY Data 1+, CPHY Lane 1:A		
C41	CSI2_D1_N	HS_CSI2_D1_N	Camera, CSI 2: DPHY Data 1–, CPHY Lane 1:B		
E45	CSI3_D0_P	HS_CSI3_D0_P	Camera, CSI 3: DPHY Data 0+, CPHY Lane 0:A	Input	MIPI D-PHY/ C-PHY
E44	CSI3_D0_N	HS_CSI3_D0_N	Camera, CSI 3: DPHY Data 0–, CPHY Lane 0:B		
F46	CSI3_CLK_P	HS_CSI3_CLK_P	Camera, CSI 3: DPHY Clock+, CPHY Lane 0:C		

Pin #	Module Pin Name	SoC Ball Name	Usage/Description (See Note 2)	Direction	Pin Type
F45	CSI3_CLK_N	HS_CSI3_CLK_N	Camera, CSI 3: DPHY Clock–, CPHY Lane 1:C		
G44	CSI3_D1_P	HS_CSI3_D1_P	Camera, CSI 3: DPHY Data 1+, CPHY Lane 1:A		
G45	CSI3_D1_N	HS_CSI3_D1_N	Camera, CSI 3: DPHY Data 1–, CPHY Lane 1:B		
G48	CSI4_D0_P	HS_CSI4_D0_P	Camera, CSI 4: DPHY Data 0+, CPHY Lane 0:A	Input	MIPI D-PHY/ C-PHY
G47	CSI4_D0_N	HS_CSI4_D0_N	Camera, CSI 4: DPHY Data 0–, CPHY Lane 0:B		
F48	CSI4_CLK_P	HS_CSI4_CLK_P	Camera, CSI 4: DPHY Clock+, CPHY Lane 0:C		
F49	CSI4_CLK_N	HS_CSI4_CLK_N	Camera, CSI 4: DPHY Clock–, CPHY Lane 1:C		
E47	CSI4_D1_P	HS_CSI4_D1_P	Camera, CSI 4: DPHY Data 1+, CPHY Lane 1:A		
E48	CSI4_D1_N	HS_CSI4_D1_N	Camera, CSI 4: DPHY Data 1–, CPHY Lane 1:B		
D42	CSI5_D0_P	HS_CSI5_D0_P	Camera, CSI 5: DPHY Data 0+, CPHY Lane 0:A	Input	MIPI D-PHY/ C-PHY
D43	CSI5_D0_N	HS_CSI5_D0_N	Camera, CSI 5: DPHY Data 0–, CPHY Lane 0:B		
C44	CSI5_CLK_P	HS_CSI5_CLK_P	Camera, CSI 5: DPHY Clock+, CPHY Lane 0:C		
C45	CSI5_CLK_N	HS_CSI5_CLK_N	Camera, CSI 5: DPHY Clock–, CPHY Lane 1:C		
D46	CSI5_D1_P	HS_CSI5_D1_P	Camera, CSI 5: DPHY Data 1+, CPHY Lane 1:A		
D45	CSI5_D1_N	HS_CSI5_D1_N	Camera, CSI 5: DPHY Data 1–, CPHY Lane 1:B		
K44	CSI6_D0_P	HS_CSI6_D0_P	Camera, CSI 6: DPHY Data 0+, CPHY Lane 0:A	Input	MIPI D-PHY/ C-PHY
K43	CSI6_D0_N	HS_CSI6_D0_N	Camera, CSI 6: DPHY Data 0–, CPHY Lane 0:B		
J44	CSI6_CLK_P	HS_CSI6_CLK_P	Camera, CSI 6: DPHY Clock+, CPHY Lane 0:C		
J45	CSI6_CLK_N	HS_CSI6_CLK_N	Camera, CSI 6: DPHY Clock–, CPHY Lane 61:C		
H46	CSI6_D1_P	HS_CSI6_D1_P	Camera, CSI 6: DPHY Data 1+, CPHY Lane 1:A		
H45	CSI6_D1_N	HS_CSI6_D1_N	Camera, CSI 6: DPHY Data 1–, CPHY Lane 1:B		
A44	CSI7_D0_P	HS_CSI7_D0_P	Camera, CSI 7: DPHY Data 0+, CPHY Lane 0:A	Input	MIPI D-PHY/ C-PHY
A45	CSI7_D0_N	HS_CSI7_D0_N	Camera, CSI 7: DPHY Data 0–, CPHY Lane 0:B		
B45	CSI7_CLK_P	HS_CSI7_CLK_P	Camera, CSI 7: DPHY Clock+, CPHY Lane 0:C		
B46	CSI7_CLK_N	HS_CSI7_CLK_N	Camera, CSI 7: DPHY Clock–, CPHY Lane 1:C		
C47	CSI7_D1_P	HS_CSI7_D1_P	Camera, CSI 7: DPHY Data 1+, CPHY Lane 1:A		
C48	CSI7_D1_N	HS_CSI7_D1_N	Camera, CSI 7: DPHY Data 1–, CPHY Lane 1:B		

Notes:

1. In the Direction column, Output is from Jetson Thor; Input is to Jetson Thor. Bidir is for Bidirectional signals.
2. The mapping of CSI CPHY signals inside Thor to the Thor pins is programmable. The default mapping is shown in the figure. Other mappings are possible and may be required in some cases.

Table 10-2. CSI Configurations for D-PHY

Module Pin Name	x2 Configurations						x4 Configurations			
	#1	#2	#3	#4	#5	#6	#1	#2	#3	#4
CSI0_D0_P/N	Data						Data			
CSI0_D1_P/N										
CSI1_D0_P/N		Data								
CSI1_D1_P/N										
CSI2_D0_P/N			Data					Data		
CSI2_D1_P/N										
CSI3_D0_P/N				Data						
CSI3_D1_P/N										
CSI4_D0_P/N					Data				Data	
CSI4_D1_P/N										
CSI5_D0_P/N										
CSI5_D1_P/N										
CSI6_D0_P/N						Data				Data
CSI6_D1_P/N										
CSI7_D0_P/N										
CSI7_D1_P/N										
CSI0_CLK_P/N	Clk						Clk			
CSI1_CLK_P/N		Clk								
CSI2_CLK_P/N			Clk					Clk		
CSI3_CLK_P/N				Clk						
CSI4_CLK_P/N					Clk				Clk	
CSI5_CLK_P/N										
CSI6_CLK_P/N						Clk				Clk
CSI7_CLK_P/N										

Notes:

1. Each 2-lane option shown in this table can also be used for one single lane camera as well.
2. Combinations of 1, 2, and 4-lane cameras are supported, as long as any 4-lane cameras match one of the four configurations.

Table 10-3. CSI Configurations for C-PHY -x2 and x4

		2-Trio Configs						4-Trio Configs			
Camera # **SoC Balls**	**C-PHY Lanes**	**#1**	**#2**	**#3**	**#4**	**#5**	**#6**	**#1**	**#2**	**#3**	**#4**
HS_CSI0_CLK_P, HS_CSI0_D0_P/N	0:0	√						√			
HS_CSI0_CLK_N, HS_CSI0_D1_P/N	0:1	√						√			
HS_CSI1_CLK_P, HS_CSI1_D0_P/N	1:0		√					√			
HS_CIS1_CLK_N, HS_CSI1_D1_P/N	1:1		√					√			
HS_CSI2_CLK_P, HS_CSI2_D0_P/N	2:0			√					√		
HS_CSI2_CLK_N, HS_CSI2_D1_P/N	2:1			√					√		
HS_CSI3_CLK_P, HS_CSI3_D0_P/N	3:0				√				√		
HS_CSI3_CLK_N, HS_CSI3_D1_P/N	3:1				√				√		
HS_CSI4_CLK_P, HS_CSI4_D0_P/N	4:0					√				√	
HS_CSI4_CLK_N, HS_CSI4_D1_P/N	4:1					√				√	
HS_CSI5_CLK_P, HS_CSI5_D0_P/N	5:0									√	
HS_CSI5_CLK_N, HS_CSI5_D1_P/N	5:1									√	
HS_CSI6_CLK_P, HS_CSI6_D0_P/N	6:0						√				√
HS_CSI6_CLK_N, HS_CSI6_D1_P/N	6:1						√				√
HS_CSI7_CLK_P, HS_CSI7_D0_P/N	7:0										√
HS_CSI7_CLK_N, HS_CSI7_D1_P/N	7:1										√

Notes: Each x2 configurations can also be used for one single lane camera (x1 configuration) as well.

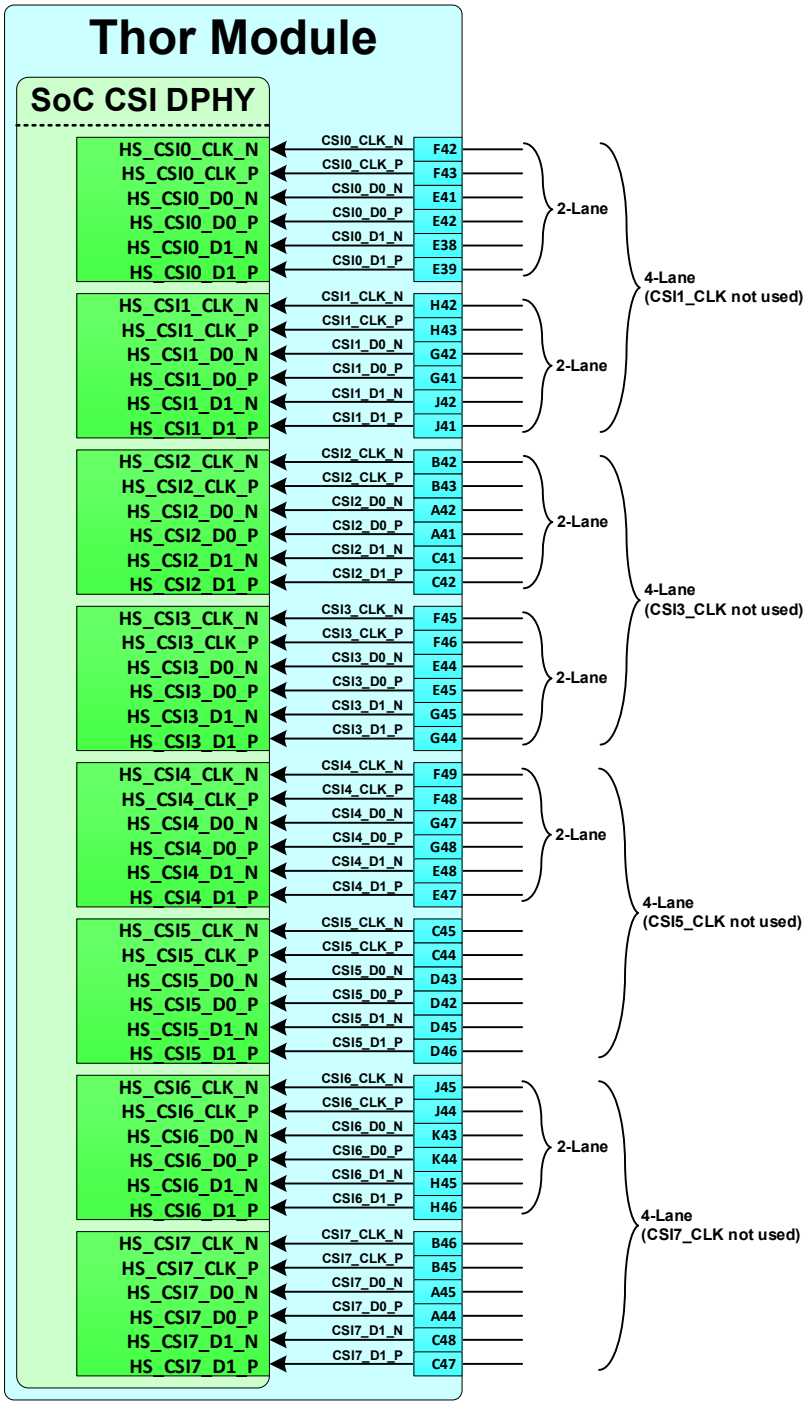
Configurations can coexist to support a mix of x1, x2, and x4 lanes, if each signal is not shared between multiple configurations.

Table 10-4. CSI Configurations C-PHY – x3 and x1

Camera # SoC Balls	x4 Blocks	C-PHY Lanes	#1	#2	#3	#4	#5	#6
HS_CSI0_CLK_P, HS_CSI0_D0_P/N	0	0:0	√					
HS_CIS0_CLK_N, HS_CSI0_D1_P/N		0:1	√					
HS_CSI1_CLK_P, HS_CSI1_D0_P/N		1:0	√					
HS_CSI1_CLK_N, HS_CSI1_D1_P/N		1:1		√				
HS_CSI2_CLK_P, HS_CSI2_D0_P/N	1	2:0			√			
HS_CSI2_CLK_N, HS_CSI2_D1_P/N		2:1			√			
HS_CSI3_CLK_P, HS_CSI3_D0_P/N		3:0			√			
HS_CSI3_CLK_N, HS_CSI3_D1_P/N		3:1				√		
HS_CSI4_CLK_P, HS_CSI4_D0_P/N	2	4:0					√	
HS_CSI4_CLK_N, HS_CSI4_D1_P/N		4:1					√	
HS_CSI5_CLK_P, HS_CSI5_D0_P/N		5:0					√	
HS_CSI5_CLK_N, HS_CSI5_D1_P/N		5:1						
HS_CSI6_CLK_P, HS_CSI6_D0_P/N	3	6:0						√
HS_CSI6_CLK_N, HS_CSI6_D1_P/N		6:1						√
HS_CSI7_CLK_P, HS_CSI7_D0_P/N		7:0						√
HS_CSI7_CLK_N, HS_CSI7_D1_P/N		7:1						

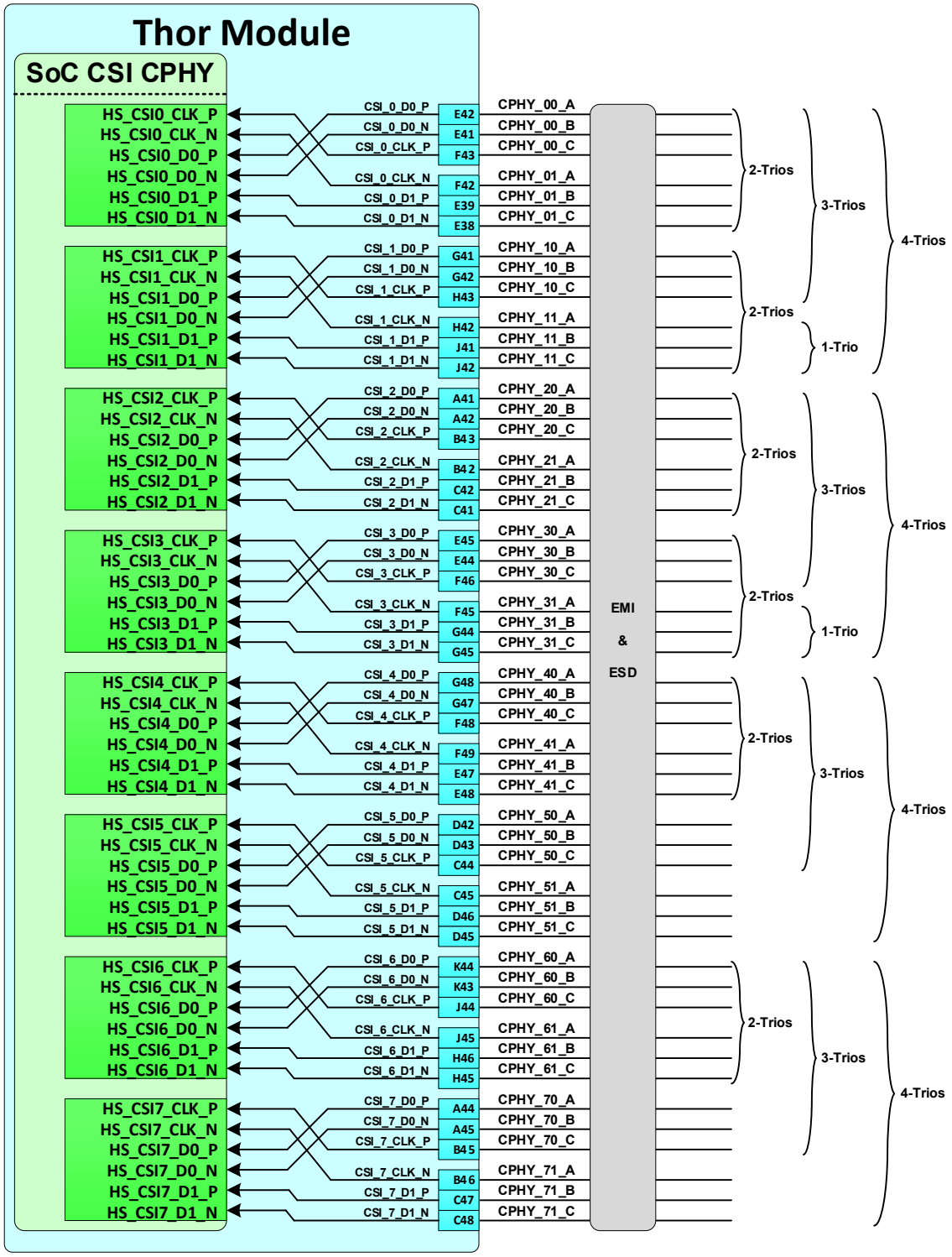
Note: Each of the above blocks (x4) can be swapped for one of the 2x2 or 1x4 configurations.

Figure 10-1. Camera CSI D-PHY Connections



Note: Any EMI/ESD devices must be tuned to minimize impact on signal quality and meet the timing and Vil/Vih requirements at the receiver and maintain signal quality and meet requirements for the frequencies supported by the design.

Figure 10-2. Camera CSI C-PHY Connections



Notes:

1. The mapping of CSI CPHY signals inside Thor to the Thor pins is programmable. The default mapping is shown in the figure. Other mappings are possible and may be required in some cases. Contact the NVIDIA Application Engineering team for further mapping information.
2. Any EMI/ESD devices must be tuned to minimize impact to signal quality and meet the timing and Vil/Vih requirements at the receiver and maintain signal quality and meet requirements for the frequencies supported by the design.

Table 10-5. MIPI CSI Signal Connections

Module Pin Name	Type	Termination	Description
DPHY Mode			
CSI[7:0]_CLK_N/P	DIFF IN	See note 1	CSI Diff. Clocks: Connect to clock pins of device. See note 2.
CSI[7:0]_D[1:0]_N/P	DIFF IN	See note 1	CSI Diff. Data Lanes: Connect to data pins of device. See note 2.
CPHY Mode			
CSI[7:0]_D0_P (Trio 0, A)	I	See note 1	CSI CPHY Trio 0, A: Connect to matching pin of device. See note 2.
CSI[7:0]_D0_N (Trio 0, B)	I	See note 1	CSI CPHY Trio 0, B: Connect to matching pin of device. See note 2.
CSI[7:0]_CLK_P (Trio 0, C)	I	See note 1	CSI CPHY Trio 0, C: Connect to matching pin of device. See note 2.
CSI[7:0]_D1_P (Trio 1, A)	I	See note 1	CSI CPHY Trio 1, A: Connect to matching pin of device. See note 2.
CSI[7:0]_D1_N (Trio 1, B)	I	See note 1	CSI CPHY Trio 1, B: Connect to matching pin of device. See note 2.
CSI[7:0]_CLK_N (Trio 1, C)	I	See note 1	CSI CPHY Trio 1, C: Connect to matching pin of device. See note 2.

Note:

1. Depending on the mechanical design of the platform and camera modules, ESD protection may be necessary. In addition, EMI control may be needed. Both are shown in the Camera Connection Example diagram. Any EMI/ESD solution must be compatible with the frequency required by the design.
2. See Configurations tables for details.

10.1 CSI D-PHY Design Guidelines

The following table details the signal routing requirements for CSI D-PHY interface.

Table 10-6. MIPI CSI D-PHY Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate (per data lane) for High-Speed mode Max Frequency (for Low Power mode)	2.5 10	Gbps MHz	
Number of Loads	1	load	
Max Loading (per pin)	10	pF	
Reference plane	GND		
Breakout Region Impedance (Single Ended)	45-50	Ω	±15%
Max PCB breakout delay	48	ps	
Trace Impedance Diff pair / Single Ended	90-100 / 45-50	Ω	
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Min Trace spacing	2x	Dielectric height	
Max Insertion loss 1 Gbps / 1.5 Gbps / 2.5 Gbps	 3.10 / 2.96 / 2.17	 dB	
Max trace length (delay) 1 Gbps 1.5 Gbps 2.5 Gbps	 435 (2610) 325 (1953) 170 (1018)	 mm (ps)	
Max Intra-pair Skew	1	ps	See Note 2
Max Trace Delay Skew between DQ and CLK 1 / 1.5 / 2.5 Gbps	 20/13.3/8	 ps	See Note 2, 3
Noise Coupling Avoidance	Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components		

Notes:

1. Up to four signal vias can share a single GND return via.
2. For DPHY only, not suitable support alters CPHY and DPHY mode.
3. Total system skew between DQ and CLK is ±0.1UI, in which PKG+CVM within ±0.03UI and connectors +flex+ 2nd PCB with camera module within ±0.05UI.

10.2 CSI C-PHY Design Guidelines

The following table details the signal routing requirements for CSI C-PHY interface.

Table 10-7. MIPI CSI C-PHY Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate (per trio)	4.5	Gsps	See notes 1 and 2
Topology	Point-Point		With RX Common Mode cap to GND
Termination	Fully ODT (on-die)		50ohms SE to common mode cap

Parameter	Requirement	Units	Notes
Max Loading (per pin)	2	pF	Single ended
Trace Impedance - Single Ended	45-50	Ω	±15%
Reference Plane	GND		
Max PCB breakout Length (Delay)	5 (30)	mm (ps)	
Via proximity (Signal via to GND return via)	< 2	mm	
Min Trace spacing	2.5x	Dielectric height	Recommendation
Inter Trio Trace spacing - Microstrip / Stripline	2x / 3x	Dielectric height	Recommend routing with loosely coupled differential impedance.
Max Insertion loss 4.5 Gsps @ 1.25GHz / 5GHz (w/o EQ) 4.5 Gsps @ 1.25GHz / 5GHz (w EQ) 3.5 Gsps @ 1.25GHz / 5GHz (w/o EQ) 2.5 Gsps @ 1.25GHz / 5GHz (w/o EQ) (Note-4)	 -0.78/ -3.76 -3.13/ -7.53 -1.4 / -7.27 -2.58/ -7.27	dB	Maximum loss of pkg+CVM is -0.87dB@1.25GHz and -2.47dB@5GHz
Max Trace Length total Direct from module conn. to device pins 4.5Gsps (w/o EQ) 4.5Gsps(w/ EQ) 3.5Gsps (w/o EQ) 2.5Gsps (w/o EQ) (Note-4)	 50.4 102 90.5 166.7	mm	It is strongly recommended that designs should be based on the loss guidelines, especially if any connectors are included in the path. The lengths provided are based on EM370 PCB Material with a dB/in loss of 0.393 for 1.25GHz and 1.036 for 5GHz. See Note 3
Max Intra-Trio Skew (Within Trios)	2	ps	A or B pin to C pin skew.
Max Inter-Trio Skew (between Trios)	55	ps	
Routing Layer Restrictions	A trio must route completely on the same layer. For DPHY compatibility, both Trio0 and Trio1 would need to route on the same layer (e.g., D0P/D0N must route on the same layer as CLKP/CLKN and thus so must D1P/D1N).		
Noise Coupling Avoidance	Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components		

Notes:

1. **Bit rate in bps is 2.286 * Gbps.**
2. **Maximum data rate may be limited by use case/memory bandwidth.**
3. **Note that the maximum lengths are estimations that do not include the loss from the end device or any connectors between the Jetson Thor connector and the end device. In addition, the effect of via transitions and reflections is not included. Any additional losses (including difference in loss coefficient for PCB material) should be considered and the maximum length recalculated.**
4. **Qualified maximum speed. Contact your NVIDIA support team if your application needs higher speed.**

Table 10-8. Recommended CSI Test Points for Initial Boards

Test Points Recommended	Location
One for each signal line.	Near Thor module pins.

Note: Test points must be done carefully to minimize signal integrity impact. Avoid stubs and keep pads small and near signal traces.

Table 10-9. Connector Specification

Parameter	CPHY Only	DPHY only	CPHY & DPHY
Characteristic impedance (z0)	SE : 45ohms – 50ohms Diff (A-B, B-C, C-A): 120ohm~80ohm	90ohms differential	SE : 45ohms – 50ohms Diff (A-B, B-C, C-A): 120ohm~80ohm
Loss	Diff (A-B, B-C, C-A): < 0.2dB@1.25GHz. < 0.5dB@5GHz	Diff (P-N): < 0.2dB@1.25GHz.	Fully GND referenced
SDD11	Diff (A-B, B-C, C-A): < -15dB@0~450MHz < -10dB@0.45~3.375GHz	Diff (P-N): < -15dB@0~450MHz < -10dB@1.25GHz	Diff (A-B, B-C, C-A): -15dB@0~450MHz -10dB@0.45~3.375GHz
SCC11	(A-B, B-C, C-A) < -2.5dB (0 to 3.375GHz)	< -2.5dB (0 to 1.25GHz)	(A-B, B-C, C-A) < -2.5dB (0 to 3.375GHz)
SDC11	(A-B, B-C, C-A) < -29dB (0 to 3.375GHz)	< -26dB (0 to 1.25GHz)	(A-B, B-C, C-A) < -29dB (0 to 3.375GHz)
SDC21	(A-B, B-C, C-A) < -26dB (0 to 3.375GHz)	N/A	(A-B, B-C, C-A) < -26dB (0 to 3.375GHz)
Cross coupling (SDD21-SCC21)	<-18dB (0 to 3.375GHz)	N/A	<-18dB (0 to 3.375GHz)

Note: When select connector takes care of “mode conversion” (SDC11 and SDC21) for CPHY mode (A-B, B-C, C-A).

Chapter 11. Audio

The Jetson Thor brings several PDM and I2S audio interfaces to the module.

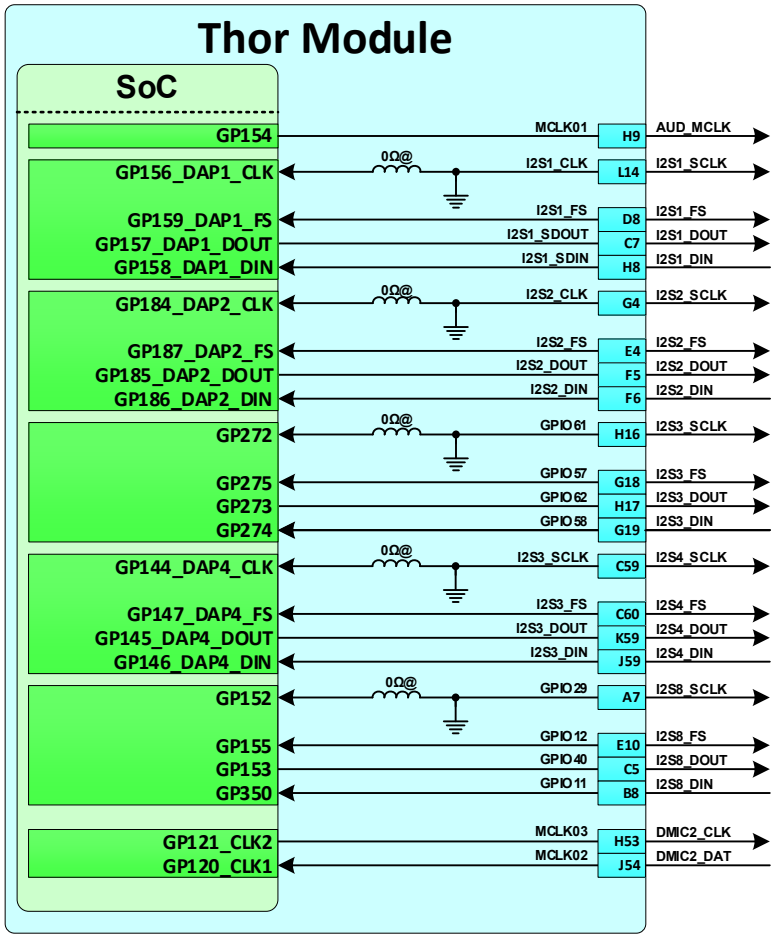
Table 11-1. Jetson Thor Audio Pin Description

Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type
H9	MCLK01	GP154	Audio Codec Reference Clock	Output	CMOS – 1.8V
L14	I2S1_CLK	GP156_DAP1_CLK	I2S Audio Port 1 Clock	Bidir	CMOS – 1.8V (I2S1)
D8	I2S1_FS	GP159_DAP1_FS	I2S Audio Port 1 Left/Right Clock	Bidir	
C7	I2S1_SDOUT	GP157_DAP1_DOUT	I2S Audio Port 1 Data Out	Output	
H8	I2S1_SDIN	GP158_DAP1_DIN	I2S Audio Port 1 Data In	Input	
G4	I2S2_CLK	GP184_DAP2_CLK	I2S Audio Port 2 Clock	Bidir	CMOS – 1.8V (I2S2)
E4	I2S2_FS	GP187_DAP2_FS	I2S Audio Port 2 Left/Right Clock	Bidir	
F5	I2S2_DOUT	GP185_DAP2_DOUT	I2S Audio Port 2 Data Out	Output	
F6	I2S2_DIN	GP186_DAP2_DIN	I2S Audio Port 2 Data In	Input	
H16	GPIO61	GP272	I2S Audio Port 3 Clock	Bidir	CMOS – 1.8V (I2S3)
G18	GPIO57	GP275	I2S Audio Port 3 Left/Right Clock	Bidir	
H17	GPIO62	GP273	I2S Audio Port 3 Data Out	Output	
G19	GPIO58	GP274	I2S Audio Port 3 Data In	Input	
C59	I2S3_SCLK	GP144_DAP4_CLK	I2S Audio Port 4 Clock	Bidir	CMOS – 1.8V (I2S4)
C60	I2S3_FS	GP147_DAP4_FS	I2S Audio Port 4 Left/Right Clock	Bidir	
K59	I2S3_DOUT	GP145_DAP4_DOUT	I2S Audio Port 4 Data Out	Output	
J59	I2S3_DIN	GP146_DAP4_DIN	I2S Audio Port 4 Data In	Input	
A7	GPIO29	GP152	I2S Audio Port 8 Clock	Bidir	CMOS – 1.8V (I2S8)
E10	GPIO12	GP155	I2S Audio Port 8 Left/Right Clock	Bidir	
C5	GPIO40	GP153	I2S Audio Port 8 Data Out	Output	
B8	GPIO11	GP350	I2S Audio Port 8 Data In	Input	
H53	MCLK03	GP121_CLK2	Digital Mic Input 2 Clock	Output	CMOS – 1.8V
J54	MCLK02	GP120_CLK1	Digital Mic Input 2 Data	Input	

Notes:

1. In the Direction column, Output is from Jetson Thor; Input is to Jetson Thor. Bidir is for Bidirectional signals.
2. The direction indicated for MCLKx, I2Sx, and GPIOx are associated with their use as I2S or MCLK signals. The pins support GPIO functionality, so they support both input and output operation (bidirectional).

Figure 11-1. Audio Device Connections



Notes:

1. The I2S interfaces can be used in either Initiator or target mode.
2. A capacitor from I2Sn_FS to GND should be included if SoC is an I2S target and the edge_cntrl configuration = 1 (SDATA driven on positive edge of CLK). The value of the capacitor should be chosen to provide a minimum of 2ns hold time for the I2Sn_FS edge after the rising edge of I2Sn_CLK.

Table 11-2. Audio Interface Signal Connections

Module Pin Name	Type	Termination	Description
I2Sx_CLK (I2Sx_SCLK)	I/O	0Ω Bead in series and 2.7pF capacitor to GND (on Thor module).	I2S Serial Clock: Connect to I2S/PDM CLK pin of audio device.
I2Sx_FS (I2Sx_LRCK)	I/O		I2S Left/Right Clock: Connect to Left/Right Clock pin of audio device.
I2Sx_DOUT (I2Sx_SDOUT)	O		I2S Data Output: Connect to Data Input pin of audio device.

Module Pin Name	Type	Termination	Description
I2Sx_DIN (I2Sx_SDIN)	I		I2S Data Input: Connect to Data Output pin of audio device.
(DMICx_CLK)	O		DMIC Clock: Connect to Digital Microphone device clock pin.
(DMICx_DAT)	I		DMIC Data: Connect to Digital Microphone device data pin.
(AUD_MCLK)	O		Audio Codec Reference Clock: Connect to clock pin of Audio Codec.

11.1 I2S Design Guidelines

The following table details the signal routing requirements for the I2S interface.

Table 11-3. I2S Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Configuration / Device Organization	1	load	
Max Loading	8	pF	
Reference plane	GND		
Breakout Region Impedance	Min width/spacing		
Trace Impedance	50	Ω	±20%
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note
Trace spacing - Microstrip or Stripline	2x	dielectric height	
Max Trace Delay	3600 (~560)	ps (mm)	
Max Trace Delay Skew between SCLK and SDATA_OUT/IN	250 (40)	ps (mm)	

Note: Up to four signal Vias can share a single GND return Via

11.2 DMIC Design Guidelines

The following table details the signal routing requirements for the DMIC interface.

Table 11-4. DMIC Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Clock Frequency/Period	12/83.33	MHz/ns	
Data Bit rate/Period (DDR24)	24/41.66	Mbps/ns	
Configuration/Device Organization	1	load	
Topology	Point to Point		
Reference plane	GND		
Trace Impedance	45-50	Ω	±20%
Via proximity (Signal via to GND return via)	< 3.8 (24)	mm (ps)	See Note
Trace spacing – Microstrip/Stripline	2x / 2x	dielectric height	
Max Trace Delay	1280	ps	
Max Trace Delay Skew between CLK and DAT	150	ps	

Note: Up to four signal vias can share a single GND return via.

Chapter 12. I2C

The Jetson Thor brings multiple I2C interfaces to the module pins.

Table 12-1. Jetson Thor I2C Pin Description

Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type
J52	I2C0_CLK	GP190_I2C0_CLK	General I2C 0 Clock	Bidir	Open-Drain – 1.8V (Back-drive capable to 1.8V)
J53	I2C0_DAT	GP191_I2C0_DAT	General I2C 0 Data		
K5	I2C1_CLK	GP188_I2C1_CLK	General I2C 1 Clock		
L8	I2C1_DAT	GP189_I2C1_DAT	General I2C 1 Data		
J61	I2C2_CLK	GP10_I2C2_CLK	General I2C 2 Clock		
K61	I2C2_DAT	GP11_I2C2_DAT	General I2C 2 Data		
D61	I2C4_CLK	GP12_I2C3_CLK	General I2C 3 Clock		
E60	I2C4_DAT	GP13_I2C3_DAT	General I2C 3 Data		
E19	DP_AUX_CH2_P	SF_DPAUX2_P	Display Port 2 Aux+ or HDMI DDC SCL. AC-Coupled on Carrier Board for DP AUX (DP) or pulled high for DDC/I2C.		
E18	DP_AUX_CH2_N	SF_DPAUX2_N	Display Port 2 Aux– or HDMI DDC SDA. AC-Coupled on Carrier Board for DP AUX (DP) or pulled high for DDC/I2C.		
G53	DP_AUX_CH0_P	SF_DPAUX0_P	Display Port 0 Aux+ or HDMI DDC SCL. AC-Coupled on Carrier Board for DP AUX (DP) or pulled high for DDC/I2C.		
G54	DP_AUX_CH0_N	SF_DPAUX0_N	Display Port 0 Aux– or HDMI DDC SDA. AC-Coupled on Carrier Board for DP AUX (DP) or pulled high for DDC/I2C.		
F52	I2C8_CLK	GP259_I2C7_CLK	General I2C 7 Clock		
F51	I2C8_DAT	GP260_I2C7_DAT	General I2C 7 Data		
F20	DP_AUX_CH3_P	SF_DPAUX3_P	Display Port 3 Aux+ or HDMI DDC SCL. AC-Coupled on Carrier Board for DP AUX (DP) or pulled high for DDC/I2C.		
F21	DP_AUX_CH3_N	SF_DPAUX3_N	Display Port 3 Aux– or HDMI DDC SDA. AC-Coupled on Carrier Board for DP AUX (DP) or pulled high for DDC/I2C.		
A53	I2C5_CLK	GP261_I2C9_CLK	General I2C 9 Clock		
C53	I2C5_DAT	GP262_I2C9_DAT	General I2C 9 Data		
D16	DP_AUX_CH1_P	SF_DPAUX1_P	Display Port 1 Aux+ or HDMI DDC SCL. AC-Coupled on Carrier Board for DP AUX (DP) or pulled high for DDC/I2C.		

Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type
D17	DP_AUX_CH1_N	SF_DPAUX1_N	Display Port 1 Aux– or HDMI DDC SDA. AC-Coupled on Carrier Board for DP AUX (DP) or pulled high for DDC/I2C.	Bidir	Open-Drain – 1.8V (Back-drive capable to 1.8V)
E27	I2C7_CLK	GP160_I2C11_CLK	General I2C 11 Clock		
E26	I2C7_DAT	GP161_I2C11_CLK	General I2C 11 Data		
F53	I2C3_CLK	GP122_I2C12_CLK	General I2C 12 Clock		
E53	I2C3_DAT	GP123_I2C12_DAT	General I2C 12 Data		
H55	MCLK04	GP129	General I2C 15 Clock		
L57	MCLK05	GP130	General I2C 15 Data		

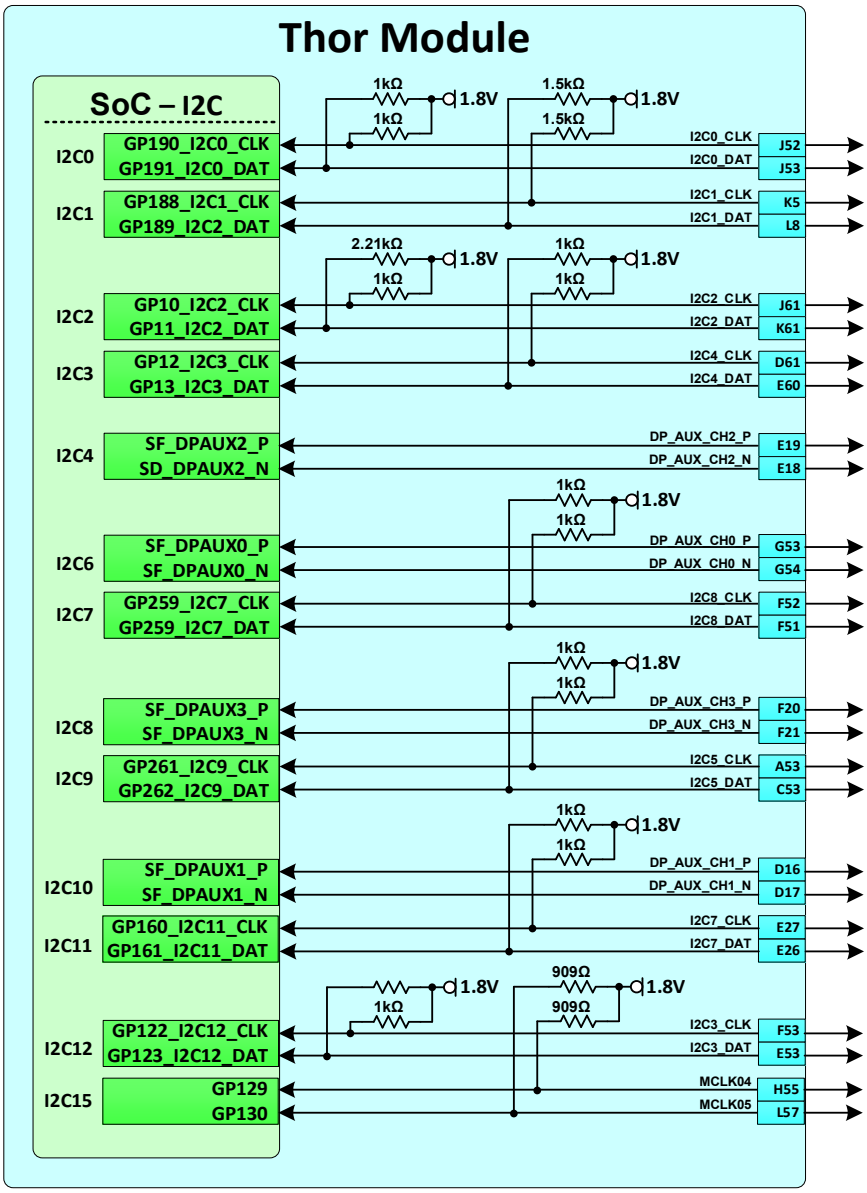
Note: In the Direction column, Output is from Jetson Thor; Input is to Jetson Thor. Bidir is for Bidirectional signals.

Table 12-2. I2C Interface Mapping

Ctrlr	Module Pin Names	Usage on Module	Thor Block	On-Module Pull-up/voltage
I2C0	I2C0_CLK/DAT		N	1KΩ to 1.8V
I2C1	I2C1_CLK/DAT	ID EEPROM (7h50)	N	1.5KΩ to 1.8V
I2C2	I2C2_CLK/DAT	Power Monitor (7H40	A_AO	2.21KΩ to 1.8V (also Power Monitor via level shifter)
I2C3	I2C4_CLK/DAT		A_AO	1KΩ to 1.8V
I2C4	DP_AUX_CH2_P/N		K	None
I2C6	DP_AUX_CH0_P/N		K	None
I2C7	I2C8_CLK/DAT		K	1KΩ to 1.8V
I2C8	DP_AUX_CH3_P/N		K	None
I2C9	I2C5_CLK/DAT		K	1KΩ to 1.8V
I2C10	DP_AUX_CH1_P/N		K	None
I2C11	I2C7_CLK/DAT		L	1KΩ to 1.8V
I2C12	I2C3_CLK/DAT		L	1KΩ to 1.8V
I2C15	MCLK04/MCLK05		L	1KΩ to 1.8V

Note: The DP_AUX_CH[3:0]_P/N pins support either I2C or DP_AUX functionality. DP_AUX is used for DP if this is implemented. HDMI uses the pins for DDC (I2C). Since the I2C and DP_AUX share the same pins, only one can be used in a design.

Figure 12-1. I2C Connections



Notes:

1. For I2C interfaces that have on-module pull-ups to 1.8V, the carrier board should either not have additional pull-ups, or only to 1.8V.
2. Any I2C pull-ups on the carrier board must be connected to power rails that are off when the Jetson Thor is off.
3. If I2C interfaces are routed to M.2 Key E or Key M connectors, it is recommended that 0Ω series resistors be included to allow these to be disconnected. Some M.2 Key E and Key M cards can cause conflicts with other devices connected to the I2C interfaces.

Table 12-3. I2C Signal Connections

Module Pin Name	Type	Termination	Description
I2Cx_CLK/DAT	I/OD	1kΩ pull-ups to 1.8V on module	General I2C Clock/Data. Connect to CLK/Data pins of 1.8V devices
DP_AUX_CHx_P/N	I/OD	See HDMI/DP sections for correct termination	DP_AUX Channel (DP) or DDC I2C to Clock and Data (HDMI). Connect to AUX_CH_P/N (DP) or SCL/SDA (HDMI). Alternately available as I2C interface.

Note: If some devices require a different voltage level than others connected to the same I2C bus, level shifters are required.

12.1 I2C Design Guidelines

Care must be taken to ensure I2C peripherals on the same I2C bus connected to Jetson Thor do not have duplicate addresses. Addresses can be in two forms: 7-bit, with the Read/Write bit removed, or 8-bit including the Read/Write bit.

Make sure I2C device addresses are compared using the same form -- all 7-bit or all 8-bit format.

Table 12-4. I2C Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency - Standard-mode / Fm / Fm+	100 / 400 / 1000	kHz	See Note 1
Topology	Single ended, bi-directional, multiple initiators / targets		
Max Loading - Standard-mode / Fm / Fm+	400	pF	Total of all loads
Reference plane	GND or PWR		
Trace Impedance	50 – 60	Ω	±15%
Trace Spacing	1x	dielectric height	
Max Trace Delay Standard Mode Fm and Fm+	 3400 (~500) 1700 (~10)	 ps (mm)	

Notes:

1. **Fm = Fast-mode, Fm+ = Fast-mode Plus**
2. **Avoid routing I2C signals near noisy traces, supplies or components, such as a switching power regulator.**
3. **No requirement for decoupling caps for PWR reference**

12.2 De-bounce

The following table contains the allowable De-bounce settings for the various I2C modes.

Table 12-5. De-bounce Settings

I2C Mode	Clock Source	Source Clock Freq	I2C Source Divisor	Sm/Fm Divisor	De-bounce Value	I2C SCL Freq
Fm+	PLLP_OUT0	408MHz	5 (0x04)	10 (0x9)	0	1016KHz
					5:1	905.8KHz
					7:6	816KHz
Fm	PLLP_OUT0	408MHz	5 (0x4)	26 (0x19)	7:0	392KHz
Sm	PLLP_OUT0	408MHz	20 (0x13)	26 (0x19)	7:0	98KHz

Note: sm = standard mode

Chapter 13. SPI

Jetson Thor provides multiple Serial Peripheral interfaces (SPI), as listed in the following table.

Table 13-1. Jetson Thor SPI Pin Description

Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type
J57	SPI1_CLK	GP115_SPI1_CLK	SPI 1 Clock	Bidir	CMOS - 1.8V
D55	SPI1_MOSI	GP117_SPI1_MOSI	SPI 1 Initiator Out / Target In		
A56	SPI1_MISO	GP116_SPI1_MISO	SPI 1 Initiator In / Target Out		
E55	SPI1_CS0_N	GP118_SPI1_CS0_N	SPI 1 Chip Select 0		
B56	SPI1_CS1_N	GP119_SPI1_CS1_N	SPI 1 Chip Select 1		
E61	SPI2_CLK	GP17_SPI2_CLK	SPI 2 Clock	Bidir	CMOS - 1.8V
F60	SPI2_MOSI	GP19_SPI2_MOSI	SPI 2 Initiator Out / Target In		
D62	SPI2_MISO	GP18_SPI2_MISO	SPI 2 Initiator In / Target Out		
D60	SPI2_CS0_N	GP20_SPI2_CS_N	SPI 2 Chip Select 0		
F55	SPI3_CLK	GP104_SPI3_CLK	SPI 3 Clock	Bidir	CMOS - 1.8V
G56	SPI3_MOSI	GP106_SPI3_MOSI	SPI 3 Initiator Out / Target In		
D56	SPI3_MISO	GP105_SPI3_MISO	SPI 3 Initiator In / Target Out		
C57	SPI3_CS0_N	GP107_SPI3_CS0_N	SPI 3 Chip Select 0		
E56	SPI3_CS1_N	GP108_SPI3_CS1_N	SPI 3 Chip Select 1		

Notes:

1. The Direction depends on whether Thor is the initiator or target. If Thor is initiator, the clock, chip select and MOSI are outputs and MISO is an input. If Thor is target, the clock, chip select and MOSI are inputs and MISO is an output.
2. In the Direction column, Output is from Jetson Thor; Input is to Jetson Thor. Bidir is for Bidirectional signals.

Figure 13-1. Jetson Thor SPI Connections

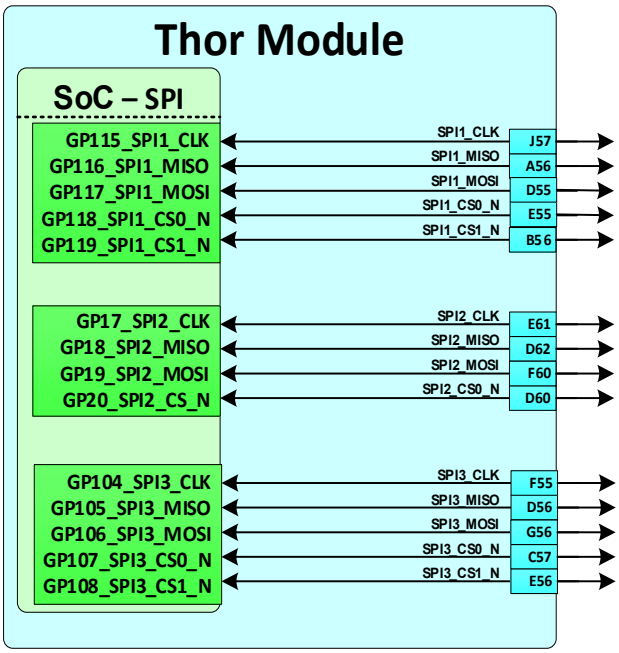


Figure 13-2. Basic SPI Connections

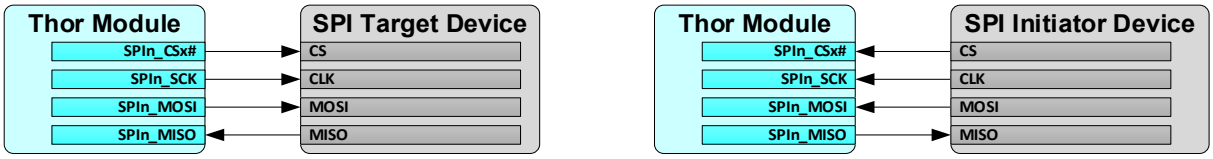


Table 13-2. SPI Signal Connections

Module Pin Names	Type	Termination	Description
SPIx_CLK	I/O		SPI Clock: Connect to Peripheral CLK pin(s)
SPIx_MOSI	I/O		SPI Data Output: Connect to Peripheral MOSI pin(s)
SPIx_MISO	I/O		SPI Data Input: Connect to Peripheral MISO pin(s)
SPIx_CS[1:0]_N	I/O		SPI Chip Selects: Connect one CS_N pin per SPI IF to each target Peripheral CS pin

13.1 SPI Design Guidelines

The following figure shows the SPI topologies.

Figure 13-3. SPI Topologies

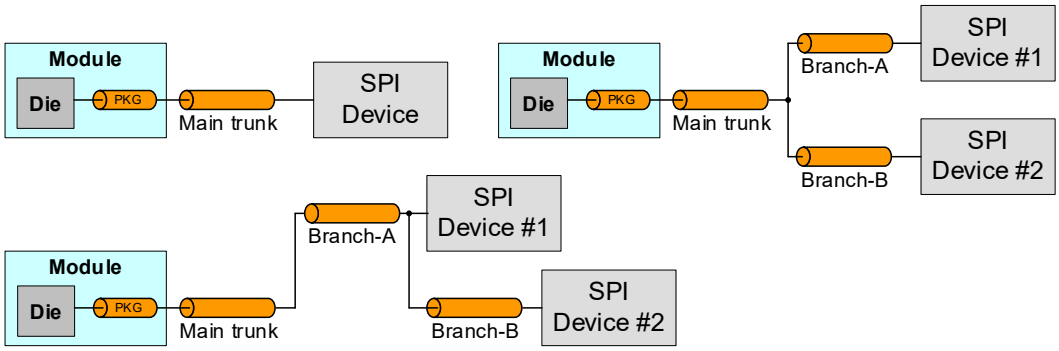


Table 13-3. SPI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency SDR32.5 (SPI devices w/Fmax >50MHz) SDR25 (SPI devices w/Fmax <50MHz) SDR15 (applies to 2-load topologies)	 65 50 30	MHz	
Configuration / Device Organization	3	load	
Max Loading (per pin)	10	pF	
Trace Impedance	45-50	Ω	±15%
Reference plane	GND or PWR		See note 1
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See note 2
Trace spacing - Microstrip / Stripline	3x / 2x	dielectric height	
PCB noise avoidance	3x	dielectric height	
Max PCB breakout delay	6.5 (40)	mm (ps)	
Max Trace Length (Delay) for MOSI, MISO, SCK and CS	109 (685)	mm (ps)	
Max Trace Length (Delay) Skew from MOSI, MISO and CS to SCK	16 (100)	mm (ps)	At any point

Notes:

1. **If PWR, add 2x 0201 0.1uF and 2x 0402 4.7uF decoupling capacitors between PWR and GND for return current.**
2. **Up to four signal vias can share a single GND return via.**

Table 13-4. Recommended SPI Test Points for Initial Boards

Test Points Recommended	Location
One for each SPI signal line used	Near Thor module and Device pins.

Chapter 14. UART

Jetson Thor brings multiple UARTs out to the main connector as listed in Table 14-1.

Table 14-1. Jetson Thor UART Pin Description

Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type
K53	UART1_TX	GP134_UART9_TXD	UART 9 Transmit	Output	CMOS – 1.8V
K54	UART1_RX	GP135_UART9_RXD	UART 9 Receive	Input	
L51	UART1_RTS	GP136_UART9_RTS_N	UART 9 Request to Send	Output	
H54	UART1_CTS	GP137_UART9_CTS_N	UART 19 Clear to Send	Input	
C58	UART2_TX	GP100_UART10_TXD	UART 10 Transmit	Output	CMOS – 1.8V
C56	UART2_RX	GP101_UART10_RXD	UART 10 Receive	Input	
G58	UART2_RTS	GP102_UART10_RTS_N	UART 10 Request to Send	Output	
A57	UART2_CTS	GP104_UART10_CTS_N	UART 10 Clear to Send	Input	
H62	UART3_TX_DEBUG	GP15_UART0_TX	UART 0 Transmit	Output	CMOS – 1.8V
K60	UART3_TX_DEBUG	GP16_UART0_RX	UART 0 Receive	Input	
J58	UART5_TX	GP109_UART5_TXD	UART 5 Transmit	Output	CMOS – 1.8V
H58	UART5_RX	GP110_UART5_RXD	UART 5 Receive	Input	
K58	UART5_RTS	GP111_UART5_RTS_N	UART 5 Request to Send	Output	
H57	UART5_CTS	GP112_UART5_CTS_N	UART 5 Clear to Send	Input	

Notes:

1. In the Direction column, Output is from Jetson Thor; Input is to Jetson Thor. Bidir is for bidirectional signals.
2. The direction indicated for the UART pins is true when used for that function. Otherwise, these pins support GPIO functionality and can support both input and output (bidirectional).
3. Some functions are shared with other functions. Only one function can be used in a design. Ensure no conflicts exist when choosing the functions for a design.

Figure 14-1. Jetson Thor UART Connections

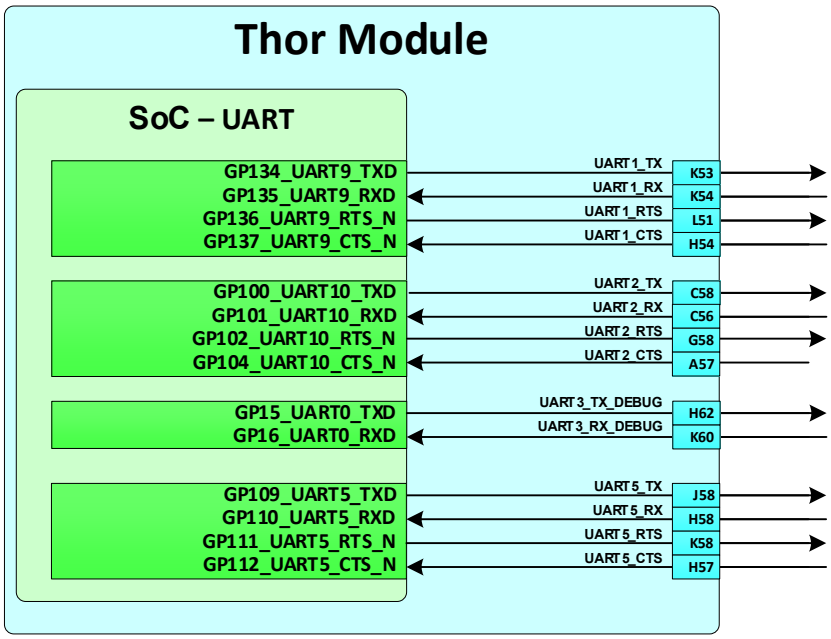


Table 14-2. UART Signal Connections

Module Pin Name	Type	Termination	Description
UARTx_TX	O		UART Transmit: Connect to Peripheral RXD pin of device
UARTx_RX	I		UART Receive: Connect to Peripheral TXD pin of device
UARTx_CTS	I		UART Clear to Send: Connect to Peripheral RTS_N pin of device
UARTx_RTS	O		UART Request to Send: Connect to Peripheral CTS pin of device

14.1 UART Design Guidelines

The following table contains the signal routing requirements for the UART interface.

Table 14-3. UART Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate	4.25	Mbps	
Configuration / Device Organization	1	load	
Reference plane	GND		
Trace Impedance	40-60	Ω	±10%
Breakout	75	ps	
Via proximity (Signal via to GND return via)	< 3.8 (24)	mm (ps)	See note 1
Min Trace spacing Microstrip / Stripline	4x / 3x	Dielectric height	
Max Trace Length (Delay)	355 (2268)	mm (ps)	Assuming 6.3 ps/mm propagation delay.
Max Trace Delay Skew from RXD to TXD	38 (240)	mm (ps)	Assuming 6.3 ps/mm propagation delay.

Note: Up to four signal vias can share a single GND return via

Chapter 15. CAN

The Jetson Thor brings four Controlled Area Network (CAN) interfaces out to the main connector.

Table 15-1. Jetson Thor CAN Pin Descriptions

Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type
G38	FSI_GPIO07/CAN0_DOUT	GP200_CAN0_DOUT	CAN 0 Transmit	Output	CMOS – 3.3V
G39	FSI_GPIO08/CAN0_DIN	GP201_CAN0_DIN	CAN 0 Receive	Input	CMOS – 3.3V
H37	FSI_GPIO09/CAN1_DOUT	GP205_CAN1_DOUT	CAN1 Transmit	Output	CMOS – 3.3V
H36	FSI_GPIO10/CAN1_DIN	GP206_CAN1_DIN	CAN1 Receive	Input	CMOS – 3.3V
D59	CAN2_DOUT	GP210_CAN2_DOUT	CAN 2 Transmit	Output	CMOS – 3.3V
F58	CAN2_DIN	GP211_CAN2_DIN	CAN 2 Receive	Input	CMOS – 3.3V
H61	CAN3_DOUT	GP215_CAN3_DOUT	CAN 3 Transmit	Output	CMOS – 3.3V
B61	CAN3_DIN	GP216_CAN3_DIN	CAN 3 Receive	Input	CMOS – 3.3V

Notes:

1. In the Direction column, Output is from Jetson Thor; Input is to Jetson Thor. Bidir is for Bidirectional signals.
2. The direction indicated for CANx is associated with their use as CAN DOUT/DIN.
3. CAN PHY is not included in the Thor module.

Figure 15-1. Jetson Thor CAN Connections

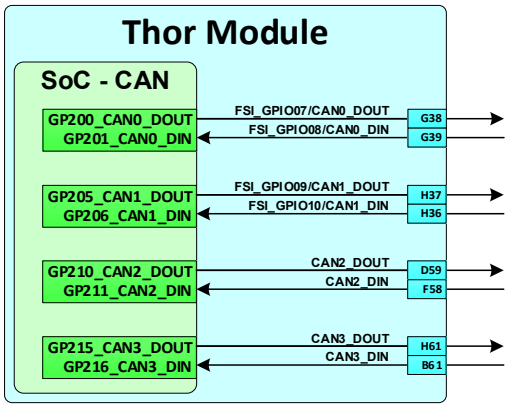


Table 15-2. CAN Signal Connections

Module Pin Name	Type	Termination	Description
CANx_DOUT	O		CAN Data Output: Connect to matching pin of device
CANx_DIN	I		CAN Input: Connect to Peripheral pin of device
GPIOx (CANx_STB)	O		CAN Standby mode control Output: Connect to STB pin of device
GPIOx (CANx_EN)	O		CAN Enable Output: Connect to EN pin of device
GPIOx (CANx_ERR)	I		CAN Error Input: Connect to ERR pin of device

15.1 CAN Design Guidelines

The following table contains the signal routing requirements for the CAN interface between Thor module and CAN PHY.

Table 15-3. CAN Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate / Frequency	8	Mbps / MHz	
Configuration / Device Organization	1	load	
Trace Impedance	50	Ω	±15%
Reference plane	GND or PWR		See note 1
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See note 2
Trace spacing - Microstrip / Stripline	3x / 2x	dielectric height	
PCB noise avoidance	3x	dielectric height	
Max PCB breakout length (delay)	6.5 (40)	mm (ps)	
Max Trace Length (delay)	307 (1933)	mm (ps)	
Max Trace Skew Length (Delay)	8 (50)	mm (ps)	

Note:

1. **If PWR, add 2x 0201 0.1uF and 2x 0402 4.7uF decoupling capacitors between PWR and GND for return current.**
2. **Up to four signal vias can share a single GND return via.**

Chapter 16. Fan

Jetson Thor provides PWM and Tachometer functionality for controlling a fan as part of the thermal solution.

- The **FAN_PWM** pin is configured as **GP_PWM4**
- The **FAN_TACH** pin is configured as **NV_THERM_FAN_TACH0**

Table 16-1. Jetson Thor Fan Pin Descriptions

Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type
E54	FAN_TACH	GP126_FAN_TACH0	Fan Tachometer signal	Input	CMOS – 1.8V
K62	FAN_PWM	GP14_PWM4	Fan Pulse Width Modulation signal	Output	Open-Drain, 1.8V

Notes:

1. In the Direction column, Output is from Jetson Thor; Input is to Jetson Thor. Bidir is for Bidirectional signals.
2. The direction indicated for FANx is associated with their use as Fan PWM/Tach. The pins support GPIO functionality, so support both input and output operation (bidirectional).

Figure 16-1. Jetson Thor Fan Connection Example

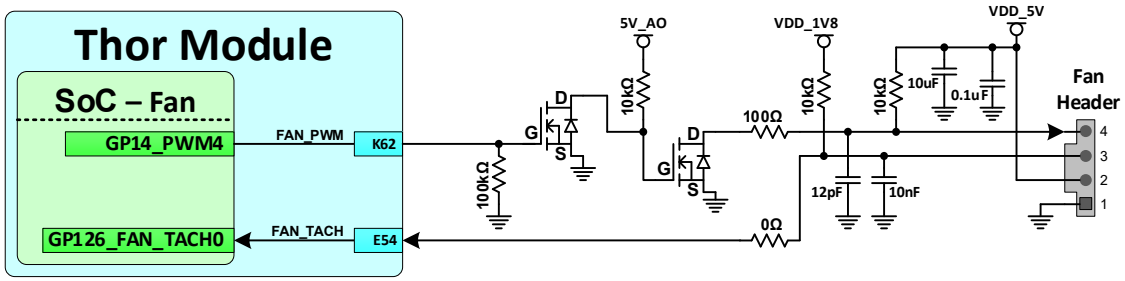


Table 16-2. Fan Signal Connections

Pin #	Module Pin Name	Type	Termination	Description
K62	FAN_PWM	O	100kΩ pulldown to GND, FET. 4.7kΩ pullup to VDD_5V, FET, series 100Ω resistor, and 10kΩ pullup to VDD_5V.	Fan Pulse Width Modulation: Connect through FET as shown in the Thor module Fan Connections figure.
E54	FAN_TACH	I	100kohm pullup to VDD_1V8	Fan Tachometer: Connect to TACH pin on fan connector.

Chapter 17. Debug

This chapter covers the interfaces that are provided for debug and development.

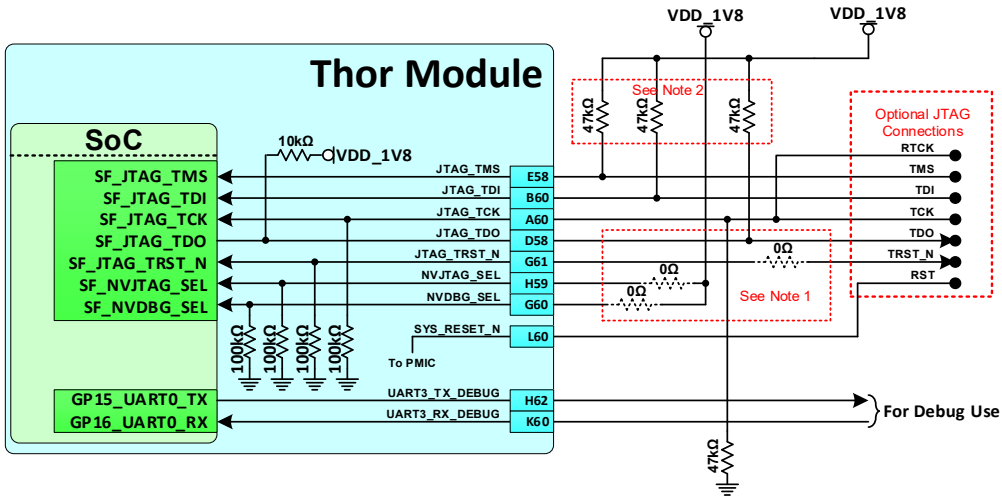
17.1 USB Recovery Mode

USB Recovery mode provides an alternate boot device (USB). In this mode, the system is connected to a host system and boots over USB. This is used when a new image needs to be flashed, or for debug purposes. To enter USB recovery mode, the **FORCE_RECOVERY_N** pin is held low when the system is powered on. **FORCE_RECOVERY_N** is the SoC RCM0 strap. Recovery mode can operate in either USB 2.0 or USB 2.0 + USB 3.2 modes. Recovery mode using USB 2.0 is from interface **USB0_N/P** only. No other signals are required or supported for entering Force Recovery mode. Neither VBUS nor ID detection is needed. If the force recovery strap is held low coming out of reset, Jetson Thor will configure USB0 as a device and enter recovery mode. For USB 3.2 recovery mode, the USB 3.2 port must be Port #1 on the UPHY_RX1/TX1 pins.

17.2 JTAG and Debug UART

The following figure shows the JTAG and UART debug connections.

Figure 17-1. JTAG and UART Debug Connections

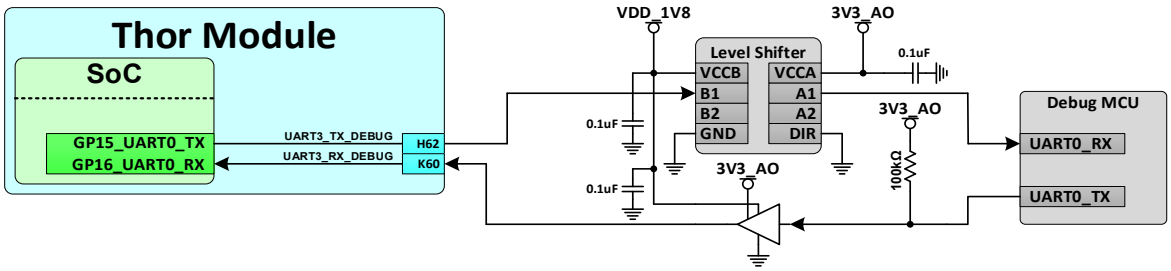


Notes:

1. NVJTAG_SEL and JTAG_TRST_N must be low for normal operation and pulled to 1.8V for Boundary Scan Mode. NVDBG is left unconnected (pulled down on module) for normal operation and pulled to 1.8V for alternate debug modes (debug over USB, etc.). for Boundary Scan test mode, JTAG_TRST_N must be driven high in the proper sequence.
2. Refer to preferred JTAG debugger documentation for JTAG PU/PD recommendations.

A simplified example to bring the debug UART out is shown in the figure below. The **UART3_DEBUG** interface is shown routed to a debug MCU through level shifters.

Figure 17-2. Simple Debug UART Header Connections



Note: These features are used at NVIDIA for internal debugging and development purposes. These are not required, and support will not be provided if implemented. Designers have the option to implement something similar on their custom carrier boards but should develop their own circuit to meet their needs.

17.2.1 JTAG

JTAG is not required but may be useful for new design bring up or for boundary scan.

Table 17-1. Thor Module JTAG Pin Description

Pin #	Module Pin Name	SoC Ball Name	Usage/Description	Direction	Pin Type	MPIO Pad Code	Power-on Reset
H59	NVJTAG_SEL	SF_NVJTAG_SEL	NVIDIA JTAG Select. Low for normal operation or Arm® JTAG debug mode. High for scan test mode. Pulled to GND through 100kΩ resistor on module.	Input Input	CMOS – 1.8V	JT_RST	z
G60	NVDBG_SEL	SF_NVDBG_SEL	NVIDIA Debug Select. Pulled to GND through 100kΩ resistor on module.		CMOS – 1.8V	JT_RST	z
A60	JTAG_TCK	SF_JTAG_TCK	JTAG Test Clock. Pulled to GND through 100kΩ resistor on module.	Input	CMOS – 1.8V	JT_RST	z
E58	JTAG_TMS	SF_JTAG_TMS	JTAG Test Mode Select	Input	CMOS – 1.8V	JT_RST	pu
D58	JTAG_TDO	SF_JTAG_TDO	JTAG Test Data Out	Output	CMOS – 1.8V	ST	z
B60	JTAG_TDI	SF_JTAG_TDI	JTAG Test Data In	Input	CMOS – 1.8V	JT_RST	pu
G61	JTAG_TRST_N	SF_JTAG_TRST_N	JTAG Test Reset. Low for normal operation or Arm JTAG debug mode. High for scan test mode. Pulled to GND through 100kΩ resistor on module.	Input	CMOS – 1.8V	JT_RST	pd

Notes:

1. In the Direction column, Output is from Jetson Thor; Input is to Jetson Thor. Bidir is for Bidirectional signals.
2. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. “z” is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Table 17-2. JTAG Signal Connections

Module Pin Name	Type	Termination	Description
JTAG_TMS	I		JTAG Mode Select: Connect to TMS pin of connector
JTAG_TCK	I	100kΩ to GND on module	JTAG Clock: Connect to TCK pin of connector
JTAG_TDO	O		JTAG Data Out: Connect to TDO pin of connector
JTAG_TDI	I		JTAG Data In: Connect to TDI pin of connector
JTAG_RTCK	I		JTAG Return Clock: Connect to RTCK pin of connector
JTAG_TRST_N	I	100kΩ to GND and 0.1uF to GND on module	JTAG General Purpose Pin #0: Leave unconnected for normal or Arm JTAG operation. Connect to TRST pin of connector or similar for Boundary Scan test mode. See the *Thor Module Boundary Scan Requirements and Usage* document for details.
NVJTAG_SEL		100kΩ to GND on module	NVIDIA JTAG Select: Used as select > Normal operation: Must be low, so leave unconnected (on-module pulldown will keep low). > Scan test mode: Connect NVJTAG_SEL to VDD_1V8. See Chapter 19: Boundary Scan Test Mode for details.
NVDBG_SEL		100kΩ to GND on module	NVIDIA Debug Select: Used as select > Normal operation: Leave series resistor from NVDBG_SEL not stuffed. > Advanced Debug modes: Connect NVDBG_SEL to VDD_1V8 (install 0Ω resistor as shown).

17.2.2 Debug UART

Jetson Thor provides **UART3_DEBUG** for debug purposes. The connections are described in the following table.

Table 17-3. Debug UART Connections

Module Pin Name	Type	Termination	Description
UART3_TX_DEBUG	O		UART Transmit: Connect to RX pin of serial device
UART3_RX_DEBUG	I	If level shifter is implemented, 100 kΩ pull-up to supply on the non-Thor module side of the device.	UART Receive: Connect to TX pin of serial device

Chapter 18. Strapping Pins

Jetson Thor has one strap (**FORCE_RECOVERY_N**) that is intended to be used on the carrier board. The **FORCE_RECOVERY_N** strap is used to enter Force Recovery mode by holding it low during power-on. Several other straps mentioned in this section are reserved for use on the module by NVIDIA only. Their state at power-on must not be affected by any connections on the carrier board.

Straps need to be at a valid logic level from the rising edge of SYS_RESET_N and must remain valid for at least 12.5us afterwards. During this period, the SoC reads the values of the strap settings.

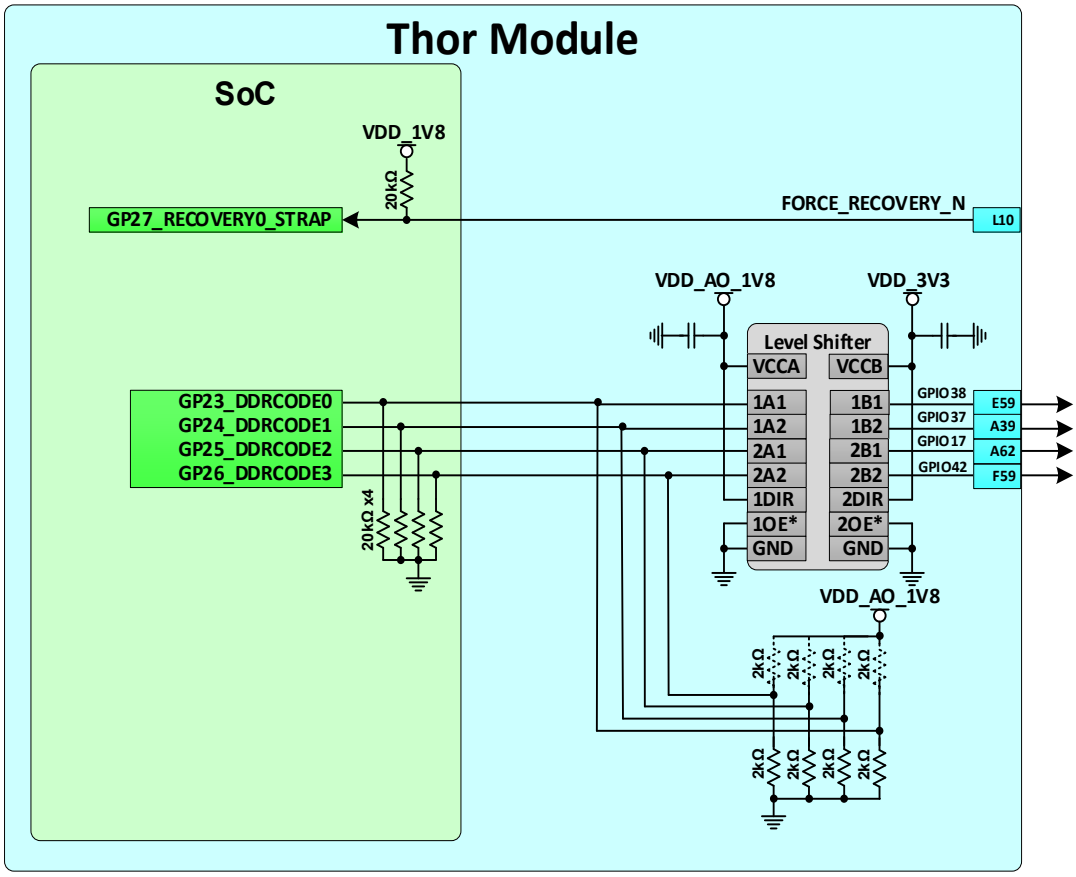
Table 18-1. Power-ON Strapping Breakdown

Strap Options	Module Pin Name	Description
RCM0	FORCE_RECOVERY_N	RECOVERY_MODE0 1: Regular Boot 0: Forced Recovery Mode. See note 1.
RAM_CODE	GPIO42 GPIO38 GPIO37 GPIO17	DRAM configuration. See Note 2.

Notes:

1. If no valid image is flashed in the QSPI NOR boot device in the module, it enters recovery mode automatically regardless of the state of the pin.
2. These pin statuses are subject to change and are not recommended for use as GPIO. Contact your NVIDIA Support Representative for additional questions.

Figure 18-1. Jetson Thor Module Strap Pins



Chapter 19. Pads

19.1 MPIO Pad Behavior when Associated Power Rail is Enabled

Jetson Thor CZ type MPIOs pins may glitch when the associated power rail is enabled or disabled. Designers should take this into account. MPIOs of this type that must maintain a low state even while the power rail is being ramped up or down may require special handling. The “Pin Descriptions” section of the Jetson Thor *Data Sheet* includes the pin type information.

19.2 Schmitt Trigger Usage

The MPIO pins have an option to enable or disable Schmitt Trigger mode on a per-pin basis. This mode is recommended for pins used for edge-sensitive functions such as input clocks, or other functions where each edge detected will affect the operation of a device. Schmitt Trigger mode provides better noise immunity and can help avoid extra edges from being “seen” by the SoC inputs. Input clocks include the I2S and SPI clocks when SoC is in target mode. The **FAN_TACH** pin is another input that could be affected by noise on the signal edges. The SPI**_SCK** pin, while used to output the clock to a SPI device, also samples the clock at the input to help with read timing. Therefore, the pin may benefit from enabling Schmitt Trigger mode. Care should be taken if the Schmitt Trigger mode setting is changed from the default initialization mode as this can influence interface timing.

19.3 Pins Pulled and Driven During Power-on

Jetson Thor is powered up before the carrier board (See Power Sequencing section). Some of the pins are pulled or driven high either by the SoC or by pull-up resistors on the module. The pins on the Jetson Thor that are pulled/driven high by the SoC can be found in the module pinmux spreadsheet. The pins that have pull-up resistors on the module are listed in the Jetson Thor “Signal Terminations” section of the “Design Checklist” chapter. Care must be taken on the carrier board design to ensure that any of these pins that connect to devices on the carrier board (or devices connected to the carrier board) do not cause damage or excessive leakage to those devices. Some of the ways to avoid issues with sensitive devices are:

- External pull-downs on the carrier board that are strong enough to keep the signals low are one solution, given that this does not affect the function of the pin. This will not work pins actively driven high by default.
- Buffers or level shifters can be used to separate the signals from devices that may be affected. The buffer and shifter should be disabled until the device power is enabled.

Chapter 20. Unused Interface Terminations

20.1 Unused MPIO Interfaces

The following Jetson Thor pins (and groups of pins) are Jetson Thor Multi-purpose Standard CMOS Pad (MPIO) pins that support either special function IOs (SFIO) and/or GPIO capabilities. Any unused pins or portions of pin groups listed in the table below that are not used can be left unconnected.

Table 20-1. Unused MPIO Pins and Pin Groups

Module Pins / Pin Groups	Module Pins / Pin Groups	Module Pins and Pin Groups
I2Sx	PEX_Cx_CLKREQ_N/RST_N	SLEEP_REQ_N
CANx	PEX_WAKE_N	MODULE_SHDN_N
FANx	PWMx	THERM_ALERT_N
SGMII	SPIx	POWER_BTN_N
GPIOx	SYSTEM_OC_N	NVJTAG_SEL
DP2x	WDT_RESET_OUT_N	NVDBG_SEL
I2Cx	VCOMP_ALERT_N	JTAGx
DPx_AUXx	MODULE_SLEEP_N	UARTx
MIDx	FORCE_RECOVERY_N	UFSx

20.2 Unused SFIO Interface Pins

The following table contains guidelines for unused dedicated special function I/O pins (SFIOs) for interfaces such as USB, PCIe, MGBE, HDMI, DisplayPort, and CSI.

Table 20-2. Unused SFIO Pin Terminations

Module Pin Name	Termination
USB 2.0	
USB[3:0]_N/P	Leave NC any unused pins
USB 3.2, PCIe, MGBE	
UPHY_TXx_N/P	Leave NC any unused TX lines
UPHY_RXx_N/P	Leave NC any unused RX lines or pull to GND through 10kohm resistors
UPHY_REFCLKx_N/P	Reference clock inputs: Leave NC or pull to GND through 10kohm resistors
PEX_CLKx_N/P	Reference clock outputs: Leave NC if not used
HDMI/DP	
HDMI_DP2_TX[3:0]_N/P	Leave NC any unused lanes
CSI	
CSI[7:0]_x_N/P	Leave NC any unused CSI lanes

Chapter 21. General Layout Guidelines

Trace and via characteristics play an important role in signal integrity and power distribution on the Jetson Thor. Vias can have a strong impact on power distribution and signal noise, so careful planning must take place to ensure designs meet the NVIDIA via requirements. Trace length or delay and impedance determine signal propagation time and reflections, both of which can greatly improve or reduce the performance of the Jetson Thor. Trace and via requirements for each signal type can be found in the corresponding chapter. This chapter provides general guidelines for via and trace placement.

21.1 Via Guidelines

The number of vias in the path of a given signal, power supply line, or ground line can greatly affect the performance of the trace. Via placement can make differences in current carrying capability, signal integrity (due to reflections and attenuation), and noise generation, all of which can impact the overall performance of the trace. The following guidelines provide basic advice for proper use of vias.

21.1.1 Via Count and Trace Width

As a rule, each ampere of current requires at least two micro-vias. A typical thru hole via can handle two amperes of current.

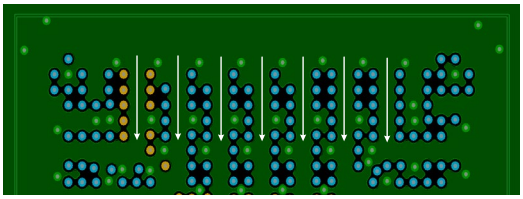
21.1.2 Via Placement

If vias are not placed carefully, they can severely degrade the robustness of a board's power plane. In standard designs that do not use blind or buried vias, construction of a via entails drilling a hole that cuts into the power and ground planes. Thus, incorrect via placement affects the amount of copper available to carry current to the power balls of the IC.

21.1.3 Via Placement and Power and Ground Corridors

Vias should be placed so that sufficiently wide power corridors are created for good power distribution, as shown in the following figure.

Figure 21-1. Via Placement for Good Power Distribution



Care should also be taken to avoid use of “thermal spokes” (also referred to as “thermal relief”) on power and ground vias. Thermal spokes are not necessary for surface-mount components, and the narrow spoke widths contribute to increased inductance. The metal on the inner layers between vias may not be flooded with copper if enough spacing is not provided. The diminished spacing creates a blockage and forces the current to find another path due to lack of copper, as shown in the following two figures. This leads to power delivery issues and impedance discontinuities when traces are routed over these plane voids.

Figure 21-2. Good Current Flow Resulting from Correct Via Placement

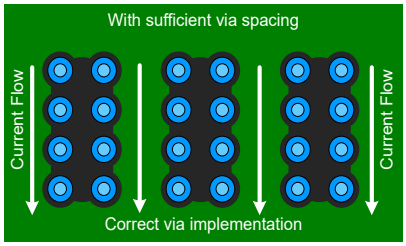
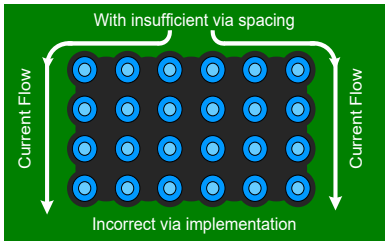


Figure 21-3. Poor Current Flow Resulting from Incorrect Via Placement



In general, a dense via population should be avoided and good PCB design principles and analysis should be applied.

21.2 Connecting Vias

To be effective, vias must be connected properly to the signal and power planes. Poor via connections make the capacitor and power planes less effective, leading to increased cost due to the need for additional capacitors to achieve equivalent performance. This not only impacts the Bill of Materials (BOM) cost of the design, but it can greatly impact quality and reliability of the design.

21.3 Trace Guidelines

Trace length/delay and impedance play a critical role in signal integrity between the driver and the receiver on the Jetson Thor. Signal trace requirements are determined by the driver characteristics, source characteristics, and signal frequency of the propagating signal.

21.3.1 Layer Stack-Up

The number of layers required is determined by the number of signal layers needed to achieve the desired performance, and the number of power rails required to achieve the optimum power delivery or noise floor. For example, high-performance boards require four signal routing layers, with at least two GND planes for reference. This comes to six layers; add another two for power, which gives eight layers minimum. Reduction from eight to six layers starts the trade-off of cost versus performance.

Power and GND planes usually serve two purposes in PCB design: power distribution and providing a signal reference for high-speed signals.

Either the power or the ground planes can be used for high-speed signal reference; this is particularly common for low-cost designs with a low layer count. When both power and GND are used for signal reference, make sure you minimize the reference plane transition for all high-speed signals. Decoupling caps or transition vias should be added close to the reference plane transitions.

21.3.2 Trace Length or Delay

The maximum trace length or delay for a given signal is determined by the maximum allowable propagation delay and impedance for the signal. Higher frequency signals must be treated as transmission lines (see Chapter 25 “Transmission Line Primer”) to determine proper trace characteristics for a signal.

All signals on the design maintain different trace guidelines. Refer to the corresponding signal chapter in the design guide to determine the guidelines for the signal.

Chapter 22. Stack-Ups

22.1 Reference Design Stack-ups

This section details the reference design stack-ups.

22.1.1 Importance of Stack-up Definition

Stack-ups define the number and order of board layers. Stack-up definition is critical to the following design:

- Circuit routability
- Signal quality
- Cost

22.1.2 Impact of Stack-up Definition on Design

- **Stack-Up Impact on Circuit Routability**
  If there are insufficient layers to maintain proper signal spacing, prevent discontinuities in reference planes, obstruct flow of sufficient current, or avoid extra vias, circuit routing can become unnecessarily complex. Layer count must be minimally appropriate for the circuit.
- **Stack-Up Impact on Signal Quality**
  Both layer count and layer order impact signal integrity. Proper inter-signal spacing must be achievable. Via count for critical signals must be minimized. Current commensurate with the performance of the board must be carried. Critical signals must be adjacent to major and minor reference planes and adhere to proximity constraints with respect to those planes. The recommended NVIDIA stack-ups achieve these requirements for the signal speeds supported by the board.
- **Stack-Up Impact on Cost**
  While defining extra layers can facilitate excellent signal integrity, current handling capability and routability, extra layers can impede the goal of hitting cost targets. The art of stack-up definition is achieving all technical and reliability circuit requirements in a cost-efficient manner. The recommended NVIDIA stack-ups achieve these requirements with efficient use of board layers.

Chapter 23. USB 3.2 and Wireless Coexistence

USB 3.2 supports a 5 Gbps (or multiple) signaling rate. The USB 3.2 specification requires USB 3.2 data to be scrambled and spread spectrum is required. The noise from the USB 3.2 data spectrum has been found from around DC to 4 GHz and beyond. This noise can desensitize nearby receivers operating in the cellular and WiFi 2.4 GHz band. This includes, for example, WiFi 802.11b/g/n or Bluetooth® including Bluetooth mouse devices, Bluetooth keyboards, and so on. This noise causes:

- WiFi sensitivity degradation
- Wireless link throughput drop
- Wireless operation range degradation

This section focuses on USB 3.2, but other high-speed interfaces such as HDMI, DP, and so on, can also cause issues with wireless subsystems. The issues and recommended mitigation techniques would be similar.

23.1 Mitigation Techniques

Each design is different due to unique construction and relative location of USB 3.2 circuits and connectors and receiving antenna. Depending on the level of noise generated, emitted, radiated, and coupled to receiver antenna, some or all of the recommendations might need to be implemented to limit unwanted noise from radiating from the circuit.

The following mitigation techniques described will help minimize the USB 3.2 de-sense.

INCREASE THE USB 3.2 TO ANTENNA SEPARATION

During the placement phase of the design, care must be taken to identify the noise source and try to physically increase the separation between the noise source and antenna. One of the major noise sources is the USB 3.2 connector itself. If possible, the antenna or USB 3.2 location can be changed to increase physical isolation. In general, doubling the distance between antenna and noise source, reduces the coupling by around 6 dB.

USB 3.2 CONNECTOR PART SELECTION: CHOOSE A BETTER USB 3.2 PART

A USB 3.2 connector has many metal fingers that are perfect in length for radiating in and around the 2.4 GHz band and beyond. A USB 3.2 connector should be selected to minimize radiation from the USB 3.2 part itself. Some recommendations are:

- Connector fully enclosed by metal
- No slots in the connector walls, or if there are slots, the size is very small. Also, the number of slots should be minimal.
- Connector has as many grounding legs as possible. More legs provide better grounding from the USB 3.2 exterior to the PCB and the structure is less likely to radiate. Choose four legged connectors over two legged connectors, and so on.

The quality of the external USB 3.2 device used in the USB 3.2 port will have impact on the overall experience. If the external USB 3.2 device used in the USB 3.2 port is of poor quality, the part itself will radiate and issues will continue. A plastic base USB 3.2 device works inferior compared to fully metalized USB 3.2 devices.

GROUND THE USB 3.2 PART SOLIDLY

The USB 3.2 connector is grounded through "the grounding legs" previously mentioned. Care must be taken to ensure the leg area is a very good RF ground. One way to do this is to increase the number of ground vias placed in the "grounding leg" area.

IMPROVE THE ROUTING AND GROUNDING AROUND THE USB 3.2 PART AREA

The routing and grounding around the USB 3.2 connector part area must be handled carefully. Since this area is very "hot," any traces running on the surface layer below the physical connector part can pick up noise and transfer it to other areas or radiate the noise. These traces need to be moved to an inner layer, and this area needs to be made a very good ground.

BURY THE USB 3.2 LINES IN INNER LAYERS

The USB 3.2 lines should be routed as impedance controlled differential pairs, with ground on either side and on the layers above and below.

SHIELD THE USB 3.2 CONNECTOR PART

The radiation from the USB 3.2 connector part is very strong. It is necessary to make a "shield" and put it on top of the USB 3.2 connectors. The shield must touch the USB 3.2 body in multiple points. The shield track must have number of grounding vias so that any emitted noise from the USB 3.2 connector is swiftly grounded.

Chapter 24. Transmission Line Primer

24.1 Basic Board Level Transmission Line Theory

NVIDIA maintains strict guidelines for high-frequency PCB transmission lines to ensure optimal signal integrity for data transmission. This section provides a brief primer into basic board-level transmission line theory.

24.1.1 Characteristics

The most important PCB transmission line characteristics are listed in the following bullets:

- Trace width/height, PCB height and dielectric constant, and layer stack-up affect the characteristic trace impedance of a transmission line.

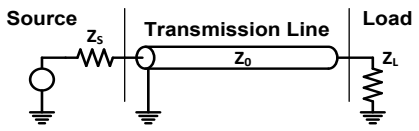
$$Z_0 \cong \left(\frac{L}{C}\right)^{1/2}$$

- Signal rise time is proportional to the transmission line impedance and load capacitance.

$$RiseTime \cong \left(\frac{Z_0 * R_{Term}}{Z_0 + R_{Term}}\right) * C_{Load}$$

- Real transmission lines (as shown in the following figure) have non-zero resistances that lead to attenuation and distortion, creating signal integrity issues.

Figure 24-1. Typical Transmission Line Circuit



Transmission lines are used to “transmit” the source signal to the load or destination with as little signal degradation or reflection as possible. For this reason, it is important to design the high-speed signal transmission line to fall within characteristic guidelines based on the signal speed and type.

24.2 Physical Transmission Line Types

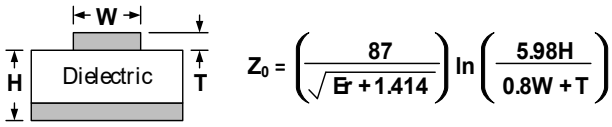
The two primary transmission line types often used for Jetson Thor board designs are:

- Microstrip transmission line (Figure 25-2)
- Stripline transmission line (Figure 25-3)

The following sections describe each type of transmission.

24.2.1 Microstrip Transmission Line

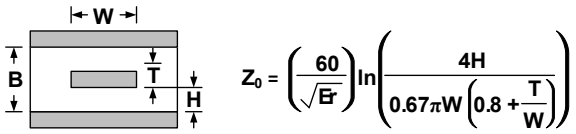
Figure 24-2. Microstrip Transmission Line



- Z0: Impedance
- W: Trace width
- T: Trace thickness
- Er: Dielectric constant of substrate
- H: Distance between signal and reference plane

24.2.2 Stripline Transmission Line

Figure 24-3. Stripline Transmission Line



- Z0: Impedance
- W: Trace width (inches)
- T: Trace thickness (inches)
- Er: Dielectric constant of substrate
- H: Distance between signal and reference plane

24.3 Driver Characteristics

Driver characteristics are important to the integrity and maximum speed of the signal. The following points identify key driver equations and concepts used to improve signal integrity and transmission speed.

- The driver (source) has resistive output impedance Z_S, which causes only a fraction of the signal voltage to propagate down the transmission line to the receiver (load).
  - Transfer function at source:

$$T1 = \frac{Z_0}{Z_S + Z_0}$$

  - Driver strength is inversely proportional to the source impedance, Z_S.
- Z_S also acts as the source termination, which helps dampen reflection.
  - Source reflection coefficient:

$$R1 = \frac{(Z_S - Z_0)}{(Z_S + Z_0)}$$

24.4 Receiver Characteristics

Receiver characteristics are important to the integrity and detectability of the signal. The following points identify key receiver concepts and equations for optimum signal integrity at the final destination.

- The receiver acts as a capacitive load and often has a high load impedance, Z_L.
- Unterminated transmission lines cause overshoot and reflection at the receiver, which can cause data corruption.
  - Output transfer function at load:

$$T2 = \frac{2 * Z_L}{Z_L + Z_0}$$

  - Load reflection coefficient:

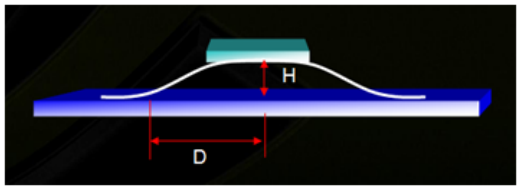
$$R2 = \frac{(Z_L - Z_0)}{(Z_L + Z_0)}$$

- Load impedance can be lowered with a termination resistor (R_{Term}) placed at the end of the transmission line.
  - Reflection is minimized when Z_L matches Z_0

24.5 Transmission Lines and Reference Planes

Defining an appropriate reference plane is vital to transmission line performance due to crosstalk and EMI issues. The following points explore appropriate reference plane identification and characteristics for optimal signal integrity:

Figure 24-4. Transmission Line Height



- Transmission line return current:
  - High-speed return current follows the path of least inductance.
  - The lowest inductance path for a transmission line is the portion of the line closest to the dielectric surface; i(D) is proportional to

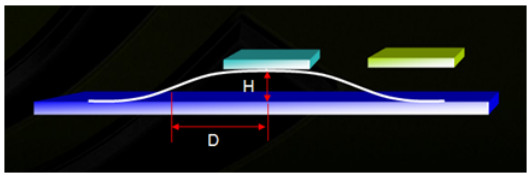
$$\frac{1}{\left(1+\left(\frac{D}{H}\right)^2\right)}$$

- Crosstalk on solid reference plane (Figure 25-5):
  - Crosstalk is caused by the mutual inductance of two parallel traces.
  - Crosstalk at the second trace is proportional to

$$\frac{1}{\left(1+\left(\frac{D}{H}\right)^2\right)}$$

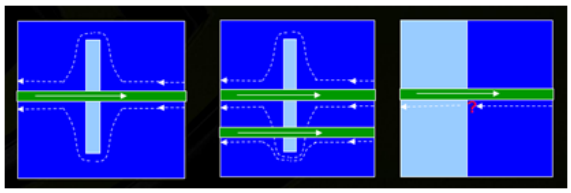
  - The signals need to be properly spaced to minimize crosstalk

Figure 24-5. Crosstalk on Reference Plane



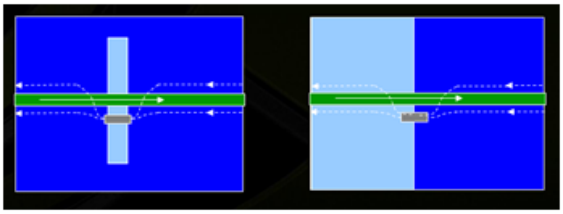
- Reference plane selection
  - Solid ground is preferred as reference plane.
  - Solid power can be used as reference plane with decoupling capacitors near driver and receiver.
  - Reference plane cuts and layer changes need to be avoided.
- Power plane cut example (Figure 25-6)
  - Power plane cuts will cause EMI issues.
  - Power plane cuts also induce crosstalk to adjacent signals.

Figure 24-6. Power Plane Cuts Example



- When a cut is unavoidable:
  - Place decoupling capacitors near transition.
  - Place transition near source or receiver when decoupling capacitors are abundant (Figure 25-7).

Figure 24-7. Power Plane Cuts Example when Decouple Capacitors are Abundant



- When signal changes plane:
  - Try not to change the reference plane, if possible.
  - When a reference plane switches to a different power rail, a stitching capacitor is required (Figure 25-8).
  - When the same ground and power reference plane changes to a different layer, a stitching via is required (Figure 25-9).

Figure 24-8. Switching Reference Planes

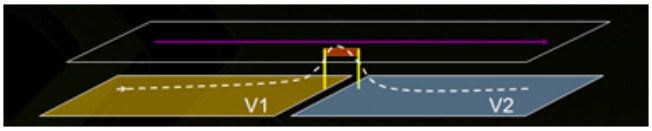
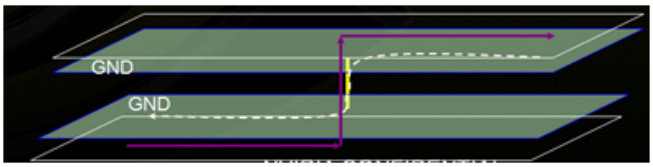


Figure 24-9. Reference Plane Switch Using Via



Chapter 25. Design Guideline Glossary

The design guidelines include various terms. The following descriptions are intended to show what these terms mean and how they should be applied to a design.

- Trace Delay
  - Max Breakout Delay
    Routing on Component layer: Maximum Trace Delay from module connector pin to point beyond pin array where normal trace spacing/impedance can be met. Routing passes to layer other than Component layer: Beyond this, normal trace spacing/impedance must be met.
  - Max Total Trace Delay
    Trace from module connector pin to device pin. This must include routing on the main PCB and any other Flex or secondary PCB. Delay is from the module connector to the final connector and device.
- Intra and Inter Pair Skews
  - Intra Pair Skew within Pair
    Difference in delay between two traces in differential pair: Shorter routes may require indirect path to equalize delays.
  - Inter Pair Skew Pair-to-Pair
    Difference between two (or possibly more) differential pairs.
- Impedance and Spacing
  - Microstrip vs. Stripline
    - Microstrip: Traces next to single reference plane.
    - Stripline: Traces between two reference planes.
  - Trace Impedance
    Impedance of trace determined by width and height of trace, distance from reference plane, and dielectric constant of PCB material. For differential traces, space between pair of traces is also a factor.
  - Board Trace Spacing and Spacing to other Nets
    Minimum distance between two traces. Usually specified in terms of dielectric height, which is distance from trace to reference layers.
  - Pair to Pair Spacing
    Spacing between differential traces.
  - Breakout Spacing
    Possible exception to board trace spacing where different spacing rules are

allowed under module connector pin to escape from the pin array. Outside device boundary, normal spacing rules apply.

- Reference Return
  - Ground Reference Return Via and Via proximity (signal to reference)
    - Signals changing layers and reference GND planes need similar return current path.
    - Accomplished by adding via, tying both GND layers together.
  - Via proximity (signal to reference) is distance between signal and reference return vias.
    - GND reference via for Differential Pair.
    - Where a differential pair changes GND reference layers, return via should be placed close to and between signal vias (example to right).
  - Signal to return via ratio
    Number of Ground Return vias per Signal vias. For critical IFs, ratio is usually 1:1. For less critical IFs, several trace vias can share fewer return vias (that is 3:2 – three trace vias and two return vias).
  - Slots in Ground Reference Layer
    - When traces cross slots in adjacent power or ground plane.
    - Return current has longer path around slot.
    - Longer slots result in larger loop areas.
    - Avoid slots in GND planes or do not route across them.
  - Routing over Split Power Layer Reference Layers
    - When traces cross different power areas on power plane.
      - Return current must find longer path - usually a distant bypass cap.
      - If possible, route traces with solid plane (GND or PWR) or keep routes across single area.
    - If traces must cross two or more power areas, use stitching capacitors.
      - Placing one cap across two PWR areas close to where traces cross area boundaries provide high-frequency path for return current.
      - Cap value typically 0.1uF and should ideally be within 0.1" of crossing.

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