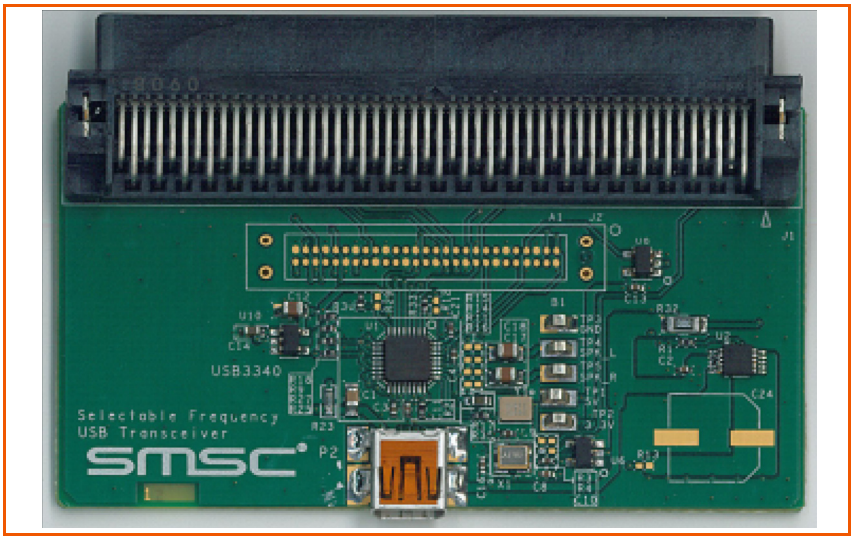
EVB-USB3340 USB Transceiver Evaluation Board User Manual



1 Introduction

This user manual is for the USB3340 USB Transceiver Evaluation Board (EVB) for use with USB3340 products with the integrated USB switch.

The USB3340 features a ULPI interface to support systems with USB Host, Device, or On-the-Go (OTG) capability. The integrated switch can be used to multiplex a Full Speed USB signal or audio signals over the HS USB DP/DM pins.

2 Overview

The USB3340 EVB is a Daughter Card designed to plug into a user's test system using a T&MT connector. The card attaches to a USB link layer to create a USB Host, Device, or On-the-Go (OTG) system. The board edge connector meets the UTMI+ Low Pin Interface (ULPI) Standard requirements for the T&MT connector.

A link to the ULPI Working Group Page is available at www.smsc.com or may be obtained from your local FAE. The USB3340 EVB includes USB3340 packaged silicon and all external components required for the USB transceiver function.

This manual describes PCB assembly PCB-7220AZ.

2.1 Supplying VBUS Voltage

In Host or OTG operation, the USB3340 EVB must provide 5 Volts on V_{BUS} at the USB connector. The USB3340 EVB includes a switch that can drive V_{BUS} using the 5 Volt supply that comes from pin 28 of the T&MT connector.

The VBUS switch is controlled by the CPEN signal from the USB3340. The USB controller dictates the state of CPEN by programming the ULPI register in the USB3340. The 5 Volt switch is backdrive protected when in the off state. The switch does not provide protection from reverse currents when it is on. See Section 2.10 and Section 2.11 for more information on configuring the USB3340 EVB for OTG and Host operation.

2.2 ULPI I/O Voltage

The USB3340 supports variable ULPI I/O voltage signaling. The ULPI I/O voltage is supplied in one of two ways. By default, the EVB is shipped with VDDIO supplied by the on-board LDO.

Resistor R18 is used to set VDDIO, the digital logic high voltage. To change the value of VDDIO, calculate a new value for R18 (ohms) as follows.

$$R18 = (VDDIO/1.225\text{-}1) \times 169000$$

VDDIO must be in the range of 1.8 Volts - 3.3 Volts nominal.

VDDIO can also be supplied to the USB3340 from the T&MT connector instead of using the LDO. To do this, the LDO (U10) must be removed.

The VDDIO voltage level that has been configured on the USB3340 EVB must be the same as the ULPI I/O voltage level that the link is using.

2.3 Edge Connector for Digital I/O

The T&MT edge connector is compliant to the ULPI specification. Part numbers and manufacturers for this connector and it's mate are given in Table 2.1.

Table 2.1 Edge Connector on the USB3340 EVB

PART NUMBER	DESCRIPTION	MANUFACTURER
2-557101-5	100 pin edge connector on USB3340 EVB	AMP
2-557-101-5	Mating connector to the USB3340 EVB	AMP
1-1734037-0	Alternate 100 pin edge connector for USB3340 EVB	TYCO
1-1734099-0	Alternate mating connector to the USB3340 EVB	TYCO

2.4 REFCLK Frequency Selection

The USB3340 EVB offers a user selectable reference clock frequency. R25 - R30 are used to configure the REFCLK[2:0] signals which will select the reference clock frequency desired on the USB3340 EVB. Ensure that the frequency of the reference clock or reference crystal being used matches the desired operation frequency configured based on Table 2.2 below. By default, the USB3340 EVB is configured for 26MHz REFCLK operation.

Table 2.2 Reference Frequency Selection Resistor Configurations

R25	R26	R27	R28	R29	R30	REFCLK FREQUENCY
INSTALL	EMPTY	INSTALL	EMPTY	EMPTY	INSTALL	26.0 MHz (Default)
EMPTY	INSTALL	INSTALL	EMPTY	EMPTY	INSTALL	12.0 MHz
EMPTY	INSTALL	EMPTY	INSTALL	EMPTY	INSTALL	52.0 MHz
INSTALL	EMPTY	INSTALL	EMPTY	INSTALL	EMPTY	24.0 MHz
INSTALL	EMPTY	EMPTY	INSTALL	INSTALL	EMPTY	19.2 MHz
EMPTY	INSTALL	INSTALL	EMPTY	INSTALL	EMPTY	27.0 MHz
EMPTY	INSTALL	EMPTY	INSTALL	INSTALL	EMPTY	38.4 MHz
INSTALL	EMPTY	EMPTY	INSTALL	EMPTY	INSTALL	13.0 MHz

2.5 USB Connector

A standard Mini-AB connector is provided to attach a USB cable or connector. Provision is made on the PCB to accept a Micro-AB connector. See the bill of materials in Section 6 for connector part numbers. Do not substitute a different part number for the Mini-AB receptacle or a short circuit of the USB signals may result at the micro-AB connector PCB footprint.

2.6 VBUS Present Detection

The USB controller must detect VBUS when a USB cable is attached in device mode or when the USB controller turns on VBUS in host or OTG mode. The USB connector VBUS signal is connected to the VBUS pin of the USB3340. The USB3340 includes all of the comparators required to detect VBUS and report the state of VBUS to the USB controller via the ULPI bus.

2.7 ULPI Signal Test Points

Probe points at location J2, provide access to all ULPI signals. Install the Tektronix logic analyzer probe retention kit at J2 to probe these signals. Ordering information for the retention kit is provided in the bill of materials.

2.8 Other Signal Test Points

There are five other test points located on the board for easy access. TP1 connects to the 5V supply coming from the T&MT connector. TP2 connects to the 3.3V VDD supply coming from the T&MT connector. TP3 connects to Ground. TP4 and TP5 connect to the Speaker Left and Speaker Right pins respectively.

2.9 Speaker Left and Speaker Right signals

The Speaker Left and Speaker Right pins can accept audio signals ranging from 0V to 3.3V. If the audio signal coming into the test points goes below 0V, biasing circuitry is required. Install R11, R14, R15, and R16 with 10k resistors to add a DC bias to the audio signal. This will ensure the best signal quality when routing through the USB3340.

2.10 Converting the EVB to an OTG System

“Out of the box”, the USB3340 EVB is delivered as a USB Device system. To convert it to be a USB OTG development board, the following modifications must be made:

1. Install R13 (zero ohm resistor). This connects the VBUS 5V switch to the VBUS signal.
2. Remove R23. This is the R_{VBUS} value required for a USB Device.
3. Install R10 (1.0K, 1W resistor). This is the R_{VBUS} value required for a USB OTG Device.

Since the USB3340 is designed to accommodate up to 30V on VBUS, R10 is rated at 1W to accommodate this entire voltage range. Refer to the USB3340 datasheet for more information on sizing this resistor.

2.11 Converting the EVB to a Host System

“Out of the box”, the USB3340 EVB is delivered as a USB Device System. To convert it to be a USB Host development board, the following modifications must be made:

1. Install R13 (zero ohm resistor). This connects the VBUS 5V switch to the VBUS signal.
2. Install C24 (120uF capacitor). This increases the value of C_{VBUS} to be USB 2.0 Host compliant.

2.12 Converting the EVB to Support ULPI Clock Input Mode

“Out of the box”, the USB3340 EVB uses a crystal (Y1) as the clock reference, and is configured for ULPI Clock Output Mode where CLKOUT sources a 60MHz clock. To convert the EVB to support ULPI Clock Input Mode, the following changes must be made:

1. Install R12 (zero ohm resistor). This shorts CLKOUT to VDD18.
2. Install R3 (zero ohm resistor). This shorts REFCLK to the System Clock pin on the T&MT connector.
3. Confirm that R4 is not populated.
4. Remove the following components to remove the crystal circuit: Y1, R17, C22, C23

Refer to the USB3340 datasheet for more information on ULPI Clock Input Mode.

2.13 T&MT Pin Description

The T&MT signal names, pin number and function are described in Table 43 and Table 44 of the ULPI Specification rev 1.1.

The USB3340 EVB fully implements a ULPI compliant interface to the T&MT connector, including support for ULPI Clock Input Mode. This EVB supports a 1.8-3.3V ULPI I/O voltages. All signals are described in Table 2.3.

Table 2.3 T&MT Connector Pin Definitions

PIN	NAME	DESCRIPTION	DIRECTION
86, 36, 85, 34, 83, 33, 82, 31	DATA[7:0] Refer to Schematic for Connector Pin Assignment	ULPI Data Bus	IN/OUT
96	STP	ULPI STP Signal	INPUT TO EVB
70	DIR	ULPI DIR Signal	OUTPUT FROM EVB
71	NXT	ULPI NXT Signal	OUTPUT FROM EVB
90	CLKOUT	ULPI Clock Signal	OUTPUT FROM EVB
55	VBUS_FAULT_N	Driven low by the VBUS switch (U2) in the event of a switch fault condition.	OUTPUT
15	SPKR_L	In USB Audio mode, SPKR_L is connected to the DP pin via an analog switch in the USB3340.	IN/OUT
45	SPKR_RM	In USB Audio mode, SPKR_RM is connected to the DP pin via an analog switch in the USB3340.	IN/OUT
17	RESET	Asserting RESET will place the USB3340 in a low power state. Upon exiting this state (RESET=0), all ULPI registers will contain power-on reset values.	INPUT
47	VBUS_IN	This pin is not connected	NO CONNECT
28	VBUS_OUT	+5V from the T&MT connector	INPUT TO EVB
8, 16, 57, 69	VDD	+3.3V from the T&MT connector	INPUT TO EVB
52	SYSTEM_CLOCK	Optional clock input to EVB. The EVB is built with the USB3340 REFCLK provided by a crystal. See Section 2.12 for more information on configuring the USB3340 EVB for ULPI Clock Input mode.	NO CONNECT (input to EVB if R3 is installed)
100	PSU_SHD_N	This pin is driven low indicating that +3.3V must be sourced from the link through the T&MT connector pins 8, 16, 57, 69 and +5.0V must be sourced from the link through the T&MT connector pin 28.	OUTPUT FROM EVB
49	DC_PSNT_N	This pin is driven low indicating a daughter card is present.	OUTPUT FROM EVB

3 Getting Started

The block diagram in Figure 3.1 gives a simplified view of the USB3340 EVB. The USB3340 EVB is ready for device operation. To modify the board for OTG or Host applications, refer to Section 2.10 or Section 2.11, respectively.

It is required to provide +5V to T&MT connector pin 28 and +3.3V on T&MT pins 8,16,57,69 to power the USB3340 EVB.

The USB3340 EVB is built with a USB Mini-AB receptacle. Do not substitute a Mini-AB receptacle different from the one specified in the bill of materials, or a short circuit may occur on the USB signals at the Micro-AB connector PCB footprint.

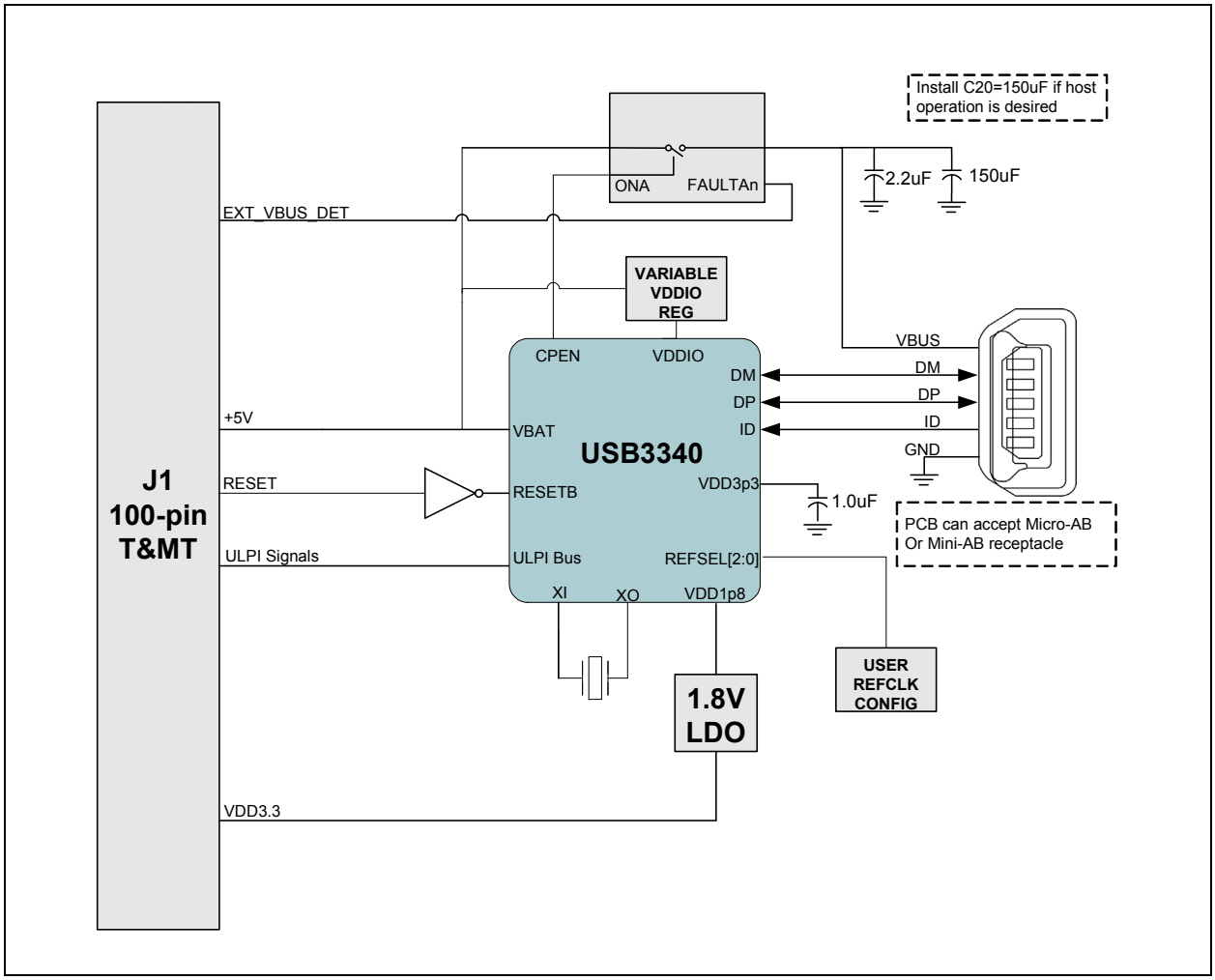


Figure 3.1 Block Diagram of USB3340 EVB

When the USB3340 EVB is powered on, check the following things to be certain the board is functioning normally:

- RESET should be de-asserted (logic low at the T&MT connector and RESETB at the USB3340 should be logic high = VDD18). If RESETB=0, the USB3340 will be in a low power state.
- The voltage at R2 (RBIAS) should be 0.8V DC. If this voltage is not present, the USB3340 is in a low power state.
- There should be a digital 60 MHz square wave signal at T&MT connector pin 90. The amplitude should be approximately VDDIO. This is the CLKOUT signal of the USB3340.

- The voltage at C3 should be approximately 3.3V. This is the USB3340 internal 3.3V voltage regulator output.
- The voltage at C4 should be 1.8V. This is the 1.8V regulator output.

4 Protecting VBUS from Non-Compliant VBUS Voltages

The USB3340 is fully tolerant to VBUS voltages up to 30V. An external resistor on the VBUS line (R_{VBUS}) is required for the integrated overvoltage protection circuit in the USB3340. R_{VBUS} is either R10 or R23 on the USB3340 EVB. For peripheral and host applications, R_{VBUS} is 10K (install R23, remove R10). For OTG applications, R_{VBUS} is 1K (install R10, remove R23).

5 USB3340 EVB Schematic

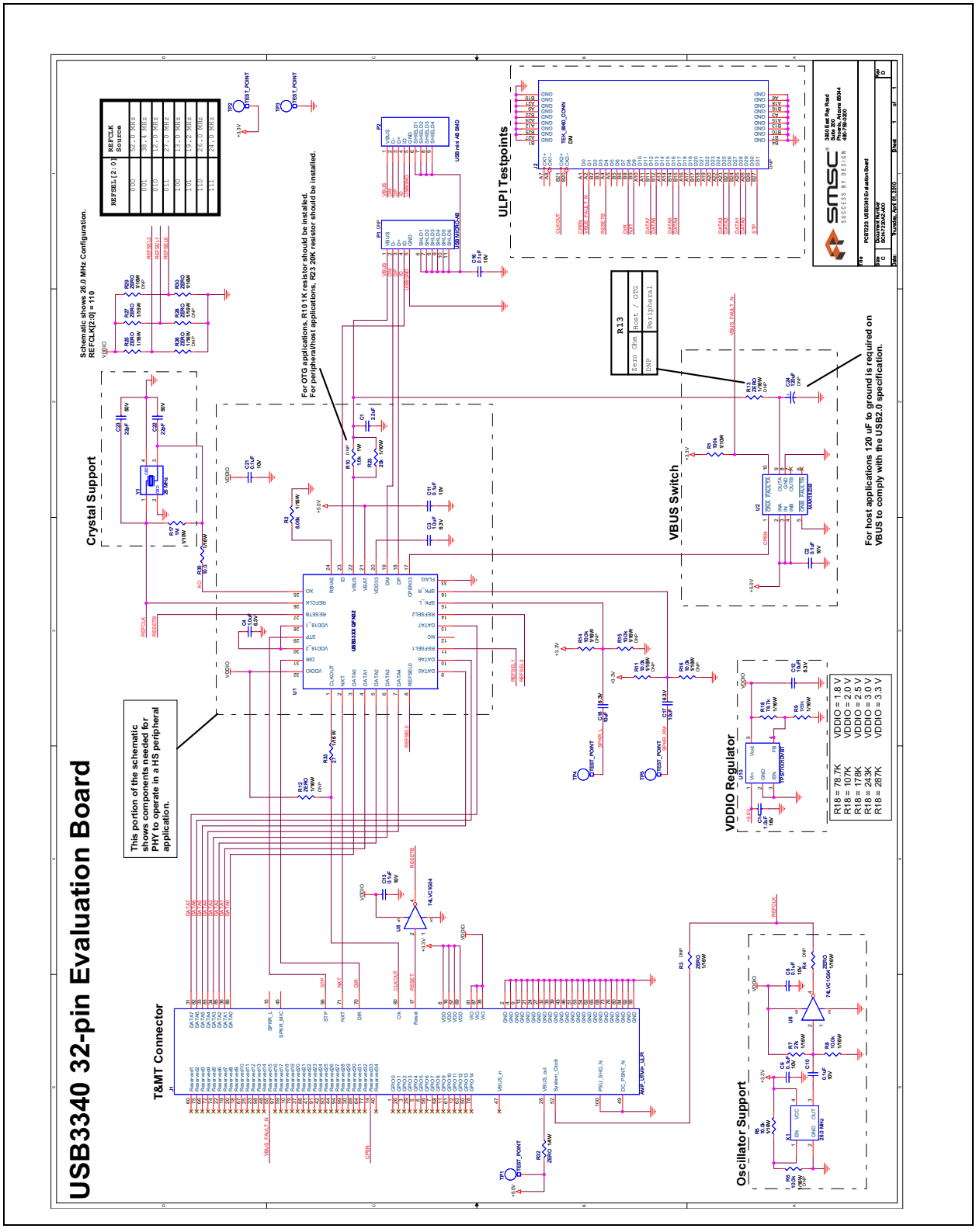


Figure 5.1 USB3340 EVB Schematic

6 USB3340 EVB Bill of Materials

Item #	Quantity	DNP	Part Reference	Description	Digikey_Number	Manuf	Manuf_PN	RoHS
1	1		C1	CAPACITOR CERAMIC 2.2UF 50V Y5V 0805	445-3464-1-ND	TDK	C2012Y5V1H225Z	Yes
2	8		C2 C8 C9 C10 C11 C13 C16	CAPACITOR CERAMIC 0.1UF 10V X5R 0402	PCC2146CT-ND	PANASONIC	ECJ-0EB1A104K	Yes
3	2		C3 C4	CAPACITOR CERAMIC 1.0UF 6.3V 20% X5R 040	490-1319-1-ND	MURATA ERIE	GRM155R60J105ME19D	Yes
4	3		C12 C17 C18	CAPACITOR CERAMIC 10UF 6.3VDC 20% X5R 08	PCC2225CT-ND	PANASONIC	ECJ-2FB0J106M	Yes
5	1		C14	CAPACITOR CERAMIC 1.0UF 16VDC 10% X5R 06	PCC2224CT-ND	PANASONIC	ECJ-1VB1C105K	Yes
6	2		C22 C23	CAPACITOR CERAMIC 22PF 5% 50V NP0 0402	478-10774-1-ND	AVX	04025A220JAT2A	Yes
7	0	C24		CAPACITOR AUMINUM ELEC 120UF 10V	565-3066-1-ND	United Chemi-Con	APXA100ARA121MH70G	Yes
8	0		J1	AMP_T&MT_UTMI+_ULPI COMBO	A33470-ND	TYCO	1-1734037-0	Yes
9	0	J2		TEK_6960_CONN_DM		TEKTRONIX	P6960DM	Yes
10	1		P2	CONNECTOR RECEPT USB MINI AB 5POS RT ANG	WM17122CT-ND	MOLEX	56579-0576	Yes
11	0	P1		CONNECTOR RECEPT MICRO USB TYPE AB SMT	A97799CT-ND	TYCO	1981584-1	Yes
12	1		R1	RESISTOR 100K OHM 1/10W 5% 0402 SMD	P100KJCT-ND	PANASONIC	ERJ-2GEJ104X	Yes
13	1		R2	RESISTOR 8.06K OHM 1/16W 1% 0402 SMD	P8.06KLCT-ND	PANASONIC	ERJ-2RKF8061X	Yes
14	3	R3 R4 R12 R13 R26 R28	R25 R27 R30	RESISTOR ZERO OHM 1/16W 5% 0402 SMD	311-0.0JRCT-ND	YAGEO	RC0402JR-070RL	Yes
15	3	R6 R11 R14 R15 R16	R5 R8	RESISTOR 10.0K OHM 1/16W 1% 0402 SMD	541-10.0KLCT-ND	VISHAY-DALE	CRCW040210K0FKED	Yes
16	1		R7	RESISTOR 27.0K OHM 1/16W 1% 0402 SMD	311-27.0KLRCT-ND	YAGEO	RC0402FR-0727KL	Yes
17	1		R9	RESISTOR 169K OHM 1/16W 1% 0402 SMD	311-169KLRCT-ND	VISHAY-DALE	CRCW0402169KFKED	Yes
18	0	R10		RESISTOR 1.0K OHM 1W 5% 2512 SMD	541-1.0KXCT-ND	VISHAY-DALE	CRCW25121K00JNEG	Yes
19	1		R17	RESISTOR 1MEG OHM 1/10W 5% 0603	311-1.0MGRCT-ND	YAGEO	RC0603JR-071ML	Yes
20	1		R18	RESISTOR 78.7K OHM 1/16W 1% 0402 SMD	541-78.7KLCT-ND	VISHAY-DALE	CRCW040278K7FKED	Yes
21	1		R23	RESISTOR 20K OHM 1/10W 0.1% 0603 SMD	P20KYCT-ND	PANASONIC	ERA-3YEB203V	Yes
22	1		R32	RESISTOR ZERO OHM 1/4W 5% 1206	311-0.0ERCT-ND	YAGEO	RC1206JR-070RL	Yes
23	1		R33	RESISTOR 27.0 OHM 1/16W 1% 0402 SMD	541-27.0LCT-ND	VISHAY-DALE	CRCW040227R0FKED	Yes
24	1		R35	RESISTOR 10.0 OHM 1/16W 1% 0402 SMD	P10.0LCT-ND	PANASONIC	ERJ-2RKF10R0X	Yes
25	5		TP1 TP2 TP3	TEST POINT	5015KCT-ND	KEYSTONE	5015	Yes
26	1		U1	USB33XX QFN32		SMSC	USB33XX	Yes
27	1		U2	IC SW DUAL USB AUTORESET 10-UMAX MAX1823	MAX1823BEUB+-ND	MAXIM	MAX1823BEUB	Yes
28	2		U6 U8	INVERTER SINGLE LVC SOT23-5 SN74LVC1G04	296-11599-1-ND	TI	SN74LVC1G04DBVR	Yes
29	1		U10	IC ADJ 50MA LDO REG SOT-23-5	296-27621-ND	TI	TPS77001DBVT	Yes
30	1		X1	OSCILLATOR PROG 3.3V +-50PPM SMD	AP3S3EC-ND	ABRACON	AP3S-26.0MHz	Yes
31	1		Y1	CRYSTAL 26.000 MHZ 10PF SMD	535-9624-1-ND	ABRACON	ABM10-26.000MHZ-7A15-T	Yes

Figure 6.1 USB3340 EVB Bill of Materials

7 User Manual Revision History

Table 7.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.1 (05-06-13)		Co-branded document.
Rev. 1.1 (12-14-10)	R9 on Schematic and BOM	Changed from 10k to 169k
Rev. 1.0 (05-01-10)	Initial Release	