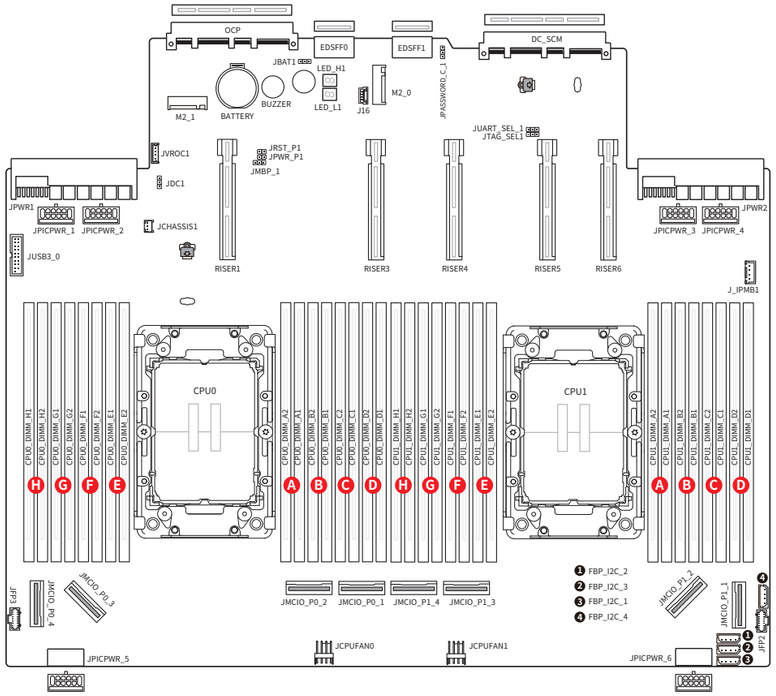
G52-S3682X1

D5062 / S5062

QUICK START GUIDE



CPU

Dual Intel® Xeon® 6700E-series, 6500P-series and 6700P-series processors, TDP up to 350W.

DC-MHS Control Panel Header

The **DC-MHS** (Data Center Modular Hardware System) control panel header for **M-PESTI** connects the **HPM** to the server' s front panel, enabling essential controls such as power, LED indicators, buttons, and sideband signals for management and monitoring.

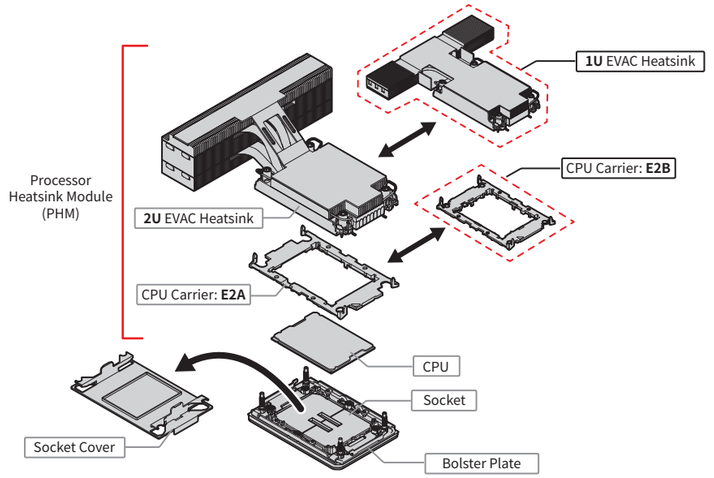
JFP2~3

20 19

2 1

1	P12V_AUX	2	GND
3	P12V_AUX	4	BMC_SMB_LVC3_PESTI1_SDA
5	NC	6	BMC_SMB_LVC3_PESTI1_SCL
7	GND	8	GND
9	USB2_BMC_PCP_ESD_D+	10	FM_FP_HPM_PCP_SB4
11	USB2_BMC_PCP_ESD_D-	12	FM_FP_HPM_PCP_SB3
13	GND	14	FM_FP_HPM_PCP_SB2
15	SPI_BMC_FP_MISO_R	16	FM_FP_HPM_PCP_SB1
17	SPI_BMC_FP_CS0_R	18	GND
19	SPI_BMC_FP_MOSI_R	20	SPI_BMC_FP_CK_R

CPU and Heatsink Installation



1. **Attach the CPU to the Carrier**
   Align the Pin 1 indicators and snap the CPU securely into the carrier.

- *Please refer to the following table for the corresponding CPU carrier.*

CPU Package Type	Thin Package	Thick Package
CPU Package Name	• Granite Rapids- SP XCC	• Granite Rapids- SP HCC/ LCC • Sierra Forest- SP
CPU Carrier Code	E2A	E2B

2. **Prepare the Heatsink**
   Remove any protective film and ensure thermal paste is applied (add if missing).
3. **Attach the Heatsink to the Carrier**
   Align the Pin 1 indicator with the heatsink' s cut corner (#1 clip) and press down until all latches engage.
4. **Form the PHM(Processor Heatsink Module)**
   Confirm the CPU, carrier, and heatsink are securely latched together.
5. **Place the PHM on the Motherboard**
   Remove the socket cover, unlock the 4 anti-tilt wires, align the Pin 1 indicators, and lower the PHM onto the bolster plate.
6. **Secure the PHM**
   Lock the anti-tilt wires outward and tighten the heatsink nuts diagonally using a Torx T30 screwdriver.

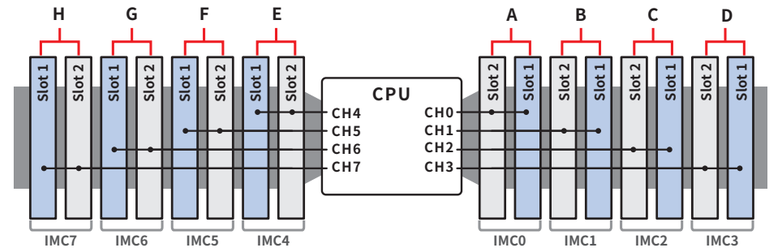
Connectors, Jumpers and LED Indicators

Name	Description
JPWR1~2	CRPS/ M-CRPS 185x73.5mm power connectors
JPICPWR_1~6	12-Pin PICPWR power connectors
RISER1,3	SFF-TA-1033 M-XIO slots (PCIe 5.0 x16, from CPU0)
RISER4~6	SFF-TA-1033 M-XIO slots (PCIe 5.0 x16, from CPU1)
JMCIO_P0_1~4	MCIO 8i connectors (PCIe 5.0 x8, from CPU0)
JMCIO_P1_1~4	MCIO 8i connectors (PCIe 5.0 x8, from CPU1)
M2_0~1	M.2 slots (M Key, PCIe 5.0 x2, 2280/ 22110)
EDSFF0~1	E1.S 9.5mm connectors (PCIe 5.0 x4, from CPU1)
OCP	OCP 3.0 mezzanine slot (PCIe 5.0 x16, from CPU0, NCSI supported)
DC-SCM	DC-SCM 2.0 edge slot
JCPUFAN0~1	4-pin fan connectors
J16	Liquid leak detection connector
JUSB3_0	USB 3.2 Gen 1 connector (5 Gbps, for 2 USB ports)
JFP2~3	DC-MHS control panel header
JRST_P1	Reset button header
JPWR_P1	Power button header
J_IPMB1	IPMB header
JVROC1	VROC connector
FBP_I2C_1~4	I2C headers
JCHASSIS1	Chassis intrusion header
JMBP_1	MBP/ I3C MIPI mode select jumper (default pin 1-2, MBP Mode)
JBAT1	CMOS clear jumper (default pin 1-2, Normal)
JPASSWORD_C_1	Password clear jumper (default pin 1-2, Normal)
JUART_SEL1	UART BMC/ CPLD select jumper (default pin 1-2, UART BMC to CPU)
JTAG_SEL1	JTAG select jumper (default pin 1-2, BMC to CPLD)
LED_H1, LED_L1	Port 80 debug LEDs

Memory

The server board supports 32 DDR5 DIMM slots, compatible with **RDIMMs** and **MRDIMMs**.

DIMM Type	Max Frequency	Max Capacity per DIMM
RDIMM	6400 MT/s (1DPC), 5200 MT/s (2DPC)	256GB
MRDIMM	8000 MT/s (only support 1DPC)	64GB



IMC#	IMC7		IMC6		IMC5		IMC4			IMC0		IMC1		IMC2		IMC3	
Channel	H		G		F		E			A		B		C		D	
	Chan 7		Chan 6		Chan 5		Chan 4			Chan 0		Chan 1		Chan 2		Chan 3	
DDR5 Qty.	H1	H2	G1	G2	F1	F2	E1	E2		A2	A1	B2	B1	C2	C1	D2	D1
1											V						
4			V				V				V				V		
	V				V								V				V
8	V		V		V		V				V		V		V		V
			V	V			V	V		V	V			V	V		
	V	V			V	V						V	V			V	V
12	V		V	V	V		V	V		V	V		V	V	V		V
16	V	V	V	V	V	V	V	V		V	V	V	V	V	V	V	V

CPU

"**V**" indicates DIMMs are populated with **DDR5**.

Important

- ***Intel® Xeon® 6700E Series*** *does not support* ***12*** *DIMMs configuration.*
- *There should be at least one DDR5 DIMM per socket.*
- *When only one DIMM is used in a channel, it must be populated in the DIMM slot farthest away from the* ***CPU (DIMM slot 1)*** *of a given channel.*
- *DDR5 memory configurations requires* ***same DIMM types, ranks, speeds, and densities****.*
- *Mixing vendors, non-3DS/3DS RDIMMs, 9x4 RDIMMs, or x8/x4 DIMMs is not allowed.*
- *Mixing DIMMs with different operating* ***frequencies*** *is not validated. When frequencies differ, the system defaults to the lowest common speed.*