USER GUIDE

multiLane

ML4066 CMIS Analyzer User Guide

CMIS Analyzer Board and CMIS Analysis and Compliance Software| Step-by-Step Guide

User Guide Revision 1.8, July 2021

Innovation for the next generation

Table of Contents

Revision Control 3

Overview 4

Analyzer Features 5

SFF Analyzer features 5

CMIS features 5

SFF Analyzer GUI 6

VCC tab 6

I2C Configuration Tab 7

I2C tab 7

Packet Descriptions 9

Functional Tests Tab 9

I2C Read/Write: 10

Memory Map Tab 11

CNTRL/ALRM Signals tab 12

Application Notes 13

I2C Tab 13

Functional Tests Tab 14

Cntrl/Alrm Tab 16

CMIS State Machine Test 19

Paged Memory Modules 19

Flat Memory Modules 20

Appendix I: Analyzer Card Diagram 21

Revision Control

Revision number	Description	Release Date
1.0	▪ Preliminary revision	11/27/2017
1.1	▪ Updated parag 3.2 to match version 1.0 of the GUI	12/13/2017
1.2	▪ Adding period selection	1/4/2018
1.3	▪ Adding Resistor pullup and Refresh button in cntrl Tab	4/26/2018
1.4	▪ Adding application notes	3/5/2018
1.5	▪ Update parag 3.3.1	6/4/2018
1.6	▪ Add Appendix	9/4/2019
1.7	▪ Add CMIS 4.0 State Machine Test	3/2/2020
1.8	▪ Format Updates	7/27/2021

Overview

The ML4066 is an adapter with diagnostic interface for the power, I2C and management interface control and alarm signals. The ML4066-ANA analyzer board is connected to the ML4066 to enable live diagnosis for the transceiver and host, ensuring that the entire data was delivered.

The ML4066 also makes use of the Common Management Interface Specification (CMIS) allows host and module software implementers to utilize a common code base across a variety of form factors. CMIS is a robust and increasingly crucial element of data center interconnects, and critical for transceiver stability.

Analyzer Features

SFF Analyzer features

- USB Interface
- Windows based GUI and API Library
- Detection and measurement of host pull up + pull down resistors on low-speed signals
- Host VCC rails sampling measurement
- VCC spectral noise analysis
- I2C Analyzer
  - Bus Speed
  - ACK/ NACK Detection
  - Clock Stretching Analysis
  - Time Event Logging
- Functional tests
  - Control signals
  - Configuration registers
  - Ability to emulate optical module by loading identification registers with custom data
  - I2C Terminated by microcontroller, I2C slave compliant with MSA
  - Implements MSA Memory map and programmable new pages
  - Memory map can be loaded to replicate optical module's identification registers
  - Ability to control/monitor all low-speed signals
  - Hot pluggable
- Alarm generation
- State Machine Emulator (CMIS)

CMIS features

- Communicate with, operate and control various MCBs boards.
- Utilize a common software across a variety of form factors.
- Communicate on multiple host simultaneously, by assigning different USB instance to each host.
- In master mode, the analyzer acts as a host module DUT
  - Load or save MSA files
  - Read/Write individual module registers
  - Stretch I2C rate
  - Drive control signals
  - State machine sequencing test with transition timing and test report generation
- In slave mode, the analyzer acts as a module for a host DUT
  - Emulate a pluggable full register mapping
  - Load any MSA file onto analyzer
  - Clock Stretching during I2C transactions

- Monitor host control signals and raise alarms

- In bypass mode, the analyzer monitors exchange between host and module
  - Analyze and log I2C packet exchange between module and host
  - Observe control and alarm signal transactions
  - Monitor VCC levels in real time

SFF Analyzer GUI

VCC tab

The VCC tab allows the measurement of the VCCTX, RX and VCC1. Select the number of samples that will be multiplied by the sampling period selected from the Combo box. The default value of this period is 0.55 µs.

You can add two markers to the graph by right-clicking with the mouse. Make sure to clear all markers to add new ones.

The values of the markers and their difference are displayed under the graph.

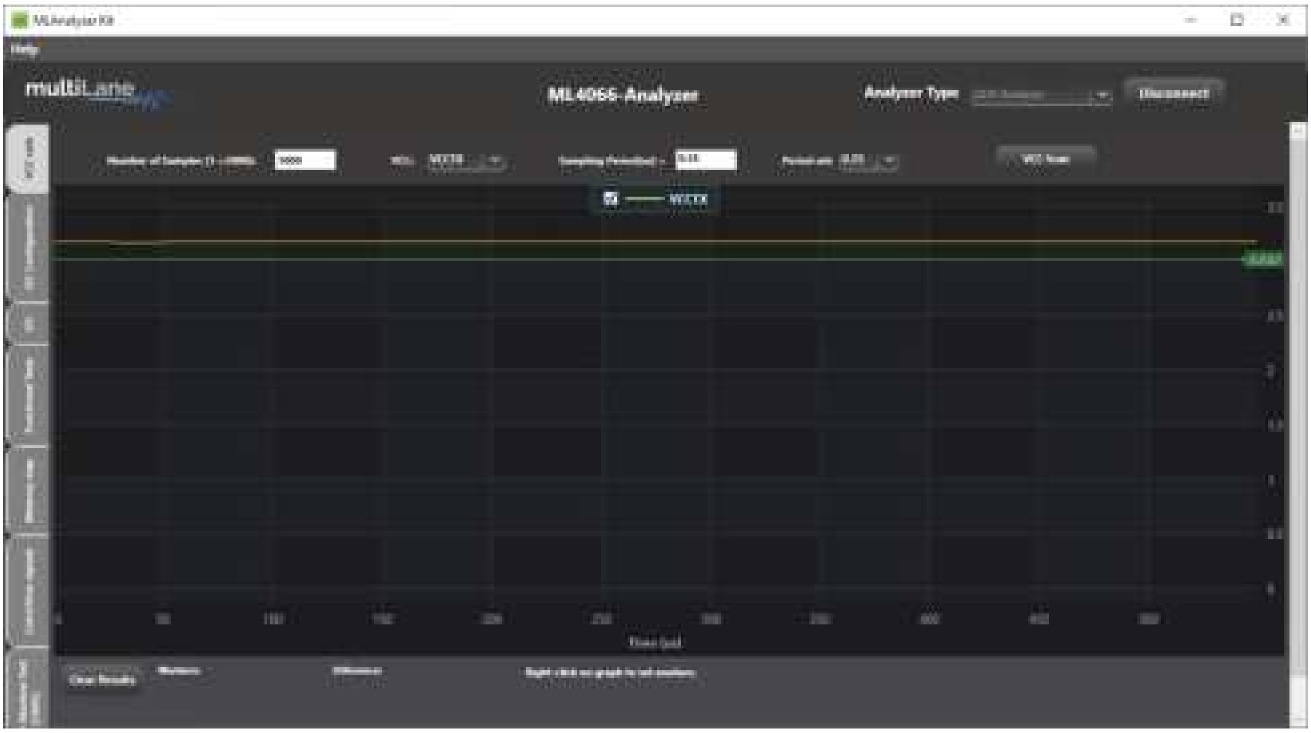
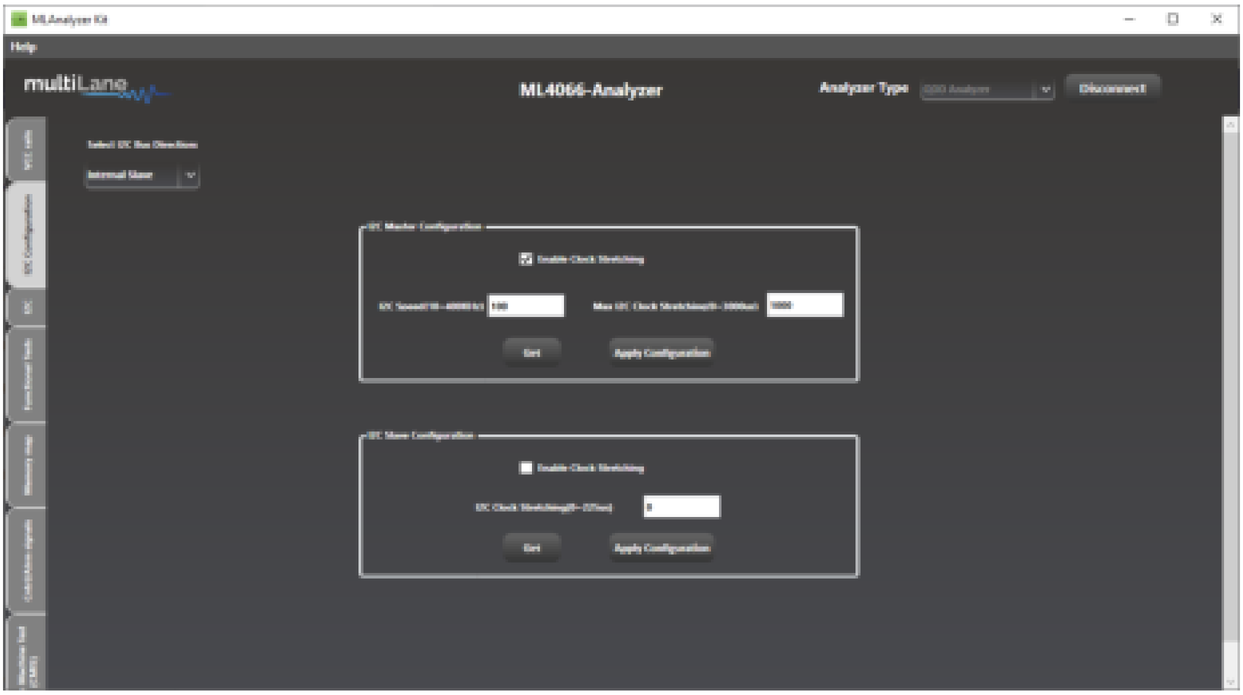


Figure 1: VCC tab

I2C Configuration Tab

This tab allows the user to manually configure the I2C bus direction, speed, and clock stretching.



Select I2C Bus Direction: Internal Slave

☑ Enable Clock Stretching

I2C Speed(10~400KHz) 100

Max I2C Clock Stretching(0~1000us) 1000

□ Enable Clock Stretching

I2C Clock Stretching 0

Figure 2: I2C Capture tab

When choosing **Internal Slave**, you can Read/Write the Data of the Analyzer's EEPROM**. Internal Master** allows User to read/write on the Module*.

Bypass mode makes the communication direct between the module and the host.

For the I2C Master configuration, use the Get button to retrieve the configuration. To change it, write the desired configuration then click "Apply Configuration". The max clock stretching corresponds to the maximum time that the Master waits for the Slave's response. To set the max clock stretching the "Enable Clock Stretching" checkbox must be checked.

For I2C slave configuration, user can choose to enable/disable clock stretching, and can also set the clock stretching time that will be forced on SCL during I2C transactions.

Disclaimer:
**MultiLane supports the replacement of this terminology with more inclusive language. These terms will be retired in the updated CMIS 5.0 specification.*

I2C tab

This tab analyzes the I2C packets. The graph displays the clock (SCL) and the data (SDA). The SCL rising edges are detected and the SDA values are displayed at each rising edge (cf. image below).

A vertical line is drawn at each rising edge and the SDA binary values are displayed under the yellow SDA curve.

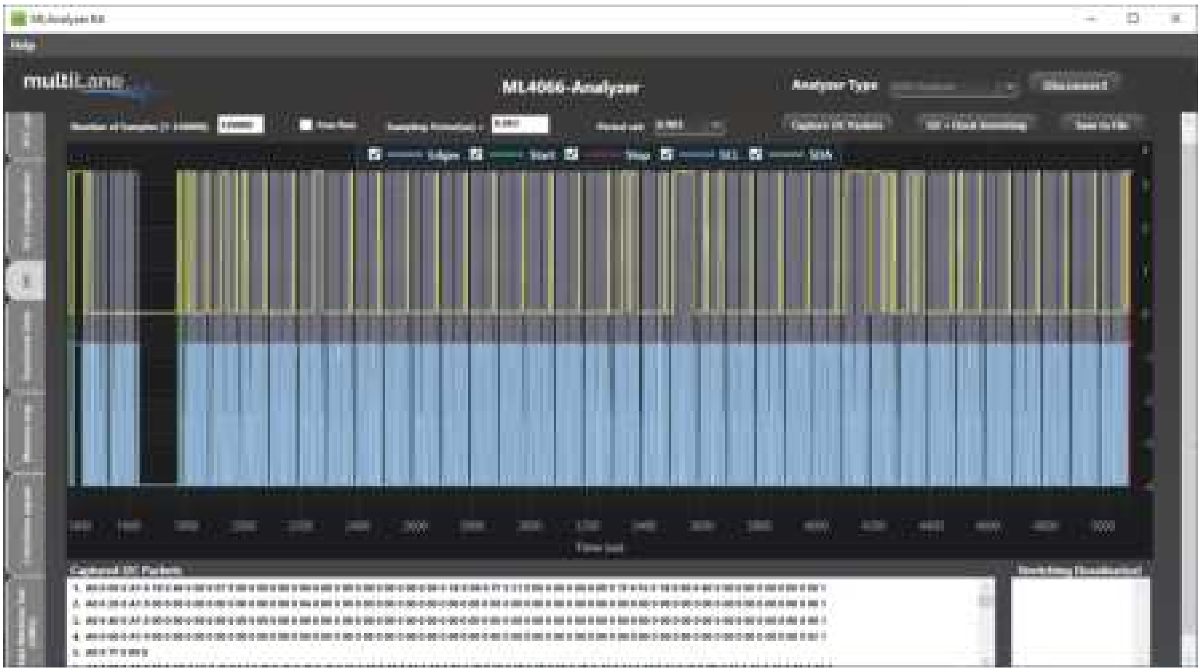


Figure 3: I2C Capture tab

The image above refers to the I2C read command. The data packets are displayed in a list under the graph.

Select the packet that you want to visualize on the graph to see the range of that packet.

Each packet is delimited on the graph by the Start (marked in green) and Stop (marked in red) conditions (cf. image above).
Note that you can show/hide any of the lines by clicking on the corresponding checkbox at the top of the graph.

You can also change the sampling period using the combo box. This period will be multiplied by the number of samples chosen. Its default value is 0.963µs.

To view the reading process, select a higher number of samples so the whole packet can be captured.

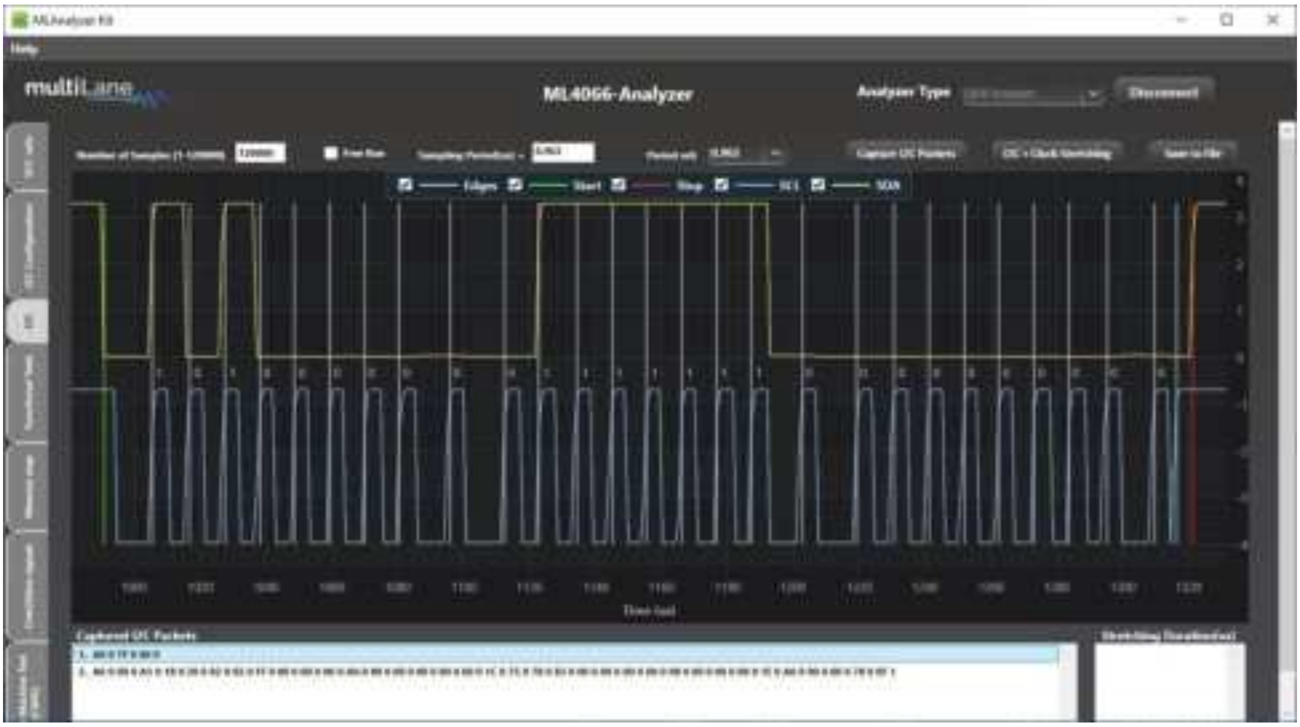


Figure 4: I2C Write

Packet Descriptions

Each packet begins with the slave address A0 followed by the acknowledgment 0. The data afterword is the Data Word (7F is the page selection and 00 is the MemPage needed to write on). The second packet presents the writing process on the address 00(hex).

The free run checkbox is used to monitor the I2C bus. When checked, the monitoring function will start sampling directly after the I2C button is clicked.

When unchecked, the monitoring function will automatically detect I2C start frame.

Functional Tests Tab

The functional tests tab gives access to the memory pages. You can read/write on registers via I2C using this tab. To read/write from the module, select the “Internal Master” bus direction from the I2C configuration tab, or the “Internal Slave” to read/write from the EEPROM.

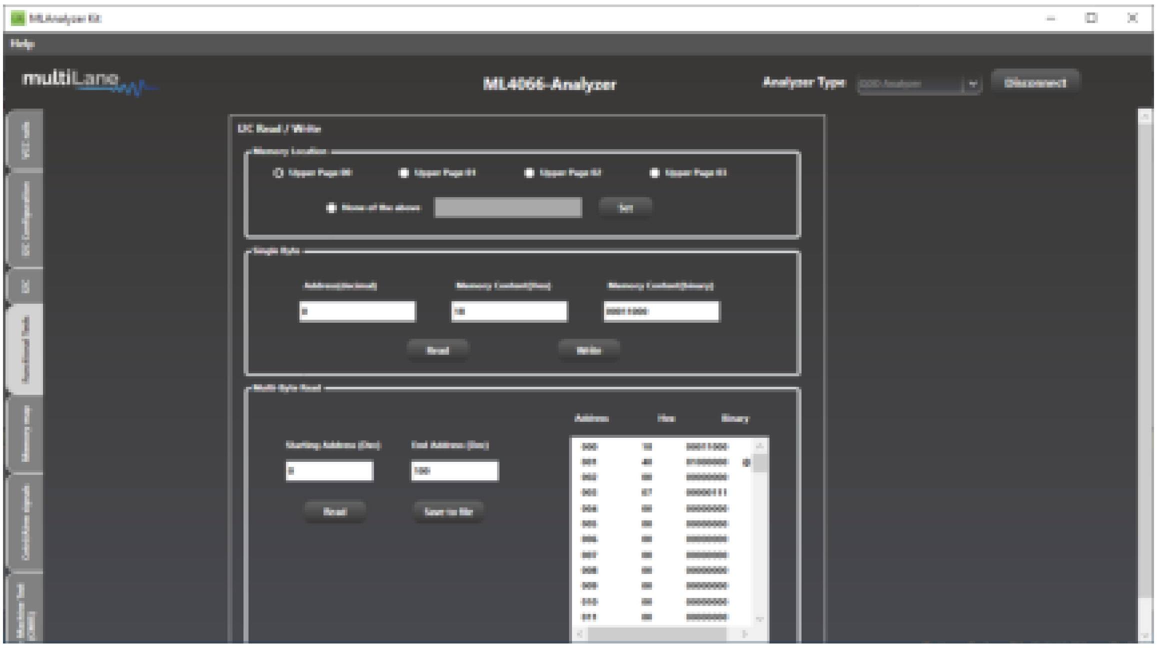


Figure 5: Functional Tests tab

For the SFP-Analyzer, the functional tests tab adds the slave addresses corresponding to the SFP standards.

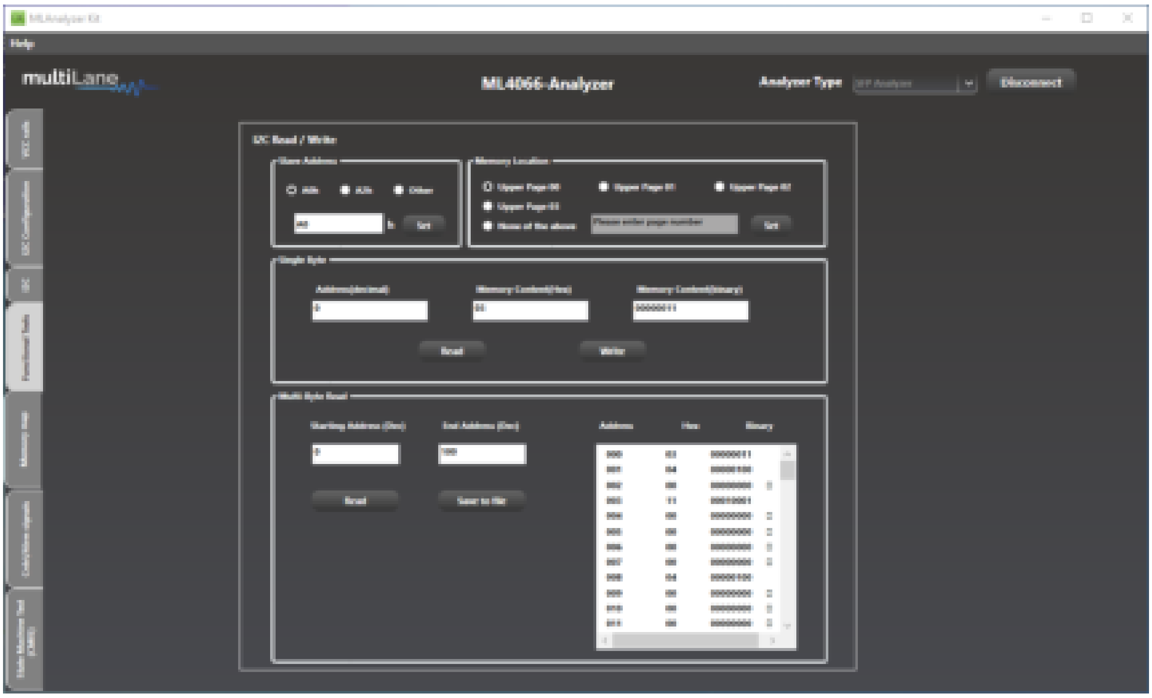


Figure 6: Functional Tests Tab for SFP-Analyzer

I2C Read/Write:

1. First, select which page you need to perform a read or write operation on in the Memory Location.
2. Then, use the “Single Byte” window to read/write one byte from the memory.
    a. Address: The address to read/write from.

b. Memory Content: The data value to be read/written to the selected address (In Hex or in Binary).

3. Alternatively, use the “Multi-byte Read” to read/write multiple bytes between a specified Starting Address and an End Address.

Memory Map Tab

This tab gives access to the memory map of the module. It can be loaded to replicate optical module’s identification registers.

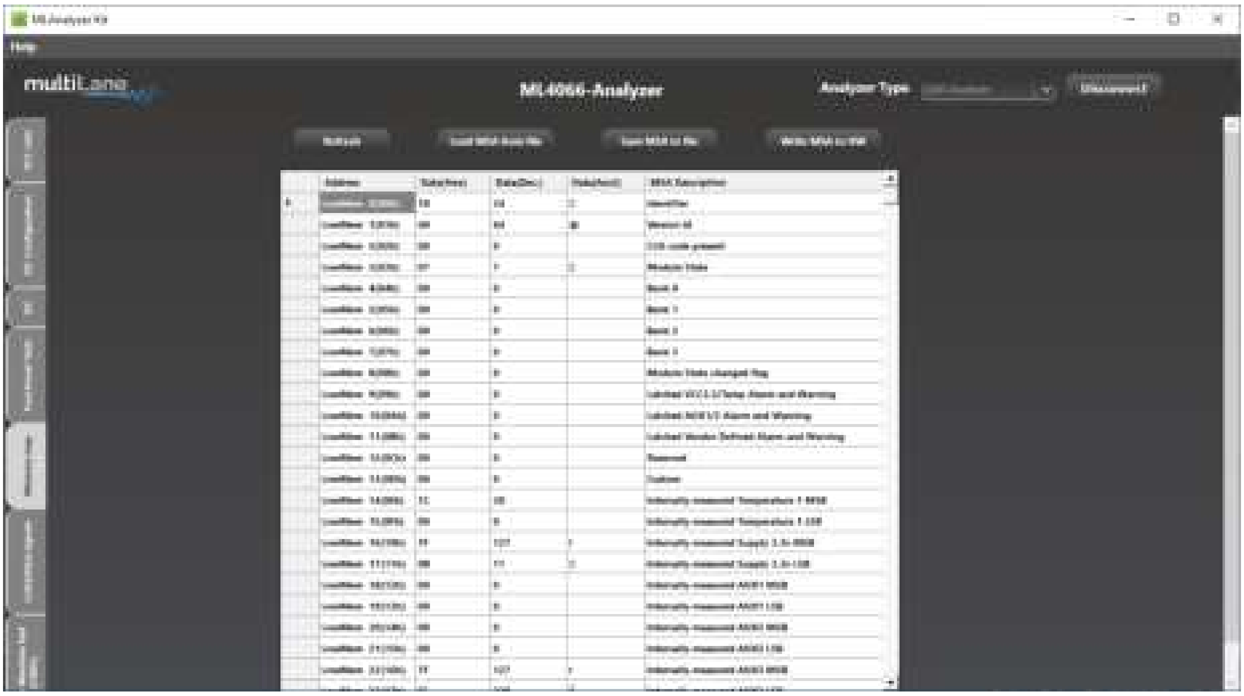


Figure 7: Memory Map tab

This screen allows you to Load or Save your custom MSA configuration.

Data is displayed according to the selected I2C Bus Direction in a grid showing: register address, hex value, Decimal Values, ASCII value, MSA description.

- **Refresh** button: Read MSA Registers, and refresh values.
- **Write MSA to HW** button: Write the current MSA configuration to OSFP module.
- **Save MSA to file** button: Saves the current MSA memory to a file using Comma separated values (CSV) format.
- **Load MSA from file** button: Loads MSA values from file and map it to MSA memory.

When choosing **Internal Slave**, you can Read/Write the Data of the Analyzer’s EEPROM**. Internal Master** allows you to read/write on the Module. **Bypass mode** makes the communication direct between the module and the host.

For the SFP-Analyzer, choose your desired slave address and page to read it.

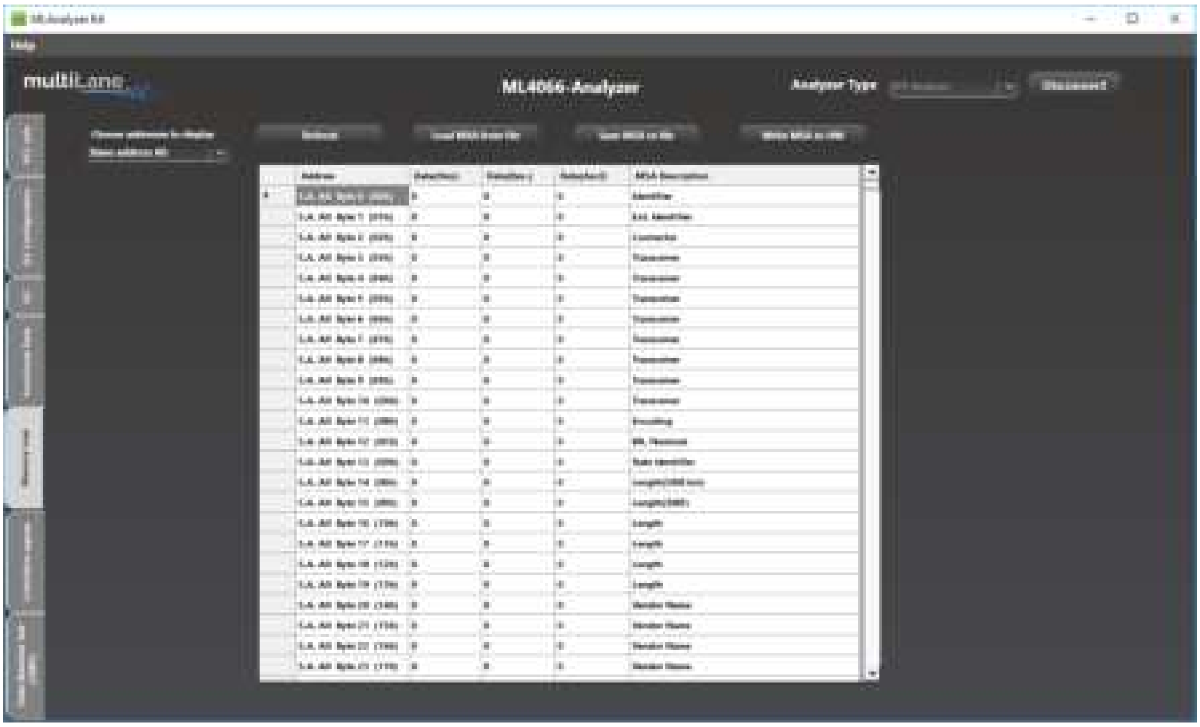


Figure 8: Memory Map tab in SFP analyzer

CNTRL/ALRM Signals tab

This tab allows detection and measurement of host pull up resistors on low speed signals and the detection of their state (either digital or analog). You can also drive these signals using the corresponding checkboxes.

- Pull-Up Resistors window: The analyzer detects if the pull-up resistor of each signal is missing or not and it calculates its value. The range between 1.3 KΩ and 10 KΩ is acceptable indicating that a pull-up resistor is present. Below 1.3 KΩ the resistor value is too low and you a short circuit. Above 10 KΩ you risk an open circuit. The marge of accuracy for the resistor's value is about 1 KΩ.
- For each signal the desired mode "Drive", "Bypass" or "Analog Sampler" is chosen. The Analog Monitor button displays the voltage of the desired signal. To manually assert/de-assert the signals, the "Drive" option must be chosen to be able to toggle the signal's checkbox. Finally, if "Bypass" mode is selected, you can control the module externally and check its status by pressing the "Get" button.
- The Refresh button resets the signals in "Drive" mode to their initial states.

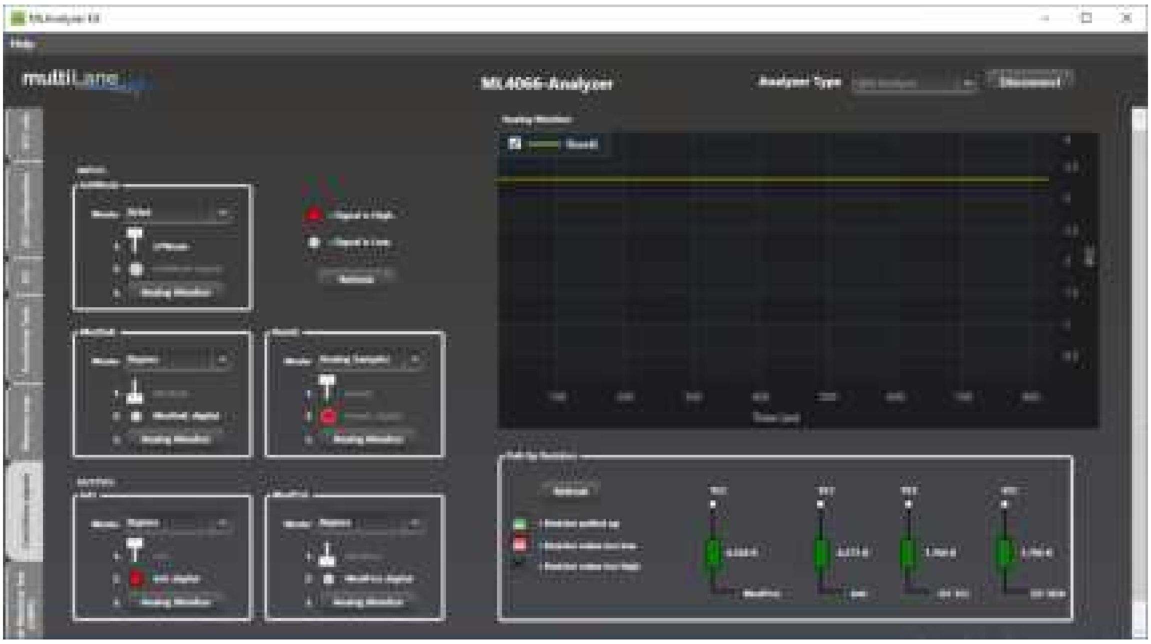


Figure 9: Cntrl/Alrm signals tab 1 in QDD analyzer

The pin pull-up resistors will differ depending on the form factor of the adaptor and module.

The SFP has different low speed control signals as seen in the figure below.

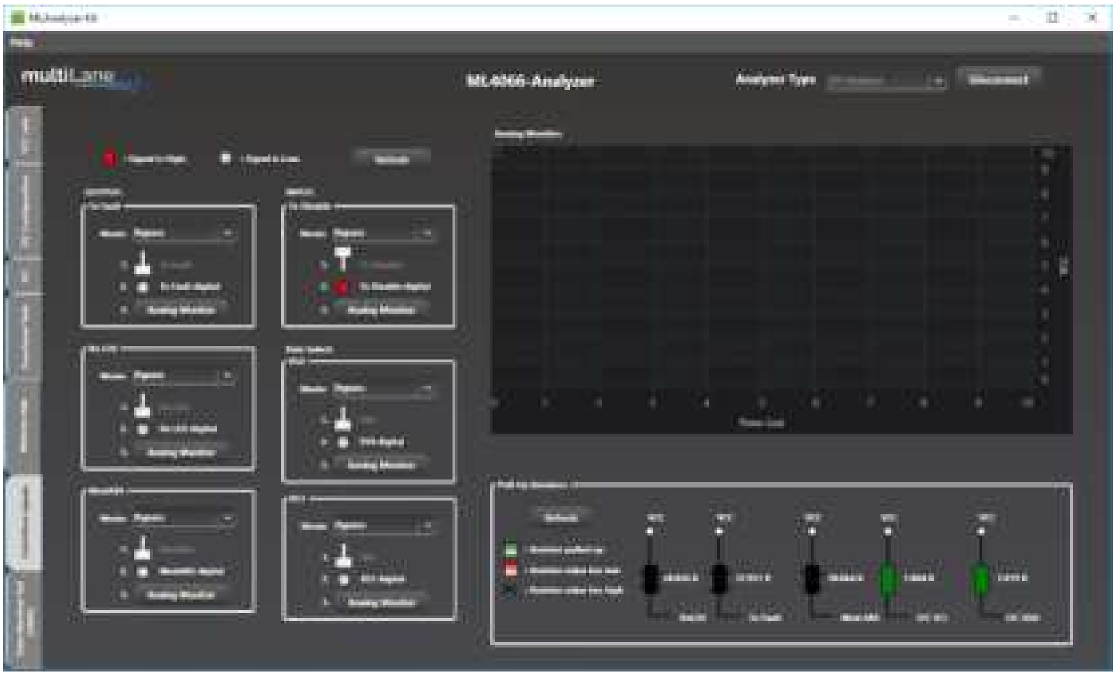


Figure 10: SFP-Analyzer Control signals

Application Notes

I2C Tab

1. Select “Bypass” mode from the “I2C Configuration” tab.

2. In the I2C tab, select the number of samples for the I2C capture, for the I2C read itshould be the maximum.
3. Without selecting the “free run” checkbox, click the I2C button to start monitoring, then using your host send an I2C command (read or write) and wait for the I2C FrameCapture.
4. If the “free run” checkbox is selected, the capturing will start immediately after the I2C buttonis clicked.

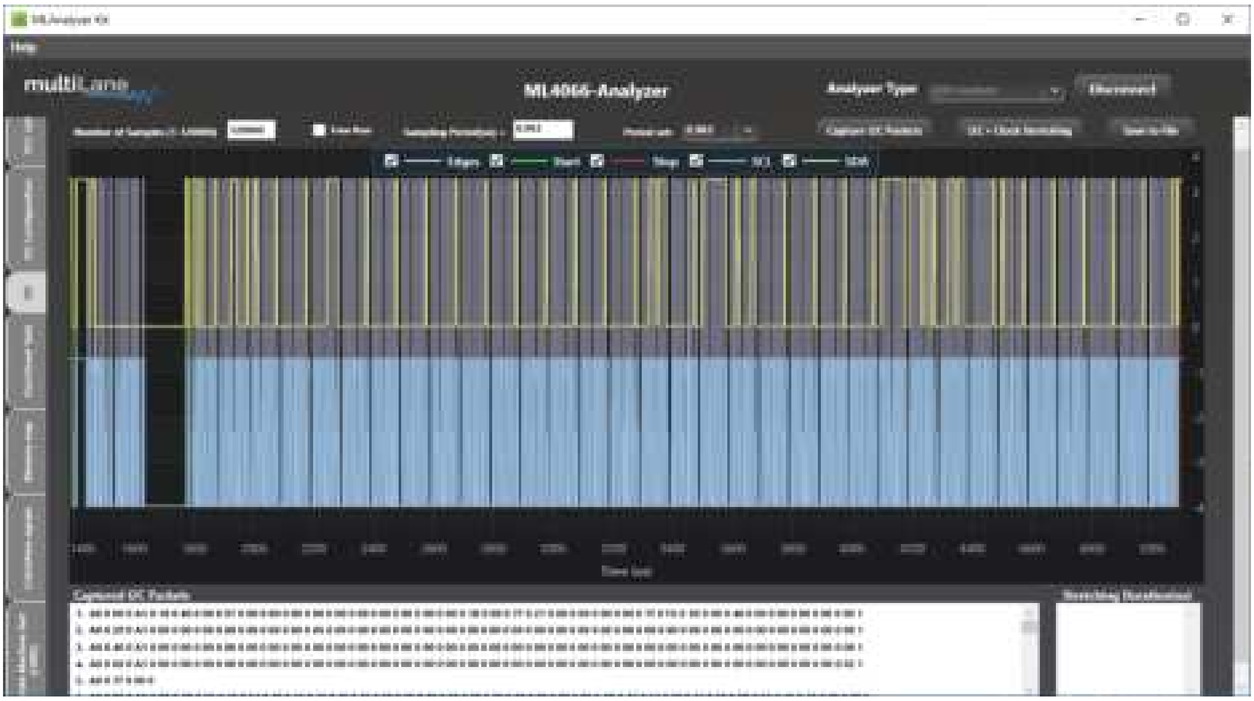


Figure 11: I2C Read

Functional Tests Tab

1. Select “Bypass” mode in the I2C configuration tab, using your host try to read/write a value from the module. In the Analyzer GUI, the read/write won’t work in this mode because the Host and module communicate directly without the interference of the Analyzer.

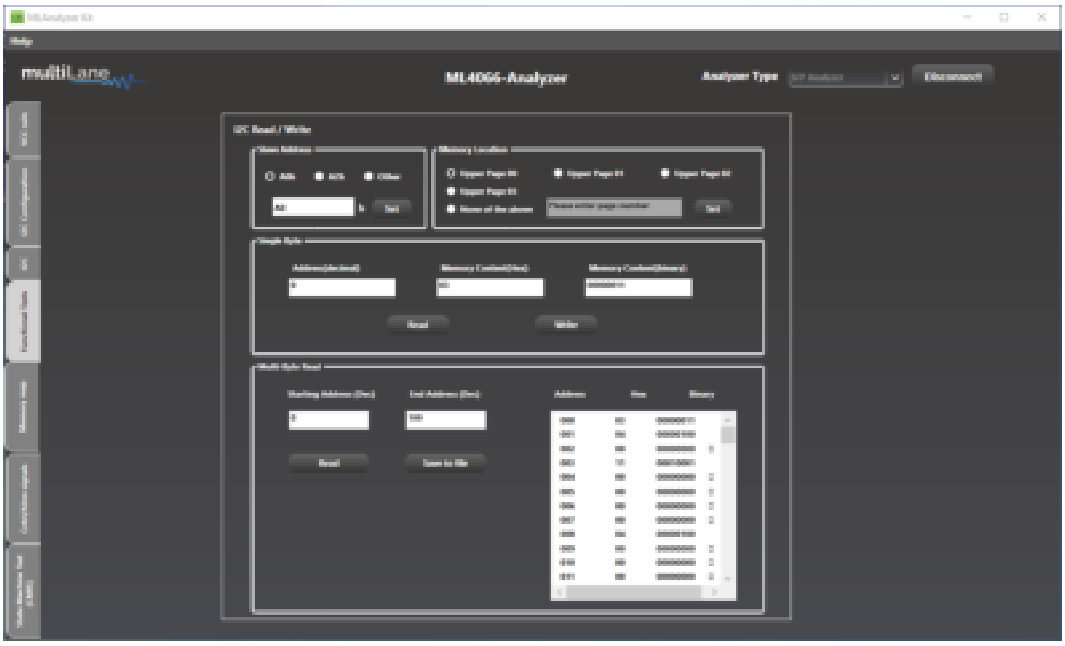


Figure 12: Functional Tab in Master Mode

2. Select “Internal Master” mode in the I2C configuration tab, read address 0 using the Analyzer GUI. This value refers to the one written on the module. The connection between the Host and the Analyzer is cut and using the Host to read will give you FF values.

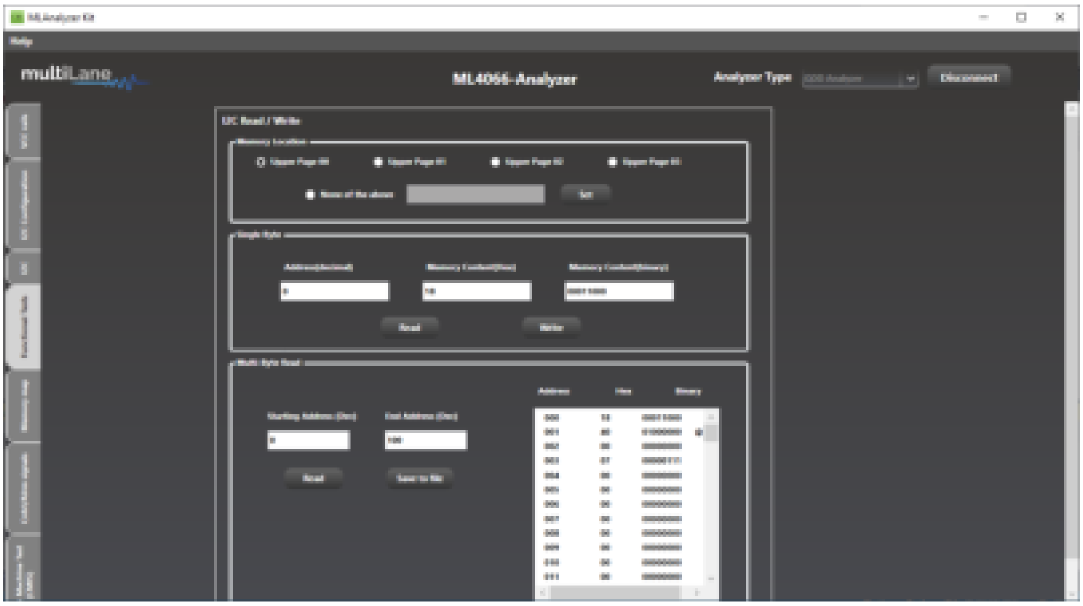


Figure 13: Functional Tab in Slave Mode

3. Select “Internal Slave” mode in the I2C configuration tab, the reading/writing command from the Analyzer or your Host will give the same value written in the EEPROM.

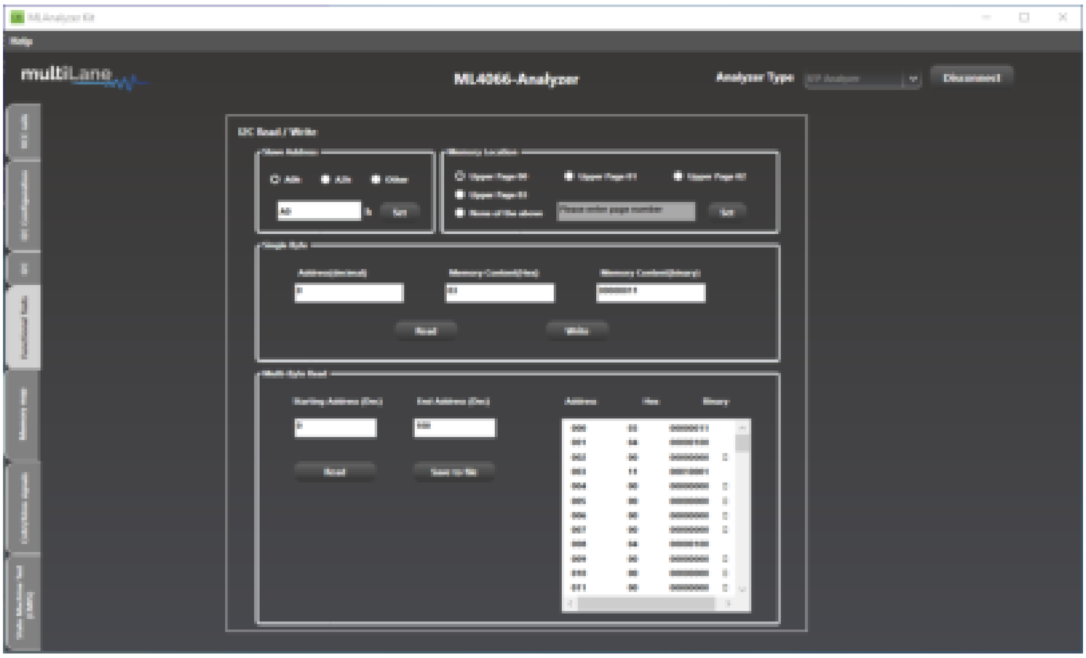


Figure 14: Reading Specific Registers from Functional Tests Tab

When clicking "Refresh" in the "Memory Map" tab, the grid displays all data written in the registers and follows the rules above.

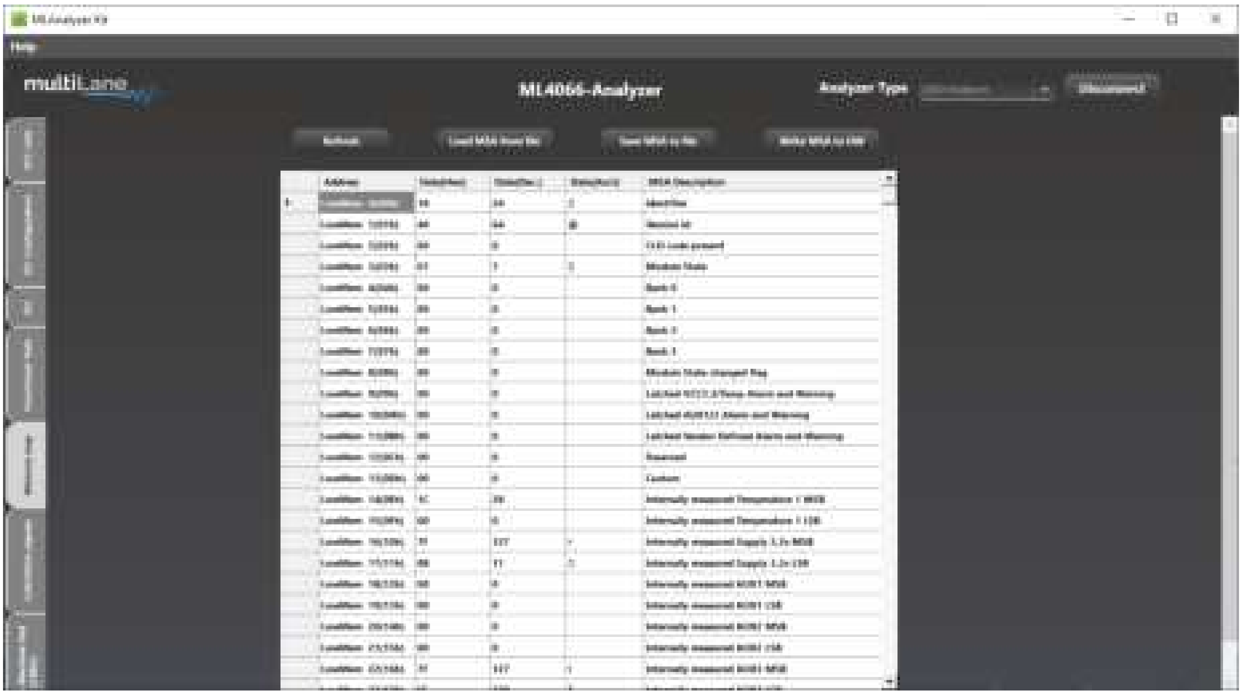


Figure 15: Internal Master

Cntrl/Alrm Tab

1. The refresh button gets the Status of the signals at the "Drive" mode and the checkboxes reflect its condition.

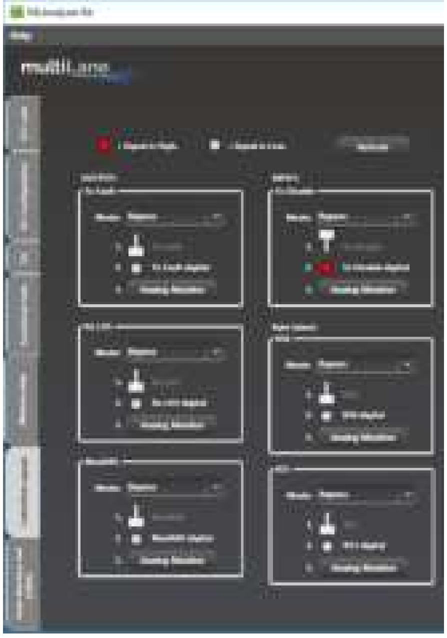


Figure 16: Cntrl/Alarm Tab

2. Select "Drive" mode for ResetL and toggle the checkbox, the ResetL signal of the module will be activated or deactivated.
3. Select "Bypass" mode, from Host try to trigger the ResetL signal. Check the analyzer GUI's status by clicking on "Get" button.
4. Select "Analog Monitor" mode and click on the "Analog Monitor" button of ResetL. The graph displays its DC voltage level from the Host side.

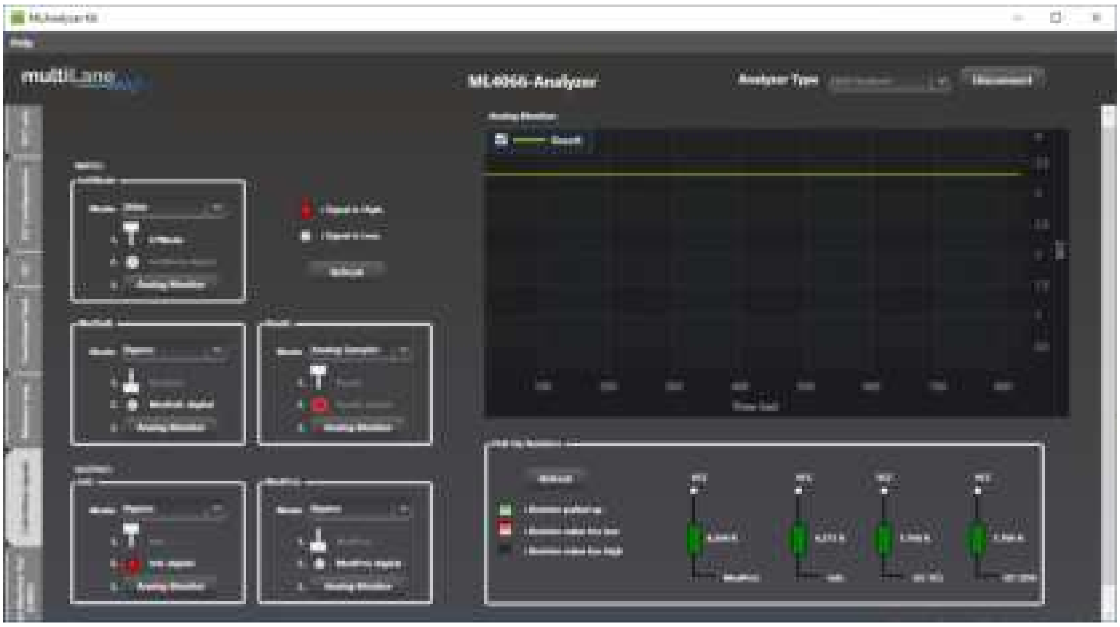


Figure 17: Reading ResetL from the Analog Monitor Window

5. In the “Pull-Up Resistors” Groupbox, click the “Refresh” button, the values displayed are the values of the pullup resistors at the Host.

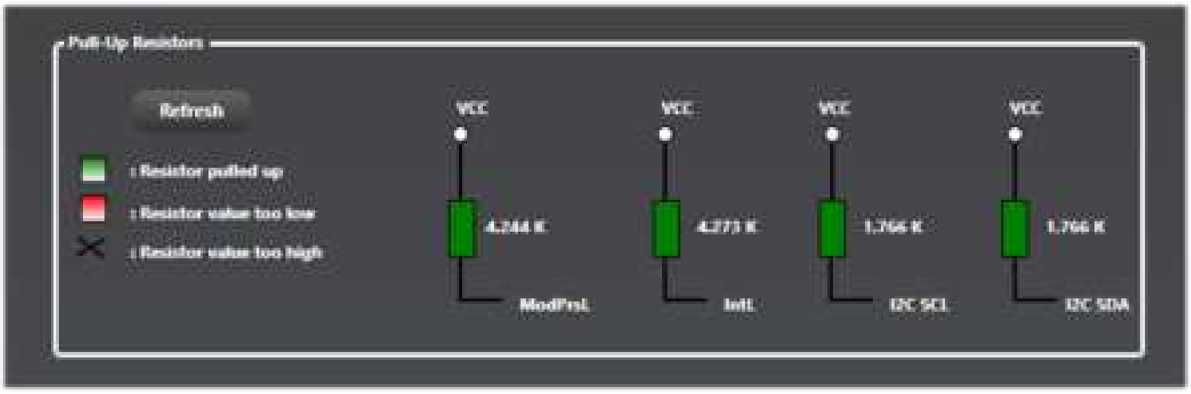
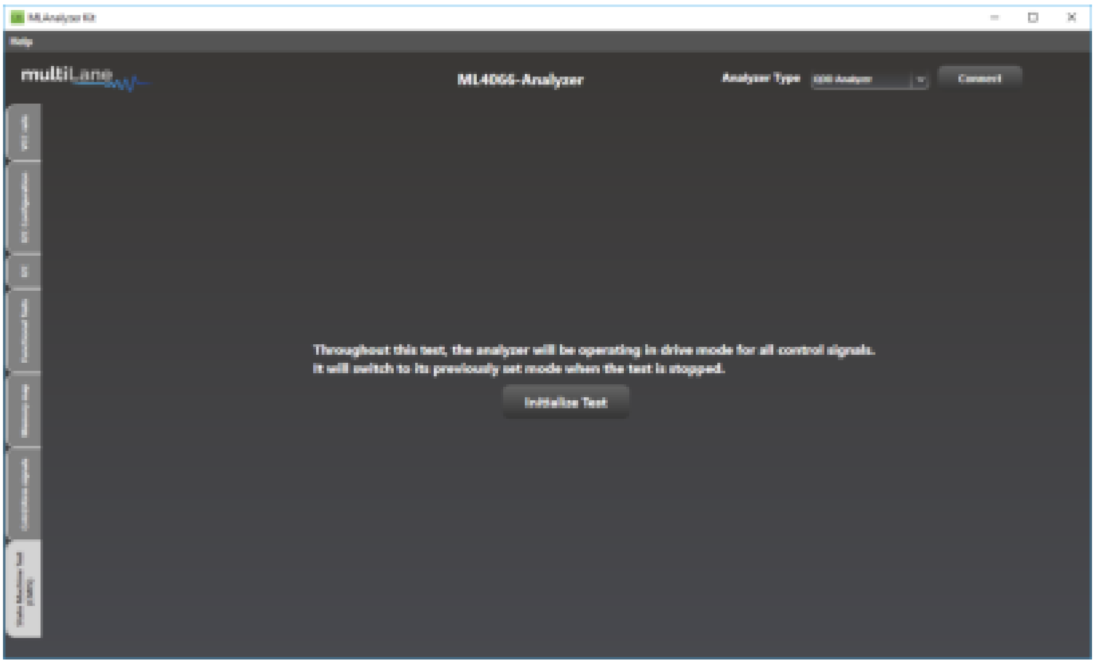


Figure 18: Pull-Up Resistor Values

CMIS State Machine Test

This analyzer test works for all QSFP and QDD modules that are both CMIS 3.0 and CMIS 4.0 compliant. In CMIS 3.0, the test skips the low power if the configuration is set to high when transitioning from state to state. In CMIS 4.0, the transition passes through the low power configuration to get to high power.

The Module State Machine is engaged after module insertion and power on, and thus the test can be started. During the test, different state transitions can be shown and tested by toggling the desired destination state. The Module State Machine is different for devices implementing a paged memory map and those implementing a flat (non-paged) memory map.



Throughout this test, the analyzer will be operating in drive mode for all control signals.
It will switch to its previously set mode when the test is stopped.

Figure 19: Landing Page for State Machine Test

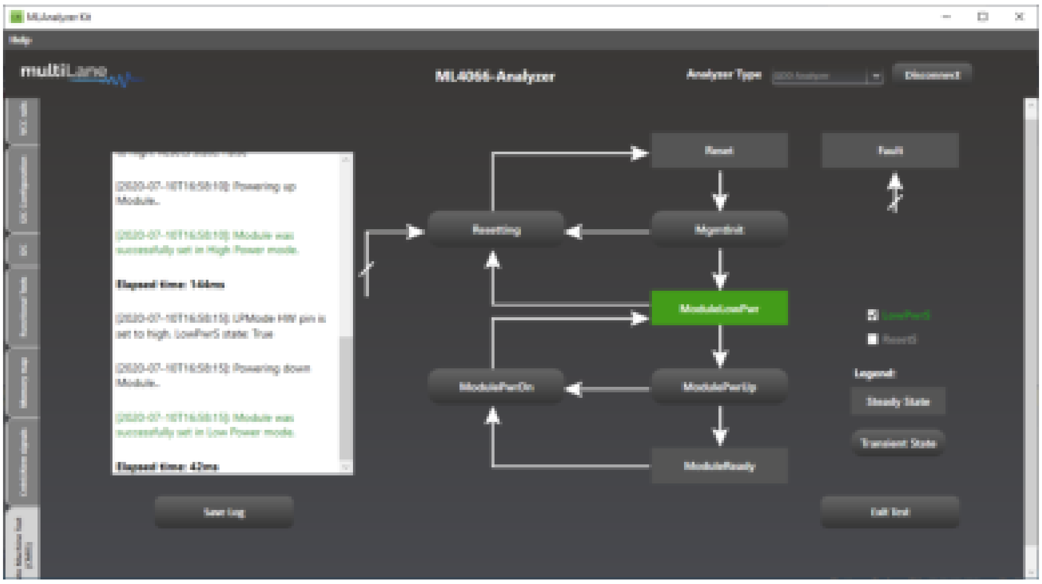
Upon test initialization, the CMIS compliance version is verified and module type is detected. If the latter is not feasible the test will not start.

Paged Memory Modules

If the detected module implements a paged memory map, the diagram below appears and displays the current state of the module and the transition signals.

Toggle another steady state (Reset, ModuleLowPwr, ModuleReady) to switch to it. State and transition signal changes will appear and events will be logged in the logging box. Logged events can be saved to a text file possessing the module serial number and the time the test was done.

If an error occurs while transitioning, the module will be thrown into a “Fault” state. This state can be exited only by resetting the module.



```
[2020-07-10T16:58:10]: Powering up Module.

[2020-07-10T16:58:10]: Module was successfully set in High Power mode.

Elapsed time: 144ms

[2020-07-10T16:58:15]: LPMode HW pin is set to high. LowPwrS state: True

[2020-07-10T16:58:15]: Powering down Module.

[2020-07-10T16:58:15]: Module was successfully set in Low Power mode.

Elapsed time: 42ms
```

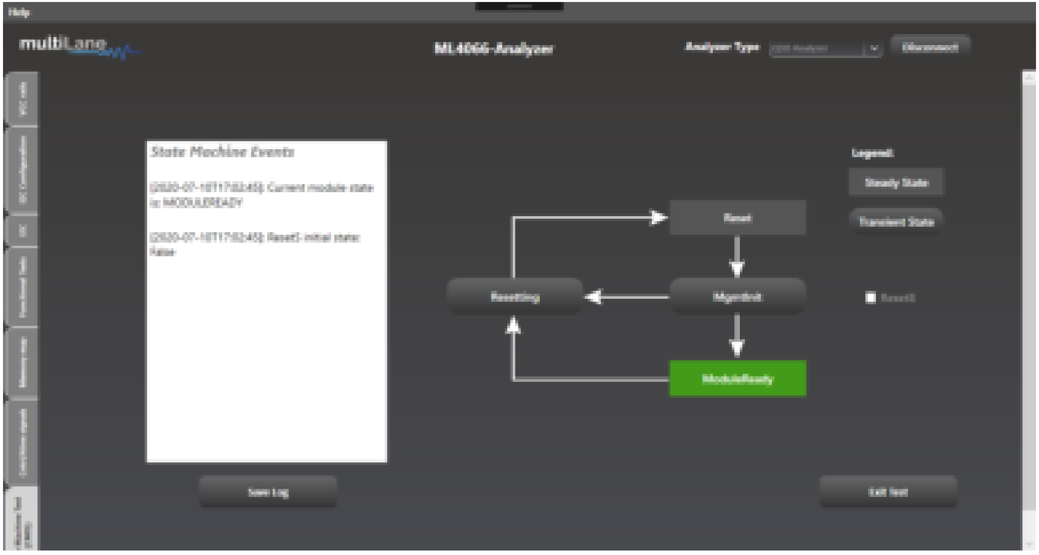
Figure 20: State Machine Test for Paged Memory Modules

Flat Memory Modules

If the detected module implements a flat (non-paged) memory map, the diagram below appears, displaying the current state of the module and the transition signal.

Toggle any of the steady states (Reset or ModuleReady) to switch between them. State and transition signal changes will appear and events will be logged in the logging box. Logged events can be saved to a text file possessing the module serial number and the time the test was done.

If an error occurs while transitioning, the module will be stuck in the transition state until resetting the module or re-initializing the test.



```
State Machine Events

[2020-07-10T17:02:45]: Current module state is: MODULEREADY

[2020-07-10T17:02:45]: ResetS initial state: False
```

Figure 21: State Machine Test for Flat Memory Modules

Appendix I: Analyzer Card Diagram