SLAS040J – MAY 2001 – REVISED DECEMBER 2006

- Low Supply-Voltage Range, 1.8 V to 3.6 V
- Ultralow Power Consumption
  - Active Mode: 200 μA at 1 MHz, 2.2 V
  - Standby Mode: 0.7 μA
  - Off Mode (RAM Retention): 0.1 μA
- Five Power-Saving Modes
- Wake-Up From Standby Mode in Less Than 6 μs
- Frequency-Locked Loop (FLL+)
- 16-Bit RISC Architecture, 125-ns Instruction Cycle Time
- 16-Bit Timer_A With Three or Five† Capture/Compare Registers
- Integrated LCD Driver for 96 Segments
- On-Chip Comparator
- Brownout Detector
- Supply Voltage Supervisor/Monitor – Programmable Level Detection on MSP430F415/417 Devices Only
- Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse
- Bootstrap Loader in Flash Devices
- Family Members Include:
  - MSP430C412: 4KB ROM, 256B RAM
  - MSP430C413: 8KB ROM, 256B RAM
  - MSP430F412: 4KB + 256B Flash 256B RAM
  - MSP430F413: 8KB + 256B Flash 256B RAM
  - MSP430F415: 16KB + 256B Flash 512B RAM
  - MSP430F417: 32KB + 256B Flash 1KB RAM
- Available in 64-Pin QFP (PM) and 64-Pin QFN (RTD/RGC) Packages
- For Complete Module Descriptions,See the *MSP430x4xx Family User's Guide*, Literature Number SLAU056

† Timer_A5 in 'F415 and 'F417 devices only

description

The Texas Instruments MSP430 family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6 μs.

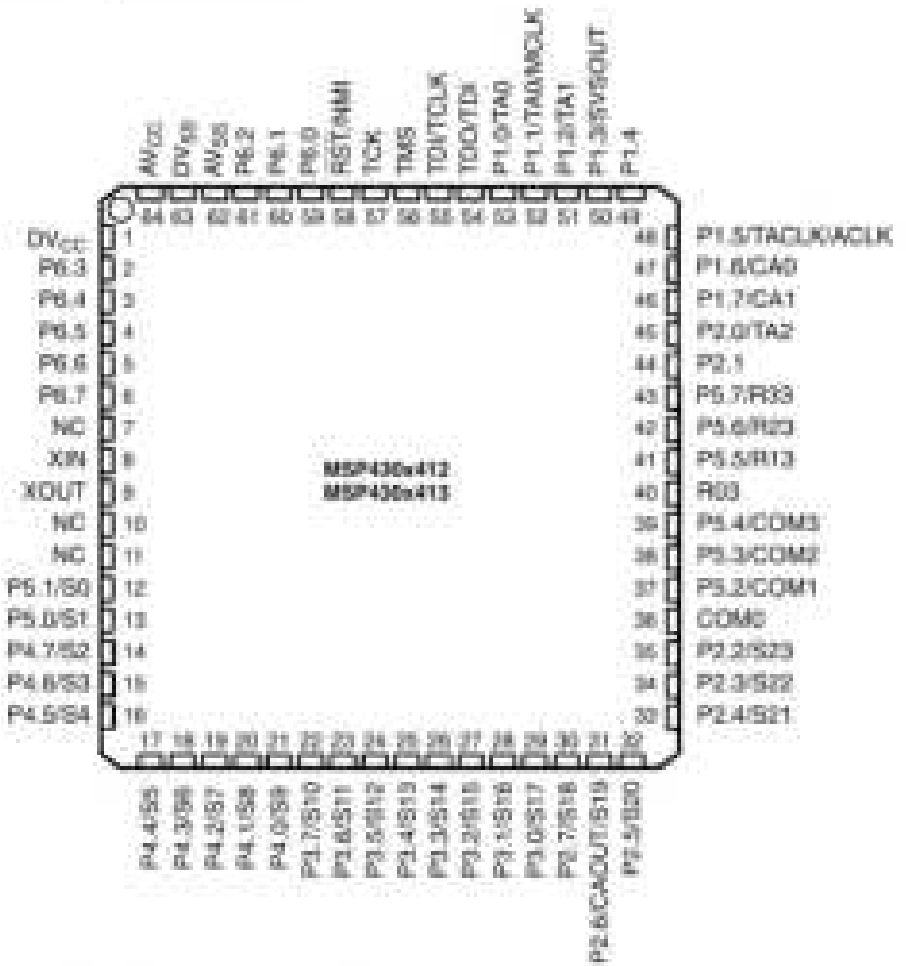
The MSP430x41x series are microcontroller configurations with one or two built-in 16-bit timers, a comparator, 96 LCD segment drive capability, and 48 I/O pins.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and process the data and transmit them to a host system. The comparator and timer make the configurations ideal for industrial meters, counter applications, handheld meters, etc.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	PLASTIC 64-PIN QFP (PM)	PLASTIC 64-PIN QFN (RTD/RGC)
–40°C to 85°C	MSP430C412PM MSP430C413PM MSP430F412PM MSP430F413PM MSP430F4133PM MSP430F417PM	MSP430C412IRGC MSP430C413IRGC MSP430F412IRTD MSP430F413IRTD MSP430F4153IRTD MSP430F417IRTD

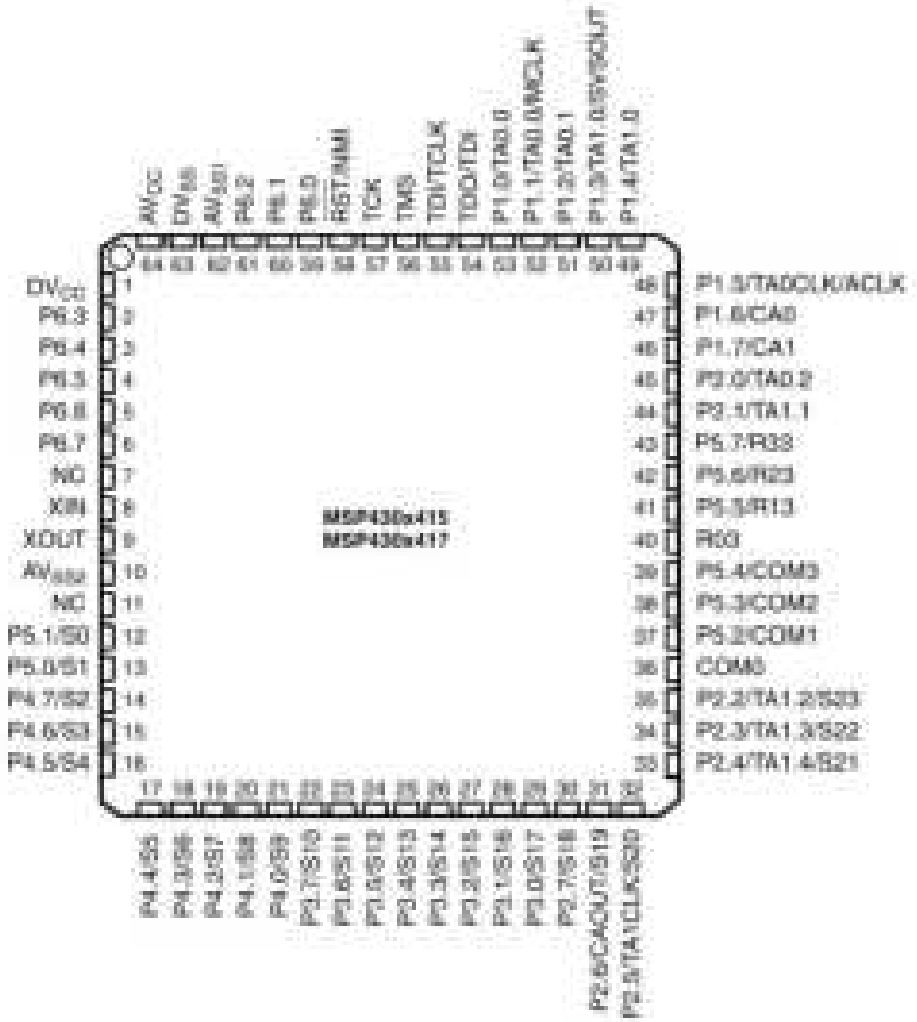
pin designation – MSP430x412, MSP430x413



NC – No internal connection. External connection to V_{SS} recommended

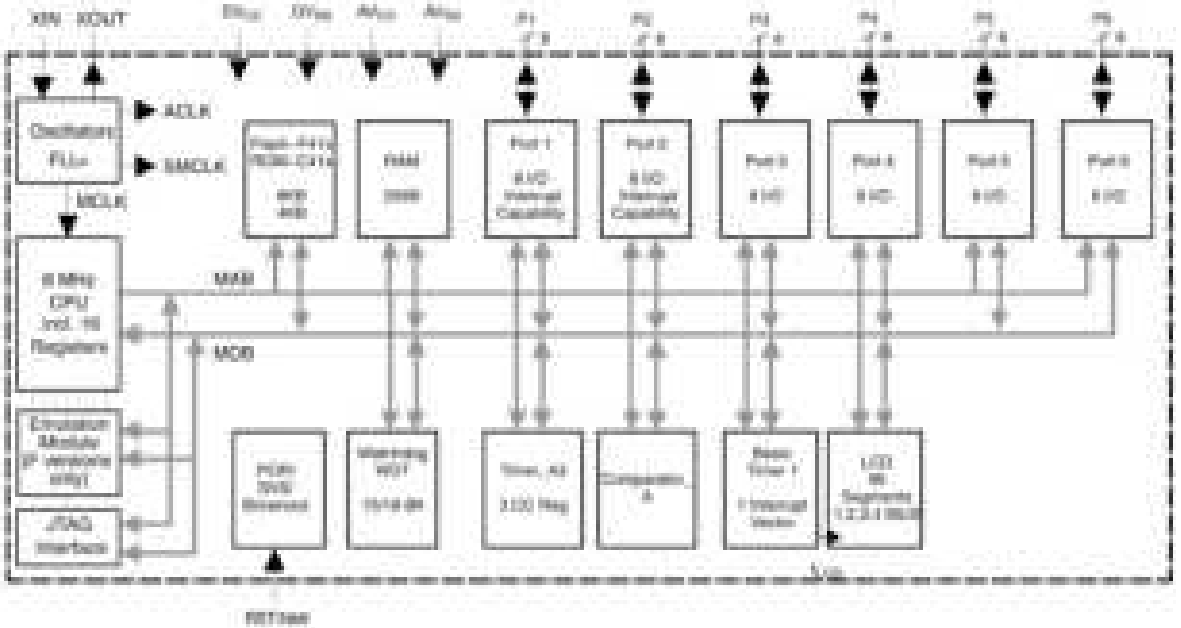
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

pin designation – MSP430x415, MSP430x417

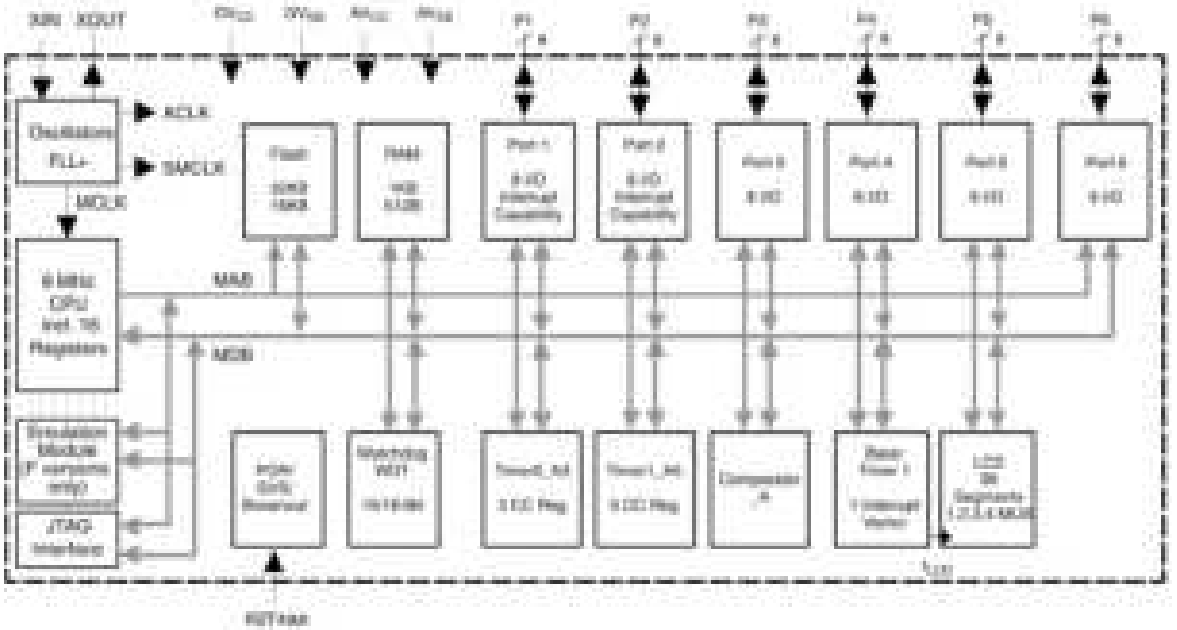


NC – No internal connection. External connection to V_{SS} recommended.

functional block diagram – MSP430x412, MSP430x413



functional block diagram – MSP430x415, MSP430x417



Terminal Functions – MSP430x412, MSP430x413

TERMINAL NAME	NO.	I/O	DESCRIPTION
AV_{CC}	64		Positive terminal that supplies SVS, brownout, oscillator, comparator_A, port 1, and LCD resistive divider circuitry; must not power up prior to DV_{CC}
AV_{SS}	62		Negative terminal that supplies SVS, brownout, oscillator, comparator_A. Needs to be externally connected to DV_{SS}
DV_{CC}	1		Digital supply voltage, positive terminal. Supplies all parts, except those which are supplied via AV_{CC}
DV_{SS}	63		Digital supply voltage, negative terminal. Supplies all digital parts, except those which are supplied via AV_{CC}/AV_{SS}
NC	7, 10, 11		Not internally connected. Connection to V_{SS} recommended.
P1.0/TA0	53	I/O	General-purpose digital I/O / Timer_A, Capture: CCI0A input, compare: Out0 output/BSL transmit
P1.1/TA0/MCLK	52	I/O	General-purpose digital I/O / Timer_A, Capture: CCI0B input/MCLK output. Note: TA0 is only an input on this pin/BSL receive.
P1.2/TA1	51	I/O	General-purpose digital I/O / Timer_A, Capture: CCI1A input, compare: Out1 output
P1.3/SVSOUT	50	I/O	General-purpose digital I/O / SVS: output of SVS comparator
P1.4	49	I/O	General-purpose digital I/O
P1.5/TACLK/ ACLK	48	I/O	General-purpose digital I/O / Input of Timer_A clock/output of ACLK
P1.6/CA0	47	I/O	General-purpose digital I/O / Comparator_A input
P1.7/CA1	46	I/O	General-purpose digital I/O / Comparator_A input
P2.0/TA2	45	I/O	General-purpose digital I/O / Timer_A capture: CCI2A input, compare: Out2 output
P2.1	44	I/O	General-purpose digital I/O
P2.2/S23	35	I/O	General-purpose digital I/O / LCD segment output 23 (see Note 1)
P2.3/S22	34	I/O	General-purpose digital I/O / LCD segment output 22 (see Note 1)
P2.4/S21	33	I/O	General-purpose digital I/O / LCD segment output 21 (see Note 1)
P2.5/S20	32	I/O	General-purpose digital I/O / LCD segment output 20 (see Note 1)
P2.6/CAOUT/S19	31	I/O	General-purpose digital I/O / Comparator_A output/LCD segment output 19 (see Note 1)
P2.7/S18	30	I/O	General-purpose digital I/O / LCD segment output 18 (see Note 1)
P3.0/S17	29	I/O	General-purpose digital I/O / LCD segment output 17 (see Note 1)
P3.1/S16	28	I/O	General-purpose digital I/O / LCD segment output 16 (see Note 1)
P3.2/S15	27	I/O	General-purpose digital I/O / LCD segment output 15 (see Note 1)
P3.3/S14	26	I/O	General-purpose digital I/O / LCD segment output 14 (see Note 1)
P3.4/S13	25	I/O	General-purpose digital I/O / LCD segment output 13 (see Note 1)
P3.5/S12	24	I/O	General-purpose digital I/O / LCD segment output 12 (see Note 1)
P3.6/S11	23	I/O	General-purpose digital I/O / LCD segment output 11 (see Note 1)
P3.7/S10	22	I/O	General-purpose digital I/O / LCD segment output 10 (see Note 1)

NOTE 1: LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.

Terminal Functions – MSP430x412, MSP430x413 (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
P4.0/S9	21	I/O	General-purpose digital I/O / LCD segment output 9 (see Note 1)
P4.1/S8	20	I/O	General-purpose digital I/O / LCD segment output 8 (see Note 1)
P4.2/S7	19	I/O	General-purpose digital I/O / LCD segment output 7 (see Note 1)
P4.3/S6	18	I/O	General-purpose digital I/O / LCD segment output 6 (see Note 1)
P4.4/S5	17	I/O	General-purpose digital I/O / LCD segment output 5 (see Note 1)
P4.5/S4	16	I/O	General-purpose digital I/O / LCD segment output 4 (see Note 1)
P4.6/S3	15	I/O	General-purpose digital I/O / LCD segment output 3 (see Note 1)
P4.7/S2	14	I/O	General-purpose digital I/O / LCD segment output 2 (see Note 1)
P5.0/S1	13	I/O	General-purpose digital I/O / LCD segment output 1 (see Note 1)
P5.1/S0	12	I/O	General-purpose digital I/O / LCD segment output 0 (see Note 1)
COM0	36	O	Common output. COM0–3 are used for LCD backplanes.
P5.2/COM1	37	I/O	General-purpose digital I/O / Common output. COM0–3 are used for LCD backplanes.
P5.3/COM2	38	I/O	General-purpose digital I/O / Common output. COM0–3 are used for LCD backplanes.
P5.4/COM3	39	I/O	General-purpose digital I/O / Common output. COM0–3 are used for LCD backplanes.
R03	40	I	Input port of fourth positive (lowest) analog LCD level (V5)
P5.5/R13	41	I/O	General-purpose digital I/O / Input port of third most positive analog LCD level (V4 or V3)
P5.6/R23	42	I/O	General-purpose digital I/O / Input port of second most positive analog LCD level (V2)
P5.7/R33	43	I/O	General-purpose digital I/O / Output port of most positive analog LCD level (V1)
P6.0	59	I/O	General-purpose digital I/O
P6.1	60	I/O	General-purpose digital I/O
P6.2	61	I/O	General-purpose digital I/O
P6.3	2	I/O	General-purpose digital I/O
P6.4	3	I/O	General-purpose digital I/O
P6.5	4	I/O	General-purpose digital I/O
P6.6	5	I/O	General-purpose digital I/O
P6.7	6	I/O	General-purpose digital I/O
RST/NMI	58	I	Reset input / Nonmaskable interrupt input
TCK	57	I	Test clock. TCK is the clock input port for device programming and test.
TDI/TCLK	55	I	Test data input / Test clock input. The device protection fuse is connected to TDI.
TDO/TDI	54	I/O	Test data output port. TDO/TDI data output or programming data input terminal.
TMS	56	I	Test mode select. TMS is used as an input port for device programming and test.
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output terminal of crystal oscillator XT1
QFN Pad	NA	NA	QFN package pad connection to V_{SS} recommended.

NOTE 2: LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.

Terminal Functions – MSP430x415, MSP430x417

TERMINAL NAME	NO.	I/O	DESCRIPTION
AV_{CC}	64		Positive terminal that supplies SVS, brownout, oscillator, comparator_A, port 1, and LCD resistive divider circuitry; must not power up prior to DV_{CC}
AV_{SS1}	62		Negative terminal that supplies SVS, brownout, oscillator, comparator_A. Needs to be externally connected to DV_{SS}.
DV_{CC}	1		Digital supply voltage, positive terminal. Supplies all parts, except those which are supplied via AV_{CC}.
DV_{SS}	63		Digital supply voltage, negative terminal. Supplies all digital parts, except those which are supplied via AV_{CC}/AV_{SS}.
AV_{SS2}	10		Negative terminal that supplies SVS, brownout, oscillator, comparator_A. Needs to be externally connected to DV_{SS}.
NC	7, 11		Not internally connected. Connection to V_{SS} recommended.
P1.0/TA0.0	53	I/O	General-purpose digital I/O / Timer0_A Capture: CCI0A input, compare: Out0 output/BSL transmit
P1.1/TA0.0/MCLK	52	I/O	General-purpose digital I/O / Timer0_A Capture: CCI0B input/MCLK output. Note: TA0 is only an input on this pin/BSL receive
P1.2/TA0.1	51	I/O	General-purpose digital I/O / Timer0_A capture: CCI1A input, compare: Out1 output
P1.3/TA1.0/ SVSOUT	50	I/O	General-purpose digital I/O / Timer1_A capture: CCI0B input/SVS output of SVS comparator
P1.4/TA1.0	49	I/O	General-purpose digital I/O / Timer1_A capture: CCI0A input, compare: Out0 output
P1.5/TA0CLK/ ACLK	48	I/O	General-purpose digital I/O / input of Timer0_A clock/output of ACLK
P1.6/CA0	47	I/O	General-purpose digital I/O / Comparator_A input
P1.7/CA1	46	I/O	General-purpose digital I/O / Comparator_A input
P2.0/TA0.2	45	I/O	General-purpose digital I/O / Timer0_A capture: CCI2A input, compare: Out2 output
P2.1/TA1.1	44	I/O	General-purpose digital I/O / Timer1_A capture: CCI1A input, compare: Out1 output
P2.2/TA1.2/S23	36	I/O	General-purpose digital I/O / Timer1_A capture: CCI2A input, compare: Out2 output/LCD segment output 23 (see Note 1)
P2.3/TA1.3/S22	34	I/O	General-purpose digital I/O / Timer1_A capture: CCI3A input, compare: Out3 output/LCD segment output 22 (see Note 1)
P2.4/TA1.4/S21	33	I/O	General-purpose digital I/O / Timer1_A capture: CCI4A input, compare: Out4 output/LCD segment output 21 (see Note 1)
P2.5/TA1CLK/S20	32	I/O	General-purpose digital I/O / input of Timer1_A clock/LCD segment output 20 (see Note 1)
P2.6/CAOUT/S19	31	I/O	General-purpose digital I/O / Comparator_A output/LCD segment output 19 (see Note 1)
P2.7/S18	30	I/O	General-purpose digital I/O / LCD segment output 18 (see Note 1)
P3.0/S17	29	I/O	General-purpose digital I/O / LCD segment output 17 (see Note 1)
P3.1/S16	28	I/O	General-purpose digital I/O / LCD segment output 16 (see Note 1)
P3.2/S15	27	I/O	General-purpose digital I/O / LCD segment output 15 (see Note 1)
P3.3/S14	26	I/O	General-purpose digital I/O / LCD segment output 14 (see Note 1)
P3.4/S13	25	I/O	General-purpose digital I/O / LCD segment output 13 (see Note 1)
P3.5/S12	24	I/O	General-purpose digital I/O / LCD segment output 12 (see Note 1)
P3.6/S11	23	I/O	General-purpose digital I/O / LCD segment output 11 (see Note 1)
P3.7/S10	22	I/O	General-purpose digital I/O / LCD segment output 10 (see Note 1)

NOTE 3: LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.

Terminal Functions – MSP430x415, MSP430x417 (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
P4.0/S9	21	I/O	General-purpose digital I/O / LCD segment output 9 (see Note 1)
P4.1/S8	20	I/O	General-purpose digital I/O / LCD segment output 8 (see Note 1)
P4.2/S7	19	I/O	General-purpose digital I/O / LCD segment output 7 (see Note 1)
P4.3/S6	18	I/O	General-purpose digital I/O / LCD segment output 6 (see Note 1)
P4.4/S5	17	I/O	General-purpose digital I/O / LCD segment output 5 (see Note 1)
P4.5/S4	16	I/O	General-purpose digital I/O / LCD segment output 4 (see Note 1)
P4.6/S3	15	I/O	General-purpose digital I/O / LCD segment output 3 (see Note 1)
P4.7/S2	14	I/O	General-purpose digital I/O / LCD segment output 2 (see Note 1)
P5.0/S1	13	I/O	General-purpose digital I/O / LCD segment output 1 (see Note 1)
P5.1/S0	12	I/O	General-purpose digital I/O / LCD segment output 0 (see Note 1)
COM0	36	O	Common output. COM0–3 are used for LCD backplanes.
P5.2/COM1	37	I/O	General-purpose digital I/O / common output. COM0–3 are used for LCD backplanes.
P5.3/COM2	38	I/O	General-purpose digital I/O / common output. COM0–3 are used for LCD backplanes.
P5.4/COM3	39	I/O	General-purpose digital I/O / common output. COM0–3 are used for LCD backplanes.
R03	40	I	Input port of fourth positive (lowest) analog LCD level (V5)
P5.5/R13	41	I/O	General-purpose digital I/O / input port of third most positive analog LCD level (V4 or V3)
P5.6/R23	42	I/O	General-purpose digital I/O / input port of second most positive analog LCD level (V2)
P5.7/R33	43	I/O	General-purpose digital I/O / output port of most positive analog LCD level (V1)
P6.0	59	I/O	General-purpose digital I/O
P6.1	60	I/O	General-purpose digital I/O
P6.2	61	I/O	General-purpose digital I/O
P6.3	2	I/O	General-purpose digital I/O
P6.4	3	I/O	General-purpose digital I/O
P6.5	4	I/O	General-purpose digital I/O
P6.6	5	I/O	General-purpose digital I/O
P6.7/SVSIN	6	I/O	General-purpose digital I/O / SVS, analog input
RST/NMI	58	I	Reset input / Nonmaskable interrupt input port
TCK	57	I	Test clock. TCK is the clock input port for device programming and test.
TDI/TCLK	55	I	Test data input / Test clock input. The device protection fuse is connected to TDI.
TDO/TDI	54	I/O	Test data output port. TDO/TDI data output or programming data input terminal.
TMS	56	I	Test mode select. TMS is used as an input port for device programming and test.
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output terminal of crystal oscillator XT1
QFN Pad	NA	NA	QFN package pad connection to V_{SS} recommended

NOTE 4: LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.

short-form description

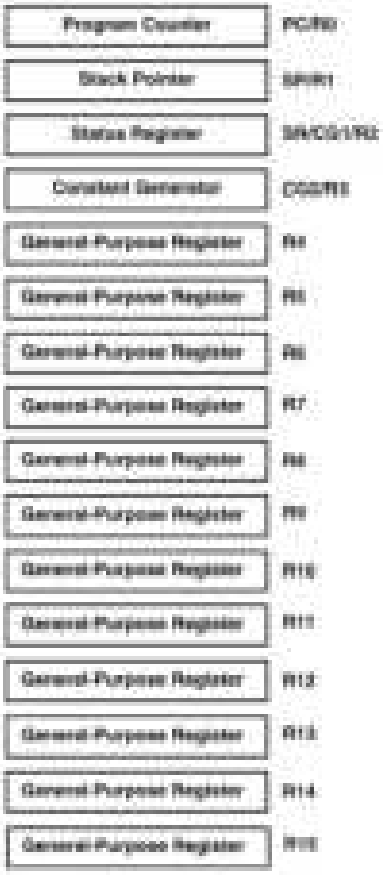
CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 ——> R5
Single operands, destination only	e.g. CALL R8	PC ——>(TOS), R8——> PC
Relative jump, unconditional	e.g. JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	•	•	MOV Rs,Rd	MOV R10,R11	R10 ——> R11
Indexed	•	•	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)——> M(6+R6)
Symbolic (PC relative)	•	•	MOV EDE,TONI		M(EDE) ——> M(TONI)
Absolute	•	•	MOV &MEM,&TCDAT		M(MEM) ——> M(TCDAT)
Indirect	•		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) ——> M(Tab+R6)
Indirect autoincrement	•		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) ——> R11 R10 + 2——> R10
Immediate	•		MOV #X,TONI	MOV #45,TONI	#45 ——> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active.
- Low-power mode 0 (LPM0)
  - CPU is disabled.
  - ACLK and SMCLK remain active, MCLK is available to modules.
  - FLL+ loop control remains active.
- Low-power mode 1 (LPM1)
  - CPU is disabled.
  - ACLK and SMCLK remain active, MCLK is available to modules.
  - FLL+ loop control is disabled.
- Low-power mode 2 (LPM2)
  - CPU is disabled.
  - MCLK, FLL+ loop control, and DCOCLK are disabled.
  - DCO's dc generator remains enabled.
  - ACLK remains active.
- Low-power mode 3 (LPM3)
  - CPU is disabled.
  - MCLK, FLL+ loop control, and DCOCLK are disabled.
  - DCO's dc generator is disabled.
  - ACLK remains active.
- Low-power mode 4 (LPM4)
  - CPU is disabled.
  - ACLK is disabled.
  - MCLK, FLL+ loop control, and DCOCLK are disabled.
  - DCO's dc generator is disabled.
  - Crystal oscillator is stopped.

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh to 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

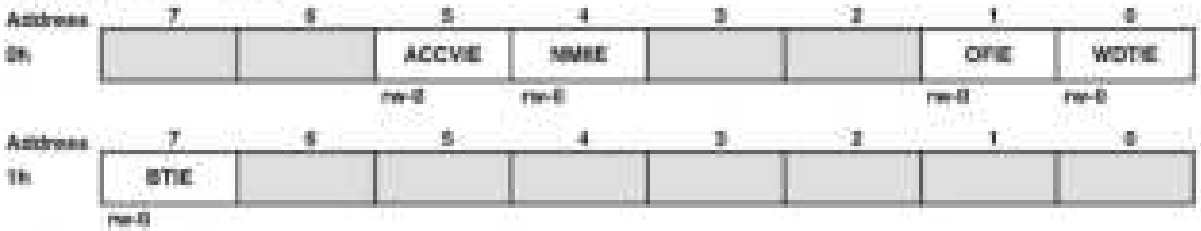
INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog Flash memory	WDTIFG KEYV (see Note 1)	Reset	0FFFEh	15, highest
NMI Oscillator fault Flash memory access violation	NMIIFG (see Notes 1 and 2) OFIFG (see Notes 1 and 3) ACCVIFG (see Notes 1 and 3)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	14
Timer1_A5 (see Note 4)	TA1CCR0 CCIFG (see Note 2)	Maskable	0FFFAh	13
Timer1_A5 (see Note 4)	TA1CCR1 to TA1CCR4 CCIFGs and TA1CTL TAIFG (see Notes 1 and 2)	Maskable	0FFF8h	12
Comparator_A	CMPAIFG	Maskable	0FFF6h	11
Watchdog timer	WDTIFG	Maskable	0FFF4h	10
			0FFF2h	9
			0FFF0h	8
			0FFEEh	7
Timer_A3/Timer0_A3	TACCR0/TA0CCR0 CCIFG (see Note 2)	Maskable	0FFECh	6
Timer_A3/Timer0_A3	TACCR1/TA0CCR1, TA0CCR2/TA0CCR2 CCIFGs and TACLT/TA0CTL TAIFG (see Notes 1 and 2)	Maskable	0FFEAh	5
I/O port P1 (eight flags)	P1IFG.0 to P1IFG.7 (see Notes 1 and 2)	Maskable	0FFE8h	4
			0FFE6h	3
			0FFE4h	2
I/O port P2 (eight flags)	P2IFG.0 to P2IFG.7 (see Notes 1 and 2)	Maskable	0FFE2h	1
Basic Timer1	BTIFG	Maskable	0FFE0h	0, lowest

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module.
3. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt-enable cannot.
4. Implemented in MSP430x415 and MSP430x417 devices only

special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1 and 2



WDTIE: Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.

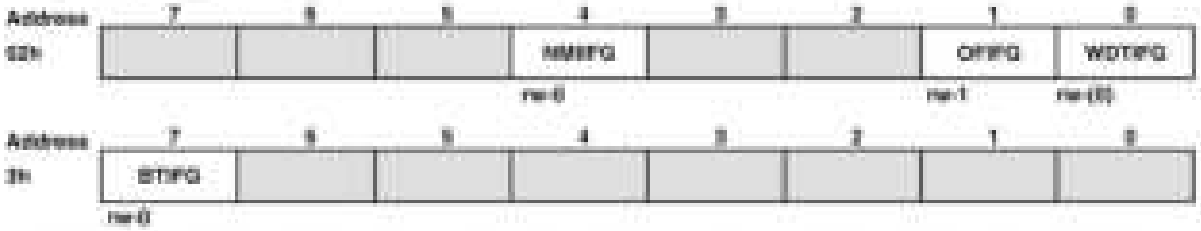
OFIE: Oscillator fault interrupt enable

NMIIE: Nonmaskable interrupt enable

ACCVIE: Flash access violation interrupt enable

BTIE: Basic Timer1 interrupt enable

interrupt flag register 1 and 2



WDTIFG: Set on watchdog-timer overflow (in watchdog mode) or security key violation. Reset with V_{CC} power-up, or a reset condition at the RST/NMI pin in reset mode.

OFIFG: Flag set on oscillator fault

NMIIFG: Set via RST/NMI pin

BTIFG: Basic Timer1 interrupt flag

module enable registers 1 and 2

Legend: rw–0,1: Bit Can Be Read and Written. It Is Reset or Set by PUC.
rw–(0,1): Bit Can Be Read and Written. It Is Reset or Set by POR.
SFR Bit Not Present in Device.

memory organization

		MSP430F412	MSP430F413	MSP430F415	MSP430F417
Memory	Size	4KB	8KB	16KB	32KB
Interrupt vector	Flash	0FFFFh to 0FFE0h	0FFFFh to 0FFE0h	0FFFFh to 0FFE0h	0FFFFh to 0FFE0h
Code memory	Flash	0FFFFh to 0F000h	0FFFFh to 0E000h	0FFFFh to 0C000h	0FFFFh to 08000h
Information memory	Size	256 Byte	256 Byte	256 Byte	256 Byte
	Flash	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h
Boot memory	Size	1KB	1KB	1KB	1KB
	ROM	0FFFh to 0C00h	0FFFh to 0C00h	0FFFh to 0C00h	0FFFh to 0C00h
RAM	Size	256 Byte	256 Byte	512 Byte	1 KB
		02FFh to 0200h	02FFh to 0200h	03FFh to 0200h	05FFh to 0200h
Peripherals	16-bit	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h
	8-bit	0FFh to 010h	0FFh to 010h	0FFh to 010h	0FFh to 010h
	8-bit SFR	0Fh to 00h	0Fh to 00h	0Fh to 00h	0Fh to 00h

		MSP430C412	MSP430C413
Memory	Size	4KB	8KB
Interrupt vector	ROM	0FFFFh to 0FFE0h	0FFFFh to 0FFE0h
Code memory	ROM	0FFFFh to 0F000h	0FFFFh to 0E000h
Information memory	Size	NA	NA
Boot memory	Size	NA	NA
RAM	Size	256 Byte	256 Byte
		02FFh to 0200h	02FFh to 0200h
Peripherals	16-bit	01FFh to 0100h	01FFh to 0100h
	8-bit	0FFh to 010h	0FFh to 010h
	8-bit SFR	0Fh to 00h	0Fh to 00h

bootstrap loader (BSL)

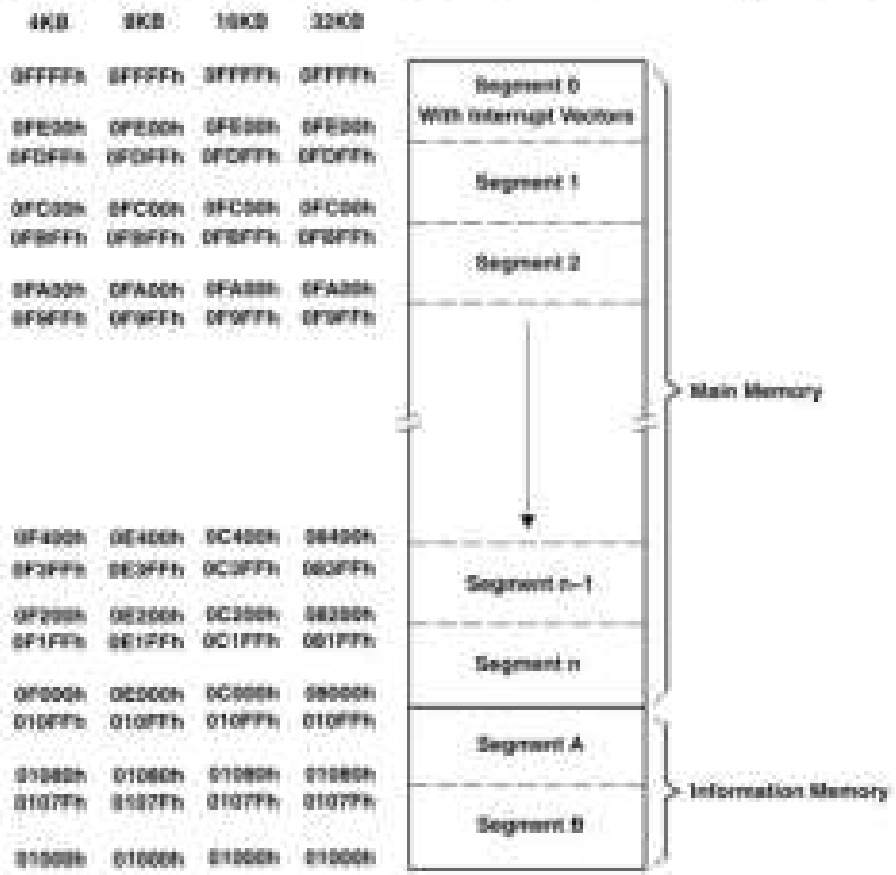
The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the application report *Features of the MSP430 Bootstrap Loader*, literature number SLAA089.

BSL FUNCTION	PW, RTD, RGC PACKAGE PINS
Data Transmit	53 - P1.0
Data Receive	52 - P1.1

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0 to n. Segments A and B are also called *information memory*.
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265