Table of Contents

Chapter 1 Summary

1.1 General Description

The 65W 70CC Dual Type C Ports PD3.0 PPS Evaluation Board (EVB4) is composed of four main controllers, DIODES™ AP33510, DIODES™ APR349, DIODES™ AP43771V and Canyon Semiconductor's CY6572. The AP33510, a highly integrated Quasi-Resonant (QR) controller with direct Enhancement Gallium Nitride (E-GaN) driver integration, is optimally designed to meet ultra-low standby power and high power density (HPD) charger applications. The APR349, a secondary side Synchronous Rectification (SR) Controller, is adopted for efficiency optimization. The AP43771V, a PD3.0 PPS protocol controller, automatically manages the PD3.0 PPS attachment process for the attached Type C-equipped Device Under Charged (DUC) regulates the feedback information of the charger to fulfill voltage and current requirements from DUC. CY6572 is a synchronous buck controller. Communication through I2C between two AP43771V, two Ports can realize smart power sharing once two ports both insert. By adopting popular E-GaN FETs, the 65W 70CC EVB4 exemplifies high power density charger design with optimized system BOM to meet market trend.

1.2 Key Features

1.2.1 System Key Features

- Quasi-Resonant operation for Critical E-GaN switch Operation and Efficiency Improvement Approaches
- Cost-Effective Implementation for HPD Chargers
- High-Voltage Startup low standby power (<20mW)
- Meets DOE VI and COC Tier 2 Efficiency Requirements
- USB Type-C Port - Support the Maximum Output of 65W PD3.0 PPS (3.3V to 21V@20mV/step, 50mA/step)
- SSR Topology Implementation with an Opto-coupler for Accurate Step Voltage / Current Control
- Low overall system BOM cost

1.2.2 AP33510 Key Features

- QR Flyback Topology with Valley-on and Valley lock
- High-Voltage Startup
- Embedded VCC LDO for VCCIN pin to Guarantee Wide Range Output Voltage
- Integration of Accurate E-GaN direct-driver
- Low Constant Output Current for Output Short
- Non-Audible-Noise QR Control
- Soft Start During Startup Process
- Frequency Fold Back for High Average Efficiency
- Secondary Winding Short Protection with FOCP
- Frequency Dithering for Reducing EMI
- Integration of X-CAP Discharge Function
- Useful Pin fault protection:
  SENSE Pin Floating Protection/
  FB/Opto-Coupler Open/Short Protection
- Comprehensive System Protection Feature: VOVP/OLP/BNO/SOVP/SUVP

1.2.3 APR349 Key Features

- SR Works with CCM / DCM / QR operation modes
- Eliminate Resonant Ringing Interference
- Fewest External Components used

1.2.4 AP43771V Key Feature

- Support USB PD Rev 3.0 V1.2
- USB-IF PD3.0/PPS Certified TID 4312
- Qualcomm QC5 Certified: QC20201127203
- MTP for System Configuration
- OTP for Main Firmware
- Operating Voltage Range: 3.3V to 21V
- Built-In Regulator for CV and CC Control
- Programmable OVP/UVP/OCP/OTP
- Support Power Saving Mode
- External N -MOSFET Control for VBUS Power Delivery
- Support e-Marker Cable Detection
- QFN-14 and QFN-24

1.2.5 CY6572 Key Feature

- Wide Input Voltage from 4.5V to 40V
- Adjustable Switching Frequency to get high Efficiency
- High Duty-Cycle Up to 99%
- CC/CV Control
- Auto Recovery after Faults
- System Protection Feature
- Thermal Enhanced TSSOP-14 Package

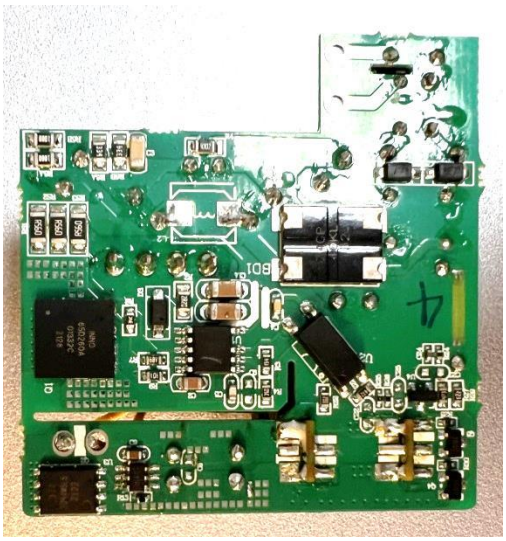
1.3 Applications

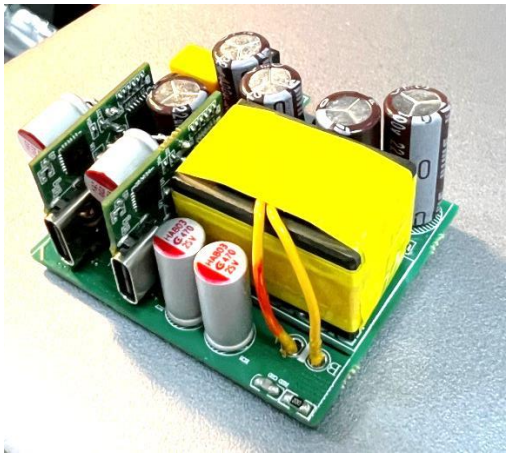
- Quick Charger with full power range of PD3.0 PPS

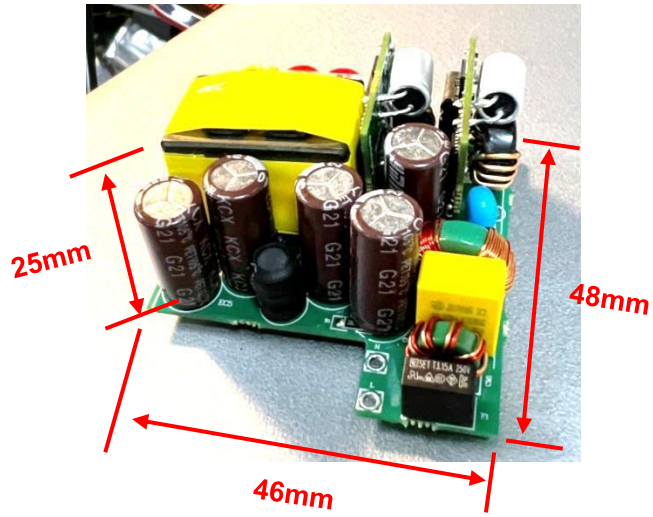
1.4 Main Power Specifications

Parameter	Value
Input Voltage	$90V_{AC}$ to $264V_{AC}$
Input standby power	< 150mW
Master port/Slave port (Vo / Io)	PDO: 5V/3A, 9V/3A, 15V/3A, 20V/3.25A,
	APDO: 3.3 to 16V/4A; 3.3V to 21V/3A
Voltage Step	PPS 20mV step voltage, 3.3V-21V
Efficiency	Comply with CoC version 5 tier-2
Total Output Power	65W
Protections	OCP, OVP, UVP, OLP, OTP, SCP
Dimensions	PCB: 48 * 50 * 21 mm^3, 1.890" * 1.968" * 0.827" $inch^3$ Case: 52 * 54 * 25 mm^3, 70CC, 4.27 CI
Power Density Index	0.93 W/CC; 15.22W/CI

1.5 Evaluation Board Pictures







*** The dimension "25mm" includes the height of bottom components**

Chapter 2 Power Supply Specification

2.1 Specification and Test Results

Parameter	Value	Test Summary
Input Voltage / Frequency	$90V_{AC}$ to $264V_{AC}$ / 50Hz or 60Hz	Test Condition
Input Current	$<2A_{RMS}$	**PASS**
Standby Power	< 150mW, load disconnected	**PASS,** 135mW@$230V_{AC}$/50Hz
C_#1: 20V/3.25A + C_#2: No load Average Efficiency	DoE VI Efficiency >87.4%	**PASS,** 90.92@115VAC/60Hz 90.37@230VAC/50Hz
C_#1: 20V/3.25A + C_#2: No load (10% Load)		**PASS,** 82.99@115VAC/60Hz 79.67@230VAC/50Hz
C_#1:11V/4A + C_#2: 9V/2.2A Average Efficiency	DoE VI Efficiency >87.3%	**PASS,** 89.39@115VAC/60Hz 89.18@230VAC/50Hz
C_#1:11V/4A + C_#2: 9V/2.2A (10% Load)		**PASS,** 83.25@115VAC/60Hz 80.94@230VAC/50Hz
C_#1:15V/3A + C_#2: 9V/2.2A Average Efficiency	DoE VI Efficiency >87.4%	**PASS,** 90.11@115VAC/60Hz 89.77@230VAC/50Hz
C_#1:15V/3A + C_#2: 9V/2.2A Efficiency (10% Load)		**PASS,** 83.14@115VAC/60Hz 81.08@230VAC/50Hz
Output Voltage Regulation Tolerance	+/- 5%	**PASS**
16V PPS	3.3V – 16V +/- 5%, 0~4A +/-150mA	**PASS**
21V PPS	3.3V – 21V +/- 5%, 0~3A +/-150mA	**PASS**
Conducted EMI	>5dB Margin; according to EN55032 Class B	**PASS**

2.2 Compliance

Parameter	Test conditions	Transition time	standard	Test Summary
Output Voltage Transition time	5V to 9V	53ms	<275ms	Pass
	9V to 15V	79ms		Pass
	15V to 20V	65ms		Pass
	20V to 15V	67ms		Pass
	15V to 9V	79ms		Pass
	9V to 5V	60ms		Pass
	20V to 5V	202ms		Pass
				Pass
Output Connector	USB Type-C *2-			
Temperature	90Vac , Full Load			
Dimensions (W /D/ H)	L50mm x 48mm x 21mm (with foldable AC pin)			

Chapter 3 Schematic

3.1 Board Schematic

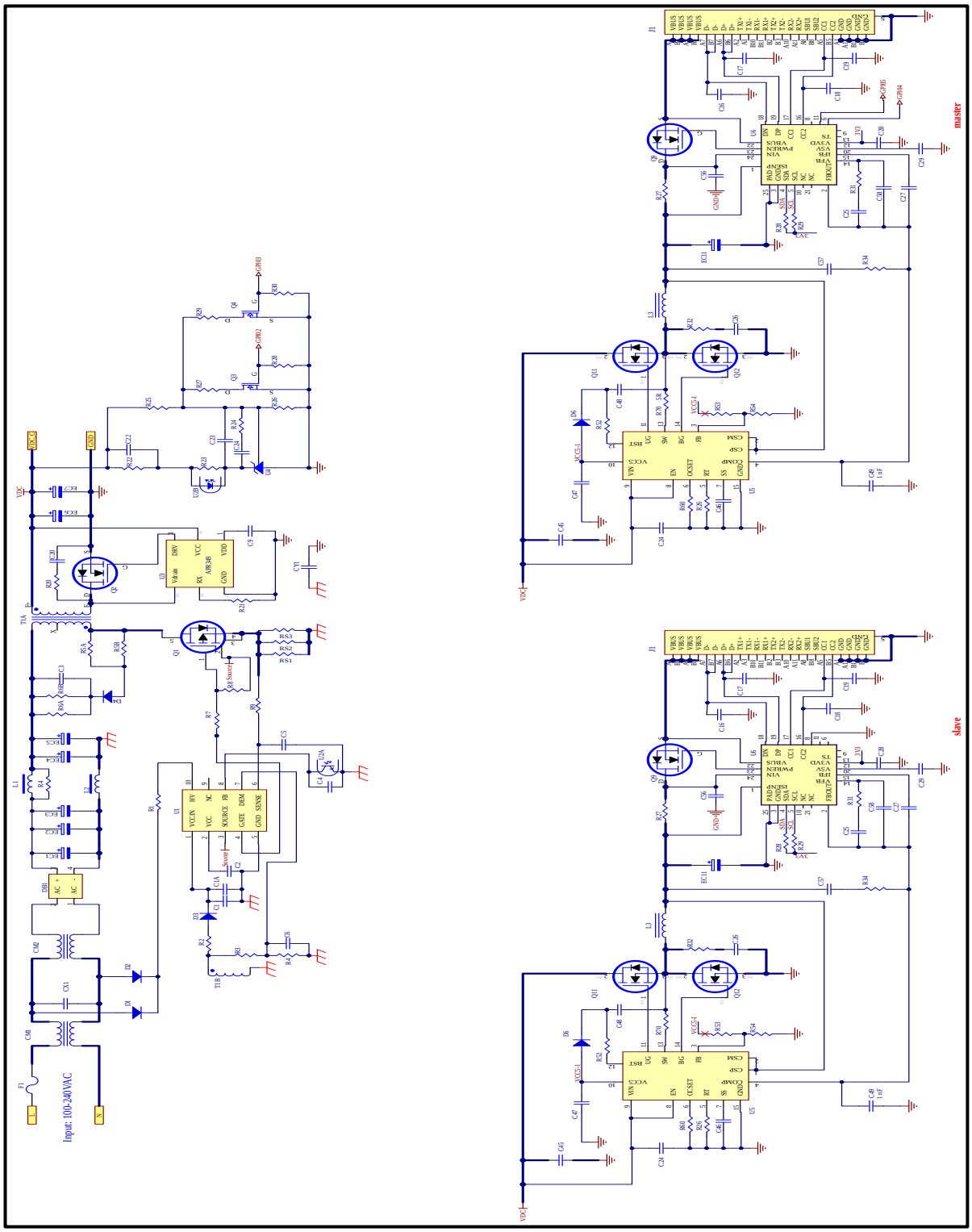


Figure 1: 65W PD3.0 PPS Adapter EVB3 Schematic

3.2 Bill of Material (BOM)

Main board BOM

Designator	Comment	Footprint	Quantity
C1 C1A	2.2μF 100V	1206	2
C2	4.7μF 35V	0805	1
C3	2.2nF/1KV	1206	1
C4	1nF/50V	0603	1
C5	100pF 16V	0603	1
C6	option	0603	1
C20	1nF/100V	0805	1
C9	3.3μF/16V	0603	1
C22, C23	option	0603	2
C24	10nF/50V	0402	1
CM1	8.4.3-22		1
CM2	20mH		1
CX1	0.22μF/275V	X6*12	1
CY1	1nF/400V Y 电容	CY10-2	1
D1, D2, D4	FR107	SOD-123	3
D3	1N4007	SOD-123	1
DB1	Z4DGP406L-HF	Z4D	1
EC1, EC2, EC3,EC4,EC5	22UF/400V	EC10.0	5
EC6, EC7	560UF/25V	EC6.0	2
F1	T3.15A/250V	FUSE4*8	1
L1	22μH		1
L2	5μH		1
Q1	INN650D260A	DFN 8*8	1
Q2	Diodes, DMTH10H4M5	DFN5*6	1
Q3, Q4	2N7002	SOT-23	2
R1	20K	1206	1
R2	2.2R	0805	1
R3	150K 1%	0603R	1
R4	11K 1%	0603R	1
R5A, R5B	100R	0805	2
R6A, R6B	330K	0805	2
R7	5ohm	0603	1
R4	10K	0805	1
R8	22K	0603	2
R9	300	0603	1
R20	20R	0805	1
R21	33K	0402	1
R22	3K	0603	1
R23	4.7K	0603	1
R24	20K	0402	1
R25	91K	0402	1
R26	51K	0402	1

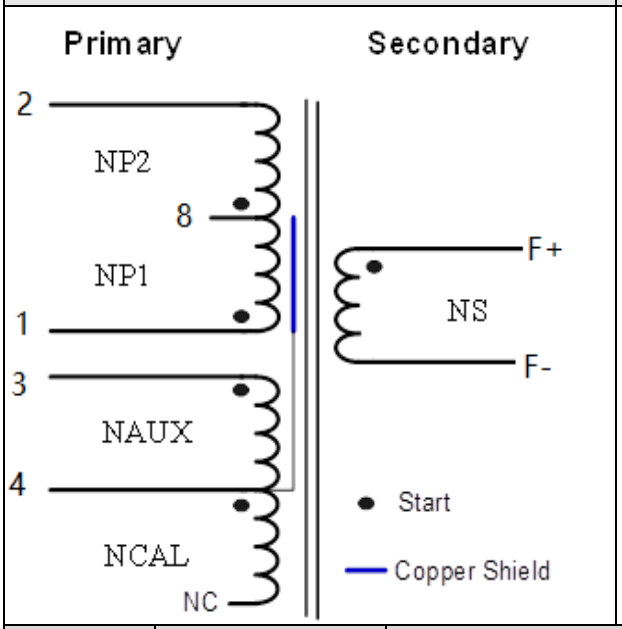
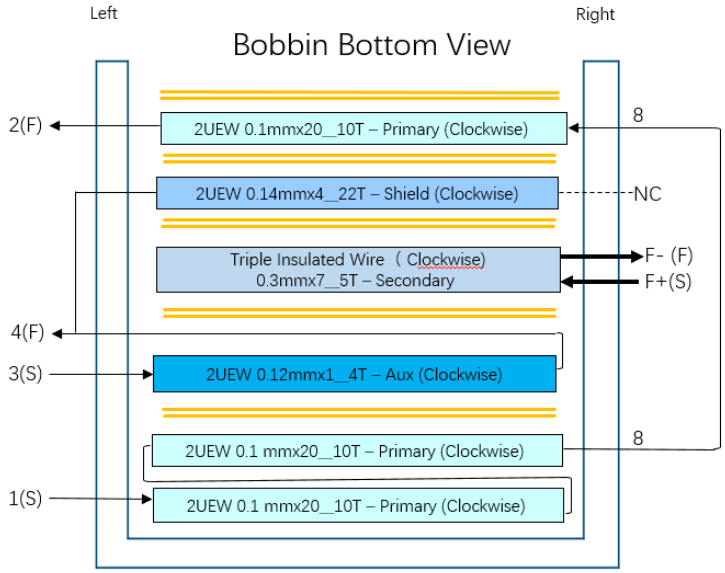
R27	47K	0603	1
R29	22K	0603	1
R28, R30	100K	0402	2
RS1	0.75R	1206	1
RS2, RS3	0.68R	1206	2
T1	ATQ2516	ATQ2716	1
U1	AP33510	SSOP-9	1
U2	OR1009	PC-SMD	1
U3	APR349	SOT-23-6	1
U4	TL431	SOT-23	1

* Note: GaN device spec can find in InnoScience website http://www.innoscience.com.cn/

Master/Slave daughter board BOM

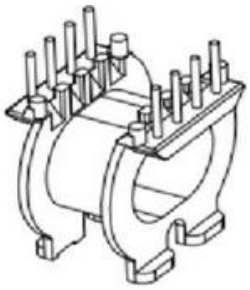
Comment	Designator	Footprint	Quantity
C16, C17, C18, C19	220pF	C-0402	4
C24	100NF/50V	0603C	1
C25	10 nF/50V	0402R	1
C26	1NF	C-0603	1
C27, C28	100NF/25V	0402R	2
C29, C47	4.7UF/10V	0603C	2
C45	4.7μF/35V	0805C	1
C46	100nF	0402R	1
C48	0.1UF	0402R	1
C49	1 nF	0402R	1
C56	0.1μF	C-0402	1
C57	10 nF/50V	C-0402	1
C58	NA	0402R	1
D6	1N4148WS	SOD-323	1
EC11	330UF/25V	EC5.5MM - 1	1
J1	TYPE-C	USBC2	1
L3	40*125 10μH		1
Q9	DMN3008	DFN3*3	1
Q11, Q12	DMT47M2SPSWQ	IC-DFN-5X6-8P-MOS	2
R26	200K	0402R	1
R27	10mR	1206R	1
R28, R29	4.7K	0402R	2
R31	43K	0402R	1
R32	4.7R	R-0805	1
R34	43K	R-0402	1
R52	10R	0402R	1
R53	13K	0402R	1
R54	1.5K	0402R	1
R60	100K	0402R	1
R70	5R	0402R	1
U5	CY6572	TSSOP-15	1
U6	AP43771V-24Q	QFN_24	1

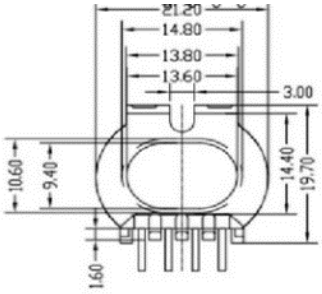
3.3 Transformer Design

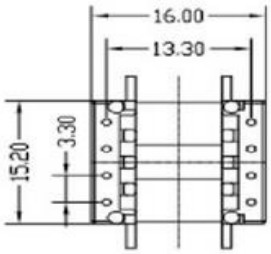
Schematic	Structure
	

Definition	Pin define (Start >> End)	Wire (φ)	No. of Turns	Layers	Layers of Tape
NP1	1 → 8	Φ0.10 2UEW*20P	20	2	2
NAUX	3 → 4	Φ0.12 2UEW*20P	12	1	2
NS	F+ → F-	Φ0.3TIW*7 (Triple Insulated Wire)	5	1	2
Shield	4 → NC	Φ0.14 2UEW*4P	22	1	2
NP2	8 → 2	Φ0.10 2UEW*20P	10	1	2

BOBBIN PIN Define:







Item	Test Condition	Rating
Primary Inductance	Pin 1-2,all other windings open, measured at 20kHz / 1V	280μH+/- 5%
Note	Bobbin/ Core: ATQ2516 （Ae=102mm²）	

3.4 Schematics Description

3.4.1 AC Input Circuit & Differential Filter

The Fuse F1 protects against overcurrent conditions which occur when some main components fails. The NF1 and NF2 are common mode chocks for the common mode noise suppression. The BD is a bridge rectifier which converts alternating current and voltage into direct current and voltage. The CE1~CE3, L1, CE4, CE5 are composed of the Pi filter for filtering the differential switching noise back to AC source.

3.4.2 AP33510 PWM Controller

AP33510, a highly integrated Quasi Resonant Flyback (QR) controller, integrates high-voltage start-up function through HV pin and X-Cap discharging function. It also integrates a VCC LDO circuit, which allows the LDO to regulate the wide range VCCL to an acceptable value. This makes the AP33510 an ideal candidate for wide range output voltage applications such as USB PD3.0 PPS. With embedded E-GaN drive, the AP33510 provides safely and accurately Gate signal to control switch Q1 (GaN FET) operations and achieve high-power density charger applications. At no load or light load, the AP33510 enters the burst mode to minimize standby power consumption.

3.4.3 APR349 Synchronous Rectification (SR) MOSFET Driver

As a high performance solution, the APR349 is a secondary side SR controller to effectively reduce the secondary side rectifier power dissipation which works in both QR/DCM/CCM operation.

3.4.4 AP43771V PD 3.0 Decoder Interface to CY6572 Sync Buck and Power Devices

Few important pins provide critical protocol decoding and regulation functions in AP43771V:

1) **CC1 & CC2 (Pin 11, 10)**: CC1 & CC2 (Configuration Channel 1 & 2) are defined by USB Type-C spec to provide the channel communication link between power source and sink device.
2) **Constant Voltage (CV)**: The CV is implemented by sensing VFB (pin 8) and comparing with internal reference voltage to generate a CV compensation signal on the OCDRV pin (pin 5). The output voltage is controlled by firmware through CC1/CC2 channel communication with the sink device.
3) **Constant Current (CC)**: The CC is implemented by sensing the current sense resistor (RCS, 10mΩ, 1%, Low TCR) and compared with internal programmable reference voltage. The output current is controlled by firmware through CC1/CC2 channel communication with the sink device.
4) **OCDRV (Pin5) to CY6572 COMP (Pin 4)**: It is the key interface link from CC/CV loop on AP43771V to Sync Buck COMP Pin(COMP) to realize Output CC/CV control. OCDRV is connected to CY6572 Pin 4(COMP) for feedback desired information based on all sensed Vbus, Current sense and CC1 & CC2 signals for getting desired Vbus voltage & current.
5) **PWR_EN (Pin2) to N-MOSFET Gate**: The pin is used to turn on/off N-MOSFET (Q9) to enable/disable voltage output to the Vbus.

3.4.5 Interface between Master and Slave Board

Master and Slave boards build interface via I2C communication. AP43771V SDA & SDL (Pin 16, 17) are defined by I2C spec to provide the channel communication link between Master and Slave, such as plug in/out, power sharing info. etc.

Chapter 4 The Evaluation Board (EVB) Connections

4.1 EVB PCB Layout

Main Board

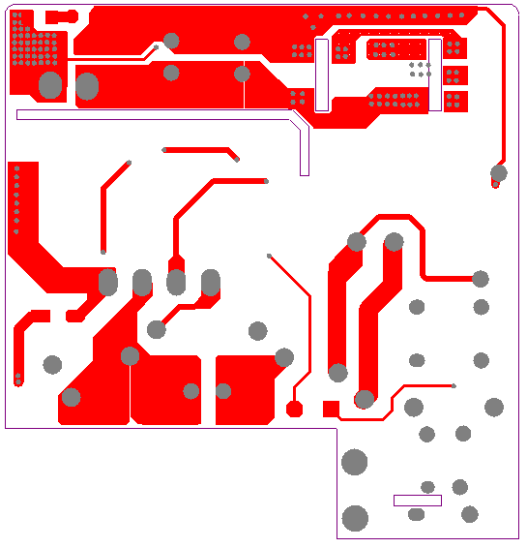


Figure 2: PCB Layout Top View

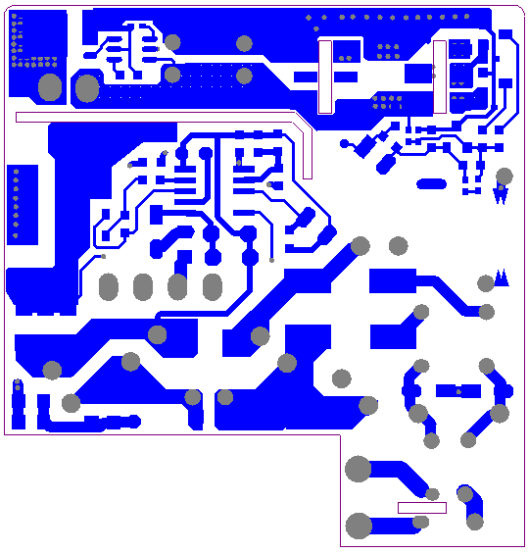


Figure 3: PCB Layout Bottom View

Daughter Board/Master

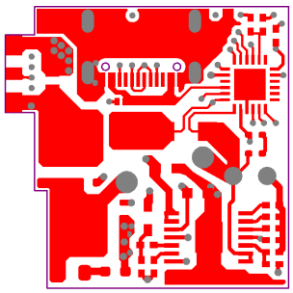


Figure 4: PCB Layout Top View

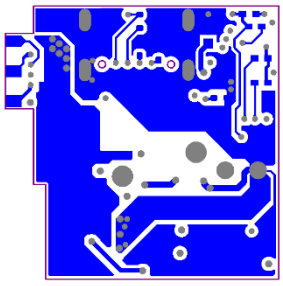


Figure 5: PCB Layout Bottom View

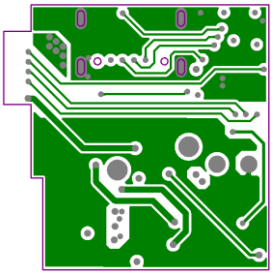


Figure 6: PCB Layout Mid1 View

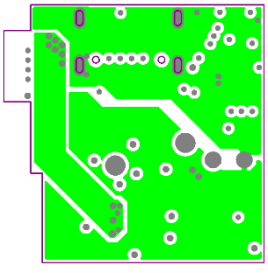


Figure 7: PCB Layout Mid2 View

Daughter Board/Slave:

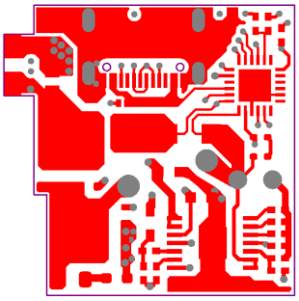


Figure 8: PCB Layout Top View

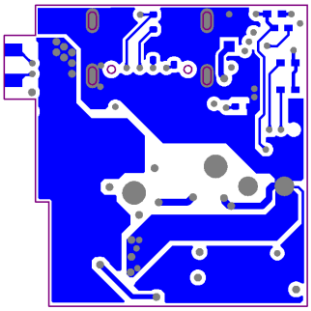


Figure 9: PCB Layout Bottom View

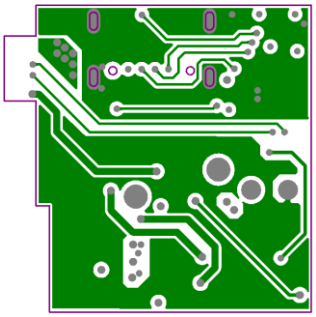


Figure 10: PCB Layout Mid1 View

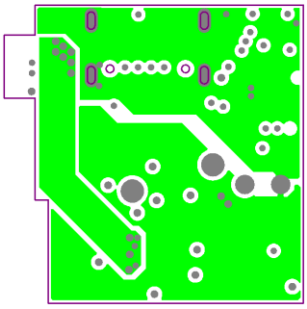


Figure 11: PCB Layout Mid2 View

4.2 Quick Start Guide before Connection

1) Before starting the 65W EVB test, the end user needs to prepare the following tool, software and manuals.

For details, please consult USBCEE sales through below link for further information.

USBCEE PD3.0 Test Kit: USBCEE Power Adapter Tester. https://www.usbcee.com/product-details/4

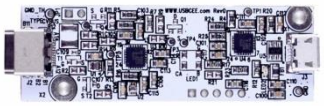
USBCEE PAT Tester	GUI Display	USB-A to Micro-B Cable	Type-C Cable
			

Figure 12: Test Kit / Test Cables

2) Prepare a certified three-foot Type-C cable and a Standard-A to Micro-B Cable.

3) Connect the AC inputs: L & N wires of EVB to AC power supply output “L and N “wires.

4) Ensure that the AC source is switched OFF or disconnected before the connection steps.

5) A type-C cable for the connection between EVB’s and Type-C receptacles of test kit.

6) Output of Type-C port & USB A-port are connected to E-load + & - terminals by cables.

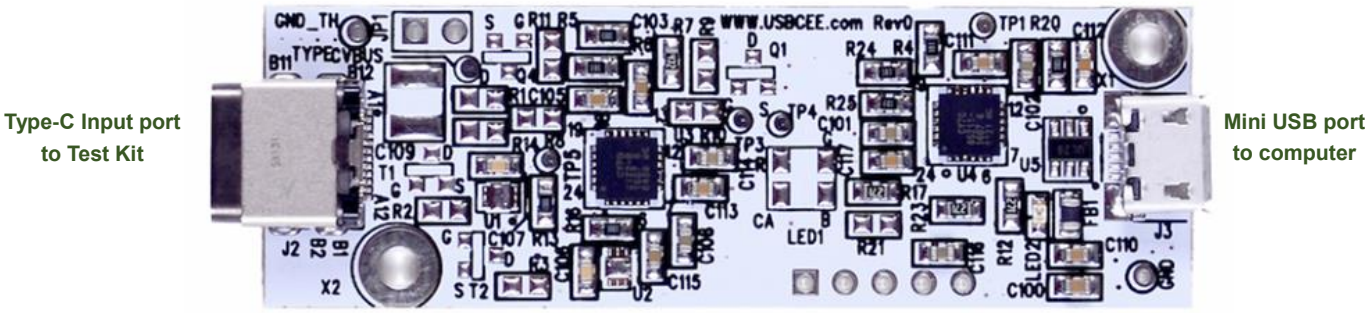


Figure 13: The Test Kit Input & Output and E-load Connections

4.3 Connection with E-Load

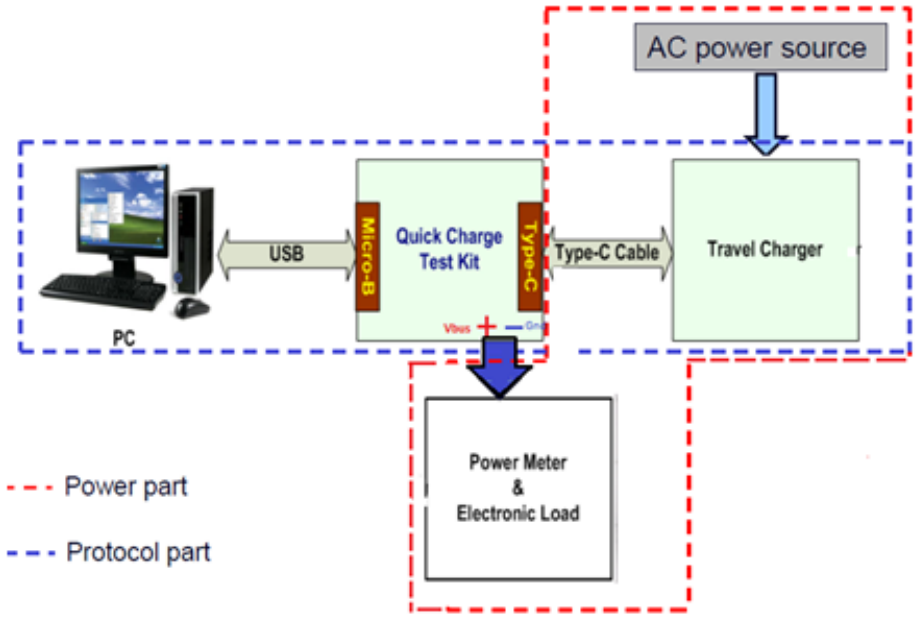


Figure 14: Diagram of Connections in the Sample Board

Chapter 5 Testing the Evaluation Board

5.1 Input & Output Characteristics

5.1.1 Input Standby Power

Vin(Vac)	F(Hz)	Pin(mW)
90	**63**	118
115	**60**	122
230	**50**	135
264	**47**	140

5.1.2 Average Efficiency at Different Loading

Smart Power Sharing Strategy:

	C_#1	C_#2
C_#1 Only	65W	-
C_#2 Only	-	65W
C_#1 and C_#2 both insert	Max 45W	20W
	20W	Max 45W

Single Port Output:
C_#1 or C_#2 : 20V / 3.25A

(Vrms)	Load %	Pin1 (W)	Vout (V)	Iout (A)	Pout (W)	Effi. (%)	Avg. Effi. (%)	DOE 6 required
90 Vac	100%	74.1	20.435	3.2528	66.470968	89.70%	90.18%	87.40%
	75%	54.57	20.376	2.437	49.656312	91.00%		
	50%	36.25	20.32	1.6249	33.017968	91.08%		
	25%	18.52	20.262	0.813	16.473006	88.95%		
	10%	7.9	20.225	0.325	6.573125	83.20%		
115 Vac	100%	72.72	20.439	3.2528	66.483979	91.42%	90.92%	87.40%
	75%	54.15	20.38	2.437	49.66606	91.72%		
	50%	36.08	20.32	1.6249	33.017968	91.51%		
	25%	18.5	20.26	0.813	16.47138	89.03%		
	10%	7.92	20.225	0.325	6.573125	82.99%		
230 Vac	100%	72.12	20.437	3.2528	66.477474	92.18%	90.37%	87.40%
	75%	54.15	20.38	2.437	49.66606	91.72%		
	50%	36.32	20.315	1.6249	33.009844	90.89%		
	25%	19	20.263	0.813	16.473819	86.70%		
	10%	8.25	20.224	0.325	6.5728	79.67%		
264 Vac	100%	72.36	20.435	3.2528	66.470968	91.86%	89.70%	87.40%
	75%	54.42	20.38	2.437	49.66606	91.26%		
	50%	36.63	20.315	1.6249	33.009844	90.12%		
	25%	19.25	20.262	0.813	16.473006	85.57%		
	10%	8.37	20.225	0.325	6.573125	78.53%		

Dual Port-C Output:
C_#1: 11V /4A + C_#2: 9V/2.2A

Vin	Load %	Pin1	Vout1	Iout1	Pout1	Vout2	Iout2	Pout2	Effi.	Avg. Effi.	DOE 6 required
(Vrms)		(W)	(V)	(A)	(W)	(V)	(A)	(W)	(%)	(%)	
90 Vac	100%	73.73	11.06	4.0005	44.24553	9.121	2.2023	20.08718	87.25%	88.64%	87.30%
	75%	54.01	11.056	3.0022	33.19232	9.087	1.6505	14.99809	89.22%		
	50%	35.78	11.062	2.003	22.15719	9.077	1.1	9.9847	89.83%		
	25%	18.23	11.062	1.0036	11.10182	9.06	0.55	4.983	88.23%		
	10%	7.7	11.066	0.4005	4.431933	9.051	0.22047	1.995474	83.47%		
115 Vac	100%	72.22	11.057	4.0005	44.23353	9.122	2.2023	20.08938	89.07%	89.39%	87.30%
	75%	53.4	11.055	3.0022	33.18932	9.086	1.6505	14.99644	90.24%		
	50%	35.68	11.063	2.003	22.15919	9.077	1.1	9.9847	90.09%		
	25%	18.24	11.063	1.0036	11.10283	9.06	0.55	4.983	88.19%		
	10%	7.72	11.066	0.4005	4.431933	9.048	0.22047	1.994813	83.25%		
230 Vac	100%	71.22	11.056	4.0005	44.22953	9.115	2.2023	20.07396	90.29%	89.18%	87.30%
	75%	53.33	11.058	3.0022	33.19833	9.088	1.6505	14.99974	90.38%		
	50%	35.92	11.062	2.003	22.15719	9.074	1.1	9.9814	89.47%		
	25%	18.58	11.065	1.0036	11.10483	9.062	0.55	4.9841	86.59%		
	10%	7.94	11.066	0.4005	4.431933	9.048	0.22047	1.994813	80.94%		
264 Vac	100%	71.02	11.05	4.0005	44.20553	9.094	2.2023	20.02772	90.44%	88.63%	87.30%
	75%	53.6	11.058	3.0022	33.19833	9.089	1.6505	15.00139	89.92%		
	50%	36.25	11.061	2.003	22.15518	9.073	1.1	9.9803	88.65%		
	25%	18.82	11.065	1.0036	11.10483	9.062	0.55	4.9841	85.49%		
	10%	8.05	11.065	0.4005	4.431533	9.046	0.22047	1.994372	79.82%		

Dual Port-C Output:
C_#1: 15V /3A + C_#2: 9V/2.2A

Vin	Load %	Pin1	Vout1	Iout1	Pout1	Vout2	Iout2	Pout2	Effi.	Avg. Effi.	DOE 6 required
(Vrms)		(W)	(V)	(A)	(W)	(V)	(A)	(W)	(%)	(%)	
90 Vac	100%	74.62	15.233	3.0022	45.73251	9.109	2.2022	20.05984	88.17%	89.32%	87.40%
	75%	54.75	15.201	2.2507	34.21289	9.084	1.6504	14.99223	89.87%		
	50%	36.21	15.178	1.5005	22.77459	9.074	1.1	9.9814	90.46%		
	25%	18.41	15.149	0.7501	11.36326	9.054	0.55	4.9797	88.77%		
	10%	7.81	15.135	0.3	4.5405	9.051	0.22043	1.995112	83.68%		
115 Vac	100%	73.12	15.232	3.0022	45.72951	9.11	2.2022	20.06204	89.98%	90.11%	87.40%
	75%	54.12	15.2	2.2507	34.21064	9.084	1.6504	14.99223	90.91%		
	50%	36.08	15.173	1.5005	22.76709	9.072	1.1	9.9792	90.76%		
	25%	18.41	15.153	0.7501	11.36627	9.055	0.55	4.98025	88.79%		
	10%	7.86	15.136	0.3	4.5408	9.047	0.22043	1.99423	83.14%		
230 Vac	100%	72.3	15.233	3.0022	45.73251	9.109	2.2022	20.05984	91.00%	89.77%	87.40%

	75%	54.03	15.206	2.2507	34.22414	9.085	1.6504	14.99388	91.09%		
	50%	36.39	15.178	1.5005	22.77459	9.071	1.1	9.9781	90.00%		
	25%	18.79	15.15	0.7501	11.36402	9.059	0.55	4.98245	87.00%		
	10%	8.06	15.136	0.3	4.5408	9.047	0.22043	1.99423	81.08%		
264 Vac	100%	72.01	15.232	3.0022	45.72951	9.095	2.2022	20.02901	91.32%	89.26%	87.40%
	75%	54.31	15.201	2.2507	34.21289	9.084	1.6504	14.99223	90.60%		
	50%	36.72	15.173	1.5005	22.76709	9.07	1.1	9.977	89.17%		
	25%	19.02	15.152	0.7501	11.36552	9.06	0.55	4.983	85.95%		
	10%	8.18	15.138	0.3	4.5414	9.047	0.22043	1.99423	79.90%		

5.2 Key Performance Waveforms

5.2.1 65W PD3.0 System Start-up Time

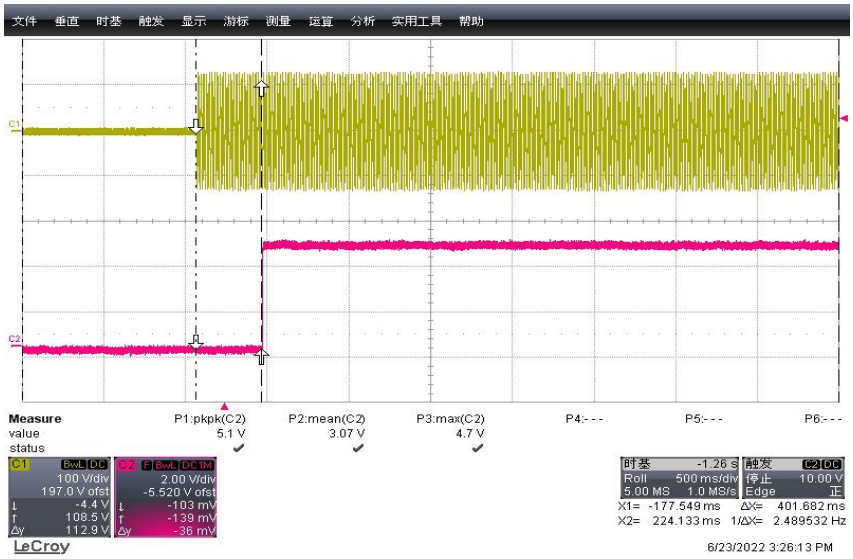


Figure 15: Turn on time is 402ms at Full Load@ 90Vac

5.2.2 Q1 / Q2 MOSFET Voltage Stress at Full Load @264Vac

Primary side MOSFET : Q1 and Secondary side SR MOSFET- Q2

Figure 16: Q1 Vds Voltage stress

Figure 17: Q2 Vds Voltage stress

Component	Vout	Vds	Vds_Max_Spec	Ratio of voltage stress
Q1	20V	592V	650V	91.08%
Q2		90.5V	100V	90.50%

5.2.3 System Output Ripple & Noise with the Cable

Connect 47μF AL Cap and 104MLCC to the cable output unit in parallel

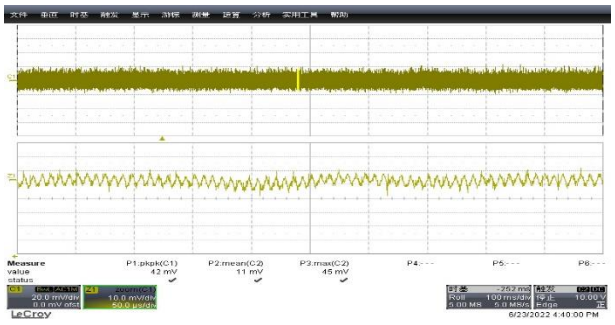


Figure 18: 90Vac/60Hz@ 3.3V/3A ΔV=42mV

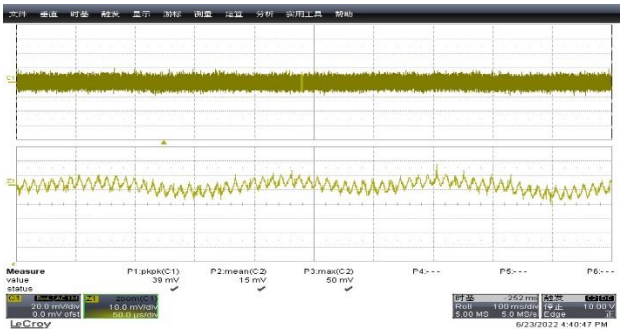


Figure 19: 264Vac/50Hz@3.3V/3A ΔV=39mV

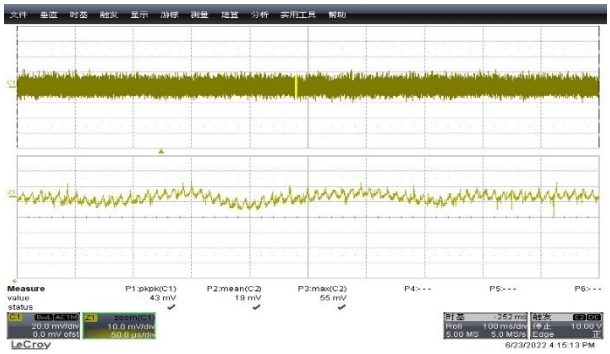


Figure 20: 90Vac/60Hz@5V/3A ΔV=43mV

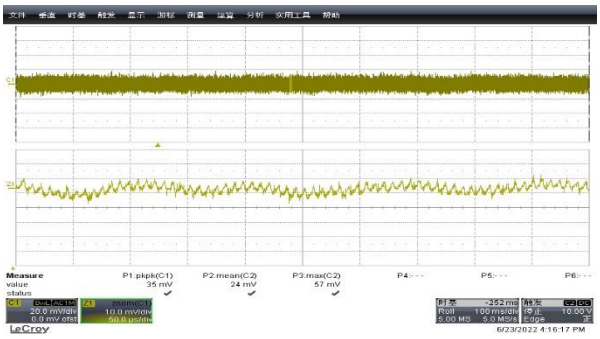


Figure 21: 264Vac/50Hz@5V/3A ΔV=35mV

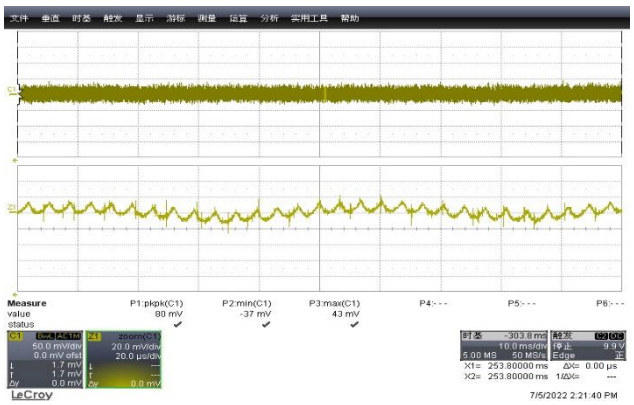


Figure 22: 90Vac/60Hz@9V/3A ΔV=80mV

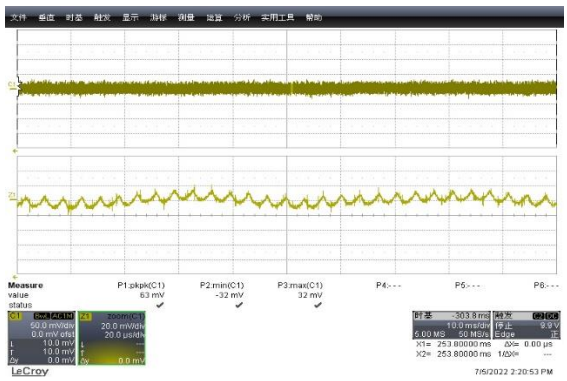


Figure 23: 264Vac/50Hz@9V/3A ΔV=63mV

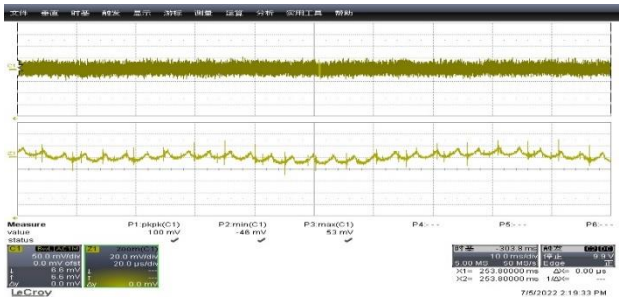


Figure 24: 90Vac/60Hz@15V/3A ΔV=100mV

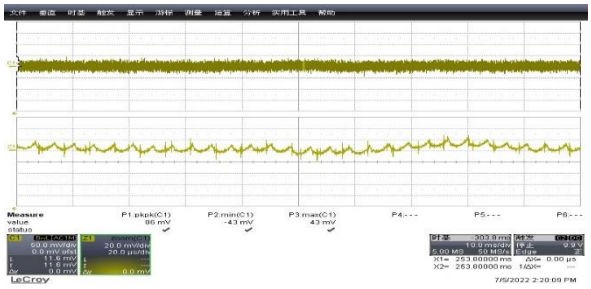


Figure 25: 264Vac/50Hz@15V/3A ΔV=86mV

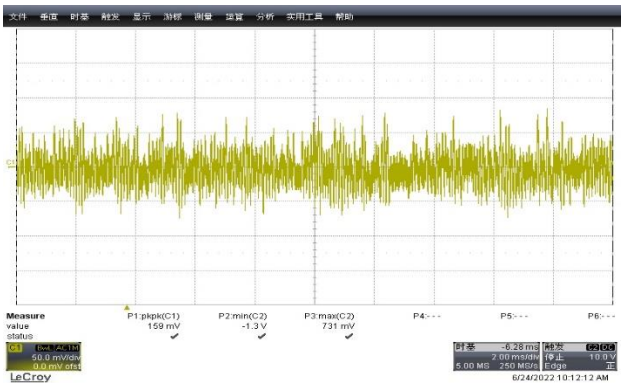


Figure 26: 90Vac/60Hz@20V/3.25A ΔV=159mV

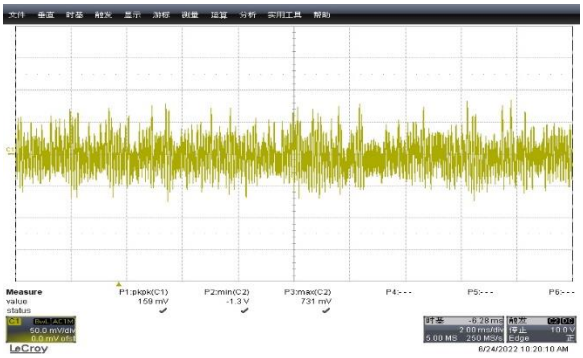


Figure 27: 90Vac/60Hz@20V/3.25A ΔV=159mV

5.2.4 Dynamic load ----0% Load~100% Load, T=20mS, Rate=15mA/μS (PCB End)

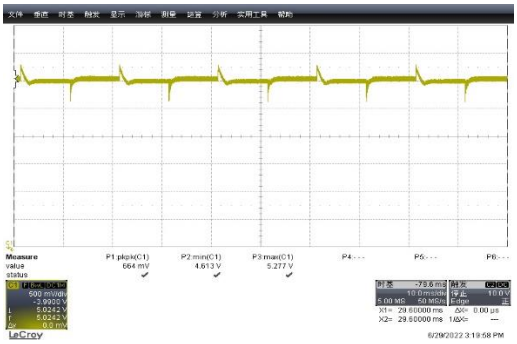


Figure 28: 90Vac/60Hz Port-C@ Vout=5V

Figure 29: 264Vac/50Hz Port-C@ Vout=5V

Figure 30: 90Vac/60Hz Port-C@ Vout=9V

Figure 31: 264Vac/50Hz Port-C@ Vout=9V

	Vo_ Undershoot(V)	Vo_ Overshoot(V)		Vo_Undershoot(V)	Vo_Overshoot(V)
Vin=90Vac@5V	4.61	5.28	Vin=90Vac@9V	8.45	9.29
Vin=264Vac@5V	4.61	5.28	Vin=264Vac@9V	8.46	9.29

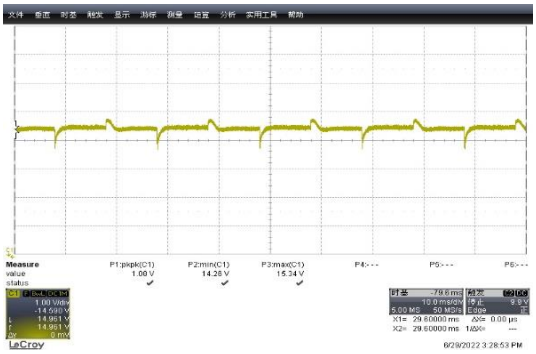


Figure 32: 90Vac/60Hz Port-C@ Vout=15V

Figure 33: 264Vac/50Hz Port-C@ Vout=15V

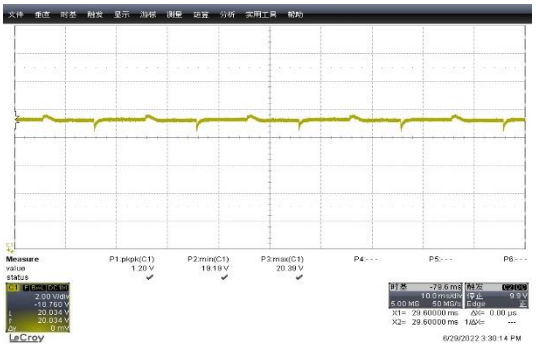


Figure 34: 90Vac/60Hz Port-C@ Vout=20V

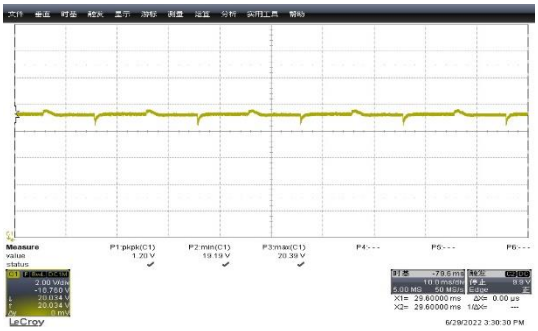


Figure 35: 264Vac/50Hz Port-C@ Vout=20V

	Vo_ Undershoot(V)	Vo_ Overshoot(V)		Vo_Undershoot(V)	Vo_Overshoot(V)
Vin=90Vac@15V	14.26	15.34	Vin=90Vac@20V	19.19	20.39
Vin=264Vac@15V	14.29	15.34	Vin=264Vac@20V	19.19	20.39

5.2.5 Output Voltage Transition Time from Low to High

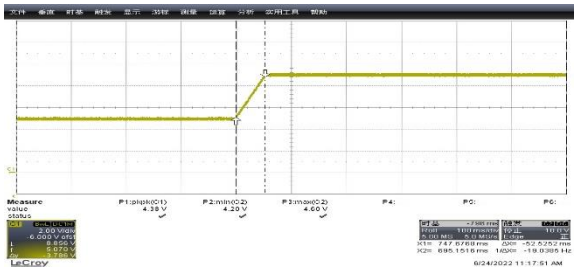


Figure 36: 5V→9V Rise Time = 52.5ms

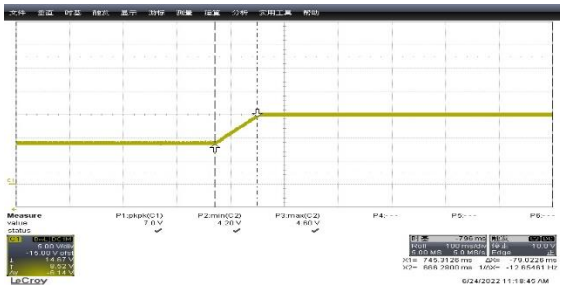


Figure 37: 9V→15V Rise Time = 79.0ms

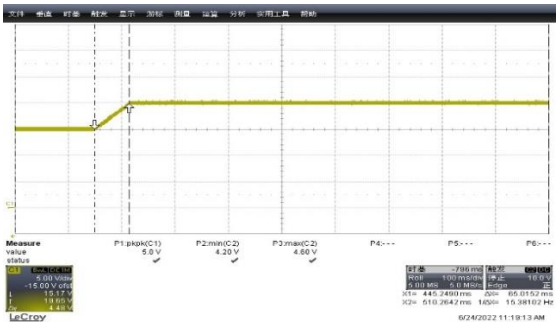


Figure 38: 15V→20V Rise Time = 65.0ms

5.2.6 Output Voltage Transition Time from High to Low

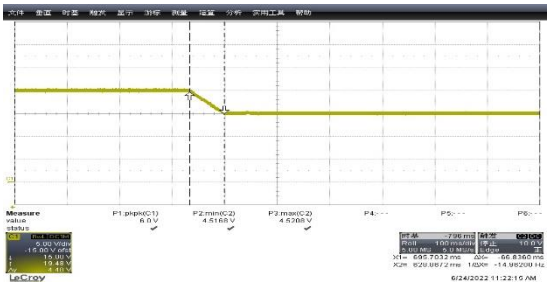


Figure 39: 20V→15V Fall Time = 66.8ms

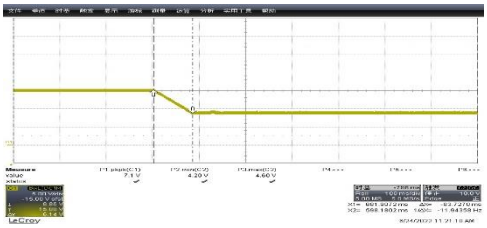


Figure 40: 15V→9V Fall Time = 83.7mS

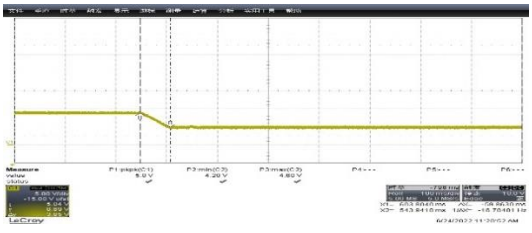


Figure 41: 9V→5V Fall Time = 59.9ms

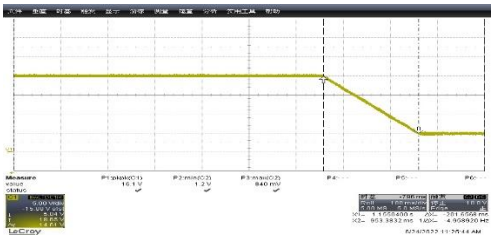


Figure 42: 20V→5V Fall Time = 202ms

5.2.7 Thermal Testing

Output Condition : 20V/3.25A

Main Voltage	Temperature (°C)							
	Ta	U1	Q1	T1-core	T1-wire	Q2	L3	DB1
90Vac/60Hz	25	103.7	123.2	96.6	110.2	98.3	107.3	102.4

Test Condition: Vin=90Vac @ 20V-3.25A Full load Open Frame

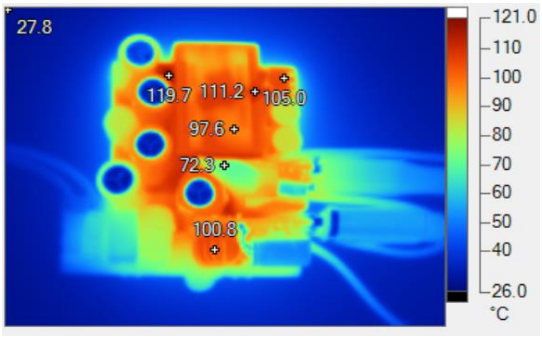


Figure 43: Top Components side

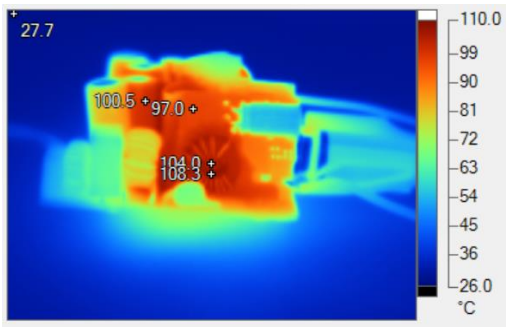


Figure 44: Bottom Suface Mount side

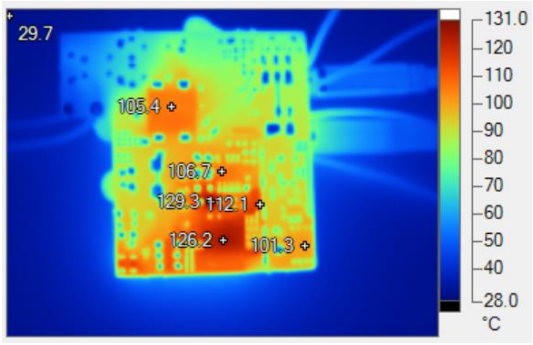


Figure 45: Bottom Suface Mount side

Test Condition: Vin=264Vac @ 20V-3.25A Full load Open Frame

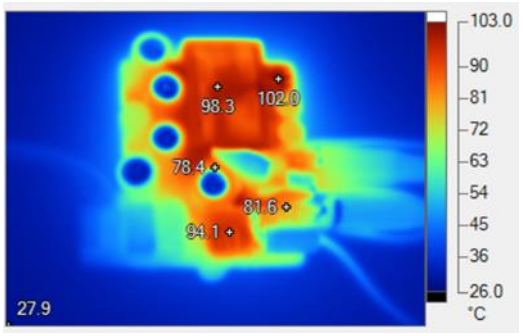


Figure 46: Top Components side

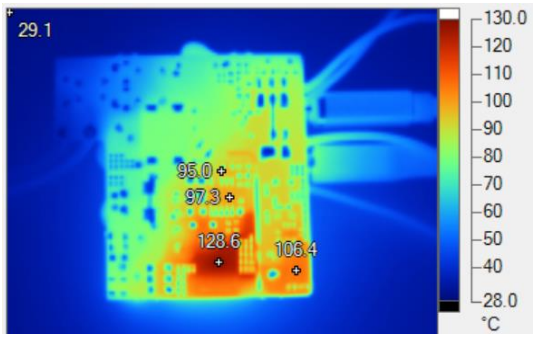


Figure 47: Bottom Suface Mount side

BD1: Bridge Rectifier
Q1 : Primary Side High Voltage GaN FET
D3 : Vcc diode
Q2 : Secondary Side Sync-Rectifier
U1 : AP33510, QR Controller
U2 : APR349, Sync-Rectifier Controller

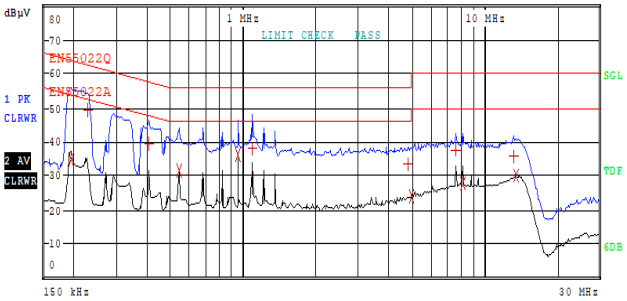
Note: Component temperature can be further optimized with various system design and thermal management approaches by manufacturers.

Main Voltage	Temperature (°C)							
	Ta	U1	Q1	T1-core	T1-wire	Q2	L3	DB1
264Vac/60Hz	25	98.1	122.8	90.9	101	103.4	80.6	76

5.3 EMI (Conduction) Testing

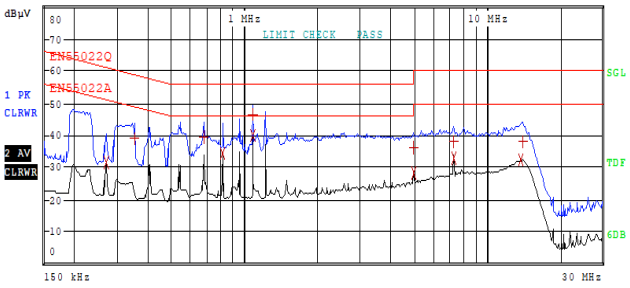
115Vac testing results

Output Condition : 20V/3.25A



	TRACE	FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2	Average	194.288447245 kHz	34.71	-19.13
1	Quasi Peak	227.818484195 kHz	49.23	-13.29
1	Quasi Peak	405.722074413 kHz	39.68	-18.05
2	Average	541.437681113 kHz	31.46	-14.53
2	Average	945.247220176 kHz	36.28	-9.71
1	Quasi Peak	1.08653730473 MHz	38.05	-17.95
1	Quasi Peak	4.78552220172 MHz	33.57	-22.42
2	Average	4.93052830996 MHz	24.27	-21.72
1	Quasi Peak	7.56332093809 MHz	37.62	-22.37
2	Average	8.10890375706 MHz	27.61	-22.38
1	Quasi Peak	13.2041199595 MHz	35.88	-24.11
2	Average	13.4695227707 MHz	30.22	-19.77

Figure 48: 115Vac/60Hz L line

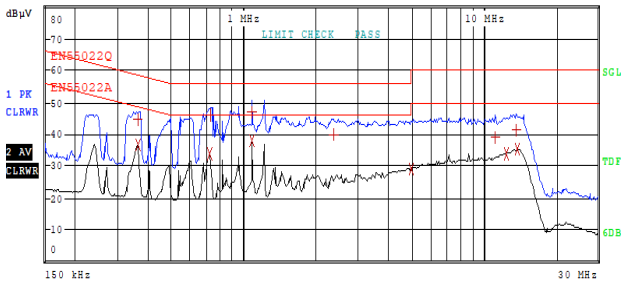


	TRACE	FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2	Average	269.806440381 kHz	31.36	-19.76
1	Quasi Peak	349.468495722 kHz	38.98	-19.99
1	Quasi Peak	673.936068749 kHz	39.70	-16.29
2	Average	806.126927408 kHz	34.57	-11.42
1	Quasi Peak	1.07577950963 MHz	46.68	-9.31
2	Average	1.07577950963 MHz	39.93	-6.06
1	Quasi Peak	4.97983359306 MHz	36.07	-19.93
2	Average	4.97983359306 MHz	28.37	-17.62
1	Quasi Peak	7.26820276052 MHz	38.01	-21.98
2	Average	7.26820276052 MHz	32.84	-17.15
2	Average	13.7402601784 MHz	32.66	-17.33
1	Quasi Peak	14.016439408 MHz	38.26	-21.73

Figure 49: 115Vac/60Hz N line

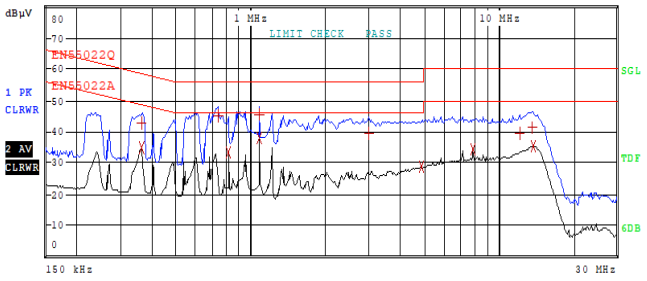
230Vac testing results

Output Condition : 20V/3.25A



	TRACE	FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
1	Quasi Peak	360.057740611 kHz	44.66	-14.05
2	Average	360.057740611 kHz	36.61	-12.11
2	Average	722.550684365 kHz	33.93	-12.06
1	Quasi Peak	729.776191209 kHz	46.30	-9.69
1	Quasi Peak	1.07577950963 MHz	47.20	-8.79
2	Average	1.07577950963 MHz	38.25	-7.74
1	Quasi Peak	2.36108594985 MHz	39.90	-16.10
2	Average	4.97983359306 MHz	29.26	-16.73
1	Quasi Peak	11.0388729048 MHz	39.03	-20.96
2	Average	12.3157210828 MHz	33.96	-16.03
1	Quasi Peak	13.6042179984 MHz	41.36	-18.63
2	Average	13.7402601784 MHz	35.33	-14.66

Figure 50: 230Vac/50Hz L line



	TRACE	FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
1	Quasi Peak	360.057740611 kHz	42.86	-15.86
2	Average	360.057740611 kHz	34.83	-13.89
1	Quasi Peak	737.073953121 kHz	45.25	-10.75
2	Average	806.126927408 kHz	33.30	-12.69
1	Quasi Peak	1.07577950963 MHz	45.45	-10.54
2	Average	1.07577950963 MHz	38.29	-7.70
1	Quasi Peak	2.96826993929 MHz	39.45	-16.54
2	Average	4.83337742374 MHz	28.98	-17.01
2	Average	7.79249712583 MHz	34.27	-15.72
1	Quasi Peak	12.073052723 MHz	39.55	-20.44
1	Quasi Peak	13.6042179984 MHz	41.47	-18.53
2	Average	13.7402601784 MHz	35.52	-14.47

Figure 51: 230Vac/50Hz N line

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