EVAL-10BT1L-MCS IEEE 802.3cg SPoE Shield

FEATURES

- Injects or receives power from the IEEE 802.3cg-compliant SPoE cable
- 10BASE-TX to 10BASE-T1L data conversion

ONLINE RESOURCES

- Schematic, PCB layout, and bill of materials

DESCRIPTION

The EVAL-10BT1L-MCS is a 10BASE-TX, traditional 4-pair Ethernet, to 10BASE-T1L single-pair power over Ethernet (SPoE) media converter shield (MCS) that is compatible with SPoE power sourcing equipment (PSE) and powered device (PD) evaluation motherboards.

The EVAL-10BT1L-MCS-AZ shield power coupling network is suited for Class 10 through Class 14 power levels. The EVAL-10BT1L-MCS-BZ shield power coupling network is suited for the higher power levels of Class 15 while compatible with Class 10 through Class 14. In the context of a PSE, the power coupling network allows for power to be coupled on the single pair Ethernet lines. Regarding the PD, the power coupling network extracts power from the combined power and data line.

The shield includes the ADIN1100, 10BASE-T1L PHY, and the ADIN1200, 10BASE-TX PHY, which provide the Ethernet data media conversion in the system. The on-board LT8301, isolated flyback converter, provides an isolated 3.3V power source to the PHYs.

BOARD PHOTOS

Figure 1. EVAL-10BT1L-MCS-AZ (Class 10 to Class 14)

Figure 2. EVAL-10BT1L-MCS-BZ (Class 15)

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REVISION HISTORY

7/2025—Revision 0: Initial Version

QUICK START PROCEDURE

This quick start procedure shows how to connect the EVAL-10BT1L-MCS shield to either SPoE PSE or PD motherboards. Follow the procedure outlined in the Board Installation on SPoE PSE or PD Motherboard section and refer to Figure 3 and Figure 4 for proper equipment setup.

BOARD INSTALLATION ON SPOE PSE OR PD MOTHERBOARD

1. Select the EVAL-10BT1L-MCS shield version, EVAL-10BT1L-MCS-AZ or EVAL-10BT1L-MCS-BZ, for the intended max class at each port.
2. Verify all power supplies are off prior to installing or removing shield.
3. Align the respective port shield headers over the headers on the motherboard. Push down firmly on the shield until all headers are flush. Verify that no pins are sticking out.

BOARD SETUP

Note that the last two female pins of P1 (the longer connector) are reserved for future use and are floating on select motherboards. Refer to Figure 3 and Figure 4 for proper alignment of the SPoE shield. Powering the SPoE PSE or PD motherboard with a misaligned shield can cause damage to the system.

Figure 3. Alignment of an EVAL-10BT1L-MCS-AZ/EVAL-10BT1L-MCS-BZ shield with SPoE PSE Motherboard

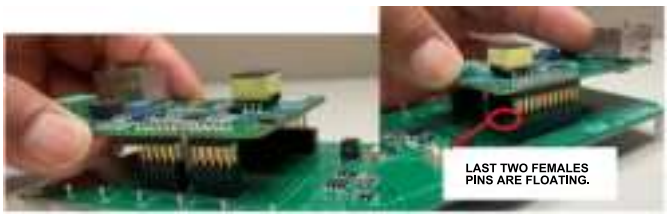

Figure 4. Alignment of an EVAL-10BT1L-MCS-AZ/EVAL-10BT1L-MCS-BZ shield with the SPoE PD Motherboard

EVALUATION BOARD FEATURES

EVAL-10BT1L-MCS-AZ (CLASS 10 TO CLASS 14) POWER COUPLING NETWORK

On the EVAL-10BT1L-MCS-AZ shield, the ADIN1100 (10BASE-T1L PHY) is coupled with SPoE Class 10 to Class 14 power with the power coupling network shown in Figure 5. Class 14 is highest power class supported by this shield. Class 14 is specified for $I_{PI(MAX)}$ = 600mA with $P_{PD(MAX)}$ = 20W.

The isolated coupled inductor (T1) provides the isolation between the PHY and the power interface. Capacitors C25 and C26 function as DC blocking capacitors. Their role is to ensure that only the AC component of the signal is propagated through. To help discharge these capacitors once power is removed, resistors R87 and R88, which have high resistance, are placed in parallel. L3 serves as the common mode choke (CMC), which is used to reduce the high frequency common mode noise from entering and exiting the power interface.

Differential mode inductors (DMI) L2 are responsible for the injection or extraction of power. It ensures that only DC power is injected or extracted, and no data is passed onto the PD or the PSE. The shields have options for using different DMIs as specified on the schematic. These inductors are selected to meet the droop, return loss, and mode conversion specification as defined in the IEEE 802.3cg. By default, the shield uses the Coilcraft MSD1278T-224KLB. This inductor features an inductance of 220µH which produces a compliant transmitter droop. If better transmission droop is required, the MSD1278H-474KED with an inductance value of 470µH can be used. On the other hand, if transmission droop is not a priority, the MSD1048H-104 inductor can be used (100µH).

The DMI on the EVAL-10BT1L-MCS-AZ of the shield is placed on the PHY side of the CMC. Placing the DMI on the PHY side, requires that the CMC be able to sustain Class 10 to Class 14 current. This coupling network is not rated for Class 15.

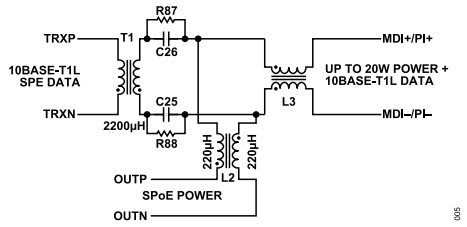

Figure 5. Class 10 to Class 14 Power Coupling Network

EVALUATION BOARD FEATURES

EVAL-10BT1L-MCS-BZ (CLASS 15) POWER COUPLING NETWORK

On the EVAL-10BT1L-MCS-BZ shield, the ADIN1100 (10BASE-T1L PHY) is coupled with SPoE Class 15 power with the power coupling network as shown in Figure 6. Class 15 is specified for $I_{PI(MAX)}$ = 1579mA with $P_{PD(MAX)}$ = 52W.

The isolated coupled inductor (L1) provides the isolation between the PHY and the power interface. In the context of the EVAL-10BT1L-MCS-BZ shield, capacitors C65 and C66 act as the DC blocking capacitors, which ensure that only the AC component of the signal is propagated through. The high resistance discharging resistors for these capacitors are R1 and R10. The CMC (L5) is used to reduce the high frequency common mode noise coming in and out of the power interface.

The DMI (L9) is responsible for the injection or extraction of power. For the EVAL-10BT1L-MCS-BZ shield, the DMI is placed on the line (cable) side of the CMC (L5). As power does not pass through the L5, this CMC can be designed to be significantly smaller than high current CMC options. Although there are high current rated CMC options available, the larger size leads to an increased leakage inductance, which might compromise the integrity of the data lines.

When the power coupling network is placed on the line side, the power coupling network must include an extra CMC (L6) to limit the common mode noise going into the PSE or PD. In this configuration, two capacitors (C60 and C61) with two resistors (R87 and R88) to ground are added to act as an AC short. Additionally, the C64 and R89 form an RC network, which is used to prevent the power coupling inductor from resonating at a frequency within the data band. The RC network then causes the coupling inductor to look like an AC short.

The shield features options for using different DMIs as specified on the schematic. These inductors are selected to meet the droop, return loss, and mode conversion specification as defined in IEEE 802.3cg.

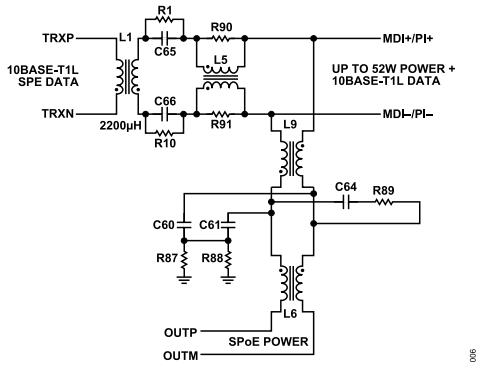

Figure 6. Class 15 Power Coupling Network

EVALUATION BOARD FEATURES

10BASE-T1L TO 10BASE-TX MEDIA CONVERSION

A 10BASE-TX data source is connected to the RJ45 magjack at J4. The data is then transferred to the ADIN1200, a 10BASE-TX Ethernet transceiver PHY. The ADIN1200 PHY interfaces with the ADIN1100, IEEE802.3cg 10BASE-T1L transceiver PHY, through a reduced media independent interface (RMII). An external 50MHz clock at the REF_CLK pin is used for both transmit and receive at the RMII. The ADIN1100 PHY then passes a single pair Ethernet data to get coupled with power before dispatching it to the SPoE connector at J5.

The configuration of the ADIN1100 is hardware based. A pull-up resistor on the SWPD_ENB pin configures the ADIN1100 to not go into software power down after reset. Another pull-up resistor on the MEDIA_CNV pin enables it to operate as a media converter. This allows the ADIN1100 to connect to a 10BASE-T PHY via either the RMII or RGMII interfaces. The ADIN1100 by default, with the MACIF_SEL0 and MACIF_SEL1 pins left floating, are in RMII mode.

The ADIN1200 features some hardware configurations on the shield. It is configured to go into software power-down mode after reset through the mode selection on LINK_ST and LED_0 pins. Pull-up resistors on the MACIF_SEL0 and MACIF_SEL1 pins configure the ADIN1200 for RMII mode. A pull-up resistor sets the MDIX_MODE pin to MODE_4, auto MDIX, prefer MDI.

The software configuration of the ADIN1200 is facilitated through the management data input/output (MDIO) interface. On both the PD and the PSE motherboards, their respective microcontrollers interface at this MDIO. The configuration commands are relayed from the motherboard to the shield headers, and subsequently electrically isolated through the ADUM1251 isolator.

Through the ADIN1200 MDIO, the execution of software commands enables the use of autonegotiation. Autonegotiation facilitates the exchange of information between the ADIN1100 and ADIN1200, enabling link partners to agree on the highest supported mode of operation. During the autonegotiation process, each PHY advertises its capabilities and compares them with those of the link partner.

To advertise 10BASE-T full duplex to the ADIN1100 PHY, 0x41 must be written to the autonegotiation advertisement Register (0x0004). The PHY must then be configured for media converter application which involves using Clause 22 access. This is done by specifying the subsystem 10BASE-T preamble generation Register (0xFF38) to be accessed in the extended register pointer Register (0x0010). Once this is set, all subsequent write and read operations to this register are performed through the extended register data Register (0x0011). To configure for the media converter application, 0x0001 must be written to Register 0xFF38 via Register 0x0011. Lastly Register 0x1300 is written to the MII control Register (0x0000) to set the speed of operation to 10Mbps, enable full duplex mode, restart the autonegotiation process, and enable the autonegotiation process.

After software configurations the ADIN1200 is configured out of the software power-down mode. The ADIN1200 then attempts to bring up links according to its media converter and autonegotiation configurations.

The push button SW1 is used to reset both the ADIN1100 and the ADIN1200.

SHIELD INTERFACE

The shield headers interface and pinouts are shown in Figure 7 and Table 1 through Table 3.

In the case of the PSE, the shield receives power from the PSE motherboard through headers J1 and J2, and deliver SPoE power and data via the SPoE connector. In the case of the PD, the shield receives SPoE power and data at the SPoE connector, and deliver power to the PD motherboard via the headers.

Additional connections to the PSE or PD motherboard at J3 are used for various signals, supply, and ground.

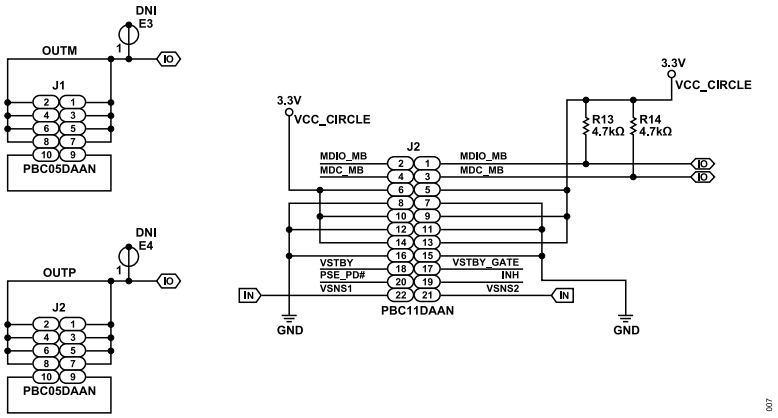

Figure 7. Shield Headers

EVALUATION BOARD FEATURES

Table 1. J1 Pinout

Pins	Signal	Function with PSE Motherboard	Function with PD Motherboard
1, 2, 3, 4, 5, 6, 7, 8	OUTM (input/output, PSE/PD power −)	Connected to the PSE output OUTM	Connected to the PD input OUTM
9, 10	Unused (tied together)	DNC	DNC

Table 2. J2 Pinout

Pins	Signal	Function with PSE Motherboard	Function with PD Motherboard
1, 2, 3, 4, 5, 6, 7, 8	OUTP (input/output, PSE/PD power +)	Connected to the PSE output OUTP	Connected to the PD input OUTP
9, 10	Unused (tied together)	Tied to local ground	Tied to local ground

Table 3. J3 Pinout

Pins[1]	Signal	Function with PSE Motherboard	Function with PD Motherboard
1, 2	MDIO (input/output, PHY management data I/O)	(Pin 2, Pin 1) connected to the motherboard microcontroller for respective port, which is pulled to the local 3.3V via 3.3kΩ. Open drain line.	(Pin 2, Pin 1) pulled up to the local 3.3V via 4.7kΩ. Open drain line.
3, 4	MDC (input, PHY management data clock)	(Pin 4, Pin 3) connected to the microcontroller for respective port, which is pulled to the local 3.3V via 3.3kΩ. Open drain line.	(Pin 4, Pin 3) pulled up to the local 3.3V via 4.7kΩ and tied to the microcontroller. Open drain line.
5, 6, 9, 10, 13, 14	3.3V (input, sourced from motherboard)	(Pin 6, Pin 5, Pin 10, Pin 9, Pin 14, Pin 13) connected to the 3.3V filtered output voltage of the on-board buck regulator.	(Pin 6, Pin 5, Pin 10, Pin 9, Pin 14, Pin 13) connected to local 3.3V output voltage of the on-board buck regulator.
7, 8, 11, 12, 15, 16	GND (non isolated shield ground, common to motherboard)	(Pin 8, Pin 7, Pin 12, Pin 11, Pin 16, Pin 15) Connected to ground.	(Pin 8, Pin 7, Pin 12, Pin 11, Pin 16, Pin 15) connected to ground.
17	VSTBY_GATE (version EVAL-10BT1L-MCS-AZ, reserved test point, not connected) NC (version EVAL-10BT1L-MCS-BZ, not connected)	(Pin 18) connected to ground.	(Pin 18) connected to the LTC9111 STBY pin.
18	VSTBY (test point for PD STBY, not connected)	(Pin 17) connected to local 3.3V.	(Pin 17) connected to the LTC9111 STBY pin.
19	INH (version EVAL-10BT1L-MCS-AZ, not connected) NC (version EVAL-10BT1L-MCS-BZ, not connected)	(Pin 20) not connected.	(Pin 20) not connected.
20	PSE_PD# (test point for PSE or PD motherboard, not connected)	(Pin 19) connected to local 3.3V.	(Pin 19) connected to ground.
21	VSNS2 (PD power interface (PI) Kelvin sense, connected to PI- through 1.1kΩ)	(Pin 22) not connected.	(Pin 22) optionally connected to the LTC9111 VSNS1 pin for closer sensing at the PI.
22	VSNS1 (PD PI Kelvin sense, connected to PI+ through 1.1kΩ)	(Pin 21) not connected.	(Pin 21) optionally connected to the LTC9111 VSNS2 pin for closer sensing at the PI.

[1] Pin 23 and Pin 24 are not on the shield but are reserved for future use on the PSE and PD motherboards.

EVALUATION BOARD FEATURES

CONNECTORS

A 10BASE-TX data source such as an Ethernet switch, or Ethernet end device such as a security camera, is connected with a traditional CAT5 Ethernet cable to the Wurth Elektronic 7498011211 RJ45 magjack at J4. This RJ45 connector is equipped with built in 10/100BASE-T Ethernet transformers and two LED indicators. The green LED signifies the establishment of a valid link, while the yellow is solid when a valid link is established and blinks to indicate link activity.

Connector J5 of the shield is a Phoenix Contact (1803280) 3-position, terminal block header for single pair Ethernet (SPE) cable connection. This compact connector, measuring 12.82mm × 10.65mm × 9.2mm, features a low contact resistance of 1.3mΩ and can carry a nominal current of up to 8A, which is suitable for the SPoE current levels. It is rated for 160V and can withstand surge voltage of 2.5kV. Connector J5 mates with the Phoenix Contact 1803581, 3-position, screw terminal, female which can be installed by screwdriver on a single pair Ethernet cable with optional cable shielding. Table 4 shows the signal pinout of J5.

Note that the polarity of the power interface is inverted between the two shields.

Table 4. J5 SPE Connector Signal Pinout

	J5 Pin		
EVAL-10BT1L-MCS Version	**1**	**2**	**3**
EVAL-10BT1L-MCS-AZ	OUTP	OUTM	Cable shield
EVAL-10BT1L-MCS-BZ	OUTM	OUTP	Cable shield

ISOLATED GROUNDS AND SUPPLIES

The EVAL-10BT1L-MCS shield features three distinct grounds namely the GND, GND_PHY, and GND_EARTH. Each ground is galvanically isolated from the other grounds.

GND is the common ground for SPoE and originates from the motherboard it is installed on, either from the LTC4296-1 or the LTC9111. The non-isolated 3.3V to the input of the LT8301 (isolated flyback), comes from the motherboard and is referenced to GND.

GND_PHY is the isolated ground reference for the PHYs. The isolated 3.3V generated from the LT8301 is referenced to GND_PHY and powers both PHYs.

GND_EARTH is an earth ground plane on the EVAL-10BT1L-MCS-AZ or on the EVAL-10BT1L-MCS-BZ, which can optionally connect via resistor (R49) and/or capacitor (C35) to the SPE cable shield (if the cable has a shield).

The shields feature an optional footprint for a 2010 resistor, R86 on the EVAL-10BT1L-MCS-AZ and R82 on the EVAL-10BT1L-MCS-BZ, which is across the isolation barrier between GND_EARTH and GND_PHY. A shunt resistor can be installed in this location if GND_EARTH and GND_PHY need to be tied together.

ISOLATION COMPONENTS

The isolated coupled inductor from TDK, ICI70CGI-222N, is used to provide the isolation between the PHY and the PI on both shields.

The ADuM1251 is used to isolate the management data input/output (MDIO) and management data clock (MDC) from the shield PHYs to the microcontroller on their respective motherboards.

Additional filter components are placed across the isolation between the GND plane and GND_EARTH for common mode noise filtering.

SURGE COMPONENTS

For the ADIN1100 and ADIN1200, PHY protection at the Ethernet lines and an optional SP3051-04HTG TVS diode array is available at D1 and D5. This part integrates eight diodes and one Zener to protect the PHYs from ESD and high surge events.

Surge protection at the power interface is handled with the D55V0M1B2WSQ-7 bidirectional TVS diode on D6. If more robust surge protection is desired, the SMAJ54CA bidirectional TVS on D7 can be installed. A gas discharge tube (GDT) on T2 provides a breakdown voltage on the line to line as well as line to ground on the SPE lines and GND_EARTH.

TERMINATION COMPONENTS

Depending on customer requirements with isolation, C35 and/or R49 on the EVAL-10BT1L-MCS-AZ shield and C36 and/or R35 on the EVAL-10BT1L-MCS-BZ shield give the option of connecting the shield on the SPE cable to the shield of the GND_EARTH (if the SPE cable features a shield).

OPTIONAL COMPONENTS

LTC9111 PD Input Kelvin Sense

The LTC9111 measures its port voltage by default at the input of SPoE PD motherboards via its R11 and R12 resistors. This measurement is desirable since the voltage is measured after the power coupling network, which can filter out excessive ringing that can be observed directly at the connector during classification.

If voltage at the SPE connector of the shield is desired, R11 and R12 can be removed, and R21 and R22 can be installed on the SPoE PD motherboard. This disconnects the Kelvin sense lines from the PD input and connects the Kelvin sense line to the shield headers. The Kelvin sense lines are then connected to the shield SPE connector through the shield R77 and R78 resistors. Optional capacitors (C55 and C56) are there for filtering.

EVALUATION BOARD FEATURES

Optional Component Figures

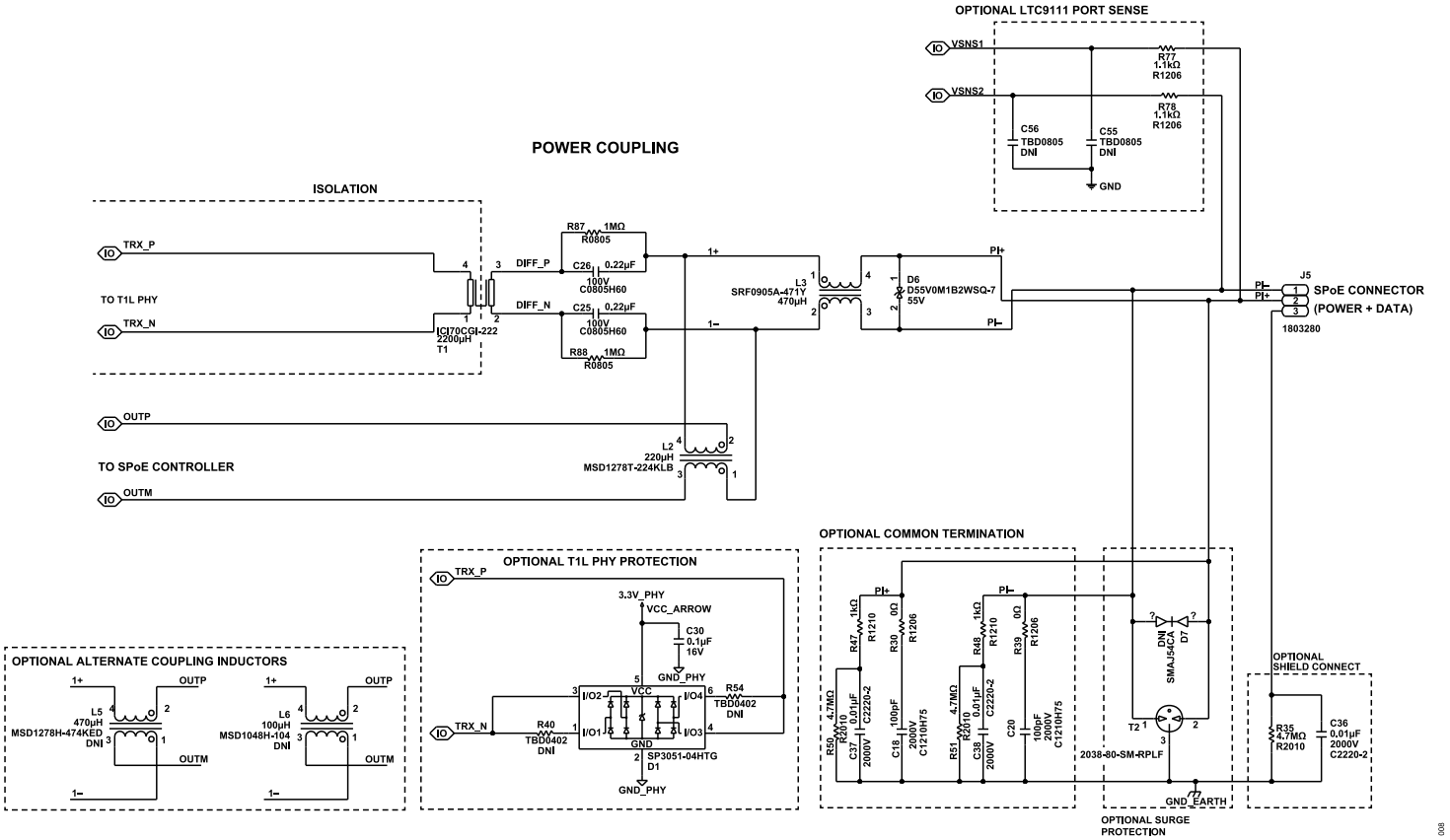

Figure 8. EVAL-10BT1L-MCS-AZ Optional Components

EVALUATION BOARD FEATURES

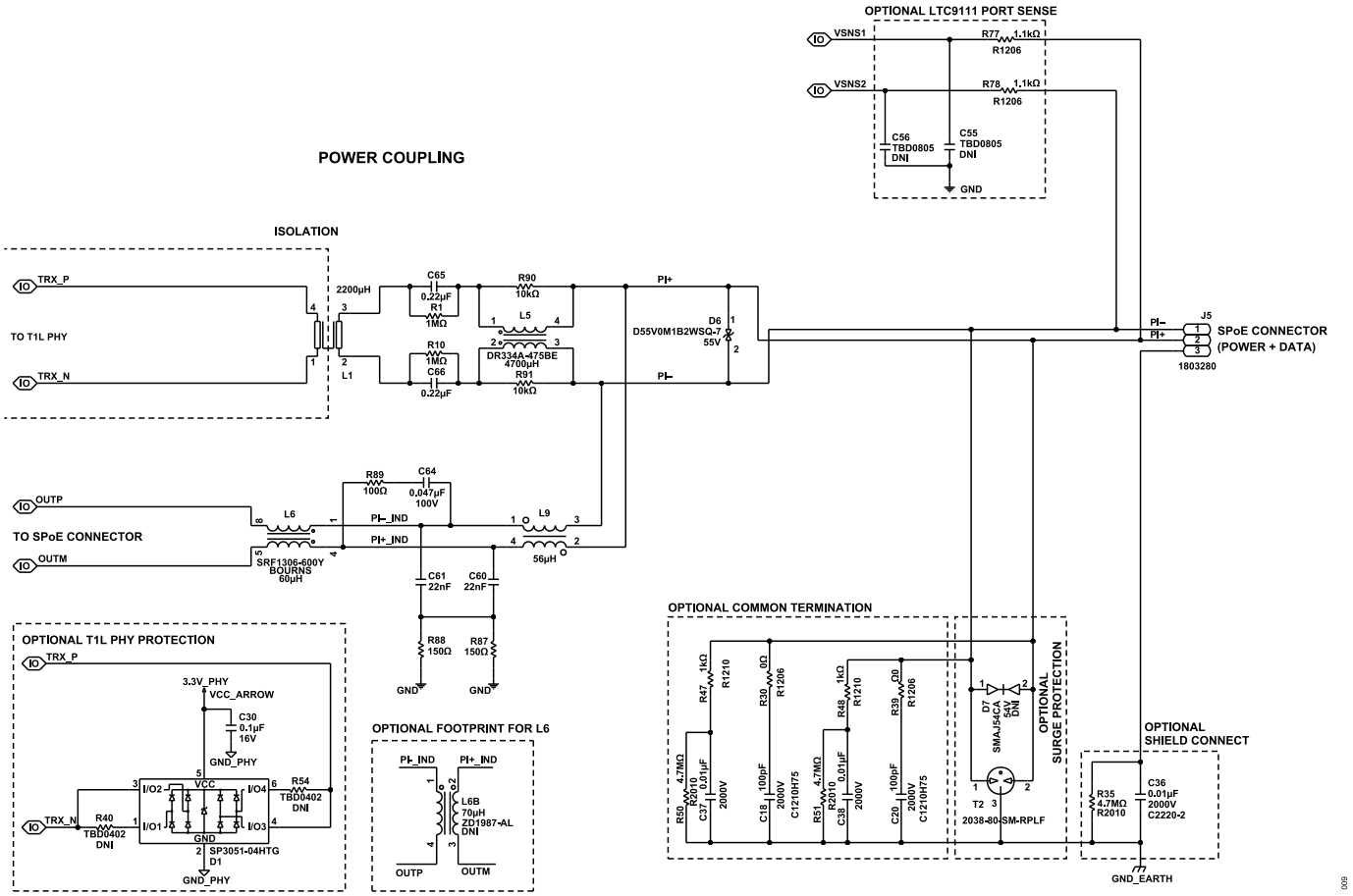

Figure 9. EVAL-10BT1L-MCS-BZ Optional Components

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.