# ISOLATED DIGITAL INPUT / FET OUTPUT BOARD

MODELS 104-IDIO-16 104-IDIO-16E 104-IDIO-8 104-IDIO-8E 104-IDIO-8 USER MANUAL

File: m104-IDIO-16.F1

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ALWAYS CONNECT AND DISCONNECT YOUR FIELD CABLING WITH THE COMPUTER POWER OFF. ALWAYS TURN COMPUTER POWER OFF BEFORE INSTALLING A BOARD. CONNECTING AND DISCONNECTING CABLES, OR INSTALLING BOARDS INTO A SYSTEM WITH THE COMPUTER OR FIELD POWER ON MAY CAUSE DAMAGE TO THE I/O BOARD AND WILL VOID ALL WARRANTIES, IMPLIED OR EXPRESSED.

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### **Chapter 1: FUNCTIONAL DESCRIPTION**

This board provides isolated digital inputs with Change of State Detection and isolated FET solid state output interfaces for PC/104 compatible computers. The board provides sixteen optically-isolated inputs for AC or DC control signals and sixteen isolated FET solid state outputs. The board occupies eight consecutive addresses in I/O space. Read and write operations are done on an 8-bit-byte oriented basis. Many versions of this board are available. The basic model includes Change Of State (COS) detection on inputs (flags an interrupt), and model 16E doesn't have COS detection and doesn't use interrupts. Models IDIO-8 and IDIO-8E provide eight inputs and outputs. Models IDO-16 and IDO-8 have sixteen and eight outputs only, respectively. In eight-channel input and output versions, the I/O headers remain fully populated.

### **INPUTS**

The isolated inputs can be driven by either AC or DC signals and are not polarity sensitive. Input signals are rectified by photocoupler diodes. A 1.8K-ohm resistor in series dissipates unused power. Standard 12/24 AC control transformer outputs can be accepted as well as DC voltages. The input voltage range is 3 to 31 volts (rms). External resistors connected in series may be used to extend the input voltage, however this will raise the input threshold range. Consult with the factory for available modified input ranges.

Each input circuit contains a switchable slow/fast filter that has a 4.7 millisecond time constant. (Without filtering, the response is 10 uSec.) The filter <u>must</u> be selected for AC inputs in order to eliminate the on/off response to AC. The filter is also valuable for use with slow DC input signals in a noisy environment. The filter may be switched out for DC inputs in order to obtain faster response. Filters are individually selected by jumpers. The filters are switched into the circuit when the jumpers are installed in position IN0 to IN15.

#### **INTERRUPTS**

When enabled by a software read to base address +2 (and when a jumper is installed to select one of the interrupt levels IRQ2-7, IRQ10-12, and IRQ14-15), the basic board asserts an interrupt whenever any of the inputs changes state from high to low, or low to high. This is called Change-of-State (COS) detection. Once an interrupt has been generated and serviced, it must be cleared. A software write to base address+1 will clear an interrupt. Before enabling the COS detection, clear any prior interrupt by writing to base address + 1. This interrupt may be disabled by a software write to base address +2, and later re-enabled. (Model IDIO-16 only)

### **OUTPUTS**

The solid state outputs are comprised of sixteen fully protected and isolated FET outputs. The FET's have built in current limiting and are protected against short-circuit, over- temperature, ESD and inductive load transients. The current limitation is activated until the thermal protection acts. The FET's are all off at power-on. Data to the FET's is latched by a write to the base address+0 and to base address+4.

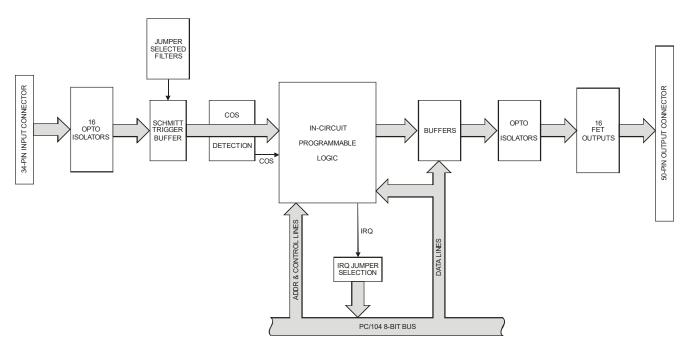


Figure 1-1: Block Diagram

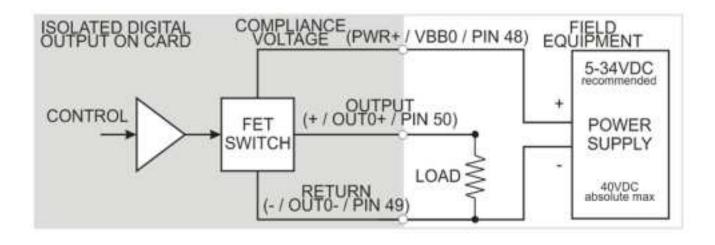


Figure 1-2: Simplified Example Output Connection Diagram

Note: FETs have two output states: Off, where the output is high impedance (no current flows between the VBB and the output — except for the FET's leakage current, amounting to a few  $\mu A$ ), and On, where VBB is connected to the output pin.

Therefore, if no load is connected the FET output will have a high floating voltage (due to the leakage current and no path to the VBB switching voltages return). To mitigate this, please add a load to ground at the output.

### **Chapter 2: INSTALLATION**

A printed Quick-Start Guide (QSG) is packed with the board for your convenience. If you've already performed the steps from the QSG, you may find this chapter to be redundant and may skip forward to begin developing your application.

The software provided with this PC/104 Board is on CD and must be installed onto your hard disk prior to use. To do this, perform the following steps as appropriate for your operating system. Substitute the appropriate drive letter for your CD-ROM where you see d: in the examples below.

### **CD** Installation

The following instructions assume the CD-ROM drive is drive "D". Please substitute the appropriate drive letter for your system as necessary.

#### DOS

- 1. Place the CD into your CD-ROM drive.
- 2. Type Die to change the active drive to the CD-ROM drive.
- 3. Type INSTALLED to run the install program.
- 4. Follow the on-screen prompts to install the software for this board.

### **WINDOWS**

- 1. Place the CD into your CD-ROM drive.
- 2. The system should automatically run the install program. If the install program does not run promptly, click START | RUN and type DIINSTALL, click OK or press ...
- 3. Follow the on-screen prompts to install the software for this board.

### LINUX

1. Please refer to linux.htm on the CD-ROM for information on installing under linux.

### Installing the Hardware

Before installing the board, carefully read Chapter 3 and Chapter 4 of this manual and configure the board according to your requirements. The SETUP Program can be used to assist in configuring jumpers on the board. Be especially careful with Address Selection. If the addresses of two installed functions overlap, you will experience unpredictable computer behavior. To help avoid this problem, refer to the FINDBASE.EXE program installed from the CD. The setup program does not set the options on the board, these must be set by jumpers.

#### To Install the Board

- Install jumpers for selected options and base address according to your application requirements, as mentioned above.
- 2. Remove power from the PC/104 stack.
- 3. Assemble standoff hardware for stacking and securing the boards.
- 4. Carefully plug the board onto the PC/104 connector on the CPU or onto the stack, ensuring proper alignment of the pins before completely seating the connectors together.
- 5. Install I/O cables onto the board's I/O connectors and proceed to secure the stack together or repeat steps 3-5 until all boards are installed using the selected mounting hardware.
- Check that all connections in your PC/104 stack are correct and secure then power up the system.
- 7. Run one of the provided sample programs appropriate for your operating system that was installed from the CD to test and validate your installation.

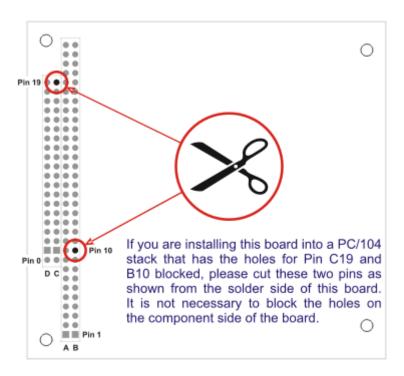


Figure 2-1: PC/104 Key Information

### **Chapter 3: OPTION SELECTION**

### **FILTER RESPONSE SWITCH**

Jumpers are used to select input filtering on a channel-by-channel basis. When jumper IN0 is installed, additional filtering is introduced for input bit 0, IN1 for bit 1, etc.

JUMPER SELECTION	Bit Filtered
IN-0	IN0
-1	IN1
-2	IN2
-3	IN3
-4	IN4
-5	IN5
-6	IN6
-7	IN7

JUMPER SELECTION	Bit Filtered
IN-8	IN8
-9	IN9
-10	IN10
-11	IN11
-12	IN12
-13	IN13
-14	IN14
-15	IN15

This additional filtering provides a slower response for DC signals as described previously and must be used when AC inputs are applied.

### **INTERRUPTS**

Select the desired interrupt level by installing a jumper at one of the locations marked IRQxx. An interrupt is asserted by the board when an Isolated Digital Input bit changes state, if enabled in software as previously described.

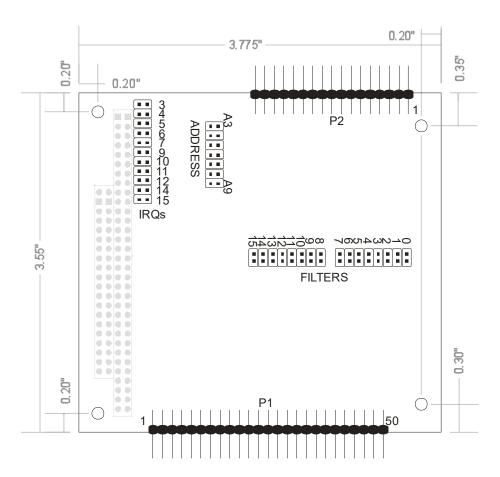


Figure 3-1: Option Selection Map

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### **Chapter 4: ADDRESS SELECTION**

The board occupies eight consecutive addresses in I/O space (although only six addresses are used). The base or starting address can be selected anywhere within the I/O address range 100-3FF provided that it does not cause an overlap with other functions. If the addresses of two installed functions overlap, you will experience unpredictable computer behavior. The FINDBASE program supplied by ACCES will assist you in selecting a base address that will avoid this conflict.

Table 4-1: Address Assignments for Computers

HEX RANGE	USAGE
000-00F	8237 DMA Controller 1
020-021	8259 Interrupt
040-043	8253 Timer
060-06F	8042 Keyboard Controller
070-07F	CMOS RAM, NMI Mask Reg, RT Clock
080-09F	DMA Page Register
0A0-0BF	8259 Slave Interrupt Controller
0C0-0DF	8237 DMA Controller 2
0F0-0F1	Math Coprocessor
0F8-0FF	Math Coprocessor
170-177	Fixed Disk Controller 2
1F0-1F8	Fixed Disk Controller 1
200-207	Game Port
238-23B	Bus Mouse
23C-23F	Alt. Bus Mouse
278-27F	Parallel Printer
2B0-2BF	EGA
2C0-2CF	EGA
2D0-2DF	EGA
2E0-2E7	GPIB (AT)
2E8-2EF	Serial Port
2F8-2FF	Serial Port
300-30F	reserved
310-31F	reserved
320-32F	Hard Disk (XT)
370-377	Floppy Controller 2
378-37F	Parallel Printer
380-38F	SDLC
3A0-3AF	SDLC
3B0-3BB	MDA
3BC-3BF	Parallel Printer
3C0-3CF	VGA EGA
3D0-3DF	CGA
3E8-3EF	Serial Port
3F0-3F7 3F8-3FF	Floppy Controller 1 Serial Port
3F0-3FF	Seliai Fuit

The base address is set up by JUMPERS. Those jumpers control address bits A3 through A9. (Lines A2, A1 and A0 are used on the board to control individual registers. How these three lines are used is described in the Programming section of this manual.)

To determine how to set these JUMPERS for a desired hex-code address, refer to the SETUP program provided with the board. If you prefer to determine proper jumper settings yourself, first convert the hex-code address to binary form. Then, for each "0", install corresponding jumpers and for each "1", remove the corresponding jumper.

The following example illustrates jumper selection corresponding to hex 300 (or binary 11 0000 0xxx). The "xxx" represents address lines A2, A1, and A0 used on the board to select individual registers as described in the Programming section of this manual.

Base Address in Hex Code	;	3	0				0
Conversion Factors	2	1	8	4	2	1	8
Binary Representation	1	1	0	0	0	0	0
Jumper Legend	A9	A8	A7	A6	A5	A4	А3
Addr. Line Controlled	A9	A8	A7	A6	A5	A4	А3
Jumper Selection	OFF	OFF	ON	ON	ON	ON	ON

Carefully review the address selection reference table on the preceding page before selecting the board address. If the addresses of two installed functions overlap, you will experience unpredictable computer behavior.

### **Chapter 5: PROGRAMMING**

The board occupies eight consecutive addresses in PC I/O space. The base, or starting address is selected during installation and will fall on an eight-byte boundary. The board's read and write functions as follows (model 16E doesn't use Base +2):

I/O Address	Read	Write
Base + 0 Base + 1 Base + 2 Base + 3 Base + 4 Base + 5	Readback Read Isolated Inputs 0 - 7 Enable IRQ N/A Readback Read Isolated Inputs 8 - 15	Write FET Outputs 0 - 7 Clear Interrupt Disable IRQ N/A Write FET Outputs 8 - 15 N/A

### **ISOLATED DIGITAL INPUTS**

Isolated digital input states are read as a single byte from the port at Base Address +1 for inputs 0 - 7 or Base Address + 5 for inputs 8 -15. Each of the eight bits within the byte corresponds to a particular digital input. A "1" signifies that the input is energized, (on/high) and a "0" signifies that the input is de-energized (off/low).

#### Read at Base +1

Bit Position	D7	D6	D5	D4	D3	D2	D1	D0
Iso Digital Input	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

### Read at Base +5

Bit Position	D7	D6	D5	D4	D3	D2	D1	D0
Iso Digital Input	IN15	IN14	IN13	IN12	IN11	IN10	IN9	IN8

The board response to inputs is rated at 10 uSec. Sometimes it is necessary to slow down that response to accommodate AC inputs or in noisy environments. Hardware installation of JUMPERS to implement filtering is provided.

The board supports interrupts on change of state of isolated digital inputs. Thus, it is **NOT** necessary to continuously poll inputs (by reading at base address +1 and 5) to detect any state change. To enable this interrupt capability, read at base address +2. To disable interrupts, write at base address +2 or remove the JUMPER that selects interrupt levels (IRQ2 - IRQ7, IRQ10 - IRQ12, IRQ14 and IRQ15).

### **SOLID STATE OUTPUTS**

At power-up, all FET's are initialized in the off state. The outputs are controlled by <u>writing</u> to the Base Address for FET's 0 - 7 and Base + 4 for FET's 8 -15. Data is written to all eight FET's as a single byte. Each bit within the byte controls a specific FET. A "0" turns on the corresponding FET output and a "1" turns it off.

### Write to Base +0

Bit Position	D7	D6	D5	D4	D3	D2	D1	D0
Output Controlled	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

### Write to Base +4

Bit Position	D7	D6	D5	D4	D3	D2	D1	D0
Output Controlled	OUT15	OUT14	OUT13	OUT12	OUT11	OUT10	OUT9	OUT8

For example, if bit D5 is turned on by writing hex DF to the base address, then the FET that is controlled by OUT5 is turned ON, switching the supply voltage (VBB5) to the + Output (OUT5+). All other outputs would be off (high-impedance) between the supply voltage and the output terminals.

Reading from +0 or +4 returns the last written byte.

### **PROGRAMMING EXAMPLES**

No complex driver software is provided with the board because programming is very simple and can be accomplished most efficiently using direct I/O instructions in the language that you are using. The following examples are in C but are readily translated into other languages:

Example: Turn on OUT0 and OUT7-turn all other bits off

Base=0x300; //Base I/O address outportb(Base, 0x7E);

Example: Read the isolated digital inputs

Y=inportb(Base+1); //isolated digital input register, bits 0-7

- -Refer to ACCES32 and WIN32IRQ software directories for Windows drivers and utilities.
- -Refer to the Linux directory on the CD for Linux drivers, utilities, and samples.

## Chapter 6: CONNECTOR PIN ASSIGNMENTS IDC 50 Pin Header Male

Table 6-1: Outputs (P1)

PIN	NAME	FUNCTION
1	VBB15	Bit 15 FET Supply Voltage
2	OUT15-	Bit 15 Power Supply Return (or Ground)
3	OUT15+	Bit 15 Switched (Supply Voltage) Output
4	VBB14	Bit 14 FET Supply Voltage
5	OUT14-	Bit 14 Power Supply Return (or Ground)
6	OUT14+	Bit 14 Switched (Supply Voltage) Output
7	VBB13	Bit 13 FET Supply Voltage
8	OUT13-	Bit 13 Power Supply Return (or Ground)
9	OUT13+	Bit 13 Switched (Supply Voltage) Output
10	VBB12	Bit 12 FET Supply Voltage
11	OUT12-	Bit 12 Power Supply Return (or Ground)
12	OUT12+	Bit 12 Switched (Supply Voltage) Output
13	VBB11	Bit 11 FET Supply Voltage
14	OUT11-	Bit 11 Power Supply Return (or Ground)
15	OUT11+	Bit 11 Switched (Supply Voltage) Output
16	VBB10	Bit 10 FET Supply Voltage
17	OUT10-	Bit 10 Power Supply Return (or Ground)
18	OUT10+	Bit 10 Switched (Supply Voltage) Output
19	VBB9	Bit 9 FET Supply Voltage
20	OUT9-	Bit 9 Power Supply Return (or Ground)
21	OUT9+	Bit 9 Switched (Supply Voltage) Output
22	VBB8	Bit 8 FET Supply Voltage
23	OUT8-	Bit 8 Power Supply Return (or Ground)
24	OUT8+	Bit 8 Switched (Supply Voltage) Output
25		
26		
27	VBB7	Bit 7 FET Supply Voltage
28	OUT7-	Bit 7 Power Supply Return (or Ground)
29	OUT7+	Bit 7 Switched (Supply Voltage) Output
30	VBB6	Bit 6 FET Supply Voltage
31	OUT6-	Bit 6 Power Supply Return (or Ground)
32	OUT6+	Bit 6 Switched (Supply Voltage) Output
33	VBB5	Bit 5 FET Supply Voltage
34	OUT5-	Bit 5 Power Supply Return (or Ground)
35	OUT5+	Bit 5 Switched (Supply Voltage) Output
36	VBB4	Bit 4 FET Supply Voltage
37	OUT4-	Bit 4 Power Supply Return (or Ground)
38	OUT4+	Bit 4 Switched (Supply Voltage) Output
39	VBB3	Bit 3 FET Supply Voltage
40	OUT3-	Bit 3 Power Supply Return (or Ground)
41	OUT3+	Bit 3 Switched (Supply Voltage) Output
42	VBB2	Bit 2 FET Supply Voltage
43	OUT2-	Bit 2 Power Supply Return (or Ground)
44	OUT2+	Bit 2 Switched (Supply Voltage) Output
45	VBB1	Bit 1 FET Supply Voltage
46	OUT1-	Bit 1 Power Supply Return (or Ground)
47	OUT1+	Bit 1 Switched (Supply Voltage) Output
48	VBB0	Bit 0 FET Supply Voltage
49	OUT0-	Bit 0 Per Supply Voltage  Bit 0 Power Supply Return (or Ground)
-		
50	OUT0+	Bit 0 Switched (Supply Voltage) Output

FET outputs are connected from the board via a 50-pin HEADER type connector named **P1**. The mating connector is an IDC type with 0.1 inch centers or equivalent. The wiring may be directly from the signal sources or may be on ribbon cable from screw terminal accessory boards. Pin assignments are as depicted on the previous page.

**Isolated Inputs** are connected to the board via a 34-pin HEADER type connector named **P2**. The mating connector is an IDC type with 0.1 inch centers or equivalent.



Table	6-2:	Inputs	(P2)
-------	------	--------	------

PIN	NAME	FUNCTION
1	IIN0 A	Isolated Input 0 A
2	IIN0 B	Isolated Input 0 B
3	IIN1 A	Isolated Input 1 A
4	IIN1 B	Isolated Input 1 B
5	IIN2 A	Isolated Input 2 A
6	IIN2 B	Isolated Input 2 B
7	IIN3 A	Isolated Input 3 A
8	IIN3 B	Isolated Input 3 B
9	IIN4 A	Isolated Input 4 A
10	IIN4 B	Isolated Input 4 B
11	IIN5 A	Isolated Input 5 A
12	IIN5 B	Isolated Input 5 B
13	IIN6 A	Isolated Input 6 A
14	IIN6 B	Isolated Input 6 B
15	IIN7 A	Isolated Input 7 A
16	IIN7 B	Isolated Input 7 B
17		
18		
19	IIN8 A	Isolated Input 8 A
20	IIN8 B	Isolated Input 8 B
21	IIN9 A	Isolated Input 9 A
22	IIN9 B	Isolated Input 9 B
23	IIN10 A	Isolated Input 10 A
24	IIN10 B	Isolated Input 10 B
25	IIN11 A	Isolated Input 11 A
26	IIN11 B	Isolated Input 11 B
27	IIN12 A	Isolated Input 12 A
28	IIN12 B	Isolated Input 12 B
29	IIN13 A	Isolated Input 13 A
30	IIN13 B	Isolated Input 13 B
31	IIN14 A	Isolated Input 14 A
32	IIN14 B	Isolated Input 14 B
33	IIN15 A	Isolated Input 15 A
34	IIN15 B	Isolated Input 15 B

### **Chapter 7: SPECIFICATIONS**

#### ISOLATED DIGITAL INPUTS

Number of inputs: Sixteen

Type: Non-polarized, optically isolated from each other and from the computer.

(CMOS compatible)

Voltage Range: 3 to 31 DC or AC (40 to 10000 Hz)

Isolation: 500V\*(see note) channel-to-ground or channel-to channel

Input Resistance: 1.8K ohms in series with opto coupler Response Time: 4.7 mSec w/filter, 10 uSec w/o filter (typical)

Interrupts: Software controlled with jumper IRQ selection (model 104-IDIO-16 only)

### **ISOLATED FET OUTPUTS**

Number of outputs: Sixteen Solid State FET's (off @ power up)

Output Type: High Side Power MOSFET Switch. Protected against short circuit, over-

temperature, ESD, can drive inductive loads.

Voltage Range: 5-34VDC recommended (customer supplied) for continuous use, 40VDC

absolute maximum

Current Rating: 2A maximum Leakage Current: 5µA maximum

Turn-on time: Rise time: 90usec (typical)
Turn-off time: Fall time: 110usec (typical)

INTERRUPTS: Interrupts are generated when isolated inputs change state if enabled by

software. (basic model only)

**POWER REQUIRED:** +5VDC @ 0.150A (all FET's ON)

#### **ENVIRONMENTAL**

Operating Temp: 0° to +70°C (optional extended operating temp -40 to +85°C)

Storage Temp: -40 to +85°C

\* Notes on Isolation: Opto-Isolators, connector and FET's are rated for at least 500V, but isolation voltage

breakdowns will vary and is affected by factors like cabling, spacing of pins, spacing between traces on the PCB, humidity, dust and other environmental factors. This is a safety issue so a careful approach is required. For CE certification, isolation was specified at 40V AC and 60V DC. The design intention was to eliminate the influence of common mode. Use proper wiring techniques to minimize voltage between channels and to ground. For example, when working with AC voltages do not connect the hot side of the line to an input. The minimum spacing found on the isolated circuits of this board is 20 mills. Tolerance of higher isolation voltage can be obtained on

request by applying a conformal coating to the board.

### **Customer Comments**

If you experience any problems with this manual or just want to give us some feedback, please email us at: **manuals@accesio.com.** Please detail any errors you find and include your mailing address so that we can send you any manual updates.

