

**DG0889**  
**Demo Guide**  
**PolarFire 12G-SDI Design**



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# 1 Revision History

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The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 1.0

The first publication of the document.

## 2 PolarFire SDI Design

This document describes the method to run the SDI demo on the PolarFire video kit and the HD-SDI daughter card.

The demo design demonstrates the following functions:

- Dual camera module featuring IMX334 Sony image sensor
- YCbCr 422 converter
- SDI Transmitter (TX) IP
- HD-SDI daughter card for the loopback of the SDI data
- SDI Receiver (RX) IP
- HDMI 2.0 IP

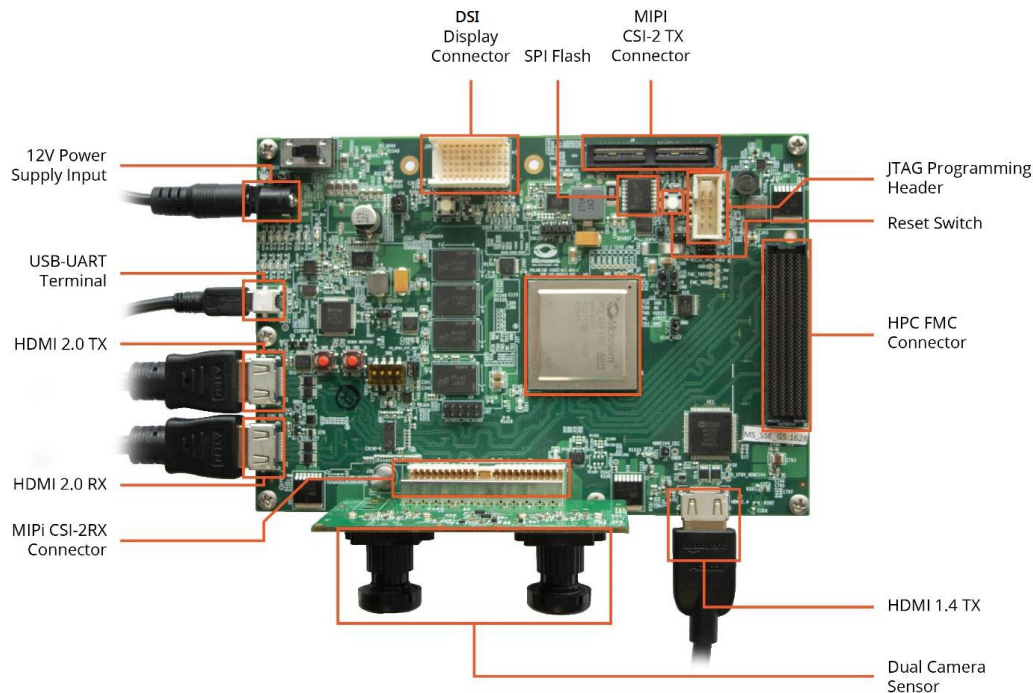
The PolarFire Video Kit (DVP-102-000512-001) features:

- A 300K LE FPGA (MPF300TS, FCG1152I)
- HDMI 2.0 with rail clamps, ReDrivers and corresponding connectors
- DSI Interface
- A High Pin Count (HPC) FMC connector to connect to high-speed interfaces (like 6G-SDI, 12G-SDI and USXGMII)

For more information about this video kit, see <https://www.microsemi.com/existing-parts/parts/150747>.

The following figure highlights the PolarFire Video Kit features:

**Figure 1 • PolarFire Video Kit (DVP-102-000512-001)**



## 2.1 Design Requirements

The following table lists the hardware and software required to run the demo.

**Table 1 • Design Requirements**

| Design Requirement           | Description                                                               |
|------------------------------|---------------------------------------------------------------------------|
| <b>Hardware</b>              |                                                                           |
| -PolarFire VIDEO KIT         | DVP-102-000512-001 REV 1.0                                                |
| -USB A to mini-B cable       | Required for FPGA programming                                             |
| -HDMI cable                  | HDMI A Male to Male cable                                                 |
| -HDMI monitor                | HDMI monitor for the HDMI 2.0 TX port.                                    |
| -Power Adapter               | 12V, 5A                                                                   |
| -Host PC                     | A host PC with USB port                                                   |
| -HD-SDI daughter card        | HDSDI daughter card with Coaxial BNC to BNC Male to Male Cable            |
| <b>Software</b>              |                                                                           |
| -Program_Debug_v12.2_win.exe | This executable file installs FlashPro Express, used to program the FPGA. |

## 2.2 Prerequisites

Before you start:

1. Download the programming job file from:  
[http://soc.microsemi.com/download/rsc/?f=mpf\\_dg0889\\_liberosoc\\_jb](http://soc.microsemi.com/download/rsc/?f=mpf_dg0889_liberosoc_jb)
2. Download and install the GUI from:  
[http://soc.microsemi.com/download/rsc/?f=mpf\\_dg0849\\_liberosoc\\_gui](http://soc.microsemi.com/download/rsc/?f=mpf_dg0849_liberosoc_gui)
3. Download and install the Program and Debug software from:  
[http://soc.microsemi.com/download/reg/download.aspx?p=f=ProgramDebug\\_v12\\_2\\_WIN](http://soc.microsemi.com/download/reg/download.aspx?p=f=ProgramDebug_v12_2_WIN)

**Note:** On this web page, download the `Program_Debug_v12.2_win.exe` binary file. Installation of this executable file installs FlashPro Express used for FPGA programming. FlashPro Express is used in this demo.

**Note:** The **Program and Debug** Software also installs the drivers on the host PC to detect the COM port for running the demo. Install this software whenever the demo is run on a different host PC.

## 2.3 Demo Resources

The `mpf_dg0889_liberosoc_jb` folder contains the following resources:

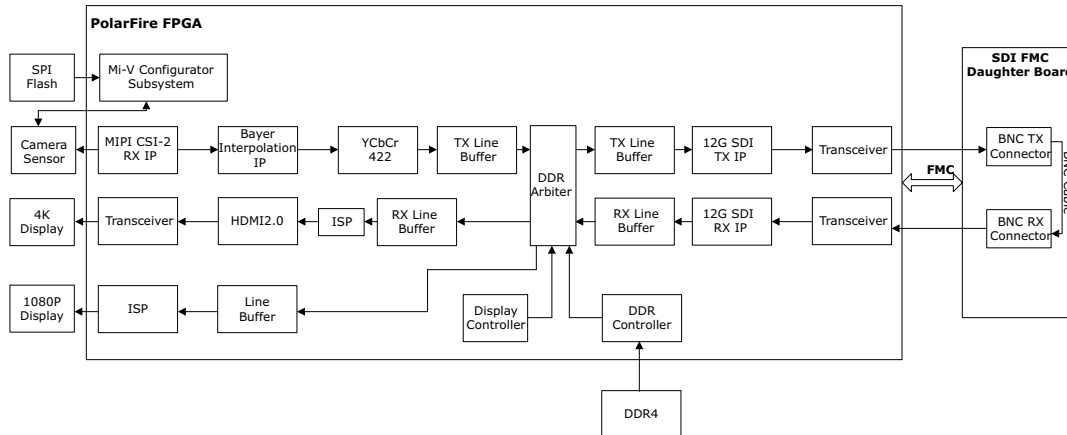
- **A job file (JOB file):** This file includes the FPGA bitstream and the SPI Flash image to be programmed.

For programming the FPGA using the job file, see [Programming the PolarFire Device](#), page 8.

## 2.4 Demo Design

The following block diagram shows the SDI demo design implemented in the PolarFire FPGA using Libero SoC.

**Figure 2 • Top-Level Block Diagram**



The following points summarize the data flow in the design:

- The demo uses a dual camera module that captures the real-time video data. This video data is received by the PolarFire FPGA via the MIPI-CSI2 RX interface on the board.
- The real-time video data is converted to the YCbCr 422 format by an Image Signal Processing (ISP) IP and stored in the DDR memory as frame buffer.
- The SDI TX IP fetches these frames and transmits the data at 12G using PolarFire Transceiver (XCVR). The 12G-SDI data is looped back via the BNC cable on the SDI daughter card and received at the receive end of the XCVR.
- The SDI RX IP receives the data and stores the frame buffer in the DDR memory in a different address space. Finally, the received data is fetched by the HDMI 2.0 IP and displayed on a HDMI monitor.

The PolarFire 12G-SDI Libero design is available at [http://soc.microsemi.com/download/rsc/?f=mpf\\_dg0889\\_liberosoc\\_df](http://soc.microsemi.com/download/rsc/?f=mpf_dg0889_liberosoc_df).

The Libero project must be opened using Libero SoC v12.2. The Libero SoC v12.2 is available for download at <https://www.microsemi.com/product-directory/design-resources/1750-libero-soc#downloads>.

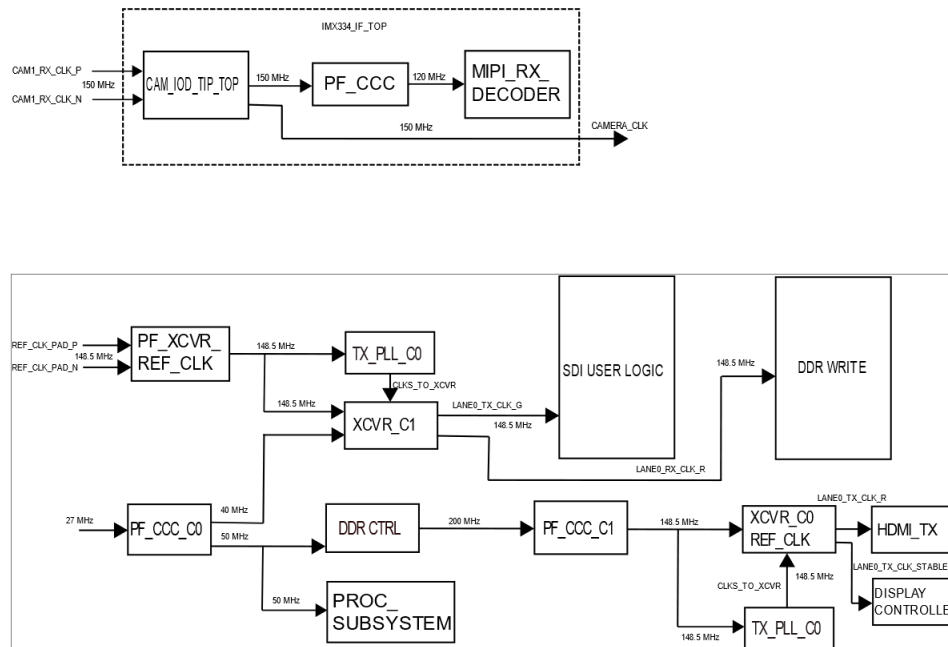
### 2.4.1 Clocking Structure

The clocks generated from the onboard oscillator are used in the demo design. Using the 27 MHz reference frequency from the onboard oscillator, PF\_CCC\_C0 generates a 40 MHz clock for the XCVR\_ERM\_C1 (SDI\_RX), and a 50 MHz clock for the Mi-V processor subsystem and DDR Controller. Using the reference frequency of 200 MHz (DDR System clock), PF\_CCC\_C1 generates a 148.5 MHz clock for XCVR\_ERM\_C0 (HDMI) and Display Controller.

Using the 148.5 MHz onboard oscillator, PF\_XCVR\_REF\_CLK generates the following clocks:

- 148.5 MHz clock (LANE0\_TX\_CLK\_G) for the SDI User Logic.
- 148.5 MHz clock (LANE0\_RX\_CLK\_R) for the DDR Write Logic.

Using the reference frequency of 150 MHz, PF\_CCC generates a 120 MHz clock for MIPI\_RX\_DECODER. Figure 3, page 5 shows the clocking structure of the design.

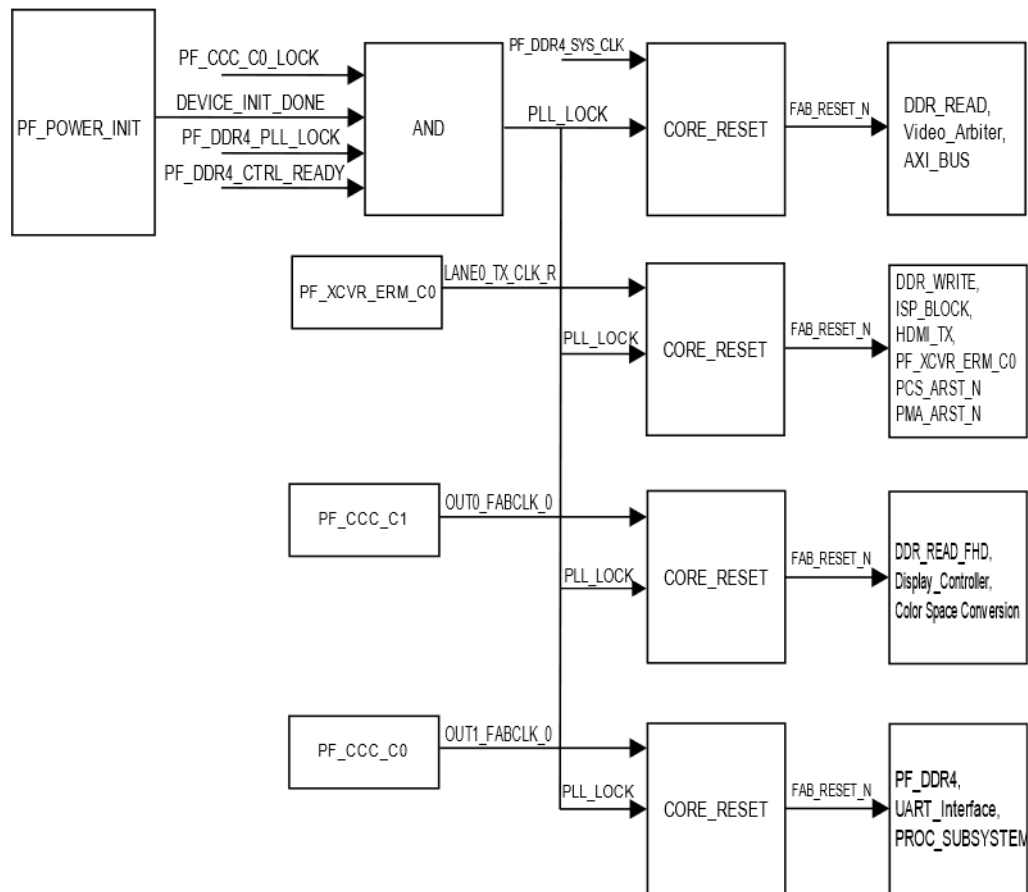
**Figure 3 • Clocking Structure**

## 2.4.2 Reset Structure

The Mi-V processor subsystem, XCVR, UART, SDI, ISP, and all other blocks are reset when the following signals are asserted:

- DEVICE\_INIT\_DONE from PF\_INIT\_MONITOR
- DDR\_CTRL\_RDY from DDR Controller
- DDR\_PLL\_LOCK
- PLL\_LOCK of PF\_CCC\_C0

The reset structure is shown in [Figure 4](#), page 6.

**Figure 4 • Reset Structure**

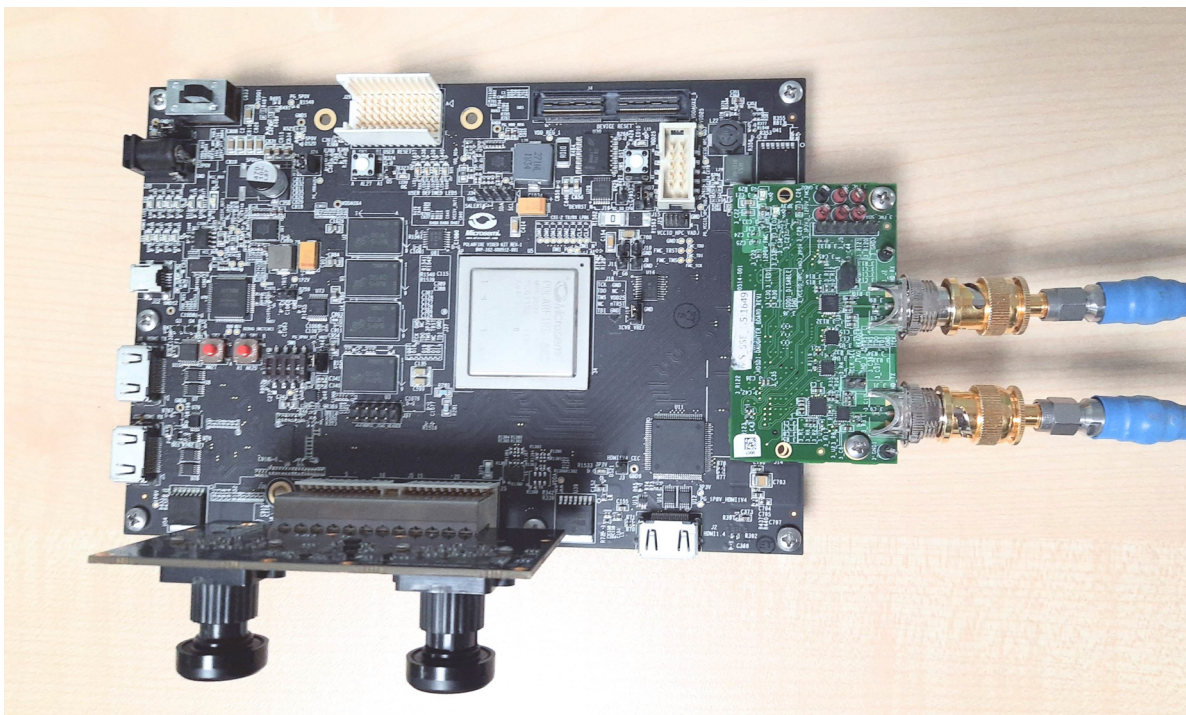
## 2.5 Setting Up the Demo

Setting up the demo involves the following processes:

- [Setting Up the Hardware](#), page 6.
- [Programming the PolarFire Device](#), page 8.

### 2.5.1 Setting Up the Hardware

Setting up the hardware involves interfacing the HD-SDI daughter board rev 1 card with the PolarFire Video Kit along with the HDMI monitor and verifying the jumper settings.

**Figure 5 • Board Setup**

Follow these steps:

1. Connect the J1 connector of the dual camera sensor module to J38 interface of the video kit.
2. Connect the Full HD HDMI monitor to J2 (HDMI 1.4 TX port) of the video kit using the HDMI cable.
3. Connect the HDMI monitor to **J1** (HDMI 2.0 TX port) of the video kit (for 4k video output).
4. Connect the host PC and the video kit through **J12** of the video kit using the USB mini cable.
5. Connect the power supply cable to **J20** of the video kit.
6. Connect the **3\_J4** of HD-SDI daughter board rev1 card to **J14** of the FMC connector of video kit.
7. On HDSOI DAUGHTER BOARD connect **HD\_TX(3\_J1)** to **HD\_RX(3\_J2)** with coaxial BNC to BNC male to male connector.
8. Ensure that the following jumper settings are set on the video kit.
9. Power-up the HDMI monitor.
10. Power-up the board using the SW4 slide switch.

**Table 2 • Jumper and Switch Settings**

| Jumper | Default Position | Functionality                                                |
|--------|------------------|--------------------------------------------------------------|
| J15    | Open             | SPI Slave and Master mode selection. By default, SPI master. |
| J17    | Open             | 100K PD for TRSTn. By default, 1K PD is connected.           |
| J19    | Pin 1&2          | Default: XCVR_VREF is connected to GND.                      |
| J28    | Pin 1&2          | Default: Programming through the FTDI.                       |
| J24    | Pin 2&4          | Default: VDDAUX4 voltage is set to 3V3.                      |
| J25    | Pin 3&4          | Bank4 voltage is set to 2V5.                                 |
| J36    | Pin 1&2          | Default: Board power up through the SW4.                     |
| SW4    | OFF              | Power ON/OFF switch.                                         |
| SW6    | ON               | User slide switch.                                           |
| J20    | 12 Volts input   | 12V input to the board.                                      |

The PolarFire SDI demo is set up. See the following section to program the PolarFire device.

## 2.5.2 Programming the PolarFire Device

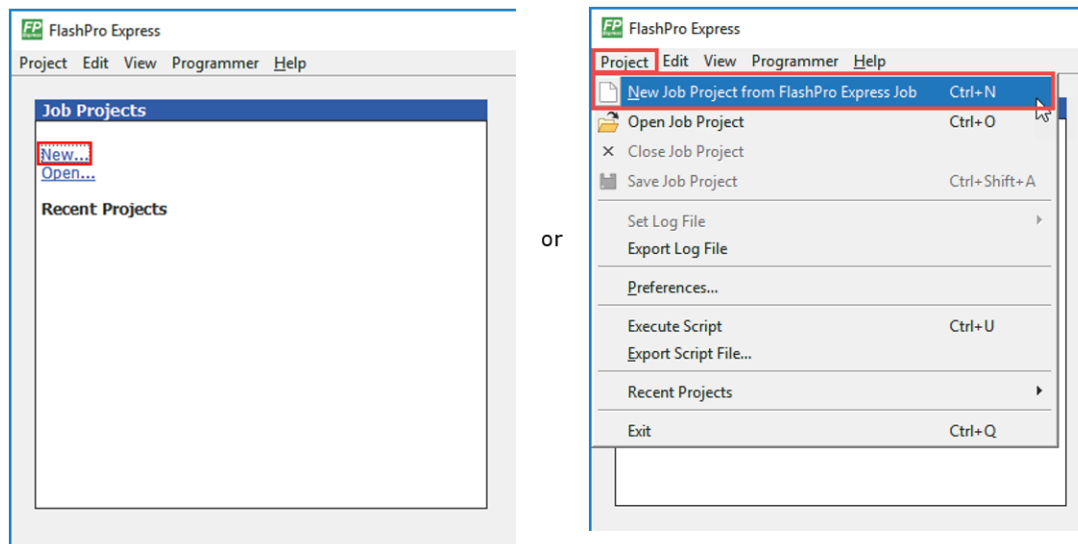
This chapter describes how to program the PolarFire device with the job file using Flashpro Express. The job file is available at the following design files folder location:

<\$Download\_Directory>\mpf\_dg0889\_liberosoc\_jb

Follow these steps:

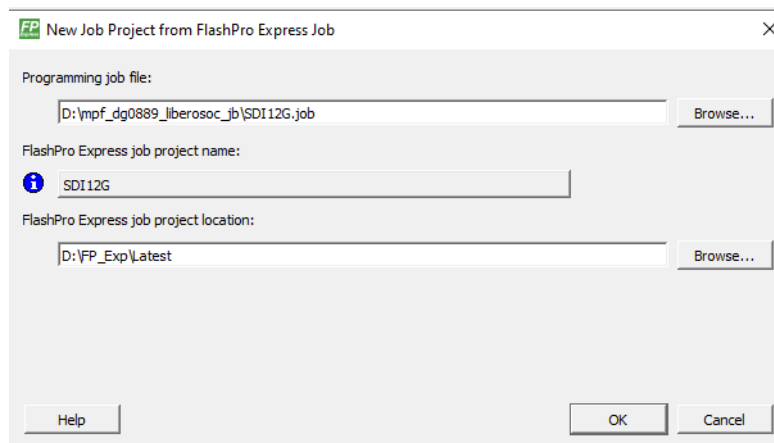
1. On the host PC, start the FlashPro Express software from its installation directory.
2. Select **New** or **New Job Project from FlashPro Express Job** from Project menu to create a new job project, as shown in the following figure.

**Figure 6 • FlashPro Express Job Project**



3. Enter the following in the New Job Project from FlashPro Express Job dialog box:
  - **Programming job file:** Click **Browse** and navigate to the location where the job file is located and select the file. The default location is:  
 <\$Download\_Directory>\mpf\_dg0889\_liberosoc\_jb
  - **FlashPro Express job project location:** Select **Browse** and navigate to the location where you want to save the project.

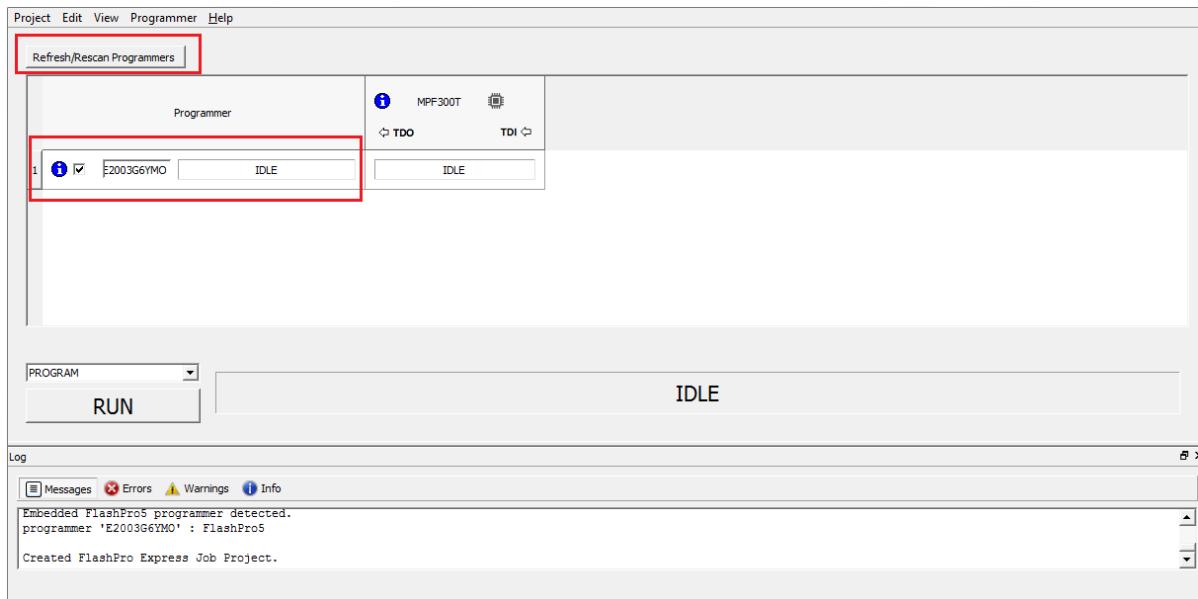
**Figure 7 • New Job Project from FlashPro Express Job**



4. Click **OK**. The required programming file is selected and ready to be programmed in the device.

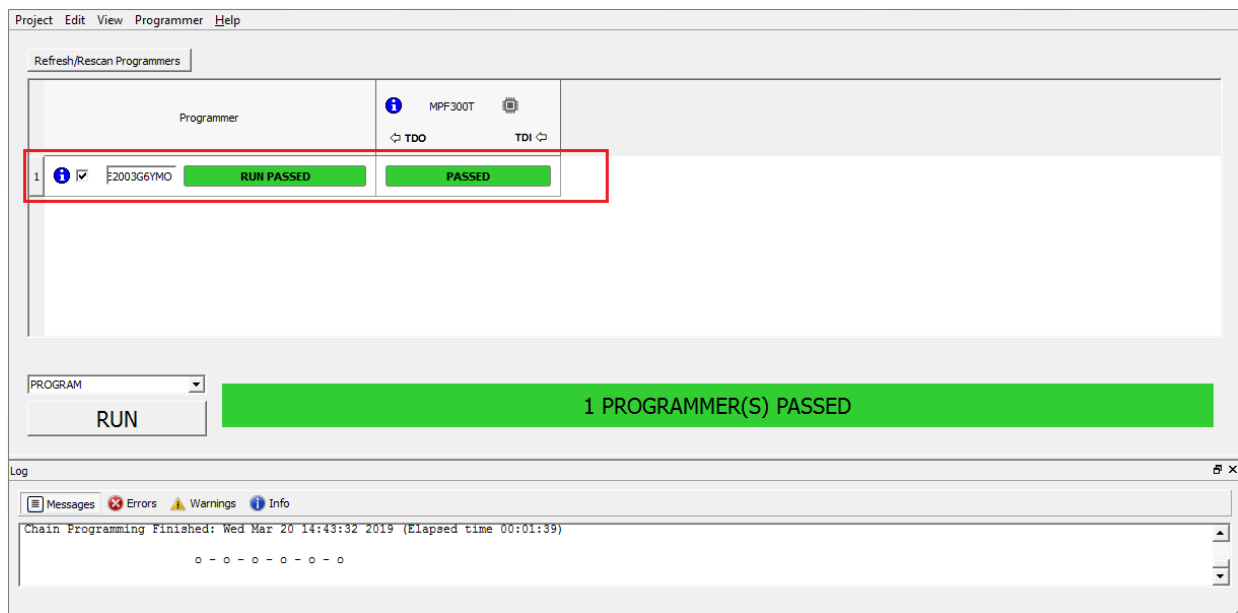
- The FlashPro Express window appears as shown in Figure 4, page 7. Confirm that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click **Refresh/Rescan Programmiers**.

**Figure 8 • Programming the Device**



- Click **RUN** to program the device. When the device is programmed successfully, a **RUN PASSED** status is displayed as shown in Figure 5, page 7. See Running the Demo, page 8.

**Figure 9 • FlashPro Express-RUN PASSED**



- Close FlashPro Express (**Project > Exit**).

The PolarFire device and SPI Flash are programmed. Power cycle the board using switch SW4. After power cycling, the HDMI monitor displays the live video from camera.

## 2.5.3 Running the Demo

The demo features receiving the MIPI Rx data from the IMX334 camera with 4K resolution at 30 frames per second (fps). The frames from camera are converted to YCbCr 422 format and stored in DDR. The 12G SDI Tx IP transmits the DDR video frames using PolarFire XCVR. The 12G SDI Rx IP receives the SDI video and stores the frames in DDR. The HDMI IP reads the frame buffer written by SDI Rx IP and sends out to HDMI display using XCVR. The image processing IPs are enabled on the display side of the video pipeline.

In the demo design, two display controllers are used to provide two video outputs:

- Full HD output (1920x1080 60Hz resolution)
- 4K output (3840x2160 30Hz resolution)

The Full HD output supports panning and Image enhancements such as contrast, brightness and color balance. The 4K output supports Image enhancements. The GUI application for image enhancements is common for both the video outputs.

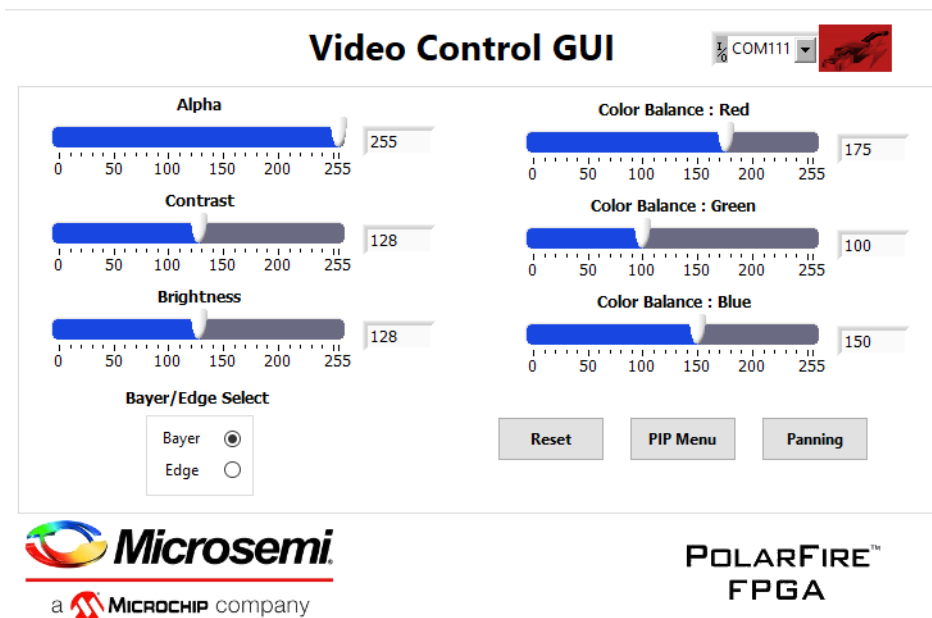
Running the demo involves verifying the imaging and video settings using the Video\_Control GUI and then observing the result on the HDMI monitor.

To use the demo GUI:

1. Start the Video\_Control GUI from the installation directory.

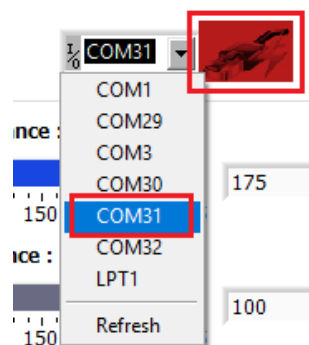
The GUI is displayed as shown in the following figure.

**Figure 10 • Video\_Control GUI**



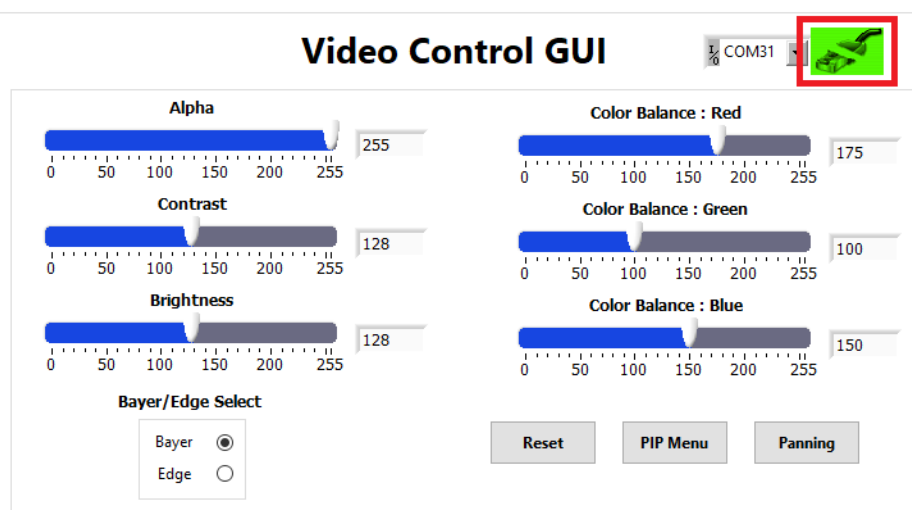
2. Select the second largest **COM** port on the GUI and select the **Connect** option.

**Figure 11 • Connecting the GUI and Video kit**



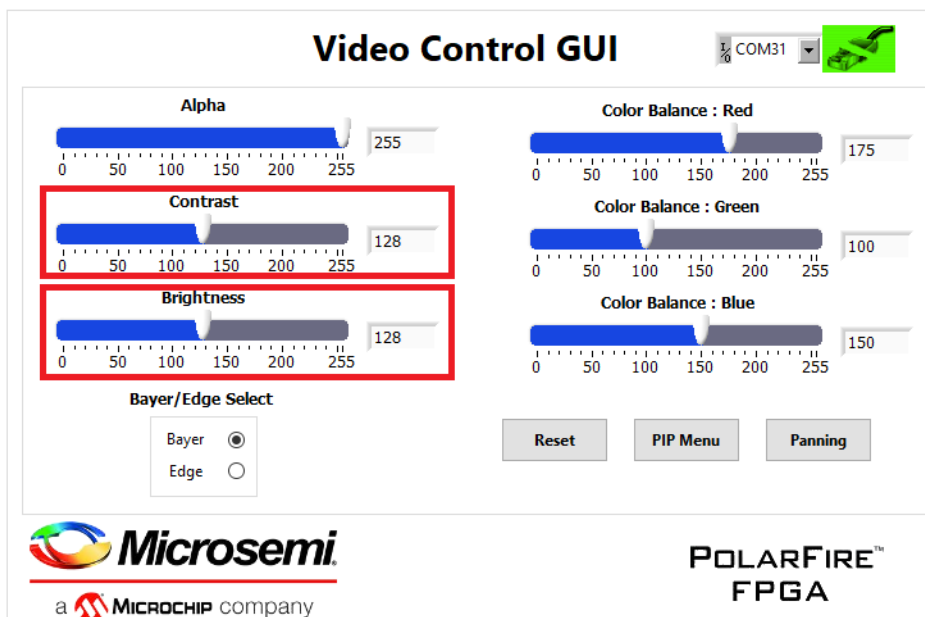
- The Connect button turns green indicating a successful connection.

**Figure 12 • Connection Successful**

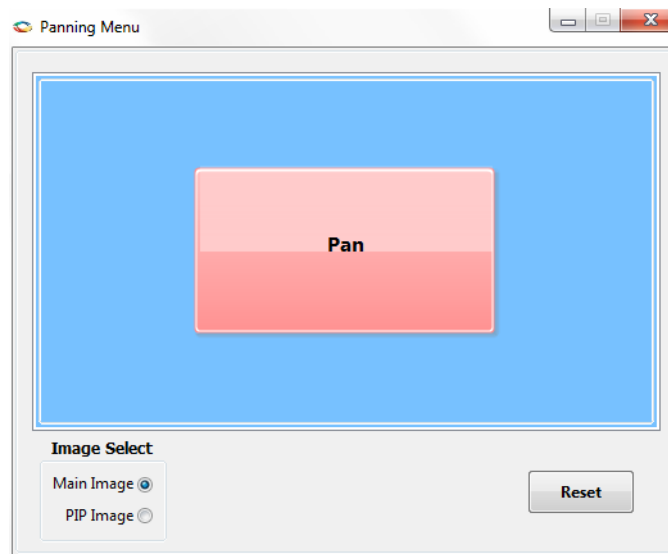


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- Use the **Contrast** and **Brightness** sliders to adjust the contrast and brightness and observe the change on the HDMI monitor. The sliders are highlighted in the following figure.

**Figure 13 • Adjusting Contrast and Brightness**

5. Similarly, adjust the color balance of the image using the color balance sliders.
6. In the main video control GUI window, select the **Panning** option to view a particular area of the main or the PIP image within a 4K image.
7. In the **Panning** Menu, use **Image Select** to select the image to be panned (Main image or PIP image). Any area of the 4K camera feed can be viewed by dragging the pink box horizontally or vertically. The **Reset** option sets the view of the **Main image** and **PIP image** to its default center position.

**Figure 14 • Panning Menu**

8. Close the **Panning Menu** to return to the main GUI.
9. Close the GUI to exit from the demo.

**Note:** The following features in the GUI are not supported in the current SDI design:

- Alpha
- Edge
- PIP

This concludes the demo.