Gowin MIPI DPHY RX TX
User Guide

IPUG112-1.0E,11/17/2017

Disclaimer

Revision History

Date	Version	Description
11/17/2017	1.0E	Initial version.

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1 About This Guide

1.1 Purpose

Gowin MIPI DPHY RX TX mainly documents its functions and features, ports, timing, configuration, and reference design, etc., which helps users to quickly learn Gowin MIPI DPHY RX TX features and usage.

1.2 Supported Products

The information in the guide applies to the following products:

1. GW1N series FPGA products: GW1N-4
2. GW1NR series FPGA products: GW1NR-4
3. GW2A series FPGA products: GW2A-18, GW2A-55;
4. GW2AR series FPGA products: GW2AR-18.

1.3 Related Documents

The latest user guides are available on our Website. Refer to the related documents via http://www.gowinsemi.com.cn:

1. GW1N series FPGA Products Data Sheet
2. GW1NR series FPGA Products Data Sheet
3. GW2A series FPGA Products Data Sheet
4. GW2AR series FPGA Products Data Sheet
5. Gowin Software User Guide

1.4 Abbreviations and Terminology

The abbreviations and terminologies used in this manual are as shown in Table **1-1** below.

Table 1-1 Abbreviations and Terminologies

Abbreviations and Terminology	Full Name	Meaning
FIFO	First Input First Output	First Input First Output
IP	Intellectual Property	Intellectual Property
RAM	Random Access Memory	Random Access Memory
LUT	Look-up Table	Look-up Table
GSR	Global System Reset	Global System Reset
ECC	Error Correcting Code	Error Correcting Code

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If any questions, comments, or suggestions, please feel free to contact us directly.

Website: http://www.gowinsemi.com.cn

E-mail：support@gowinsemi.com

Tel: +86 755 8262 0391

2 Overview

2.1 MIPI DPHY TX RX IP

Gowin MIPI DPHY TX RX IP applies to Display Serial Interface(DSI) and Camera Serial Interface (CSI), which is designed for receiving and sending pictures or video data. MIPI DPHY provides a physical layer definition.

Table 2-1 MIPI DPHY RX/TX IP

MIPI DPHY RX/TX IP	
IP Core Application	
Supported Devices	GW1N-4, GW1NR-4, GW2A-18, GW2AR-18, GW2A-55
Logic Resource	Please refer to Table 3-2 and Table 3-3.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Designs	Verilog
TestBench	Verilog
Test and Design Flow	
Integrated Software	Synplify_Pro
Application Software	GowinYunYuan

2.2 MIPI DPHY

Mobile Industry Processor Interface (MIPI) is an interface standard for mobile devices. MIPI DPHY provides a physical definition for DSI and CSI and describes the physical layer interface protocols of source synchronous, high speed, and low power. In accordance with application requirements, MIPI DPHY includes RX and TX, used for receiving or transmitting the data in line with MIPI DPHY. Figure 2-1 shows the structure view.

MIPI DHPY typically incorporates one clock lane and from one to four data lanes. You can configure the number of data lanes using IDE. The clock and data lanes can switch between1.2V LVCMOS signal and SLVS-200 differential signal.

MIPI DPHY supports the following two data transmission modes:

- High-speed (HS) mode
- Low-power (LP) mode

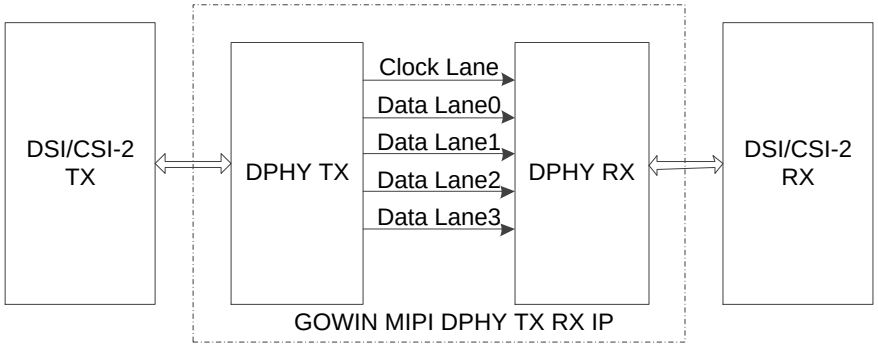
In HS mode, video data is delivered over a differential pair. Depending on the applications, the HS mode can be utilized at all times, or the DPHY can switch from HS differential lanes to signal ended.

When DPHY is sending single ended data, this is called LP mode.

Note!

- In camera and display applications, LP mode is entered to reduce power during the blanking period;
- In display applications, LP mode is used for screen configuration.

Figure 2-1 MIPI DPHY Structure View



3 Features and Performance

3.1 Key Features

- In line with MIPI Alliance Standard for DPHY Specification, version 1.1;
- Interfaces to MIPI CSI2 and DSI, RX and TX devices;
- Supports unidirectional High-speed (HS) mode;
- Supports bidirectional Low-power operation mode;
- Deserializes and serializes High-speed data into byte data packets;
- In HS mode, Line Rate of single channel port supports the range from 80Mb/s to 1GMb/s.
- Data transmission is kept in LP mode with the speed of 10Mb/s.

3.2 Max. Frequency

The max. frequency of MIPI DPHY is mainly determined by Line Rate and the speed grade of the devices.

3.3 Latency

DPHY TX Latency is the time delay period from data_in [7:0] to HS_DATA output.

DPHY RX Latency is the time delay period from the input of HS_DATA SOT (start-of-transmission) to data_out [7:0] output.

See Table 3-1 for the detailed Latency.

Table 3-1 DPHY TX RX Latency

Module	Line Rate（Mb/s）	Lanes	Latency (byteclk Latency (1) Cycle)
DPHY TX	800	1	3
DPHY RX	800	1	11

Note!

[1] Frequency of byteclk (MHz) = line rate in Mb/s / 8

3.4 Resource Utilization

Implement MIPI DPHY RX and TX with Verilog Performance and utilization may vary when using the design in a different device, density, speed, or grade.

MIPI DPHY RX and TX applies to GW1N-4. See Table 3-2 and Table 3-3 for the resource utilization. For the applications on the other GOWINSEMI devices, please refer to the later release.

Table 3-2 MIPI DPHY RX Resource Utilization

Device	Speed Grade	Name	Resource Utilization	Remarks
GW1N-4	-5	LUT	318	● contains four data lanes ● contains word alignment and lane alignment modules ● no clk_cross_fifo
		IODELAY	4	
		REG	300	
		BSRAM	4	
		IDES8	5	
		CLKDIV	1	
		DQCE	1	

Table 3-3 MIPI DPHY TX Resource Utilization

Device	Speed Grade	Name	Resource Utilization	Remarks
GW1N-4	-5	LUT	16	Internal PLL is not configured.
		REG	4	
		CLKDIV	1	
		OSER8	4	
		DQCE	1	

4 Functional Description

MIPI DPHY contains the following two DPHY IP modules:

- DPHY RX
- DPHY TX

In DPHY RX and DPHY TX modules, HS data is deserialized / serialized to and from single data rate byte packets respectively. The data in LP mode can be transmitted bidirectionally on any data channel or clock channel.

Note!

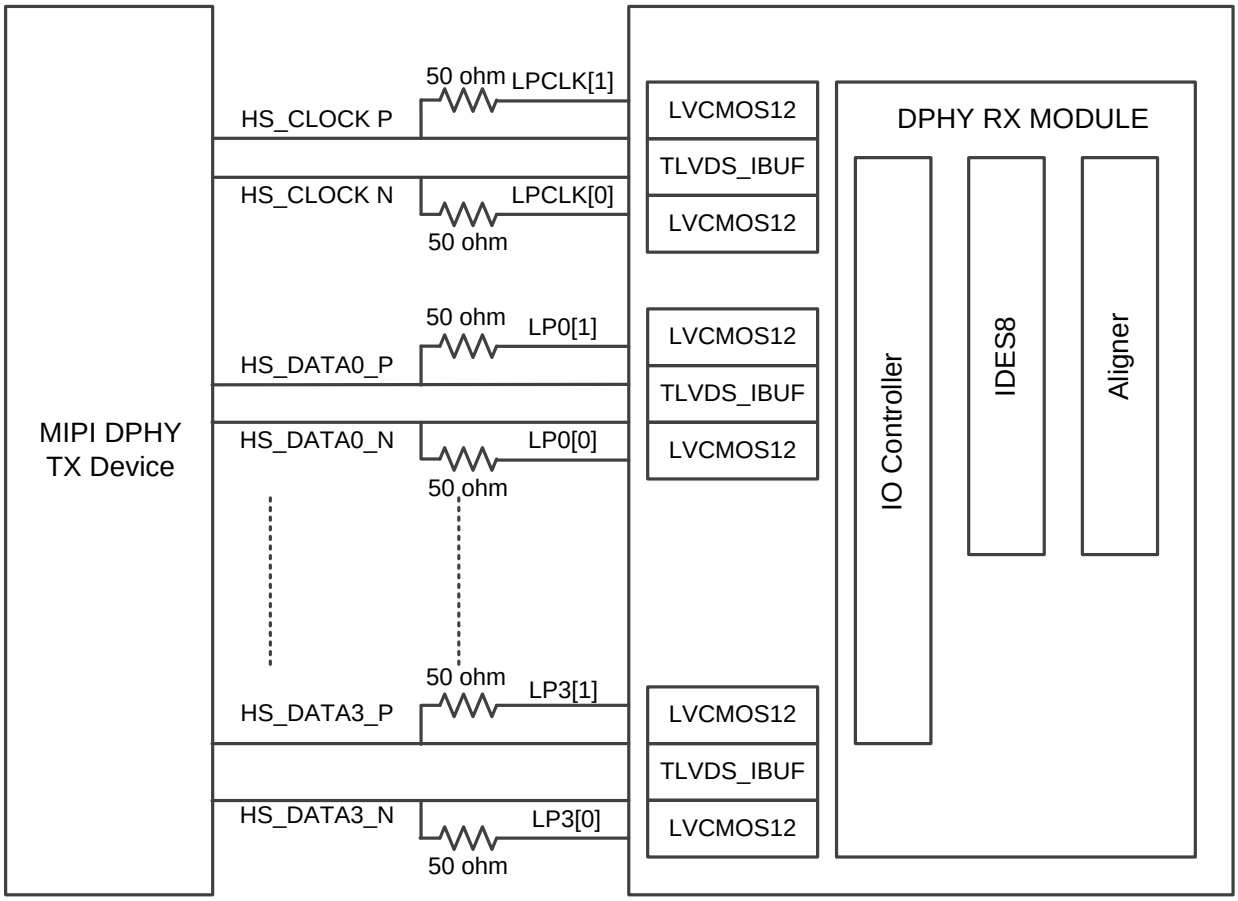
DPHY RX and DPHY TX have different resister network, but both modules support bidirectional LP communication and unidirectional HS communication.

4.1 MIPI DPHY RX Structure and Function

HS data can be received on one clock lane and four clock data lanes by using DPHY RX.

Each clock and data lane uses four IOs. Two IO pins are used to receive HS data with TLVDS differential IO. TLVDS IO is used to handle 200mV common mode voltage. The other two IOs are used as serial termination in HS mode, and can be used to transmit or receive 1.2V CMOS data in LP mode, as shown in Figure 4-1.

Figure 4-1 HS Mode and LP Mode Interface Implementation



In DPHY RX module, HS data is deserialized using IDES8. FPGA drives a divide-by-4 clock and 8-bit byte data directly using IDES8.

Note!

The number of data lanes can be configured. Options are 1, 2,3, or 4 data lanes.

When the data is deserialized to 8-bit byte data, and the lane is aligned, MIPI byte data is available on each byte clock cycle.

Note!

- The alignment is done based on the recognition of MIPI HS_Ready sequence.
- MIPI HS_Ready sequence is transimitted on all data lanes one clock cycle before the packet header.

hs_en is used to reset the alignment module:

1. When hs_en is low, the word alignment module is reset;
2. When hs_en is high, the word alignment module looks for the next HS_Ready sequence;
3. When HS_Ready sequence is detected, the sync signal will go high, and the byte data at the output of the aligner are properly aligned.

The aligner module consists of two subsidiary modules as below:

- The first module aligns the 8-bit data from the deserializer.
- The second module aligns each of the data lanes to each other.

Note!

- In some cases, lane alignment or lane and word alignment is not needed;
- Turn on and off the word and lane alignment using Macro compiling commands.

HS termination is designed to be implemented by controlling IO_Ctrol_RX module with term_en signal. Although there is no direction detection mechanism, the following two ways can be used to enable HS termination:

1. One way is to use HS clock to observe LP to HS data transition on one data lane;
2. Compared with data lane, clock lane will enter HS mode sooner and exit HS mode later. The other way is to initialize LP signals as input at startup, and then observe the clock and data lanes of LP and HS. Once the sequence is detected, term_en can be set as "low" by enabling HS_termination.

IO_Ctrol_RX module also controls LP signal.

Each data lane has a lp*_dir signal, which controls LP data direction between FPGA and the transmitting device.

You can turn on/off LP IP for each clock and data lane individually by using Macro complier directives. This can be handy if the use needs LP mode for one or two MIPI DPHY data lanes.

The LP signals are defined as two bit buses. Signal 1 is usually connected to the P wire side, and 0 to the N wire side, which keeps consistency with LP transition identification scheme.

4.2 MIPI DPHY TX Structure and Function

DPHY TX IP gives users the ability to utilize one clock lane and up to four data lanes. Each lane has four IOs. Two IO pins transmit HS data with ELVDS type or TLVDS type IO. The other two IO pins are used to provide voltage dividing circuit in HS mode and to transmit or receive 1.2V CMOS data in LP mode. For the circuit structure of HS data adopting ELVDS type IO, please refer to Figure 4-2; for the circuit structure of adopting TLVDS type IO, please refer to Figure 4-2.

Figure 4-2 HS Mode and LP Mode Interface Implementation, HS Adopting ELVDS

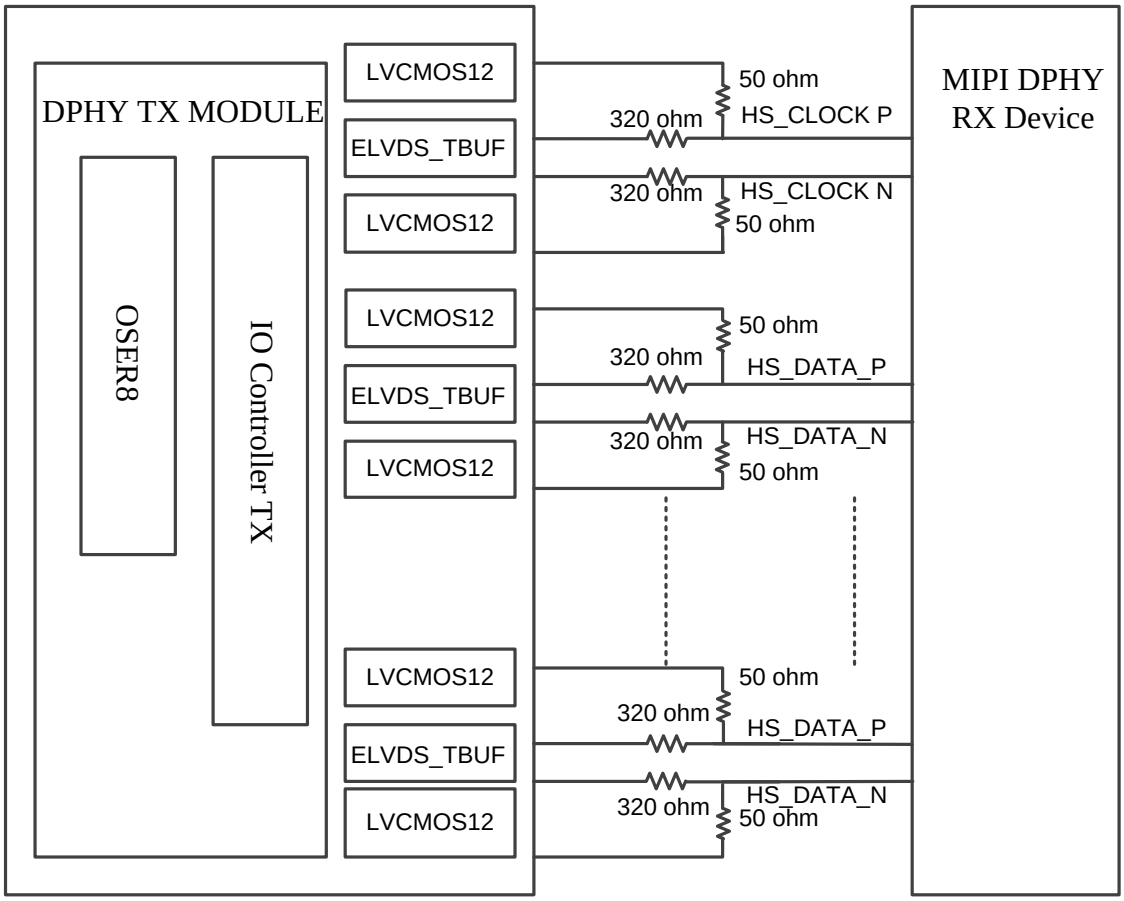
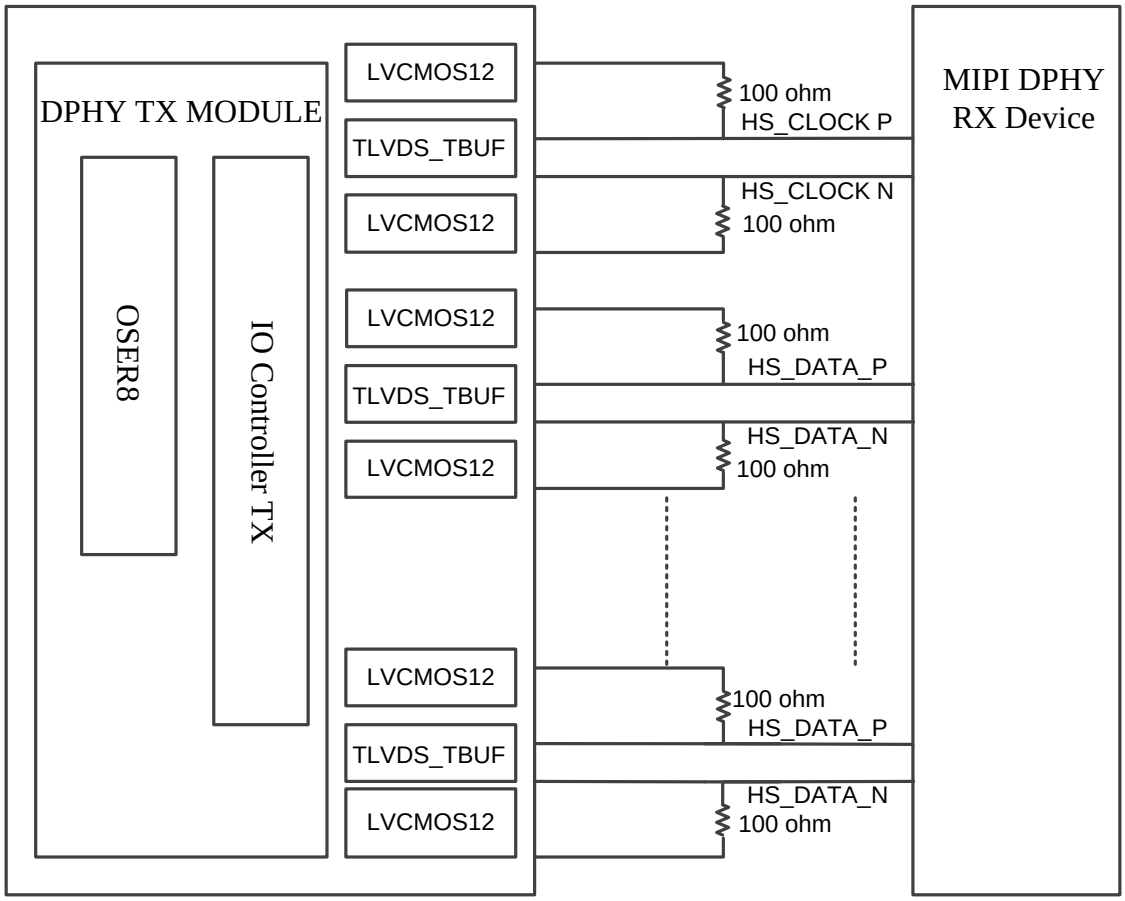


Figure 4-3 HS Mode and LP Mode Interface Implementation, HS Adopting TLVDS



In DPHY TX module, HS data is serialized using OSER8. DPHY TX data is center aligned, so HS data lane and clock lane adopt the clock output signal with a phase shifting 0 and 90 degree generated by PLL respectively. Users can select to use external PLL or internal PLL to provide clock. It should be noted that it takes some time for the internal PLL in FPGA to lock.

IO_Ctrol_TX module controls HS and LP data traffic:

- When hs_clk_en and hs_data_en signals are high, clock and data lanes are enabled in HS mode. In HS mode, IO_Ctrol_TX sets CMOS signals low to create a voltage divider network on LVDS output signals to achieve a 200mV common mode voltage;
- When hs_clk_en or hs_data_en is low, ELVDS IO is set to high impedance, so it does not interfere with LP data transmissions. As MIPI specification defines clock lane going in to or out of HS mode before or after the data lanes, there is an hs_clk_en control signal and an hs_data_en signal;

lp_data_dir signal controls the LP mode direction:

- When hs_*_en='1', the lp*_dir control signal is overwritten;
- While in LP mode, IO_Ctrol_TX module also controls LP data traffic. lp*_dir signal controls LP mode data traffic direction. The LP signals

are defined as two bit buses. Signal 1 is usually connected to the P wire side, and 0 to the N wire side, which keeps consistency with LP transition identification scheme.

5 Ports Description

5.1 MIPI DPHY RX Ports

For the MIPI DPHY RX IO ports description, please refer to Table 5-1.

Table 5-1 DPHY RX IO Ports

Signal	I/O	Description
reset_n	Input	Reset signal, active low
HS_CLK	Input	HCLK
HS_DATA<*N*>	Input	High-speed data lane
hs_en	Input	Initialize the word alignment module at the next HS-Ready sequence
clk_byte	Output	Clock Byte = HS_CLK/4
data_out<*n*> [7:0]	Output	Parallel data output, data lane <*n*>
ready	Output	Active "high" when parallel data is aligned
LP_CLK [1:0]	Bidirectional	LP clock lane; LP_CLK[1] = P wire, LPCLK[0] = N wire
LP_DATA<*N*> [1:0]	Bidirectional	LP data lane<*N*>; LP<*N*> [1] = P wire, LP<*N*> [0] = N wire
term_en	Input	Controls the termination resister of LP signals at outputs, and overwrites lp_data_dir<*n*> control signal when output is "0".
lp_clk_dir	Input	Control the direction of LP clock '0': LP clock receive '1': LP clock transmit
lp_data<*n*>_dir	Input	Controls the direction of LP data '0': LP data receive '1': LP data transmit
lp_clk_out [1:0]	Output	LP clock receive Available when lp_clk_dir = '0' and term_en = '0'

Signal	I/O	Description
lp_data<*n*>_out [1:0]	Output	LP data receive Available when lp_ data<*n*>_dir = '0' and term_en = '0'
lp_clk_in [1:0]	Input	LP clock transmit Available when lp_clk_dir = '1' and term_en = '0'
lp_data<*n*>_in [1:0]	Input	LP data transmit Available when lp_ data<*n*>_dir = '1' and term_en = '0'

5.2 MIPI DPHY TX Ports

For the MIPI DPHY TX IO ports description, please refer to Table 5-2.

Table 5-2 DPHY TX IO

Signal	I/O	Description
reset_n	Input	Reset signal, active low
HS_CLK	Output	HCLK
HS_DATA<*N*>	Output	High-speed data lane<*N*>
clk_byte	Input	Clock Byte = HS_CLK/4 input clock when using internal PLL
CLKOP	Input	The input clock while adopting external PLL. The phase difference between CLKOP and CLKOS is 90°, and they have same frequency with HS_CLK;
CLKOS	Input	
data_in<*n*> [7:0]	Input	Parallel data output, data lane <*n*>, input data 8bit
LP_CLK [1:0]	Bidirectional	LP clock lane; LPCLK[1] = P wire, LPCLK[0] = N wire
LP_DATA<*N*> [1:0]	Bidirectional	LP data lane<*N*>; LP<*N*> [1] = P wire, LP<*N*> [0] = N wire
hs_clk_en	Input	Enables HS clock on output, set LP_CLK signals as 0, and overwrite lp_clk_dir signal
hs_data_en	Input	Enables HS clock on output, set LP_DATA<*N*> signals as 0, and overwrite lp_data<*n*>_dir signal
lp_clk_dir	Input	Control the direction of LP clock '0': LP clock receive '1': LP clock transmit
lp_data<*n*>_dir	Input	Controls the direction of LP data '0': LP data receive '1': LP data transmit

Signal	I/O	Description
lp_clk_out [1:0]	Input	LP clock transmit Available when lp_clk_dir = '1' and hs_clk_en = '0'
lp_data<*n*>_out [1:0]	Input	LP data transmit Available when lp_ data<*n*>_dir = '1' and hs_data_en = '0'
lp_clk_in [1:0]	Output	LP clock receive Available when lp_clk_dir = '0' and hs_clk_en = '0'
lp_data<*n*>_in [1:0]	Output	LP data receive Available when lp_ data<*n*>_dir = '0' and hs_clk_en = '0'

6 Timing Description

This chapter mainly describes the input signals timing of MIPI DPHY RX and TX in HS mode.

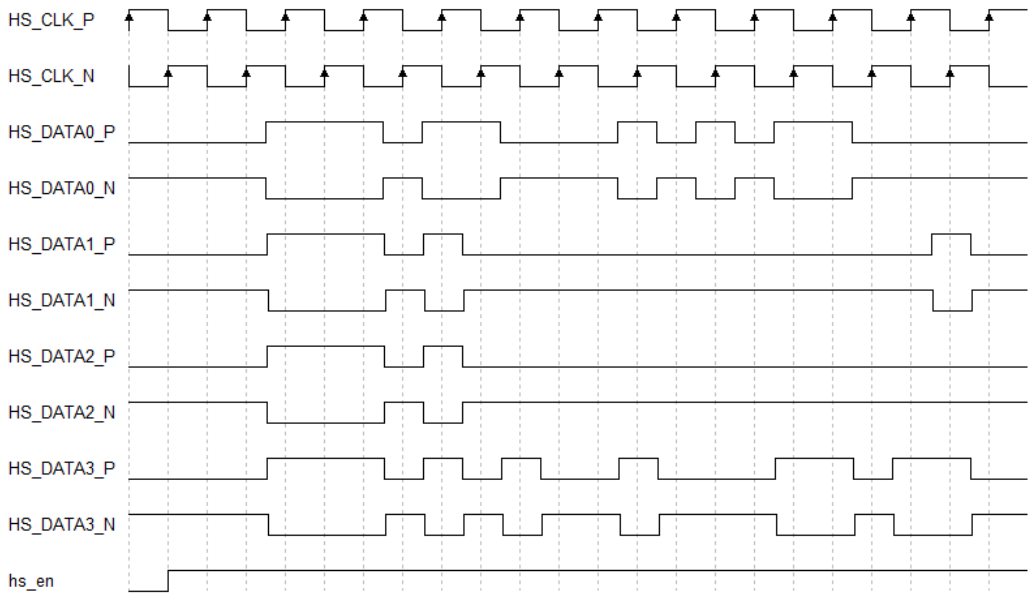
In practical applications, RX and TX can be connected; i.e., RX output can be TX input, and TX output can be RX input. Therefore, only the timing for RX and TX input signals is described as below.

6.1 RX Input Signal Timing

The clock and data lane signal timing of MIPI DPHY RX in HS mode is as shown in Figure 6-1.

In the diagram, one clock lane (HS_CLK) and four data lanes (HS_DATA0, HS_DATA1, HS_DATA2, and HS_DATA3) are used. Clock lane and data lane are all differential signal input. In HS mode, clock and data center is aligned when transmitting image data. The signal hs_en needs to be set as high before receiving HS_DATA data.

Figure 6-1 Input Signal Timing of MIPI DPHY RX in HS Mode



6.2 TX Input Signal Timing

The clock and data lane signal timing of MIPI DPHY TX in HS mode is as shown in Figure 6-2.

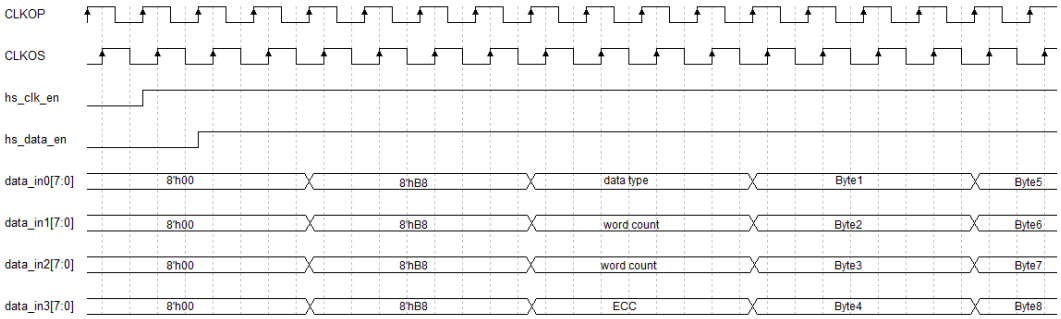
When using TX:

- If internal PLL is set to use, clk_byte needs to be provided (the frequency is 1/4 of HS_CLK);
- If internal PLL is not set to use, CLKOP and CLKOS with 90 degree phase difference need to be provided. (CLKOP, CLKOS, and HS_CLK have same frequency)

In Figure 6-2, one clock lane (HS_CLK) and four data lanes (data_in0, data_in1, data_in2, and data_in3) are used. The signal hs_clk_en and hs_data_en need to be set as high before receiving data_in data.

In the timing diagram. RGB888 type data is transmitted using TX. Therefore, the data types for the four data lanes are the packet head B8, data_type, word_count, ECC, and data, etc.

Figure 6-2 Input Signal Timing of MIPI DPHY TX in HS Mode



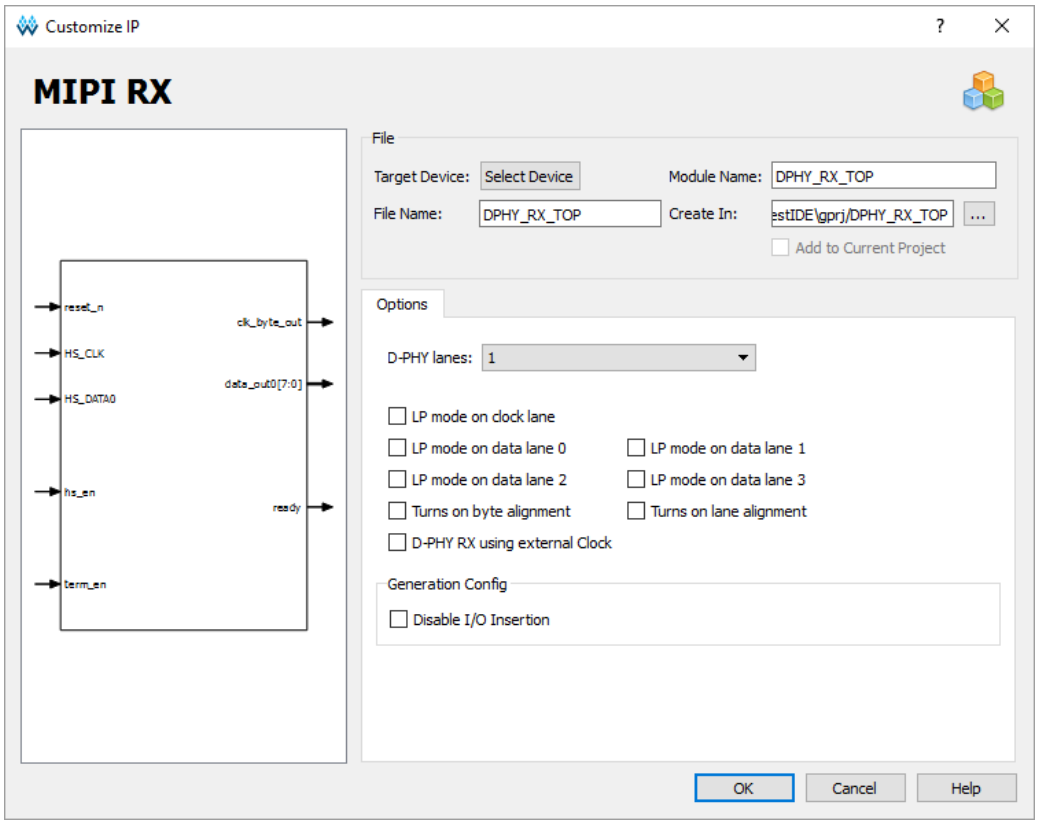
7 MIPI DPHY RX/TX Configuration and Generation

Start "IP Core Generator" from the "Tools" menu in Gowin YunYuan software, and then configure and generate MIPI DPHY RX and MIPI DPHY TX.

7.1 MIPI DPHY RX Configuration

MIPI DPHY RX Configuration is as shown in Figure 7-1.

Figure 7-1 MIPI DPHY RX Configuration



1. Create MIPI DPHY RX file name by modifying "File Name";

2. Create the top module name of MIPI DPHY RX by modifying "Module Name";
3. Configure "Options" to configure the number of HS data lane, the clock and data lane in LP mode, and byte alignment or lane alignment, etc. Table 7-1 lists the detailed options configuration;
4. Only one HS clock lane and one HS clock lane are used by default.

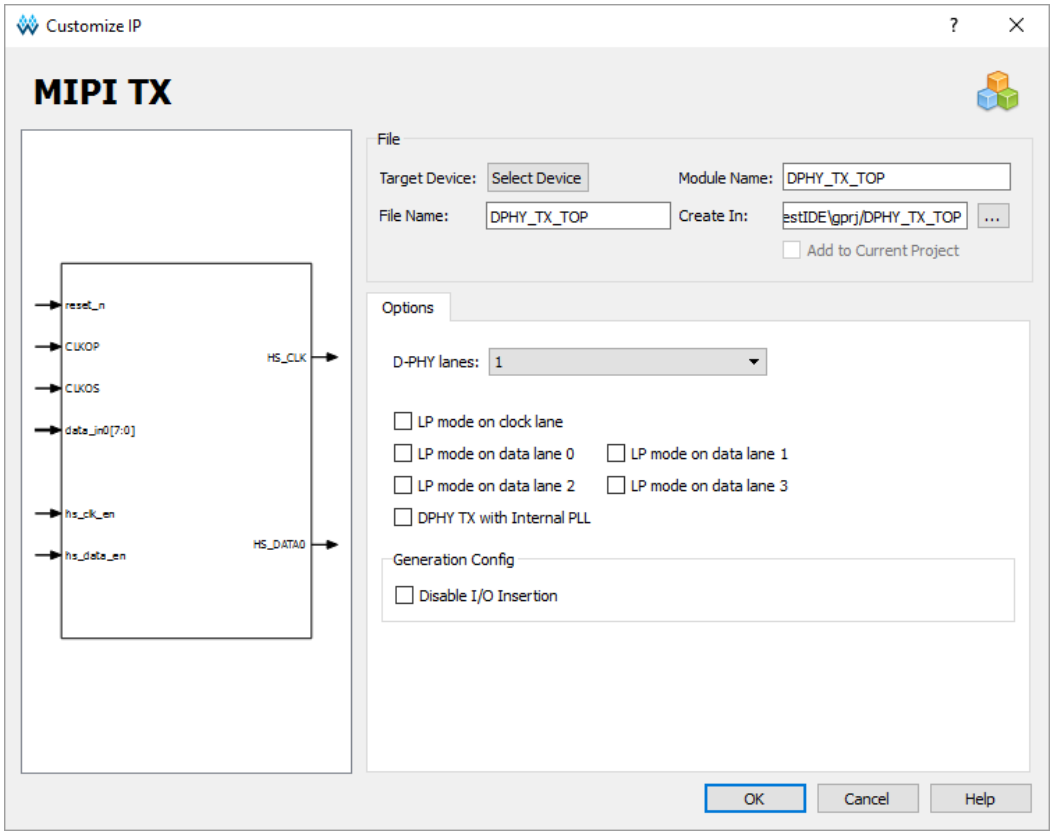
Table 7-1 MIPI DPHY RX Options

Options	Description
D-PHY lanes	1: generates one data lane HS_DATA0;
	2: generates two data lanes HS_DATA0 and HS_DATA1;
	3: generates three data lanes HS_DATA0, HS_DATA1, and HS_DATA2;
	4: generates four data lanes HS_DATA0, HS_DATA1, HS_DATA2, and HS_DATA3.
LP mode on clock lane	Generates LP_CLK[1:0] and the other IO ports for LP mode on clock lane.
LP mode on data lane0	Generates LP_DATA0[1:0] and the other IO ports for LP mode on data lane0.
LP mode on data lane1	Generates LP_DATA1[1:0] and the other IO ports for LP mode on data lane1.
LP mode on data lane2	Generates LP_DATA2[1:0] and the other IO ports for LP mode on data lane2.
LP mode on data lane3	Generates LP_DATA3[1:0] and the other IO ports for LP mode on data lane3.
Turns on byte alignment	Check this option to enable byte alignment, used to align the bytes after deserializing on one lane.
Turns on lane alignment	Check this option to enable lane alignment, used to align different data lanes;
D-PHY RX using cross external Clock	Check this option for RX module to use an external clock (clk_byte), and data_out0/1/2/3 will align at clk_byte.

7.2 MIPI DPHY TX Configuration

MIPI DPHY TX Configuration is as shown in Figure 7-2.

Figure 7-2 MIPI DPHY TX Configuration



1. Create MIPI DPHY TX file name by modifying "File Name";
2. Create the top module name of MIPI DPHY TX by modifying "Module Name";
3. Configure "Options" to configure the number of HS data lane, whether the clock and data lane in LP mode use the internal PLL or not, etc. Table 7-2 lists the detailed options configuration;
4. Only one HS clock lane and one HS clock lane are used by default.

Table 7-2 MIPI DPHY TX Options

Options	Description
D-PHY lanes	1: generates one data lane HS_DATA0;
	2: generates two data lanes HS_DATA0 and HS_DATA1;
	3: generates three data lanes HS_DATA0, HS_DATA1, and HS_DATA2;
	4: generates four data lanes HS_DATA0, HS_DATA1, HS_DATA2, and HS_DATA3.
LP mode on clock lane	Generates LP_CLK[1:0] and the other IO ports for LP mode on clock lane.
LP mode on data lane0	Generates LP_DATA0[1:0] and the other IO ports for LP mode on data lane0.

Options	Description
LP mode on data lane1	Generates LP_DATA1 [1:0] and the other IO ports for LP mode on data lane1.
LP mode on data lane2	Generates LP_DATA2 [1:0] and the other IO ports for LP mode on data lane2
LP mode on data lane3	Generates LP_DATA3 [1:0] and the other IO ports for LP mode on data lane3.
D-PHY TX with Internal PLL	In this mode, TX module will use an internal PLL. The internal PLL will generate a pair of clock with 90 degree phase difference.

8 Reference Designs

This chapter mainly introduces MIPI reference design examples and application. The basic structure for a MIPI DPHY design example is as shown in Figure 8-1. There are two modules in this example --- “Example DPHY RX” and “Example DPHY TX”.

The operating procedures in this design example are as follows:

1. DPHY RX receives MIPI data, and then converts the date into pixel data;
2. Output the data after converted by DPHY TX.

Table 8-1 lists RGB888 data format.

During designs, users can add the other designs between the two modules, such as the "User Design" in this Figure.

In this reference design, MIPI DPHY RX and TX all adopt four data lanes, among which:

1. DPHY RX adopts Word Aligner. Lane Aligner is not used;
2. DPHY TX adopts external clock instead of internal PLL.

Figure 8-1 Structure of MIPI Reference Design Example

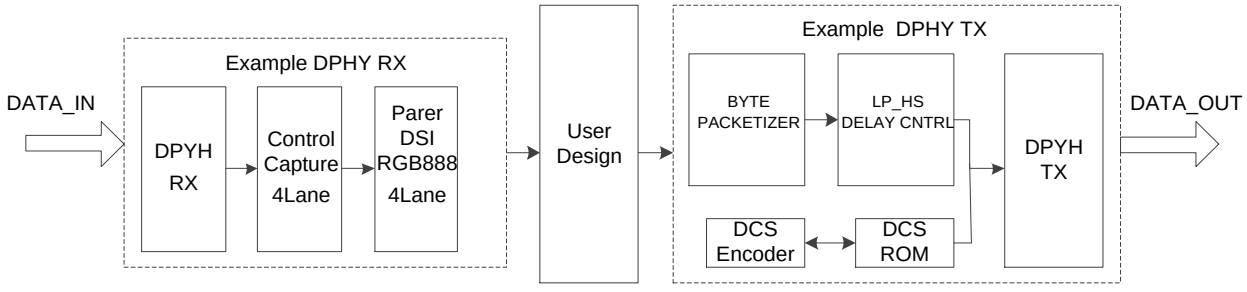


Table 8-1 RGB888 Data Format

Data Type	Format
RGB888	PIXDATA= {R[7:0],G[7:0],B[7:0]}

8.1 Example DPHY RX

This reference design is to receive external data, and then convert the data into RGB888 pixel data after byte alignment. DSI2RGB888_TOP is the top module, and the basic structure is as shown in Figure 8-2. Table 8-2 lists the port definition. The modules functions are as follows:

- MIPI DPHY RX: used for data deserializing and alignment;
- Control Capture 4Lane: used to extract data packet info., judge the packet header, data type, etc., and control the signals VSYNC and HSYNC output;
- Parser DSI RGB888 4Lane: convert MIPI byte data into Pixel Data. MIPI byte data is converted into RGB888 pixel data in this example;
- GW_PLL: used to provide pixel clock and generate the clocks CLKOP and CLKOS.

Figure 8-2 Example DPHY RX Structure View

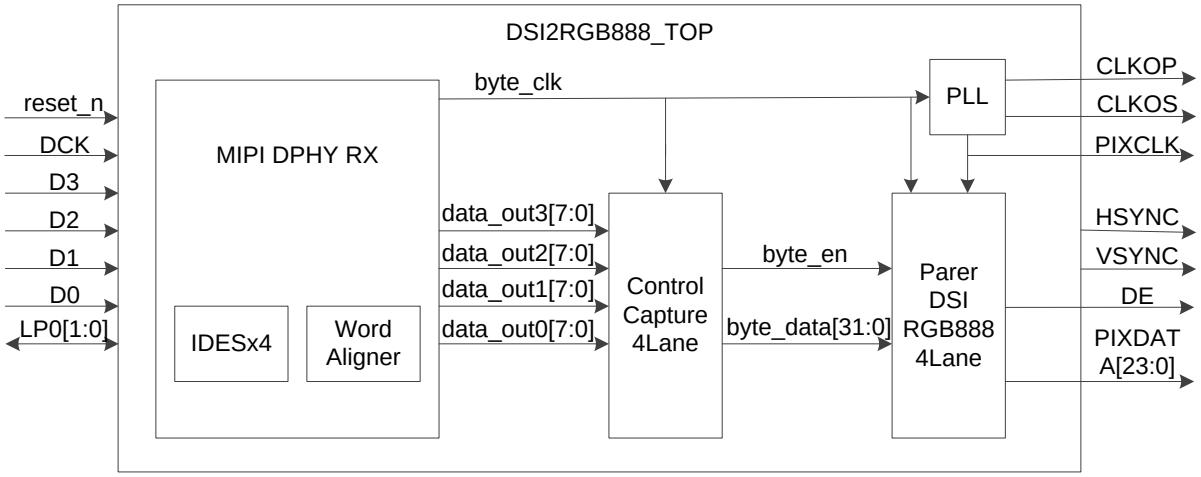


Table 8-2 Example DPHY RX Ports Definition

Signal	I/O	Description
reset_n	Input	Reset signal, active low
DCK	Input	High speed Clock, HS_CLK
D3	Input	High-speed data lane3, HS_DATA3
D2	Input	High-speed data lane2, HS_DATA2
D1	Input	High-speed data lane1, HS_DATA1
D0	Input	High-speed data lane0, HS_DATA0
LP0[1:0]	Bidirectional	LP data lane 0, used to generate the control signal;
PIXCLK_adj	Output	Pixel Data clock;
PIXDATA[23:0]	Output	Pixel Data;
DE	Output	Pixel Data Enable signal;
HSYNC	Output	Horizontal Sync Signal
VSYNC	Output	Vertical Sync Signal
CLKOP	Output	Same frequency with HSCLK

Signal	I/O	Description
CLKOS	Output	Same frequency with HSCLK, 90 degree phase difference with CLKOP;
byte_clk	Output	Byte data clock

8.2 Example DPHY TX

This reference design is to convert RGB888 pixel data into MIPI byte data, packet and deserialize the data, and then output it. RGB8882DSI_TOP is the top module, and the basic structure is as shown in Figure 8-3. Table 8-3 lists the port definition. The modules functions are as follows:

- byte_packetizer: convert pixel data into byte data and add data header, parity bit, and EoTp end of transfer packet in the byte packets;
- LP HS DELAY CNTRL: control the delay between clock lane and data lane when entering or exiting HS mode; control HS data output delay in HS mode;
- MIPI DPHY TX: used for data deserializing;
- DCS Encoder: convert 8bit data into 2bit LP data;
- DCS ROM: ROM controller, generate DCS (Display Command Set) directives used to control and initialize the displayer.

Figure 8-3 Example DPHY TX Structure View

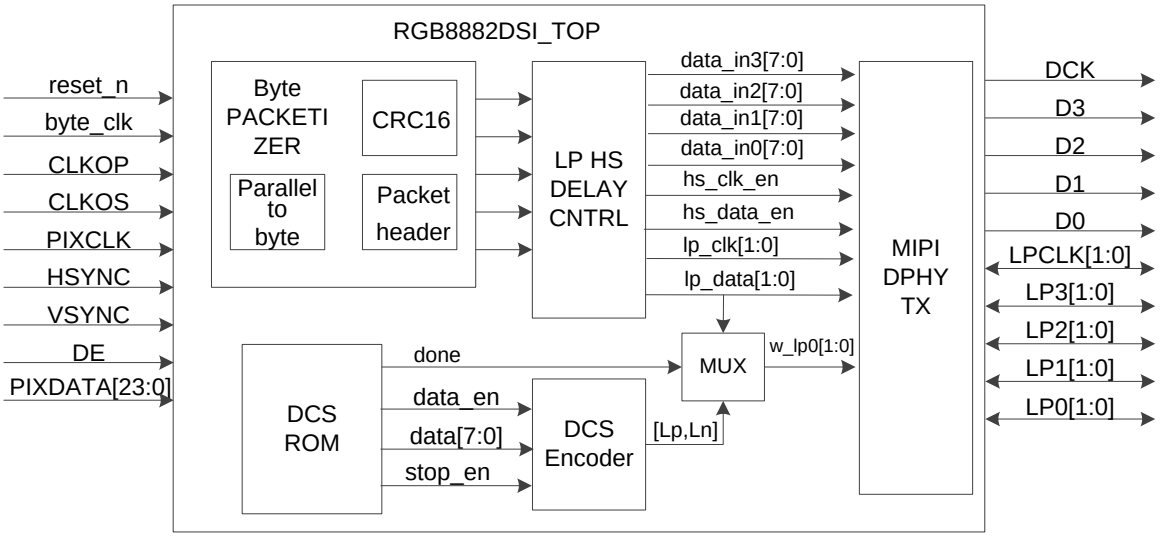


Table 8-3 Example DPHY TX Ports Definition

Signal	I/O	Description
reset_n	Input	Reset signal, active low
PIXCLK_adj	Input	Pixel Data clock
PIXDATA[23:0]	Input	Pixel Data
DE	Input	Pixel Data Enable signal
HSYNC	Input	Horizontal Sync Signal
VSYNC	Input	Vertical Sync Signal
CLKOP	Input	Same frequency with HSCLK
CLKOS	Input	Same frequency with HSCLK, 90 degree phase difference with CLKOP;
byte_clk	Input	Byte data clock
DCK	Output	High speed Clock, HS_CLK

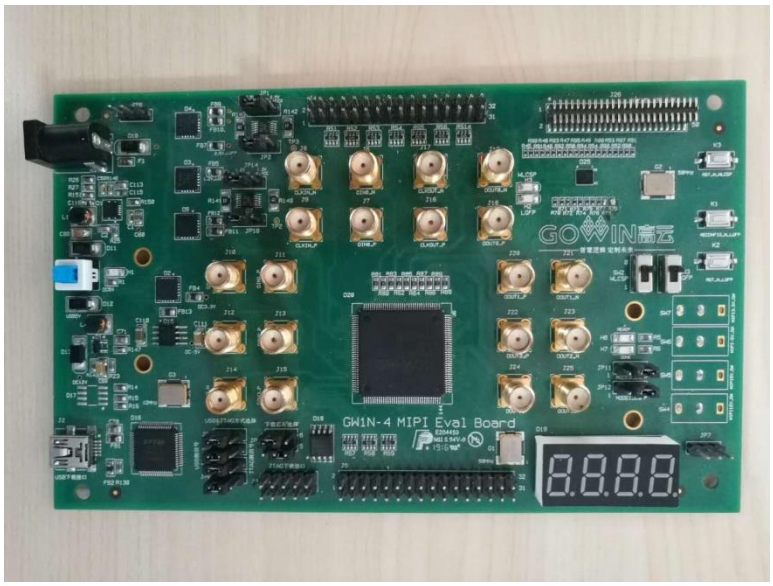
Signal	I/O	Description
D3	Output	High-speed data lane3, HS_DATA3
D2	Output	High-speed data lane2, HS_DATA2
D1	Output	High-speed data lane1, HS_DATA1
D0	Output	High-speed data lane0, HS_DATA0
LPCLK1:0]	Bidirectional	LP clock
LP3[1:0]	Bidirectional	LP data lane3
LP2[1:0]	Bidirectional	LP data lane2
LP1[1:0]	Bidirectional	LP data lane1
LP0[1:0]	Bidirectional	LP data lane0

8.3 Applications

DPHY functions can be verified quickly using this design. If this reference design is implemented in board test, users need to provide proper excitation. Use oscilloscope or Gowin Analyzer Oscilloscope to observe the signal.

The external connection of MIPI DPHY ports should meet LVDS electrical specification and match the corresponding resistance network. For the resistance network, please refer to the structure in Figure 4-1 or Figure 4-2. GOWINSEMI can provide MIPI test board, which allows users to design and test more easily and quickly.

Figure 8-4 GW1N-4 MIPI Test Board

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