EFR32xG25 Wireless Gecko Reference Manual

The EFR32xG25 SoC is an ideal solution for sub-GHz Wi-SUN applications for metering, lighting, and distribution automation.

The high-performance sub-GHz radio provides long range and is not susceptible to 2.4 GHz interference from technologies like Wi-Fi.

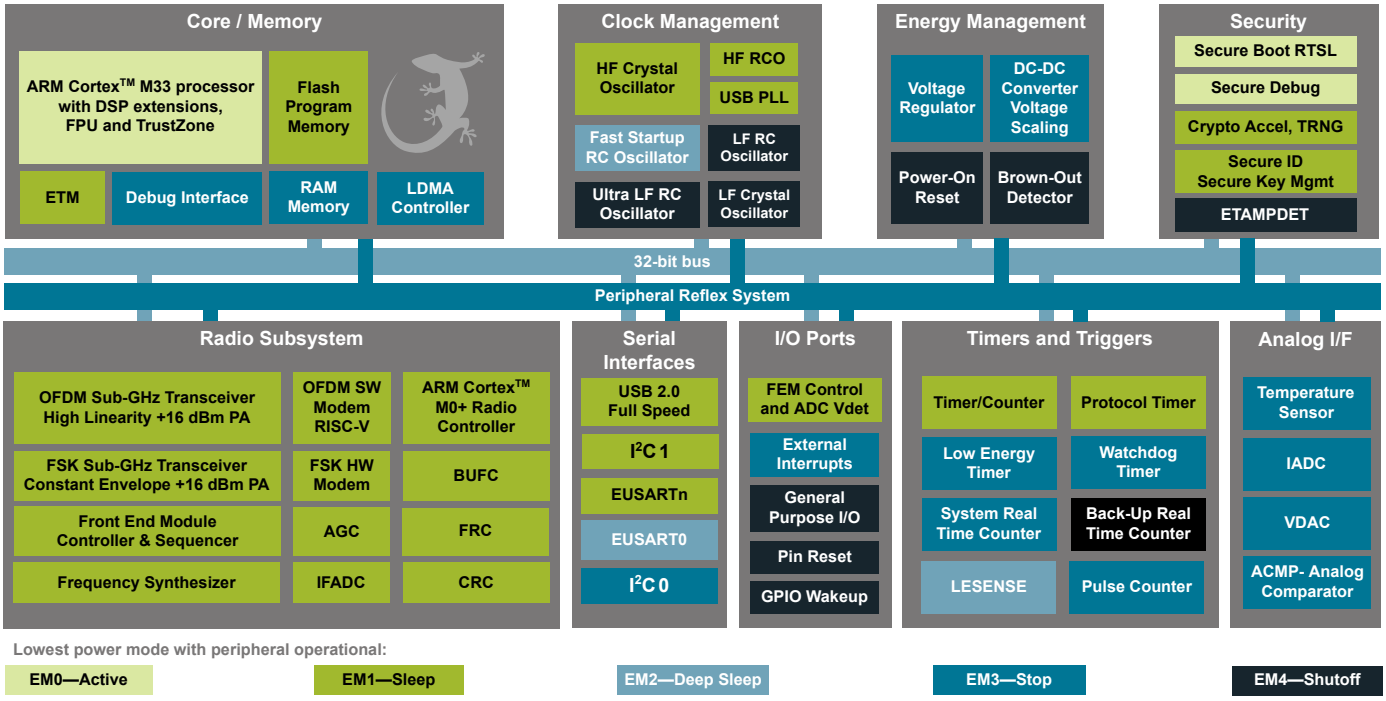
The single die, multi-core solution, provides industry leading security, high throughput, and an integrated power amplifier to enable the next level of secure connectivity for IoT devices.

EFR32xG25 applications include:

- Smart Electric Metering
- Street Lighting
- Distribution automation
- Industrial applications
- Municipal infrastructure

KEY FEATURES

- 32-bit ARM® Cortex®-M33 core with 97.5 MHz maximum operating frequency
- Up to 1920 kB of flash and 512 kB of RAM
- Wi-SUN Multi-rate OFDM, FSK, and O-QPSK modulations
- Integrated PA with up to 16 dBm (Sub-GHz) TX power
- Robust peripheral set and up to 37 GPIO
- Operation up to 125 °C



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1. About This Document

1.1 Introduction

This document contains reference material for the EFR32xG25 devices. All modules and peripherals in the EFR32xG25 devices are described in general terms. Not all modules are present in all devices and the feature set for each device might vary. Such differences, including pinout, are covered in the device data sheets.

1.2 Conventions

Register Names

Register names are given with a module name prefix followed by the short register name:

TIMERn_CTRL - Control Register

The "n" denotes the module number for modules which can exist in more than one instance.

Some registers are grouped which leads to a group name following the module prefix:

GPIO_Px_DOUT - Port Data Out Register

The "x" denotes the different ports.

Bit Fields

Registers contain one or more bit fields which can be 1 to 32 bits wide. Bit fields wider than 1 bit are given with start (x) and stop (y) bit [y:x].

Bit fields containing more than one bit are unsigned integers unless otherwise is specified.

Unspecified bit field settings must not be used, as this may lead to unpredictable behaviour.

Address

The address for each register can be found by adding the base address of the module found in the Memory Map (see Figure 4.1 System Address Space with Core and Code Space Listing on page 46), and the offset address for the register (found in module Register Map).

Access Type

The register access types used in the register descriptions are explained in Table 1.1 Register Access Types on page 32.

Table 1.1. Register Access Types

Access Type	Description
R	Read only. Writes are ignored
RW	Readable and writable
RW1	Readable and writable. Only writes to 1 have effect
W1	Read value undefined. Only writes to 1 have effect
W	Write only. Read value undefined.
RWH	Readable, writable, and updated by hardware
RW(nB), RWH(nB), etc.	"(nB)" suffix indicates that a bitfield explicitly does not support peripheral bit set/clear/toggle operations (see 4. Memory and Bus System)
RW(r), R(r), etc.	"(r)" suffix indicates that reading the register causes an action and may alter the register value.

Number format

0x prefix is used for hexadecimal numbers

0b prefix is used for binary numbers

Numbers without prefix are in decimal representation.

Reserved

Registers and bit fields marked with **reserved** are reserved for future use. These should be written to their reset value unless otherwise stated in the Register Description. Read values for reserved bits may be different in future or prior devices.

Reset Value

The reset value denotes the value after reset.

Registers denoted with X have unknown value out of reset and need to be initialized before use. Note that read-modify-write operations on these registers before they are initialized results in undefined register values.

Pin Connections

Pin connections are given with a module prefix followed by a short pin name:

CMU_CLKOUT1 (Clock management unit, clock output pin number 1)

The location for the pin names given in the module documentation can be found in the device-specific datasheet.

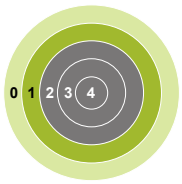
1.3 Related Documentation

Further documentation on the EFR32xG25 devices and the ARM Cortex-M33 can be found at the Silicon Labs and ARM web pages:

www.silabs.com

www.arm.com

2. System Overview





Quick Facts

What?

The EFR32 Wireless Gecko is a highly integrated, configurable and low power wireless System-on-Chip (SoC) with a robust set of MCU and radio peripherals.

Why?

The Radio enables support for protocols in sub-GHz frequency bands while the MCU system allows customized protocols and applications to run efficiently.

How?

Dynamic or fixed packet lengths, optional address recognition, and flexible CRC and security schemes makes the EFR32xG25 ideal for many wireless IoT applications. High performance analog and digital peripherals allow complete applications to run on the EFR32xG25 SoC.

2.1 Introduction

The high level features of EFR32xG25 include:

- High performance radio transceiver
  - Low power consumption in transmit, receive, and standby modes
  - Excellent receiver performance, including sensitivity, selectivity, and blocking
  - Excellent transmitter performance, including programmable output power, low phase noise, and power-amplifier (PA) ramping
- Configurable protocol support, including standards and customer-developed protocols
  - Preamble and frame synchronization insertion in transmit, and recovery in receive
  - Flexible CRC support, including configurable polynomial and multiple CRCs for single data frames
  - Basic address filtering performed in hardware
- High performance, low power MCU system
  - High Performance 32-bit ARM Cortex-M33 CPU
  - Flexible and efficient energy management
  - Complete set of digital peripherals
  - Peripheral Reflex System (PRS)
  - Precision analog peripherals
- Low external component count
  - Integrated tunable crystal loading capacitors
- Security
  - Secure Boot with Root of Trust and Secure Loader (RTSL)
  - Hardware Cryptographic Acceleration with DPA countermeasures for AES128/256, SHA-1, SHA-2 (up to 256-bit), ECC (up to 256-bit), ECDSA, ECDH and J-Pake
  - True Random Number Generator (TRNG) compliant with NIST SP800-90 and AIS-31
  - ARM® TrustZone®
  - Secure Debug with lock/unlock

A further introduction to the MCU and radio system is included in the following sections.

Note: Detailed performance numbers, current consumption, pinout etc. are available in the device datasheets.

2.2 Block Diagrams

The block diagram for the EFR32xG25 System-On-Chip series is shown in (Figure 2.1 EFR32xG25 System-On-Chip Block Diagram on page 36).

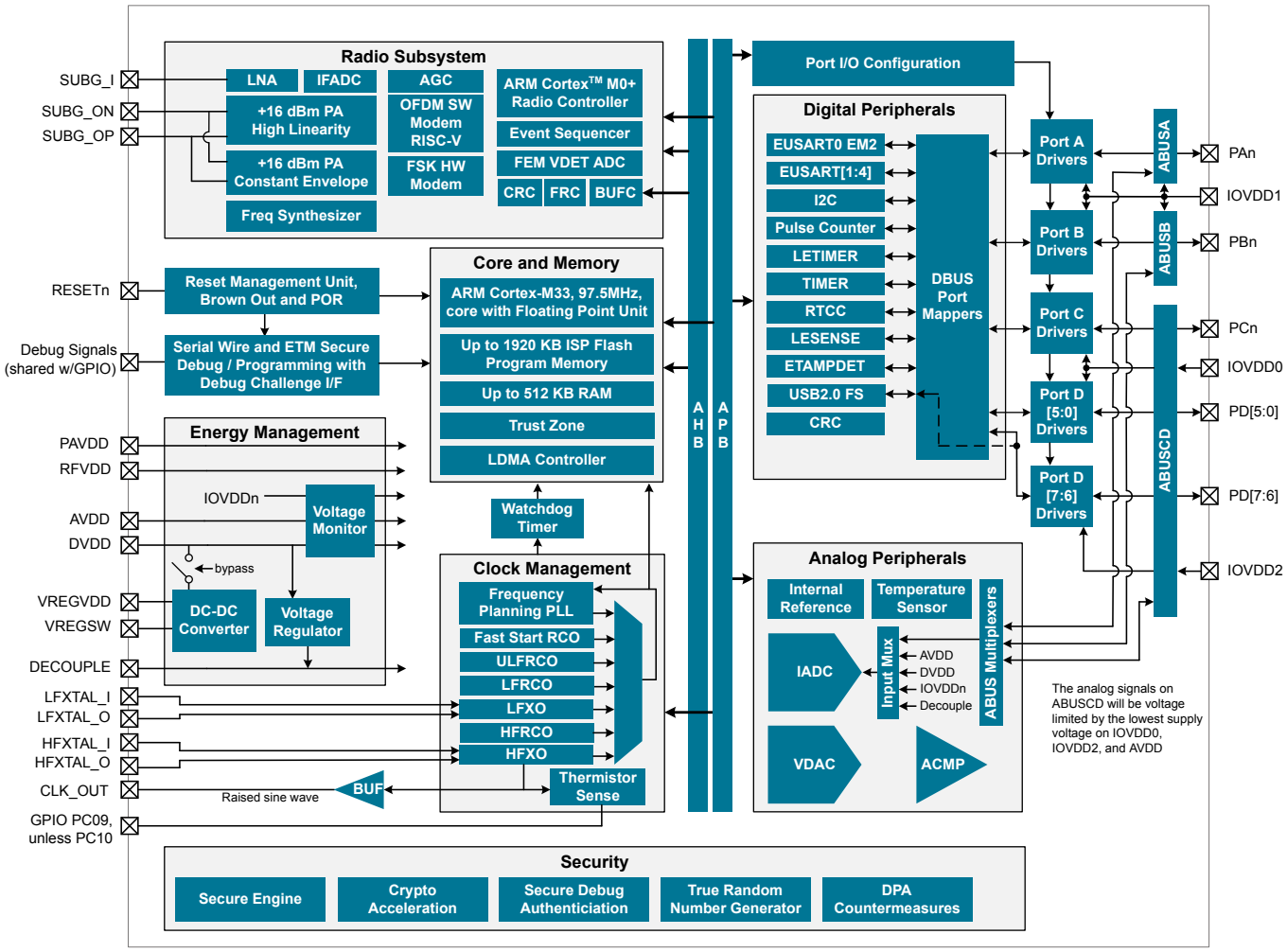


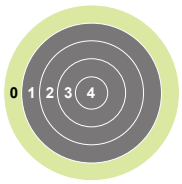
Figure 2.1. EFR32xG25 System-On-Chip Block Diagram

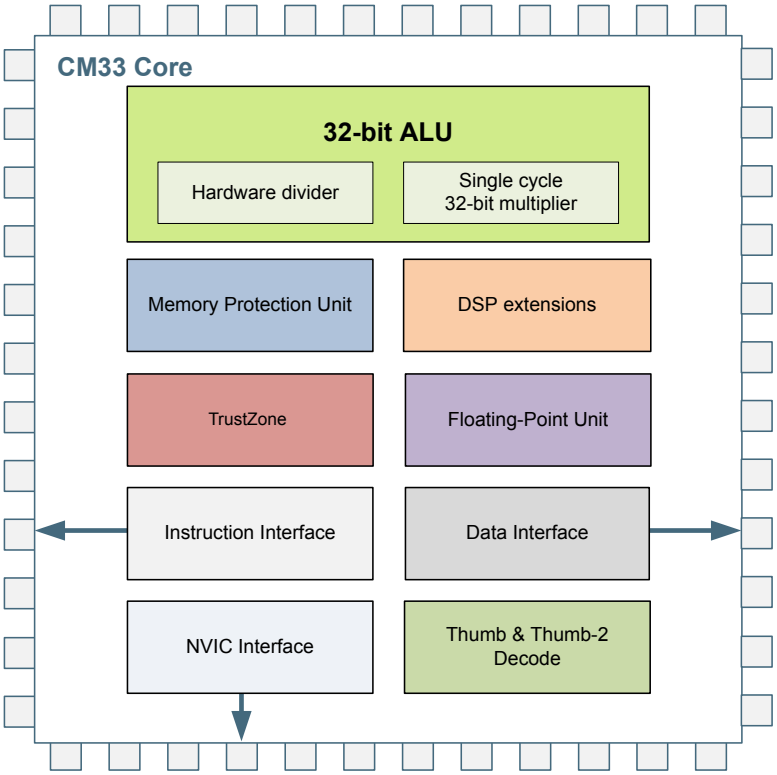
2.3 MCU Features overview

- **ARM Cortex-M33 CPU platform**
  - High Performance 32-bit processor @ up to 97.5 MHz
  - DSP instruction support and floating-point unit
  - Memory Protection Unit
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - Five Energy Modes from EM0 to EM4 provide flexibility between higher performance and low power
  - Power routing configurations including DCDC control
  - Voltage Monitoring and Brown Out Detection
  - Automatic voltage scaling for additional energy savings
  - State Retention
- **Supported Modulation Format**
  - Wi-SUN MR OFDM MCS 0-6 (all 4 Options)
  - Wi-SUN MR O-QPSK with DSSS
  - Wi-SUN FSK
  - 2 (G)FSK with fully configurable shaping
  - (G)MSK
- **Protocol Support**
  - Proprietary
  - Wi-SUN
- **Up to 1920 kB Flash**
- **Up to 512 kB RAM**
- **Up to 37 General Purpose I/O pins**
  - Configurable push-pull, open-drain, pull-up/down, input filter, slew rate
  - Configurable peripheral I/O locations
  - 16 asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- **16 Channel DMA Controller**
  - Alternate/primary descriptors with scatter-gather/ping-pong operation
- **12 Channel Peripheral Reflex System (PRS)**
  - Autonomous inter-peripheral signaling enables smart operation in low energy modes
  - 12 asynchronous channels with configurable logic functionality
  - 4 synchronous channels for high-speed signalling between TIMER, IADC, and VDAC
- **General Purpose Cyclic Redundancy Check (GPCRC)**
  - Programmable 16-bit polynomial, fixed 32-bit polynomial
  - The GPCRC module is in addition to the radio CRC
- **Communication interfaces**
  - 1 × USB2.0 Full Speed Port, Device mode only
  - 5 × Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)
    - UART/SPI/IrDA support
    - High-speed operation in EM0/1 using high-frequency clock source
    - One instance with low-energy operation in EM2 using 32.768 kHz clock source
    - Buffered full/half-duplex operation
    - Hardware flow control
    - 7/8/9 data bits
  - 2 × I^2C Interface (I2C) with SMBus support
    - Address recognition in EM3 Stop Mode

- **Timers/Counters**
  - 2 × 32-bit and 6 × 16-bit Timer/Counters (TIMER)
    - 3 Compare/Capture/PWM channels
    - Dead-Time Insertion
  - 24-bit Low Energy Timer (LETIMER)
  - 32-bit Real-Time Counter (SYSRTC)
  - 32-bit Ultra Low Energy Backup Real Time Counter (BURTC) for periodic wake-up from any Energy Mode
  - 16-bit Pulse Counter
    - Asynchronous pulse counting/quadrature decoding
  - 2 × Watchdog Timer (WDOG)
- **Ultra low power precision analog peripherals**
  - Incremental Analog to Digital Converter (IADC) with 12-bit resolution at 1 Msps and 16-bit resolution at 76.9 ksps
    - Single ended or differential operation
    - Conversion tailgating for predictable latency
  - 12-bit 500 ksps Digital to Analog Converter (VDAC)
    - 2 single ended channels/1 differential channel
  - 2 × Analog Comparator (ACMP)
    - Programmable speed/current
  - Analog Bus (ABUS) signal routing
  - Accurate die temperature sensor
  - External thermistor interface
- **Low-energy sensor interface**
  - Autonomous sensor monitoring in deep sleep mode
  - Wide range of supported sensors, including LC sensors and capacitive touch switches
- **Ultra efficient Power-on Reset (POR) and Brown-Out Detector (BOD)**
- **Debug Interface**
  - 4-pin Joint Test Action Group (JTAG) interface
  - 2-pin serial-wire debug (SWD) interface
  - Embedded Trace (ETM) interface with 4 data lines
- **Security**
  - Secure Boot with Root of Trust and Secure Loader (RTSL)
    - Prevents malware injection and rollback
    - Ensures authentic firmware execution and OTA updates
  - Dedicated Secure Core
    - Delivers faster, more energy efficient hardware crypto with Differential Power Analysis (DPA) countermeasures for AES128/256, SHA-1, SHA-2 (up to 256-bit), ECC (up to 256-bit), ECDSA, ECDH and J-Pake
    - Provides isolation with the application core
    - Provides hardware cryptographic acceleration
    - True Random Number Generator (TRNG) compliant with NIST SP800-90 and AIS-31
  - ARM® TrustZone®
  - Secure Debug with lock/unlock
    - Allows authenticated access for enhanced Failure Analysis (FA)

3. System Processor





Quick Facts

What?

The EFR32xG25 features the industry leading Cortex-M33 CPU from ARM.

Why?

The ARM Cortex-M33 is designed for exceptionally short response time, high code density, and high 32-bit throughput while maintaining a strict cost and power consumption budget.

How?

Combined with the ultra low energy peripherals available in EFR32xG25 devices, the Cortex-M33 processor's Harvard architecture, 3 stage pipeline, single cycle instructions, Thumb-2 instruction set support, and fast interrupt handling make it perfect for 8-bit, 16-bit, and 32-bit applications.

3.1 Introduction

The ARM Cortex-M33 32-bit RISC processor provides outstanding computational performance and exceptional system response to interrupts while meeting low cost requirements and low power consumption.

The ARM Cortex-M33 implemented is revision r1p0.

3.2 Features

- Harvard architecture
  - Separate data and program memory buses (No memory bottleneck as in a single bus system)
- 3-stage pipeline
- Thumb-2 instruction set
  - Enhanced levels of performance, energy efficiency, and code density
- Single cycle multiply and hardware divide instructions
  - 32-bit multiplication in a single cycle
  - Signed and unsigned divide operations between 2 and 11 cycles
- 1.5 DMIPS/MHz
- TrustZone
  - Independent Secure and Privileged states
  - Accelerated context switching
- 16 Region MPU
- 24-bit System Tick Timer for Real Time OS
- Excellent 32-bit migration choice for 8/16 bit architecture based designs
  - Simplified stack-based programmer's model is compatible with traditional ARM architecture and retains the programming simplicity of legacy 8-bit and 16-bit architectures
- Aligned or unaligned data storage and access
  - Contiguous storage of data requiring different byte lengths
  - Data access in a single core access cycle
- Integrated power modes
  - Sleep Now mode for immediate transfer to low power state
  - Sleep on Exit mode for entry into low power state after the servicing of an interrupt
  - Ability to extend power savings to other system components
- Optimized for low latency, nested interrupts

3.3 Functional Description

For a full functional description of the ARM Cortex-M33 implementation in the EFR32xG25 family, the reader is referred to the ARM Cortex-M33 documentation.

3.3.1 Interrupt Operation

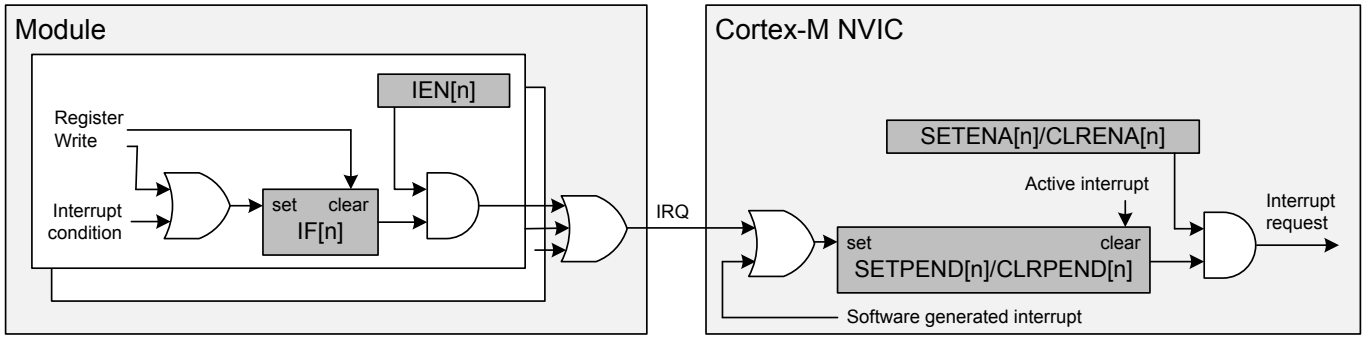


Figure 3.1. Interrupt Operation

The interrupt request (IRQ) lines are connected to the Cortex-M33. Each of these lines (shown in 3.3.3 Interrupt Request Lines (IRQ)) is connected to one or more interrupt flags in one or more modules. The interrupt flags are set by hardware on an interrupt condition. It is also possible to set/clear the interrupt flags through the IF register interface. When setting or clearing and interrupt through the IF register use of the IF_SET or IF_CLR bit operation registers is required; directly writing the main interrupt flag register will have no effect.

Each interrupt flag is then qualified with its own interrupt enable bit (IEN register), before being OR'ed with the other interrupt flags to generate the IRQ. A high IRQ line will set the corresponding pending bit (can also be set/cleared with the SETPEND/CLRPEND bits in ISPRn/ICPRn) in the Cortex-M33 NVIC. The pending bit is then qualified with an enable bit (set/cleared with SETENA/CLRENA bits in ISERn/ICERn) before generating an interrupt request to the core. Figure 3.1 Interrupt Operation on page 41 illustrates the interrupt system. For more information on how the interrupts are handled inside the Cortex-M33, the reader is referred to the **ARM Cortex-M33 Processor Technical Reference Manual**.

3.3.1.1 Avoiding Extraneous Interrupts

There can be latencies in the system such that clearing an interrupt flag could take longer than leaving an Interrupt Service Routine (ISR). This can lead to the ISR being re-entered as the interrupt flag has yet to clear immediately after leaving the ISR. To avoid this, when clearing an interrupt flag at the end of an ISR, the user should execute ARM's Data Synchronization Barrier (DSB) instruction. Another approach is to clear the interrupt flag immediately after identifying the interrupt source and then service the interrupt as shown in the pseudo-code below. The ISR typically is sufficiently long to more than cover the few cycles it may take to clear the interrupt status, and also allows the status to be checked for further interrupts before exiting the ISR.

```
irqXServiceRoutine() {
   do {
      clearIrqXStatus();
      serviceIrqX();
   } while(irqXStatusIsActive());
}
```

3.3.2 TrustZone

The Cortex-M33 implements ARM TrustZone which provides the ability to restrict access to peripherals and memory regions based on the CPU security attribute. TrustZone works in combination which the MPU which controls privileged/unprivileged execution of code to provide a full security solution. The Security Management Unit (SMU) is used to configure access restrictions in the various modes. Refer to 10. SMU - Security Management Unit for more information.

For information about TrustZone features in the core or information on TrustZone specific instructions please see the ARM Cortex-M33 Processor Technical Reference Manual provided by ARM

3.3.3 Interrupt Request Lines (IRQ)

This table shows all IRQ's for the system processor. M33 High Speed interrupts are indicated by an '*'.

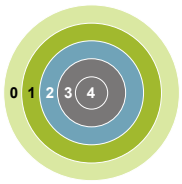
See the individual peripheral chapters for more information on interrupt function.

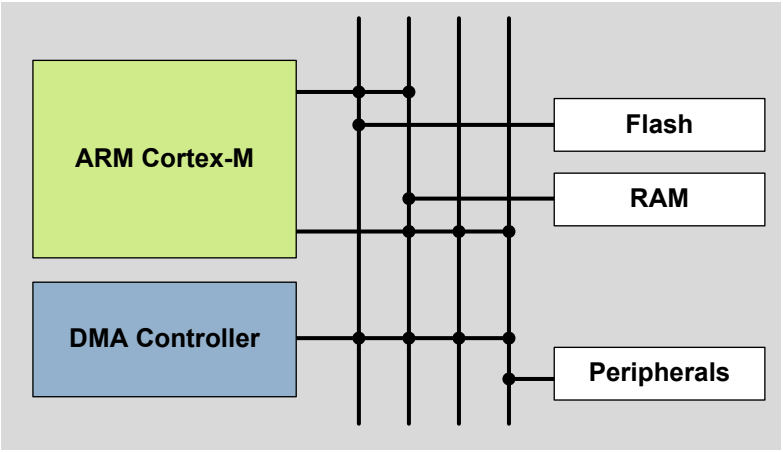
IRQ #	Name
0*	SMU_SECURE
1*	SMU_S_PRIVILEGED
2*	SMU_NS_PRIVILEGED
3*	EMU
4*	TIMER0
5*	TIMER1
6*	TIMER2
7*	TIMER3
8*	ETAMPDET
9*	TIMER4
10*	TIMER5
11*	TIMER6
12*	TIMER7
13*	EUSART0_RX
14*	EUSART0_TX
15*	EUSART1_RX
16*	EUSART1_TX
17*	EUSART2_RX
18*	EUSART2_TX
19*	EUSART3_RX
20*	EUSART3_TX
21*	EUSART4_RX
22*	EUSART4_TX
23*	ICACHE0
24*	BURTC
25*	LETIMER0
26*	SYSCFG
27*	MPAHBRAM
28*	LDMA
29*	LFXO
30*	LFRCO
31*	ULFRCO
32*	GPIO_ODD
33*	GPIO_EVEN

IRQ #	Name
34*	I2C0
35*	I2C1
36*	EMUDG
37*	AGC
38*	BUFC
39*	FRC_PRI
40*	FRC
41*	MODEM
42*	PROTIMER
43*	RAC_RSM
44*	RAC_SEQ
45*	HOSTMAILBOX
46*	SYNTH
47*	ACMP0
48*	ACMP1
49*	WDOG0
50*	WDOG1
51*	HFXO0
52*	HFRCO0
53*	HFRCOEM23
54*	CMU
55*	AES
56*	IADC
57*	MSC
58*	DPLL0
60*	DCDC
61*	VDAC
62*	PCNT0
63*	USB
64*	SW0
65*	SW1
66*	SW2
67*	SW3
68*	KERNEL0
69*	KERNEL1
70*	M33CTI0
71*	M33CTI1

IRQ #	Name
72*	FPUEXH
73*	SETAMPERHOST
74*	SEMBRX
75*	SEMBTX
76*	LESENSE
77*	SYSRTC_APP
78*	SYSRTC_SEQ
79*	RFECA0
80*	RFECA1
81*	RFFPLL
82*	USBPLL0
83*	AHB2AHB0
84*	AHB2AHB1
85*	AHB2AHB2
86*	AHB2AHB3
87*	RFTIMER
88*	SOFTM
89*	RFLDMA

4. Memory and Bus System





Quick Facts

What?

A low latency memory system including low energy Flash and RAM with data retention which makes the low energy modes attractive.

Why?

RAM retention reduces the need for storing data in Flash and enables frequent use of the ultra low energy modes EM2 and EM3.

How?

Low energy and non-volatile Flash memory stores program and application data in all energy modes and can easily be reprogrammed in system. Low leakage RAM with data retention in EM0 to EM3 removes the data restore time penalty, and the DMA ensures fast autonomous transfers with predictable response time.

4.1 Introduction

The EFR32xG25 contains a set of AMBA buses which move data between peripherals, memory, and the CPU. All memories and register interfaces are memory mapped into a unified address space.

4.2 Functional Description

The internal memory segments of the Cortex-M33 are mapped into the system memory map as shown by Figure 4.1 System Address Space with Core and Code Space Listing on page 46.

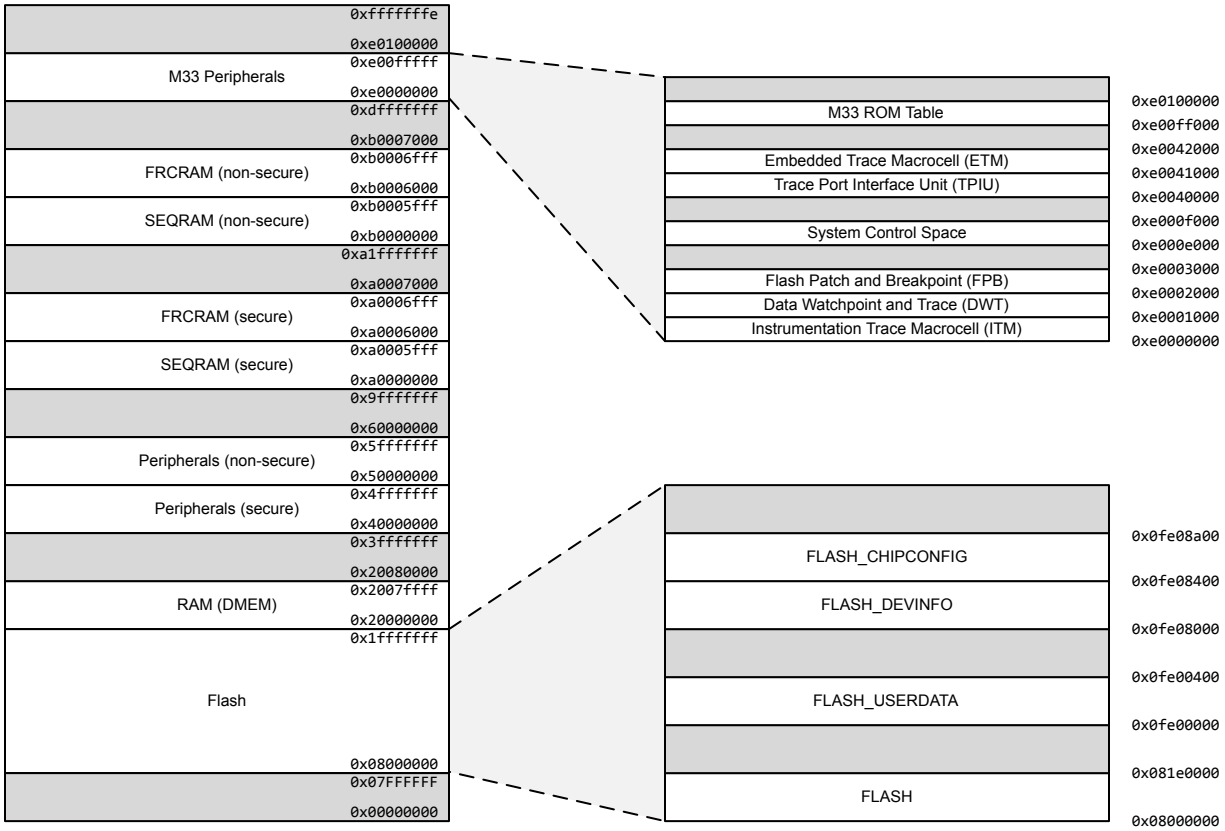


Figure 4.1. System Address Space with Core and Code Space Listing

Flash for the main program memory (CODE) is located at address 0x08000000 in the memory map of the EFR32xG25. Flash memory also contains a USERDATA area intended for user-defined data storage, the DEVINFO space with device characteristics and identifying information, and CHIPCONFIG with internal production test and calibration information.

SRAM for the main data memory (RAM) is located at address 0x20000000 in the memory map of the EFR32xG25. When running code located in RAM, the Cortex-M33 uses the System bus interface to fetch instructions. This results in reduced performance as the Cortex-M33 accesses stack, other data in SRAM and peripherals using the System bus interface.

The Sequencer RAM (SEQRAM) is located at address 0xA0000000 and is used by the Sequencer for both instructions and data. This RAM is also available for general use if not required by the RF subsystem.

4.2.1 Bus Matrix

A multilayer AMBA AHB bus matrix connects the manager bus interfaces to the AHB subordinates. The bus matrix allows several AHB subordinates to be accessed simultaneously. An AMBA APB interface is used for the peripherals, which are accessed through an AHB-to-APB bridge connected to the AHB bus matrix.

The CPU has two AHB bus managers (Code and System) so that it may retrieve instructions and data in parallel. The Code manager is used to access all memory below address 0x20000000 and the System manager access addresses 0x20000000 and above.

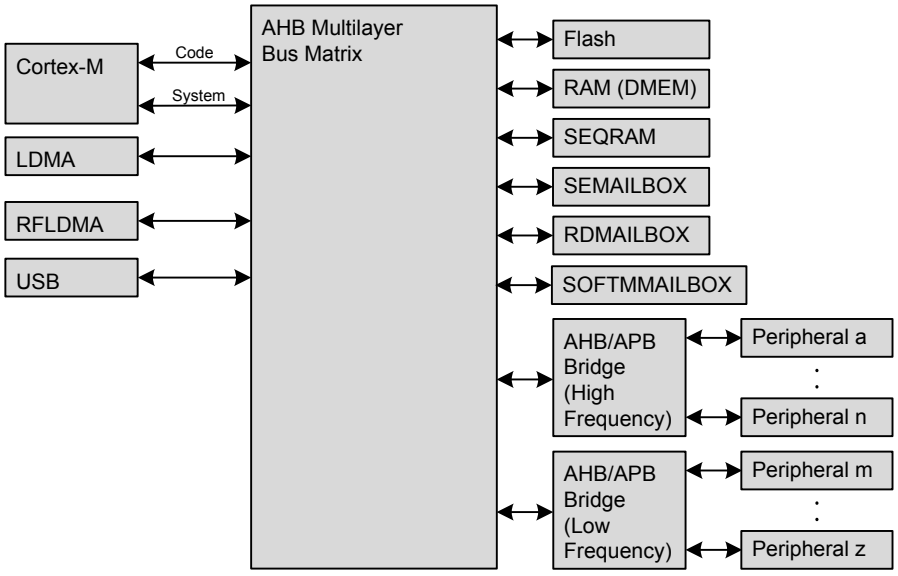


Figure 4.2. EFR32xG25 Bus System

4.2.1.1 Arbitration

The Bus Matrix uses a round-robin arbitration algorithm which enables high throughput and low latency, while starvation of simultaneous accesses to the same bus subordinate are eliminated. Round-robin does not assign a fixed priority to each bus manager. The arbiter does not insert any bus wait-states during peak interaction. However, one wait state is inserted for manager accesses occurring after a prolonged inactive time. This wait state allows for increased power efficiency during manager idle time.

4.2.1.2 Bus Faults

System accesses from the core can receive a bus fault in the following condition(s):

- The core attempts to access an address that is not assigned to any peripheral or other system device. These faults can be enabled or disabled by setting the ADDRFAULTEN bit in the SYSCFG_CTRL register.
- The core attempts to access a peripheral register that is LOCKED.
- The core attempts to access a peripheral or system device that has its clock disabled. This fault can be enabled or disabled by setting the ADDRFAULTEN bit in the SYSCFG_CTRL register.
- System RAM controller or RADIO RAM controller detects a 2bit ECC error. These faults can be enabled or disabled by setting the RAMECCERRFAULTEN bit in the SYSCFG_CTRL register.
- Registers with synchronization requirements may generate bus faults if accessed incorrectly. See 4.2.4.4 Peripheral Access Performance for more details on register access types. In particular the following actions can cause bus faults:
  - Config register written while peripheral enabled.
  - Sync register written while peripheral disabled.
  - LfSync register written while a previous write is pending.
  - Peripheral disabled while any LfSync write is pending.
  - Peripheral registers written or module re-enabled while DISABLING is set.
  - Peripheral registers other than write-only fields or SWRST read while RESETTING is set.
  - Peripheral registers other than read-only fields (including SWRST) written while RESETTING is set.

In addition to any condition-specific bus fault control bits, the bus fault interrupt itself can be enabled or disabled in the same way as all other internal core interrupts.

4.2.2 Flash

The Flash retains data in any state and typically stores the application code and special user data. The Flash memory is typically programmed through the debug interface, but can also be erased and written to from software.

- Up to 1920 kB of memory
- Page size of 8 KB (minimum erase unit)
- Minimum 10k erase cycles endurance
- Greater than 10 years data retention at 85°C
- Lock registers for memory protection
- Data retention in any state

4.2.3 SRAM

The primary task of the SRAM memory is to store application data. Additionally, it is possible to execute instructions from SRAM, and the DMA may be set up to transfer data between the SRAM, Flash and peripherals.

The device contains several blocks of SRAM for various purposes including general data memory (RAM) and various RF subsystem rams (SEQRAM, FRCRAM). For more detailed information see 6. MSC - Memory System Controller .

- Up to 512 kB of memory (RAM)
- RAM blocks may be powered down when not in use
- Data retention of the entire memory or selected banks in EM2 and EM3

4.2.4 Peripherals

The peripherals are mapped into the peripheral memory segment, each with a fixed size address range shown in the 4.2.4.1 Peripheral Map

4.2.4.1 Peripheral Map

This table shows the address range for each peripheral. In addition it shows the lowest energy mode in which the peripheral is powered. Note that EM3 is defined as EM2 with all clocks disabled. Therefore all peripherals powered in EM2 are also powered in EM3 but may not function if they require a running clock.

See the individual peripheral chapters for more information on low power operation.

Address Range	Module Name	Power Domain
0x40000000 - 0x40003FFF	SCRATCHPAD	EM1
0x40004000 - 0x40007FFF	EMU	EM2 (PD0A)
0x40008000 - 0x4000BFFF	CMU	EM2 (PD0B)
0x40010000 - 0x40013FFF	HFRCO0	EM1
0x40018000 - 0x4001BFFF	FSRCO	EM2 (PD0A)
0x4001C000 - 0x4001FFFF	DPLL0	EM1
0x40020000 - 0x40023FFF	LFXO	EM4
0x40024000 - 0x40027FFF	LFRCO	EM4
0x40028000 - 0x4002BFFF	ULFRCO	EM4
0x40030000 - 0x40033FFF	MSC	EM1
0x40034000 - 0x40037FFF	ICACHE0	EM1
0x40038000 - 0x4003BFFF	PRS	EM2 (PD0E)
0x4003C000 - 0x4003FFFF	GPIO	EM2 (PD0B)
0x40040000 - 0x40043FFF	LDMA	EM1
0x40044000 - 0x40047FFF	LDMAXBAR	EM1
0x40048000 - 0x4004BFFF	TIMER0	EM1
0x4004C000 - 0x4004FFFF	TIMER1	EM1
0x40050000 - 0x40053FFF	TIMER2	EM1
0x40054000 - 0x40057FFF	TIMER3	EM1
0x40058000 - 0x4005BFFF	TIMER4	EM1
0x4005C000 - 0x4005FFFF	TIMER5	EM1
0x40060000 - 0x40063FFF	TIMER6	EM1
0x40064000 - 0x40067FFF	TIMER7	EM1
0x4006C000 - 0x4006FFFF	BURTC	EM4
0x40070000 - 0x40073FFF	I2C1	EM1
0x40078000 - 0x4007BFFF	SYSCFG	EM1
0x4007C000 - 0x4007FFFF	SYSCFG	EM1
0x40080000 - 0x40083FFF	BURAM	EM4
0x40088000 - 0x4008BFFF	GPCRC	EM1
0x40094000 - 0x40097FFF	DCDC	EM2 (PD0B)
0x40098000 - 0x4009BFFF	HOSTMAILBOX	EM1
0x400A0000 - 0x400A3FFF	EUSART1	EM1
0x400A4000 - 0x400A7FFF	EUSART2	EM1

Address Range	Module Name	Power Domain
0x400A8000 - 0x400ABFFF	EUSART3	EM1
0x400AC000 - 0x400AFFFF	EUSART4	EM1
0x400B0000 - 0x400B3FFF	SYSRTC0	EM2 (PD0A)
0x400C0000 - 0x400C3FFF	DMEM	EM1
0x400C4000 - 0x400C7FFF	PFMXPPRF	EM1
0x400C8000 - 0x400CBFFF	RFFPLL0	EM1
0x400D0000 - 0x400D3FFF	ETAMPDET	EM4
0x42000000 - 0x42003FFF	BUFC	EM1
0x44000000 - 0x440007FF	RADIOAES	EM1
0x44008000 - 0x4400BFFF	SMU	EM1
0x4400C000 - 0x4400FFFF	SMU	EM1
0x46000000 - 0x4603FFFF	USBAHB	EM1
0x47000000 - 0x47003FFF	USB	USB
0x47004000 - 0x47007FFF	USBPLL0	USB
0x49000000 - 0x49003FFF	LETIMER0	EM2 (PD0B)
0x49004000 - 0x49007FFF	IADC0	EM2 (PD0B)
0x49008000 - 0x4900BFFF	ACMP0	EM2 (PD0B)
0x4900C000 - 0x4900FFFF	ACMP1	EM2 (PD0B)
0x49024000 - 0x49027FFF	VDAC0	EM2 (PD0B)
0x49030000 - 0x49033FFF	PCNT0	EM2 (PD0B)
0x49038000 - 0x4903BFFF	LESENSE	EM2 (PD0B)
0x4A000000 - 0x4A003FFF	HFRCOEM23	EM2 (PD0C)
0x4A004000 - 0x4A007FFF	HFXO0	EM2 (PD0C)
0x4B000000 - 0x4B003FFF	I2C0	EM2, (PD0D)
0x4B004000 - 0x4B007FFF	WDOG0	EM2, (PD0D)
0x4B008000 - 0x4B00BFFF	WDOG1	EM2, (PD0D)
0x4B010000 - 0x4B013FFF	EUSART0	EM2, (PD0D)
0x4C000000 - 0x4C00007F	SEMAILBOX	EM1
0x50000000 - 0x50003FFF	SCRATCHPAD_NS	EM1
0x50004000 - 0x50007FFF	EMU_NS	EM2 (PD0A)
0x50008000 - 0x5000BFFF	CMU_NS	EM2 (PD0B)
0x50010000 - 0x50013FFF	HFRCO0_NS	EM1
0x50018000 - 0x5001BFFF	FSRCO_NS	EM2 (PD0A)
0x5001C000 - 0x5001FFFF	DPLL0_NS	EM1
0x50020000 - 0x50023FFF	LFXO_NS	EM4
0x50024000 - 0x50027FFF	LFRCO_NS	EM4
0x50028000 - 0x5002BFFF	ULFRCO_NS	EM4

Address Range	Module Name	Power Domain
0x50030000 - 0x50033FFF	MSC_NS	EM1
0x50034000 - 0x50037FFF	ICACHE0_NS	EM1
0x50038000 - 0x5003BFFF	PRS_NS	EM2 (PD0E)
0x5003C000 - 0x5003FFFF	GPIO_NS	EM2 (PD0B)
0x50040000 - 0x50043FFF	LDMA_NS	EM1
0x50044000 - 0x50047FFF	LDMAXBAR_NS	EM1
0x50048000 - 0x5004BFFF	TIMER0_NS	EM1
0x5004C000 - 0x5004FFFF	TIMER1_NS	EM1
0x50050000 - 0x50053FFF	TIMER2_NS	EM1
0x50054000 - 0x50057FFF	TIMER3_NS	EM1
0x50058000 - 0x5005BFFF	TIMER4_NS	EM1
0x5005C000 - 0x5005FFFF	TIMER5_NS	EM1
0x50060000 - 0x50063FFF	TIMER6_NS	EM1
0x50064000 - 0x50067FFF	TIMER7_NS	EM1
0x5006C000 - 0x5006FFFF	BURTC_NS	EM4
0x50070000 - 0x50073FFF	I2C1_NS	EM1
0x50078000 - 0x5007BFFF	SYSCFG_NS	EM1
0x5007C000 - 0x5007FFFF	SYSCFG_NS	EM1
0x50080000 - 0x50083FFF	BURAM_NS	EM4
0x50088000 - 0x5008BFFF	GPCRC_NS	EM1
0x50094000 - 0x50097FFF	DCDC_NS	EM2 (PD0B)
0x50098000 - 0x5009BFFF	HOSTMAILBOX_NS	EM1
0x500A0000 - 0x500A3FFF	EUSART1_NS	EM1
0x500A4000 - 0x500A7FFF	EUSART2_NS	EM1
0x500A8000 - 0x500ABFFF	EUSART3_NS	EM1
0x500AC000 - 0x500AFFFF	EUSART4_NS	EM1
0x500B0000 - 0x500B3FFF	SYSRTC0_NS	EM2 (PD0A)
0x500C0000 - 0x500C3FFF	DMEM_NS	EM1
0x500C4000 - 0x500C7FFF	PFMXPPRF_NS	EM1
0x500C8000 - 0x500CBFFF	RFFPLL0_NS	EM1
0x500D0000 - 0x500D3FFF	ETAMPDET_NS	EM4
0x52000000 - 0x52003FFF	BUFC_NS	EM1
0x54000000 - 0x540007FF	RADIOAES_NS	EM1
0x54008000 - 0x5400BFFF	SMU_NS	EM1
0x5400C000 - 0x5400FFFF	SMU_NS	EM1
0x56000000 - 0x5603FFFF	USBAHB_NS	EM1
0x57000000 - 0x57003FFF	USB_NS	USB

Address Range	Module Name	Power Domain
0x57004000 - 0x57007FFF	USBPLL0_NS	USB
0x59000000 - 0x59003FFF	LETIMER0_NS	EM2 (PD0B)
0x59004000 - 0x59007FFF	IADC0_NS	EM2 (PD0B)
0x59008000 - 0x5900BFFF	ACMP0_NS	EM2 (PD0B)
0x5900C000 - 0x5900FFFF	ACMP1_NS	EM2 (PD0B)
0x59024000 - 0x59027FFF	VDAC0_NS	EM2 (PD0B)
0x59030000 - 0x59033FFF	PCNT0_NS	EM2 (PD0B)
0x59038000 - 0x5903BFFF	LESENSE_NS	EM2 (PD0B)
0x5A000000 - 0x5A003FFF	HFRCOEM23_NS	EM2 (PD0C)
0x5A004000 - 0x5A007FFF	HFXO0_NS	EM2 (PD0C)
0x5B000000 - 0x5B003FFF	I2C0_NS	EM2, (PD0D)
0x5B004000 - 0x5B007FFF	WDOG0_NS	EM2, (PD0D)
0x5B008000 - 0x5B00BFFF	WDOG1_NS	EM2, (PD0D)
0x5B010000 - 0x5B013FFF	EUSART0_NS	EM2, (PD0D)
0x5C000000 - 0x5C00007F	SEMAILBOX_NS	EM1

Note:

1. Peripherals listed as being in EM2 (PD0A) always remain powered in EM2 and EM3. Other EM2 power domains (PD0B, PD0C, etc.) are powered down in EM2 and EM3 if all peripherals on that domain are unused.

4.2.4.2 Peripheral non-word access behavior

When writing to peripheral registers, all accesses are treated as 32-bit accesses. This means that writes to a register need to be large enough to cover all bits of register, otherwise, any uncovered bits may become corrupted from the partial-word transfer. Thus, the safest practice is to always do 32-bit writes to peripheral registers.

When reading, there is generally no issue with partial word accesses, however, note that any read action (e.g. FIFO popping) will be triggered regardless of whether the actual FIFO bit-field was included in the transfer size.

4.2.4.3 Peripheral Bit Set and Clear

The EFR32xG25 supports bit set, bit clear, and bit toggle access to most peripheral registers. The bit set and bit clear functionality (also called Bit Access) enables modification of bit fields without the need to perform a read-modify-write. Also, the operation is contained within a single bus access. Bit access registers and their addresses are shown in the register map for each peripheral. Peripherals with no _SET, _CLR, or _TGL registers in the register map to not support these functions.

Each register with Bit Set functionality will have a _SET register. Whenever a bit in the SET register is written to a 1 the corresponding bit in its target register is set. The SET register is located at TARGET + 0x1000 where TARGET is the address of the target register and has the same name as the target register with '_SET' appended.

Each register with Bit Clear functionality will have a CLR register. Whenever a bit in the CLR register is written to a 1 the corresponding bit in its target register is cleared. The CLR register is located at TARGET + 0x2000 where TARGET is the address of the target register and has the same name as the target register with '_CLR' appended.

Each register with Bit Toggle functionality will have a TGL register. Whenever a bit in the TGL register is written to a 1 the corresponding bit in its target register is inverted. The TGL register is located at TARGET + 0x3000 where TARGET is the address of the target register and has the same name as the target register with '_TGL' appended.

Note: It is possible to combine bit clear and bit set operations in order to arbitrarily modify multi-bit register fields without affecting other fields in the same register. In this case, care should be taken to ensure that the field does not have intermediate values that can lead to erroneous behavior. For example, if bit clear and bit set operations are used to change an analog tuning register field from 0x2 to 0x4 by clearing bit 1 and then setting bit 2, the field would take on a value of zero for short time. If the analog module is active at the time, this could lead to undesired behavior.

4.2.4.4 Peripheral Access Performance

The Cortex-M33, DMA Controller, and peripherals run on clocks which can be pre-scaled separately. Clocks and pre-scaling are described in more detail in 8. CMU - Clock Management Unit. This section describes the access performance for a peripheral register based on its frequency relative to the CPUCLK frequency and its access type. For this discussion, PERCLK refers to a selected peripheral's clock frequency and CPUCLK refers to the core's clock frequency.

The type of each register in a peripheral is indicated in the 'Access' column of the peripherals register table. Register types are: ENABLE, CONFIG, SYNC, LFSYNC, and INTFLAG. If not type is listed then the register is a Generic register.

4.2.4.4.1 Generic Registers

Registers with no type listed are generic registers. They may be read or written to at any time. Access will not stall the CPU.

4.2.4.4.2 CONFIG Registers

CONFIG Registers contain configuration that does not change during peripheral operation.

CONFIG registers may only be written when a peripheral is disabled. Writing to a CONFIG register when a peripheral is enabled will result in a BUSFAULT. CONFIG register writes will not stall the CPU.

CONFIG registers may be read at any time. Reads will not stall the CPU.

4.2.4.4.3 SYNC Registers

SYNC registers are used to communicate with running high-speed peripherals where PERCLK is expected to be either higher or marginally slower (within an order of magnitude) than CPUCLK. For example, a timer can be running at 80 MHz (HFRCO) when the core is at 39 MHz (HFXO), or a timer can run at 16 MHz (HFRCO) when the core is 97.5 MHz (RFFPLLSYS). In these cases, CPU stalls of several PERCLK cycles do not significantly impact overall system performance in most systems.

SYNC registers may only be written to when the peripheral is enabled. Writing to a SYNC register when a peripheral is disabled will result in a BUSFAULT. A write will take several (2 - 3) PERCLK cycles to complete (take effect) during which time the entire module will be in a pending state. If a SYNC register is written to while the peripheral is already in a pending state, the CPU is stalled until the previous write finishes. If a SYNC register is written to while the peripheral is not in a pending state, the CPU is not stalled.

SYNC registers may be read at any time. If a SYNC register is read while the peripheral is disabled, the CPU is not stalled. If a SYNC register is read while the peripheral is enabled, the CPU will be stalled for several (2 -3) PERCLK cycles while up to date values are retrieved from the peripheral.

4.2.4.4.4 LFSYNC Registers

LFSYNC registers are used to communicate with running low frequency peripherals where PERCLK is expected to be much lower than the CPU clock and synchronization delays may be long. For example, an LETIMER can be running at 32 kHz when the core is at 97.5 MHz (RFFPLLSYS). In this case CPU stalls of several PERCLK cycles represent a significant blockage of the CPU and need to be avoided whenever possible. LFSYNC registers accommodate this by allowing the CPU to write the register and continue to do other work while the value is synchronized.

LFSYNC registers may be written at any time. A write will take several (3 -4) PERCLK cycles to complete during which the register will be in a pending state. If a LFSYNC register is written to while it is in a pending state, a BUSFAULT will occur. Each LFSYNC register has a status bit indicating if it is currently pending.

LFSYNC registers may be read at any time. The CPU is never stalled on a read. If a LFSYNC register is read while pending, the pending (recently written) data will be returned even though it has not yet taken effect. Software may use the busy status bit to determine if the read value has been applied to the hardware.

4.2.4.4.5 ENABLE Registers

ENABLE registers contain the enable bit for a peripheral.

ENABLE registers may be written at any time. When the peripheral is enabled it takes some time for the enable to take effect during which time the module is pending. Peripherals will be in the pending state for a few (2 - 3) PERCLK cycles when first enabled. Since the clock source for the peripheral may not be running before the peripheral is enabled, the start up time for the clock source may increase the pending time. See EFR32xG25 Wireless Gecko for more information on on-demand clock sources.

When EN is cleared to 0, the peripheral will be disabled. The DISABLING status bit will be set to 1 until the operation is complete. During disablement, the module will wait for any SYNCBUSY status to clear, reset the core peripheral function, and de-assert the peripheral clock. Entry into low energy modes EM2 and EM3 will be delayed while a peripheral is disabling.

While DISABLING is set, writing to any register in the module, including attempts to re-enable with EN, will cause a bus fault condition. Any register in the module can be read while DISABLING.

4.2.4.4.6 SWRST Registers

SWRST registers are available in some blocks to reset the module back to the intial condition, similar to a power-on reset.

SWRST registers have a SWRST bit, which will reset the peripheral when written to 1. These registers also contain a status bit, RESETTING, which indicates that a reset is in progress.

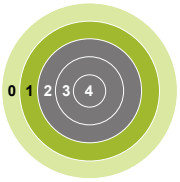
If a peripheral is resetting due to SWRST, entry into low energy modes EM2 and EM3 will be delayed. Writing to the SWRST bit or any other writeable register while a reset is in progress will generate a bus fault condition.

4.2.4.4.7 INTFLAG Registers

INTFLAG registers contain interrupt flags. To set or clear an interrupt flag, the _SET or _CLR register alias must be used. Writing directly to the INTFLAG register will have no effect.

Note that for an interrupt to occur when a flag is set the IRQ must be enabled in the NVIC.

5. Radio Transceiver





Quick Facts

What?

The Radio Transceiver provides access to transmit and receive data, radio settings and control interface.

Why?

The Radio Transceiver enables the user to communicate using a wide range of data rates, modulation and frame formats.

How?

Dynamic or fixed frame lengths, optional address recognition, flexible CRC and crypto schemes makes the EFR32 Series 2 perfectly suit any application using low or medium data rate radio communication.

5.1 Introduction

The EFR32xG25 Short Range Wireless Transceiver (SRW) consists of two main portions. The new portion is a SW Modem using RISC-V with dedicated RAM, and a highly linear Power Amplifier which is capable of Wi-SUN OFDM and SUN O-QPSK. This SW Modem architecture can accommodate some updates to the radio as the Wi-SUN standard evolves more so than a hardware only architecture. The purpose is to support the Wi-SUN PHY Working Group Amendment version 1VA8 which is in review during development of EFR32xG25. Unique customization using this SW Modem is not enabled.

The other main portion is the Legacy SRW which is like the Radio Transceiver of the EFR32FG23. This does enable the user to control a wide range of settings and options for tailoring constant envelope radio operation precisely to the user's need. It provides access to the transmit and receive data buffers and supports both dynamic and static frame lengths, as well as automatic address filtering and CRC insertion/verification.

As seen in the Radio Overview illustration (), the radio consists of several modules all responsible for specific tasks. Please refer to the abbreviations section (Appendix 1. Abbreviations) for a comprehensive description of acronyms.

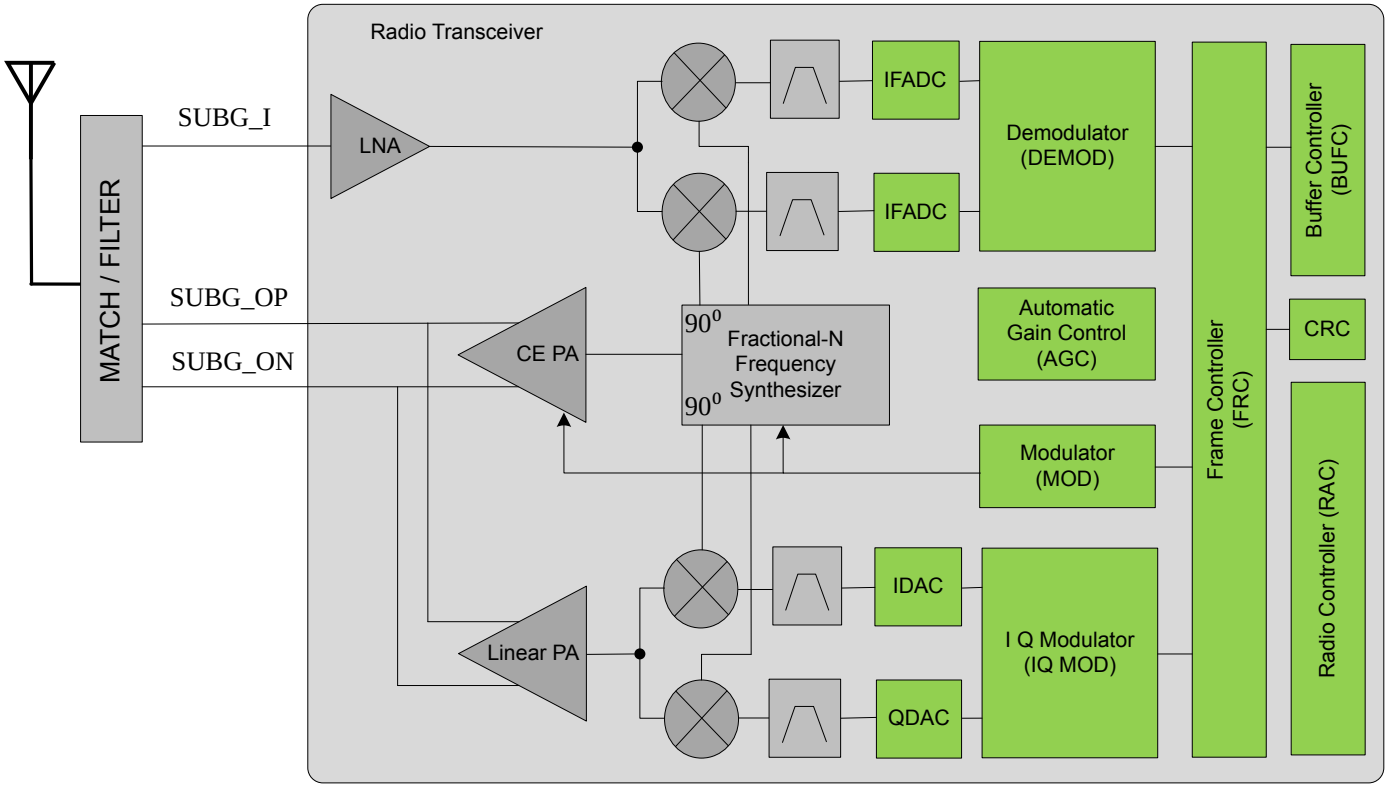


Figure 5.1. Radio Overview

During transmission (TX), the Radio Controller enables the SYNTH, Modulator and PA. The Modulator requests data from the Frame Controller, which reads data from a buffer. Based upon modulation format and data to send, the Modulator manipulates the SYNTH to output the correct frequency and phase. When the whole frame has been transmitted, the radio can automatically switch to receive mode.

In receive mode (RX), the radio controller enables the LNA, SYNTH, Mixer, ADC and Demodulator. The Demodulator searches for valid frames according to modulation format and data rate. If a frame is detected, the demodulated data is handed to the Frame Controller, which stores the data in the Buffer. When the complete frame has been received (determined by the Frame Controller), it is possible to either go to TX or stay in RX to search for a new frame.

The Radio Transceiver interface is accessible through software drivers provided by Silicon Labs.

5.1.1 RF Frequency Synthesizer

The Fractional-N RF Frequency Synthesizer (SYNTH) provides a low phase noise LO signal to be used in both receive and transmit modes.

The capabilities of the SYNTH include:

- High performance, low phase noise
- Fast frequency settling
- Fast and fully automated calibration
- Sub 100 Hz frequency resolution across the supported frequency bands

5.1.2 Modulation Modes

EFR32xG25 supports a wide range of modulation modes in transmit and receive:

- 2-FSK, 2-GFSK, 4-FSK, MSK, GMSK, O-QPSK with half-sine shaping, ASK / OOK, DBPSK TX
- Wi-SUN OFDM Options 1, 2, 3, and 4, with MCS index 0 through 6, and SUN O-QPSK
- NRZ or Manchester support
- UART mode over air for legacy protocols
- Baudrates ranging from below 100 Baud/s to 2 MBaud/s, allowing data rates up to 4 MBit/s
- Configurable frequency deviation
- Configurable Direct Sequence Spread Spectrum (DSSS), with spread sequences up to 32 chips encoding up to 4 information bits
- Configurable 4-FSK symbol encoding

5.1.3 Transmit Mode

In transmit mode EFR32xG25 performs the following functionality:

- Automatic PA power ramping during the start and end of a frame transmit
- Programmable output power
- Optional preamble and synchronization word insertion
- Accurate transmit frame timing to support time synchronized radio protocols
- Optional Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) hardware support
- Integrated transmit test modes, as described in 5.1.12 RF Test Modes

5.1.4 Receive Mode

In receive mode EFR32xG25 performs the following functionality:

- A single-ended LNA amplifies the input RF signal. The amplified signal is then mixed to a low-IF signal through the quadrature down-coversion mixer. Further signal filtering is performed before conversion to a digital signal through the I/Q ADC.
- Digitally configurable receiver bandwidth from 100 Hz to 2.5 MHz
- Timing recovery on received data, including simultaneous support for two different frame synchronization words
- Automatic frequency offset compensation, to compensate for carrier frequency offset between the transmitter and receiver
- Support for a wide range of modulation formats as described in section

5.1.5 Data Buffering

EFR32xG25 supports buffered transmit and receive modes through its buffer controller (BUFC), with four individually configurable buffers. The BUFC uses the system RAM as storage, and each buffer can be individually configured with parameters such as:

- Buffer size
- Buffer interrupt thresholds
- Buffer RAM location
- Overflow and underflow detection

In receive mode, data following frame synchronization is moved directly from the demodulator to the buffer storage.

In transmit mode, data following the inserted preamble and synchronization word is moved directly from the buffer storage to the modulator.

5.1.6 Unbuffered Data Transfer

For most system designs it is recommended to use the data buffering within EFR32xG25 to provide a convenient user interface.

In unbuffered data transfer modes the hardware support provided by EFR32xG25 to perform preamble and frame synchronization insertion in transmit mode and detection in receive mode can still optionally be used.

5.1.7 Frame Format Support

EFR32xG25 has an extensive support for frame handling in transmit and receive modes, which allows effective handling of even advanced protocols. The frame format support is controlled by the Frame Controller (FRC). The support includes:

- Preamble and frame synchronization inserted into transmitted frames
- Full frame synchronization of received frames
- Simple address matching of received frames in hardware, further configurable address and frame filtering supported through sequencer
- Support for variable length frames
- Automated CRC calculation and verification
- Configurable bit ordering, with the most or least significant bit transmitted and received first

5.1.8 Hardware CRC Support

EFR32xG25 supports a configurable CRC generation in transmit and verification in receive mode:

- 8, 16, 24 or 32 bit CRC value
- Configurable polynomial and initialization value
- Optional inversion of CRC value over air
- Configurable CRC byte ordering
- Support for multiple CRC values calculated and verified per transmitted or received frame
- The CRC module is typically controlled by the Frame Controller (FRC) for in-line operations in transmit and receive modes. Alternatively, the CRC module may be accessed directly from software to calculate and verify CRC data.

5.1.9 Convolutional Encoding / Decoding

EFR32xG25 includes hardware support for convolutional encoding and decoding, for forward error correction (FEC). This feature is performed by the Frame Controller (FRC) module:

- Constraint length configurable up to 7, for the highest robustness
- Configurable puncturing, to achieve rates between 1/2 rate and full rate
- Configurable soft decision or hard decision decoding
- Convolutional coding may be used together with the symbol interleaver to improve robustness against burst errors

5.1.10 Binary Block Encoding / Decoding

EFR32xG25 includes hardware support for binary block encoding and decoding, both performed real-time in the the transmit and receive path. This is performed in the Frame Controller (FRC) module:

The block coding works on blocks of up to 16 bits of data and adds parity bits to be capable of single or multiple bit corrections by the receiver.

- One or more parity bits can be added and verified
- Bit error correction
- Lookup-codes can be used to implement virtually any block coding scheme

5.1.11 Data Encryption and Authentication

EFR32xG25 has hardware support for AES encryption, decryption and authentication modes. These security operations can be performed on data in RAM or any data buffer, without further CPU intervention. The key size is 128 bits.

AES modes of operations directly supported by the EFR32xG25 hardware are listed in Table 5.1 AES modes of operation with hardware support on page 59. In addition to these modes, other modes can also be implemented by using combinations of modes. For example, the CCM mode can be implemented using the CTR and CBC-MAC modes in combination.

Table 5.1. AES modes of operation with hardware support

AES Mode	Encryption / Decryption	Authentication	Comment
ECB	Yes	-	Electronic Code Book
CTR	Yes	-	Counter mode
CCM	Yes	Yes	Counter with CBC-MAC
CCM*	Yes	Yes	CCM with encryption-only and integrity-only capabilities
GCM	Yes	Yes	Galois Counter Mode
CBC	Yes	-	Cipher Block Chaining
CBC-MAC	-	Yes	Cipher Block Chaining, Message Authentication Code
CMAC	-	Yes	Cipher-based MAC
CFB	Yes	-	Cipher Feedback
OFB	Yes	-	Output Feedback

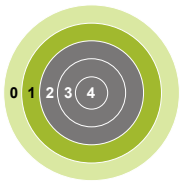
The Cryptographic Acceleration module can operate directly on data buffers provided by the buffer controller (BUFC) module. It is also possible to provide data directly from the embedded Cortex-M33 or via DMA.

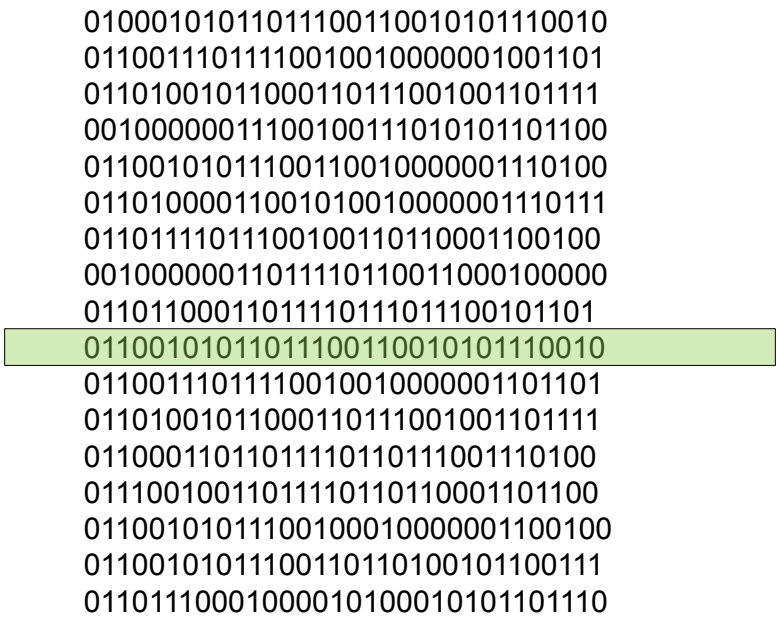
5.1.12 RF Test Modes

EFR32xG25 supports a wide range of RF test modes typically used for characterization and regulation compliance testing, including:

- Unmodulated carrier transmit
- Modulated carrier transmit, with internal configurable pseudo random data generator
- Continuous data reception for Bit Error Rate (BER) measurements
- Storing of raw receiver data to RAM
- Transmit of raw frequency data from RAM

6. MSC - Memory System Controller





Quick Facts

What?

The user can perform flash memory read, read configuration, and write operations through the Memory System Controller (MSC). SRAM operation may be configured though System Configuration (SYSCFG).

Why?

The MSC allows the application code and user data to be stored in non-volatile flash memory. Certain memory system functions, such as program memory wait-states and flash lock bits are configured from the MSC peripheral register interface, giving the developer the ability to dynamically customize the memory system performance, security level, energy consumption and error handling capabilities to the requirements at hand.

How?

The MSC integrates a low-energy flash IP with a charge pump, enabling minimum energy consumption while eliminating the need for external programming voltage to erase the memory. An easy to use write and erase interface is supported by an internal, fixed-frequency oscillator and autonomous flash timing and control reduces software complexity while not using other timer resources.

A highly efficient low energy instruction cache reduces the number of flash reads significantly, thus saving energy. Performance is also improved when wait-states are used, since many of the wait-states are eliminated. Built-in performance counters can be used to measure the efficiency of the instruction cache.

Instruction prefetcher improves program execution performance by reducing the number of wait-state cycles needed.

6.1 Introduction

The Memory System Controller (MSC) is the program memory unit of the EFR32xG25 microcontroller. The flash memory is readable and writable from both the Cortex-M33 and DMA. The flash memory is divided into two blocks: the main block and the information block. Program code is normally written to the main block. The information block is available for special user data. There is also a read-only page in the information block containing system and device calibration data. Flash read and write operations are supported in energy modes EM0 and EM1.

6.2 Features

- AHB read interface
  - Scalable access performance to optimize the Cortex-M33 code interface
    - Advanced energy optimization functionality
      - Conditional branch target prefetch suppression
      - Cortex-M33 disfolding of if-then (IT) blocks
      - Instruction Cache
      - Instruction Prefetch
  - DMA read support in EM0 and EM1
- Command and status interface
  - Flash write and erase
    - Accessible from Cortex-M33 in EM0
    - DMA write support in EM0 and EM1
  - Core clock independent Flash timing
    - Internal oscillator and internal timers for precise and autonomous Flash timing
      - General purpose timers are not occupied during Flash erase and write operations
      - No special time scaling registers needed
  - Configurable interrupt erase abort
    - Improved interrupt predictability
  - Memory and bus fault control
- Security features
  - Lockable debug access
  - Page lock registers
  - SW Mass erase and User Data lock bits
- End-of-write and end-of-erase interrupts

6.3 Functional Description

The size of the main flash block is device dependent. The largest size available is 1920 kB (240 pages). The information block has 1 kB available for user data. The information block also contains chip configuration data located in a reserved area. The main block is mapped to address 0x08000000 and the information block is mapped to address 0x0FE00000. Table 6.1 MSC Flash Memory Mapping on page 61 outlines how the flash is mapped in the memory space. All flash memory is organized into 8 kB pages.

Table 6.1. MSC Flash Memory Mapping

Block	Page	Base address	Write/Erase by...	Software Readable?	Purpose/Name	Size
Main	0	0x08000000	Software, debug	Yes	User code and data	64 kB - 1920 kB
	1	0x08002000	Software, debug	Yes		
	...		Software, debug	Yes		
	239[1]	0x081DE000	Software, debug	Yes		
Information	N/A	0x0FE00000	Software, debug	Yes	User Data (UD)	1 kB
	N/A	0x0FE08000	-	Yes	Device Information (DI)	1 kB

Note:

1. 240 pages for largest device.

6.3.1 Ram Configuration

The SYSCFG module contains controls for configuring the various RAM blocks on the device. Options include enabling EM2/EM3 data retention, ECC, prefetch, and cache. For a complete description see 6.6 SYSCFG - System Configuration.

6.3.2 Instruction Cache

The instruction cache improves the speed and power consumption of the Cortex-M33 by providing fast, low-power access to recently executed instructions. For detailed information see 6.5 ICACHE - Instruction Cache

6.3.3 Device Information (DI) Page

This read-only page holds calibration data from the production test, several unique device IDs, and other part specific information. For a complete description see 6.4 DEVINFO - Device Info Page.

6.3.4 User Data (UD) Page Description

This is the user data page in the information block. The page can be erased and written by software when MISCLOCKWORD.UDLOCKBIT is 0.

6.3.5 Bootloader

The EFR32xG25 supports use of the Gecko Bootloader detailed in *UG266: Silicon Labs Gecko Bootloader User's Guide* (https://www.silabs.com/support/resources).To enable bootloader functionality, the second stage of the bootloader must be configured and programmed into the beginning of flash. The first stage of the bootloader is provided by the SE and is not user accessible. For more details on SE bootloader support, see the SE peripheral documentation.

6.3.6 Post-reset Behavior

Calibration values are automatically written to registers by the MSC before application code start-up. The values can also be read from the DI page by software. Other information such as the device ID and production date is also stored in the DI page and is readable from software.

As part of the reset, hardware performs repeated flash reads to determine when flash is fully powered up and available for use by the CPU. PWRUPCKBDFAILCOUNT in MSC_STATUS contains the number of failed reads during the last reset.

6.3.7 Flash Startup

Flash wakeup on demand is supported when waking from EM2/3 to EM0. Set bit FLASHPWRUPONDEMAND of register EMU_CTRL to enable the power up on demand. When enabled, flash will not be powered up until accessed. In this case it is possible for the MCU to wake, execute out of RAM or cache, and return to sleep mode without ever powering on the Flash. Software can force the flash to power up by writing PWRUP in MSC_CMD. When flash is powered via MSC_CMD the MSC_IF.PWRUPF interrupt flag will be set when power up is complete and the CPU will be interrupted if MSC_IEN.PWRUPF is set.

6.3.8 Flash EM0 / EM1 Power Down

It is also possible to put the flash in a power-saving sleep mode when the system is in EM0 or EM1. Flash power down can be configured to happen on entering EM1, radio-only sleep, or with an immediate manual operation.

During EM0, software can instruct the flash to go to power down mode with the MSC_CMD.PWROFF command. Any system IRQ or flash read will wake the flash. The MSC_CMD.PWRUP command is used to power the flash back up in the absence of a wake event.

The MSC_PWRCTRL register allows the flash to be configured to automatically enter sleep mode on entering EM1 or radio-only sleep with the bits PWROFFONEM1ENTRY and PWROFFONEM1PENTRY, respectively. If the flash is configured to sleep during one of these states, it may sometimes be powered back up without processor intervention in EM0 (for example, if DMA reads flash in EM1). By default, the flash will remain powered on after such access. If the PWROFFENTRYAGAIN bit is set, it instructs the flash to re-enter the power down state if no further access is seen during the timeout period defined by PWROFFDLY. Flash must be idle for PWROFFDLY * 64 bus clocks before it will enter sleep again.

6.3.9 Wait-states

Since the CPU may be clocked faster than the flash can respond, it is necessary to configure wait-states for flash accesses at higher CPU clock speeds. See the device Datasheet for information on the maximum allowed frequency for each wait-state setting. To configure the flash wait-states set the MODE field in MSC_READCTRL.

When changing wait states, care should be taken that the system is never in an invalid state. To ensure this, MODE should be changed after the clock is changed when reducing clock speed and before the clock is changed when increasing clock speed.

6.3.10 Cortex-M33 If-Then Block Folding

The Cortex-M33 offers a mechanism known as if-then block folding. This is a form of speculative prefetching where small if-then blocks are collapsed in the prefetch buffer if the condition evaluates to false. The instructions in the block then appear to execute in zero cycles. With this scheme, performance is optimized at the cost of higher energy consumption as the processor fetches more instructions from memory than it actually executes. To disable the mode, write a 1 to the DISFOLD bit in the NVIC Auxiliary Control Register; see the Cortex-M33 Technical Reference Manual for details. Normally, it is expected that this feature is most efficient when operating with 0 wait-states. Folding is enabled by default.

6.3.11 Line Buffering (Prefetch)

The MSC reads a 2-word line from flash on any flash access. The data being accessed is returned immediately and the other word locally cached so that it can be provided immediately if accessed. This has the effect of pre-fetching the second word when the first is read, resulting in fewer wait-states when executing sequential code. This feature may be disabled by setting DOUTBUFEN in MSC_READCTRL.

6.3.12 Erase and Write Operations

The 20 MHz FSRCO is used for timing during flash write and erase operations. The default values in MSC_FLASHPROGRAMTIME and MSC_FLASHERASETIME contain the recommended programming configuration.

To erase a page first set WREN in MSC_WRITECTRL and load any address in the page to be erased into the MSC_ADDRB register. Next check INVADDR, LOCKED, and WREADY in MSC_STATUS to ensure that the address is valid, not locked, and the MSC is ready to modify flash. Writing ERASEPAGE in MSC_WRITEMD will execute the page erase operation. ERASE in MSC_IF will be set when the page erase is complete. If ERASE in MSC_IEN is set, the end of a page erase will also trigger an interrupt. Finally, clear WREN to disable flash operations.

In addition to a page erase, a mass erase will clear the entire contents of the main flash array. A mass erase can be initiated by the Secure Engine. User Data page contents are not included in a mass erase.

To perform a programming operation, set WREN and load the address to be programmed into the MSC_ADDRB register. Next check INVADDR, LOCKED, WREADY, and WDATAREADY in MSC_STATUS to ensure that the address is valid, not locked, the MSC is ready to modify flash, and the write data buffer is clear. Writing data to MSC_WDATA will begin the programming operation. If a burst write is being performed, the next data word can be programmed to MSC_WDATA as soon as WDATAREADY is set. WRITE in MSC_IF will be set when the programming operation is complete. If WRITE in MSC_IEN is set, the end of the program operation will also trigger an interrupt. Finally, clear WREN to disable flash operations.

If data is written to the MSC_WDATA register faster than it can be processed, WDATAOV in MSC_IF will be set. If WDATAOV in MSC_IEN is set an interrupt will also be fired.

The MSC_ADDRB register only has to be written once when writing to sequential words. After each word is written, ADDRB is incremented automatically by 4. The INVADDR bit of the MSC_STATUS register is set if the loaded address is outside the flash. The LOCKED bit of the MSC_STATUS register is set if the page addressed is locked. Any attempts to erase or write to the page are ignored if INVADDR or the LOCKED bits of the MSC_STATUS register are set.

Write and erase operations may be aborted by software. To abort an erase, set the ERASEABORT bit in the MSC_WRITECMD register. To abort a write, set WRITEEND in MSC_WRITECMD

For a DMA write, CLEARWDATA in MSC_WRITECMD to assert a DMA request and transfer the first word. Alternately the first word may be programmed manually into MSC_WDATA by code.

By default, if any interrupt occurs during an erase operation, the erase is aborted. This feature may be disabled by clearing IRQERASEABORT in MSC_WRITECTRL. When an erase is aborted due to an interrupt, ERASEABORTED in MSC_STAUTS is set by hardware.

Software may observe the status of the MSC via the MSC_STATUS register. When a flash operation is in progress, BUSY will be set. If a flash operation has been requested but not yet started, PENDING will be set. This may occur if a subsystem is performing MSC operations. When the write buffer underflows, TIMEOUT will be set. Buffer underflow is a normal part of the write procedure since it will occur once the last word has been written and no more data is available.

The Flash memory is organized into 64-bit wide double-words. Each 64-bit double-word can be written only twice between erase cycles. The lower and upper 32-bit words may be written sequentially in any order, or one at a time. Each flash bit is 1 after erase. Writing a 0 will clear the bit. Writing a 1 will not change the bit value.

While it is possible to write twice to the lower or upper 32-bit word of the 64-bit double word, then the other 32-bit word cannot be used. In this case, it is permitted to write to either the lower or upper 32-bit word twice between each erase, so long as no bit is ever cleared more than once.

Note: The ERASEPAGE bit in WRITECMD and the WDATA register cannot safely be written from code in flash. It is recommended to place a small code section in RAM to set these bits and wait for the operation to complete. Also note that DMA transfers to or from any other address in flash while a write or erase operation is in progress will produce unpredictable results.

Note: During a write or erase, flash read accesses will be stalled, effectively halting code execution from flash. Code execution continues upon write/erase completion. Code residing in RAM or ICACHE may be executed during a write/erase operation.

6.3.12.1 Low-Power Write

To limit maximum current, the programming operations can be slowed down. Set LPWRITE in MSC_WRITECTRL to double the write time and halve the write current.

6.3.12.2 Flash Lock

The ability to program or erase individual flash pages may be disabled using the MSC_PAGELOCKn registers. The bits in these registers may only be set to 1 by software on the device and are cleared when the device is reset. This means that once locked, a page may not be unlocked until a reset occurs. Users wishing to lock accesses to flash should implement code to write to the MSC_PAGELOCKn registers immediately after a reset. Any page locked in this way cannot be written to or erased.

User Data can be locked by setting MSC_MISCLOCKWORD.UDLOCK to 1. Mass erase is enabled out of reset, however if firmware sets MELOCKBIT in the MSC_MISCLOCKWORD register, then mass erase can only be issued by the SE.

6.4 DEVINFO - Device Info Page

The Device Info Page holds factory programmed information about the device. It contains the following data:

- Calibration values for reconfiguring the device
- Unique ID's
- OPN identifiers (family, feature set, flash size, etc.)

6.4.1 DEVINFO Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	DEVINFO_INFO	R	DI Information
0x004	DEVINFO_PART	R	Part Info
0x008	DEVINFO_MEMINFO	R	Memory Info
0x00C	DEVINFO_MSIZE	R	Memory Size
0x010	DEVINFO_PKGINFO	R	Misc Device Info
0x014	DEVINFO_CUSTOMINFO	R	Custom Part Info
0x018	DEVINFO_SWFIX	R	SW Fix Register
0x01C	DEVINFO_SWCAPA0	R	Software Restriction
0x020	DEVINFO_SWCAPA1	R	Software Restriction
0x028	DEVINFO_EXTINFO	R	External Component Info
0x040	DEVINFO_EUI48L	R	EUI 48 Low
0x044	DEVINFO_EUI48H	R	EUI 48 High
0x048	DEVINFO_EUI64L	R	EUI64 Low
0x04C	DEVINFO_EUI64H	R	EUI64 High
0x050	DEVINFO_CALTEMP	R	Calibration Temperature
0x054	DEVINFO_EMUTEMP	R	EMU Temp
0x058	DEVINFO_HFRCODPLLCALn	R	HFRCODPLL Calibration
0x0A0	DEVINFO_HFRCOEM23CALn	R	HFRCOEM23 Calibration
0x130	DEVINFO_MODULENAME0	R	Module Name Information
0x134	DEVINFO_MODULENAME1	R	Module Name Information
0x138	DEVINFO_MODULENAME2	R	Module Name Information
0x13C	DEVINFO_MODULENAME3	R	Module Name Information
0x140	DEVINFO_MODULENAME4	R	Module Name Information
0x144	DEVINFO_MODULENAME5	R	Module Name Information
0x148	DEVINFO_MODULENAME6	R	Module Name Information
0x14C	DEVINFO_MODULEINFO	R	Module Information
0x150	DEVINFO_MODXOCAL	R	Module External Oscillator Calibration Information
0x17C	DEVINFO_HFXOCAL	R	High Frequency Crystal Oscillator Calibration Data
0x180	DEVINFO_IADC0GAIN0	R	IADC Gain Calibration
0x184	DEVINFO_IADC0GAIN1	R	IADC Gain Calibration
0x188	DEVINFO_IADC0OFFSETCAL0	R	IADC Offset Calibration
0x18C	DEVINFO_IADC0NORMALOFF-SETCAL0	R	IADC Offset Calibration
0x190	DEVINFO_IADC0NORMALOFF-SETCAL1	R	IADC Offset Calibration

Offset	Name	Type	Description
0x194	DEVINFO_IADC0HISPDOFF-SETCAL0	R	IADC Offset Calibration
0x198	DEVINFO_IADC0HISPDOFF-SETCAL1	R	IADC Offset Calibration
0x1FC	DEVINFO_LEGACY	R	Legacy Device Info

6.4.2 DEVINFO Register Description

6.4.2.1 DEVINFO_INFO - DI Information

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x12								0x0								0x0															
Access	R								R								R															
Name	DEVINFOREV								PRODREV								CRC															

Bit	Name	Reset	Access	Description
31:24	DEVINFOREV	0x12	R	**DI Page Version**
	DEVINFO layout revision as unsigned integer (initially 1)			
23:16	PRODREV	0x0	R	**Production Revision**
	Production revision as unsigned integer			
15:0	CRC	0x0	R	**CRC**
	CRC of DI-page (CRC-16-CCITT)			

6.4.2.2 DEVINFO_PART - Part Info

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset			0x0								0x0						0x0															
Access			R								R						R															
Name			FAMILY								FAMILYNUM						DEVICENUM															

Bit	Name	Reset	Access	Description
31:30	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
29:24	FAMILY	0x0	R	**Device Family**
	Encoded portion of the Device Family			
	Value	Mode		Description
	0	FG		Flex Gecko
23:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21:16	FAMILYNUM	0x0	R	**Device Family**
	Numeric portion of the Device Family			
15:0	DEVICENUM	0x0	R	**Device Number**
	Device Number. The device number is one letter and 3 digits. NUMBER = (alpha-'A')*1000 + numeric. 0 = A000; 1123 = B123			

6.4.2.3 DEVINFO_MEMINFO - Memory Info

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x100																0x1								0x3							
Access	R																R								R							
Name	DILEN																UDPAGESIZE								FLASHPAGESIZE							

Bit	Name	Reset	Access	Description
31:16	DILEN	0x100	R	**Length of DI Page**
	Length of DI area (number of 32-bit words included in CRC)			
15:8	UDPAGESIZE	0x1	R	**User Data Page Size**
	User Data page size			
7:0	FLASHPAGESIZE	0x3	R	**Flash Page Size**
	Flash page size in bytes coded as 2^((MEMINFO.PAGESIZE +10) & 0xFF. For example, the value of 0xFF = 512 bytes			

6.4.2.4 DEVINFO_MSIZE - Memory Size

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset						0x0											0x0															
Access						R											R															
Name						SRAM											FLASH															

Bit	Name	Reset	Access	Description
31:27	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
26:16	SRAM	0x0	R	**Sram Size**
	Ram size, kbyte count as unsighed integer (eg 16)			
15:0	FLASH	0x0	R	**Flash Size**
	Flash size, kbyte count as unsigned integer (eg. 128)			

6.4.2.5 DEVINFO_PKGINFO - Misc Device Info

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset									0x0								0x0								0x0							
Access									R								R								R							
Name									PINCOUNT								PKGTYPE								TEMPGRADE							

Bit	Name	Reset	Access	Description
31:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:16	PINCOUNT	0x0	R	**Pin Count**
	Device pin count as unsigned integer (eg. 48)			
15:8	PKGTYPE	0x0	R	**Package Type**
	Package identifier as character			

Value	Mode	Description
74	WLCSP	WLCSP package
76	BGA	BGA package
77	QFN	QFN package
81	QFP	QFP package

Bit	Name	Reset	Access	Description
7:0	TEMPGRADE	0x0	R	**Temperature Grade**
	Temperature Grade of product as unsigned integer enumeration			

Value	Mode	Description
0	N40TO85	-40 to 85 degC
1	N40TO125	-40 to 125 degC
2	N40TO105	-40 to 105 degC
3	N0TO70	0 to 70 degC

6.4.2.6 DEVINFO_CUSTOMINFO - Custom Part Info

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	PARTNO																															

Bit	Name	Reset	Access	Description
31:16	PARTNO	0x0	R	**Part Number**
	Custom part identifier as unsigned integer (eg. 903). 65535 for standard product			
15:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

6.4.2.7 DEVINFO_SWFIX - SW Fix Register

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFFFFFFFF																													
Access	R																													
Name	RSV																													

Bit	Name	Reset	Access	Description
31:0	RSV	0xFFFFFFFF	R	**Reserved**
	Reserved for future use			

6.4.2.8 DEVINFO_SWCAPA0 - Software Restriction

Offset	Bit Position																											
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset						0x0					0x0				0x0				0x0				0x0				0x0				0x0	
Access						R					R				R				R				R				R				R	
Name						ZWAVE					SRI				CONNECT				BTSMART				RF4CE				THREAD				ZIGBEE	

Bit	Name	Reset	Access	Description
31:27	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
26:24	ZWAVE	0x0	R	**Z-Wave Capability**
	Z-Wave Stack Capability			

Value	Mode	Description
0	LEVEL0	Z-Wave stack capability not available
1	LEVEL1	Z-Wave Gateway
2	LEVEL2	Z-Wave End Device
3	LEVEL3	Z-Wave Sensor
4	LEVEL4	Z-Wave Lighting

Bit	Name	Reset	Access	Description
23:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21:20	SRI	0x0	R	**RAIL Capability**
	RAIL capability not available			

Value	Mode	Description
0	LEVEL0	RAIL capability not available
1	LEVEL1	RAIL enabled
2	LEVEL2	N/A
3	LEVEL3	N/A

Bit	Name	Reset	Access	Description
19:18	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
17:16	CONNECT	0x0	R	**Connect Capability**
	Connect stack capability level			

Value	Mode	Description
0	LEVEL0	Connect stack capability not available
1	LEVEL1	Connect enabled
2	LEVEL2	N/A
3	LEVEL3	N/A

Bit	Name	Reset	Access	Description
15:14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13:12	BTSMART	0x0	R	**Bluetooth Smart Capability**
	Bluetooth SMART stack capability level			
	Value	Mode		Description
	0	LEVEL0		Bluetooth SMART stack capability not available
	1	LEVEL1		Bluetooth SMART enabled
	2	LEVEL2		N/A
	3	LEVEL3		N/A
11:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	RF4CE	0x0	R	**RF4CE Capability**
	RF4CE stack capability level			
	Value	Mode		Description
	0	LEVEL0		Thread stack capability not available
	1	LEVEL1		Thread stack enabled
	2	LEVEL2		N/A
	3	LEVEL3		N/A
7:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:4	THREAD	0x0	R	**Thread Capability**
	Thread stack capability level			
	Value	Mode		Description
	0	LEVEL0		RF4CE stack capability not available
	1	LEVEL1		RF4CE stack enabled
	2	LEVEL2		N/A
	3	LEVEL3		N/A
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	ZIGBEE	0x0	R	**Zigbee Capability**
	ZigBee stack capability level			
	Value	Mode		Description
	0	LEVEL0		ZigBee stack capability not available
	1	LEVEL1		GreenPower only
	2	LEVEL2		ZigBee and GreenPower
	3	LEVEL3		ZigBee Only

6.4.2.9 DEVINFO_SWCAPA1 - Software Restriction

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0	0x1	0x1	0x1
Access																													R	R	R	R
Name																													XOUT	GWEN	NCPEN	RFMCUEN

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	XOUT	0x0	R	**XOUT**
	XOUT feature available			
2	GWEN	0x1	R	**Gateway**
	Gateway enabled part			
1	NCPEN	0x1	R	**NCP**
	Network co-processor enabled part. NCP only if RFMCUEN = 0			
0	RFMCUEN	0x1	R	**RF-MCU**
	RF-MCU enabled part. RF-MCU only if NCPEN = 0			

6.4.2.10 DEVINFO_EXTINFO - External Component Info

Offset	Bit Position																													
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset									0xFF								0xFF								0xFF							
Access									R								R								R							
Name									REV								CONNECTION								TYPE							

Bit	Name	Reset	Access	Description
31:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:16	REV	0xFF	R	**Revision**
	MCM Revision			
15:8	CONNECTION	0xFF	R	**Connection**
	Connection protocol to external interface			
	Value	Mode		Description
	0	SPI		SPI control interface
	255	NONE		No interface
7:0	TYPE	0xFF	R	**Type**
	External Component			
	Value	Mode		Description
	255	NONE		

6.4.2.11 DEVINFO_EUI48L - EUI 48 Low

Offset	Bit Position																													
0x040	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0								0x0																							
Access	R								R																							
Name	OUI48L								UNIQUEID																							

Bit	Name	Reset	Access	Description
31:24	OUI48L	0x0	R	**OUI48L**
	Lower Octet of EUI48 Organizationally Unique Identifier			
23:0	UNIQUEID	0x0	R	**Unique ID**
	Unique identifier			

6.4.2.12 DEVINFO_EUI48H - EUI 48 High

Offset	Bit Position																													
0x044	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFFFF																0x0															
Access	R																R															
Name	RESERVED																OUI48H															

Bit	Name	Reset	Access	Description
31:16	RESERVED	0xFFFF	R	**RESERVED**
	Reserved			
15:0	OUI48H	0x0	R	**OUI48H**
	Upper two Octets of EUI48 OUI			

6.4.2.13 DEVINFO_EUI64L - EUI64 Low

Offset	Bit Position																													
0x048	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	UNIQUEL																															

Bit	Name	Reset	Access	Description
31:0	UNIQUEL	0x0	R	**UNIQUEL**
	Lower 32 bits of EUI64 Unique Identifier			

6.4.2.14 DEVINFO_EUI64H - EUI64 High

Offset	Bit Position																													
0x04C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																								0x0							
Access	R																								R							
Name	OUI64																								UNIQUEH							

Bit	Name	Reset	Access	Description
31:8	OUI64	0x0	R	**OUI64**
	24-bit OUI identifier			
7:0	UNIQUEH	0x0	R	**UNIQUEH**
	Upper 8 bits of EUI64 unique identifier			

6.4.2.15 DEVINFO_CALTEMP - Calibration Temperature

Offset	Bit Position																													
0x050	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									R							
Name																									TEMP							

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	TEMP	0x0	R	**Cal Temp**
	Calibration temperature as an unsigned int in DegC. (0x19 = 25DegC)			

6.4.2.16 DEVINFO_EMUTEMP - EMU Temp

Offset	Bit Position																													
0x054	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																										0x0						
Access																										R						
Name																										EMUTEMPROOM						

Bit	Name	Reset	Access	Description
31:11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10:2	EMUTEMPROOM	0x0	R	**Emu Room Temperature**
	EMU_TEMP temperature reading at room (calibration) temperature.			
1:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

6.4.2.17 DEVINFO_HFRCODPLLCALn - HFRCODPLL Calibration

Offset	Bit Position																													
0x058	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0				0x0		0x0		0x0			0x0					0x0		0x0							0x0						
Access	R				R		R		R			R					R		R							R						
Name	IREFTC				CMPSEL		CLKDIV		CMPBIAS			FREQRANGE					LDOHP		FINETUNING							TUNING						

Bit	Name	Reset	Access	Description
31:28	IREFTC	0x0	R	
	Tempco Trim			
27:26	CMPSEL	0x0	R	
	Comparator Load Select			
25:24	CLKDIV	0x0	R	
	Locally Divide HFRCO Clock Output			
23:21	CMPBIAS	0x0	R	
	Comparator Bias Current			
20:16	FREQRANGE	0x0	R	
	Frequency Range			
15	LDOHP	0x0	R	
	LDO High Power Mode			
14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13:8	FINETUNING	0x0	R	
	Fine Tuning Value			
7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:0	TUNING	0x0	R	
	Tuning Value			

6.4.2.18 DEVINFO_HFRCOEM23CALn - HFRCOEM23 Calibration

Offset	Bit Position																													
0x0A0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0				0x0		0x0		0x0			0x0					0x0		0x0							0x0						
Access	R				R		R		R			R					R		R							R						
Name	IREFTC				CMPSEL		CLKDIV		CMPBIAS			FREQRANGE					LDOHP		FINETUNING							TUNING						

Bit	Name	Reset	Access	Description
31:28	IREFTC	0x0	R	
	Tempco Trim			
27:26	CMPSEL	0x0	R	
	Comparator Load Select			
25:24	CLKDIV	0x0	R	
	Locally Divide HFRCO Clock Output			
23:21	CMPBIAS	0x0	R	
	Comparator Bias Current			
20:16	FREQRANGE	0x0	R	
	Frequency Range			
15	LDOHP	0x0	R	
	LDO High Power Mode			
14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13:8	FINETUNING	0x0	R	
	Fine Tuning Value			
7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:0	TUNING	0x0	R	
	Tuning Value			

6.4.2.19 DEVINFO_MODULENAME0 - Module Name Information

Offset	Bit Position																													
0x130	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFF								0xFF								0xFF								0xFF							
Access	R								R								R								R							
Name	MODCHAR4								MODCHAR3								MODCHAR2								MODCHAR1							

Bit	Name	Reset	Access	Description
31:24	MODCHAR4	0xFF	R	
	Fourth character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			
23:16	MODCHAR3	0xFF	R	
	Third character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			
15:8	MODCHAR2	0xFF	R	
	Second character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			
7:0	MODCHAR1	0xFF	R	
	First character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			

6.4.2.20 DEVINFO_MODULENAME1 - Module Name Information

Offset	Bit Position																													
0x134	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFF								0xFF								0xFF								0xFF							
Access	R								R								R								R							
Name	MODCHAR8								MODCHAR7								MODCHAR6								MODCHAR5							

Bit	Name	Reset	Access	Description
31:24	MODCHAR8	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			
23:16	MODCHAR7	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			
15:8	MODCHAR6	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			
7:0	MODCHAR5	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			

6.4.2.21 DEVINFO_MODULENAME2 - Module Name Information

Offset	Bit Position																													
0x138	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFF								0xFF								0xFF								0xFF							
Access	R								R								R								R							
Name	MODCHAR12								MODCHAR11								MODCHAR10								MODCHAR9							

Bit	Name	Reset	Access	Description
31:24	MODCHAR12	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			
23:16	MODCHAR11	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			
15:8	MODCHAR10	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			
7:0	MODCHAR9	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			

6.4.2.22 DEVINFO_MODULENAME3 - Module Name Information

Offset	Bit Position																													
0x13C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFF								0xFF								0xFF								0xFF							
Access	R								R								R								R							
Name	MODCHAR16								MODCHAR15								MODCHAR14								MODCHAR13							

Bit	Name	Reset	Access	Description
31:24	MODCHAR16	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			
23:16	MODCHAR15	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			
15:8	MODCHAR14	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			
7:0	MODCHAR13	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			

6.4.2.23 DEVINFO_MODULENAME4 - Module Name Information

Offset	Bit Position																													
0x140	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFF								0xFF								0xFF								0xFF							
Access	R								R								R								R							
Name	MODCHAR20								MODCHAR19								MODCHAR18								MODCHAR17							

Bit	Name	Reset	Access	Description
31:24	MODCHAR20	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			
23:16	MODCHAR19	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			
15:8	MODCHAR18	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			
7:0	MODCHAR17	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			

6.4.2.24 DEVINFO_MODULENAME5 - Module Name Information

Offset	Bit Position																													
0x144	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFF								0xFF								0xFF								0xFF							
Access	R								R								R								R							
Name	MODCHAR24								MODCHAR23								MODCHAR22								MODCHAR21							

Bit	Name	Reset	Access	Description
31:24	MODCHAR24	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			
23:16	MODCHAR23	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			
15:8	MODCHAR22	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			
7:0	MODCHAR21	0xFF	R	
	Character of Module Name, 0xFF = unwritten, 0x00 = character not used in name			

6.4.2.25 DEVINFO_MODULENAME6 - Module Name Information

Offset	Bit Position																													
0x148	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFFFF																0xFF								0xFF							
Access	R																R								R							
Name	RSV																MODCHAR26								MODCHAR25							

Bit	Name	Reset	Access	Description
31:16	RSV	0xFFFF	R	
	Reserved for future use			
15:8	MODCHAR26	0xFF	R	
	Last possible character of module name, 0xFF = unwritten, 0x00 = character not used in name			
7:0	MODCHAR25	0xFF	R	
	0xFF = unwritten, 0x00 = character not used in name			

6.4.2.26 DEVINFO_MODULEINFO - Module Information

Offset	Bit Position																													
0x14C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x1	0x1	0x1	0x1FF									0x1	0x1	0x1	0x1	0x1	0x7F							0x7			0x1F				
Access	R	R	R	R									R	R	R	R	R	R							R			R				
Name	EXTVALID	PHYLIMITED	PADCDC	MODNUMBERMSB									HFXOCALVAL	LFXOCALVAL	EXPRESS	LFXO	TYPE	MODNUMBER							ANTENNA			HWREV				

Bit	Name	Reset	Access	Description
31	EXTVALID	0x1	R	
	EXTINFO entry used			
	Value	Mode		Description
	0	EXTUSED		
	1	EXTUNUSED		
30	PHYLIMITED	0x1	R	
	PHY Limited			
	Value	Mode		Description
	0	LIMITED		
	1	UNLIMITED		
29	PADCDC	0x1	R	
	PAVDD Connection			
	Value	Mode		Description
	0	VDCDC		
	1	OTHER		
28:20	MODNUMBERMSB	0x1FF	R	
	Counter allowing unique identification of module per lookup when combined with MODNUMBER			
19	HFXOCALVAL	0x1	R	
	HFXO Factory Calibrated			
	Value	Mode		Description
	0	VALID		
	1	NOTVALID		
18	LFXOCALVAL	0x1	R	

Bit	Name	Reset	Access	Description
	LFXO Factory Calibrated			
	Value	Mode		Description
	0	VALID		
	1	NOTVALID		
17	EXPRESS	0x1	R	
	Blue Gecko Express			
	Value	Mode		Description
	0	SUPPORTED		
	1	NONE		
16	LFXO	0x1	R	
	Module has LFXO			
	Value	Mode		Description
	0	NONE		
	1	PRESENT		
15	TYPE	0x1	R	
	Module Type			
	Value	Mode		Description
	0	PCB		
	1	SIP		
14:8	MODNUMBER	0x7F	R	
	Counter allowing unique identification of module per lookup when combined with MODNUMBER MSB			
7:5	ANTENNA	0x7	R	
	Module Antenna Type			
	Value	Mode		Description
	0	BUILTIN		None
	1	CONNECTOR		
	2	RFPAD		
	3	INVERTEDF		
4:0	HWREV	0x1F	R	
	Module Hardware Revision. Starting from 0			

6.4.2.27 DEVINFO_MODXOCAL - Module External Oscillator Calibration Information

Offset	Bit Position																													
0x150	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset										0x7F							0xFF								0xFF							
Access										R							R								R							
Name										LFXOCAPTUNE							HFXOCTUNEXOANA								HFXOCTUNEXIANA							

Bit	Name	Reset	Access	Description
31:23	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
22:16	LFXOCAPTUNE	0x7F	R	
	LFXO Cap Tuning			
15:8	HFXOCTUNEXOANA	0xFF	R	
	Tuning capacitance on XO			
7:0	HFXOCTUNEXIANA	0xFF	R	
	Tuning capacitance on XI			

6.4.2.28 DEVINFO_HFXOCAL - High Frequency Crystal Oscillator Calibration Data

Offset	Bit Position																													
0x17C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFFFFFF																								0x0				0x0			
Access	R																								R				R			
Name	RESERVED																								VTRTRIMANA				SHUNTBIASANA			

Bit	Name	Reset	Access	Description
31:8	RESERVED	0xFFFFFF	R	**New BitField**
	Reserved			
7:4	VTRTRIMANA	0x0	R	
	BUFOUT Reference Trim			
3:0	SHUNTBIASANA	0x0	R	
	Shunt Regulator Bias Current			

Value	Mode	Description
0	I20UA	
1	I30UA	
2	I40UA	
3	I50UA	
4	I60UA	
5	I70UA	
6	I80UA	
7	I90UA	
8	I100UA	
9	I110UA	
10	I120UA	
11	I130UA	
12	I140UA	
13	I150UA	
14	I160UA	
15	I170UA	

6.4.2.29 DEVINFO_IADC0GAIN0 - IADC Gain Calibration

Offset	Bit Position																													
0x180	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																0x0															
Access	R																R															
Name	GAINCANA2																GAINCANA1															

Bit	Name	Reset	Access	Description
31:16	GAINCANA2	0x0	R	
	Input Gain = 2x			
15:0	GAINCANA1	0x0	R	
	Input Gain = 1x and 0.5x			

6.4.2.30 DEVINFO_IADC0GAIN1 - IADC Gain Calibration

Offset	Bit Position																													
0x184	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																0x0															
Access	R																R															
Name	GAINCANA4																GAINCANA3															

Bit	Name	Reset	Access	Description
31:16	GAINCANA4	0x0	R	
	Input Gain = 4x			
15:0	GAINCANA3	0x0	R	
	Input Gain = 3x			

6.4.2.31 DEVINFO_IADC0OFFSETCAL0 - IADC Offset Calibration

Offset	Bit Position																													
0x188	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																0x0															
Access	R																R															
Name	OFFSETANA1HIACC																OFFSETANABASE															

Bit	Name	Reset	Access	Description
31:16	OFFSETANA1HIACC	0x0	R	
	High-accuracy OSR adjustment term			
15:0	OFFSETANABASE	0x0	R	
	Base analog offset term			

6.4.2.32 DEVINFO_IADC0NORMALOFFSETCAL0 - IADC Offset Calibration

Offset	Bit Position																													
0x18C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																0x0															
Access	R																R															
Name	OFFSETANA2NORM																OFFSETANA1NORM															

Bit	Name	Reset	Access	Description
31:16	OFFSETANA2NORM	0x0	R	
	Normal mode offset gain adjustment term			
15:0	OFFSETANA1NORM	0x0	R	
	Normal mode analog offset term at OSR=2x, gain = 1x			

6.4.2.33 DEVINFO_IADC0NORMALOFFSETCAL1 - IADC Offset Calibration

Offset	Bit Position																													
0x190	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	R															
Name																	OFFSETANA3NORM															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	OFFSETANA3NORM	0x0	R	
	Normal mode offset term for OSR>=4x			

6.4.2.34 DEVINFO_IADC0HISPDOFFSETCAL0 - IADC Offset Calibration

Offset	Bit Position																													
0x194	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset								0x0									0x0															
Access								R									R															
Name								OFFSETANA2HISPD									OFFSETANA1HISPD															

Bit	Name	Reset	Access	Description
31:16	OFFSETANA2HISPD	0x0	R	
	High speed mode offset gain adjustment term			
15:0	OFFSETANA1HISPD	0x0	R	
	High speed mode analog offset term at OSR=2x, gain = 1x			

6.4.2.35 DEVINFO_IADC0HISPDOFFSETCAL1 - IADC Offset Calibration

Offset	Bit Position																													
0x198	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	R															
Name																	OFFSETANA3HISPD															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	OFFSETANA3HISPD	0x0	R	
	High-speed mode offset term for OSR>=4x			

6.4.2.36 DEVINFO_LEGACY - Legacy Device Info

Offset	Bit Position																													
0x1FC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset												0x80																				
Access												R																				
Name												DEVICEFAMILY																				

Bit	Name	Reset	Access	Description
31:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:16	DEVICEFAMILY Device Family	0x80	R	**Device Family**

Value	Mode	Description
16	EFR32MG1P	EFR32 Mighty Gecko Family Series 1 Device Config 1
17	EFR32MG1B	EFR32 Mighty Gecko Family Series 1 Device Config 1
18	EFR32MG1V	EFR32 Mighty Gecko Family Series 1 Device Config 1
19	EFR32BG1P	EFR32 Blue Gecko Family Series 1 Device Config 1
20	EFR32BG1B	EFR32 Blue Gecko Family Series 1 Device Config 1
21	EFR32BG1V	EFR32 Blue Gecko Family Series 1 Device Config 1
25	EFR32FG1P	EFR32 Flex Gecko Family Series 1 Device Config 1
26	EFR32FG1B	EFR32 Flex Gecko Family Series 1 Device Config 1
27	EFR32FG1V	EFR32 Flex Gecko Family Series 1 Device Config 1
28	EFR32MG12P	EFR32 Mighty Gecko Family Series 1 Device Config 2
29	EFR32MG12B	EFR32 Mighty Gecko Family Series 1 Device Config 2
30	EFR32MG12V	EFR32 Mighty Gecko Family Series 1 Device Config 2
31	EFR32BG12P	EFR32 Blue Gecko Family Series 1 Device Config 2
32	EFR32BG12B	EFR32 Blue Gecko Family Series 1 Device Config 2
33	EFR32BG12V	EFR32 Blue Gecko Family Series 1 Device Config 2
37	EFR32FG12P	EFR32 Flex Gecko Family Series 1 Device Config 2
38	EFR32FG12B	EFR32 Flex Gecko Family Series 1 Device Config 2
39	EFR32FG12V	EFR32 Flex Gecko Family Series 1 Device Config 2
40	EFR32MG13P	EFR32 Mighty Gecko Family Series 13 Device Config 3
41	EFR32MG13B	EFR32 Mighty Gecko Family Series 13 Device Config 3
42	EFR32MG13V	EFR32 Mighty Gecko Family Series 1 Device Config 3
43	EFR32BG13P	EFR32 Blue Gecko Family Series 1 Device Config 3

Bit	Name	Reset	Access	Description
	44	EFR32BG13B		EFR32 Blue Gecko Family Series 1 Device Config 3
	45	EFR32BG13V		EFR32 Blue Gecko Family Series 1 Device Config 3
	49	EFR32FG13P		EFR32 Flex Gecko Family Series 1 Device Config 3
	50	EFR32FG13B		EFR32 Flex Gecko Family Series 1 Device Config 3
	51	EFR32FG13V		EFR32 Flex Gecko Family Series 1 Device Config 3
	52	EFR32MG14P		EFR32 Mighty Gecko Family Series 1 Device Config 4
	53	EFR32MG14B		EFR32 Mighty Gecko Family Series 1 Device Config 4
	54	EFR32MG14V		EFR32 Mighty Gecko Family Series 1 Device Config 4
	55	EFR32BG14P		EFR32 Blue Gecko Family Series 1 Device Config 4
	56	EFR32BG14B		EFR32 Blue Gecko Family Series 1 Device Config 4
	57	EFR32BG14V		EFR32 Blue Gecko Family Series 1 Device Config 4
	61	EFR32FG14P		EFR32 Flex Gecko Family Series 1 Device Config 4
	62	EFR32FG14B		EFR32 Flex Gecko Family Series 1 Device Config 4
	63	EFR32FG14V		EFR32 Flex Gecko Family Series 1 Device Config 4
	71	EFM32G		EFM32 Gecko Device Family
	72	EFM32GG		EFM32 Giant Gecko Device Family
	73	EFM32TG		EFM32 Tiny Gecko Device Family
	74	EFM32LG		EFM32 Leopard Gecko Device Family
	75	EFM32WG		EFM32 Wonder Gecko Device Family
	76	EFM32ZG		EFM32 Zero Gecko Device Family
	77	EFM32HG		EFM32 Happy Gecko Device Family
	81	EFM32PG1B		EFM32 Pearl Gecko Device Family Series 1 Device Config 1
	83	EFM32JG1B		EFM32 Jade Gecko Device Family Series 1 Device Config 1
	85	EFM32PG12B		EFM32 Pearl Gecko Device Family Series 1 Device Config 2
	87	EFM32JG12B		EFM32 Jade Gecko Device Family Series 1 Device Config 2
	89	EFM32PG13B		EFM32 Pearl Gecko Device Family Series 1 Device Config 3
	91	EFM32JG13B		EFM32 Jade Gecko Device Family Series 1 Device Config 3
	100	EFM32GG11B		EFM32 Giant Gecko Device Family Series 1 Device Config 1
	103	EFM32TG11B		EFM32 Giant Gecko Device Family Series 1 Device Config 1
	120	EZR32LG		EZR32 Leopard Gecko Device Family
	121	EZR32WG		EZR32 Wonder Gecko Device Family
	122	EZR32HG		EZR32 Happy Gecko Device Family
	128	SERIES2V0		DI page is encoded with the series 2 layout. Check alternate location.
15:0	*Reserved*			*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*

6.5 ICACHE - Instruction Cache

The ICACHE provides fast access to recently executed instructions, improving both speed and power consumption of code execution. The instruction cache is enabled by default, but can be disabled by setting CACHEDIS in ICACHE_CTRL. When enabled, the instruction cache typically reduces the number of flash reads significantly, thus saving energy. In most cases, a cache hit-rate of more than 70 % is achievable. When a 32-bit instruction fetch hits in the cache, the data is returned to the processor in one clock cycle, bypassing the flash access wait-states. The cache content is retained in EM2 and EM3.

The instruction cache is connected directly to the CODE bus on the ARM core and functions as a memory access filter between the processor and the memory system, as illustrated in Figure 6.1 Instruction Cache Block Diagram on page 96. The cache consists of an access filter, lookup logic, SRAM, and three performance counters. The access filter checks if a transfer is an instruction fetch located in a cacheable region. If it is the cache lookup logic and SRAM is enabled. Otherwise, the cache is bypassed and the access is forwarded to the memory system. If lookup is enabled data is either returned from the cache (hit) or fetch from the memory system and cached (miss).

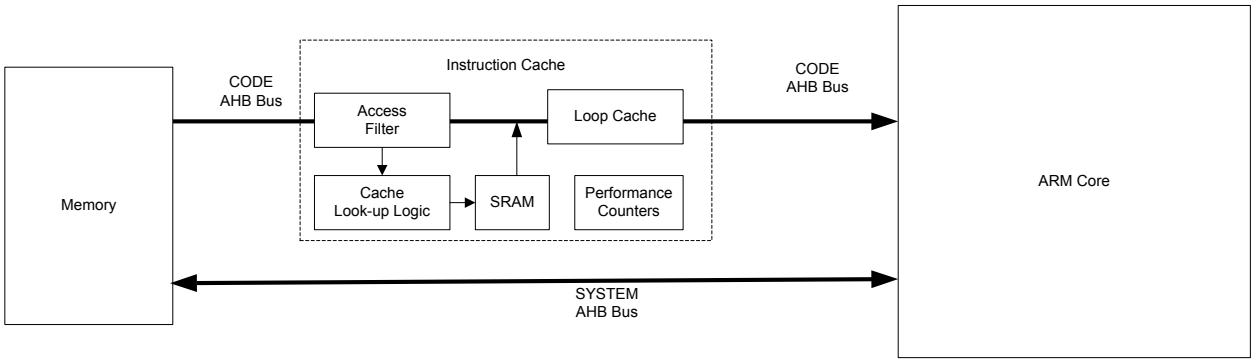


Figure 6.1. Instruction Cache Block Diagram

Note that while all access to code spaces use the CODE bus only instruction fetches are cached. Data accesses to the CODE region are passed through the ICACHE.

6.5.1 Cache Operation

It is highly recommended to keep the cache enabled. To improve cache-efficiency, sections of code with very low cache hit rate should not be cached. This is achieved by placing these code sections in non-cacheable MPU regions and setting USEMPU in ICACHE_CTRL. When USEMPU is set, instruction fetches to non-cacheable MPU regions will not be looked up or saved in cache. This feature may also be used to avoid instructions from low-power memory taking up space from more power-hungry memory. For more information on the MPU see the ARM Cortex-M33 MPU documentation.

The optional loop-cache is optimized to store smaller code-loops efficiently. The loop-cache is enabled when LPLEVEL in ICACHE_LPMODE is set to ADVANCED or MINACTIVITY. The difference between the two settings is that when MINACTIVITY is selected loop-cache outputs may be gated off to reduce power at the cost of more wait-states due to loop-cache misses. Having LPLEVEL set to BASIC disables the loop-cache functionality completely. NESTFACTOR in ICACHE _LPMODE is used to decide when to stick with the currently detected loop rather than start tracking a new loop. Optimal value will depend on the actual code running, meaning that this setting may be tuned for optimal performance.

By default, the instruction cache is automatically invalidated when the contents of the flash are changed (i.e. written or erased). In many cases, however, the application only makes changes to data in the flash, not code. In this case, the automatic invalidate feature can be disabled by setting AUTOFLUSHDIS in ICACHE_CTRL. The cache can also be manually invalidated by writing 1 to FLUSH in ICACHE_CMD.

In the event that a parity error in the cache is detected, the RAMERROR flag will be set in ICACHE_IF. The data is automatically reloaded when this occurs so no action is required by software. This flag is informational only and can be used to detect the rate of corruption events. If RAMERROR in ICACHE_IEN is set, an interrupt will be triggered.

The cache is automatically flushed whenever a bus fault occurs. If this occurs during performance counting the counts will be effected.

6.5.2 Performance Measurement

To measure the hit-rate of a code-section, the built-in performance counters can be used. Before the section, start the performance counters by setting STARTPC in ICACHE_CMD register. This starts the performance counters, counting from 0. At the end of the section, stop the performance counters by setting STOPPC in ICACHE_CMD. The number of cache hits and cache misses for that section can then be read from PCHITS and PCMISSES. The cache hit-ratio can be calculated as PCHITS / (PCHITS + PCMISSES). PCAHITS contains the loopcache hits only. Any hits in PCAHITS are also counted in PCHITS. The loopcache hit-ratio can be calculated as PCAHITS / (PCHITS + PCMISSES). When PCHITS/PCAHITS/PCMISSES overflow, the HITOF/AHITOF/MISSOF interrupt flags are set respectively. These flags must be cleared by software. The range of the performance counters can be extended by increasing a counter in the interrupt routine. The performance counters only count when a cache lookup is performed. Access to non-cacheable regions, data fetches, and access made while the ICACHE is disabled do not increment PCMISSES.

Software may check the if the performance counters are running using PCRUNNING in ICACHE_STATUS.

6.5.3 ICACHE Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	ICACHE_IPVERSION	R	IP Version
0x004	ICACHE_CTRL	RW	Control Register
0x008	ICACHE_PCHITS	RH	Performance Counter Hits
0x00C	ICACHE_PCMISSES	RH	Performance Counter Misses
0x010	ICACHE_PCAHITS	RH	Performance Counter Advanced Hits
0x014	ICACHE_STATUS	RH	Status Register
0x018	ICACHE_CMD	W	Command Register
0x01C	ICACHE_LPMODE	RW	Low Power Mode
0x020	ICACHE_IF	RWH INTFLAG	Interrupt Flag
0x024	ICACHE_IEN	RW	Interrupt Enable
0x1000	ICACHE_IPVERSION_SET	R	IP Version
0x1004	ICACHE_CTRL_SET	RW	Control Register
0x1008	ICACHE_PCHITS_SET	RH	Performance Counter Hits
0x100C	ICACHE_PCMISSES_SET	RH	Performance Counter Misses
0x1010	ICACHE_PCAHITS_SET	RH	Performance Counter Advanced Hits
0x1014	ICACHE_STATUS_SET	RH	Status Register
0x1018	ICACHE_CMD_SET	W	Command Register
0x101C	ICACHE_LPMODE_SET	RW	Low Power Mode
0x1020	ICACHE_IF_SET	RWH INTFLAG	Interrupt Flag
0x1024	ICACHE_IEN_SET	RW	Interrupt Enable
0x2000	ICACHE_IPVERSION_CLR	R	IP Version
0x2004	ICACHE_CTRL_CLR	RW	Control Register
0x2008	ICACHE_PCHITS_CLR	RH	Performance Counter Hits
0x200C	ICACHE_PCMISSES_CLR	RH	Performance Counter Misses
0x2010	ICACHE_PCAHITS_CLR	RH	Performance Counter Advanced Hits
0x2014	ICACHE_STATUS_CLR	RH	Status Register
0x2018	ICACHE_CMD_CLR	W	Command Register
0x201C	ICACHE_LPMODE_CLR	RW	Low Power Mode
0x2020	ICACHE_IF_CLR	RWH INTFLAG	Interrupt Flag
0x2024	ICACHE_IEN_CLR	RW	Interrupt Enable
0x3000	ICACHE_IPVERSION_TGL	R	IP Version
0x3004	ICACHE_CTRL_TGL	RW	Control Register
0x3008	ICACHE_PCHITS_TGL	RH	Performance Counter Hits
0x300C	ICACHE_PCMISSES_TGL	RH	Performance Counter Misses
0x3010	ICACHE_PCAHITS_TGL	RH	Performance Counter Advanced Hits

Offset	Name	Type	Description
0x3014	ICACHE_STATUS_TGL	RH	Status Register
0x3018	ICACHE_CMD_TGL	W	Command Register
0x301C	ICACHE_LPMODE_TGL	RW	Low Power Mode
0x3020	ICACHE_IF_TGL	RWH INTFLAG	Interrupt Flag
0x3024	ICACHE_IEN_TGL	RW	Interrupt Enable

6.5.4 ICACHE Register Description

6.5.4.1 ICACHE_IPVERSION - IP Version

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x0	R	**IP version ID**
	The read only IPVERSION field gives the version for this module. There may be minor software changes required for modules with different values of IPVERSION.			

6.5.4.2 ICACHE_CTRL - Control Register

Offset	Bit Position																														
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x0	0x0	0x0
Access																														RW	RW	RW
Name																														AUTOFLUSHDIS	USEMPU	CACHEDIS

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	AUTOFLUSHDIS	0x0	RW	**Automatic Flushing Disable**
	Disables automatic flushing based on Internal Flash write/erase			
1	USEMPU	0x0	RW	**Use MPU**
	Use MPU to select non/cacheable regions			
0	CACHEDIS	0x0	RW	**Cache Disable**
	Disables caching for all regions			

6.5.4.3 ICACHE_PCHITS - Performance Counter Hits

Offset	Bit Position																														
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	PCHITS																															

Bit	Name	Reset	Access	Description
31:0	PCHITS	0x0	R	**Performance Counter Hits**
	Hit counter value			

6.5.4.4 ICACHE_PCMISSES - Performance Counter Misses

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	PCMISSES																															

Bit	Name	Reset	Access	Description
31:0	PCMISSES	0x0	R	**Performance Counter Misses**
	Miss counter value			

6.5.4.5 ICACHE_PCAHITS - Performance Counter Advanced Hits

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	PCAHITS																															

Bit	Name	Reset	Access	Description
31:0	PCAHITS	0x0	R	**Performance Counter Advanced Hits**
	Hit counter value for hits due to Advanced Buffering mode. These hits are also represented in PCHITS.			

6.5.4.6 ICACHE_STATUS - Status Register

Offset	Bit Position																														
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																R
Name																																PCRUNNING

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	PCRUNNING	0x0	R	**PC Running**
	Performance Counters are running			

6.5.4.7 ICACHE_CMD - Command Register

Offset	Bit Position																														
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x0	0x0	0x0
Access																														W(nB)	W(nB)	W(nB)
Name																														STOPPC	STARTPC	FLUSH

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	STOPPC	0x0	W(nB)	**Stop Performance Counters**
	Stops the Performance Counters			
1	STARTPC	0x0	W(nB)	**Start Performance Counters**
	Starts the Performance Counters			
0	FLUSH	0x0	W(nB)	**Flush**
	Clears Cached Data			

6.5.4.8 ICACHE_LPMODE - Low Power Mode

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x2						0x3	
Access																									RW						RW	
Name																									NESTFACTOR						LPLEVEL	

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:4	NESTFACTOR	0x2	RW	**Low Power Nest Factor** Parameter used in the advanced buffering mode to control its estimation when a branch access is likely to be accssed in the near future. In general, a higher number will improve performance in code with deeply nested loops.
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	LPLEVEL	0x3	RW	**Low Power Level** Controls the low-power level of the cache. In general, the default setting is best for most applications.

Value	Mode	Description
0	BASIC	Base instruction cache functionality
1	ADVANCED	Advanced buffering mode, where the cache uses the fetch pattern to predict highly accessed data and store it in low-energy memory
3	MINACTIVITY	Minimum activity mode, which allows the cache to minimize activity in logic that it predicts has a low probability being used. This mode can introduce wait-states into the instruction fetch stream when the cache exits one of its low-activity states. The number of wait-states introduced is small, but users running with 0-wait-state memory and wishing to reduce the variability that the cache might introduce with additional wait-states may wish to lower the cache low-power level. Note, this mode includes the advanced buffering mode functionality.

6.5.4.9 ICACHE_IF - Interrupt Flag

Offset	Bit Position																														
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																								0x0						0x0	0x0	0x0
Access																								RW						RW	RW	RW
Name																								RAMERROR						AHITOF	MISSOF	HITOF

Bit	Name	Reset	Access	Description
31:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8	RAMERROR	0x0	RW	**RAM error Interrupt Flag**
	RAM parity error detected			
7:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	AHITOF	0x0	RW	**Advanced Hit Overflow Interrupt Flag**
	Advanced hit performance counter has overflowed			
1	MISSOF	0x0	RW	**Miss Overflow Interrupt Flag**
	Miss performance counter has overflowed			
0	HITOF	0x0	RW	**Hit Overflow Interrupt Flag**
	Hit performance counter has overflowed			

6.5.4.10 ICACHE_IEN - Interrupt Enable

Offset	Bit Position																														
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																								0x0						0x0	0x0	0x0
Access																								RW						RW	RW	RW
Name																								RAMERROR						AHITOF	MISSOF	HITOF

Bit	Name	Reset	Access	Description
31:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8	RAMERROR	0x0	RW	**RAM error Interrupt Enable**
	Enable RAMERROR interrupt			
7:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	AHITOF	0x0	RW	**Advanced Hit Overflow Interrupt Enable**
	Enable AHITOF interrupt			
1	MISSOF	0x0	RW	**Miss Overflow Interrupt Enable**
	Enable MISSOF interrupt			
0	HITOF	0x0	RW	**Hit Overflow Interrupt Enable**
	Enable HITOF interrupt			

6.6 SYSCFG - System Configuration

The SYSCFG block is used to configure SRAM. It also contains some interrupt flags for software use. The system has the following major SRAM blocks:

- DMEM0 - Primary system data memory (RAM)
- FRCRAM - Frame Rate Controller SRAM
- SEQRAM - Sequencer SRAM
- DEMODRAM - Demodulator SRAM

6.6.1 Ram Retention

DMEM0 is broken into 32 KB banks. By default all banks are retained in EM2/EM3. Sleep mode current can be significantly reduced by fully powering down banks that do not need to be retained. To select the amount of RAM to be powered down in EM2/EM3, set RAMRETNCTRL in SYSCFG_DMEM0RETNCTRL to the desired value.

FRCRAM and SEQRAM may be powered down in EM2/EM3 if not required. To disable retention, set FRCRAMRETNCTRL or SEQRAMRETNCTRL in SYSCFG_RADIORAMRETNCTRL.

6.6.2 ECC

DMEM0, FRCRAM, and SEQRAM support one bit correction and two bit detection ECC.

To enable error detection for FRCRAM and SEQRAM, set FRCRAMECCCHKEN and SEQRAMECCCHKEN in SYSCFG_RADIOECCCTRL. To enable auto-correction of one bit errors in FRCRAM and SEQRAM, set FRCRAMECCEWEN and SEQRAMECCEWEN in SYSCFG_RADIOECCCTRL. When ECC error events in FRCRAM and SEQRAM are detected, the corresponding flags in SYSCFG_IF are set. When a flag is set, an interrupt will be triggered if the corresponding interrupt enable bit is set in SYSCFG_IEN. When an error occurs, the address of the detected error is written to SYSCFG_FRCRAMECCADDR or SYSCF_SEQRAMECCERR depending on the source of the error.

To enable error detection for DMEM0, set ECCEN in MPAHBRAM_CTRL. To enable auto-correction of one bit errors in DMEM0, set ECCWEN in MPAHBRAM_CTRL.

When ECC error events in DMEM0 are detected, the corresponding bits in MPAHBRAM_IF are set. Errors arising from a specific port 'x' will be indicated by the AHBxERR1B or AHBxERR2B flags. When a flag is set, an interrupt will be triggered if the corresponding interrupt enable bit is set in MPAHBRAM_IEN. When an error occurs, the address of the detected error is written to MPAHBRAM_ECCERRADDRx for the respective port 'x'. The address registers are sticky and will not be loaded with a new address until they are cleared through MPAHBRAM_CMD.CLEARECCADDRx. If multiple ECC errors occur without ECCERRADDRn being cleared, the Px bit in MPAHBRAM_ECCMERRIND will be set. These status bits are also sticky, and are cleared with MPAHBRAM_CMD.CLEARECCADDRx.

Upon a two bit ECC error in DMEM, MPAHBRAM can also issue a bus fault. To enable this, set the ECCERRFAULTEN bit in MPAHBRAM_CTRL.

The recommend procedure for initializing ECC RAM is to first enable ECC, then write zeros to all locations. This will clear the RAM and initialize the syndrome. If the ECC RAM is not written as described, then any reads to uninitialized RAM locations will result in an ECC error.

Note: The RAM ECC feature must be enabled to achieve good long term reliability. The long term reliability of the RAM is only specified with ECC enabled.

6.6.3 Software Interrupts

The SYSCFG block also provides some software interrupts that can be used to communicate between software tasks. To trigger a software interrupt set the corresponding bit in SYSCFG_IF.

6.6.4 Bus faults

By default, two bit ECC errors and reads to unmapped addresses trigger a BusFault. These bus fault sources can be disabled by clearing RAMECCERRFAULTEN and ADDRFAULTEN in SYSCFG_CTRL.

6.6.5 SYSCFG Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x004	SYSCFG_IPVERSION	R	IP Version ID
0x008	SYSCFG_IF	RWH INTFLAG	Interrupt Flag
0x00C	SYSCFG_IEN	RW	Interrupt Enable
0x014	SYSCFG_CHIPREVHW	RWH	Chip Revision, Hard-Wired
0x018	SYSCFG_CHIPREV	RW	Chip Revision
0x024	SYSCFG_CFGSYSTIC	RW	Configure Sys-Tick
0x200	SYSCFG_CTRL	RW	Control
0x208	SYSCFG_DMEM0RETNCTRL	RW	DMEM0 Retention Control
0x30C	SYSCFG_RAMBIASCONF	RW	RAM Bias Configuration
0x400	SYSCFG_RADIORAM-RETNCTRL	RW	RADIO SEQRAM Retention Control
0x408	SYSCFG_RADIOECCCTRL	RW	RADIO SEQRAM ECC Control Register
0x410	SYSCFG_SEQRAMECCADDR	RH	SEQRAM ECC Address
0x414	SYSCFG_FRCRAMECCADDR	RH	FRCRAM ECC Address
0x418	SYSCFG_ICACHERAM-RETNCTRL	RW	HOST ICACHERAM Retention Control
0x41C	SYSCFG_DMEM0PORTMAP-SEL	RW	DMEM0 Port Remap Selection
0x600	SYSCFG_ROOTDATA0	RW	Data Register 0
0x604	SYSCFG_ROOTDATA1	RW	Data Register 1
0x608	SYSCFG_ROOTLOCKSTATUS	RH	Lock Status
0x60C	SYSCFG_ROOTSESWVER-SION	RW	SE SW Version
0x1004	SYSCFG_IPVERSION_SET	R	IP Version ID
0x1008	SYSCFG_IF_SET	RWH INTFLAG	Interrupt Flag
0x100C	SYSCFG_IEN_SET	RW	Interrupt Enable
0x1014	SYSCFG_CHIPREVHW_SET	RWH	Chip Revision, Hard-Wired
0x1018	SYSCFG_CHIPREV_SET	RW	Chip Revision
0x1024	SYSCFG_CFGSYSTIC_SET	RW	Configure Sys-Tick
0x1200	SYSCFG_CTRL_SET	RW	Control
0x1208	SYSCFG_DMEM0RETNCTRL_SET	RW	DMEM0 Retention Control
0x130C	SYSCFG_RAMBIASCONF_SET	RW	RAM Bias Configuration
0x1400	SYSCFG_RADIORAM-RETNCTRL_SET	RW	RADIO SEQRAM Retention Control
0x1408	SYSCFG_RADIO-ECCCTRL_SET	RW	RADIO SEQRAM ECC Control Register

Offset	Name	Type	Description
0x1410	SYSCFG_SEQRAMEC-CADDR_SET	RH	SEQRAM ECC Address
0x1414	SYSCFG_FRCRAMEC-CADDR_SET	RH	FRCRAM ECC Address
0x1418	SYSCFG_ICACHERAM-RETNCTRL_SET	RW	HOST ICACHERAM Retention Control
0x141C	SYSCFG_DMEM0PORTMAP-SEL_SET	RW	DMEM0 Port Remap Selection
0x1600	SYSCFG_ROOTDATA0_SET	RW	Data Register 0
0x1604	SYSCFG_ROOTDATA1_SET	RW	Data Register 1
0x1608	SYSCFG_ROOTLOCKSTA-TUS_SET	RH	Lock Status
0x160C	SYSCFG_ROOTSESWVER-SION_SET	RW	SE SW Version
0x2004	SYSCFG_IPVERSION_CLR	R	IP Version ID
0x2008	SYSCFG_IF_CLR	RWH INTFLAG	Interrupt Flag
0x200C	SYSCFG_IEN_CLR	RW	Interrupt Enable
0x2014	SYSCFG_CHIPREVHW_CLR	RWH	Chip Revision, Hard-Wired
0x2018	SYSCFG_CHIPREV_CLR	RW	Chip Revision
0x2024	SYSCFG_CFGSYSTIC_CLR	RW	Configure Sys-Tick
0x2200	SYSCFG_CTRL_CLR	RW	Control
0x2208	SYSCFG_DMEM0RETNCTRL_CLR	RW	DMEM0 Retention Control
0x230C	SYSCFG_RAMBIASCONF_CLR	RW	RAM Bias Configuration
0x2400	SYSCFG_RADIORAM-RETNCTRL_CLR	RW	RADIO SEQRAM Retention Control
0x2408	SYSCFG_RADIO-ECCCTRL_CLR	RW	RADIO SEQRAM ECC Control Register
0x2410	SYSCFG_SEQRAMEC-CADDR_CLR	RH	SEQRAM ECC Address
0x2414	SYSCFG_FRCRAMEC-CADDR_CLR	RH	FRCRAM ECC Address
0x2418	SYSCFG_ICACHERAM-RETNCTRL_CLR	RW	HOST ICACHERAM Retention Control
0x241C	SYSCFG_DMEM0PORTMAP-SEL_CLR	RW	DMEM0 Port Remap Selection
0x2600	SYSCFG_ROOTDATA0_CLR	RW	Data Register 0
0x2604	SYSCFG_ROOTDATA1_CLR	RW	Data Register 1
0x2608	SYSCFG_ROOTLOCKSTA-TUS_CLR	RH	Lock Status
0x260C	SYSCFG_ROOTSESWVER-SION_CLR	RW	SE SW Version
0x3004	SYSCFG_IPVERSION_TGL	R	IP Version ID

Offset	Name	Type	Description
0x3008	SYSCFG_IF_TGL	RWH INTFLAG	Interrupt Flag
0x300C	SYSCFG_IEN_TGL	RW	Interrupt Enable
0x3014	SYSCFG_CHIPREVHW_TGL	RWH	Chip Revision, Hard-Wired
0x3018	SYSCFG_CHIPREV_TGL	RW	Chip Revision
0x3024	SYSCFG_CFGSYSTIC_TGL	RW	Configure Sys-Tick
0x3200	SYSCFG_CTRL_TGL	RW	Control
0x3208	SYSCFG_DMEM0RETNCTRL_TGL	RW	DMEM0 Retention Control
0x330C	SYSCFG_RAMBIASCONF_TGL	RW	RAM Bias Configuration
0x3400	SYSCFG_RADIORAM-RETNCTRL_TGL	RW	RADIO SEQRAM Retention Control
0x3408	SYSCFG_RADIO-ECCCTRL_TGL	RW	RADIO SEQRAM ECC Control Register
0x3410	SYSCFG_SEQRAMEC-CADDR_TGL	RH	SEQRAM ECC Address
0x3414	SYSCFG_FRCRAMEC-CADDR_TGL	RH	FRCRAM ECC Address
0x3418	SYSCFG_ICACHERAM-RETNCTRL_TGL	RW	HOST ICACHERAM Retention Control
0x341C	SYSCFG_DMEM0PORTMAP-SEL_TGL	RW	DMEM0 Port Remap Selection
0x3600	SYSCFG_ROOTDATA0_TGL	RW	Data Register 0
0x3604	SYSCFG_ROOTDATA1_TGL	RW	Data Register 1
0x3608	SYSCFG_ROOTLOCKSTA-TUS_TGL	RH	Lock Status
0x360C	SYSCFG_ROOTSESWVER-SION_TGL	RW	SE SW Version

6.6.6 SYSCFG Register Description

6.6.6.1 SYSCFG_IPVERSION - IP Version ID

Offset	Bit Position																															
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x4																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x4	R	**New BitField**
	ID indicating version of IP			

6.6.6.2 SYSCFG_IF - Interrupt Flag

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset			0x0	0x0			0x0	0x0		0x0	0x0	0x0		0x0	0x0	0x0	0x0		0x0	0x0	0x0	0x0	0x0	0x0					0x0	0x0	0x0	0x0
Access			RW	RW			RW	RW		RW	RW	RW		RW	RW	RW	RW		RW	RW	RW	RW	RW	RW					RW	RW	RW	RW
Name			FRCRAMERR2B	FRCRAMERR1B			SEQRAMERR2B	SEQRAMERR1B		SOFTMITCMRAMERRIF	SOFTMDTCMRAMERRIF	SOFTMBUSERRIF		SOFTM2SRWBUSERR	SRW2SOFTMBUSERR	SRW2HOSTBUSERR	HOST2SRWBUSERR		FPIXC	FPIDC	FPOFC	FPUFC	FPDZC	FPIOC					SW3	SW2	SW1	SW0

Bit	Name	Reset	Access	Description
31:30	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
29	FRCRAMERR2B	0x0	RW	**FRCRAM Error 2-bit Interrupt Flag**
	FRCRAM 2-bit ECC Error Interrupt flag.			
28	FRCRAMERR1B	0x0	RW	**FRCRAM Error 1-bit Interrupt Flag**
	FRCRAM 1-bit ECC Error Interrupt flag.			
27:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25	SEQRAMERR2B	0x0	RW	**SEQRAM Error 2-bit Interrupt Flag**
	SEQRAM 2-bit ECC Error Interrupt flag.			
24	SEQRAMERR1B	0x0	RW	**SEQRAM Error 1-bit Interrupt Flag**
	SEQRAM 1-bit ECC Error Interrupt flag.			
23	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
22	SOFTMITCMRAMER-RIF	0x0	RW	**Softm ITCM Error Interrupt Flag**
	SOFTM ITCM RAM ECC Error Interrupt flag.			
21	SOFTMDTCMRAMER-RIF	0x0	RW	**Softm DTCM Error Interrupt Flag**
	SOFTM DTCM RAM ECC Error Interrupt flag.			
20	SOFTMBUSERRIF	0x0	RW	**Softm bus error Interrupt Flag**
	Softmodem bus error (internal OBI error) interrupt			
19	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
18	SOFTM2SRWBUSERR	0x0	RW	**SOFTM2SRWBUSERR Interrupt Flag**
	AHB Softmodem to AHB SRW Bus Error Interrupt Flag			
17	SRW2SOFTMBUSERR	0x0	RW	**SRW2SOFTMBUSERR Interrupt Flag**

Bit	Name	Reset	Access	Description
	AHB SRW to AHB Softmodem Bus Error Interrupt Flag			
16	SRW2HOSTBUSERR	0x0	RW	**SRW2HOSTBUSERR Interrupt Flag**
	AHB SRW to AHB HOST Bus Error Interrupt Flag			
15	HOST2SRWBUSERR	0x0	RW	**HOST2SRWBUSERR Interrupt Flag**
	AHB Host to AHB SRW Bus Error Interrupt Flag			
14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13	FPIXC	0x0	RW	**FPU Inexact interrupt flag**
	Set upon FPU inexact exception			
12	FPIDC	0x0	RW	**FPU Input denormal interrupt flag**
	Set upon FPU input denormal exception			
11	FPOFC	0x0	RW	**FPU Overflow interrupt flag**
	Set upon FPU overflow exception			
10	FPUFC	0x0	RW	**FPU Underflow interrupt flag**
	Set upon FPU underflow exception			
9	FPDZC	0x0	RW	**FPU Divide by zero interrupt flag**
	Set upon FPU divide by zero operation			
8	FPIOC	0x0	RW	**FPU Invalid Operation interrupt flag**
	Set upon FPU invalid operation			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	SW3	0x0	RW	**Software Interrupt Flag**
	Software interrupts			
2	SW2	0x0	RW	**Software Interrupt Flag**
	Software interrupts			
1	SW1	0x0	RW	**Software Interrupt Flag**
	Software interrupts			
0	SW0	0x0	RW	**Software Interrupt Flag**
	Software interrupts			

6.6.6.3 SYSCFG_IEN - Interrupt Enable

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset			0x0	0x0			0x0	0x0		0x0	0x0	0x0		0x0	0x0	0x0	0x0		0x0	0x0	0x0	0x0	0x0	0x0					0x0	0x0	0x0	0x0
Access			RW	RW			RW	RW		RW	RW	RW		RW	RW	RW	RW		RW	RW	RW	RW	RW	RW					RW	RW	RW	RW
Name			FRCRAMERR2B	FRCRAMERR1B			SEQRAMERR2B	SEQRAMERR1B		SOFTMITCMRAMERRIEN	SOFTMDTCMRAMERRIEN	SOFTMBUSERRIEN		SOFTM2SRWBUSERR	SRW2SOFTMBUSERR	SRW2HOSTBUSERR	HOST2SRWBUSERR		FPIXC	FPIDC	FPOFC	FPUFC	FPDZC	FPIOC					SW3	SW2	SW1	SW0

Bit	Name	Reset	Access	Description
31:30	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
29	FRCRAMERR2B	0x0	RW	**FRCRAM Error 2-bit Interrupt Enable**
	Set to enable the FRCRAM2ERR2BIF Interrupt			
28	FRCRAMERR1B	0x0	RW	**FRCRAM Error 1-bit Interrupt Enable**
	Set to enable the FRCRAM2ERR1BIF Interrupt			
27:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25	SEQRAMERR2B	0x0	RW	**SEQRAM Error 2-bit Interrupt Enable**
	Set to enable the SEQRAM2ERR2BIF Interrupt			
24	SEQRAMERR1B	0x0	RW	**SEQRAM Error 1-bit Interrupt Enable**
	Set to enable the SEQRAM2ERR1BIF Interrupt			
23	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
22	SOFTMITCMRAMER-RIEN	0x0	RW	**Softm ITCM Error Interrupt Enable**
	SOFTM ITCM RAM ECC Error Interrupt enable			
21	SOFTMDTCMRAMER-RIEN	0x0	RW	**Softm DTCM Error Interrupt Enable**
	SOFTM DTCM RAM ECC Error Interrupt enable			
20	SOFTMBUSERRIEN	0x0	RW	**Softm bus error interrupt Enable**
	Softmodem bus error interrupt enable			
19	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
18	SOFTM2SRWBUSERR	0x0	RW	**SOFTM2SRWBUSERR Interrupt Enable**
	Set to enable the SOFTM2SRWBUSERR Interrupt			
17	SRW2SOFTMBUSERR	0x0	RW	**SRW2SOFTMBUSERR Interrupt Enable**

Bit	Name	Reset	Access	Description
	Set to enable the SRW2SOFTMBUSERR Interrupt			
16	SRW2HOSTBUSERR	0x0	RW	**SRW2HOSTBUSERR Interrupt Enable**
	Set to enable the SRW2HOSTBUSERR Interrupt			
15	HOST2SRWBUSERR	0x0	RW	**HOST2SRWBUSERR Interrupt Enable**
	Set to enable the HOST2SRWBUSERR Interrupt			
14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13	FPIXC	0x0	RW	**FPU Inexact Interrupt Enable**
	Set to enable the FPIXCIF Interrupt			
12	FPIDC	0x0	RW	**FPU Input denormal Interrupt Enable**
	Set to enable the FPIDCIF Interrupt			
11	FPOFC	0x0	RW	**FPU Overflow Interrupt Enable**
	Set to enable the FPOFCIF Interrupt			
10	FPUFC	0x0	RW	**FPU Underflow Interrupt Enable**
	Set to enable the FPUFCIF Interrupt			
9	FPDZC	0x0	RW	**FPU Divide by zero Interrupt Enable**
	Set to enable the FPDZCIF Interrupt			
8	FPIOC	0x0	RW	**FPU Invalid Operation Interrupt Enable**
	Set to enable the FPIOCIF Interrupt			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	SW3	0x0	RW	**Software Interrupt Enable**
	Set to enable the Software Interrupts			
2	SW2	0x0	RW	**Software Interrupt Enable**
	Set to enable the Software Interrupts			
1	SW1	0x0	RW	**Software Interrupt Enable**
	Set to enable the Software Interrupts			
0	SW0	0x0	RW	**Software Interrupt Enable**
	Set to enable the Software Interrupts			

6.6.6.4 SYSCFG_CHIPREVHW - Chip Revision, Hard-Wired

Offset	Bit Position																															
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x1				0x0				0x10											
Access													RW				RW				RW											
Name													MAJOR				MINOR				PARTNUMBER											

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	MAJOR	0x1	RW	**Hardwired Chip Revision Major value**
	Hardwired Chip Revision Major signal value			
15:12	MINOR	0x0	RW	**Hardwired Chip Revision Minor value**
	Hardwired Chip Revision Minor signal value			
11:0	PARTNUMBER	0x10	RW	**Hardwired Chip Part Number value**
	Hardwired Chip Part Number signal value			

6.6.6.5 SYSCFG_CHIPREV - Chip Revision

Offset	Bit Position																															
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0				0x0				0x0											
Access													RW				RW				RW											
Name													MAJOR				MINOR				PARTNUMBER											

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	MAJOR	0x0	RW	**Chip Revision Major value**
	Chip Revision Major value			
15:12	MINOR	0x0	RW	**Chip Revision Minor value**
	Chip Revision Minor value			
11:0	PARTNUMBER	0x0	RW	**Chip Part Number value**
	Chip Family value			

6.6.6.6 SYSCFG_CFGSYSTIC - Configure Sys-Tick

Offset	Bit Position																															
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																RW
Name																																SYSTICEXTCLKEN

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	SYSTICEXTCLKEN	0x0	RW	**System-Tick External Clock Enable**
	Set 1 to use an external clock as the M33 System Tick.			

6.6.6.7 SYSCFG_CTRL - Control

Offset	Bit Position																														
0x200	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x1				0x1	0x1
Access																											RW				RW	RW
Name																											RAMECCERRFAULTEN				CLKDISFAULTEN	ADDRFAULTEN

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	RAMECCERRFAULTEN	0x1	RW	**Two bit ECC error bus fault response ena**
	When this bit is set, busfaults are generated if 2-bit ECC error occurs.			
4:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	CLKDISFAULTEN	0x1	RW	**Disabled Clkbus Bus Fault Enable**
	When this bit is set, busfaults are generated on accesses to peripherals with disabled bus clock			
0	ADDRFAULTEN	0x1	RW	**Invalid Address Bus Fault Response Enabl**
	When this bit is set, busfaults are generated on accesses to unmapped parts of system and code address space			

6.6.6.8 SYSCFG_DMEM0RETNCTRL - DMEM0 Retention Control

Offset	Bit Position																													
0x208	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									RW							
Name																									RAMRETNCTRL							

Bit	Name	Reset	Access	Description
31:15	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
14:0	RAMRETNCTRL	0x0	RW	**DMEM0 blockset retention control**

DMEM0 RAM blockset retention controls in EM23 with full access in EM01.

Value	Mode	Description
0	ALLON	None of the RAM blocks powered down
16384	BLK15	Power down RAM block 15
24576	BLK14TO15	Power down RAM blocks 14 and above
28672	BLK13TO15	Power down RAM blocks 13 and above
30720	BLK12TO15	Power down RAM blocks 12 and above
31744	BLK11TO15	Power down RAM blocks 11 and above
32256	BLK10TO15	Power down RAM blocks 10 and above
32512	BLK9TO15	Power down RAM blocks 9 and above
32640	BLK8TO15	Power down RAM blocks 8 and above
32704	BLK7TO15	Power down RAM blocks 7 and above
32736	BLK6TO15	Power down RAM blocks 6 and above
32752	BLK5TO15	Power down RAM blocks 5 and above
32760	BLK4TO15	Power down RAM blocks 4 and above
32764	BLK3TO15	Power down RAM blocks 3 and above
32766	BLK2TO15	Power down RAM blocks 2 and above
32767	BLK1TO15	Power down RAM blocks 1 and above

6.6.6.9 SYSCFG_RAMBIASCONF - RAM Bias Configuration

Offset	Bit Position																															
0x30C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x2		
Access																													RW		
Name																													RAMBIASCTRL		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	RAMBIASCTRL	0x2	RW	**RAM Bias Control**

RAM blockset Bias control. Voltage Source Bias control setting

Value	Mode	Description
0	NO	None
1	VSB100	Voltage Source Bias 100mV
2	VSB200	Voltage Source Bias 200mV
4	VSB300	Voltage Source Bias 300mV
8	VSB400	Voltage Source Bias 400mV

6.6.6.10 SYSCFG_RADIORAMRETNCTRL - RADIO SEQRAM Retention Control

Offset	Bit Position																															
0x400	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0						0x0				0x0													0x0							0x0	
Access	RW						RW				RW													RW							RW	
Name	AHBRAMRETNCTRL						DTCRAMRETNCTRL				ITCRAMRETNCTRL													FRCRAMRETNCTRL							SEQRAMRETNCTRL	

Bit	Name	Reset	Access	Description
31:28	AHBRAMRETNCTRL	0x0	RW	**AHBRAM Retention Control**

Soft Modem AHB RAM power-down in EM23 with full access in EM01

Value	Mode	Description
0	ALLON	no banks powered down
8	BLK3	power down blk3
12	BLK2TO3	power down blk 2 to 3
14	BLK1TO3	power down blk 1 to 3
15	ALLOFF	power down all blocks

27:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*

25:24	DTCRAMRETNCTRL	0x0	RW	**DTCRAM Retention Control**

Soft Modem DTC RAM power-down in EM23 with full access in EM01

Value	Mode	Description
0	ALLON	None of the RAMs powered down
2	BLK1	
3	ALLOFF	

23:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*

21:12	ITCRAMRETNCTRL	0x0	RW	**ITCRAM Retention Control**

Soft Modem ITC RAM power-down in EM23 with full access in EM01

Value	Mode	Description
0	ALLON	None of the RAM blocks powered down
512	BLK9	Power down RAM block 9
768	BLK8TO9	Power down RAM block 8 and above
896	BLK7TO9	Power down RAM block 7 and above

Bit	Name	Reset	Access	Description
	960	BLK6TO9		Power down RAM block 6 and above
	992	BLK5TO9		Power down RAM block 5 and above
	1008	BLK4TO9		Power down RAM block 4 and above
	1016	BLK3TO9		Power down RAM block 3 and above
	1020	BLK2TO9		Power down RAM block 2 and above
	1022	BLK1TO9		Power down RAM block 1 and above
	1023	ALLOFF		All of the RAM blocks powered down
11:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8	FRCRAMRETNCTRL	0x0	RW	**FRCRAM Retention Control**
	FRC RAM power-down in EM23 with full access in EM01			
	Value	Mode		Description
	0	ALLON		FRCRAM not powered down
	1	ALLOFF		Power down FRCRAM
7:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2:0	SEQRAMRETNCTRL	0x0	RW	**SEQRAM Retention Control**
	SEQUENCER RAM power-down in EM23 with full access in EM01			
	Value	Mode		Description
	0	ALLON		SEQRAM not powered down
	1	BLK0		Power down SEQRAM block 0
	2	BLK1		Power down SEQRAM block 1
	4	BLK2		Power down SEQRAM block 2
	6	BLK1TO2		Power down SEQRAM block 1 to 2
	7	ALLOFF		Power down all SEQRAM blocks

6.6.6.11 SYSCFG_RADIOECCCTRL - RADIO SEQRAM ECC Control Register

Offset	Bit Position																													
0x408	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0	0x0							0x0	0x0
Access																							RW	RW							RW	RW
Name																							FRCRAMECCEWEN	FRCRAMECCEN							SEQRAMECCEWEN	SEQRAMECCEN

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	FRCRAMECCEWEN	0x0	RW	**FRCRAM ECC Error Writeback Enable**
	FRC ECC Error Writeback Enable. When set, errors will be corrected when encountered.			
8	FRCRAMECCEN	0x0	RW	**FRCRAM ECC Enable**
	FRCRAM ECC Enable.			
7:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	SEQRAMECCEWEN	0x0	RW	**SEQRAM ECC Error Writeback Enable**
	SEQRAM ECC Error Writeback Enable. When set, errors will be corrected when encountered.			
0	SEQRAMECCEN	0x0	RW	**SEQRAM ECC Enable**
	SEQRAM ECC Enable.			

6.6.6.12 SYSCFG_SEQRAMECCADDR - SEQRAM ECC Address

Offset	Bit Position																													
0x410	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	SEQRAMECCADDR																															

Bit	Name	Reset	Access	Description
31:0	SEQRAMECCADDR	0x0	R	**SEQRAM ECC Address**
	Indicates Address of SEQRAM at which ECC error occured			

6.6.6.13 SYSCFG_FRCRAMECCADDR - FRCRAM ECC Address

Offset	Bit Position																													
0x414	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	FRCRAMECCADDR																															

Bit	Name	Reset	Access	Description
31:0	FRCRAMECCADDR	0x0	R	**FRCRAM ECC Error Address**
	Indicates Address of FRCRAM at which ECC error occured			

6.6.6.14 SYSCFG_ICACHERAMRETNCTRL - HOST ICACHERAM Retention Control

Offset	Bit Position																														
0x418	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																RW
Name																																RAMRETNCTRL

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	RAMRETNCTRL	0x0	RW	**ICACHERAM Retention control**

Host ICACHE RAM power-down in EM23 with full access in EM01.

Value	Mode	Description
0	ALLON	None of the Host ICACHE RAM blocks powered down
1	ALLOFF	Power down all Host ICACHE RAM blocks

6.6.6.15 SYSCFG_DMEM0PORTMAPSEL - DMEM0 Port Remap Selection

Offset	Bit Position																													
0x41C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																								0x0	0x1	0x0	0x0	0x1	0x0	0x0	0x1	0x1
Access																								RW	RW	RW	RW	RW	RW	RW	RW	RW
Name																								BUFCPORTSEL	USBPORTSEL	SRWLDMAPORTSEL	LDMA1PORTSEL	SRWECA1PORTSEL	SRWECA0PORTSEL	AHBSRWPORTSEL	SRWAESPORTSEL	LDMAPORTSEL

Bit	Name	Reset	Access	Description
31:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8	BUFCPORTSEL	0x0	RW	**BUFC portmap selection**
	BUFC address remap selection, default configured to MPAHBRAM0			
7	USBPORTSEL	0x1	RW	**USB portmap selection**
	USB address remap selection, default configured to MPAHBRAM1			
6	SRWLDMAPORTSEL	0x0	RW	**SRWLDMA port1 portmap selection**
	SRWLDMA port1 address remap selection, default configured to MPAHBRAM0			
5	LDMA1PORTSEL	0x0	RW	**LDMA port1 portmap selection**
	LDMA port 1 address remap selection, default configured to MPAHBRAM0			
4	SRWECA1PORTSEL	0x1	RW	**SRWECA1 portmap selection**
	SRWECA1 address remap selection, default configured to MPAHBRAM1			
3	SRWECA0PORTSEL	0x0	RW	**SRWECA0 portmap selection**
	SRWECA0 address remap selection, default configured to MPAHBRAM0			
2	AHBSRWPORTSEL	0x0	RW	**AHBSRW portmap selection**
	AHBSRW address remap selection, default configured to MPAHBRAM0			
1	SRWAESPORTSEL	0x1	RW	**SRWAES portmap selection**
	SRWAES address remap selection, default configured to MPAHBRAM1			
0	LDMAPORTSEL	0x1	RW	**LDMA portmap selection**
	LDMA address remap selection, default configured to MPAHBRAM1			

6.6.6.16 SYSCFG_ROOTDATA0 - Data Register 0

Offset	Bit Position																													
0x600	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	DATA																															

Bit	Name	Reset	Access	Description
31:0	DATA	0x0	RW	**Data**
	Generic data space for user to pass to root, e.g., address of struct in mem			

6.6.6.17 SYSCFG_ROOTDATA1 - Data Register 1

Offset	Bit Position																													
0x604	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	DATA																															

Bit	Name	Reset	Access	Description
31:0	DATA	0x0	RW	**Data**
	Generic data space for user to pass to root, e.g., address of struct in mem			

6.6.6.18 SYSCFG_ROOTLOCKSTATUS - Lock Status

Offset	Bit Position																														
0x608	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0									0x1	0x1	0x1	0x1	0x1	0x1	0x1								0x1						0x1	0x1	0x1
Access	R									R	R	R	R	R	R	R								R						R	R	R
Name	EFUSEUNLOCKED									RADIOSMDBGLOCK	RADIODBGLOCK	USERSPNIDLOCK	USERSPIDLOCK	USERNIDLOCK	USERDBGLOCK	USERDBGAPLOCK								ROOTDBGLOCK						MFRLOCK	REGLOCK	BUSLOCK

Bit	Name	Reset	Access	Description
31	EFUSEUNLOCKED	0x0	R	**E-Fuse Unlocked**
	E-Fuse Unlocked when 1; Locked when 0.			
30:23	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
22	RADIOSMDBGLOCK	0x1	R	**Radio Soft Modem Debug Lock**
	Locked when 1; unlocked when 0.			
21	RADIODBGLOCK	0x1	R	**Radio Debug Lock**
	Locked when 1; unlocked when 0.			
20	USERSPNIDLOCK	0x1	R	**User Secure Non-invasive Debug Lock**
	Locked when 1; unlocked when 0.			
19	USERSPIDLOCK	0x1	R	**User Secure Invasive Debug Lock**
	Locked when 1; unlocked when 0.			
18	USERNIDLOCK	0x1	R	**User Non-invasive Debug Lock**
	Locked when 1; unlocked when 0.			
17	USERDBGLOCK	0x1	R	**User Invasive Debug Lock**
	Locked when 1; unlocked when 0.			
16	USERDBGAPLOCK	0x1	R	**User Debug Access Port Lock**
	Locked when 1; unlocked when 0.			
15:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8	ROOTDBGLOCK	0x1	R	**Root Debug Lock**
	Locked when 1; unlocked when 0.			
7:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	MFRLOCK	0x1	R	**Manufacture Lock**
	Locked when 1; unlocked when 0.			
1	REGLOCK	0x1	R	**Register Lock**

Bit	Name	Reset	Access	Description
	Locked when 1; unlocked when 0.			
0	BUSLOCK	0x1	R	**Bus Lock**
	Locked when 1; unlocked when 0.			

6.6.6.19 SYSCFG_ROOTSESWVERSION - SE SW Version

Offset	Bit Position																															
0x60C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	SWVERSION																															

Bit	Name	Reset	Access	Description
31:0	SWVERSION	0x0	RW	**SW Version**
	Location for SE to write the Firmware version and host to read it			

6.6.7 MPAHBRAM Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	MPAHBRAM_IPVERSION	R	IP Version ID
0x004	MPAHBRAM_CMD	W	Command Register
0x008	MPAHBRAM_CTRL	RW	Control Register
0x00C	MPAHBRAM_ECCERRADDR0	RH	ECC Error Address 0
0x010	MPAHBRAM_ECCERRADDR1	RH	ECC Error Address 1
0x01C	MPAHBRAM_ECCMERRIND	RH	Multiple ECC Error Indication
0x020	MPAHBRAM_IF	RWH INTFLAG	Interrupt Flags
0x024	MPAHBRAM_IEN	RW	Interrupt Enable
0x028	MPAHBRAM_RAMBANKSVALID	RW	New Register
0x02C	MPAHBRAM_CFGSRTOP	RW	Sequential Region on Top
0x030	MPAHBRAM_CFGSRMAP	RW	Sequential Region Map
0x034	MPAHBRAM_CFGIU0MAP	RW	Interleaving Unit 0 Map
0x038	MPAHBRAM_CFGIU1MAP	RW	Interleaving Unit 1 Map
0x1000	MPAHBRAM_IPVERSION_SET	R	IP Version ID
0x1004	MPAHBRAM_CMD_SET	W	Command Register
0x1008	MPAHBRAM_CTRL_SET	RW	Control Register
0x100C	MPAHBRAM_ECCER-RADDR0_SET	RH	ECC Error Address 0
0x1010	MPAHBRAM_ECCER-RADDR1_SET	RH	ECC Error Address 1
0x101C	MPAHBRAM_ECCMER-RIND_SET	RH	Multiple ECC Error Indication
0x1020	MPAHBRAM_IF_SET	RWH INTFLAG	Interrupt Flags
0x1024	MPAHBRAM_IEN_SET	RW	Interrupt Enable
0x1028	MPAHBRAM_RAMBANKSVAL-ID_SET	RW	New Register
0x102C	MPAHBRAM_CFGSRTOP_SET	RW	Sequential Region on Top
0x1030	MPAHBRAM_CFGSRMAP_SET	RW	Sequential Region Map
0x1034	MPAHBRAM_CFGIU0MAP_SET	RW	Interleaving Unit 0 Map
0x1038	MPAHBRAM_CFGIU1MAP_SET	RW	Interleaving Unit 1 Map
0x2000	MPAHBRAM_IPVERSION_CLR	R	IP Version ID
0x2004	MPAHBRAM_CMD_CLR	W	Command Register
0x2008	MPAHBRAM_CTRL_CLR	RW	Control Register
0x200C	MPAHBRAM_ECCER-RADDR0_CLR	RH	ECC Error Address 0
0x2010	MPAHBRAM_ECCER-RADDR1_CLR	RH	ECC Error Address 1

Offset	Name	Type	Description
0x201C	MPAHBRAM_ECCMER-RIND_CLR	RH	Multiple ECC Error Indication
0x2020	MPAHBRAM_IF_CLR	RWH INTFLAG	Interrupt Flags
0x2024	MPAHBRAM_IEN_CLR	RW	Interrupt Enable
0x2028	MPAHBRAM_RAMBANKSVAL-ID_CLR	RW	New Register
0x202C	MPAHBRAM_CFGSRTOP_CLR	RW	Sequential Region on Top
0x2030	MPAHBRAM_CFGSRMAP_CLR	RW	Sequential Region Map
0x2034	MPAHBRAM_CFGIU0MAP_CLR	RW	Interleaving Unit 0 Map
0x2038	MPAHBRAM_CFGIU1MAP_CLR	RW	Interleaving Unit 1 Map
0x3000	MPAHBRAM_IPVERSION_TGL	R	IP Version ID
0x3004	MPAHBRAM_CMD_TGL	W	Command Register
0x3008	MPAHBRAM_CTRL_TGL	RW	Control Register
0x300C	MPAHBRAM_ECCER-RADDR0_TGL	RH	ECC Error Address 0
0x3010	MPAHBRAM_ECCER-RADDR1_TGL	RH	ECC Error Address 1
0x301C	MPAHBRAM_ECCMER-RIND_TGL	RH	Multiple ECC Error Indication
0x3020	MPAHBRAM_IF_TGL	RWH INTFLAG	Interrupt Flags
0x3024	MPAHBRAM_IEN_TGL	RW	Interrupt Enable
0x3028	MPAHBRAM_RAMBANKSVAL-ID_TGL	RW	New Register
0x302C	MPAHBRAM_CFGSRTOP_TGL	RW	Sequential Region on Top
0x3030	MPAHBRAM_CFGSRMAP_TGL	RW	Sequential Region Map
0x3034	MPAHBRAM_CFGIU0MAP_TGL	RW	Interleaving Unit 0 Map
0x3038	MPAHBRAM_CFGIU1MAP_TGL	RW	Interleaving Unit 1 Map

6.6.8 MPAHBRAM Register Description

6.6.8.1 MPAHBRAM_IPVERSION - IP Version ID

Offset	Bit Position																													
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x2	
Access																															R	
Name																															IPVERSION	

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	IPVERSION	0x2	R	**New BitField**

6.6.8.2 MPAHBRAM_CMD - Command Register

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															W(nB)	W(nB)
Name																															CLEARECCADDR1	CLEARECCADDR0

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	CLEARECCADDR1	0x0	W(nB)	**Clear ECCERRADDR1**
	Write 1 to clear ECCERRADDR1 and ECCMERRIND.P1.			
0	CLEARECCADDR0	0x0	W(nB)	**Clear ECCERRADDR0**
	Write 1 to clear ECCERRADDR0 and ECCMERRIND.P0.			

6.6.8.3 MPAHBRAM_CTRL - Control Register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																										0x1		0x0		0x0	0x0	0x0
Access																										RW		RW		RW	RW	RW
Name																										ADDRFAULTEN		AHBPORTPRIORITY		ECCERRFAULTEN	ECCWEN	ECCEN

Bit	Name	Reset	Access	Description
31:7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6	ADDRFAULTEN	0x1	RW	**Address fault bus fault enable**
	Enable bus fault upon address fault			
5:3	AHBPORTPRIORITY	0x0	RW	**AHB port arbitration priority**

Value	Mode	Description
0	NONE	No AHB port have raised priority.
1	PORT0	AHB port 0 has raised priority.
2	PORT1	AHB port 1 has raised priority.

2	ECCERRFAULTEN	0x0	RW	**ECC Error bus fault enable**
	Enable bus fault upon 2 bit ECC error			
1	ECCWEN	0x0	RW	**Enable ECC syndrome writes**
0	ECCEN	0x0	RW	**Enable ECC functionality**

6.6.8.4 MPAHBRAM_ECCERRADDR0 - ECC Error Address 0

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	ADDR																															

Bit	Name	Reset	Access	Description
31:0	ADDR	0x0	R	**ECC Error Address**
	Last captured ECC error address on AHB port 0. Cleared by CMD.CLEARECCADDR0			

6.6.8.5 MPAHBRAM_ECCERRADDR1 - ECC Error Address 1

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	ADDR																															

Bit	Name	Reset	Access	Description
31:0	ADDR	0x0	R	**ECC Error Address**
	Last captured ECC error address on AHB port 1. Cleared by CMD.CLEARECCADDR1			

6.6.8.6 MPAHBRAM_ECCMERRIND - Multiple ECC Error Indication

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	R
Name																															P1	P0

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	P1	0x0	R	**Multiple ECC errors on AHB port 1**
	Multiple ECC error indication on AHB port 1. Cleared by CMD.CLEARECCADDR1.			
0	P0	0x0	R	**Multiple ECC errors on AHB port 0**
	Multiple ECC error indication on AHB port 0. Cleared by CMD.CLEARECCADDR0.			

6.6.8.7 MPAHBRAM_IF - Interrupt Flags

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0	0x0			0x0	0x0
Access																											RW	RW			RW	RW
Name																											AHB1ERR2B	AHB0ERR2B			AHB1ERR1B	AHB0ERR1B

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	AHB1ERR2B	0x0	RW	**AHB1 2-bit ECC Error Interrupt Flag**
4	AHB0ERR2B	0x0	RW	**AHB0 2-bit ECC Error Interrupt Flag**
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	AHB1ERR1B	0x0	RW	**AHB1 1-bit ECC Error Interrupt Flag**
0	AHB0ERR1B	0x0	RW	**AHB0 1-bit ECC Error Interrupt Flag**

6.6.8.8 MPAHBRAM_IEN - Interrupt Enable

Offset	Bit Position																													
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0	0x0			0x0	0x0
Access																											RW	RW			RW	RW
Name																											AHB1ERR2B	AHB0ERR2B			AHB1ERR1B	AHB0ERR1B

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	AHB1ERR2B	0x0	RW	**AHB1 2-bit ECC Error Interrupt Enable**
4	AHB0ERR2B	0x0	RW	**AHB0 2-bit ECC Error Interrupt Enable**
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	AHB1ERR1B	0x0	RW	**AHB1 1-bit ECC Error Interrupt Enable**
0	AHB0ERR1B	0x0	RW	**AHB0 1-bit ECC Error Interrupt Enable**

6.6.8.9 MPAHBRAM_RAMBANKSVALID - New Register

Offset	Bit Position																													
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0xFFFFFFFF															
Access																	RW															
Name																	RAMBANKSVALID															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	RAMBANKSVALID	0xFFFFFFFF	RW	**Enable bits for RAM banks 0-31**

Value	Mode	Description
1	BLK0	Enable RAM block0
3	BLK0TO1	Enable RAM block0 to block1
7	BLK0TO2	Enable RAM block0 to block2
15	BLK0TO3	Enable RAM block0 to block3
31	BLK0TO4	Enable RAM block0 to block4
63	BLK0TO5	Enable RAM block0 to block5
127	BLK0TO6	Enable RAM block0 to block6
255	BLK0TO7	Enable RAM block0 to block7
511	BLK0TO8	Enable RAM block0 to block8
1023	BLK0TO9	Enable RAM block0 to block9
2047	BLK0TO10	Enable RAM block0 to block10
4095	BLK0TO11	Enable RAM block0 to block11
8191	BLK0TO12	Enable RAM block0 to block12
16383	BLK0TO13	Enable RAM block0 to block13
32767	BLK0TO14	Enable RAM block0 to block14
65535	BLK0TO15	Enable RAM block0 to block15

6.6.8.10 MPAHBRAM_CFGSRTOP - Sequential Region on Top

Offset	Bit Position																														
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																RW
Name																																SRTOP

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	SRTOP	0x0	RW	**Sequential region on top**
	Determines the relative ordering of the sequential region vs the interleaving region. If set, the sequential region is mapped to the upper part of the address space.			

6.6.8.11 MPAHBRAM_CFGSRMAP - Sequential Region Map

Offset	Bit Position																														
0x030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0xFFFFFFFF															
Access																	RW															
Name																	MAP															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	MAP	0xFFFFFFFF	RW	
	RAM bank mapping for the sequential region.			

6.6.8.12 MPAHBRAM_CFGIU0MAP - Interleaving Unit 0 Map

Offset	Bit Position																													
0x034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	RW															
Name																	MAP															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	MAP	0x0	RW	
	RAM bank mapping for interleaving unit 0.			

6.6.8.13 MPAHBRAM_CFGIU1MAP - Interleaving Unit 1 Map

Offset	Bit Position																													
0x038	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	RW															
Name																	MAP															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	MAP	0x0	RW	
	RAM bank mapping for interleaving unit 1.			

6.7 MSC Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	MSC_IPVERSION	R	IP Version ID
0x004	MSC_READCTRL	RW	Read Control Register
0x008	MSC_RDATACTRL	RW	Read Data Control Register
0x00C	MSC_WRITECTRL	RW	Write Control Register
0x010	MSC_WRITECMD	W	Write Command Register
0x014	MSC_ADDRB	RWH	Page Erase/Write Address Buffer
0x018	MSC_WDATA	RWH	Write Data Register
0x01C	MSC_STATUS	RH	Status Register
0x020	MSC_IF	RWH	Interrupt Flag Register
0x024	MSC_IEN	RW	Interrupt Enable Register
0x034	MSC_USERDATASIZE	R	User Data Region Size Register
0x038	MSC_CMD	W	Command Register
0x03C	MSC_LOCK	W	Configuration Lock Register
0x040	MSC_MISCLOCKWORD	RW	Mass Erase and User Data Page Lock Word
0x050	MSC_PWRCTRL	RW	Power Control Register
0x120	MSC_PAGELOCK0	RW	Main Space Page 0-31 Lock Word
0x124	MSC_PAGELOCK1	RW	Main Space Page 32-63 Lock Word
0x128	MSC_PAGELOCK2	RW	Main Space Page 64-95 Lock Word
0x12C	MSC_PAGELOCK3	RW	Main Space Page 96-127 Lock Word
0x130	MSC_PAGELOCK4	RW	Main Space Page 128-159 Lock Word
0x134	MSC_PAGELOCK5	RW	Main Space Page 160-191 Lock Word
0x138	MSC_PAGELOCK6	RW	Main Space Page 192-223 Lock Word
0x13C	MSC_PAGELOCK7	RW	Main Space Page 224-256 Lock Word
0x1000	MSC_IPVERSION_SET	R	IP Version ID
0x1004	MSC_READCTRL_SET	RW	Read Control Register
0x1008	MSC_RDATACTRL_SET	RW	Read Data Control Register
0x100C	MSC_WRITECTRL_SET	RW	Write Control Register
0x1010	MSC_WRITECMD_SET	W	Write Command Register
0x1014	MSC_ADDRB_SET	RWH	Page Erase/Write Address Buffer
0x1018	MSC_WDATA_SET	RWH	Write Data Register
0x101C	MSC_STATUS_SET	RH	Status Register
0x1020	MSC_IF_SET	RWH	Interrupt Flag Register
0x1024	MSC_IEN_SET	RW	Interrupt Enable Register
0x1034	MSC_USERDATASIZE_SET	R	User Data Region Size Register
0x1038	MSC_CMD_SET	W	Command Register

Offset	Name	Type	Description
0x103C	MSC_LOCK_SET	W	Configuration Lock Register
0x1040	MSC_MISCLOCKWORD_SET	RW	Mass Erase and User Data Page Lock Word
0x1050	MSC_PWRCTRL_SET	RW	Power Control Register
0x1120	MSC_PAGELOCK0_SET	RW	Main Space Page 0-31 Lock Word
0x1124	MSC_PAGELOCK1_SET	RW	Main Space Page 32-63 Lock Word
0x1128	MSC_PAGELOCK2_SET	RW	Main Space Page 64-95 Lock Word
0x112C	MSC_PAGELOCK3_SET	RW	Main Space Page 96-127 Lock Word
0x1130	MSC_PAGELOCK4_SET	RW	Main Space Page 128-159 Lock Word
0x1134	MSC_PAGELOCK5_SET	RW	Main Space Page 160-191 Lock Word
0x1138	MSC_PAGELOCK6_SET	RW	Main Space Page 192-223 Lock Word
0x113C	MSC_PAGELOCK7_SET	RW	Main Space Page 224-256 Lock Word
0x2000	MSC_IPVERSION_CLR	R	IP Version ID
0x2004	MSC_READCTRL_CLR	RW	Read Control Register
0x2008	MSC_RDATACTRL_CLR	RW	Read Data Control Register
0x200C	MSC_WRITECTRL_CLR	RW	Write Control Register
0x2010	MSC_WRITECMD_CLR	W	Write Command Register
0x2014	MSC_ADDRB_CLR	RWH	Page Erase/Write Address Buffer
0x2018	MSC_WDATA_CLR	RWH	Write Data Register
0x201C	MSC_STATUS_CLR	RH	Status Register
0x2020	MSC_IF_CLR	RWH	Interrupt Flag Register
0x2024	MSC_IEN_CLR	RW	Interrupt Enable Register
0x2034	MSC_USERDATASIZE_CLR	R	User Data Region Size Register
0x2038	MSC_CMD_CLR	W	Command Register
0x203C	MSC_LOCK_CLR	W	Configuration Lock Register
0x2040	MSC_MISCLOCKWORD_CLR	RW	Mass Erase and User Data Page Lock Word
0x2050	MSC_PWRCTRL_CLR	RW	Power Control Register
0x2120	MSC_PAGELOCK0_CLR	RW	Main Space Page 0-31 Lock Word
0x2124	MSC_PAGELOCK1_CLR	RW	Main Space Page 32-63 Lock Word
0x2128	MSC_PAGELOCK2_CLR	RW	Main Space Page 64-95 Lock Word
0x212C	MSC_PAGELOCK3_CLR	RW	Main Space Page 96-127 Lock Word
0x2130	MSC_PAGELOCK4_CLR	RW	Main Space Page 128-159 Lock Word
0x2134	MSC_PAGELOCK5_CLR	RW	Main Space Page 160-191 Lock Word
0x2138	MSC_PAGELOCK6_CLR	RW	Main Space Page 192-223 Lock Word
0x213C	MSC_PAGELOCK7_CLR	RW	Main Space Page 224-256 Lock Word
0x3000	MSC_IPVERSION_TGL	R	IP Version ID
0x3004	MSC_READCTRL_TGL	RW	Read Control Register
0x3008	MSC_RDATACTRL_TGL	RW	Read Data Control Register

Offset	Name	Type	Description
0x300C	MSC_WRITECTRL_TGL	RW	Write Control Register
0x3010	MSC_WRITECMD_TGL	W	Write Command Register
0x3014	MSC_ADDRB_TGL	RWH	Page Erase/Write Address Buffer
0x3018	MSC_WDATA_TGL	RWH	Write Data Register
0x301C	MSC_STATUS_TGL	RH	Status Register
0x3020	MSC_IF_TGL	RWH	Interrupt Flag Register
0x3024	MSC_IEN_TGL	RW	Interrupt Enable Register
0x3034	MSC_USERDATASIZE_TGL	R	User Data Region Size Register
0x3038	MSC_CMD_TGL	W	Command Register
0x303C	MSC_LOCK_TGL	W	Configuration Lock Register
0x3040	MSC_MISCLOCKWORD_TGL	RW	Mass Erase and User Data Page Lock Word
0x3050	MSC_PWRCTRL_TGL	RW	Power Control Register
0x3120	MSC_PAGELOCK0_TGL	RW	Main Space Page 0-31 Lock Word
0x3124	MSC_PAGELOCK1_TGL	RW	Main Space Page 32-63 Lock Word
0x3128	MSC_PAGELOCK2_TGL	RW	Main Space Page 64-95 Lock Word
0x312C	MSC_PAGELOCK3_TGL	RW	Main Space Page 96-127 Lock Word
0x3130	MSC_PAGELOCK4_TGL	RW	Main Space Page 128-159 Lock Word
0x3134	MSC_PAGELOCK5_TGL	RW	Main Space Page 160-191 Lock Word
0x3138	MSC_PAGELOCK6_TGL	RW	Main Space Page 192-223 Lock Word
0x313C	MSC_PAGELOCK7_TGL	RW	Main Space Page 224-256 Lock Word

6.8 MSC Register Description

6.8.1 MSC_IPVERSION - IP Version ID

Offset	Bit Position																													
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x4																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x4	R	**IP Version ID**
	IP Version ID			

6.8.2 MSC_READCTRL - Read Control Register

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset											0x2																				
Access											RW																				
Name											MODE																				

Bit	Name	Reset	Access	Description
31:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21:20	MODE	0x2	RW	**Read Mode**

When changing to a higher frequency, this register must be set to a large number of wait states before the core clock is switched to the higher frequency. When changing to a lower frequency, this register should be set to a lower number of wait states after the frequency transition has been completed. The maximum frequency for each wait state setting is listed in the datasheet.

Value	Mode	Description
0	WS0	Zero wait-states inserted in fetch or read transfers
1	WS1	One wait-state inserted for each fetch or read transfer. See Flash Wait-States table for details
2	WS2	Two wait-states inserted for eatch fetch or read transfer. See Flash Wait-States table for details
3	WS3	Three wait-states inserted for eatch fetch or read transfer. See Flash Wait-States table for details

19:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

6.8.3 MSC_RDATACTRL - Read Data Control Register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																				0x1											0x0	
Access																				RW											RW	
Name																				DOUTBUFEN											AFDIS	

Bit	Name	Reset	Access	Description
31:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12	DOUTBUFEN	0x1	RW	**Flash dout pipeline buffer enable**
	Flag to enable or bypass flash data output buffer			
11:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	AFDIS	0x0	RW	**Automatic Invalidate Disable**
	When this bit is set the cache is not automatically invalidated when a write or page erase is performed.			
0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

6.8.4 MSC_WRITECTRL - Write Control Register

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset												0x0																	0x0		0x0	0x0
Access												RW																	RW		RW	RW
Name												RANGECOUNT																	LPWRITE		IRQERASEABORT	WREN

Bit	Name	Reset	Access	Description
31:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25:16	RANGECOUNT	0x0	RW	**EraseRange Count**
	Apply only with EraseRange command. Define number of pages to be erased.			
15:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	LPWRITE	0x0	RW	**Low-Power Write**
	When set, write times might double while reducing current consumption			
2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	IRQERASEABORT	0x0	RW	**Abort Page Erase on Interrupt**
	When this bit is set to 1, any Cortex-M4 interrupt aborts any current page erase operation. Executing that interrupt vector from Flash will halt the CPU.			
0	WREN	0x0	RW	**Enable Write/Erase Controller**
	When this bit is set, the MSC write and erase functionality is enabled			

6.8.5 MSC_WRITECMD - Write Command Register

Offset	Bit Position																														
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																				0x0				0x0			0x0	0x0		0x0	0x0	
Access																				W				W			W	W		W	W	
Name																				CLEARWDATA				ERASEMAIN0			ERASEABORT	ERASERANGE		WRITEEND	ERASEPAGE	

Bit	Name	Reset	Access	Description
31:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12	CLEARWDATA	0x0	W	**Clear WDATA state**
	Will set WDATAREADY and DMA request. Should only be used when no write is active.			
11:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8	ERASEMAIN0	0x0	W	**Mass erase region 0**
	Initiate mass erase of flash memory. If MELOCKBIT in MSC_MISCLOCKWORD is set, user firmware cannot initiate mass erase, and only the SE may initiate mass erase.			
7:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	ERASEABORT	0x0	W	**Abort erase sequence**
	Writing to this bit will abort an ongoing erase sequence.			
4	ERASERANGE	0x0	W	**Erase range of pages**
	Erase a range of user defined pages started from the MSC_ADDRB register. The WREN bit in the MSC_WRITECTRL register must be set in order to use this command.			
3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	WRITEEND	0x0	W	**End Write Mode**
	Write 1 to abort a write command.			
1	ERASEPAGE	0x0	W	**Erase Page**
	Erase any user defined page selected by the MSC_ADDRB register. The WREN bit in the MSC_WRITECTRL register must be set in order to use this command.			
0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

6.8.6 MSC_ADDRB - Page Erase/Write Address Buffer

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	ADDRB																															

Bit	Name	Reset	Access	Description
31:0	ADDRB	0x0	RW	**Page Erase or Write Address Buffer**
	This register holds the system address for the erase or write operation. Address should be word aligned address.The MSB bit is not ignored for ADDRB			

6.8.7 MSC_WDATA - Write Data Register

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	DATAW																															

Bit	Name	Reset	Access	Description
31:0	DATAW	0x0	RW	**Write Data**
	The data to be written to the address in MSC_ADDRB. This register must be written when the WDATAREADY bit of MSC_STATUS is set.This register does not support write mask.			

6.8.8 MSC_STATUS - Status Register

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0				0x1			0x0								0x0									0x0	0x0	0x0	0x0	0x1	0x0	0x0	0x0
Access	R				R			R								R									R	R	R	R	R	R	R	R
Name	PWRUPCKBDFAILCOUNT				WREADY			PWRON								REGLOCK									RANGEPARTIAL	TIMEOUT	PENDING	ERASEABORTED	WDATAREADY	INVADDR	LOCKED	BUSY

Bit	Name	Reset	Access	Description
31:28	PWRUPCKBDFAIL-COUNT	0x0	R	**Flash power up checkerboard pattern chec**
	This field tells how many times checkboard pattern check fail occured after a reset sequence.			
27	WREADY	0x1	R	**Flash Write Ready**
	When this bit is set, flash has completed the power up sequence and is ready for write/erase commands.			
26:25	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
24	PWRON	0x0	R	**Flash power on status**
	When this bit is set, flash is powered on. If zero, flash is powered off and reads from flash return indeterminate data.			
23:17	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
16	REGLOCK	0x0	R	**Register Lock Status**
	Indicates the current status of register lock			

Value	Mode	Description
0	UNLOCKED	
1	LOCKED	

15:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7	RANGEPARTIAL	0x0	R	**EraseRange with skipped locked pages**
6	TIMEOUT	0x0	R	**Write command timeout flag**
	When this bit is set, flash has completed the power up sequence and is ready for write/erase commands.			
5	PENDING	0x0	R	**Write command is in queue**
	When this bit is set, flash is powered on. If zero, flash is powered off and reads from flash return indeterminate data.			
4	ERASEABORTED	0x0	R	**The Current Flash Erase Operation Aborte**
	Indicates the current status of register lock			

Bit	Name	Reset	Access	Description
3	WDATAREADY	0x1	R	**WDATA Write Ready**
	When this bit is set, the content of MSC_WDATA is read by MSC Flash Write Controller and the register may be updated with the next 32-bit word to be written to flash. This bit is cleared when writing to MSC_WDATA.			
2	INVADDR	0x0	R	**Invalid Write Address or Erase Page**
	When this bit is set, software has attempted to load an invalid (unmapped) address into the MSC_ADDRB register.			
1	LOCKED	0x0	R	**Access Locked**
	When set, the last erase or write was aborted due to erase/write access constraints.			
0	BUSY	0x0	R	**Erase/Write Busy**
	When set, an erase or write operation is in progress and new commands are ignored.			

6.8.9 MSC_IF - Interrupt Flag Register

Offset	Bit Position																												
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0	0x0						0x0	0x0	0x0
Access																							RW	RW						RW	RW	RW
Name																							PWROFF	PWRUPF						WDATAOV	WRITE	ERASE

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	PWROFF	0x0	RW	**Flash Power Off Sequence Complete Flag**
	Set after MSC_CMD.PWROFF received, flash powered off complete			
8	PWRUPF	0x0	RW	**Flash Power Up Sequence Complete Flag**
	Set after MSC_CMD.PWRUP received, flash powered up complete and ready for read/write			
7:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	WDATAOV	0x0	RW	**Host write buffer overflow**
	If set, flash controller write buffer overflow detected			
1	WRITE	0x0	RW	**Host Write Done Interrupt Read Flag**
	Set when a write is done			
0	ERASE	0x0	RW	**Host Erase Done Interrupt Read Flag**
	Set when erase is done			

6.8.10 MSC_IEN - Interrupt Enable Register

Offset	Bit Position																														
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0	0x0						0x0	0x0	0x0
Access																							RW	RW						RW	RW	RW
Name																							PWROFF	PWRUPF						WDATAOV	WRITE	ERASE

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	PWROFF interrupt enable	0x0	RW	**Flash Power Off Seq done irq enable**
8	PWRUPF interrupt enable	0x0	RW	**Flash Power Up Seq done irq enable**
7:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	WDATAOV interrupt enable	0x0	RW	**write data buffer overflow irq enable**
1	WRITE interrupt enable	0x0	RW	**Write Done Interrupt enable**
0	ERASE interrupt enable	0x0	RW	**Erase Done Interrupt enable**

6.8.11 MSC_USERDATASIZE - User Data Region Size Register

Offset	Bit Position																													
0x034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x4				
Access																											R				
Name																											USERDATASIZE				

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:0	USERDATASIZE	0x4	R	**User Data Size**
	This field determines user data region size. SIZE = 256B * USERDATASIZE.			

6.8.12 MSC_CMD - Command Register

Offset	Bit Position																													
0x038	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0				0x0
Access																												W				W
Name																												PWROFF				PWRUP

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	PWROFF	0x0	W	**Flash power off/sleep command**
	Write to this bit to power down the Flash. User code should execute from RAM afterwards. Read from flash after flash being powered down will cause undetermined behavior. To power up, either set CMD.PWRUP bit or try read from flash.			
3:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	PWRUP	0x0	W	**Flash Power Up Command**
	Write to this bit to power up the Flash. IRQ PWRUPF will be fired when power up sequence completed.			

6.8.13 MSC_LOCK - Configuration Lock Register

Offset	Bit Position																															
0x03C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																								0x0								
Access																								W								
Name																								LOCKKEY								

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LOCKKEY	0x0	W	**Configuration Lock**

Write any other value than the unlock code to lock access to MSC_RDATACTRL, MSC_READCTRL, and MSC_WRITECTRL. Write the unlock code to enable access. When reading the register, bit 0 is set when the lock is enabled.

Value	Mode	Description
0	LOCK	
7025	UNLOCK	

6.8.14 MSC_MISCLOCKWORD - Mass Erase and User Data Page Lock Word

Offset	Bit Position																															
0x040	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x1				0x1
Access																												RW				RW
Name																												UDLOCKBIT				MELOCKBIT

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	UDLOCKBIT	0x1	RW	**User Data Lock**

Zero means host can write/erase to the user data area. Host is only allowed to write one. Root and debug can clear this bit.

3:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	MELOCKBIT	0x1	RW	**Mass Erase Lock**

Zero means host can mass erase the main space. Host is only allowed to write one. Root and debug can clear this bit.

6.8.15 MSC_PWRCTRL - Power Control Register

Offset	Bit Position																													
0x050	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset												0x10																0x0			0x1	0x0
Access												RW																RW			RW	RW
Name												PWROFFDLY																PWROFFENTRYAGAIN			PWROFFONEM1PENTRY	PWROFFONEM1ENTRY

Bit	Name	Reset	Access	Description
31:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:16	PWROFFDLY	0x10	RW	**Power down delay**
	Defines delay cycles before flash enters sleep mode. Works together with PWROFFENTRYAGAIN bit. The power off delay is 64 * PWROFFDLY bus clock cycles.			
15:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	PWROFFENTRYAGAIN	0x0	RW	**POWER down flash again in EM1/EM1p**
	If enabled, flash will enter sleep mode again when POWEROFFONEM1ENTRY/POWEROFFONEM1PENTRY is set and no flash activities occur for the time determined by PWROFFDLY.			
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	PWROFFONEM1PENTRY	0x1	RW	**Power down Flash macro when enter EM1P**
	If enabled, flash will be in sleep mode when entering EM1P (radio-only sleep).			
0	PWROFFONEM1ENTRY	0x0	RW	**Power down Flash macro when enter EM1**
	If enabled, flash will be in sleep mode when entering EM1.			

6.8.16 MSC_PAGELOCK0 - Main Space Page 0-31 Lock Word

Offset	Bit Position																													
0x120	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	LOCKBIT																															

Bit	Name	Reset	Access	Description
31:0	LOCKBIT	0x0	RW	**page lock bit**
	Zero means the corresponding page is allowed to write/erase. change to one will prevent corresponding page from write/erase. bit[0] for main space page 0, and bit[1] for page 1... bit[31] for page 31. Reset to zero. Host is only allowed to write one. Root and Debug are allowed to clear this register			

6.8.17 MSC_PAGELOCK1 - Main Space Page 32-63 Lock Word

Offset	Bit Position																													
0x124	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	LOCKBIT																															

Bit	Name	Reset	Access	Description
31:0	LOCKBIT	0x0	RW	**page lock bit**
	Zero means the corresponding page is allowed to write/erase. change to one will prevent corresponding page from write/erase. bit[0] for main space page 32, and bit[1] for page 33... bit[31] for page 63. Reset to zero. Host is only allowed to write one. Root and Debug are allowed to clear this register			

6.8.18 MSC_PAGELOCK2 - Main Space Page 64-95 Lock Word

Offset	Bit Position																															
0x128	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	LOCKBIT																															

Bit	Name	Reset	Access	Description
31:0	LOCKBIT	0x0	RW	**page lock bit**
	Zero means the corresponding page is allowed to write/erase. change to one will prevent corresponding page from write/erase. bit[0] for main space page 64, and bit[1] for page 65... bit[31] for page 95. Reset to zero. Host is only allowed to write one. Root and Debug are allowed to clear this register			

6.8.19 MSC_PAGELOCK3 - Main Space Page 96-127 Lock Word

Offset	Bit Position																															
0x12C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	LOCKBIT																															

Bit	Name	Reset	Access	Description
31:0	LOCKBIT	0x0	RW	**page lock bit**
	Zero means the corresponding page is allowed to write/erase. change to one will prevent corresponding page from write/erase. bit[0] for main space page 96, and bit[1] for page 97... bit[31] for page 127. Reset to zero. Host is only allowed to write one. Root and Debug are allowed to clear this register			

6.8.20 MSC_PAGELOCK4 - Main Space Page 128-159 Lock Word

Offset	Bit Position																													
0x130	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	LOCKBIT																															

Bit	Name	Reset	Access	Description
31:0	LOCKBIT	0x0	RW	**page lock bit**
	Zero means the corresponding page is allowed to write/erase. change to one will prevent corresponding page from write/erase. bit[0] for main space page 128, and bit[1] for page 129... bit[31] for page 159. Reset to zero. Host is only allowed to write one. Root and Debug are allowed to clear this register			

6.8.21 MSC_PAGELOCK5 - Main Space Page 160-191 Lock Word

Offset	Bit Position																													
0x134	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	LOCKBIT																															

Bit	Name	Reset	Access	Description
31:0	LOCKBIT	0x0	RW	**page lock bit**
	Zero means the corresponding page is allowed to write/erase. change to one will prevent corresponding page from write/erase. bit[0] for main space page 160, and bit[1] for page 161... bit[31] for page 191. Reset to zero. Host is only allowed to write one. Root and Debug are allowed to clear this register			

6.8.22 MSC_PAGELOCK6 - Main Space Page 192-223 Lock Word

Offset	Bit Position																															
0x138	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	LOCKBIT																															

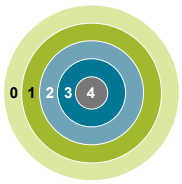
Bit	Name	Reset	Access	Description
31:0	LOCKBIT	0x0	RW	**page lock bit**
	Zero means the corresponding page is allowed to write/erase. change to one will prevent corresponding page from write/erase. bit[0] for main space page 192, and bit[1] for page 193... bit[31] for page 223. Reset to zero. Host is only allowed to write one. Root and Debug are allowed to clear this register			

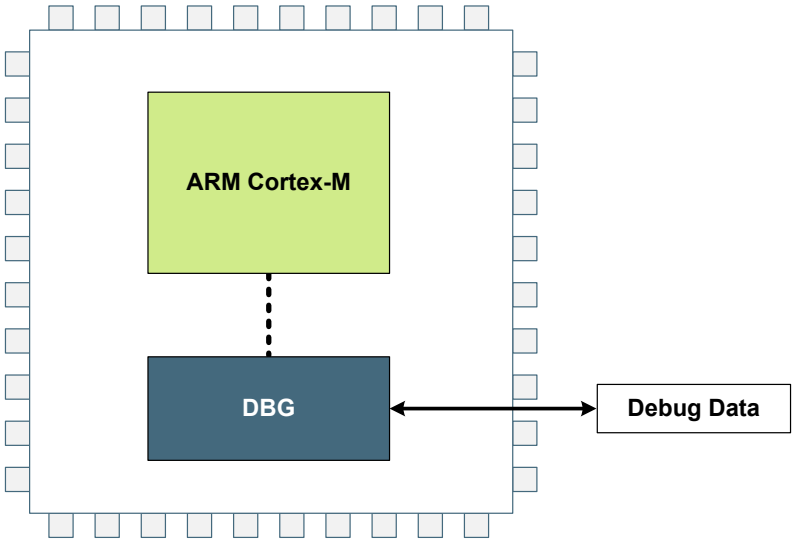
6.8.23 MSC_PAGELOCK7 - Main Space Page 224-256 Lock Word

Offset	Bit Position																															
0x13C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	LOCKBIT																															

Bit	Name	Reset	Access	Description
31:0	LOCKBIT	0x0	RW	**page lock bit**
	Zero means the corresponding page is allowed to write/erase. change to one will prevent corresponding page from write/erase. bit[0] for main space page 224, and bit[1] for page 225... bit[31] for page 255. Reset to zero. Host is only allowed to write one. Root and Debug are allowed to clear this register			

7. DBG - Debug Interface





Quick Facts

What?

The Debug Interface is used to program and debug EFR32xG25 devices.

Why?

The Debug Interface makes it easy to re-program and update the system in the field, and allows debugging with minimal I/O pin usage.

How?

The Cortex-M33 supports advanced debugging features. EFR32xG25 devices can use a minimum of two port pins for debugging or programming. The internal and external state of the system can be examined with debug extensions supporting instruction or data access break and watch points.

7.1 Introduction

The EFR32xG25 devices include hardware debug support through a 2-pin serial-wire debug (SWD) interface or a 4-pin Joint Test Action Group (JTAG) interface, as well as an Embedded Trace Module (ETM) for data/instruction tracing. In addition, there is also a Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

For more technical information about the debug interface the reader is referred to:

- ARM Cortex-M33 Technical Reference Manual
- ARM CoreSight Components Technical Reference Manual
- ARM Debug Interface v5 Architecture Specification
- IEEE Standard for Test Access Port and Boundary-Scan Architecture, IEEE 1149.1-2013

7.2 Features

- Debug Access Port Serial Wire JTAG (DAPSWJ)
  - Implements the ADIv5 debug interface
- ARM Trustzone
  - Enables secure debugging
- Breakpoint unit (BPU)
  - Implement up to 8 hardware breakpoints
- Data Watch point and Trace (DWT) unit
  - Implement up to 4 watch points, trigger resources and system profiling
- Instrumentation Trace Macrocell (ITM)
  - Application-driven trace source that supports printf style debugging
- Embedded Trace Macrocell v3.5 (ETM)
  - Real time instruction and data trace information of the processor
- Cross Trigger Interface (CTI)
  - Issues synchronous triggers based on system events
  - Can be used to generate IRQs or route to PRS signalling

7.3 Functional Description

There are debug and trace pins available on the device. Operation of these pins is described in the following sections.

7.3.1 Debug Pins

The following pins are the debug connections for the device:

- Serial Wire Clock Input and Test Clock Input (SWCLKTCK) (SWCLK) : This pin is enabled after power-up and has a built-in pull-down.
- Serial Wire Data Input/Output and Test Mode Select Input (SWDIOTMS) (SWDIO) : This pin is enabled after power-up and has a built-in pull-up.
- Test Data Output (TDO): This pin is assigned to JTAG functionality after power-up. However, it remains in high-Z state until the first valid JTAG command is received.
- Test Data Input (TDI): This pin is assigned to JTAG functionality after power-up. However, it remains in high-Z state until the first valid JTAG command is received. Once enabled, the pin has a built-in pull-up.
- Serial Wire Viewer (SWV): This pin is disabled after reset.

The debug pins have integrated pull devices that are enabled by default after a reset. Leaving them enabled may increase current consumption if the pins are connected to power or ground. The debug pins have enable bits in the GPIO_DBGROUTEPEN register; refer to the GPIO chapter for more details. Upon disabling the debug pins, debug contact with the device is lost once the DAPSWJ power request bits are deasserted. By default after a power cycle, the DAPSWJ is in JTAG mode. If during a debugging session the device is switched to SWD mode, a power cycle is needed to return to JTAG mode.

7.3.2 Embedded Trace Macrocell V3.5 (ETM)

ETM makes it possible to non-intrusively trace both instruction and data from the processor in real time. Trace can be controlled through a set of triggering and filtering resources. The resources include 4 address comparators, 2 data value comparators, 2 counters, a context ID comparator and a sequencer. Before enabling the ETM, the CMU_TRACECLKCTRL register must be configured to select the desired trace clock source. (See the CMU chapter for details.)

The trace can be exported through a set of trace pins, which include:

- Trace Clock (TRACECLK): Functions as a sample clock for the trace. This pin is disabled after reset.
- Trace Data 0-3 (TRACEDATA0, TRACEDATA1, TRACEDATA2, TRACEDATA3): The trace data pins provide the compressed trace stream. These pins are disabled after reset.

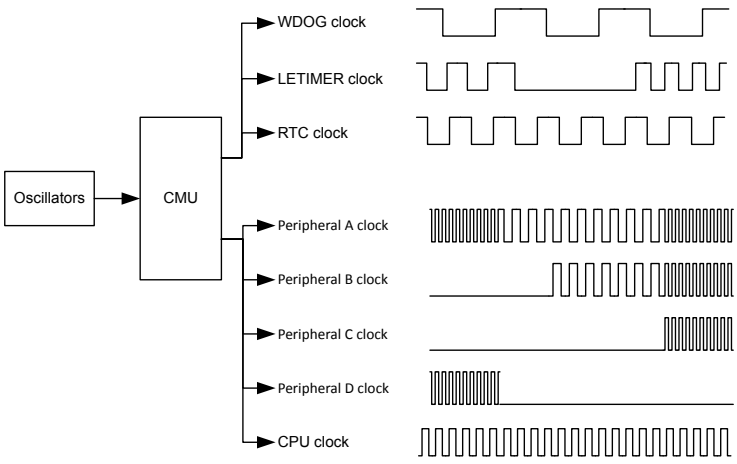
For information on how to configure the ETM, see the ARM Embedded Trace Macrocell Architecture Specification. The Trace Clock and Trace Data pins are enabled through a GPIO register. For more information on how to enable the ETM pins, refer to the GPIO chapter.

7.3.3 Debug and EM2/EM3

Debug connectivity in EM2 and EM3 is unavailable by default, to reduce current consumption. Debugging through EM2 and EM3 can be enabled by setting the EM2DBGEN bit in the EMU_CTRL register. Setting EM2DBGEN ensures that power domain associated with the debug circuitry will remain active, but will result in a small amount of additional current in EM2 and EM3.

Leaving the debugger connected when issuing a WFI or WFE to enter EM2 or EM3 will make the system enter a special EM2 mode. This mode differs from regular EM2 and EM3 in that the high frequency clocks are still enabled, and certain core functionality is still powered in order to maintain debug functionality. Because of this, the current consumption in this mode is closer to EM1, and it is, therefore, important to deassert the power requests in the DAPSWJ and disconnect the debugger before undertaking current consumption measurements.

8. CMU - Clock Management Unit



Quick Facts

What?

The CMU controls clock switching and distribution. EFR32xG25 supports several different oscillators with minimized power consumption and short start-up time. The CMU has HW support for calibration of RC oscillators.

Why?

Oscillators and clocks contribute significantly to the power consumption of the MCU. With the low power oscillators combined with the flexible clock control scheme, it is possible to minimize the energy consumption in any given application.

How?

The CMU switches different clock sources for various peripherals and sets the prescaler for the bus clocks. The short oscillator start-up times makes duty-cycling between active mode and the different low energy modes (EM2 DeepSleep, EM3 Stop, and EM4) very efficient. The calibration feature ensures high accuracy RC oscillators. Interrupts are available to avoid CPU polling of flags.

8.1 Introduction

The Clock Management Unit (CMU) is responsible for switching among various oscillator sources and provides clocks to the peripheral modules. Oscillators are automatically turned on and off based on demand from the peripherals to minimize power consumption.

8.2 Features

- Multiple clock sources available:
  - 160 MHz Radio Frequency Friendly Phase Locked Loop (RFFPLLRADIO)
  - Up to 100 MHz for RFFPLLSYS (Nominally 97.5 MHz)
  - 38 MHz - 40 MHz High Frequency Crystal Oscillator (HFXO)
  - 1 MHz - 80 MHz High Frequency RC Oscillator (HFRCODPLL / HFRCO0)
  - 1 MHz - 40 MHz Deep Sleep High Frequency RC Oscillator (HFRCOEM23)
  - 20 MHz Fast Startup RC Oscillator (FSRCO)
  - 1 MHz - 38 MHz External Clock from Input Pins (CLKIN0)
  - 32768 Hz Low Frequency Crystal Oscillator (LFXO)
  - 32768 Hz Low Frequency RC Oscillator (LFRCO)
  - 1000 Hz Ultra Low Frequency RC Oscillator (ULFRCO)
  - 48 MHz USB Phase Locked Loop (USBPLL0)
- On-demand oscillator request.
- Low power oscillators.
- Fast start-up times.
- Cascaded prescalers for AHB Clocks (HCLK), APB Clocks (PCLK).
- Independent clock control for Radio Sub-system.
- Independent clock control for USB Sub-system.
- Clock gating on an individual basis to all peripherals based on module enable.
- Selectable clocks can be output on external pins and/or PRS.
- Hardware support for calibration of RC oscillators.

8.3 Functional Description

The CMU is comprised of several programmable clock trees, which connect oscillator resources to peripherals and buses. This section describes clock sources and peripherals available to the largest devices in the EFR32xG25 family. Please refer to the Configuration Summary in the Device Datasheet to see which core and peripheral modules, and therefore clock connections, are present in a specific device. Bus clock selection, including peripherals clocked directly from bus clocks, is shown in Figure 8.1 Bus Clocks on page 160. Clock selection for peripherals with multiple high-frequency clock sources is shown in Figure 8.2 High Frequency Peripheral Clocks on page 161. Clock selection for peripherals with multiple low-frequency clock sources is shown in Figure 8.3 Low Frequency Peripheral Clocks on page 162. Clock selection for peripherals that can select from a high or low frequency clock source is shown in Figure 8.4 Mixed Frequency Peripheral Clocks on page 163. Additionally, two sub-systems have self-contained CMU. The radio sub-system clock portion is shown in Figure 8.5 Radio Sub-system Clocks on page 164. The USB sub-system clock portion is shown in Figure 8.6 USB Sub-system Clocks on page 164.

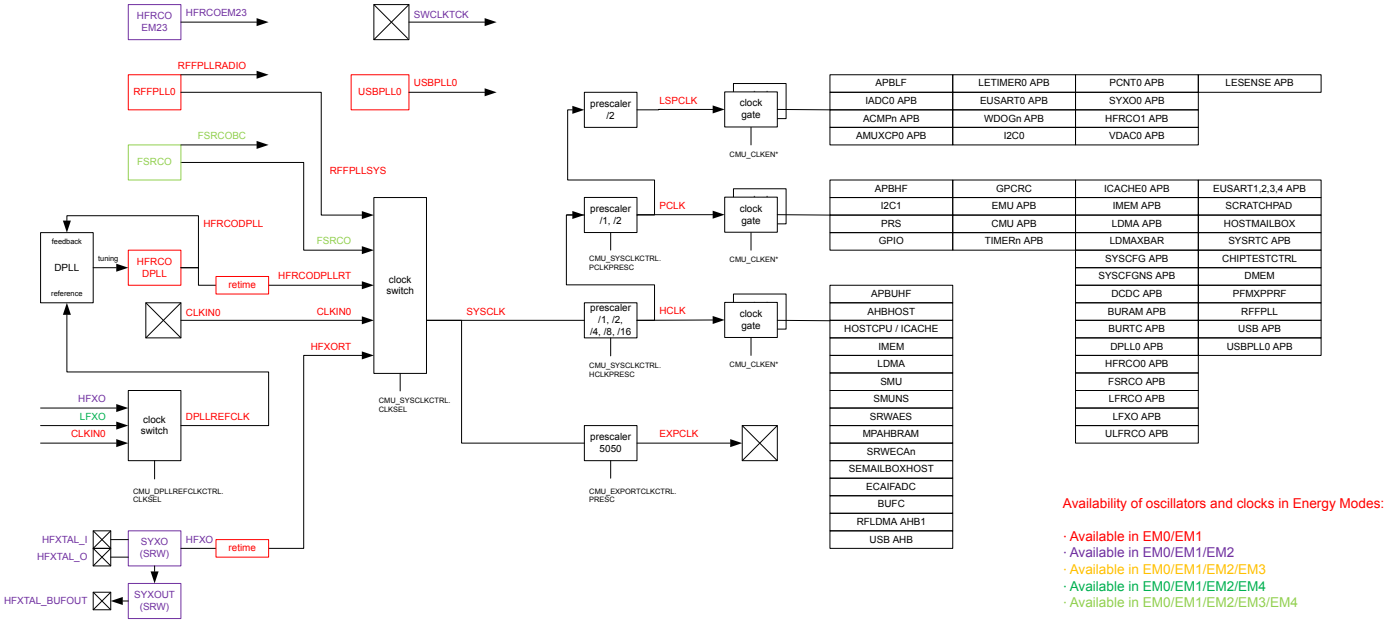


Figure 8.1. Bus Clocks

Availability of oscillators and clocks in Energy Modes:

- Available in EM0/EM1
- Available in EM0/EM1/EM2
- Available in EM0/EM1/EM2/EM3
- Available in EM0/EM1/EM2/EM4
- Available in EM0/EM1/EM2/EM3/EM4

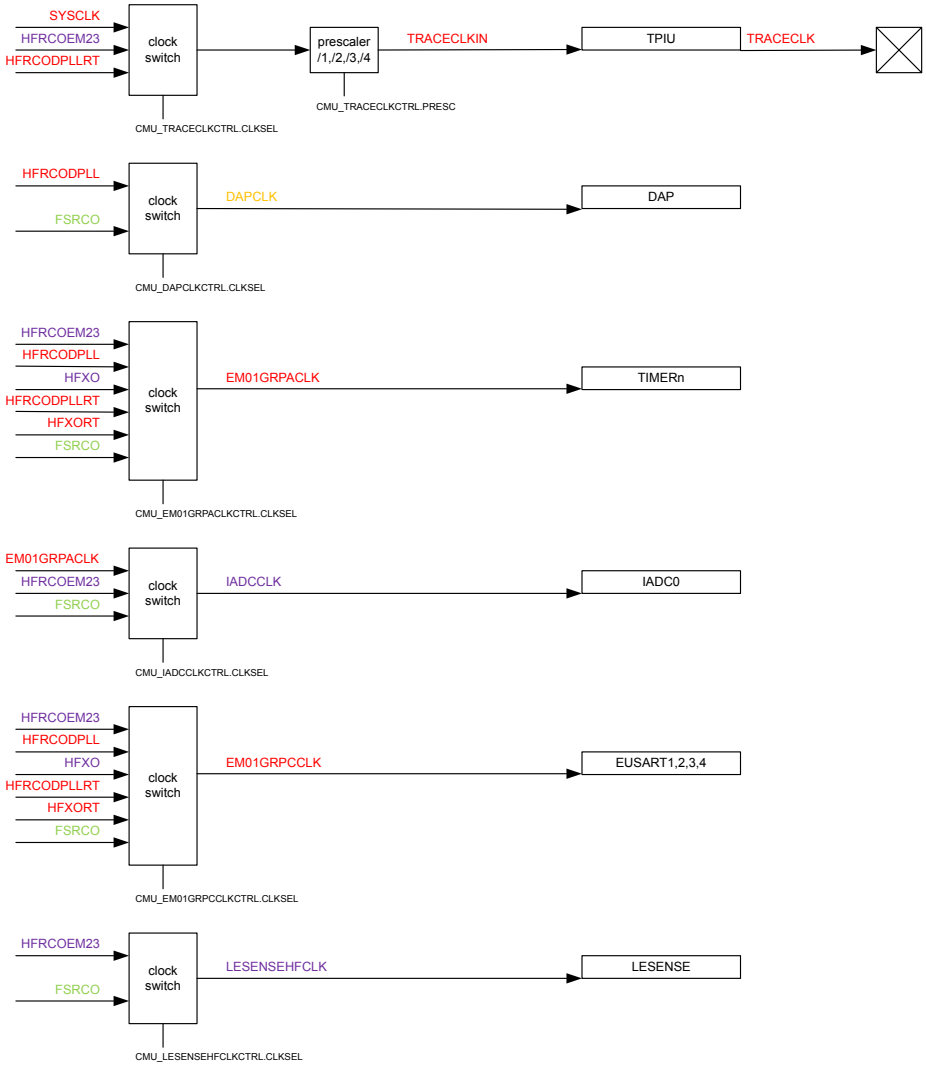


Figure 8.2. High Frequency Peripheral Clocks

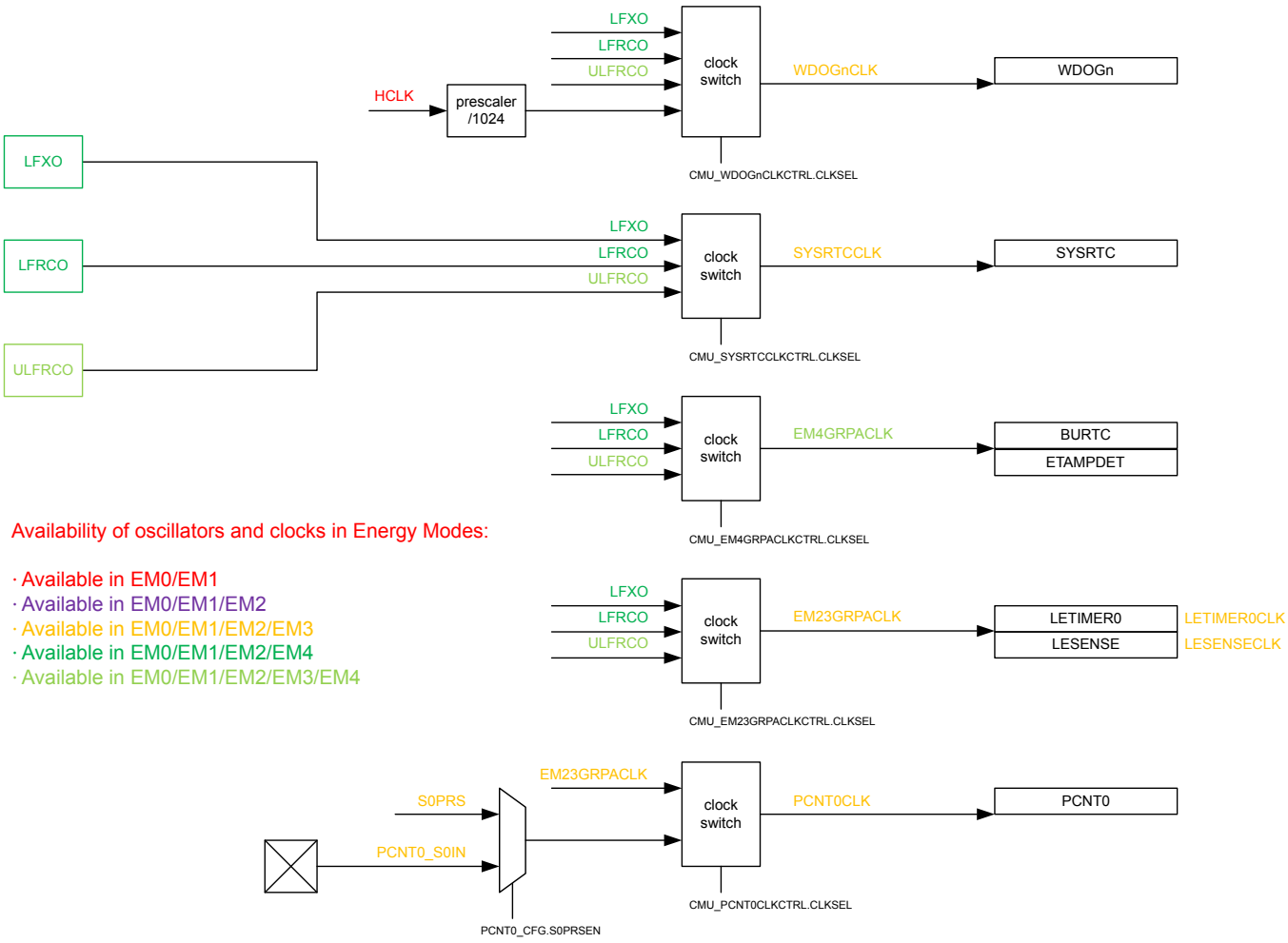


Figure 8.3. Low Frequency Peripheral Clocks

Availability of oscillators and clocks in Energy Modes:

- Available in EM0/EM1
- Available in EM0/EM1/EM2
- Available in EM0/EM1/EM2/EM3
- Available in EM0/EM1/EM2/EM4
- Available in EM0/EM1/EM2/EM3/EM4

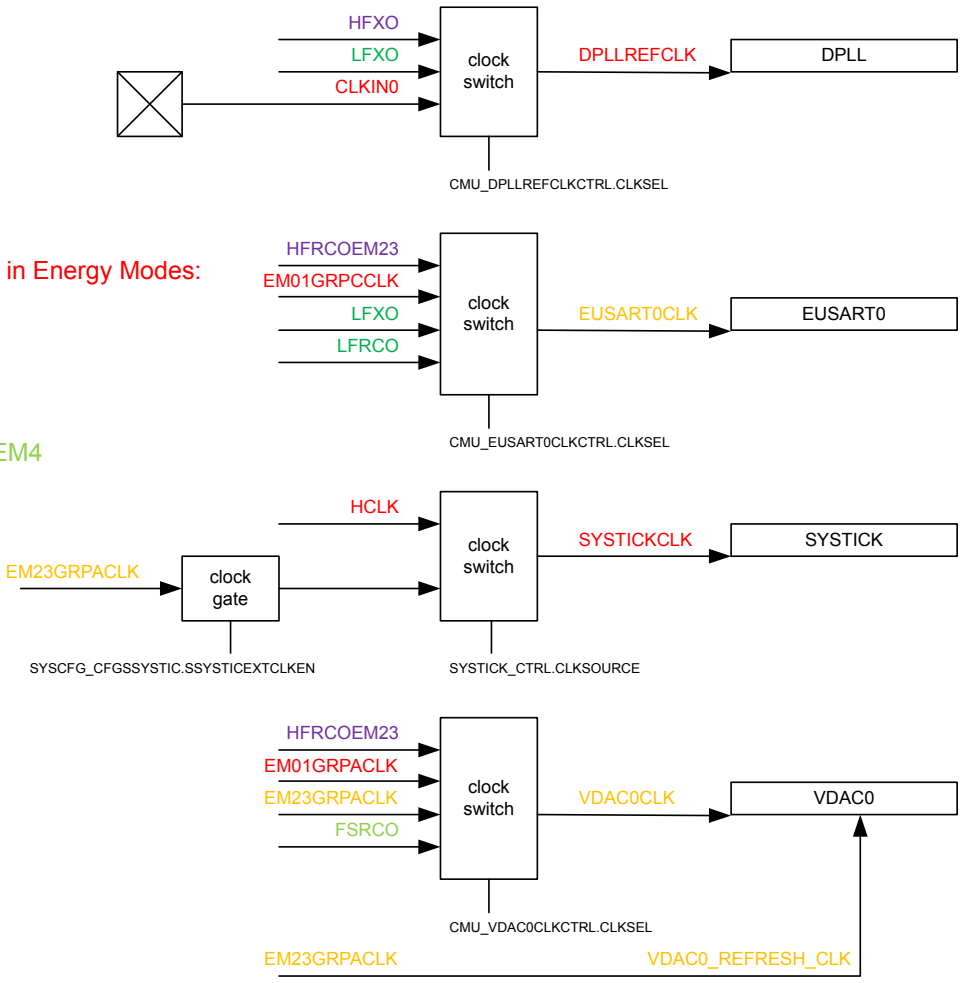


Figure 8.4. Mixed Frequency Peripheral Clocks

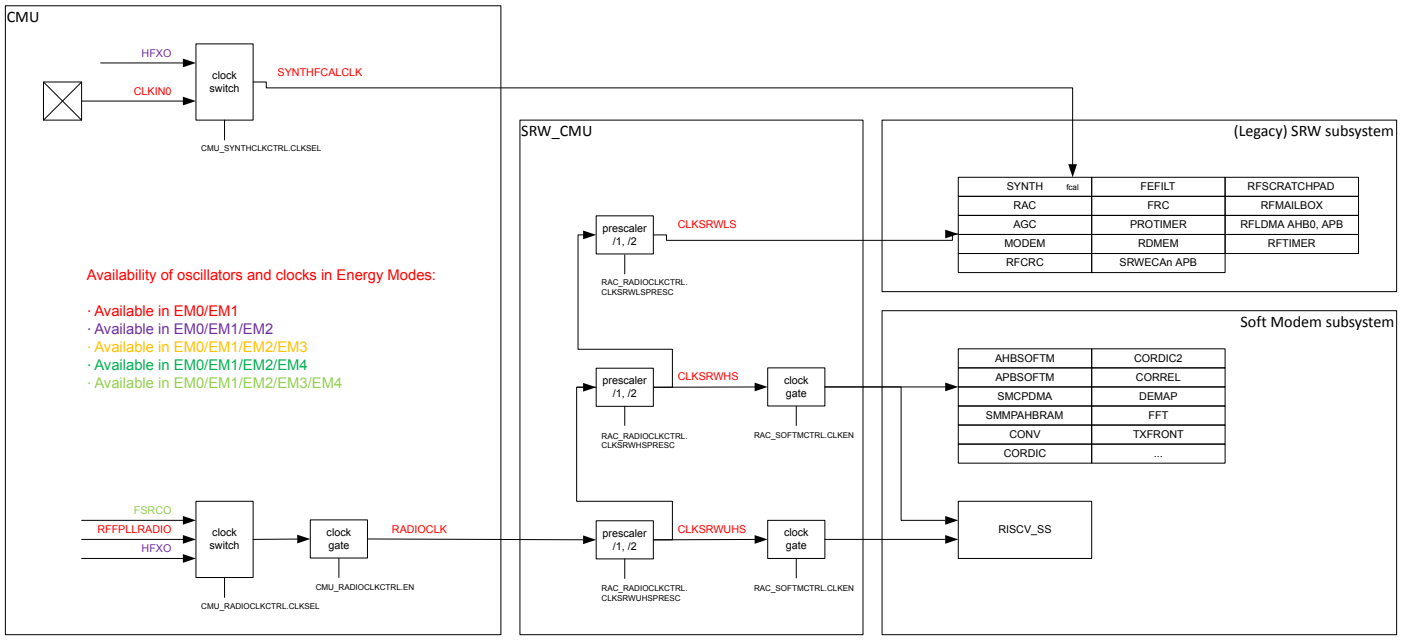


Figure 8.5. Radio Sub-system Clocks

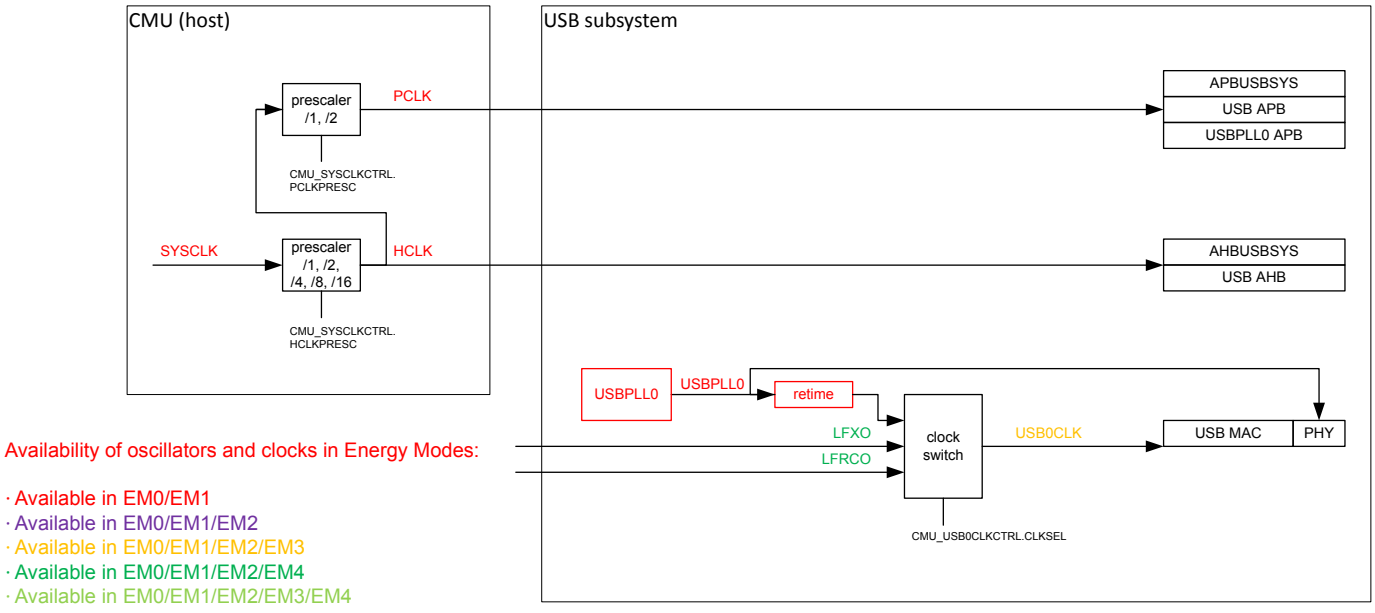


Figure 8.6. USB Sub-system Clocks

8.3.1 System Clocks

8.3.1.1 SYSCLK - Bus System Clock

SYSCLK is the selected System Clock. HCLK is an optionally prescaled version of SYSCLK. PCLK is an optionally prescaled version of HCLK. LSPCLK is always PCLK prescaled by 2. The SYSCLK, and therefore HCLK, PCLK, and LSPCLK, can be driven by a high-frequency oscillator or be driven from a pin. By default, the FSRCO is selected as the bootup oscillator. To change the selected clock source, write to the CLKSEL bitfield in CMU_SYSCLKCTRL. If an invalid option is programmed into CLKSEL, FSRCO will be selected. The SYSCLK is running in EM0 Active and EM1 Sleep and is automatically stopped in EM2 DeepSleep.

The prescaler setting can be changed dynamically and the new setting takes effect immediately. When switching to a higher frequency oscillator source, prescaler setting should be adjusted before clock selection to prevent over clocking. For the same reason, when switching to a lower frequency oscillator source, prescaler setting cannot be adjusted until the clock selection is made.

The HFXO clock is fed directly to the Radio Transceiver. The clock received by the Radio Transceiver is therefore not affected by the selected clock source for SYSCLK nor by any clock prescaler.

8.3.1.2 HCLK - AHB Clock

HCLK is a prescaled version of SYSCLK. This clock drives the AHB bus interface. Example modules include the CPU, Cache, MSC, DMA, and AES. HCLK can be prescaled by setting HCLKPRESC in CMU_SYSCLKCTRL to DIV2, DIV4, DIV8, or DIV16. This prescales HCLK to all AHB bus clocks and is typically used to save energy in applications where the system is not required to run at the highest frequency. The setting can be changed dynamically and the new setting takes effect immediately. Some of the modules that are driven by this clock can be clock gated completely when not in use. This is done by clearing the module enable (EN) bit in the module's EN register.

8.3.1.3 PCLK - APB Clock

PCLK is a prescaled version of HCLK. This clock drives the APB bus interface. Example modules include I2C, and CRC. PCLK can be prescaled by setting PCLKPRESC in CMU_SYSCLKCTRL to DIV2. This prescales PCLK to all APB bus clocks and is necessary to prevent PCLK from exceeding the maximum frequency of 50 MHz. The setting can be changed dynamically and the new setting takes effect immediately. Some of the peripherals that are driven by this clock can be clock gated completely when not in use. This is done by clearing the module enable (EN) bit in the module's EN register.

8.3.1.4 LSPCLK - Low Speed APB Clock

LSPCLK is a prescaled version of PCLK. This clock drives the Low Speed APB bus interface. Example modules include I2C. LSPCLK is always prescaled by two. This prescales LSPCLK to all Low Speed APB bus clocks and is necessary to prevent LSPCLK from exceeding the maximum frequency of 25 MHz. Some of the peripherals that are driven by this clock can be clock gated completely when not in use. This is done by clearing the module enable (EN) bit in the module's EN register.

8.3.1.5 EM01GRPACLK - Energe Mode 01 Group A Clock

EM01GRPACLK is the selected clock for the Group A Peripherals operating in Energy Modes 0 or 1. These are typically high clock frequency peripheral modules. The selection is configured using the CLKSEL field in CMU_EM01GRPACLKCTRL.

Each High Frequency Peripheral that is clocked by EM01GRPACLK may have its own prescaler setting and enable bit. The prescaler settings, if available, can be found in the peripheral's control registers. The enable bit can be found in the module's EN register.

When selecting the re-timed options, check with datasheet for frequency limitation at each voltage scaling setting.

8.3.1.6 EM01GRPCCLK - Energe Mode 01 Group C Clock

EM01GRPCCLK is the selected clock for the Group C Peripherals operating in Energy Modes 0 or 1. These are typically high clock frequency peripheral modules. The selection is configured using the CLKSEL field in CMU_EM01GRPCCLKCTRL.

Each High Frequency Peripheral that is clocked by EM01GRPCCLK may have its own prescaler setting and enable bit. The prescaler settings, if available, can be found in the peripheral's control registers. The enable bit can be found in the module's EN register.

When selecting the re-timed options, check with datasheet for frequency limitation at each voltage scaling setting.

8.3.1.7 EM23GRPACLK - Energe Mode 23 Group A Clock

EM23GRPACLK is the selected clock for the Group A Peripherals operating down to Energy Modes 2 or 3. These are typically low energy consumption peripheral modules. The selection is configured using the CLKSEL field in CMU_EM23GRPACLKCTRL.

Each Low Energy Peripheral that is clocked by EM23GRPACLK may have its own prescaler setting and enable bit. The prescaler settings, if available, can be found in the peripheral's control registers. The enable bit can be found in the module's EN register.

8.3.1.8 EM4GRPACLK - Energy Mode 4 Group A Clock

EM4GRPACLK is the selected clock for the Group A Peripherals operating down to Energy Mode 4. These are typically ultra low energy consumption peripheral modules. The selection is configured using the CLKSEL field in CMU_EM4GRPACLKCTRL.

Note:

EM4GRPACLK is in a different power domain than EM23GRPACLK, which makes it available all the way down to EM4.

Each Low Energy Peripheral that is clocked by EM4GRPACLK may have its own prescaler setting and enable bit. The prescaler settings, if available, can be found in the peripheral's control registers. The enable bit can be found in the module's EN register.

8.3.1.9 Peripheral Bus Clock Enable

Peripherals each have an individual bus clock enable bit in the CMU_CLKEN0 or CMU_CLKEN1 registers. Disabling the bus clock to a peripheral can save energy, even when that peripheral is not active.

8.3.1.10 IADCCLK - IADC Clock

IADCCLK is the selected clock for the ADC. The selection is configured using the CLKSEL field in CMU_IADCCLKCTRL.

Note:

When using a Timer as the synchronous trigger for IADC conversion, EM01GRPACLK must be selected, because Timer runs from EM01GRPACLK.

IADC has its own prescaler setting and enable bit. The prescaler settings can be found in the IADC's control registers. The enable bit can be found in the IADC's EN register.

Whichever clock source is selected as the IADC clock via the CLKSEL bitfield in the CMU_IADCCLKCTRL register, this clock will become active automatically when needed. The IADC can automatically start and stop it.

8.3.1.11 VDAC0CLK - VDAC Clock

VDAC0CLK is the selected clock for the Voltage DAC. The selection is configured using the CLKSEL field in CMU_VDAC0CLKCTRL. If operating in EM2, the EM01GRPACLK must not be chosen, as EM01GRPACLK will be shut down in these lower energy modes.

Note:

When using a Timer as the synchronous trigger for VDAC conversion, EM01GRPACLK must be selected, because Timer runs from EM01GRPACLK.

VDAC has its own prescaler setting and enable bit. The prescaler settings can be found in the VDAC's config register. The enable bit can be found in the VDAC's EN register.

Whichever clock source is selected as the VDAC clock via the CLKSEL bitfield in the CMU_VDAC0CLKCTRL register, this clock will become active automatically when needed. The VDAC can automatically start and stop it.

8.3.1.12 LESENSEHFCLK - LESENSE High Frequency Clock

LESENSEHFCLK is the selected clock for the high frequency logic of LESENSE. The selection is configured using the CLKSEL field in CMU_LESENSEHFCLKCTRL.

LESENSE has its own prescaler setting and enable bit. The prescaler settings can be found in the LESENSE's timing control registers. The enable bit can be found in the LESENSE's EN register.

Whichever clock source is selected as the LESENSEHFCLK clock via the CLKSEL bitfield in the CMU_LESENSEHFCLKCTRL register, this clock will become active automatically when needed. The LESENSE can automatically start and stop it.

8.3.1.13 SYSRTCCLK - System RTC Clock

SYSRTCCLK is the selected clock for the System Real Time Clock. The selection is configured using the CLKSEL field in CMU_SYSRTCCLKCTRL.

8.3.1.14 SYSTICKCLK - SysTick Timer Clock

SYSTICKCLK is the selected clock for CPU's SysTick Timer. The clock source can be an external clock or the processor clock, which is the HCLK frequency. The external clock source is a branch of the EM23GRPACLK that is gated by the control field SSYSTICEXTCLKEN in the SYSCFG_CFGSSYSTIC register.

8.3.1.15 PCNT0CLK - Pulse Counter Clock

PCNT0CLK is the selected clock for the Pulse Counter. The PCNT0CLK source may be selected from EM23GRPACLK switch or an external source. The selection is configured using the CLKSEL field in CMU_PCNT0CLKCTRL. The external source may come from a PRS or a GPIO, depending on the S0PRSEN setting in the PCNT's config register.

8.3.1.16 EUSART0CLK - EUSART Clock

EUSART0CLK is the selected clock for the EUSART peripherals. The selection is configured using the CLKSEL field in CMU_EUSART0CLKCTRL. If operating in EM2, the EM01GRPCCLK must not be chosen, as EM01GRPCCLK will be shut down in these lower energy modes.

EUSART has its own prescaler setting and enable bit. The prescaler settings can be found in the EUSART's config registers. The enable bit can be found in the EUSART's EN register.

8.3.1.17 TRACECLK - Debug Trace Clock

TRACECLKIN is the selected clock for the TPIU. The TPIU acts as a bridge between the on-chip trace data from the Embedded Trace Macrocell (ETM) and the Instrumentation Trace Macrocell (ITM). The selection is configured using the CLKSEL field in CMU_TRACECLKCTRL. In addition, the CMU scales this clock via the PRESC field in the CMU_TRACECLKCTRL register. The debug trace clock input is limited to 40 MHz maximum. Therefore, if the SYSCLK or other selected sources is 40 MHz or less, the default DIV1 setting may be used. Otherwise, use DIV2 or higher divider to avoid data pump overflow. Note that this register should be configured properly before enabling ETM.

8.3.1.18 DAPCLK - Debug Access Port Clock

DAPCLK is the selected clock for all debug access port. By default, the FSRCO is selected as the clock source. When debug access port is used to trim FSRCO frequency, software needs to change the selected clock source by writing to the CLKSEL bitfield in CMU_DAPCLKCTRL. This allows debug access port to operate with another clock source uninterrupted, while FSRCO frequency is changing.

8.3.1.19 WDOGCLK - Watchdog Timer Clock

The Watchdog Timer (WDOG) can be configured to use one of the low frequency clock sources. Select option HCLKDIV1024 to track Watchdog timeout with CPU clock speed.

8.3.1.20 RADIOCLK - Radio Sub-System Clock

RADIOCLK is the selected Radio Transceiver Sub-system clock. CLKSRWUHS is an optionally prescaled version of RADIOCLK. CLKSRWHS is an optionally prescaled version of CLKSRWUHS. CLKSRWLS is an optionally prescaled version of CLKSRWHS. Because the Radio Transceiver Sub-system has a clock switch independent from SYSCLK, the clock received by the Radio Transceiver is not affected by SYSCLK. By default, the FSRCO is selected as the bootup oscillator. To change the selected clock source, write to the CLKSEL bitfield in CMU_RADIOCLKCTRL.

A clock enable controls the entire Radio Transceiver Sub-system. Before accessing the radio bus bridge, this clock enable, EN in CMU_RADIOCLKCTRL, must be set. A corresponding running status, RADIOCLKRUNNING in CMU_STATUS, should be polled before issuing bus transactions to avoid bus fault. Similarly, a clock enable controls the Soft Modem Sub-system. Before accessing the soft modem bus bridge, this clock enable, CLKEN in RAC_SOFTMCTRL, must be set. In the same register, a running status, CLKRUNNING, should be polled before issuing bus transactions to avoid bus fault.

Controls for prescaling CLKSRWUHS, CLKSRWHS, and CLKSRWLS are located in RAC_RADIOCLKCTRL register. CLKSRWUHS must be kept below the maximum frequency of 160 MHz, close to 80 MHz or 160 MHz depending on the MIPS requirement of the RISCV processor. CLKSRWHS must be kept below the maximum frequency of 80 MHz and close to 80 MHz for the proper operation of the soft modem coprocessors. CLKSRWLS must be kept below the maximum frequency of 40 MHz and close to 40 MHz for the legacy SRW Sub-system.

8.3.1.21 USB0CLK - USB MAC Clock

USB0CLK is the selected USB MAC clock. By default, the USBPLL0 is selected as the clock source generating a 48 MHz clock frequency. Before USB enters suspend mode, software should configure the CLKSEL bitfield in CMU_USB0CLKCTRL to select one of the low frequency clock sources (LFXO or LFRCO) to ensure that wakeup events are captured during USB suspend while the system is in EM2.

To mitigate radio frequency interference, the USBPLL0 clock is retimed before driving USB MAC logic. However, the USB PHY interface must use non-retimed clock to avoid jitter. Special synchronization logic transfers data between the USB MAC and USB PHY.

All the system bus interface logic in the USB Sub-system are driven by HCLK and PCLK from the host bus system clock. Before accessing the USB bus bridge (including USB APB and USBPLL0 APB), the USB bus clock enable bit, CMU_CLKEN1.USB, must be set to avoid a bus fault.

8.3.2 Switching Clock Source

The FSRCO oscillator is a fixed frequency (20 MHz), low energy oscillator with extremely short start-up time. Therefore, this oscillator is chosen by hardware as the clock source for SYSCLK when the device starts up (e.g. after reset).

Software can switch between the different clock sources at run-time. For example, when the HFRCODPLL is the clock source, software can switch to HFXO by writing the field CLKSEL in the CMU_SYSCLKCTRL register. See Figure 8.7 CMU Switching From HFRCO to HFXO Before HFXO is Ready on page 169 for a description of the sequence of events for this specific operation.

When switching the SYSCLK to HFXO via the CLKSEL bitfield in CMU_SYSCLKCTRL, HFXO is automatically started. Switching to an oscillator that is not ready yet, the SYSCLK will stop for the duration of the oscillator start-up time. This effectively stalls the Core Modules. It is possible to avoid this by first enabling the target oscillator (e.g. HFXO) and then waiting for that oscillator to become ready before switching the clock source. This way, the system continues to run on the HFRCO until the target oscillator (e.g. HFXO) is ready and provides a reliable clock. This sequence of events is shown in Figure 8.8 CMU Switching From HFRCO to HFXO After HFXO is Ready on page 170.

Generally, all oscillators have a separate flag that is set when the oscillator is ready. This flag can also be configured to generate an interrupt.

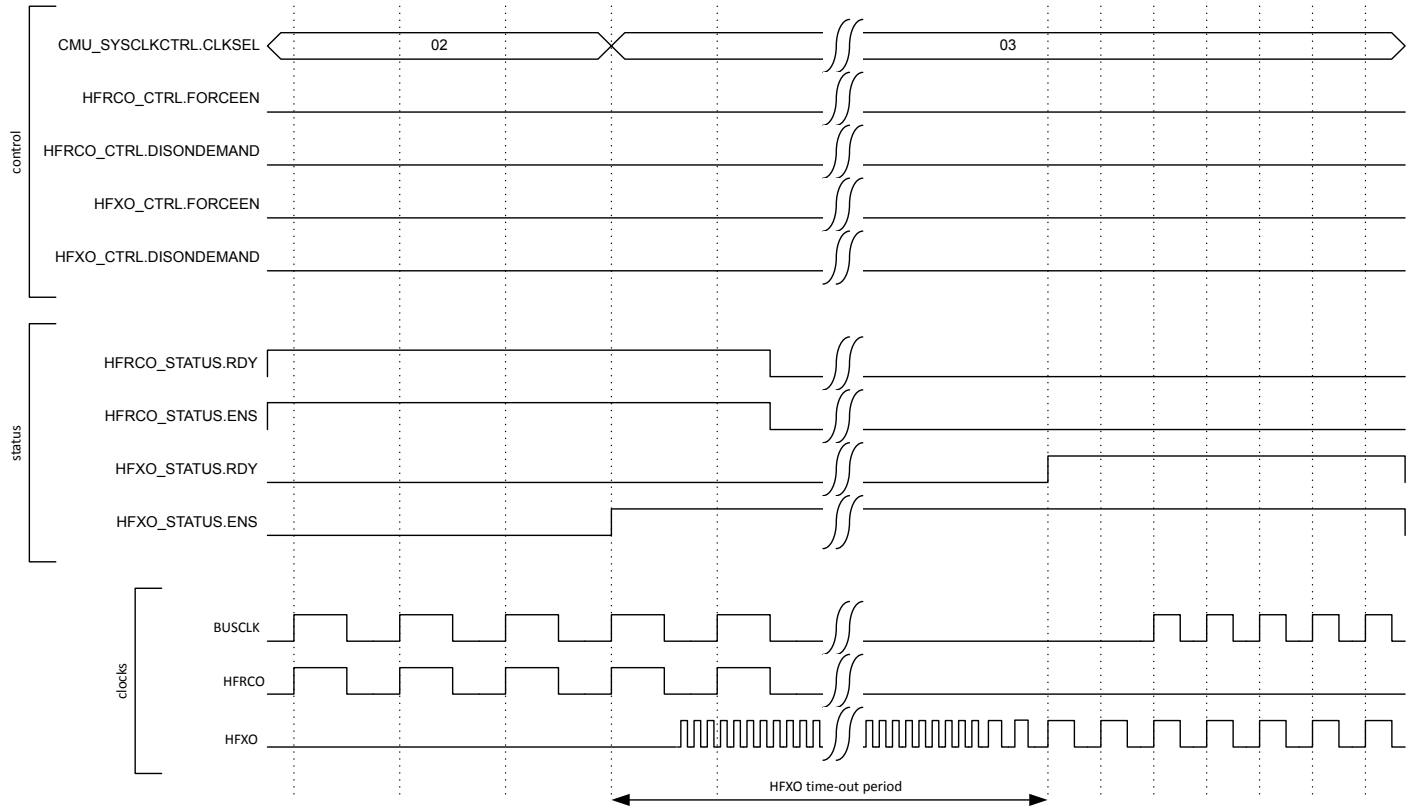


Figure 8.7. CMU Switching From HFRCO to HFXO Before HFXO is Ready

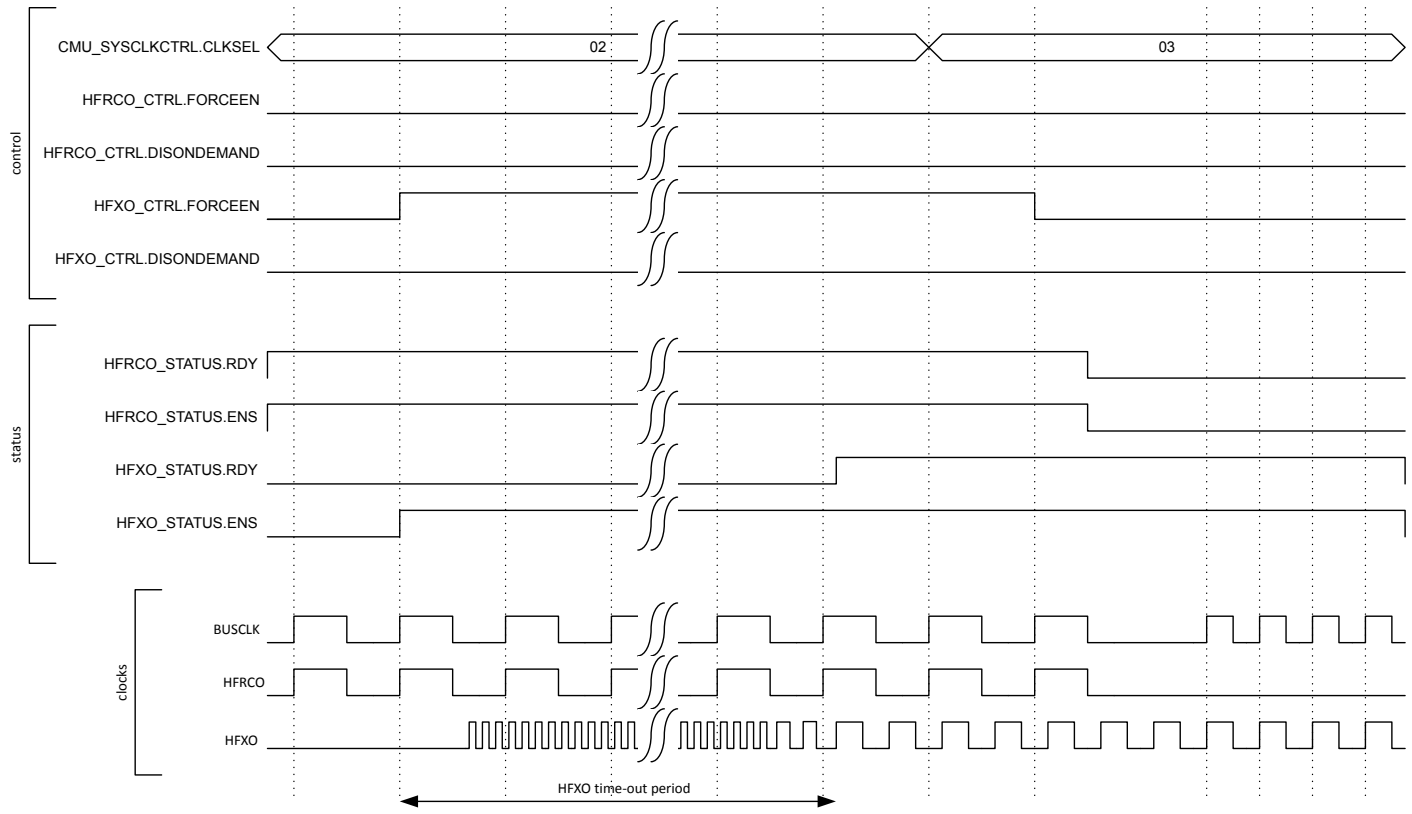


Figure 8.8. CMU Switching From HFRCO to HFXO After HFXO is Ready

Switching clock source for various clock switches is done by setting the CLKSEL bitfields in CMU_*CLKCTRL. To ensure no stalls in the peripherals, the clock source should be ready before switching to it.

Note: To save energy, remember to disable all clock switches and/or module enable bits when not in use.

8.3.3 RC Oscillator Calibration

The CMU has built-in HW support to efficiently calibrate the RC oscillators (LFRCO, HFRCODPLL, HFRCOEM23) at run-time, see Figure 8.9 HW-support for RC Oscillator Calibration on page 171 for an illustration of this circuit.

The concept is to select a reference and compare the RC frequency with the reference frequency. When the calibration circuit is started, one down-counter running on a selectable clock (DOWNSEL in CMU_CALCTRL) and one up-counter running on a selectable clock (UPSEL in CMU_CALCTRL) are started simultaneously. The top value for the down-counter must be written (CALTOP in CMU_CALTOP) before calibration is started. The down-counter counts for CALTOP+1 cycles. When the down-counter has reached 0, the up-counter is sampled and the CALRDYIF interrupt flag is set. If CONT in CMU_CALCTRL is cleared, the counters are stopped after finishing the ongoing calibration. If continuous mode is selected by setting CONT in CMU_CALCTRL, the down-counter reloads the top value and continues counting, while the up-counter restarts from 0.

Software can then read out the sampled up-counter value from CMU_CALCNT. The up-counter has counted (the sampled value)+1 cycles. The ratio between the reference and the oscillator subject to the calibration can easily be found using (the top value)+1 and (the sampled value)+1. Overflows of the up-counter will not occur. If the up-counter reaches its top value before the down-counter reaches 0, the up-counter stays at its top value. Calibration can be started and stopped by writing CALSTART and CALSTOP bitfields in CMU_CALCMD respectively. With this HW support, it is simple to write efficient calibration algorithms in software.

If the wrap-around feature is enabled by setting WRAPUP in CMU_CALCTRL, the up-counter will continue to count from 0 after reaching its top value. The software should know if wrap-around happened based on the DOWN clock frequency and the expected UP clock frequency. In this case, the total up-counter value can be calculated by adding the value from CMU_CALCNT and its top value.

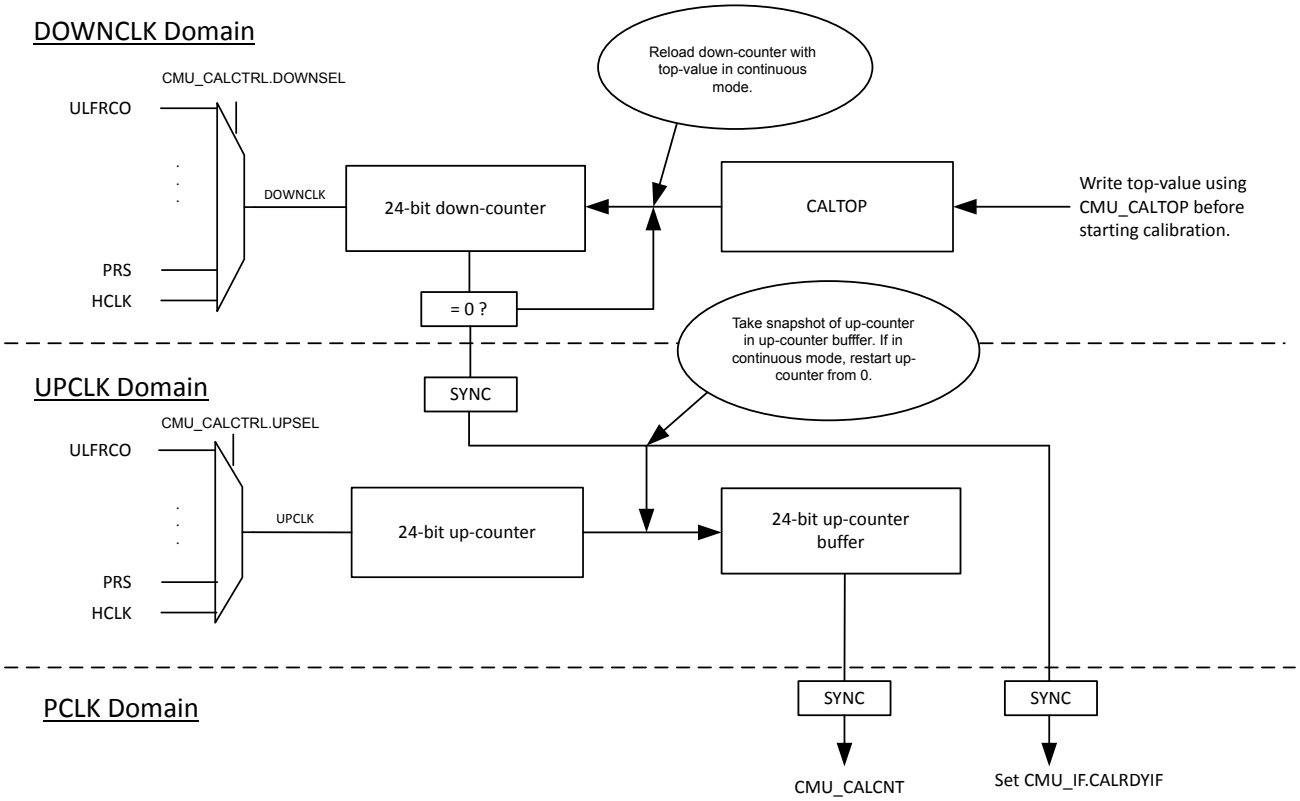


Figure 8.9. HW-support for RC Oscillator Calibration

The counter operation for single and continuous mode are shown in Figure 8.10 Single Calibration (CONT=0) on page 172 and Figure 8.11 Continuous Calibration (CONT=1) on page 172 respectively.

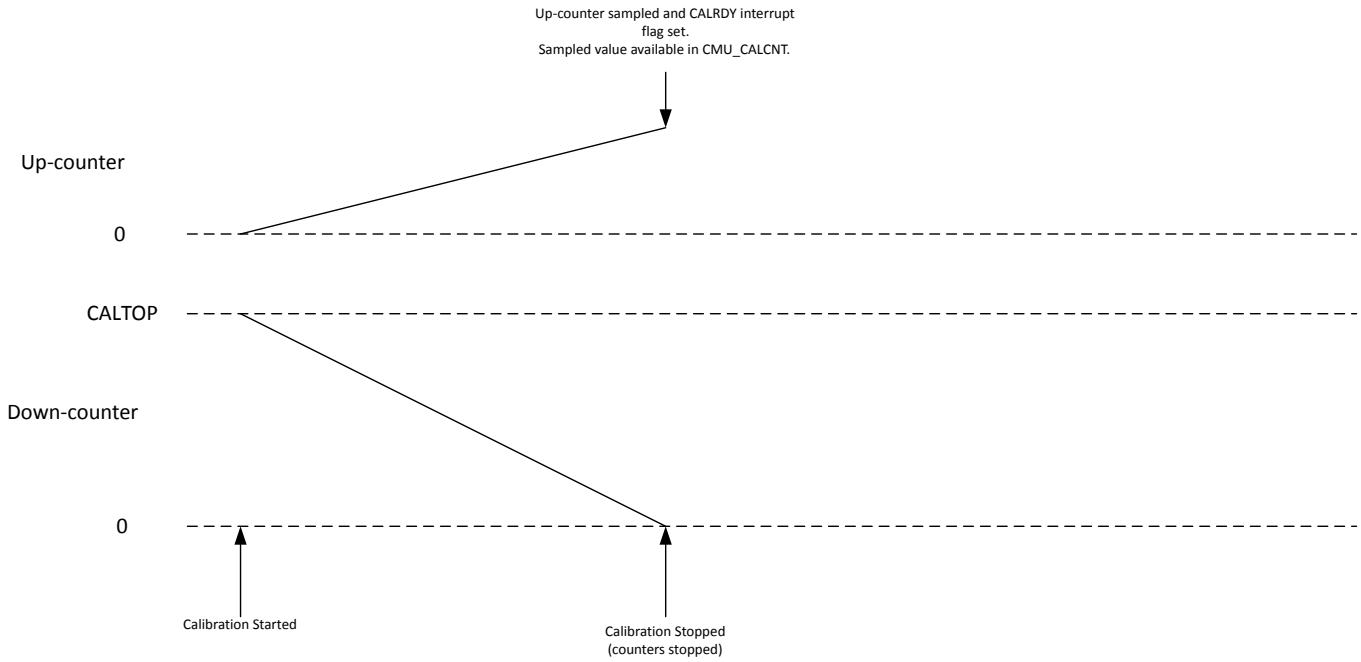


Figure 8.10. Single Calibration (CONT=0)

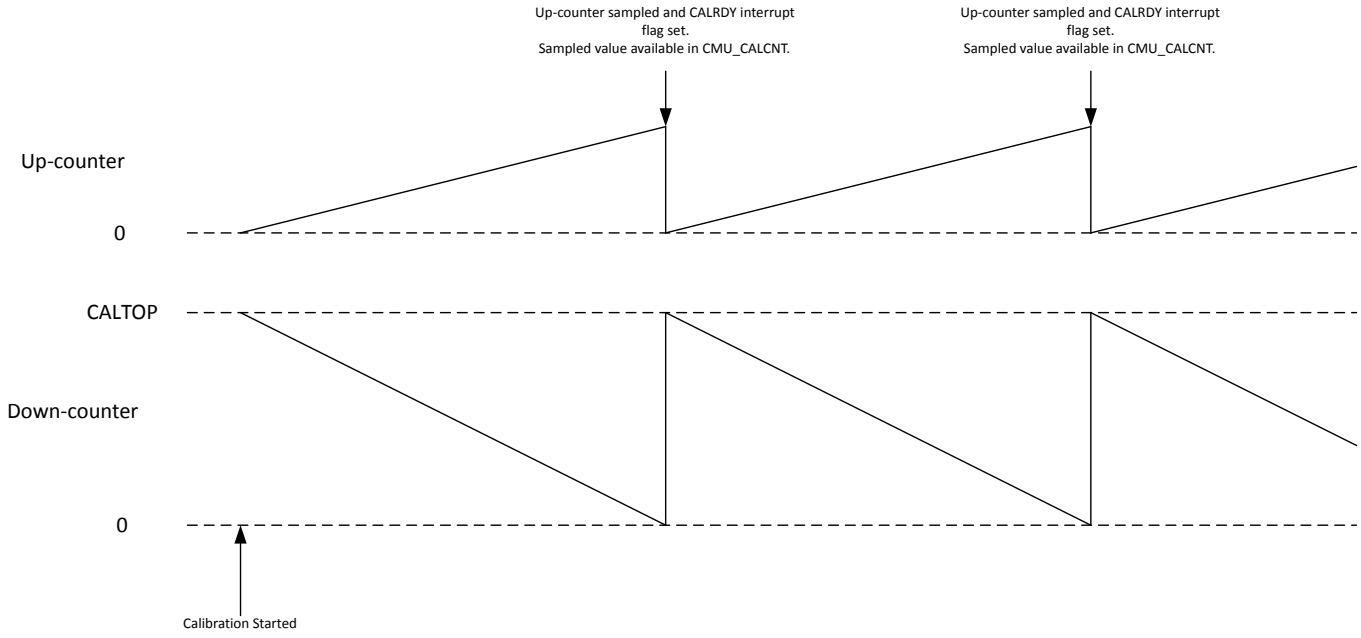


Figure 8.11. Continuous Calibration (CONT=1)

8.3.4 Energy Modes

The availability of oscillators and clocks depends on the chosen energy mode. By default, the high frequency oscillators (HFRCODPLL, HFRCOEM23, and HFXO) and high frequency clocks (SYSCLK, HCLK, PCLK, RADIOCLK, and EM01GRPACLK) are available down to EM1 Sleep. From EM2 DeepSleep onwards these oscillators and clocks are normally off, although special cases exist as summarized in Table 8.1 Oscillator and clock availability in Energy Modes on page 173. The CMU overview figure in Figure 8.1 Bus Clocks on page 160 also indicates which oscillators and clocks can be used in what energy modes.

The low frequency oscillators (LFRCO and LFXO) are available in all energy modes except in EM3 Stop when they are off by definition. By default, these oscillators are also off in EM4 Shutoff, but they can be requested on in these states as well if needed. The ultra low frequency oscillator (ULFRCO) is on in all energy modes, except for EM4 Shutoff, but it can be requested on in that state as well if needed. The low frequency clocks (EM23GRPACLK, EM4GRPACLK, WDOGCLK, SYSRTCCLK) are in various power domains and therefore their availability not only depends on the chosen clock source, but also on the chosen energy mode as indicated in Table 8.1 Oscillator and clock availability in Energy Modes on page 173.

Table 8.1. Oscillator and clock availability in Energy Modes

	EM0 Active / EM1 Sleep	EM2 DeepSleep	EM3 Stop	EM4 Shutoff
HFRCODPLL	On[1]	Off	Off	Off
RFFPLL	On[1]	Off	Off	Off
PLL0	On[1]	Off	Off	Off
HFXO	On[1]	On[2]	On[2]	Off
HFRCOEM23	On[1]	On[2]	On[2]	Off
LFRCO, LFXO	On[1]	On[2]	Off	On[2]
ULFRCO	On	On	On	On[2]
SYSCLK, HCLK, PCLK, RADIOCLK, EM01GRPACLK	On[1]	Off	Off	Off
IADCCLK	On[1]	On[2]	On[2]	Off
EM23GRPACLK, WDOGCLK, SYSRTCCLK	On[1]	On[2]	On[3]	Off
EM4GRPACLK	On[1]	On[2]	On[3]	On[2]

1 Under software control.
2 Default off, but kept active if requested by modules.
3 On only if ULFRCO is used as clock source.

8.3.5 Clock Output

The CMU has up to three CLKOUTn signals that can be routed to the PRS or GPIO. The selections for CLKOUTn are controlled using the CLKOUTSELn bitfields in CMU_EXPORTCLKCTRL (CLKOUTSEL0 controls CLKOUT0, for example).

The following clocks can be selected for CLKOUTn:

- HCLK and EXPORTCLK. The HCLK is the high frequency clock for AHB. The EXPORTCLK is a prescaled version of SYSCLK as controlled by the PRESC bitfield in the CMU_EXPORTCLKCTRL register.
- The qualified clock from any of the on-chip oscillators. A qualified clock will not have any glitches or skewed duty-cycle during start-up. For the LFXO and HFXO, correct configuration of the TIMEOUT bitfield(s) in LFXO_CFG and HFXO_XTALCFG, respectively is required to guarantee a properly qualified clock.

HCLK will only have a 50-50 duty cycle when HCLKPRESC in CMU_SYSCLKCTRL is DIV1. EXPORTCLK will only be 50-50 duty cycle when the selected division factor is even.

The CLKOUTn signals may be routed to GPIO via the DBUS as CMU.CLKOUTn using controls in the GPIO registers. The required output pins must be enabled in the GPIO_CMU_ROUTEEN register and the pin locations can be configured in the GPIO_CMU_CLKOUTnROUTE registers.

The CLKOUTn signals can also be used as PRS producers (see 14.3.3 Producers for more detail on PRS producers). CLKOUTn signals used as PRS producers may be simultaneously routed to GPIO, but this is not required to use CLKOUTn as a PRS producer.

8.3.6 Clock Input from a Pin

It is possible to configure the CMU to input a clock from the CMU_CLKI0. This clock can be selected to drive SYSCLK and DPLL reference using CMU_SYSCLKCTRL.CLKSEL and CMU_DPLLREFCLKCTRL.CLKSEL respectively. The required input pin locations can be configured in the GPIO_CMU_CLKIN0ROUTE register.

8.3.7 Interrupts

The interrupts generated by the CMU module are combined into one interrupt vector. If CMU interrupts are enabled, an interrupt will be made if one or more of the interrupt flags in CMU_IF and their corresponding bits in CMU_IEN are set.

8.3.8 Protection

It is possible to lock the control and command registers to prevent unintended software writes to critical clock settings. This is controlled by the CMU_LOCK register.

The WDOGCLKCTRL registers are separately locked by CMU_WDOGLOCK register. This is to prevent EM3 Stop mode from disabling the watch dog clocks inadvertently.

In addition to software locks, hardware locks are implemented to prevent metastability. CMU_CALCTRL is locked by hardware when calibration is started by CMU_CALCMD.CALSTART. CMU_DPLLREFCLKCTRL is locked by hardware when DPLL is enabled via DPLL_EN.EN. Because these switches are not glitch-less, clock selection must be configured before enabling the operation and cannot be changed during operation.

8.4 CMU Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	CMU_IPVERSION	R	IP Version ID
0x008	CMU_STATUS	RH	Status Register
0x010	CMU_LOCK	W	Configuration Lock Register
0x014	CMU_WDOGLOCK	W	WDOG Configuration Lock Register
0x020	CMU_IF	RWH INTFLAG	Interrupt Flag Register
0x024	CMU_IEN	RW	Interrupt Enable Register
0x050	CMU_CALCMD	W	Calibration Command Register
0x054	CMU_CALCTRL	RW	Calibration Control Register
0x058	CMU_CALCNT	R	Calibration Result Counter Register
0x05C	CMU_CALTOP	RW	Calibration Top Value Register
0x064	CMU_CLKEN0	RW	Clock Enable Register 0
0x068	CMU_CLKEN1	RW	Clock Enable Register 1
0x070	CMU_SYSCLKCTRL	RW	System Clock Control
0x080	CMU_TRACECLKCTRL	RW	Debug Trace Clock Control
0x090	CMU_EXPORTCLKCTRL	RW	Export Clock Control
0x100	CMU_DPLLREFCLKCTRL	RW	Digital PLL Reference Clock Control
0x120	CMU_EM01GRPACLKCTRL	RW	EM01 Peripheral Group a Clock Control
0x128	CMU_EM01GRPCCLKCTRL	RW	EM01 Peripheral Group C Clock Control
0x140	CMU_EM23GRPACLKCTRL	RW	EM23 Peripheral Group a Clock Control
0x160	CMU_EM4GRPACLKCTRL	RW	EM4 Peripheral Group a Clock Control
0x180	CMU_IADCCLKCTRL	RW	IADC Clock Control
0x200	CMU_WDOG0CLKCTRL	RW	Watchdog0 Clock Control
0x208	CMU_WDOG1CLKCTRL	RW	Watchdog1 Clock Control
0x220	CMU_EUSART0CLKCTRL	RW	EUSART0 Clock Control
0x240	CMU_SYSRTC0CLKCTRL	RW	System RTC0 Clock Control
0x260	CMU_VDAC0CLKCTRL	RW	VDAC0 Clock Control
0x270	CMU_PCNT0CLKCTRL	RW	Pulse Counter 0 Clock Control
0x280	CMU_RADIOCLKCTRL	RW	Radio Clock Control
0x284	CMU_DAPCLKCTRL	RW	DAP Clock Control
0x290	CMU_LESENSEHFCLKCTRL	RW	LESENSE HF Clock Control
0x2A0	CMU_USB0CLKCTRL	RW	USB0 Clock Control
0x1000	CMU_IPVERSION_SET	R	IP Version ID
0x1008	CMU_STATUS_SET	RH	Status Register
0x1010	CMU_LOCK_SET	W	Configuration Lock Register
0x1014	CMU_WDOGLOCK_SET	W	WDOG Configuration Lock Register

Offset	Name	Type	Description
0x1020	CMU_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x1024	CMU_IEN_SET	RW	Interrupt Enable Register
0x1050	CMU_CALCMD_SET	W	Calibration Command Register
0x1054	CMU_CALCTRL_SET	RW	Calibration Control Register
0x1058	CMU_CALCNT_SET	R	Calibration Result Counter Register
0x105C	CMU_CALTOP_SET	RW	Calibration Top Value Register
0x1064	CMU_CLKEN0_SET	RW	Clock Enable Register 0
0x1068	CMU_CLKEN1_SET	RW	Clock Enable Register 1
0x1070	CMU_SYSCLKCTRL_SET	RW	System Clock Control
0x1080	CMU_TRACECLKCTRL_SET	RW	Debug Trace Clock Control
0x1090	CMU_EXPORTCLKCTRL_SET	RW	Export Clock Control
0x1100	CMU_DPLLREFCLKCTRL_SET	RW	Digital PLL Reference Clock Control
0x1120	CMU_EM01GRPACLKCTRL_SET	RW	EM01 Peripheral Group a Clock Control
0x1128	CMU_EM01GRPCCLKCTRL_SET	RW	EM01 Peripheral Group C Clock Control
0x1140	CMU_EM23GRPACLKCTRL_SET	RW	EM23 Peripheral Group a Clock Control
0x1160	CMU_EM4GRPACLKCTRL_SET	RW	EM4 Peripheral Group a Clock Control
0x1180	CMU_IADCCLKCTRL_SET	RW	IADC Clock Control
0x1200	CMU_WDOG0CLKCTRL_SET	RW	Watchdog0 Clock Control
0x1208	CMU_WDOG1CLKCTRL_SET	RW	Watchdog1 Clock Control
0x1220	CMU_EUSART0CLKCTRL_SET	RW	EUSART0 Clock Control
0x1240	CMU_SYSRTC0CLKCTRL_SET	RW	System RTC0 Clock Control
0x1260	CMU_VDAC0CLKCTRL_SET	RW	VDAC0 Clock Control
0x1270	CMU_PCNT0CLKCTRL_SET	RW	Pulse Counter 0 Clock Control
0x1280	CMU_RADIOCLKCTRL_SET	RW	Radio Clock Control
0x1284	CMU_DAPCLKCTRL_SET	RW	DAP Clock Control
0x1290	CMU_LESENSEHFCLKCTRL_SET	RW	LESENSE HF Clock Control
0x12A0	CMU_USB0CLKCTRL_SET	RW	USB0 Clock Control
0x2000	CMU_IPVERSION_CLR	R	IP Version ID
0x2008	CMU_STATUS_CLR	RH	Status Register
0x2010	CMU_LOCK_CLR	W	Configuration Lock Register
0x2014	CMU_WDOGLOCK_CLR	W	WDOG Configuration Lock Register
0x2020	CMU_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x2024	CMU_IEN_CLR	RW	Interrupt Enable Register
0x2050	CMU_CALCMD_CLR	W	Calibration Command Register
0x2054	CMU_CALCTRL_CLR	RW	Calibration Control Register

Offset	Name	Type	Description
0x2058	CMU_CALCNT_CLR	R	Calibration Result Counter Register
0x205C	CMU_CALTOP_CLR	RW	Calibration Top Value Register
0x2064	CMU_CLKEN0_CLR	RW	Clock Enable Register 0
0x2068	CMU_CLKEN1_CLR	RW	Clock Enable Register 1
0x2070	CMU_SYSCLKCTRL_CLR	RW	System Clock Control
0x2080	CMU_TRACECLKCTRL_CLR	RW	Debug Trace Clock Control
0x2090	CMU_EXPORTCLKCTRL_CLR	RW	Export Clock Control
0x2100	CMU_DPLLREFCLKCTRL_CLR	RW	Digital PLL Reference Clock Control
0x2120	CMU_EM01GRPACLKCTRL_CLR	RW	EM01 Peripheral Group a Clock Control
0x2128	CMU_EM01GRPCCLKCTRL_CLR	RW	EM01 Peripheral Group C Clock Control
0x2140	CMU_EM23GRPACLKCTRL_CLR	RW	EM23 Peripheral Group a Clock Control
0x2160	CMU_EM4GRPACLKCTRL_CLR	RW	EM4 Peripheral Group a Clock Control
0x2180	CMU_IADCCLKCTRL_CLR	RW	IADC Clock Control
0x2200	CMU_WDOG0CLKCTRL_CLR	RW	Watchdog0 Clock Control
0x2208	CMU_WDOG1CLKCTRL_CLR	RW	Watchdog1 Clock Control
0x2220	CMU_EUSART0CLKCTRL_CLR	RW	EUSART0 Clock Control
0x2240	CMU_SYSRTC0CLKCTRL_CLR	RW	System RTC0 Clock Control
0x2260	CMU_VDAC0CLKCTRL_CLR	RW	VDAC0 Clock Control
0x2270	CMU_PCNT0CLKCTRL_CLR	RW	Pulse Counter 0 Clock Control
0x2280	CMU_RADIOCLKCTRL_CLR	RW	Radio Clock Control
0x2284	CMU_DAPCLKCTRL_CLR	RW	DAP Clock Control
0x2290	CMU_LESENSEHFCLKCTRL_CLR	RW	LESENSE HF Clock Control
0x22A0	CMU_USB0CLKCTRL_CLR	RW	USB0 Clock Control
0x3000	CMU_IPVERSION_TGL	R	IP Version ID
0x3008	CMU_STATUS_TGL	RH	Status Register
0x3010	CMU_LOCK_TGL	W	Configuration Lock Register
0x3014	CMU_WDOGLOCK_TGL	W	WDOG Configuration Lock Register
0x3020	CMU_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x3024	CMU_IEN_TGL	RW	Interrupt Enable Register
0x3050	CMU_CALCMD_TGL	W	Calibration Command Register
0x3054	CMU_CALCTRL_TGL	RW	Calibration Control Register
0x3058	CMU_CALCNT_TGL	R	Calibration Result Counter Register
0x305C	CMU_CALTOP_TGL	RW	Calibration Top Value Register
0x3064	CMU_CLKEN0_TGL	RW	Clock Enable Register 0
0x3068	CMU_CLKEN1_TGL	RW	Clock Enable Register 1

Offset	Name	Type	Description
0x3070	CMU_SYSCLKCTRL_TGL	RW	System Clock Control
0x3080	CMU_TRACECLKCTRL_TGL	RW	Debug Trace Clock Control
0x3090	CMU_EXPORTCLKCTRL_TGL	RW	Export Clock Control
0x3100	CMU_DPLLREFCLKCTRL_TGL	RW	Digital PLL Reference Clock Control
0x3120	CMU_EM01GRPACLKCTRL_TGL	RW	EM01 Peripheral Group a Clock Control
0x3128	CMU_EM01GRPCCLKCTRL_TGL	RW	EM01 Peripheral Group C Clock Control
0x3140	CMU_EM23GRPACLKCTRL_TGL	RW	EM23 Peripheral Group a Clock Control
0x3160	CMU_EM4GRPACLKCTRL_TGL	RW	EM4 Peripheral Group a Clock Control
0x3180	CMU_IADCCLKCTRL_TGL	RW	IADC Clock Control
0x3200	CMU_WDOG0CLKCTRL_TGL	RW	Watchdog0 Clock Control
0x3208	CMU_WDOG1CLKCTRL_TGL	RW	Watchdog1 Clock Control
0x3220	CMU_EUSART0CLKCTRL_TGL	RW	EUSART0 Clock Control
0x3240	CMU_SYSRTC0CLKCTRL_TGL	RW	System RTC0 Clock Control
0x3260	CMU_VDAC0CLKCTRL_TGL	RW	VDAC0 Clock Control
0x3270	CMU_PCNT0CLKCTRL_TGL	RW	Pulse Counter 0 Clock Control
0x3280	CMU_RADIOCLKCTRL_TGL	RW	Radio Clock Control
0x3284	CMU_DAPCLKCTRL_TGL	RW	DAP Clock Control
0x3290	CMU_LESENSEHFCLKCTRL_TGL	RW	LESENSE HF Clock Control
0x32A0	CMU_USB0CLKCTRL_TGL	RW	USB0 Clock Control

8.5 CMU Register Description

8.5.1 CMU_IPVERSION - IP Version ID

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x4																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x4	R	**IP Version ID**

8.5.2 CMU_STATUS - Status Register

Offset	Bit Position																														
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0																														0x0
Access	R	R																														R
Name	LOCK	WDOGLOCK																														CALRDY

Bit	Name	Reset	Access	Description
31	LOCK	0x0	R	**Configuration Lock Status**
	Indicates the current status of configuration lock			
	Value	Mode		Description
	0	UNLOCKED		Configuration lock is unlocked
	1	LOCKED		Configuration lock is locked
30	WDOGLOCK	0x0	R	**Configuration Lock Status for WDOG**
	Indicates the current status of WDOG configuration lock			
	Value	Mode		Description
	0	UNLOCKED		WDOG configuration lock is unlocked
	1	LOCKED		WDOG configuration lock is locked
29:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	CALRDY	0x0	R	**Calibration Ready**
	Calibration is Ready (0 when calibration is ongoing).			

8.5.3 CMU_LOCK - Configuration Lock Register

Offset	Bit Position																															
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x93F7															
Access																	W															
Name																	LOCKKEY															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LOCKKEY	0x93F7	W	**Configuration Lock Key**

Write any other value than the unlock code to lock registers from editing. Write the unlock code to unlock.

Value	Mode	Description
37879	UNLOCK	Write this value to unlock

8.5.4 CMU_WDOGLOCK - WDOG Configuration Lock Register

Offset	Bit Position																															
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x5257															
Access																	W															
Name																	LOCKKEY															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LOCKKEY	0x5257	W	**Configuration Lock Key**

Write any other value than the unlock code to lock registers from editing. Write the unlock code to unlock.

Value	Mode	Description
37879	UNLOCK	Write this value to unlock

8.5.5 CMU_IF - Interrupt Flag Register

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															RW	RW
Name																															CALOF	CALRDY

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	CALOF	0x0	RW	**Calibration Overflow Interrupt Flag**
	Set when calibration overflow has occurred (i.e. if a new calibration completes before CMU_CALSTATUS has been read)			
0	CALRDY	0x0	RW	**Calibration Ready Interrupt Flag**
	Set when calibration is completed			

8.5.6 CMU_IEN - Interrupt Enable Register

Offset	Bit Position																													
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															RW	RW
Name																															CALOF	CALRDY

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	CALOF	0x0	RW	**Calibration Overflow Interrupt Enable**
	Enable/disable CALOF interrupt			
0	CALRDY	0x0	RW	**Calibration Ready Interrupt Enable**
	Enable/disable CALRDY interrupt			

8.5.7 CMU_CALCMD - Calibration Command Register

Offset	Bit Position																													
0x050	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															W(nB)	W(nB)
Name																															CALSTOP	CALSTART

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	CALSTOP	0x0	W(nB)	**Calibration Stop**
	Stops the calibration counters.			
0	CALSTART	0x0	W(nB)	**Calibration Start**
	Starts the calibration, effectively loading the CMU_CALCTRL.CALCNT into the down-counter and start decrementing.			

8.5.8 CMU_CALCTRL - Calibration Control Register

Offset	Bit Position																													
0x054	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0				0x0				0x0	0x0																						
Access	RW				RW				RW	RW																						
Name	DOWNSEL				UPSEL				CONT	WRAPUP																						

Bit	Name	Reset	Access	Description
31:28	DOWNSEL	0x0	RW	**Calibration Down-counter Select**

Selects clock source for the calibration down-counter. Changing this while calibration is running results in bus fault..

Value	Mode	Description
0	DISABLED	Down-counter is not clocked
1	HCLK	HCLK is clocking down-counter
2	PRS	PRS CMU_CALDN consumer is clocking down-counter
3	HFXO	HFXO is clocking down-counter
4	LFXO	LFXO is clocking down-counter
5	HFRCODPLL	HFRCODPLL is clocking down-counter
6	HFRCOEM23	HFRCOEM23 is clocking down-counter
9	FSRCO	FSRCO is clocking down-counter
10	LFRCO	LFRCO is clocking down-counter
11	ULFRCO	ULFRCO is clocking down-counter

Bit	Name	Reset	Access	Description
27:24	UPSEL	0x0	RW	**Calibration Up-counter Select**

Selects clock source for the calibration up-counter. Changing this while calibration is running results in bus fault.

Value	Mode	Description
0	DISABLED	Up-counter is not clocked
1	HCLK	HCLK is clocking up-counter
2	PRS	PRS CMU_CALUP consumer is clocking up-counter
3	HFXO	HFXO is clocking up-counter
4	LFXO	LFXO is clocking up-counter
5	HFRCODPLL	HFRCODPLL is clocking up-counter
6	HFRCOEM23	HFRCOEM23 is clocking up-counter
9	FSRCO	FSRCO is clocking up-counter
10	LFRCO	LFRCO is clocking up-counter
11	ULFRCO	ULFRCO is clocking up-counter

Bit	Name	Reset	Access	Description
23	CONT	0x0	RW	**Continuous Calibration**
	Set this bit to enable continuous calibration. Changing this while calibration is running results in bus fault.			
22	WRAPUP	0x0	RW	**Wrap around Up-counter**
	Set this bit to wrap around the up-counter. By default, the up-counter is clamped at max value. Changing this while calibration is running results in bus fault.			
21:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

8.5.9 CMU_CALCNT - Calibration Result Counter Register

Offset	Bit Position																													
0x058	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset									0x0																					
Access									R																					
Name									CALCNT																					

Bit	Name	Reset	Access	Description
31:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:0	CALCNT	0x0	R	**Calibration Result Counter Value**
	Read calibration result when Calibration Ready flag has been set.			

8.5.10 CMU_CALTOP - Calibration Top Value Register

Offset	Bit Position																													
0x05C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset									0x0																					
Access									RW																					
Name									CALTOP																					

Bit	Name	Reset	Access	Description
31:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:0	CALTOP	0x0	RW	**Calibration Counter Top Value**
	Write top value before calibration. Changing this while calibration is running results in bus fault.			

8.5.11 CMU_CLKEN0 - Clock Enable Register 0

Offset	Bit Position																															
0x064	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name	DCDC	SYSRTC0	BURTC	BURAM	PRS	GPIO	LESENSE	ULFRCO	LFXO	LFRCO	FSRCO	HFXO0	HFRCOEM23	HFRCO0	DPLL0	SYSCFG	I2C1	I2C0	WDOG0	LETIMER0	AMUXCP0	IADC0	TIMER5	TIMER4	TIMER3	TIMER2	TIMER1	TIMER0	GPCRC	RADIOAES	LDMAXBAR	LDMA

Bit	Name	Reset	Access	Description
31	DCDC	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
30	SYSRTC0	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
29	BURTC	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
28	BURAM	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
27	PRS	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
26	GPIO	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
25	LESENSE	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
24	ULFRCO	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
23	LFXO	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
22	LFRCO	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
21	FSRCO	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
20	HFXO0	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
19	HFRCOEM23	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
18	HFRCO0	0x0	RW	**Enable Bus Clock**

Bit	Name	Reset	Access	Description
	Enables HFRCODPLL/HFRCO0 module PCLK/HCLK			
17	DPLL0	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
16	SYSCFG	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
15	I2C1	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
14	I2C0	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
13	WDOG0	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
12	LETIMER0	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
11	AMUXCP0	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
10	IADC0	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
9	TIMER5	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
8	TIMER4	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
7	TIMER3	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
6	TIMER2	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
5	TIMER1	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
4	TIMER0	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
3	GPCRC	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
2	RADIOAES	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
1	LDMAXBAR	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
0	LDMA	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			

8.5.12 CMU_CLKEN1 - Clock Enable Register 1

Offset	Bit Position																															
0x068	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0	0x0	0x0	0x0			0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0								
Access	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW								
Name	USB	TIMER7	TIMER6	ETAMPDET	DMEM			EUSART2	EUSART1	EUSART0	PCNT0	VDAC0	ACMP1	ACMP0	WDOG1	MSC	ICACHE0	SMU	EUSART4	EUSART3	BUFC	SEMAILBOXHOST	RFFPLL0	HOSTMAILBOX								

Bit	Name	Reset	Access	Description
31	USB	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
30	TIMER7	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
29	TIMER6	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
28	ETAMPDET	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
27	DMEM	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
26:25	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
24	EUSART2	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
23	EUSART1	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
22	EUSART0	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
21	PCNT0	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
20	VDAC0	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
19	ACMP1	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
18	ACMP0	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
17	WDOG1	0x0	RW	**Enable Bus Clock**

Bit	Name	Reset	Access	Description
	Enables module PCLK/HCLK			
16	MSC	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
15	ICACHE0	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
14	SMU	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
13	EUSART4	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
12	EUSART3	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
11	BUFC	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
10	SEMAILBOXHOST	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
9	RFFPLL0	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
8	HOSTMAILBOX	0x0	RW	**Enable Bus Clock**
	Enables module PCLK/HCLK			
7:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

8.5.13 CMU_SYSCLKCTRL - System Clock Control

Offset	Bit Position																															
0x070	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0					0x0									0x1	
Access																	RW					RW									RW	
Name																	HCLKPRESC					PCLKPRESC									CLKSEL	

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:12	HCLKPRESC	0x0	RW	**HCLK Prescaler**

Specifies the clock divider for HCLK

Value	Mode	Description
0	DIV1	HCLK is SYSCLK divided by 1
1	DIV2	HCLK is SYSCLK divided by 2
3	DIV4	HCLK is SYSCLK divided by 4
7	DIV8	HCLK is SYSCLK divided by 8
15	DIV16	HCLK is SYSCLK divided by 16

Bit	Name	Reset	Access	Description
11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10	PCLKPRESC	0x0	RW	**PCLK Prescaler**

Specifies the clock divider for PCLK

Value	Mode	Description
0	DIV1	PCLK is HCLK divided by 1
1	DIV2	PCLK is HCLK divided by 2

Bit	Name	Reset	Access	Description
9:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2:0	CLKSEL	0x1	RW	**Clock Select**

Selects the clock source for SYSCLK.

Value	Mode	Description
1	FSRCO	FSRCO is clocking SYSCLK
2	HFRCODPLL	HFRCODPLL is clocking SYSCLK
3	HFXO	HFXO is clocking SYSCLK
4	CLKIN0	CLKIN0 is clocking SYSCLK
5	RFFPLL0SYS	RFFPLL0SYS is clocking SYSCLK

8.5.14 CMU_TRACECLKCTRL - Debug Trace Clock Control

Offset	Bit Position																													
0x080	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0				0x1	
Access																											RW				RW	
Name																											PRESC				CLKSEL	

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:4	PRESC	0x0	RW	**TRACECLK Prescaler**

Clock prescaler for debug trace logic. Changing this while HOSTCPU TRCENA is set results in bus fault.

Value	Mode	Description
0	DIV1	TRACECLK is SYSCLK divided by 1
1	DIV2	TRACECLK is SYSCLK divided by 2
2	DIV3	TRACECLK is SYSCLK divided by 3
3	DIV4	TRACECLK is SYSCLK divided by 4

Bit	Name	Reset	Access	Description
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	CLKSEL	0x1	RW	**Clock Select**

Selects clock source for for debug trace logic. Changing this while HOSTCPU TRCENA is set results in bus fault.

Value	Mode	Description
0	DISABLE	TRACE clock is disable
1	SYSCLK	SYSCLK is driving TRACE
2	HFRCOEM23	HFRCOEM23 is driving TRACE
3	HFRCODPLLRT	HFRCODPLLRT is driving TRACE

8.5.15 CMU_EXPORTCLKCTRL - Export Clock Control

Offset	Bit Position																													
0x090	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset				0x0									0x0								0x0								0x0			
Access				RW									RW								RW								RW			
Name				PRESC									CLKOUTSEL2								CLKOUTSEL1								CLKOUTSEL0			

Bit	Name	Reset	Access	Description
31:29	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
28:24	PRESC	0x0	RW	**EXPORTCLK Prescaler**
	Specifies the clock divider for EXPORTCLK (relative to SYSCLK).			
23:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	CLKOUTSEL2	0x0	RW	**Clock Output Select 2**
	Controls the clock output 2 multiplexer.			

Value	Mode	Description
0	DISABLED	CLKOUT2 is not clocked
1	HCLK	HCLK is clocking CLKOUT2
2	HFEXPCLK	EXPORTCLK is clocking CLKOUT2
3	ULFRCO	ULFRCO is clocking CLKOUT2
4	LFRCO	LFRCO is clocking CLKOUT2
5	LFXO	LFXO is clocking CLKOUT2
6	HFRCODPLL	HFRCODPLL is clocking CLKOUT2
7	HFXO	HFXO is clocking CLKOUT2
8	FSRCO	FSRCO is clocking CLKOUT2
9	HFRCOEM23	HFRCOEM23 is clocking CLKOUT2

15:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:8	CLKOUTSEL1	0x0	RW	**Clock Output Select 1**
	Controls the clock output 1 multiplexer.			

Value	Mode	Description
0	DISABLED	CLKOUT1 is not clocked
1	HCLK	HCLK is clocking CLKOUT1
2	HFEXPCLK	EXPORTCLK is clocking CLKOUT1

Bit	Name	Reset	Access	Description
	3	ULFRCO		ULFRCO is clocking CLKOUT1
	4	LFRCO		LFRCO is clocking CLKOUT1
	5	LFXO		LFXO is clocking CLKOUT1
	6	HFRCODPLL		HFRCODPLL is clocking CLKOUT1
	7	HFXO		HFXO is clocking CLKOUT1
	8	FSRCO		FSRCO is clocking CLKOUT1
	9	HFRCOEM23		HFRCOEM23 is clocking CLKOUT1
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	CLKOUTSEL0	0x0	RW	**Clock Output Select 0**

Controls the clock output 0 multiplexer.

Value	Mode	Description
0	DISABLED	CLKOUT0 is not clocked
1	HCLK	HCLK is clocking CLKOUT0
2	HFEXPCLK	EXPORTCLK is clocking CLKOUT0
3	ULFRCO	ULFRCO is clocking CLKOUT0
4	LFRCO	LFRCO is clocking CLKOUT0
5	LFXO	LFXO is clocking CLKOUT0
6	HFRCODPLL	HFRCODPLL is clocking CLKOUT0
7	HFXO	HFXO is clocking CLKOUT0
8	FSRCO	FSRCO is clocking CLKOUT0
9	HFRCOEM23	HFRCOEM23 is clocking CLKOUT0

8.5.16 CMU_DPLLREFCLKCTRL - Digital PLL Reference Clock Control

Offset	Bit Position																													
0x100	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	
Access																															RW	
Name																															CLKSEL	

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	CLKSEL	0x0	RW	**Clock Select**

Selects the clock source for DPLL reference. Changing this while DPLL is enabled results in bus fault.

Value	Mode	Description
0	DISABLED	DPLLREFCLK is not clocked
1	HFXO	HFXO is clocking DPLLREFCLK
2	LFXO	LFXO is clocking DPLLREFCLK
3	CLKIN0	CLKIN0 is clocking DPLLREFCLK

8.5.17 CMU_EM01GRPACLKCTRL - EM01 Peripheral Group a Clock Control

Offset	Bit Position																													
0x120	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x1		
Access																														RW		
Name																														CLKSEL		

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2:0	CLKSEL	0x1	RW	**Clock Select**

Selects the clock source for EM01 Group A Clock.

Value	Mode	Description
1	HFRCODPLL	HFRCODPLL is clocking EM01GRPACLK
2	HFXO	HFXO is clocking EM01GRPACLK
3	FSRCO	FSRCO is clocking EM01GRPACLK
4	HFRCOEM23	HFRCOEM23 is clocking EM01GRPACLK
5	HFRCODPLLRT	HFRCODPLL (retimed) is clocking EM01GRPACLK. Check with datasheet for frequency limitation when using retiming with voltage scaling.
6	HFXORT	HFXO (retimed) is clocking EM01GRPACLK. Check with datasheet for frequency limitation when using retiming with voltage scaling.

8.5.18 CMU_EM01GRPCCLKCTRL - EM01 Peripheral Group C Clock Control

Offset	Bit Position																													
0x128	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x1		
Access																														RW		
Name																														CLKSEL		

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2:0	CLKSEL	0x1	RW	**Clock Select**

Selects the clock source for EM01 Group C Clock.

Value	Mode	Description
1	HFRCODPLL	HFRCODPLL is clocking EM01GRPCCLK
2	HFXO	HFXO is clocking EM01GRPCCLK
3	FSRCO	FSRCO is clocking EM01GRPCCLK
4	HFRCOEM23	HFRCOEM23 is clocking EM01GRPCCLK
5	HFRCODPLLRT	HFRCODPLL (retimed) is clocking EM01GRPCCLK. Check with datasheet for frequency limitation when using retiming with voltage scaling.
6	HFXORT	HFXO (retimed) is clocking EM01GRPCCLK. Check with datasheet for frequency limitation when using retiming with voltage scaling.

8.5.19 CMU_EM23GRPACLKCTRL - EM23 Peripheral Group a Clock Control

Offset	Bit Position																													
0x140	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x1	
Access																															RW	
Name																															CLKSEL	

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	CLKSEL	0x1	RW	**Clock Select**

Selects the clock source for EM23 Group A Clock.

Value	Mode	Description
1	LFRCO	LFRCO is clocking EM23GRPACLK
2	LFXO	LFXO is clocking EM23GRPACLK
3	ULFRCO	ULFRCO is clocking EM23GRPACLK

8.5.20 CMU_EM4GRPACLKCTRL - EM4 Peripheral Group a Clock Control

Offset	Bit Position																													
0x160	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x1	
Access																															RW	
Name																															CLKSEL	

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	CLKSEL	0x1	RW	**Clock Select**

Selects the clock source for EM4 Group A Clock.

Value	Mode	Description
1	LFRCO	LFRCO is clocking EM4GRPACLK
2	LFXO	LFXO is clocking EM4GRPACLK
3	ULFRCO	ULFRCO is clocking EM4GRPACLK

8.5.21 CMU_IADCCLKCTRL - IADC Clock Control

Offset	Bit Position																													
0x180	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x1	
Access																															RW	
Name																															CLKSEL	

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	CLKSEL	0x1	RW	**Clock Select**

Selects the clock source for for IADC. EM01GRPACLK should never be selected as clock source for IADC when disabling the EM01GRACLK (e.g. because of EM23 entry).

Value	Mode	Description
1	EM01GRPACLK	EM01GRPACLK is clocking IADCCLK
2	FSRCO	FSRCO is clocking IADCCLK
3	HFRCOEM23	HFRCOEM23 is clocking IADCCLK

8.5.22 CMU_WDOG0CLKCTRL - Watchdog0 Clock Control

Offset	Bit Position																													
0x200	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x1	
Access																															RW	
Name																															CLKSEL	

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2:0	CLKSEL	0x1	RW	**Clock Select**

Selects the clock source for WDOG0.

Value	Mode	Description
1	LFRCO	LFRCO is clocking WDOG0CLK
2	LFXO	LFXO is clocking WDOG0CLK
3	ULFRCO	ULFRCO is clocking WDOG0CLK
4	HCLKDIV1024	HCLKDIV1024 is clocking WDOG0CLK

8.5.23 CMU_WDOG1CLKCTRL - Watchdog1 Clock Control

Offset	Bit Position																													
0x208	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x1		
Access																														RW		
Name																														CLKSEL		

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2:0	CLKSEL	0x1	RW	**Clock Select**

Selects the clock source for WDOG1.

Value	Mode	Description
1	LFRCO	LFRCO is clocking WDOG0CLK
2	LFXO	LFXO is clocking WDOG0CLK
3	ULFRCO	ULFRCO is clocking WDOG0CLK
4	HCLKDIV1024	HCLKDIV1024 is clocking WDOG0CLK

8.5.24 CMU_EUSART0CLKCTRL - EUSART0 Clock Control

Offset	Bit Position																														
0x220	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x1		
Access																														RW		
Name																														CLKSEL		

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2:0	CLKSEL	0x1	RW	**Clock Select**

This bit controls which clock is used for EUSART0. EM01GRPCCLK should never be selected as clock source when disabling the EM01GRCCLK (e.g. because of EM23 entry).

Value	Mode	Description
0	DISABLED	EUSART0 is not clocked
1	EM01GRPCCLK	EM01GRPCCLK is clocking EUSART0
2	HFRCOEM23	HFRCOEM23 is clocking EUSART0
3	LFRCO	LFRCO is clocking EUSART0
4	LFXO	LFXO is clocking EUSART0

8.5.25 CMU_SYSRTC0CLKCTRL - System RTC0 Clock Control

Offset	Bit Position																													
0x240	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x1	
Access																															RW	
Name																															CLKSEL	

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	CLKSEL	0x1	RW	**Clock Select**

Selects the clock source for SYSRTC0.

Value	Mode	Description
1	LFRCO	LFRCO is clocking SYSRTC0CLK
2	LFXO	LFXO is clocking SYSRTC0CLK
3	ULFRCO	ULFRCO is clocking SYSRTC0CLK

8.5.26 CMU_VDAC0CLKCTRL - VDAC0 Clock Control

Offset	Bit Position																													
0x260	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x1		
Access																														RW		
Name																														CLKSEL		

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2:0	CLKSEL	0x1	RW	**Clock Select**

This bit controls which clock is used for VDAC. EM01GRPACLK should never be selected as clock source when disabling the EM01GRACLK (e.g. because of EM23 entry).

Value	Mode	Description
0	DISABLED	VDAC is not clocked
1	EM01GRPACLK	EM01GRPACLK is clocking VDAC
2	EM23GRPACLK	EM23GRPACLK is clocking VDAC
3	FSRCO	FSRCO is clocking VDAC
4	HFRCOEM23	HFRCOEM23 is clocking VDAC

8.5.27 CMU_PCNT0CLKCTRL - Pulse Counter 0 Clock Control

Offset	Bit Position																													
0x270	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x1	
Access																															RW	
Name																															CLKSEL	

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	CLKSEL	0x1	RW	**Clock Select**

This bit controls which clock is used for PCNT0.

Value	Mode	Description
0	DISABLED	PCNT0 is not clocked
1	EM23GRPACLK	EM23GRPACLK is clocking PCNT0
2	PCNTS0	External pin PCNT_S0 is clocking PCNT0

8.5.28 CMU_RADIOCLKCTRL - Radio Clock Control

Offset	Bit Position																													
0x280	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																						0x1									0x0
Access	RW																						RW									RW
Name	DBGCLK																						CLKSEL									EN

Bit	Name	Reset	Access	Description
31	DBGCLK	0x0	RW	**Enable Clock for Debugger**
	When set to 1, this forces radio busmatrix and RAC clocks to run, allowing RAC sequencer debugger to stay attached.			
30:11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10:8	CLKSEL	0x1	RW	**Clock Select**
	Selects the clock source for radio sub-system			

Value	Mode	Description
1	FSRCO	FSRCO is clocking RADIOCLK
2	RFFPLL0RADIO	RFFPLL0RADIO is clocking RADIOCLK
3	HFXO	HFXO is clocking RADIOCLK

7:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	EN	0x0	RW	**Enable**
	Enables radio bridge clock			

8.5.29 CMU_DAPCLKCTRL - DAP Clock Control

Offset	Bit Position																													
0x284	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x1	
Access																															RW	
Name																															CLKSEL	

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	CLKSEL	0x1	RW	**Clock Select**

This bit is used to control which clock is for DAP

Value	Mode	Description
0	DISABLED	DAP is not clocked
1	FSRCO	FSRCO is clocking DAP
2	HFRCODPLL	HFRCODPLL is clocking DAP

8.5.30 CMU_LESENSEHFCLKCTRL - LESENSE HF Clock Control

Offset	Bit Position																													
0x290	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x1	
Access																															RW	
Name																															CLKSEL	

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	CLKSEL	0x1	RW	**Clock Select**

Selects the clock source for LESENSE high frequency logic.

Value	Mode	Description
1	FSRCO	FSRCO is clocking LESENSEHFCLK
2	HFRCOEM23	HFRCOEM23 is clocking LESENSEHFCLK

8.5.31 CMU_USB0CLKCTRL - USB0 Clock Control

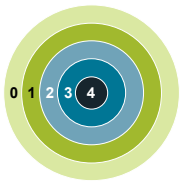
Offset	Bit Position																													
0x2A0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x1	
Access																															RW	
Name																															CLKSEL	

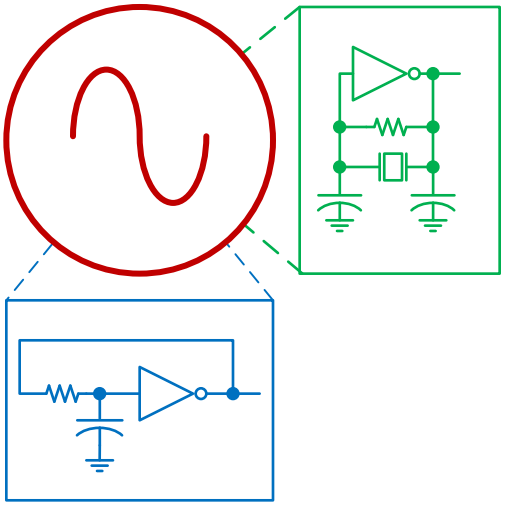
Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	CLKSEL	0x1	RW	**Clock Select**

Selects the clock source for USB0 logic.

Value	Mode	Description
1	USBPLL0	USBPLL0 is clocking USB0CLK
2	LFXO	LFXO is clocking USB0CLK
3	LFRCO	LFRCO is clocking USB0CLK

9. Oscillators





Quick Facts

What?

The EFR32xG25 has a wide range of high frequency and low frequency oscillators.

Why?

The High Frequency oscillators support EM0/1 operation. The Low-frequency oscillators provide a low frequency clock for the low energy peripherals in EM/2/3/4.

How?

The HFXO supports high frequency crystal oscillators. The LFXO supports 32.768 kHz crystal oscillators. The RC oscillators are internal oscillators that require no external components.

9.1 Introduction

The EFR32xG25 has several oscillators. This chapter contains a detailed function description and register descriptions for each oscillator. The CMU chapter includes information on how to select clock sources. Each oscillator may require some initial configuration or calibration before being enabled. The CMU supports clock on demand and can enable and disable oscillators. Therefore, it is important to properly configure each oscillator before selecting it as a clock source in the CMU.

9.2 HFXO - High Frequency Crystal Oscillator

9.2.1 Introduction

The High Frequency Crystal Oscillator (HFXO) uses an external high frequency crystal and provides a sequencer for starting up the crystal safely and reliably, while minimize energy consumption. An external sine wave clock source can also be used in the absence of a crystal.

9.2.2 Features

- Optimized for 39 MHz crystals
- Multiple programming options of start-up parameters to enable optimization of different crystals, supporting a wide range of ESR and ESL
- Support for external sine wave input
- Programmable two-phase start-up to minimize energy consumption
- Built-in current optimization (Automatic oscillation amplitude control)
- Independent on-chip frequency tuning capacitors
- Hardware request for on-demand enable/disable
- Dedicated high-quality clock output
- Register lock

9.2.3 Functional Description

9.2.3.1 Enabling and Disabling

While the HFXO supports on-demand clocking, it is generally recommended to manually manage the HFXO, at least initially, because it requires software configuration and has a long start-up time. Software can set the FORCEEN to start HFXO and keep it enabled even if it is not selected as a clock source.

However, once started and before EM2 entry, switching the HFXO to on-demand mode may be desirable. This allows the MCU to enter EM2 and then restart the HFXO automatically upon EM2 exit. (During EM1P the HFXO can be conditionally started, depending on the wake-up trigger source.)

The HFXO can be enabled and disabled via both hardware and software mechanisms. Enabling via software is done by setting the FORCEEN bit in the HFXO_CTRL register. Disabling via software is done by setting the DISONDEMAND bit and clearing FORCEEN bit in the HFXO_CTRL register. The hardware controlled on-demand mode is enabled by clearing the FORCEEN and DISONDEMAND bits in the HFXO_CTRL register. Once configured the on-demand mode hardware can autonomously start and stop the HFXO based on various peripheral clock requests in combination with clock switch selections in the CMU. The HFXO is automatically stopped when entering EM2, EM3, or EM4. Hardware can also stop the HFXO via hardware in response to change in peripheral requests and clock switch selections in the CMU.

9.2.3.2 Start-up Time

The start-up time differs for different crystals and the HFXO has a configurable time-out to accommodate each crystal type. Software configures the timeout by setting the various TIMEOUT bit fields of the HFXO_XTALCFG register. The time-out delays the assertion of the RDY signal for HFXO. The programmed timeout should allow enough time for the oscillator to stabilize. The time-out can be optimized for the chosen crystal used in the application.

The start-up behavior of the HFXO also depends on how and how long the HFXO is disabled.

9.2.3.3 Configuration

The High Frequency Crystal Oscillator needs to be configured to ensure safe start-up for the given crystal. Refer to the Device Data sheet and application notes for guidelines in selecting correct components and crystals as well as for configuration trade-offs.

The HFXO crystal is connected to the HFXTAL_I/HFXTAL_O pins as shown in Figure 9.1 HFXO Pin Connection on page 208.

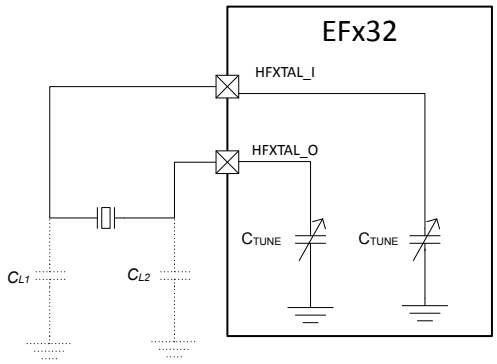


Figure 9.1. HFXO Pin Connection

Upon enabling the HFXO, a hardware state machine sequentially applies the configurable start-up state, intermediate start-up state, and steady state control settings from the HFXO_XTALCFG and HFXO_XTALCTRL registers. After reaching the steady operation state of the HFXO, it is recommended to further optimize current consumption using the Core Bias Optimization Algorithm to trade off noise and current consumption.

Refer to AN0016.2 for more information on settings for different crystals. Write the configuration values, which depends on the crystal's CL, RESR and oscillation frequency, into HFXO_XTALCFG and HFXO_XTALCTRL registers.

- COREBIASSTARTUP (HFXO_XTALCFG) - current setting applied at start-up time
- COREBIASSTARTUPI (HFXO_XTALCFG) - current setting applied at intermediate start-up time
- COREBIASANA (HFXO_XTALCTRL) - current setting applied at steady state
- CTUNEXISTARTUP (HFXO_XTALCFG) - tuning cap setting for XI applied at start-up time
- CTUNEXIANA (HFXO_XTALCTRL) - tuning cap setting for XI applied at steady state
- CTUNEXOSTARTUP (HFXO_XTALCFG) - tuning cap setting for XO applied at start-up time
- CTUNEXOANA (HFXO_XTALCTRL) - tuning cap setting for XO applied at steady state
- CTUNEFIXANA (HFXO_XTALCTRL) - fixed tuning cap setting applied throughout
- TIMEOUTSTEADY (HFXO_XTALCFG) - duration for the steady state settling time
- TIMEOUTCBLSB (HFXO_XTALCFG) - duration for the optimization settling after each step

All HFXO configuration needs to be performed prior to enabling the HFXO, whether via software by setting FORCEEN bit field, or allowing hardware request by clearing DISONDEMAND bit field in the HFXO_CTRL register.

By default, the HFXO is started in crystal mode, but it is possible to connect an active external sine or clipped sine wave clock source to the HFXTAL_I pin of the HFXO. By configuring the MODE field in HFXO_CFG to EXTCLK, the HFXO can be bypassed and the source clock can be provided through the HFXTAL_I pin.

9.2.3.4 Status Flags

The ENS flag in the HFXO_STATUS indicates if the HFXO has been successfully enabled. Once the HFXO oscillation amplitude has exceeded the start-up threshold and intermediate start-up threshold, the steady state settling timeout begins. When the steady state timeout has expired, the HFXO is ready for use as indicated by the RDY flag in the HFXO_STATUS. Once Core Bias Optimization is enabled, the COREBIASOPTRDY flag in the CMU_STATUS register indicates when the optimization is ready. It is advised to wait for this flag before using the HFXO, because optimization can cause minor disturbance to the oscillator frequency.

9.2.3.5 On-Demand Clocking

Software can request to enable the HFXO by setting the HFXO_CTRL.FORCEEN bit field. The HFXO can also optionally be configured via the HFXO_CTRL.DISONDEMAND to shut down when no hardware request is present. This is known as on-demand clocking and allows the oscillator to be controlled without any software intervention. On-demand HFXO enable can be used, for example, upon wake-up of the Radio Controller (RAC). The RAC module always requires the HFXO for its operation. Any hardware request for HFXO, including request from RAC, is indicated in the HWREQ bit field of the HFXO_STATUS register. This request enables the HFXO, provided that DISONDEMAND bit field is cleared in HFXO_CTRL register. The HFXO is only disabled by hardware upon EM2, EM3 or EM4 entry.

A typical use scenario of the on-demand feature is as follows. Set up the SYSRTC to periodically generate a compare match. Setup a PRS channel which uses this SYSRTC compare match as its source to cause a wake-up into EM1. Setup the RAC to use the PRS channel as its source for TXEN or RXEN. Now, when the EFR32 is in EM2 and the SYSRTC generates a compare match, a wake-up into EM1 occurs, and the HFXO will automatically start. When HFXO is ready, the RAC performs its work and triggers a transition back into EM2 when finished. The system starts, uses, and stops the HFXO without ever being in EM0.

The HFXO analog circuitry can optionally continue operating with the clock output shut off when the HFXO is disabled. This is configured by setting the KEEPWARM bit in HFXO_STATUS.

9.2.3.6 Interrupts

RDYIF and COREBIASOPTRDYIF are interrupt flags as well as status flags. This allows software flexibility to implement interrupt service routine or polling loop for these events. When steady state timeout has exceeded, sticky RDYIF is set until it is cleared by software. If optimization is enabled, sticky COREBIASOPTRDYIF is set when optimization is completed successfully. However, if optimization fails to complete, sticky COREBIASOPTERRIF is set, and the HFXO control state machine stays in the error state until the oscillator is disabled. Similarly, if HFXO fails to start-up, meaning it has not reached the steady state, sticky DNSERRIF is set. The HFXO control state machine stays in the error state until the oscillator is disabled.

9.2.3.7 Protection

It is possible to lock the control registers, configuration registers, and command register to prevent unintended software writes to critical clock settings. This is controlled by the HFXO_LOCK register. A LOCK bit is available in HFXO_STATUS register. Furthermore, these registers are locked automatically by hardware to prevent clock domain crossing malfunction. To gain access to these registers while oscillator is in steady operation state, set FORCEEN to 1, then set DISONDEMAND to 1 in the HFXO_CTRL register. A FSMLOCK bit in HFXO_STATUS register indicates when it is safe for software to update control registers and configuration registers. When software is finished with updates, put the oscillator back to on-demand mode by clearing DISONDEMAND to 0, followed by clearing FORCEEN to 0 in the HFXO_CTRL register. While DISONDEMAND is 0, FSMLOCK is always set, even if hardware is not requesting. This is to prevent a race condition between software access and hardware lock.

9.2.3.8 Tuning

While the oscillator is running in steady operation state, it may be desirable to change control settings. One example is frequency tuning by modifying the tuning capacitance via CTUNEXIANA and CTUNEXOANA fields in the HFXO_XTALCTRL register. When tuning, care should be taken to make small changes to the CTUNE registers. Ideally, change the CTUNE registers by one LSB at a time and alternate between the XI and XO registers. Sufficient wait time for settling, on the order of TIMEOUTSTEADY, should pass before new frequency measurement is taken.

Note: While the HFXO can support crystals with a tuning range of 38 MHz to 40 MHz, the radio specifically requires a 39 MHz crystal. There may also be specific crystal tolerance requirements for each RF protocol supported by the radio.

9.2.3.9 High Frequency Clock Output (HFCLKOUT)

Certain device package options include a dedicated HFCLKOUT pin. This signal is designed to be a very high quality sinusoidal clock output operating at the crystal frequency. It is suitable for driving the crystal input on other Silicon Labs EFR products, and enables multi-radio systems operating from a single crystal. When using the HFCLKOUT feature, there are additional controls and considerations.

Enabling and Disabling

The HFCLKOUT feature can be enabled and disabled through software or hardware. To enable the output buffer in software the FORCEENBUFOUT bit in HFXO_CTRL should be set to 1. To disable, the DISONDEMANDBUFOUT bit should be set to 1 and FORCEENBUFOUT cleared to 0 in HFXO_CTRL.

Hardware (on-demand) control is possible as well. The on-demand hardware mechanism uses a GPIO input (HFXO0.BUFOUT_REQ_IN_ASYNC, routed to PA or PB pin in the GPIO interface) to allow the other radio device to request the oscillator output. The external device requests HFCLKOUT by setting the input high. If the HFXO is not already running when external hardware requests HFCLKOUT, the HFXO will automatically be enabled and stabilized before the HFCLKOUT buffer turns on. When the external hardware enable request becomes inactive (input logic low), the HFXO block may also be automatically shut down to save energy if no other HFXO requestors are active.

Hardware control is enabled by clearing both the FORCEENBUFOUT and DISONDEMANDBUFOUT bits in the HFXO_CTRL register.

Note: Under hardware control, HFCLKOUT is available in EM0, EM1, EM2 and EM3 and will be automatically shut down in EM4.

Tuning

If the HFCLKOUT feature is enabled, CTUNEXIBUFOUTANA should normally be set to CTUNEXIANA. This will guarantee a maximum capacitance change of ±300 fF between enabling/disabling HFCLKOUT (expected maximum frequency shift of ±10 ppm for a typical crystal). For a lower frequency shift, it is recommended to tune CTUNEXIBUFOUTANA at the target frequency while HFCLKOUT is enabled.

9.2.4 HFXO Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	HFXO_IPVERSION	R	IP Version ID
0x010	HFXO_XTALCFG	RW SYNC	Crystal Configuration Register
0x018	HFXO_XTALCTRL	RWH SYNC	Crystal Control Register
0x020	HFXO_CFG	RW SYNC	Configuration Register
0x028	HFXO_CTRL	RWH SYNC	Control Register
0x040	HFXO_BUFOUTTRIM	RW SYNC	BUFOUT Trim Configuration Register
0x044	HFXO_BUFOUTCTRL	RW SYNC	BUFOUT Control Register
0x050	HFXO_CMD	W SYNC	Command Register
0x058	HFXO_STATUS	RH	Status Register
0x070	HFXO_IF	RWH INTFLAG	Interrupt Flag Register
0x074	HFXO_IEN	RW	Interrupt Enable Register
0x080	HFXO_LOCK	W	Configuration Lock Register
0x1000	HFXO_IPVERSION_SET	R	IP Version ID
0x1010	HFXO_XTALCFG_SET	RW SYNC	Crystal Configuration Register
0x1018	HFXO_XTALCTRL_SET	RWH SYNC	Crystal Control Register
0x1020	HFXO_CFG_SET	RW SYNC	Configuration Register
0x1028	HFXO_CTRL_SET	RWH SYNC	Control Register
0x1040	HFXO_BUFOUTTRIM_SET	RW SYNC	BUFOUT Trim Configuration Register
0x1044	HFXO_BUFOUTCTRL_SET	RW SYNC	BUFOUT Control Register
0x1050	HFXO_CMD_SET	W SYNC	Command Register
0x1058	HFXO_STATUS_SET	RH	Status Register
0x1070	HFXO_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x1074	HFXO_IEN_SET	RW	Interrupt Enable Register
0x1080	HFXO_LOCK_SET	W	Configuration Lock Register
0x2000	HFXO_IPVERSION_CLR	R	IP Version ID
0x2010	HFXO_XTALCFG_CLR	RW SYNC	Crystal Configuration Register
0x2018	HFXO_XTALCTRL_CLR	RWH SYNC	Crystal Control Register
0x2020	HFXO_CFG_CLR	RW SYNC	Configuration Register
0x2028	HFXO_CTRL_CLR	RWH SYNC	Control Register
0x2040	HFXO_BUFOUTTRIM_CLR	RW SYNC	BUFOUT Trim Configuration Register
0x2044	HFXO_BUFOUTCTRL_CLR	RW SYNC	BUFOUT Control Register
0x2050	HFXO_CMD_CLR	W SYNC	Command Register
0x2058	HFXO_STATUS_CLR	RH	Status Register
0x2070	HFXO_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x2074	HFXO_IEN_CLR	RW	Interrupt Enable Register

Offset	Name	Type	Description
0x2080	HFXO_LOCK_CLR	W	Configuration Lock Register
0x3000	HFXO_IPVERSION_TGL	R	IP Version ID
0x3010	HFXO_XTALCFG_TGL	RW SYNC	Crystal Configuration Register
0x3018	HFXO_XTALCTRL_TGL	RWH SYNC	Crystal Control Register
0x3020	HFXO_CFG_TGL	RW SYNC	Configuration Register
0x3028	HFXO_CTRL_TGL	RWH SYNC	Control Register
0x3040	HFXO_BUFOUTTRIM_TGL	RW SYNC	BUFOUT Trim Configuration Register
0x3044	HFXO_BUFOUTCTRL_TGL	RW SYNC	BUFOUT Control Register
0x3050	HFXO_CMD_TGL	W SYNC	Command Register
0x3058	HFXO_STATUS_TGL	RH	Status Register
0x3070	HFXO_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x3074	HFXO_IEN_TGL	RW	Interrupt Enable Register
0x3080	HFXO_LOCK_TGL	W	Configuration Lock Register

9.2.5 HFXO Register Description

9.2.5.1 HFXO_IPVERSION - IP Version ID

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x4																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x4	R	**IP Version ID**
	The read only IPVERSION field gives the version for this module. There may be minor software changes required for modules with different values of IPVERSION.			

9.2.5.2 HFXO_XTALCFG - Crystal Configuration Register

Offset	Bit Position																											
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0xB				0xC				0x0				0x0				0x20						0x20					
Access					RW				RW				RW				RW				RW						RW					
Name					TIMEOUTCBLSB				TIMEOUTSTEADY				CTUNEXOSTARTUP				CTUNEXISTARTUP				COREBIASSTARTUP						COREBIASSTARTUPI					

Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27:24	TIMEOUTCBLSB	0xB	RW	**Core Bias LSB Change Timeout**

wait duration for the COREBIAS change to settle out, used at each step of COREBIAS optimization algorithm

Value	Mode	Description
0	T8US	The core bias LSB change timeout is set to 8 us minimum. The maximum can be +40%.
1	T20US	The core bias LSB change timeout is set to 20 us minimum. The maximum can be +40%.
2	T41US	The core bias LSB change timeout is set to 41 us minimum. The maximum can be +40%.
3	T62US	The core bias LSB change timeout is set to 62 us minimum. The maximum can be +40%.
4	T83US	The core bias LSB change timeout is set to 83 us minimum. The maximum can be +40%.
5	T104US	The core bias LSB change timeout is set to 104 us minimum. The maximum can be +40%.
6	T125US	The core bias LSB change timeout is set to 125 us minimum. The maximum can be +40%.
7	T166US	The core bias LSB change timeout is set to 166 us minimum. The maximum can be +40%.
8	T208US	The core bias LSB change timeout is set to 208 us minimum. The maximum can be +40%.
9	T250US	The core bias LSB change timeout is set to 250 us minimum. The maximum can be +40%.
10	T333US	The core bias LSB change timeout is set to 333 us minimum. The maximum can be +40%.
11	T416US	The core bias LSB change timeout is set to 416 us minimum. The maximum can be +40%.
12	T833US	The core bias LSB change timeout is set to 833 us minimum. The maximum can be +40%.

Bit	Name	Reset	Access	Description
	13	T1250US		The core bias LSB change timeout is set to 1250 us minimum. The maximum can be +40%.
	14	T2083US		The core bias LSB change timeout is set to 2083 us minimum. The maximum can be +40%.
	15	T3750US		The core bias LSB change timeout is set to 3750 us minimum. The maximum can be +40%.
23:20	TIMEOUTSTEADY	0xC	RW	**Steady State Timeout**
	wait duration for the steady state settings to settle out			
	Value	Mode		Description
	0	T4US		The steady state timeout is set to 4 us minimum. The maximum can be +40%.
	1	T16US		The steady state timeout is set to 16 us minimum. The maximum can be +40%.
	2	T41US		The steady state timeout is set to 41 us minimum. The maximum can be +40%.
	3	T83US		The steady state timeout is set to 83 us minimum. The maximum can be +40%.
	4	T125US		The steady state timeout is set to 125 us minimum. The maximum can be +40%.
	5	T166US		The steady state timeout is set to 166 us minimum. The maximum can be +40%.
	6	T208US		The steady state timeout is set to 208 us minimum. The maximum can be +40%.
	7	T250US		The steady state timeout is set to 250 us minimum. The maximum can be +40%.
	8	T333US		The steady state timeout is set to 333 us minimum. The maximum can be +40%.
	9	T416US		The steady state timeout is set to 416 us minimum. The maximum can be +40%.
	10	T500US		The steady state timeout is set to 500 us minimum. The maximum can be +40%.
	11	T666US		The steady state timeout is set to 666 us minimum. The maximum can be +40%.
	12	T833US		The steady state timeout is set to 833 us minimum. The maximum can be +40%.
	13	T1666US		The steady state timeout is set to 1666 us minimum. The maximum can be +40%.
	14	T2500US		The steady state timeout is set to 2500 us minimum. The maximum can be +40%.
	15	T4166US		The steady state timeout is set to 4166 us minimum. The maximum can be +40%.
19:16	CTUNEXOSTARTUP	0x0	RW	**Startup Tuning Capacitance on XO**
	4 most significant bits of CTUNEXOANA applied during startup phase			
15:12	CTUNEXISTARTUP	0x0	RW	**Startup Tuning Capacitance on XI**

Bit	Name	Reset	Access	Description
	4 most significant bits of CTUNEXIANA applied during startup phase			
11:6	COREBIASSTARTUP	0x20	RW	**Startup Core Bias Current**
	6 most significant bits of COREBIASANA applied during startup phase			
5:0	COREBIASSTARTUPI	0x20	RW	**Intermediate Startup Core Bias Current**
	6 most significant bits of COREBIASANA applied during intermediate startup phase			

9.2.5.3 HFXO_XTALCTRL - Crystal Control Register

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0				0x0		0x3		0x3C								0x3C								0x3C							
Access	RW				RW		RW		RW								RW								RW							
Name	SKIPCOREBIASOPT				COREDGENANA		CTUNEFIXANA		CTUNEXOANA								CTUNEXIANA								COREBIASANA							

Bit	Name	Reset	Access	Description
31	SKIPCOREBIASOPT	0x0	RW	**Skip Core Bias Optimization**
	Set to skip the core bias current optimization algorithm at next startup. Reuse the value stored in COREBIASANA. At the successful completion of core bias current optimization algorithm, hardware sets this bit to skip optimization during subsequent startup.			
30:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27:26	COREDGENANA	0x0	RW	**Core Degeneration**
	Core degeneration control			

Value	Mode	Description
0	NONE	Do not apply core degeneration resistence
1	DGEN33	Apply 33 ohm core degeneration resistence
2	DGEN50	Apply 50 ohm core degeneration resistence
3	DGEN100	Apply 100 ohm core degeneration resistence

Bit	Name	Reset	Access	Description
25:24	CTUNEFIXANA	0x3	RW	**Fixed Tuning Capacitance**
	Adds or removes fixed capacitance on XI or XO			

Value	Mode	Description
0	NONE	Remove fixed capacitance on XI and XO nodes
1	XI	Adds fixed capacitance on XI node
2	XO	Adds fixed capacitance on XO node
3	BOTH	Adds fixed capacitance on both XI and XO nodes

Bit	Name	Reset	Access	Description
23:16	CTUNEXOANA	0x3C	RW	**Tuning Capacitance on XO**
	Approximately 80fF per step. 0 is min. 255 is max.			
15:8	CTUNEXIANA	0x3C	RW	**Tuning Capacitance on XI**
	Approximately 80fF per step. 0 is min. 255 is max.			
7:0	COREBIASANA	0x3C	RW	**Core Bias Current**

Bit	Name	Reset	Access	Description
	Approximately 10uA per step			

9.2.5.4 HFXO_CFG - Configuration Register

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset				0x1																									0x0	0x0		0x0
Access				RW																									RW	RW		RW
Name				FORCELFTIMEOUT																									SQBUFSCHTRGANA	ENXIDCBIASANA		MODE

Bit	Name	Reset	Access	Description
31:29	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
28	FORCELFTIMEOUT	0x1	RW	**Force Low Frequency Timeout**
	For deterministic timeout, clear this bit and configure PRS to trigger based on 32kHz timer (e.g., RTC).			
27:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	SQBUFSCHTRGANA	0x0	RW	**Squaring Buffer Schmitt Trigger**
	Used in EXTCLK mode to prevent self oscillation			

Value	Mode	Description
0	DISABLE	Squaring buffer schmitt trigger is disabled
1	ENABLE	Squaring buffer schmitt trigger is enabled

2	ENXIDCBIASANA	0x0	RW	**Enable XI Internal DC Bias**
	Set to enable internal DC bias. Bit is ignored in XTAL mode.			
1:0	MODE	0x0	RW	**Crystal Oscillator Mode**
	Set this to configure the external source for the HFXO.			

Value	Mode	Description
0	XTAL	crystal oscillator
1	EXTCLK	external sinusoidal clock can be supplied on XI pin.
2	EXTCLKPKDET	external sinusoidal clock can be supplied on XI pin (peak detector used).

9.2.5.5 HFXO_CTRL - Control Register

Offset	Bit Position																													
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset						0x1	0x1	0x1						0x0	0x0	0x0	0x0				0x0					0x1	0x0	0x0	0x0	0x0		0x0
Access						RW	RW	RW						RW	RW	RW	RW				RW					RW	RW	RW	RW	RW		RW
Name						DISONDEMANDBUFOUT	DISONDEMANDPRS	DISONDEMAND						FORCEENBUFOUT	FORCEENPRS	FORCEEN	PRSSTATUSSEL1				PRSSTATUSSEL0					FORCECTUNEMAX	FORCEXO2GNDANA	FORCEXI2GNDANA	EM23ONDEMAND	KEEPWARM		BUFOUTFREEZE

Bit	Name	Reset	Access	Description
31:27	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
26	DISONDEMANDBUFOUT	0x1	RW	**Disable On-demand For BUFOUT**
	Disable On Demand for the BUFOUT request interface.			
25	DISONDEMANDPRS	0x1	RW	**Disable On-demand For PRS**
	Disable On Demand for the PRS request interface.			
24	DISONDEMAND	0x1	RW	**Disable On-demand For Digital Clock**
	Disable On Demand for the digital clock request interface.			
23:19	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
18	FORCEENBUFOUT	0x0	RW	**Force BUFOUT Request**
	Force BUFOUT request.			
17	FORCEENPRS	0x0	RW	**Force PRS Oscillator Request**
	Force PRS oscillator request.			
16	FORCEEN	0x0	RW	**Force Digital Clock Request**
	Force digital clock request.			
15:12	PRSSTATUSSEL1	0x0	RW	**PRS Status 1 Output Select**
	Mux select for various status signals to be output through PRS.			

Value	Mode	Description
0	DISABLED	PRS mux outputs 0
1	ENS	PRS mux outputs enabled status
2	COREBIASOPTRDY	PRS mux outputs core bias optimization ready status
3	RDY	PRS mux outputs ready status
4	PRSRDY	PRS mux outputs PRS ready status
5	BUFOUTRDY	PRS mux outputs BUFOUT ready status

Bit	Name	Reset	Access	Description
	8	HWREQ		PRS mux outputs oscillator requested by digital clock status
	9	PRSHWREQ		PRS mux outputs oscillator requested by PRS request status
	10	BUFOUTHWREQ		PRS mux outputs oscillator requested by BUFOUT request status
11:8	PRSSTATUSSEL0	0x0	RW	**PRS Status 0 Output Select**
	Mux select for various status signals to be output through PRS.			
	Value	Mode		Description
	0	DISABLED		PRS mux outputs 0
	1	ENS		PRS mux outputs enabled status
	2	COREBIASOPTRDY		PRS mux outputs core bias optimization ready status
	3	RDY		PRS mux outputs ready status
	4	PRSRDY		PRS mux outputs PRS ready status
	5	BUFOUTRDY		PRS mux outputs BUFOUT ready status
	8	HWREQ		PRS mux outputs oscillator requested by digital clock status
	9	PRSHWREQ		PRS mux outputs oscillator requested by PRS request status
	10	BUFOUTHWREQ		PRS mux outputs oscillator requested by BUFOUT request status
7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6	FORCECTUNEMAX	0x1	RW	**Force Tuning Cap to Max Value**
	When oscillator is disabled, force tuning capacitor to maximum value. Set this bit to 1 in XTAL mode to prevent overshoot upon disable.			
5	FORCEXO2GNDANA	0x0	RW	**Force XO Pin to Ground**
	Set to enable grounding of XO pin.			
	Value	Mode		Description
	0	DISABLE		Disabled (not pulled)
	1	ENABLE		Enabled (pulled)
4	FORCEXI2GNDANA	0x0	RW	**Force XI Pin to Ground**
	Set to enable grounding of XI pin. Do not enable if MODE=EXTCLK and an external source is supplied.			
	Value	Mode		Description
	0	DISABLE		Disabled (not pulled)
	1	ENABLE		Enabled (pulled)
3	EM23ONDEMAND	0x0	RW	**On-demand During EM23**
	Use this bit to prevent EM23 shutdown of the module's power domain upon EM23 entry. Set this bit to 1 if on-demand requests are supposed to be honored while in EM23.			
2	KEEPWARM	0x0	RW	**Keep Warm**

Bit	Name	Reset	Access	Description
	Upon disable, if this bit is set, analog oscillator will keep running, while clock output is shutoff. Clearing this bit has no effect until the next disable event.			
1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	BUFOUTFREEZE	0x0	RW	**Freeze BUFOUT Controls**
	Freeze BUFOUT Controls in current state (ON or OFF).			

9.2.5.6 HFXO_BUFOUTTRIM - BUFOUT Trim Configuration Register

Offset	Bit Position																															
0x040	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x8		
Access																													RW		
Name																													VTRTRIMANA		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	VTRTRIMANA	0x8	RW	**BUFOUT Reference Trim**
	Change this field to set bias levels between 200uA and 400uA. bias_current = VTRTCANA * VTRTRIMANA * scale_factor. The default setting corresponds to 200uA.			

9.2.5.7 HFXO_BUFOUTCTRL - BUFOUT Control Register

Offset	Bit Position																													
0x044	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0								0x6				0x4				0x3				0xC				0x1				0x5			
Access	RW								RW				RW				RW				RW				RW				RW			
Name	MINIMUMSTARTUPDELAY								TIMEOUTSTARTUP				TIMEOUTCTUNE				PEAKDETTHRESANA				XOUTGMANA				XOUTCFANA				XOUTBIASANA			

Bit	Name	Reset	Access	Description
31	MINIMUMSTARTUPDE-LAY	0x0	RW	**Minimum Startup Delay**
	If set, BUFOUT does not start until timeout expires. This prevents waste of power if BUFOUT is ready too early.			
30:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:20	TIMEOUTSTARTUP	0x6	RW	**Oscillator Startup Timeout**
	Wait duration for the typical oscillator startup sequence to prevent BUFOUT starting too early, used when MINIMUMSTARTUPDELAY is set.			

Value	Mode	Description
0	T42US	The oscillator startup timeout is set to 42 us minimum. The maximum can be +40%.
1	T83US	The oscillator startup timeout is set to 83 us minimum. The maximum can be +40%.
2	T108US	The oscillator startup timeout is set to 108 us minimum. The maximum can be +40%.
3	T133US	The oscillator startup timeout is set to 133 us minimum. The maximum can be +40%.
4	T158US	The oscillator startup timeout is set to 158 us minimum. The maximum can be +40%.
5	T183US	The oscillator startup timeout is set to 183 us minimum. The maximum can be +40%.
6	T208US	The oscillator startup timeout is set to 208 us minimum. The maximum can be +40%.
7	T233US	The oscillator startup timeout is set to 233 us minimum. The maximum can be +40%.
8	T258US	The oscillator startup timeout is set to 258 us minimum. The maximum can be +40%.
9	T283US	The oscillator startup timeout is set to 283 us minimum. The maximum can be +40%.

Bit	Name	Reset	Access	Description
	10	T333US		The oscillator startup timeout is set to 333 us minimum. The maximum can be +40%.
	11	T375US		The oscillator startup timeout is set to 375 us minimum. The maximum can be +40%.
	12	T417US		The oscillator startup timeout is set to 417 us minimum. The maximum can be +40%.
	13	T458US		The oscillator startup timeout is set to 458 us minimum. The maximum can be +40%.
	14	T500US		The oscillator startup timeout is set to 500 us minimum. The maximum can be +40%.
	15	T667US		The oscillator startup timeout is set to 667 us minimum. The maximum can be +40%.
19:16	TIMEOUTCTUNE	0x4	RW	**Tuning Cap Change Timeout**

Wait duration for the CTUNE change to settle out, used when CTUNE changes as result of enabling BUFOUT.

Value	Mode	Description
0	T2US	The tuning cap change timeout is set to 2 us minimum. The maximum can be +40%.
1	T5US	The tuning cap change timeout is set to 5 us minimum. The maximum can be +40%.
2	T10US	The tuning cap change timeout is set to 10 us minimum. The maximum can be +40%.
3	T16US	The tuning cap change timeout is set to 16 us minimum. The maximum can be +40%.
4	T21US	The tuning cap change timeout is set to 21 us minimum. The maximum can be +40%.
5	T26US	The tuning cap change timeout is set to 26 us minimum. The maximum can be +40%.
6	T31US	The tuning cap change timeout is set to 31 us minimum. The maximum can be +40%.
7	T42US	The tuning cap change timeout is set to 42 us minimum. The maximum can be +40%.
8	T52US	The tuning cap change timeout is set to 52 us minimum. The maximum can be +40%.
9	T63US	The tuning cap change timeout is set to 63 us minimum. The maximum can be +40%.
10	T83US	The tuning cap change timeout is set to 83 us minimum. The maximum can be +40%.
11	T104US	The tuning cap change timeout is set to 104 us minimum. The maximum can be +40%.
12	T208US	The tuning cap change timeout is set to 208 us minimum. The maximum can be +40%.
13	T313US	The tuning cap change timeout is set to 313 us minimum. The maximum can be +40%.
14	T521US	The tuning cap change timeout is set to 521 us minimum. The maximum can be +40%.

Bit	Name	Reset	Access	Description
	15	T938US		The tuning cap change timeout is set to 938 us minimum. The maximum can be +40%.
15:12	PEAKDETTHRESANA	0x3	RW	**Peak Detector Threshold for XOUT**
	Sets the peak detector threshold for BUFOUT. Approximately, settings map to voltage values as follows. 0=132mV, 1=161mV, 2=189mV, 3=217mV, 4=245mV, 5=272mV, 6=300mV, 7=327mV, 8=355mV, 9=382mV, 10=409mV, 11=436mV, 12=461mV, 13=486mV, 14=508mV, 15=530mV.			
11:8	XOUTGMANA	0xC	RW	
7:4	XOUTCFANA	0x1	RW	**Buffer Gain**
	Buffer gain.			
3:0	XOUTBIASANA	0x5	RW	**Driver Bias Current**
	Driver bias current.			

9.2.5.8 HFXO_CMD - Command Register

Offset	Bit Position																															
0x050	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																W(nB)
Name																																COREBIASOPT

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	COREBIASOPT	0x0	W(nB)	**Core Bias Optimizaton**
	Starts the core bias current optimization algorithm and runs it one time. Optimization should be executed if the temperature changes by more than 40degC. Do not run this command while the radio is in RX or TX modes. Do not issue this command more than once until COREBIASOPTRDY is asserted, or the previous command may be cancelled.			

9.2.5.9 HFXO_STATUS - Status Register

Offset	Bit Position																													
0x058	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0									0x0	0x0	0x0		0x0	0x0	0x0												0x0	0x0	0x0	0x0
Access	R	R									R	R	R		R	R	R												R	R	R	R
Name	LOCK	SYNCBUSY									BUFOUTHWREQ	PRSHWREQ	ISWARM		HWREQ	ENS	BUFOUTFROZEN												BUFOUTRDY	PRSRDY	COREBIASOPTRDY	RDY

Bit	Name	Reset	Access	Description
31	LOCK	0x0	R	**Configuration Lock Status**
	Indicates the current status of configuration lock.			

Value	Mode	Description
0	UNLOCKED	Configuration lock is unlocked
1	LOCKED	Configuration lock is locked

30	SYNCBUSY	0x0	R	**Sync Busy**
	Indicates synchronization is ongoing.			
29:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21	BUFOUTHWREQ	0x0	R	**Oscillator Requested by BUFOUT Request**
	Oscillator is requested by the BUFOUT oscillator request interface.			
20	PRSHWREQ	0x0	R	**Oscillator Requested by PRS Request**
	Oscillator is requested by the PRS oscillator request interface.			
19	ISWARM	0x0	R	**Oscillator Is Kept Warm**
	Oscillator is currently kept in warm state. Re-enable from warm state skips startup sequence.			
18	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
17	HWREQ	0x0	R	**Oscillator Requested by Digital Clock**
	Oscillator is requested by digital clock request interface.			
16	ENS	0x0	R	**Enabled Status**
	Oscillator is enabled.			
15	BUFOUTFROZEN	0x0	R	**BUFOUT Frozen**
	FSM is frozen with respect to starting BUFOUT enable or disable sequences.			
14:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	BUFOUTRDY	0x0	R	**BUFOUT Ready Status**
	The BUFOUT clock is ready.			

Bit	Name	Reset	Access	Description
2	PRSRDY	0x0	R	**PRS Ready Status**
	The PRS oscillator startup is ready.			
1	COREBIASOPTRDY	0x0	R	**Core Bias Optimization Ready**
	Core bias current optimization algorithm is complete.			
0	RDY	0x0	R	**Ready Status**
	The digital clock branch (osc.clk_qual) is ready.			

9.2.5.10 HFXO_IF - Interrupt Flag Register

Offset	Bit Position																													
0x070	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0	0x0	0x0	0x0						0x0	0x0					0x0												0x0	0x0	0x0	0x0
Access	RW	RW	RW	RW	RW						RW	RW					RW												RW	RW	RW	RW
Name	COREBIASOPTERR	LFTIMEOUTERR	DNSERR	BUFOUTDNSERR	BUFOUTFREEZEERR						BUFOUTERR	PRSERR					BUFOUTFROZEN												BUFOUTRDY	PRSRDY	COREBIASOPTRDY	RDY

Bit	Name	Reset	Access	Description
31	COREBIASOPTERR	0x0	RW	**Core Bias Optimization Error Interrupt**
	Core bias current optimization algorithm fails to complete.			
30	LFTIMEOUTERR	0x0	RW	**Low Frequency Timeout Error Interrupt**
	Low frequency timeout triggers before the steady state timeout triggers.			
29	DNSERR	0x0	RW	**Did Not Start Error Interrupt**
	Crystal oscillator fails to startup.			
28	BUFOUTDNSERR	0x0	RW	**BUFOUT Did Not Start Error Interrupt**
	BUFOUT fails to startup.			
27	BUFOUTFREEZEERR	0x0	RW	**BUFOUT Freeze Error Interrupt**
	BUFOUTFREEZE should not be set when HWREQ is low as this can prevent service to companion chip indefinitely.			
26:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21	BUFOUTERR	0x0	RW	**BUFOUT Request Error Interrupt**
	BUFOUT request is asserted while oscillator is forced to shutdown.			
20	PRSERR	0x0	RW	**PRS Requset Error Interrupt**
	PRS request is asserted while oscillator is forced to shutdown.			
19:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15	BUFOUTFROZEN	0x0	RW	**BUFOUT FROZEN Interrupt**
	FSM is frozen with respect to starting BUFOUT enable or disable sequences.			
14:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	BUFOUTRDY	0x0	RW	**BUFOUT Ready Interrupt**
	The BUFOUT clock is ready.			
2	PRSRDY	0x0	RW	**PRS Ready Interrupt**
	The PRS oscillator startup is ready.			
1	COREBIASOPTRDY	0x0	RW	**Core Bias Optimization Ready Interrupt**

Bit	Name	Reset	Access	Description
	Core bias current optimization algorithm is complete.			
0	RDY	0x0	RW	**Digital Clock Ready Interrupt**
	The digital clock branch (osc.clk_qual) is ready.			

9.2.5.11 HFXO_IEN - Interrupt Enable Register

Offset	Bit Position																													
0x074	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0	0x0	0x0	0x0						0x0	0x0					0x0												0x0	0x0	0x0	0x0
Access	RW	RW	RW	RW	RW						RW	RW					RW												RW	RW	RW	RW
Name	COREBIASOPTERR	LFTIMEOUTERR	DNSERR	BUFOUTDNSERR	BUFOUTFREEZEERR						BUFOUTERR	PRSERR					BUFOUTFROZEN												BUFOUTRDY	PRSRDY	COREBIASOPTRDY	RDY

Bit	Name	Reset	Access	Description
31	COREBIASOPTERR	0x0	RW	**Core Bias Optimization Error Interrupt**
	Core bias current optimization algorithm fails to complete.			
30	LFTIMEOUTERR	0x0	RW	**Low Frequency Timeout Error Interrupt**
	Low frequency timeout triggers before the steady state timeout triggers.			
29	DNSERR	0x0	RW	**Did Not Start Error Interrupt**
	Crystal oscillator fails to startup.			
28	BUFOUTDNSERR	0x0	RW	**BUFOUT Did Not Start Error Interrupt**
	BUFOUT fails to startup.			
27	BUFOUTFREEZEERR	0x0	RW	**BUFOUT Freeze Error Interrupt**
	BUFOUTFREEZE should not be set when HWREQ is low as this can prevent service to companion chip indefinitely.			
26:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21	BUFOUTERR	0x0	RW	**BUFOUT Request Error Interrupt**
	BUFOUT request is asserted while oscillator is forced to shutdown.			
20	PRSERR	0x0	RW	**PRS Requset Error Interrupt**
	PRS request is asserted while oscillator is forced to shutdown.			
19:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15	BUFOUTFROZEN	0x0	RW	**BUFOUT FROZEN Interrupt**
	FSM is frozen with respect to starting BUFOUT enable or disable sequences.			
14:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	BUFOUTRDY	0x0	RW	**BUFOUT Ready Interrupt**
	The BUFOUT clock is ready.			
2	PRSRDY	0x0	RW	**PRS Ready Interrupt**
	The PRS oscillator startup is ready.			
1	COREBIASOPTRDY	0x0	RW	**Core Bias Optimization Ready Interrupt**

Bit	Name	Reset	Access	Description
	Core bias current optimization algorithm is complete.			
0	RDY	0x0	RW	**Digital Clock Ready Interrupt**
	The digital clock branch (osc.clk_qual) is ready.			

9.2.5.12 HFXO_LOCK - Configuration Lock Register

Offset	Bit Position																													
0x080	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x580E															
Access																	W															
Name																	LOCKKEY															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LOCKKEY	0x580E	W	**Configuration Lock Key**
	Write any other value than the unlock code to lock registers from editing. Write the unlock code to unlock.			

Value	Mode	Description
22542	UNLOCK	Write this value to unlock

9.3 HFRCO - High-Frequency RC Oscillator

9.3.1 Introduction

The HFRCO is a calibrated internal High Frequency RC oscillator.

9.3.2 Features

- 1 MHz - 80 MHz High Frequency RC Oscillator with DPLL working in EM01 (HFRCODPLL)
- 1 MHz - 40 MHz High Frequency RC Oscillator working in EM23 (HFRCOEM23)
- Low start-up time
- Run-time band change or tuning

9.3.3 Functional Description

9.3.3.1 Start-up

The HFRCO starts up quickly in a few micro-seconds (refer to device data sheet for start-up time specifications.) After the start-up time, the RDY status bit will go high and the RDY interrupt will be triggered. It can take another two clock cycles for the clock to propagate through the CMU before the clock is seen by peripherals.

9.3.3.2 On-Demand Clocking

Software can request to enable the HFRCO by setting the HFRCO_CTRL.FORCEEN bit field. The HFRCO can also optionally be configured via the HFRCO_CTRL.DISONDEMAND to shut down when no hardware request is present. This is known as on-demand clocking and allows the oscillator to be controlled without any software intervention. This means that HFRCO receives a request for clock from the CMU whenever the oscillator clock is needed. These requests can come at any time from any power domain (depending on the which peripheral is requesting the clock.)

9.3.3.2.1 EM2/EM3 On-Demand Operation (HFRCOEM23)

The HFRCOEM23 can be used by certain peripherals as an on-demand, high-speed clock source in energy modes down to EM3. To enable operation as an on-demand clock in EM2 and EM3, the EM23ONDEMAND bit in the CTRL register should be set to 1. Setting this bit ensures that the associated PD0 power domain will remain active and allow the oscillator to honor the requesst.

Note: This feature is not available on the HFRCODPLL oscillator, which only operates in EM0 and EM1.

9.3.3.3 Calibration

Several different frequencies are calibrated during production test on every device. In order to use a factory-calibrated value, software must read the value from the appropriate location in the DEVINFO page and write it to the CAL register.

The TUNING and FINETUNING bit fields in the CAL register can be used to trim HFRCO manually.

Software may write the CAL register at any time. If there is already a frequency updating occuring, the current change would apply when the previous update is done. FREQBSY in STATUS register indicates if the updating is finished.

The minimum and maximum frequencies attainable for each setting of the FREQRANGE field are listed in the device data sheet.

Table 9.1. HFRCODPLL Calibration Frequencies

DEVINFO Location	Target Frequency
HFRCODPLLCAL0	4 MHz
HFRCODPLLCAL3	7 MHz
HFRCODPLLCAL6	13 MHz
HFRCODPLLCAL7	16 MHz
HFRCODPLLCAL8	19 MHz (default)
HFRCODPLLCAL10	26 MHz
HFRCODPLLCAL11	32 MHz
HFRCODPLLCAL12	38 MHz
HFRCODPLLCAL13	48 MHz
HFRCODPLLCAL14	56 MHz
HFRCODPLLCAL15	64 MHz
HFRCODPLLCAL16	80 MHz

Table 9.2. HFRCOEM23 Calibration Frequencies

DEVINFO Location	Target Frequency
HFRCOEM23CAL0	4 MHz
HFRCOEM23CAL1	5 MHz
HFRCOEM23CAL3	7 MHz
HFRCOEM23CAL4	10 MHz
HFRCOEM23CAL6	13 MHz
HFRCOEM23CAL7	16 MHz
HFRCOEM23CAL8	19 MHz (default)
HFRCOEM23CAL9	20 MHz
HFRCOEM23CAL10	26 MHz
HFRCOEM23CAL11	32 MHz
HFRCOEM23CAL12	40 MHz

9.3.3.4 Interrupts

HFRCO has one interrupt: IF.RDY. RDY is triggered when the timeout has finished and the qualified HFRCO clock is ready. The clock is gated until it is ready.

9.3.3.5 Status Flags

9.3.3.5.1 FREQBSY

The FREQBSY bit indicates the HFRCO is busy updating its frequency after writing to the CAL register. The FREQBSY bit should be used whenever frequency is changed. E.g. After software writes to the CAL register, FREQBSY would assert immediately. Software should wait for FREQBSY to be zero before attempting to write to the CAL register again.

For band-change, FREQBSY would not de-assert until after the timeout upon being re-enabled.

For normal start-up, FREQBSY would not assert.

When DPLL is on, FREQBSY would not assert as the frequency change is not caused by writing to the CAL register. When disabling DPLL the last tuning value is written back to the CAL register, which will assert FREQBSY.

9.3.3.5.2 ENS

ENS indicates the HFRCO is enabled. This flag is used to check if the HFRCO is enabled by any requester.

Note: When a band change occurs, the HFRCO is disabled and re-enabled. This will cause the ENS bit to briefly de-assert.

9.3.3.5.3 RDY

RDY indicates HFRCO is enabled and start-up timeout has exceeded. Used to check if the HFRCO clock is ready after enable.

Changing bands will de-assert RDY as the oscillator must reset and start up again.

9.3.3.5.4 SYNCBUSY

SYNCBUSY indicates ongoing synchronization of CAL register fields. Same as all other modules.

9.3.3.6 Forced Oscillator Control

The HFRCO can be forced on and off using the FORCEEN and DISONDEMAND bits in the CTRL register.

Setting FORCEEN will force the oscillator core to run, but peripherals will still need to request the clock to un-gate the clock signal.

9.3.3.7 Oscillator Modes

The HFRCO has three modes of operation, an **on-demand** mode (which is the normal software use case), a **force on** and a **force off** mode.

In **on-demand** mode the oscillator will start whenever a peripheral requests it. Which in most cases is whenever the peripheral is enabled.

In **force on** mode the analog core will run independently of whether it is requested or not. This can be useful for measuring analog current without any digital load on the clocks.

In **force off** mode, the analog core will be shut off independently of whether it is requested or not. This can be useful for changing analog test settings without risking glitches on the clock.

The DISONDEMAND bit can also be used to give software full control over the clock for exceptional cases where software control is desired.

Table 9.3. Oscillator modes

Bit Field	FORCEEN	DISONDEMAND
On-Demand (normal operation)	0	0
Forced On	1	X
Forced Off	0	1

9.3.4 HFRCO Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	HFRCO_IPVERSION	R	IP Version ID
0x004	HFRCO_CTRL	RW	Ctrl Register
0x008	HFRCO_CAL	RWH SYNC	Calibration Register
0x00C	HFRCO_STATUS	RH	Status Register
0x010	HFRCO_IF	RWH INTFLAG	Interrupt Flag Register
0x014	HFRCO_IEN	RW	Interrupt Enable Register
0x01C	HFRCO_LOCK	W	Lock Register
0x1000	HFRCO_IPVERSION_SET	R	IP Version ID
0x1004	HFRCO_CTRL_SET	RW	Ctrl Register
0x1008	HFRCO_CAL_SET	RWH SYNC	Calibration Register
0x100C	HFRCO_STATUS_SET	RH	Status Register
0x1010	HFRCO_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x1014	HFRCO_IEN_SET	RW	Interrupt Enable Register
0x101C	HFRCO_LOCK_SET	W	Lock Register
0x2000	HFRCO_IPVERSION_CLR	R	IP Version ID
0x2004	HFRCO_CTRL_CLR	RW	Ctrl Register
0x2008	HFRCO_CAL_CLR	RWH SYNC	Calibration Register
0x200C	HFRCO_STATUS_CLR	RH	Status Register
0x2010	HFRCO_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x2014	HFRCO_IEN_CLR	RW	Interrupt Enable Register
0x201C	HFRCO_LOCK_CLR	W	Lock Register
0x3000	HFRCO_IPVERSION_TGL	R	IP Version ID
0x3004	HFRCO_CTRL_TGL	RW	Ctrl Register
0x3008	HFRCO_CAL_TGL	RWH SYNC	Calibration Register
0x300C	HFRCO_STATUS_TGL	RH	Status Register
0x3010	HFRCO_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x3014	HFRCO_IEN_TGL	RW	Interrupt Enable Register
0x301C	HFRCO_LOCK_TGL	W	Lock Register

9.3.5 HFRCO Register Description

9.3.5.1 HFRCO_IPVERSION - IP Version ID

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x2																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x2	R	**IP Version**
	The read only IPVERSION field gives the version for this module. There may be minor software changes required for modules with different values of IPVERSION.			

9.3.5.2 HFRCO_CTRL - Ctrl Register

Offset	Bit Position																															
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x0	0x0	0x0
Access																														RW	RW	RW
Name																														EM23ONDEMAND	DISONDEMAND	FORCEEN

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	EM23ONDEMAND	0x0	RW	**EM23 On-demand**
	Use this bit to prevent EM23 shutdown of the HFRCOEM23 low power domain (PD0C) upon EM23 entry. Set this bit to 1 if on-demand requests are supposed to be honored while in EM23.			
1	DISONDEMAND	0x0	RW	**Disable On-demand**
	Setting this bit disable HFRCO on-demand feature			
0	FORCEEN	0x0	RW	**Force Enable**
	Setting this bit force HFRCO enabled			

9.3.5.3 HFRCO_CAL - Calibration Register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xA				0x2		0x0		0x3			0x8					0x1		0x1F							0x7F						
Access	RW				RW		RW		RW			RW					RW		RW							RW						
Name	IREFTC				CMPSEL		CLKDIV		CMPBIAS			FREQRANGE					LDOHP		FINETUNING							TUNING						

Bit	Name	Reset	Access	Description
31:28	IREFTC	0xA	RW	**Tempco Trim on Comparator Current**
	Writing this field adjusts the temperature coefficient trim on comparator current.			
27:26	CMPSEL	0x2	RW	**Comparator Load Select**
	Writing this field adjusts the active load for comparators.			
25:24	CLKDIV	0x0	RW	**Locally Divide HFRCO Clock Output**
	Writing this field configures the HFRCO clock output divider.			

Value	Mode	Description
0	DIV1	Divide by 1.
1	DIV2	Divide by 2.
2	DIV4	Divide by 4.

23:21	CMPBIAS	0x3	RW	**Comparator Bias Current**
	Writing this field adjusts the HFRCO comparator bias current.			
20:16	FREQRANGE	0x8	RW	**Frequency Range**
	Writing this field adjusts the HFRCO frequency range.			
15	LDOHP	0x1	RW	**LDO High Power Mode**
	Settings this bit puts the HFRCO LDO in high power mode.			
14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13:8	FINETUNING	0x1F	RW	**Fine Tuning Value**
	Writing this field adjusts the HFRCO fine tuning value. Higher value means lower frequency.			
7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:0	TUNING	0x7F	RW	**Tuning Value**
	Writing this field adjusts the HFRCO tuning value. Higher value means lower frequency.			

9.3.5.4 HFRCO_STATUS - Status Register

Offset	Bit Position																														
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0															0x0														0x0	0x0	0x0
Access	R															R														R	R	R
Name	LOCK															ENS														SYNCBUSY	FREQBSY	RDY

Bit	Name	Reset	Access	Description
31	LOCK	0x0	R	**Lock Status**
	If set, all HFRCO lockable registers are locked.			

Value	Mode	Description
0	UNLOCKED	HFRCO is unlocked
1	LOCKED	HFRCO is locked

30:17	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
16	ENS	0x0	R	**Enable Status**
	HFRCO is enabled.			
15:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	SYNCBUSY	0x0	R	**Synchronization Busy**
	This bit is set when there is an ongoing synchronization of CAL register bitfields.			
1	FREQBSY	0x0	R	**Frequency Updating Busy**
	HFRCO is busy updating frequency.			
0	RDY	0x0	R	**Ready**
	HFRCO is enabled and start-up time has exceeded.			

9.3.5.5 HFRCO_IF - Interrupt Flag Register

Offset	Bit Position																														
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																RW
Name																																RDY

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	RDY	0x0	RW	**Ready Interrupt Flag**
	Set when HFRCO is ready (start-up time exceeded).			

9.3.5.6 HFRCO_IEN - Interrupt Enable Register

Offset	Bit Position																														
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																RW
Name																																RDY

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	RDY	0x0	RW	**RDY Interrupt Enable**
	Enable/disable the RDY interrupt			

9.3.5.7 HFRCO_LOCK - Lock Register

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x8195						
Access																									W						
Name																									LOCKKEY						

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LOCKKEY	0x8195	W	**Lock Key**

Write any other value than the unlock code to lock registers from editing. Write the unlock code to unlock.

Value	Mode	Description
33173	UNLOCK	Unlock code

9.4 DPLL - Digital Phased Locked Loop

9.4.1 Introduction

The Digital Phase-Locked Loop (DPLL) uses a reference clock to generate a desired clock frequency at a specified ratio to the reference clock.

9.4.2 Features

- Frequency Lock Mode
- Phase-Lock Mode
- Output frequency = F_{REF}*(N+1)/(M+1), where N and M are 12-bit values
- Very fast lock time
- Very fast transient tracking
- Low output jitter
- Lock detection with an interrupt
- Lock fail detection with interrupts

9.4.3 Functional Description

9.4.3.1 Enabling and Disabling

The DPLL can be enabled and disabled by software via the DPLL_EN register. Before enabling DPLL, software should:

1. Select reference clock by setting the CLKSEL field in CMU_DPLLREFCLKCTRL.
2. The CMU should not be running from the HFRCO. If necessary, the CMU should switch to the FSRCO until after the DPLL has locked to avoid over-clocking due to overshoot. If necessary, select FSRCO or HFXO in the CMU_SYSCLKCTRL register CLKSEL field.
3. Configure the DPLL.
4. Make certain that the ENS bit in DPLL_STATUS is low.

The DPLL is disabled automatically when entering EM2, EM3, or EM4. Note that disabling the DPLL will not automatically turn off the reference clock. The CLKSEF field in CMU_DPLLREFCLKCTRL must be set to DISABLED before entering EM2 or the selected REFCLK may continue to run in EM2.

9.4.3.2 Lock Modes

The DPLL provides two lock modes, referred to as frequency-lock loop mode (FREQLL) and phase-lock loop mode (PHASELL). FREQLL mode keeps the DCO frequency-locked to the reference clock, which means the DCO frequency will be accurate. However, the phase error can accumulate over time and cause a non-zero average frequency error. FREQLL mode also provides better jitter and transient performance. PHASELL mode keeps the DCO phase-locked to the reference clock, which means the phase error does not accumulate over time, which makes the average frequency error zero. FREQLL mode should be used unless specific phase requirement exists.

9.4.3.3 Configurations

The formula for the DPLL output frequqncy is FREF*(N+1)/(M+1). The user should calculate N and M in DPLL_CFG1 to achieve the target frequency. Note that with a larger value of N, the DCO lock time would increase and DCO jitter would decrease. Both effects are approximately linear. This relationship can be used to select N for a given application to strike a compromise between lock time and output jitter. For example if an ratio of 3 is desired, the DPLL could be configured as {N=599, M=199} for fast lock time but high jitter, or as {N=2999, M=999} for lower jitter but longer lock time.

Note: All configuration settings should be done before enabling the DPLL. They should not be changed when DPLL is running. The final tuning values can be read back from TUNING and FINETUNING in HFRCO_CAL, after DPLL is disabled and DPLLENS in DPLL_STATUS is low.

9.4.3.4 Lock Detection

The DPLL has 3 different types of output events: ready, lock fail due to period underflow, and lock fail due to period overflow. Each of the events has its own interrupt flag. DPLLRDY is set when DPLL successfully locks to the reference clock based on the software configuration. DPLLLOCKFAILLOW is set when the DPLL fails to lock because the period lower boundary is hit. DPLLLOCKFAILHIGH is set when the DPLL fails to lock because the period upper boundary is hit. If the interrupt flags are set and the corresponding interrupt enable bits in DPLL_IEN are set, the DPLL will request an interrupt. Based on different interrupt events, software should take different actions:

- If the DPLLRDY interrupt is received first, it means target clock is ready and it is safe to switch to use DCO's output.
- If the DPLLLOCKFAILLOW interrupt is received first, it indicates the RANGE in HFRCO_CAL is too small. Software should disable the DPLL and write a larger value to RANGE, then enable the DPLL again to lock.
- If the DPLLLOCKFAILHIGH interrupt is received first, it indicates the RANGE in HFRCO_CAL is too large. Software should disable DPLL and write a smaller value to RANGE, then enable DPLL again to lock.
- If the DPLLRDY interrupt is received first and then DPLLLOCKFAILLOW or DPLLLOCKFAILHIGH is received later, it means reference clock drifted over 1% and the DPLL has lost its locked status.
  - If AUTORECOVER in DPLL_CFG is not set, software should disable the DPLL and enable DPLL again to lock.
  - If AUTORECOVER in DPLL_CFG is set, hardware will re-lock automatically. When the target frequency is near the boundary of a range, the drift may cause underflow or overflow. In this case the fail interrupt will still be received. Software should disable the DPLL and modify RANGE in HFRCO_CAL in corresponding direction, depending on whether the DPLLLOCKFAILLOW or DPLLLOCKFAILHIGH bit is set. Then enable DPLL again to lock.

9.4.4 DPLL Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	DPLL_IPVERSION	R	IP Version
0x004	DPLL_EN	RW ENABLE	Enable
0x008	DPLL_CFG	RW CONFIG	Config
0x00C	DPLL_CFG1	RW CONFIG	Config1
0x010	DPLL_IF	RWH INTFLAG	Interrupt Flag
0x014	DPLL_IEN	RW	Interrupt Enable
0x018	DPLL_STATUS	RH	Status
0x024	DPLL_LOCK	W	Lock
0x1000	DPLL_IPVERSION_SET	R	IP Version
0x1004	DPLL_EN_SET	RW ENABLE	Enable
0x1008	DPLL_CFG_SET	RW CONFIG	Config
0x100C	DPLL_CFG1_SET	RW CONFIG	Config1
0x1010	DPLL_IF_SET	RWH INTFLAG	Interrupt Flag
0x1014	DPLL_IEN_SET	RW	Interrupt Enable
0x1018	DPLL_STATUS_SET	RH	Status
0x1024	DPLL_LOCK_SET	W	Lock
0x2000	DPLL_IPVERSION_CLR	R	IP Version
0x2004	DPLL_EN_CLR	RW ENABLE	Enable
0x2008	DPLL_CFG_CLR	RW CONFIG	Config
0x200C	DPLL_CFG1_CLR	RW CONFIG	Config1
0x2010	DPLL_IF_CLR	RWH INTFLAG	Interrupt Flag
0x2014	DPLL_IEN_CLR	RW	Interrupt Enable
0x2018	DPLL_STATUS_CLR	RH	Status
0x2024	DPLL_LOCK_CLR	W	Lock
0x3000	DPLL_IPVERSION_TGL	R	IP Version
0x3004	DPLL_EN_TGL	RW ENABLE	Enable
0x3008	DPLL_CFG_TGL	RW CONFIG	Config
0x300C	DPLL_CFG1_TGL	RW CONFIG	Config1
0x3010	DPLL_IF_TGL	RWH INTFLAG	Interrupt Flag
0x3014	DPLL_IEN_TGL	RW	Interrupt Enable
0x3018	DPLL_STATUS_TGL	RH	Status
0x3024	DPLL_LOCK_TGL	W	Lock

9.4.5 DPLL Register Description

9.4.5.1 DPLL_IPVERSION - IP Version

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x1																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x1	R	**IP Version ID**
	The read only IPVERSION field gives the version for this module. There may be minor software changes required for modules with different values of IPVERSION.			

9.4.5.2 DPLL_EN - Enable

Offset	Bit Position																															
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	RW
Name																															DISABLING	EN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DISABLING	0x0	R	**Disablement Busy Status**
	When EN is cleared, DISABLING status is set immediately, and cleared when disablement finishes. Disablement resets peripheral cores and not APB registers except hardware updated registers such as INTFLAGs and FIFO			
0	EN	0x0	RW	**Module Enable**
	The ENABLE bit enables the module. Software should write to CONFIG type registers before setting the ENABLE bit. Software should write to SYNC type registers only after setting the ENABLE bit.			

9.4.5.3 DPLL_CFG - Config

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																										0x0				0x0	0x0	0x0
Access																										RW				RW	RW	RW
Name																										DITHEN				AUTORECOVER	EDGESEL	MODE

Bit	Name	Reset	Access	Description
31:7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6	DITHEN	0x0	RW	**Dither Enable Control**
	Set to enable dither function			
5:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	AUTORECOVER	0x0	RW	**Automatic Recovery Control**
	Set to enable automatic recovery function			
1	EDGESEL	0x0	RW	**Reference Edge Select**
	This bit controls which edge of reference is detected			
0	MODE	0x0	RW	**Operating Mode Control**
	This bit controls which mode DPLL is operating when enabled			

Value	Mode	Description
0	FLL	Frequency Lock Mode
1	PLL	Phase Lock Mode

9.4.5.4 DPLL_CFG1 - Config1

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0x0																0x0											
Access					RW																RW											
Name					N																M										

Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27:16	N	0x0	RW	**Factor N**
	The locked DCO frequency is given by: Fdco = Fref * (N + 1)/(M+1). N is required to be larger than 300.			
15:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:0	M	0x0	RW	**Factor M**
	The locked DCO frequency is given by: Fdco = Fref * (N + 1)/(M+1). M can be any value.			

9.4.5.5 DPLL_IF - Interrupt Flag

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x0	0x0	0x0
Access																														RW	RW	RW
Name																														LOCKFAILHIGH	LOCKFAILLOW	LOCK

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	LOCKFAILHIGH	0x0	RW	**Lock Failure High Interrupt Flag**
	Set when DPLL fail to lock because of period overflow.			
1	LOCKFAILLOW	0x0	RW	**Lock Failure Low Interrupt Flag**
	Set when DPLL fail to lock because of period underflow.			
0	LOCK	0x0	RW	**Lock Interrupt Flag**
	Set when DPLL achieve the lock.			

9.4.5.6 DPLL_IEN - Interrupt Enable

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x0	0x0	0x0
Access																														RW	RW	RW
Name																														LOCKFAILHIGH	LOCKFAILLOW	LOCK

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	LOCKFAILHIGH	0x0	RW	**LOCKFAILHIGH Interrupt Enable**
	LOCKFAILHIGH Interrupt Enable			
1	LOCKFAILLOW	0x0	RW	**LOCKFAILLOW Interrupe Enable**
	LOCKFAILLOW Interrupe Enable			
0	LOCK	0x0	RW	**LOCK interrupt Enable**
	LOCK interrupt Enable			

9.4.5.7 DPLL_STATUS - Status

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																														0x0	0x0
Access	R																														R	R
Name	LOCK																														ENS	RDY

Bit	Name	Reset	Access	Description
31	LOCK	0x0	R	**Lock Status**
	Indicates the current status of configuration lock			

Value	Mode	Description
0	UNLOCKED	DPLL is unlocked
1	LOCKED	DPLL is locked

30:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	ENS	0x0	R	**Enable Status**
	DPLL is enabled.			
0	RDY	0x0	R	**Ready Status**
	DPLL is enabled and locked.			

9.4.5.8 DPLL_LOCK - Lock

Offset	Bit Position																													
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x7102															
Access																	W															
Name																	LOCKKEY															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LOCKKEY	0x7102	W	**Lock Key**
	Write any other value than the unlock code to lock registers from editing. Write the unlock code to unlock.			

Value	Mode	Description
28930	UNLOCK	Unlock code

9.5 LFXO - Low-Frequency Crystal Oscillator

9.5.1 Introduction

The Low Frequency Crystal Oscillator (LFXO) uses an external 32.768 kHz crystal to provide an accurate low-frequency clock. The module is available in all energy modes, except EM3. The main interaction is with the CMU through the clock requesting mechanism.

9.5.2 Features

High-level features.

- Crystal calibration
- Functional in all energy modes, except EM3
- Failure detection and EM4WU
- External CMOS mode
- Edge interrupts and EM2WU
- On-demand oscillator enabling

9.5.3 Functional Description

9.5.3.1 Modes

The LFXO can be used in three different modes. The mode can be programmed by setting MODE bit field in the LFXO_CFG register. If MODE is set to XTAL, the LFXO is programmed to operate in crystal mode and a 32.768 kHz crystal oscillator should be connected to LF crystal pads, LFXTAL_I and LFXTAL_O (see the device data sheet for details). If MODE is set to BUFEXTCLK, the LFXO is programmed to operate in external sine mode and the sine wave should be supplied to LFXTAL_I pin. If MODE is set to DIGEXTCLK, LFXO is programmed to operate in external CMOS mode and the external 32.768 kHz clock should be provided on LFXTAL_I pin. See the register descriptions for more details.

9.5.3.2 Enabling

There are two ways to turn on the LFXO clock. One is to turn it on in FORCEON mode by setting FORCEEN bit to 1 in LFXO_CTRL register. Another is to keep it ready to be turned on in ONDEMAND mode by setting FORCEEN bit to 0 and DISONDEMAND bit to 0 in LFXO_CTRL register. This means that the oscillator will be off unless its clock requested. When a peripheral requests the clock, hardware will automatically enable the LFXO without any software intervention. The oscillator will remain on as long as the peripheral requests it. DISONDEMAND setting does not have any impact when FORCEEN set to 1. LFXO is in FORCEOFF mode when FORCEEN set to 0 and DISONDEMAND set to 1. In FORCEOFF mode all requests are blocked and LFXO will not generate the clock. The LFXO clock is available in all energy modes, except EM3.

9.5.3.3 Clock Qualification

Once the LFXO is enabled, the clock should not be used until it has had time to stabilize. Therefore, a number of cycles are required to qualify the clock. Before the clock is qualified, no clock requesters will receive the LFXO clock. The number of cycles used to qualify the clock can be programmed by setting the TIMEOUT bit field in the LFXO_CFG register. The TIMEOUT default value is set to 32,728 cycles, which is much more than necessary for stabilization. The stabilization time required will depend on the particular crystal, oscillator settings, and frequency accuracy requirements. A value of 4096 clocks is generally recommended for most applications. A low timeout of 2 cycles may be used in DIGEXTCLK mode in order to filter out the first glitch from the pad. The 2 clock cycle timeout should not be used with crystals. There are two status bits and one interrupt associated with enabling the oscillator and qualifying its clock. Once the oscillator gets enabled the ENS bit in LFXO_STATUS register will be set high. Note that due to the nature of on demand clocking, the oscillator can be enabled anytime, so if software reads ENS low it is not safe to assume that ENS stays low during the next instruction. It is only safe to assume that oscillator is OFF at the time ENS is being read. Similarly, if software reads ENS high it is not safe to assume that ENS stays high during the next instruction. Once the clock is qualified, the RDY status is set high in the LFXO_STATUS register. The same uncertainties also apply to the RDY bit. However, software can wait for RDY bit to go high to detect that LFXO clock is qualified. Or it can enable the interrupt with RDYIEN in LFXO_IEN register and receive RDYIF interrupt available in LFXO_IF register. RDYIF also acts as EM2 wakeup source if RDYIEN set high. If put into FORCEON mode, the LFXO will start the qualification and once qualified it will gate off the clock but immediately start with no qualification upon receiving a request. If in ONDEMAND mode, the LFXO starts the qualification every time it is switched from off to on due to clock requests. The qualification can take up to 32k cycles. Note that only enabling RDY interrupt does not act as a clock request.

9.5.3.4 Edge Detection Interrupts

There is a possibility for software to detect rising or falling edges of the LFXO clock. The edge detection is enabled if any of POSEDGEIEN and NEGEDGEIEN is set to 1. The corresponding flags are available in POSEDGEIF and NEGEDGEIF. If none of the interrupts are enabled, the edge detection is disabled and POSEDGEIF and NEGEDGEIF hold their last value until cleared or set by software. Disabling the edge detection is only allowed on NEGEDGEIF. Both flags act as EM2 wakeup sources if the corresponding IEN is set high.

9.5.3.5 Clock Failure

In case the oscillator or crystal stops or does not output clock when expected, a failure interrupt can be raised. The failure occurs if fewer than 3 LFXO clock positive edges happen during one 1ms. The failure detection is enabled by setting FAILDETEN to 1 in LFXO_CTRL register. This bit acts as a clock requester. Once enabled, failure detection status can be checked by reading FAILIF in LFXO_IF register. If FAILIEN is set high, failure will generate both interrupt and EM2 wakeup. Failure detection is also implemented as EM4 wakeup source. To wakeup from EM4 on LFXO failure detection, set FAILDETEM4WUEN high in LFXO_CTRL.

9.5.3.6 Automatic Gain Control

AGC and HIGHAMPL in LFXO_CFG are settings applied to the LFXO oscillator. Both settings provide higher crystal oscillation amplitude. This will improve duty cycle in the output clock and give lower sensitivity to noise, but at the cost of higher current consumption. The AGC bit is used to enable the Automatic Gain Control module that adjusts the amplitude of the oscillations. It is enabled by default. When disabled, the LFXO will run at the start-up current and the crystal will oscillate rail-to-rail or limited by the start-up current. The HIGHAMPL bit will have no effect when AGC is disabled. When AGC is enabled setting the HIGHAMPL bit will give about 70% higher crystal oscillation amplitude.

9.5.3.7 Force Off

It is not allowed to write to LFXO_CFG unless LFXO is in FORCEOFF mode. If this guideline is violated, the write access is blocked and a bus fault is generated. Writing to CFG registers has no effect in DIGEXTCLK mode. Note: when putting the oscillators to FORCEOFF mode, wait for ENS status to go low for the oscillator to completely shut off. Once the oscillator is forced off, it is safe to write to the LFXO_CFG register.

9.5.3.8 Register Synchronization

While the CFG registers are static LFXO configuration, LFXO_CAL register has GAIN and CAPTUNE bit fields which can be written to while the oscillator is running. This is used to calibrate the LFXO clock. These registers are allowed to be written only if CALBSY in LFXO_SYNCBUSY register is low. If this guideline is violated, the write access is blocked and a bus fault is generated. CALBSY is guaranteed to be low in FORCEOFF mode. When exiting FORCEOFF mode, CALBSY will go high and stay high until the initial internal synchronization is done. CALBSY is also guaranteed to be low in DIGEXTCLK mode since writing to CAL register has no effect in DIGEXTCLK mode. CAPTUNE is allowed to be incremented or decremented by one LSB when not in FORCEOFF mode. Note that CAPTUNE tunes the internal capacitors connected to LFXTAL_I and LFXTAL_O pads (see Register map for more details). By programming GAIN bit field it is possible to optimize start-up time and power consumption for a given crystal. Internal capacitances are not provided on all chips (see the device data sheet for more details).

9.5.3.9 Register Lock

See the LFXO_LOCK register on how to lock certain registers. Registers LFXO_CTRL, LFXO_CFG, and LFXO_CAL are lockable. The LOCK bit in LFXO_STATUS register is available to check whether the registers are locked. If locked, all updates to these registers are blocked and bus faults are issued.

9.5.3.10 Reset Behavior

Upon reset, the LFXO is configured for the safe crystal start-up. The TIMEOUT is set to 32k cycles, The MODE is set to XTAL and the reset state is FORCEOFF. In order to minimize the start-up time and power consumption for a given crystal, it is possible to adjust the start-up gain in the oscillator by programming GAIN in LFXO_CAL. All controls are retained in EM4, except LFXO_IEN register which is reset after EM4 wakeup.

9.5.4 LFXO Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	LFXO_IPVERSION	R	LFXO IP Version
0x004	LFXO_CTRL	RW	LFXO Control Register
0x008	LFXO_CFG	RW	LFXO Configuration Register
0x010	LFXO_STATUS	RH	LFXO Status Register
0x014	LFXO_CAL	RW LFSYNC	LFXO Calibration Register
0x018	LFXO_IF	RWH INTFLAG	Interrupt Flag Register
0x01C	LFXO_IEN	RW	Interrupt Enable Register
0x020	LFXO_SYNCBUSY	RH	LFXO Sync Busy Register
0x024	LFXO_LOCK	W	Configuration Lock Register
0x1000	LFXO_IPVERSION_SET	R	LFXO IP Version
0x1004	LFXO_CTRL_SET	RW	LFXO Control Register
0x1008	LFXO_CFG_SET	RW	LFXO Configuration Register
0x1010	LFXO_STATUS_SET	RH	LFXO Status Register
0x1014	LFXO_CAL_SET	RW LFSYNC	LFXO Calibration Register
0x1018	LFXO_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x101C	LFXO_IEN_SET	RW	Interrupt Enable Register
0x1020	LFXO_SYNCBUSY_SET	RH	LFXO Sync Busy Register
0x1024	LFXO_LOCK_SET	W	Configuration Lock Register
0x2000	LFXO_IPVERSION_CLR	R	LFXO IP Version
0x2004	LFXO_CTRL_CLR	RW	LFXO Control Register
0x2008	LFXO_CFG_CLR	RW	LFXO Configuration Register
0x2010	LFXO_STATUS_CLR	RH	LFXO Status Register
0x2014	LFXO_CAL_CLR	RW LFSYNC	LFXO Calibration Register
0x2018	LFXO_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x201C	LFXO_IEN_CLR	RW	Interrupt Enable Register
0x2020	LFXO_SYNCBUSY_CLR	RH	LFXO Sync Busy Register
0x2024	LFXO_LOCK_CLR	W	Configuration Lock Register
0x3000	LFXO_IPVERSION_TGL	R	LFXO IP Version
0x3004	LFXO_CTRL_TGL	RW	LFXO Control Register
0x3008	LFXO_CFG_TGL	RW	LFXO Configuration Register
0x3010	LFXO_STATUS_TGL	RH	LFXO Status Register
0x3014	LFXO_CAL_TGL	RW LFSYNC	LFXO Calibration Register
0x3018	LFXO_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x301C	LFXO_IEN_TGL	RW	Interrupt Enable Register
0x3020	LFXO_SYNCBUSY_TGL	RH	LFXO Sync Busy Register

Offset	Name	Type	Description
0x3024	LFXO_LOCK_TGL	W	Configuration Lock Register

9.5.5 LFXO Register Description

9.5.5.1 LFXO_IPVERSION - LFXO IP Version

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x1																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x1	R	**IP Version ID**
	The read only IPVERSION field gives the version for this module. There may be minor software changes required for modules with different values of IPVERSION.			

9.5.5.2 LFXO_CTRL - LFXO Control Register

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0	0x0			0x1	0x0
Access																											RW	RW			RW	RW
Name																											FAILDETEM4WUEN	FAILDETEN			DISONDEMAND	FORCEEN

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	FAILDETEM4WUEN	0x0	RW	**LFXO Failure Detection EM4WU Enable**
	Set this bit to enable EM4 exit on the oscillator failure detection.			
4	FAILDETEN	0x0	RW	**LFXO Failure Detection Enable**
	Set this bit to enable the oscillator failure detection feature. Note that setting this bit will enable the oscillator core.			
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DISONDEMAND	0x1	RW	**LFXO Disable On-demand requests**
	Set this bit to disable On-demand requests.			
0	FORCEEN	0x0	RW	**LFXO Force Enable**
	Set this bit to enable the oscillator core. The oscillator core is enabled regardless of On-demand requests.			

9.5.5.3 LFXO_CFG - LFXO Configuration Register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x7				0x0				0x0	0x1
Access																							RW				RW				RW	RW
Name																							TIMEOUT				MODE				HIGHAMPL	AGC

Bit	Name	Reset	Access	Description
31:11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10:8	TIMEOUT	0x7	RW	**LFXO Start-up Delay**

Configures the start-up delay for LFXO.

Value	Mode	Description
0	CYCLES2	Timeout period of 2 cycles
1	CYCLES256	Timeout period of 256 cycles
2	CYCLES1K	Timeout period of 1024 cycles
3	CYCLES2K	Timeout period of 2048 cycles
4	CYCLES4K	Timeout period of 4096 cycles
5	CYCLES8K	Timeout period of 8192 cycles
6	CYCLES16K	Timeout period of 16384 cycles
7	CYCLES32K	Timeout period of 32768 cycles

7:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:4	MODE	0x0	RW	**LFXO Mode**

Selects the LFXO mode.

Value	Mode	Description
0	XTAL	A 32768Hz crystal should be connected to the LF crystal pads. Voltage must not exceed VDDIO.
1	BUFEXTCLK	An external sine source with minimum amplitude 100mv (zero-to-peak) and maximum amplitude 500mV (zero-to-peak) should be connected in series with LFXTAL_I pin. Minimum voltage should be larger than ground and maximum voltage smaller than VDDIO. The sine source does not need to be ac coupled externally as it is ac couples inside LFXO. LFXTAL_O is free to be used as a general purpose GPIO.
2	DIGEXTCLK	An external 32KHz CMOS clock should be provided on LFXTAL_I. LFXTAL_O is free to be used as a general purpose GPIO.

Bit	Name	Reset	Access	Description
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	HIGHAMPL	0x0	RW	**LFXO High Amplitude Enable**
	Set this bit to enable high XTAL oscillation amplitude.			
0	AGC	0x1	RW	**LFXO AGC Enable**
	Set this bit to enable automatic gain control which limits XTAL oscillation amplitude.			

9.5.5.4 LFXO_STATUS - LFXO Status Register

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0															0x0																0x0
Access	R															R																R
Name	LOCK															ENS																RDY

Bit	Name	Reset	Access	Description
31	LOCK	0x0	R	**LFXO Locked Status**
	If set, all LFXO lockable registers are locked.			

Value	Mode	Description
0	UNLOCKED	LFXO lockable registers are not locked
1	LOCKED	LFXO lockable registers are locked

30:17	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
16	ENS	0x0	R	**LFXO Enable Status**
	LFXO is enabled.			
15:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	RDY	0x0	R	**LFXO Ready Status**
	LFXO is enabled and start-up time has exceeded.			

9.5.5.5 LFXO_CAL - LFXO Calibration Register

Offset	Bit Position																															
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x1						0x0			
Access																							RW						RW			
Name																							GAIN						CAPTUNE			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	GAIN	0x1	RW	**LFXO Startup Gain** The optimal value depends on the chosen crystal.
7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:0	CAPTUNE	0x0	RW	**Internal Capacitance Tuning** Program internal load capacitance connected between X_N pin and ground and X_P pin and ground. The bus affects tuning capacitances on both pins symmetrically. CAPTUNE value must not exceed 0x4F. When updating CAPTUNE, its value must only be incremented or decremented by 1 which provides a tuning step of 0.25pF. The maximum value is estimated to be 20pF. Please refer to the device Datasheet for more information.

9.5.5.6 LFXO_IF - Interrupt Flag Register

Offset	Bit Position																															
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0	0x0	0x0	0x0
Access																													RW	RW	RW	RW
Name																													FAIL	NEGEDGE	POSEDGE	RDY

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	FAIL	0x0	RW	**LFXO Failure Interrupt Flag**
	Set when LFXO failure is detected. Write 1 to clear the interrupt flag.			
2	NEGEDGE	0x0	RW	**Falling Edge Interrupt Flag**
	Triggers on every negative edge of the LFXO clock.			
1	POSEDGE	0x0	RW	**Rising Edge Interrupt Flag**
	Triggers on every positive edge of the LFXO clock.			
0	RDY	0x0	RW	**LFXO Ready Interrupt Flag**
	Set when LFXO is ready (start-up time exceeded). Write 1 to clear the interrupt flag.			

9.5.5.7 LFXO_IEN - Interrupt Enable Register

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0	0x0	0x0	0x0
Access																													RW	RW	RW	RW
Name																													FAIL	NEGEDGE	POSEDGE	RDY

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	FAIL	0x0	RW	**LFXO Failure Interrupt Enable**
	Write 1 to enable FAILIF			
2	NEGEDGE	0x0	RW	**Falling Edge Interrupt Enable**
	Write 1 to enable NEGEDGEIF.			
1	POSEDGE	0x0	RW	**Rising Edge Interrupt Enable**
	Write 1 to enable POSEDGEIF.			
0	RDY	0x0	RW	**LFXO Ready Interrupt Enable**
	Write 1 to enable RDYIF.			

9.5.5.8 LFXO_SYNCBUSY - LFXO Sync Busy Register

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																R
Name																																CAL

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	CAL	0x0	R	**LFXO Synchronization status**
	This bit is set when there is an ongoing synchronization of CAL register bitfields. Do not write to CAL register while this bit is set.			

9.5.5.9 LFXO_LOCK - Configuration Lock Register

Offset	Bit Position																													
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																								0x1A20								
Access																								W								
Name																								LOCKKEY								

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LOCKKEY	0x1A20	W	**Lock Key**

Write any other value than UNLOCK to lock CTRL, CFG and CAL registers. Write UNLOCK value to unlock the registers.

Value	Mode	Description
6688	UNLOCK	Unlock LFXO lockable registers

9.6 LFRCO - Low-Frequency RC Oscillator

9.6.1 Introduction

The LFRCO is an integrated low-frequency (32.768 kHz) RC oscillator that may be used as a timing reference in low energy modes when crystal accuracy is not required.

9.6.2 Features

- 32.768 kHz oscillator
- High Accuracy
- Available in all energy modes, except EM3
- On-demand
- EM2 wakeup interrupt for oscillator ready
- EM2 wakeup interrupts for rising and falling edges of the clock
- Lockable registers
- Trim bit synchronization

9.6.3 Functional Description

9.6.3.1 Start-up

The LFRCO has a fast start-up time (refer to the data sheet electrical specifications for the exact start-up time). When the oscillator has started up and is ready to use, the RDY status bit will go high and the RDY interrupt will be triggered. After start-up, it may take two clock cycles for the clock to propagate through the CMU to the peripherals.

9.6.3.2 On-Demand Clocking

Software may forceably enable the LFRCO by setting the LFRCO_CTRL.FORCEEN bit field. However, by default, the LFRCO is configured to be enabled only when required by hardware, and to shut down when no hardware request is present (i.e. LFRCO_CTRL.DISONDEMAND=0 and LFRCO_CTRL.FORCEEN=0). This is known as on-demand clocking and allows the oscillator to be controlled without any software intervention.

9.6.3.3 Calibration

The LFRCO is trimmed in production and the trim values are automatically written to the FREQTRIM field in the LFRCO_CAL register, before user code execution. Normally, software does not need to modify the to the LFRCO_CAL register. However, it is possible for software to re-calibrate the LFRCO by modifying the FREQTRIM value. This might be desired, for example if re-calibration is needed at a specific temperature, or there is a desire to use different trim values at different temperatures.

It is possible to recalibrate the LFRCO by modifying the FREQTRIM value in the LFRCO_CAL register. Software may modify the LFRCO_CAL register while it is running. However, the LFRCO_CAL has hardware synchronization, and should only be written after checking that SYNCBUSY_CALBSY is not set.

9.6.3.4 Interrupts

LFRCO has three interrupts, RDYIF, POSEDGEIF and NEGEDGEIF. Each will trigger an EM2 wakeup if the corresponding IEN is set.

RDYIF is triggered after start-up, when the LFRCO startup sequence is complete and the oscillator is ready to use.

POSEDGEIF and NEGEDGEIF are triggered by the rising and falling edge of LFRCO respectively. These flags will only get set if either of the interrupts are enabled (with POSEDGEIEN or NEGEDGEIEN), as the interrupt enable acts as a clock requester and keeps the oscillator running.

9.6.4 LFRCO Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	LFRCO_IPVERSION	R	IP Version
0x008	LFRCO_STATUS	RH	Status Register
0x00C	LFRCO_CAL	RW	Calibration Register
0x014	LFRCO_IF	RWH INTFLAG	Interrupt Flag Register
0x018	LFRCO_IEN	RW	Interrupt Enable Register
0x01C	LFRCO_SYNCBUSY	RH	Synchronization Busy Register
0x020	LFRCO_LOCK	W	Configuration Lock Register
0x1000	LFRCO_IPVERSION_SET	R	IP Version
0x1008	LFRCO_STATUS_SET	RH	Status Register
0x100C	LFRCO_CAL_SET	RW	Calibration Register
0x1014	LFRCO_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x1018	LFRCO_IEN_SET	RW	Interrupt Enable Register
0x101C	LFRCO_SYNCBUSY_SET	RH	Synchronization Busy Register
0x1020	LFRCO_LOCK_SET	W	Configuration Lock Register
0x2000	LFRCO_IPVERSION_CLR	R	IP Version
0x2008	LFRCO_STATUS_CLR	RH	Status Register
0x200C	LFRCO_CAL_CLR	RW	Calibration Register
0x2014	LFRCO_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x2018	LFRCO_IEN_CLR	RW	Interrupt Enable Register
0x201C	LFRCO_SYNCBUSY_CLR	RH	Synchronization Busy Register
0x2020	LFRCO_LOCK_CLR	W	Configuration Lock Register
0x3000	LFRCO_IPVERSION_TGL	R	IP Version
0x3008	LFRCO_STATUS_TGL	RH	Status Register
0x300C	LFRCO_CAL_TGL	RW	Calibration Register
0x3014	LFRCO_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x3018	LFRCO_IEN_TGL	RW	Interrupt Enable Register
0x301C	LFRCO_SYNCBUSY_TGL	RH	Synchronization Busy Register
0x3020	LFRCO_LOCK_TGL	W	Configuration Lock Register

9.6.5 LFRCO Register Description

9.6.5.1 LFRCO_IPVERSION - IP Version

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x0	R	**IP version ID**
	The read only IPVERSION field gives the version for this module. There may be minor software changes required for modules with different values of IPVERSION.			

9.6.5.2 LFRCO_STATUS - Status Register

Offset	Bit Position																															
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0															0x0																0x0
Access	R															R																R
Name	LOCK															ENS																RDY

Bit	Name	Reset	Access	Description
31	LOCK	0x0	R	**Lock Status**
	This bit is set when LFRCO is locked.			

Value	Mode	Description
0	UNLOCKED	Access to configuration registers not locked
1	LOCKED	Access to configuration registers locked

30:17	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*

Bit	Name	Reset	Access	Description
16	ENS	0x0	R	**Enabled Status**
	This bit is set when LFRCO is enabling the analog core.			

15:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*

Bit	Name	Reset	Access	Description
0	RDY	0x0	R	**Ready Status**
	This bit is set when qualification is done and LFRCO is ready.			

9.6.5.3 LFRCO_CAL - Calibration Register

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0xA5				
Access																												RW				
Name																												FREQTRIM				

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	FREQTRIM	0xA5	RW	**Frequency Trim**
	Trims the clock frequency of the LFRCO			

9.6.5.4 LFRCO_IF - Interrupt Flag Register

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x0	0x0	0x0
Access																														RW	RW	RW
Name																														NEGEDGE	POSEDGE	RDY

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	NEGEDGE	0x0	RW	**Falling Edge Interrupt Flag**
	Triggers on every negative edge of the LFRCO clock.			
1	POSEDGE	0x0	RW	**Rising Edge Interrupt Flag**
	Triggers on every positive edge of the LFRCO clock.			
0	RDY	0x0	RW	**Ready Interrupt Flag**
	Triggers when the oscillator becomes ready			

9.6.5.5 LFRCO_IEN - Interrupt Enable Register

Offset	Bit Position																														
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x0	0x0	0x0
Access																														RW	RW	RW
Name																														NEGEDGE	POSEDGE	RDY

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	NEGEDGE	0x0	RW	**Falling Edge Interrupt Enable**
	Enables the negedge interrupt and will cause the oscillator to run. EM2 wakeup source.			
1	POSEDGE	0x0	RW	**Rising Edge Interrupt Enable**
	Enables the posedge interrupt and will cause the oscillator to run. EM2 wakeup source.			
0	RDY	0x0	RW	**Ready Interrupt Enable**
	Enables the ready interrupt. EM2 wakeup source.			

9.6.5.6 LFRCO_SYNCBUSY - Synchronization Busy Register

Offset	Bit Position																														
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																R
Name																																CAL

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	CAL	0x0	R	**CAL Busy**
	CAL register synchronization busy bit			

9.6.5.7 LFRCO_LOCK - Configuration Lock Register

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																								0x2603								
Access																								W								
Name																								LOCKKEY								

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LOCKKEY	0x2603	W	**Lock Key**

Writing the lock key will unlock the lfrco configuration registers (CAL, CTRL and TEST). Writing any other value will lock them.

Value	Mode	Description
0	LOCK	Lock Configuration Registers
9731	UNLOCK	Unlock Configuaration Registers

9.7 FSRCO - Fast Start RCO

9.7.1 Introduction

This is an RC oscillator which can start and stop very fast. It is a fixed frequency oscillator, with no frequency configurability and as such any user of this clock can rely on it being a specific frequency independent of the system state. This is the first oscillator used during power up and hence it minimizes dependency to other blocks.

9.7.2 Features

- 20 MHz nominal frequency
- Low energy consumption

9.7.3 Functional Description

There are no programmable registers in this module. Software can choose to use this as system clock in the CMU block. the only way to enable or disable the FSRCO is by requesting it as a clock source in the CMU clock select registers.

9.7.4 FSRCO Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	FSRCO_IPVERSION	R	IP Version
0x1000	FSRCO_IPVERSION_SET	R	IP Version
0x2000	FSRCO_IPVERSION_CLR	R	IP Version
0x3000	FSRCO_IPVERSION_TGL	R	IP Version

9.7.5 FSRCO Register Description

9.7.5.1 FSRCO_IPVERSION - IP Version

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x0	R	**IP Version**
				The read only IPVERSION field gives the version for this module. There may be minor software changes required for modules with different values of IPVERSION.

9.8 ULFRCO - Ultra Low Frequency RC Oscillator

9.8.1 Introduction

The ULFRCO is an ultra low power 1 kHz oscillator which is available in all energy modes. The ULFRCO is available to many low-frequency peripherals as a lower power alternative to one of the 32 kHz oscillators. This oscillator is also used for internal bias and housekeeping tasks in EM0-EM3.

9.8.2 Features

- 1 kHz nominal frequency
- Low energy consumption

9.8.3 Functional Description

There are no user programmable registers in this module. The oscillator is always on in all energy modes except EM4. In EM4, the oscillator is available on-demand by peripheral requests.

9.9 RFFPLL - Radio Frequency Friendly PLL

9.9.1 Introduction

The Radio Frequency Friendly Phase Locked Loop (RFFPLL) provides the sequence for starting up the bias circuit and the phase locked loop to provide two high frequency clocks. RFFPLLRADIO clock runs at 160 MHz, while the RFFPLLSYS clock runs at 100 MHz. It receives a 39 MHz (40 MHz) reference clock from HFXO. For radio frequency interference mitigation, the 160 MHz clock can vary within the range of 154 MHz to 166 MHz. Likewise, the 100 MHz clock can vary within the range of 100 MHz to 106 MHz.

9.9.2 Features

- Two output clocks at 160 MHz (ranging 154 MHz to 166 MHz) and 100 MHz (ranging 100 MHz to 106 MHz)
- Clocks are independently turned on based on request
- Automatically request HFXO as reference clock
- Automatically start up necessary bias circuitry
- Offers frequency planning to move the high-order frequency spur out of the receiving channel
- User lock

9.9.3 Functional Description

9.9.3.1 Enabling and Disabling

RFFPLL can be enabled and disabled via both hardware and software mechanisms. Enabling via software is done by setting the FORCEEN bit in the RFFPLL_CTRL register. Disabling via software is done by setting the DISONDEMAND bit and clearing FORCEEN bit in RFFPLL_CTRL register.

Hardware mechanism (on-demand) is given control by clearing FORCEEN and DISONDEMAND bits in the RFFPLL_CTRL register. Then, enabling via hardware can be performed by clock switch selections in the CMU.

9.9.3.2 Status Flags

The ENS flag in the RFFPLL_STATUS indicates that the RFFPLL has been enabled. Once the RFFPLL is locked, output clocks are ready for use as indicated by the RFFPLLSYSRDY (100MHz clock) and RFFPLLRADIORDY (160 MHz clock) flags in the RFFPLL_STATUS. The HWREQSYS and HWREQRADIO flags indicate that CMU clock switch is currently requesting 100 MHz and 160 MHz clocks, respectively.

9.9.3.3 Interrupts

RFFPLLSYSRDYIF and RFFPLLRADIORDYIF are interrupt flags as well as status flags. This allows software flexibility to implement interrupt service routine or polling loop for these events. When lock is achieved and 100 MHz output clock is running, sticky RFFPLLSYSRDYIF is set until they are cleared by software. Likewise, it is the same for 160 MHz output clock and RFFPLLRADIOR-DYIF

9.9.3.4 Protection

It is possible to lock the control register to prevent unintended software writes to critical clock settings. This is controlled by the RFFPLL_LOCK register. A LOCK bit is available in RFFPLL_STATUS register.

9.9.4 RFFPLL Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	RFFPLL_IPVERSION	R	IP Version ID
0x014	RFFPLL_CTRL	RW SYNC	Control Register
0x020	RFFPLL_STATUS	RH	Status Register
0x058	RFFPLL_RFFPLLCTRL1	RW	PLL Control Register 1
0x080	RFFPLL_IF	RWH INTFLAG	Interrupt Flag Register
0x084	RFFPLL_IEN	RW	Interrupt Enable Register
0x0B0	RFFPLL_LOCK	W	Configuration Lock Register
0x1000	RFFPLL_IPVERSION_SET	R	IP Version ID
0x1014	RFFPLL_CTRL_SET	RW SYNC	Control Register
0x1020	RFFPLL_STATUS_SET	RH	Status Register
0x1058	RFFPLL_RFFPLLCTRL1_SET	RW	PLL Control Register 1
0x1080	RFFPLL_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x1084	RFFPLL_IEN_SET	RW	Interrupt Enable Register
0x10B0	RFFPLL_LOCK_SET	W	Configuration Lock Register
0x2000	RFFPLL_IPVERSION_CLR	R	IP Version ID
0x2014	RFFPLL_CTRL_CLR	RW SYNC	Control Register
0x2020	RFFPLL_STATUS_CLR	RH	Status Register
0x2058	RFFPLL_RFFPLLCTRL1_CLR	RW	PLL Control Register 1
0x2080	RFFPLL_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x2084	RFFPLL_IEN_CLR	RW	Interrupt Enable Register
0x20B0	RFFPLL_LOCK_CLR	W	Configuration Lock Register
0x3000	RFFPLL_IPVERSION_TGL	R	IP Version ID
0x3014	RFFPLL_CTRL_TGL	RW SYNC	Control Register
0x3020	RFFPLL_STATUS_TGL	RH	Status Register
0x3058	RFFPLL_RFFPLLCTRL1_TGL	RW	PLL Control Register 1
0x3080	RFFPLL_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x3084	RFFPLL_IEN_TGL	RW	Interrupt Enable Register
0x30B0	RFFPLL_LOCK_TGL	W	Configuration Lock Register

9.9.5 RFFPLL Register Description

9.9.5.1 RFFPLL_IPVERSION - IP Version ID

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x1																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x1	R	**IP Version ID**
	The read only IPVERSION field gives the version for this module. There may be minor software changes required for modules with different values of IPVERSION.			

9.9.5.2 RFFPLL_CTRL - Control Register

Offset	Bit Position																															
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																								0x0							0x0	
Access																								RW							RW	
Name																								DISONDEMAND							FORCEEN	

Bit	Name	Reset	Access	Description
31:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8	DISONDEMAND	0x0	RW	**Disable On-demand request**
	Disable On Demand hardware request			
7:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	FORCEEN	0x0	RW	**Force PLL Enable**
	Force on the RFFPLL			
0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

9.9.5.3 RFFPLL_STATUS - Status Register

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0														0x0	0x0								0x0							0x0	0x0
Access	R														R	R								R							R	R
Name	LOCK														HWREQSYS	HWREQRADIO								ENS							RFFPLLSYSRDY	RFFPLLRADIORDY

Bit	Name	Reset	Access	Description
31	LOCK	0x0	R	**Configuration Lock Status**
	Indicates the current status of configuration lock.			
	Value	Mode		Description
	0	UNLOCKED		Configuration lock is unlocked
	1	LOCKED		Configuration lock is locked
30:18	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
17	HWREQSYS	0x0	R	**PLL Digital System Output Requested**
	PLL digital system clock is requested by digital system request interface.			
16	HWREQRADIO	0x0	R	**PLL Radio Output Requested**
	PLL radio clock is requested by radio request interface.			
15:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8	ENS	0x0	R	**Enabled Status**
	PLL is enabled.			
7:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	RFFPLLSYSRDY	0x0	R	**Digital System Clock Output Ready**
	Indicate that the Digital System clock is stable.			
0	RFFPLLRADIORDY	0x0	R	**Radio Clock Output Ready**
	Indicate that the Radio clock is stable.			

9.9.5.4 RFFPLL_RFFPLLCTRL1 - PLL Control Register 1

Offset	Bit Position																															
0x058	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset														0x11					0x6										0x57			
Access														RW					RW										RW			
Name														DIVY					DIVX										DIVN			

Bit	Name	Reset	Access	Description
31:21	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
20:16	DIVY	0x11	RW	**Clock Divider Ratio for digital**
	Digital clock output divider ratio. Valid range is 8 to 31. Only allowed to modify through EMLIB/Studio.			
15:12	DIVX	0x6	RW	**Clock Divider Ratio for Radio**
	Radio ADC/DAC/MODEM output divider ratio. Valid range is 4 to 15. Only allowed to modify through EMLIB/Studio.			
11:7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:0	DIVN	0x57	RW	**Feedback Divider Ratio**
	PLL feedback divider ratio. Valid range is 32 to 127. Only allowed to modify through EMLIB/Studio.			

9.9.5.5 RFFPLL_IF - Interrupt Flag Register

Offset	Bit Position																															
0x080	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															RW	RW
Name																															RFFPLLSYSRDY	RFFPLLRADIORDY

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	RFFPLLSYSRDY	0x0	RW	**Digital System Output Ready Interrupt**
	Digital System clock is stable.			
0	RFFPLLRADIORDY	0x0	RW	**Radio Output Ready Interrupt**
	Radio clock is stable			

9.9.5.6 RFFPLL_IEN - Interrupt Enable Register

Offset	Bit Position																													
0x084	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															RW	RW
Name																															RFFPLLSYSRDY	RFFPLLRADIORDY

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	RFFPLLSYSRDY	0x0	RW	**Digital System Output Ready Interrupt**
	Digital System clock is stable.			
0	RFFPLLRADIORDY	0x0	RW	**Radio Output Ready Interrupt**
	Radio clock is stable.			

9.9.5.7 RFFPLL_LOCK - Configuration Lock Register

Offset	Bit Position																													
0x0B0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x85A9															
Access																	W															
Name																	LOCKKEY															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LOCKKEY	0x85A9	W	**Configuration Lock Key**
	Write any other value than the unlock code to lock registers from editing. Write the unlock code to unlock.			

Value	Mode	Description
34217	UNLOCK	Write this value to unlock

9.10 USBPLL0 - Universal Serial Bus PLL

9.10.1 Introduction

The USBPLL0 provides an accurate (2500 ppm) 48 MHz clock to the USB from multiple HFXO input reference clock frequencies (e.g., 38 MHz, 38.4 MHz, 39 MHz, and 40 MHz). The USBPLL0 will only run in EM0 or EM1.

The USBPLL0 does not have an Enable, but uses an "always-on" concept, allowing it to be effectively enabled but not running until a clock request comes in. Two bitfields in the CTRL register may be used to change the "always-on" behavior:

- CTRL.DISONDEMAND can be used to ignore a clock request and keep the USBPLL0 in IDLE with no clock output.
- CTRL.FORCEEN can be used to override the clock request and DISONDEMAND behavior and force the USBPLL0 to run and always generate a clock.

9.10.2 Features

- Disable on demand
- Force enable
- LOCKKEY mechanism for preventing unwanted register overwrites
- USBPLL Ready interrupt
- Frequency multiplication and division controlled with DIVR, DIVX, and DIVN.
- Programmable warmup time

9.10.3 Functional Description

The USBPLL0 is used to generate an accurate 2500 ppm clock using a 38 MHz, 38.4 MHz, 39 MHz, or 40 MHz input reference clock from the external crystal. The default mode of operation is an always-on mode, where the USBPLL0 is powered but not clocking and waiting for a clock request input. For example, the USB module sends a clock request to the USBPLL0, which in turn requests a clock from the HFXO crystal. After the HFXO is ready, the USBPLL0 is able to LOCK and its output is un-gated, providing a 48 MHz clock to the USB.

9.10.4 USBPLL Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	USBPLL_IPVERSION	R	IP Version ID
0x00C	USBPLL_CTRL	RW SYNC	Control
0x010	USBPLL_STATUS	RH SYNC	Status
0x01C	USBPLL_DCOCTRL	RW	DAC Oscillator Control
0x030	USBPLL_LOCK	W	Lock PLL
0x034	USBPLL_IF	RWH INTFLAG	Interrupt Flag Register
0x038	USBPLL_IEN	RW	Interrupt Enable Register
0x1000	USBPLL_IPVERSION_SET	R	IP Version ID
0x100C	USBPLL_CTRL_SET	RW SYNC	Control
0x1010	USBPLL_STATUS_SET	RH SYNC	Status
0x101C	USBPLL_DCOCTRL_SET	RW	DAC Oscillator Control
0x1030	USBPLL_LOCK_SET	W	Lock PLL
0x1034	USBPLL_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x1038	USBPLL_IEN_SET	RW	Interrupt Enable Register
0x2000	USBPLL_IPVERSION_CLR	R	IP Version ID
0x200C	USBPLL_CTRL_CLR	RW SYNC	Control
0x2010	USBPLL_STATUS_CLR	RH SYNC	Status
0x201C	USBPLL_DCOCTRL_CLR	RW	DAC Oscillator Control
0x2030	USBPLL_LOCK_CLR	W	Lock PLL
0x2034	USBPLL_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x2038	USBPLL_IEN_CLR	RW	Interrupt Enable Register
0x3000	USBPLL_IPVERSION_TGL	R	IP Version ID
0x300C	USBPLL_CTRL_TGL	RW SYNC	Control
0x3010	USBPLL_STATUS_TGL	RH SYNC	Status
0x301C	USBPLL_DCOCTRL_TGL	RW	DAC Oscillator Control
0x3030	USBPLL_LOCK_TGL	W	Lock PLL
0x3034	USBPLL_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x3038	USBPLL_IEN_TGL	RW	Interrupt Enable Register

9.10.5 USBPLL Register Description

9.10.5.1 USBPLL_IPVERSION - IP Version ID

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x1																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x1	R	**IP Version ID**

9.10.5.2 USBPLL_CTRL - Control

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset								0xD							0x10					0x1								0x0			0x0	0x0
Access								RW							RW					RW								RW			RW	RW
Name								DIVN							DIVX					DIVR								SHUNTREGLPEN			DISONDEMAND	FORCEEN

Bit	Name	Reset	Access	Description
31:25	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
24:18	DIVN	0xD	RW	**Divider N**
	Final divider from FREQ_OUT = FREG_REF / DIVR * DIVX / DIVN. Useful values are d13(01101), d19(10011), d20(10100), and d25(11001)			
17:13	DIVX	0x10	RW	**Divider X**
	Middle divider from FREQ_OUT = FREG_REF / DIVR * DIVX / DIVN.(actually 2 separate inverter loops that form a multiplier). Useful values are d16(10000), d24(11000), and d25(11001)			
12:8	DIVR	0x1	RW	**Divider R**
	First divider from FREQ_OUT = FREG_REF / DIVR * DIVX / DIVN. Useful value is d1(00001)			
7:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	SHUNTREGLPEN	0x0	RW	**Shunt Regulator LP Enable**
	Shunt regulator LP enabble			
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DISONDEMAND	0x0	RW	**Disable on Demand**
	Disable the on demand (USBPLL clkreq input) from starting the USBPLL			
0	FORCEEN	0x0	RW	**Force Enable**
	Force the FSM to turn on the USBPLL			

9.10.5.3 USBPLL_STATUS - Status

Offset	Bit Position																															
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0													0x0	0x0																
Access	R	R													R	R																
Name	LOCK	SYNCBUSY													PLLLOCK	PLLRDY																

Bit	Name	Reset	Access	Description
31	LOCK	0x0	R	**Locks out registers**
	Configuration Lock status			
	Value	Mode		Description
	0	UNLOCKED		Configuration is unlocked
	1	LOCKED		Configuration is locked
30	SYNCBUSY	0x0	R	**Sync Busy**
	Indicates synchronization is ongoing			
29:18	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
17	PLLLOCK	0x0	R	**USBPLL is locked**
16	PLLRDY	0x0	R	**USBPLL Ready**
	USBPLL ready			
15:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

9.10.5.4 USBPLL_DCOCTRL - DAC Oscillator Control

Offset	Bit Position																														
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x1									
Access																							RW									
Name																							DCOBIASHALF									

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	DCOBIASHALF	0x1	RW	**DCO Half bias** Control scaling of current in bias. When HIGH the bias current is iref/2. (default for halfrate). When LOW the bias used is iref. (default for fullrate)

Value	Mode	Description
0	DISABLE	
1	ENABLE	

Bit	Name	Reset	Access	Description
8:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

9.10.5.5 USBPLL_LOCK - Lock PLL

Offset	Bit Position																														
0x030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x580E															
Access																	W															
Name																	LOCKKEY															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LOCKKEY LOCKKEY	0x580E	W	**Configuration Lock Key**

Value	Mode	Description
22542	UNLOCK	Write this value to unlock

9.10.5.6 USBPLL_IF - Interrupt Flag Register

Offset	Bit Position																														
0x034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x0	0x0	0x0
Access																														RW	RW	RW
Name																														PLLNOLOCKIF	PLLLOCKIF	PLLRDY

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	PLLNOLOCKIF	0x0	RW	**USBPLL Loss of Lock Interrupt Flag**
	Set when USBPLL has lost lock.			
1	PLLLOCKIF	0x0	RW	**USBPLL Lock Interrupt Flag**
	Set when USBPLL is locked.			
0	PLLRDY	0x0	RW	**USBPLL Ready Interrupt Flag**
	Set when USBPLL is ready.			

9.10.5.7 USBPLL_IEN - Interrupt Enable Register

Offset	Bit Position																														
0x038	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x0	0x0	0x0
Access																														RW	RW	RW
Name																														PLLNOLOCKIEN	PLLLOCKIEN	PLLRDY

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	PLLNOLOCKIEN	0x0	RW	**USBPLL Loss of Lock Interrupt Enable**
	USBPLL Loss of Lock Interrupt Enable			
1	PLLLOCKIEN	0x0	RW	**USBPLL Lock Interrupt Enable**
	USBPLL Lock Interrupt Enable			
0	PLLRDY	0x0	RW	**USBPLL Ready Interrupt Enable**
	USBPLL Ready Interrupt Enable			

10. SMU - Security Management Unit



Quick Facts

What?

The Security Management Unit (SMU) provides configuration and status reporting for ARM TrustZone on the EFR32xG25.

Why?

Enables a robust solution at the system level.

How?

Hardware context switching and enhanced security provided by ARM TrustZone. Extension of the ARM MPU to control peripheral access.

10.1 Introduction

The Security Management Unit is used to configure and extend TrustZone bus level security provided by the Cortex-M33. In addition it increases the effective MPU regions by providing MPU control over peripheral access.

10.2 Features

- Per peripheral privileged and secure attributes
- Per manager privileged and secure attributes
- Separate interrupt flags for privileged, secure, or instruction access exceptions.
- Separate interrupt flag for secure manager access exceptions
- Secure and Privileged exception IRQs
- Configurable secure, non-secure, and non-secure-callable memory regions.

10.3 Functional Description

10.3.1 Bus Level Security

Bus level security is the ability to control the flow of information on the device. The components of bus level security are the Cortex-M33, the Bus Manager Protect Unit (BMPU), and the Peripheral Protection Unit (PPU) as highlighted in Figure 10.1 Bus Level Security Implementation on page 280. The SMU controls and configures all the components used in bus level security.

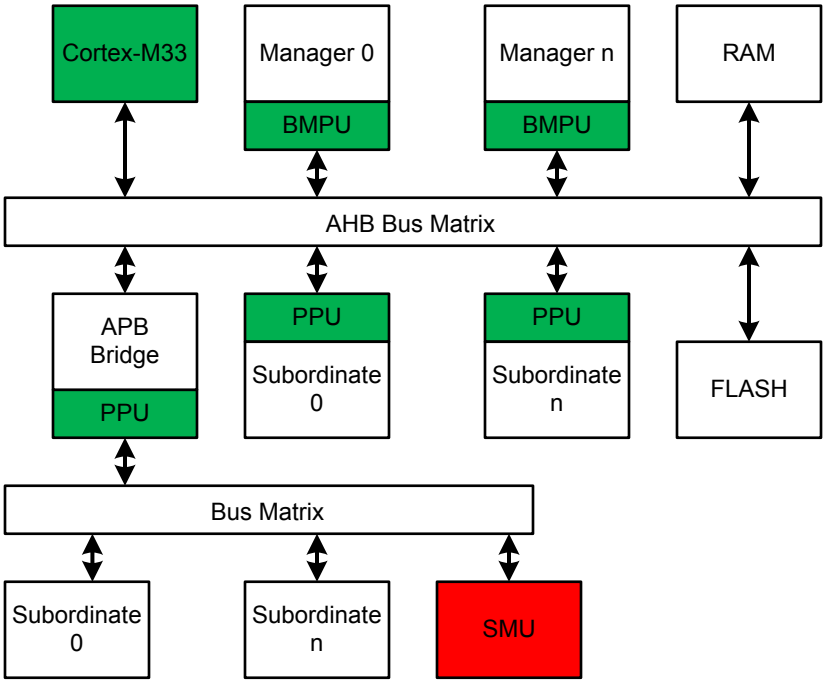


Figure 10.1. Bus Level Security Implementation

The BMPU is responsible for preventing managers (CPU, DMA, Etc..) from accessing secure addresses without authorization. For example, if a DMA configured as non-secure tries to access memory that is marked secure the BMPU will prevent access and set the corresponding interrupt flag. The BMPU prevents access of secure addresses by non-secure managers. The Cortex-M33 has BMPU functionality built into the TrustZone implementation.

The PPU is primarily responsible for blocking access to privileged peripherals from unprivileged managers. In addition, it also ensures that secure and non-secure peripherals are only accessible at the appropriate secure or non-secure addresses as described in 10.3.6 Configuring Peripherals.

Since FLASH and RAM have no PPU, bus managers of any privilege state may access those resources. The Cortex-M33 has an MPU which prevents execution of privileged memory when the CPU is in an unprivileged state. For more information on the MPU refer to the ARM Cortex-M33 documentation.

10.3.2 Privileged Access Control

The Cortex-M33 and all other managers can be in either the privileged or unprivileged state. All bus access to peripherals are tested for privilege level by the PPU and resolved as shown in Table 10.1 Privileged Access Table on page 281.

If an exception is detected on a write, the write will be ignored and the appropriate interrupt flag set. If an exception is detected on a read 0x0 will be returned and the appropriate interrupt flag set.

Table 10.1. Privileged Access Table

Manager Attribute	Peripheral Attribute	Result
privileged	privileged	Success
privileged	unprivileged	Success
unprivileged	privileged	Exception
unprivileged	unprivileged	Success

10.3.3 Secure Access Control

The Cortex-M33 and all other managers can be in either the secure or non-secure state. All bus accesses are tested for security status by the BMPUs and PPUs and resolve as shown in Table 10.2 Secure Access Table on page 281 Secure access is computed using the secure attribute of the manager and the address region being accessed. If a peripheral is being accessed, the secure attribute of the peripheral is also used. For more information on the relationship between the address regions and peripheral security attributes please see 10.3.6 Configuring Peripherals

If an exception is detected on a write the write will be ignored and the appropriate interrupt flag set. If an exception is detected on a read 0x0 will be returned and the appropriate interrupt flag set.

Table 10.2. Secure Access Table

Manager Attribute	Address Attribute	Peripheral Attribute	Result
secure	secure	N/A	Success
secure	secure	secure	Success
secure	secure	non-secure	Exception
secure	non-secure	N/A	Exception
secure	non-secure	secure	Exception
secure	non-secure	non-secure	Success
non-secure	secure	N/A	Exception
non-secure	secure	secure	Exception
non-secure	secure	non-secure	Exception
non-secure	non-secure	N/A	Success
non-secure	non-secure	secure	Exception
non-secure	non-secure	non-secure	Success

10.3.4 ARM TrustZone

ARM TrustZone is used to control what addresses are accessible by the CPU at any given time. There are two security states: secure and non-secure. In addition the MPU provides two privilege levels: privileged and unprivileged. This results in 4 possible states: secure-privileged, non-secure-privileged, secure-unprivileged and non-secure-unprivileged.

Non-secure code may not directly call secure code. To call secure code, non-secure code must first call a shim located in specially marked non-secure-callable memory. Unprivileged code may invoke privileged code and change the processor state to privileged by either issuing an SVC instruction or taking an interrupt. The processor is returned to unprivileged state when software manually reconfigures the security state or exits an interrupt.

For more information on secure/non-secure and privileged/unprivileged state transitions see the ARM Cortex-M33 documentation.

There are two primary use cases for TrustZone and the MPU. The first is simply partitioning a monolithic application in to the 4 states to protect some pieces of the system from bugs or attacks on others. The second is to use a RTOS to isolate several tasks from each other. In this case the RTOS itself normally consumes the privileged states with all other code running in the unprivileged states. Whenever a task switch occurs the RTOS can reconfigure the device so the new task has access to only the components it requires, protecting other tasks from interference.

In both use cases the TrustZone and MPU feature of the Cortex-M33 both secures and accelerates mode transitions while the SMU provides the ability to configure the security and privilege attributes of peripherals and memory.

The core is in secure-privileged state after a reset.

10.3.5 Configuring Managers

The SMU provides the ability to configure the current secure and privileged attribute of all bus managers except for the CPU which is controlled as described in 10.3.4 ARM TrustZone.

To configure the privileged attribute of a manager set the appropriate bit in SMU_BMPUPATDn. To configure the secure attribute of a manager set the appropriate bit in SMU_BMPUPSATDn.

10.3.6 Configuring Peripherals

The SMU provides the ability to configure the current secure and privileged state of all peripherals. To configure the privileged attribute of a peripheral set the appropriate bit in SMU_PPUPATDn.

Each peripheral is accessible at one of two addresses: A secure address and an non-secure address. Which address is valid depends on the security attribute of the peripheral configured in the SMU. When configured as secure a peripheral may only be accessed at its secure address and when configured as non-secure the peripheral may only be accessed at its non-secure address. This forces code to be aware of the security attribute of the peripheral being accessed, preventing secure code from accessing a non-secure peripheral unintentionally.

The device memory map contains 4 regions of fixed length and fixed security attribute to facilitate the secure access of peripherals and RF peripherals. There is one secure (0x40000000) and one non-secure (0x50000000) region for peripherals and one secure (0xA0000000) and non-secure (0xB0000000) region for the radio subsystem. While each peripheral can be configured independently the radio subsystem is configured as a unit.

To configure the security attribute of a peripheral set the appropriate bit in SMU_PPUSATDn.

10.3.7 Configuring Memory

The SMU provides the ability to configure the security attribute of memory. There are 13 configurable regions in total. There are three regions in FLASH (0 - 2) and three in RAM (4-6) which have pre-determined secure attributes and user selectable sizes. Regions 3 and 11 cover the flash info page and ARM EPPB space respectively and have a fixed size. These regions can be configured as secure or non-secure by setting ESAUR3NS in SMU_ESAURTYPES0 and ESAUR11NS in SMU_ESAURTYPES1 respectively.

The size of the FLASH and RAM regions are controlled by the SMU_ESAUMRBRxy registers as shown in Table 10.3 Memory Configuration Regions on page 283. Region sizes are adjusted in 4 kB increments with the lower 12 bits of SMU_ESAUMRBRxy ignored. The non-secure-callable regions may be set to size 0 but secure and non-secure regions must be at least 4 kB.

Table 10.3. Memory Configuration Regions

Region	Memory	Attributes	Start	End
0	FLASH	secure	0x00000000	SMU_ESAUMRBR01-1
1	FLASH	non-secure-callable	SMU_ESAUMRBR01	SMU_ESAUMRBR12-1
2	FLASH	non-secure	SMU_ESAUMRBR12	0x0FDFFFFF
3	FLASH (info page)	secure or non-secure	0x0FE00000	0x0FFFFFFF
4	RAM	secure	0x20000000	SMU_ESAUMRBR45-1
5	RAM	non-secure-callable	SMU_ESAUMRBR45	SMU_ESAUMRBR56-1
6	RAM	non-secure	SMU_ESAUMRBR56	0x2FFFFFFF
7	Peripherals	secure	0x40000000	0x4FFFFFFF
8	Peripherals	non-secure	0x50000000	0x5FFFFFFF
9	SEQRAM/ FRCRAM	secure	0xA0000000	0xAFFFFFFF
10	SEQRAM/ FRCRAM	non-secure	0xB0000000	0xBFFFFFFF
11	EPPB	secure or non-secure	0xE0044000	0xE00FDFFF
12	Cortex-M33 Processor ROM table	exempt	0xE00FE000	0xE00FEFFF

10.3.8 Cortex-M33 Integration

In addition to the SMU based access controls the Cortex-M33 has additional security features for controlling both secure and privileged access.

The Security Attribution Unit (SAU) provides that ability to setup secure memory regions in addition to those configured by the SMU. To disable the SAU and rely entirely on the SMU for security management clear ENABLE and set ALLNS in the SAU CTRL register. To enable a combination of SMU and SAU control set ENABLE in the SAU CTRL register. If both ENABLE and ALLNS are cleared all Cortex-M33 will treat all transactions as secure.

When both SAU and SMU are in use, a memory address is considered secure if either the SAU or SMU have it configured as secure. When enabled the SAU applies ONLY to access by the Cortex-M33 and does not effect any other managers. For more information on the SAU refer to ARM documentation.

Note: It is highly recommended that systems avoid using the SAU unless necessary. Since the SAU does not affect any managers outside the Cortex-M33, extreme care must be taken to ensure the SAU regions can not be trivially by bypassed through use of another manager such as the DMA.

In addition to the Cortex-M33 MPU provides the ability to control which regions of FLASH and RAM are marked as privileged and prevent execution of privileged code by a CPU in unprivileged state. For more information on the configuration and use of the MPU refer to ARM documentation.

10.3.9 Exception Handling

When a BMPU detects a non-secure manager attempting to access a secure address, the BMPUSECIF in SMU_IF is set and the ID of the Manager block is written to SMU_BMPUFS. If BMPUSECIEN is set and the SMU's Secure IRQ enabled, the CPU will be interrupted.

When a PPU detects an access to a secure peripheral at its non-secure address or an access to a non-secure peripheral at its secure address, PPUSECIF in SMU_IF is set and the ID of the peripheral being accessed is written to SMU_PPUFS. If PPUSECIEN is set and the SMU's Secure IRQ enabled, the CPU will be interrupted.

If a PPU detects an attempt to fetch an instruction from a peripheral, PPUINSTIF in SMU_IF will be set and the ID of the peripheral being accessed is written to SMU_PPUFS. If PPUINSTIEN is set and the SMU's Privileged IRQ enabled, the CPU will be interrupted.

If a PPU detects an attempt to access a privileged peripheral by an unprivileged manager, PPUPRIVIF in SMU_IF will be set and the ID of the peripheral being accessed is written to SMU_PPUFS. If PPUPRIVIEN is set and the SMU's Privileged IRQ enabled, the CPU will be interrupted.

When any IRQ is trigged the Cortex-M33 is automatically placed in the privileged state. The security state is determined by configuration inside the Cortex-M33. Refer to ARM's documentation for more details.

If the SMU is configured in an inconsistent way, the SMUPRGERR flag in SMU_STATUS will be set. One example of an invalid configuration is setting SMU_ESAUMRBR01 to a value larger than SMU_ESAUMRBR23. SMUPRGERR should be checked after the SMU is configured.

10.3.10 SMU Lock

The SMU registers can be locked to prevent unintended modifications. SMULOCK in SMU_STATUS indicates if the SMU is currently locked. To unlock the SMU write 0xACCE55 to the SMU_LOCK register. To lock write any other value to SMU_LOCK.

In addition to locking the SMU registers the SMU can prevent access to the Cortex-M33 ASU, MPU, SMPU, VTOR and VTAIRCR registers. To lock access to one or more of these blocks set the corresponding bit in SMU_M33CTRL.

10.4 SMU Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	SMU_IPVERSION	R	IP Version
0x004	SMU_STATUS	RH	Status Register
0x008	SMU_LOCK	W	Lock Register
0x00C	SMU_IF	RWH INTFLAG	Interrupt Flag Register
0x010	SMU_IEN	RW	Interrupt Enable Register
0x020	SMU_M33CTRL	RW	M33 Control Settings
0x040	SMU_PPUPATD0	RW	Privileged Access
0x044	SMU_PPUPATD1	RW	Privileged Access
0x060	SMU_PPUSATD0	RW	Secure Access
0x064	SMU_PPUSATD1	RW	Secure Access
0x140	SMU_PPUFS	RH	Fault Status
0x150	SMU_BMPUPATD0	RW	Privileged Attribute
0x170	SMU_BMPUSATD0	RW	Secure Attribute
0x250	SMU_BMPUFS	RH	Fault Status
0x254	SMU_BMPUFSADDR	RH	Fault Status Address
0x260	SMU_ESAURTYPES0	RW	Region Types 0
0x264	SMU_ESAURTYPES1	RW	Region Types 1
0x270	SMU_ESAUMRB01	RW	Movable Region Boundary
0x274	SMU_ESAUMRB12	RW	Movable Region Boundary
0x280	SMU_ESAUMRB45	RW	Movable Region Boundary
0x284	SMU_ESAUMRB56	RW	Movable Region Boundary
0x1000	SMU_IPVERSION_SET	R	IP Version
0x1004	SMU_STATUS_SET	RH	Status Register
0x1008	SMU_LOCK_SET	W	Lock Register
0x100C	SMU_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x1010	SMU_IEN_SET	RW	Interrupt Enable Register
0x1020	SMU_M33CTRL_SET	RW	M33 Control Settings
0x1040	SMU_PPUPATD0_SET	RW	Privileged Access
0x1044	SMU_PPUPATD1_SET	RW	Privileged Access
0x1060	SMU_PPUSATD0_SET	RW	Secure Access
0x1064	SMU_PPUSATD1_SET	RW	Secure Access
0x1140	SMU_PPUFS_SET	RH	Fault Status
0x1150	SMU_BMPUPATD0_SET	RW	Privileged Attribute
0x1170	SMU_BMPUSATD0_SET	RW	Secure Attribute
0x1250	SMU_BMPUFS_SET	RH	Fault Status

Offset	Name	Type	Description
0x1254	SMU_BMPUFSADDR_SET	RH	Fault Status Address
0x1260	SMU_ESAURTYPES0_SET	RW	Region Types 0
0x1264	SMU_ESAURTYPES1_SET	RW	Region Types 1
0x1270	SMU_ESAUMRB01_SET	RW	Movable Region Boundary
0x1274	SMU_ESAUMRB12_SET	RW	Movable Region Boundary
0x1280	SMU_ESAUMRB45_SET	RW	Movable Region Boundary
0x1284	SMU_ESAUMRB56_SET	RW	Movable Region Boundary
0x2000	SMU_IPVERSION_CLR	R	IP Version
0x2004	SMU_STATUS_CLR	RH	Status Register
0x2008	SMU_LOCK_CLR	W	Lock Register
0x200C	SMU_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x2010	SMU_IEN_CLR	RW	Interrupt Enable Register
0x2020	SMU_M33CTRL_CLR	RW	M33 Control Settings
0x2040	SMU_PPUPATD0_CLR	RW	Privileged Access
0x2044	SMU_PPUPATD1_CLR	RW	Privileged Access
0x2060	SMU_PPUSATD0_CLR	RW	Secure Access
0x2064	SMU_PPUSATD1_CLR	RW	Secure Access
0x2140	SMU_PPUFS_CLR	RH	Fault Status
0x2150	SMU_BMPUPATD0_CLR	RW	Privileged Attribute
0x2170	SMU_BMPUSATD0_CLR	RW	Secure Attribute
0x2250	SMU_BMPUFS_CLR	RH	Fault Status
0x2254	SMU_BMPUFSADDR_CLR	RH	Fault Status Address
0x2260	SMU_ESAURTYPES0_CLR	RW	Region Types 0
0x2264	SMU_ESAURTYPES1_CLR	RW	Region Types 1
0x2270	SMU_ESAUMRB01_CLR	RW	Movable Region Boundary
0x2274	SMU_ESAUMRB12_CLR	RW	Movable Region Boundary
0x2280	SMU_ESAUMRB45_CLR	RW	Movable Region Boundary
0x2284	SMU_ESAUMRB56_CLR	RW	Movable Region Boundary
0x3000	SMU_IPVERSION_TGL	R	IP Version
0x3004	SMU_STATUS_TGL	RH	Status Register
0x3008	SMU_LOCK_TGL	W	Lock Register
0x300C	SMU_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x3010	SMU_IEN_TGL	RW	Interrupt Enable Register
0x3020	SMU_M33CTRL_TGL	RW	M33 Control Settings
0x3040	SMU_PPUPATD0_TGL	RW	Privileged Access
0x3044	SMU_PPUPATD1_TGL	RW	Privileged Access
0x3060	SMU_PPUSATD0_TGL	RW	Secure Access

Offset	Name	Type	Description
0x3064	SMU_PPUSATD1_TGL	RW	Secure Access
0x3140	SMU_PPUFS_TGL	RH	Fault Status
0x3150	SMU_BMPUPATD0_TGL	RW	Privileged Attribute
0x3170	SMU_BMPUSATD0_TGL	RW	Secure Attribute
0x3250	SMU_BMPUFS_TGL	RH	Fault Status
0x3254	SMU_BMPUFSADDR_TGL	RH	Fault Status Address
0x3260	SMU_ESAURTYPES0_TGL	RW	Region Types 0
0x3264	SMU_ESAURTYPES1_TGL	RW	Region Types 1
0x3270	SMU_ESAUMRB01_TGL	RW	Movable Region Boundary
0x3274	SMU_ESAUMRB12_TGL	RW	Movable Region Boundary
0x3280	SMU_ESAUMRB45_TGL	RW	Movable Region Boundary
0x3284	SMU_ESAUMRB56_TGL	RW	Movable Region Boundary

10.5 SMU Register Description

10.5.1 SMU_IPVERSION - IP Version

Offset	Bit Position																													
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x4																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x4	R	**IP Version**
	The read only IPVERSION field gives the version for this module. There may be minor software changes required for modules with different values of IPVERSION.			

10.5.2 SMU_STATUS - Status Register

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	R
Name																															SMUPRGERR	SMULOCK

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	SMUPRGERR	0x0	R	**SMU Programming Error**
	Indicates if SMU Registers were programmed incorrectly.			
0	SMULOCK	0x0	R	**SMU Lock**
	Indicates if SMU Registers are locked.			

Value	Mode	Description
0	UNLOCKED	
1	LOCKED	

10.5.3 SMU_LOCK - Lock Register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset									0x0																							
Access									W																							
Name									SMULOCKKEY																							

Bit	Name	Reset	Access	Description
31:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:0	SMULOCKKEY	0x0	W	
	Write anything but UNLOCK to lock registers.			

Value	Mode	Description
11325013	UNLOCK	Unlocks Registers

10.5.4 SMU_IF - Interrupt Flag Register

Offset	Bit Position																														
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset															0x0	0x0														0x0		0x0
Access															RW	RW														RW		RW
Name															BMPUSEC	PPUSEC														PPUINST		PPUPRIV

Bit	Name	Reset	Access	Description
31:18	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
17	BMPUSEC	0x0	RW	**BMPU Security Interrupt Flag**
	Triggered when a security fault occurs in the Bus Manager Protection Unit			
16	PPUSEC	0x0	RW	**PPU Security Interrupt Flag**
	Triggered when a security fault occurs in the Peripheral Protection Unit			
15:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	PPUINST	0x0	RW	**PPU Instruction Interrupt Flag**
	Triggered when a instruction fault occurs in the Peripheral Protection Unit			
1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	PPUPRIV	0x0	RW	**PPU Privilege Interrupt Flag**
	Triggered when a privilege fault occurs in the Peripheral Protection Unit			

10.5.5 SMU_IEN - Interrupt Enable Register

Offset	Bit Position																														
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset															0x0	0x0														0x0		0x0
Access															RW	RW														RW		RW
Name															BMPUSEC	PPUSEC														PPUINST		PPUPRIV

Bit	Name	Reset	Access	Description
31:18	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
17	BMPUSEC	0x0	RW	**BMPU Security Interrupt Enable**
	Set to enable the BMPUSECIF Interrupt			
16	PPUSEC	0x0	RW	**PPU Security Interrupt Enable**
	Set to enable the PPUSECIF Interrupt			
15:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	PPUINST	0x0	RW	**PPU Instruction Interrupt Enable**
	Set to enable the PPUINSTIF Interrupt			
1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	PPUPRIV	0x0	RW	**PPU Privilege Interrupt Enable**
	Set to enable the PPUPRIVIF Interrupt			

10.5.6 SMU_M33CTRL - M33 Control Settings

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												RW	RW	RW	RW	RW
Name																												LOCKSAU	LOCKNSMPU	LOCKSMPU	LOCKNSVTOR	LOCKSVTAIRCR

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	LOCKSAU	0x0	RW	**New BitField**
	Set to 1 lock security attribution unit			
3	LOCKNSMPU	0x0	RW	**New BitField**
	Set to 1 lock non-secure MPU configuration			
2	LOCKSMPU	0x0	RW	**New BitField**
	Set to 1 lock secure MPU configuration			
1	LOCKNSVTOR	0x0	RW	**New BitField**
	Set to 1 lock non-secure VTOR			
0	LOCKSVTAIRCR	0x0	RW	**New BitField**
	Set to 1 lock secure VTAIRCR			

10.5.7 SMU_PPUPATD0 - Privileged Access

Offset	Bit Position																															
0x040	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name	HOSTMAILBOX	DCDC	GPCRC	BURAM	SYSCFG	SYSCFGCFGNS	CHIPTESTCTRL	I2C1	BURTC	TIMER7	TIMER6	TIMER5	TIMER4	TIMER3	TIMER2	TIMER1	TIMER0	LDMAXBAR	LDMA	GPIO	PRS	ICACHE0	MSC	ULFRCO	LFRCO	LFXO	DPLL0	FSRCO	HFRCO0	CMU	EMU	SCRATCHPAD

Bit	Name	Reset	Access	Description
31	HOSTMAILBOX	0x1	RW	**HOSTMAILBOX Privileged Access**
	HOSTMAILBOX Privileged Access			
30	DCDC	0x1	RW	**DCDC Privileged Access**
	DCDC Privileged Access			
29	GPCRC	0x1	RW	**GPCRC Privileged Access**
	GPCRC Privileged Access			
28	BURAM	0x1	RW	**BURAM Privileged Access**
	BURAM Privileged Access			
27	SYSCFG	0x1	RW	**SYSCFG Privileged Access**
	SYSCFG Privileged Access			
26	SYSCFGCFGNS	0x1	RW	**SYSCFGCFGNS Privileged Access**
	SYSCFGCFGNS Privileged Access			
25	CHIPTESTCTRL	0x1	RW	**CHIPTESTCTRL Privileged Access**
	CHIPTESTCTRL Privileged Access			
24	I2C1	0x1	RW	**I2C1 Privileged Access**
	I2C1 Privileged Access			
23	BURTC	0x1	RW	**BURTC Privileged Access**
	BURTC Privileged Access			
22	TIMER7	0x1	RW	**TIMER7 Privileged Access**
	TIMER7 Privileged Access			
21	TIMER6	0x1	RW	**TIMER6 Privileged Access**
	TIMER6 Privileged Access			
20	TIMER5	0x1	RW	**TIMER5 Privileged Access**
	TIMER5 Privileged Access			
19	TIMER4	0x1	RW	**TIMER4 Privileged Access**
	TIMER4 Privileged Access			
18	TIMER3	0x1	RW	**TIMER3 Privileged Access**

Bit	Name	Reset	Access	Description
	TIMER3 Privileged Access			
17	TIMER2	0x1	RW	**TIMER2 Privileged Access**
	TIMER2 Privileged Access			
16	TIMER1	0x1	RW	**TIMER1 Privileged Access**
	TIMER1 Privileged Access			
15	TIMER0	0x1	RW	**TIMER0 Privileged Access**
	TIMER0 Privileged Access			
14	LDMAXBAR	0x1	RW	**LDMAXBAR Privileged Access**
	LDMAXBAR Privileged Access			
13	LDMA	0x1	RW	**LDMA Privileged Access**
	LDMA Privileged Access			
12	GPIO	0x1	RW	**GPIO Privileged Access**
	GPIO Privileged Access			
11	PRS	0x1	RW	**PRS Privileged Access**
	PRS Privileged Access			
10	ICACHE0	0x1	RW	**ICACHE0 Privileged Access**
	ICACHE0 Privileged Access			
9	MSC	0x1	RW	**MSC Privileged Access**
	MSC Privileged Access			
8	ULFRCO	0x1	RW	**ULFRCO Privileged Access**
	ULFRCO Privileged Access			
7	LFRCO	0x1	RW	**LFRCO Privileged Access**
	LFRCO Privileged Access			
6	LFXO	0x1	RW	**LFXO Privileged Access**
	LFXO Privileged Access			
5	DPLL0	0x1	RW	**DPLL0 Privileged Access**
	DPLL0 Privileged Access			
4	FSRCO	0x1	RW	**FSRCO Privileged Access**
	FSRCO Privileged Access			
3	HFRCO0	0x1	RW	**HFRCO0 Privileged Access**
	HFRCO0 Privileged Access			
2	CMU	0x1	RW	**CMU Privileged Access**
	CMU Privileged Access			
1	EMU	0x1	RW	**EMU Privileged Access**
	EMU Privileged Access			
0	SCRATCHPAD	0x1	RW	**SCRATCHPAD Privileged Access**
	SCRATCHPAD Privileged Access			

10.5.8 SMU_PPUPATD1 - Privileged Access

Offset	Bit Position																															
0x044	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset			0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1
Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name			AHBRADIO	SEMAILBOX	EUSART0	WDOG1	WDOG0	I2C0	HFXO0	HFRCO1	LESENSE	PCNT	VDAC0	AMUXCP0	ACMP1	ACMP0	IADC0	LETIMER0	AHBUSBSYS	SMUCFGNS	SMU	RADIOAES	BUFC	ETAMPDET	RFFPLL0	PFMXPPRF	DMEM	SYSRTC	EUSART4	EUSART3	EUSART2	EUSART1

Bit	Name	Reset	Access	Description
31:30	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
29	AHBRADIO	0x1	RW	**AHBRADIO Privileged Access**
	AHBRADIO Privileged Access			
28	SEMAILBOX	0x1	RW	**SEMAILBOX Privileged Access**
	SEMAILBOX Privileged Access			
27	EUSART0	0x1	RW	**EUSART0 Privileged Access**
	EUSART0 Privileged Access			
26	WDOG1	0x1	RW	**WDOG1 Privileged Access**
	WDOG1 Privileged Access			
25	WDOG0	0x1	RW	**WDOG0 Privileged Access**
	WDOG0 Privileged Access			
24	I2C0	0x1	RW	**I2C0 Privileged Access**
	I2C0 Privileged Access			
23	HFXO0	0x1	RW	**HFXO0 Privileged Access**
	HFXO0 Privileged Access			
22	HFRCO1	0x1	RW	**HFRCO1 Privileged Access**
	HFRCO1 Privileged Access			
21	LESENSE	0x1	RW	**LESENSE Privileged Access**
	LESENSE Privileged Access			
20	PCNT	0x1	RW	**PCNT Privileged Access**
	PCNT Privileged Access			
19	VDAC0	0x1	RW	**VDAC0 Privileged Access**
	VDAC0 Privileged Access			
18	AMUXCP0	0x1	RW	**AMUXCP0 Privileged Access**
	AMUXCP0 Privileged Access			
17	ACMP1	0x1	RW	**ACMP1 Privileged Access**
	ACMP1 Privileged Access			

Bit	Name	Reset	Access	Description
16	ACMP0	0x1	RW	**ACMP0 Privileged Access**
	ACMP0 Privileged Access			
15	IADC0	0x1	RW	**IADC0 Privileged Access**
	IADC0 Privileged Access			
14	LETIMER0	0x1	RW	**LETIMER0 Privileged Access**
	LETIMER0 Privileged Access			
13	AHBUSBSYS	0x1	RW	**AHBUSBSYS Privileged Access**
	AHBUSBSYS Privileged Access			
12	SMUCFGNS	0x1	RW	**SMUCFGNS Privileged Access**
	SMUCFGNS Privileged Access			
11	SMU	0x1	RW	**SMU Privileged Access**
	SMU Privileged Access			
10	RADIOAES	0x1	RW	**RADIOAES Privileged Access**
	RADIOAES Privileged Access			
9	BUFC	0x1	RW	**BUFC Privileged Access**
	BUFC Privileged Access			
8	ETAMPDET	0x1	RW	**ETAMPDET Privileged Access**
	ETAMPDET Privileged Access			
7	RFFPLL0	0x1	RW	**RFFPLL0 Privileged Access**
	RFFPLL0 Privileged Access			
6	PFMXPPRF	0x1	RW	**PFMXPPRF Privileged Access**
	PFMXPPRF Privileged Access			
5	DMEM	0x1	RW	**DMEM Privileged Access**
	DMEM Privileged Access			
4	SYSRTC	0x1	RW	**SYSRTC Privileged Access**
	SYSRTC Privileged Access			
3	EUSART4	0x1	RW	**EUSART4 Privileged Access**
	EUSART4 Privileged Access			
2	EUSART3	0x1	RW	**EUSART3 Privileged Access**
	EUSART3 Privileged Access			
1	EUSART2	0x1	RW	**EUSART2 Privileged Access**
	EUSART2 Privileged Access			
0	EUSART1	0x1	RW	**EUSART1 Privileged Access**
	EUSART1 Privileged Access			

10.5.9 SMU_PPUSATD0 - Secure Access

Offset	Bit Position																															
0x060	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name	HOSTMAILBOX	DCDC	GPCRC	BURAM	SYSCFG	SYSCFGCFGNS	CHIPTESTCTRL	I2C1	BURTC	TIMER7	TIMER6	TIMER5	TIMER4	TIMER3	TIMER2	TIMER1	TIMER0	LDMAXBAR	LDMA	GPIO	PRS	ICACHE0	MSC	ULFRCO	LFRCO	LFXO	DPLL0	FSRCO	HFRCO0	CMU	EMU	SCRATCHPAD

Bit	Name	Reset	Access	Description
31	HOSTMAILBOX	0x1	RW	**HOSTMAILBOX Secure Access**
	HOSTMAILBOX Secure Access			
30	DCDC	0x1	RW	**DCDC Secure Access**
	DCDC Secure Access			
29	GPCRC	0x1	RW	**GPCRC Secure Access**
	GPCRC Secure Access			
28	BURAM	0x1	RW	**BURAM Secure Access**
	BURAM Secure Access			
27	SYSCFG	0x1	RW	**SYSCFG Secure Access**
	SYSCFG Secure Access			
26	SYSCFGCFGNS	0x1	RW	**SYSCFGCFGNS Secure Access**
	SYSCFGCFGNS Secure Access			
25	CHIPTESTCTRL	0x1	RW	**CHIPTESTCTRL Secure Access**
	CHIPTESTCTRL Secure Access			
24	I2C1	0x1	RW	**I2C1 Secure Access**
	I2C1 Secure Access			
23	BURTC	0x1	RW	**BURTC Secure Access**
	BURTC Secure Access			
22	TIMER7	0x1	RW	**TIMER7 Secure Access**
	TIMER7 Secure Access			
21	TIMER6	0x1	RW	**TIMER6 Secure Access**
	TIMER6 Secure Access			
20	TIMER5	0x1	RW	**TIMER5 Secure Access**
	TIMER5 Secure Access			
19	TIMER4	0x1	RW	**TIMER4 Secure Access**
	TIMER4 Secure Access			
18	TIMER3	0x1	RW	**TIMER3 Secure Access**

Bit	Name	Reset	Access	Description
	TIMER3 Secure Access			
17	TIMER2	0x1	RW	**TIMER2 Secure Access**
	TIMER2 Secure Access			
16	TIMER1	0x1	RW	**TIMER1 Secure Access**
	TIMER1 Secure Access			
15	TIMER0	0x1	RW	**TIMER0 Secure Access**
	TIMER0 Secure Access			
14	LDMAXBAR	0x1	RW	**LDMAXBAR Secure Access**
	LDMAXBAR Secure Access			
13	LDMA	0x1	RW	**LDMA Secure Access**
	LDMA Secure Access			
12	GPIO	0x1	RW	**GPIO Secure Access**
	GPIO Secure Access			
11	PRS	0x1	RW	**PRS Secure Access**
	PRS Secure Access			
10	ICACHE0	0x1	RW	**ICACHE0 Secure Access**
	ICACHE0 Secure Access			
9	MSC	0x1	RW	**MSC Secure Access**
	MSC Secure Access			
8	ULFRCO	0x1	RW	**ULFRCO Secure Access**
	ULFRCO Secure Access			
7	LFRCO	0x1	RW	**LFRCO Secure Access**
	LFRCO Secure Access			
6	LFXO	0x1	RW	**LFXO Secure Access**
	LFXO Secure Access			
5	DPLL0	0x1	RW	**DPLL0 Secure Access**
	DPLL0 Secure Access			
4	FSRCO	0x1	RW	**FSRCO Secure Access**
	FSRCO Secure Access			
3	HFRCO0	0x1	RW	**HFRCO0 Secure Access**
	HFRCO0 Secure Access			
2	CMU	0x1	RW	**CMU Secure Access**
	CMU Secure Access			
1	EMU	0x1	RW	**EMU Secure Access**
	EMU Secure Access			
0	SCRATCHPAD	0x1	RW	**SCRATCHPAD Secure Access**
	SCRATCHPAD Secure Access			

10.5.10 SMU_PPUSATD1 - Secure Access

Offset	Bit Position																															
0x064	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset			0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1
Access			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name			AHBRADIO	SEMAILBOX	EUSART0	WDOG1	WDOG0	I2C0	HFXO0	HFRCO1	LESENSE	PCNT	VDAC0	AMUXCP0	ACMP1	ACMP0	IADC0	LETIMER0	AHBUSBSYS	SMUCFGNS	SMU	RADIOAES	BUFC	ETAMPDET	RFFPLL0	PFMXPPRF	DMEM	SYSRTC	EUSART4	EUSART3	EUSART2	EUSART1

Bit	Name	Reset	Access	Description
31:30	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
29	AHBRADIO	0x1	RW	**AHBRADIO Secure Access**
	AHBRADIO Secure Access			
28	SEMAILBOX	0x1	RW	**SEMAILBOX Secure Access**
	SEMAILBOX Secure Access			
27	EUSART0	0x1	RW	**EUSART0 Secure Access**
	EUSART0 Secure Access			
26	WDOG1	0x1	RW	**WDOG1 Secure Access**
	WDOG1 Secure Access			
25	WDOG0	0x1	RW	**WDOG0 Secure Access**
	WDOG0 Secure Access			
24	I2C0	0x1	RW	**I2C0 Secure Access**
	I2C0 Secure Access			
23	HFXO0	0x1	RW	**HFXO0 Secure Access**
	HFXO0 Secure Access			
22	HFRCO1	0x1	RW	**HFRCO1 Secure Access**
	HFRCO1 Secure Access			
21	LESENSE	0x1	RW	**LESENSE Secure Access**
	LESENSE Secure Access			
20	PCNT	0x1	RW	**PCNT Secure Access**
	PCNT Secure Access			
19	VDAC0	0x1	RW	**VDAC0 Secure Access**
	VDAC0 Secure Access			
18	AMUXCP0	0x1	RW	**AMUXCP0 Secure Access**
	AMUXCP0 Secure Access			
17	ACMP1	0x1	RW	**ACMP1 Secure Access**
	ACMP1 Secure Access			

Bit	Name	Reset	Access	Description
16	ACMP0	0x1	RW	**ACMP0 Secure Access**
	ACMP0 Secure Access			
15	IADC0	0x1	RW	**IADC0 Secure Access**
	IADC0 Secure Access			
14	LETIMER0	0x1	RW	**LETIMER0 Secure Access**
	LETIMER0 Secure Access			
13	AHBUSBSYS	0x1	RW	**AHBUSBSYS Secure Access**
	AHBUSBSYS Secure Access			
12	SMUCFGNS	0x1	RW	**SMUCFGNS Secure Access**
	SMUCFGNS Secure Access			
11	SMU	0x1	RW	**SMU Secure Access**
	SMU Secure Access			
10	RADIOAES	0x1	RW	**RADIOAES Secure Access**
	RADIOAES Secure Access			
9	BUFC	0x1	RW	**BUFC Secure Access**
	BUFC Secure Access			
8	ETAMPDET	0x1	RW	**ETAMPDET Secure Access**
	ETAMPDET Secure Access			
7	RFFPLL0	0x1	RW	**RFFPLL0 Secure Access**
	RFFPLL0 Secure Access			
6	PFMXPPRF	0x1	RW	**PFMXPPRF Secure Access**
	PFMXPPRF Secure Access			
5	DMEM	0x1	RW	**DMEM Secure Access**
	DMEM Secure Access			
4	SYSRTC	0x1	RW	**SYSRTC Secure Access**
	SYSRTC Secure Access			
3	EUSART4	0x1	RW	**EUSART4 Secure Access**
	EUSART4 Secure Access			
2	EUSART3	0x1	RW	**EUSART3 Secure Access**
	EUSART3 Secure Access			
1	EUSART2	0x1	RW	**EUSART2 Secure Access**
	EUSART2 Secure Access			
0	EUSART1	0x1	RW	**EUSART1 Secure Access**
	EUSART1 Secure Access			

10.5.11 SMU_PPUFS - Fault Status

Offset	Bit Position																													
0x140	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									R							
Name																									PPUFSPERIPHID							

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	PPUFSPERIPHID	0x0	R	**Peripheral ID** ID of the peripheral that caused the fault.

10.5.12 SMU_BMPUPATD0 - Privileged Attribute

Offset	Bit Position																													
0x150	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1
Access																							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name																							USB	SEEXTDMA	RFLDMA	RFECA1	RFECA0	LDMA1	LDMA0	BUFC	RADIOSUBSYSTEM	RADIOAES

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	USB	0x1	RW	**USB privileged mode**
	USB privileged mode			
8	SEEXTDMA	0x1	RW	**SEEXTDMA privileged mode**
	SEEXTDMA privileged mode			
7	RFLDMA	0x1	RW	**RFLDMA privileged mode**
	RFLDMA privileged mode			
6	RFECA1	0x1	RW	**RFECA1 privileged mode**
	RFECA1 privileged mode			
5	RFECA0	0x1	RW	**RFECA0 privileged mode**
	RFECA0 privileged mode			
4	LDMA1	0x1	RW	**MCU LDMA port 1 privileged mode**
	MCU LDMA port 1 privileged mode			
3	LDMA0	0x1	RW	**MCU LDMA port 0 privileged mode**
	MCU LDMA port 0 privileged mode			
2	BUFC	0x1	RW	**BUFC privileged mode**
	BUFC privileged mode			
1	RADIOSUBSYSTEM	0x1	RW	**RADIO subsystem manager privileged mode**
	RADIO subsystem manager privileged mode			
0	RADIOAES	0x1	RW	**RADIO AES DMA privileged mode**
	RADIO AES DMA privileged mode			

10.5.13 SMU_BMPUSATD0 - Secure Attribute

Offset	Bit Position																													
0x170	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1
Access																							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name																							USB	SEEXTDMA	RFLDMA	RFECA1	RFECA0	LDMA1	LDMA0	BUFC	RADIOSUBSYSTEM	RADIOAES

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	USB	0x1	RW	**USB secure mode**
	USB secure mode			
8	SEEXTDMA	0x1	RW	**SEEXTDMA secure mode**
	SEEXTDMA secure mode			
7	RFLDMA	0x1	RW	**RFLDMA secure mode**
	RFLDMA secure mode			
6	RFECA1	0x1	RW	**RFECA1 secure mode**
	RFECA1 secure mode			
5	RFECA0	0x1	RW	**RFECA0 secure mode**
	RFECA0 secure mode			
4	LDMA1	0x1	RW	**MCU LDMA port 1 secure mode**
	MCU LDMA port 1 secure mode			
3	LDMA0	0x1	RW	**MCU LDMA port 0 secure mode**
	MCU LDMA port 0 secure mode			
2	BUFC	0x1	RW	**BUFC secure mode**
	BUFC secure mode			
1	RADIOSUBSYSTEM	0x1	RW	**RADIO subsystem manager secure mode**
	RADIO subsystem manager secure mode			
0	RADIOAES	0x1	RW	**RADIO AES DMA secure mode**
	RADIO AES DMA secure mode			

10.5.14 SMU_BMPUFS - Fault Status

Offset	Bit Position																													
0x250	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									R							
Name																									BMPUFSMASTERID							

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	BMPUFSMASTERID	0x0	R	**Bus Manager ID**
	ID of Bus Manager that triggered fault			

10.5.15 SMU_BMPUFSADDR - Fault Status Address

Offset	Bit Position																													
0x254	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																0x0																
Access																R																
Name																BMPUFSADDR																

Bit	Name	Reset	Access	Description
31:0	BMPUFSADDR	0x0	R	**Fault Address**
	Access address that triggered fault			

10.5.16 SMU_ESAURTYPES0 - Region Types 0

Offset	Bit Position																															
0x260	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																				0x0												
Access																				RW												
Name																				ESAUR3NS												

Bit	Name	Reset	Access	Description
31:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12	ESAUR3NS	0x0	RW	**Region 3 Non-Secure** Set to 1 to configure Region 3 as Non-secure
11:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

10.5.17 SMU_ESAURTYPES1 - Region Types 1

Offset	Bit Position																															
0x264	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																				0x0												
Access																				RW												
Name																				ESAUR11NS												

Bit	Name	Reset	Access	Description
31:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12	ESAUR11NS	0x0	RW	**Region 11 Non-Secure** Set to 1 to configure Region 11 as Non-secure
11:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

10.5.18 SMU_ESAUMRB01 - Movable Region Boundary

Offset	Bit Position																															
0x270	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0xA000																											
Access					RW																											
Name					ESAUMRB01																											

Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27:12	ESAUMRB01	0xA000	RW	**Moveable Region Boundary**
	Moveable Region Boundary between Region 0 and Region 1. Address Represents the start of Region 1 at a 4kB offset.			
11:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

10.5.19 SMU_ESAUMRB12 - Movable Region Boundary

Offset	Bit Position																															
0x274	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0xC000																											
Access					RW																											
Name					ESAUMRB12																											

Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27:12	ESAUMRB12	0xC000	RW	**Moveable Region Boundary**
	Moveable Region Boundary between Region 1 and Region 2. Address Represents the start of Region 2 at a 4kB offset.			
11:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

10.5.20 SMU_ESAUMRB45 - Movable Region Boundary

Offset	Bit Position																															
0x280	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0x2000																											
Access					RW																											
Name					ESAUMRB45																											

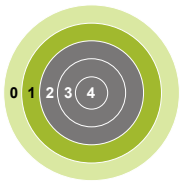
Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27:12	ESAUMRB45	0x2000	RW	**Moveable Region Boundary** Moveable Region Boundary between Regions 4 and 5. This represents the starting address of Region 5.
11:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

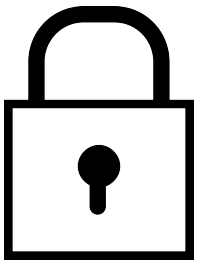
10.5.21 SMU_ESAUMRB56 - Movable Region Boundary

Offset	Bit Position																															
0x284	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0x4000																											
Access					RW																											
Name					ESAUMRB56																											

Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27:12	ESAUMRB56	0x4000	RW	**Moveable Region Boundary** Moveable Region Boundary between Regions 5 and 6. This represents the starting address of Region 6.
11:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

11. SE - Secure Engine Subsystem





Quick Facts

What?

The Secure Engine Subsystem encapsulates security peripherals providing both improved system security and ease of use.

Why?

Isolation of security hardware from the Cortex-M33 protects the SE system from exploits that target the main CPU. The subsystem also provides autonomous cryptographic operations allowing the main CPU to perform other tasks or enter EM1 to save power.

How?

Security peripherals are completely isolated from the main CPU and controlled with a processor internal to the SE subsystem.

11.1 Introduction

The Secure Engine (SE) provides several security features and acts as a barrier protecting the security hardware from activity on the Cortex-M33. It also enables autonomous operation of security features.

Available features include:

- Secure Boot with Root of Trust and Secure Loader (RTSL)
- Hardware Cryptographic Acceleration with DPA countermeasures for AES128/256, SHA-1, SHA-2 (up to 256-bit), ECC (up to 256-bit), ECDSA, ECDH and J-Pake
- True Random Number Generator (TRNG) compliant with NIST SP800-90 and AIS-31
- ARM® TrustZone®
- Secure Debug with lock/unlock

All Secure Engine functions are enabled by software. These functions are fully described in the Secure Engine emlib online documentation located at the following link:

https://docs.silabs.com/mcu/latest/efr32mg21/group-SE

11.2 Security Features

11.2.1 Security Features Overview

- Acceleration of cryptographic functions
  - AES encryption and decryption with 128, 192, or 256-bit keys
  - Supported block cipher modes of operation for AES include: ECB, CTR, CBC, CFB, CBC-MAC, CMAC, CCM, GCM and GMAC.
  - ECC over GF(P) up to 256-bit
  - Supported ECC NIST recommended curves include P-192 and P-256
  - SHA-1 and SHA-2 up to 256-bit
- True Random Number Generation
  - Entropy Source complies to NIST 800-90B requirements
  - Online Health tests comply to NIST 800-90 and AIS31 requirements
  - Random Data Passes NIST 800-22 and NIST 800-90B test suites
- Secure Boot Loader (First Stage Boot Loader)

11.2.2 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).

It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed, and protects Over The Air updates.

For more information about this feature, see AN1218: Series 2 Secure Boot with RTSL.

11.2.3 Secure Debug

The SE provides a secure debug unlock function that allows users to grant debug access to locked devices on a device by device basis. To use this function the device must be programmed with a public Command key by the user. To unlock a device, a unique challenge (a device-unique persistent random set of bytes) must be read out and signed by the private key associated with public Command key creating an unlock token. The device can then be unlocked by providing the valid unlock token. The token can be used to unlock the device any number of times. There is also a command to force the device to update its challenge, which revokes the previously-generated token.

More information on Secure Debug can be found in the AN1190: Secure Debug application note.

Note: Secure debug locking a device will limit the capability for Silicon Labs to perform failure analysis on the device. Provide secure debug tokens for each device when submitting parts for failure analysis.

11.2.4 Cryptographic Accelerator

The Cryptographic Accelerator is an autonomous hardware accelerator with Differential Power Analysis (DPA) countermeasures to protect keys.

It supports AES encryption and decryption with 128/192/256-bit keys, ChaCha20 encryption, and Elliptic Curve Cryptography (ECC) to support public key operations, and hashes.

Supported block cipher modes of operation for AES include:

- ECB (Electronic Code Book)
- CTR (Counter Mode)
- CBC (Cipher Block Chaining)
- CFB (Cipher Feedback)
- GCM (Galois Counter Mode)
- CCM (Counter with CBC-MAC)
- CBC-MAC (Cipher Block Chaining Message Authentication Code)
- GMAC (Galois Message Authentication Code)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the NIST (National Institute of Standards and Technology) recommended curves including P-192, P-256, P-384, and P-521 for ECDH (Elliptic Curve Diffie-Hellman) key derivation, and ECDSA (Elliptic Curve Digital Signature Algorithm) sign and verify operations. Also supported is the non-NIST Curve25519 for ECDH and Ed25519 for EdDSA (Edwards-curve Digital Signature Algorithm) sign and verify operations.

Secure Vault also supports ECJ-PAKE (Elliptic Curve variant of Password Authenticated Key Exchange by Juggling) and PBKDF2 (Password-Based Key Derivation Function 2).

Supported hashes include SHA-1, SHA-2/256/384/512 and Poly1305.

This implementation provides a fast and energy efficient solution to state of the art cryptographic needs.

11.2.5 True Random Number Generation

The SE provides access to a non-deterministic random number generator based on a full hardware solution. The TRNG output passes the NIST 800-22 and AIS31 test suites. The TRNG module includes several built-in self tests to detect issues with the noise source, ensure entropy, and meet cryptography standards. The Repetition Count Test and Adaptive Proportion Test with window sizes of 64 and 4096 bits described in section 6.5.1.2 of NIST-800-90B are implemented in hardware and run continuously on the data.

http://csrc.nist.gov/publications/drafts/800-90/draft-sp800-90b.pdf

The AIS31 Online Test described in section 5.5.3 of AIS 31 is also implemented in hardware, and runs continuously on the data.

https://www.bsi.bund.de/SharedDocs/Downloads/DE/BSI/Zertifizierung/Interpretationen/AIS_31_Functionality_classes_for_random_number_generators_e.pdf

11.3 SE Mailbox

All communication with the Secure Engine Subsystem takes place through the SE Mailbox. Operations are performed by using the mailbox to sending a command and then receive the SE response. The mailbox is a bidirectional 64 word FIFO.

11.3.1 Sending Commands

The TX FIFO has two status flags in SE_TX_STATUS register. TXFULL is set when the FIFO is full and TXINT is set if there is space in the FIFO for at least 16 words. If TXINTEN in SE_CONFIGURATION is set an interrupt will be generated when TXINT is set.

Writing to any SE_DATAn register will result in data being placed in the FIFO. For example, to write 16 words to the FIFO software may write SE_DATA0 16 times, or may make a single write to each of the 16 SE_DATAn registers. If the FIFO is written when no space is available, the CPU will be stalled until spaces becomes available and the write can be completed.

To send a command, first check TXINT to ensure that there is space available in the FIFO. Then write SE_TX_HEADER with the command length and protection bit. Finally, write the command data into the SE_DATAn registers. While the command is being written, BYTERM in SE_TX_STATUS will contain the number of bytes remaining in the command. To ensure minimal performance impact, software should ensure that space exists in the FIFO before writing to it.

11.3.2 Receiving Responses

The RX FIFO has two status flags in SE_RX_STATUS register. RXEMPTY is set when the FIFO is empty and RXINT is set if there are at least 4 words in the FIFO or if the final word of the message is present in the FIFO. If RXINTEN in SE_CONFIGURATION is set, an interrupt will be generated when RXINT is set.

Reading from any SE_DATAn register will result in data being read from the FIFO. For example, to read 16 words from the FIFO, software may read SE_DATA0 16 times, or may make a single read from each of the 16 SE_DATAn registers. If the FIFO is read when it is empty and no message is available, a 0x0 will be read. If the FIFO is read when empty and a message is being processed, the CPU will be stalled until data becomes available.

Software may check for responses by polling RXINT, RXEMPTY, or RXHEADER in SE_RX_STATUS. The RXINT interrupt may also be used to notify the CPU when data is available. To receive a response first read the response header from SE_RX_HEADER. Software may read the message size from SE_RX_HEADER, or use BYTERM in SE_RX_STATUS, which contains the number of words remaining in the response.

The command status is available in both SE_RX_STATUS and SE_RX_HEADER and indicates if the command completed successfully.

11.3.3 MAILBOX Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	MAILBOX_MSGPTRx	RW	Message Pointer
0x040	MAILBOX_IF	RW INTFLAG	Interrupt Flag Register
0x044	MAILBOX_IEN	RW	Interrupt Enable Register
0x1000	MAILBOX_MSGPTRx_SET	RW	Message Pointer
0x1040	MAILBOX_IF_SET	RW INTFLAG	Interrupt Flag Register
0x1044	MAILBOX_IEN_SET	RW	Interrupt Enable Register
0x2000	MAILBOX_MSGPTRx_CLR	RW	Message Pointer
0x2040	MAILBOX_IF_CLR	RW INTFLAG	Interrupt Flag Register
0x2044	MAILBOX_IEN_CLR	RW	Interrupt Enable Register
0x3000	MAILBOX_MSGPTRx_TGL	RW	Message Pointer
0x3040	MAILBOX_IF_TGL	RW INTFLAG	Interrupt Flag Register
0x3044	MAILBOX_IEN_TGL	RW	Interrupt Enable Register

11.3.4 MAILBOX Register Description

11.3.4.1 MAILBOX_MSGPTRx - Message Pointer

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	PTR																															

Bit	Name	Reset	Access	Description
31:0	PTR	0x0	RW	**Pointer**
	The Memory Address of the message.			

11.3.4.2 MAILBOX_IF - Interrupt Flag Register

Offset	Bit Position																															
0x040	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0	0x0	0x0	0x0
Access																													RW	RW	RW	RW
Name																													MBOXIF3	MBOXIF2	MBOXIF1	MBOXIF0

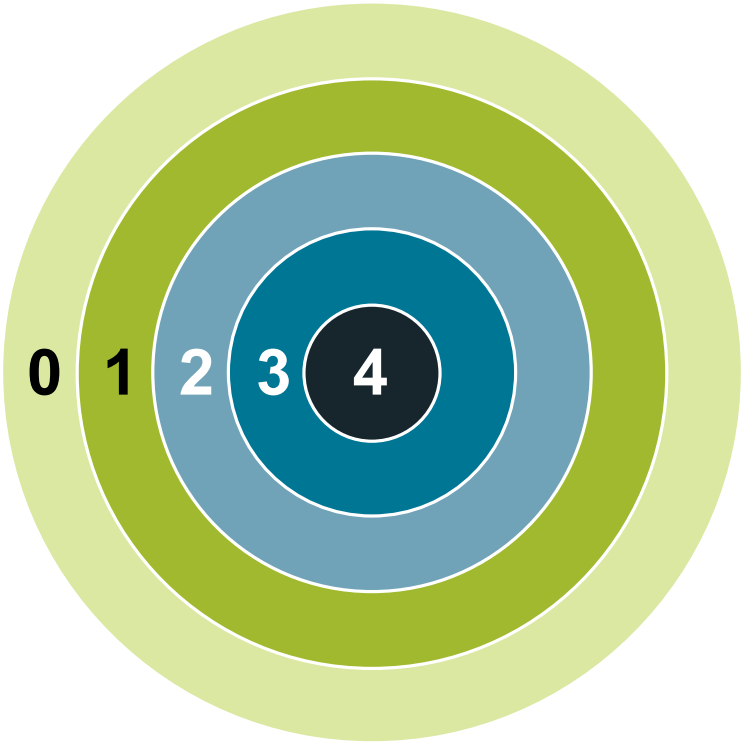
Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	MBOXIF3	0x0	RW	**Mailbox Interupt Flag**
	When set, Mailbox Message Availble.			
2	MBOXIF2	0x0	RW	**Mailbox Interupt Flag**
	When set, Mailbox Message Availble.			
1	MBOXIF1	0x0	RW	**Mailbox Interupt Flag**
	When set, Mailbox Message Availble.			
0	MBOXIF0	0x0	RW	**Mailbox Interupt Flag**
	When set, Mailbox Message Availble.			

11.3.4.3 MAILBOX_IEN - Interrupt Enable Register

Offset	Bit Position																													
0x044	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0	0x0	0x0	0x0
Access																													RW	RW	RW	RW
Name																													MBOXIEN3	MBOXIEN2	MBOXIEN1	MBOXIEN0

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	MBOXIEN3	0x0	RW	**Mailbox Interrupt Enable**
	Set to enable the MBOXIF Interrupt			
2	MBOXIEN2	0x0	RW	**Mailbox Interrupt Enable**
	Set to enable the MBOXIF Interrupt			
1	MBOXIEN1	0x0	RW	**Mailbox Interrupt Enable**
	Set to enable the MBOXIF Interrupt			
0	MBOXIEN0	0x0	RW	**Mailbox Interrupt Enable**
	Set to enable the MBOXIF Interrupt			

12. ETAMPDET - External Tamper Detect



Quick Facts

What?

ETAMPDET can alert the system to unauthorized physical access with very low current consumption

Why?
Detecting physical tampering can enhance security.

How?

Send low frequency random digital pulse out one pin and detect them returning on another.

12.1 Introduction

The External Tamper Detect (ETAMPDET) block functions to detect external physical tampering. For example, this feature can alert the system of an unauthorized opening of the surrounding enclosure, and the system can automatically initiate a pre-programmed response. Common implementations are to route the signal through switches that open when an enclosure is opened, or through a meander trace covering sensitive areas of PCB such that accessing the PCB requires breaking the trace thus breaking the conduction path. The ETAMPDET system uses a linear feedback shift register (LFSR) to send a time-varying pseudo random bit sequence (PRBS) digital waveform out on an ETAMPOUTx pin, and monitors a signal returned on a corresponding ETAMPINx pin. Using a random bit sequence for this makes it more difficult to thwart detection. These pins are electrically connected by an external conduction path which must be broken to gain physical access to the system. The returned PRBS signal is checked. If it is missing or does not match the sent PRBS (due to a broken trace between the IO pads), a tamper interrupt is sent and/or a PRS signal is triggered. The system designer has several choices of how to respond to alerts from ETAMPDET.

External tamper protection is useful during storage and other long periods of inactivity. This ETAMPDET feature is available in energy modes down to EM4, and current consumption is minimized to extend battery life while using this feature.

The pin pairs which can be used for this feature are limited, and are shown in GPIO Alternate Function Table of the datasheet.

12.2 Features

- Generates and compares time-varying PRBS waveform that runs down to EM4 mode
- Supports a distinct waveform per channel
- Supports software triggered reloading of LFSR
- Clock source
  - EM4GRPACLK (supports LFXO, LFRCO, ULFRCO as clock sources)
- Mismatch in waveform compare triggers
  - Wakeup event from EM1/2/3/4
  - Interrupt (individual interrupt flag per channel)
  - Tamper event signal
- Supports configurable clock divider up to divide by 4096
- Selectable 1 clock delay of compare value to support traces with propagation delay > 1 clock cycle
- Filtering against spurious tamper detection

12.3 Functional Description

A basic overview of the ETAMPDET function is shown in Figure 12.1 ETAMPDET Block Diagram on page 313. Only one channel is shown in the diagram. Each channel has individual configuration and controls. The clock prescaler circuitry and output logic (IRQ, PRS) are shared between channels.

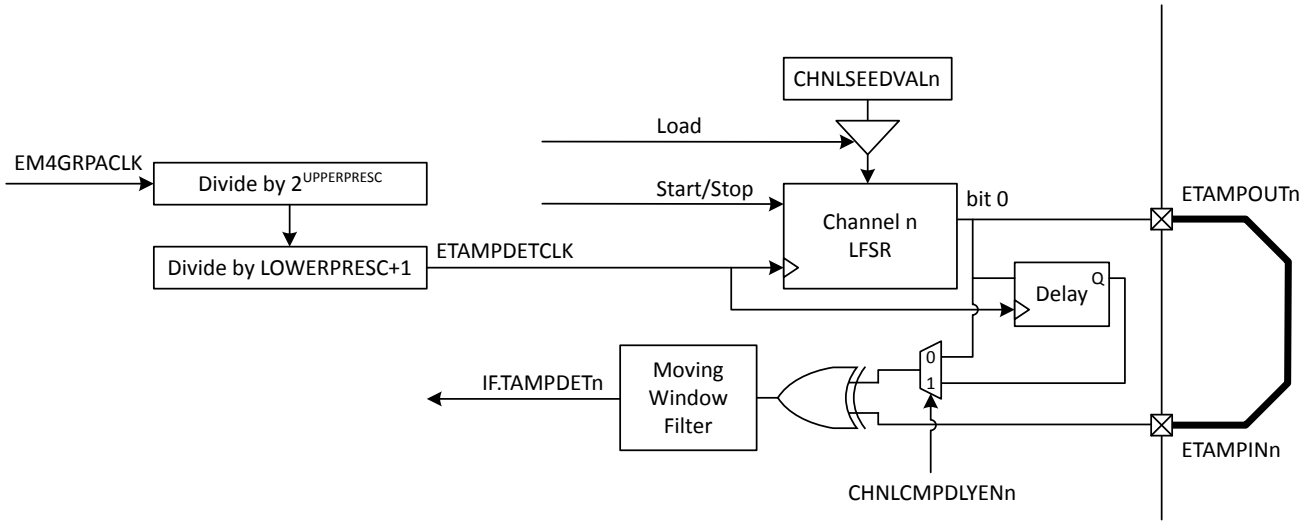


Figure 12.1. ETAMPDET Block Diagram

12.3.1 Configuration

Software will typically configure and enable the ETAMPDET block after a device reset, and leave the block running without intervention. The general procedure to enable this function is:

1. Configure the GPIO signals associated with the used channels in the GPIO block.
2. Configure the desired options and seed values for each channel used in the ETAMPDET module.
3. Write the EN.EN bit to '1' to enable the module (note that this will drive the selected ETAMPOUT pins).
4. Poll SYNCBUSY.EN to let the register write clock through.
5. Load the LFSR seed(s) by writing to CMD.CHNLLOADn.
6. Start the LFSR for the channel(s) by writing to CMD.CHNLSTARTn.
7. Poll the SYNCBUSY register to let the command writes take effect.

The following sections detail configuration options that are available for the ETAMPDET block. These options are generally configured before writing EN.EN, and not changed during operation.

12.3.2 Clocking

The ETAMPDET block is clocked from the EM4GRPACLK. The block has a two-stage clock prescaler which sets the desired operation frequency. The first stage is a ripple counter controlled by the UPPERPRESC field in the CLKPRESCVAL register, and the second stage is a binary counter controlled by LOWERPRESC in the CLKPRESCVAL. Figure 12.2 ETAMPDET Frequency on page 314 shows the calculated frequency after the prescalers.

$$f_{ETAMPDET} = f_{EM4GRPACLK} / (2^{UPPERPRESC}) / (LOWERPRESC + 1)$$

Figure 12.2. ETAMPDET Frequency

12.3.3 Filtering

The ETAMPDET block implements a filtering mechanism to help prevent false triggers. When enabled, the filter will only trigger a tamper detect if a configurable number of mismatches has been detected within a defined number of clock cycles. This is implemented as a moving window over the collected results, counting the number of mismatches within the window and raising a tamper detected event if the allowable mismatches are exceeded.

Each channel has its own individual filter controls:

- CHNLTAMPDETFILTEN[n] in CFG register: Enables filtering for channel [n].
- CHNLFILTWINSIZE[n] in CHNLFILTWINSIZE register: Sets the moving window filter size in bits for channel [n].
- CHNLCNTMISMATCHMAX[n] in CNTMISMATCHMAX register: Sets the filter mismatch threshold in bits for channel [n].

When a tamper event has been detected, the contents of the moving window will be flushed, to avoid subsequently triggering due to the same mismatches, but will not block a new mismatch input on next clock cycle.

Figure 12.3 Moving Window Filter Example on page 314 shows a sample sequence of filter inputs and the corresponding response, with a window size of 6 and a mismatch threshold of 3.

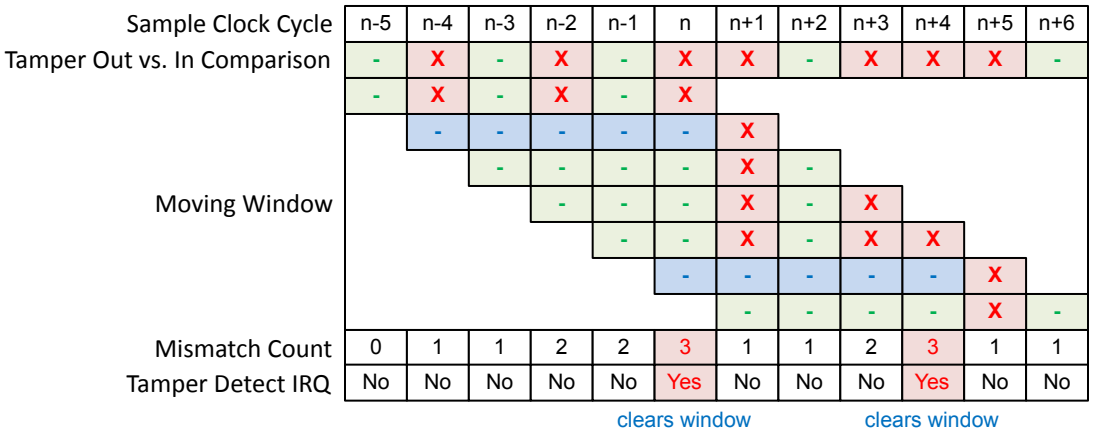


Figure 12.3. Moving Window Filter Example

12.3.4 Lock / Unlock

The ETAMPDET registers can be locked down to prevent rogue code from accidentally changing settings. Key control and configuration registers can be write-locked using the LOCK register. Reads are unaffected when the registers are locked. Writing the UNLOCK value to the LOCK register will unlock the register interface and allow access. Writing any other value to LOCK will lock the registers. The STATUS.LOCKSTATUS bit indicates whether the registers are locked.

12.3.5 Wakeup and Interrupt Sources

Each ETAMPDET channel can be individually configured to generate interrupts when a tamper event is detected, and to wake the system from low power modes down to EM4. The tamper interrupt source for each individual channel is enabled using the TAMPDETx bit in the ETAMPDET_IEN register. When a tamper event is detected, the TAMPDETx bit for the corresponding channel will be set in the IF register, and if the interrupt is enabled, an IRQ will be generated. The tamper event may also be routed via the PRS interface to other blocks in the system, or to a GPIO pin.

To enable waking from EM4, the CHNLEM4WUEN bit for the corresponding channel in the EM4WUEN register must be set to 1.

12.3.6 Commands

ETAMPDET commands can be issued through the CMD register when the module is enabled via the EN.EN bit. Three commands are available for each channel: LOAD, START, and STOP.

- A LOAD command is initiated by the CMD.CHNLLOADn bit. LOAD commands will reload the LFSR with a new seed value from the CHNLSEEDVALn register. LOAD commands can be issued before starting the counter, or while the counter is running. A LOAD command will require between 3 and 6 clocks of EM4GRPACLK and one fully divided (post-prescaler) ETAMPDET clock to take effect.
- A START command is initiated by the CMD.CHNLSTARTn bit, and will enable the LFSR shifting and tamper detection for the channel. A START command will require 6 clocks of EM4GRPACLK and one fully divided (post-prescaler) ETAMPDET clock to take effect.
- A STOP command is initiated by the CMD.CHNLSTOPn bit, and will disable the LFSR shifting and tamper detection for the channel. A STOP command will require between 3 and 6 clocks of EM4GRPACLK and one fully divided (post-prescaler) ETAMPDET clock to take effect.

The SYNCBUSY register can be polled after initiating commands to determine when the command has taken effect.

12.4 ETAMPDET Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	ETAMPDET_IPVERSION	R	IP Version ID
0x004	ETAMPDET_EN	RW ENABLE	Module Enable Register
0x00C	ETAMPDET_CFG	RW CONFIG	Configuration Register
0x010	ETAMPDET_CNTMISMATCH-MAX	RW CONFIG	Filter Threshold Register
0x014	ETAMPDET_CHNLFILTWIN-SIZE	RW CONFIG	Filter Moving Window Size Register
0x018	ETAMPDET_CMD	W LFSYNC	Command Register
0x01C	ETAMPDET_SYNCBUSY	RH	Syncbusy Status Register
0x020	ETAMPDET_IEN	RW	Interrupt Enable Register
0x024	ETAMPDET_IF	RWH INTFLAG	Interrupt Flag Register
0x028	ETAMPDET_STATUS	RH	Status Register
0x02C	ETAMPDET_EM4WUEN	RW CONFIG	EM4 Wakeup Request Enable Register
0x030	ETAMPDET_CHNLSEEDVAL0	RW	CHNL0 LFSR Seed Ctrl Register
0x034	ETAMPDET_CHNLSEEDVAL1	RW	CHNL1 LFSR Seed Ctrl Register
0x038	ETAMPDET_CLKPRESCVAL	RW CONFIG	Prescaler Ctrl Register
0x048	ETAMPDET_LOCK	W	Configuration Lock Register
0x1000	ETAMPDET_IPVERSION_SET	R	IP Version ID
0x1004	ETAMPDET_EN_SET	RW ENABLE	Module Enable Register
0x100C	ETAMPDET_CFG_SET	RW CONFIG	Configuration Register
0x1010	ETAMPDET_CNTMISMATCH-MAX_SET	RW CONFIG	Filter Threshold Register
0x1014	ETAMPDET_CHNLFILTWIN-SIZE_SET	RW CONFIG	Filter Moving Window Size Register
0x1018	ETAMPDET_CMD_SET	W LFSYNC	Command Register
0x101C	ETAMPDET_SYNCBUSY_SET	RH	Syncbusy Status Register
0x1020	ETAMPDET_IEN_SET	RW	Interrupt Enable Register
0x1024	ETAMPDET_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x1028	ETAMPDET_STATUS_SET	RH	Status Register
0x102C	ETAMPDET_EM4WUEN_SET	RW CONFIG	EM4 Wakeup Request Enable Register
0x1030	ETAMPDET_CHNLSEEDV-AL0_SET	RW	CHNL0 LFSR Seed Ctrl Register
0x1034	ETAMPDET_CHNLSEEDV-AL1_SET	RW	CHNL1 LFSR Seed Ctrl Register
0x1038	ETAMPDET_CLKPRESCV-AL_SET	RW CONFIG	Prescaler Ctrl Register
0x1048	ETAMPDET_LOCK_SET	W	Configuration Lock Register
0x2000	ETAMPDET_IPVERSION_CLR	R	IP Version ID

Offset	Name	Type	Description
0x2004	ETAMPDET_EN_CLR	RW ENABLE	Module Enable Register
0x200C	ETAMPDET_CFG_CLR	RW CONFIG	Configuration Register
0x2010	ETAMPDET_CNTMISMATCH-MAX_CLR	RW CONFIG	Filter Threshold Register
0x2014	ETAMPDET_CHNLFILTWIN-SIZE_CLR	RW CONFIG	Filter Moving Window Size Register
0x2018	ETAMPDET_CMD_CLR	W LFSYNC	Command Register
0x201C	ETAMPDET_SYNCBUSY_CLR	RH	Syncbusy Status Register
0x2020	ETAMPDET_IEN_CLR	RW	Interrupt Enable Register
0x2024	ETAMPDET_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x2028	ETAMPDET_STATUS_CLR	RH	Status Register
0x202C	ETAMPDET_EM4WUEN_CLR	RW CONFIG	EM4 Wakeup Request Enable Register
0x2030	ETAMPDET_CHNLSEEDV-AL0_CLR	RW	CHNL0 LFSR Seed Ctrl Register
0x2034	ETAMPDET_CHNLSEEDV-AL1_CLR	RW	CHNL1 LFSR Seed Ctrl Register
0x2038	ETAMPDET_CLKPRESCV-AL_CLR	RW CONFIG	Prescaler Ctrl Register
0x2048	ETAMPDET_LOCK_CLR	W	Configuration Lock Register
0x3000	ETAMPDET_IPVERSION_TGL	R	IP Version ID
0x3004	ETAMPDET_EN_TGL	RW ENABLE	Module Enable Register
0x300C	ETAMPDET_CFG_TGL	RW CONFIG	Configuration Register
0x3010	ETAMPDET_CNTMISMATCH-MAX_TGL	RW CONFIG	Filter Threshold Register
0x3014	ETAMPDET_CHNLFILTWIN-SIZE_TGL	RW CONFIG	Filter Moving Window Size Register
0x3018	ETAMPDET_CMD_TGL	W LFSYNC	Command Register
0x301C	ETAMPDET_SYNCBUSY_TGL	RH	Syncbusy Status Register
0x3020	ETAMPDET_IEN_TGL	RW	Interrupt Enable Register
0x3024	ETAMPDET_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x3028	ETAMPDET_STATUS_TGL	RH	Status Register
0x302C	ETAMPDET_EM4WUEN_TGL	RW CONFIG	EM4 Wakeup Request Enable Register
0x3030	ETAMPDET_CHNLSEEDV-AL0_TGL	RW	CHNL0 LFSR Seed Ctrl Register
0x3034	ETAMPDET_CHNLSEEDV-AL1_TGL	RW	CHNL1 LFSR Seed Ctrl Register
0x3038	ETAMPDET_CLKPRESCV-AL_TGL	RW CONFIG	Prescaler Ctrl Register
0x3048	ETAMPDET_LOCK_TGL	W	Configuration Lock Register

12.5 ETAMPDET Register Description

12.5.1 ETAMPDET_IPVERSION - IP Version ID

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x1																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x1	R	**IP Version ID**

12.5.2 ETAMPDET_EN - Module Enable Register

Offset	Bit Position																															
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	RW
Name																															DISABLING	EN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DISABLING	0x0	R	**Disablement busy status** When EN is cleared, DISABLING is set immediately, and cleared when disablement finishes. Disablement resets peripheral cores and not APB registers except hardware updated registers such as INTFLAGs and FIFOs. The CNT and PRECNT count registers are not reset during disablement.
0	EN	0x0	RW	**ETAMPDET Enable** Enable the ETAMPDET to make the peripheral clock available to the module

12.5.3 ETAMPDET_CFG - Configuration Register

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0	0x0	0x0	0x0	0x0	0x0
Access																											RW	RW	RW	RW	RW	RW
Name																											CHNLPADEN1	CHNLTAMPDETFILTEN1	CHNLCMPDLYEN1	CHNLPADEN0	CHNLTAMPDETFILTEN0	CHNLCMPDLYEN0

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	CHNLPADEN1	0x0	RW	**enable driving pad**
	Enables channel 1 driving pad			
	Value	Mode		Description
	0	DISABLE		Disables channel 0 Tamper detect filtering feature
	1	ENABLE		Enables channel 0 Tamper detect filtering feature
4	CHNLTAMPDETFIL-TEN1	0x0	RW	**enable detect filtering**
	Enables channel 1 Tamper detect filtering feature			
	Value	Mode		Description
	0	DISABLE		Disables channel 1 Tamper detect filtering feature
	1	ENABLE		Enables channel 1 Tamper detect filtering feature
3	CHNLCMPDLYEN1	0x0	RW	**enable delay for comparison**
	Enables 1 clock delay to the TX value used for comparison. This is to support trace propagation delay more than 1 clock cycle			
	Value	Mode		Description
	0	DISABLE		Disables 1 clock delay to the TX value used for comparison.
	1	ENABLE		Enables 1 clock delay to the TX value used for comparison.
2	CHNLPADEN0	0x0	RW	**enable driving pad**
	Enables channel 0 driving pad			
	Value	Mode		Description
	0	DISABLE		Disables channel 0 Tamper detect filtering feature
	1	ENABLE		Enables channel 0 Tamper detect filtering feature

Bit	Name	Reset	Access	Description
1	CHNLTAMPDETFIL-TEN0	0x0	RW	**enable detect filtering**
	Enables channel 0 Tamper detect filtering feature			

Value	Mode	Description
0	DISABLE	Disables channel 0 Tamper detect filtering feature
1	ENABLE	Enables channel 0 Tamper detect filtering feature

Bit	Name	Reset	Access	Description
0	CHNLCMPDLYEN0	0x0	RW	**enable delay for comparison**
	Enables 1 clock delay to the TX value used for comparison. This is to support trace propagation delay more than 1 clock cycle			

Value	Mode	Description
0	X0	Disables 1 clock delay to the TX value used for comparison.
1	X1	Enables 1 clock delay to the TX value used for comparison.

12.5.4 ETAMPDET_CNTMISMATCHMAX - Filter Threshold Register

Offset	Bit Position																															
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0			0x0		
Access																											RW			RW		
Name																											CHNLCNTMISMATCHMAX1			CHNLCNTMISMATCHMAX0		

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:3	CHNLCNTMISMATCH-MAX1	0x0	RW	**channel 1 filter counter threshold**

Channel 1 filter threshold value where a tamper detect will be triggered

Value	Mode	Description
0	DETECTFILTERTHRES-HOLD1	Detect filter raise detect flag after seeing 1 event before reset counter expire
1	DETECTFILTERTHRES-HOLD2	Detect filter raise detect flag after seeing 2 events before reset counter expire
2	DETECTFILTERTHRES-HOLD3	Detect filter raise detect flag after seeing 3 events before reset counter expire
3	DETECTFILTERTHRES-HOLD4	Detect filter raise detect flag after seeing 4 events before reset counter expire
4	DETECTFILTERTHRES-HOLD5	Detect filter raise detect flag after seeing 5 events before reset counter expire
5	DETECTFILTERTHRES-HOLD6	Detect filter raise detect flag after seeing 6 events before reset counter expire
6	DETECTFILTERTHRES-HOLD7	Detect filter raise detect flag after seeing 7 events before reset counter expire
7	DETECTFILTERTHRES-HOLD8	Detect filter raise detect flag after seeing 8 events before reset counter expire

Bit	Name	Reset	Access	Description
2:0	CHNLCNTMISMATCH-MAX0	0x0	RW	**channel 0 filter counter threshold**

Channel 0 filter threshold value where a tamper detect will be triggered

Value	Mode	Description
0	DETECTFILTERTHRES-HOLD1	Detect filter raise detect flag after seeing 1 event before reset counter expire

Bit	Name	Reset	Access	Description
	1	DETECTFILTERTHRES-HOLD2		Detect filter raise detect flag after seeing 2 events before reset counter expire
	2	DETECTFILTERTHRES-HOLD3		Detect filter raise detect flag after seeing 3 events before reset counter expire
	3	DETECTFILTERTHRES-HOLD4		Detect filter raise detect flag after seeing 4 events before reset counter expire
	4	DETECTFILTERTHRES-HOLD5		Detect filter raise detect flag after seeing 5 events before reset counter expire
	5	DETECTFILTERTHRES-HOLD6		Detect filter raise detect flag after seeing 6 events before reset counter expire
	6	DETECTFILTERTHRES-HOLD7		Detect filter raise detect flag after seeing 7 events before reset counter expire
	7	DETECTFILTERTHRES-HOLD8		Detect filter raise detect flag after seeing 8 events before reset counter expire

12.5.5 ETAMPDET_CHNLFILTWINSIZE - Filter Moving Window Size Register

Offset	Bit Position																															
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0				0x0			
Access																									RW				RW			
Name																									CHNLFILTWINSIZE1				CHNLFILTWINSIZE0			

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:4	CHNLFILTWINSIZE1	0x0	RW	**channel 1 Filter moving window size**

Channel 1 Filter moving window size

Value	Mode	Description
0	RESERVED	Reserved
1	DETECTFILTERMOVING-WINSIZE2	Detect filter moving window size is 2
2	DETECTFILTERMOVING-WINSIZE3	Detect filter moving window size is 3
3	DETECTFILTERMOVING-WINSIZE4	Detect filter moving window size is 4
4	DETECTFILTERMOVING-WINSIZE5	Detect filter moving window size is 5
5	DETECTFILTERMOVING-WINSIZE6	Detect filter moving window size is 6
6	DETECTFILTERMOVING-WINSIZE7	Detect filter moving window size is 7
7	DETECTFILTERMOVING-WINSIZE8	Detect filter moving window size is 8
8	DETECTFILTERMOVING-WINSIZE9	Detect filter moving window size is 9
9	DETECTFILTERMOVING-WINSIZE10	Detect filter moving window size is 10
10	DETECTFILTERMOVING-WINSIZE11	Detect filter moving window size is 11
11	DETECTFILTERMOVING-WINSIZE12	Detect filter moving window size is 12
12	DETECTFILTERMOVING-WINSIZE13	Detect filter moving window size is 13

Bit	Name	Reset	Access	Description
	13	DETECTFILTERMOVING-WINSIZE14		Detect filter moving window size is 14
	14	DETECTFILTERMOVING-WINSIZE15		Detect filter moving window size is 15
	15	DETECTFILTERMOVING-WINSIZE16		Detect filter moving window size is 16
3:0	CHNLFILTWINSIZE0	0x0	RW	**channel 0 Filter moving window size**

Channel 0 Filter moving window size

Value	Mode	Description
0	RESERVED	Reserved
1	DETECTFILTERMOVING-WINSIZE2	Detect filter moving window size is 2
2	DETECTFILTERMOVING-WINSIZE3	Detect filter moving window size is 3
3	DETECTFILTERMOVING-WINSIZE4	Detect filter moving window size is 4
4	DETECTFILTERMOVING-WINSIZE5	Detect filter moving window size is 5
5	DETECTFILTERMOVING-WINSIZE6	Detect filter moving window size is 6
6	DETECTFILTERMOVING-WINSIZE7	Detect filter moving window size is 7
7	DETECTFILTERMOVING-WINSIZE8	Detect filter moving window size is 8
8	DETECTFILTERMOVING-WINSIZE9	Detect filter moving window size is 9
9	DETECTFILTERMOVING-WINSIZE10	Detect filter moving window size is 10
10	DETECTFILTERMOVING-WINSIZE11	Detect filter moving window size is 11
11	DETECTFILTERMOVING-WINSIZE12	Detect filter moving window size is 12
12	DETECTFILTERMOVING-WINSIZE13	Detect filter moving window size is 13
13	DETECTFILTERMOVING-WINSIZE14	Detect filter moving window size is 14
14	DETECTFILTERMOVING-WINSIZE15	Detect filter moving window size is 15
15	DETECTFILTERMOVING-WINSIZE16	Detect filter moving window size is 16

12.5.6 ETAMPDET_CMD - Command Register

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0	0x0	0x0	0x0	0x0	0x0
Access																											W(nB)	W(nB)	W(nB)	W(nB)	W(nB)	W(nB)
Name																											CHNLLOAD1	CHNLSTOP1	CHNLSTART1	CHNLLOAD0	CHNLSTOP0	CHNLSTART0

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	CHNLLOAD1	0x0	W(nB)	**Start channel 1 tamper detection**
	Set to 1 to load seed value into channel 1 LFSR			
4	CHNLSTOP1	0x0	W(nB)	**Stop channel 1 tamper detection**
	Stop channel 1 tamper detection			
3	CHNLSTART1	0x0	W(nB)	**Start channel 1 tamper detection**
	Start channel 1 tamper detection			
2	CHNLLOAD0	0x0	W(nB)	**Start channel 0 tamper detection**
	Set to 1 to load seed value into channel 0 LFSR			
1	CHNLSTOP0	0x0	W(nB)	**Stop channel 0 tamper detection**
	Stop channel 0 tamper detection			
0	CHNLSTART0	0x0	W(nB)	**Start channel 0 tamper detection**
	Start channel 0 tamper detection			

12.5.7 ETAMPDET_SYNCBUSY - Syncbusy Status Register

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0	0x0	0x0	0x0	0x0	0x0
Access																											R	R	R	R	R	R
Name																											CHNLLOAD1	CHNLSTOP1	CHNLSTART1	CHNLLOAD0	CHNLSTOP0	CHNLSTART0

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	CHNLLOAD1	0x0	R	**Synchronizer busy status**
	Last writing of CHNL1LOAD is synchronizing to LF clock			
4	CHNLSTOP1	0x0	R	**Synchronizer busy status**
	Last writing of CHNL1STOP is synchronizing to LF clock			
3	CHNLSTART1	0x0	R	**Synchronizer busy status**
	Last writing of CHNL1START is synchronizing to LF clock			
2	CHNLLOAD0	0x0	R	**Synchronizer busy status**
	Last writing of CHNLLOAD is synchronizing to LF clock			
1	CHNLSTOP0	0x0	R	**Synchronizer busy status**
	Last writing of CHNL0STOP is synchronizing to LF clock			
0	CHNLSTART0	0x0	R	**Synchronizer busy status**
	Last writing of CHNL0START is synchronizing to LF clock			

12.5.8 ETAMPDET_IEN - Interrupt Enable Register

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															RW	RW
Name																															TAMPDET1	TAMPDET0

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	TAMPDET1	0x0	RW	**TAMPDET1 interrupt enable**
	Set to enable TAMPDET1 interrupt			
0	TAMPDET0	0x0	RW	**TAMPDET0 interrupt enable**
	Set to enable TAMPDET0 interrupt			

12.5.9 ETAMPDET_IF - Interrupt Flag Register

Offset	Bit Position																													
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															RW	RW
Name																															TAMPDET1	TAMPDET0

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	TAMPDET1	0x0	RW	**Tamper1 Detect Flag**
	Set when a tamper detect occurs on channel 1			
0	TAMPDET0	0x0	RW	**Tamper0 Detect Flag**
	Set when a tamper detect occurs on channel 0			

12.5.10 ETAMPDET_STATUS - Status Register

Offset	Bit Position																													
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																														0x0	0x0
Access	R																														R	R
Name	LOCKSTATUS																														CHNLRUNNING1	CHNLRUNNING0

Bit	Name	Reset	Access	Description
31	LOCKSTATUS	0x0	R	**Lock Status**
	Indicates the Indicates the current status of ETAMPDET Lock			

Value	Mode	Description
0	UNLOCKED	ETAMPDET registers are unlocked
1	LOCKED	ETAMPDET registers are locked

30:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	CHNLRUNNING1	0x0	R	**Channel1 Running Status**
	Set when channel 1 is running			
0	CHNLRUNNING0	0x0	R	**Channel0 Running Status**
	Set when channel 0 is running			

12.5.11 ETAMPDET_EM4WUEN - EM4 Wakeup Request Enable Register

Offset	Bit Position																													
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															RW	RW
Name																															CHNLEM4WUEN1	CHNLEM4WUEN0

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	CHNLEM4WUEN1	0x0	RW	**Channel1 Tampdet EM4 Wakeup Enable**
	Set to enable EM4 wakeup when channel 1 tamper detect is set			
0	CHNLEM4WUEN0	0x0	RW	**Channel0 Tampdet EM4 Wakeup Enable**
	Set to enable EM4 wakeup when channel 0 tamper detect is set			

12.5.12 ETAMPDET_CHNLSEEDVAL0 - CHNL0 LFSR Seed Ctrl Register

Offset	Bit Position																													
0x030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																0x0																
Access																RW																
Name																CHNLSEEDVAL0																

Bit	Name	Reset	Access	Description
31:0	CHNLSEEDVAL0	0x0	RW	**Channel 0 LFSR Seed Value**
	Seed value to load into channel 0 LFSR			

12.5.13 ETAMPDET_CHNLSEEDVAL1 - CHNL1 LFSR Seed Ctrl Register

Offset	Bit Position																													
0x034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	CHNLSEEDVAL1																															

Bit	Name	Reset	Access	Description
31:0	CHNLSEEDVAL1	0x0	RW	**Channel 1 LFSR Seed Value**
	Seed value to load into channel 1 LFSR			

12.5.14 ETAMPDET_CLKPRESCVAL - Prescaler Ctrl Register

Offset	Bit Position																															
0x038	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																						0x0					0x0					
Access																						RW					RW					
Name																						UPPERPRESC					LOWERPRESC					

Bit	Name	Reset	Access	Description
31:11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10:8	UPPERPRESC	0x0	RW	**Upper part of divider ripple counter**
	Upper part of divider ripple counter			

Value	Mode	Description
0	BYPASS	Ripple counter divider is bypassed
1	DIVIDEBY2	Divide by 2
2	DIVIDEBY4	Divide by 4
3	DIVIDEBY8	Divide by 8
4	DIVIDEBY16	Divide by 16
5	DIVIDEBY32	Divide by 32
6	DIVIDEBY64	Divide by 64
7	RESERVED	Reserved, programing to this value is equal to programing 0x0

7:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:0	LOWERPRESC	0x0	RW	**Lower part of divider binary counter**
	Lower part of divider binary counter			

Value	Mode	Description
0	BYPASS	Divider is bypassed
1	DIVIDEBY2	Divide by 2
2	DIVIDEBY3	Divide by 3
3	DIVIDEBY4	Divide by 4
4	DIVIDEBY5	Divide by 5
5	DIVIDEBY6	Divide by 6
6	DIVIDEBY7	Divide by 7
7	DIVIDEBY8	Divide by 8
8	DIVIDEBY9	Divide by 9

Bit	Name	Reset	Access	Description
	9	DIVIDEBY10		Divide by 10
	10	DIVIDEBY11		Divide by 11
	11	DIVIDEBY12		Divide by 12
	12	DIVIDEBY13		Divide by 13
	13	DIVIDEBY14		Divide by 14
	14	DIVIDEBY15		Divide by 15
	15	DIVIDEBY16		Divide by 16
	16	DIVIDEBY17		Divide by 17
	17	DIVIDEBY18		Divide by 18
	18	DIVIDEBY19		Divide by 19
	19	DIVIDEBY20		Divide by 20
	20	DIVIDEBY21		Divide by 21
	21	DIVIDEBY22		Divide by 22
	22	DIVIDEBY23		Divide by 23
	23	DIVIDEBY24		Divide by 24
	24	DIVIDEBY25		Divide by 25
	25	DIVIDEBY26		Divide by 26
	26	DIVIDEBY27		Divide by 27
	27	DIVIDEBY28		Divide by 28
	28	DIVIDEBY29		Divide by 29
	29	DIVIDEBY30		Divide by 30
	30	DIVIDEBY31		Divide by 31
	31	DIVIDEBY32		Divide by 32
	32	DIVIDEBY33		Divide by 33
	33	DIVIDEBY34		Divide by 34
	34	DIVIDEBY35		Divide by 35
	35	DIVIDEBY36		Divide by 36
	36	DIVIDEBY37		Divide by 37
	37	DIVIDEBY38		Divide by 38
	38	DIVIDEBY39		Divide by 39
	39	DIVIDEBY40		Divide by 40
	40	DIVIDEBY41		Divide by 41
	41	DIVIDEBY42		Divide by 42
	42	DIVIDEBY43		Divide by 43
	43	DIVIDEBY44		Divide by 44
	44	DIVIDEBY45		Divide by 45
	45	DIVIDEBY46		Divide by 46

Bit	Name	Reset	Access	Description
	46	DIVIDEBY47		Divide by 47
	47	DIVIDEBY48		Divide by 48
	48	DIVIDEBY49		Divide by 49
	49	DIVIDEBY50		Divide by 50
	50	DIVIDEBY51		Divide by 51
	51	DIVIDEBY52		Divide by 52
	52	DIVIDEBY53		Divide by 53
	53	DIVIDEBY54		Divide by 54
	54	DIVIDEBY55		Divide by 55
	55	DIVIDEBY56		Divide by 56
	56	DIVIDEBY57		Divide by 57
	57	DIVIDEBY58		Divide by 58
	58	DIVIDEBY59		Divide by 59
	59	DIVIDEBY60		Divide by 60
	60	DIVIDEBY61		Divide by 61
	61	DIVIDEBY62		Divide by 62
	62	DIVIDEBY63		Divide by 63
	63	DIVIDEBY64		Divide by 64

12.5.15 ETAMPDET_LOCK - Configuration Lock Register

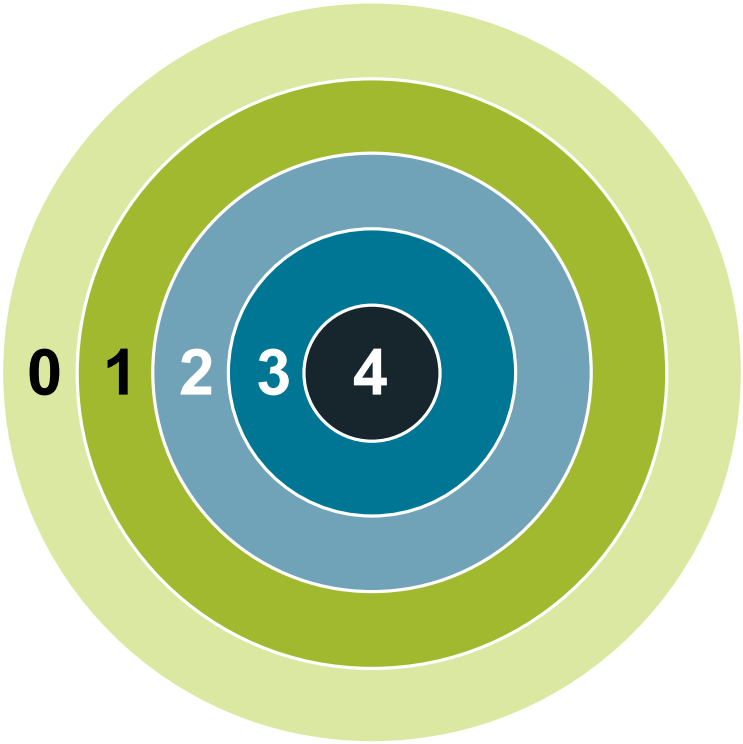
Offset	Bit Position																													
0x048	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0xAEE8															
Access																	W															
Name																	LOCKKEY															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LOCKKEY	0xAEE8	W	**Configuration Lock Key**

Write any other value than the unlock code to lock EN, CFG, CNTMISMATCHMAX, CHNLFILTWINSIZE, CMD, EM4WUEN, CHNLSEEDVAL0/1 and CLKPRESCVAL registers from editing. Write the unlock code to unlock.

Value	Mode	Description
44776	UNLOCK	Write to unlock all BURTC lockable registers

13. EMU - Energy Management Unit



Quick Facts

What?

The EMU (Energy Management Unit) handles the different low energy modes in EFR32xG25

Why?

The need for performance and peripheral functions varies over time in most applications. By efficiently scaling the available resources in real time to match the demands of the application, the energy consumption can be kept at a minimum.

How?

With a broad selection of energy modes, a high number of low-energy peripherals available even in EM2, and short wake-up time, applications can dynamically minimize energy consumption during program execution.

13.1 Introduction

The Energy Management Unit (EMU) manages all the low energy modes (EM) in EFR32xG25. Each energy mode manages whether the CPU and the various peripherals are available. The energy modes range from EM0 to EM4. EM0 mode provides the highest amount of features, enabling the CPU, Radio, and peripherals with the highest clock frequency. EM4 Mode provides the lowest power state, allowing the part to return to EM0 on a wake-up condition. The EMU also controls the internal regulators settings and voltage monitoring needed for optimal power configuration and protection.

13.2 Features

The primary features of the EMU are listed below:

- Energy Modes control
  - Entry into EM4
  - Configuration of regulators and clocks for each Energy Mode
  - Configuration of various EM4 wake-up conditions
  - Configuration of GPIO retention settings
- Power routing configurations
  - DCDC control and bypass
- Temperature sensor
- Brown Out Detection
- Supply voltage scaling
  - EM0 / EM1 voltage scaling
  - EM2 / EM3 voltage scaling
- Reset Management
  - Power-on Reset (POR)
  - Brown-out Detection (BOD) on the following power domains:
    - Analog Unregulated Power Domain AVDD
    - Digital Unregulated Power Domain DVDD
    - I/O Unregulated Power Domain IOVDDx
    - Regulated Digital Domain DECOUPLE (DEC)
  - RESETn pin reset
  - Watchdog (WDOG) reset
  - Software triggered reset (SYSRESETREQ)
  - Core LOCKUP condition
  - EM4 Detection
  - EM4 wakeup reset from GPIO pin
  - Configurable reset levels
  - A software readable register indicates the cause of the last reset

13.3 Functional Description

The EMU is responsible for managing the wide range of energy modes available in EFR32xG25. The block works in harmony with the entire platform to easily transition between energy modes in the most efficient manner possible. The following diagram Figure 13.1 EMU Overview on page 336, shows the relative connectivity to the various blocks in the system.

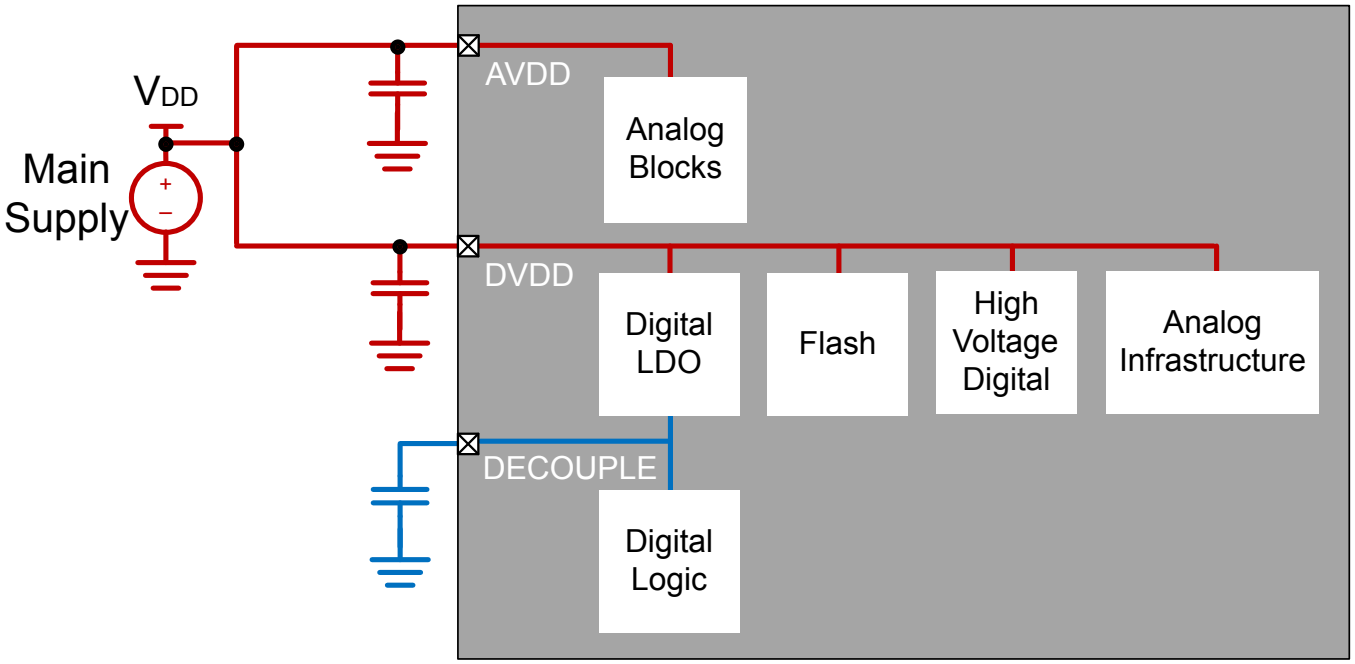


Figure 13.1. EMU Overview

The EMU is available on the peripheral bus. The energy management state machine controls the internal voltage regulators, oscillators, memories, and interrupt system. Events, interrupts, and resets can trigger the energy management state machine to return to the active state. This is further described in the following sections.

13.3.1 Energy Modes

EFR32xG25 features five main energy modes, referred to as Energy Mode 0 (EM0) through Energy Mode 4 (EM4). The Cortex-M33 is only available for program execution in EM0. In EM0 Active/EM1 Sleep any peripheral function can be enabled. EM2 through EM4, also referred to as low energy modes, provide a significantly reduced energy consumption while still allowing a rich set of peripheral functionality. The following Table 13.1 table on page 337 shows the possible transitions between different energy modes.

Table 13.1. Energy Mode Transitions

Current Mode	EM Transition Action				
	Enter EM0	Enter EM1	Enter EM2	Enter EM3	Enter EM4
EM0		Sleep (WFI, WFE)	Deep Sleep (WFI, WFE)	Deep Sleep (WFI, WFE)	EM4 Entry
EM1	IRQ		Peripheral wake up done[1]	Peripheral wake up done [1]	
EM2	IRQ	Peripheral wake up req [1]			
EM3	IRQ	Peripheral wake up req [1]			
EM4	Wake Up				

Note:
1. Peripheral wake-up from EM2/3 to EM1 and then automatically back to EM2/3 when done.

Peripherals such as the IADC and radio have the ability to temporarily wake up the part from either EM2 or EM3 to EM1 in order to transfer data. Once completed, the part is automatically placed back into the EM2 or EM3 mode.

The Core can always request to go to EM1 with the WFI or WFE command during EM0. The core will be prevented from entering EM2 or EM3 if the radio is transferring data or if flash is programming or erasing.

An overview of supported energy modes and available functionality is shown in the following table. For each energy mode, the system will typically default to its lowest power configuration, with non-essential clocks and peripherals disabled. Functionality may be then selectively enabled by software.

Refer to 13.3.4 Power Domains for more detail about peripheral power domain consumption.

Table 13.2. Energy Modes

	EM0 / EM1	EM2 / EM3	EM4	Low Power Domain
Cortex-M33 Core Active	Yes, in EM0 only	-	-	-
Debug	Available	See Note [1]	-	PD0D
Digital logic and system RAM retained	Yes	Yes	-	-
Flash Memory Access	Available	-	-	-
LDMA (Linked DMA Controller)	Available	Available [2]	-	-
Radio Controller	Available	Available [3]	-	-
High Frequency Clocks (BUSCLK, HCLK, PCLK, RADIOCLK, EM01GRPACLK, EM01GRPCCLK)	Available	-	-	-
High Frequency Oscillator (HFXO)	Available	-	-	PD0C

	EM0 / EM1	EM2 / EM3	EM4	Low Power Domain
High Frequency RC Oscillator (HFRCODPLL)	Available	-	-	-
ADC Clock (IADCCLK) and VDAC0 Clock (VDAC0CLK)	Available	Available [4]	-	-
EM2/3 High Frequency Oscillator (HFRCOEM23)	Available	Available [4]	-	PD0C
Fast Startup RC Oscillator (FSRCO)	Available	Available [4]	-	PD0A
Low Frequency RC Oscillator (LFRCO)	Available	EM2 Only	Available [5]	PDHV
Low Frequency Crystal Oscillator (LFXO)	Available	EM2 Only	Available [5]	PDHV
Low Energy Clocks (EM23GRPACLK, WDOGnCLK, SYSRTCCCLK, PCNT0CLK, EUSART0CLK)	Available	Available [6]	-	-
EM4 Clock (EM4GRPACLK)	Available	Available [6]	Available [5]	-
ULFRCO (Ultra Low Frequency Oscillator)	On	On	Available[5]	PDHV
GPCRC (General Purpose Cyclic Redundancy Check)	Available	-	-	-
SYSRTC (System Real-Time Clock	Available	Available [6]	-	PD0A
BURTC (Back-Up Real-Time Clock)	Available	Available [6]	Available	PDHV
BURAM (Back-Up RAM)	Available	Available	Available	PDHV
EUSART0	Available	Available [9]	-	PD0D
EUSART[4:1] (UART/SPI)	Available	-	-	-
I^2C0	Available	Available [8]	-	PD0D
I^2C1	Available	-	-	-
TIMER (Timer/Counter)	Available	-	-	-
LETIMER (Low Energy Timer)	Available	Available [6]	-	PD0B
WDOG (Watchdog)	Available	Available [6]	-	PD0D
ACMP (Analog Comparator)	Available	Available [7]	-	PD0B
IADC (Analog to Digital Converter)	Available	Available [2]	-	PD0B
VDAC (Digital-to-Analog Converter)	Available	Available [2]	-	PD0B
LESENSE (Low energy Sense)	Available	Available [2]	-	PD0B
PCNT (Pulse Counter)	Available	Available [2]	-	PD0B
USB (Universal Serial Bus)	Available	Available [12]	-	PDU
USBPLL0 (USB Phase Locked Loop)	Available	-	-	PDU
ETAMPDET (Tamper Detect)	Available	Available	Available	PDHV
DC-DC	Available	Available	-	PD0A
EMU Temperature Change	Available	Available	-	PD0A

	EM0 / EM1	EM2 / EM3	EM4	Low Power Domain
Brown-Out Detect/Power-on Reset	Available	Available	Available	-
Pin Reset	Available	Available	Available	-
PRS (Peripheral Reflex System)	Available	Available	-	PD0E
GPIO Pin Interrupts	Available	Available	Available [10]	-
GPIO Pin State Retention	Yes	Yes	Available [11]	-

Note:

1. Leaving the debugger connected when in EM2 or EM3 will cause the system to enter a higher power EM2 mode in which the high frequency clocks are still enabled and certain core functionality is still powered-up in order to maintain debug-functionality.
2. The LDMA can be used with some low power peripherals (e.g., IADC) in EM2/3. Features required by the LDMA which are not supported in EM2/3 (e.g., HCLK), will be automatically enabled prior to the LDMA transfer and then automatically disabled afterwards.
3. EM2 only. The RAC can be woken via a PRS interrupt to EM1 to transfer data. Once complete, the system will return to EM2.
4. Default off, but kept active if used by the IADC or VDAC.
5. Default off, but kept active if used by the BURTC
6. Must use ULFRCO in EM3 (LFRCO & LFXO not available in EM3)
7. ACMP functionality in EM2/3 limited to edge interrupt
8. I2C functionality limited to receive address recognition in EM2/3. Not supported on all GPIO Ports.
9. EUSART functionality limited to low-frequency UART or SPI secondary in EM2/3. Not supported on all GPIO Ports.
10. Pin wake-up in EM4 supported only on GPIO_EM4WUx pins. Consult data sheet for complete list of pins.
11. If enabled in EMU->EM4CTRL.EM4IORETMODE.
12. EM2 only. USB functionality in EM2 limited to USB Suspend mode and wake on bus activity.

The different energy modes are summarized in the following sections.

13.3.1.1 EM0

EM0 provides all system features.

- Cortex-M33 is executing code
- Radio functionality is available
- High and low frequency clock trees are active
- All oscillators are available
- All peripheral functionality is available

13.3.1.2 EM1

EM1 disables the core but leaves the remaining system fully available.

- Cortex-M33 is in sleep mode. Clocks to the core are off
- Radio functionality is available
- High and low frequency clock trees are active
- All oscillators are available
- All peripheral functionality is available

13.3.1.3 EM1P

EM1P is a subset of EM1 which allows the radio to operate while the core and high-speed peripherals are shut down to save energy. It is entered when the radio is active and software requests to enter EM2.

- Cortex-M33 is in sleep mode. Clocks to the core and all high-speed peripherals are off
- Radio and HFXO remain active
- All peripherals and oscillators capable of EM2, EM3 or EM4 operation are available

13.3.1.4 EM2

This is the first level into the low power energy modes. Most of the high frequency peripherals are disabled or have reduced functionality. Memory and registers retain their values.

- Cortex-M33 is in sleep mode. Clocks to the core are off.
- Radio inactive
- High frequency clock tree is inactive
- Low frequency clock tree is active
- The following oscillators are available
  - LFRCO, LFXO, ULFRCO
  - On-demand if used by peripherals: FSRCO, HFRCOEM23
- The following low frequency peripherals are available
  - SYSRTC, BURTC, WDOG, LETIMER, PCNT, LESENSE, I2C0, and EUSART0 (UART or SPI secondary only)
- The following analog peripherals are available (with potential limitations on functionality)
  - ACMP, IADC, VDAC
- Wake-up to EM0 through
  - Peripheral interrupt, reset pin, power on reset, asynchronous pin interrupt, I2C0 address recognition
- Wake-up to EM1 through
  - Peripheral data transfer request
  - Part returns to EM2 when transfers are complete
- RAM and register values are preserved
  - RAM blocks may be optionally powered down for lower power
- GPIO pin state is retained
- Debug connectivity is unavailable by default to reduce current consumption. Debug connectivity can be enabled by setting the EM2DBGEN bit in the EMU_CTRL register, and will consume about 0.5 uA extra supply current.

13.3.1.5 EM3

In this low energy mode, all low frequency oscillators (LFXO, LFRCO) and all low frequency clocks derived from them are stopped, as well as all high frequency clocks. Most peripherals are disabled or have reduced functionality. Memory and registers retain their values.

- Cortex-M33 is in sleep mode. Clocks to the core are off.
- Radio inactive
- High frequency clock tree is inactive
- All low frequency clock trees derived from the low frequency oscillators (LFXO, LFRCO) are inactive
- The following oscillators are available
  - ULFRCO
  - On-demand if used by peripherals: FSRCO, HFRCOEM23
- The following low frequency peripherals are available if clocked by the ULFRCO
  - SYSRTC, BURTC, WDOG, LETIMER, PCNT, LESENSE, I2C0, and EUSART0 (SPI secondary only)
- The following analog peripherals are available (with potential limitations on functionality)
  - ACMP, IADC, VDAC
- Wake-up to EM0 through
  - Peripheral interrupt, reset pin, power on reset, asynchronous pin interrupt, I2C0 address recognition
- Wake-up to EM1 through
  - Peripheral data transfer request
  - Part returns to EM3 when transfers are complete
- RAM and register values are preserved
  - RAM blocks may be optionally powered down for lower power
- GPIO pin state is retained
- Debug connectivity is unavailable by default to reduce current consumption. Debug connectivity can be enabled by setting the EM2DBGEN bit in the EMU_CTRL register, and will consume about 0.5 uA extra supply current.

13.3.1.6 EM4

EM4 is the lowest energy mode of the part. There is no retention except for GPIO PAD state and BURAM values. Wake-up from EM4 requires a reset to the system, returning it back to EM0.

- Cortex-M33 is off
- Radio is off
- High frequency clock tree is off
- Low frequency clock tree may be active
- No RAM or register values are retained, except for the BURAM.
- The following oscillators are on if used by the BURTC or ETAMPDET:
  - LFRCO, LFXO, ULFRCO
- The following low frequency peripherals are available
  - BURTC, ETAMPDET
- Wake-up to EM0 through
  - BURTC interrupt, reset pin, power on reset, asynchronous pin interrupt (on GPIO_EM4WUx pins only)
- GPIO pin state may be retained (depending on EMU->EM4CTRL.EM4IORETMODE configuration)

13.3.2 Entering Low Energy Modes

The following sections describe the requirements for entering the various energy modes.

13.3.2.1 Entry Into EM1

Energy mode EM1 is entered when the Cortex-M33 executes the Wait For Interrupt (WFI) or Wait For Event (WFE) instruction while the SLEEPDEEP bit in the Cortex-M33 System Control Register is cleared. The MCU can re-enter sleep automatically out of an Interrupt Service Routine (ISR) if the SLEEPONEXIT bit in the Cortex-M33 System Control Register is set. Refer to ARM documentation on entering Sleep modes.

Alternatively, EM1 can be entered from either EM2 or EM3 due to certain peripheral wake-up requests, allowing transfers from the peripheral to system RAM. The system will return back to EM2 or EM3 once the peripheral has completed its transfers and processing.

13.3.2.2 Entry Into EM2 or EM3

Energy mode EM2 or EM3 may be entered when **all** of the following conditions are true:

- Radio state machine is in OFF state
- Cortex-M33 (if present) is in DEEPSLEEP state
- Flash Program/Erase Inactive
- DMA done with all current requests
- A debugger is not currently connected.

  Note: The device will still enter a sleep state which emulates the behavior of EM2 or EM3 when an active debug connection is present, but it will draw more than the specified sleep current.

Energy mode EM2 is entered from EM0 when the Cortex-M33 executes the Wait For Interrupt (WFI) or Wait For Event (WFE) instruction while the SLEEPDEEP bit in the Cortex-M33 System Control Register is set. The MCU can re-enter DeepSleep automatically out of an Interrupt Service Routine (ISR) if the SLEEPONEXIT bit in the Cortex-M33 System Control Register is set. Refer to ARM documentation on entering Sleep modes.

Alternately, EM2 or EM3 is entered from EM1 upon the completion of a Peripheral Wake-Up Request from capable peripherals if no EM0 wake-up happens in the meantime.

When entering EM2 or EM3, if any peripheral on an auxiliary low power domain (PD0B, PD0C, etc.) is enabled, that auxiliary low power domain will be powered, causing higher current draw. Otherwise, the auxiliary power domain will be powered down. See 13.3.4 Power Domains for more information.

13.3.2.3 Entry Into EM4

Energy mode EM4 is entered through register access.

Software must ensure no modules are active, such as the Radio, when entering EM4.

Software may enter EM4 from EM0 by writing the sequence 2,3,2,3,2,3,2,3,2 to EM4CTRL->EM4ENTRY bit field. If the EM4BLOCK bit in WDOGn_CTRL is set, the CPU will be prevented from entering EM4 by software request.

An active debugger connection will prevent entry into EM4.

13.3.3 Exiting a Low Energy Mode

A system in EM2 and EM3 can be woken up to EM0 through regular interrupt requests from active peripherals. Since state and RAM retention is available, the EFR32 Series 2 is fully restored and can continue to operate as before it went into the Low Energy Mode.

Wake-up from EM4 is performed through a reset. Wake-up from a specific module must be enabled in that module's EM4WUEN register.

Enabled interrupts that can cause wake-up from EM2, EM3, and EM4 are shown in the following table. The wake-up triggers always return the device to EM0. Additionally, any reset source will return to EM0.

Table 13.3. Wake-Up Triggers from Low Energy Modes

Peripheral	Wake-Up Trigger	EM2	EM3	EM4
LETIMER	Any enabled interrupt	Yes	-	-
LFXO	Ready Interrupt	Yes	-	-
LFRCO	Ready Interrupt	Yes	-	-
WDOG	Any enabled interrupt	Yes	Yes	-
I^2C0	Receive address recognition	Yes	Yes	-
EUSART	Any enabled interrupt	Yes	-	-
SYSRTC	Any enabled interrupt	Yes	Yes	-
BURTC	Timeout	Yes	Yes	Yes [1]
EMU Temperature Sensor	Measured temperature outside the defined limits	Yes	Yes	-
Pin Interrupts	Transition	Yes[2]	Yes[2]	Yes [1 3]
Reset Pin	Assertion	Yes	Yes	Yes
Power	Cycle Off/On	Yes	Yes	Yes

Note:

1. Corresponding bit in the module's EM4WUEN must be set.
2. Available on Port A, Port B, and all EM4WU pins.
3. Only available on EM4WU pins.

13.3.4 Power Domains

Peripherals may exist on several independent power domains which are powered down to minimize supply current when not in use. Power domains are managed automatically by the EMU.

The lowest-energy power domain is the "high-voltage" power domain (PDHV), which supports extremely low-energy infrastructure and peripherals. Circuits powered from PDHV are always on and available in all energy modes down to EM4.

The next power domain is the low power domain (PD0), which is further divided to power subsets of peripherals. All PD0 power domains are shut down in EM4. Circuits powered from PD0 power domains may be available in EM0, EM1, EM2, and EM3.

Low power domain A (PD0A) is the base power domain for EM2 and EM3 and will always remain on in EM0-EM3. It powers the most commonly-used EM2 and EM3-capable peripherals and infrastructure required to operate in EM2 and EM3. Auxiliary PD0 power domains (PD0B, PD0C, PD0D, PD0E) power additional EM2 and EM3-capable peripherals on demand. If any peripherals on one of the auxiliary power domains is enabled, that power domain will be active in EM2 and EM3. Otherwise, the auxiliary PD0 power domains will be shut down to reduce current.

Note: Power domain PD0E is also turned on when peripherals on PD0B, PD0C, or PD0D are used.

The active power domain (PD1) powers the rest of the device circuitry, including the CPU core and EM0 / EM1 peripherals. PD1 is always powered on in EM0 and EM1. PD1 is always shut down in EM2, EM3, and EM4.

Table 13.4 Peripheral Power Subdomains on page 343 shows the peripherals on the PDHV and PD0x domains. Any peripheral not listed is on PD1.

Table 13.4. Peripheral Power Subdomains

Always On in EM2/EM3		Selectively On in EM2/3				
PDHV[1]	PD0A	PD0B[2]	PD0C[2]	PD0D[2]	PD0E	PDU
LFRCO	SYSRTC	LETIMER0	HFRCOEM23	DEBUG	GPIO	USB
LFXO	FSRCO	IADC0	HFXO	WDOG0	PRS	USBPLL0
BURTC		PCNT0		WDOG1		
BURAM		ACMP0		EUSART0		
ETAMPDET		ACMP1		I2C0		
ULFRCO		LESENSE				
		VDAC0				

Note:
1. Peripherals on PDHV are also available in EM4.
2. If any of PD0B, PD0C, or PD0D are enabled, PD0E will also be automatically enabled.

13.3.5 Voltage Scaling

The EFR32xG25 supports supply voltage scaling for the LDO powering DECOUPLE. Voltage scaling helps to optimize the energy efficiency of the system by operating at lower voltages when possible. Three supply voltage operating points are available:

Table 13.5. Voltage Scaling Options

VSCALE Setting	DECOUPLE Voltage	Operating Conditions
VSCALE2	1.1 V	EM0/EM1 Operation up to 100 MHz EM2 and EM3
VSCALE1	1.0 V	EM2 and EM3 Only
VSCALE0	0.9 V	EM2 and EM3 Only

13.3.5.1 Voltage Scaling in EM0 and EM1

In EM0 and EM1 VSCALE2 is to be used.

The current VSCALE setting can be read at any time from the EMU_STATUS_VSCALE field.

13.3.5.2 Voltage Scaling in EM2 and EM3

A separate voltage scaling value is used during EM2 and EM3. This allows the core to run at a higher voltage when in EM0 / EM1 and reduce the voltage in EM2 and EM3 for power savings. The voltage scale level for EM2 and EM3 is set using the EMU_CTRL_EMU23VSCALE field. The new voltage scaling level will be applied when the system is in EM2 or EM3, and return to the EM0 / EM1 voltage scaling level automatically when the system exits the low energy mode.

13.3.6 EM0 / EM1 Peripheral Register Retention

When the device enters EM2 or EM3, all peripherals will retain their register configurations by default. Retention for peripherals on the PD1 power domain (i.e. those which do not operate in EM2 and EM3), can optionally be disabled by setting bit 0 of the EMU_PD1PARETCTRL_PD1PARETDIS field. Disabling retention reduces the supply current in EM2 and EM3 slightly. However, the peripheral register interfaces will be reset upon exit to EM0.

Important: This feature is not currently supported by Silicon Labs software stacks. It is the responsibility of the user software to reconfigure any peripherals as necessary when the device wakes to EM0.

13.3.7 Power Configurations

In order to provide the lowest power solutions, the EFR32xG25 comes with a DC-DC module to power internal circuits. The EFR32xG25 may be operated with or without the DC-DC. When used, the DC-DC requires an external inductor and capacitor (refer to the data sheet for recommended values).

The EFR32xG25 has multiple power supply rails: a DC-DC regulator input (VREGVDD), IO Supply (IOVDD), Analog (AVDD), RF Analog Supply (RFVDD), RF Power Amplifier Supply (PAVDD), Digital LDO and flash (DVDD), and Low Voltage Digital Supply (DECOUPLE). Additional detail for each configuration and option is given in the following sections.

Due to on-chip circuitry (e.g., diodes), some power supply pins have a dependent relationship with one or more other power supply pins. These internal relationships between the external voltages applied to the various EFR32 supply pins are defined below. Exceeding the below constraints can result in damage to the device and/or increased current draw.

- VREGVDD >= DVDD

  Note: In systems not using the DC-DC converter, VREGVDD must be shorted to DVDD external to the device.

- PAVDD >= RFVDD
- DVDD >= DECOUPLE
- AVDD, IOVDD: No supply sequencing dependency. Additional leakage may occur if DVDD remains unpowered with power applied to these supplies.

Additionally, there are other system-level considerations when assigning power supplies.

- The usable range for analog signals connected to GPIO (such as IADC inputs) will be limited to the lower of AVDD and IOVDD.
- The RESETn pin has an internal pullup to the DVDD supply. If RESETn is driven by external circuitry above DVDD, additional current may flow into the pin due to this pullup.

13.3.7.1 Power Configuration 0: STARTUP

Upon power-on reset (POR), the system is configured in a safe Startup Configuration that supports all of the available Power Configurations. The Startup Configuration is shown in the simplified diagram below.

In the Startup configuration the DC-DC converter's Bypass switch is ON (i.e., the VREGVDD pin is shorted internally to the DVDD pin).

After power on, firmware can elect to turn on the DC-DC if the external hardware configuration supports it.

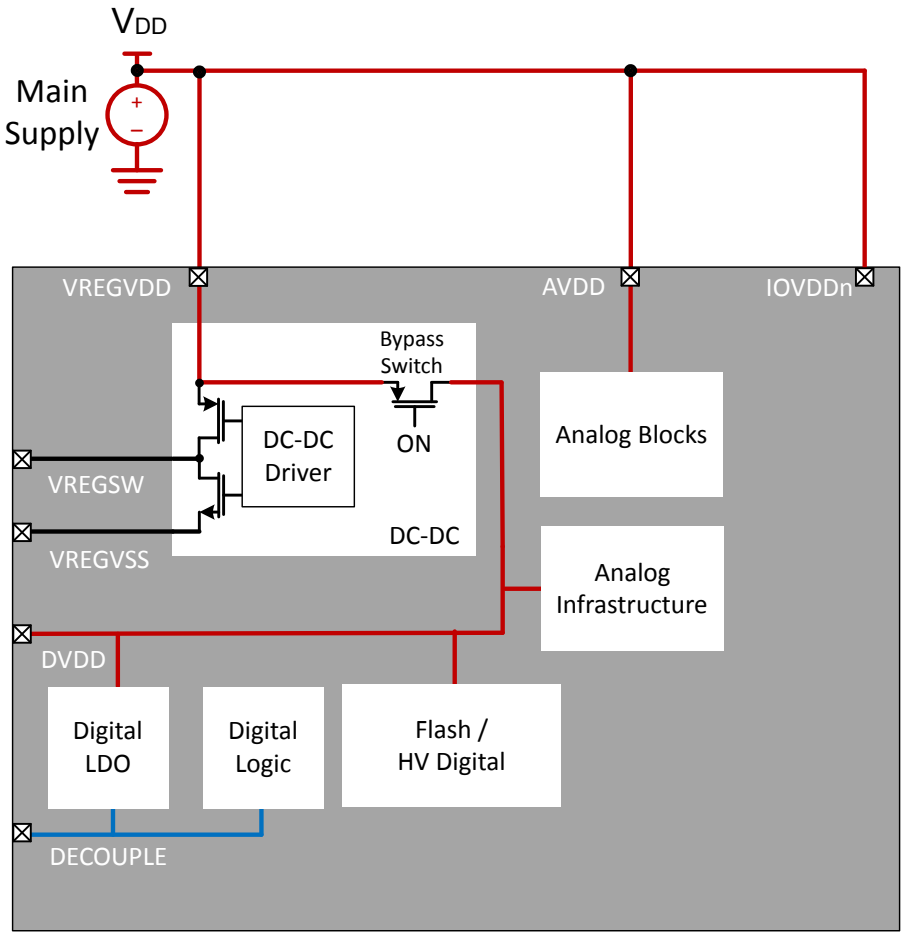


Figure 13.2. Startup Power Configuration

13.3.7.2 Power Configuration 1: No DC-DC

In Power Configuration 1, the DC-DC converter is unused, and all power is supplied by external sources. The DVDD pin must be shorted to VREGVDD.

Other supplies may be supplied by the same supply as VREGIN and DVDD (as shown in 13.3.7.2 Power Configuration 1: No DC-DC), or they may be powered from a separate source.

VREGSW must be left disconnected in this configuration.

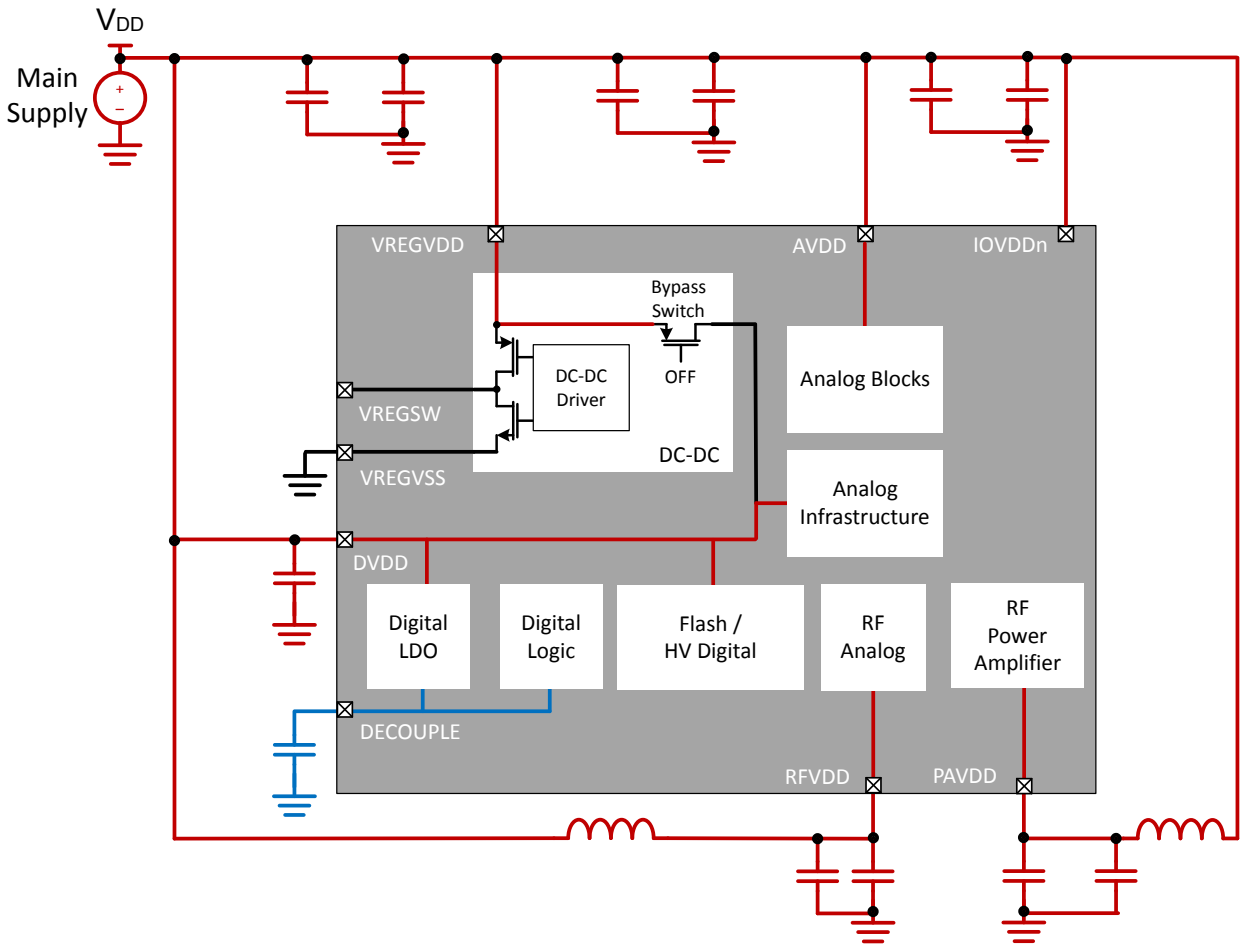


Figure 13.3. DC-DC Off Power Configuration

13.3.7.3 Power Configuration 2: DC-DC

For the lowest power applications, the DC-DC converter can be used to power the rest of the supplies on the device. When the DC-DC converter is used to regulate the voltage at DVDD, the maximum supply voltage may be limited by the operating temperature and/or the average lifetime load conditions. Refer to the device datasheet for additional details.

In Power Configuration 2, the DC-DC Output (V_{DCDC}) is connected to DVDD and optionally, to all the other supplies on the chip. In the configuration shown in Figure 13.4 DC-DC Power Configuration on page 347, the AVDD and IOVDD supplies are connected to the main supply to support higher voltage external interfaces.

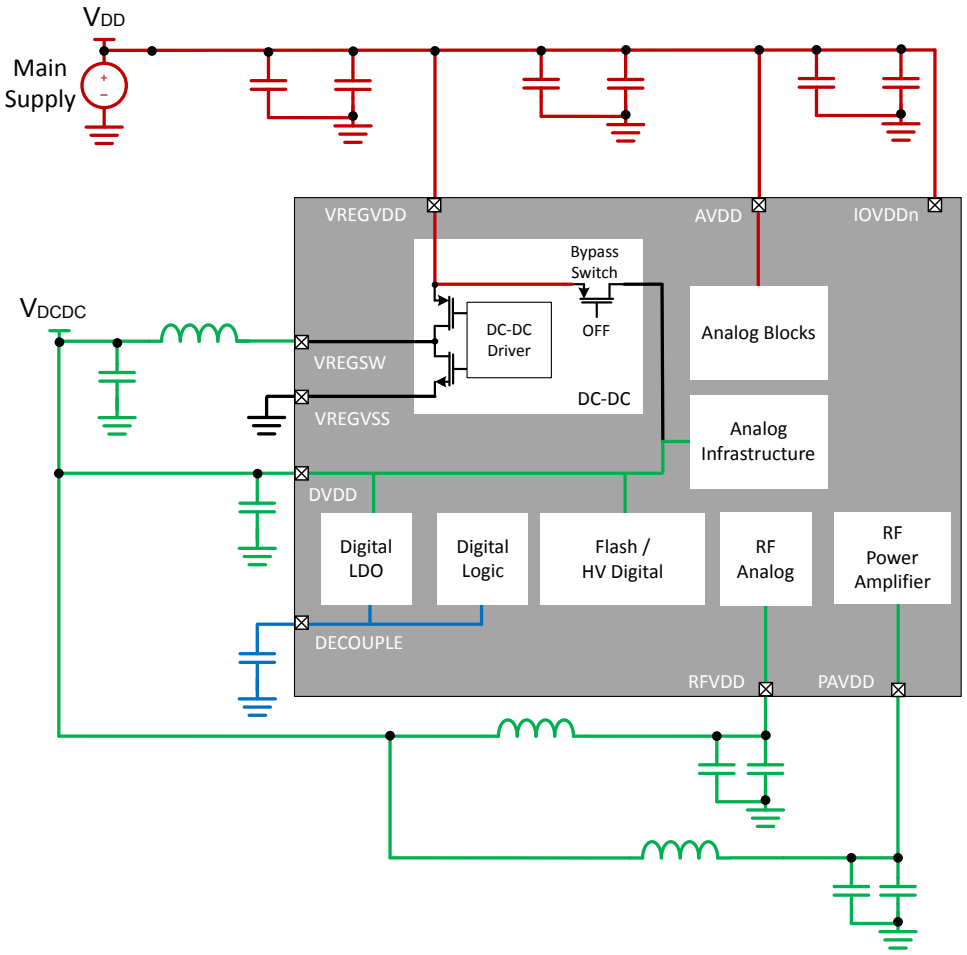


Figure 13.4. DC-DC Power Configuration

As the Main Supply voltage approaches the DC-DC output voltage, it eventually reaches a point where becomes inefficient (or impossible) for the DC-DC module to regulate V_{DCDC}. At this point, firmware can enable bypass mode, which effectively disables the DC-DC and shorts the Main Supply voltage directly to the DC-DC output. If and when sufficient voltage margin on the Main Supply returns, the system can be switched back into DC-DC regulation mode.

13.3.7.4 Power Configuration 3: DC-DC With Separate PAVDD

For power-conscious applications that require higher RF transmitter output power (> 14 dBm), PAVDD may be powered from the system supply, while the DC-DC converter can be used to power other supplies on the device. This situation is very similar to 13.3.7.3 Power Configuration 2: DC-DC, but PAVDD has been separated out to achieve higher transmitter power.

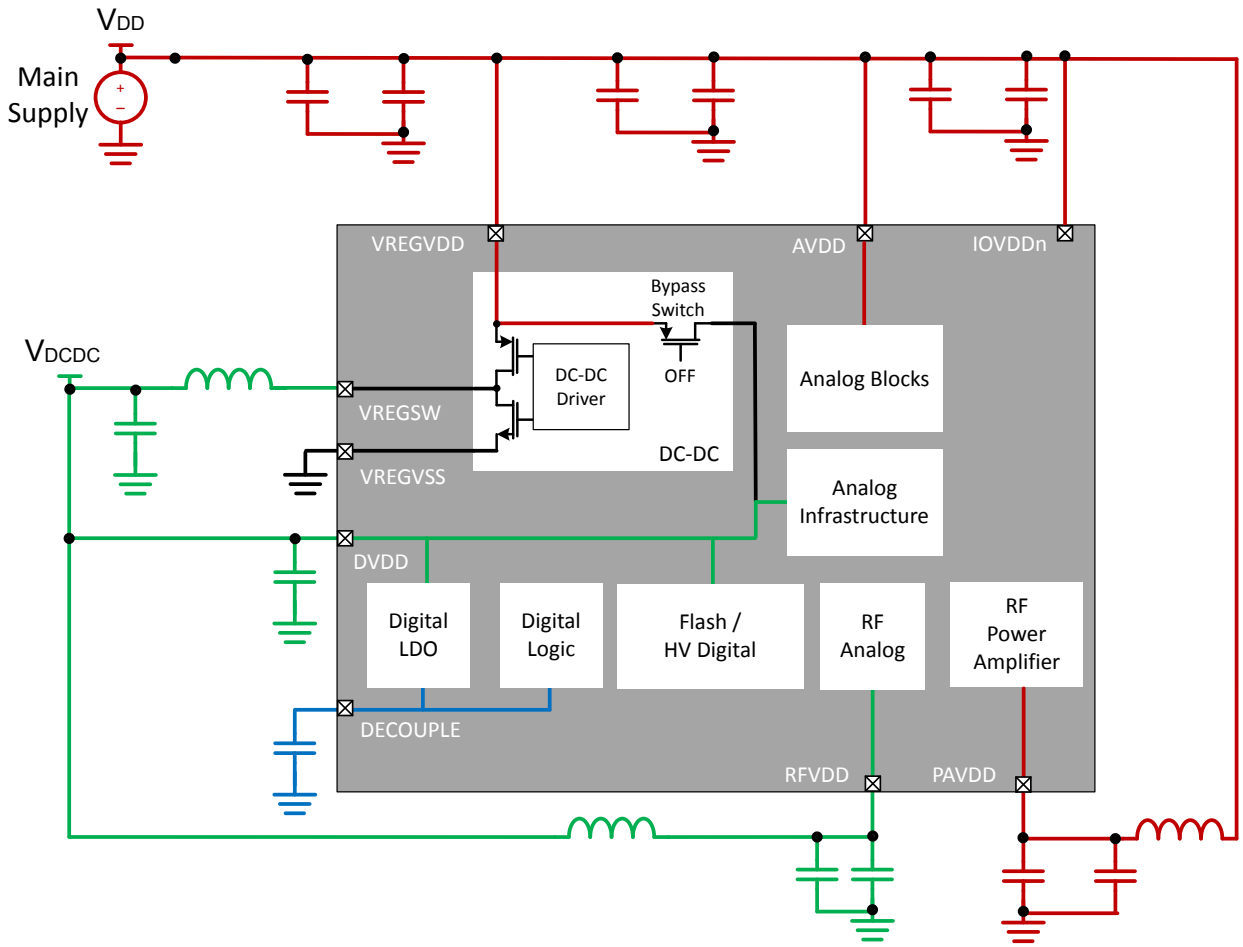


Figure 13.5. DC-DC Power Configuration With Separate PAVDD

13.3.8 Buck DC-DC Interface

The EFR32xG25 devices feature a DC-DC buck converter which requires a single external inductor and a single external capacitor. The input supply is the VREGVDD pin, and the DC-DC converter will produce a nominal 1.8 V output at the DVDD pin to power radio and MCU functions. The DC-DC converter is an efficient PFM (Pulse Frequency Modulation) architecture. In addition, the DC-DC converter supports an unregulated bypass mode, in which the input voltage is directly shorted to the DC-DC output. An integrated programmable supply monitor and dedicated interrupt allows software to enable the bypass switch when the VREGVDD supply voltage is below the minimum allowable voltage for the output current load.

The input supply VREGVDD has a maximum range between 1.8 V and 3.8 V, but is limited by application parameters, including transient current load, operating junction temperature, and the lifetime average current load.

Refer to the device datasheet for more details on the input supply voltage range.

13.3.8.1 Buck DC-DC Mode Bypass and VREGVDD Comparator

The buck DC-DC converter implements a bypass mode which shorts the VREGVDD input voltage directly to the DC-DC converter output through an internal switch. Bypass mode is enabled automatically during a power-on-reset. Bypass mode can also be enabled and disabled through software, using the DCDC_CTRL_MODE field. When set to BYPASS, the bypass switch is enabled and DC-DC regulation will be disabled. Consult the data sheet for the bypass switch impedance specification.

The EFR32xG25 includes a supply comparator circuit to help software determine when the VREGVDD supply is high enough to enable the buck DC-DC, or when to change to bypass mode. The THRESSEL field in the EMU_VREGVDDCMPCTRL register sets the comparator threshold between 2.0 and 2.3 V, and the VREGINCMPEN bit is used to enable the supply comparator. When the VREGVDD comparator is used, DCDC_STATUS_VREGIN can be read by software to determine whether VREGVDD is above or below the established threshold.

The VREGVDD comparator can also generate interrupt events when the input supply is above or below the specified threshold. The VREGINHIGHIEN and VREGINLOWIEN bits in DCDC_IEN are used to enable the above / below threshold interrupts, respectively. The VREGVDD comparator will be active and generate interrupts in EM0 and EM1 only.

The VREGVDD Comparator status is always captured and stored in RMURSTCAUSE.VREGIN on any reset event, even if the reset is not caused by VREGVDD being too low. At startup, the firmware should determine if the last reset was caused by a low VREGVDD condition by checking the following:

EMU_RSTCAUSE_VREGIN & (EMU_RMURSTCAUSE_DVDDBOD | EMU_RMURSTCAUSE_DVDDLEBOD)

If true, the part should remain in bypass mode with the DCDC disabled.

13.3.8.2 Buck DC-DC Startup

Out of power-on-reset (POR), the DC-DC converter defaults to bypass mode and the DC-DC block is disabled. Before enabling the DC-DC, software should first configure and enable the VREGVDD comparator. Once the thresholds for the VREGVDD comparator have been configured and the comparator enabled, the DCDC_STATUS.VREGIN bit should be checked to ensure that the input supply is above the threshold. When the input supply is sufficient, the DC-DC may be configured and enabled. The following steps outline this procedure:

1. Set VREGVDD comparator threshold with EMU_VREGVDDCMPCTRL.THRESSEL
2. Enable VREGVDD comparator with EMU_VREGVDDCMPCTRL.VREGINCMPEN
3. Check DCDC_STATUS.VREGIN:
   - If low, VREGIN is above the programmed threshold and it is safe to enter DC-DC mode
   - If high, VREGIN is below the programmed threshold and firmware should remain in bypass mode
4. Enable the DC-DC module with DCDC_EN_EN = 1
5. Configure the IPKVAL and DRVSPEED settings in DCDC_EM01CTRL0 and DCDC_EM23CTRL0.
6. Enable any required interrupts via DCDC_IEN.
7. Start the DC-DC by setting DCDC_CTRL.MODE to DCDCREGULATION.

The DC-DC will enter a warmup phase for approximately 100 us, then disable the bypass switch and begin using the DC-DC core to regulate the output voltage. The DCDC_IF.RUNNINGIF interrupt flag will indicate when the switch from bypass to DC-DC is complete, however this does not indicate that the output is regulated. Until the output capacitor discharges due to normal current draw from the system, the voltage may be higher than 1.8 V. The DCDC_IF.REGULATIONIF interrupt flag will indicate when the DC-DC has reached regulation and is providing the desired output voltage.

If the VREGINLOWIF interrupt occurs, software should immediately switch back to bypass mode by clearing DCDC_CTRL.MODE to BYPASS.

13.3.8.3 Buck DC-DC Recommended Configuration Settings

Certain DC-DC parameters are adjustable for fine-tuning of performance, but the majority of applications will not need to use any other than the recommended settings. All datasheet parameters are specified using the recommended settings detailed in this section. The configuration settings must be set before DC-DC regulation is started, and must not be changed while the DC-DC is active.

The DCDC_EM01CTRL0 and DCDC_EM23CTRL0 registers each have an IPKVAL field to adjust the maximum peak / load current, and a DRVSPEED field to adjust the driver speed. DCDC_EM01CTRL0 sets the configuration for EM0 and EM1 operation while DCDC_EM23CTRL0 sets the configuration for EM2 and EM3 operation. The DCDC_CTRL.IPKTMAXCTRL field adjusts the maximum time for peak current detection, which impacts the voltage ripple at the DC-DC output. The recommended settings are shown in Table 13.6 DRVSPEED, IPKVAL, and IPKMAXCTRL Recommended Settings for buck DC-DC on page 350.

Table 13.6. DRVSPEED, IPKVAL, and IPKMAXCTRL Recommended Settings for buck DC-DC

Bit Field	Recommended Setting
DCDC_EM01CTRL0.IPKVAL	9 (LOAD60MA)
DCDC_EM01CTRL0.DRVSPEED	1 (DEFAULT_SETTING)
DCDC_EM23CTRL0.IPKVAL	3 (LOAD5MA)
DCDC_EM23CTRL0.DRVSPEED	3 (BEST_EFFICIENCY)
DCDC_CTRL.IPKTMAXCTRL	4 (TMAX_1P19US)

13.3.8.4 Buck DC-DC EM4 Entry

The buck DC-DC is available in all energy modes except for EM4. If the system wants to enter EM4, the DC-DC converter must first be turned off and switched over to bypass mode. The system will not enter EM4 if the DC-DC is active. If an attempt is made to go into EM4 with DC-DC active, it will be blocked, and the DCDC_IF_EM4ERR flag will be set.

13.3.9 Brown Out Detector (BOD)

Brown out detectors ensure that the minimum supply required for the chip to operate properly and safely is provided to the EFR32xG25. Once triggered, a BOD will generate a system reset.

All BODs detect when the supply falls below a programmed threshold except DECOVMBOD (Over Voltage Monitoring),which detects when the supply goes above a predefined threshold.

All BODs except DVDDBOD and DVDDLEBOD can be individually enabled by firmware.

Table 13.7. EFR32xG25 BODs

BOD	Control Register	Supported Energy Modes	Function
DVDDBOD	n/a	EM0/1	Monitors the DVDD supply in EM0 and EM1. Hardware enables this BOD automatically in EM0/EM1 and disables it in EM2/EM3/EM4
DVDDLEBOD	n/a	EM2/3/4	Low Energy BOD monitors the DVDD supply in EM2/EM3/ EM4. DVDDLEBOD is automatically masked by hardware for ~100us after it is enabled to allow it to settle
DECBOD	EMU_DECBOD	EM0/1/2/3	Monitors the DECOUPLE supply. DECBOD is automatically masked by hardware for ~20us after it is enabled to allow it to settle.
DECOVMBOD	EMU_DECBOD	EM0/1/2/3	Monitors the DECOUPLE supply Over Voltage by detecting DECOUPLE going over a specified threshold. DECOVMBOD is automatically masked by hardware for ~20us after it is enabled to allow it to settle.
AVDDBOD	EMU_BOD3SENSE	EM0/1/2/3/4	Monitors the AVDD supply. Automatically masked by hardware for ~100us after it is enabled to allow it to settle.
IOVDD0BOD	EMU_BOD3SENSE	EM0/1/2/3/4	Monitors the IOVDD0 supply. Automatically masked by hardware for ~100us after it is enabled to allow it to settle.
IOVDD1BOD	EMU_BOD3SENSE	EM0/1/2/3/4	Monitors the IOVDD1 supply. Automatically masked by hardware for ~100us after it is enabled to allow it to settle.
IOVDD2BOD	EMU_BOD3SENSE	EM0/1/2/3/4	Monitors the IOVDD2 supply. Automatically masked by hardware for ~100us after it is enabled to allow it to settle.

13.3.10 Reset Management Unit

EMU RMU (Reset Management Unit) ensures correct reset operation. It is responsible for connecting the different reset sources to the reset lines of the EFR32xG25. After reset, the M33 loads the stack pointer and program entry point from memory and start execution.

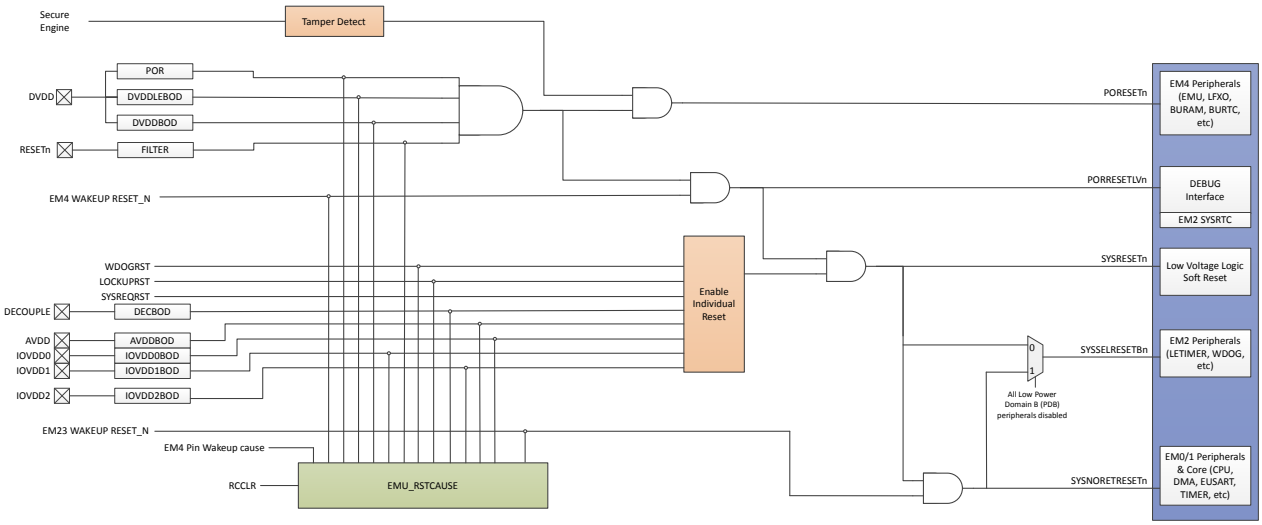


Figure 13.6. Reset Tree

There are two types of reset:

- HARD resets. Resets the entire chip. After a hard reset, the EFR32xG25 goes through its power up sequence. For reset timing specifications, please refer to the device datasheet.
- SOFT resets. Resets only some of the digital low voltage logic. Resets the MCU subsystems and peripherals but doesn't affect digital HV logic (e.g., Power control, BURTC). For reset timing specifications, please refer to the device datasheet.

EFR32xG25 Reset sources

- Power-on Reset (POR)
  - The POR ensures that EFR32xG25 does not start up before the supply voltage DVDD has reached the threshold voltage VPORthr (see Device Datasheet Electrical Characteristics for details). Before the threshold voltage is reached, EFR32xG25 is kept in reset state.
- RESET pin Reset
  - The RESETn pin includes an on-chip pull-up resistor to the DVDD supply, and can therefore be left unconnected if no external reset source is needed. Also connected to the RESETn line is a filter which prevents glitches from resetting the EFR32xG25.
- EM4 wakeup
  - System reset following EM4 exit.
- Watchdog reset
  - The Watchdog circuit is a timer which (when enabled) must be cleared by software regularly. If software does not clear it, a Watchdog reset is activated. This functionality provides recovery from a software stalemate. Refer to the Watchdog section for specifications and description.
- Core lockup condition
  - A MCU lockup is the result of the core being locked up because of an unrecoverable exception following the activation of the processor's built-in system state protection hardware.
- Software triggered reset
  - Software may initiate a reset (e.g. if it finds itself in a non-recoverable state). By asserting the SYSRESETREQ in the Application Interrupt and Reset Control Register, a reset is issued.
- Brown-Out Detection (BOD)
  - EFR32xG25 has multiple built in Brown-out detection (BOD) circuits, which monitor supply voltage level during operation. BOD circuits compare supply voltage to a programmed threshold level and issue a reset request when triggered.
- Secure Engine Tamper detection
  - Secure Engine may issue a system reset request upon tamper detection.

Whether a reset source trigger event lead to a system reset can be controlled via EMU_RMUCTRL register.

EMU_RSTCAUSE register

User can determine the cause of the last reset by querying the EMU_RSTCAUSE register. Once read, EMU_RSTCAUSE should be cleared via EMU_CMD_RCCLR.

Table 13.8. Reset Sources Summary

RSTCAUSE Bit	Name	Type	Can be Disabled?	Description
0	POR	Hard	No	Power On Reset.
1	PIN	Hard	No	Pin Reset.
2	EM4	Soft	No	EM4 Wakeup
3	WDOG0	Soft	Yes	Watchdog 0
4	WDOG1	Soft	Yes	Watchdog 1
5	LOCKUP	Soft	Yes	M33 Lockup
6	SYSREQ	Soft	Yes	M33 Core System Reset
7	DVDDBOD	Hard	No	DVDD BOD
8	DVDDLEBOD	Hard	No	DVDD LEBOD
9	DECBOD	Hard	Yes	DECOUPLE BOD
10	AVDDBOD	Soft	Yes	AVDD BOD
11	IOVDD0BOD	Soft	Yes	IOVDD 0 BOD
12	IOVDD1BOD	Soft	Yes	IOVDD 1 BOD
20	IOVDD2BOD	Soft	Yes	IOVDD 2 BOD

13.3.11 Temperature Sensor

EMU provides a low energy periodic temperature measurement. A temperature measurement is taken once every 250 ms, with the 9-bit result stored in TEMP bit-field in EMU_TEMP register. The temperature value is expressed in degrees Kelvin. EMU_TEMP_TEMPLSB represents the measured temperature fractional part (in ¼ degree Kelvin).

Note: The EMU temperature sensor is always periodically taking single temperature measurements, except in EM4 (shutoff) mode.

To obtain better noise resolution, the temperature sensor also implements a hardware averaging function, and averaged results can be requested using the EMU_CMD_TEMPAVGREQ command. When TEMPAVGREQ is set by software, the temperature sensor will take 16 or 64 samples as quickly as possible. The TEMPAVGNUM field in EMU_CTRL determines how many temperature measurements will be averaged. The averaged result is stored in the 11-bit field EMU_TEMP_TEMPAVG, which represents the full temperature with resolution of ¼ degree Kelvin.

The EMU provides the following features around temperature changes:

- Interrupt when temperature is updated (EMU_IF_TEMP)
- Interrupt when averaged temperature result is updated (EMU_IF_TEMPAVG)
- Interrupt from LOW level trip (generate interrupt EMU_IF_TEMPLOWIF when measured temperature in EMU_TEMP_TEMP is below programmed threshold EMU_TEMPLIMITS_TEMPLOW)
- Interrupt from HIGH level trip (generate interrupt EMU_IF_TEMPHIGHIF when measured temperature in EMU_TEMP_TEMP is above programmed threshold EMU_TEMPLIMITS_TEMPHI)

High and Low thresholds are specified as 9-bit degree Kelvin values and compared against the single temperature result (EMU_IF_TEMP).

Measured temperature can be converted to degrees Celsius by subtracting 273.15 ($T_{Celsius} = T_{Kelvin} - 273.15$).

13.3.11.1 Linearization, Offset Correction, and Calibration

The raw value reported by the EMU temperature sensor follows a predictable curve. The output may be linearized and the systematic offset removed to achieve die temperature readings with better than +/- 2.5 degrees C accuracy over the full operating temperature range. Further accuracy can be achieved using in-system calibration.

To linearize the measurement and correct for the systematic offset, a second or third-order polynomial equation representing the nominal curve is used. For example, a third-order correction equation takes the form:

$T_{corr} = a*x^3 + b*x^2 + c*x^1 + d$

Where:

- T_{corr} is the corrected temperature (in degrees Celsius)
- x is the measured temperature (in degrees Celsius)
- a is the x^3 term
- b is the x^2 term
- c is the x^1 term
- d is the x^0 term

Polynomial coefficients for both third and second-order polynomials are shown in Table 13.9 Polynomial Coefficients on page 353. Note that the polynomial coefficients provided assume the raw output (in Kelvin) has been converted to Celsius prior to linearization.

Table 13.9. Polynomial Coefficients

Polynomial Order	x^3 Term	x^2 Term	x^1 Term	x^0 Term
Third Order	-2.360E-7	-6.742E-5	1.028	-1.569
Second Order	n/a	-2.870E-4	1.033	-1.211

Additional accuracy may be achieved by performing an in-system calibration at known temperatures and operating conditions after linearization.

13.3.12 Register Locks

EMU EMU_LOCK (for user accessible registers) can be used to control access to the EMU_RMUCTRL, EMU_CTRL, and EMU_DECBOD registers. The DCDC_LOCK register can be used to control access to the DC-DC registers.

13.4 EMU Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x010	EMU_DECBOD	RW	DECOUPLE LVBOD Control Register
0x020	EMU_BOD3SENSE	RW	BOD3SENSE Control Register
0x03C	EMU_VREGVDDCMPCTRL	RW	DC-DC VREGVDD Comparator Control Register
0x040	EMU_PD1PARETCTRL	RW	PD1 Partial Retention Control
0x05C	EMU_IPVERSION	R	IP Version
0x060	EMU_LOCK	W	EMU Configuration Lock Register
0x064	EMU_IF	RWH INTFLAG	Interrupt Flags
0x068	EMU_IEN	RW	Interrupt Enables
0x06C	EMU_EM4CTRL	RW	EM4 Control
0x070	EMU_CMD	W	EMU Command Register
0x074	EMU_CTRL	RW	EMU Control Register
0x078	EMU_TEMPLIMITS	RW	EMU Temperature Thresholds
0x084	EMU_STATUS	RH	EMU Status Register
0x088	EMU_TEMP	RH	Temperature
0x090	EMU_RSTCTRL	RW	Reset Management Control Register
0x094	EMU_RSTCAUSE	RH	Reset Cause
0x098	EMU_TAMPERRSTCAUSE	RH	Tamper Reset Cause
0x0A0	EMU_DGIF	RWH INTFLAG	Interrupt Flags Debug
0x0A4	EMU_DGIEN	RW	Interrupt Enables Debug
0x1010	EMU_DECBOD_SET	RW	DECOUPLE LVBOD Control Register
0x1020	EMU_BOD3SENSE_SET	RW	BOD3SENSE Control Register
0x103C	EMU_VREGVDDCMPCTRL_SET	RW	DC-DC VREGVDD Comparator Control Register
0x1040	EMU_PD1PARETCTRL_SET	RW	PD1 Partial Retention Control
0x105C	EMU_IPVERSION_SET	R	IP Version
0x1060	EMU_LOCK_SET	W	EMU Configuration Lock Register
0x1064	EMU_IF_SET	RWH INTFLAG	Interrupt Flags
0x1068	EMU_IEN_SET	RW	Interrupt Enables
0x106C	EMU_EM4CTRL_SET	RW	EM4 Control
0x1070	EMU_CMD_SET	W	EMU Command Register
0x1074	EMU_CTRL_SET	RW	EMU Control Register
0x1078	EMU_TEMPLIMITS_SET	RW	EMU Temperature Thresholds
0x1084	EMU_STATUS_SET	RH	EMU Status Register
0x1088	EMU_TEMP_SET	RH	Temperature
0x1090	EMU_RSTCTRL_SET	RW	Reset Management Control Register

Offset	Name	Type	Description
0x1094	EMU_RSTCAUSE_SET	RH	Reset Cause
0x1098	EMU_TAMPERRSTCAUSE_SET	RH	Tamper Reset Cause
0x10A0	EMU_DGIF_SET	RWH INTFLAG	Interrupt Flags Debug
0x10A4	EMU_DGIEN_SET	RW	Interrupt Enables Debug
0x2010	EMU_DECBOD_CLR	RW	DECOUPLE LVBOD Control Register
0x2020	EMU_BOD3SENSE_CLR	RW	BOD3SENSE Control Register
0x203C	EMU_VREGVDDCMPCTRL_CLR	RW	DC-DC VREGVDD Comparator Control Register
0x2040	EMU_PD1PARETCTRL_CLR	RW	PD1 Partial Retention Control
0x205C	EMU_IPVERSION_CLR	R	IP Version
0x2060	EMU_LOCK_CLR	W	EMU Configuration Lock Register
0x2064	EMU_IF_CLR	RWH INTFLAG	Interrupt Flags
0x2068	EMU_IEN_CLR	RW	Interrupt Enables
0x206C	EMU_EM4CTRL_CLR	RW	EM4 Control
0x2070	EMU_CMD_CLR	W	EMU Command Register
0x2074	EMU_CTRL_CLR	RW	EMU Control Register
0x2078	EMU_TEMPLIMITS_CLR	RW	EMU Temperature Thresholds
0x2084	EMU_STATUS_CLR	RH	EMU Status Register
0x2088	EMU_TEMP_CLR	RH	Temperature
0x2090	EMU_RSTCTRL_CLR	RW	Reset Management Control Register
0x2094	EMU_RSTCAUSE_CLR	RH	Reset Cause
0x2098	EMU_TAMPER-RSTCAUSE_CLR	RH	Tamper Reset Cause
0x20A0	EMU_DGIF_CLR	RWH INTFLAG	Interrupt Flags Debug
0x20A4	EMU_DGIEN_CLR	RW	Interrupt Enables Debug
0x3010	EMU_DECBOD_TGL	RW	DECOUPLE LVBOD Control Register
0x3020	EMU_BOD3SENSE_TGL	RW	BOD3SENSE Control Register
0x303C	EMU_VREGVDDCMPCTRL_TGL	RW	DC-DC VREGVDD Comparator Control Register
0x3040	EMU_PD1PARETCTRL_TGL	RW	PD1 Partial Retention Control
0x305C	EMU_IPVERSION_TGL	R	IP Version
0x3060	EMU_LOCK_TGL	W	EMU Configuration Lock Register
0x3064	EMU_IF_TGL	RWH INTFLAG	Interrupt Flags
0x3068	EMU_IEN_TGL	RW	Interrupt Enables
0x306C	EMU_EM4CTRL_TGL	RW	EM4 Control
0x3070	EMU_CMD_TGL	W	EMU Command Register
0x3074	EMU_CTRL_TGL	RW	EMU Control Register
0x3078	EMU_TEMPLIMITS_TGL	RW	EMU Temperature Thresholds

Offset	Name	Type	Description
0x3084	EMU_STATUS_TGL	RH	EMU Status Register
0x3088	EMU_TEMP_TGL	RH	Temperature
0x3090	EMU_RSTCTRL_TGL	RW	Reset Management Control Register
0x3094	EMU_RSTCAUSE_TGL	RH	Reset Cause
0x3098	EMU_TAMPERRSTCAUSE_TGL	RH	Tamper Reset Cause
0x30A0	EMU_DGIF_TGL	RWH INTFLAG	Interrupt Flags Debug
0x30A4	EMU_DGIEN_TGL	RW	Interrupt Enables Debug

13.5 EMU Register Description

13.5.1 EMU_DECBOD - DECOUPLE LVBOD Control Register

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x1	0x0			0x1	0x0
Access																											RW	RW			RW	RW
Name																											DECOVMBODMASK	DECOVMBODEN			DECBODMASK	DECBODEN

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	DECOVMBODMASK	0x1	RW	**Over Voltage Monitor Mask**
	DECOUPLE BOD Over Voltage Monitor Mask			
4	DECOVMBODEN	0x0	RW	**Over Voltage Monitor enable**
	DECOUPLE BOD Over Voltage Monitor enable. Enables LVBOD below vref high. BOD is masked for 20us after enable			
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DECBODMASK	0x1	RW	**DECBOD Mask**
	DECOUPLE BOD Mask			
0	DECBODEN	0x0	RW	**DECBOD enable**
	DECOUPLE BOD enable. Enables LVBOD above vref low. BOD is masked for 20us after enable			

13.5.2 EMU_BOD3SENSE - BOD3SENSE Control Register

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0	0x0	0x0	0x0
Access																													RW	RW	RW	RW
Name																													IOVDD2BODEN	IOVDD1BODEN	IOVDD0BODEN	AVDDBODEN

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	IOVDD2BODEN	0x0	RW	**IOVDD2 BOD enable**
	BOD output is automatically masked for 100us by HW after enable is set			
2	IOVDD1BODEN	0x0	RW	**IOVDD1 BOD enable**
	BOD output is automatically masked for 100us by HW after enable is set			
1	IOVDD0BODEN	0x0	RW	**IOVDD0 BOD enable**
	BOD output is automatically masked for 100us by HW after enable is set			
0	AVDDBODEN	0x0	RW	**AVDD BOD enable**
	BOD output is automatically masked for 100us by HW after enable is set			

13.5.3 EMU_VREGVDDCMPCTRL - DC-DC VREGVDD Comparator Control Register

Offset	Bit Position																														
0x03C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x3		0x0
Access																														RW		RW
Name																														THRESSEL		VREGINCMPEN

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2:1	THRESSEL	0x3	RW	**VREGVDD comparator threshold programming**
	VREGVDD comparator threshold programming: 2.0->2.3V, 0.1V/step			
0	VREGINCMPEN	0x0	RW	**VREGVDD comparator enable**
	VREGVDD comparator enable. Output is masked for 5us after enabled. Automatically disabled in EM2.			

13.5.4 EMU_PD1PARETCTRL - PD1 Partial Retention Control

Offset	Bit Position																													
0x040	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									RW							
Name																									PD1PARETDIS							

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	PD1PARETDIS	0x0	RW	**Disable PD1 Partial Retention**

Select PD1 registers groups that are NOT retained in EM2/EM3. Each bit controls a register group. MCU core group is always retained. Bit[0]: Disables PD1 retention for MCU Peripherals group. Bit[1]: Disables PD1 retention for RADIO group. Bit [15:2]: Unused. Setting PD1 retention for MCU Peripherals group will also allow PD0B/C/D power domains to be turned OFF in EM23 if all peripherals on those power domains are turned off on EM23 entry

Value	Mode	Description
1	PERIPHNORETAIN	Retain associated registers when in EM2/3
2	RADIONORETAIN	Bit[1]. When set, do not retain RADIO associated registers when in EM2/3

13.5.5 EMU_IPVERSION - IP Version

Offset	Bit Position																													
0x05C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																0x4																
Access																R																
Name																IPVERSION																

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x4	R	**IP Version**
	IP Version			

13.5.6 EMU_LOCK - EMU Configuration Lock Register

Offset	Bit Position																													
0x060	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0xADE8															
Access																	W															
Name																	LOCKKEY															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LOCKKEY	0xADE8	W	**Lock Key**

Write any other value than the unlock code to lock

Value	Mode	Description
44520	UNLOCK	Unlock EMU register

13.5.7 EMU_IF - Interrupt Flags

Offset	Bit Position																															
0x064	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0	0x0		0x0			0x0					0x0	0x0	0x0	0x0																
Access	RW	RW	RW		RW			RW					RW	RW	RW	RW																
Name	TEMPHIGH	TEMPLOW	TEMP		TEMPAVG			EM23WAKEUP					IOVDD2BOD	IOVDD1BOD	IOVDD0BOD	AVDDBOD																

Bit	Name	Reset	Access	Description
31	TEMPHIGH	0x0	RW	**Temperature high Interrupt flag**
	Measured temperature above threshold			
30	TEMPLOW	0x0	RW	**Temperature low Interrupt flag**
	Measured temperature below threshold			
29	TEMP	0x0	RW	**Temperature Interrupt flag**
	Temperature Update			
28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27	TEMPAVG	0x0	RW	**Temperature Average Interrupt flag**
	Averaged Temperature Update			
26:25	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
24	EM23WAKEUP	0x0	RW	**EM23 Wake up Interrupt flag**
	EM23 wake up			
23:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19	IOVDD2BOD	0x0	RW	**IOVDD2 BOD Interrupt flag**
	IOVDD2 BOD triggered			
18	IOVDD1BOD	0x0	RW	**IOVDD1 BOD Interrupt flag**
	IOVDD1 BOD triggered			
17	IOVDD0BOD	0x0	RW	**IOVDD0 BOD Interrupt flag**
	IOVDD0 BOD triggered			
16	AVDDBOD	0x0	RW	**AVDD BOD Interrupt flag**
	AVDD BOD triggered			
15:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

13.5.8 EMU_IEN - Interrupt Enables

Offset	Bit Position																															
0x068	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0	0x0		0x0			0x0					0x0	0x0	0x0	0x0																
Access	RW	RW	RW		RW			RW					RW	RW	RW	RW																
Name	TEMPHIGH	TEMPLOW	TEMP		TEMPAVG			EM23WAKEUP					IOVDD2BOD	IOVDD1BOD	IOVDD0BOD	AVDDBOD																

Bit	Name	Reset	Access	Description
31	TEMPHIGH	0x0	RW	**Temperature high Interrupt enable**
	Measured temperature above threshold Interrupt enable			
30	TEMPLOW	0x0	RW	**Temperature low Interrupt enable**
	Measured temperature below threshold Interrupt enable			
29	TEMP	0x0	RW	**Temperature Interrupt enable**
	Temperature Update Interrupt enable			
28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27	TEMPAVG	0x0	RW	**Temperature Interrupt enable**
	Averaged Temperature Interrupt enable			
26:25	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
24	EM23WAKEUP	0x0	RW	**EM23 Wake up Interrupt enable**
	EM23 wake up Interrupt enable			
23:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19	IOVDD2BOD	0x0	RW	**IOVDD2 BOD Interrupt enable**
	IOVDD2 BOD Interrupt enable			
18	IOVDD1BOD	0x0	RW	**IOVDD1 BOD Interrupt enable**
	IOVDD1 BOD Interrupt enable			
17	IOVDD0BOD	0x0	RW	**IOVDD0 BOD Interrupt enable**
	IOVDD0 BOD Interrupt enable			
16	AVDDBOD	0x0	RW	**AVDD BOD Interrupt enable**
	AVDD BOD Interrupt enable			
15:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

13.5.9 EMU_EM4CTRL - EM4 Control

Offset	Bit Position																													
0x06C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																								0x0			0x0				0x0	
Access																								RW			RW				RW	
Name																								BOD3SENSEEM4WU			EM4IORETMODE				EM4ENTRY	

Bit	Name	Reset	Access	Description
31:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8	BOD3SENSEEM4WU	0x0	RW	**Set BOD3SENSE as EM4 wakeup** Enable BOD3SENSE as EM4 wakeup source
7:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:4	EM4IORETMODE	0x0	RW	**EM4 IO retention mode** Determine when IO retention will be applied and removed

Value	Mode	Description
0	DISABLE	No Retention: Pads enter reset state when entering EM4
1	EM4EXIT	Retention through EM4: Pads enter reset state when exiting EM4
2	SWUNLATCH	Retention through EM4 and Wakeup: software writes UNLATCH register to remove retention

3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	EM4ENTRY	0x0	RW	**EM4 entry request** This field is used to enter the Energy Mode 4 sequence. Writing the sequence 2,3,2,3,2,3,2,3,2 will enter the part into Energy Mode 4

13.5.10 EMU_CMD - EMU Command Register

Offset	Bit Position																														
0x070	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset														0x0	0x0													0x0			0x0	
Access														W(nB)	W(nB)													W(nB)			W(nB)	
Name														TAMPERRCCLR	RSTCAUSECLR													TEMPAVGREQ			EM4UNLATCH	

Bit	Name	Reset	Access	Description
31:19	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
18	TAMPERRCCLR	0x0	W(nB)	**Tamper Reset Cause Clear**
	Set this bit to clear the TAMPERRSTCAUSE register. Root access only			
17	RSTCAUSECLR	0x0	W(nB)	**Reset Cause Clear**
	Set this bit to clear the RMURSTCAUSE register			
16:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	TEMPAVGREQ	0x0	W(nB)	**Temperature Average Request**
	Request for Averaged Temperature Measurement			
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	EM4UNLATCH	0x0	W(nB)	**EM4 unlatch**
	GPIO unlatch request after EM4 wakeup. Only valid when EM4IORETMODE== SWUNLATCH			
0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

13.5.11 EMU_CTRL - EMU Control Register

Offset	Bit Position																													
0x074	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																0x0							0x2						0x0			0x0
Access																RW							RW						RW			RW
Name																FLASHPWRUPONDEMAND							EM23VSCALE						TEMPAVGNUM			EM2DBGEN

Bit	Name	Reset	Access	Description
31:17	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
16	FLASHPWRUPONDE-MAND	0x0	RW	**Enable flash on demand wakeup**
	When set, during wake up, Flash will be in power down mode until either incoming Flash data fetch or when software issue powerup command to IMEM->MSC_CMD register			
15:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	EM23VSCALE	0x2	RW	**EM2/EM3 Vscale**
	Set VSCALE value for EM2/EM3 mode			

Value	Mode	Description
0	VSCALE0	VSCALE0. 0.9v
1	VSCALE1	VSCALE1. 1.0v
2	VSCALE2	VSCALE2. 1.1v

Bit	Name	Reset	Access	Description
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	TEMPAVGNUM	0x0	RW	**Averaged Temperature samples num**
	Number of samples taken for Averaged Temperature Measurement			

Value	Mode	Description
0	N16	16 measurements
1	N64	64 measurements

Bit	Name	Reset	Access	Description
2:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	EM2DBGEN	0x0	RW	**Enable debugging in EM2**
	Force PD0B to stay on on EM2 entry. This allows debugger to remain connected in EM2.			

13.5.12 EMU_TEMPLIMITS - EMU Temperature Thresholds

Offset	Bit Position																														
0x078	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset												0x1FF																0x0				
Access												RW																RW				
Name												TEMPHIGH																TEMPLOW				

Bit	Name	Reset	Access	Description
31:25	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
24:16	TEMPHIGH	0x1FF	RW	**Temp High limit**
	Temp threshold in degree Kelvin. The TEMPHIGH interrupt flag is set when a periodic temperature measurement is equal to or higher than this value.			
15:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8:0	TEMPLOW	0x0	RW	**Temp Low limit**
	Temp threshold in degree Kelvin. The TEMPLOW interrupt flag is set when a periodic temperature measurement is equal to or lower than this value.			

13.5.13 EMU_STATUS - EMU Status Register

Offset	Bit Position																														
0x084	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																		0x0		0x0		0x0							0x0	0x0	0x0	0x0
Access																		R		R		R							R	R	R	R
Name																		EM2ENTERED		EM4IORET		RACACTIVE							TEMPAVGACTIVE	TEMPACTIVE	FIRSTTEMPDONE	LOCK

Bit	Name	Reset	Access	Description
31:15	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
14	EM2ENTERED	0x0	R	**EM2 entered**
	Confirm chip entered EM2 state. EM2 Entry request can be delayed or denied by peripherals.			
13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12	EM4IORET	0x0	R	**EM4 IO retention status**
	The status of IO retention. Will be set upon EM4 entry based on EM4IORETMODE in EMU_EM4CTRL. Cleared by setting EM4UNLATCH in EMU_CMD			
11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10	RACACTIVE	0x0	R	**RAC active**
	This bit indicates the status of the RAC state machine. System can not enter EM2 or lower if set.			
9:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	TEMPAVGACTIVE	0x0	R	**Temp Average active**
	Average Temperature Measurement active			
2	TEMPACTIVE	0x0	R	**Temp active**
	Temperature Measurement active			
1	FIRSTTEMPDONE	0x0	R	**First Temp done**
	First Temperatue mesaurement completed			
0	LOCK	0x0	R	**Lock status**
	Indicates the current status of EMU Lock			

Value	Mode	Description
0	UNLOCKED	All EMU lockable registers are unlocked.
1	LOCKED	All EMU lockable registers are locked.

13.5.14 EMU_TEMP - Temperature

Offset	Bit Position																													
0x088	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset						0x0																0x0									0x0	
Access						R																R									R	
Name						TEMPAVG																TEMP									TEMPLSB	

Bit	Name	Reset	Access	Description
31:27	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
26:16	TEMPAVG	0x0	R	**Averaged Temperature**
	Averaged Temperature Measurement. Temperature in Kelvin. 9 integer bits and 2 decimal bits (0.25 Degree resolution)			
15:11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10:2	TEMP	0x0	R	**Temperature measured**
	Temperature in Kelvin. Value of last periodic temperature measurement. Value is asynchronously updated.			
1:0	TEMPLSB	0x0	R	**Temperature measured decimal part**
	Temperature decimal part			

13.5.15 EMU_RSTCTRL - Reset Management Control Register

Offset	Bit Position																												
0x090	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																						0x1	0x0	0x0	0x0	0x0			0x0	0x1		0x1
Access																						RW	RW	RW	RW	RW			RW	RW		RW
Name																						DECBODRMODE	IOVDD2BODRMODE	IOVDD1BODRMODE	IOVDD0BODRMODE	AVDDBODRMODE			LOCKUPRMODE	SYSRMODE		WDOG0RMODE

Bit	Name	Reset	Access	Description
31:11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10	DECBODRMODE	0x1	RW	**Enable DECBOD reset**

LVBOD Reset Mode. DECOUPLE monitoring. BOD must be trimmed before it is used as a reset source.

Value	Mode	Description
0	DISABLED	Reset request is blocked
1	ENABLED	The entire device is reset

Bit	Name	Reset	Access	Description
9	IOVDD2BODRMODE	0x0	RW	**Enable IOVDD2 BOD reset**

LEBOD4 Reset Mode. IOVDD2 monitoring. BOD must be trimmed before it is used as a reset source.

Value	Mode	Description
0	DISABLED	Reset request is blocked
1	ENABLED	The entire device is reset except some EMU registers

Bit	Name	Reset	Access	Description
8	IOVDD1BODRMODE	0x0	RW	**Enable IOVDD1 BOD reset**

LEBOD3 Reset Mode. IOVDD1 monitoring. BOD must be trimmed before it is used as a reset source.

Value	Mode	Description
0	DISABLED	Reset request is blocked
1	ENABLED	The entire device is reset except some EMU registers

Bit	Name	Reset	Access	Description
7	IOVDD0BODRMODE	0x0	RW	**Enable IOVDD0 BOD reset**

LEBOD2 Reset Mode. IOVDD0 monitoring. BOD must be trimmed before it is used as a reset source.

Value	Mode	Description
0	DISABLED	Reset request is blocked
1	ENABLED	The entire device is reset except some EMU registers

Bit	Name	Reset	Access	Description
6	AVDDBODRMODE	0x0	RW	**Enable AVDD BOD reset**

Bit	Name	Reset	Access	Description
	LEBOD1 Reset Mode. AVDD monitoring. BOD must be trimmed before it is used as a reset source.			
	Value	Mode		Description
	0	DISABLED		Reset Request is block
	1	ENABLED		The entire device is reset except some EMU registers
5:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	LOCKUPRMODE	0x0	RW	**Enable M33 Lockup reset**
	Core LOCKUP Reset Mode			
	Value	Mode		Description
	0	DISABLED		Reset Request is Block
	1	ENABLED		The entire device is reset except some EMU registers
2	SYSRMODE	0x1	RW	**Enable M33 System reset**
	Core Sysreset Reset Mode			
	Value	Mode		Description
	0	DISABLED		Reset request is blocked
	1	ENABLED		Device is reset except some EMU registers
1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	WDOG0RMODE	0x1	RW	**Enable WDOG0 reset**
	WDOG0 Reset Mode			
	Value	Mode		Description
	0	DISABLED		Reset request is blocked
	1	ENABLED		The entire device is reset except some EMU registers

13.5.16 EMU_RSTCAUSE - Reset Cause

Offset	Bit Position																													
0x094	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0											0x0							0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access	R											R							R	R	R	R	R	R	R	R	R	R	R	R	R
Name	VREGIN											IOVDD2BOD							SETAMPER	IOVDD1BOD	IOVDD0BOD	AVDDBOD	DECBOD	DVDDLEBOD	DVDDBOD	SYSREQ	LOCKUP	WDOG1	WDOG0	EM4	PIN	POR

Bit	Name	Reset	Access	Description
31	VREGIN	0x0	R	**DCDC VREGIN comparator**
	DCDC VREGIN comparator below threshold. For Information only, not a direct source for reset. Should be used to determine whether the previous reset was caused by DCDC input being too low to support current load. In this case it is advised to keep the chip in BYPASS mode and check battery level before re-enabling integrated DCDC			
30:21	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
20	IOVDD2BOD	0x0	R	**LEBOD4 Reset**
	Brown Out Detector monitoring IOVDD2			
19:14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13	SETAMPER	0x0	R	**SE Tamper event Reset**
	Last reset was a SE Tamper event reset			
12	IOVDD1BOD	0x0	R	**LEBOD3 Reset**
	Brown Out Detector monitoring IOVDD1			
11	IOVDD0BOD	0x0	R	**LEBOD2 Reset**
	Brown Out Detector monitoring IOVDD0			
10	AVDDBOD	0x0	R	**LEBOD1 Reset**
	Brown Out Detector monitoring AVDD			
9	DECBOD	0x0	R	**LVBOD Reset**
	Brown Out Detector monitoring DECOUPLE			
8	DVDDLEBOD	0x0	R	**LEBOD Reset**
	Brown Out Detector monitoring DVDD in EM2/3			
7	DVDDBOD	0x0	R	**HVBOD Reset**
	Brown Out Detector monitoring DVDD in EM0/1			
6	SYSREQ	0x0	R	**M33 Core Sys Reset**
	Last Reset was as M33 Core System reset			
5	LOCKUP	0x0	R	**M33 Core Lockup Reset**
	Last Reset was as M33 Core Lockup reset			
4	WDOG1	0x0	R	**Watchdog 1 Reset**

Bit	Name	Reset	Access	Description
	Last reset was a Watchdog 1 reset			
3	WDOG0	0x0	R	**Watchdog 0 Reset**
	Last reset was a Watchdog 0 reset			
2	EM4	0x0	R	**EM4 Wakeup Reset**
	Last reset was a EM4 Wakeup			
1	PIN	0x0	R	**Pin Reset**
	Last reset was a Pin reset			
0	POR	0x0	R	**Power On Reset**
	Last reset was a Power On Reset			

13.5.17 EMU_TAMPERRSTCAUSE - Tamper Reset Cause

Offset	Bit Position																														
0x098	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	TAMPERRST																															

Bit	Name	Reset	Access	Description
31:0	TAMPERRST	0x0	R	**Tamper reset vector**
	Tamper reset vector. Reset cause indicator defining which tamper response index triggered the previous tamper reset. Cleared with TAMPERRCCLR			

13.5.18 EMU_DGIF - Interrupt Flags Debug

Offset	Bit Position																															
0x0A0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0	0x0					0x0																								
Access	RW	RW	RW					RW																								
Name	TEMPHIGHDGIF	TEMPLOWDGIF	TEMPDGIF					EM23WAKEUPDGIF																								

Bit	Name	Reset	Access	Description
31	TEMPHIGHDGIF	0x0	RW	**Temperature high Interrupt flag**
	Measured temperature above threshold			
30	TEMPLOWDGIF	0x0	RW	**Temperature low Interrupt flag**
	Measured temperature below threshold			
29	TEMPDGIF	0x0	RW	**Temperature Interrupt flag**
	Temperature Update			
28:25	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
24	EM23WAKEUPDGIF	0x0	RW	**EM23 Wake up Interrupt flag**
	EM23 wake up			
23:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

13.5.19 EMU_DGIEN - Interrupt Enables Debug

Offset	Bit Position																															
0x0A4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0	0x0					0x0																								
Access	RW	RW	RW					RW																								
Name	TEMPHIGHDGIEN	TEMPLOWDGIEN	TEMPDGIEN					EM23WAKEUPDGIEN																								

Bit	Name	Reset	Access	Description
31	TEMPHIGHDGIEN	0x0	RW	**Temperature high Interrupt enable**
	Measured temperature above threshold			
30	TEMPLOWDGIEN	0x0	RW	**Temperature low Interrupt enable**
	Measured temperature below threshold			
29	TEMPDGIEN	0x0	RW	**Temperature Interrupt enable**
	Temperature Update			
28:25	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
24	EM23WAKEUPDGIEN	0x0	RW	**EM23 Wake up Interrupt enable**
	EM23 wake up			
23:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

13.6 DCDC Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	DCDC_IPVERSION	R	IPVERSION
0x004	DCDC_CTRL	RW SYNC	Control
0x00C	DCDC_EM01CTRL0	RW SYNC	EM01 Control
0x014	DCDC_EM23CTRL0	RW SYNC	EM23 Control
0x024	DCDC_PFMXCTRL	RW SYNC	PFMX Control Register
0x02C	DCDC_IF	RWH INTFLAG	Interrupt Flags
0x030	DCDC_IEN	RW	Interrupt Enable
0x034	DCDC_STATUS	RH	Status Register
0x038	DCDC_SYNCBUSY	RH	Syncbusy Status Register
0x040	DCDC_LOCK	W	Lock Register
0x044	DCDC_LOCKSTATUS	RH	Lock Status Register
0x1000	DCDC_IPVERSION_SET	R	IPVERSION
0x1004	DCDC_CTRL_SET	RW SYNC	Control
0x100C	DCDC_EM01CTRL0_SET	RW SYNC	EM01 Control
0x1014	DCDC_EM23CTRL0_SET	RW SYNC	EM23 Control
0x1024	DCDC_PFMXCTRL_SET	RW SYNC	PFMX Control Register
0x102C	DCDC_IF_SET	RWH INTFLAG	Interrupt Flags
0x1030	DCDC_IEN_SET	RW	Interrupt Enable
0x1034	DCDC_STATUS_SET	RH	Status Register
0x1038	DCDC_SYNCBUSY_SET	RH	Syncbusy Status Register
0x1040	DCDC_LOCK_SET	W	Lock Register
0x1044	DCDC_LOCKSTATUS_SET	RH	Lock Status Register
0x2000	DCDC_IPVERSION_CLR	R	IPVERSION
0x2004	DCDC_CTRL_CLR	RW SYNC	Control
0x200C	DCDC_EM01CTRL0_CLR	RW SYNC	EM01 Control
0x2014	DCDC_EM23CTRL0_CLR	RW SYNC	EM23 Control
0x2024	DCDC_PFMXCTRL_CLR	RW SYNC	PFMX Control Register
0x202C	DCDC_IF_CLR	RWH INTFLAG	Interrupt Flags
0x2030	DCDC_IEN_CLR	RW	Interrupt Enable
0x2034	DCDC_STATUS_CLR	RH	Status Register
0x2038	DCDC_SYNCBUSY_CLR	RH	Syncbusy Status Register
0x2040	DCDC_LOCK_CLR	W	Lock Register
0x2044	DCDC_LOCKSTATUS_CLR	RH	Lock Status Register
0x3000	DCDC_IPVERSION_TGL	R	IPVERSION
0x3004	DCDC_CTRL_TGL	RW SYNC	Control

Offset	Name	Type	Description
0x300C	DCDC_EM01CTRL0_TGL	RW SYNC	EM01 Control
0x3014	DCDC_EM23CTRL0_TGL	RW SYNC	EM23 Control
0x3024	DCDC_PFMXCTRL_TGL	RW SYNC	PFMX Control Register
0x302C	DCDC_IF_TGL	RWH INTFLAG	Interrupt Flags
0x3030	DCDC_IEN_TGL	RW	Interrupt Enable
0x3034	DCDC_STATUS_TGL	RH	Status Register
0x3038	DCDC_SYNCBUSY_TGL	RH	Syncbusy Status Register
0x3040	DCDC_LOCK_TGL	W	Lock Register
0x3044	DCDC_LOCKSTATUS_TGL	RH	Lock Status Register

13.7 DCDC Register Description

13.7.1 DCDC_IPVERSION - IPVERSION

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x2																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x2	R	**IPVERSION**
	IPVERSION number			

13.7.2 DCDC_CTRL - Control

Offset	Bit Position																															
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																										0x10						0x0
Access																										RW						RW
Name																										IPKTMAXCTRL						MODE

Bit	Name	Reset	Access	Description
31:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8:4	IPKTMAXCTRL	0x10	RW	**Ton_max timeout control**
	Ton_max = (ipk_tmax_ctrl + 1)*0.07us; specifies the timeout duration when attempting to hit programmed peak current; TMAX interrupt flag gives user information whether timeout was hit before reaching peak current			
3:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	MODE	0x0	RW	**DCDC/Bypass Mode Control**
	Used to switch between bypass and dcdc regulation, this triggers a sequence of controls. IF/STATUS registers can be used to check the true status of DCDC regulator/bypass switch			

Value	Mode	Description
0	BYPASS	DCDC is OFF, bypass switch is enabled
1	DCDCREGULATION	Request DCDC regulation, bypass switch disabled

13.7.3 DCDC_EM01CTRL0 - EM01 Control

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x1		0x9				0x9			
Access																							RW		RW				RW			
Name																							DRVSPEED		IPKDECVAL				IPKVAL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	DRVSPEED	0x1	RW	**EM01 Drive Speed Setting**

Used to configure drive speed for tradeoff between EMI and Efficiency

Value	Mode	Description
0	BEST_EMI	Lowest Efficiency, Lowest EMI.. Small decrease in efficiency from default setting
1	DEFAULT_SETTING	Default Efficiency, Acceptable EMI level
2	INTERMEDIATE	Small increase in efficiency from the default setting
3	BEST_EFFICIENCY	Highest Efficiency, Highest EMI.. Small increase in efficiency from INTERMEDIATE setting

7:4	IPKDECVAL	0x9	RW	**EM01 Dec Peak Current Setting**

Used to configure dec for required peak/load current in EM01; Max load current is approximately 0.4*Ipk; ipk_dac=4*ipkdecval+round(ipktrim*(ipkdecval+6)/16);

3:0	IPKVAL	0x9	RW	**EM01 Peak Current Setting**

Used to configure for required peak/load current in EM01; Max load current is approximately 0.4*Ipk; ipk_dac=4*ipkval +round(ipktrim*(ipkval+6)/16);

Value	Mode	Description
3	LOAD36MA	Ipeak = 90mA, Iload = 36mA
4	LOAD40MA	Ipeak = 100mA, Iload = 40mA
5	LOAD44MA	Ipeak = 110mA, Iload = 44mA
6	LOAD48MA	Ipeak = 120mA, Iload = 48mA
7	LOAD52MA	Ipeak = 130mA, Iload = 52mA
8	LOAD56MA	Ipeak = 140mA, Iload = 56mA
9	LOAD60MA	Ipeak = 150mA, Iload = 60mA

13.7.4 DCDC_EM23CTRL0 - EM23 Control

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x1		0x3				0x3			
Access																							RW		RW				RW			
Name																							DRVSPEED		IPKDECVAL				IPKVAL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	DRVSPEED	0x1	RW	**EM23 Drive Speed Setting**

Used to configure drive speed for tradeoff between EMI and Efficiency

Value	Mode	Description
0	BEST_EMI	Lowest Efficiency, Lowest EMI.. Small decrease in efficiency from default setting
1	DEFAULT_SETTING	Default Efficiency, Acceptable EMI level
2	INTERMEDIATE	Small increase in efficiency from the default setting
3	BEST_EFFICIENCY	Highest Efficiency, Highest EMI.. Small increase in efficiency from INTERMEDIATE setting

7:4	IPKDECVAL	0x3	RW	**EM23 dec Peak Current Setting**

Used to configure dec for required peak/load current in EM23; Max load current is approximately 0.4*Ipk; ipk_dac=4*ipkdecval+round(ipktrim*(ipkdecval+6)/16);

3:0	IPKVAL	0x3	RW	**EM23 Peak Current Setting**

Used to configure for required peak/load current in EM23; Max load current is approximately 0.4*Ipk; ipk_dac=4*ipkval +round(ipktrim*(ipkval+6)/16);

Value	Mode	Description
3	LOAD36MA	Ipeak = 90mA, Iload = 36mA
4	LOAD40MA	Ipeak = 100mA, Iload = 40mA
5	LOAD44MA	Ipeak = 110mA, Iload = 44mA
6	LOAD48MA	Ipeak = 120mA, Iload = 48mA
7	LOAD52MA	Ipeak = 130mA, Iload = 52mA
8	LOAD56MA	Ipeak = 140mA, Iload = 56mA
9	LOAD60MA	Ipeak = 150mA, Iload = 60mA

13.7.5 DCDC_PFMXCTRL - PFMX Control Register

Offset	Bit Position																															
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																						0xC								0xC		
Access																						RW								RW		
Name																						IPKTMAXCTRL								IPKVAL		

Bit	Name	Reset	Access	Description
31:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12:8	IPKTMAXCTRL	0xC	RW	**Ton_max timeout control**
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	IPKVAL	0xC	RW	**PFMX mode Peak Current Setting** Used to configure for required peak/load current in PFMX mode; Max load current is approximately 0.4*Ipk; ipk_dac=4*ipkval+round(ipktrim*(ipkval+6)/16);

13.7.6 DCDC_IF - Interrupt Flags

Offset	Bit Position																													
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name																							PFMXMODE	PPMODE	EM4ERR	TMAX	REGULATION	VREGINHIGH	VREGINLOW	RUNNING	WARM	BYPSW

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	PFMXMODE	0x0	RW	**Entered PFMX mode**
	Entered PFMX mode			
8	PPMODE	0x0	RW	**Entered Pulse Pairing mode**
	Entered Pulse Pairing mode			
7	EM4ERR	0x0	RW	**EM4 Entry Request Error**
	EM4 entry error - software requesting EM4 entry when bypass switch is disabled			
6	TMAX	0x0	RW	**Ton_max Timeout Reached**
	Ton_max timeout was reached before peak current could be achieved			
5	REGULATION	0x0	RW	**DCDC in regulation**
	DCDC in regulation, output voltage is in range of target voltage			
4	VREGINHIGH	0x0	RW	**VREGIN above threshold**
	VREGIN/VBAT above threshold			
3	VREGINLOW	0x0	RW	**VREGIN below threshold**
	VREGIN/VBAT below threshold			
2	RUNNING	0x0	RW	**DCDC Running**
	biasen, vcmpen, buckmodeen=1, bypass switch has been turned off.. Note that DCDC might not be in regulation yet. ie output voltage may not be in range of target voltage			
1	WARM	0x0	RW	**DCDC Warmup Time Done**
	100us DCDC warmup time since biasen=1 and dcdcvcmpen=1 complete			
0	BYPSW	0x0	RW	**Bypass Switch Enabled**
	Bypass Switch Enabled			

13.7.7 DCDC_IEN - Interrupt Enable

Offset	Bit Position																													
0x030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name																							PFMXMODE	PPMODE	EM4ERR	TMAX	REGULATION	VREGINHIGH	VREGINLOW	RUNNING	WARM	BYPSW

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	PFMXMODE	0x0	RW	**PFMX Mode Interrupt Enable**
	PFMX Mode Interrupt Enable			
8	PPMODE	0x0	RW	**Pulse Pairing Mode Interrupt Enable**
	Pulse Pairing Mode Interrupt Enable			
7	EM4ERR	0x0	RW	**EM4 Entry Req Interrupt Enable**
	EM4 Entry Request Error Interrupt Enable			
6	TMAX	0x0	RW	**Ton_max Timeout Interrupt Enable**
	Ton_max Timeout Interrupt Enable			
5	REGULATION	0x0	RW	**DCDC in Regulation Interrupt Enable**
	DCDC in Regulation Interrupt Enable			
4	VREGINHIGH	0x0	RW	**VREGIN above threshold Interrupt Enable**
	VREGIN above threshold Interrupt Enable			
3	VREGINLOW	0x0	RW	**VREGIN below threshold Interrupt Enable**
	VREGIN below threshold Interrupt Enable			
2	RUNNING	0x0	RW	**DCDC Running Interrupt Enable**
	DCDC Running Interrupt Enable			
1	WARM	0x0	RW	**DCDC Warmup Time Done Interrupt Enable**
	DCDC Warmup Time Done Interrupt Enable			
0	BYPSW	0x0	RW	**Bypass Switch Enabled Interrupt Enable**
	Bypass Switch Enabled Interrupt Enable			

13.7.8 DCDC_STATUS - Status Register

Offset	Bit Position																															
0x034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0	0x0				0x0	0x0	0x0	0x0	0x0
Access																							R	R				R	R	R	R	R
Name																							PFMXMODE	PPMODE				BYPCMPOUT	VREGIN	RUNNING	WARM	BYPSW

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	PFMXMODE	0x0	R	**DCDC in PFMX mode**
	DCDC in pfmx mode			
8	PPMODE	0x0	R	**DCDC in pulse-pairing mode**
	DCDC in pulse pairing mode			
7:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	BYPCMPOUT	0x0	R	**Bypass Comparator Output**
	Bypass Comparator Output			
3	VREGIN	0x0	R	**VREGIN comparator status**
	0: VREGIN/VBAT above threshold, 1: VREGIN/VBAT below threshold			
2	RUNNING	0x0	R	**DCDC is running**
	DCDC is running (buckmodeen=1, dcdcvcmpen=1, biasen=1, bypsw=0)			
1	WARM	0x0	R	**DCDC Warmup Done**
	100us DCDC warmup time since biasen=1 and dcdcvcmpen=1 complete			
0	BYPSW	0x0	R	**Bypass Switch is currently enabled**
	Bypass switch is currently enabled			

13.7.9 DCDC_SYNCBUSY - Syncbusy Status Register

Offset	Bit Position																													
0x038	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0				0x0	0x0	0x0	0x0
Access																									R				R	R	R	R
Name																									PFMXCTRL				EM23CTRL0	EM01CTRL1	EM01CTRL0	CTRL

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7	PFMXCTRL	0x0	R	**PFMXCTRL Sync Busy Status**
	PFMXCTRL Sync Busy Status			
6:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	EM23CTRL0	0x0	R	**EM23CTRL0 Sync Busy Status**
	EM23CTRL0 Sync Busy Status			
2	EM01CTRL1	0x0	R	**EM01CTRL1 Sync Bust Status**
	EM01CTRL1 Sync Bust Status			
1	EM01CTRL0	0x0	R	**EM01CTRL0 Sync Busy Status**
	EM01CTRL0 Sync Busy Status			
0	CTRL	0x0	R	**CTRL Sync Busy Status**
	CTRL Sync Busy Status			

13.7.10 DCDC_LOCK - Lock Register

Offset	Bit Position																													
0x040	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									W							
Name																									LOCKKEY							

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LOCKKEY	0x0	W	**Configuration Lock Key**
	Write any other value than the unlock code to lock all DCDC registers			

Value	Mode	Description
43981	UNLOCKKEY	

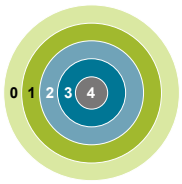
13.7.11 DCDC_LOCKSTATUS - Lock Status Register

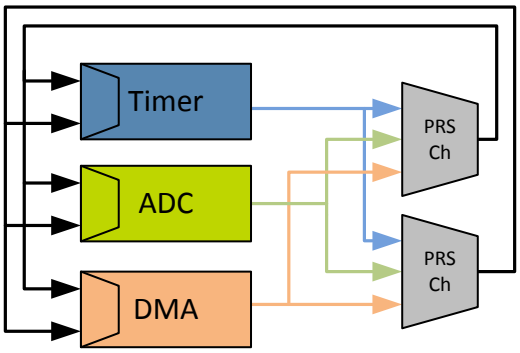
Offset	Bit Position																													
0x044	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																R
Name																																LOCK

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	LOCK	0x0	R	**Lock Status**
	Lock Status Read-Only Register			

Value	Mode	Description
0	UNLOCKED	Unlocked State
1	LOCKED	LOCKED STATE

14. PRS - Peripheral Reflex System





Quick Facts

What?

The PRS (Peripheral Reflex System) allows configurable, fast, and autonomous communication between peripherals.

Why?

Events and signals from one peripheral can be used as input signals to trigger actions in other peripherals. PRS reduces latency and ensures predictable timing by reducing software overhead and thus current consumption.

How?

Without CPU intervention the peripherals can send reflex signals to each other in single- or chained steps. The peripherals can be set up to perform actions based on the incoming reflex signals. This results in improved system performance and reduced energy consumption.

14.1 Introduction

The Peripheral Reflex System is a signal routing network allowing direct communication between different peripheral modules without involving the CPU. Peripheral modules which send out reflex signals to the PRS are called producers, and modules accepting reflex signals are called consumers. The PRS routes the reflex signals from producer to consumer peripherals, which perform actions depending on the reflex signals received.

14.2 Features

12 configurable asynchronous channels

- Each channel can be connected to any producer
- Consumers can be configured to listen to any asynchronous channel
- Can generate events to the CPU and the DMA
- Software controlled channel output using the SWPULSE and SWLEVEL registers
- Configurable logic to implement combinational functions between channels; multiple channels may be cascaded to produce more complex functions

4 configurable synchronous channels

- Special set of channels for high speed signalling between IADC and TIMER blocks

14.3 Functional Description

The PRS contains 12 asynchronous and 4 synchronous reflex channels. An overview of an asynchronous PRS reflex channel is shown in Figure 14.1 PRS Asynchronous Channel Overview on page 388. Synchronous channels are similar but do not include the configurable logic block or SWLEVEL / SWPULSE features. Asynchronous channels can be connected to any signal offered by the producers while the synchronous channels are restricted to special signals from the TIMER, IADC, and VDAC modules.

Similarly on the consumer side, all the peripherals can listen to asynchronous channels while only the TIMER, IADC, and VDAC modules can listen to synchronous channels. The consumers of a channel (synchronous or asynchronous) can choose which PRS channel to listen to and perform actions based on the reflex signals routed through that channel. Synchronous channels are only available in EM0 and EM1 while asynchronous channels are available in EM0, EM1, EM2 and EM3.

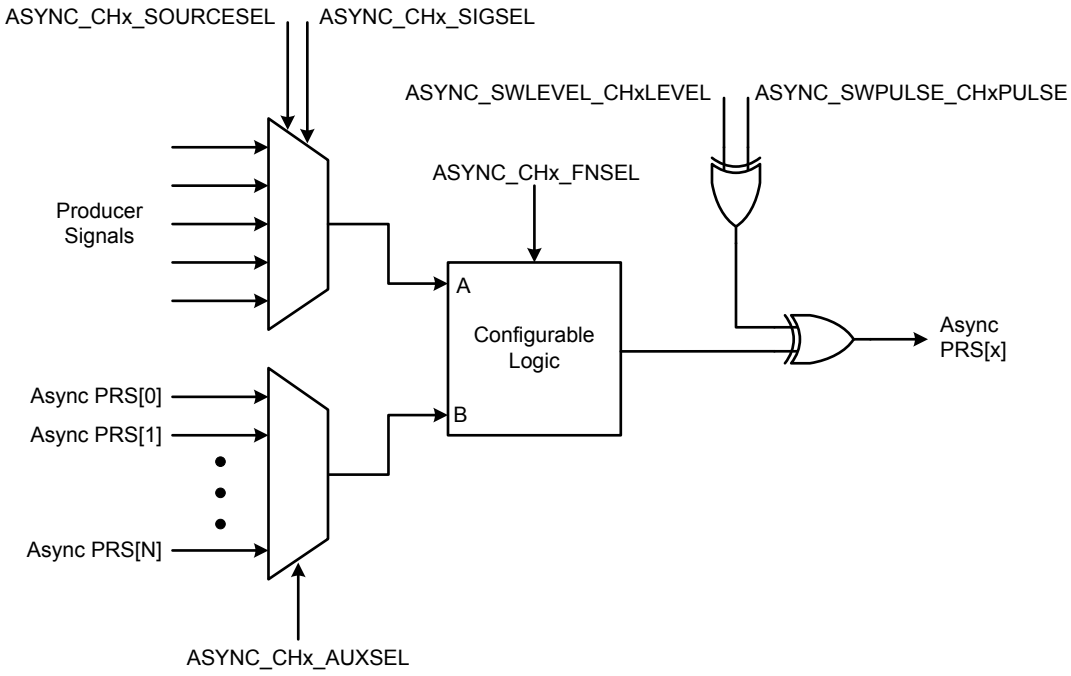


Figure 14.1. PRS Asynchronous Channel Overview

14.3.1 Asynchronous Channel Functions

Different functions can be applied to a reflex signal within the PRS. The asynchronous PRS channels can be manually triggered by writing to PRS_ASYNC_SWPULSE or PRS_ASYNC_SWLEVEL. SWLEVEL[n] is a programmable level for each asynchronous channel and holds the value it is programmed to. Setting SWPULSE[n] will cause the asynchronous channel to output a high pulse that is one EM01GRPACLK clock cycle wide. The SWLEVEL[n] and SWPULSE[n] signals are then XOR'ed with the output from the configurable logic block to form the output signal and is sent to the channel selection logic for every consumer signal. For example, when SWLEVEL[n] is set, if configurable logic produces a signal of 1, this will cause a channel output of 0.

14.3.2 Configurable Logic

The configurable logic feature enables a PRS channel to perform logic operations on the signal coming from the selected producer. Every asynchronous channel has a configurable logic block that can be programmed using the FNSEL field in the asynchronous channel control register. The configurable logic block for each channel has two inputs. Input A is the signal from the selected producer determined by SOURCESEL and SIGSEL of PRS_ASYNCHn_CTRL. Input B may be selected from the output of any other asynchronous PRS channel using the ASYNC_CHx_AUXSEL field. This allows for more complex logic functions to be created using multiple PRS channels.

Table 14.1. Configurable Logic Look up Table

A	B	FNSEL
0	0	FNSEL[0]
0	1	FNSEL[1]
1	0	FNSEL[2]
1	1	FNSEL[3]

The configurable logic feature is implemented as a 2 input look up table, with each bit of FNSEL representing the outcome for a specific input combination (see Table 14.1 Configurable Logic Look up Table on page 389). For example, if input A is 0 and input B is 1, then the PRS output will assume the value of bit 1 of FNSEL (FNSEL[1]).

To calculate the FNSEL field for an "A NAND B" function, the truth table can be filled out as:

Table 14.2. A NAND B Example

A	B	FNSEL = (A NAND B)
0	0	FNSEL[0] = 1
0	1	FNSEL[1] = 1
1	0	FNSEL[2] = 1
1	1	FNSEL[3] = 0

In this example, the value of FNSEL has been calculated to be 0111 (binary), or 0x7.

Using the FNSEL field, a total of 16 two-input logic functions can be implemented, as shown in Table 14.3 List of Logic Functions on page 389.

Table 14.3. List of Logic Functions

FNSEL value	Implemented Function
0x0	0
0x1	A NOR B
0x2	(NOT A) AND B
0x3	NOT A
0x4	A AND (NOT B)
0x5	(NOT B)
0x6	A XOR B
0x7	A NAND B
0x8	A AND B
0x9	A XNOR B

FNSEL value	Implemented Function
0xA	B
0xB	(NOT A) OR B
0xC	A
0xD	A OR (NOT B)
0xE	A OR B
0xF	1

The default value of FNSEL is 0xC, meaning that the input from the selected producer goes through unchanged. This feature can be used to combine multiple channels to get even more complex functions.

14.3.3 Producers

Through SOURCESEL in PRS_SYNCHx_CTRL or PRS_ASYNCHx_CTRL, each PRS channel (synchronous and asynchronous respectively) selects its signal producers. Each producer outputs one or more signals which can be selected by setting the SIGSEL field. Setting the SOURCESEL bits to 0 (Off) leads to a constant 0 output from the input mux regardless of SIGSEL.

The GPIO producer signals depend on settings in the GPIO module. They are selected using the edge interrupt configuration settings described in 24.3.10.1 Standard Interrupt Generation. PIN0 uses settings for the EXTI0 interrupt, PIN1 uses settings for EXTI1, and so on.

For example, to route PB00 as a producer for PRS channel 2, EXTI0, EXTI1, EXTI2, or EXTI3 should be configured to connect to PB00, and the corresponding GPIO PINx should be selected as the PRS channel 2 producer. If we choose EXTI1 via PRS producer "GPIO PIN1":

1. GPIO_EXTIPSELL_EXTIPSEL1 = PORTB, and GPIO_EXTIPINSELL_EXTIPINSEL1 = PIN0 connect PB00 through the EXTI1 signal.
2. PRS_ASYNC_CH2_CTRL_SOURCESEL = GPIO, and PRS_ASYNC_CH2_CTRL_SIGSEL = PIN1 connects the PIN1 (EXTI1) signal to asynchronous PRS channel 2 as a producer.

14.3.3.1 Producer Details

Table 14.4. Synchronous PRS Producers

Peripheral	SOURCESEL	Signal	SIGSEL
TIMER0	TIMER0 (0x01)	UF	0x0
		OF	0x1
		CC0	0x2
		CC1	0x3
		CC2	0x4
TIMER1	TIMER1 (0x02)	UF	0x0
		OF	0x1
		CC0	0x2
		CC1	0x3
		CC2	0x4
IADC0	IADC0 (0x03)	SCANENTRYDONE	0x0
		SCANTABLEDONE	0x1
		SINGLEDONE	0x2
TIMER2	TIMER2 (0x04)	UF	0x0
		OF	0x1
		CC0	0x2
		CC1	0x3
		CC2	0x4
TIMER3	TIMER3 (0x05)	UF	0x0
		OF	0x1
		CC0	0x2
		CC1	0x3
		CC2	0x4
TIMER4	TIMER4 (0x06)	UF	0x0
		OF	0x1
		CC0	0x2
		CC1	0x3
		CC2	0x4
VDAC0	VDAC0 (0x07)	CH0DONESYNC	0x0
		CH1DONESYNC	0x1

Peripheral	SOURCESEL	Signal	SIGSEL
TIMER5	TIMER5 (0x08)	UF	0x0
		OF	0x1
		CC0	0x2
		CC1	0x3
		CC2	0x4
TIMER6	TIMER6 (0x09)	UF	0x0
		OF	0x1
		CC0	0x2
		CC1	0x3
		CC2	0x4
TIMER7	TIMER7 (0x0A)	UF	0x0
		OF	0x1
		CC0	0x2
		CC1	0x3
		CC2	0x4

Table 14.5. Asynchronous PRS Producers

Peripheral	SOURCESEL	Signal	SIGSEL
IADC0	IADC0 (0x01)	SCANENTRYDONE	0x0
		SCANTABLEDONE	0x1
		SINGLEDONE	0x2
LETIMER0	LETIMER0 (0x02)	CH0	0x0
		CH1	0x1
BURTC	BURTC (0x03)	COMP	0x0
		OVERFLOW	0x1
GPIO	GPIO (0x04)	PIN0	0x0
		PIN1	0x1
		PIN2	0x2
		PIN3	0x3
		PIN4	0x4
		PIN5	0x5
		PIN6	0x6
		PIN7	0x7
CMU	CMUL (0x05)	CLKOUT0	0x0
		CLKOUT1	0x1
		CLKOUT2	0x2

Peripheral	SOURCESEL	Signal	SIGSEL
PRS	PRSL (0x08)	ASYNCH0	0x0
		ASYNCH1	0x1
		ASYNCH2	0x2
		ASYNCH3	0x3
		ASYNCH4	0x4
		ASYNCH5	0x5
		ASYNCH6	0x6
		ASYNCH7	0x7
	PRS (0x09)	ASYNCH8	0x0
		ASYNCH9	0x1
		ASYNCH10	0x2
		ASYNCH11	0x3
ACMP0	ACMP0 (0x0A)	OUT	0x0
ACMP1	ACMP1 (0x0B)	OUT	0x0
VDAC0	VDAC0L (0x0C)	CH0WARM	0x0
		CH1WARM	0x1
		CH0DONEASYNC	0x2
		CH1DONEASYNC	0x3
		INTERNALTIMEROF	0x4
		REFRESHTIMEROF	0x5
PCNT0	PCNT0 (0x0E)	DIR	0x0
		UFOF	0x1
SYSRTC0	SYSRTC0 (0x0F)	GRP0OUT0	0x0
		GRP0OUT1	0x1
		GRP1OUT0	0x2
		GRP1OUT1	0x3
LESENSE	LESENSE (0x10)	DECOUT0	0x0
		DECOUT1	0x1
		DECOUT2	0x2
		DECCMP	0x3
HFXO0	HFXO0L (0x11)	STATUS	0x0
		STATUS1	0x1

Peripheral	SOURCESEL	Signal	SIGSEL
EUSART0	EUSART0L (0x13)	CS	0x0
		IRDATX	0x1
		RTS	0x2
		RXDATAV	0x3
		TX	0x4
		TXC	0x5
		RXFL	0x6
		TXFL	0x7
ETAMPDET	ETAMPDET (0x15)	TAMPERSRCETAMPDET	0x0
TIMER0	TIMER0 (0x20)	UF	0x0
		OF	0x1
		CC0	0x2
		CC1	0x3
		CC2	0x4
TIMER1	TIMER1 (0x21)	UF	0x0
		OF	0x1
		CC0	0x2
		CC1	0x3
		CC2	0x4
TIMER2	TIMER2 (0x22)	UF	0x0
		OF	0x1
		CC0	0x2
		CC1	0x3
		CC2	0x4
TIMER3	TIMER3 (0x23)	UF	0x0
		OF	0x1
		CC0	0x2
		CC1	0x3
		CC2	0x4
CORE	CORE (0x24)	CTIOUT0	0x0
		CTIOUT1	0x1
		CTIOUT2	0x2
		CTIOUT3	0x3

Peripheral	SOURCESEL	Signal	SIGSEL
AGC	AGCL (0x25)	CCA	0x0
		CCAREQ	0x1
		GAINADJUST	0x2
		GAINOK	0x3
		GAINREDUCED	0x4
		IFPKI1	0x5
		IFPKQ2	0x6
		IFPKRST	0x7
	AGC (0x26)	PEAKDET	0x0
		PROPAGATED	0x1
		RSSIDONE	0x2
BUFC	BUFCL (0x27)	AHBMBUSY	0x4
		HOSTCLKREQ	0x5
		BUFBUSY0	0x7
	BUFC (0x28)	BUFBUSY1	0x0
		BUFBUSY2	0x1
		BUFBUSY3	0x2

Peripheral	SOURCESEL	Signal	SIGSEL
MODEM	MODEML (0x29)	ADVANCE	0x0
		ANT0	0x1
		ANT1	0x2
		COHDSADET	0x3
		COHDSALIVE	0x4
		DCLK	0x5
		DOUT	0x6
		FRAMEDET	0x7
	MODEM (0x2A)	FRAMESENT	0x0
		LOWCORR	0x1
		LRDSADET	0x2
		LRDSALIVE	0x3
		NEWSYMBOL	0x4
		NEWWND	0x5
		POSTPONE	0x6
		PREDET	0x7
	MODEMH (0x2B)	PRESENT	0x0
		RSSIJUMP	0x1
		SYNCSENT	0x2
		TIMDET	0x3
		WEAK	0x4
		EOF	0x5
FRC	FRC (0x2C)	DCLK	0x0
		DOUT	0x1

Peripheral	SOURCESEL	Signal	SIGSEL
PROTIMER	PROTIMERL (0x2D)	BOF	0x0
		CC0	0x1
		CC1	0x2
		CC2	0x3
		CC3	0x4
		CC4	0x5
		LBTF	0x6
		LBTR	0x7
	PROTIMER (0x2E)	LBTS	0x0
		POF	0x1
		T0MATCH	0x2
		T0UF	0x3
		T1MATCH	0x4
		T1UF	0x5
		WOF	0x6
SYNTH	SYNTH (0x2F)	MUX0	0x0
		MUX1	0x1
RAC	RACL (0x30)	ACTIVE	0x0
		LNAEN	0x1
		PAEN	0x2
		RX	0x3
		TX	0x4
		CTIOUT0	0x5
		CTIOUT1	0x6
		CTIOUT2	0x7
	RAC (0x31)	CTIOUT3	0x0
		AUXADCDATA	0x1
		AUXADCDATAVALID	0x2
TIMER4	TIMER4 (0x32)	UF	0x0
		OF	0x1
		CC0	0x2
		CC1	0x3
		CC2	0x4

Peripheral	SOURCESEL	Signal	SIGSEL
EUSART1	EUSART1L (0x33)	CS	0x0
		IRDATX	0x1
		RTS	0x2
		RXDATAV	0x3
		TX	0x4
		TXC	0x5
		RXFL	0x6
		TXFL	0x7
EUSART2	EUSART2L (0x35)	CS	0x0
		IRDATX	0x1
		RTS	0x2
		RXDATAV	0x3
		TX	0x4
		TXC	0x5
		RXFL	0x6
		TXFL	0x7
EUSART3	EUSART3L (0x37)	CS	0x0
		IRDATX	0x1
		RTS	0x2
		RXDATAV	0x3
		RXFL	0x4
		TX	0x5
		TXC	0x6
		TXFL	0x7
EUSART4	EUSART4L (0x39)	CS	0x0
		IRDATX	0x1
		RTS	0x2
		RXDATAV	0x3
		RXFL	0x4
		TX	0x5
		TXC	0x6
		TXFL	0x7
TIMER5	TIMER5 (0x3B)	UF	0x0
		OF	0x1
		CC0	0x2
		CC2	0x3
		CC1	0x4

Peripheral	SOURCESEL	Signal	SIGSEL
TIMER6	TIMER6 (0x3C)	UF	0x0
		OF	0x1
		CC0	0x2
		CC1	0x3
		CC2	0x4
TIMER7	TIMER7 (0x3D)	UF	0x0
		OF	0x1
		CC0	0x2
		CC1	0x3
		CC2	0x4
RFFPLL0	RFFPLL0L (0x3E)	CLKDIGDIV4	0x0
		CLKMODEMDIV4	0x1
FEFILT0	FEFILT0 (0x40)	REMPTY	0x0
		WFULL	0x1
FEFILT1	FEFILT1 (0x41)	REMPTY	0x0
		WFULL	0x1
SMCTRL	SMCTRLL (0x42)	SOFTM0	0x0
		SOFTM1	0x1
		SOFTM2	0x2
		SOFTM3	0x3
		SOFTM4	0x4
		SOFTM5	0x5
		SOFTM6	0x6
		SOFTM7	0x7
	SMCTRL (0x43)	SOFTM8	0x0
		SOFTM9	0x1
		SOFTM10	0x2
		SOFTM11	0x3

14.3.4 Consumers

Consumer peripherals can be set to listen to a PRS channel and perform an action based on the signal received on that channel. This is done by programming the PRSSEL or SPRSSEL in the consumer registers. SPRSSEL is only present for signals with the ability to listen to synchronous channels. The consumer registers follow the naming convention PRS_CONSUMER_<peripheral_name>_<signal_name>. For example, the PRS_CONSUMER_TIMER0_CC0 register is used to select which PRS channel output is sent to the TIMER0 peripheral's CC0 signal. In turn, the target peripheral should be configured to use the associated PRS trigger as desired. This is described in the individual peripheral chapters.

Note: When configuring the synchronous PRS consumer registers, the target peripheral should be disabled or configured to not use the affected PRS signal. This will ensure that no false triggers occur at the consumer.

14.3.4.1 Event on PRS

The PRS can be used to send events to the MCU to wake the system. This is very useful in combination with the Wait For Event (WFE) instruction. Any asynchronous PRS channel can be selected for this using PRSSEL in PRS_CONSUMER_CORE_M33RXEV.

Using this feature, one can e.g. set up a timer to trigger an event to the MCU periodically, every time letting the MCU continue from a WFE instruction in its program. This can help in performance-critical sections where timing is known, and the goal is to wait for an event, execute some code, then wait for another event, execute some code, and so on.

14.3.4.2 DMA Request on PRS

Up to two independent DMA requests can be generated by the PRS. The PRS asynchronous channels triggering the DMA requests are selected with the PRSSEL fields in the PRS_CONSUMER_LDMAXBAR_DMAREQx registers.The requests are set whenever the selected asynchronous PRS outputs are high.

14.4 PRS Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	PRS_IPVERSION	R	PRS IPVERSION
0x008	PRS_ASYNC_SWPULSE	W	Software Pulse Register
0x00C	PRS_ASYNC_SWLEVEL	RW	Software Level Register
0x010	PRS_ASYNC_PEEK	RH	Async Channel Values
0x014	PRS_SYNC_PEEK	RH	Sync Channel Values
0x018	PRS_ASYNC_CHx_CTRL	RW	Async Channel Control Register
0x048	PRS_SYNC_CHx_CTRL	RW	Sync Channel Control Register
0x058	PRS_CONSUM-ER_CMU_CALDN	RW	CALDN Consumer Register
0x05C	PRS_CONSUMER_CMU_CAL-UP	RW	CALUP Consumer Register
0x060	PRS_CONSUMER_EU-SART0_CLK	RW	CLK Consumer Register
0x064	PRS_CONSUMER_EU-SART0_RX	RW	RX Consumer Register
0x068	PRS_CONSUMER_EU-SART0_TRIGGER	RW	TRIGGER Consumer Register
0x06C	PRS_CONSUMER_EU-SART1_CLK	RW	CLK Consumer Register
0x070	PRS_CONSUMER_EU-SART1_RX	RW	RX Consumer Register
0x074	PRS_CONSUMER_EU-SART1_TRIGGER	RW	TRIGGER Consumer Register
0x078	PRS_CONSUMER_EU-SART2_CLK	RW	CLK Consumer Register
0x07C	PRS_CONSUMER_EU-SART2_RX	RW	RX Consumer Register
0x080	PRS_CONSUMER_EU-SART2_TRIGGER	RW	TRIGGER Consumer Register
0x084	PRS_CONSUMER_EU-SART3_CLK	RW	CLK Consumer Register
0x088	PRS_CONSUMER_EU-SART3_RX	RW	RX Consumer Register
0x08C	PRS_CONSUMER_EU-SART3_TRIGGER	RW	TRIGGER Consumer Register
0x090	PRS_CONSUMER_EU-SART4_CLK	RW	CLK Consumer Register
0x094	PRS_CONSUMER_EU-SART4_RX	RW	RX Consumer Register
0x098	PRS_CONSUMER_EU-SART4_TRIGGER	RW	TRIGGER Consumer Register

Offset	Name	Type	Description
0x09C	PRS_CONSUMER_FRC_RXRAW	RW	RXRAW Consumer Register
0x0A0	PRS_CONSUMER_IADC0_SCANTRIGGER	RW	SCAN Consumer Register
0x0A4	PRS_CONSUMER_IADC0_SINGLETRIGGER	RW	SINGLE Consumer Register
0x0A8	PRS_CONSUMER_LDMAXBAR_DMAREQ0	RW	DMAREQ0 Consumer Register
0x0AC	PRS_CONSUMER_LDMAXBAR_DMAREQ1	RW	DMAREQ1 Consumer Register
0x0B0	PRS_CONSUMER_LESENSE_DECIN0	RW	DECIN0 Consumer Register
0x0B4	PRS_CONSUMER_LESENSE_DECIN1	RW	DECIN1 Consumer Register
0x0B8	PRS_CONSUMER_LESENSE_DECIN2	RW	DECIN2 Consumer Register
0x0BC	PRS_CONSUMER_LESENSE_DECIN3	RW	DECIN3 Consumer Register
0x0C0	PRS_CONSUMER_LESENSE_START	RW	START Consumer Register
0x0C4	PRS_CONSUMER_LETIMER0_CLEAR	RW	CLEAR Consumer Register
0x0C8	PRS_CONSUMER_LETIMER0_START	RW	START Consumer Register
0x0CC	PRS_CONSUMER_LETIMER0_STOP	RW	STOP Consumer Register
0x0D0	PRS_CONSUMER_MODEM_DIN	RW	DIN Consumer Register
0x0D4	PRS_CONSUMER_PCNT0_S0IN	RW	S0IN Consumer Register
0x0D8	PRS_CONSUMER_PCNT0_S1IN	RW	S1IN Consumer Register
0x108	PRS_CONSUMER_RAC_CLR	RW	CLR Consumer Register
0x10C	PRS_CONSUMER_RAC_CTIIN0	RW	CTI Consumer Register
0x110	PRS_CONSUMER_RAC_CTIIN1	RW	CTI Consumer Register
0x114	PRS_CONSUMER_RAC_CTIIN2	RW	CTI Consumer Register
0x118	PRS_CONSUMER_RAC_CTIIN3	RW	CTI Consumer Register
0x11C	PRS_CONSUMER_RAC_FORCETX	RW	FORCETX Consumer Register
0x120	PRS_CONSUMER_RAC_RXDIS	RW	RXDIS Consumer Register
0x124	PRS_CONSUMER_RAC_RXEN	RW	RXEN Consumer Register
0x128	PRS_CONSUMER_RAC_TXEN	RW	TXEN Consumer Register
0x12C	PRS_CONSUMER_SETAMPER_TAMPERSRC26	RW	TAMPERSRC26 Consumer Register

Offset	Name	Type	Description
0x130	PRS_CONSUMER_SETAM-PER_TAMPERSRC27	RW	TAMPERSRC27 Consumer Register
0x134	PRS_CONSUMER_SETAM-PER_TAMPERSRC28	RW	TAMPERSRC28 Consumer Register
0x138	PRS_CONSUMER_SETAM-PER_TAMPERSRC29	RW	TAMPERSRC29 Consumer Register
0x13C	PRS_CONSUMER_SETAM-PER_TAMPERSRC30	RW	TAMPERSRC30 Consumer Register
0x140	PRS_CONSUMER_SETAM-PER_TAMPERSRC31	RW	TAMPERSRC31 Consumer Register
0x144	PRS_CONSUM-ER_SYSRTC0_IN0	RW	IN0 Consumer Register
0x148	PRS_CONSUM-ER_SYSRTC0_IN1	RW	IN1 Consumer Register
0x14C	PRS_CONSUMER_HFXO0_OS-CREQ	RW	OSCREQ Consumer Register
0x150	PRS_CONSUM-ER_HFXO0_TIMEOUT	RW	TIMEOUT Consumer Register
0x154	PRS_CONSUM-ER_CORE_CTIIN0	RW	CTI Consumer Register
0x158	PRS_CONSUM-ER_CORE_CTIIN1	RW	CTI Consumer Register
0x15C	PRS_CONSUM-ER_CORE_CTIIN2	RW	CTI Consumer Register
0x160	PRS_CONSUM-ER_CORE_CTIIN3	RW	CTI Consumer Register
0x164	PRS_CONSUM-ER_CORE_M33RXEV	RW	M33 Consumer Register
0x168	PRS_CONSUMER_TIM-ER0_CC0	RW	CC0 Consumer Register
0x16C	PRS_CONSUMER_TIM-ER0_CC1	RW	CC1 Consumer Register
0x170	PRS_CONSUMER_TIM-ER0_CC2	RW	CC2 Consumer Register
0x174	PRS_CONSUMER_TIMER0_DTI	RW	DTI Consumer Register
0x178	PRS_CONSUMER_TIM-ER0_DTIFS1	RW	DTI Consumer Register
0x17C	PRS_CONSUMER_TIM-ER0_DTIFS2	RW	DTI Consumer Register
0x180	PRS_CONSUMER_TIM-ER1_CC0	RW	CC0 Consumer Register
0x184	PRS_CONSUMER_TIM-ER1_CC1	RW	CC1 Consumer Register
0x188	PRS_CONSUMER_TIM-ER1_CC2	RW	CC2 Consumer Register
0x18C	PRS_CONSUMER_TIMER1_DTI	RW	DTI Consumer Register

Offset	Name	Type	Description
0x190	PRS_CONSUMER_TIMER1_DTIFS1	RW	DTI Consumer Register
0x194	PRS_CONSUMER_TIMER1_DTIFS2	RW	DTI Consumer Register
0x198	PRS_CONSUMER_TIMER2_CC0	RW	CC0 Consumer Register
0x19C	PRS_CONSUMER_TIMER2_CC1	RW	CC1 Consumer Register
0x1A0	PRS_CONSUMER_TIMER2_CC2	RW	CC2 Consumer Register
0x1A4	PRS_CONSUMER_TIMER2_DTI	RW	DTI Consumer Register
0x1A8	PRS_CONSUMER_TIMER2_DTIFS1	RW	DTI Consumer Register
0x1AC	PRS_CONSUMER_TIMER2_DTIFS2	RW	DTI Consumer Register
0x1B0	PRS_CONSUMER_TIMER3_CC0	RW	CC0 Consumer Register
0x1B4	PRS_CONSUMER_TIMER3_CC1	RW	CC1 Consumer Register
0x1B8	PRS_CONSUMER_TIMER3_CC2	RW	CC2 Consumer Register
0x1BC	PRS_CONSUMER_TIMER3_DTI	RW	DTI Consumer Register
0x1C0	PRS_CONSUMER_TIMER3_DTIFS1	RW	DTI Consumer Register
0x1C4	PRS_CONSUMER_TIMER3_DTIFS2	RW	DTI Consumer Register
0x1C8	PRS_CONSUMER_TIMER4_CC0	RW	CC0 Consumer Register
0x1CC	PRS_CONSUMER_TIMER4_CC1	RW	CC1 Consumer Register
0x1D0	PRS_CONSUMER_TIMER4_CC2	RW	CC2 Consumer Register
0x1D4	PRS_CONSUMER_TIMER4_DTI	RW	DTI Consumer Register
0x1D8	PRS_CONSUMER_TIMER4_DTIFS1	RW	DTI Consumer Register
0x1DC	PRS_CONSUMER_TIMER4_DTIFS2	RW	DTI Consumer Register
0x1E0	PRS_CONSUMER_TIMER5_CC0	RW	CC0 Consumer Register
0x1E4	PRS_CONSUMER_TIMER5_CC1	RW	CC1 Consumer Register
0x1E8	PRS_CONSUMER_TIMER5_CC2	RW	CC2 Consumer Register
0x1EC	PRS_CONSUMER_TIMER5_DTI	RW	DTI Consumer Register
0x1F0	PRS_CONSUMER_TIMER5_DTIFS1	RW	DTI Consumer Register

Offset	Name	Type	Description
0x1F4	PRS_CONSUMER_TIMER5_DTIFS2	RW	DTI Consumer Register
0x1F8	PRS_CONSUMER_TIMER6_CC0	RW	CC0 Consumer Register
0x1FC	PRS_CONSUMER_TIMER6_CC1	RW	CC1 Consumer Register
0x200	PRS_CONSUMER_TIMER6_CC2	RW	CC2 Consumer Register
0x204	PRS_CONSUMER_TIMER6_DTI	RW	DTI Consumer Register
0x208	PRS_CONSUMER_TIMER6_DTIFS1	RW	DTI Consumer Register
0x20C	PRS_CONSUMER_TIMER6_DTIFS2	RW	DTI Consumer Register
0x210	PRS_CONSUMER_TIMER7_CC0	RW	CC0 Consumer Register
0x214	PRS_CONSUMER_TIMER7_CC1	RW	CC1 Consumer Register
0x218	PRS_CONSUMER_TIMER7_CC2	RW	CC2 Consumer Register
0x21C	PRS_CONSUMER_TIMER7_DTI	RW	DTI Consumer Register
0x220	PRS_CONSUMER_TIMER7_DTIFS1	RW	DTI Consumer Register
0x224	PRS_CONSUMER_TIMER7_DTIFS2	RW	DTI Consumer Register
0x228	PRS_CONSUMER_VDAC0_ASYNCTRIGCH0	RW	ASYNCTRIG Consumer Register
0x22C	PRS_CONSUMER_VDAC0_ASYNCTRIGCH1	RW	ASYNCTRIG Consumer Register
0x230	PRS_CONSUMER_VDAC0_SYNCTRIGCH0	RW	SYNCTRIG Consumer Register
0x234	PRS_CONSUMER_VDAC0_SYNCTRIGCH1	RW	SYNCTRIG Consumer Register
0x238	PRS_CONSUMER_WDOG0_SRC0	RW	SRC0 Consumer Register
0x23C	PRS_CONSUMER_WDOG0_SRC1	RW	SRC1 Consumer Register
0x240	PRS_CONSUMER_WDOG1_SRC0	RW	SRC0 Consumer Register
0x244	PRS_CONSUMER_WDOG1_SRC1	RW	SRC1 Consumer Register
0x1000	PRS_IPVERSION_SET	R	PRS IPVERSION
0x1008	PRS_ASYNC_SWPULSE_SET	W	Software Pulse Register
0x100C	PRS_ASYNC_SWLEVEL_SET	RW	Software Level Register
0x1010	PRS_ASYNC_PEEK_SET	RH	Async Channel Values
0x1014	PRS_SYNC_PEEK_SET	RH	Sync Channel Values

Offset	Name	Type	Description
0x1018	PRS_ASYNC_CHx_CTRL_SET	RW	Async Channel Control Register
0x1048	PRS_SYNC_CHx_CTRL_SET	RW	Sync Channel Control Register
0x1058	PRS_CONSUM-ER_CMU_CALDN_SET	RW	CALDN Consumer Register
0x105C	PRS_CONSUMER_CMU_CAL-UP_SET	RW	CALUP Consumer Register
0x1060	PRS_CONSUMER_EU-SART0_CLK_SET	RW	CLK Consumer Register
0x1064	PRS_CONSUMER_EU-SART0_RX_SET	RW	RX Consumer Register
0x1068	PRS_CONSUMER_EU-SART0_TRIGGER_SET	RW	TRIGGER Consumer Register
0x106C	PRS_CONSUMER_EU-SART1_CLK_SET	RW	CLK Consumer Register
0x1070	PRS_CONSUMER_EU-SART1_RX_SET	RW	RX Consumer Register
0x1074	PRS_CONSUMER_EU-SART1_TRIGGER_SET	RW	TRIGGER Consumer Register
0x1078	PRS_CONSUMER_EU-SART2_CLK_SET	RW	CLK Consumer Register
0x107C	PRS_CONSUMER_EU-SART2_RX_SET	RW	RX Consumer Register
0x1080	PRS_CONSUMER_EU-SART2_TRIGGER_SET	RW	TRIGGER Consumer Register
0x1084	PRS_CONSUMER_EU-SART3_CLK_SET	RW	CLK Consumer Register
0x1088	PRS_CONSUMER_EU-SART3_RX_SET	RW	RX Consumer Register
0x108C	PRS_CONSUMER_EU-SART3_TRIGGER_SET	RW	TRIGGER Consumer Register
0x1090	PRS_CONSUMER_EU-SART4_CLK_SET	RW	CLK Consumer Register
0x1094	PRS_CONSUMER_EU-SART4_RX_SET	RW	RX Consumer Register
0x1098	PRS_CONSUMER_EU-SART4_TRIGGER_SET	RW	TRIGGER Consumer Register
0x109C	PRS_CONSUM-ER_FRC_RXRAW_SET	RW	RXRAW Consumer Register
0x10A0	PRS_CONSUM-ER_IADC0_SCANTRIG-GER_SET	RW	SCAN Consumer Register
0x10A4	PRS_CONSUMER_IADC0_SIN-GLETRIGGER_SET	RW	SINGLE Consumer Register
0x10A8	PRS_CONSUMER_LDMAX-BAR_DMAREQ0_SET	RW	DMAREQ0 Consumer Register
0x10AC	PRS_CONSUMER_LDMAX-BAR_DMAREQ1_SET	RW	DMAREQ1 Consumer Register

Offset	Name	Type	Description
0x10B0	PRS_CONSUMER_LESENSE_DECIN0_SET	RW	DECIN0 Consumer Register
0x10B4	PRS_CONSUMER_LESENSE_DECIN1_SET	RW	DECIN1 Consumer Register
0x10B8	PRS_CONSUMER_LESENSE_DECIN2_SET	RW	DECIN2 Consumer Register
0x10BC	PRS_CONSUMER_LESENSE_DECIN3_SET	RW	DECIN3 Consumer Register
0x10C0	PRS_CONSUMER_LESENSE_START_SET	RW	START Consumer Register
0x10C4	PRS_CONSUMER_LETIMER0_CLEAR_SET	RW	CLEAR Consumer Register
0x10C8	PRS_CONSUMER_LETIMER0_START_SET	RW	START Consumer Register
0x10CC	PRS_CONSUMER_LETIMER0_STOP_SET	RW	STOP Consumer Register
0x10D0	PRS_CONSUMER_MODEM_DIN_SET	RW	DIN Consumer Register
0x10D4	PRS_CONSUMER_PCNT0_S0IN_SET	RW	S0IN Consumer Register
0x10D8	PRS_CONSUMER_PCNT0_S1IN_SET	RW	S1IN Consumer Register
0x1108	PRS_CONSUMER_RAC_CLR_SET	RW	CLR Consumer Register
0x110C	PRS_CONSUMER_RAC_CTIIN0_SET	RW	CTI Consumer Register
0x1110	PRS_CONSUMER_RAC_CTIIN1_SET	RW	CTI Consumer Register
0x1114	PRS_CONSUMER_RAC_CTIIN2_SET	RW	CTI Consumer Register
0x1118	PRS_CONSUMER_RAC_CTIIN3_SET	RW	CTI Consumer Register
0x111C	PRS_CONSUMER_RAC_FORCETX_SET	RW	FORCETX Consumer Register
0x1120	PRS_CONSUMER_RAC_RXDIS_SET	RW	RXDIS Consumer Register
0x1124	PRS_CONSUMER_RAC_RXEN_SET	RW	RXEN Consumer Register
0x1128	PRS_CONSUMER_RAC_TXEN_SET	RW	TXEN Consumer Register
0x112C	PRS_CONSUMER_SETAMPER_TAMPERSRC26_SET	RW	TAMPERSRC26 Consumer Register
0x1130	PRS_CONSUMER_SETAMPER_TAMPERSRC27_SET	RW	TAMPERSRC27 Consumer Register
0x1134	PRS_CONSUMER_SETAMPER_TAMPERSRC28_SET	RW	TAMPERSRC28 Consumer Register

Offset	Name	Type	Description
0x1138	PRS_CONSUMER_SETAM-PER_TAMPERSRC29_SET	RW	TAMPERSRC29 Consumer Register
0x113C	PRS_CONSUMER_SETAM-PER_TAMPERSRC30_SET	RW	TAMPERSRC30 Consumer Register
0x1140	PRS_CONSUMER_SETAM-PER_TAMPERSRC31_SET	RW	TAMPERSRC31 Consumer Register
0x1144	PRS_CONSUM-ER_SYSRTC0_IN0_SET	RW	IN0 Consumer Register
0x1148	PRS_CONSUM-ER_SYSRTC0_IN1_SET	RW	IN1 Consumer Register
0x114C	PRS_CONSUMER_HFXO0_OS-CREQ_SET	RW	OSCREQ Consumer Register
0x1150	PRS_CONSUM-ER_HFXO0_TIMEOUT_SET	RW	TIMEOUT Consumer Register
0x1154	PRS_CONSUM-ER_CORE_CTIIN0_SET	RW	CTI Consumer Register
0x1158	PRS_CONSUM-ER_CORE_CTIIN1_SET	RW	CTI Consumer Register
0x115C	PRS_CONSUM-ER_CORE_CTIIN2_SET	RW	CTI Consumer Register
0x1160	PRS_CONSUM-ER_CORE_CTIIN3_SET	RW	CTI Consumer Register
0x1164	PRS_CONSUM-ER_CORE_M33RXEV_SET	RW	M33 Consumer Register
0x1168	PRS_CONSUMER_TIM-ER0_CC0_SET	RW	CC0 Consumer Register
0x116C	PRS_CONSUMER_TIM-ER0_CC1_SET	RW	CC1 Consumer Register
0x1170	PRS_CONSUMER_TIM-ER0_CC2_SET	RW	CC2 Consumer Register
0x1174	PRS_CONSUMER_TIM-ER0_DTI_SET	RW	DTI Consumer Register
0x1178	PRS_CONSUMER_TIM-ER0_DTIFS1_SET	RW	DTI Consumer Register
0x117C	PRS_CONSUMER_TIM-ER0_DTIFS2_SET	RW	DTI Consumer Register
0x1180	PRS_CONSUMER_TIM-ER1_CC0_SET	RW	CC0 Consumer Register
0x1184	PRS_CONSUMER_TIM-ER1_CC1_SET	RW	CC1 Consumer Register
0x1188	PRS_CONSUMER_TIM-ER1_CC2_SET	RW	CC2 Consumer Register
0x118C	PRS_CONSUMER_TIM-ER1_DTI_SET	RW	DTI Consumer Register
0x1190	PRS_CONSUMER_TIM-ER1_DTIFS1_SET	RW	DTI Consumer Register

Offset	Name	Type	Description
0x1194	PRS_CONSUMER_TIMER1_DTIFS2_SET	RW	DTI Consumer Register
0x1198	PRS_CONSUMER_TIMER2_CC0_SET	RW	CC0 Consumer Register
0x119C	PRS_CONSUMER_TIMER2_CC1_SET	RW	CC1 Consumer Register
0x11A0	PRS_CONSUMER_TIMER2_CC2_SET	RW	CC2 Consumer Register
0x11A4	PRS_CONSUMER_TIMER2_DTI_SET	RW	DTI Consumer Register
0x11A8	PRS_CONSUMER_TIMER2_DTIFS1_SET	RW	DTI Consumer Register
0x11AC	PRS_CONSUMER_TIMER2_DTIFS2_SET	RW	DTI Consumer Register
0x11B0	PRS_CONSUMER_TIMER3_CC0_SET	RW	CC0 Consumer Register
0x11B4	PRS_CONSUMER_TIMER3_CC1_SET	RW	CC1 Consumer Register
0x11B8	PRS_CONSUMER_TIMER3_CC2_SET	RW	CC2 Consumer Register
0x11BC	PRS_CONSUMER_TIMER3_DTI_SET	RW	DTI Consumer Register
0x11C0	PRS_CONSUMER_TIMER3_DTIFS1_SET	RW	DTI Consumer Register
0x11C4	PRS_CONSUMER_TIMER3_DTIFS2_SET	RW	DTI Consumer Register
0x11C8	PRS_CONSUMER_TIMER4_CC0_SET	RW	CC0 Consumer Register
0x11CC	PRS_CONSUMER_TIMER4_CC1_SET	RW	CC1 Consumer Register
0x11D0	PRS_CONSUMER_TIMER4_CC2_SET	RW	CC2 Consumer Register
0x11D4	PRS_CONSUMER_TIMER4_DTI_SET	RW	DTI Consumer Register
0x11D8	PRS_CONSUMER_TIMER4_DTIFS1_SET	RW	DTI Consumer Register
0x11DC	PRS_CONSUMER_TIMER4_DTIFS2_SET	RW	DTI Consumer Register
0x11E0	PRS_CONSUMER_TIMER5_CC0_SET	RW	CC0 Consumer Register
0x11E4	PRS_CONSUMER_TIMER5_CC1_SET	RW	CC1 Consumer Register
0x11E8	PRS_CONSUMER_TIMER5_CC2_SET	RW	CC2 Consumer Register
0x11EC	PRS_CONSUMER_TIMER5_DTI_SET	RW	DTI Consumer Register

Offset	Name	Type	Description
0x11F0	PRS_CONSUMER_TIMER5_DTIFS1_SET	RW	DTI Consumer Register
0x11F4	PRS_CONSUMER_TIMER5_DTIFS2_SET	RW	DTI Consumer Register
0x11F8	PRS_CONSUMER_TIMER6_CC0_SET	RW	CC0 Consumer Register
0x11FC	PRS_CONSUMER_TIMER6_CC1_SET	RW	CC1 Consumer Register
0x1200	PRS_CONSUMER_TIMER6_CC2_SET	RW	CC2 Consumer Register
0x1204	PRS_CONSUMER_TIMER6_DTI_SET	RW	DTI Consumer Register
0x1208	PRS_CONSUMER_TIMER6_DTIFS1_SET	RW	DTI Consumer Register
0x120C	PRS_CONSUMER_TIMER6_DTIFS2_SET	RW	DTI Consumer Register
0x1210	PRS_CONSUMER_TIMER7_CC0_SET	RW	CC0 Consumer Register
0x1214	PRS_CONSUMER_TIMER7_CC1_SET	RW	CC1 Consumer Register
0x1218	PRS_CONSUMER_TIMER7_CC2_SET	RW	CC2 Consumer Register
0x121C	PRS_CONSUMER_TIMER7_DTI_SET	RW	DTI Consumer Register
0x1220	PRS_CONSUMER_TIMER7_DTIFS1_SET	RW	DTI Consumer Register
0x1224	PRS_CONSUMER_TIMER7_DTIFS2_SET	RW	DTI Consumer Register
0x1228	PRS_CONSUMER_VDAC0_ASYNCTRIGCH0_SET	RW	ASYNCTRIG Consumer Register
0x122C	PRS_CONSUMER_VDAC0_ASYNCTRIGCH1_SET	RW	ASYNCTRIG Consumer Register
0x1230	PRS_CONSUMER_VDAC0_SYNCTRIGCH0_SET	RW	SYNCTRIG Consumer Register
0x1234	PRS_CONSUMER_VDAC0_SYNCTRIGCH1_SET	RW	SYNCTRIG Consumer Register
0x1238	PRS_CONSUMER_WDOG0_SRC0_SET	RW	SRC0 Consumer Register
0x123C	PRS_CONSUMER_WDOG0_SRC1_SET	RW	SRC1 Consumer Register
0x1240	PRS_CONSUMER_WDOG1_SRC0_SET	RW	SRC0 Consumer Register
0x1244	PRS_CONSUMER_WDOG1_SRC1_SET	RW	SRC1 Consumer Register

Offset	Name	Type	Description
0x2000	PRS_IPVERSION_CLR	R	PRS IPVERSION
0x2008	PRS_ASYNC_SWPULSE_CLR	W	Software Pulse Register
0x200C	PRS_ASYNC_SWLEVEL_CLR	RW	Software Level Register
0x2010	PRS_ASYNC_PEEK_CLR	RH	Async Channel Values
0x2014	PRS_SYNC_PEEK_CLR	RH	Sync Channel Values
0x2018	PRS_ASYNC_CHx_CTRL_CLR	RW	Async Channel Control Register
0x2048	PRS_SYNC_CHx_CTRL_CLR	RW	Sync Channel Control Register
0x2058	PRS_CONSUM-ER_CMU_CALDN_CLR	RW	CALDN Consumer Register
0x205C	PRS_CONSUMER_CMU_CAL-UP_CLR	RW	CALUP Consumer Register
0x2060	PRS_CONSUMER_EU-SART0_CLK_CLR	RW	CLK Consumer Register
0x2064	PRS_CONSUMER_EU-SART0_RX_CLR	RW	RX Consumer Register
0x2068	PRS_CONSUMER_EU-SART0_TRIGGER_CLR	RW	TRIGGER Consumer Register
0x206C	PRS_CONSUMER_EU-SART1_CLK_CLR	RW	CLK Consumer Register
0x2070	PRS_CONSUMER_EU-SART1_RX_CLR	RW	RX Consumer Register
0x2074	PRS_CONSUMER_EU-SART1_TRIGGER_CLR	RW	TRIGGER Consumer Register
0x2078	PRS_CONSUMER_EU-SART2_CLK_CLR	RW	CLK Consumer Register
0x207C	PRS_CONSUMER_EU-SART2_RX_CLR	RW	RX Consumer Register
0x2080	PRS_CONSUMER_EU-SART2_TRIGGER_CLR	RW	TRIGGER Consumer Register
0x2084	PRS_CONSUMER_EU-SART3_CLK_CLR	RW	CLK Consumer Register
0x2088	PRS_CONSUMER_EU-SART3_RX_CLR	RW	RX Consumer Register
0x208C	PRS_CONSUMER_EU-SART3_TRIGGER_CLR	RW	TRIGGER Consumer Register
0x2090	PRS_CONSUMER_EU-SART4_CLK_CLR	RW	CLK Consumer Register
0x2094	PRS_CONSUMER_EU-SART4_RX_CLR	RW	RX Consumer Register
0x2098	PRS_CONSUMER_EU-SART4_TRIGGER_CLR	RW	TRIGGER Consumer Register
0x209C	PRS_CONSUM-ER_FRC_RXRAW_CLR	RW	RXRAW Consumer Register

Offset	Name	Type	Description
0x20A0	PRS_CONSUMER_IADC0_SCANTRIGGER_CLR	RW	SCAN Consumer Register
0x20A4	PRS_CONSUMER_IADC0_SINGLETRIGGER_CLR	RW	SINGLE Consumer Register
0x20A8	PRS_CONSUMER_LDMAXBAR_DMAREQ0_CLR	RW	DMAREQ0 Consumer Register
0x20AC	PRS_CONSUMER_LDMAXBAR_DMAREQ1_CLR	RW	DMAREQ1 Consumer Register
0x20B0	PRS_CONSUMER_LESENSE_DECIN0_CLR	RW	DECIN0 Consumer Register
0x20B4	PRS_CONSUMER_LESENSE_DECIN1_CLR	RW	DECIN1 Consumer Register
0x20B8	PRS_CONSUMER_LESENSE_DECIN2_CLR	RW	DECIN2 Consumer Register
0x20BC	PRS_CONSUMER_LESENSE_DECIN3_CLR	RW	DECIN3 Consumer Register
0x20C0	PRS_CONSUMER_LESENSE_START_CLR	RW	START Consumer Register
0x20C4	PRS_CONSUMER_LETIMER0_CLEAR_CLR	RW	CLEAR Consumer Register
0x20C8	PRS_CONSUMER_LETIMER0_START_CLR	RW	START Consumer Register
0x20CC	PRS_CONSUMER_LETIMER0_STOP_CLR	RW	STOP Consumer Register
0x20D0	PRS_CONSUMER_MODEM_DIN_CLR	RW	DIN Consumer Register
0x20D4	PRS_CONSUMER_PCNT0_S0IN_CLR	RW	S0IN Consumer Register
0x20D8	PRS_CONSUMER_PCNT0_S1IN_CLR	RW	S1IN Consumer Register
0x2108	PRS_CONSUMER_RAC_CLR_CLR	RW	CLR Consumer Register
0x210C	PRS_CONSUMER_RAC_CTIIN0_CLR	RW	CTI Consumer Register
0x2110	PRS_CONSUMER_RAC_CTIIN1_CLR	RW	CTI Consumer Register
0x2114	PRS_CONSUMER_RAC_CTIIN2_CLR	RW	CTI Consumer Register
0x2118	PRS_CONSUMER_RAC_CTIIN3_CLR	RW	CTI Consumer Register
0x211C	PRS_CONSUMER_RAC_FORCETX_CLR	RW	FORCETX Consumer Register
0x2120	PRS_CONSUMER_RAC_RXDIS_CLR	RW	RXDIS Consumer Register
0x2124	PRS_CONSUMER_RAC_RXEN_CLR	RW	RXEN Consumer Register

Offset	Name	Type	Description
0x2128	PRS_CONSUMER_RAC_TXEN_CLR	RW	TXEN Consumer Register
0x212C	PRS_CONSUMER_SETAMPER_TAMPERSRC26_CLR	RW	TAMPERSRC26 Consumer Register
0x2130	PRS_CONSUMER_SETAMPER_TAMPERSRC27_CLR	RW	TAMPERSRC27 Consumer Register
0x2134	PRS_CONSUMER_SETAMPER_TAMPERSRC28_CLR	RW	TAMPERSRC28 Consumer Register
0x2138	PRS_CONSUMER_SETAMPER_TAMPERSRC29_CLR	RW	TAMPERSRC29 Consumer Register
0x213C	PRS_CONSUMER_SETAMPER_TAMPERSRC30_CLR	RW	TAMPERSRC30 Consumer Register
0x2140	PRS_CONSUMER_SETAMPER_TAMPERSRC31_CLR	RW	TAMPERSRC31 Consumer Register
0x2144	PRS_CONSUMER_SYSRTC0_IN0_CLR	RW	IN0 Consumer Register
0x2148	PRS_CONSUMER_SYSRTC0_IN1_CLR	RW	IN1 Consumer Register
0x214C	PRS_CONSUMER_HFXO0_OSCREQ_CLR	RW	OSCREQ Consumer Register
0x2150	PRS_CONSUMER_HFXO0_TIMEOUT_CLR	RW	TIMEOUT Consumer Register
0x2154	PRS_CONSUMER_CORE_CTIIN0_CLR	RW	CTI Consumer Register
0x2158	PRS_CONSUMER_CORE_CTIIN1_CLR	RW	CTI Consumer Register
0x215C	PRS_CONSUMER_CORE_CTIIN2_CLR	RW	CTI Consumer Register
0x2160	PRS_CONSUMER_CORE_CTIIN3_CLR	RW	CTI Consumer Register
0x2164	PRS_CONSUMER_CORE_M33RXEV_CLR	RW	M33 Consumer Register
0x2168	PRS_CONSUMER_TIMER0_CC0_CLR	RW	CC0 Consumer Register
0x216C	PRS_CONSUMER_TIMER0_CC1_CLR	RW	CC1 Consumer Register
0x2170	PRS_CONSUMER_TIMER0_CC2_CLR	RW	CC2 Consumer Register
0x2174	PRS_CONSUMER_TIMER0_DTI_CLR	RW	DTI Consumer Register
0x2178	PRS_CONSUMER_TIMER0_DTIFS1_CLR	RW	DTI Consumer Register
0x217C	PRS_CONSUMER_TIMER0_DTIFS2_CLR	RW	DTI Consumer Register
0x2180	PRS_CONSUMER_TIMER1_CC0_CLR	RW	CC0 Consumer Register

Offset	Name	Type	Description
0x2184	PRS_CONSUMER_TIMER1_CC1_CLR	RW	CC1 Consumer Register
0x2188	PRS_CONSUMER_TIMER1_CC2_CLR	RW	CC2 Consumer Register
0x218C	PRS_CONSUMER_TIMER1_DTI_CLR	RW	DTI Consumer Register
0x2190	PRS_CONSUMER_TIMER1_DTIFS1_CLR	RW	DTI Consumer Register
0x2194	PRS_CONSUMER_TIMER1_DTIFS2_CLR	RW	DTI Consumer Register
0x2198	PRS_CONSUMER_TIMER2_CC0_CLR	RW	CC0 Consumer Register
0x219C	PRS_CONSUMER_TIMER2_CC1_CLR	RW	CC1 Consumer Register
0x21A0	PRS_CONSUMER_TIMER2_CC2_CLR	RW	CC2 Consumer Register
0x21A4	PRS_CONSUMER_TIMER2_DTI_CLR	RW	DTI Consumer Register
0x21A8	PRS_CONSUMER_TIMER2_DTIFS1_CLR	RW	DTI Consumer Register
0x21AC	PRS_CONSUMER_TIMER2_DTIFS2_CLR	RW	DTI Consumer Register
0x21B0	PRS_CONSUMER_TIMER3_CC0_CLR	RW	CC0 Consumer Register
0x21B4	PRS_CONSUMER_TIMER3_CC1_CLR	RW	CC1 Consumer Register
0x21B8	PRS_CONSUMER_TIMER3_CC2_CLR	RW	CC2 Consumer Register
0x21BC	PRS_CONSUMER_TIMER3_DTI_CLR	RW	DTI Consumer Register
0x21C0	PRS_CONSUMER_TIMER3_DTIFS1_CLR	RW	DTI Consumer Register
0x21C4	PRS_CONSUMER_TIMER3_DTIFS2_CLR	RW	DTI Consumer Register
0x21C8	PRS_CONSUMER_TIMER4_CC0_CLR	RW	CC0 Consumer Register
0x21CC	PRS_CONSUMER_TIMER4_CC1_CLR	RW	CC1 Consumer Register
0x21D0	PRS_CONSUMER_TIMER4_CC2_CLR	RW	CC2 Consumer Register
0x21D4	PRS_CONSUMER_TIMER4_DTI_CLR	RW	DTI Consumer Register
0x21D8	PRS_CONSUMER_TIMER4_DTIFS1_CLR	RW	DTI Consumer Register
0x21DC	PRS_CONSUMER_TIMER4_DTIFS2_CLR	RW	DTI Consumer Register

Offset	Name	Type	Description
0x21E0	PRS_CONSUMER_TIMER5_CC0_CLR	RW	CC0 Consumer Register
0x21E4	PRS_CONSUMER_TIMER5_CC1_CLR	RW	CC1 Consumer Register
0x21E8	PRS_CONSUMER_TIMER5_CC2_CLR	RW	CC2 Consumer Register
0x21EC	PRS_CONSUMER_TIMER5_DTI_CLR	RW	DTI Consumer Register
0x21F0	PRS_CONSUMER_TIMER5_DTIFS1_CLR	RW	DTI Consumer Register
0x21F4	PRS_CONSUMER_TIMER5_DTIFS2_CLR	RW	DTI Consumer Register
0x21F8	PRS_CONSUMER_TIMER6_CC0_CLR	RW	CC0 Consumer Register
0x21FC	PRS_CONSUMER_TIMER6_CC1_CLR	RW	CC1 Consumer Register
0x2200	PRS_CONSUMER_TIMER6_CC2_CLR	RW	CC2 Consumer Register
0x2204	PRS_CONSUMER_TIMER6_DTI_CLR	RW	DTI Consumer Register
0x2208	PRS_CONSUMER_TIMER6_DTIFS1_CLR	RW	DTI Consumer Register
0x220C	PRS_CONSUMER_TIMER6_DTIFS2_CLR	RW	DTI Consumer Register
0x2210	PRS_CONSUMER_TIMER7_CC0_CLR	RW	CC0 Consumer Register
0x2214	PRS_CONSUMER_TIMER7_CC1_CLR	RW	CC1 Consumer Register
0x2218	PRS_CONSUMER_TIMER7_CC2_CLR	RW	CC2 Consumer Register
0x221C	PRS_CONSUMER_TIMER7_DTI_CLR	RW	DTI Consumer Register
0x2220	PRS_CONSUMER_TIMER7_DTIFS1_CLR	RW	DTI Consumer Register
0x2224	PRS_CONSUMER_TIMER7_DTIFS2_CLR	RW	DTI Consumer Register
0x2228	PRS_CONSUMER_VDAC0_ASYNCTRIGCH0_CLR	RW	ASYNCTRIG Consumer Register
0x222C	PRS_CONSUMER_VDAC0_ASYNCTRIGCH1_CLR	RW	ASYNCTRIG Consumer Register
0x2230	PRS_CONSUMER_VDAC0_SYNCTRIGCH0_CLR	RW	SYNCTRIG Consumer Register
0x2234	PRS_CONSUMER_VDAC0_SYNCTRIGCH1_CLR	RW	SYNCTRIG Consumer Register

Offset	Name	Type	Description
0x2238	PRS_CONSUMER_WDOG0_SRC0_CLR	RW	SRC0 Consumer Register
0x223C	PRS_CONSUMER_WDOG0_SRC1_CLR	RW	SRC1 Consumer Register
0x2240	PRS_CONSUMER_WDOG1_SRC0_CLR	RW	SRC0 Consumer Register
0x2244	PRS_CONSUMER_WDOG1_SRC1_CLR	RW	SRC1 Consumer Register
0x3000	PRS_IPVERSION_TGL	R	PRS IPVERSION
0x3008	PRS_ASYNC_SWPULSE_TGL	W	Software Pulse Register
0x300C	PRS_ASYNC_SWLEVEL_TGL	RW	Software Level Register
0x3010	PRS_ASYNC_PEEK_TGL	RH	Async Channel Values
0x3014	PRS_SYNC_PEEK_TGL	RH	Sync Channel Values
0x3018	PRS_ASYNC_CHx_CTRL_TGL	RW	Async Channel Control Register
0x3048	PRS_SYNC_CHx_CTRL_TGL	RW	Sync Channel Control Register
0x3058	PRS_CONSUMER_CMU_CALDN_TGL	RW	CALDN Consumer Register
0x305C	PRS_CONSUMER_CMU_CALUP_TGL	RW	CALUP Consumer Register
0x3060	PRS_CONSUMER_EUSART0_CLK_TGL	RW	CLK Consumer Register
0x3064	PRS_CONSUMER_EUSART0_RX_TGL	RW	RX Consumer Register
0x3068	PRS_CONSUMER_EUSART0_TRIGGER_TGL	RW	TRIGGER Consumer Register
0x306C	PRS_CONSUMER_EUSART1_CLK_TGL	RW	CLK Consumer Register
0x3070	PRS_CONSUMER_EUSART1_RX_TGL	RW	RX Consumer Register
0x3074	PRS_CONSUMER_EUSART1_TRIGGER_TGL	RW	TRIGGER Consumer Register
0x3078	PRS_CONSUMER_EUSART2_CLK_TGL	RW	CLK Consumer Register
0x307C	PRS_CONSUMER_EUSART2_RX_TGL	RW	RX Consumer Register
0x3080	PRS_CONSUMER_EUSART2_TRIGGER_TGL	RW	TRIGGER Consumer Register
0x3084	PRS_CONSUMER_EUSART3_CLK_TGL	RW	CLK Consumer Register
0x3088	PRS_CONSUMER_EUSART3_RX_TGL	RW	RX Consumer Register
0x308C	PRS_CONSUMER_EUSART3_TRIGGER_TGL	RW	TRIGGER Consumer Register
0x3090	PRS_CONSUMER_EUSART4_CLK_TGL	RW	CLK Consumer Register

Offset	Name	Type	Description
0x3094	PRS_CONSUMER_EUSART4_RX_TGL	RW	RX Consumer Register
0x3098	PRS_CONSUMER_EUSART4_TRIGGER_TGL	RW	TRIGGER Consumer Register
0x309C	PRS_CONSUMER_FRC_RXRAW_TGL	RW	RXRAW Consumer Register
0x30A0	PRS_CONSUMER_IADC0_SCANTRIGGER_TGL	RW	SCAN Consumer Register
0x30A4	PRS_CONSUMER_IADC0_SINGLETRIGGER_TGL	RW	SINGLE Consumer Register
0x30A8	PRS_CONSUMER_LDMABAR_DMAREQ0_TGL	RW	DMAREQ0 Consumer Register
0x30AC	PRS_CONSUMER_LDMABAR_DMAREQ1_TGL	RW	DMAREQ1 Consumer Register
0x30B0	PRS_CONSUMER_LESENSE_DECIN0_TGL	RW	DECIN0 Consumer Register
0x30B4	PRS_CONSUMER_LESENSE_DECIN1_TGL	RW	DECIN1 Consumer Register
0x30B8	PRS_CONSUMER_LESENSE_DECIN2_TGL	RW	DECIN2 Consumer Register
0x30BC	PRS_CONSUMER_LESENSE_DECIN3_TGL	RW	DECIN3 Consumer Register
0x30C0	PRS_CONSUMER_LESENSE_START_TGL	RW	START Consumer Register
0x30C4	PRS_CONSUMER_LETIMER0_CLEAR_TGL	RW	CLEAR Consumer Register
0x30C8	PRS_CONSUMER_LETIMER0_START_TGL	RW	START Consumer Register
0x30CC	PRS_CONSUMER_LETIMER0_STOP_TGL	RW	STOP Consumer Register
0x30D0	PRS_CONSUMER_MODEM_DIN_TGL	RW	DIN Consumer Register
0x30D4	PRS_CONSUMER_PCNT0_S0IN_TGL	RW	S0IN Consumer Register
0x30D8	PRS_CONSUMER_PCNT0_S1IN_TGL	RW	S1IN Consumer Register
0x3108	PRS_CONSUMER_RAC_CLR_TGL	RW	CLR Consumer Register
0x310C	PRS_CONSUMER_RAC_CTIIN0_TGL	RW	CTI Consumer Register
0x3110	PRS_CONSUMER_RAC_CTIIN1_TGL	RW	CTI Consumer Register
0x3114	PRS_CONSUMER_RAC_CTIIN2_TGL	RW	CTI Consumer Register
0x3118	PRS_CONSUMER_RAC_CTIIN3_TGL	RW	CTI Consumer Register

Offset	Name	Type	Description
0x311C	PRS_CONSUMER_RAC_FORCETX_TGL	RW	FORCETX Consumer Register
0x3120	PRS_CONSUMER_RAC_RXDIS_TGL	RW	RXDIS Consumer Register
0x3124	PRS_CONSUMER_RAC_RXEN_TGL	RW	RXEN Consumer Register
0x3128	PRS_CONSUMER_RAC_TXEN_TGL	RW	TXEN Consumer Register
0x312C	PRS_CONSUMER_SETAMPER_TAMPERSRC26_TGL	RW	TAMPERSRC26 Consumer Register
0x3130	PRS_CONSUMER_SETAMPER_TAMPERSRC27_TGL	RW	TAMPERSRC27 Consumer Register
0x3134	PRS_CONSUMER_SETAMPER_TAMPERSRC28_TGL	RW	TAMPERSRC28 Consumer Register
0x3138	PRS_CONSUMER_SETAMPER_TAMPERSRC29_TGL	RW	TAMPERSRC29 Consumer Register
0x313C	PRS_CONSUMER_SETAMPER_TAMPERSRC30_TGL	RW	TAMPERSRC30 Consumer Register
0x3140	PRS_CONSUMER_SETAMPER_TAMPERSRC31_TGL	RW	TAMPERSRC31 Consumer Register
0x3144	PRS_CONSUMER_SYSRTC0_IN0_TGL	RW	IN0 Consumer Register
0x3148	PRS_CONSUMER_SYSRTC0_IN1_TGL	RW	IN1 Consumer Register
0x314C	PRS_CONSUMER_HFXO0_OSCREQ_TGL	RW	OSCREQ Consumer Register
0x3150	PRS_CONSUMER_HFXO0_TIMEOUT_TGL	RW	TIMEOUT Consumer Register
0x3154	PRS_CONSUMER_CORE_CTIIN0_TGL	RW	CTI Consumer Register
0x3158	PRS_CONSUMER_CORE_CTIIN1_TGL	RW	CTI Consumer Register
0x315C	PRS_CONSUMER_CORE_CTIIN2_TGL	RW	CTI Consumer Register
0x3160	PRS_CONSUMER_CORE_CTIIN3_TGL	RW	CTI Consumer Register
0x3164	PRS_CONSUMER_CORE_M33RXEV_TGL	RW	M33 Consumer Register
0x3168	PRS_CONSUMER_TIMER0_CC0_TGL	RW	CC0 Consumer Register
0x316C	PRS_CONSUMER_TIMER0_CC1_TGL	RW	CC1 Consumer Register
0x3170	PRS_CONSUMER_TIMER0_CC2_TGL	RW	CC2 Consumer Register
0x3174	PRS_CONSUMER_TIMER0_DTI_TGL	RW	DTI Consumer Register

Offset	Name	Type	Description
0x3178	PRS_CONSUMER_TIMER0_DTIFS1_TGL	RW	DTI Consumer Register
0x317C	PRS_CONSUMER_TIMER0_DTIFS2_TGL	RW	DTI Consumer Register
0x3180	PRS_CONSUMER_TIMER1_CC0_TGL	RW	CC0 Consumer Register
0x3184	PRS_CONSUMER_TIMER1_CC1_TGL	RW	CC1 Consumer Register
0x3188	PRS_CONSUMER_TIMER1_CC2_TGL	RW	CC2 Consumer Register
0x318C	PRS_CONSUMER_TIMER1_DTI_TGL	RW	DTI Consumer Register
0x3190	PRS_CONSUMER_TIMER1_DTIFS1_TGL	RW	DTI Consumer Register
0x3194	PRS_CONSUMER_TIMER1_DTIFS2_TGL	RW	DTI Consumer Register
0x3198	PRS_CONSUMER_TIMER2_CC0_TGL	RW	CC0 Consumer Register
0x319C	PRS_CONSUMER_TIMER2_CC1_TGL	RW	CC1 Consumer Register
0x31A0	PRS_CONSUMER_TIMER2_CC2_TGL	RW	CC2 Consumer Register
0x31A4	PRS_CONSUMER_TIMER2_DTI_TGL	RW	DTI Consumer Register
0x31A8	PRS_CONSUMER_TIMER2_DTIFS1_TGL	RW	DTI Consumer Register
0x31AC	PRS_CONSUMER_TIMER2_DTIFS2_TGL	RW	DTI Consumer Register
0x31B0	PRS_CONSUMER_TIMER3_CC0_TGL	RW	CC0 Consumer Register
0x31B4	PRS_CONSUMER_TIMER3_CC1_TGL	RW	CC1 Consumer Register
0x31B8	PRS_CONSUMER_TIMER3_CC2_TGL	RW	CC2 Consumer Register
0x31BC	PRS_CONSUMER_TIMER3_DTI_TGL	RW	DTI Consumer Register
0x31C0	PRS_CONSUMER_TIMER3_DTIFS1_TGL	RW	DTI Consumer Register
0x31C4	PRS_CONSUMER_TIMER3_DTIFS2_TGL	RW	DTI Consumer Register
0x31C8	PRS_CONSUMER_TIMER4_CC0_TGL	RW	CC0 Consumer Register
0x31CC	PRS_CONSUMER_TIMER4_CC1_TGL	RW	CC1 Consumer Register
0x31D0	PRS_CONSUMER_TIMER4_CC2_TGL	RW	CC2 Consumer Register

Offset	Name	Type	Description
0x31D4	PRS_CONSUMER_TIMER4_DTI_TGL	RW	DTI Consumer Register
0x31D8	PRS_CONSUMER_TIMER4_DTIFS1_TGL	RW	DTI Consumer Register
0x31DC	PRS_CONSUMER_TIMER4_DTIFS2_TGL	RW	DTI Consumer Register
0x31E0	PRS_CONSUMER_TIMER5_CC0_TGL	RW	CC0 Consumer Register
0x31E4	PRS_CONSUMER_TIMER5_CC1_TGL	RW	CC1 Consumer Register
0x31E8	PRS_CONSUMER_TIMER5_CC2_TGL	RW	CC2 Consumer Register
0x31EC	PRS_CONSUMER_TIMER5_DTI_TGL	RW	DTI Consumer Register
0x31F0	PRS_CONSUMER_TIMER5_DTIFS1_TGL	RW	DTI Consumer Register
0x31F4	PRS_CONSUMER_TIMER5_DTIFS2_TGL	RW	DTI Consumer Register
0x31F8	PRS_CONSUMER_TIMER6_CC0_TGL	RW	CC0 Consumer Register
0x31FC	PRS_CONSUMER_TIMER6_CC1_TGL	RW	CC1 Consumer Register
0x3200	PRS_CONSUMER_TIMER6_CC2_TGL	RW	CC2 Consumer Register
0x3204	PRS_CONSUMER_TIMER6_DTI_TGL	RW	DTI Consumer Register
0x3208	PRS_CONSUMER_TIMER6_DTIFS1_TGL	RW	DTI Consumer Register
0x320C	PRS_CONSUMER_TIMER6_DTIFS2_TGL	RW	DTI Consumer Register
0x3210	PRS_CONSUMER_TIMER7_CC0_TGL	RW	CC0 Consumer Register
0x3214	PRS_CONSUMER_TIMER7_CC1_TGL	RW	CC1 Consumer Register
0x3218	PRS_CONSUMER_TIMER7_CC2_TGL	RW	CC2 Consumer Register
0x321C	PRS_CONSUMER_TIMER7_DTI_TGL	RW	DTI Consumer Register
0x3220	PRS_CONSUMER_TIMER7_DTIFS1_TGL	RW	DTI Consumer Register
0x3224	PRS_CONSUMER_TIMER7_DTIFS2_TGL	RW	DTI Consumer Register
0x3228	PRS_CONSUMER_VDAC0_ASYNCTRIGCH0_TGL	RW	ASYNCTRIG Consumer Register

Offset	Name	Type	Description
0x322C	PRS_CONSUMER_VDAC0_ASYNCTRIGCH1_TGL	RW	ASYNCTRIG Consumer Register
0x3230	PRS_CONSUMER_VDAC0_SYNCTRIGCH0_TGL	RW	SYNCTRIG Consumer Register
0x3234	PRS_CONSUMER_VDAC0_SYNCTRIGCH1_TGL	RW	SYNCTRIG Consumer Register
0x3238	PRS_CONSUMER_WDOG0_SRC0_TGL	RW	SRC0 Consumer Register
0x323C	PRS_CONSUMER_WDOG0_SRC1_TGL	RW	SRC1 Consumer Register
0x3240	PRS_CONSUMER_WDOG1_SRC0_TGL	RW	SRC0 Consumer Register
0x3244	PRS_CONSUMER_WDOG1_SRC1_TGL	RW	SRC1 Consumer Register

14.5 PRS Register Description

14.5.1 PRS_IPVERSION - PRS IPVERSION

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x4																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x4	R	**New BitField**
	The read only IPVERSION field goves the version for this module. There may be minor software changes required for modules with different values of IPVERSION			

14.5.2 PRS_ASYNC_SWPULSE - Software Pulse Register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																					0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																					W(nB)	W(nB)	W(nB)	W(nB)	W(nB)	W(nB)	W(nB)	W(nB)	W(nB)	W(nB)	W(nB)	W(nB)
Name																					CH11PULSE	CH10PULSE	CH9PULSE	CH8PULSE	CH7PULSE	CH6PULSE	CH5PULSE	CH4PULSE	CH3PULSE	CH2PULSE	CH1PULSE	CH0PULSE

Bit	Name	Reset	Access	Description
31:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11	CH11PULSE	0x0	W(nB)	**Channel pulse**
	Channel 11 pulse generation			
10	CH10PULSE	0x0	W(nB)	**Channel pulse**
	Channel 10 pulse generation			
9	CH9PULSE	0x0	W(nB)	**Channel pulse**
	Channel 9 pulse generation			
8	CH8PULSE	0x0	W(nB)	**Channel pulse**
	Channel 8 pulse generation			
7	CH7PULSE	0x0	W(nB)	**Channel pulse**
	Channel 7 pulse generation			
6	CH6PULSE	0x0	W(nB)	**Channel pulse**
	Channel 6 pulse generation			
5	CH5PULSE	0x0	W(nB)	**Channel pulse**
	Channel 5 pulse generation			
4	CH4PULSE	0x0	W(nB)	**Channel pulse**
	Channel 4 pulse generation			
3	CH3PULSE	0x0	W(nB)	**Channel pulse**
	Channel 3 pulse generation			
2	CH2PULSE	0x0	W(nB)	**Channel pulse**
	Channel 2 pulse generation			
1	CH1PULSE	0x0	W(nB)	**Channel pulse**
	Channel 1 pulse generation			
0	CH0PULSE	0x0	W(nB)	**Channel pulse**
	Channel 0 pulse generation			

14.5.3 PRS_ASYNC_SWLEVEL - Software Level Register

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																					0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name																					CH11LEVEL	CH10LEVEL	CH9LEVEL	CH8LEVEL	CH7LEVEL	CH6LEVEL	CH5LEVEL	CH4LEVEL	CH3LEVEL	CH2LEVEL	CH1LEVEL	CH0LEVEL

Bit	Name	Reset	Access	Description
31:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11	CH11LEVEL	0x0	RW	**Channel Level**
	Channel 11 Software Level			
10	CH10LEVEL	0x0	RW	**Channel Level**
	Channel 10 Software Level			
9	CH9LEVEL	0x0	RW	**Channel Level**
	Channel 9 Software Level			
8	CH8LEVEL	0x0	RW	**Channel Level**
	Channel 8 Software Level			
7	CH7LEVEL	0x0	RW	**Channel Level**
	Channel 7 Software Level			
6	CH6LEVEL	0x0	RW	**Channel Level**
	Channel 6 Software Level			
5	CH5LEVEL	0x0	RW	**Channel Level**
	Channel 5 Software Level			
4	CH4LEVEL	0x0	RW	**Channel Level**
	Channel 4 Software Level			
3	CH3LEVEL	0x0	RW	**Channel Level**
	Channel 3 Software Level			
2	CH2LEVEL	0x0	RW	**Channel Level**
	Channel 2 Software Level			
1	CH1LEVEL	0x0	RW	**Channel Level**
	Channel 1 Software Level			
0	CH0LEVEL	0x0	RW	**Channel Level**
	Channel 0 Software Level			

14.5.4 PRS_ASYNC_PEEK - Async Channel Values

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																					0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																					R	R	R	R	R	R	R	R	R	R	R	R
Name																					CH11VAL	CH10VAL	CH9VAL	CH8VAL	CH7VAL	CH6VAL	CH5VAL	CH4VAL	CH3VAL	CH2VAL	CH1VAL	CH0VAL

Bit	Name	Reset	Access	Description
31:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11	CH11VAL	0x0	R	**Channel 11 Current Value**
	See bit 0.			
10	CH10VAL	0x0	R	**Channel 10 Current Value**
	See bit 0.			
9	CH9VAL	0x0	R	**Channel 9 Current Value**
	See bit 0.			
8	CH8VAL	0x0	R	**Channel 8 Current Value**
	See bit 0.			
7	CH7VAL	0x0	R	**Channel 7 Current Value**
	See bit 0.			
6	CH6VAL	0x0	R	**Channel 6 Current Value**
	See bit 0.			
5	CH5VAL	0x0	R	**Channel 5 Current Value**
	See bit 0.			
4	CH4VAL	0x0	R	**Channel 4 Current Value**
	See bit 0.			
3	CH3VAL	0x0	R	**Channel 3 Current Value**
	See bit 0.			
2	CH2VAL	0x0	R	**Channel 2 Current Value**
	See bit 0.			
1	CH1VAL	0x0	R	**Channel 1 Current Value**
	See bit 0.			
0	CH0VAL	0x0	R	**Channel 0 Current Value**
	Sample the current output value of channel 0. This value may be one or two clock delayed			

14.5.5 PRS_SYNC_PEEK - Sync Channel Values

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0	0x0	0x0	0x0
Access																													R	R	R	R
Name																													CH3VAL	CH2VAL	CH1VAL	CH0VAL

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	CH3VAL Channel 3 current value	0x0	R	**Channel Value**
2	CH2VAL Channel 2 current value	0x0	R	**Channel Value**
1	CH1VAL Channel 1 current value	0x0	R	**Channel Value**
0	CH0VAL Channel 0 current value	0x0	R	**Channel Value**

14.5.6 PRS_ASYNC_CHx_CTRL - Async Channel Control Register

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0x0								0xC					0x0												0x0		
Access					RW								RW					RW												RW		
Name					AUXSEL								FNSEL					SOURCESEL												SIGSEL		

Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27:24	AUXSEL	0x0	RW	**Aux Select**
	Select Asynchronous PRS channel as input B of LUT function. Async PRS[n] is selected with AUXSEL = n.			
23:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	FNSEL	0xC	RW	**Function Select**
	Look up table function select. Signal A is the selected producer input. Signal B is the output of the previous PRS channel.			

Value	Mode	Description
0	LOGICAL_ZERO	Logical 0
1	A_NOR_B	A NOR B
2	NOT_A_AND_B	(!A) AND B
3	NOT_A	!A
4	A_AND_NOT_B	A AND (!B)
5	NOT_B	!B
6	A_XOR_B	A XOR B
7	A_NAND_B	A NAND B
8	A_AND_B	A AND B
9	A_XNOR_B	A XNOR B
10	B	B
11	NOT_A_OR_B	(!A) OR B
12	A	A
13	A_OR_NOT_B	A OR (!B)
14	A_OR_B	A OR B
15	LOGICAL_ONE	Logical 1

15	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
14:8	SOURCESEL	0x0	RW	**Source Select**

Bit	Name	Reset	Access	Description
	Select input source for asynchronous PRS channel. See Asynchronous Producers table for details.			
7:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2:0	SIGSEL	0x0	RW	**Signal Select**
	Select signal input for asynchronous PRS channel. See Asynchronous Producers table for details.			

Value	Mode	Description
0	NONE	

14.5.7 PRS_SYNC_CHx_CTRL - Sync Channel Control Register

Offset	Bit Position																													
0x048	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																					0x0										0x0	
Access																					RW										RW	
Name																					SOURCESEL										SIGSEL	

Bit	Name	Reset	Access	Description
31:15	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
14:8	SOURCESEL	0x0	RW	**Source Select**
	Select input source to sync PRS channel.			
7:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2:0	SIGSEL	0x0	RW	**Signal Select**
	Select signal input to sync PRS channel.			

Value	Mode	Description
0	NONE	

14.5.8 PRS_CONSUMER_CMU_CALDN - CALDN Consumer Register

Offset	Bit Position																															
0x058	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CALDN async channel select**
	CALDN async channel select			

14.5.9 PRS_CONSUMER_CMU_CALUP - CALUP Consumer Register

Offset	Bit Position																															
0x05C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CALUP async channel select**
	CALUP async channel select			

14.5.10 PRS_CONSUMER_EUSART0_CLK - CLK Consumer Register

Offset	Bit Position																															
0x060	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CLK async channel select**
	CLK async channel select			

14.5.11 PRS_CONSUMER_EUSART0_RX - RX Consumer Register

Offset	Bit Position																															
0x064	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**RX async channel select**
	RX async channel select			

14.5.12 PRS_CONSUMER_EUSART0_TRIGGER - TRIGGER Consumer Register

Offset	Bit Position																															
0x068	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**TRIGGER async channel select**
	TRIGGER async channel select			

14.5.13 PRS_CONSUMER_EUSART1_CLK - CLK Consumer Register

Offset	Bit Position																															
0x06C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CLK async channel select**
	CLK async channel select			

14.5.14 PRS_CONSUMER_EUSART1_RX - RX Consumer Register

Offset	Bit Position																															
0x070	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**RX async channel select**
	RX async channel select			

14.5.15 PRS_CONSUMER_EUSART1_TRIGGER - TRIGGER Consumer Register

Offset	Bit Position																															
0x074	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**TRIGGER async channel select**
	TRIGGER async channel select			

14.5.16 PRS_CONSUMER_EUSART2_CLK - CLK Consumer Register

Offset	Bit Position																															
0x078	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CLK async channel select**
	CLK async channel select			

14.5.17 PRS_CONSUMER_EUSART2_RX - RX Consumer Register

Offset	Bit Position																															
0x07C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**RX async channel select**
	RX async channel select			

14.5.18 PRS_CONSUMER_EUSART2_TRIGGER - TRIGGER Consumer Register

Offset	Bit Position																															
0x080	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**TRIGGER async channel select**
	TRIGGER async channel select			

14.5.19 PRS_CONSUMER_EUSART3_CLK - CLK Consumer Register

Offset	Bit Position																															
0x084	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CLK async channel select**
	CLK async channel select			

14.5.20 PRS_CONSUMER_EUSART3_RX - RX Consumer Register

Offset	Bit Position																															
0x088	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**RX async channel select**
	RX async channel select			

14.5.21 PRS_CONSUMER_EUSART3_TRIGGER - TRIGGER Consumer Register

Offset	Bit Position																															
0x08C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**TRIGGER async channel select**
	TRIGGER async channel select			

14.5.22 PRS_CONSUMER_EUSART4_CLK - CLK Consumer Register

Offset	Bit Position																															
0x090	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CLK async channel select**
	CLK async channel select			

14.5.23 PRS_CONSUMER_EUSART4_RX - RX Consumer Register

Offset	Bit Position																															
0x094	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**RX async channel select**
	RX async channel select			

14.5.24 PRS_CONSUMER_EUSART4_TRIGGER - TRIGGER Consumer Register

Offset	Bit Position																															
0x098	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**TRIGGER async channel select**
	TRIGGER async channel select			

14.5.25 PRS_CONSUMER_FRC_RXRAW - RXRAW Consumer Register

Offset	Bit Position																															
0x09C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**RXRAW async channel select**
	RXRAW async channel select			

14.5.26 PRS_CONSUMER_IADC0_SCANTRIGGER - SCAN Consumer Register

Offset	Bit Position																													
0x0A0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**SCAN sync channel select**
	SCAN sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**SCAN async channel select**
	SCAN async channel select			

14.5.27 PRS_CONSUMER_IADC0_SINGLETRIGGER - SINGLE Consumer Register

Offset	Bit Position																													
0x0A4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**SINGLE sync channel select**
	SINGLE sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**SINGLE async channel select**
	SINGLE async channel select			

14.5.28 PRS_CONSUMER_LDMAXBAR_DMAREQ0 - DMAREQ0 Consumer Register

Offset	Bit Position																															
0x0A8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DMAREQ0 async channel select**
	DMAREQ0 async channel select			

14.5.29 PRS_CONSUMER_LDMAXBAR_DMAREQ1 - DMAREQ1 Consumer Register

Offset	Bit Position																															
0x0AC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DMAREQ1 async channel select**
	DMAREQ1 async channel select			

14.5.30 PRS_CONSUMER_LESENSE_DECIN0 - DECIN0 Consumer Register

Offset	Bit Position																															
0x0B0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DECIN0 async channel select**
	DECIN0 async channel select			

14.5.31 PRS_CONSUMER_LESENSE_DECIN1 - DECIN1 Consumer Register

Offset	Bit Position																															
0x0B4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DECIN1 async channel select**
	DECIN1 async channel select			

14.5.32 PRS_CONSUMER_LESENSE_DECIN2 - DECIN2 Consumer Register

Offset	Bit Position																															
0x0B8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DECIN2 async channel select**
	DECIN2 async channel select			

14.5.33 PRS_CONSUMER_LESENSE_DECIN3 - DECIN3 Consumer Register

Offset	Bit Position																															
0x0BC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DECIN3 async channel select**
	DECIN3 async channel select			

14.5.34 PRS_CONSUMER_LESENSE_START - START Consumer Register

Offset	Bit Position																															
0x0C0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**START async channel select**
	START async channel select			

14.5.35 PRS_CONSUMER_LETIMER0_CLEAR - CLEAR Consumer Register

Offset	Bit Position																															
0x0C4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CLEAR async channel select**
	CLEAR async channel select			

14.5.36 PRS_CONSUMER_LETIMER0_START - START Consumer Register

Offset	Bit Position																															
0x0C8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**START async channel select**
	START async channel select			

14.5.37 PRS_CONSUMER_LETIMER0_STOP - STOP Consumer Register

Offset	Bit Position																															
0x0CC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**STOP async channel select**
	STOP async channel select			

14.5.38 PRS_CONSUMER_MODEM_DIN - DIN Consumer Register

Offset	Bit Position																															
0x0D0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DIN async channel select**
	DIN async channel select			

14.5.39 PRS_CONSUMER_PCNT0_S0IN - S0IN Consumer Register

Offset	Bit Position																															
0x0D4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**S0IN async channel select**
	S0IN async channel select			

14.5.40 PRS_CONSUMER_PCNT0_S1IN - S1IN Consumer Register

Offset	Bit Position																															
0x0D8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**S1IN async channel select**
	S1IN async channel select			

14.5.41 PRS_CONSUMER_RAC_CLR - CLR Consumer Register

Offset	Bit Position																															
0x108	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CLR async channel select**
	CLR async channel select			

14.5.42 PRS_CONSUMER_RAC_CTIIN0 - CTI Consumer Register

Offset	Bit Position																															
0x10C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CTI async channel select**
	CTI async channel select			

14.5.43 PRS_CONSUMER_RAC_CTIIN1 - CTI Consumer Register

Offset	Bit Position																															
0x110	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CTI async channel select**
	CTI async channel select			

14.5.44 PRS_CONSUMER_RAC_CTIIN2 - CTI Consumer Register

Offset	Bit Position																															
0x114	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CTI async channel select**
	CTI async channel select			

14.5.45 PRS_CONSUMER_RAC_CTIIN3 - CTI Consumer Register

Offset	Bit Position																															
0x118	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CTI async channel select**
	CTI async channel select			

14.5.46 PRS_CONSUMER_RAC_FORCETX - FORCETX Consumer Register

Offset	Bit Position																															
0x11C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**FORCETX async channel select**
	FORCETX async channel select			

14.5.47 PRS_CONSUMER_RAC_RXDIS - RXDIS Consumer Register

Offset	Bit Position																															
0x120	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**RXDIS async channel select**
	RXDIS async channel select			

14.5.48 PRS_CONSUMER_RAC_RXEN - RXEN Consumer Register

Offset	Bit Position																															
0x124	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**RXEN async channel select**
	RXEN async channel select			

14.5.49 PRS_CONSUMER_RAC_TXEN - TXEN Consumer Register

Offset	Bit Position																															
0x128	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**TXEN async channel select**
	TXEN async channel select			

14.5.50 PRS_CONSUMER_SETAMPER_TAMPERSRC26 - TAMPERSRC26 Consumer Register

Offset	Bit Position																															
0x12C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0		
Access																													RW		
Name																													PRSSEL		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**TAMPERSRC26 async channel select**
	TAMPERSRC26 async channel select			

14.5.51 PRS_CONSUMER_SETAMPER_TAMPERSRC27 - TAMPERSRC27 Consumer Register

Offset	Bit Position																															
0x130	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0		
Access																													RW		
Name																													PRSSEL		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**TAMPERSRC27 async channel select**
	TAMPERSRC27 async channel select			

14.5.52 PRS_CONSUMER_SETAMPER_TAMPERSRC28 - TAMPERSRC28 Consumer Register

Offset	Bit Position																															
0x134	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**TAMPERSRC28 async channel select**
	TAMPERSRC28 async channel select			

14.5.53 PRS_CONSUMER_SETAMPER_TAMPERSRC29 - TAMPERSRC29 Consumer Register

Offset	Bit Position																															
0x138	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**TAMPERSRC29 async channel select**
	TAMPERSRC29 async channel select			

14.5.54 PRS_CONSUMER_SETAMPER_TAMPERSRC30 - TAMPERSRC30 Consumer Register

Offset	Bit Position																															
0x13C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**TAMPERSRC30 async channel select**
	TAMPERSRC30 async channel select			

14.5.55 PRS_CONSUMER_SETAMPER_TAMPERSRC31 - TAMPERSRC31 Consumer Register

Offset	Bit Position																															
0x140	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**TAMPERSRC31 async channel select**
	TAMPERSRC31 async channel select			

14.5.56 PRS_CONSUMER_SYSRTC0_IN0 - IN0 Consumer Register

Offset	Bit Position																															
0x144	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**IN0 async channel select**
	IN0 async channel select			

14.5.57 PRS_CONSUMER_SYSRTC0_IN1 - IN1 Consumer Register

Offset	Bit Position																															
0x148	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**IN1 async channel select**
	IN1 async channel select			

14.5.58 PRS_CONSUMER_HFXO0_OSCREQ - OSCREQ Consumer Register

Offset	Bit Position																															
0x14C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**OSC async channel select**
	OSC async channel select			

14.5.59 PRS_CONSUMER_HFXO0_TIMEOUT - TIMEOUT Consumer Register

Offset	Bit Position																															
0x150	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**TIMEOUT async channel select**
	TIMEOUT async channel select			

14.5.60 PRS_CONSUMER_CORE_CTIIN0 - CTI Consumer Register

Offset	Bit Position																															
0x154	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CTI async channel select**
	CTI async channel select			

14.5.61 PRS_CONSUMER_CORE_CTIIN1 - CTI Consumer Register

Offset	Bit Position																															
0x158	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CTI async channel select**
	CTI async channel select			

14.5.62 PRS_CONSUMER_CORE_CTIIN2 - CTI Consumer Register

Offset	Bit Position																															
0x15C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CTI async channel select**
	CTI async channel select			

14.5.63 PRS_CONSUMER_CORE_CTIIN3 - CTI Consumer Register

Offset	Bit Position																															
0x160	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CTI async channel select**
	CTI async channel select			

14.5.64 PRS_CONSUMER_CORE_M33RXEV - M33 Consumer Register

Offset	Bit Position																													
0x164	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0		
Access																													RW		
Name																													PRSSEL		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**M33 async channel select**
	M33 async channel select			

14.5.65 PRS_CONSUMER_TIMER0_CC0 - CC0 Consumer Register

Offset	Bit Position																													
0x168	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0		
Access																							RW						RW		
Name																							SPRSSEL						PRSSEL		

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC0 sync channel select**
	CC0 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC0 async channel select**
	CC0 async channel select			

14.5.66 PRS_CONSUMER_TIMER0_CC1 - CC1 Consumer Register

Offset	Bit Position																													
0x16C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC1 sync channel select**
	CC1 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC1 async channel select**
	CC1 async channel select			

14.5.67 PRS_CONSUMER_TIMER0_CC2 - CC2 Consumer Register

Offset	Bit Position																													
0x170	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC2 sync channel select**
	CC2 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC2 async channel select**
	CC2 async channel select			

14.5.68 PRS_CONSUMER_TIMER0_DTI - DTI Consumer Register

Offset	Bit Position																															
0x174	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.69 PRS_CONSUMER_TIMER0_DTIFS1 - DTI Consumer Register

Offset	Bit Position																															
0x178	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.70 PRS_CONSUMER_TIMER0_DTIFS2 - DTI Consumer Register

Offset	Bit Position																															
0x17C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.71 PRS_CONSUMER_TIMER1_CC0 - CC0 Consumer Register

Offset	Bit Position																															
0x180	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC0 sync channel select**
	CC0 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC0 async channel select**
	CC0 async channel select			

14.5.72 PRS_CONSUMER_TIMER1_CC1 - CC1 Consumer Register

Offset	Bit Position																													
0x184	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC1 sync channel select**
	CC1 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC1 async channel select**
	CC1 async channel select			

14.5.73 PRS_CONSUMER_TIMER1_CC2 - CC2 Consumer Register

Offset	Bit Position																													
0x188	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC2 sync channel select**
	CC2 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC2 async channel select**
	CC2 async channel select			

14.5.74 PRS_CONSUMER_TIMER1_DTI - DTI Consumer Register

Offset	Bit Position																															
0x18C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.75 PRS_CONSUMER_TIMER1_DTIFS1 - DTI Consumer Register

Offset	Bit Position																															
0x190	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.76 PRS_CONSUMER_TIMER1_DTIFS2 - DTI Consumer Register

Offset	Bit Position																															
0x194	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.77 PRS_CONSUMER_TIMER2_CC0 - CC0 Consumer Register

Offset	Bit Position																															
0x198	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC0 sync channel select**
	CC0 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC0 async channel select**
	CC0 async channel select			

14.5.78 PRS_CONSUMER_TIMER2_CC1 - CC1 Consumer Register

Offset	Bit Position																													
0x19C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC1 sync channel select**
	CC1 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC1 async channel select**
	CC1 async channel select			

14.5.79 PRS_CONSUMER_TIMER2_CC2 - CC2 Consumer Register

Offset	Bit Position																													
0x1A0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC2 sync channel select**
	CC2 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC2 async channel select**
	CC2 async channel select			

14.5.80 PRS_CONSUMER_TIMER2_DTI - DTI Consumer Register

Offset	Bit Position																															
0x1A4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0		
Access																													RW		
Name																													PRSSEL		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.81 PRS_CONSUMER_TIMER2_DTIFS1 - DTI Consumer Register

Offset	Bit Position																															
0x1A8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0		
Access																													RW		
Name																													PRSSEL		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.82 PRS_CONSUMER_TIMER2_DTIFS2 - DTI Consumer Register

Offset	Bit Position																															
0x1AC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0		
Access																													RW		
Name																													PRSSEL		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.83 PRS_CONSUMER_TIMER3_CC0 - CC0 Consumer Register

Offset	Bit Position																															
0x1B0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC0 sync channel select**
	CC0 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC0 async channel select**
	CC0 async channel select			

14.5.84 PRS_CONSUMER_TIMER3_CC1 - CC1 Consumer Register

Offset	Bit Position																													
0x1B4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC1 sync channel select**
	CC1 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC1 async channel select**
	CC1 async channel select			

14.5.85 PRS_CONSUMER_TIMER3_CC2 - CC2 Consumer Register

Offset	Bit Position																													
0x1B8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC2 sync channel select**
	CC2 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC2 async channel select**
	CC2 async channel select			

14.5.86 PRS_CONSUMER_TIMER3_DTI - DTI Consumer Register

Offset	Bit Position																															
0x1BC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0		
Access																													RW		
Name																													PRSSEL		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.87 PRS_CONSUMER_TIMER3_DTIFS1 - DTI Consumer Register

Offset	Bit Position																															
0x1C0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0		
Access																													RW		
Name																													PRSSEL		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.88 PRS_CONSUMER_TIMER3_DTIFS2 - DTI Consumer Register

Offset	Bit Position																															
0x1C4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0		
Access																													RW		
Name																													PRSSEL		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.89 PRS_CONSUMER_TIMER4_CC0 - CC0 Consumer Register

Offset	Bit Position																															
0x1C8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0		
Access																							RW						RW		
Name																							SPRSSEL						PRSSEL		

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC0 sync channel select**
	CC0 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC0 async channel select**
	CC0 async channel select			

14.5.90 PRS_CONSUMER_TIMER4_CC1 - CC1 Consumer Register

Offset	Bit Position																													
0x1CC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC1 sync channel select**
	CC1 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC1 async channel select**
	CC1 async channel select			

14.5.91 PRS_CONSUMER_TIMER4_CC2 - CC2 Consumer Register

Offset	Bit Position																													
0x1D0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC2 sync channel select**
	CC2 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC2 async channel select**
	CC2 async channel select			

14.5.92 PRS_CONSUMER_TIMER4_DTI - DTI Consumer Register

Offset	Bit Position																															
0x1D4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.93 PRS_CONSUMER_TIMER4_DTIFS1 - DTI Consumer Register

Offset	Bit Position																															
0x1D8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.94 PRS_CONSUMER_TIMER4_DTIFS2 - DTI Consumer Register

Offset	Bit Position																															
0x1DC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0		
Access																													RW		
Name																													PRSSEL		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.95 PRS_CONSUMER_TIMER5_CC0 - CC0 Consumer Register

Offset	Bit Position																															
0x1E0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0		
Access																							RW						RW		
Name																							SPRSSEL						PRSSEL		

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC0 sync channel select**
	CC0 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC0 async channel select**
	CC0 async channel select			

14.5.96 PRS_CONSUMER_TIMER5_CC1 - CC1 Consumer Register

Offset	Bit Position																													
0x1E4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC1 sync channel select**
	CC1 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC1 async channel select**
	CC1 async channel select			

14.5.97 PRS_CONSUMER_TIMER5_CC2 - CC2 Consumer Register

Offset	Bit Position																													
0x1E8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC2 sync channel select**
	CC2 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC2 async channel select**
	CC2 async channel select			

14.5.98 PRS_CONSUMER_TIMER5_DTI - DTI Consumer Register

Offset	Bit Position																															
0x1EC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0		
Access																													RW		
Name																													PRSSEL		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.99 PRS_CONSUMER_TIMER5_DTIFS1 - DTI Consumer Register

Offset	Bit Position																															
0x1F0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0		
Access																													RW		
Name																													PRSSEL		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.100 PRS_CONSUMER_TIMER5_DTIFS2 - DTI Consumer Register

Offset	Bit Position																															
0x1F4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0		
Access																													RW		
Name																													PRSSEL		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.101 PRS_CONSUMER_TIMER6_CC0 - CC0 Consumer Register

Offset	Bit Position																															
0x1F8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC0 sync channel select**
	CC0 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC0 async channel select**
	CC0 async channel select			

14.5.102 PRS_CONSUMER_TIMER6_CC1 - CC1 Consumer Register

Offset	Bit Position																													
0x1FC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC1 sync channel select**
	CC1 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC1 async channel select**
	CC1 async channel select			

14.5.103 PRS_CONSUMER_TIMER6_CC2 - CC2 Consumer Register

Offset	Bit Position																													
0x200	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC2 sync channel select**
	CC2 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC2 async channel select**
	CC2 async channel select			

14.5.104 PRS_CONSUMER_TIMER6_DTI - DTI Consumer Register

Offset	Bit Position																															
0x204	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.105 PRS_CONSUMER_TIMER6_DTIFS1 - DTI Consumer Register

Offset	Bit Position																															
0x208	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.106 PRS_CONSUMER_TIMER6_DTIFS2 - DTI Consumer Register

Offset	Bit Position																															
0x20C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.107 PRS_CONSUMER_TIMER7_CC0 - CC0 Consumer Register

Offset	Bit Position																															
0x210	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC0 sync channel select**
	CC0 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC0 async channel select**
	CC0 async channel select			

14.5.108 PRS_CONSUMER_TIMER7_CC1 - CC1 Consumer Register

Offset	Bit Position																													
0x214	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC1 sync channel select**
	CC1 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC1 async channel select**
	CC1 async channel select			

14.5.109 PRS_CONSUMER_TIMER7_CC2 - CC2 Consumer Register

Offset	Bit Position																													
0x218	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0						0x0			
Access																							RW						RW			
Name																							SPRSSEL						PRSSEL			

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**CC2 sync channel select**
	CC2 sync channel select			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**CC2 async channel select**
	CC2 async channel select			

14.5.110 PRS_CONSUMER_TIMER7_DTI - DTI Consumer Register

Offset	Bit Position																															
0x21C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.111 PRS_CONSUMER_TIMER7_DTIFS1 - DTI Consumer Register

Offset	Bit Position																															
0x220	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.112 PRS_CONSUMER_TIMER7_DTIFS2 - DTI Consumer Register

Offset	Bit Position																															
0x224	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**DTI async channel select**
	DTI async channel select			

14.5.113 PRS_CONSUMER_VDAC0_ASYNCTRIGCH0 - ASYNCTRIG Consumer Register

Offset	Bit Position																															
0x228	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**ASYNCTRIG async channel select**
	ASYNCTRIG async channel select			

14.5.114 PRS_CONSUMER_VDAC0_ASYNCTRIGCH1 - ASYNCTRIG Consumer Register

Offset	Bit Position																													
0x22C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0		
Access																													RW		
Name																													PRSSEL		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**ASYNCTRIG async channel select**
	ASYNCTRIG async channel select			

14.5.115 PRS_CONSUMER_VDAC0_SYNCTRIGCH0 - SYNCTRIG Consumer Register

Offset	Bit Position																													
0x230	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0								
Access																							RW								
Name																							SPRSSEL								

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**SYNCTRIG sync channel select**
	SYNCTRIG sync channel select			
7:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

14.5.116 PRS_CONSUMER_VDAC0_SYNCTRIGCH1 - SYNCTRIG Consumer Register

Offset	Bit Position																													
0x234	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0								
Access																							RW								
Name																							SPRSSEL								

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	SPRSSEL	0x0	RW	**SYNCTRIG sync channel select**
	SYNCTRIG sync channel select			
7:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

14.5.117 PRS_CONSUMER_WDOG0_SRC0 - SRC0 Consumer Register

Offset	Bit Position																													
0x238	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0		
Access																													RW		
Name																													PRSSEL		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**SRC0 async channel select**
	SRC0 async channel select			

14.5.118 PRS_CONSUMER_WDOG0_SRC1 - SRC1 Consumer Register

Offset	Bit Position																															
0x23C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**SRC1 async channel select**
	SRC1 async channel select			

14.5.119 PRS_CONSUMER_WDOG1_SRC0 - SRC0 Consumer Register

Offset	Bit Position																															
0x240	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

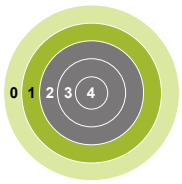
Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**SRC0 async channel select**
	SRC0 async channel select			

14.5.120 PRS_CONSUMER_WDOG1_SRC1 - SRC1 Consumer Register

Offset	Bit Position																															
0x244	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													PRSSEL			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	PRSSEL	0x0	RW	**SRC1 async channel select**
	SRC1 async channel select			

15. GPCRC - General Purpose Cyclic Redundancy Check



Quick Facts

What?

The GPCRC is an error-detecting module commonly used in digital networks and storage systems to detect accidental changes to data.

Why?

The GPCRC module can detect errors in data, giving a higher system reliability and robustness.

How?

Blocks of data entering GPCRC module can have a short checksum, based on the remainder of a polynomial division of their contents; on retrieval the calculation is repeated, and corrective action can be taken against presumed data corruption if the check values do not match.

15.1 Introduction

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7(IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application. Common 16-bit polynomials are 0x1021 (CCITT-16), 0x3D65 (IEC16-MBus), and 0x8005 (zigbee, 802.15.4, and USB).

15.2 Features

- Programmable 16-bit polynomial, fixed 32-bit polynomial
- Byte-level bit reversal for the CRC input
- Byte-order reorientation for the CRC input
- Word or half-word bit reversal of the CRC result
- Ability to configure and seed an operation in a single register write
- Single-cycle CRC computation for 32-, 16-, or 8-bit blocks
- DMA operation

15.3 Functional Description

An overview of the GPCRC module is shown in Figure 15.1 GPCRC Overview on page 486.

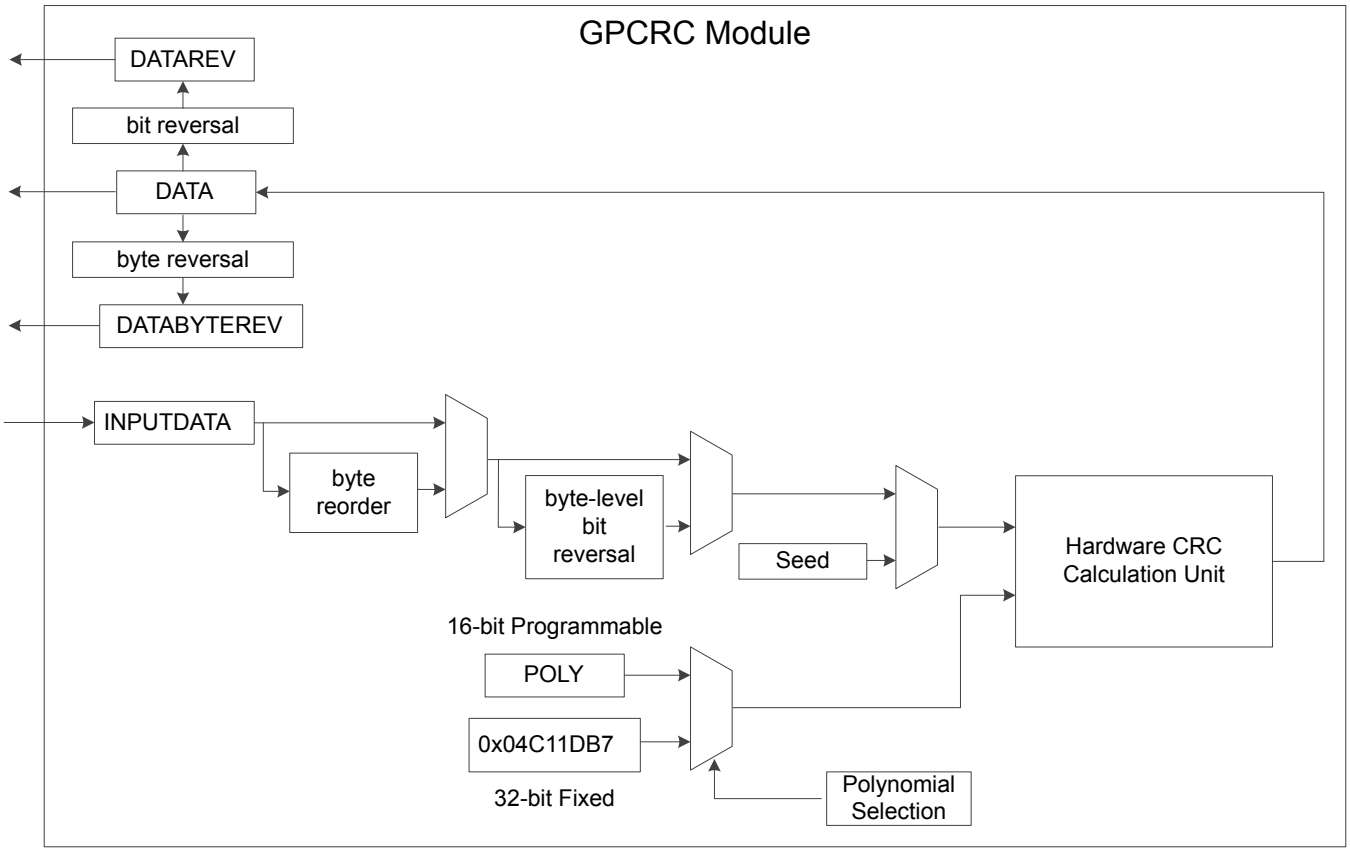


Figure 15.1. GPCRC Overview

15.3.1 Polynomial Specification

POLYSEL in GPCRC_CTRL selects between 32-bit and 16-bit polynomial functions. When a 32-bit polynomial is selected, the fixed IEEE 802.3 polynomial(0x04C11DB7) is used. When a 16-bit polynomial is selected, any valid polynomial can be defined by the user in GPCRC_POLY.

A valid 16-bit CRC polynomial must have an x^16 term and an x^0 term. Theoretically, a 16-bit polynomial has 17 terms total. The convention used is to omit the x^16 term. The polynomial should be written in **reversed** (little endian) bit order. The most significant bit corresponds to the lowest order term. Thus, the most significant bit in CRC_POLY represents the x^0 term, and the least significant bit in CRC_POLY represents the x^15 term. The highest significant bit of CRC_POLY should always set to 1.The polynomial representation for the CRC-16-CCIT polynomial x^16 + x^12 + x^5 + 1, or 0x8408 in reversed order, is shown in Figure 15.2 Polynomial Representation on page 487.

CRC-16-CCITT Normal: 0x1021 Reversed: 0x8408

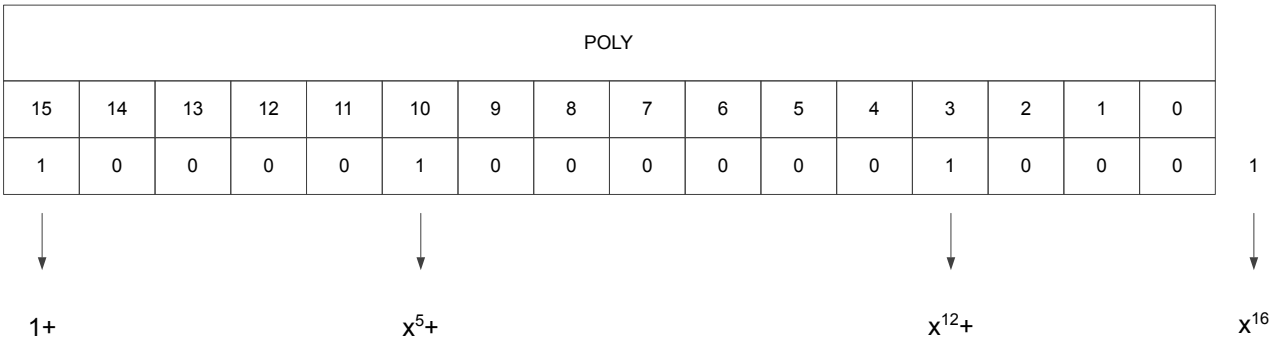


Figure 15.2. Polynomial Representation

15.3.2 Input and Output Specification

The CRC input data can be written to the GPCRC_INPUTDATA, GPCRC_INPUTDATAHWORD or GPCRC_INPUTDATABYTE register via the APB bus based on different data size. If BYTEMODE in GPCRC_CTRL is set, only the least significant byte of the data word will be used for the CRC calculation no matter which input register is written. There are also three output registers for different ordering. Reading from GPCRC_DATA will get the result based on the polynomial in reversed order, while reading from GPCRC_DATAREV will get the result based on the polynomial in normal order. The CRC calculation completes in one clock cycle. Reads from the GPCRC_DATA, GPCRC_DATAREV or GPCRC_DATABYTEREV registers and writes to the GPCRC_CMD register are halted while the calculation is in progress.

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15.3.3 Initialization

The CRC can be pre-loaded or re-initialized by first writing a 32-bit programmable init value to INIT in GPCRC_INIT and then setting INIT in GPCRC_CMD. It can also be re-initialized automatically when read from DATA, DATAREV or DATABYTEREV provided that AUTOINIT in GPCRC_CTRL is set, the CRC would be re-initialized with the stored init value.

15.3.4 DMA Usage

A DMA channel may be used to transfer data into the CRC engine. All bytes and half-word writes must be word-aligned. The recommended DMA usage model is to use the DMA to transfer all available words of data and use software writes to capture any remaining bytes.

15.3.5 Byte-Level Bit Reversal and Byte Reordering

The byte-level bit reversal and byte reordering operations occur before the data is used in the CRC calculation. Byte reordering can occur on words or half words. The hardware ignores the BYTEREVERSE field with any byte writes or operations with byte mode enabled (BYTEMODE = 1), but the bit reversal settings (BITREVERSE) are still applied to the byte. 32-bit little endian MSB-first data can be treated like 32-bit little endian LSB-first data, as shown in Figure 15.3 Data Ordering Example - 32-bit MSB -first to LSB-first on page 488. In this example, 32-bit data is written to GPCRC_INPUTDATA, BYTEREVERSE is set for byte ordering, and BITREVERSE is set for byte-level bit reversal.

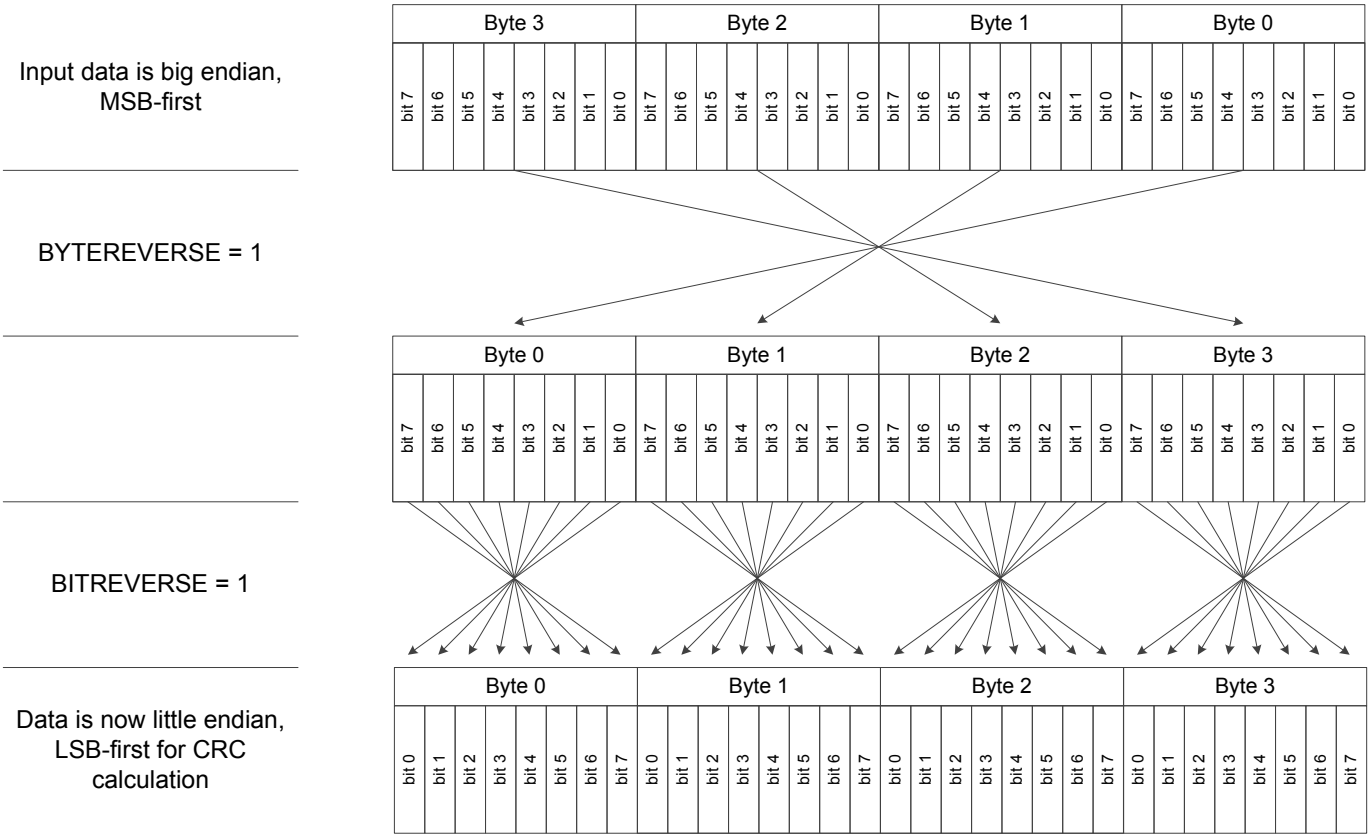


Figure 15.3. Data Ordering Example - 32-bit MSB -first to LSB-first

When handling 16-bit data, the byte reordering function only swap the two lowest bytes and clear the two highest bytes, as shown in Figure 15.4 Data Ordering Example - 16-bit MSB -first to LSB-first on page 489. In this example, 16-bit data is written to GPCRC_INPUTDATAHWORD, BYTEREVERSE is set for byte ordering, and BITREVERSE is set for byte-level bit reversal.

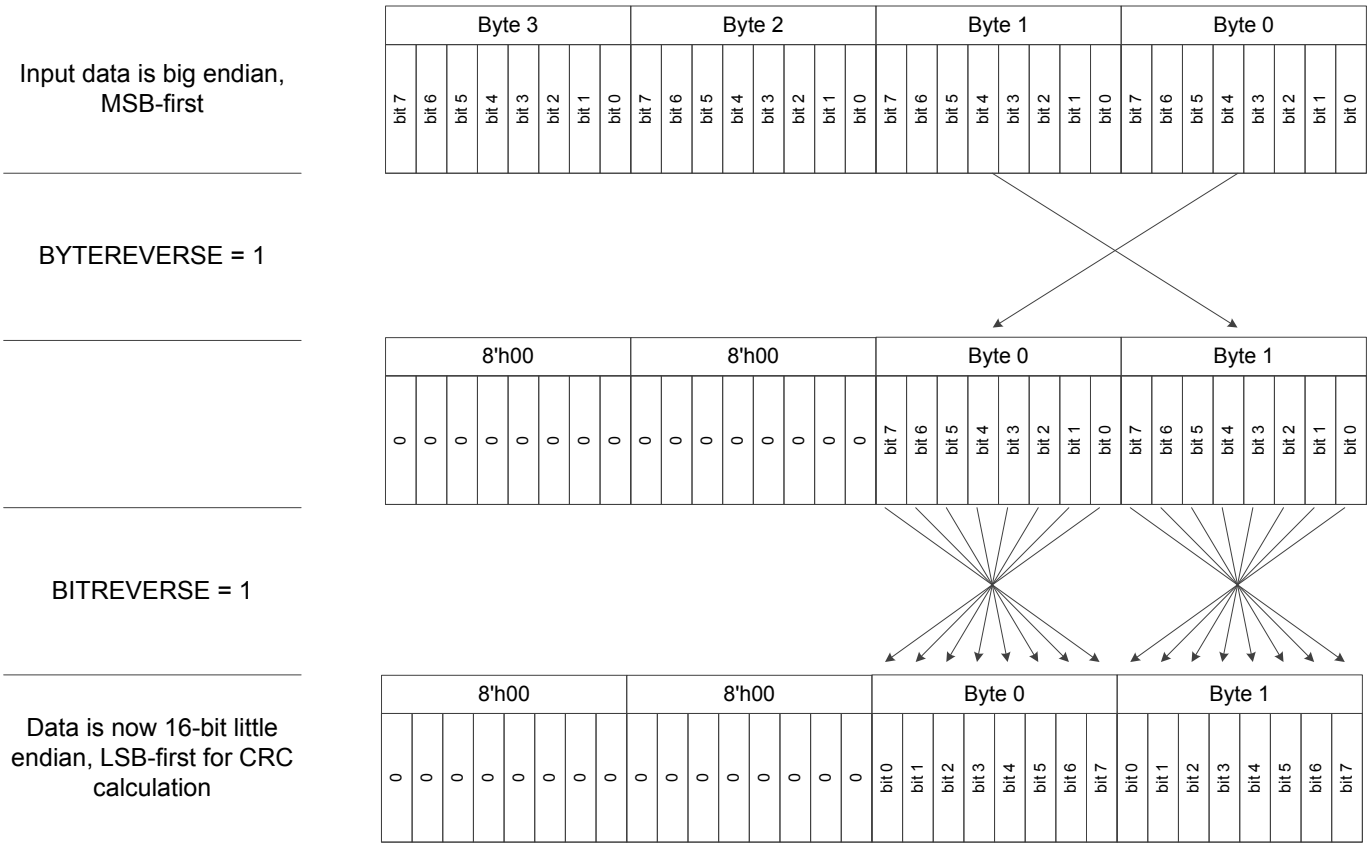


Figure 15.4. Data Ordering Example - 16-bit MSB -first to LSB-first

Assuming a word input byte order of B3 B2 B1 B0, the values used in the CRC calculation for the various settings of the byte-level bit reversal and byte reordering are shown in Table 15.1 Byte-Level Bit Reversal and Byte Reordering Results (B3 B2 B1 B0 Input Order) on page 489.

Table 15.1. Byte-Level Bit Reversal and Byte Reordering Results (B3 B2 B1 B0 Input Order)

Input Width(bits)	BYTEREVERSE Setting	BITREVERSE Setting	Input to CRC Calculation
32	0	0	B3 B2 B1 B0
32	1	1	'B0 'B1 'B2 'B3
32	1	0	B0 B1 B2 B3
32	0	1	'B3 'B2 'B1 'B0
16	0	0	XX XX B1 B0
16	1	1	XX XX 'B0 'B1
16	1	0	XX XX B0 B1
16	0	1	XX XX 'B1 'B0
8	-	0	XX XX XX XX B0
8	-	1	XX XX XX XX 'B0

Input Width(bits)	BYTEREVERSE Setting	BITREVERSE Setting	Input to CRC Calculation

Notes:

1. X indicates a "don't care".
2. Bn is the byte field within the word.
3. 'Bn is the bit-reversed byte field within the word.

15.4 GPCRC Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	GPCRC_IPVERSION	R	IP Version ID
0x004	GPCRC_EN	RW	CRC Enable
0x008	GPCRC_CTRL	RW	Control Register
0x00C	GPCRC_CMD	W	Command Register
0x010	GPCRC_INIT	RWH	CRC Init Value
0x014	GPCRC_POLY	RW	CRC Polynomial Value
0x018	GPCRC_INPUTDATA	W	Input 32-Bit Data Register
0x01C	GPCRC_INPUTDATAHWORD	W	Input 16-Bit Data Register
0x020	GPCRC_INPUTDATABYTE	W	Input 8-Bit Data Register
0x024	GPCRC_DATA	RH(r)	CRC Data Register
0x028	GPCRC_DATAREV	RH(r)	CRC Data Reverse Register
0x02C	GPCRC_DATABYTEREV	RH(r)	CRC Data Byte Reverse Register
0x1000	GPCRC_IPVERSION_SET	R	IP Version ID
0x1004	GPCRC_EN_SET	RW	CRC Enable
0x1008	GPCRC_CTRL_SET	RW	Control Register
0x100C	GPCRC_CMD_SET	W	Command Register
0x1010	GPCRC_INIT_SET	RWH	CRC Init Value
0x1014	GPCRC_POLY_SET	RW	CRC Polynomial Value
0x1018	GPCRC_INPUTDATA_SET	W	Input 32-Bit Data Register
0x101C	GPCRC_INPUTDATAH-WORD_SET	W	Input 16-Bit Data Register
0x1020	GPCRC_INPUTDATA-BYTE_SET	W	Input 8-Bit Data Register
0x1024	GPCRC_DATA_SET	RH(r)	CRC Data Register
0x1028	GPCRC_DATAREV_SET	RH(r)	CRC Data Reverse Register
0x102C	GPCRC_DATABYTEREV_SET	RH(r)	CRC Data Byte Reverse Register
0x2000	GPCRC_IPVERSION_CLR	R	IP Version ID
0x2004	GPCRC_EN_CLR	RW	CRC Enable
0x2008	GPCRC_CTRL_CLR	RW	Control Register
0x200C	GPCRC_CMD_CLR	W	Command Register
0x2010	GPCRC_INIT_CLR	RWH	CRC Init Value
0x2014	GPCRC_POLY_CLR	RW	CRC Polynomial Value
0x2018	GPCRC_INPUTDATA_CLR	W	Input 32-Bit Data Register
0x201C	GPCRC_INPUTDATAH-WORD_CLR	W	Input 16-Bit Data Register
0x2020	GPCRC_INPUTDATA-BYTE_CLR	W	Input 8-Bit Data Register

Offset	Name	Type	Description
0x2024	GPCRC_DATA_CLR	RH(r)	CRC Data Register
0x2028	GPCRC_DATAREV_CLR	RH(r)	CRC Data Reverse Register
0x202C	GPCRC_DATABYTEREV_CLR	RH(r)	CRC Data Byte Reverse Register
0x3000	GPCRC_IPVERSION_TGL	R	IP Version ID
0x3004	GPCRC_EN_TGL	RW	CRC Enable
0x3008	GPCRC_CTRL_TGL	RW	Control Register
0x300C	GPCRC_CMD_TGL	W	Command Register
0x3010	GPCRC_INIT_TGL	RWH	CRC Init Value
0x3014	GPCRC_POLY_TGL	RW	CRC Polynomial Value
0x3018	GPCRC_INPUTDATA_TGL	W	Input 32-Bit Data Register
0x301C	GPCRC_INPUTDATAH-WORD_TGL	W	Input 16-Bit Data Register
0x3020	GPCRC_INPUTDATA-BYTE_TGL	W	Input 8-Bit Data Register
0x3024	GPCRC_DATA_TGL	RH(r)	CRC Data Register
0x3028	GPCRC_DATAREV_TGL	RH(r)	CRC Data Reverse Register
0x302C	GPCRC_DATABYTEREV_TGL	RH(r)	CRC Data Byte Reverse Register

15.5 GPCRC Register Description

15.5.1 GPCRC_IPVERSION - IP Version ID

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x0	R	**IP Version ID**
	The read only IPVERSION field gives the version for this module. There may be minor software changes required for modules with different values of IPVERSION.			

15.5.2 GPCRC_EN - CRC Enable

Offset	Bit Position																															
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																RW
Name																																EN

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	EN	0x0	RW	**CRC Enable**

The ENABLE bit enables the module. Software should write to CONFIG type registers before setting the ENABLE bit. Software should write to SYNC type registers only after setting the ENABLE bit.

Value	Mode	Description
0	DISABLE	Disable CRC function. Reordering functions are still available. Only BITREVERSE and BYTEREVERSE bits are configurable in this mode.
1	ENABLE	Writes to INPUTDATA registers will result in CRC operations.

15.5.3 GPCRC_CTRL - Control Register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																			0x0			0x0	0x0	0x0				0x0				
Access																			RW			RW	RW	RW				RW				
Name																			AUTOINIT			BYTEREVERSE	BITREVERSE	BYTEMODE				POLYSEL				

Bit	Name	Reset	Access	Description
31:14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13	AUTOINIT	0x0	RW	**Auto Init Enable**
	Enables auto init by re-seeding the CRC result based on the value in INIT after reading of DATA, DATAREV or DATABYTEREV.			
12:11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10	BYTEREVERSE	0x0	RW	**Byte Reverse Mode**
	Allows byte level reverse of bytes B3, B2, B1, B0 within the 32-bit data word			

Value	Mode	Description
0	NORMAL	No reverse: B3, B2, B1, B0
1	REVERSED	Reverse byte order. For 32-bit: B0, B1, B2, B3; For 16-bit: 0, 0, B0, B1

Bit	Name	Reset	Access	Description
9	BITREVERSE	0x0	RW	**Byte-level Bit Reverse Enable**
	Reverses bits within each byte of the 32-bit data word			

Value	Mode	Description
0	NORMAL	No reverse
1	REVERSED	Reverse bit order in each byte

Bit	Name	Reset	Access	Description
8	BYTEMODE	0x0	RW	**Byte Mode Enable**
	Treats all writes as bytes. Only the least significant byte of the data-word will be used for CRC calculation for all writes			
7:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	POLYSEL	0x0	RW	**Polynomial Select**
	Selects 16-bit CRC programmable polynomial or 32-bit CRC fixed polynomial			

Value	Mode	Description
0	CRC32	CRC-32 (0x04C11DB7) polynomial selected
1	CRC16	16-bit CRC programmable polynomial selected

Bit	Name	Reset	Access	Description
3:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

15.5.4 GPCRC_CMD - Command Register

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																W
Name																																INIT

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	INIT	0x0	W	**Initialization Enable**
	Writing 1 to this bit initialize the CRC by writing the INIT value in CRC_INIT to CRC_DATA.			

15.5.5 GPCRC_INIT - CRC Init Value

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																0x0																
Access																RW																
Name																INIT																

Bit	Name	Reset	Access	Description
31:0	INIT	0x0	RW	**CRC Initialization Value**
	This value is loaded into CRC_DATA upon issuing the INIT command in CRC_CMD			

15.5.6 GPCRC_POLY - CRC Polynomial Value

Offset	Bit Position																															
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	RW															
Name																	POLY															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	POLY	0x0	RW	**CRC Polynomial Value**
	This value defines 16-bit POLY, which is used as the polynomial during the 16-bit CRC calculation. The polynomial is defined in reversed representation, meaning that the lowest degree term is in the highest bit position of POLY. Additionally, the highest degree term in the polynomial is implicit. Further examples of the CRC configuration can be found in the documentation.			

15.5.7 GPCRC_INPUTDATA - Input 32-Bit Data Register

Offset	Bit Position																															
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																0x0																
Access																W																
Name																INPUTDATA																

Bit	Name	Reset	Access	Description
31:0	INPUTDATA	0x0	W	**Input Data for 32-bit**
	CRC Input 32-bit Data can be written to this register. Each time this register is written, the CRC value is updated.			

15.5.8 GPCRC_INPUTDATAHWORD - Input 16-Bit Data Register

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	W															
Name																	INPUTDATAHWORD															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	INPUTDATAHWORD	0x0	W	**Input Data for 16-bit**
	CRC Input 16-bit Data can be written to this register. Each time this register is written, the CRC value is updated.			

15.5.9 GPCRC_INPUTDATABYTE - Input 8-Bit Data Register

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									W							
Name																									INPUTDATABYTE							

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	INPUTDATABYTE	0x0	W	**Input Data for 8-bit**
	CRC Input 8-bit Data can be written to this register. Each time this register is written, the CRC value is updated.			

15.5.10 GPCRC_DATA - CRC Data Register

Offset	Bit Position																													
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R(r)																															
Name	DATA																															

Bit	Name	Reset	Access	Description
31:0	DATA	0x0	R(r)	**CRC Data Register**
	CRC Data Register, read only. The CRC data register may still be indirectly written from software, by writing the INIT register and then issue an INITIALIZE command.			

15.5.11 GPCRC_DATAREV - CRC Data Reverse Register

Offset	Bit Position																													
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R(r)																															
Name	DATAREV																															

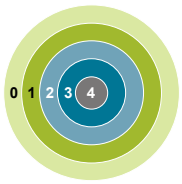
Bit	Name	Reset	Access	Description
31:0	DATAREV	0x0	R(r)	**Data Reverse Value**
	Bit reversed version of CRC Data register. When a 32-bit CRC polynomial is selected, the reversal occurs on the entire 32-bit word. When a 16-bit CRC polynomial is selected, the bits [15:0] are reversed.			

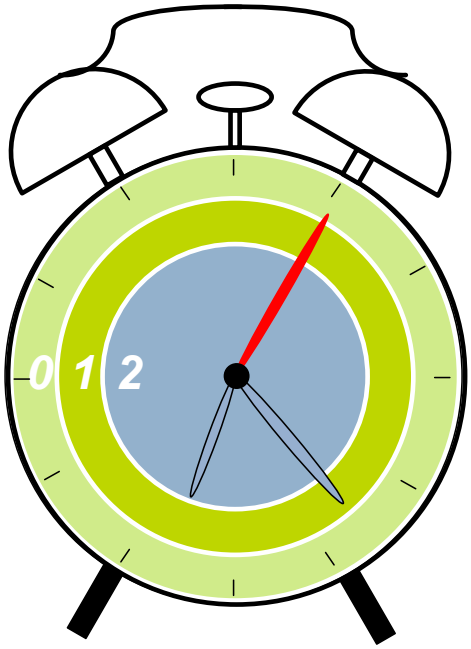
15.5.12 GPCRC_DATABYTEREV - CRC Data Byte Reverse Register

Offset	Bit Position																													
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R(r)																															
Name	DATABYTEREV																															

Bit	Name	Reset	Access	Description
31:0	DATABYTEREV	0x0	R(r)	**Data Byte Reverse Value**
	Byte reversed version of CRC Data register. When a 32-bit CRC polynomial is selected, the bytes are swizzled to {B0, B1, B2, B3}. When a 16-bit CRC polynomial is selected, the bytes are swizzled to {0, 0, B0, B1}.			

16. SYSRTC - System RTC





Quick Facts

What?

The System Real-Time Counter (SYSRTC) is a 32-bit Real Time Clock ensuring timekeeping in low energy modes.

Why?

Timekeeping over long time periods while using as little power as possible is required in many low power applications.

How?

The SYSRTC operates a central counter off a low-frequency oscillator source. It has configurable compare and capture channels which can be used to trigger wake-up, generate PRS signalling, or capture system events. The SYSRTC allows the system to stay in low energy modes for long periods of time and maintain reliable timekeeping.

16.1 Introduction

The SYSRTC (System Real Time Counter), is a 32-bit counter kept running down to energy mode EM3. It can be used as a sleep timer / wakeup source as well as a timekeeping counter during low energy modes. Multiple groups of capture / compare registers are available to different cores in the system, allowing the peripheral and time base to be shared across cores and save energy. Only group 0 registers are directly accessible to the main processor core, but compare / capture signals and interrupts from group 1 are also available to the main processor.

Capture compare channels can be used to trigger interrupts, generate PRS signals, capture PRS events, and to wake the device up from EM1, EM2, or EM3.

Note: Critical portions of the EFR32/EFM32 software stack related to system timing and power management make use of SYSRTC in such a way that it is effectively unavailable to user software. Please refer to relevant software documentation for additional information.

16.2 Features

- 32-bit counter
- Debug mode
- 32.768 kHz LFXO or LFRCO / 1 kHz ULFRCO
- Low energy wake-up source
- Separate groups of capture / compare registers and signals
  - MCU core and Radio core each control one group
  - 2 compare channels per group
  - 1 capture channel per group
  - Separate interrupt vectors for MCU and Radio events
  - Capture / compare available in PRS

16.3 Functional Description

16.3.1 Interrupts and Wake Events

Each group has a dedicated, independent interrupt line, and has the ability to wake the system. The Group 0 interrupt line (SYSRTC_APP) is used and fully controlled by user code running on the main processor. The Group 1 interrupt line (SYSRTC_SEQ) is also available to the main processor, but Group 1 registers and configuration are not directly available to the user application.

16.3.2 Counter

A single counter value (CNT) is used across all groups. The SYSRTC module is enabled by setting its EN bit field. The counter value is asserted to 0x00000000 on reset. The counter can be started/stopped by writing to the START/STOP bit fields in the CMD register. The RUNNING field in the STATUS register indicates that the counter is running when it is set.

Once started, the counter increments by 1 on each cycle (typically 32.768 kHz). The counter value can be programmed directly by writing to the CNT register. Once the programmed value is applied and the counter is running, the counter will increment on every clock starting from the newly programmed value.

When the counter reaches its maximum value of 0xFFFFFFFF, an overflow event is generated, followed by a counter wrap-around to its reset value (from which counting continues) and the OVF interrupt flag (OVFIF) on the next cycle. The overflow event is common for all the groups, i.e. OVFIF flags in all groups get set.

The normal operation of SYSRTC is to configure it, enable it, start it, and then leave it running. This should be done by a single core so that other cores only access the registers for their designated group as needed. If SYSRTC needs to be disabled, it is recommended to stop it first using the STOP command.

16.3.3 Compare Events

A compare event for channel "x" of group "n" is generated whenever the counter is RUNNING, the CMPxEN bit is set / enabled in the GRPn_CTRL register, and the CNT value is equal to the GRPn_CMPxVALUE register setting. This event is followed by GRPn_IF.CMPxIF being set on the next counter clock cycle.

Compare events can be routed as PRS producers on the GRPnOUTx signals. There are several options for the match action, selected by CMPxCMOA in GRPn_CTRL. Note that when using the PULSE option, the PRS output should already be cleared for the pulse to get set and the PULSE option should remain configured until the pulse is cleared (otherwise if the PULSE option is reprogrammed to the SET option, the "pulse" remains set). A possible use case when using the CMPIF option is to signal early events prior to the following wake-up. After wakeup, the compare flag should be processed and cleared. To avoid a race condition on the PRS output, the compare flag should be cleared away from the next possible compare event.

Note that when setting the compare value to the current counter value, a compare event may not get generated until the counter overflows and reaches the current value again. To generate a compare event quickly, it is recommended to program the compare value to the current counter value + 1. Compare events are group-specific.

16.3.4 Capture Events

SYSRTC groups support counter value capture triggered by PRS consumer signals. For group "n" the SYSRTC0 "INn" PRS consumer is used to trigger captures. Capture can be triggered on RISING, FALLING, or BOTH edges, according to the setting programmed in CAP0EDGE of the GRPn_CTRL register. A capture event for group "n" is generated whenever the counter is RUNNING, the CAP0EN bit is set / enabled in the GRPn_CTRL register, and the desired event occurs on the PRS output.

A capture event is followed by GRPn_IF_CAP0IF being set after up to 3 counter clock cycles. At the same time the flag is set, the GRPn_CAP0VALUE register captures the current counter value. Note that PRS input edges should not occur more frequently than once every three counter cycles. If the counter is being started/stopped or GRPn_CTRL.CAP0EN / GRPn_CTRL.CAP0EDGE is changed close to the PRS input edge, a race condition may occur. Capture events are group-specific.

16.3.5 SYSRTC Behavior on SWRST/Disablement/STOP

On SWRST / Disablement, the counter is reset to 0x00000000, PRS outputs are cleared, compare/capture events are disabled, compare/capture flags are reset, and the CAP0VALUE register is reset.

When the counter is stopped using the STOP command in the CMD register, all other settings remain unchanged, except that the RUNNING status will return to 0, which blocks any compare/capture events until the counter is started again.

16.3.6 Debug Functionality

By default, the counter value is frozen when the main processor is halted during debugging. The RUNNING status bit is not affected by debug halt, and will continue to indicate that the counter is active. If DEBUGRUN in the CFG register is set, the counter will not halt when the main processor is halted, and SYSRTC will continue to count clocks.

Note that the main processor runs on a much higher frequency than the counter and that the halt condition needs to last long enough (more than 3 counter cycles) for the counter to reach the frozen state.

16.4 SYSRTC Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	SYSRTC_IPVERSION	R	IP VERSION
0x004	SYSRTC_EN	RW ENABLE	Module Enable Register
0x008	SYSRTC_SWRST	RW SWRST	Software Reset Register
0x00C	SYSRTC_CFG	RW CONFIG	Configuration Register
0x010	SYSRTC_CMD	W LFSYNC	Command Register
0x014	SYSRTC_STATUS	RH	Status Register
0x018	SYSRTC_CNT	RWH LFSYNC	Counter Value Register
0x01C	SYSRTC_SYNCBUSY	RH	Synchronization Busy Register
0x020	SYSRTC_LOCK	W	Configuration Lock Register
0x040	SYSRTC_GRP0_IF	RWH INTFLAG	Group Interrupt Flags
0x044	SYSRTC_GRP0_IEN	RW	Group Interrupt Enables
0x048	SYSRTC_GRP0_CTRL	RW	Group Control Register
0x04C	SYSRTC_GRP0_CMP0VALUE	RW	Compare 0 Value Register
0x050	SYSRTC_GRP0_CMP1VALUE	RW	Compare 1 Value Register
0x054	SYSRTC_GRP0_CAP0VALUE	RH	Capture 0 Value Register
0x058	SYSRTC_GRP0_SYNCBUSY	RH	Synchronization Busy Register
0x1000	SYSRTC_IPVERSION_SET	R	IP VERSION
0x1004	SYSRTC_EN_SET	RW ENABLE	Module Enable Register
0x1008	SYSRTC_SWRST_SET	RW SWRST	Software Reset Register
0x100C	SYSRTC_CFG_SET	RW CONFIG	Configuration Register
0x1010	SYSRTC_CMD_SET	W LFSYNC	Command Register
0x1014	SYSRTC_STATUS_SET	RH	Status Register
0x1018	SYSRTC_CNT_SET	RWH LFSYNC	Counter Value Register
0x101C	SYSRTC_SYNCBUSY_SET	RH	Synchronization Busy Register
0x1020	SYSRTC_LOCK_SET	W	Configuration Lock Register
0x1040	SYSRTC_GRP0_IF_SET	RWH INTFLAG	Group Interrupt Flags
0x1044	SYSRTC_GRP0_IEN_SET	RW	Group Interrupt Enables
0x1048	SYSRTC_GRP0_CTRL_SET	RW	Group Control Register
0x104C	SYSRTC_GRP0_CMP0VAL-UE_SET	RW	Compare 0 Value Register
0x1050	SYSRTC_GRP0_CMP1VAL-UE_SET	RW	Compare 1 Value Register
0x1054	SYSRTC_GRP0_CAP0VAL-UE_SET	RH	Capture 0 Value Register
0x1058	SYSRTC_GRP0_SYN-CBUSY_SET	RH	Synchronization Busy Register
0x2000	SYSRTC_IPVERSION_CLR	R	IP VERSION

Offset	Name	Type	Description
0x2004	SYSRTC_EN_CLR	RW ENABLE	Module Enable Register
0x2008	SYSRTC_SWRST_CLR	RW SWRST	Software Reset Register
0x200C	SYSRTC_CFG_CLR	RW CONFIG	Configuration Register
0x2010	SYSRTC_CMD_CLR	W LFSYNC	Command Register
0x2014	SYSRTC_STATUS_CLR	RH	Status Register
0x2018	SYSRTC_CNT_CLR	RWH LFSYNC	Counter Value Register
0x201C	SYSRTC_SYNCBUSY_CLR	RH	Synchronization Busy Register
0x2020	SYSRTC_LOCK_CLR	W	Configuration Lock Register
0x2040	SYSRTC_GRP0_IF_CLR	RWH INTFLAG	Group Interrupt Flags
0x2044	SYSRTC_GRP0_IEN_CLR	RW	Group Interrupt Enables
0x2048	SYSRTC_GRP0_CTRL_CLR	RW	Group Control Register
0x204C	SYSRTC_GRP0_CMP0VAL-UE_CLR	RW	Compare 0 Value Register
0x2050	SYSRTC_GRP0_CMP1VAL-UE_CLR	RW	Compare 1 Value Register
0x2054	SYSRTC_GRP0_CAP0VAL-UE_CLR	RH	Capture 0 Value Register
0x2058	SYSRTC_GRP0_SYN-CBUSY_CLR	RH	Synchronization Busy Register
0x3000	SYSRTC_IPVERSION_TGL	R	IP VERSION
0x3004	SYSRTC_EN_TGL	RW ENABLE	Module Enable Register
0x3008	SYSRTC_SWRST_TGL	RW SWRST	Software Reset Register
0x300C	SYSRTC_CFG_TGL	RW CONFIG	Configuration Register
0x3010	SYSRTC_CMD_TGL	W LFSYNC	Command Register
0x3014	SYSRTC_STATUS_TGL	RH	Status Register
0x3018	SYSRTC_CNT_TGL	RWH LFSYNC	Counter Value Register
0x301C	SYSRTC_SYNCBUSY_TGL	RH	Synchronization Busy Register
0x3020	SYSRTC_LOCK_TGL	W	Configuration Lock Register
0x3040	SYSRTC_GRP0_IF_TGL	RWH INTFLAG	Group Interrupt Flags
0x3044	SYSRTC_GRP0_IEN_TGL	RW	Group Interrupt Enables
0x3048	SYSRTC_GRP0_CTRL_TGL	RW	Group Control Register
0x304C	SYSRTC_GRP0_CMP0VAL-UE_TGL	RW	Compare 0 Value Register
0x3050	SYSRTC_GRP0_CMP1VAL-UE_TGL	RW	Compare 1 Value Register
0x3054	SYSRTC_GRP0_CAP0VAL-UE_TGL	RH	Capture 0 Value Register
0x3058	SYSRTC_GRP0_SYN-CBUSY_TGL	RH	Synchronization Busy Register

16.5 SYSRTC Register Description

16.5.1 SYSRTC_IPVERSION - IP VERSION

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x1																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x1	R	**IP VERSION**
	Gives access to the IP VERSION of SYSRTC			

16.5.2 SYSRTC_EN - Module Enable Register

Offset	Bit Position																															
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	RW
Name																															DISABLING	EN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DISABLING	0x0	R	**Disablement busy status**
	Set when EN cleared and cleared when the peripheal core reset is finished			
0	EN	0x0	RW	**SYSRTC Enable**
	Enable the SYSRTC by requesting Clk from CMU			

16.5.3 SYSRTC_SWRST - Software Reset Register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	W
Name																															RESETTING	SWRST

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	RESETTING	0x0	R	**Software reset busy status** When SWRST command is issued, resetting logic sets this status immediately and it is later cleared when the reset process is finished
0	SWRST	0x0	W	**Software reset command** A software reset command field resets the module back to the initial condition, similar to the power-on reset condition

16.5.4 SYSRTC_CFG - Configuration Register

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																RW
Name																																DEBUGRUN

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	DEBUGRUN	0x0	RW	**Debug Mode Run Enable** Set this bit to keep the SYSRTC running during a debug halt.

Value	Mode	Description
0	DISABLE	SYSRTC is frozen in debug mode
1	ENABLE	SYSRTC is running in debug mode

16.5.5 SYSRTC_CMD - Command Register

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															W(nB)	W(nB)
Name																															STOP	START

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	STOP	0x0	W(nB)	**Stop SYSRTC**
	Write a 1 to stop the SYSRTC			
0	START	0x0	W(nB)	**Start SYSRTC**
	Write a 1 to start the SYSRTC			

16.5.6 SYSRTC_STATUS - Status Register

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	R
Name																															LOCKSTATUS	RUNNING

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	LOCKSTATUS	0x0	R	**Lock Status**
	Indicates the current status of SYSRTC Lock			

Value	Mode	Description
0	UNLOCKED	SYSRTC registers are unlocked
1	LOCKED	SYSRTC registers are locked

Bit	Name	Reset	Access	Description
0	RUNNING	0x0	R	**SYSRTC running status**
	Indicates the current status of SYSRTC running			

16.5.7 SYSRTC_CNT - Counter Value Register

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	CNT																															

Bit	Name	Reset	Access	Description
31:0	CNT	0x0	RW	**Counter Value**
	Gives access to the counter value of the SYSRTC.			

16.5.8 SYSRTC_SYNCBUSY - Synchronization Busy Register

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x0	0x0	0x0
Access																														R	R	R
Name																														CNT	STOP	START

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	CNT	0x0	R	**Sync busy for CNT bitfield**
	Last writing of CNT is synchronizing to LF clock			
1	STOP	0x0	R	**Sync busy for STOP bitfield**
	Last writing of STOP is synchronizing to LF clock			
0	START	0x0	R	**Sync busy for START bitfield**
	Last writing of START is synchronizing to LF clock			

16.5.9 SYSRTC_LOCK - Configuration Lock Register

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									W							
Name																									LOCKKEY							

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LOCKKEY	0x0	W	**Configuration Lock Key**
	Write any other value than the unlock code to lock EN, SWRST, CFG, CMD, CNT registers from editing. Write the unlock code to unlock.			

Value	Mode	Description
18294	UNLOCK	Write to unlock SYSRTC lockable registers

16.5.10 SYSRTC_GRP0_IF - Group Interrupt Flags

Offset	Bit Position																													
0x040	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0	0x0	0x0	0x0
Access																													RW	RW	RW	RW
Name																													CAP0	CMP1	CMP0	OVF

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	CAP0	0x0	RW	**Capture 0 Interrupt Flag**
	This bit is set when CAP0VALUE is updated			
2	CMP1	0x0	RW	**Compare 1 Interrupt Flag**
	This bit is set when counter matches COMP1VALUE			
1	CMP0	0x0	RW	**Compare 0 Interrupt Flag**
	This bit is set when counter matches COMP0VALUE			
0	OVF	0x0	RW	**Overflow Interrupt Flag**
	This bit is set when counter overflows			

16.5.11 SYSRTC_GRP0_IEN - Group Interrupt Enables

Offset	Bit Position																													
0x044	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0	0x0	0x0	0x0
Access																													RW	RW	RW	RW
Name																													CAP0	CMP1	CMP0	OVF

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	CAP0 Enable CAP0 interrupt	0x0	RW	**Capture 0 Interrupt Enable**
2	CMP1 Enable CMP1 interrupt	0x0	RW	**Compare 1 Interrupt Enable**
1	CMP0 Enable CMP0 interrupt	0x0	RW	**Compare 0 Interrupt Enable**
0	OVF Enable OVF interrupt	0x0	RW	**Overflow Interrupt Enable**

16.5.12 SYSRTC_GRP0_CTRL - Group Control Register

Offset	Bit Position																															
0x048	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																						0x0		0x0			0x0			0x0	0x0	0x0
Access																						RW		RW			RW			RW	RW	RW
Name																						CAP0EDGE		CMP1CMOA			CMP0CMOA			CAP0EN	CMP1EN	CMP0EN

Bit	Name	Reset	Access	Description
31:11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10:9	CAP0EDGE	0x0	RW	**Capture 0 Edge Select**
	Select edge detection for Capture 0			
	Value	Mode		Description
	0	RISING		Rising edges detected
	1	FALLING		Falling edges detected
	2	BOTH		Both edges detected
8:6	CMP1CMOA	0x0	RW	**Compare 1 Compare Match Output Action**
	Select PRS output action on Compare 1 match			
	Value	Mode		Description
	0	CLEAR		Cleared on the next cycle
	1	SET		Set on the next cycle
	2	PULSE		Set on the next cycle, cleared on the cycle after
	3	TOGGLE		Inverted on the next cycle
	4	CMPIF		Export this channel's CMP IF
5:3	CMP0CMOA	0x0	RW	**Compare 0 Compare Match Output Action**
	Select PRS output action on Compare 0 match			
	Value	Mode		Description
	0	CLEAR		Cleared on the next cycle
	1	SET		Set on the next cycle
	2	PULSE		Set on the next cycle, cleared on the cycle after
	3	TOGGLE		Inverted on the next cycle
	4	CMPIF		Export this channel's CMP IF
2	CAP0EN	0x0	RW	**Capture 0 Enable**
	Set this bit to enable Capture 0			

Bit	Name	Reset	Access	Description
1	CMP1EN	0x0	RW	**Compare 1 Enable**
	Set this bit to enable Compare 1			
0	CMP0EN	0x0	RW	**Compare 0 Enable**
	Set this bit to enable Compare 0			

16.5.13 SYSRTC_GRP0_CMP0VALUE - Compare 0 Value Register

Offset	Bit Position																													
0x04C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	CMP0VALUE																															

Bit	Name	Reset	Access	Description
31:0	CMP0VALUE	0x0	RW	**Compare 0 Value**
	Compare 0 match value			

16.5.14 SYSRTC_GRP0_CMP1VALUE - Compare 1 Value Register

Offset	Bit Position																													
0x050	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	CMP1VALUE																															

Bit	Name	Reset	Access	Description
31:0	CMP1VALUE	0x0	RW	**Compare 1 Value**
	Compare 1 match value			

16.5.15 SYSRTC_GRP0_CAP0VALUE - Capture 0 Value Register

Offset	Bit Position																															
0x054	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	CAP0VALUE																															

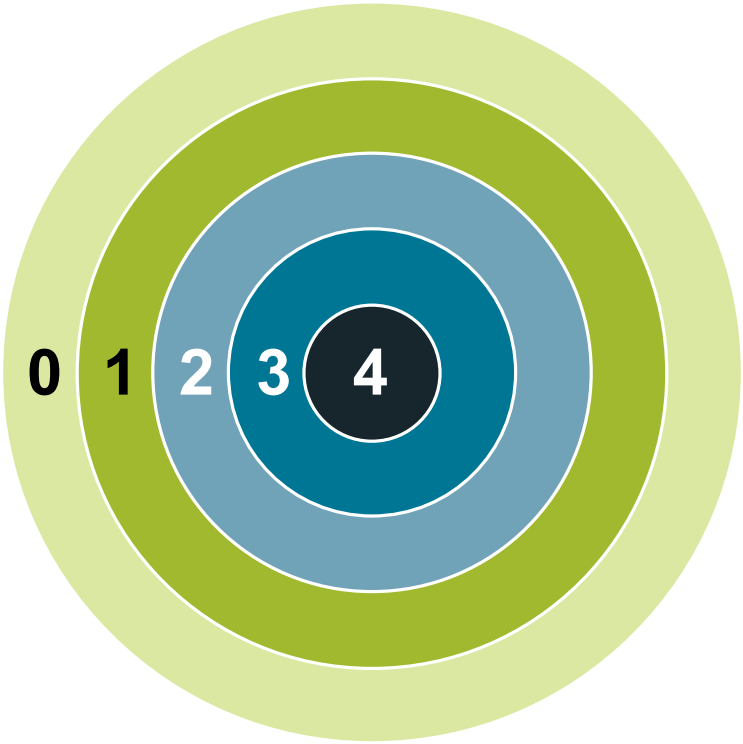
Bit	Name	Reset	Access	Description
31:0	CAP0VALUE	0x0	R	**Capture 0 Value**
	Capture 0 captured value			

16.5.16 SYSRTC_GRP0_SYNCBUSY - Synchronization Busy Register

Offset	Bit Position																															
0x058	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x0	0x0	0x0
Access																														R	R	R
Name																														CMP1VALUE	CMP0VALUE	CTRL

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	CMP1VALUE	0x0	R	**Sync busy for CMP1VALUE register**
	Last writing of CMP1VALUE is synchronizing to LF clock			
1	CMP0VALUE	0x0	R	**Sync busy for CMP0VALUE register**
	Last writing of CMP0VALUE is synchronizing to LF clock			
0	CTRL	0x0	R	**Sync busy for CTRL register**
	Last writing of CTRL is synchronizing to LF clock			

17. BURTC - Back-Up Real Time Counter



Quick Facts

What?

The BURTC is a 32 bit counter which operates on a low frequency oscillator, and is capable of running in all Energy Modes.

Why?

It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode.

The availability of the BURTC in EM4, where most of the device is powered down, makes it ideal for keeping track of time in EM4.

How?

The BURTC provides a very wide range of periods for the interrupts facilitating flexible ultra-low energy operation.

17.1 Introduction

The Back-Up Real Time Counter (BURTC) is a 32-bit counter which operates on a low frequency oscillator, and is capable of running in all Energy Modes. It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The BURTC provides a very wide range of periods for the interrupts facilitating flexible ultra-low energy operation. The availability of the BURTC in EM4, where most of the device is powered down, makes it ideal for keeping track of time in EM4. A single compare channel is available which can be used to trigger an interrupt and/or wake the device up from a low energy mode.

17.2 Features

A low frequency oscillator is used as clock signal and the BURTC with one compare channel which can trigger wake-up, generate PRS signalling, or capture system events. 32-bit resolution and selectable prescaling allows the system to stay in low energy modes for long periods of time and still maintain reliable timekeeping.

- 32-bit Real Time Counter
- 15-bit pre-counter for flexible frequency scaling of main counter
- EM2/3/4 operation and wakeup
- Reset only by External Pin and Power-On Resets
- Interrupt/wake up event after deterministic intervals
- PRS Outputs
- Debug mode
  - Configurable to either run or stop when processor is stopped (break)

17.3 Functional Description

An overview of the BURTC module is shown in Figure 17.1 BURTC Overview on page 515.

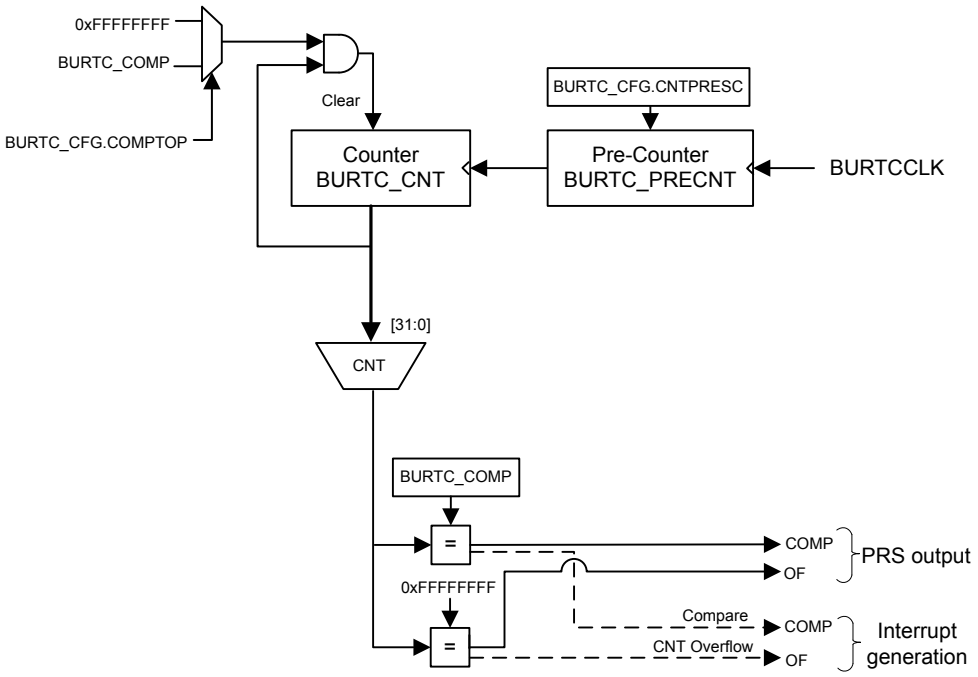


Figure 17.1. BURTC Overview

17.3.1 Clock Selection

The BURTC source clock (BURTCCLK) can be selected to be the LFXO, LFRCO, or ULFRCO by configuring the CMU_EM4GRPACLKCTRL.CLKSEL bitfield. Note that in EM3, only ULFRCO is a valid source clock.

17.3.2 Configuration

To configure and use the BURTC properly, the following programming sequence must be followed:

1. Configure any desired options in the BURTC_CFG register. Note that the BURTC_CFG register can only be written when BURTC_EN.EN = 0 - a bus fault will occur if writing BURTC_CFG register while BURTC_EN.EN = 1.
2. Set BURTC_EN.EN = 1.
3. Set BURTC_CMD.START = 1 to start the BURTC counter.

   Note: All low frequency synchronization registers can only be programmed after EN is set to 1. The BURTC counter will only start to count once START command is issued. For HV Sync registers (e.g., BURTC_CMD), the first bitfield write will occur without issue. However, on subsequent bitfield writes to HV Sync registers, the firmware needs to poll the corresponding bit in BURTC_SYNCBUSY before programming the same bitfield once again.

To stop the BURTC, set BURTC_CMD.STOP = 1

17.3.3 Debug Features and Description

By default, the BURTC is halted when code execution is halted from the debugger. By setting the DEBUGRUN bit in the BURTC_CFG register, the BURTC will continue to run even when the debugger has halted the system.

17.3.4 Counter

The BURTC consists of two counters: the 32-bit main counter, BURTC_CNT, and a 15-bit pre-counter, BURTC_PRECNT. The pre-counter is a free running counter clocked by low frequency clock, used to generate a specific frequency for the main counter. The pre-counter will be counting only when the BURTC_CFG.CNTPRESC value is set greater than 0.

The BURTC peripheral clock is requested by setting the EN bit in BURTC_EN. Then the BURTC counters can be started by setting the command register START in BURTC_CMD. When BURTC_CMD.START has been initiated and BURTC_CFG.CNTPRESC > 0, the pre-counter (BURTC_PRECNT) increments upon each positive clock edge of the BURTCCLK, wrapping around to zero when it overflows.

The main counter can be accessed in BURTC_CNT register, and counts at frequency determined by the CNTPRESC bitfiled in BURTC_CFG. Setting CNTPRESC to 0 gives the maximum resolution, with the main counter clocked at the same frequency as the BURTCCLK. When CNTPRESC > 0, the main counter increments upon each tick given from the pre-counter, allowing the main counter ticks to be power-of-2 divisions of the BURTCCLK.

The Table 17.1 BURTC Resolution vs Overflow, $F_{BURTCCLK}$ = 32768 Hz on page 516 table below shows the BURTC Resolution vs Overflow Time when using a 32768 Hz oscillator as the source clock of BURTC.

Table 17.1. BURTC Resolution vs Overflow, $F_{BURTCCLK}$ = 32768 Hz

BURTC_CFG.CNTPRESC	Main counter period, T_{CNT}	Overflow Time
DIV1	30.5 µs	36.4 hours
DIV2	61 µs	72.8 hours
DIV4	122 µs	145.6 hours
DIV8	244 µs	12 days
DIV16	488 µs	24 days
DIV32	977 µs	48 days
DIV64	1.95 ms	97 days
DIV128	3.91 ms	194 days
DIV256	7.81 ms	388 days
DIV512	15.6 ms	776 days
DIV1024	31.25 ms	4.2 years
DIV2048	62.5 ms	8.5 years
DIV4096	0.125 s	17 years
DIV8192	0.25 s	34 years
DIV16384	0.5 s	68 years
DIV32768	1 s	136 years

By default, the counter will keep counting until it reaches the top value, 0xFFFFFFFF, and then it wrap around and continue counting from zero. If COMPTOP in BURTC_CFG is set, the main counter will wrap to 0 on a Compare value match (i.e., BURTC_CNT = BURTC_COMP). If using the Compare value match, make sure to set COMPTOP prior to or at the same time the BURTC is enabled. Setting COMPTOP after enabling the BURTC will result in a bus fault error.

The counters of the BURTC, BURTC_CNT and BURTC_PRECNT, can at any time be written by software, as long as the registers are not locked using BURTC_LOCKKEY. All BURTC control registers with Sync Type HV uses the 2 FF synchronization scheme.

Note: Writing to the BURTC_PRECNT register may alter the frequency of the ticks for the BURTC_CNT register.

17.3.5 Compare Channel

A single compare channel is available in the BURTC. The compare value is set in BURTC_COMP register. If BURTC_CFG.COMPTOP is set, the main counter will clear to 0 when it matches the value set in BURTC_COMP.

17.3.6 Interrupts

The BURTC has 2 interrupts: one for Overflow and another for for Compare match event. Individual interrupts are enabled by BURTC_IEN register bits, and the respective bits can be used as EM2 wakeup. BURTC_EM4WUEN enables the wakeup enable from EM4 for those events.

17.3.7 Register Lock

To prevent accidental writes to the BURTC registers, the BURTC_LOCK register can be written to any other value than the unlock value. To unlock the register, write the unlock value to BURTC_LOCKKEY. Registers affected by this lock are:

- BURTC_CFG
- BURTC_EN
- BURTC_CMD
- BURTC_PRECNT
- BURTC_CNT
- BURTC_COMP
- BURTC_IEN

17.4 BURTC Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	BURTC_IPVERSION	R	IP Version ID
0x004	BURTC_EN	RW ENABLE	Module Enable Register
0x008	BURTC_CFG	RW CONFIG	Configuration Register
0x00C	BURTC_CMD	W LFSYNC	Command Register
0x010	BURTC_STATUS	RH	Status Register
0x014	BURTC_IF	RWH INTFLAG	Interrupt Flag Register
0x018	BURTC_IEN	RW	Interrupt Enable Register
0x01C	BURTC_PRECNT	RWH LFSYNC	Pre-Counter Value Register
0x020	BURTC_CNT	RWH LFSYNC	Counter Value Register
0x024	BURTC_EM4WUEN	RW	EM4 Wakeup Request Enable Register
0x028	BURTC_SYNCBUSY	RH	Synchronization Busy Register
0x02C	BURTC_LOCK	W	Configuration Lock Register
0x030	BURTC_COMP	RW LFSYNC	Compare Value Register
0x1000	BURTC_IPVERSION_SET	R	IP Version ID
0x1004	BURTC_EN_SET	RW ENABLE	Module Enable Register
0x1008	BURTC_CFG_SET	RW CONFIG	Configuration Register
0x100C	BURTC_CMD_SET	W LFSYNC	Command Register
0x1010	BURTC_STATUS_SET	RH	Status Register
0x1014	BURTC_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x1018	BURTC_IEN_SET	RW	Interrupt Enable Register
0x101C	BURTC_PRECNT_SET	RWH LFSYNC	Pre-Counter Value Register
0x1020	BURTC_CNT_SET	RWH LFSYNC	Counter Value Register
0x1024	BURTC_EM4WUEN_SET	RW	EM4 Wakeup Request Enable Register
0x1028	BURTC_SYNCBUSY_SET	RH	Synchronization Busy Register
0x102C	BURTC_LOCK_SET	W	Configuration Lock Register
0x1030	BURTC_COMP_SET	RW LFSYNC	Compare Value Register
0x2000	BURTC_IPVERSION_CLR	R	IP Version ID
0x2004	BURTC_EN_CLR	RW ENABLE	Module Enable Register
0x2008	BURTC_CFG_CLR	RW CONFIG	Configuration Register
0x200C	BURTC_CMD_CLR	W LFSYNC	Command Register
0x2010	BURTC_STATUS_CLR	RH	Status Register
0x2014	BURTC_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x2018	BURTC_IEN_CLR	RW	Interrupt Enable Register
0x201C	BURTC_PRECNT_CLR	RWH LFSYNC	Pre-Counter Value Register
0x2020	BURTC_CNT_CLR	RWH LFSYNC	Counter Value Register

Offset	Name	Type	Description
0x2024	BURTC_EM4WUEN_CLR	RW	EM4 Wakeup Request Enable Register
0x2028	BURTC_SYNCBUSY_CLR	RH	Synchronization Busy Register
0x202C	BURTC_LOCK_CLR	W	Configuration Lock Register
0x2030	BURTC_COMP_CLR	RW LFSYNC	Compare Value Register
0x3000	BURTC_IPVERSION_TGL	R	IP Version ID
0x3004	BURTC_EN_TGL	RW ENABLE	Module Enable Register
0x3008	BURTC_CFG_TGL	RW CONFIG	Configuration Register
0x300C	BURTC_CMD_TGL	W LFSYNC	Command Register
0x3010	BURTC_STATUS_TGL	RH	Status Register
0x3014	BURTC_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x3018	BURTC_IEN_TGL	RW	Interrupt Enable Register
0x301C	BURTC_PRECNT_TGL	RWH LFSYNC	Pre-Counter Value Register
0x3020	BURTC_CNT_TGL	RWH LFSYNC	Counter Value Register
0x3024	BURTC_EM4WUEN_TGL	RW	EM4 Wakeup Request Enable Register
0x3028	BURTC_SYNCBUSY_TGL	RH	Synchronization Busy Register
0x302C	BURTC_LOCK_TGL	W	Configuration Lock Register
0x3030	BURTC_COMP_TGL	RW LFSYNC	Compare Value Register

17.5 BURTC Register Description

17.5.1 BURTC_IPVERSION - IP Version ID

Offset	Bit Position																													
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x1																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x1	R	**IP Version ID**

17.5.2 BURTC_EN - Module Enable Register

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	RW
Name																															DISABLING	EN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DISABLING	0x0	R	**Disablement busy status** When EN is cleared, DISABLING is set immediately, and cleared when disablement finishes. Disablement resets peripheral cores and not APB registers except hardware updated registers such as INTFLAGs and FIFOs. The CNT and PRECNT count registers are not reset during disablement.
0	EN	0x0	RW	**BURTC Enable** Enable the BURTC to make the peripheral clock available to the module

17.5.3 BURTC_CFG - Configuration Register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0						0x0	0x0
Access																									RW						RW	RW
Name																									CNTPRESC						COMPTOP	DEBUGRUN

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:4	CNTPRESC	0x0	RW	**Counter prescaler value.** Configure counting frequency of the CNT register

Value	Mode	Description
0	DIV1	CLK_CNT = (BURTC LF CLK)/1
1	DIV2	CLK_CNT = (BURTC LF CLK)/2
2	DIV4	CLK_CNT = (BURTC LF CLK)/4
3	DIV8	CLK_CNT = (BURTC LF CLK)/8
4	DIV16	CLK_CNT = (BURTC LF CLK)/16
5	DIV32	CLK_CNT = (BURTC LF CLK)/32
6	DIV64	CLK_CNT = (BURTC LF CLK)/64
7	DIV128	CLK_CNT = (BURTC LF CLK)/128
8	DIV256	CLK_CNT = (BURTC LF CLK)/256
9	DIV512	CLK_CNT = (BURTC LF CLK)/512
10	DIV1024	CLK_CNT = (BURTC LF CLK)/1024
11	DIV2048	CLK_CNT = (BURTC LF CLK)/2048
12	DIV4096	CLK_CNT = (BURTC LF CLK)/4096
13	DIV8192	CLK_CNT = (BURTC LF CLK)/8192
14	DIV16384	CLK_CNT = (BURTC LF CLK)/16384
15	DIV32768	CLK_CNT = (BURTC LF CLK)/32768

3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	COMPTOP	0x0	RW	**Compare Channel is Top Value** When set, the counter is cleared in the clock cycle after a compare match with compare channel

Value	Mode	Description
0	DISABLE	The top value of the BURTC is 4294967295 (0xFFFFFFFF)

Bit	Name	Reset	Access	Description
	1	ENABLE		The top value of the BURTC is given by COMP
0	DEBUGRUN	0x0	RW	**Debug Mode Run Enable**
	Set this bit to enable the BURTC to keep running in debug			

Value	Mode	Description
0	X0	BURTC is frozen in debug mode
1	X1	BURTC is running in debug mode

17.5.4 BURTC_CMD - Command Register

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															W(nB)	W(nB)
Name																															STOP	START

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	STOP	0x0	W(nB)	**Stop BURTC counter**
	Write a 1 to stop the BURTC counter.			
0	START	0x0	W(nB)	**Start BURTC counter**
	Write a 1 to start the BURTC counter.			

17.5.5 BURTC_STATUS - Status Register

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	R
Name																															LOCK	RUNNING

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	LOCK	0x0	R	**Configuration Lock Status**
	Indicates the current status of BURTC Lock			

Value	Mode	Description
0	UNLOCKED	All BURTC lockable registers are unlocked.
1	LOCKED	All BURTC lockable registers are locked.

0	RUNNING	0x0	R	**BURTC running status**
	Indicates the current status of BURTC running			

17.5.6 BURTC_IF - Interrupt Flag Register

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															RW	RW
Name																															COMP	OF

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	COMP	0x0	RW	**Compare Match Interrupt Flag**
	Set on a compare match between CNT and COMP.			
0	OF	0x0	RW	**Overflow Interrupt Flag**
	Set on a CNT value overflow.			

17.5.7 BURTC_IEN - Interrupt Enable Register

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															RW	RW
Name																															COMP	OF

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	COMP	0x0	RW	**Compare Match Interrupt Flag**
	Set to enable the COMPIF Interrupt			
0	OF	0x0	RW	**Overflow Interrupt Flag**
	Set to enable the OFIF Interrupt			

17.5.8 BURTC_PRECNT - Pre-Counter Value Register

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																		0x0														
Access																		RW														
Name																		PRECNT														

Bit	Name	Reset	Access	Description
31:15	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
14:0	PRECNT	0x0	RW	**Pre-Counter Value**
	Gives access to the Pre-counter value of the BURTC.			

17.5.9 BURTC_CNT - Counter Value Register

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	CNT																															

Bit	Name	Reset	Access	Description
31:0	CNT	0x0	RW	**Counter Value**
	Gives access to the counter value of the BURTC.			

17.5.10 BURTC_EM4WUEN - EM4 Wakeup Request Enable Register

Offset	Bit Position																													
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															RW	RW
Name																															COMPEM4WUEN	OFEM4WUEN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	COMPEM4WUEN	0x0	RW	**Compare Match EM4 Wakeup Enable**
	Compare Match EM4 wakeup requests. No Synchronization done into peripheral clock domain.			
0	OFEM4WUEN	0x0	RW	**Overflow EM4 Wakeup Enable**
	Overflow EM4 Wakeup request. No Synchronization done into peripheral clock domain.			

17.5.11 BURTC_SYNCBUSY - Synchronization Busy Register

Offset	Bit Position																													
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												R	R	R	R	R
Name																												COMP	CNT	PRECNT	STOP	START

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	COMP	0x0	R	**Sync busy for COMP**
	Last writing of COMP is synchronizing to LF clock			
3	CNT	0x0	R	**Sync busy for CNT**
	Last writing of CNT is synchronizing to LF clock			
2	PRECNT	0x0	R	**Sync busy for PRECNT**
	Last writing of PRECNT is synchronizing to LF clock			
1	STOP	0x0	R	**Sync busy for STOP**
	Last writing of STOP is synchronizing to LF clock			
0	START	0x0	R	**Sync busy for START**
	Last writing of START is synchronizing to LF clock			

17.5.12 BURTC_LOCK - Configuration Lock Register

Offset	Bit Position																													
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																								0xAEE8								
Access																								W								
Name																								LOCKKEY								

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LOCKKEY	0xAEE8	W	**Configuration Lock Key**

Write any other value than the unlock code to lock BURTC_EN, BURTC_CFG, BURTC_CMD, BURTC_PRECNT, BURTC_CNT and BURTC_COMP registers from editing. Write the unlock code to unlock.

Value	Mode	Description
44776	UNLOCK	Write to unlock all BURTC lockable registers

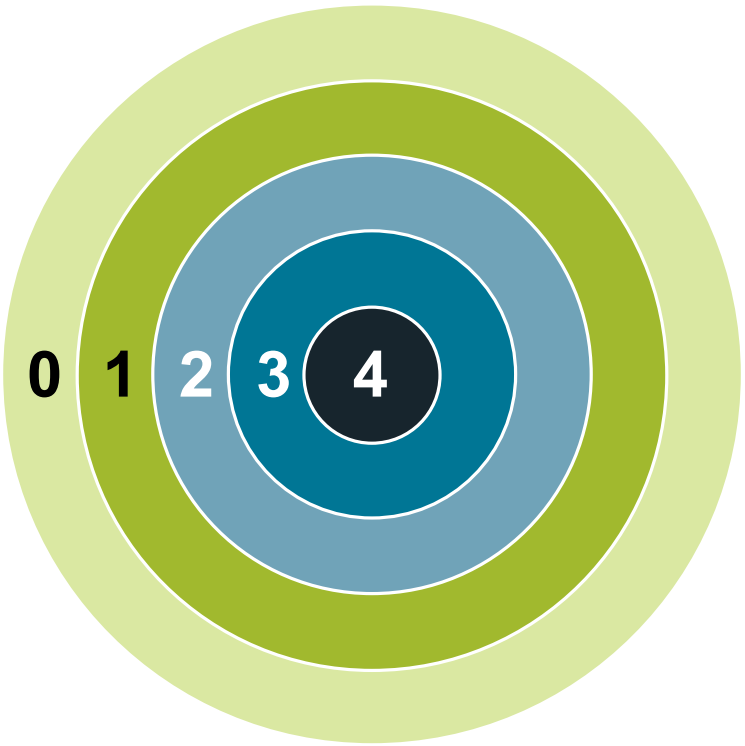
17.5.13 BURTC_COMP - Compare Value Register

Offset	Bit Position																													
0x030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																0x0																
Access																RW																
Name																COMP																

Bit	Name	Reset	Access	Description
31:0	COMP	0x0	RW	**Compare Value**

A compare match event occurs when CNT is equal to this value. This event sets the COMP interrupt flag. It is also available as a PRS signal.

18. BURAM - Backup RAM



Quick Facts

What?

The BURAM is a dedicated 128-byte low-power RAM that is retained in EM4.

Why?

Most of the system, including the RAM, is powered off at EM4 entry to minimize current draw. The purpose of the BURAM is to retain critical data for use when the system wakes up.

How?

Because it is separate from the main system RAM, the BURAM has a dedicated power supply that is not shutdown when the system enters EM4.

18.1 Introduction

The Back-Up RAM (BURAM) is a dedicated 128-byte RAM that remains powered when the system enters EM4. Upon exit from EM4, the data retained in the BURAM can be accessed by the application software.

18.2 Functional Description

The BURAM consists of 32 x 32-bit registers, which are retained in all energy modes, including EM4. Each word in the BURAM is accessible through the corresponding 32 RETx_REG register. Note that each RETx_REG register has an undefined state out of reset.

18.3 BURAM Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	BURAM_RETx_REG	RW	Retention Register
0x1000	BURAM_RETx_REG_SET	RW	Retention Register
0x2000	BURAM_RETx_REG_CLR	RW	Retention Register
0x3000	BURAM_RETx_REG_TGL	RW	Retention Register

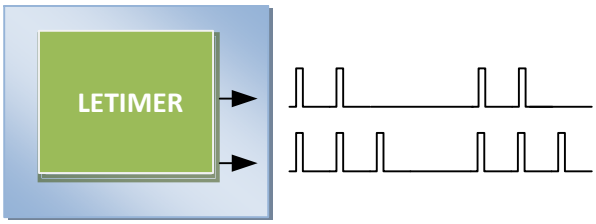
18.4 BURAM Register Description

18.4.1 BURAM_RETx_REG - Retention Register

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	RETREG																															

Bit	Name	Reset	Access	Description
31:0	RETREG	0x0	RW	**Latch based Retention register** The RETREG registers are undefined out of reset. Any written RETREG values will be retained through any event other than a brownout or power-on reset.

19. LETIMER - Low Energy Timer



Quick Facts

What?

The LETIMER is a down-counter that can keep track of time and output configurable waveforms. Running on a 32768 Hz clock, the LETIMER is available in EM0 Active, EM1 Sleep, EM2 DeepSleep, and EM3 Stop.

Why?

The LETIMER can be used to provide repeatable waveforms to external components while remaining in EM2 DeepSleep. It is well suited for applications such as metering systems or to provide more compare values than available in the SYSRTC.

How?

With buffered repeat and top value registers, the LETIMER can provide glitch-free waveforms at frequencies up to 16 kHz. It can be coupled with SYSRTC using PRS, allowing advanced time-keeping and wake-up functions in EM2 DeepSleep and EM3 Stop

19.1 Introduction

The LETIMER is a down-counter that can keep track of time and output configurable waveforms with minimal software intervention. Running on a Low Frequency clock, the LETIMER is available in Energy Mode0, Energy Mode 1 and optionally available in Energy Mode 2 and Energy Mode 3. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. It is well suited for applications such as metering systems or to provide more compare values than available in the SYSRTC. With buffered repeat and top value registers, the LETIMER can provide glitch-free waveforms at frequencies up to 16 kHz. It can be coupled with other peripherals using PRS, allowing advanced time-keeping and wake-up functions

19.2 Features

High-level features

- 24-bit Down counter
- 8-bit prescalar
- 2 Compare match registers
- TOP register can be Timer top value
- TOP register can be double buffered using TOPBUFF register
- Double buffered 8-bit Repeat Register
- Timer Start/Stop/Clear trigger can be from PRS or Software
- Configurable 2 Output pins - Toggle/Pulse/PWM
- Interrupt - Compare match/Timer underflow/Repeat done
- Optionally runs during debug
- 2 output pins can optionally be configured to provide different waveforms on timer underflow:
  - Toggle output pin
  - Pulse output with width of One Prescaled clock period
  - PWM
- 2 PRS Output

19.3 Functional Description

An overview of the LETIMER module is shown in Figure 19.1 LETIMER Overview on page 531. The LETIMER is a 24-bit down-counter with two compare registers, LETIMERn_COMP0 and LETIMERn_COMP1. The LETIMERn_TOP register can optionally act as a top value for the counter. The repeat counter LETIMERn_REP0 allows the timer to count a specified number of times before it stops. Both the LETIMERn_TOP and LETIMERn_REP0 registers can be double buffered by the LETIMERn_TOPBUFF and LETIMERn_REP1 registers to allow continuous operation. The timer can generate a single pin output, or two linked outputs.

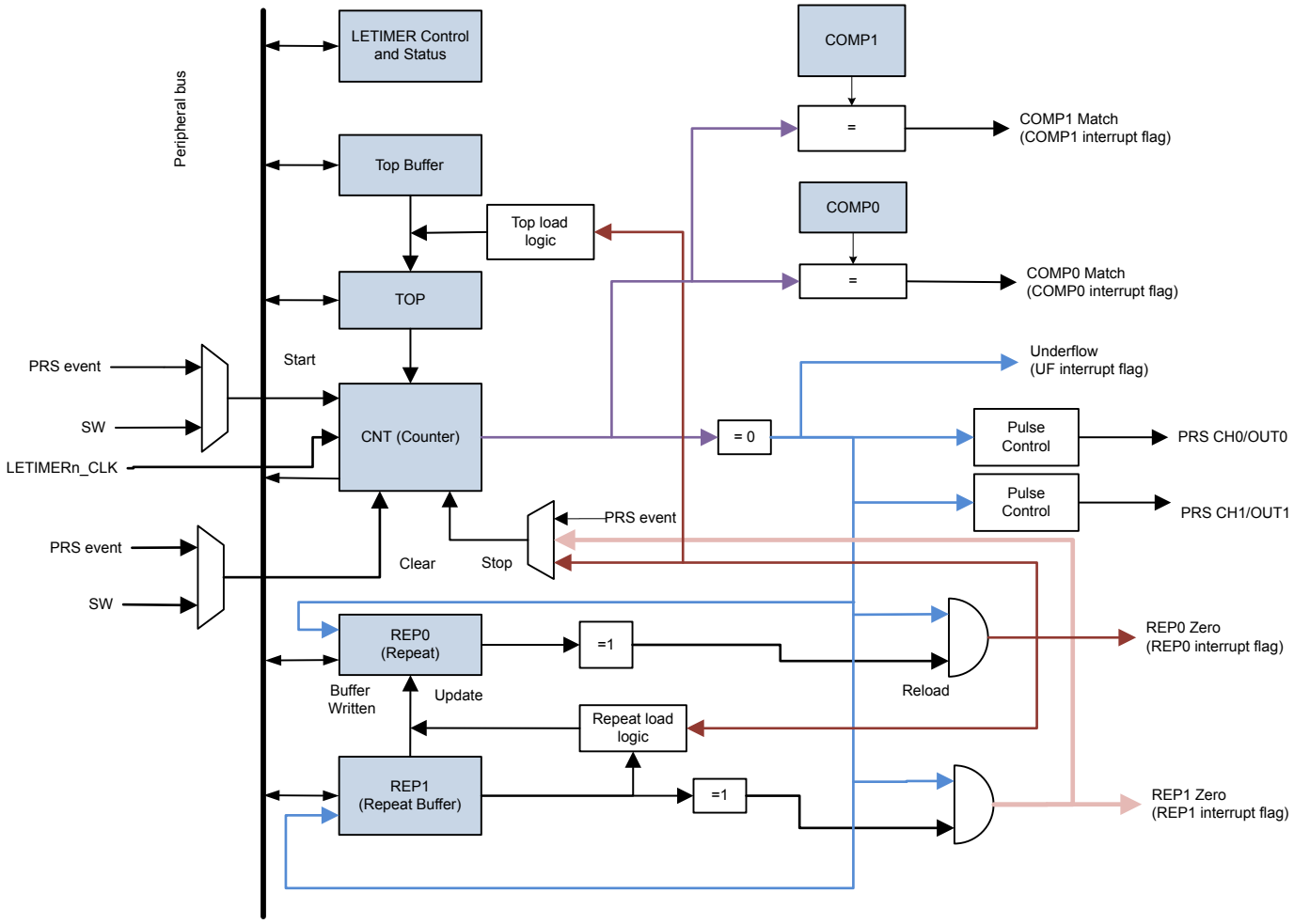


Figure 19.1. LETIMER Overview

19.3.1 Internal Overview

Timer

The timer value can be read using the LETIMERn_CNT register. The value can be written, and it can also be cleared by setting the CLEAR command bit in LETIMERn_CMD. If the CLEAR and START commands are issued at the same time, the timer will be cleared, then start counting at the top value.

Compare Registers

- The LETIMER has two compare match registers, LETIMERn_COMP0 and LETIMERn_COMP1. Each of these compare registers are capable of generating an interrupt when the counter value LETIMERn_CNT is equal to their value. When LETIMERn_CNT is equal to the value of LETIMERn_COMP0, the interrupt flag COMP0 in LETIMERn_IF is set, and when LETIMERn_CNT is equal to the value of LETIMERn_COMP1, the interrupt flag COMP1 in LETIMERn_IF is set.
- **Top Value**

  If CNTTOPEN in LETIMERn_CTRL is set, the value of LETIMERn_TOP acts as the top value of the timer, and LETIMERn_TOP is loaded into LETIMERn_CNT on timer underflow. If CNTTOPEN is cleared to 0, the timer wraps around to 0xFFFFFF. The underflow interrupt flag UF in LETIMERn_IF is set when the timer reaches zero.
- **Repeat Modes**

  By default, the timer wraps around to the top value or 0xFFFFFF on each underflow, and continues counting. The repeat counters can be used to get more control of the operation of the timer, including defining the number of times the counter should wrap around. Four different repeat modes are available, see Table 19.1 LETIMER Repeat Modes on page 532.

Table 19.1. LETIMER Repeat Modes

REPMODE	Mode	Description
0b00	Free-running	The timer runs until it is stopped.
0b01	One-shot	The timer runs as long as LETIMERn_REP0 != 0. LETIMERn_REP0 is decremented at each timer underflow.
0b10	Buffered	The timer runs as long as LETIMERn_REP0 != 0. LETIMERn_REP0 is decremented on each timer underflow. If LETIMERn_REP1 has been written with Non zero value, then it is loaded into LETIMERn_REP0 when LETIMERn_REP0 is about to be decremented to 0 and Timer countinue counting with new LETIMERn_REP0.
0b11	Double	The timer runs as long as LETIMERn_REP0 != 0 or LETIMERn_REP1 != 0. Both LETIMERn_REP0 and LETIMERn_REP1 are decremented at each timer underflow.

  The interrupt flags REP0 and REP1 in LETIMERn_IF are set whenever LETIMERn_REP0 or LETIMERn_REP1 are decremented to 0 respectively. REP0 is also set when the value of LETIMERn_REP1 is loaded into LETIMERn_REP0 in buffered mode.

  Write operations to LETIMERn_REP0 have priority over buffer loads from LETIMERn_REP1.
- **Buffered Top Value**

  In Buffered Mode, If BUFTOP in LETIMERn_CTRL is set, the value of LETIMERn_TOP is buffered by LETIMERn_TOPBUFF. In this mode, the value of LETIMERn_TOPBUFF is loaded into LETIMERn_TOP every time LETIMERn_REP0 is about to decrement to 0. This can be used to generate continually changing output waveforms.

  Write operations to LETIMERn_TOP have priority over buffer loads from LETIMERn__TOPBUFF.

19.3.2 Free Running Mode

In free-running mode, the LETIMER acts as a regular timer and the repeat operation is disabled. When started, the timer runs until it is stopped using the STOP command bit in LETIMERn_CMD/PRS. A state machine for this mode is shown in Figure 19.2 LETIMER State Machine for Free-running Mode on page 533 .

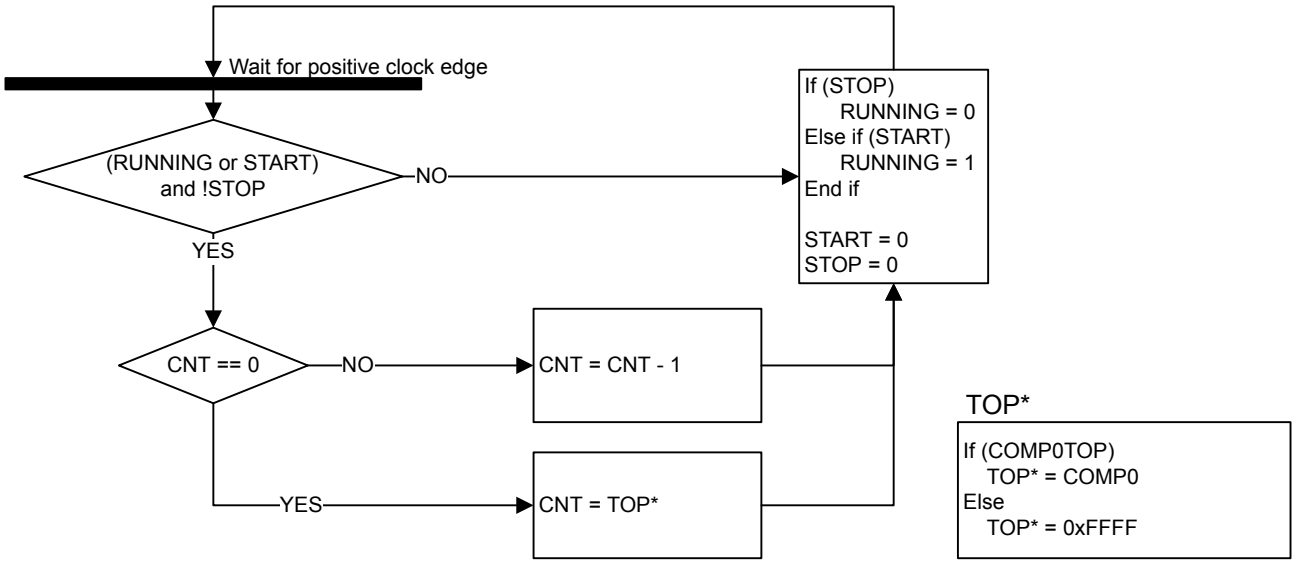


Figure 19.2. LETIMER State Machine for Free-running Mode

Note that the CLEAR command bit in LETIMERn_CMD always has priority over Decrement and Load TOP to LETIMERn_CNT. When the clear command is used, LETIMERn_CNT is set to 0 and an underflow event will not be generated when LETIMERn_CNT wraps around to the top value or 0xFFFFFF. Since no underflow event is generated, no output action is performed. LETIMERn_REP0, LETIMERn_REP1, LETIMERn_COMP0 and LETIMERn_COMP1 are also left untouched.

19.3.3 One-shot Mode

The one-shot repeat mode is the most basic repeat mode. In this mode, the repeat register LETIMERn_REP0 is decremented every time the timer underflows, and the timer stops when LETIMERn_REP0 goes from 1 to 0. In this mode, the timer counts down LETIMERn_REP0 times, i.e. the timer underflows LETIMERn_REP0 times.

Note: Note that write operations to LETIMERn_REP0 have priority over the timer decrement event. If LETIMERn_REP0 is assigned a new value in the same cycle as a timer decrement event occurs, the timer decrement will not occur and the new value is assigned.

LETIMERn_REP0 can be written while the timer is running to allow the timer to run for longer periods at a time without stopping. Write to LETIMERn_REP0 should be done after checking SYNC busy statusFigure 19.3 LETIMER One-shot Repeat State Machine on page 534 .

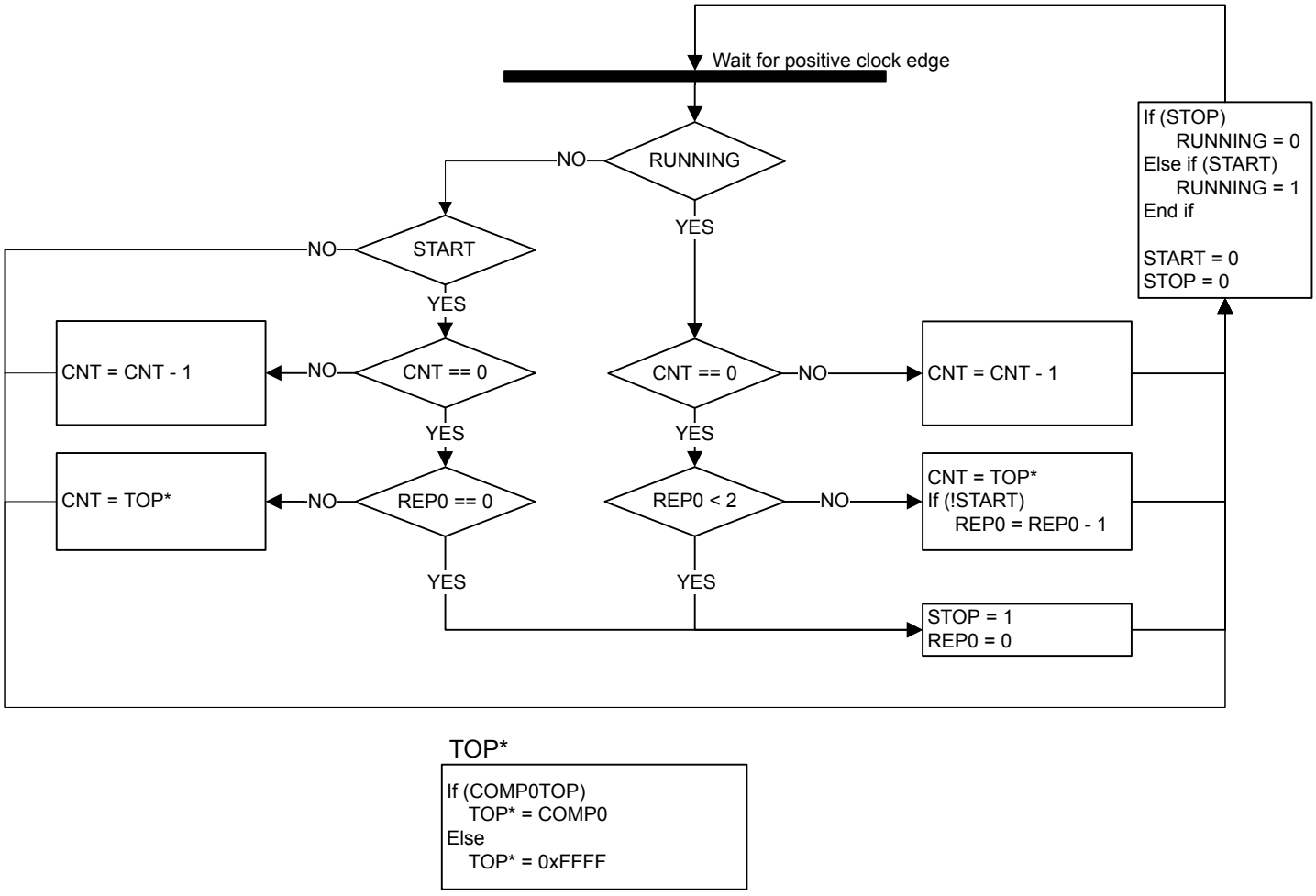


Figure 19.3. LETIMER One-shot Repeat State Machine

19.3.4 Buffered Mode

The Buffered repeat mode allows buffered timer operation. When started, the timer runs LETIMERn_REP0 number of times. If LETIMERn_REP1 has been written since the last time it was used and if it is nonzero, LETIMERn_REP1 is then loaded into LETIMERn_REP0, and counting continues the new number of times. The timer keeps going as long as LETIMERn_REP1 is updated with a nonzero value before LETIMERn_REP0 is finished counting down. The timer top value (LETIMERn_TOP) may also optionally be buffered using Top buff value (LETIMERn_TOPBUFF) by setting BUFTOP in LETIMERn_CTRL.

If the timer is started when both LETIMERn_CNT and LETIMERn_REP0 are zero but LETIMERn_REP1 is non-zero, LETIMERn_REP1 is loaded into LETIMERn_REP0, and the counter counts the loaded number of times.

Used in conjunction with a buffered top value, both the top and repeat values of the timer may be buffered, and the timer can for instance be set to run 4 times with period 7 (top value 6), 6 times with period 200, then 3 times with period 50.

A state machine for the buffered repeat mode is shown in Figure 19.4 LETIMER Buffered Repeat State Machine on page 535. $REP1_{USED}$ shown in the state machine is an internal variable that keeps track of whether the value in LETIMERn_REP1 has been loaded into LETIMERn_REP0 or not. The purpose of this is that a value written to LETIMERn_REP1 should only be counted once. $REP1_{USED}$ is cleared whenever LETIMERn_REP1 is used.

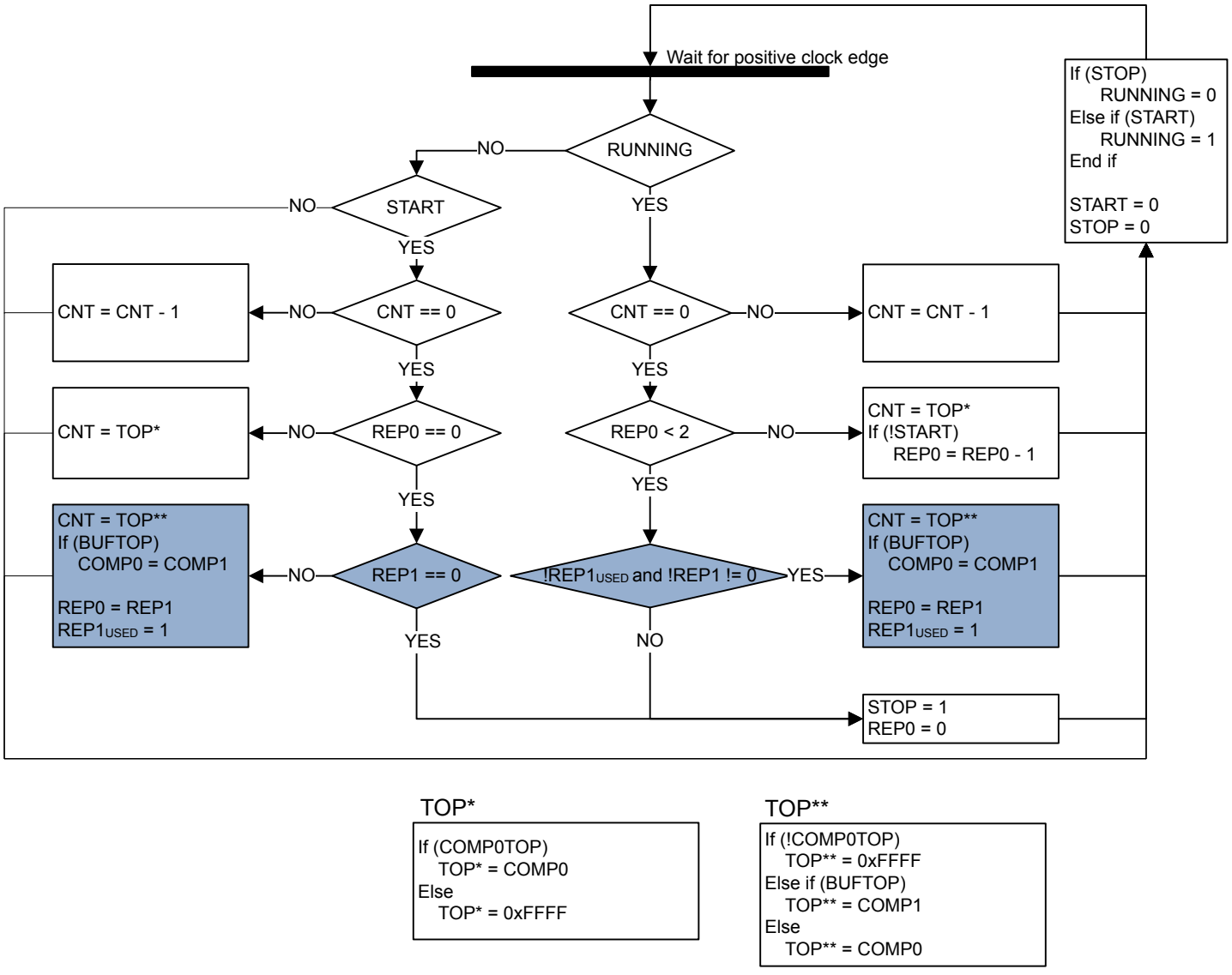


Figure 19.4. LETIMER Buffered Repeat State Machine

19.3.5 Double Mode

The Double repeat mode works much like the one-shot repeat mode. The difference is that, where the one-shot mode counts as long as LETIMERn_REP0 is larger than 0, the double mode counts as long as either LETIMERn_REP0 or LETIMERn_REP1 is larger than 0. As an example, say LETIMERn_REP0 is 3 and LETIMERn_REP1 is 10 when the timer is started. If no further interaction is done with the timer, LETIMERn_REP0 will now be decremented 3 times, and LETIMERn_REP1 will be decremented 10 times. The timer counts a total of 10 times, and LETIMERn_REP0 is 0 after the first three timer underflows and stays at 0. LETIMERn_REP0 and LETIMERn_REP1 can be written at any time. After a write to either of these, the timer is guaranteed to underflow at least the written number of times if the timer is running. Use the Double repeat mode to generate output on both the LETIMER outputs at the same time. The state machine for this repeat mode can be seen in Figure 19.5 LETIMER Double Repeat State Machine on page 536.

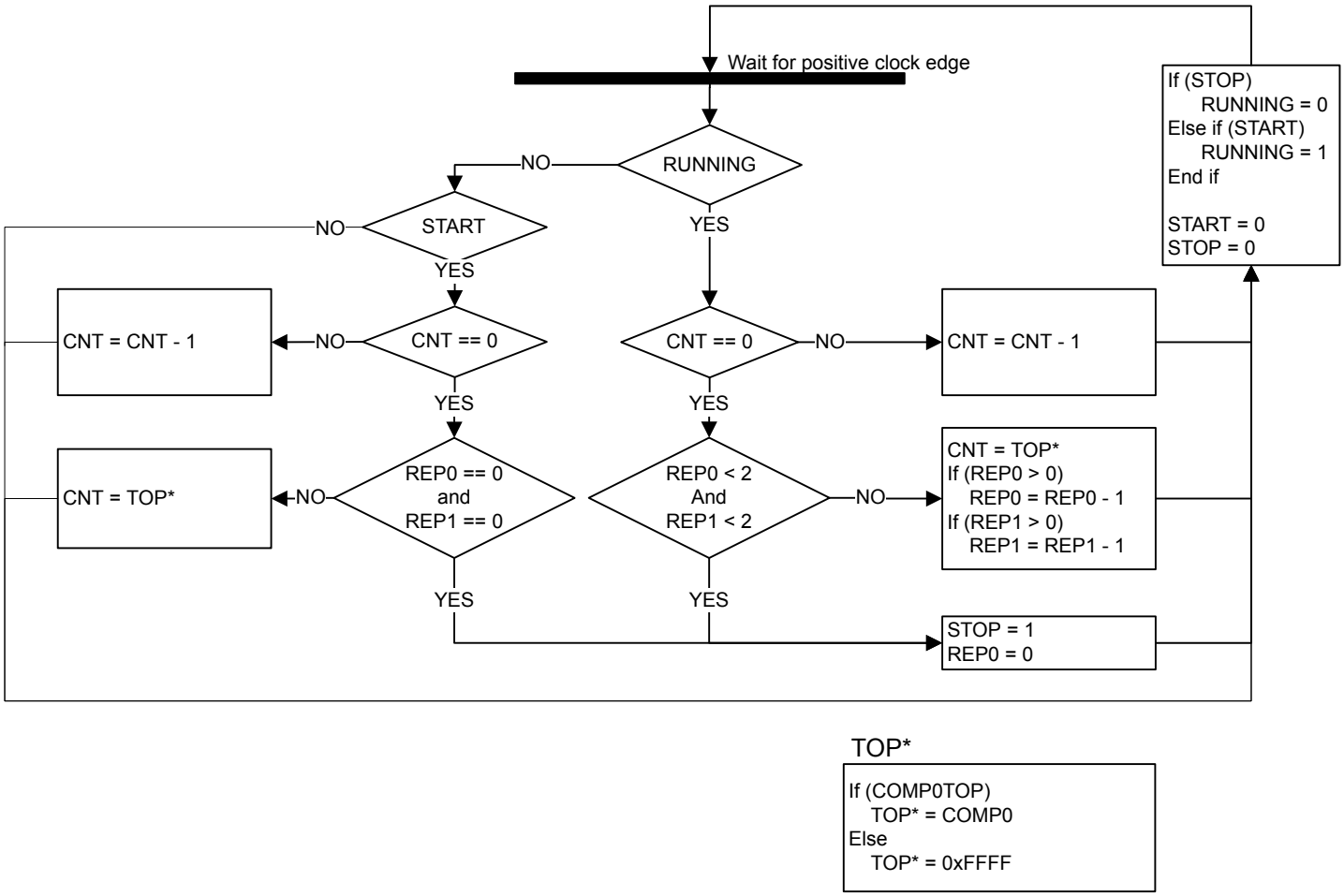


Figure 19.5. LETIMER Double Repeat State Machine

19.4 Clock Frequency

The LETIMER clock source is derived from EM23GRPACLK, which is selected in the Clock Management Unit (CMU), and is typically configured to have a frequency of 32 kHz in EM0/1/2 and 1 kHz in EM3. The LETIMER clock prescaler is defined by LETIMERn_CTRL->CNTPRESC.

The LETIMER Prescaled clock frequency is given by Figure 19.6 LETIMER Clock Frequency on page 537.

EM0/1/2 - Clocked by LFRCO

$$f_{LETIMERn\_CLK} = 32768/2^{CNTPRESC}$$

EM3 - Clocked by ULFRCO

$$f_{LETIMERn\_CLK} = 1024/2^{CNTPRESC}$$

Figure 19.6. LETIMER Clock Frequency

The exponent CNTPRESC is a 4 bit value in the LETIMERn_CTRL->CNTPRESC register bits.

To use this module, the LETIMERn_CLK must be enabled by writing 1 to LETIMERn_EN->EN.

19.5 PRS Input Triggers

The LETIMER can be configured to start, stop, and/or clear based on PRS inputs. The diagram showing the functions of the PRS input triggers is shown in Figure 19.7 LETIMER PRS input triggers. on page 538.

There are 3 PRS inputs to the LETIMER, allowing the LETIMER to be started, stopped, or cleared based on the PRS inputs. The PRSSTARTMODE, PRSSTOPMODE, and PRSCLEARMODE bitfields in LETIMERn->PRSMODE select which edge or edge(s) will trigger the start, stop, and/or clear action.

The PRS channel inputs can be configured in the PRS_CONSUMER_LETIMERn_CLEAR, PRS_CONSUMER_LETIMERn_START, and PRS_CONSUMER_LETIMERn_STOP registers in the PRS module.

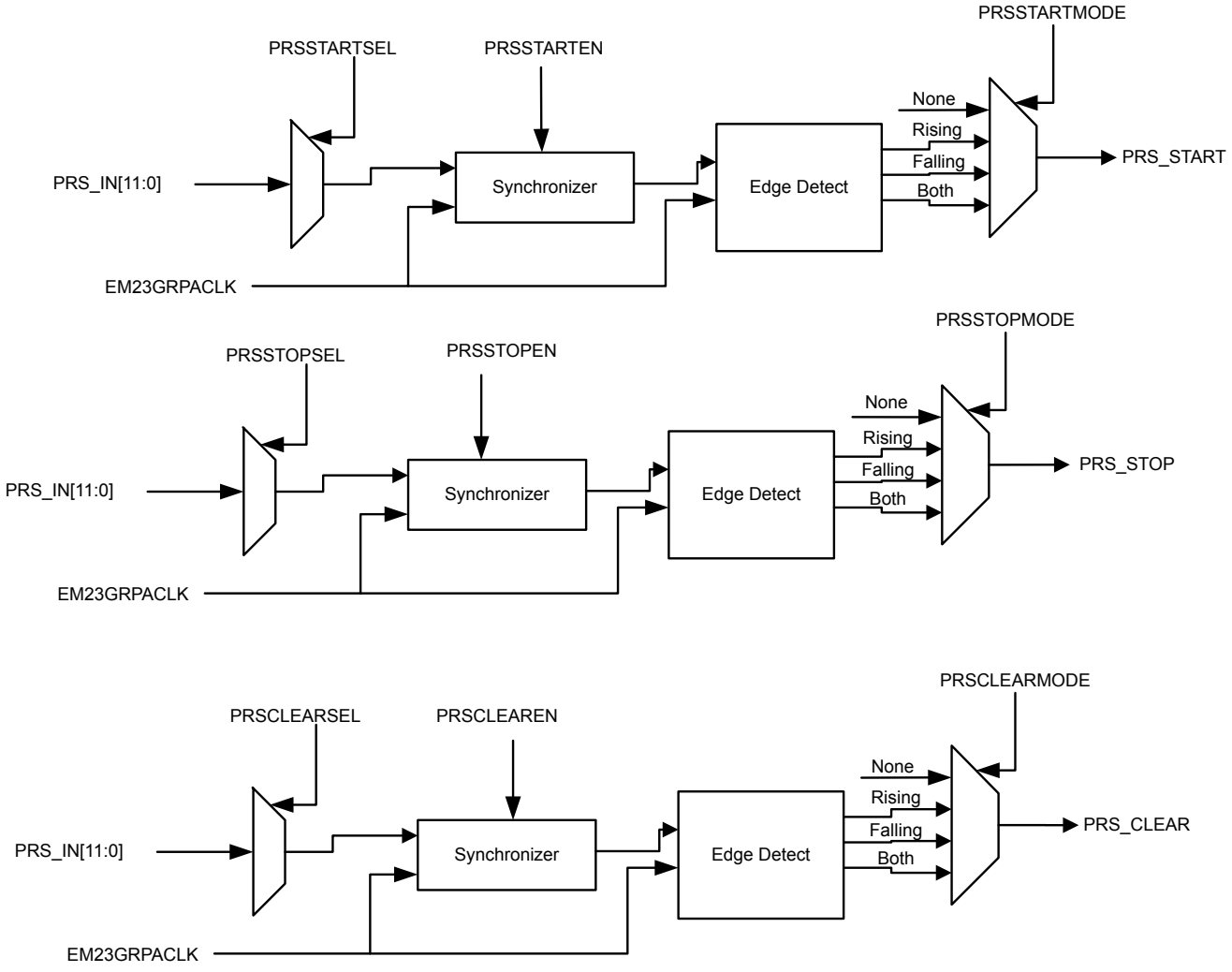


Figure 19.7. LETIMER PRS input triggers.

19.6 Debug

If DEBUGRUN in LETIMERn_CTRL is cleared, the LETIMER automatically stops counting when the CPU is halted during a debug session, and resumes operation when the CPU continues. Because of synchronization, the LETIMER is halted two clock cycles after the CPU is halted, and continues running two clock cycles after the CPU continues. RUNNING in LETIMERn_STATUS is not cleared when the LETIMER stops because of a debug-session.

Set DEBUGRUN in LETIMERn_CTRL to allow the LETIMER to continue counting even when the CPU is halted in debug mode.

19.7 Output Action

For each of the Outputs, an output action can be set.

The output actions can be set by configuring UFOA0 and UFOA1 in LETIMERn_CTRL. UFOA0 defines the action on output 0, while UFOA1 defines the action on output 1. The possible actions are defined in Table 19.2 LETIMER Underflow Output Actions on page 539.

Table 19.2. LETIMER Underflow Output Actions

UF0A0/UF0A1	Mode	Description
0b00	Idle	The output is held at its idle value
0b01	Toggle	The output is toggled on LETIMERn_CNT underflow
0b10	Pulse	The output is held active for one LF clock cycle on LETIMERn_CNT underflow It then returns to its idle value
0b11	PWM	The output is set idle on LETIMERn_CNT underflow and active on compare match with LETIMERn_COMP0/1.

Note: For the Pulse output Disabling LETIMER, Clearing Output while pulse output is generated can affect the pulse width.

Note: For Double mode, OUT0/1 generation is enabled when LETIMERn_REP0/1 != 0 respectively.

The polarity of the outputs can be set individually by configuring OPOL0 and OPOL1 in LETIMERn_CTRL. When these are cleared, their respective outputs have a low idle value and a high active value. When they are set, the idle value is high, and the active value is low. It is recommended to Clear outputs after changing polarity to makesure outputs take their default value.

When using the toggle action, the outputs can be driven to their idle values by setting their respective CTO0/CTO1 command bits in LETIMERn_CTRL. This can be used to put the output in a well-defined state before beginning to generate toggle output, which may be important in some applications. The command bit can also be used while the timer is running.

19.8 PRS Output

The LETIMER outputs can be routed out onto the PRS system. LETn_O0 can be routed to PRS channel 0, and LETn_O1 can be routed to PRS channel 1. Enabling the PRS connection can be done by setting SOURCESEL to LETIMERx and SIGSEL to LETIMERxCHn in PRS_CHx_CTRL.

19.9 Interrupts

The interrupts generated by the LETIMER are combined into one interrupt vector. If the interrupt for the LETIMER is enabled, an interrupt will be made if one or more of the interrupt flags in LETIMERn_IF and their corresponding bits in LETIMER_IEN are set.

19.10 Using the LETIMER in EM3

The LETIMER can be enabled all the way down to EM3 by using the ULFRCO as clock source. This is done by setting CMU_EM23GRPACLKCTRL.CLKSEL to ULFRCO before enabling the LETIMER block. This will make the SYSRTC use the internal 1 kHz ultra low frequency RC oscillator (ULFRCO), consuming very little energy. Please note that the ULFRCO is not accurate over temperature and voltage, and it should be verified that the ULFRCO fulfills the timekeeping needs of the application before using this in the design.

19.11 Register Access

This module is a Low Energy Peripheral, and supports immediate synchronization. For description regarding immediate synchronization, refer to 4.2.4.4 Peripheral Access Performance.

Since this module is a Low Energy Peripheral, and runs off a clock which is asynchronous to the APB register clock, special considerations must be taken when accessing registers.

19.12 Programmer's Model

Important Note : Before writing any LFSYNC register, the module must be enabled (LETIMER_EN->EN) and the LETIMER_SYNCBUSY register should be polled to ensure the SYNC busy of that particular register field is not high.

Write LETIMER Configuration into LETIMER_CTRL Register

Enable clock to LETIMER module by setting LETIMER_EN->EN = 1

If used, write compare values into LETIMER_COMP0 and LETIMER_COMP1

If used, write repeat values into LETIMER_REP0 and LETIMER_REP1

If used, write LETIMER_TOP and LETIMER_TOPBUFF

If PRS is used as a trigger, configure LETIMER_PRSMODE accordingly

Enable Interrupts in LETIMER_IEN

Write LETIMER_CMD register to START Timer

19.12.1 Free Running Mode

LETIMER operation in Free running Mode with different output modes are shown in Figure 19.8 LETIMER - Free Running Mode Waveform on page 540. In this example, REPMODE in LETIMERn_CTRL is set to FREE, CNTTOPEN also in LETIMERn_CTRL has been set and LETIMERn_TOP has been written to 3. As seen in the figure, LETIMERn_TOP now decides the length of the signal periods. For the toggle mode, the period of the output signal is 2(LETIMERn_TOP + 1), and for the pulse modes, the periods of the output signals are LETIMERn_TOP+1. Note that the pulse outputs are delayed by one period relative to the toggle output. The pulses come at the end of their periods.

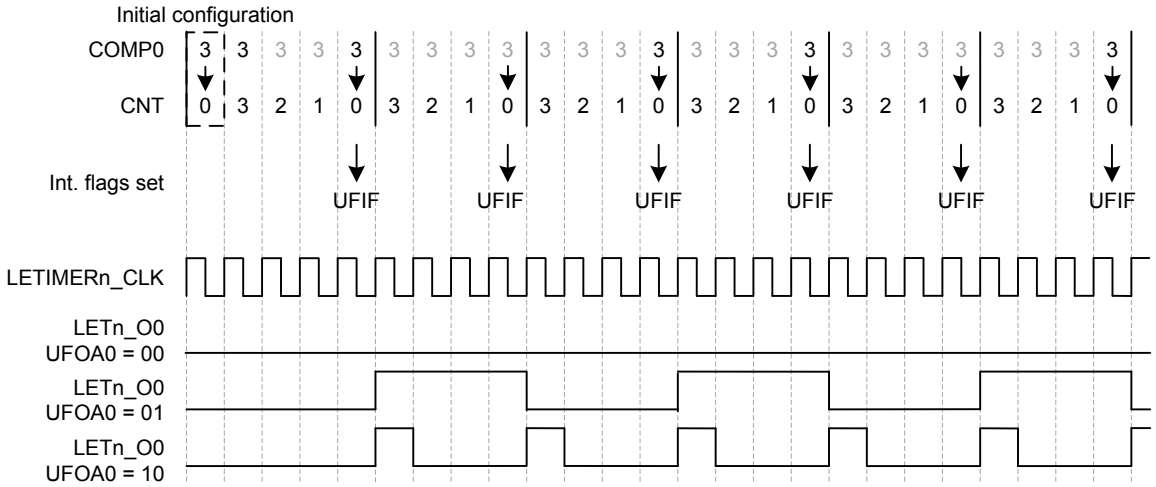


Figure 19.8. LETIMER - Free Running Mode Waveform

19.12.2 One Shot Mode

LETIMER operation in ONESHOT Mode with different output modes are shown in Figure 19.9 LETIMER - One Shot Mode Waveform on page 541. In this example, REPMODE in LETIMERn_CTRL is set to ONESHOT, CNTTOPEN also in LETIMERn_CTRL has been set and LETIMERn_TOP has been written to 3 and LETIMERn_REP0 has been written to 3. The resulting behavior is pretty similar to that shown in Figure 6, but in this case, the timer stops after counting to zero LETIMERn_REP0 times. By using LETIMERn_REP0 the user has full control of the number of pulses/toggles generated on the output.

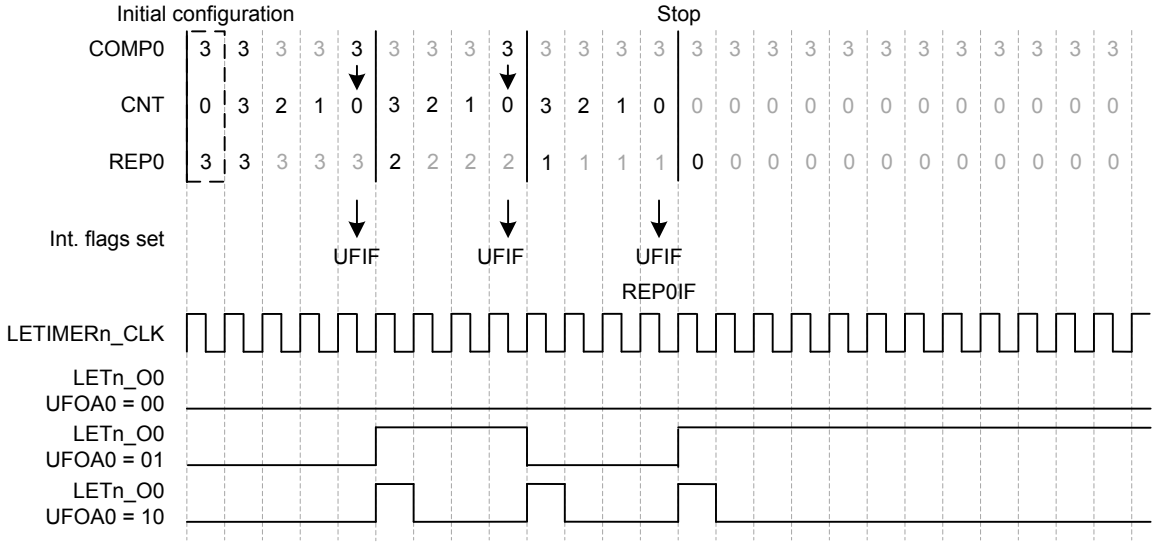


Figure 19.9. LETIMER - One Shot Mode Waveform

19.12.3 DOUBLE Mode

LETIMER operation in DOUBLE Mode with both outputs is shown in Figure 19.10 LETIMER - Double Mode Waveform on page 541. UFOA0 and UFOA1 in LETIMERn_CTRL are configured for pulse output and the outputs are configured for low idle polarity. As seen in the figure, the number written to the repeat registers determine the number of pulses generated on each of the outputs.

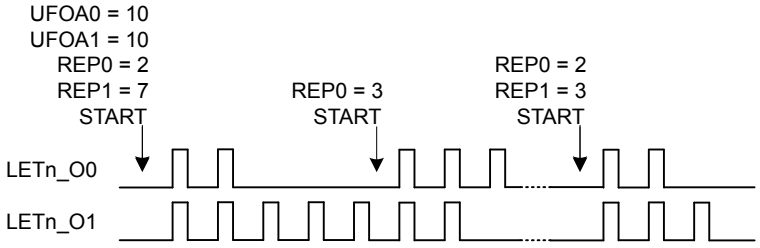


Figure 19.10. LETIMER - Double Mode Waveform

19.12.4 BUFFERED Mode

In BUFFERED Mode LETIMERn_TOPBUFF and LETIMERn_REP1 registers are used as Buffers for LETIMERn_TOP and LETIMERn_REP0 respectiverly. If both LETIMERn_TOP and LETIMERn_REP0 are 0 in buffered mode, and CNTTOPEN and BUFTOP in LETIMERn_CTRL are set, the values of LETIMERn_TOPBUFF and LETIMERn_REP1 are loaded into LETIMERn_TOP and LETIMERn_REP0 respectively when the timer is started. If no additional writes to LETIMERn_REP1 are done before the timer stops, LETIMERn_REP1 determines the number of pulses/toggles generated on the output, and LETIMERn_TOPBUFF determines the period lengths.

As the SYSRTC can also be used via PRS to start the LETIMER, the SYSRTC and LETIMER can thus be combined to generate specific pulse-trains at given intervals. Software can update LETIMERn_TOPBUFF and LETIMERn_REP1 to change the number of pulses and pulse-period in each train, but if changes are not required, software does not have to update the registers between each pulse train.

For the example in Figure 19.11 LETIMER - Buffered Mode Waveform on page 542, the initial values cause the LETIMER to generate two pulses with 3 cycle periods, or a single pulse 3 cycles wide every time the LETIMER is started. After the output has been generated, the LETIMER stops, and is ready to be triggered again.

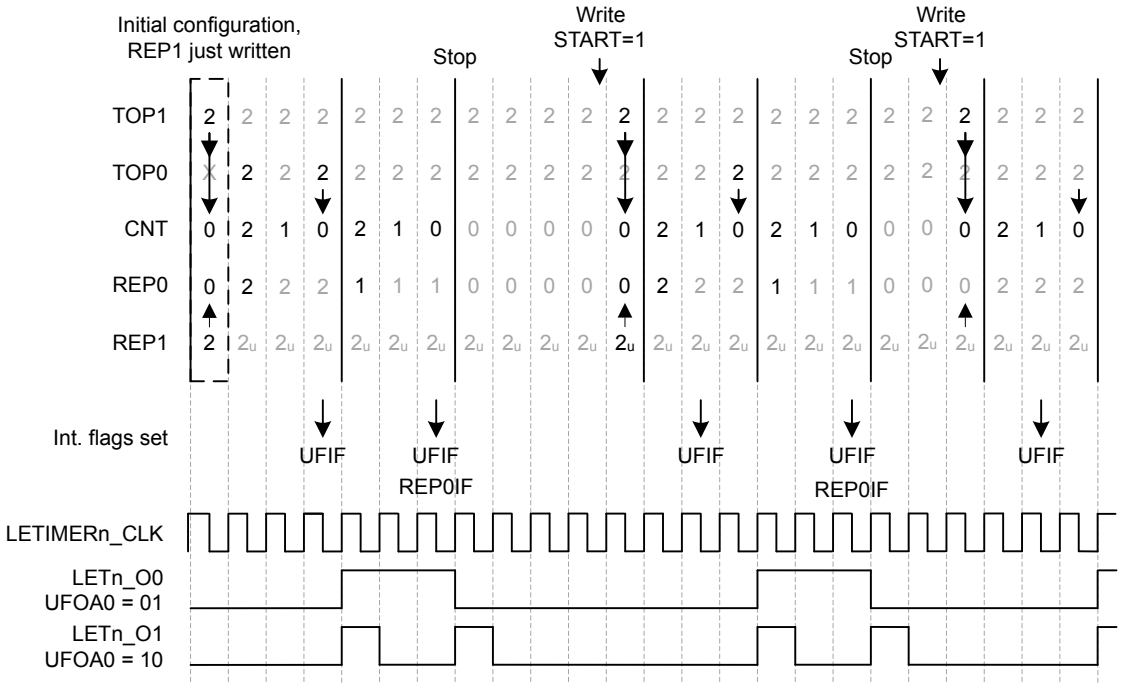


Figure 19.11. LETIMER - Buffered Mode Waveform

19.12.5 Continuous Output Generation

In some scenarios, it might be desired to make LETIMER generate a continuous waveform. Very simple constant waveforms can be generated without the repeat counter as shown in Figure 19.8 LETIMER - Free Running Mode Waveform on page 540, but to generate changing waveforms, using the repeat counter and buffer registers can prove advantageous.

For the example in Figure 19.12 LETIMER - Continuous Operation on page 543, the goal is to produce a pulse train consisting of 3 sequences with the following properties:

- 3 pulses with periods of 3 cycles
- 4 pulses with periods of 2 cycles
- 2 pulses with periods of 3 cycles

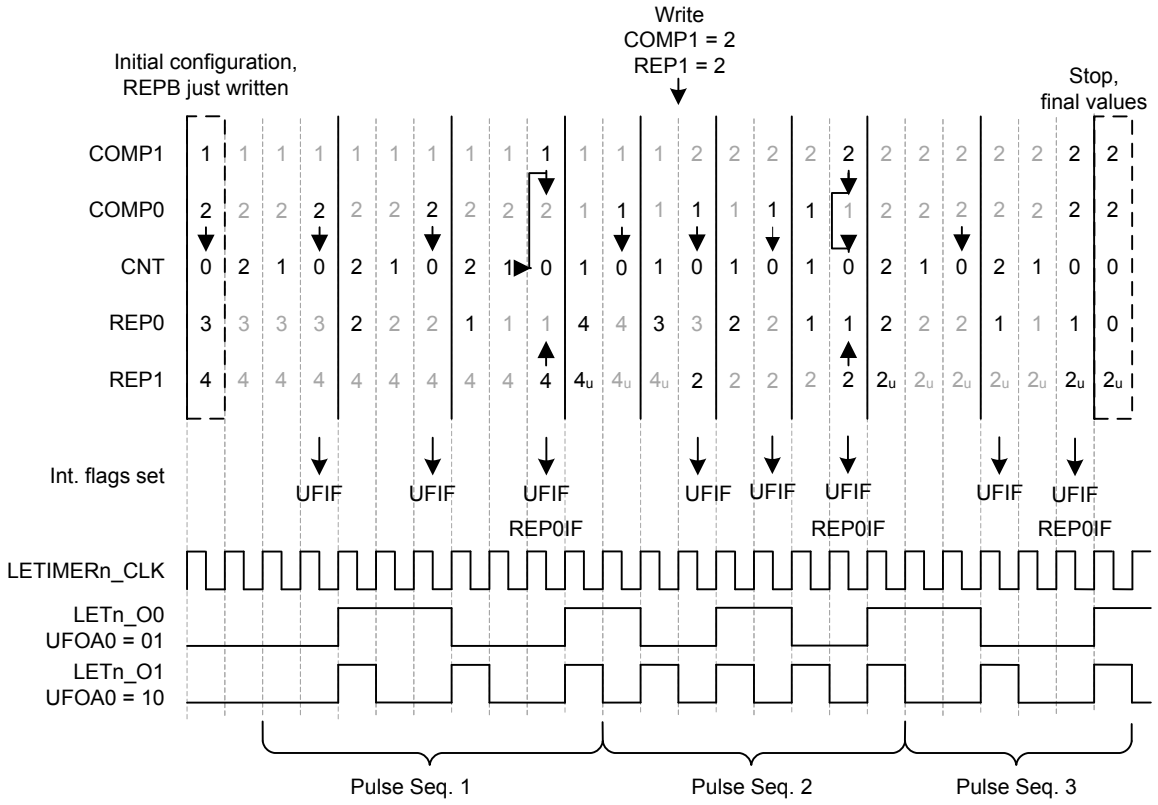


Figure 19.12. LETIMER - Continuous Operation

The first two sequences are loaded into the LETIMER before the timer is started.

LETIMERn_TOP is set to 2 (cycles – 1), and LETIMERn_REP0 is set to 3 for the first sequence, and the second sequence is loaded into the buffer registers, i.e. TOPBUFF is set to 1 and LETIMERn_REP1 is set to 4.

The LETIMER is set to trigger an interrupt when LETIMERn_REP0 is done by setting REP0 in LETIMERn_IEN. This interrupt is a good place to update the values of the buffers. Last but not least REPMODE in LETIMERn_CTRL is set to buffered mode, and the timer is started.

In the interrupt routine the buffers are updated with the values for the third sequence. If this had not been done, the timer would have stopped after the second sequence.

The final result is shown in Figure 19.12 LETIMER - Continuous Operation on page 543. The pulse output is grouped to show which sequence generated which output. Toggle output is also shown in the figure. Note that the toggle output is not aligned with the pulse outputs.

Note: Multiple LETIMER cycles are required to write a value to the LETIMER registers. The example in Figure 19.12 LETIMER - Continuous Operation on page 543 assumes that writes are done in advance so they arrive in the LETIMER as described in the figure.

Figure 19.13 LETIMERn_CNT Not Initialized to 0 on page 544 shows an example where the LETIMER is started while LETIMERn_CNT is nonzero. In this case the length of the first repetition is given by the value in LETIMERn_CNT.

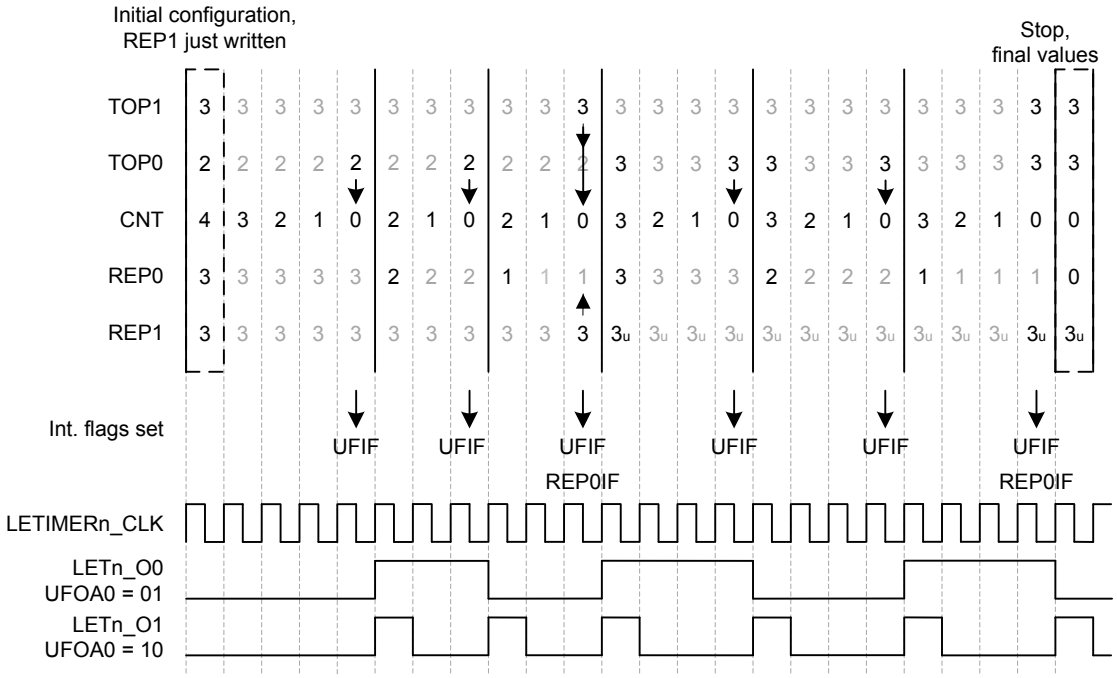


Figure 19.13. LETIMERn_CNT Not Initialized to 0

19.12.6 PWM Output

There are several ways of generating PWM output with the LETIMER, but the most straight-forward way is to use the PWM output mode. This mode is enabled by setting UFOA0 or UFOA1 in LETIMERn_CTRL to 3. In PWM mode, the output is set to idle on timer underflow, and active on LETIMERn_COMP0/1 match, so if for instance CNTTOPEN = 1 and OPOL0 = 0 in LETIMERn_CTRL, LETIMERn_TOP determines the PWM period, and LETIMERn_COMP0/1 determines the active period.

The PWM period in PWM mode is LETIMERn_TOP + 1. There is no special handling of the case where LETIMERn_COMP0/1 > LETIMERn_TOP, so if LETIMERn_COMP0/1 > LETIMERn_TOP, the PWM output is given by the idle output value. This means that for OPOLx = 0 in LETIMERn_CTRL, the PWM output will always be 0 for at least one clock cycle, and for OPOLx = 1 LETIMERn_CTRL, the PWM output will always be 1 for at least one clock cycle.

To generate a PWM signal using the full PWM range, invert OPOLx when LETIMERn_COMP0/1 is set to a value larger than LETIMERn_TOP.

19.13 LETIMER Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	LETIMER_IPVERSION	R	IP Version
0x004	LETIMER_EN	RW ENABLE	Module En
0x008	LETIMER_SWRST	RW SWRST	Software Reset Register
0x00C	LETIMER_CTRL	RW	Control Register
0x010	LETIMER_CMD	W LFSYNC	Command Register
0x014	LETIMER_STATUS	RH	Status Register
0x018	LETIMER_CNT	RWH LFSYNC	Counter Value Register
0x01C	LETIMER_COMP0	RW	Compare Value Register 0
0x020	LETIMER_COMP1	RW	Compare Value Register 1
0x024	LETIMER_TOP	RWH LFSYNC	Counter TOP Value Register
0x028	LETIMER_TOPBUFF	RW	Buffered Counter TOP Value
0x02C	LETIMER_REP0	RWH LFSYNC	Repeat Counter Register 0
0x030	LETIMER_REP1	RWH LFSYNC	Repeat Counter Register 1
0x034	LETIMER_IF	RWH INTFLAG	Interrupt Flag Register
0x038	LETIMER_IEN	RW	Interrupt Enable Register
0x03C	LETIMER_LOCK	W	Configuration Lock Register
0x040	LETIMER_SYNCBUSY	RH	Synchronization Busy Register
0x050	LETIMER_PRSMODE	RW	PRS Input Mode Select Register
0x1000	LETIMER_IPVERSION_SET	R	IP Version
0x1004	LETIMER_EN_SET	RW ENABLE	Module En
0x1008	LETIMER_SWRST_SET	RW SWRST	Software Reset Register
0x100C	LETIMER_CTRL_SET	RW	Control Register
0x1010	LETIMER_CMD_SET	W LFSYNC	Command Register
0x1014	LETIMER_STATUS_SET	RH	Status Register
0x1018	LETIMER_CNT_SET	RWH LFSYNC	Counter Value Register
0x101C	LETIMER_COMP0_SET	RW	Compare Value Register 0
0x1020	LETIMER_COMP1_SET	RW	Compare Value Register 1
0x1024	LETIMER_TOP_SET	RWH LFSYNC	Counter TOP Value Register
0x1028	LETIMER_TOPBUFF_SET	RW	Buffered Counter TOP Value
0x102C	LETIMER_REP0_SET	RWH LFSYNC	Repeat Counter Register 0
0x1030	LETIMER_REP1_SET	RWH LFSYNC	Repeat Counter Register 1
0x1034	LETIMER_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x1038	LETIMER_IEN_SET	RW	Interrupt Enable Register
0x103C	LETIMER_LOCK_SET	W	Configuration Lock Register
0x1040	LETIMER_SYNCBUSY_SET	RH	Synchronization Busy Register

Offset	Name	Type	Description
0x1050	LETIMER_PRSMODE_SET	RW	PRS Input Mode Select Register
0x2000	LETIMER_IPVERSION_CLR	R	IP Version
0x2004	LETIMER_EN_CLR	RW ENABLE	Module En
0x2008	LETIMER_SWRST_CLR	RW SWRST	Software Reset Register
0x200C	LETIMER_CTRL_CLR	RW	Control Register
0x2010	LETIMER_CMD_CLR	W LFSYNC	Command Register
0x2014	LETIMER_STATUS_CLR	RH	Status Register
0x2018	LETIMER_CNT_CLR	RWH LFSYNC	Counter Value Register
0x201C	LETIMER_COMP0_CLR	RW	Compare Value Register 0
0x2020	LETIMER_COMP1_CLR	RW	Compare Value Register 1
0x2024	LETIMER_TOP_CLR	RWH LFSYNC	Counter TOP Value Register
0x2028	LETIMER_TOPBUFF_CLR	RW	Buffered Counter TOP Value
0x202C	LETIMER_REP0_CLR	RWH LFSYNC	Repeat Counter Register 0
0x2030	LETIMER_REP1_CLR	RWH LFSYNC	Repeat Counter Register 1
0x2034	LETIMER_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x2038	LETIMER_IEN_CLR	RW	Interrupt Enable Register
0x203C	LETIMER_LOCK_CLR	W	Configuration Lock Register
0x2040	LETIMER_SYNCBUSY_CLR	RH	Synchronization Busy Register
0x2050	LETIMER_PRSMODE_CLR	RW	PRS Input Mode Select Register
0x3000	LETIMER_IPVERSION_TGL	R	IP Version
0x3004	LETIMER_EN_TGL	RW ENABLE	Module En
0x3008	LETIMER_SWRST_TGL	RW SWRST	Software Reset Register
0x300C	LETIMER_CTRL_TGL	RW	Control Register
0x3010	LETIMER_CMD_TGL	W LFSYNC	Command Register
0x3014	LETIMER_STATUS_TGL	RH	Status Register
0x3018	LETIMER_CNT_TGL	RWH LFSYNC	Counter Value Register
0x301C	LETIMER_COMP0_TGL	RW	Compare Value Register 0
0x3020	LETIMER_COMP1_TGL	RW	Compare Value Register 1
0x3024	LETIMER_TOP_TGL	RWH LFSYNC	Counter TOP Value Register
0x3028	LETIMER_TOPBUFF_TGL	RW	Buffered Counter TOP Value
0x302C	LETIMER_REP0_TGL	RWH LFSYNC	Repeat Counter Register 0
0x3030	LETIMER_REP1_TGL	RWH LFSYNC	Repeat Counter Register 1
0x3034	LETIMER_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x3038	LETIMER_IEN_TGL	RW	Interrupt Enable Register
0x303C	LETIMER_LOCK_TGL	W	Configuration Lock Register
0x3040	LETIMER_SYNCBUSY_TGL	RH	Synchronization Busy Register
0x3050	LETIMER_PRSMODE_TGL	RW	PRS Input Mode Select Register

19.14 LETIMER Register Description

19.14.1 LETIMER_IPVERSION - IP Version

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x1																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x1	R	**IP Version**
	The read only IPVERSION field gives the version for this module. There may be minor software changes required for modules with different values of IPVERSION.			

19.14.2 LETIMER_EN - Module En

Offset	Bit Position																															
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	RW
Name																															DISABLING	EN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DISABLING	0x0	R	**Disablement busy status**
	When EN is cleared, DISABLING is set immediately, and cleared when disablement finishes. Disablement resets peripheral cores and not APB registers except hardware updated registers such as INTFLAGs, FIFOs etc.			
0	EN	0x0	RW	**module en**
	Enable the LETIMER module. Software should write to CONFIG type registers before setting the ENABLE bit. Software should write to SYNC type registers only after setting the ENABLE bit. When EN is cleared(disablement), it halts module operation immediately, and initialize the core domain such that when the is re-enabled, it starts cleanly.			

19.14.3 LETIMER_SWRST - Software Reset Register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	W
Name																															RESETTING	SWRST

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	RESETTING	0x0	R	**Software reset busy status** When SWRST command is issued, resetting logic sets RESETTING status immediately, and later it is cleared when reset process finishes.
0	SWRST	0x0	W	**Software reset command** A software reset command field resets the module back to the initial condition, similar to a power on reset condition

19.14.4 LETIMER_CTRL - Control Register

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0							0x0			0x0	0x0	0x0	0x0	0x0		0x0		0x0	
Access													RW							RW			RW	RW	RW	RW	RW		RW		RW	
Name													CNTPRESC							DEBUGRUN			CNTTOPEN	BUFTOP	OPOL1	OPOL0	UFOA1		UFOA0		REPMODE	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	CNTPRESC	0x0	RW	**Counter prescaler value**

Configure counting frequency of the CNT register. - Note - its not recommended to change this setting on the fly.

Value	Mode	Description
0	DIV1	CLK_CNT = (LETIMER LF CLK)/1
1	DIV2	CLK_CNT = (LETIMER LF CLK)/2
2	DIV4	CLK_CNT = (LETIMER LF CLK)/4
3	DIV8	CLK_CNT = (LETIMER LF CLK)/8
4	DIV16	CLK_CNT = (LETIMER LF CLK)/16
5	DIV32	CLK_CNT = (LETIMER LF CLK)/32
6	DIV64	CLK_CNT = (LETIMER LF CLK)/64
7	DIV128	CLK_CNT = (LETIMER LF CLK)/128
8	DIV256	CLK_CNT = (LETIMER LF CLK)/256

15:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12	DEBUGRUN	0x0	RW	**Debug Mode Run Enable**

Set to keep the LETIMER running in debug mode.

Value	Mode	Description
0	DISABLE	LETIMER is frozen in debug mode
1	ENABLE	LETIMER is running in debug mode

11:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	CNTTOPEN	0x0	RW	**Compare Value 0 Is Top Value**

When set, TOP value will be used as Counter Top Value

Value	Mode	Description
0	DISABLE	The top value of the LETIMER is 65535 (0xFFFF)

Bit	Name	Reset	Access	Description
	1	ENABLE		The top value of the LETIMER is given by COMP0
8	BUFTOP	0x0	RW	**Buffered Top**
	Set to load TOPBUFF into TOP when REP0 reaches 0 in BUFFERED mode, allowing a buffered top value.			
	Value	Mode		Description
	0	DISABLE		COMP0 is only written by software
	1	ENABLE		COMP0 is set to COMP1 when REP0 reaches 0
7	OPOL1	0x0	RW	**Output 1 Polarity**
	Defines the idle value of output 1.			
6	OPOL0	0x0	RW	**Output 0 Polarity**
	Defines the idle value of output 0.			
5:4	UFOA1	0x0	RW	**Underflow Output Action 1**
	Defines the action on OUT1 on a LETIMER underflow - IDLE/TOGGLE/PULSE/PWM			
	Value	Mode		Description
	0	NONE		LETIMERn_OUT1 is held at its idle value as defined by OPOL1
	1	TOGGLE		LETIMERn_OUT1 is toggled on CNT underflow
	2	PULSE		LETIMERn_OUT1 is held active for one LETIMER0 clock cycle on CNT underflow. The output then returns to its idle value as defined by OPOL1
	3	PWM		LETIMERn_OUT1 is set idle on CNT underflow, and active on compare match with COMP1
3:2	UFOA0	0x0	RW	**Underflow Output Action 0**
	Defines the action on OUT0 on a LETIMER underflow - IDLE/TOGGLE/PULSE/PWM			
	Value	Mode		Description
	0	NONE		LETIMERn_OUT0 is held at its idle value as defined by OPOL0
	1	TOGGLE		LETIMERn_OUT0 is toggled on CNT underflow
	2	PULSE		LETIMERn_OUT0 is held active for one LETIMER0 clock cycle on CNT underflow. The output then returns to its idle value as defined by OPOL0
	3	PWM		LETIMERn_OUT0 is set idle on CNT underflow, and active on compare match with COMP1
1:0	REPMODE	0x0	RW	**Repeat Mode**
	Repeat Mode - FREE/ONESHOT/BUFFERED/DOUBLE			
	Value	Mode		Description
	0	FREE		When started, the LETIMER counts down until it is stopped by software
	1	ONESHOT		The counter counts REP0 times. When REP0 reaches zero, the counter stops

Bit	Name	Reset	Access	Description
	2	BUFFERED		The counter counts REP0 times. If REP1 has been written, it is loaded into REP0 when REP0 reaches zero, otherwise the counter stops
	3	DOUBLE		Both REP0 and REP1 are decremented when the LETIMER wraps around. The LETIMER counts until both REP0 and REP1 are zero

19.14.5 LETIMER_CMD - Command Register

Offset	Bit Position																															
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												W(nB)	W(nB)	W(nB)	W(nB)	W(nB)
Name																												CTO1	CTO0	CLEAR	STOP	START

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	CTO1	0x0	W(nB)	**Clear Toggle Output 1**
	Set to drive toggle output 1 to its idle value			
3	CTO0	0x0	W(nB)	**Clear Toggle Output 0**
	Set to drive toggle output 0 to its idle value			
2	CLEAR	0x0	W(nB)	**Clear LETIMER**
	Set to clear LETIMER			
1	STOP	0x0	W(nB)	**Stop LETIMER**
	Set to stop LETIMER			
0	START	0x0	W(nB)	**Start LETIMER**
	Set to start LETIMER			

19.14.6 LETIMER_STATUS - Status Register

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	R
Name																															LETIMERLOCKSTATUS	RUNNING

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	LETIMERLOCKSTATUS	0x0	R	**LETIMER Lock Status**
	Indicates the current status of LETIMER Lock			

Value	Mode	Description
0	UNLOCKED	LETIMER registers are unlocked
1	LOCKED	LETIMER registers are locked

0	RUNNING	0x0	R	**LETIMER Running**
	Set when LETIMER is running.			

19.14.7 LETIMER_CNT - Counter Value Register

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset									0x0																							
Access									RW																							
Name									CNT																							

Bit	Name	Reset	Access	Description
31:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:0	CNT	0x0	RW	**Counter Value**
	Use to read the current value of the LETIMER.			

19.14.8 LETIMER_COMP0 - Compare Value Register 0

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset									0x0																						
Access									RW																						
Name									COMP0																						

Bit	Name	Reset	Access	Description
31:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:0	COMP0	0x0	RW	**Compare Value 0**
	Compare value for LETIMER.			

19.14.9 LETIMER_COMP1 - Compare Value Register 1

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset									0x0																						
Access									RW																						
Name									COMP1																						

Bit	Name	Reset	Access	Description
31:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:0	COMP1	0x0	RW	**Compare Value 1**
	Compare and optionally buffered top value for LETIMER.			

19.14.10 LETIMER_TOP - Counter TOP Value Register

Offset	Bit Position																													
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset									0x0																						
Access									RW																						
Name									TOP																						

Bit	Name	Reset	Access	Description
31:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:0	TOP	0x0	RW	**Counter TOP Value**
	TOP will be used as Counter TOP Value if CNTTOPEN is set to 1			

19.14.11 LETIMER_TOPBUFF - Buffered Counter TOP Value

Offset	Bit Position																													
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset									0x0																						
Access									RW																						
Name									TOPBUFF																						

Bit	Name	Reset	Access	Description
31:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:0	TOPBUFF	0x0	RW	**Buffered Counter TOP Value**
	TOPBUFF will be used as Counter TOP Value in BUFFERED Mode if CNTTOPEN and BUFFTOP is set set to 1			

19.14.12 LETIMER_REP0 - Repeat Counter Register 0

Offset	Bit Position																													
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									RW							
Name																									REP0							

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	REP0	0x0	RW	**Repeat Counter 0**
	Optional repeat counter.			

19.14.13 LETIMER_REP1 - Repeat Counter Register 1

Offset	Bit Position																													
0x030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									RW							
Name																									REP1							

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	REP1	0x0	RW	**Repeat Counter 1**
	Optional repeat counter or buffer for REP0.			

19.14.14 LETIMER_IF - Interrupt Flag Register

Offset	Bit Position																														
0x034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												RW	RW	RW	RW	RW
Name																												REP1	REP0	UF	COMP1	COMP0

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	REP1	0x0	RW	**Repeat Counter 1 Interrupt Flag**
	Set when repeat counter 1 reaches zero.			
3	REP0	0x0	RW	**Repeat Counter 0 Interrupt Flag**
	Set when repeat counter 0 reaches zero or when the REP1 interrupt flag is loaded into the REP0 interrupt flag.			
2	UF	0x0	RW	**Underflow Interrupt Flag**
	Set on LETIMER underflow.			
1	COMP1	0x0	RW	**Compare Match 1 Interrupt Flag**
	Set when LETIMER reaches the value of COMP1.			
0	COMP0	0x0	RW	**Compare Match 0 Interrupt Flag**
	Set when LETIMER reaches the value of COMP0.			

19.14.15 LETIMER_IEN - Interrupt Enable Register

Offset	Bit Position																													
0x038	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												RW	RW	RW	RW	RW
Name																												REP1	REP0	UF	COMP1	COMP0

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	REP1	0x0	RW	**Repeat Counter 1 Interrupt Enable**
	Repeat Counter 1 Interrupt Enable			
3	REP0	0x0	RW	**Repeat Counter 0 Interrupt Enable**
	Repeat Counter 0 Interrupt Enable			
2	UF	0x0	RW	**Underflow Interrupt Enable**
	Underflow Interrupt Enable			
1	COMP1	0x0	RW	**Compare Match 1 Interrupt Enable**
	Compare Match 1 Interrupt Enable			
0	COMP0	0x0	RW	**Compare Match 0 Interrupt Enable**
	Compare Match 0 Interrupt Enable			

19.14.16 LETIMER_LOCK - Configuration Lock Register

Offset	Bit Position																													
0x03C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									W							
Name																									LETIMERLOCKKEY							

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LETIMERLOCKKEY	0x0	W	**Configuration Lock Key**

Write any other value than the unlock code to lock LETIMER_EN, LETIMER_SWRST, LETIMER_CTRL, LETIMER_CMD, LETIMER_CNT, LETIMER_COMP0, LETIMER_COMP1, LETIMER_TOP, LETIMER_TOPBUFF, LETIMER_REP0, LETIMER_REP1 and PRSMODE registers from editing. Write the unlock code to unlock.

Value	Mode	Description
52476	UNLOCK	Write to unock LETIMER lockable registers

19.14.17 LETIMER_SYNCBUSY - Synchronization Busy Register

Offset	Bit Position																													
0x040	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0		0x0
Access																							R	R	R	R	R	R	R	R		R
Name																							CTO1	CTO0	CLEAR	STOP	START	REP1	REP0	TOP		CNT

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	CTO1	0x0	R	**Sync busy for CTO1**
	Sync busy for CTO1			
8	CTO0	0x0	R	**Sync busy for CTO0**
	Sync busy for CTO0			
7	CLEAR	0x0	R	**Sync busy for CLEAR**
	Sync busy for CLEAR			
6	STOP	0x0	R	**Sync busy for STOP**
	Sync busy for STOP			
5	START	0x0	R	**Sync busy for START**
	Sync busy for START			
4	REP1	0x0	R	**Sync busy for REP1**
	Sync busy for REP1			
3	REP0	0x0	R	**Sync busy for REP0**
	Sync busy for REP0			
2	TOP	0x0	R	**Sync busy for TOP**
	Sync busy for TOP			
1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	CNT	0x0	R	**Sync busy for CNT**
	Sync busy for CNT			

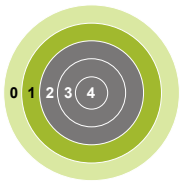
19.14.18 LETIMER_PRSMODE - PRS Input Mode Select Register

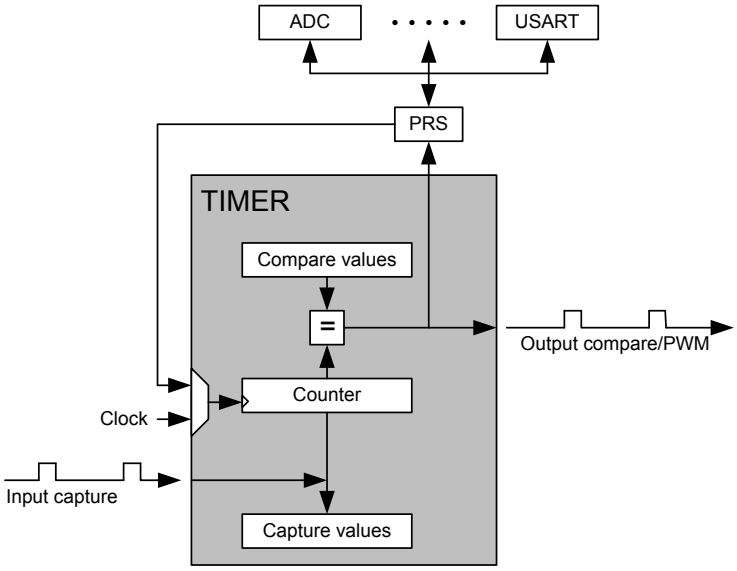
Offset	Bit Position																													
0x050	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0x0				0x0				0x0																			
Access					RW				RW				RW																			
Name					PRSCLEARMODE				PRSSTOPMODE				PRSSTARTMODE																			

Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27:26	PRSCLEARMODE	0x0	RW	**PRS Clear Mode**
	Mode-NONE/RISING/FALLING/BOTH			
	Value	Mode		Description
	0	NONE		PRS cannot clear the LETIMER
	1	RISING		Rising edge of selected PRS input can clear the LETIMER
	2	FALLING		Falling edge of selected PRS input can clear the LETIMER
	3	BOTH		Both the rising or falling edge of the selected PRS input can clear the LETIMER
25:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:22	PRSSTOPMODE	0x0	RW	**PRS Stop Mode**
	Mode-NONE/RISING/FALLING/BOTH			
	Value	Mode		Description
	0	NONE		PRS cannot stop the LETIMER
	1	RISING		Rising edge of selected PRS input can stop the LETIMER
	2	FALLING		Falling edge of selected PRS input can stop the LETIMER
	3	BOTH		Both the rising or falling edge of the selected PRS input can stop the LETIMER
21:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:18	PRSSTARTMODE	0x0	RW	**PRS Start Mode**
	Mode-NONE/RISING/FALLING/BOTH			
	Value	Mode		Description
	0	NONE		PRS cannot start the LETIMER
	1	RISING		Rising edge of selected PRS input can start the LETIMER

Bit	Name	Reset	Access	Description
	2	FALLING		Falling edge of selected PRS input can start the LETIMER
	3	BOTH		Both the rising or falling edge of the selected PRS input can start the LETIMER
17:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

20. TIMER - Timer/Counter





Quick Facts

What?

The TIMER (Timer/Counter) keeps track of timing and counts events, generates output waveforms, and triggers timed actions in other peripherals.

Why?

Most applications have activities that need to be timed accurately with as little CPU intervention and energy consumption as possible.

How?

The flexible 16/32-bit timer can be configured to provide PWM waveforms with optional dead-time insertion (e.g. motor control) or work as a frequency generator. The timer can also count events and control other peripherals through the PRS, which offloads the CPU and reduces energy consumption.

20.1 Introduction

The general purpose timer has 3 or 4 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output.

The TIMER module may be 16 or 32 bits wide. Some timers also include a Dead-Time Insertion module suitable for motor control applications.

Refer to the device data sheet to determine the capabilities (capture/compare channel count, width, and DTI) of each timer instance.

20.2 Features

- 16/32-bit auto reload up/down counter
  - Dedicated 16/32-bit reload register which serves as counter maximum
- 3 or 4 Compare/Capture channels
  - Individually configurable as either input capture or output compare/PWM
- Multiple Counter modes
  - Count up
  - Count down
  - Count up/down
  - Quadrature Decoder
  - Direction and count from external pins
- 2x Count Mode
- Counter control from PRS or external pin
  - Start
  - Stop
  - Reload and start
- Inter-Timer connection
  - Allows 32-bit counter mode
  - Start/stop synchronization between several timers
- Input Capture
  - Period measurement
  - Pulse width measurement
  - Two capture registers for each capture channel
    - Capture on either positive or negative edge
    - Capture on both edges
  - Optional digital noise filtering on capture inputs
- Output Compare
  - Compare output toggle/pulse on compare match
  - Immediate update of compare registers
- PWM
  - Up-count PWM
  - Up/down-count PWM
  - Predictable initial PWM output state (configured by SW)
  - Buffered compare register to ensure glitch-free update of compare values
  - Output re-timing to mitigate RF interference
- Clock sources
  - $HFPERCLK_{TIMERn}$
    - 10-bit Prescaler
  - External pin
  - Peripheral Reflex System
- Debug mode
  - Configurable to either run or stop when processor is stopped (halt/breakpoint)
- Interrupts, PRS output and/or DMA request on:
  - Underflow
  - Overflow
  - Compare/Capture event

- Dead-Time Insertion Unit
  - Complementary PWM outputs with programmable dead-time
    - Dead-time is specified independently for rising and falling edge
      - 10-bit prescaler
      - 6-bit time value
    - Outputs have configurable polarity
    - Outputs can be set inactive individually by software.
  - Configurable action on fault
    - Set outputs inactive
    - Clear output
    - Tristate output
  - Individual fault sources
    - One or two PRS signals
    - Debugger
      - Support for automatic restart
    - Core lockup
    - EM2/EM3 entry
  - Configuration lock

20.3 Functional Description

An overview of the TIMER module is shown in Figure 20.1 TIMER Block Overview on page 564 and it consists of a 16/32 bit up/down counter with 3 compare/capture channels connected to pins TIMn_CC0, TIMn_CC1, and TIMn_CC2.

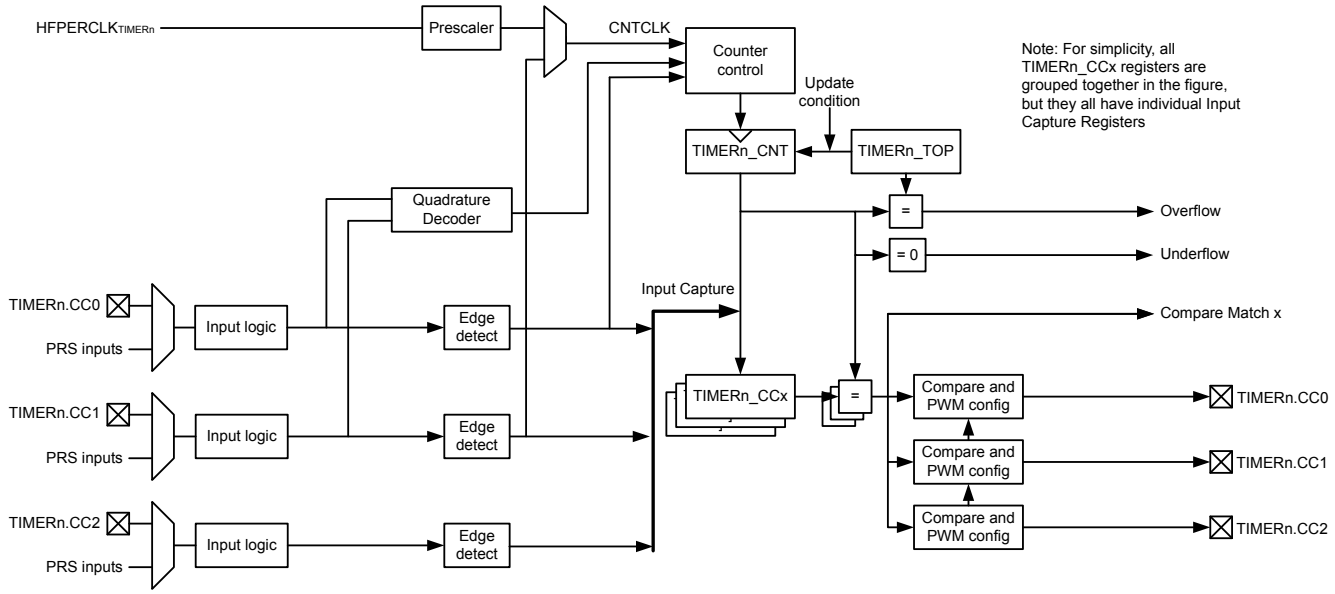


Figure 20.1. TIMER Block Overview

20.3.1 Register Access

The timer module interface consists of multiple register types. Registers of type "RW CONFIG" should only be written when the module is disabled (TIMERn_EN_EN = 0). Registers of type "W SYNC", "R SYNC" or "RW SYNC" should only be read or written when the module is enabled (TIMERn_EN_EN = 1). A typical setup sequence for a TIMER module is as follows:

1. With the TIMER disabled (TIMERn_EN_EN = 0), program any CONFIG registers required for the application.
2. Enable the TIMER by setting EN in TIMERn_EN to 1.
3. Program any non-CONFIG registers required for the application.
4. The TIMER is then ready for use.

20.3.2 Counter Modes

The timer consists of a counter that can be configured to the following modes, using the MODE field in TIMERn_CFG:

- Up-count: Counter counts up until it reaches the value in TIMERn_TOP, where it is reset to 0 before counting up again.
- Down-count: The counter starts at the value in TIMERn_TOP and counts down. When it reaches 0, it is reloaded with the value in TIMERn_TOP.
- Up/Down-count: The counter starts at 0 and counts up. When it reaches the value in TIMERn_TOP, it counts down until it reaches 0 and starts counting up again.
- Quadrature Decoder: Two input channels where one determines the count direction, while the other pin triggers a clock event.

In addition to the TIMER modes listed above, the TIMER also supports a 2x count mode. In this mode the counter increments/decrements by 2 on each clock edge. The 2x count mode can be used to double the PWM frequency when the compare/capture channel is put into PWM mode. The 2x count mode is enabled by setting the X2CNT bitfield in the TIMERn_CTRL register.

The counter value can be read or written by software any time the module is enabled by accessing the CNT field in TIMERn_CNT.

20.3.2.1 Events

The main counter can generate overflow and underflow events during operation.

Overflow (TIMERn_IF_OF) is set when the counter value shifts from TIMERn_TOP to the next value when counting up. In up-count mode and quadrature decoder mode the next value is 0. In up/down-count mode, the next value is TIMERn_TOP-1.

Underflow (TIMERn_IF_UF) is set when the counter value shifts from 0 to the next value when counting down. In down-count mode and quadrature decoder mode, the next value is TIMERn_TOP. In up/down-count mode the next value is 1.

An update event occurs on overflow in up-count mode and on underflow in down-count or up/down count mode. Additionally, an update event also occurs on overflow and underflow in quadrature decoder . This event is used to time updates of buffered values.

20.3.2.2 Operation

Figure 20.2 TIMER Hardware Timer/Counter Control on page 566 shows the hardware timer/counter control. Software can start or stop the counter by setting the START or STOP bits in TIMERn_CMD. The counter value (CNT in TIMERn_CNT) can always be written by software to any 16/32-bit value.

It is also possible to control the counter through either an external pin or PRS input. This is done through the input logic for the compare/capture Channel 0. The timer/counter allows individual actions (start, stop, reload) to be taken for rising and falling input edges. This is configured in the RISEA and FALLA fields in TIMERn_CTRL. The reload value is 0 in up-count and up/down-count mode and TOP in down-count mode.

The RUNNING bit in TIMERn_STATUS indicates if the timer is running or not. If the SYNC bit in TIMERn_CFG is set, the timer is started/stopped/reloaded (external pin or PRS) when any of the other timers are started/stopped/reloaded.

The DIR bit in TIMERn_STATUS indicates the counting direction of the timer at any given time. The counter value can be read or written by software through the CNT field in TIMERn_CNT. In Up/Down-Count mode the count direction will be set to up if the CNT value is written by software.

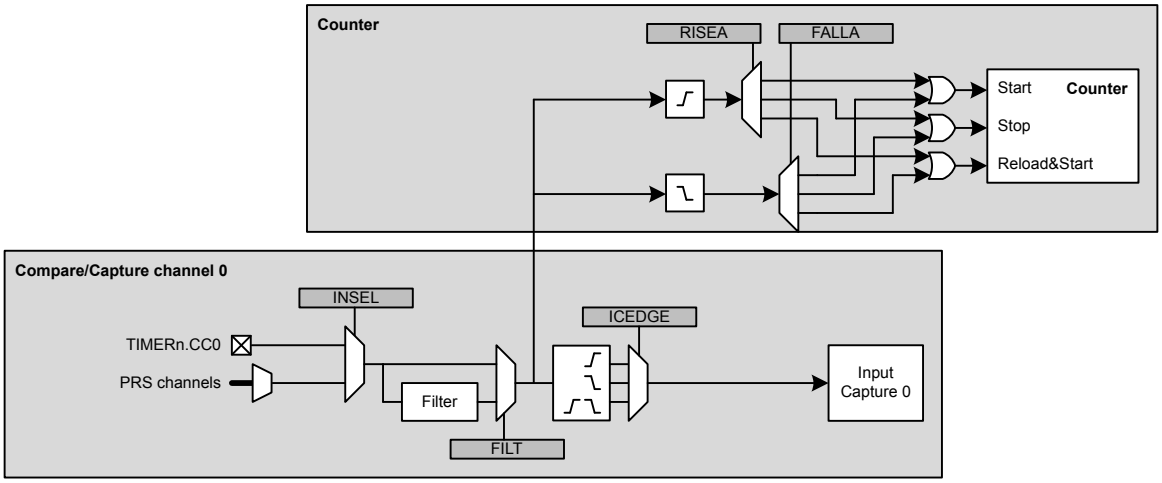


Figure 20.2. TIMER Hardware Timer/Counter Control

20.3.2.3 Clock Source

The counter can be clocked from several sources, which are all synchronized with the incoming peripheral clock for the timer. See Figure 20.3 TIMER Clock Selection on page 566.

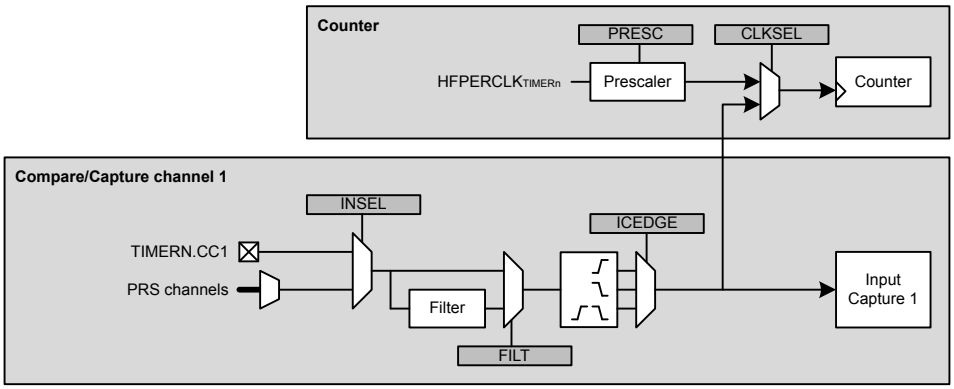


Figure 20.3. TIMER Clock Selection

20.3.2.4 Peripheral Clock

The peripheral clock for the timer ($HFPERCLK_{TIMERn}$) clocks the logic for the timer block, even when it is not the selected clock source.

All TIMER instances in this device family use EM01GRPACLK selected in CMU_EM01GRPACLKCTRL_CLKSEL as their peripheral clock source ($HFPERCLK_{TIMERn}$).

The peripheral clock to each timer can be used as a source with a configurable 10-bit prescaler. The PRESC bitfield in TIMERn_CFG sets the prescaler value, and the incoming peripheral clock will be divided by a factor of (PRESC+1). However, if 2x count mode is enabled and the compare/capture channels are configured for PWM mode, the CC output is updated on both clock edges, so prescaling the peripheral clock will produce an incorrect result. The internal prescale counter is stopped and reset when the timer is stopped.

20.3.2.5 Compare/Capture Channel 1 Input

The timer can also be clocked by positive and/or negative edges on the compare/capture channel 1 input. This input can either come from the TIMn_CC1 pin or one of the PRS channels. The input signal must not have a higher frequency than $f_{HFPERCLK\_TIMERn}/3$ when running from a pin input or a PRS input with FILT enabled in TIMERn_CCx_CFG. When running from PRS without FILT, the frequency can be as high as $f_{HFPERCLK\_TIMERn}$. Note that when clocking the timer from the same pulse that triggers a start (through RISEA/FALLA in TIMERn_CTRL), the starting pulse will not update the counter value.

20.3.2.6 Underflow/Overflow From Neighboring Timer

All timers are linked together (see Figure 20.4 TIMER Connections on page 567), allowing timers to count on overflow/underflow from the lower numbered neighbouring timers to form a larger timer. Note that all timers must be set to count the same direction and less significant timer(s) can only be set to count up or down.

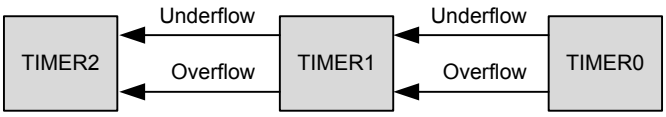


Figure 20.4. TIMER Connections

20.3.2.7 One-Shot Mode

By default, the counter counts continuously until it is stopped. If the OSMEN bit is set in the TIMERn_CFG register, however, the counter is disabled by hardware on the first *update event* (see 20.3.2.1 Events). Note that when the counter is running with CC1 as clock source and OSMEN is set, a CC1 capture event will not take place on the *update event* (CC1 rising edge) that stops the timer.

20.3.2.8 Top Value Buffer

The TIMERn_TOP register can be altered either by writing it directly or by writing to the TIMER_TOPB (buffer) register. When writing to the buffer register the TIMERn_TOPB register will be written to TIMERn_TOP on the next *update event*. Buffering ensures that the TOP value is not set below the actual count value. The TOPBV flag in TIMERn_STATUS indicates whether the TIMERn_TOPB register contains data that has not yet been written to the TIMERn_TOP register (see Figure 20.5 TIMER TOP Value Update Functionality on page 568).

Note: When writing to TIMERn_TOP register directly, the TIMERn_TOPB register value will be invalidated and the TOPBV flag will be cleared. This prevents TIMERn_TOP register from being immediately updated by an existing valid TIMERn_TOPB value during the next *update event*.

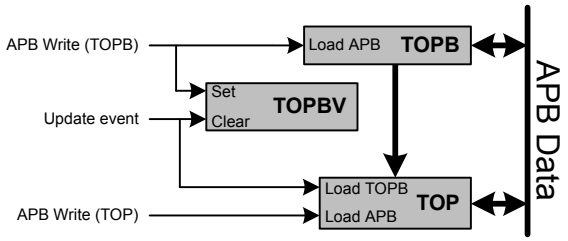


Figure 20.5. TIMER TOP Value Update Functionality

20.3.2.9 Quadrature Decoder

Quadrature decoding mode is used to track motion and determine both rotation direction and position. The quadrature decoder uses two input channels that are 90 degrees out of phase (see Figure 20.6 TIMER Quadrature Encoded Inputs on page 569).

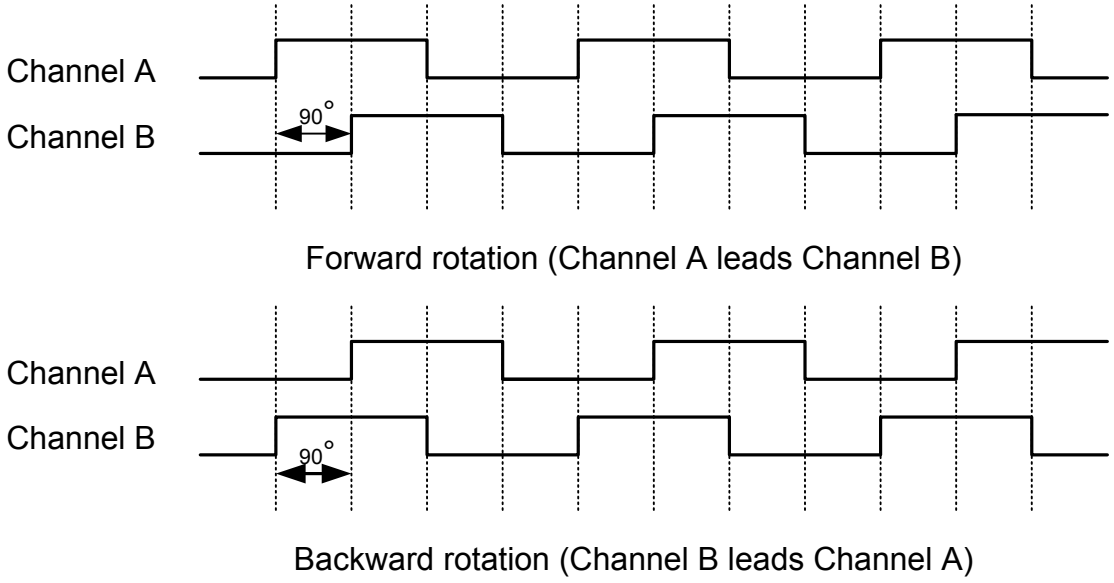


Figure 20.6. TIMER Quadrature Encoded Inputs

In the timer these inputs are tapped from the compare/capture channel 0 (Channel A) and 1 (Channel B) inputs before edge detection. The timer/counter then increments or decrements the counter, based on the phase relation between the two inputs. The DIRCHG flag in TIMERn_IF is set if the count direction changes in quadrature decoder mode. The quadrature decoder supports two channels, but if a third channel (Z-terminal) is available, this can be connected to an external interrupt and trigger a counter reset from the interrupt service routine. By connecting a periodic signal from another timer as input capture on compare/capture Channel 2, it is also possible to calculate speed and acceleration.

Note: In quadrature decoder mode, overflow and underflow triggers an *update event.*

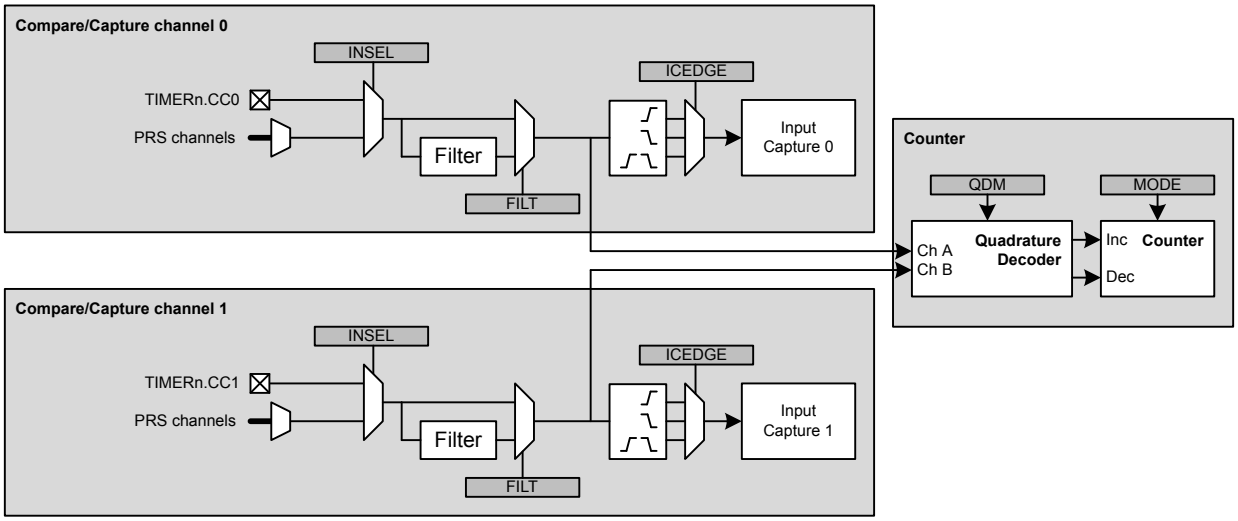


Figure 20.7. TIMER Quadrature Decoder Configuration

The quadrature decoder can be set in either X2 or X4 mode, which is configured in the QDM bit in TIMERn_CFG. See Figure 20.7 TIMER Quadrature Decoder Configuration on page 569

20.3.2.10 X2 Decoding Mode

In X2 Decoding mode, the counter increments or decrements on every edge of Channel A, see Table 20.1 TIMER Counter Response in X2 Decoding Mode on page 570 and Figure 20.8 TIMER X2 Decoding Mode on page 570.

Table 20.1. TIMER Counter Response in X2 Decoding Mode

Channel B	Channel A	
	Rising	Falling
0	Increment	Decrement
1	Decrement	Increment

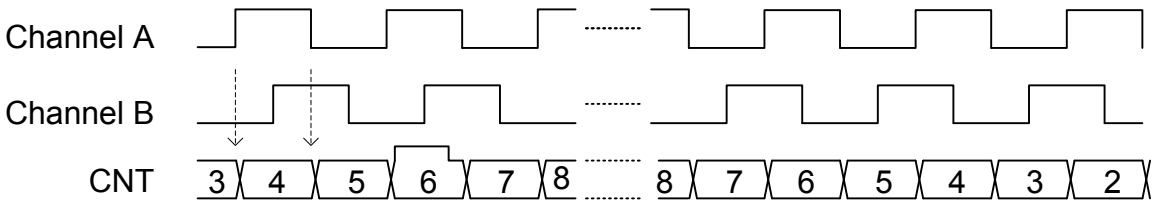


Figure 20.8. TIMER X2 Decoding Mode

20.3.2.11 X4 Decoding Mode

In X4 Decoding mode, the counter increments or decrements on every edge of Channel A and Channel B, see Figure 20.9 TIMER X4 Decoding Mode on page 570 and Table 20.2 TIMER Counter Response in X4 Decoding Mode on page 570.

Table 20.2. TIMER Counter Response in X4 Decoding Mode

Opposite Channel	Channel A		Channel B	
	Rising	Falling	Rising	Falling
Channel A = 0			Decrement	Increment
Channel A = 1			Increment	Decrement
Channel B = 0	Increment	Decrement		
Channel B = 1	Decrement	Increment		

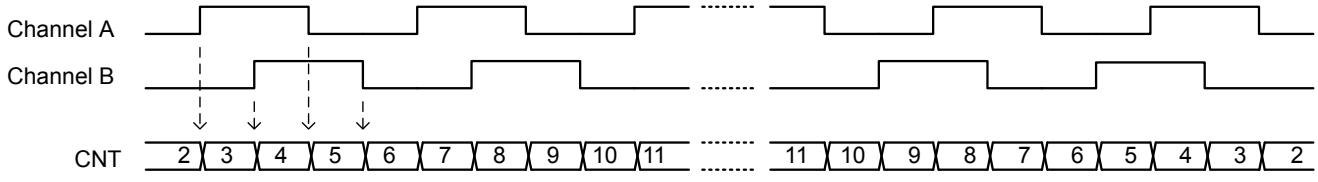


Figure 20.9. TIMER X4 Decoding Mode

20.3.2.12 Rotational Position

To calculate a position Figure 20.10 TIMER Rotational Position Equation on page 571 can be used.

$$pos° = (CNT/X \times N) \times 360°$$

Figure 20.10. TIMER Rotational Position Equation

where X = Encoding type and N = Number of pulses per revolution.

20.3.3 Compare/Capture Channels

The timer contains compare/capture channels, which can be independently configured in the following modes:

1. Input Capture
2. Output Compare
3. PWM

20.3.3.1 Input Pin Logic

Each compare/capture channel can be configured as an input source for the Capture Unit or as external clock source for the timer (see Figure 20.11 TIMER Input Pin Logic on page 571). Compare/capture channels 0 and 1 are the inputs for the quadrature decoder . The input channel can be filtered before it is used, which requires the input to remain stable for up to 5 cycles in a row before the input is propagated to the output.

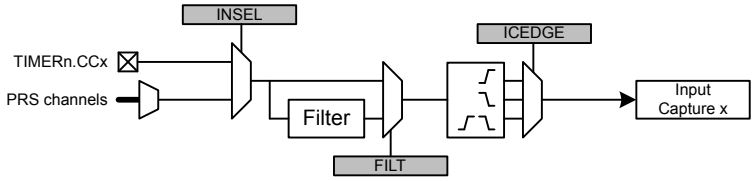


Figure 20.11. TIMER Input Pin Logic

The capture input to the timer may be selected from the dedicated CCx signal for the channel, or a PRS signal. INSEL in TIMERn_CCx_CFG determines the input to the channel. When set to PIN, the selected CCx pin will be used. When INSEL is set to PRSSYNC, a synchronous PRS channel is selected as the source. The synchronous PRS channel is determined by the SPRSSEL field in the PRS_TIMERn_CCx register. Setting INSEL to PRSASYNCLEVEL or PRSASYNCPULSE selects an asynchronous PRS channel as the source. The aynchronous PRS channel is determined by the PRSSEL field in the PRS_TIMERn_CCx register.

The PIN and PRSASYNCLEVEL selections are qualified by a 2-clock input sampler. To recognize and capture the incoming signal, it must be at the new level for at least 2 $HFPERCLK_{TIMERn}$ clock cycles. An additional 5 $HFPERCLK_{TIMERn}$ cycles of filtering can be applied to the signal by enabling the FILT bit in TIMERn_CCx_CFG.

The PRSASYNCPULSE selection can be used to capture higher-speed pulses on an asynchronous PRS input. The input logic for this selection does not qualify the level of the incoming signal. Instead, it will recognize positive or negative edges directly. While the pulse time can be shorter than 1 $HFPERCLK_{TIMERn}$, this mode requires at least 3 $HFPERCLK_{TIMERn}$ clocks between adjacent events. The FILT option is not used in this mode.

Synchronous PRS signals are inherently synchronized to the module clock, and the 2-clock input sampler is not used. However, it is possible to use FILT to enable the 5 $HFPERCLK_{TIMERn}$ filter when using the PRSSYNC option.

20.3.3.2 Compare/Capture Registers

The compare/capture channel registers are prefixed with TIMERn_CCx_, where the x stands for the channel number. Since the compare/capture channels serve three functions (input capture, compare, PWM), different registers are used, depending on the mode the channel is set in.

20.3.3.3 Input Capture

In input capture, the counter value (TIMERn_CNT) can be captured in the Input Capture Register (TIMERn_CCx_ICF) (see Figure 20.12 TIMER Input Capture on page 572). The CCPOL bits in TIMERn_STATUS indicate the polarity of the edge that triggered the capture in TIMERn_CCx_ICF.

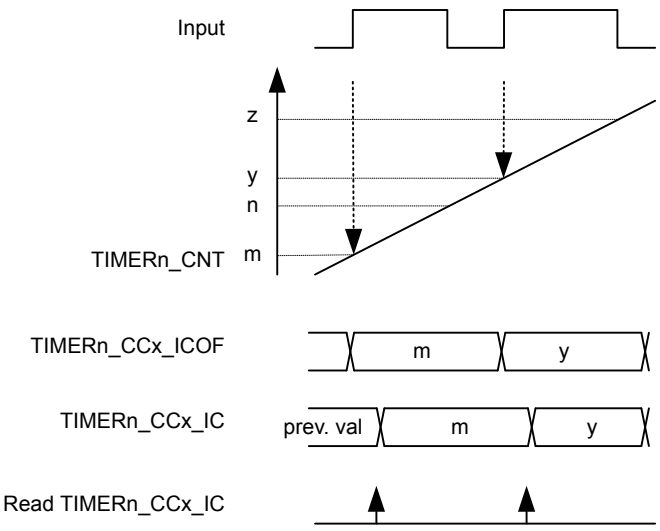


Figure 20.12. TIMER Input Capture

Input captures are buffered into a 2-entry FIFO, allowing 2 subsequent capture events to take place before a read-out is required. Reading TIMERn_CCx_ICF from software or DMA pops the oldest unread value from the FIFO. If TIMERn_CCx_ICF is read when the FIFO is empty (ICFEMPTY in TIMERn_STATUS = 1), the FIFO underflow flag for the channel (ICFUF in TIMERn_IF) will be set. The Input Capture Overflow Register (TIMERn_CCx_ICOF) always contains the newest value in the FIFO. If a new capture is triggered while the FIFO is full, the value in TIMERn_CCx_ICOF will be over-written with the latest value and the FIFO overflow flag (ICFOF in TIMERn_IF) for the channel will be set. Reading TIMERn_CCx_ICOF does not alter the FIFO contents.

The input capture FIFO also has a programmable watermark level that can be configured to generate interrupts or trigger DMA requests when a certain number of empty spots are left in the FIFO. The ICFWLFULL flag inTIMERn_IF will be set when the number of empty spots left in the FIFO is less than or equal to the watermark level programmed in TIMERn_CCx_CFG_ICFWL. At a minimum, a TIMER module will have two FIFO entries, but may have more on future devices.

The ICFEMPTY flag in TIMERn_STATUS indicates when the capture buffer is empty. When this bit reads '0', there is a valid unread capture in the FIFO.

Note: In input capture mode, the timer will only trigger interrupts when it is running.

20.3.3.4 Period/Pulse-Width Capture

Period and/or pulse-width capture can only be possible with Channel 0 (CC0), because this is the only channel that can start and stop the timer. This can be done by setting the RISEA field in TIMERn_CTRL to Clear&Start, and selecting the desired input from either external pin or PRS, see Figure 20.13 TIMER Period and/or Pulse Width Capture on page 573. For period capture, the compare/capture channel should then be set to input capture on a rising edge of the same input signal. To capture the width of a high pulse, the compare/capture channel should be set to capture on a falling edge of the input signal. To measure the low pulse-width of a signal, opposite polarities should be chosen.

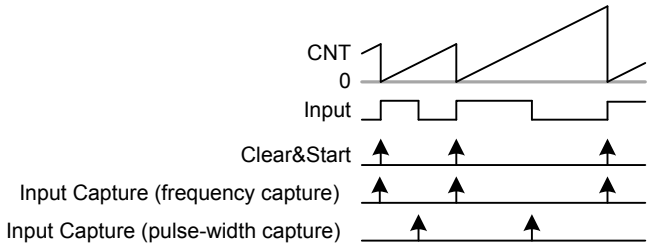


Figure 20.13. TIMER Period and/or Pulse Width Capture

20.3.3.5 Compare

Each compare/capture channel contains a comparator which outputs a compare match if the contents of TIMERn_CCx_OC matches the counter value, see Figure 20.14 TIMER Block Diagram Showing Comparison Functionality on page 574. In compare mode, each compare channel can be configured to either set, clear or toggle the output on an event (compare match, overflow or underflow). The output from each channel is represented as an alternative function on the port it is connected to, which needs to be enabled for the CC outputs to propagate to the pins.

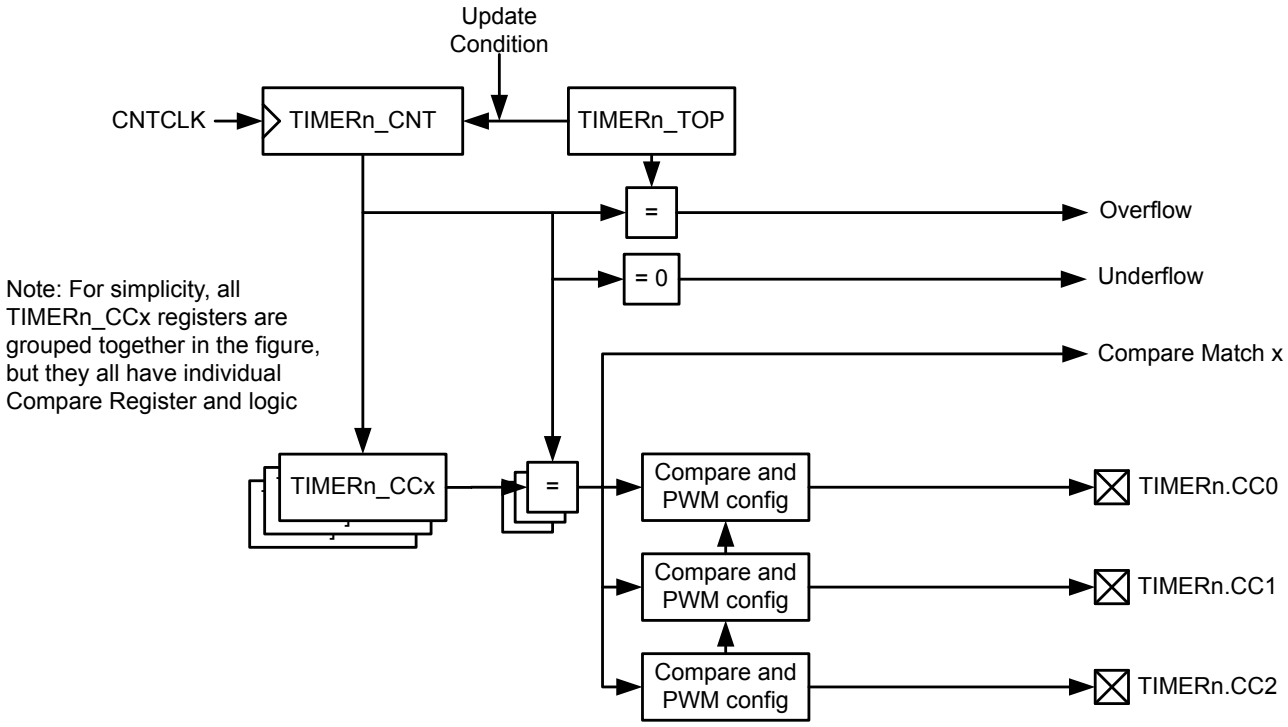


Figure 20.14. TIMER Block Diagram Showing Comparison Functionality

The compare output is delayed by one cycle to allow for full 0% to 100% PWM generation. If occurring in the same cycle, match action will have priority over overflow or underflow action.

The input selected (through PRSSEL in PRS_CONSUMER_TIMERn_CCx, INSEL and FILT in TIMERn_CCx_CFG) for the CC channel will also be sampled on compare match and the result is found in the CCPOL bits in TIMERn_STATUS. It is also possible to configure the CCPOL to always track the inputs by setting ATI in TIMERn_CFG.

Note: When using synchronous PRS sources, it is recommended to configure the PRS consumer registers prior to selecting PRS triggering to avoid any false triggers.

The COIST bit in TIMERn_CCx_CFG is the initial state of the compare/PWM output. The COIST bit can also be used as an initial value to the compare outputs on a reload-start when RSSCOIST is set in TIMERn_CFG. Also the resulting output can be inverted by setting OUTINV in TIMERn_CCx_CTRL. It is recommended to turn off the CC channel before configuring the output state to avoid any unwanted pulses on the output. The CC channel can be turned off by setting MODE to OFF in TIMER_CCx_CFG. The following figure shows the output logic for the TIMER module.

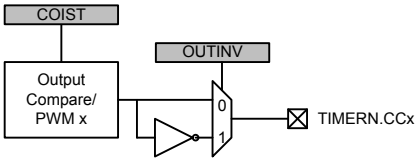


Figure 20.15. TIMER Output Logic

20.3.3.6 Compare Mode Registers

When running in output compare or PWM mode, the value in TIMERn_CCx_OC will be compared against the count value. In Compare mode the output can be configured to toggle, clear or set on compare match, overflow, and underflow through the CMOA, COFOA and CUFOA fields in TIMERn_CCx_CTRL. TIMERn_CCx_OC can be accessed directly or through the buffer register TIMERn_CCx_OCB, see Figure 20.16 TIMER Output Compare/PWM Buffer Functionality Detail on page 575. When writing to the buffer register, the value in TIMERn_CCx_OCB will be written to TIMERn_CCx_OC on the next *update event*. This functionality ensures glitch free PWM outputs. The OCBV flag in TIMERn_STATUS indicates whether the TIMERn_CCx_OCB register contains data that has not yet been written to the TIMERn_CCx_OC register. Note that when writing 0 to TIMERn_CCx_OCB in up-down count mode the OC value is updated when the timer counts from 0 to 1. Thus, the compare match for the next period will not happen until the timer reaches 0 again on the way down.

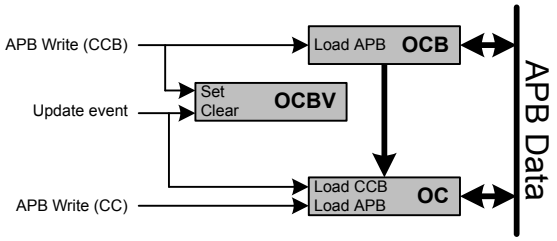


Figure 20.16. TIMER Output Compare/PWM Buffer Functionality Detail

20.3.3.7 Frequency Generation (FRG)

Frequency generation (see Figure 20.17 TIMER Up-count Frequency Generation on page 576) can be achieved in compare mode by:

- Setting the counter in up-count mode
- Enabling buffering of the TOP value.
- Setting the CC channels overflow action to toggle

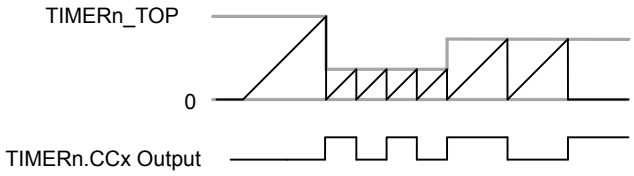


Figure 20.17. TIMER Up-count Frequency Generation

The output frequency is given by Figure 20.18 TIMER Up-count Frequency Generation Equation on page 576

$$f_{FRG} = f_{HFPERCLK\_TIMERn} / [2 \times (PRESC + 1) \times (TOP + 1)]$$

Figure 20.18. TIMER Up-count Frequency Generation Equation

The figure below provides cycle accurate timing and event generation information for frequency generation.

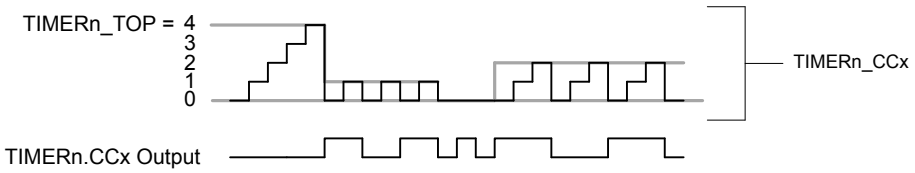


Figure 20.19. TIMER Up-count Frequency Generation Detail

20.3.3.8 Pulse-Width Modulation (PWM)

In PWM mode, TIMERn_CCx_OC is buffered to avoid glitches in the output. The settings in the Compare Output Action configuration bits are ignored in PWM mode and PWM generation is only supported for up-count and up/down-count mode.

20.3.3.9 Up-count (Single-slope) PWM

If the counter is set to up-count and the compare/capture channel is put in PWM mode, single slope PWM output will be generated (see Figure 20.20 TIMER Up-count PWM Generation on page 577). In up-count mode the PWM period is TOP+1 cycles and the PWM output will be high for a number of cycles equal to TIMERn_CCx_OC. This means that a constant high output is achieved by setting TIMERn_CCx_OC to TOP+1 or higher. The PWM resolution (in bits) is then given by Figure 20.21 TIMER Up-count PWM Resolution Equation on page 577.

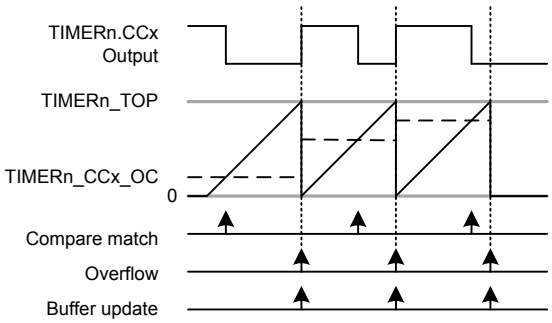


Figure 20.20. TIMER Up-count PWM Generation

$$R_{PWM_{up}} = \log(TOP+1)/\log(2)$$

Figure 20.21. TIMER Up-count PWM Resolution Equation

The PWM frequency is given by Figure 20.22 TIMER Up-count PWM Frequency Equation on page 577:

$$f_{PWM_{up}} = f_{HFPERCLK\_TIMERn} / [(PRESC + 1) \times (TOP + 1)]$$

Figure 20.22. TIMER Up-count PWM Frequency Equation

The high duty cycle is given by Figure 20.23 TIMER Up-count Duty Cycle Equation on page 577

$$DS_{up} = OCx/(TOP+1)$$

Figure 20.23. TIMER Up-count Duty Cycle Equation

The figure below provides cycle accurate timing and event generation information for up-count mode.

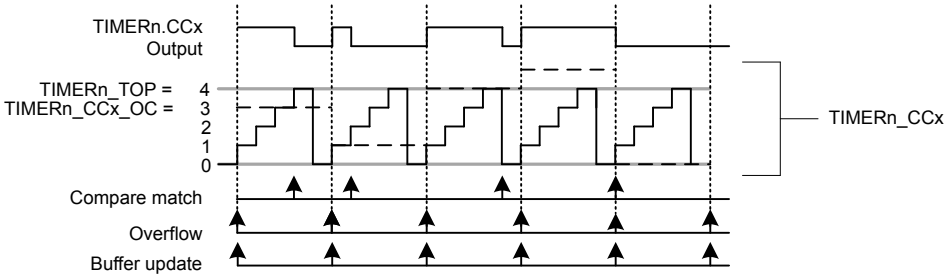


Figure 20.24. TIMER Up-count PWM Generation Detail

20.3.3.10 2x Count Mode (Up-count)

When the timer is set in 2x mode, the TIMER will count up by two for every (prescaled) clock. This will in effect make any odd Top value be rounded down to the closest even number. Similarly, any odd OC value will generate a match on the closest lower even value as shown in Figure 20.25 TIMER CC Out in 2x Mode on page 578

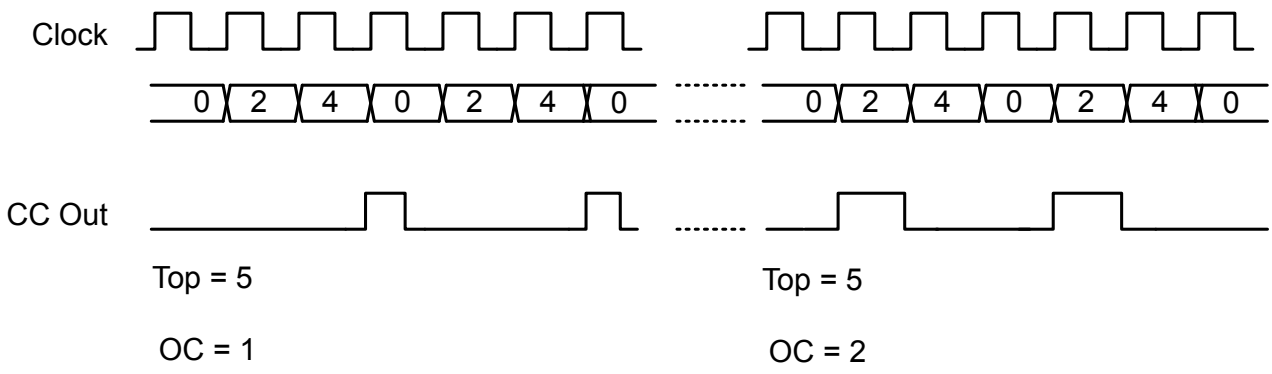


Figure 20.25. TIMER CC Out in 2x Mode

The PWM resolution is given by Figure 20.26 TIMER 2x PWM Resolution Equation on page 578.

$$R_{PWM_{2xmode}} = \log(TOP/2+1)/\log(2)$$

Figure 20.26. TIMER 2x PWM Resolution Equation

The PWM frequency is given by Figure 20.27 TIMER 2x Mode PWM Frequency Equation (Up-count) on page 578:

$$f_{PWM_{2xmode}} = f_{HFPERCLK\_TIMERn} / [(PRESC + 1) \times (\text{floor}(TOP/2)+1)]$$

Figure 20.27. TIMER 2x Mode PWM Frequency Equation (Up-count)

The high duty cycle is given by Figure 20.28 TIMER 2x Mode Duty Cycle Equation on page 578

$$DS_{2xmode} = OCx/((\text{floor}(TOP/2)+1)*2)$$

Figure 20.28. TIMER 2x Mode Duty Cycle Equation

20.3.3.11 Up/Down-count (Dual-slope) PWM

If the counter is set to up-down count and the compare/capture channel is put in PWM mode, dual slope PWM output will be generated by Figure 20.29 TIMER Up/Down-count PWM Generation on page 579. The resolution (in bits) is given by Figure 20.30 TIMER Up/Down-count PWM Resolution Equation on page 579.

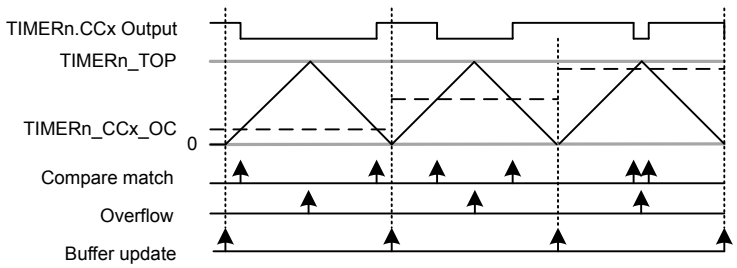


Figure 20.29. TIMER Up/Down-count PWM Generation

$$R_{PWM_{up/down}} = \log(TOP+1)/\log(2)$$

Figure 20.30. TIMER Up/Down-count PWM Resolution Equation

The PWM frequency is given by Figure 20.31 TIMER Up/Down-count PWM Frequency Equation on page 579:

$$f_{PWM_{up/down}} = f_{HFPERCLK\_TIMERn} / (2 \times (PRESC + 1) \times TOP))$$

Figure 20.31. TIMER Up/Down-count PWM Frequency Equation

The high duty cycle is given by Figure 20.32 TIMER Up/Down-count Duty Cycle Equation on page 579

$$DS_{up/down} = OCx/TOP$$

Figure 20.32. TIMER Up/Down-count Duty Cycle Equation

The figure below provides cycle accurate timing and event generation information for up-count mode.

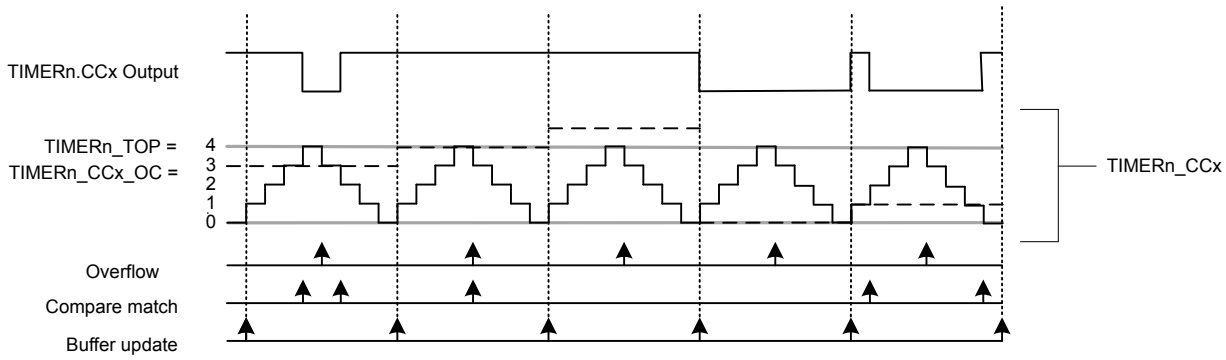


Figure 20.33. TIMER Up/Down-count PWM Generation

20.3.3.12 2x Count Mode (Up/Down-count)

When the timer is set in 2x mode, the TIMER will count up/down by two. This will in effect make any odd Top value be rounded down to the closest even number. Similarly, any odd OC value will generate a match on the closest lower even value as shown in Figure 20.34 TIMER CC Out in 2x mode on page 580

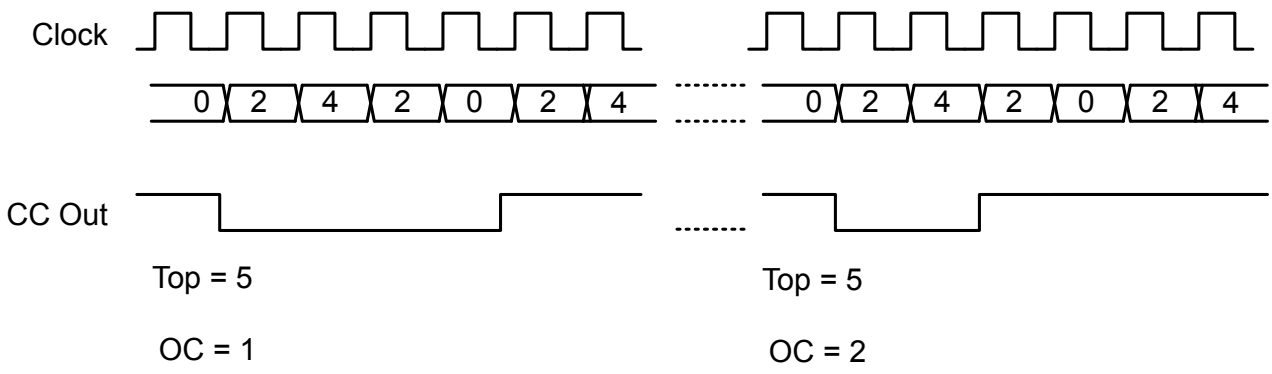


Figure 20.34. TIMER CC Out in 2x mode

Figure 20.35 TIMER 2x PWM Resolution Equation on page 580.

$$R_{PWM_{2xmode}} = \log(TOP/2+1)/\log(2)$$

Figure 20.35. TIMER 2x PWM Resolution Equation

The PWM frequency is given by Figure 20.36 TIMER 2x Mode PWM Frequency Equation (Up/Down-count) on page 580:

$$f_{PWM_{2xmode}} = f_{HFPERCLK\_TIMERn} / (2 \times (PRESC + 1) \times (\text{floor}(TOP/2)))$$

Figure 20.36. TIMER 2x Mode PWM Frequency Equation (Up/Down-count)

The high duty cycle is given by two equations based on the OCx values.Figure 20.37 TIMER 2x Mode Duty Cycle Equation for OCx = 1 or OCx = Even on page 580 and Figure 20.38 TIMER 2x Mode Duty Cycle Equation for all Other OCx = Odd Values on page 580

$$DS_{2xmode} = (OCx*2)/(\text{floor}(TOP/2)*4)$$

Figure 20.37. TIMER 2x Mode Duty Cycle Equation for OCx = 1 or OCx = Even

$$DS_{2xmode} = (OCx*2 - OCx)/(\text{floor}(TOP/2)*4)$$

Figure 20.38. TIMER 2x Mode Duty Cycle Equation for all Other OCx = Odd Values

20.3.3.13 Re-Timing PWM Outputs

PWM outputs are normally synchrous to the TIMER peripheral clock. However for radio applications, it can be desirable to synchronize PWM edges to radio clocks to reduce the interference with RF signalling.

Re-timing is enabled by setting the RETIMEEN bit in TIMERn_CFG to 1. When RETIMEEN is enabled, PWM X2CNT mode should not be enabled. Doing so may result in unpredictable PWM behavior.

Direct re-timing is supported at peripheral clock frequencies up to 50 MHz. For higher peripheral clock frequencies, set the RETIMESEL bit in TIMERn_CFG to 1. This allows PWM outputs to be re-timed at frequencies up to 80 MHz, but will introduce up to 1 $HFPERCLK_{TIMERn}$ cycle of jitter between the PWM outputs.

20.3.3.14 Timer Configuration Lock

To prevent software errors from making changes to the timer configuration, a configuration lock is available. Writing any value but 0xCE80 to LOCKKEY in TIMERn_LOCK will lock writes to TIMERn_CTRL, TIMERn_CFG, TIMERn_CMD, TIMERn_TOP, TIMERn_TOPB, TIMERn_CNT, TIMERn_CCx_CTRL, TIMERn_CCx_CFG, TIMERn_CCx_OC, and TIMERn_CCx_OCB. To unlock the registers, write 0xCE80 to LOCKKEY in TIMERn_LOCK. The value of TIMERLOCKSTATUS in TIMERn_STATUS is 1 when the lock is active, and 0 when the registers are unlocked.

20.3.4 Dead-Time Insertion Unit

Some timer modules include a Dead-Time Insertion unit suitable for motor control applications. Refer to the device data sheet to check which timer instances have this feature. The example settings in this section are for TIMER0, but identical settings can be used for other timers with DTI as well. The Dead-Time Insertion Unit aims to make control of brushless DC (BLDC) motors safer and more efficient by introducing complementary PWM outputs with dead-time insertion and fault handling, see Figure 20.39 TIMER Dead-Time Insertion Unit Overview on page 582.

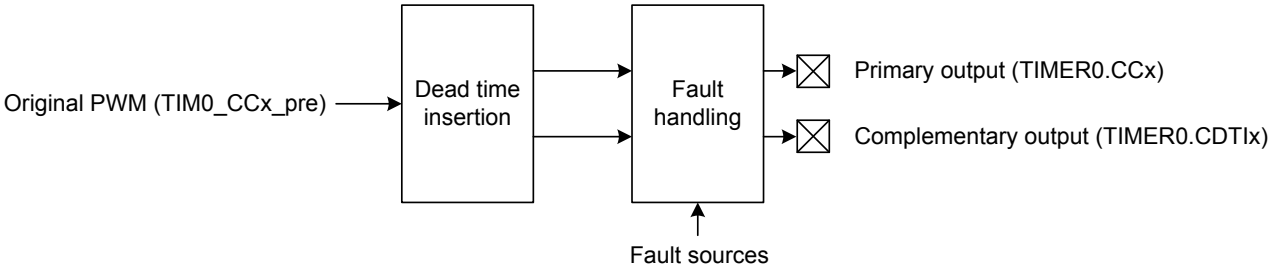


Figure 20.39. TIMER Dead-Time Insertion Unit Overview

When used for motor control, the PWM outputs TIM0_CC0, TIM0_CC1 and TIM0_CC2 are often connected to the high-side transistors of a triple half-bridge setup (UH, VH and WH), and the complementary outputs connected to the respective low-side transistors (UL, VL, WL shown in Figure 20.40 TIMER Triple Half-Bridge on page 582). Transistors used in such a bridge often do not open/close instantaneously, and using the exact complementary inputs for the high and low side of a half-bridge may result in situations where both gates are open. This can give unnecessary current-draw and short circuit the power supply. The DTI unit provides dead-time insertion to deal with this problem.

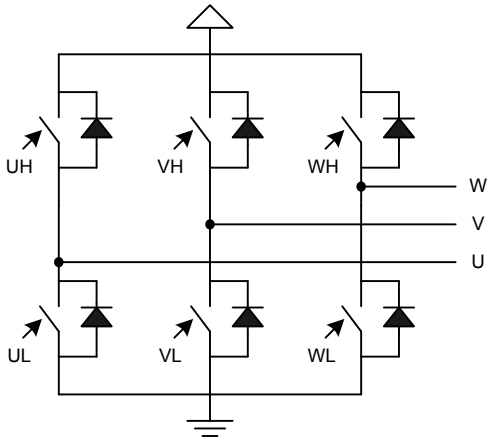


Figure 20.40. TIMER Triple Half-Bridge

For each of the 3 compare-match outputs of TIMER0, an additional complementary output is provided by the DTI unit. These outputs, named TIM0_CDTI0, TIM0_CDTI1 and TIM0_CDTI2 are provided to make control of e.g. 3-channel BLDC or permanent magnet AC (PMAC) motors possible using only a single timer, see Figure 20.41 TIMER Overview of Dead-Time Insertion Block for a Single PWM Channel on page 583.

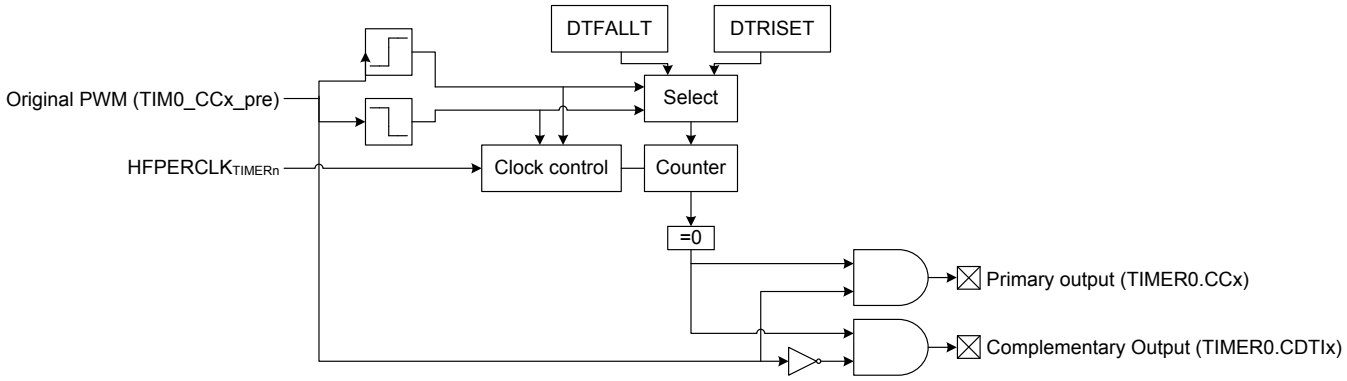


Figure 20.41. TIMER Overview of Dead-Time Insertion Block for a Single PWM Channel

The DTI unit is enabled by setting DTEN in TIMER0_DTCFG. In addition to providing the complementary outputs, the DTI unit then also overrides the compare match outputs from the timer.

The DTI unit gives the rising edges of the PWM outputs and the rising edges of the complementary PWM outputs a configurable time delay. By doing this, the DTI unit introduces a dead-time where both the primary and complementary outputs in a pair are inactive as seen in Figure 20.42 TIMER Polarity of Both Signals are Set as Active-High on page 583.

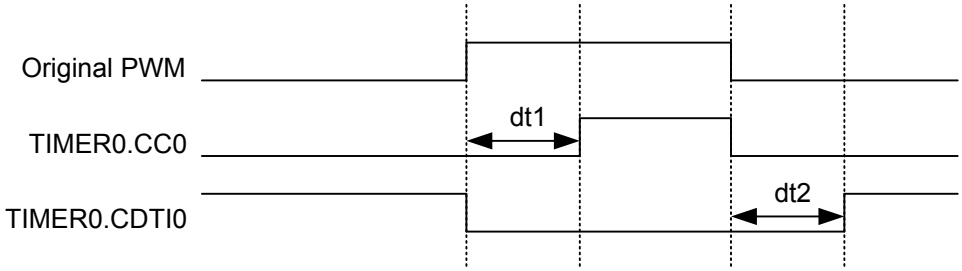


Figure 20.42. TIMER Polarity of Both Signals are Set as Active-High

Dead-time is specified individually for the rising and falling edge of the original PWM. These values are shared across all the three PWM channels of the DTI unit. A single prescaler value is provided for the DTI unit, meaning that both the rising and falling edge dead-times share prescaler value. The prescaler divides the $HFPERCLK_{TIMER0}$ by a configurable factor between 1 and 1024, which is set in the DTPRESC field in TIMER0_DTTIMECFG. The rising and falling edge dead-times are configured in DTRISET and DTFALLT in TIMER0_DTTIMECFG to any number between 1-64 $HFPERCLK_{TIMER0}$ cycles.

The DTAR and DTFATS bits in TIMER0_DTCFG control the DTI output behavior when the timer stops. By default the DTI block stops when the timer is stopped. Setting the DTAR bit will cause the DTI output on channel 0 to continue when the timer is stopped. DTAR effects only channel 0. See 20.3.4.2 PRS Channel as a Source for an example of when this can be used. While in this mode the undivided $HFPERCLK_{TIMER0}$ (DTPRESC=0) is always used regardless of the programmed DTPRESC value in TIMER0_DTTIMECFG. This means that rise and fall dead times are calculated assuming DTPRESC = 0.

When the timer stops, DTI outputs are frozen by default, preserving their last state. To allow the outputs to go to a safe state, program the DTFA field of the TIMER0_DTFCFG register to the safe values and set the DTFATS bitfield in the TIMER0_DTCFG register. Note that when DTAR is also set, DTAR has priority over DTFATS for DTI channel 0 output.

The following table shows the DTI output when the timer is halted.

Table 20.3. DTI Output When Timer Halted

DTAR	DTFATS	State
0	0	frozen
0	1	safe
1	0	running
1	1	running

20.3.4.1 Output Polarity

The value of the primary and complementary outputs in a pair will never be set active at the same time by the DTI unit. The polarity of the outputs can be changed if this is required by the application. The active values of the primary and complementary outputs are set by the DTIPOL and DTCINV bits in the TIMER0_DTCTRL register. The DTIPOL bit of this register specifies the base polarity. If DTIPOL = 0, then the outputs are active-high, and if DTIPOL = 1 they are active-low. The relative phase of the primary and complementary outputs is not changed by DTIPOL, as the polarity of both outputs is changed, see Figure 20.43 TIMER Output Polarities on page 584.

In some applications, it may be required that the primary outputs are active-high, while the complementary outputs are active-low. This can be accomplished by manipulating the DTCINV bit of the TIMER0_DTCTRL register, which inverts the polarity of the complementary outputs relative to the primary outputs. As an example, DTIPOL = 0 and DTCINV = 0 results in outputs with opposite phase and active-high states. Similarly, DTIPOL = 1 and DTCINV = 1 results in outputs with equal phase and the primary output will be active-high while the complementary will be active-low.

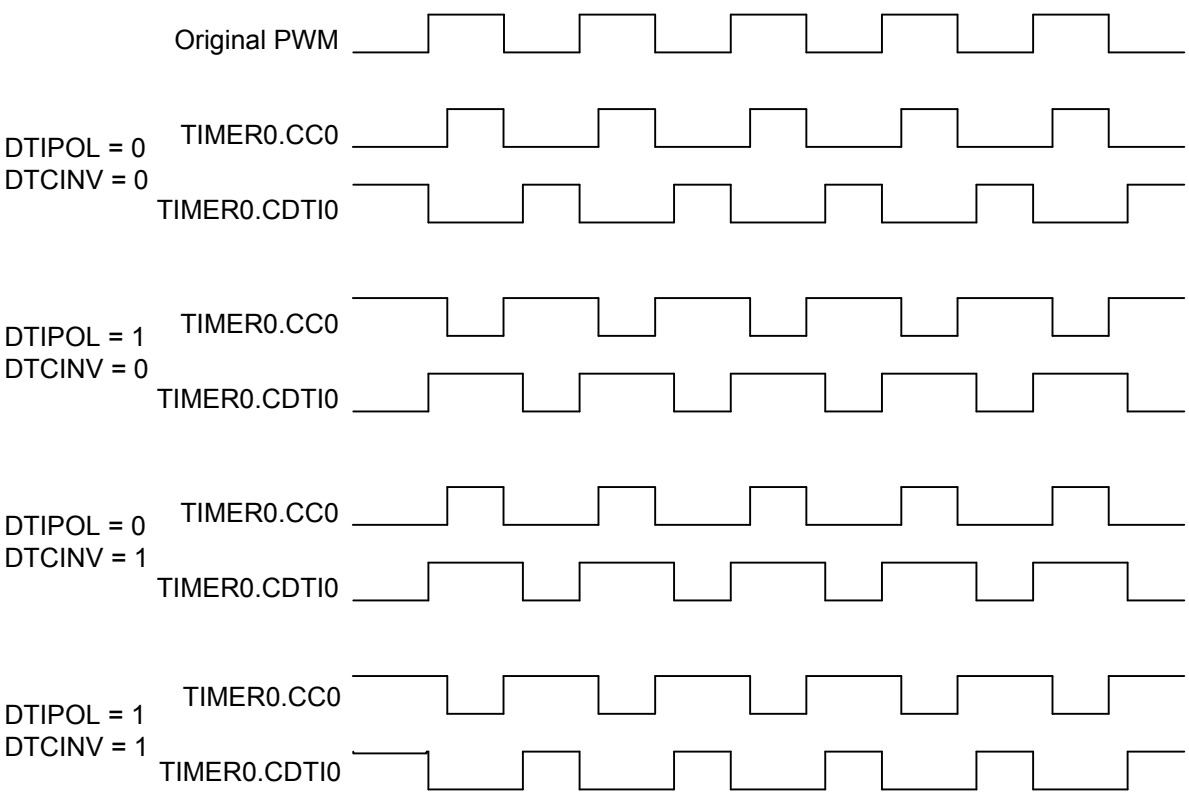


Figure 20.43. TIMER Output Polarities

Output generation on the individual DTI outputs can be disabled by configuring TIMER0_DTOGEN. When output generation on an output is disabled that output will go to and stay in its inactive state.

20.3.4.2 PRS Channel as a Source

A PRS channel can be used as input to the DTI module instead of the PWM output from the timer for DTI channel 0. Setting DTPRSEN in TIMER0_DTCFG will override the source of the first DTI channel, driving TIM0_CC0 and TIM0_CDTI0, with the value on the PRS channel. The rest of the DTI channels will continue to be driven by the PWM output from the timer. The input PRS channel is chosen within the PRS module with PRSSEL in the PRS_CONSUMER_TIMERn_DTI register. Note that the timer must be running even when PRS is used as the DTI source. However, if it is required to keep the DTI channel 0 running even when the timer is stopped, set DTAR in TIMER0_DTCFG. When this bit is set, it uses DTPRESC=0 regardless of the value programmed in DTPRESC in TIMER0_DTTIMECFG.

Note: When using synchronous PRS sources, it is recommended to configure the PRS consumer registers prior to selecting PRS triggering to avoid any false triggers.

The DTI prescaler, set by DTPRESC in TIMER0_DTTIMECFG determines the accuracy with which the DTI can insert dead-time into a PRS signal. The maximum dead-time error equals DTIPRESC+1 clock cycles. With DTIPRESC = 0, the inserted dead-times are therefore accurate, but they may be inaccurate for larger prescaler settings.

20.3.4.3 Fault Handling

The fault handling system of the DTI unit allows the outputs of the DTI unit to be put in a well-defined state in case of a fault. This hardware fault handling system enables a fast reaction to faults, reducing the possibility of damage to the system.

The fault sources which trigger a fault in the DTI module are determined by the bitfields of TIMER0_DTFCFG register. Any combination of the available error sources can be selected:

- PRS source 1, determined by PRSSEL in PRS_CONSUMER_TIMERn_DTIFS1
- PRS source 2, determined by PRSSEL in PRS_CONSUMER_TIMERn_DTIFS2
- Debugger
- Core Lockup
- EM2 or EM3 Entry

One or two PRS channels can be used as an error source. When PRS source 1 is selected as an error source, PRSSEL in PRS_CONSUMER_TIMERn_DTIFS1 determines which PRS channel is used for this source. PRSSEL in PRS_CONSUMER_TIMERn_DTIFS2 determines which PRS channel is selected as PRS source 2. Note that for Core Lockup, the LOCKUPRDIS in RMU_CTRL must be set. Otherwise this will generate a full reset of the chip.

Note: When using synchronous PRS sources, it is recommended to configure the PRS consumer registers prior to selecting PRS triggering to avoid any false triggers.

20.3.4.4 Action on Fault

When a fault occurs, the bit representing the fault source is set in TIMER0_DTFAULT register, and the outputs from the DTI unit are set to a well-defined state. The following options are available, and can be enabled by configuring DTFA in TIMER0_DTFCFG:

- Set outputs to inactive level
- Clear outputs
- Tristate outputs

With the first option enabled, the output state in case of a fault depends on the polarity settings for the individual outputs. An output set to be active high will be set low if a fault is detected, while an output set to be active low will be driven high.

When a fault occurs, the fault source(s) can be read out from TIMER0_DTFAULT register.

Additionally a fault action can also be triggered when the timer stops if DTFATS in TIMER0_DTCFG is set. This allows the DTI output to go to safe state specified by DTFA in TIMER0_DTFCFG when the timer stops. When DTAR and DTFATS in TIMER0_DTCFG are both set, DTI channel 0 keeps running even when the timer stops. This is useful when DTI channel 0 has an input coming from PRS.

20.3.4.5 Exiting Fault State

When a fault is triggered by the PRS system, software intervention is required to re-enable the outputs of the DTI unit. This is done by manually clearing bits in the TIMER0_DTFAULT register. If the fault source as determined by checking TIMER0_DTFAULT is the debugger alone, the outputs can be automatically restarted when the debugger exits. To enable automatic restart set DTDAS in TIMER0_DCTFG. When an automatic restart occurs the DTDBGF bit in TIMER0_DTFAULT will be automatically cleared by hardware. If any other bits in the TIMER0_DTFAULT register are set when the hardware clears DTDBGF the DTI module will not exit the fault state.

20.3.4.6 DTI Configuration Lock

To prevent software errors from making changes to the DTI configuration, a configuration lock is available. Writing any value but 0xCE80 to LOCKKEY in TIMER0_DTLOCK locks writes to registers TIMER0_DTCFG, TIMER0_DTFCFG, TIMER0_DTCTRL, and TIMER0_DTTIMECFG. To unlock the registers, write 0xCE80 to LOCKKEY in TIMER0_DTLOCK. The value of DTILOCKSTATUS in TIMERn_STATUS is 1 when the lock is active, and 0 when the registers are unlocked.

20.3.5 Debug Mode

When the CPU is halted in debug mode, the timer can be configured to either continue to run or to be frozen. This is configured in DEBUGRUN in TIMERn_CFG.

20.3.6 Interrupts, DMA and PRS Output

The timer can generate several type of output events:

- Counter Underflow
- Counter Overflow
- Quadrature Decoder Direction Change
- Compare match or input capture (one per compare/capture channel)

Each of the events has its own interrupt flag. Also, there are interrupt flags for each compare/capture channel which are set on FIFO overflow or underflow in capture mode. FIFO overflow happens when a new capture over-writes an old unread capture in TIMERn_CCx_ICF. FIFO underflow happens when software reads TIMERn_CCx_ICF while the FIFO is empty.

If the interrupt flags are set and the corresponding interrupt enable bits in TIMERn_IEN are set high, the timer will send out an interrupt request. Each of the events may optionally trigger signals to PRS channels. The PRSCONF field in TIMERn_CCx_CFG determines how PRS events are generated. When PRSCONF is set to PULSE, and event will lead to a one $HFPERCLK_{TIMERn}$ cycle high pulse on individual PRS outputs. Setting PRSCONF to LEVEL will make the PRS output follow the compare match output. Interrupts are cleared by setting the corresponding bit in the TIMERn_IFC register.

Each of the events will also set a DMA request when they occur. The different DMA requests are cleared when certain acknowledge conditions are met, see Table 20.4 TIMER DMA Events on page 586. Events which clear the DMA requests do not clear interrupt flags. Software must still manually clear the interrupt flag if interrupts are in use.

If DMACLRACT is set in TIMERn_CFG, the DMA request is cleared when the triggered DMA channel is active, without having to access any timer registers. This is useful in cases where a timer event is used to trigger a DMA transfer in output compare or PWM mode that does not target the OC or OCB registers. DMACLRACT is not applicable in input capture mode.

Table 20.4. TIMER DMA Events

Event	Acknowledge/Clear
Underflow/Overflow	Read or write to TIMERn_CNT or TIMERn_TOPB
CC0 Input Capture - ICFWLFULL0 flag set	ICFEMPTY0 flag set (read FIFO via TIMERn_CC0_ICF)
CC1 Input Capture - ICFWLFULL1 flag set	ICFEMPTY1 flag set (read FIFO via TIMERn_CC1_ICF)
CC2 Input Capture - ICFWLFULL2 flag set	ICFEMPTY2 flag set (read FIFO via TIMERn_CC2_ICF)
CC3 Input Capture - ICFWLFULL3 flag set	ICFEMPTY3 flag set (read FIFO via TIMERn_CC3_ICF)
CC0 Output Compare / PWM - Match event	Write TIMERn_CC0_OC or TIMERn_CC0_OCB
CC1 Output Compare / PWM - Match event	Write TIMERn_CC1_OC or TIMERn_CC1_OCB
CC2 Output Compare / PWM - Match event	Write TIMERn_CC2_OC or TIMERn_CC2_OCB
CC3 Output Compare / PWM - Match event	Write TIMERn_CC3_OC or TIMERn_CC3_OCB

20.3.7 GPIO Input/Output

The TIMn_CCx inputs/outputs and TIMn_CDTIx outputs are accessible as alternate functions through GPIO. Each pin connection can be enabled/disabled separately using the GPIO module control registers. See the device data sheet for the available locations for each signal.

20.4 TIMER Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	TIMER_IPVERSION	R	IP Version ID
0x004	TIMER_CFG	RW CONFIG	Configuration Register
0x008	TIMER_CTRL	RW SYNC	Control Register
0x00C	TIMER_CMD	W SYNC	Command Register
0x010	TIMER_STATUS	RH	Status Register
0x014	TIMER_IF	RWH INTFLAG	Interrupt Flag Register
0x018	TIMER_IEN	RW	Interrupt Enable Register
0x01C	TIMER_TOP	RWH SYNC	Counter Top Value Register
0x020	TIMER_TOPB	RW SYNC	Counter Top Value Buffer Register
0x024	TIMER_CNT	RWH SYNC	Counter Value Register
0x02C	TIMER_LOCK	W	TIMER Configuration Lock Register
0x030	TIMER_EN	RW ENABLE	Module En
0x060	TIMER_CCx_CFG	RW CONFIG	CC Channel Configuration Register
0x064	TIMER_CCx_CTRL	RW SYNC	CC Channel Control Register
0x068	TIMER_CCx_OC	RWH SYNC	OC Channel Value Register
0x070	TIMER_CCx_OCB	RW SYNC	OC Channel Value Buffer Register
0x074	TIMER_CCx_ICF	RH(r)	IC Channel Value Register
0x078	TIMER_CCx_ICOF	RH SYNC	IC Channel Value Overflow Register
0x0E0	TIMER_DTCFG	RW CONFIG	DTI Configuration Register
0x0E4	TIMER_DTTIMECFG	RW CONFIG	DTI Time Configuration Register
0x0E8	TIMER_DTFCFG	RW CONFIG	DTI Fault Configuration Register
0x0EC	TIMER_DTCTRL	RW SYNC	DTI Control Register
0x0F0	TIMER_DTOGEN	RW SYNC	DTI Output Generation Enable Register
0x0F4	TIMER_DTFAULT	RH	DTI Fault Register
0x0F8	TIMER_DTFAULTC	W SYNC	DTI Fault Clear Register
0x0FC	TIMER_DTLOCK	W	DTI Configuration Lock Register
0x1000	TIMER_IPVERSION_SET	R	IP Version ID
0x1004	TIMER_CFG_SET	RW CONFIG	Configuration Register
0x1008	TIMER_CTRL_SET	RW SYNC	Control Register
0x100C	TIMER_CMD_SET	W SYNC	Command Register
0x1010	TIMER_STATUS_SET	RH	Status Register
0x1014	TIMER_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x1018	TIMER_IEN_SET	RW	Interrupt Enable Register
0x101C	TIMER_TOP_SET	RWH SYNC	Counter Top Value Register
0x1020	TIMER_TOPB_SET	RW SYNC	Counter Top Value Buffer Register

Offset	Name	Type	Description
0x1024	TIMER_CNT_SET	RWH SYNC	Counter Value Register
0x102C	TIMER_LOCK_SET	W	TIMER Configuration Lock Register
0x1030	TIMER_EN_SET	RW ENABLE	Module En
0x1060	TIMER_CCx_CFG_SET	RW CONFIG	CC Channel Configuration Register
0x1064	TIMER_CCx_CTRL_SET	RW SYNC	CC Channel Control Register
0x1068	TIMER_CCx_OC_SET	RWH SYNC	OC Channel Value Register
0x1070	TIMER_CCx_OCB_SET	RW SYNC	OC Channel Value Buffer Register
0x1074	TIMER_CCx_ICF_SET	RH(r)	IC Channel Value Register
0x1078	TIMER_CCx_ICOF_SET	RH SYNC	IC Channel Value Overflow Register
0x10E0	TIMER_DTCFG_SET	RW CONFIG	DTI Configuration Register
0x10E4	TIMER_DTTIMECFG_SET	RW CONFIG	DTI Time Configuration Register
0x10E8	TIMER_DTFCFG_SET	RW CONFIG	DTI Fault Configuration Register
0x10EC	TIMER_DTCTRL_SET	RW SYNC	DTI Control Register
0x10F0	TIMER_DTOGEN_SET	RW SYNC	DTI Output Generation Enable Register
0x10F4	TIMER_DTFAULT_SET	RH	DTI Fault Register
0x10F8	TIMER_DTFAULTC_SET	W SYNC	DTI Fault Clear Register
0x10FC	TIMER_DTLOCK_SET	W	DTI Configuration Lock Register
0x2000	TIMER_IPVERSION_CLR	R	IP Version ID
0x2004	TIMER_CFG_CLR	RW CONFIG	Configuration Register
0x2008	TIMER_CTRL_CLR	RW SYNC	Control Register
0x200C	TIMER_CMD_CLR	W SYNC	Command Register
0x2010	TIMER_STATUS_CLR	RH	Status Register
0x2014	TIMER_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x2018	TIMER_IEN_CLR	RW	Interrupt Enable Register
0x201C	TIMER_TOP_CLR	RWH SYNC	Counter Top Value Register
0x2020	TIMER_TOPB_CLR	RW SYNC	Counter Top Value Buffer Register
0x2024	TIMER_CNT_CLR	RWH SYNC	Counter Value Register
0x202C	TIMER_LOCK_CLR	W	TIMER Configuration Lock Register
0x2030	TIMER_EN_CLR	RW ENABLE	Module En
0x2060	TIMER_CCx_CFG_CLR	RW CONFIG	CC Channel Configuration Register
0x2064	TIMER_CCx_CTRL_CLR	RW SYNC	CC Channel Control Register
0x2068	TIMER_CCx_OC_CLR	RWH SYNC	OC Channel Value Register
0x2070	TIMER_CCx_OCB_CLR	RW SYNC	OC Channel Value Buffer Register
0x2074	TIMER_CCx_ICF_CLR	RH(r)	IC Channel Value Register
0x2078	TIMER_CCx_ICOF_CLR	RH SYNC	IC Channel Value Overflow Register
0x20E0	TIMER_DTCFG_CLR	RW CONFIG	DTI Configuration Register
0x20E4	TIMER_DTTIMECFG_CLR	RW CONFIG	DTI Time Configuration Register

Offset	Name	Type	Description
0x20E8	TIMER_DTFCFG_CLR	RW CONFIG	DTI Fault Configuration Register
0x20EC	TIMER_DTCTRL_CLR	RW SYNC	DTI Control Register
0x20F0	TIMER_DTOGEN_CLR	RW SYNC	DTI Output Generation Enable Register
0x20F4	TIMER_DTFAULT_CLR	RH	DTI Fault Register
0x20F8	TIMER_DTFAULTC_CLR	W SYNC	DTI Fault Clear Register
0x20FC	TIMER_DTLOCK_CLR	W	DTI Configuration Lock Register
0x3000	TIMER_IPVERSION_TGL	R	IP Version ID
0x3004	TIMER_CFG_TGL	RW CONFIG	Configuration Register
0x3008	TIMER_CTRL_TGL	RW SYNC	Control Register
0x300C	TIMER_CMD_TGL	W SYNC	Command Register
0x3010	TIMER_STATUS_TGL	RH	Status Register
0x3014	TIMER_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x3018	TIMER_IEN_TGL	RW	Interrupt Enable Register
0x301C	TIMER_TOP_TGL	RWH SYNC	Counter Top Value Register
0x3020	TIMER_TOPB_TGL	RW SYNC	Counter Top Value Buffer Register
0x3024	TIMER_CNT_TGL	RWH SYNC	Counter Value Register
0x302C	TIMER_LOCK_TGL	W	TIMER Configuration Lock Register
0x3030	TIMER_EN_TGL	RW ENABLE	Module En
0x3060	TIMER_CCx_CFG_TGL	RW CONFIG	CC Channel Configuration Register
0x3064	TIMER_CCx_CTRL_TGL	RW SYNC	CC Channel Control Register
0x3068	TIMER_CCx_OC_TGL	RWH SYNC	OC Channel Value Register
0x3070	TIMER_CCx_OCB_TGL	RW SYNC	OC Channel Value Buffer Register
0x3074	TIMER_CCx_ICF_TGL	RH(r)	IC Channel Value Register
0x3078	TIMER_CCx_ICOF_TGL	RH SYNC	IC Channel Value Overflow Register
0x30E0	TIMER_DTCFG_TGL	RW CONFIG	DTI Configuration Register
0x30E4	TIMER_DTTIMECFG_TGL	RW CONFIG	DTI Time Configuration Register
0x30E8	TIMER_DTFCFG_TGL	RW CONFIG	DTI Fault Configuration Register
0x30EC	TIMER_DTCTRL_TGL	RW SYNC	DTI Control Register
0x30F0	TIMER_DTOGEN_TGL	RW SYNC	DTI Output Generation Enable Register
0x30F4	TIMER_DTFAULT_TGL	RH	DTI Fault Register
0x30F8	TIMER_DTFAULTC_TGL	W SYNC	DTI Fault Clear Register
0x30FC	TIMER_DTLOCK_TGL	W	DTI Configuration Lock Register

20.5 TIMER Register Description

20.5.1 TIMER_IPVERSION - IP Version ID

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x1																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x1	R	**IP Version ID**
	The read only IPVERSION field gives the version for this module. There may be minor software changes required for modules with different values of IPVERSION.			

20.5.2 TIMER_CFG - Configuration Register

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0x0										0x0	0x0				0x0	0x0	0x0	0x0		0x0	0x0	0x0	0x0	0x0		0x0	
Access					RW										RW	RW				RW	RW	RW	RW		RW	RW	RW	RW	RW		RW	
Name					PRESC										RSSCOIST	ATI				RETIMESEL	DISSYNCOUT	RETIMEEN	CLKSEL		DMACLRACT	DEBUGRUN	QDM	OSMEN	SYNC		MODE	

Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27:18	PRESC	0x0	RW	**Prescaler Setting**

These bits select the prescaling factor for the counter clock. The selected timer clock will be divided by PRESC+1 before clocking the counter. The following modes are provided for easier software porting from Series 0 or Series 1 devices. However, the prescaler is not limited to these options.

Value	Mode	Description
0	DIV1	No prescaling
1	DIV2	Prescale by 2
3	DIV4	Prescale by 4
7	DIV8	Prescale by 8
15	DIV16	Prescale by 16
31	DIV32	Prescale by 32
63	DIV64	Prescale by 64
127	DIV128	Prescale by 128
255	DIV256	Prescale by 256
511	DIV512	Prescale by 512
1023	DIV1024	Prescale by 1024

17	RSSCOIST	0x0	RW	**Reload-Start Sets COIST**

When enabled, compare output is set to COIST value on a Reload-Start event.

16	ATI	0x0	RW	**Always Track Inputs**

Enabling ATI makes CCPOL always track the polarity of the inputs.

15:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12	RETIMESEL	0x0	RW	**PWM output retime select**

When RETIMEEN is set, the PWM output stage will be re-timed to synchronize edges with radio clocks and reduce RF interference. This will introduce up to 1 cycle of clock jitter between PWM outputs.

11	DISSYNCOUT	0x0	RW	**Disable Timer Start/Stop/Reload output**

When this bit is set, the Timer does not start/stop/reload other timers with SYNC bit set.

Bit	Name	Reset	Access	Description
	Value	Mode		Description
	0	EN		Timer can start/stop/reload other timers with SYNC bit set
	1	DIS		Timer cannot start/stop/reload other timers with SYNC bit set
10	RETIMEEN	0x0	RW	**PWM output retimed enable**
	Enable retiming of PWM output.			
	Value	Mode		Description
	0	DISABLE		PWM outputs are not re-timed.
	1	ENABLE		PWM outputs are re-timed.
9:8	CLKSEL	0x0	RW	**Clock Source Select**
	These bits select the clock source for the timer.			
	Value	Mode		Description
	0	PRESCEM01GRPACLK		Prescaled EM01GRPACLK
	1	CC1		Compare/Capture Channel 1 Input
	2	TIMEROUF		Timer is clocked by underflow(down-count) or overflow(up-count) in the lower numbered neighbor Timer
7	DMACLRACT	0x0	RW	**DMA Request Clear on Active**
	When this bit is set, the DMA requests are cleared when the corresponding DMA channel is active. This enables the timer DMA requests to be cleared without accessing the timer.			
6	DEBUGRUN	0x0	RW	**Debug Mode Run Enable**
	Set this bit to enable timer to run in debug mode.			
	Value	Mode		Description
	0	HALT		Timer is halted in debug mode
	1	RUN		Timer is running in debug mode
5	QDM	0x0	RW	**Quadrature Decoder Mode Selection**
	This bit sets the mode for the quadrature decoder.			
	Value	Mode		Description
	0	X2		X2 mode selected
	1	X4		X4 mode selected
4	OSMEN	0x0	RW	**One-shot Mode Enable**
	Enable/disable one shot mode.			
3	SYNC	0x0	RW	**Timer Start/Stop/Reload Synchronization**
	When this bit is set, the Timer is started/stopped/reloaded by start/stop/reload commands in the other timers.			
	Value	Mode		Description
	0	DISABLE		Timer operation is unaffected by other timers.

Bit	Name	Reset	Access	Description
	1	ENABLE		Timer may be started, stopped and re-loaded from other timer instances.
2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	MODE	0x0	RW	**Timer Mode**

These bits set the counting mode for the Timer. Note, when Quadrature Decoder Mode is selected (MODE = 'b11), the CLKSEL is don't care. The Timer is clocked by the Decoder Mode clock output.

Value	Mode	Description
0	UP	Up-count mode
1	DOWN	Down-count mode
2	UPDOWN	Up/down-count mode
3	QDEC	Quadrature decoder mode

20.5.3 TIMER_CTRL - Control Register

Offset	Bit Position																															
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0		0x0	
Access																												RW	RW		RW	
Name																												X2CNT	FALLA		RISEA	

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	X2CNT	0x0	RW	**2x Count Mode**
	Enable 2x count mode			
3:2	FALLA	0x0	RW	**Timer Falling Input Edge Action**
	These bits select the action taken in the counter when a falling edge occurs on the input.			

Value	Mode	Description
0	NONE	No action
1	START	Start counter without reload
2	STOP	Stop counter without reload
3	RELOADSTART	Reload and start counter

1:0	RISEA	0x0	RW	**Timer Rising Input Edge Action**
	These bits select the action taken in the counter when a rising edge occurs on the input.			

Value	Mode	Description
0	NONE	No action
1	START	Start counter without reload
2	STOP	Stop counter without reload
3	RELOADSTART	Reload and start counter

20.5.4 TIMER_CMD - Command Register

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															W(nB)	W(nB)
Name																															STOP	START

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	STOP	0x0	W(nB)	**Stop Timer**
	Write a 1 to this bit to stop timer			
0	START	0x0	W(nB)	**Start Timer**
	Write a 1 to this bit to start timer			

20.5.5 TIMER_STATUS - Status Register

Offset	Bit Position																														
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset						0x0	0x0	0x0						0x0	0x0	0x0						0x0	0x0	0x0		0x0	0x0	0x0		0x0	0x0	0x0
Access						R	R	R						R	R	R						R	R	R		R	R	R		R	R	R
Name						CCPOL2	CCPOL1	CCPOL0						ICFEMPTY2	ICFEMPTY1	ICFEMPTY0						OCBV2	OCBV1	OCBV0		SYNCBUSY	DTILOCKSTATUS	TIMERLOCKSTATUS		TOPBV	DIR	RUNNING

Bit	Name	Reset	Access	Description
31:27	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
26	CCPOL2	0x0	R	**Compare/Capture Polarity**
	In Input Capture mode, this bit indicates the polarity of the edge that triggered capture in TIMERn_CCx_CCV. In Compare/PWM mode, this bit indicates the polarity of the selected input to CC channel x. These bits are cleared when CCMODE is written to 0b00 (Off).			
	Value	Mode		Description
	0	LOWRISE		CCx polarity low level/rising edge
	1	HIGHFALL		CCx polarity high level/falling edge
25	CCPOL1	0x0	R	**Compare/Capture Polarity**
	In Input Capture mode, this bit indicates the polarity of the edge that triggered capture in TIMERn_CCx_CCV. In Compare/PWM mode, this bit indicates the polarity of the selected input to CC channel x. These bits are cleared when CCMODE is written to 0b00 (Off).			
	Value	Mode		Description
	0	LOWRISE		CCx polarity low level/rising edge
	1	HIGHFALL		CCx polarity high level/falling edge
24	CCPOL0	0x0	R	**Compare/Capture Polarity**
	In Input Capture mode, this bit indicates the polarity of the edge that triggered capture in TIMERn_CCx_CCV. In Compare/PWM mode, this bit indicates the polarity of the selected input to CC channel x. These bits are cleared when CCMODE is written to 0b00 (Off).			
	Value	Mode		Description
	0	LOWRISE		CCx polarity low level/rising edge
	1	HIGHFALL		CCx polarity high level/falling edge
23:19	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
18	ICFEMPTY2	0x0	R	**Input capture fifo empty**
	Set when input capture FIFO is empty			

Bit	Name	Reset	Access	Description
17	ICFEMPTY1	0x0	R	**Input capture fifo empty**
	Set when input capture FIFO is empty			
16	ICFEMPTY0	0x0	R	**Input capture fifo empty**
	Set when input capture FIFO is empty			
15:11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10	OCBV2	0x0	R	**Output Compare Buffer Valid**
	This field indicates that the TIMERn_CCx_CCVB registers contain data which have not been written to TIMERn_CCx_CCV. These bits are only used in OUTPUTCOMPARE or PWM mode and are cleared when CCMODE is written to 0b00 (Off).			
9	OCBV1	0x0	R	**Output Compare Buffer Valid**
	This field indicates that the TIMERn_CCx_CCVB registers contain data which have not been written to TIMERn_CCx_CCV. These bits are only used in OUTPUTCOMPARE or PWM mode and are cleared when CCMODE is written to 0b00 (Off).			
8	OCBV0	0x0	R	**Output Compare Buffer Valid**
	This field indicates that the TIMERn_CCx_CCVB registers contain data which have not been written to TIMERn_CCx_CCV. These bits are only used in OUTPUTCOMPARE or PWM mode and are cleared when CCMODE is written to 0b00 (Off).			
7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6	SYNCBUSY	0x0	R	**Sync Busy**
	Indicates synchronization ongoing			
5	DTILOCKSTATUS	0x0	R	**DTI lock status**
	Indicates current status of DTI lock			

Value	Mode	Description
0	UNLOCKED	DTI registers are unlocked
1	LOCKED	DTI registers are locked

4	TIMERLOCKSTATUS	0x0	R	**Timer lock status**
	Indicates current status of Timer lock			

Value	Mode	Description
0	UNLOCKED	TIMER registers are unlocked
1	LOCKED	TIMER registers are locked

3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	TOPBV	0x0	R	**TOP Buffer Valid**
	This indicates that TIMERn_TOPB contains valid data that has not been written to TIMERn_TOP. This bit is also cleared when TIMERn_TOP is written.			
1	DIR	0x0	R	**Direction**
	Indicates count direction.			

Value	Mode	Description

Bit	Name	Reset	Access	Description
	0	UP		Counting up
	1	DOWN		Counting down
0	RUNNING	0x0	R	**Running**
	Indicates if timer is running or not.			

20.5.6 TIMER_IF - Interrupt Flag Register

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset						0x0	0x0	0x0		0x0	0x0	0x0		0x0	0x0	0x0										0x0	0x0	0x0		0x0	0x0	0x0
Access						RW	RW	RW		RW	RW	RW		RW	RW	RW										RW	RW	RW		RW	RW	RW
Name						ICFUF2	ICFUF1	ICFUF0		ICFOF2	ICFOF1	ICFOF0		ICFWLFULL2	ICFWLFULL1	ICFWLFULL0										CC2	CC1	CC0		DIRCHG	UF	OF

Bit	Name	Reset	Access	Description
31:27	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
26	ICFUF2	0x0	RW	**Input capture FIFO underflow**
	Indicates that software tried to read an empty FIFO on channel 2.			
25	ICFUF1	0x0	RW	**Input capture FIFO underflow**
	Indicates that software tried to read an empty FIFO on channel 1.			
24	ICFUF0	0x0	RW	**Input capture FIFO underflow**
	Indicates that software tried to read an empty FIFO on channel 0.			
23	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
22	ICFOF2	0x0	RW	**Input Capture FIFO overflow**
	Indicates that input capture FIFO for channel 2 has overflown, and a prior captured value was lost. The latest captured value can be read from the ICOF register.			
21	ICFOF1	0x0	RW	**Input Capture FIFO overflow**
	Indicates that input capture FIFO for channel 1 has overflown, and a prior captured value was lost. The latest captured value can be read from the ICOF register.			
20	ICFOF0	0x0	RW	**Input Capture FIFO overflow**
	Indicates that input capture FIFO for channel 0 has overflown, and a prior captured value was lost. The latest captured value can be read from the ICOF register.			
19	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
18	ICFWLFULL2	0x0	RW	**Input Capture Watermark Level Full**
	This bit indicates that the Input capture FIFO watermark for channel 2 has been exceeded.			
17	ICFWLFULL1	0x0	RW	**Input Capture Watermark Level Full**
	This bit indicates that the Input capture FIFO watermark for channel 1 has been exceeded.			
16	ICFWLFULL0	0x0	RW	**Input Capture Watermark Level Full**
	This bit indicates that the Input capture FIFO watermark for channel 0 has been exceeded.			
15:7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6	CC2	0x0	RW	**Capture Compare Channel 2 Interrupt Flag**

Bit	Name	Reset	Access	Description
	In INPUT CAPTURE mode this bit indicates that a new Capture event has taken place. In OUTPUTCOMPARE or PWM mode this bit indicates that a match event has taken place			
5	CC1	0x0	RW	**Capture Compare Channel 1 Interrupt Flag**
	In INPUT CAPTURE mode this bit indicates that a new Capture event has taken place. In OUTPUTCOMPARE or PWM mode this bit indicates that a match event has taken place			
4	CC0	0x0	RW	**Capture Compare Channel 0 Interrupt Flag**
	In INPUT CAPTURE mode this bit indicates that a new Capture event has taken place. In OUTPUTCOMPARE or PWM mode this bit indicates that a match event has taken place			
3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	DIRCHG	0x0	RW	**Direction Change Detect Interrupt Flag**
	This bit is set when count direction changes. Set only in Quadrature Decoder mode			
1	UF	0x0	RW	**Underflow Interrupt Flag**
	This bit indicates that there has been an underflow.			
0	OF	0x0	RW	**Overflow Interrupt Flag**
	This bit indicates that there has been an overflow.			

20.5.7 TIMER_IEN - Interrupt Enable Register

Offset	Bit Position																														
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset						0x0	0x0	0x0		0x0	0x0	0x0		0x0	0x0	0x0										0x0	0x0	0x0		0x0	0x0	0x0
Access						RW	RW	RW		RW	RW	RW		RW	RW	RW										RW	RW	RW		RW	RW	RW
Name						ICFUF2	ICFUF1	ICFUF0		ICFOF2	ICFOF1	ICFOF0		ICFWLFULL2	ICFWLFULL1	ICFWLFULL0										CC2	CC1	CC0		DIRCHG	UF	OF

Bit	Name	Reset	Access	Description
31:27	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
26	ICFUF2	0x0	RW	**ICFUF2 Interrupt Enable**
	Enable/Disable the ICFUF2 interrupt			
25	ICFUF1	0x0	RW	**ICFUF1 Interrupt Enable**
	Enable/Disable the ICFUF1 interrupt			
24	ICFUF0	0x0	RW	**ICFUF0 Interrupt Enable**
	Enable/Disable the ICFUF0 interrupt			
23	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
22	ICFOF2	0x0	RW	**ICFOF2 Interrupt Enable**
	Enable/Disable the ICFOF2 interrupt			
21	ICFOF1	0x0	RW	**ICFOF1 Interrupt Enable**
	Enable/Disable the ICFOF1 interrupt			
20	ICFOF0	0x0	RW	**ICFOF0 Interrupt Enable**
	Enable/Disable the ICFOF0 interrupt			
19	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
18	ICFWLFULL2	0x0	RW	**ICFWLFULL2 Interrupt Enable**
	Enable/Disable the ICFWLFULL2 interrupt			
17	ICFWLFULL1	0x0	RW	**ICFWLFULL1 Interrupt Enable**
	Enable/Disable the ICFWLFULL1 interrupt			
16	ICFWLFULL0	0x0	RW	**ICFWLFULL0 Interrupt Enable**
	Enable/Disable the ICFWLFULL0 interrupt			
15:7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6	CC2	0x0	RW	**CC2 Interrupt Enable**
	Enable/Disable the CC2 interrupt			
5	CC1	0x0	RW	**CC1 Interrupt Enable**

Bit	Name	Reset	Access	Description
	Enable/Disable the CC1 interrupt			
4	CC0	0x0	RW	**CC0 Interrupt Enable**
	Enable/Disable the CC0 interrupt			
3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	DIRCHG	0x0	RW	**Direction Change Detect Interrupt Enable**
	Enable/Disable the DIRCHG interrupt			
1	UF	0x0	RW	**Underflow Interrupt Enable**
	Enable/Disable the UF interrupt			
0	OF	0x0	RW	**Overflow Interrupt Enable**
	Enable/Disable the OF interrupt			

20.5.8 TIMER_TOP - Counter Top Value Register

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0xFFFF																															
Access	RW																															
Name	TOP																															

Bit	Name	Reset	Access	Description
31:0	TOP	0xFFFF	RW	**Counter Top Value**
	These bits hold the TOP value for the counter			

20.5.9 TIMER_TOPB - Counter Top Value Buffer Register

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	TOPB																															

Bit	Name	Reset	Access	Description
31:0	TOPB	0x0	RW	**Counter Top Buffer Register**
	These bits hold the TOP buffer value.			

20.5.10 TIMER_CNT - Counter Value Register

Offset	Bit Position																															
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	CNT																															

Bit	Name	Reset	Access	Description
31:0	CNT	0x0	RW	**Counter Value**
	These bits hold the counter value.			

20.5.11 TIMER_LOCK - TIMER Configuration Lock Register

Offset	Bit Position																															
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	W															
Name																	LOCKKEY															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LOCKKEY	0x0	W	**Timer Lock Key**
	Write any other value than the unlock code to lock TIMERn_CTRL, TIMERn_CFG, TIMERn_CMD, TIMERn_TOP, TIMERn_CNT, TIMERn_CCx_CTRL, TIMERn_CCx_CFG, and TIMERn_CCx_OC from editing. Write the unlock code to unlock these registers.			

Value	Mode	Description
52864	UNLOCK	Write to unlock TIMER registers

20.5.12 TIMER_EN - Module En

Offset	Bit Position																													
0x030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	RW
Name																															DISABLING	EN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DISABLING	0x0	R	**Disablement busy status** When EN is cleared, DISABLING status is set immediately, and cleared when disablement finishes. Disablement resets peripheral cores and not APB registers except hardware updated registers such as INTFLAGs and FIFO
0	EN	0x0	RW	**Timer Module Enable** The ENABLE bit enables the module. Software should write to CONFIG type registers before setting the ENABLE bit. Software should write to SYNC type registers only after setting the ENABLE bit.

20.5.13 TIMER_CCx_CFG - CC Channel Configuration Register

Offset	Bit Position																															
0x060	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset											0x0	0x0	0x0	0x0														0x0			0x0	
Access											RW	RW	RW	RW														RW			RW	
Name											ICFWL	FILT	PRSCONF	INSEL														COIST			MODE	

Bit	Name	Reset	Access	Description
31:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21	ICFWL	0x0	RW	**Input Capture FIFO watermark level**
	Sets the watermark level for generation of the ICFWLFULL interrupt and DMA requests. ICFWLFULL will be set and DMA requests may be generated if the number of free FIFO entries is less than or equal to ICFWL.			
20	FILT	0x0	RW	**Digital Filter**
	Enable digital filter.			

Value	Mode	Description
0	DISABLE	Digital Filter Disabled
1	ENABLE	Digital Filter Enabled

Bit	Name	Reset	Access	Description
19	PRSCONF	0x0	RW	**PRS Configuration**
	Select PRS pulse or level for PRS output.			

Value	Mode	Description
0	PULSE	Each CC event will generate a one EM01GRPACLK cycle high pulse
1	LEVEL	The PRS channel will follow CC out

Bit	Name	Reset	Access	Description
18:17	INSEL	0x0	RW	**Input Selection**
	Select Compare/Capture channel input.			

Value	Mode	Description
0	PIN	TIMERnCCx pin is selected
1	PRSSYNC	Synchornous PRS selected
2	PRSASYNCLEVEL	Asynchronous Level PRS selected
3	PRSASYNCPULSE	Asynchronous Pulse PRS selected

Bit	Name	Reset	Access	Description
16:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	COIST	0x0	RW	**Compare Output Initial State**

Bit	Name	Reset	Access	Description
	This bit is only used in Output Compare and PWM mode. When this bit is set in Compare or PWM mode,the output is set high when the counter is disabled. When counting resumes, this value will represent the initial value for the output. If the bit is cleared, the output will be cleared when the counter is disabled.			
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	MODE	0x0	RW	**CC Channel Mode**

These bits select the mode for Compare/Capture channel.

Value	Mode	Description
0	OFF	Compare/Capture channel turned off
1	INPUTCAPTURE	Input Capture
2	OUTPUTCOMPARE	Output Compare
3	PWM	Pulse-Width Modulation

20.5.14 TIMER_CCx_CTRL - CC Channel Control Register

Offset	Bit Position																													
0x064	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0x0		0x0												0x0		0x0		0x0							0x0		
Access					RW		RW												RW		RW		RW							RW		
Name					ICEVCTRL		ICEDGE												CUFOA		COFOA		CMOA							OUTINV		

Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27:26	ICEVCTRL	0x0	RW	**Input Capture Event Control**

These bits control when a Compare/Capture PRS output pulse and interrupt flag is set. DMA request however is set on every capture.

Value	Mode	Description
0	EVERYEDGE	PRS output pulse and interrupt flag set on every capture
1	EVERYSECONDEDGE	PRS output pulse and interrupt flag set on every second capture
2	RISING	PRS output pulse and interrupt flag set on rising edge only (if ICEDGE = BOTH)
3	FALLING	PRS output pulse and interrupt flag set on falling edge only (if ICEDGE = BOTH)

25:24	ICEDGE	0x0	RW	**Input Capture Edge Select**

These bits control which edges the edge detector triggers on. The output is used for input capture and external clock input.

Value	Mode	Description
0	RISING	Rising edges detected
1	FALLING	Falling edges detected
2	BOTH	Both edges detected
3	NONE	No edge detection, signal is left as it is

23:14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13:12	CUFOA	0x0	RW	**Counter Underflow Output Action**

Select output action on counter underflow.

Value	Mode	Description
0	NONE	No action on counter underflow
1	TOGGLE	Toggle output on counter underflow
2	CLEAR	Clear output on counter underflow
3	SET	Set output on counter underflow

Bit	Name	Reset	Access	Description
11:10	COFOA	0x0	RW	**Counter Overflow Output Action**
	Select output action on counter overflow.			

Value	Mode	Description
0	NONE	No action on counter overflow
1	TOGGLE	Toggle output on counter overflow
2	CLEAR	Clear output on counter overflow
3	SET	Set output on counter overflow

9:8	CMOA	0x0	RW	**Compare Match Output Action**
	Select output action on compare match.			

Value	Mode	Description
0	NONE	No action on compare match
1	TOGGLE	Toggle output on compare match
2	CLEAR	Clear output on compare match
3	SET	Set output on compare match

7:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	OUTINV	0x0	RW	**Output Invert**
	Setting this bit inverts the output from the CC channel (Output compare or PWM mode).			
1:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

20.5.15 TIMER_CCx_OC - OC Channel Value Register

Offset	Bit Position																															
0x068	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	OC																															

Bit	Name	Reset	Access	Description
31:0	OC	0x0	RW	**Output Compare Value**
	This fields holds the output compare value			

20.5.16 TIMER_CCx_OCB - OC Channel Value Buffer Register

Offset	Bit Position																													
0x070	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	OCB																															

Bit	Name	Reset	Access	Description
31:0	OCB	0x0	RW	**Output Compare Value Buffer**
	This field holds the Output Compare buffer value which will be written to TIMERn_CCx_OC on an update event if TIMERn_CCx_OCB contains valid data			

20.5.17 TIMER_CCx_ICF - IC Channel Value Register

Offset	Bit Position																													
0x074	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R(r)																															
Name	ICF																															

Bit	Name	Reset	Access	Description
31:0	ICF	0x0	R(r)	**Input Capture FIFO**
	This FIFO holds captured values in input capture mode. Reading this register will pop the oldest unread value from the FIFO.			

20.5.18 TIMER_CCx_ICOF - IC Channel Value Overflow Register

Offset	Bit Position																													
0x078	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	ICOF																															

Bit	Name	Reset	Access	Description
31:0	ICOF	0x0	R	**Input Capture FIFO Overflow**
	This register always contains the most recent input capture value. If the input capture FIFO is full and a new capture occurs, this register will be updated and the previous caputre value is over-written.			

20.5.19 TIMER_DTCFG - DTI Configuration Register

Offset	Bit Position																													
0x0E0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																					0x0	0x0	0x0								0x0	0x0
Access																					RW	RW	RW								RW	RW
Name																					DTPRSEN	DTFATS	DTAR								DTDAS	DTEN

Bit	Name	Reset	Access	Description
31:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11	DTPRSEN	0x0	RW	**DTI PRS Source Enable**
	Enable/disable PRS as DTI input.			
10	DTFATS	0x0	RW	**DTI Fault Action on Timer Stop**
	When Timer stops, DTI block outputs go to safe state as programmed in DTFA field of TIMERn_DTFC register. However, when DTAR is also set,DTAR having higher priority allows channel0 to output the incoming PRS input while the other channels go to safe state			
9	DTAR	0x0	RW	**DTI Always Run**
	This is used only for DTI channel 0. It Allows DTI channel 0 to keep running even when the timer is stopped. This is useful when its input source is PRS. However, here the undivided peripheral clock is always used regardless of the programmed value in DTPRESC.			
8:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DTDAS	0x0	RW	**DTI Automatic Start-up Functionality**
	Configure DTI restart on debugger exit.			

Value	Mode	Description
0	NORESTART	No DTI restart on debugger exit
1	RESTART	DTI restart on debugger exit

0	DTEN	0x0	RW	**DTI Enable**
	Enable/disable DTI.			

20.5.20 TIMER_DTTIMECFG - DTI Time Configuration Register

Offset	Bit Position																															
0x0E4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset											0x0						0x0						0x0									
Access											RW						RW						RW									
Name											DTFALLT						DTRISET						DTPRESC									

Bit	Name	Reset	Access	Description
31:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21:16	DTFALLT	0x0	RW	**DTI Fall-time**
	Set time span for the falling edge. The fall time is DTFALLT+1 prescaled peripheral clock cycles			
15:10	DTRISET	0x0	RW	**DTI Rise-time**
	Set time span for the rising edge. The rise time is DTRISET+1 prescaled peripheral clock cycles			
9:0	DTPRESC	0x0	RW	**DTI Prescaler Setting**
	These bits select the prescaling factor for DTI. The selected timer clock will be divided by DTPRESC+1 before clocking the DTI logic.			

20.5.21 TIMER_DTFCFG - DTI Fault Configuration Register

Offset	Bit Position																															
0x0E8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset				0x0	0x0	0x0	0x0	0x0							0x0																	
Access				RW	RW	RW	RW	RW							RW																	
Name				DTEM23FEN	DTLOCKUPFEN	DTDBGFEN	DTPRS1FEN	DTPRS0FEN							DTFA																	

Bit	Name	Reset	Access	Description
31:29	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
28	DTEM23FEN	0x0	RW	**DTI EM23 Fault Enable**
	Set this bit to 1 to enable EM2 or EM3 entry as a fault source			
27	DTLOCKUPFEN	0x0	RW	**DTI Lockup Fault Enable**
	Set this bit to 1 to enable core lockup as a fault source			
26	DTDBGFEN	0x0	RW	**DTI Debugger Fault Enable**
	Set this bit to 1 to enable debugger as a fault source			
25	DTPRS1FEN	0x0	RW	**DTI PRS 1 Fault Enable**
	Set this bit to 1 to enable PRS source 1 as a fault source			
24	DTPRS0FEN	0x0	RW	**DTI PRS 0 Fault Enable**
	Set this bit to 1 to enable PRS source 0 as a fault source			
23:18	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
17:16	DTFA	0x0	RW	**DTI Fault Action**
	Select fault action.			

Value	Mode	Description
0	NONE	No action on fault
1	INACTIVE	Set outputs inactive
2	CLEAR	Clear outputs
3	TRISTATE	Tristate outputs

15:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

20.5.22 TIMER_DTCTRL - DTI Control Register

Offset	Bit Position																													
0x0EC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															RW	RW
Name																															DTIPOL	DTCINV

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DTIPOL	0x0	RW	**DTI Inactive Polarity**
	Set inactive polarity of outputs			
0	DTCINV	0x0	RW	**DTI Complementary Output Invert.**
	DTI Complementary Output Invert.			

20.5.23 TIMER_DTOGEN - DTI Output Generation Enable Register

Offset	Bit Position																													
0x0F0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0	0x0	0x0	0x0	0x0	0x0
Access																											RW	RW	RW	RW	RW	RW
Name																											DTOGCDTI2EN	DTOGCDTI1EN	DTOGCDTI0EN	DTOGCC2EN	DTOGCC1EN	DTOGCC0EN

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	DTOGCDTI2EN	0x0	RW	**DTI CDTIn Output Generation Enable**
	This bit enables/disables output generation for the CDTI output from the DTI.			
4	DTOGCDTI1EN	0x0	RW	**DTI CDTIn Output Generation Enable**
	This bit enables/disables output generation for the CDTI output from the DTI.			
3	DTOGCDTI0EN	0x0	RW	**DTI CDTIn Output Generation Enable**
	This bit enables/disables output generation for the CDTI output from the DTI.			
2	DTOGCC2EN	0x0	RW	**DTI CCn Output Generation Enable**
	This bit enables/disables output generation for the CC output from the DTI.			
1	DTOGCC1EN	0x0	RW	**DTI CCn Output Generation Enable**
	This bit enables/disables output generation for the CC output from the DTI.			
0	DTOGCC0EN	0x0	RW	**DTI CCn Output Generation Enable**
	This bit enables/disables output generation for the CC output from the DTI.			

20.5.24 TIMER_DTFAULT - DTI Fault Register

Offset	Bit Position																													
0x0F4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												R	R	R	R	R
Name																												DTEM23F	DTLOCKUPF	DTDBGF	DTPRS1F	DTPRS0F

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	DTEM23F	0x0	R	**DTI EM23 Entry Fault**
	This bit is set to 1 if EM2 or EM3 entry has occurred and DTEM23FEN is set to 1. The TIMER0_DTFAULTC register can be used to clear fault bits.			
3	DTLOCKUPF	0x0	R	**DTI Lockup Fault**
	This bit is set to 1 if a core lockup fault has occurred and DTLOCKUPFEN is set to 1. The TIMER0_DTFAULTC register can be used to clear fault bits.			
2	DTDBGF	0x0	R	**DTI Debugger Fault**
	This bit is set to 1 if a debugger fault has occurred and DTDBGFEN is set to 1. The TIMER0_DTFAULTC register can be used to clear fault bits.			
1	DTPRS1F	0x0	R	**DTI PRS 1 Fault**
	This bit is set to 1 if a PRS 1 fault has occurred and DTPRS1FEN is set to 1. The TIMER0_DTFAULTC register can be used to clear fault bits.			
0	DTPRS0F	0x0	R	**DTI PRS 0 Fault**
	This bit is set to 1 if a PRS 0 fault has occurred and DTPRS0FEN is set to 1. The TIMER0_DTFAULTC register can be used to clear fault bits.			

20.5.25 TIMER_DTFAULTC - DTI Fault Clear Register

Offset	Bit Position																													
0x0F8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												W(nB)	W(nB)	W(nB)	W(nB)	W(nB)
Name																												DTEM23FC	DTLOCKUPFC	DTDBGFC	DTPRS1FC	DTPRS0FC

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	DTEM23FC	0x0	W(nB)	**DTI EM23 Fault Clear**
	Write 1 to this bit to clear EM23 entry fault.			
3	DTLOCKUPFC	0x0	W(nB)	**DTI Lockup Fault Clear**
	Write 1 to this bit to clear core lockup fault.			
2	DTDBGFC	0x0	W(nB)	**DTI Debugger Fault Clear**
	Write 1 to this bit to clear debugger fault.			
1	DTPRS1FC	0x0	W(nB)	**DTI PRS1 Fault Clear**
	Write 1 to this bit to clear PRS 1 fault.			
0	DTPRS0FC	0x0	W(nB)	**DTI PRS0 Fault Clear**
	Write 1 to this bit to clear PRS 0 fault.			

20.5.26 TIMER_DTLOCK - DTI Configuration Lock Register

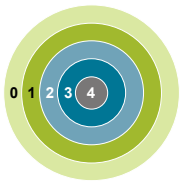
Offset	Bit Position																															
0x0FC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									W							
Name																									DTILOCKKEY							

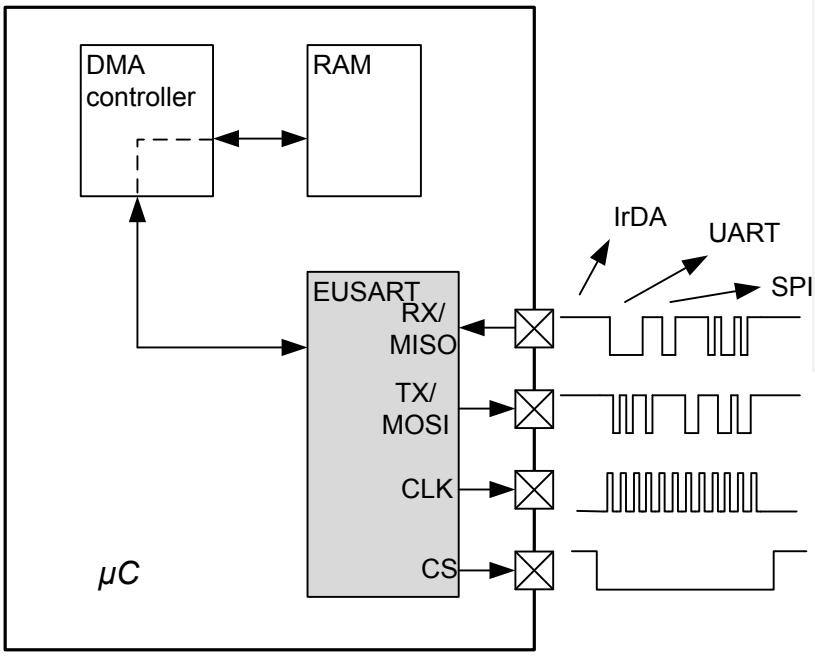
Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	DTILOCKKEY	0x0	W	**DTI Lock Key**

Write any other value than the unlock code to lock TIMER_ROUTE, TIMER_DTCTRL, TIMER_DTCFG, TIMER_DTTIMECFG and TIMER_DTFCFG from editing. Write the unlock code to unlock the DTI registers.

Value	Mode	Description
52864	UNLOCK	Write to unlock TIMER DTI registers

21. EUSART - Universal Synchronous Asynchronous Receiver/Transmitter





Quick Facts

What?

The EUSART handles high-speed UART, SPI-bus, and IrDA communication.

Why?

Serial communication is frequently used in embedded systems and the EUSART allows efficient communication with a wide range of external devices.

How?

The EUSART has a wide selection of operating modes, frame formats and baud rates. The multiprocessor mode allows the EUSART to remain idle when not addressed. 16-deep FIFOs and DMA support makes high data-rates possible with minimal CPU intervention and it is possible to transmit and receive large frames while the MCU remains in EM1 Sleep.

21.1 Introduction

The Enhanced Universal Synchronous Asynchronous serial Receiver and Transmitter (EUSART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as SPI, MicroWire. It can also interface with IrDA devices.

21.2 Features

- Asynchronous (UART) and synchronous (SPI) communication
- Full duplex and half duplex
- Separate TX/RX enable
- Separate receive / transmit 16 deep FIFOs, with additional separate shift registers
- Can operate using HF clock or LF clock (UART only)
- Programmable baud rate, generated as an fractional division from the peripheral clock ($HFPERCLK_{EUSARTn}$)
- Max bit-rate
  - Main SPI mode: 20 MHz
  - Secondary SPI mode: 10 MHz
  - UART mode, HF peripheral clock rate/16, 8, 6, or 4
  - UART mode, 32 KHz LF peripheral clock: 9600 (oversampling not supported with LF operation)
- Supports transmission and reception in EM0 (also EM1 and EM2 in certain modes) with
  - Full DMA support
  - UART mode, specified start-frame can start reception automatically
- UART mode, capable of sleep-mode wake-up on received frame (EM2 Capable instance only)
  - Either wake-up on any received byte or
  - Wake up only on specified start and signal frames
- SPI mode, capable of sleep-mode wake-up on received frame (EM2/3 Capable instance only)
  - Either wake-up on CS active or
  - Wake up on Receive FIFO level matching Watermark Level Setting
- Asynchronous mode supports
  - Configurable number of data bits 7-9 (plus the parity bit, if enabled)
  - HW parity bit generation and check
  - Majority vote baud-reception
  - False start-bit detection
  - Break generation/detection
  - Multi-processor mode
  - Configurable number of stop bits in asynchronous mode:
    - HF clock EM0/1 operation: 0.5, 1, 1.5, 2
    - LF clock operation: 1, 2
  - HW collision detection
  - IrDA support
    - HF clock EM0/1 operation: IrDA modulator
    - LF clock operation: Pulse extender, RX-only
  - Hardware Flow Control
  - Automatic Baud Rate Detection
- Synchronous mode supports
  - Configurable number of data bits 8-16
  - All 4 SPI clock polarity/phase configurations
  - Main and Secondary interface modes
- Data can be transmitted LSB first or MSB first
- Separate interrupt vectors for receive and transmit interrupts
- Loopback mode
  - Half duplex communication
  - Communication debugging
- PRS RX input
- DMA Support
- EM2 operation with LF clock (EM2/3 Capable instance only), wakeup to EM1 for DMA interaction
- Async mode Automatic Baud Rate Detection operating with HF clock in EM0/1

21.3 Functional Description

An overview of the EUSART module is shown in Figure 21.1 EUSART Overview on page 620.

This section describes all posible EUSART features. Please refer to the Device Datasheet to see what features a specific EUSART instance supports.

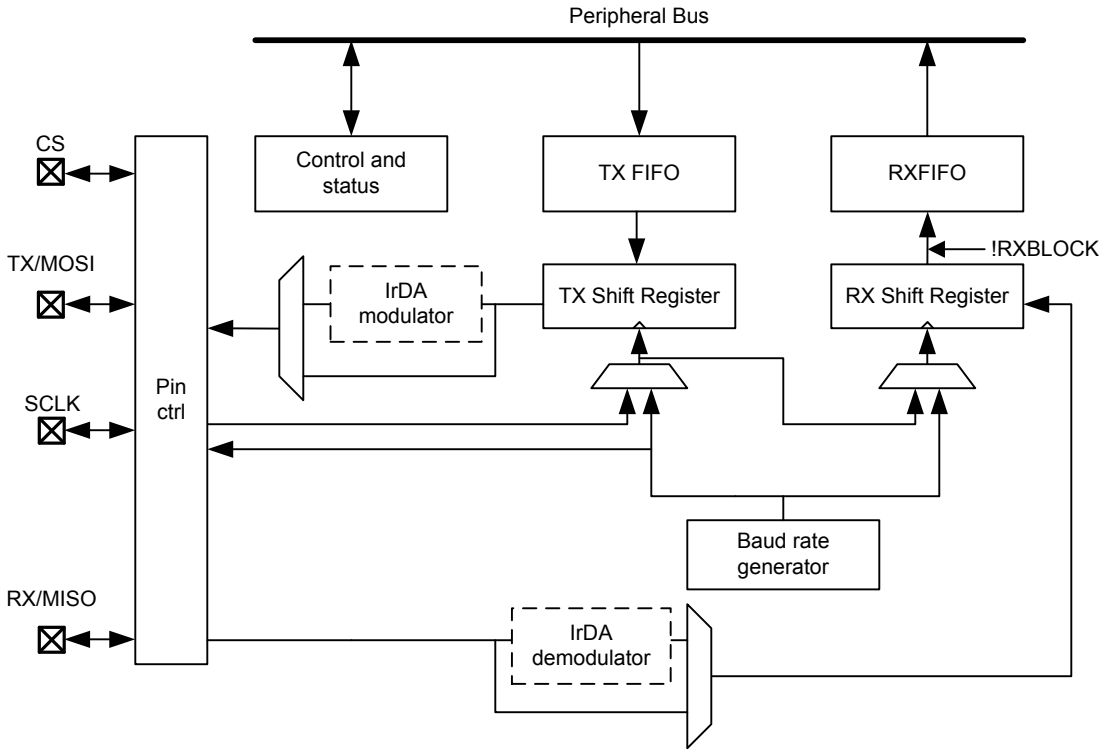


Figure 21.1. EUSART Overview

21.3.1 Modes of Operation

The EUSART operates in either asynchronous or synchronous mode.

In synchronous mode, a separate clock signal is transmitted with the data. This clock signal is generated by the main interface on the bus, and both the main and secondary devices sample and transmit data according to this clock. Both main and secondary interface modes are supported by the EUSART. The synchronous communication mode is compatible with the Serial Peripheral Interface Bus (SPI) standard.

In asynchronous mode, no separate clock signal is transmitted with the data on the bus. The EUSART receiver thus has to determine where to sample the data on the bus from the actual data. To make this possible, additional synchronization bits are added to the data when operating in asynchronous mode, resulting in a slight overhead.

Asynchronous or synchronous mode can be selected by configuring SYNC in EUSARTn_CFG0. The options are listed with supported protocols in Table 21.1 EUSART Asynchronous vs. Synchronous Mode on page 621. Full duplex and half duplex communication is supported in both asynchronous and synchronous mode.

Table 21.1. EUSART Asynchronous vs. Synchronous Mode

SYNC	Communication Mode	Supported Protocols
0	Asynchronous	RS-232, IrDA
1	Synchronous	SPI, MicroWire

Table 21.2 EUSART Pin Usage on page 621 explains the functionality of the different EUSART pins when the EUSART operates in different modes. Pin functionality enclosed in square brackets is optional, and depends on additional configuration parameters. LOOPBK and MASTER are discussed in 21.3.2.7 Local Loopback and 21.3.3.3 Main SPI Interface Mode (Clock Driver) respectively.

Table 21.2. EUSART Pin Usage

SYNC	LOOPBK	MASTER	Pin Functionality			
			TX (MOSI)	RX (MISO)	CLK	CS
0	0	x	Data out	Data in	-	-
0	1	x	Data out/in	-	-	-
1	0	0	Data in	Data out	Clock in	Secondary select
1	0	1	Data out	Data in	Clock out	[Auto secondary select]
1	1	0	Data out/in	-	Clock in	Secondary select
1	1	1	Data out/in	-	Clock out	[Auto secondary select]

21.3.2 Asynchronous Operation

EUSART can operate in asynchronous mode when EUSARTn_CFG0.SYNC is set to 0.

EUSART0 may operate as either a high-speed peripheral running from a high-frequency clock source (HF mode, available in EM0 an EM1), or as a low-energy peripheral operating from a low-frequency clock source (LF mode, available in EM0, EM1, or EM2). EUSART0 operates in HF mode when the EUSART0CLK clock selected in CMU_EUSART0CLKCTRL_CLKSEL is EM01GRPACLK or HFRCOEM23. EUSART0 operates in LF mode when the selected clock is LFXO or LFRCO. Baud rate generation differs between these two modes, and there are certain operational restrictions in LF mode discussed in this chapter. It is not generally useful to switch between modes on-the-fly in a single application.

Other EUSART instances operate only as a high-speed peripheral running from the EM01GRPCCLK selected using CMU_EM01GRPCCLKCTRL_CLKSEL.

21.3.2.1 Frame Format

The frame format used in asynchronous mode consists of a set of data bits in addition to bits for synchronization and optionally a parity bit for error checking. A frame starts with one start-bit (S), where the line is driven low for one bit-period. This signals the start of a frame, and is used for synchronization. Following the start bit are 7 to 9 data bits and an optional parity bit. Finally, a number of stop-bits, where the line is driven high that indicates the end of the frame. An example frame is shown in Figure 21.2 Frame Format on page 622.

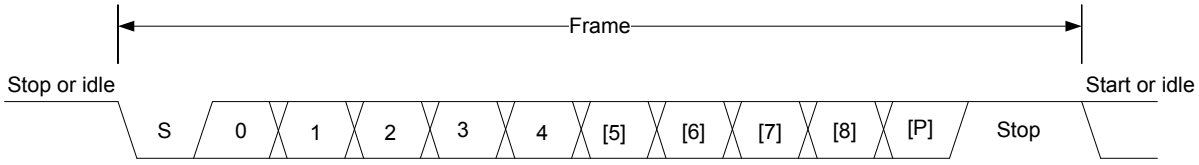


Figure 21.2. Frame Format

The number of data bits in a frame is set by DATABITS in EUSARTn_FRAMECFG, see Table 21.3 Data Bits on page 622, and the number of stop-bits is set by STOPBITS in EUSARTn_FRAMECFG, see Table 21.4 Stop Bits on page 622. Whether or not a parity bit should be included, and whether it should be even or odd is defined by PARITY, also in EUSARTn_FRAMECFG. For proper and reliable communication, all parties of a transfer must agree on the frame format prior to the start of the transfer.

Table 21.3. Data Bits

EUSARTn_FRAMECFG_DATABITS[3:0]	Number of Data bits
0001	7
0010	8 (Default)
0011	9

Table 21.4. Stop Bits

EUSARTn_FRAMECFG_STOPBITS[1:0]	Number of Stop bits
00	0.5 (HF clock operation only)
01	1 (Default)
10	1.5 (HF clock operation only)
11	2

The order in which the data bits are transmitted and received is defined by MSBF in EUSARTn_CFG0. When MSBF is cleared, data in a frame is sent and received with the least significant bit first. When it is set, the most significant bit comes first.

The frame format used by the transmitter can be inverted by setting TXINV in EUSARTn_CFG0, and the format expected by the receiver can be inverted by setting RXINV in EUSARTn_CFG0. These bits affect the entire frame, not only the data bits. An inverted frame has a low idle state, a high start-bit, inverted data and parity bits, and low stop-bits.

21.3.2.2 Parity Bit Calculation and Handling

When parity bit is enabled, hardware automatically calculates and inserts a parity bit into outgoing frames, and verifies the received parity bit in incoming frames. The possible parity modes are defined in Table 21.5 Parity Bits on page 623. When even parity is chosen, a parity bit is inserted to make the number of high bits (data + parity) even. If odd parity is chosen, the parity bit makes the total number of high bits odd. When parity bit is disabled, which is the default configuration, the parity bit is omitted.

Table 21.5. Parity Bits

EUSARTn_FRAMECFG_PARITY[1:0]	Description
00	No parity bit (Default)
01	Reserved
10	Even parity
11	Odd parity

21.3.2.3 Clock Generation

The EUSART clock defines the transmission and reception data rate. The baud rate is given by Figure 21.3 EUSART Baud Rate on page 624.

$$br = f_{EUSARTn}/(oversample \times (1 + EUSARTn\_CLKDIV/256))$$

Figure 21.3. EUSART Baud Rate

where $f_{EUSARTn}$ is the peripheral clock frequency and oversample is the oversampling rate as defined by OVS in EUSARTn_CFG0, see Table 21.6 Oversampling (EUSARTn_CFG0_OVS) on page 624. Note that different instances of the EUSART inside a device may use different peripheral clocks. The peripheral clock may be generically referred to in this chapter as clk_per.

Note: Please note that high frequency clocks should not be selected as UART clock source when nominal voltage is 0.9V.

Note:

Please note that when EUSARTn_CFG0_OVS is set to OVS_DISABLE (0x4), the peripheral clock frequency must be at least three times higher than the chosen baud rate. This condition is given in Figure 21.4 Requirement for EUSARTn_CFG0_OVS = OVS_DISABLE on page 624.

$$f_{EUSARTn} / br >= 3.0$$

Figure 21.4. Requirement for EUSARTn_CFG0_OVS = OVS_DISABLE

Table 21.6. Oversampling (EUSARTn_CFG0_OVS)

OVS[2:0]	Oversample
000	16 (HF clock operation only)
001	8 (HF clock operation only)
010	6 (HF clock operation only)
011	4 (HF clock operation only)
100	1 (OVS disabled - LF clock operation only)

Note: Please note that EUSARTn_CFG0_OVS must not be set to OVS_DISABLE (0x4) when one of the high frequency clocks is selected as EUSARTn peripheral clock source. When one of the low frequency clocks (LFXO/LFRCO) is selected as EUSARTn peripheral clock source, EUSARTn_CFG0_OVS must be set to OVS_DISABLE (0x4).

The EUSART has a fractional clock divider to allow the EUSART clock to be controlled more accurately than what is possible with a standard integral divider. The clock divider used in the EUSART is a 20-bit value, with a 15-bit integral part and an 5-bit fractional part. The fractional part is configured in the lower 5 bits of DIV in EUSARTn_CLKDIV. Fractional clock division is implemented by distributing the selected fraction over thirty two baud periods. The fractional part of the divider tells how many of these periods should be extended by one peripheral clock cycle.

Given a desired baud rate *brdesired*, the clock divider EUSARTn_CLKDIV can be calculated by using Figure 21.5 EUSART Desired Baud Rate on page 624:

$$EUSARTn\_CLKDIV = 256 \times (f_{EUSARTn}/(oversample \times brdesired) - 1)$$

Figure 21.5. EUSART Desired Baud Rate

Table 21.7 EUSART Baud Rates @ 4 MHz Peripheral Clock with 20 Bit CLKDIV on page 625 shows a set of desired baud rates and how accurately the EUSART is able to generate these baud rates when running at a 4 MHz peripheral clock, using 16x or 8x oversampling.

Table 21.7. EUSART Baud Rates @ 4 MHz Peripheral Clock with 20 Bit CLKDIV

Desired baud rate [baud/s]	EUSARTn_CFG0_OVS =00			EUSARTn_CFG0_OVS =01		
	EUSARTn_CLKDIV/256 (to 32nd position)	Actual baud rate [baud/s]	Error %	EUSARTn_CLKDIV/256 (to 32nd position)	Actual baud rate [baud/s]	Error[1] [%]
600	415,6563	600,015	0,003	832,3438	599,9925	-0,001
1200	207,3438	1199,94	-0,005	415,6563	1200,03	0,003
2400	103,1563	2400,24	0,010	207,3438	2399,88	-0,005
4800	51,09375	4799,04	-0,020	103,1563	4800,48	0,010
9600	25,03125	9603,842	0,040	51,09375	9598,08	-0,020
14400	16,375	14388,49	-0,080	33,71875	14401,44	0,010
19200	12,03125	19184,65	-0,080	25,03125	19207,68	0,040
28800	7,6875	28776,98	-0,080	16,375	28776,98	-0,080
38400	5,5	38461,54	0,160	12,03125	38369,3	-0,080
57600	3,34375	57553,96	-0,080	7,6875	57553,96	-0,080
76800	2,25	76923,08	0,160	5,5	76923,08	0,160
115200	1,15625	115942	0,644	3,34375	115107,9	-0,080
230400	0,09375	228571,4	-0,794	1,15625	231884,1	0,644

1 In addition to error introduced by oscillator frequency variation

Table 21.8 EUSART0 Baud Rates in LF mode @ 32.768 kHz Peripheral Clock with 20 bit CLKDIV on page 625 shows a set of desired baud rates and how accurately the EUSART0 is able to generate these baud rates when running from a 32.768 kHz peripheral clock in LF mode.

Table 21.8. EUSART0 Baud Rates in LF mode @ 32.768 kHz Peripheral Clock with 20 bit CLKDIV

Desired baud rate [baud/s]	EUSART0_CLKDIV/256	Actual baud rate [baud/s]	Error[1] [%]
300	108,21875	300,0217	0.01
600	53,625	599,8719	-0.02
1200	26,3125	1199,744	-0.02
2400	12,65625	2399,487	-0.02
4800	5,8125	4809,982	0.21
9600	2,40625	9619,963	0.21

1 In addition to error introduced by oscillator frequency variation

21.3.2.4 Auto Baud Detection (HF clock only)

Setting AUTOBAUDEN in EUSARTn_CFG0 uses the first frame received to automatically set the baud rate provided that it contains 0x55 (IrDA uses 0x00) and is sent out as LSB first and there is no break in the frame. The receiver will measure the number of local clock cycles between the beginning of the START bit and the beginning of the 8th data bit. The DIV field in EUSARTn_CLKDIV will be overwritten with the new value. The OVS in EUSARTn_CFG0 and the +1 count of the Baud Rate equation are already factored into the result that gets written into the DIV field. To restart autobaud detection, clear AUTOBAUDEN and set it high again. Since the auto baud rate detection is done over 8 baud times, only the upper 3 bits of the fractional part of the clock divider are populated.

Auto baud detection has associated status bit EUSARTn_STATUS_AUTOBAUDDONE and interrupt flag EUSARTn_IF_AUTOBAUDDONE. Both the status and the interrupt flag get set after auto baud detection is complete and DIV field in EUSARTn_CLKDIV is overwritten with the new value.

Note:

- If autobaud detection is enabled, software must wait for autobaud detection to complete before transmitting any data.
- Autobaud should be used only during times when it is known that the transmitter will be sending the required data word.
- Autobaud detection is not available when operating with LF clock source.
- For autobaud to work with IrDA, there should be odd parity or no parity in the received data frame.

21.3.2.5 Data Transmission

Asynchronous data transmission is initiated by writing data to the transmit FIFO using one of the methods described in 21.3.2.5.1 Transmit FIFO Operation. When the transmission shift register is empty and if the transmitter is enabled, a frame from the transmit FIFO is loaded into the shift register and transmission begins. Note that the frame loading in to the shift register can also be blocked if CTSEN is set in EUSARTn_CFG0 but the CTS input is inactive. When the frame has been transmitted, a new frame is loaded into the shift register if available, and transmission continues. If the transmit FIFO is empty, the transmitter goes to an idle state, waiting for a new frame to become available.

Transmission is enabled through the command register EUSARTn_CMD by setting TXEN, and disabled by setting TXDIS in the same command register. When the transmitter is disabled using TXDIS, any ongoing transmission is aborted, and any frame currently being transmitted is discarded. When disabled, the TX output goes to an idle state, which by default is a high value. Whether or not the transmitter is enabled at a given time can be read from TXENS in EUSARTn_STATUS.

When the EUSART transmitter is enabled and there is no data in the transmit shift register or transmit FIFO, the TXC status flag in EUSARTn_STATUS and the TXC interrupt flag in EUSARTn_IF are set, signaling that the transmission is complete. The TXC status flag is cleared when a new frame becomes available for transmission, but the TXC interrupt flag must be cleared by software.

Note: (1) Condition for TX to send data out: TX is enabled and there is data available in the TX FIFO and CTS is either not enabled, or if it is enabled, then it is active. (2) If TX output is tri-stated using TXDIS command or TXDISAT setting, then the TX module will still send out data (emptying the FIFO) if condition in point 1 is satisfied, even though the pad is tristated. Restriction: User should not set TXEN when the output is tristated.

21.3.2.5.1 Transmit FIFO Operation

The transmit FIFO is a 16 deep FIFO. A frame can be loaded into the FIFO by writing to EUSARTn_TXDATA. Using EUSARTn_TXDATA allows 9 bits to be written to the FIFO, as well as a set of control bits regarding the transmission of the written frame. Every frame in the FIFO is stored with 9 data bits and additional transmission control bits. A frame is loaded from the FIFO in to the shift register if the transmitter is enabled.

Figure 21.6 Transmit FIFO Operation on page 627 shows the basics of the transmit FIFO.

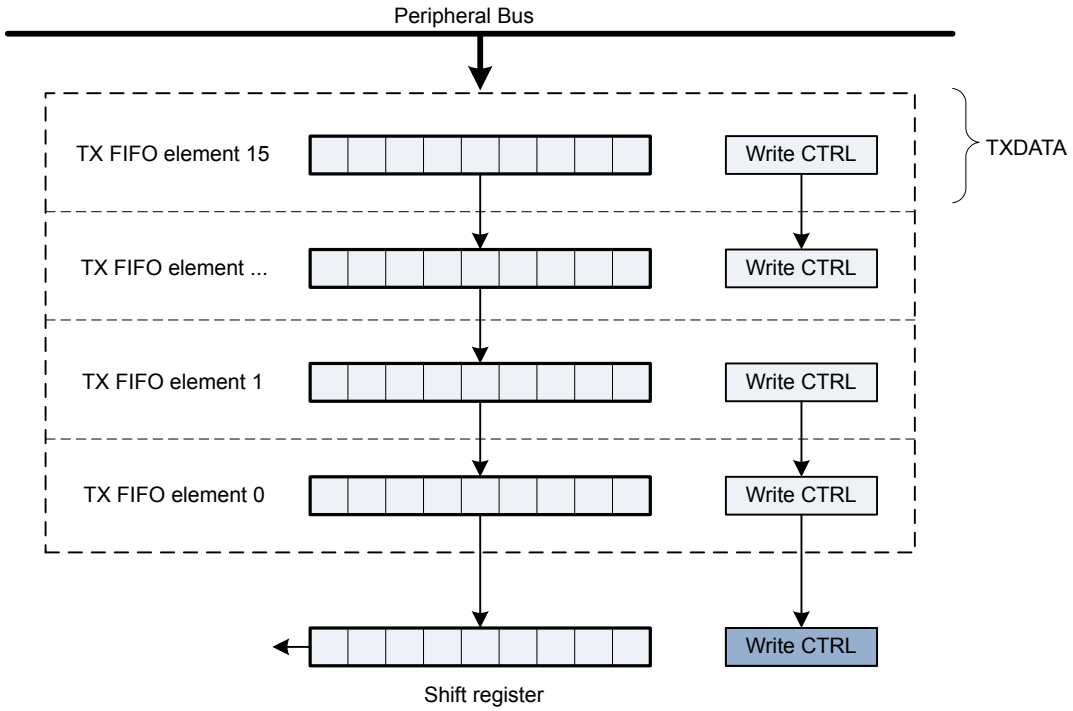


Figure 21.6. Transmit FIFO Operation

In addition to the interrupt flag TXC in EUSARTn_IF and status flag TXC in EUSARTn_STATUS which are set when the transmission is complete, TXFL in EUSARTn_STATUS and the TXFL interrupt flag in EUSARTn_IF are used to indicate the level of the transmit FIFO. TXFIW in EUSARTn_CFG1 controls the level at which these bits are set. The user can choose a transmit FIFO watermark level in TXFIW field of EUSARTn_CFG1 register in order to program when the TXFL interrupt should be triggered.

There is a TXIDLE status bit in EUSARTn_STATUS to provide an indication of when the transmitter is idle. The count of TX valid FIFO entries is called TXFCNT in EUSARTn_STATUS.

The transmit FIFO can be cleared by setting CLEARTX in EUSARTn_CMD. Since this is an Async FIFO, the user needs to first issue the CLEARTX command and then wait on the CLEARTXBUSY status flag until it goes low. EUSART must be enabled (EUSARTn_EN should be set) for the flush to work. EUSART should not be transmitting when CLEARTX command gets issued (can be achieved by disabling the trasmitter). Any frame present in the transmit shift register currently being transmitted will not be aborted due to the flush. Transmission of this frame will be completed. Note that the transmit shift register is never used to store a transmit frame, i.e., if the transmitter is not enabled then the data stays in the transmit FIFO until the transmitter gets enabled. Whenever a frame is loaded in to the transmit shift register, the transmission starts immediately.

Transmit FIFO Status Flags

TX FIFO has two associated status flags: TXFL (set when there is space for data in the TX FIFO, depends on the setting in the TXFIW in CFG1 register) and TXFCNT (count of number of TX frames in the FIFO). These status flags remain set as long as the underlying condition is true, even if the EUSART is disabled (i.e., EUSARTn_EN is 0). It is possible to write to the TX FIFO while EUSART is disabled, this will impact the two flags mentioned above.

Transmit FIFO Interrupt Flags

TX FIFO has two associated interrupt flags: TXFL and TXOF. TXFL is set when space becomes available in the FIFO, depends on TXFIW in CFG1 register. Reset value for TXFIW is such that TXFL gets set as soon the chip comes out of reset (so the interrupt should

be cleared once TXFIW is updated). TXFL remains set as long as the underlying condition is true even if the EUSART is disabled. This means that if a software clear is done for TXFL, then the interrupt will get set again after the clear if the underlying condition is still true (this will happen even if the EUSART is disabled). Writing more data to the FIFO or disabling the TXFL will make the TXFL go away (even if the EUSART is disabled). When writing more frames to the transmit FIFO than there is free space for, the TXOF interrupt flag in EUSARTn_IF will be set, indicating the overflow. The data already in the transmit FIFO is preserved in this case, and no data is written. Note that TXOF can also trigger if DMA tries to write to the FIFO while a TX Flush operation is going on (Flush is activated by setting CMD.CLEARTX). No data will be written to the FIFO in this case. TXOF triggers only once every time an overflow occurs.

Note: (EUSART0 only) In LF clock mode, the TXFL interrupt flag and the TXFL wakeup flag differ slightly in their behavior. IF.TXFL is always set out of reset since there is space available in the FIFO. However, the TXFL wakeup flag is only set after a FIFO read happens and the space that becomes available in the FIFO is the same as programmed in TXFIW in EUSART0_CFG1.

21.3.2.5.2 Frame Transmission Control

The transmission control bits, which can be written using EUSARTn_TXDATA, affect the transmission of the written frame. The following options are available:

- Generate break: By setting TXBREAK, the output will be held low during the stop-bit period to generate a framing error. A receiver that supports break detection detects this state, allowing it to be used e.g. for framing of larger data packets. The line is driven high before the next frame is transmitted so the next start condition can be identified correctly by the recipient. Continuous breaks lasting longer than a EUSART frame are thus not supported. GPIO can be used for this.
- Disable transmitter after transmission: If TXDISAT is set, the transmitter is disabled after the frame has been fully transmitted.
- Enable receiver after transmission: If RXENAT is set, the receiver is enabled after the frame has been fully transmitted. It is enabled in time to detect a start-bit directly after the last stop-bit has been transmitted.
- Unblock receiver after transmission: If UBRXAT is set, the receiver is unblocked and RXBLOCK is cleared after the frame has been fully transmitted.
- Tristate transmitter after transmission: If TXTRIAT is set, TXTRI is set after the frame has been fully transmitted, tristating the transmitter output. Note that if there are more frames in the TX FIFO after the tristating has happened and the transmitter is enabled, then the transmitter will try to send them out but since the output is tristated, nothing will show up at the transmitter output. The FIFO however will get emptied because of the transmitter attempting to send these frames out. If the target is to automatically tristate the TX line whenever the transmitter is idle, then that can be done by setting AUTOTRI in EUSARTn_CFG0. If AUTOTRI is set TXTRI status flag is always read as 0.

21.3.2.5.3 TX Status Flags

The following status flags should be used with care keeping in mind the external sources that can impact these flags as well as the synchronization delay when the status signal crosses over from the EUSART Core clock domain to the APB clock domain. FIFO related status flags were already discussed in 21.3.2.5.1 Transmit FIFO Operation, the remaining flags are mentioned below:

- TXENS: Enable sources: (1) TXEN command from software, (2) PRS trigger (when TXTEN=1). Disable Sources: (1) TXDIS command from software, (2) PERR/FERR (when ERRSTX=1), (3) Software when TXDISAT is set to 1 for a frame.
- TXTRI: Enable sources: (1) TXTRIEN command from software, (2) Software when TXTRIAT is set to 1 for a frame. Disable sources: (1) TXTRIDIS command from software.
- TXIDLE: Set whenever the TX module is idle.
- TXC: Set whenever the TX module goes to idle and both the TX FIFO and the TX shift register are empty. Cleared when either TX FIFO or the TX shift register has data.

21.3.2.5.4 Transmission Delay

By configuring TXDELAY in EUSARTn_CFG1, the transmitter can be forced to wait a number of bit-periods from when it is ready to transmit data, to when it actually transmits the data. This delay is only applied to the first frame transmitted after the transmitter has been idle. When transmitting frames back-to-back the delay is not introduced between the transmitted frames.

This is useful on half duplex buses, because the receiver always returns received frames to software during the first stop-bit. The bus may still be driven for up to 3 bit periods, depending on the current frame format. Using the transmission delay, a transmission can be started when a frame is received, and it is possible to make sure that the transmitter does not begin driving the output before the frame on the bus is completely transmitted.

21.3.2.6 Data Reception

Data reception is enabled by setting RXEN in EUSARTn_CMD. When the receiver is enabled, it actively samples the input looking for a transition from high to low indicating the start baud of a new frame. When a start baud is found, reception of the new frame begins. When the frame has been received, it is pushed into the receive FIFO, making the shift register ready for another frame of data, and the receiver starts looking for another start baud. If a frame is received while the receive FIFO is full, the received frame is discarded and the RXOF interrupt flag in EUSARTn_IF is set to indicate the FIFO overflow.

The receiver can be disabled by setting the command bit RXDIS in EUSARTn_CMD. Any frame currently being received, when the receiver is disabled, is discarded. Whether or not the receiver is enabled at a given time can be read out from RXENS in EUSARTn_STATUS.

21.3.2.6.1 Receive FIFO Operation

The receive-FIFO is a 16 deep FIFO. Data can be read from the receive FIFO via EUSARTn_RXDATA. EUSARTn_RXDATA gives access to the received frame. This register also contains parity error and framing error information of the received frame. When a frame is read from the receive FIFO using EUSARTn_RXDATA, the frame is pulled out of the FIFO, making room for a new frame. If an attempt is done to read more frames from the FIFO than what is available, the RXUF interrupt flag in EUSARTn_IF is set to signal the underflow, and the data read from the FIFO is undefined.

Frames can be read from the receive FIFO without removing the data by using EUSARTn_RXDATAP. EUSARTn_RXDATAP gives access to the first frame in the FIFO with status bits. The data read from this register when the receive FIFO is empty is undefined. No underflow interrupt is generated by a read using this register, i.e. RXUF in EUSARTn_IF is never set as a result of reading from EUSARTn_RXDATAP.

The basic operation of the receive FIFO is shown in Figure 21.7 EUSART Receive FIFO Operation on page 630.

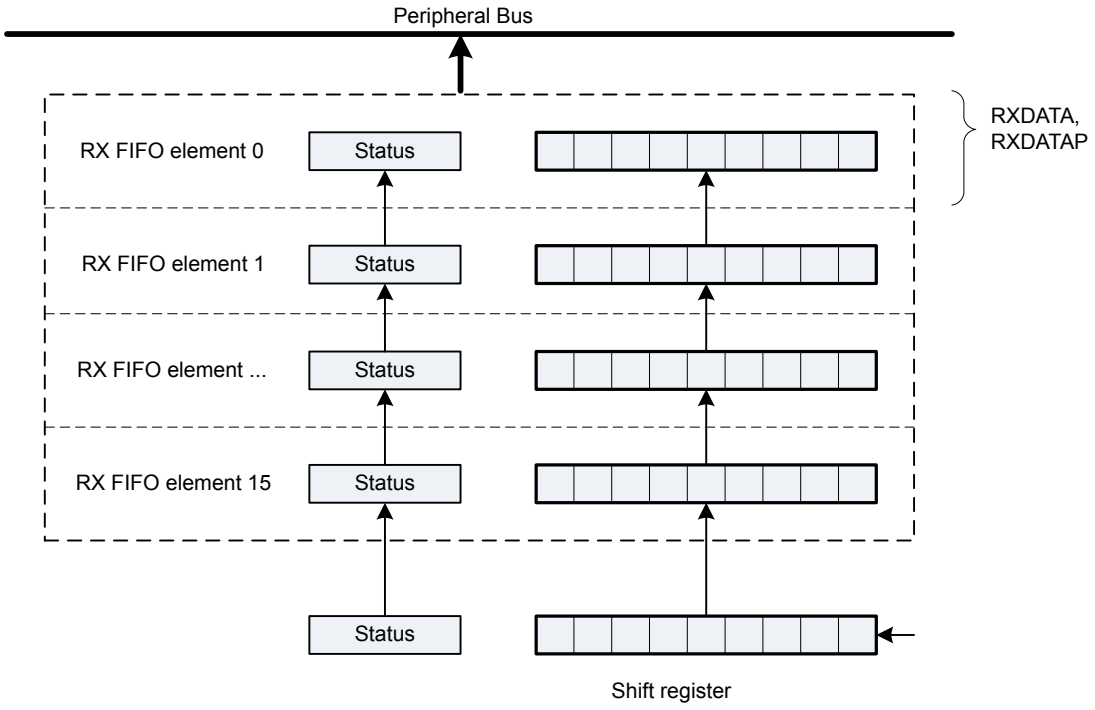


Figure 21.7. EUSART Receive FIFO Operation

Receive FIFO Status Flags

Receive FIFO has two associated status flags: RXFL (set when number of available frames in the receive FIFO is at least number of frames set by RXFIW in CFG1 register) and RXFULL (set when receive FIFO is full). These status flags remain set as long as the underlying condition is true, even if the EUSART is disabled (i.e., EUSARTn_EN is 0). It is possible to read from the receive FIFO while EUSART is disabled, this will impact the two status flags mentioned above. The status flags RXFL and RXFULL are automatically cleared by hardware when their condition is no longer true.

Receive FIFO Interrupt Flags

Receive FIFO has four associated interrupt flags: RXFL, RXFULL, RXOF and RXUF. RXFL is set when number of available frames in the receive FIFO is at least number of frames set by RXFIW in CFG1 register. RXFULL is set when receive FIFO is full. Both RXFL and RXFULL remains set as long as the underlying condition is true even if EUSART is disabled. This means that if a software clear is done for RXFL / RXFULL while the undelying condition of respective interrupt is still true, the corresponding interrupt will get set again after the clear (this will happen even if EUSART is disabled). Reading data from the FIFO or disabling the RXFL / RXFULL will block the respective interrupt to get set after a software clear (even if EUSART is disabled). RXOF is set when a new frame is received while the receive FIFO is full, indicating overflow. The new frame is discarded. RXOF triggers only once every time an overflow occurs. RXUF is set when an attempt (via RXDATA or DMA) is done to read more frames from the receive FIFO than what is available, indicating underflow. The data read from the FIFO is undefined. RXUF triggers every time an underflow occurs even if EUSART is disabled.

21.3.2.6.2 Blocking Incoming Data

When using hardware frame recognition, as detailed in 21.3.2.6.9 Multi-Processor Mode and 21.3.2.8 Collision Detection, it is necessary to be able to let the receiver sample incoming frames without loading them into the receive FIFO. This is accomplished by blocking incoming data.

Incoming data is blocked as long as RXBLOCK in EUSARTn_STATUS is set. When blocked, frames received by the receiver will not be loaded into the receive FIFO, and software is not notified by the RXFL flag in EUSARTn_STATUS or the RXFL interrupt flag in EUSARTn_IF at their arrival. For data to be loaded into the receive FIFO, RXBLOCK must be cleared in the instant a frame is fully received by the receiver. RXBLOCK is set by setting RXBLOCKEN in EUSARTn_CMD and disabled by setting RXBLOCKDIS also in EUSARTn_CMD. There is one exception where data is loaded into the receive FIFO even when RXBLOCK is set. This is when an address frame is received while operating in multi-processor mode. See 21.3.2.6.9 Multi-Processor Mode for more information.

Frames received containing framing or parity errors will not result in the FERR and PERR interrupt flags in EUSARTn_IF being set while RXBLOCK in EUSARTn_STATUS is set. Hardware recognition is not applied to these erroneous frames, and they are silently discarded.

The overflow interrupt flag RXOF in EUSARTn_IF will also not be set while RXBLOCK in EUSARTn_STATUS is set.

21.3.2.6.3 Data Sampling and Filtering

The receiver can sample incoming signal at a rate 16, 8, 6 or 4 times higher than the given baud rate, depending on the oversampling mode given by OVS in EUSARTn_CFG0. Lower oversampling rates make higher baud rates possible, but give less room for errors.

When a high-to-low transition is registered on the input while the receiver is idle, this is recognized as a start-bit, and the baud rate generator is synchronized with the incoming frame.

For oversampling modes 16, 8 and 6, every bit in the incoming frame is sampled three times to gain a level of noise immunity. These samples are aimed at the middle of the bit-periods, as visualized in Figure 21.8 EUSART Sampling of Start and Data Bits on page 632. With OVS=0 in EUSARTn_CFG0, the start and data bits are thus sampled at locations 8, 9 and 10 in the figure, locations 4, 5 and 6 for OVS=1 and locations 3, 4, and 5 for OVS=2. The value of a sampled bit is determined by majority vote. If two or more of the three bit-samples are high, the resulting bit value is high. If the majority is low, the resulting bit value is low.

Majority vote is used for all oversampling modes except 4X oversampling and when oversampling is disabled. In 4X oversampling mode, a single sample is taken at position 3 as shown in Figure 21.8 EUSART Sampling of Start and Data Bits on page 632.

When oversampling is disabled i.e. OVS = DISABLE, there is only one available location for sampling the start and data bits and so majority vote is not used.

Note: When operating in HF clock mode, oversampling must be set to 4, 6, 8, or 16x. When operating in LF clock mode, oversampling must be disabled.

Software can disable majority vote by setting MVDIS in EUSARTn_CFG0. When majority vote is disabled by software, a single sample is taken at location 9 in the figure for OVS=0, location 5 for OVS=1 and location 4 for OVS=2.

If the value of the start bit is found to be high, the reception of the frame is aborted, filtering out false start bits possibly generated by noise on the input.

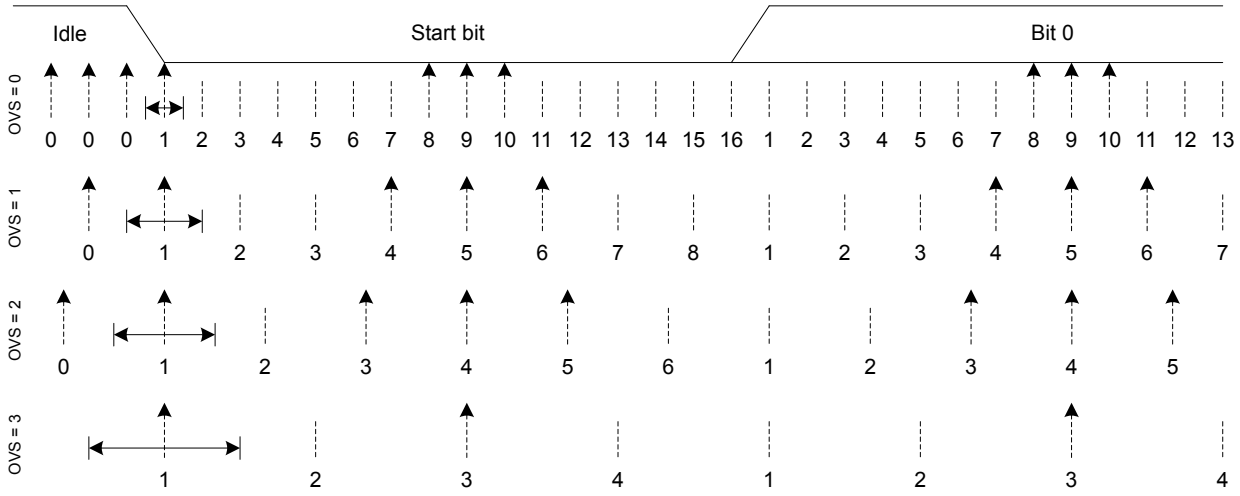


Figure 21.8. EUSART Sampling of Start and Data Bits

If the baud rate of the transmitter and receiver differ, the location each bit is sampled will be shifted towards the previous or next bit in the frame. This is acceptable for small errors in the baud rate, but for larger errors, it will result in transmission errors.

When the number of stop bits is 1 or more, stop bits are sampled like the start and data bits as seen in Figure 21.9 EUSART Sampling of Stop Bits when Number of Stop Bits are 1 or More on page 633. When a stop bit has been detected, EUSARTn is ready for a new start bit.

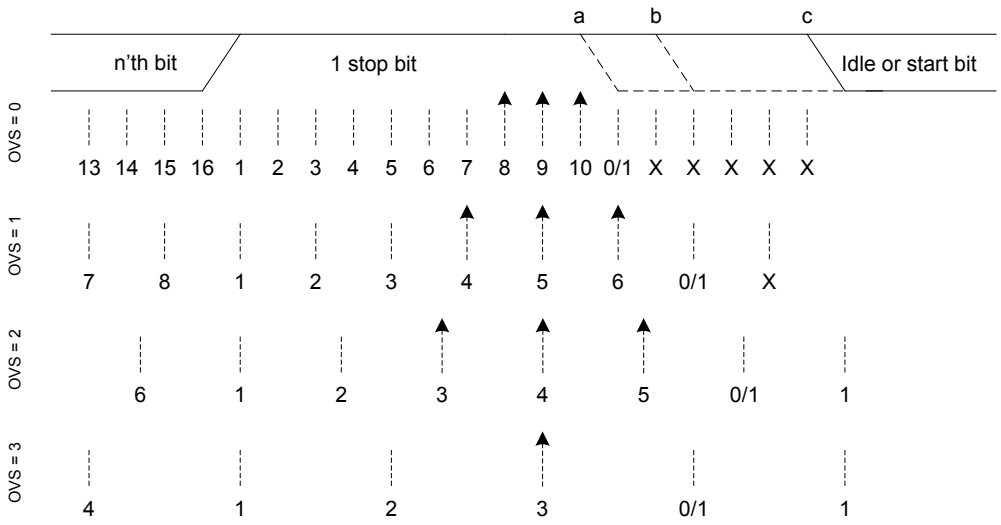


Figure 21.9. EUSART Sampling of Stop Bits when Number of Stop Bits are 1 or More

When working with stop bit lengths of half a baud period, the above sampling scheme no longer suffices. In this case, the stop-bit is not sampled, and no framing error is generated in the receiver if the stop-bit is not generated. However, the line must still be driven high before the next start bit for the EUSART to successfully identify the start bit.

21.3.2.6.4 RX Status Flags

The following status flags should be used with care keeping in mind the external sources that can impact these flags as well as the synchronization delay when the status signal crosses over from the EUSART Core clock domain to the APB clock domain. FIFO related status flags were already discussed in 21.3.2.6.1 Receive FIFO Operation, the remaining flags are mentioned below:

- RXENS: set when RX is enabled. Enable sources: (1) RXEN command from software, (2) PRS trigger (when RXTEN=1), (3) TX (when RXENAT=1). Disable Sources: (1) RXDIS command from software, (2) Parity / framing error (when ERRSRX=1).
- RXBLOCK: set when RX is blocked which means RX keeps receiving frames but does not push received frame to receive FIFO. Enable sources: (1) RXBLOCKEN command from software. Disable Sources: (1) RXBLOCKDIS command from software, (2) STARTFRAME match (when SFUBRX=1), (3) TX (when UBRXAT=1).
- RXIDLE: Set when RX module completes pushing the last received frame to receive FIFO (if receive FIFO has space) and is not receiving any new frame or when RX gets disabled.
- AUTOBAUDDONE: Set when auto baud detection is complete and DIV field in EUSARTn_CLKDIV is overwritten with the detected value.

21.3.2.6.5 Parity Error

When parity bits are enabled, a parity check is automatically performed on incoming frames. When a parity error is detected in an incoming frame, the data parity error bit PERR in the frame is set, as well as the interrupt flag PERR in EUSARTn_IF. Frames with parity errors are loaded into the receive FIFO like regular frames.

PERR can be accessed by reading the frame from the receive FIFO using the EUSARTn_RXDATA, or EUSARTn_RXDATAP registers.

If ERRSTX in EUSARTn_CFG0 is set, the transmitter is disabled on received parity errors. If ERRSRX in EUSARTn_CFG0 is set, the receiver is disabled on parity errors.

21.3.2.6.6 Framing Error and Break Detection

A framing error is the result of an asynchronous frame where the stop bit was sampled to a value of 0. This can be the result of noise and baud rate errors, but can also be the result of a break generated by the transmitter on purpose.

When a framing error is detected in an incoming frame, the framing error bit FERR in the frame is set. The interrupt flag FERR in EUSARTn_IF is also set. Frames with framing errors are loaded into the receive FIFO like regular frames.

If ERRSTX in EUSARTn_CFG0 is set, the transmitter is disabled on received framing errors. If ERRSRX in EUSARTn_CFG0 is set, the receiver is disabled on framing errors.

21.3.2.6.7 Programmable Start Frame

The EUSART can be configured to start receiving data when a special start frame is detected on the input. This can be useful when operating in low energy modes, allowing other devices to gain the attention of the EUSART by transmitting a given frame.

When SFUBRX in EUSARTn_CFG1 is set, an incoming frame matching the frame defined in EUSARTn_STARTFRAME will result in RXBLOCK in EUSARTn_STATUS being cleared. This can be used to enable reception when a specified start frame is detected. If the receiver is enabled and blocked, i.e. RXENS and RXBLOCK in EUSARTn_STATUS are set, the receiver will receive all incoming frames, but unless an incoming frame is a start frame it will be discarded and not loaded into the receive FIFO. When a start frame is detected, the block is cleared, and frames received from that point, including the start frame, are loaded into the receive FIFO.

An incoming start frame results in the STARTFIF interrupt flag in EUSARTn_IF being set, regardless of the value of SFUBRX in EUSARTn_CFG1. This allows an interrupt to be made when the start frame is detected. The interrupt will be set even if the receiver is blocked i.e. EUSARTn_STATUS_RXBLOCK = 1.

Note: The receiver must be enabled for start frames to be detected. Please note that, if another UART device sends a start frame but a parity and/or framing error occurs during the receiption, the received frame is not detected as a start frame.

21.3.2.6.8 Programmable Signal Frame

As well as the configurable start frame, a special signal frame can be specified. When a frame matching the frame defined in EUSARTn_SIGFRAME is detected by the receiver, the SIGF interrupt flag in EUSARTn_IF is set. As like start frame detection, the interrupt will be set even if the receiver is blocked i.e. EUSARTn_STATUS_RXBLOCK = 1.

One use of the programmable signal frame is to signal the end of a multi-frame message transmitted to the EUSART. An interrupt will then be triggered when the packet has been completely received, allowing software to process it. Used in conjunction with the programmable start frame and DMA, this makes it possible for the EUSART to automatically begin the reception of a packet on a specified start frame, load the entire packet into memory, and give an interrupt when reception of a packet has completed. When one of the low frequency oscillators (LFXO,LFRCO) is used as EUSART0 peripheral clock source, the device can thus wait for data packets in EM2, and only be woken up when a packet has been completely received.

Note: The receiver must be enabled for a signal frame to be detected. If a parity and/or framing error occurs during the reception of a signal frame, the received frame is not detected as a signal frame.

21.3.2.6.9 Multi-Processor Mode

To simplify communication between multiple processors, the EUSART supports a special multi-processor mode. In this mode the 9th data bit in each frame is used to indicate whether the content of the remaining 8 bits is data or an address.

When multi-processor mode is enabled, an incoming 9-bit frame with the 9th bit equal to the value of MPAB in EUSARTn_CFG0 is identified as an address frame. When an address frame is detected, the MPAF interrupt flag in EUSARTn_IF is set, and the address frame is loaded into the receive register. This happens regardless of the value of RXBLOCK in EUSARTn_STATUS.

Multi-processor mode is enabled by setting MPM in EUSARTn_CFG0, and the value of the 9th bit in address frames can be configured in EUSARTn_CFG0_MPAB. Note that the receiver must be enabled for address frames to be detected. The receiver can be blocked however, preventing data from being loaded into the receive FIFO while looking for address frames.

The following section explains basic usage of the multi-processor mode:

EUSART Multi-processor Mode Example

1. All devices on the bus enable multi-processor mode and enable and block the receiver. They will now not receive data unless it is an address frame. MPAB in EUSARTn_CFG0 is set to desired value to identify frames with the 9th bit value equal to MPAB as address frames.
2. A transmitting device sends a frame containing the address of a different device and with the 9th bit set to value of MPAB.
3. All devices receive the address frame and get an interrupt. They can read the address from the receive FIFO. The selected device unblocks the receiver to start receiving data from the transmitter.
4. The transmitter sends data with the 9th bit set to opposite value of MPAB.
5. Only the addressed device with RX enabled and unblocked receives the data. When transmission is complete, the device blocks the receiver and waits for a new address frame.

When a device has received an address frame and wants to receive the following data, it must make sure the receiver is unblocked before the next frame has been completely received in order to prevent data loss. One option is to set SFUBRX in EUSARTn_CFG1 and set the address frame as start frame in EUSARTn_STARTFRAME. This will handle automatic unblocking of RX when address frame is received.

21.3.2.6.10 RX Timeout

A RX timeout function can be enabled by setting EUSART_CFG1_RXTIMEOUT to desired value. When enabled, a timer gets started after every successful frame reception. If timeout occurs before the next RX start bit is received, EUSART_IF_RXTO gets set which can be used to wake-up the system to handle received data. This is shown in Figure 21.10 RX Timeout on page 635 If the next RX start bit is received before timeout occurs, no interrupt gets generated, the timer is reset and will only be started again after the on-going frame reception is complete.

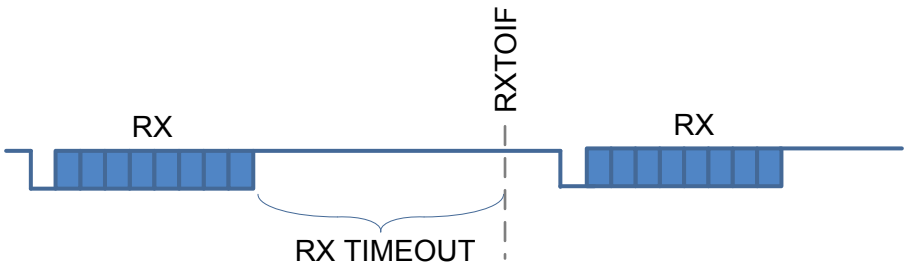


Figure 21.10. RX Timeout

Please note that the timer does not get started in following scnearios:

- If auto baud rate detection is enabled and auto baud rate has not been found, the timer does not get started after the first frame which is used to detect the baud rate automatically.
- If a frame is received while RX is blocked, the timer does not get started.
- If EUSART_CFG0_SKIPPERRF is set to '1' and a frame is received with a parity error, the timer does not get started.

Please also note that the UART RX input line must be in idle state after frame reception for the timer to start.

Note: When EUSARTn_FRAMECFG_STOPBITS is set to a fractional value i.e. 'HALF' or 'ONEANDHALF', the fractional value is rounded to nearest value and so RX timeout is extended by 0.5 baud width per frame.

21.3.2.7 Local Loopback

The EUSARTn receiver samples RX by default, and the transmitter drives TX by default. This is not the only option however. When LOOPBK in EUSARTn_CFG0 is set, the RX pin is connected to the TX pin as shown in Figure 21.11 EUSART Local Loopback on page 636. This is useful for debugging, as the EUSARTn can receive the data it transmits, but it is also used to allow the EUSARTn to read and write to the same pin, which is required for some half duplex communication modes. In this mode, the TX pin must be enabled as an output in the GPIO.

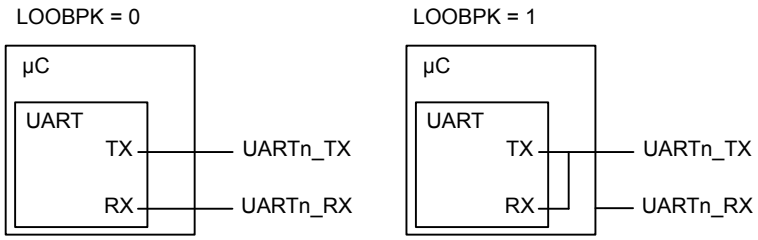


Figure 21.11. EUSART Local Loopback

21.3.2.8 Collision Detection

EUSARTn supports a basic form of collision detection. When the receiver is connected to the output of the transmitter, either by using the LOOPBK bit in EUSARTn_CFG0 or through an external connection, this feature can be used to detect whether data transmitted on the bus by the EUSARTn did get corrupted by a simultaneous transmission by another device on the bus.

For collision detection to be enabled, CCEN in EUSARTn_CFG0 must be set, and the receiver enabled. The data sampled by the receiver is then continuously compared with the data output by the transmitter. If they differ, the CCF interrupt flag in EUSARTn_IF is set. The collision check includes all bits of the transmitted frames. The CCF interrupt flag is set once for each bit sampled by the receiver that differs from the bit output by the transmitter. When the transmitter output is disabled, i.e. the transmitter is tristated, collisions are not registered.

Note: Please note that collision detection supports only baudrates up to 1mbps.

21.3.2.9 Half Duplex Communication

When doing full duplex communication, two data links are provided, making it possible for data to be sent and received at the same time. In half duplex mode, data is only sent in one direction at a time. There are several possible half duplex setups, as described in the following sections.

21.3.2.9.1 Single Data-link

In this setup, the EUSART both receives and transmits data on the same pin. This is enabled by setting LOOPBK in EUSARTn_CFG0, which connects the receiver to the transmitter output. Because they are both connected to the same line, it is important that the EUSART transmitter does not drive the line when receiving data, as this would corrupt the data on the line.

When communicating over a single data-link, the transmitter must thus be tristated whenever not transmitting data. This is done by setting the command bit TXTRIEN in EUSARTn_CMD, which tristates the transmitter. Before transmitting data, the command bit TXTRIDIS, also in EUSARTn_CMD, must be set to enable transmitter output again. Whether or not the output is tristated at a given time can be read from TXTRI in EUSARTn_STATUS. If TXTRI is set when transmitting data, the data is shifted out of the shift register, but is not put out on TX line.

When operating a half duplex data bus, it is common to have a main bus controller, which first transmits a request to one of the secondary devices on the bus, then receives a reply. In this case, the frame transmission control bits, which can be set by writing to EUSARTn_TXDATA, can be used to make the EUSART automatically disable transmission, tristate the transmitter and enable reception when the request has been transmitted, making it ready to receive a response from the secondary device.

Tristating the transmitter can also be performed automatically by the EUSART by using AUTOTRI in EUSARTn_CFG0. When AUTOTRI is set, the EUSART automatically tristates TX line whenever the transmitter is idle, and enables transmitter output when the transmitter goes active. If AUTOTRI is set TXTRI is always read as 0.

Note: Another way to tristate the transmitter is to enable wired-and or wired-or mode in GPIO. For wired-and mode, outputting a 1 will be the same as tristating the output, and for wired-or mode, outputting a 0 will be the same as tristating the output. This can only be done on buses with a pull-up or pull-down resistor respectively.

21.3.2.9.2 Single Data-link with External Driver

Some communication schemes, such as RS-485 rely on an external driver. Here, the driver has an extra input which enables it, and instead of tristating the transmitter when receiving data, the external driver must be disabled.

This can be done manually by assigning a GPIO to turn the driver on or off.

Figure 21.12 EUSART Half Duplex Communication with External Driver on page 637 shows an example configuration using an external driver.

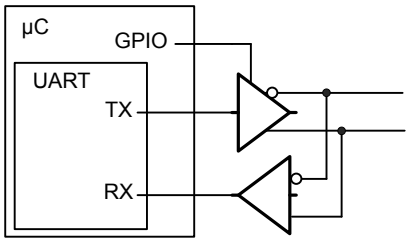


Figure 21.12. EUSART Half Duplex Communication with External Driver

21.3.2.9.3 Two Data-links

Some limited devices only support half duplex communication even though two data links are available. In this case software is responsible for making sure data is not transmitted when incoming data is expected.

21.3.2.10 Hardware Flow Control

Hardware flow control can be used to hold off the link partner's transmission until receive FIFO space is available. Use RTSPEN in GPIO_DBUSEUSARTn_ROUTEEN to enable RTS pin (CTS is an input so its pin is enabled by default). Port and Pin selection for RTS and CTS can be done in GPIO_DBUSEUSARTn_RTSROUTE/CTSROUTE. RTS is an out going signal which indicates that receive FIFO space is available to receive a frame. The link partner is being requested to send its data when RTS is active. RTS activation can be made dependent on how much space is available in the receive FIFO using RTSRXFW in EUSARTn_CFG1. For debug use set DBGHALT in EUSARTn_CFG1 which will force the RTS to request one frame from the link partner when the CPU core single steps. RTS is deactivated when RX is disabled.

CTS is an incoming signal to stop the next TX data from going out. CTS indicates that the link partner has receive FIFO space available, and the local transmitter is clear to send. When CTS deactivates in the middle of a frame, the frame currently being transmitted is completed before stopping. CTS operation needs to be enabled using CFG1.CTSEN.

The RTS and CTS are active low by default, but their polarity can be changed with RTSINV and CTSINV in EUSARTn_CFG1 respectively.

21.3.2.11 Debug Halt

During single stepping, debug halt feature allows halting EUSART frame reception by deactivating RTS when the core is halted and continuing frame reception by activating RTS when the core is unhalted. EUSART debug halt can be enabled by setting DBGHALT in EUSART_CFG1 to '1'. EUSART receiver must be enabled for debug halting.

When EUSART_CFG1_DBGHALT is not set or EUSART_CFG1_DBGHALT is set but chip halt is low, RTS is only dependent on the receive FIFO having space available to receive at least number of frames given by EUSART_CFG1_RTSRXFW settings.

When EUSART_CFG1_DBGHALT is set, RTS will remain deactivated as long as chip halt is high. When a low pulse is detected on chip halt while DBGHALT is set, RTS will be activated if receive FIFO has space available to receive at least number of frames given by EUSART_CFG1_RTSRXFW settings and no frame is being received. RTS will be deactivated again if chip halt goes back to high and receiver starts receiving a new frame or if receive FIFO does not have space available to receive at least number of frames given by EUSART_CFG1_RTSRXFW settings. This behavior allows single stepping to pulse the chip halt low for a cycle, and receive the next frame.

Please note that, if chip halt remains low for a short duration after RX is enabled while DBGHALT is set, initial low value of chip halt will be treated the same as a low pulse on chip halt.

As incoming frame is always received until receive FIFO is full regardless of the state of DBGHALT or chip halt, the link partner must stop transmitting when RTS is deactivated, or the receive FIFO could overflow.

All data in the transmit FIFO is sent out even when chip halt is asserted; therefore, DMA will need to be set to stop sending EUSART TX data during chip halt.

21.3.2.12 PRS-triggered Transmissions

If a transmission must be started on an event with very little delay, the PRS system can be used to trigger the transmission. The PRS channel to use as a trigger can be selected using EUSARTn_TRIGGER.PRSSEL in PRS. When a positive edge is detected on PRS signal, the receiver is enabled if RXTEN in EUSARTn_TRIGCTRL is set, and the transmitter is enabled if TXTEN in EUSARTn_TRIGCTRL is set. Only one signal input is supported by the EUSART.

21.3.2.13 PRS RX Input

The EUSART can be configured to receive data directly from a PRS channel by setting RXPRSEN in EUSARTn_CFG1. The PRS channel used is selected using EUSARTn_RX.PRSSEL in PRS.

21.3.2.14 DMA Support

The EUSART has full DMA support. The DMA controller can write to the transmit FIFO using the register EUSARTn_TXDATA, and it can read from the receive FIFO using the register EUSARTn_RXDATA. This enables 9 bit data + control/status bits transfers both to and from the EUSART.

A request for the DMA controller to read from the EUSART receive buffer can come from the following source:

- Receive FIFO is loaded with at least number of frames set by RXFIW.

A write request can come from the following source:

- Transmit FIFO has space for at least number of frames set by TXFIW

In some cases, it may be sensible to temporarily stop DMA read access to the EUSART when an error such as parity or framing error has occurred. This is enabled by setting ERRSDMA in EUSARTn_CFG0.

EUSART0 (EM2 Capable instance only) can also work with the DMA in low power mode so that the system does not have to wake up to EM0 to consume data. This can happen if TXDMAWU or RXDMAWU in the EUSARTn_CFG1 is set. The DMA will be triggered when TXFIW/RXFIW samples are in the corresponding FIFO. The chip will enter EM1, DMA will then pop/ push all the elements of the corresponding FIFO and then the system will be put back to EM2.

21.3.2.15 Interrupts

The interrupts generated by the EUSART are combined into two interrupt vectors. Interrupts related to reception are assigned to one interrupt vector, and interrupts related to transmission are assigned to the other. Separating the interrupts in this way allows different priorities to be set for transmission and reception interrupts.

The transmission interrupt vector groups the transmission-related interrupts generated by the following interrupt flags:

- TXC
- TXFL
- TXOF
- CCF
- TXIDLE

The reception interrupt on the other hand groups the reception-related interrupts, triggered by the following interrupt flags:

- RXFL
- RXFULL
- RXOF
- RXUF
- PERR
- FERR
- MPAF
- START
- SIGF
- AUTOBAUDDONE
- RXTO

If EUSARTn interrupts are enabled, an interrupt will be made if one or more of the interrupt flags in EUSARTn_IF and their corresponding bits in EUSARTn_IEN are set. All interrupts can serve as wake up interupts if enabled (EM2 Capable instance only).

21.3.2.16 EM2 operation (EUSART0 Only)

EUSART0 can operate in EM2 when running from an LF oscillator source (LF mode). Note that sending and receiving data in EM2 requires that the EUSART be connected to GPIO that are capable of operating in EM2. This includes all pins on Port A and Port B. Pins on Port C and Port D are not available for digital peripheral signalling in EM2 or EM3.

EM2 operation allows the EUSART to wait for an incoming UART frame, or even wait on the programmable start or signal frames while the system is consumiung very little energy. When a UART frame is completely received, or a start/signal frame is detected, the CPU can quickly be woken up. Alternatively, multiple frames can be transferred via the Direct Memory Access (DMA) module into RAM memory before waking up the CPU. Similarly, data can be transmitted in EM2 with data from the CPU or through use of the DMA.

All interrupts can be used as wake up interrupts if enabled. None of the interrupts are sticky, i.e., the interrupt triggers only once whenever the interrupt condition is reached.

Note: When RXDMAWU or TXDMAWU is set in EUSART0_CFG1, the system will not be able to go to EM2 before all related EUSART0 DMA requests have been processed. This means that if RXDMAWU is set and the EUSART receives a frame, the system will wait to go to EM2 before the frame has been read from the EUSART. In order for the system to go back to EM2 during or after the final transmission (i.e. when DMA will no add more data to the TX FIFO), the wake request to DMA must be removed. There are two methods for doing this:

1. If RX does not need to remain active, software can disable the peripheral and clear the TXDMAWU bit in the ISR to prevent further DMA requests. The peripheral may be re-enabled after TXDMAWU is cleared. Note that while the peripheral is disabled, the EUSART cannot receive any new data, so this option should only be used if no data is expected.
2. If RX must remain active, it is recommended to disable TX, and then write dummy information into the FIFO until the TXFL flag will no longer trigger a new wakeup. This will prevent new DMA requests.

21.3.2.17 PRS

All PRS inputs are synchronized to the peripheral clock (clk_per) for the EUSART instance.

- RX PRS: Input goes to RX module for data reception if RXPRSEN set to 1
- TRIGGER PRS: Can be used to Enable TX and/or RX if TXTEN/RXTEN are set to 1

All PRS outputs come from clk_per flops.

- PRS_TX: Same as TX output (tx_out) of EUSART
- PRS_TXC: Same as the TXC status flag
- PRS_IRDA_TX: Registered (clk_per) version of IRHF output
- PRS_RXFL: Set if (rxdata_fifo_cnt > RXFIW)
- PRS_RTS: Same as RTS output (rts_out) of EUSART

21.3.2.18 IrDA operation

The EUSART supports IrDA operation using both HF and LF clocks. For IrDA with HF clock, the controls are given in IRHFCFG register. For IrDA with LF clock (32.768 kHz), only RX is supported and the controls are given in IRLFCFG register. Note that OVS must be disabled for LF operation.

Note: Note that break generation/ detection feature is not supported while IrDA is enabled, i.e., either IRHFEN or IRLFEN is set.

21.3.2.18.1 IRHF

The IRHF modulator implements the physical layer of the IrDA specification, which is necessary for communication over IrDA. The modulator takes the signal output from the EUSART module, and modulates it before it leaves the EUSART. In the same way, the input signal is demodulated before it enters the actual EUSART module. The modulator implements the original Rev. 1.0 physical layer and one high speed extension which supports speeds from 2.4 kbps to 1.152 Mbps.

The data from and to the EUSART is represented in a NRZ (Non Return to Zero) format, where the signal value is at the same level through the entire bit period. For IrDA, the required format is RZI (Return to Zero Inverted), a format where a “1” is signalled by holding the line low, and a “0” is signalled by a short high pulse. An example is given in Figure 21.13 EUSART Example RZI Signal for a given EUSART Frame on page 640.

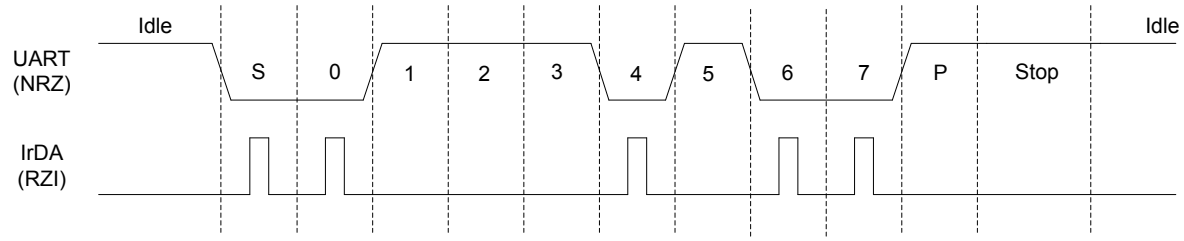


Figure 21.13. EUSART Example RZI Signal for a given EUSART Frame

The IrDA HF module is enabled by setting IRHFEN in IRHFCFG. The EUSART transmitter output and receiver input is then routed through the IrDA HF modulator.

The width of the pulses generated by the IrDA HF modulator is set by configuring IRHFPW in IRHFCFG register. Four pulse widths are available, each defined relative to the configured bit period as listed in Table 21.9 EUSART IrDA Pulse Widths on page 640.

Table 21.9. EUSART IrDA Pulse Widths

IRHFPW	Pulse width OVS=0	Pulse width OVS=1	Pulse width OVS=2	Pulse width OVS=3
00	1/16	1/8	1/6	1/4
01	2/16	2/8	2/6	N/A
10	3/16	3/8	N/A	N/A
11	4/16	N/A	N/A	N/A

By default, no filter is enabled in the IrDA HF demodulator. A filter can be enabled by setting IRHFFILT in IRHFCFG. When the filter is enabled, an incoming pulse has to last for 5 consecutive clock cycles to be detected by the IrDA demodulator. When the filter is enabled, the minimum clock frequency required is based on the baud rate and OVS chosen. The frequency requirements are listed in table Table 21.10 EUSART IrDA IRHFFILT=1, Min Clock Frequency Requirement (MHz) on page 640.

Table 21.10. EUSART IrDA IRHFFILT=1, Min Clock Frequency Requirement (MHz)

OVS	2.4 kb/s	9.6 kb/s	19.2 kb/s	38.4 kb/s	57.6 kb/s	115.2 kb/s	0.576 Mb/s	1.152 Mb/s
3 (x4)	1.0 MHz	1.0 MHz	1.0 MHz	1.0 MHz	1.4 MHz	2.8 MHz	13.8 MHz	27.6 MHz
2 (x6)	1.0 MHz	1.0 MHz	1.0 MHz	1.4 MHz	2.1 MHz	4.1 MHz	20.7 MHz	41.5 MHz
1 (x8)	1.0 MHz	1.0 MHz	1.0 MHz	1.0 MHz	1.4 MHz	2.8 MHz	13.8 MHz	27.6 MHz
0 (x16)	1.0 MHz	1.0 MHz	1.0 MHz	1.0 MHz	1.1 MHz	2.2 MHz	11.1 MHz	22.1 MHz

Note that by default, the idle value of the EUSART data signal is high. This means that the IrDA modulator generates negative pulses, and the IrDA demodulator expects negative pulses. To make the IrDA module use RZI signalling, both TXINV and RXINV in EUSARTn_CFG0 must be set.

Since the incoming signal is only sampled on positive clock edges, the width of the incoming pulses must be at least two clk_per periods wide for reliable detection by the receiver.

21.3.2.18.2 IRLF

IRLF only supports RX operation. This feature will stay operational even in EM2. It is possible to cause a wake up when a certain frame is received and then switch to IRHF if TX is required. IRLFEN in IRLFCFG must be set for this to work.

21.3.2.19 DALI operation

EUSART supports DALI (Digitally Addressable Lighting Interface) operation using both HF and LF clocks. DALICFG register holds the configuration for DALI operation. Once DALIEN is set to 1 in DALICFG, DALI mode gets enabled. DALI is available only in EUSART asynchronous mode, i.e., SYNC field in CFG0 register must be set to 0.

21.3.2.19.1 DALI Frame Format

DALI frames are Manchester encoded. Details:

- The TX/RX lines are high when idle.
- The Start bit is Manchester encoded to logic 1.
- Data bits are progammable (from 8-32) and are also Manchester encoded.
- Each DALI frame has two Stop bits, which are represented by a high on the line (same as idle status).
- DALI frame does not have parity bits.

DALI TX and RX data bits are independently programmable (each being from 8 to 32) using DALITXDATABITS and DALIRXDATABITS in the DALICFG register. The DALI bus is half-duplex so everything transmitted on the EUSART DALI TX pin will also show up on EUSART DALI RX pin. In order to ensure that whatever is sent out by EUSART TX is not sampled by EUSART RX, RX enable gets automatically masked to low during an active EUSART transmission. Once the transmission completes, the masking is removed (so if RX was enabled, removing the masking will result in RX getting enabled again and if RX was not enabled, RX enable will stay low even after removing the masking. This feature can be overridden for debugging by setting DALIRXENDT to 1 in DALICFG register. In that case, RX enable will not get masked during EUSART TX (i.e., if EUSART RX was already enabled, it will stay enabled during EUSART TX operation) and whatever is sent out will also be received by EUSART itself. In this case, it is important to set DALIRXDATABITS the same as DALITXDATABITS.

If LOOPBK in CFG0 is set to 1 in order to do loopback testing for DALI, then in this case DALIRXENDT should be set to 1 and DALIRXDATABITS should be set the same as DALITXDATABITS. Advantage of DALI loopback testing is that it can be done without connecting to an actual DALI bus since the data is looped back in from the TX pad.

21.3.2.19.2 DALI Baud Rate Formula

The EUSART clock defines DALI transmission and reception data rate. DALI mode supports any data rate from 300 baud up to 115.2 kbaud. DALI has a baudrate formula that differs from the standard EUSART UART mode baud rate formula. Whenever DALIEN in DALICFG is set to 1, then the DALI mode is enabled and the baud rate is given by Figure 21.14 DALI Baud Rate on page 641:

$$br = f_{EUSARTn}/(\text{oversample} \times 2 \times (1 + EUSARTn\_CLKDIV/256))$$

Figure 21.14. DALI Baud Rate

where $f_{EUSARTn}$ is the peripheral clock frequency and oversample is the oversampling rate as defined by OVS in EUSARTn_CFG0.

Given a desired baud rate brdesired, the clock divider EUSARTn_CLKDIV can be calculated by using Figure 21.15 DALI Desired Baud Rate DIV on page 641:

$$EUSARTn\_CLKDIV = 256 \times (f_{EUSARTn}/(\text{oversample} \times 2 \times brdesired) - 1)$$

Figure 21.15. DALI Desired Baud Rate DIV

The EUSART DALI mode can tolerate a 10% variation in baud rate as required in the DALI standard.

21.3.2.19.3 DALI Features

DALI mode is enabled by setting DALIEN to 1 in DALICFG register. A limited set of UART mode features are supported in DALI mode. Deatils below capture the feature set in DALI mode:

- A framing error interrupt (FERRIF) is generated if 2 stop bits are not received at the end of the frame. The received frame is still loaded into the RXDATA register.
- RXDATA and RXDATAP registers serve as RX FIFO. All 16 bits in these registers are treated as data in DALI mode. When DALI is disabled (DALIEN=0) while CFG0.SYNC=0, then these registers contain both data (max 9 bits) and also control information (PERR, FERR).
- When DALIEN is set to 1, then all 16 bits in TXDATA are treated as data. When DALIEN is 0 (DALI mode disabled) and CFG0.SYNC=0, then TXDATA contains both data bits and control bits.
- TXDATA and RXDATA registers are 16 bits wide but the DALI TX and RX data bits can be programmed to be anywhere between 8 and 32. In order to support data bits greater than 16 bits, special programming model applies. Please see the programming model section for details.
- DALI mode is not supported in EM2. TXDMAWU and RXDMAWU in CFG1 register are not supported in DALI mode.
- SKIPERRF feature in CFG0 register is not supported in DALI mode.
- ERRSDMA, ERRSRX and ERRSTX features in CFG0 register are not supported in DALI mode.
- Multiprocessor mode is not supported in DALI mode.
- TX-tristating is not supported in DALI mode. The TX pin is driven high when idle.
- Collision detection is not supported in DALi mode.
- Autobaud detection is not supported in DALI mode.
- Hardware flow control and DBGHALT are not supported in DALI mode.
- RXTIMEOUT and TXDELAY features are not supported in DALI mode.
- Start frame feature is not supported in DALI mode.
- All settings in FRAMECFG are not used in DALI mode. DALICFG register settings are used instead.
- RX blocking feature is not supported in DALI mode.
- IrDA feature (IRLFCFG, IRHFCFG) cannot be enabled while DALI mode is enabled.

21.3.3 Synchronous Operation

Synchronous mode shares some common features with asynchronous mode such as: Loopback, inversion of RX/TX, MSBF, TX/RX Interrupt watermarks. They both share the EUSARTn_TRIGCTRL, CMD, TXDATA, RXDATA, STATUS and Interrupt registers.

In synchronous mode, EUSART can be configured to work either as a main (clock driver) or secondary (clock receiver) interface through EUSARTn_CFG2.MASTER.

21.3.3.1 Frame Format

The frames used in synchronous mode need no start and stop bits since a single clock is available to all parts participating in the communication. Parity bits cannot be used in synchronous mode.

The EUSART supports frame lengths of 8 to 16 bits per frame. Larger frames can be simulated by transmitting multiple smaller frames, i.e. a 22 bit frame can be sent using two 11-bit frames, and a 24 bit frame can be generated by transmitting three 8-bit frames. The number of bits in a frame is set using DATABITS in EUSARTn_FRAMECFG.

The frames in synchronous mode are by default transmitted with the least significant bit first like in asynchronous mode. The bit-order can be reversed by setting MSBF in EUSARTn_CFG0.

The frame format used by the transmitter can be inverted by setting TXINV in EUSARTn_CFG0, and the format expected by the receiver can be inverted by setting RXINV, also in EUSARTn_CFG0.

21.3.3.2 Clock Generation

The bit-rate in synchronous mode is given by Figure 21.16 EUSART Synchronous Mode Bit Rate on page 643. The clock division is derived from EUSARTn_CFG2.SDIV, which is applicable when acting as a Main interface only.

$$br = f_{HFPERCLK}/(1 + EUSARTn\_CFG2.SDIV)$$

Figure 21.16. EUSART Synchronous Mode Bit Rate

Given a desired baud rate brdesired, the clock divider EUSARTn_CFG2.SDIV can be calculated using Figure 21.17 EUSART Synchronous Mode Clock Division Factor on page 643

$$EUSARTn\_CFG2.SDIV = (f_{HFPERCLK}/brdesired - 1)$$

Figure 21.17. EUSART Synchronous Mode Clock Division Factor

On every clock edge data on the data lines, MOSI and MISO, is either set up or sampled. When CLKPHA in EUSARTn_CTRL is cleared, data is sampled on the leading clock edge and set-up is done on the trailing edge. If CLKPHA is set however, data is set-up on the leading clock edge, and sampled on the trailing edge. In addition to this, the polarity of the clock signal can be changed by setting CLKPOL in EUSARTn_CTRL, which also defines the idle state of the clock. This results in four different modes which are summarized in Table 21.11 EUSART SPI Modes on page 643. Figure 21.18 EUSART SPI Timing on page 643 shows the resulting timing of data set-up and sampling relative to the bus clock.

Table 21.11. EUSART SPI Modes

SPI mode	CLKPOL	CLKPHA	Leading edge	Trailing edge
0	0	0	Rising, sample	Falling, set-up
1	0	1	Rising, set-up	Falling, sample
2	1	0	Falling, sample	Rising, set-up
3	1	1	Falling, set-up	Rising, sample

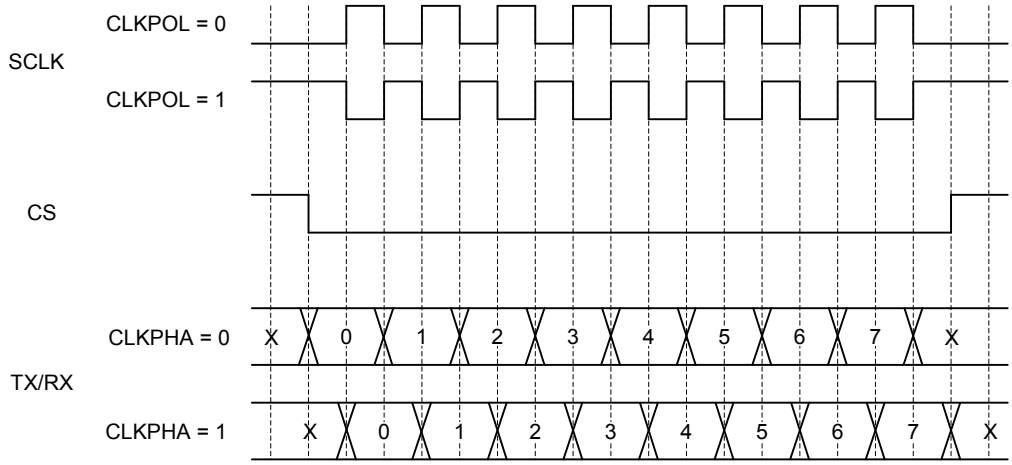


Figure 21.18. EUSART SPI Timing

The RX overflow interrupt flag, RXOF, is set at the end of the overflow frame if the receive FIFO is full. When a transfer has been performed, interrupt flags TXC are updated on the first setup clock edge of the succeeding frame, or when CS is deasserted.

21.3.3.3 Main SPI Interface Mode (Clock Driver)

EUSART operating as a main SPI interface is available only in EM0/EM1 with an HF clock source selected. When configured as a main interface, the EUSART is in full control of the data flow on the synchronous bus. When operating in full duplex mode, the secondary devices cannot transmit data to the main device without the main device transmitting to the secondary. The main device outputs the bus clock on SCLK.

Communication starts whenever there is data in the transmit FIFO and the transmitter is enabled. The EUSART clock then starts, and the main device shifts bits out from the transmit shift register using the internal clock.

When there are no more frames in the transmit FIFO and the transmit shift register is empty, the clock stops, and communication ends. When the receiver is enabled, it samples incoming data when the transmitter transmits data. Operation of the RX and TX FIFOs is as in asynchronous mode.

EUSARTn_CFG2.RXBLOCK can be used to block incoming RX data from pushing into RX FIFO.

21.3.3.4 Operation of CS Pin

When operating as a main interface, the CS pin can have one of two functions, or it can be disabled by clearing CSPEN in GPIO_EUSARn_ROUTEEN register.

If CS is disabled and there is a need to disable TX during the operation, then TX should be disabled at the end of transaction only indicated by the trigger of TXC interrupt to maintain synchronicity between TX and RX and avoid causing sudden stop to secondary devices.

If CS is configured as an output, it can be used to automatically generate a chip select for a single secondary device by setting AUTOCS in EUSARTn_CTRL. If AUTOCS is set, CS is activated before a transmission begins, and deactivated after the last bit has been transmitted and there is no more data in the transmit FIFO.

The time duration between assertion of CS and the start of transmission can be controlled using CSSETUP in EUSARTn_TIMINGCFG. If new data is ready for transmission before CS is deasserted, the data is sent without deasserting CS in between. CSHOLD in EUSARTn_TIMINGCFG keeps CS asserted after the end of frame for the number of baud-times specified.

By default, CS is active low, but its polarity can be inverted by setting CSINV in EUSARTn_CFG2.

21.3.3.5 AUTOTX

The main device on a synchronous bus is required to transmit data (send a clock) to a secondary device in order to receive data from that device. In some cases, only a few words are transmitted and a lot of data is then received from the secondary device. In that case, one solution is to keep feeding the TX with data to transmit, but that consumes system bandwidth. Instead AUTOTX can be used.

When AUTOTX in EUSARTn_CFG2 is set and TX FIFO is filled with initial data, EUSART will fully transmit the loaded data and then continue transmitting the last sent bit as long as there is available space in the RX FIFO for the chosen frame size. This happens even though there is no more data in the TX FIFO. The TX underflow interrupt flag TXUF in EUSARTn_IF is set on the first word that is transmitted which does not contain valid data.

During AUTOTX the EUSART will always send the previous sent bit, thus reducing the number of transitions on the TX output. So if the last bit sent was a 0, 0's will be sent during AUTOTX and if the last bit sent was a 1, 1's will be sent during AUTOTX.

21.3.3.6 Secondary SPI Interface Mode (Clock Receiver)

When the EUSART is in secondary interface mode, data transmission is not controlled by the EUSART, but by an external main SPI device. The EUSART is therefore not able to initiate a transmission, and has no control over the number of bytes written to the external main device.

The output and input to the EUSART are also swapped when in secondary mode, making the receiver take its input from TX (MOSI) and the transmitter drive RX (MISO).

To transmit data when in secondary mode, the device must load data into the transmit FIFO and enable the transmitter. The data will remain in the EUSART until the main device starts a transmission by pulling the CS input low and transmitting data. For every frame transmitted from main to secondary device, a frame is transferred from secondary to main as well.

If the transmitter is enabled in synchronous secondary mode and the main device starts transmission of a frame, the underflow interrupt flag TXUF in EUSARTn_IF will be set if no data is available for transmission. At the same time, the secondary device will transmit the default TX data, which can be set through EUSARTn_DTXDATCFG for the current and subsequent frames until the FIFO is filled. Note that when TX is enabled (with or without data in TXFIFO) in the middle of transaction, TXUF can be triggered if it's transmitting default TX data.

Similar to when operating as a synchronous main interface, EUSARTn_CFG2.RXBLOCK can be used to block incoming RX data from pushing into RX FIFO.

If the secondary device needs to control its own chip select signal, this can be achieved by clearing CSPEN in the GPIO_EUSARTn_ROUTEEN register. The internal chip select signal can then be controlled through CSINV in the CTRL register. The chip select signal will be CSINV inverted, i.e. if CSINV is cleared, the chip select is active and vice versa. In such cases, SCLK could arrive anytime that the device doesn't have prior notification from CS. Hence, EUSARTn_CFG2.FORCELOAD bit can be used to control how the device transmits the first dataword. If this bit is not set, the next outgoing dataword will be a DEFAULT TX data even if the FIFO had been loaded before SCLK arrives, followed by the loaded TX data. EUSARTn_IF.LOADERRIF Interrupt will never be triggered when EUSARTn_CFG2.FORCELOAD is not set. If this bit is set, as soon as the transmitter becomes ready the shift register will be loaded immediately and send data once SCLK arrives. The transmitter becomes ready when TX is enabled and TXFIFO is filled. On top of that, at word-boundary it will automatically trigger setup window check against the programmed EUSARTn_TIMINGCFG.SETUPWINDOW, which specifies the minimum duration (in APB bus clock cycles) between transmitter becoming ready and the incoming SCLK. If the measured duration is less than SETUPWINDOW bus clock cycles, an EUSARTn_IF.LOADERRIF Interrupt will be triggered. Besides, if the transmitter is enabled or disabled or the empty TXFIFO is loaded not at word-boundary during a transaction (SCLK is toggling), LOADERRIF will also be triggered immediately without checking for SETUPWINDOW. It's recommended that the transmitter should be ready while SCLK is idling or at word-boundary and at sufficient margin before SCLK toggles. Once LOADERRIF Interrupt is set, it may require to reset the secondary interface by disabling the module and re-enabling it because the transmitted data could be undeterministic.

21.3.4 Debug Halt

When DBGHALT in EUSART_CTRLX is clear, RTS is only dependent on the RX FIFO having space available to receive data. Incoming data is always received until both the RX FIFO is full and the RX shift register is full regardless of the state of DBGHALT or chip halt. Additional incoming data is discarded. When DBGHALT is set, RTS deasserts on RX FIFO full or when chip halt is high. However, a low pulse detected on chip halt will keep RTS asserted when no frame is being received. At the start of frame reception, RTS will deassert if chip halt is high and DBGHALT is set. This behavior allows single stepping to pulse the chip halt low for a cycle, and receive the next frame. The link partner must stop transmitting when RTS is deasserted, or the RX FIFO could overflow. All data in the transmit FIFO is sent out even when chip halt is asserted; therefore, the DMA will need to be set to stop sending the EUSART TX data during chip halt.

21.3.5 PRS-triggered Transmissions

If a transmission must be started on an event with very little delay, the PRS system can be used to trigger the transmission. The PRS channel to use as a trigger can be selected using TSEL in EUSARTn_TRIGCTRL. When a positive edge is detected on this signal, the receiver is enabled if RXTEN in EUSARTn_TRIGCTRL is set, and the transmitter is enabled if TXTEN in EUSARTn_TRIGCTRL is set. Only one signal input is supported by the EUSART.

AUTOTXTEN can also be combined with TXTEN to make the EUSART transmit a command to the external device prior to clocking out data. To do this, disable TX using the TXDIS command, load the TX FIFO with the command and enable AUTOTXTEN and TXTEN. When the selected PRS input goes high, the EUSART will now transmit the loaded command, and then continue clocking out while both the PRS input is high and there is room in the RX FIFO

21.3.6 PRS RX Input

The EUSART can be configured to receive data directly from a PRS channel by setting RXPRS in EUSARTn_INPUT. The PRS channel used is selected using RXPRSSEL in EUSARTn_INPUT. This way, for example, a differential RX signal can be input to the ACMP and the output routed via PRS to the EUSART.

21.3.7 PRS CLK Input

The EUSART can be configured to receive clock directly from a PRS channel by setting CLKPRS in EUSARTn_INPUT. The PRS channel used is selected using CLKPRSSEL in EUSARTn_INPUT. This is useful in secondary synchronous mode and can together with RX PRS input be used to input data from PRS.

21.3.8 DMA Support

The EUSART has full DMA support. The DMA controller can write to the transmit FIFO using the registers EUSARTn_TXDATA and it can read from the receive FIFO using the registers EUSARTn_RXDATA. This enables single byte transfers, 9 bit data + control/status bits, double byte and double byte + control/status transfers both to and from the EUSART.

A request for the DMA controller to read from the EUSART receive FIFO can come from the following source:

- Receive FIFO level satisfying EUSARTn_CFG1.RXFIW setting

A write request can come from one of the following sources:

- Transmit FIFO level satisfying EUSARTn_CFG1.TXFIW setting.

Even though there are two sources for write requests to the DMA, only one should be used at a time, since the requests from both sources are cleared even though only one of the requests are used.

In some cases, it may be sensible to temporarily stop DMA access to the EUSART when an error such as a framing error has occurred. This is enabled by setting ERRSDMA in EUSARTn_CTRL.

Note: For Synchronous mode full duplex operation, if both receive FIFO and transmit FIFO are served by DMA, to make sure receive FIFO is not overflowed the settings below should be followed.

- The DMA channel that serves receive FIFO should have higher priority than the DMA channel that serves transmit FIFO.
- IGNORESREQ should be set for both DMA channel.

21.4 EUSART Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	EUSART_IPVERSION	R	IP Version ID
0x004	EUSART_EN	RW ENABLE	Enable Register
0x008	EUSART_CFG0	RW CONFIG	Configuration 0 Register
0x00C	EUSART_CFG1	RW CONFIG	Configuration 1 Register
0x010	EUSART_CFG2	RW CONFIG	Configuration 2 Register
0x014	EUSART_FRAMECFG	RW CONFIG	Frame Format Register
0x018	EUSART_DTXDATCFG	RW CONFIG	Default TX DATA Register
0x01C	EUSART_IRHFCFG	RW CONFIG	HF IrDA Mod Config Register
0x020	EUSART_IRLFCFG	RW CONFIG	LF IrDA Pulse Config Register
0x024	EUSART_TIMINGCFG	RW CONFIG	Timing Register
0x028	EUSART_STARTFRAMECFG	RW CONFIG	Start Frame Register
0x02C	EUSART_SIGFRAMECFG	RW CONFIG	Signal Frame Register
0x030	EUSART_CLKDIV	RWH LFSYNC	Clock Divider Register
0x034	EUSART_TRIGCTRL	RW LFSYNC	Trigger Control Register
0x038	EUSART_CMD	W LFSYNC	Command Register
0x03C	EUSART_RXDATA	RH	RX Data Register
0x040	EUSART_RXDATAP	RH	RX Data Peek Register
0x044	EUSART_TXDATA	W	TX Data Register
0x048	EUSART_STATUS	RH	Status Register
0x04C	EUSART_IF	RWH INTFLAG	Interrupt Flag Register
0x050	EUSART_IEN	RW	Interrupt Enable Register
0x054	EUSART_SYNCBUSY	RH	Synchronization Busy Register
0x058	EUSART_DALICFG	RW CONFIG	DALI Config Register
0x1000	EUSART_IPVERSION_SET	R	IP Version ID
0x1004	EUSART_EN_SET	RW ENABLE	Enable Register
0x1008	EUSART_CFG0_SET	RW CONFIG	Configuration 0 Register
0x100C	EUSART_CFG1_SET	RW CONFIG	Configuration 1 Register
0x1010	EUSART_CFG2_SET	RW CONFIG	Configuration 2 Register
0x1014	EUSART_FRAMECFG_SET	RW CONFIG	Frame Format Register
0x1018	EUSART_DTXDATCFG_SET	RW CONFIG	Default TX DATA Register
0x101C	EUSART_IRHFCFG_SET	RW CONFIG	HF IrDA Mod Config Register
0x1020	EUSART_IRLFCFG_SET	RW CONFIG	LF IrDA Pulse Config Register
0x1024	EUSART_TIMINGCFG_SET	RW CONFIG	Timing Register
0x1028	EUSART_STARTFRA-MECFG_SET	RW CONFIG	Start Frame Register

Offset	Name	Type	Description
0x102C	EUSART_SIGFRAMECFG_SET	RW CONFIG	Signal Frame Register
0x1030	EUSART_CLKDIV_SET	RWH LFSYNC	Clock Divider Register
0x1034	EUSART_TRIGCTRL_SET	RW LFSYNC	Trigger Control Register
0x1038	EUSART_CMD_SET	W LFSYNC	Command Register
0x103C	EUSART_RXDATA_SET	RH	RX Data Register
0x1040	EUSART_RXDATAP_SET	RH	RX Data Peek Register
0x1044	EUSART_TXDATA_SET	W	TX Data Register
0x1048	EUSART_STATUS_SET	RH	Status Register
0x104C	EUSART_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x1050	EUSART_IEN_SET	RW	Interrupt Enable Register
0x1054	EUSART_SYNCBUSY_SET	RH	Synchronization Busy Register
0x1058	EUSART_DALICFG_SET	RW CONFIG	DALI Config Register
0x2000	EUSART_IPVERSION_CLR	R	IP Version ID
0x2004	EUSART_EN_CLR	RW ENABLE	Enable Register
0x2008	EUSART_CFG0_CLR	RW CONFIG	Configuration 0 Register
0x200C	EUSART_CFG1_CLR	RW CONFIG	Configuration 1 Register
0x2010	EUSART_CFG2_CLR	RW CONFIG	Configuration 2 Register
0x2014	EUSART_FRAMECFG_CLR	RW CONFIG	Frame Format Register
0x2018	EUSART_DTXDATCFG_CLR	RW CONFIG	Default TX DATA Register
0x201C	EUSART_IRHFCFG_CLR	RW CONFIG	HF IrDA Mod Config Register
0x2020	EUSART_IRLFCFG_CLR	RW CONFIG	LF IrDA Pulse Config Register
0x2024	EUSART_TIMINGCFG_CLR	RW CONFIG	Timing Register
0x2028	EUSART_STARTFRA-MECFG_CLR	RW CONFIG	Start Frame Register
0x202C	EUSART_SIGFRAMECFG_CLR	RW CONFIG	Signal Frame Register
0x2030	EUSART_CLKDIV_CLR	RWH LFSYNC	Clock Divider Register
0x2034	EUSART_TRIGCTRL_CLR	RW LFSYNC	Trigger Control Register
0x2038	EUSART_CMD_CLR	W LFSYNC	Command Register
0x203C	EUSART_RXDATA_CLR	RH	RX Data Register
0x2040	EUSART_RXDATAP_CLR	RH	RX Data Peek Register
0x2044	EUSART_TXDATA_CLR	W	TX Data Register
0x2048	EUSART_STATUS_CLR	RH	Status Register
0x204C	EUSART_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x2050	EUSART_IEN_CLR	RW	Interrupt Enable Register
0x2054	EUSART_SYNCBUSY_CLR	RH	Synchronization Busy Register
0x2058	EUSART_DALICFG_CLR	RW CONFIG	DALI Config Register
0x3000	EUSART_IPVERSION_TGL	R	IP Version ID

Offset	Name	Type	Description
0x3004	EUSART_EN_TGL	RW ENABLE	Enable Register
0x3008	EUSART_CFG0_TGL	RW CONFIG	Configuration 0 Register
0x300C	EUSART_CFG1_TGL	RW CONFIG	Configuration 1 Register
0x3010	EUSART_CFG2_TGL	RW CONFIG	Configuration 2 Register
0x3014	EUSART_FRAMECFG_TGL	RW CONFIG	Frame Format Register
0x3018	EUSART_DTXDATCFG_TGL	RW CONFIG	Default TX DATA Register
0x301C	EUSART_IRHFCFG_TGL	RW CONFIG	HF IrDA Mod Config Register
0x3020	EUSART_IRLFCFG_TGL	RW CONFIG	LF IrDA Pulse Config Register
0x3024	EUSART_TIMINGCFG_TGL	RW CONFIG	Timing Register
0x3028	EUSART_STARTFRA-MECFG_TGL	RW CONFIG	Start Frame Register
0x302C	EUSART_SIGFRAMECFG_TGL	RW CONFIG	Signal Frame Register
0x3030	EUSART_CLKDIV_TGL	RWH LFSYNC	Clock Divider Register
0x3034	EUSART_TRIGCTRL_TGL	RW LFSYNC	Trigger Control Register
0x3038	EUSART_CMD_TGL	W LFSYNC	Command Register
0x303C	EUSART_RXDATA_TGL	RH	RX Data Register
0x3040	EUSART_RXDATAP_TGL	RH	RX Data Peek Register
0x3044	EUSART_TXDATA_TGL	W	TX Data Register
0x3048	EUSART_STATUS_TGL	RH	Status Register
0x304C	EUSART_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x3050	EUSART_IEN_TGL	RW	Interrupt Enable Register
0x3054	EUSART_SYNCBUSY_TGL	RH	Synchronization Busy Register
0x3058	EUSART_DALICFG_TGL	RW CONFIG	DALI Config Register

21.5 EUSART Register Description

21.5.1 EUSART_IPVERSION - IP Version ID

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x2																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x2	R	**IP version ID**
	The read only IPVERSION field gives the version for this module. There may be minor software changes required for modules with different values of IPVERSION.			

21.5.2 EUSART_EN - Enable Register

Offset	Bit Position																															
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	RW
Name																															DISABLING	EN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DISABLING	0x0	R	**Disablement busy status**
	Disabling status when the module is disabled.			
0	EN	0x0	RW	**Module enable**
	Set to enable the module.			

21.5.3 EUSART_CFG0 - Configuration 0 Register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0						0x0	0x0	0x0		0x0			0x0			0x0	0x0			0x0			0x0			0x0	0x0	0x0	0x0	0x0
Access	RW	RW						RW	RW	RW		RW			RW			RW	RW			RW			RW			RW	RW	RW	RW	RW
Name	AUTOBAUDEN	MVDIS						ERRSTX	ERRSRX	ERRSDMA		SKIPPERRF			AUTOTRI			TXINV	RXINV			MSBF			OVS			MPAB	MPM	CCEN	LOOPBK	SYNC

Bit	Name	Reset	Access	Description
31	AUTOBAUDEN	0x0	RW	**AUTOBAUD detection enable**
	Detects the baud rate based on receiving a 0x55 frame (0x00 for IrDA). Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
30	MVDIS	0x0	RW	**Majority Vote Disable**
	Disable majority vote for 16x, 8x and 6x oversampling modes. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
29:25	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
24	ERRSTX	0x0	RW	**Disable TX On Error**
	When set, the transmitter is disabled on framing and parity errors in the receiver. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			

Value	Mode	Description
0	DISABLE	Received framing and parity errors have no effect on transmitter
1	ENABLE	Received framing and parity errors disable the transmitter

Bit	Name	Reset	Access	Description
23	ERRSRX	0x0	RW	**Disable RX On Error**
	When set, the receiver is disabled on framing and parity errors. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			

Value	Mode	Description
0	DISABLE	Framing and parity errors have no effect on receiver
1	ENABLE	Framing and parity errors disable the receiver

Bit	Name	Reset	Access	Description
22	ERRSDMA	0x0	RW	**Halt DMA Read On Error**
	When set, DMA read requests will be cleared on framing and parity errors. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			

Value	Mode	Description
0	DISABLE	Framing and parity errors have no effect on DMA requests from the EUSART
1	ENABLE	DMA requests from the EUSART are blocked while the PERR or FERR interrupt flags are set

Bit	Name	Reset	Access	Description
21	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

Bit	Name	Reset	Access	Description
20	SKIPPERRF	0x0	RW	**Skip Parity Error Frames**
	When set, the receiver discards frames with parity errors. The PERR interrupt flag is still set. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
19:18	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
17	AUTOTRI	0x0	RW	**Automatic TX Tristate**
	When enabled, TXTRI is set by hardware whenever the transmitter is idle, and TXTRI is cleared by hardware when transmission starts. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			

Value	Mode	Description
0	DISABLE	The output on UARTn_TX when the transmitter is idle is defined by TXINV
1	ENABLE	UARTn_TX is tristated whenever the transmitter is idle

16:15	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
14	TXINV	0x0	RW	**Transmitter output Invert**
	The output from the EUSART transmitter can optionally be inverted by setting this bit.			

Value	Mode	Description
0	DISABLE	Output from the transmitter is passed unchanged to UARTn_TX
1	ENABLE	Output from the transmitter is inverted before it is passed to UARTn_TX

13	RXINV	0x0	RW	**Receiver Input Invert**
	Setting this bit will invert the input to the EUSART receiver.			

Value	Mode	Description
0	DISABLE	Input is passed directly to the receiver
1	ENABLE	Input is inverted before it is passed to the receiver

12:11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10	MSBF	0x0	RW	**Most Significant Bit First**
	Decides whether data is sent with the least significant bit first, or the most significant bit first.			

Value	Mode	Description
0	DISABLE	Data is sent with the least significant bit first
1	ENABLE	Data is sent with the most significant bit first

9:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:5	OVS	0x0	RW	**Oversampling**
	Sets the number of clock periods in a EUSART bit-period. More clock cycles gives better robustness, while less clock cycles gives better performance. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			

Value	Mode	Description

Bit	Name	Reset	Access	Description
	0	X16		16X oversampling
	1	X8		8X oversampling
	2	X6		6X oversampling
	3	X4		4X oversampling
	4	DISABLE		Disable oversampling (for LF operation)
4	MPAB	0x0	RW	**Multi-Processor Address-Bit**
	Defines the value of the multi-processor address bit. An incoming frame with its 9th bit equal to the value of this bit marks the frame as a multi-processor address frame. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
3	MPM	0x0	RW	**Multi-Processor Mode**
	Multi-processor mode uses the 9th bit of the EUSART frames to tell whether the frame is an address frame or a data frame. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
	Value	Mode		Description
	0	DISABLE		The 9th bit of incoming frames has no special function
	1	ENABLE		An incoming frame with the 9th bit equal to MPAB will be loaded into the RX FIFO regardless of RXBLOCK and will result in the MPAB interrupt flag being set
2	CCEN	0x0	RW	**Collision Check Enable**
	Enables collision checking on data when operating in half duplex modus. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
	Value	Mode		Description
	0	DISABLE		Collision check is disabled
	1	ENABLE		Collision check is enabled. The receiver must be enabled for the check to be performed
1	LOOPBK	0x0	RW	**Loopback Enable**
	Allows the receiver to be connected directly to the EUSART transmitter for loopback and half duplex communication.			
	Value	Mode		Description
	0	DISABLE		The receiver is connected to and receives data from UARTn_RX
	1	ENABLE		The receiver is connected to and receives data from UARTn_TX
0	SYNC	0x0	RW	**Synchronous Mode**
	Determines whether the EUSART is operating in asynchronous or synchronous mode. When switching between SYNC and ASYNC mode, module Disablement is required.			
	Value	Mode		Description
	0	ASYNC		The EUSART operates in asynchronous mode
	1	SYNC		The EUSART operates in synchronous mode

21.5.4 EUSART_CFG1 - Configuration 1 Register

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset		0x0					0x0						0x0				0x0				0x0	0x0	0x0			0x0			0x0	0x0	0x0	0x0
Access		RW					RW						RW				RW				RW	RW	RW			RW			RW	RW	RW	RW
Name		RXFIW					RTSRXFW						TXFIW				RXPRSEN				SFUBRX	RXDMAWU	TXDMAWU			RXTIMEOUT			RTSINV	CTSEN	CTSINV	DBGHALT

Bit	Name	Reset	Access	Description
31	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
30:27	RXFIW	0x0	RW	**RX FIFO Interrupt Watermark**

Determines the interrupt and status level of the Receive FIFO. Also impacts RX DMA request.

Value	Mode	Description
0	ONEFRAME	RXFL status flag and IF are set when the RX FIFO has at least one frame in it.
1	TWOFRAMES	RXFL status flag and IF are set when the RX FIFO has at least two frames in it.
2	THREEFRAMES	RXFL status flag and IF are set when the RX FIFO has at least three frames in it.
3	FOURFRAMES	RXFL status flag and IF are set when the RX FIFO has at least four frames in it.
4	FIVEFRAMES	RXFL status flag and IF are set when the RX FIFO has at least five frames in it.
5	SIXFRAMES	RXFL status flag and IF are set when the RX FIFO has at least six frames in it.
6	SEVENFRAMES	RXFL status flag and IF are set when the RX FIFO has at least seven frames in it.
7	EIGHTFRAMES	RXFL status flag and IF are set when the RX FIFO has at least eight frames in it.
8	NINEFRAMES	RXFL status flag and IF are set when the RX FIFO has at least nine frames in it.
9	TENFRAMES	RXFL status flag and IF are set when the RX FIFO has at least ten frames in it.
10	ELEVENFRAMES	RXFL status flag and IF are set when the RX FIFO has at least eleven frames in it.
11	TWELVEFRAMES	RXFL status flag and IF are set when the RX FIFO has at least twelve frames in it.
12	THIRTEENFRAMES	RXFL status flag and IF are set when the RX FIFO has at least thriteen frames in it.
13	FOURTEENFRAMES	RXFL status flag and IF are set when the RX FIFO has at least fourteen frames in it.

Bit	Name	Reset	Access	Description
	14	FIFTEENFRAMES		RXFL status flag and IF are set when the RX FIFO has at least fifteen frames in it.
	15	SIXTEENFRAMES		RXFL status flag and IF are set when the RX FIFO has at least sixteen frames in it.
26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25:22	RTSRXFW	0x0	RW	**Request-to-send RX FIFO Watermark**
	Set Request-to-send watermark level. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
	Value	Mode		Description
	0	ONEFRAME		RTS is set if there is space for at least one more frame in the RX FIFO.
	1	TWOFRAMES		RTS is set if there is space for at least two more frames in the RX FIFO.
	2	THREEFRAMES		RTS is set if there is space for at least three more frames in the RX FIFO.
	3	FOURFRAMES		RTS is set if there is space for four more frames in the RX FIFO.
	4	FIVEFRAMES		RTS is set if there is space for five more frames in the RX FIFO.
	5	SIXFRAMES		RTS is set if there is space for six more frames in the RX FIFO.
	6	SEVENFRAMES		RTS is set if there is space for seven more frames in the RX FIFO.
	7	EIGHTFRAMES		RTS is set if there is space for eight more frames in the RX FIFO.
	8	NINEFRAMES		RTS is set if there is space for nine more frames in the RX FIFO.
	9	TENFRAMES		RTS is set if there is space for ten more frames in the RX FIFO.
	10	ELEVENFRAMES		RTS is set if there is space for eleven more frames in the RX FIFO.
	11	TWELVEFRAMES		RTS is set if there is space for twelve more frames in the RX FIFO.
	12	THIRTEENFRAMES		RTS is set if there is space for thirteen more frames in the RX FIFO.
	13	FOURTEENFRAMES		RTS is set if there is space for fourteen more frames in the RX FIFO.
	14	FIFTEENFRAMES		RTS is set if there is space for fifteen more frames in the RX FIFO.
	15	SIXTEENFRAMES		RTS is set if there is space for sixteen more frames in the RX FIFO.
21:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	TXFIW	0x0	RW	**TX FIFO Interrupt Watermark**
	Determines the interrupt and status level of the transmit FIFO. Also impacts TX DMA request.			
	Value	Mode		Description

Bit	Name	Reset	Access	Description
	0	ONEFRAME		TXFL status flag and IF are set when the TX FIFO has space for at least one more frame.
	1	TWOFRAMES		TXFL status flag and IF are set when the TX FIFO has space for at least two more frames.
	2	THREEFRAMES		TXFL status flag and IF are set when the TX FIFO has space for at least three more frames.
	3	FOURFRAMES		TXFL status flag and IF are set when the TX FIFO has space for at least four more frames.
	4	FIVEFRAMES		TXFL status flag and IF are set when the TX FIFO has space for at least five more frames.
	5	SIXFRAMES		TXFL status flag and IF are set when the TX FIFO has space for at least six more frames.
	6	SEVENFRAMES		TXFL status flag and IF are set when the TX FIFO has space for at least seven more frames.
	7	EIGHTFRAMES		TXFL status flag and IF are set when the TX FIFO has space for at least eight more frames.
	8	NINEFRAMES		TXFL status flag and IF are set when the TX FIFO has space for at least nine more frames.
	9	TENFRAMES		TXFL status flag and IF are set when the TX FIFO has space for at least ten more frames.
	10	ELEVENFRAMES		TXFL status flag and IF are set when the TX FIFO has space for at least eleven more frames.
	11	TWELVEFRAMES		TXFL status flag and IF are set when the TX FIFO has space for at least twelve more frames.
	12	THIRTEENFRAMES		TXFL status flag and IF are set when the TX FIFO has space for at least thriteen more frames.
	13	FOURTEENFRAMES		TXFL status flag and IF are set when the TX FIFO has space for at least fourteen more frames.
	14	FIFTEENFRAMES		TXFL status flag and IF are set when the TX FIFO has space for at least fifteen more frames.
	15	SIXTEENFRAMES		TXFL status flag and IF are set when the TX FIFO has space for at least sixteen more frames.
15	RXPRSEN	0x0	RW	**PRS RX Enable**
	When set, the PRS channel selected as input to RX.			
14:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11	SFUBRX	0x0	RW	**Start Frame Unblock Receiver**
	Set to unblock RX on Start frame reception. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
10	RXDMAWU	0x0	RW	**Receiver DMA Wakeup**
	Set to enable wakeup from EM2 to EM1 for DMA/ RX interaction. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
9	TXDMAWU	0x0	RW	**Transmitter DMA Wakeup**
	Set to enable wakeup from EM2 to EM1 for DMA/ TX interaction. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			

Bit	Name	Reset	Access	Description
8:7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:4	RXTIMEOUT	0x0	RW	**RX Timeout**

When enabled, determines how long, in units of frame, RX needs to remain idle after a frame reception before RXTOIF gets set. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.

Value	Mode	Description
0	DISABLED	
1	ONEFRAME	
2	TWOFRAMES	
3	THREEFRAMES	
4	FOURFRAMES	
5	FIVEFRAMES	
6	SIXFRAMES	
7	SEVENFRAMES	

3	RTSINV	0x0	RW	**Request-to-send Invert Enable**

When set, the RTS pin polarity is inverted. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.

Value	Mode	Description
0	DISABLE	The RTS pin is active low
1	ENABLE	The RTS pin is active high

2	CTSEN	0x0	RW	**Clear-to-send Enable**

When set, frames in the TX FIFO will not be sent until link partner asserts CTS. Any data in the TX shift register will continue transmitting, the next TX FIFO data will not load into the TX shift register. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.

Value	Mode	Description
0	DISABLE	Ignore CTS
1	ENABLE	Stop transmitting when CTS is inactive

1	CTSINV	0x0	RW	**Clear-to-send Invert Enable**

When set, the CTS pin polarity is inverted. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.

Value	Mode	Description
0	DISABLE	The CTS pin is active low
1	ENABLE	The CTS pin is active high

0	DBGHALT	0x0	RW	**Debug halt**

Set to halt operation when core is halted. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.

Value	Mode	Description
0	DISABLE	Continue normal EUSART operation even if core is halted

Bit	Name	Reset	Access	Description
	1	ENABLE		If core is halted, receive one frame and then halt reception by deactivating RTS. Next frame reception happens when the core is unhalted during single stepping.

21.5.5 EUSART_CFG2 - Configuration 2 Register

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																								0x0	0x0	0x1	0x0	0x0	0x0	0x0	0x0
Access	RW																								RW	RW	RW	RW	RW	RW	RW	RW
Name	SDIV																								FORCELOAD	CLKPRSEN	AUTOCS	AUTOTX	CSINV	CLKPHA	CLKPOL	MASTER

Bit	Name	Reset	Access	Description
31:24	SDIV	0x0	RW	**Sync Clock Div**
	Sets the clock rate for synchronous main mode operation only (To set the clock rate for asynchronous operation, see the CLKDIV field). Clock division value = SDIV + 1. Only applicable when CFG0.SYNC bit is set to 'SYNC' and CFG2.MASTER is set to 'MASTER'.			
23:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7	FORCELOAD	0x0	RW	**Force Load to Shift Register**
	When this bit is set, if TXEN is already enabled, any loading of an empty FIFO will immediately load the data into the shift register. This bit is recommended to be used in 3-wire setting where CS is not used, or in a custom 4-wire mode where SCLK is in long idle state between two transactions with CS always in active mode (this typically happens between 2 transactions where the main interface holds SCLK idling to give additional time for the secondary interface to load data). If FORCELOAD bit is not set, the next out-going frame will be a DEFAULT TX data, followed by the loaded TX data in TX FIFO. When FORCELOAD is set, it will automatically trigger setup window check against the programmed EUSARTn_TIMINGCFG.SETUPWINDOW, which specifies the minimum duration between empty fifo loading event and first encountered edge of SCLK. If the measured duration is less than SETUPWINDOW bus clock cycles, a EUSARTn_IF.LOADERRIF Interrupt will be triggered. Only applicable when CFG0.SYNC bit is set to 'SYNC' and CFG2.MASTER is set to 'SLAVE'.			
6	CLKPRSEN	0x0	RW	**PRS CLK Enable**
	When set, the PRS channel selected as input to CLK. Only applicable when CFG0.SYNC bit is set to 'SYNC' and CFG2.MASTER is set to 'SLAVE'.			
5	AUTOCS	0x1	RW	**Automatic Chip Select**
	When enabled, the output on CS will be activated one baud-period before transmission starts, and deactivated when transmission ends. Only applicable when CFG0.SYNC bit is set to 'SYNC' and CFG2.MASTER is set to 'MASTER'.			
4	AUTOTX	0x0	RW	**Always Transmit When RXFIFO Not Full**
	Transmits as long as RXFIFO is not full. If TX is empty, underflows are generated. Only applicable when CFG0.SYNC bit is set to 'SYNC' and CFG2.MASTER is set to 'MASTER'.			
3	CSINV	0x0	RW	**Chip Select Invert**
	Default value is active low. This affects both the selection of external secondary devices, as well as the selection of the microcontroller in secondary mode. Only applicable when CFG0.SYNC bit is set to 'SYNC'.			

Value	Mode	Description
0	AL	Chip select is active low
1	AH	Chip select is active high

Bit	Name	Reset	Access	Description
2	CLKPHA	0x0	RW	**Clock Edge for Setup/Sample**

Bit	Name	Reset	Access	Description
	Determines where data is set-up and sampled according to the bus clock when in synchronous mode. Only applicable when CFG0.SYNC bit is set to 'SYNC'.			

Value	Mode	Description
0	SAMPLELEADING	Data is sampled on the leading edge and set-up on the trailing edge of the bus clock in synchronous mode
1	SAMPLETRAILING	Data is set-up on the leading edge and sampled on the trailing edge of the bus clock in synchronous mode

Bit	Name	Reset	Access	Description
1	CLKPOL	0x0	RW	**Clock Polarity**
	Determines the clock polarity of the bus clock used in synchronous mode. Only applicable when CFG0.SYNC bit is set to 'SYNC'.			

Value	Mode	Description
0	IDLELOW	The bus clock used in synchronous mode has a low base value
1	IDLEHIGH	The bus clock used in synchronous mode has a high base value

Bit	Name	Reset	Access	Description
0	MASTER	0x0	RW	**Main mode**
	Set this bit to put EUSART to main interface mode. When unset, EUSART operates in secondary interface mode. When changing between Main and Secondary mode, module Disablement is required. Only applicable when CFG0.SYNC bit is set to 'SYNC'.			

Value	Mode	Description
0	SLAVE	Secondary mode
1	MASTER	Main mode

21.5.6 EUSART_FRAMECFG - Frame Format Register

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																			0x1				0x0						0x2			
Access																			RW				RW						RW			
Name																			STOPBITS				PARITY						DATABITS			

Bit	Name	Reset	Access	Description
31:14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13:12	STOPBITS	0x1	RW	**Stop-Bit Mode**

Determines the number of stop-bits used. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.

Value	Mode	Description
0	HALF	The transmitter generates a half stop bit. Stop-bits are not verified by receiver
1	ONE	One stop bit is generated and verified
2	ONEANDAHALF	The transmitter generates one and a half stop bit. The receiver verifies the first stop bit
3	TWO	The transmitter generates two stop bits. The receiver checks the first stop-bit only

11:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	PARITY	0x0	RW	**Parity-Bit Mode**

Determines whether parity bits are enabled, and whether even or odd parity should be used. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.

Value	Mode	Description
0	NONE	Parity bits are not used
2	EVEN	Even parity are used. Parity bits are automatically generated and checked by hardware.
3	ODD	Odd parity is used. Parity bits are automatically generated and checked by hardware.

7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	DATABITS	0x2	RW	**Data-Bit Mode**

Sets the number of data bits in a EUSART frame.

Value	Mode	Description
1	SEVEN	Each frame contains 7 data bits
2	EIGHT	Each frame contains 8 data bits

Bit	Name	Reset	Access	Description
	3	NINE		Each frame contains 9 data bits
	4	TEN		Each frame contains 10 data bits
	5	ELEVEN		Each frame contains 11 data bits
	6	TWELVE		Each frame contains 12 data bits
	7	THIRTEEN		Each frame contains 13 data bits
	8	FOURTEEN		Each frame contains 14 data bits
	9	FIFTEEN		Each frame contains 15 data bits
	10	SIXTEEN		Each frame contains 16 data bits

21.5.7 EUSART_DTXDATCFG - Default TX DATA Register

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									RW							
Name																									DTXDAT							

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	DTXDAT	0x0	RW	**Default TX DATA**
	This is the default transmitted data when the TXFIFO is empty. Only applicable when CFG0.SYNC bit is set to 'SYNC' and CFG2.MASTER is set to 'SLAVE'.			

21.5.8 EUSART_IRHFCFG - HF IrDA Mod Config Register

Offset	Bit Position																															
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0	0x0		0x0
Access																													RW	RW		RW
Name																													IRHFFILT	IRHFPW		IRHFEN

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	IRHFFILT	0x0	RW	**IrDA RX Filter**
	Set to enable filter on demodulator.			

Value	Mode	Description
0	DISABLE	No filter enabled
1	ENABLE	Filter enabled. IrDA pulse must be high for at least 5 consecutive clock cycles to be detected

Bit	Name	Reset	Access	Description
2:1	IRHFPW	0x0	RW	**IrDA TX Pulse Width**
	Configure the pulse width generated by the modulator as a fraction of the configured EUSART bit period.			

Value	Mode	Description
0	ONE	IrDA pulse width is 1/16 for OVS=0 and 1/8 for OVS=1
1	TWO	IrDA pulse width is 2/16 for OVS=0 and 2/8 for OVS=1
2	THREE	IrDA pulse width is 3/16 for OVS=0 and 3/8 for OVS=1
3	FOUR	IrDA pulse width is 4/16 for OVS=0 and 4/8 for OVS=1

Bit	Name	Reset	Access	Description
0	IRHFEN	0x0	RW	**Enable IrDA Module**
	Enable IrDA module and route EUSART signals through it. Used when EUSART has HF clock. Only applicable when CFG0.SYNC bit is set to 'ASYNC'			

21.5.9 EUSART_IRLFCFG - LF IrDA Pulse Config Register

Offset	Bit Position																															
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																RW
Name																																IRLFEN

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	IRLFEN	0x0	RW	**Pulse Generator/Extender Enable** Filter EUSART output through pulse generator and the EUSART input through the pulse extender. Used for LF operation. Only applicable when CFG0.SYNC bit is set to 'ASYNC'

21.5.10 EUSART_TIMINGCFG - Timing Register

Offset	Bit Position																													
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x5					0x0				0x0				0x0					0x0	
Access													RW					RW				RW				RW					RW	
Name													SETUPWINDOW					ICS				CSHOLD				CSSETUP					TXDELAY	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	SETUPWINDOW	0x5	RW	**Setup Window**
	When CFG2.FORCELOAD is set, this defines the number of bus clock cycles that empty FIFO load or enabling of TX or disabling of TX must be performed before the sampling edge of SCLK at word-boundary to avoid load error. Word boundary is defined as followings:before the transaction starts, or between 2 transactions or the first bit between 2 datawords. If baud-rate is more than 5 MHz, a value of 4 is recommended, any values smaller than that can be tried out but avoid using 0. If baud-rate is less than 5 MHz, value of 5 is recommended, any values higher than 5 can be used but it may make the load error easy to occur. The recommended values for frequency bands should be sufficient to work all the time. Only applicable when CFG0.SYNC bit is set to 'SYNC' and CFG2.MASTER is set to 'SLAVE' and CFG2.FORCELOAD is set.			
15	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
14:12	ICS	0x0	RW	**Inter-Character Spacing**
	Inter-character spacing after each TX frame while the TX FIFO is not empty. Only applicable when CFG0.SYNC bit is set to 'SYNC' and CFG2.MASTER is set to 'MASTER'.			

Value	Mode	Description
0	ZERO	There is no space between charcters
1	ONE	Create a space of 1 baud-times between frames
2	TWO	Create a space of 2 baud-times between frames
3	THREE	Create a space of 3 baud-times between frames
4	FOUR	Create a space of 4 baud-times between frames
5	FIVE	Create a space of 5 baud-times between frames
6	SIX	Create a space of 6 baud-times between frames
7	SEVEN	Create a space of 7 baud-times between frames

11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10:8	CSHOLD	0x0	RW	**Chip Select Hold**
	Chip Select will be de-asserted after the end of frame transmission. Only applicable when CFG0.SYNC bit is set to 'SYNC' and CFG2.MASTER is set to 'MASTER'.			

Value	Mode	Description

Bit	Name	Reset	Access	Description
	0	ZERO		CS is de-asserted half or 1 baud-time after the end of transmission depending on CLKPHASE equal to 1 or 0 respectively
	1	ONE		CS is de-asserted 1 additional baud-time after the end of transmission
	2	TWO		CS is de-asserted 2 additional baud-times after the end of transmission
	3	THREE		CS is de-asserted 3 additional baud-times after the end of transmission
	4	FOUR		CS is de-asserted 4 additional baud-times after the end of transmission
	5	FIVE		CS is de-asserted 5 additional baud-times after the end of transmission
	6	SIX		CS is de-asserted 6 additional baud-times after the end of transmission
	7	SEVEN		CS is de-asserted 7 additional baud-times after the end of transmission
7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:4	CSSETUP	0x0	RW	**Chip Select Setup**
	Chip Select will be asserted before the start of frame transmission. Only applicable when CFG0.SYNC bit is set to 'SYNC' and CFG2.MASTER is set to 'MASTER'.			
	Value	Mode		Description
	0	ZERO		CS is asserted half or 1 baud-time before the start of transmission depending on CLKPHASE equal to 1 or 0 respectively
	1	ONE		CS is asserted 1 additional baud-time before start of transmission
	2	TWO		CS is asserted 2 additional baud-times before start of transmission
	3	THREE		CS is asserted 3 additional baud-times before start of transmission
	4	FOUR		CS is asserted 4 additional baud-times before start of transmission
	5	FIVE		CS is asserted 5 additional baud-times before start of transmission
	6	SIX		CS is asserted 6 additional baud-times before start of transmission
	7	SEVEN		CS is asserted 7 additional baud-times before start of transmission
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	TXDELAY	0x0	RW	**TX Delay Transmission**
	Configurable delay before new rtansfers. Frames sent back-to-back are not delayed. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
	Value	Mode		Description

Bit	Name	Reset	Access	Description
	0	NONE		Frames are transmitted immediately.
	1	SINGLE		Transmission of new frames is delayed by a single bit period.
	2	DOUBLE		Transmission of new frames is delayed by a two bit periods.
	3	TRIPPLE		Transmission of new frames is delayed by a three bit periods.

21.5.11 EUSART_STARTFRAMECFG - Start Frame Register

Offset	Bit Position																															
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0				
Access																												RW				
Name																												STARTFRAME				

Bit	Name	Reset	Access	Description
31:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8:0	STARTFRAME	0x0	RW	**Start Frame**
	When a frame matching STARTFRAME is received, the receiver detects that and STARTF interrupt flag is set. If SFUBRX is set, RXBLOCK is cleared and the start frame is loaded in to the RX FIFO. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			

21.5.12 EUSART_SIGFRAMECFG - Signal Frame Register

Offset	Bit Position																															
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																0x0																
Access																RW																
Name																SIGFRAME																

Bit	Name	Reset	Access	Description
31:0	SIGFRAME	0x0	RW	**Signal Frame Value**
	When a frame matching SIGFRAME is detected by the receiver, SIGF interrupt flag is set. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			

21.5.13 EUSART_CLKDIV - Clock Divider Register

Offset	Bit Position																															
0x030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset										0x0																						
Access										RW																						
Name										DIV																						

Bit	Name	Reset	Access	Description
31:23	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
22:3	DIV	0x0	RW	**Fractional Clock Divider**
	Specifies the fractional clock divider. Setting AUTOBAUDEN in CFG1 register will overwrite the DIV field. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
2:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

21.5.14 EUSART_TRIGCTRL - Trigger Control Register

Offset	Bit Position																															
0x034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x0	0x0	0x0
Access																														RW	RW	RW
Name																														AUTOTXTEN	TXTEN	RXTEN

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	AUTOTXTEN	0x0	RW	**AUTOTX Trigger Enable**
	When set, AUTOTX is enabled as long as the selected PRS channel has a high value. Only applicable when CFG0.SYNC bit is set to 'SYNC' and CFG2.MASTER is set to 'MASTER'.			
1	TXTEN	0x0	RW	**Transmit Trigger Enable**
	When set, the positive edge of the selected PRS channel sets TXEN, enabling the transmitter.			
0	RXTEN	0x0	RW	**Receive Trigger Enable**
	When set, the positive edge of the selected PRS channel sets RXEN, enabling the receiver.			

21.5.15 EUSART_CMD - Command Register

Offset	Bit Position																															
0x038	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																								0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																								W(nB)	W(nB)	W(nB)	W(nB)	W(nB)	W(nB)	W(nB)	W(nB)	W(nB)
Name																								CLEARTX	TXTRIDIS	TXTRIEN	RXBLOCKDIS	RXBLOCKEN	TXDIS	TXEN	RXDIS	RXEN

Bit	Name	Reset	Access	Description
31:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8	CLEARTX	0x0	W(nB)	**Clear TX FIFO**
	Set to clear TX FIFO. Only applicable when CFG0.SYNC bit is set to 'ASYNC'. Note that before issuing this command, firmware should first set the transmitter disable bit (CMD.TXDIS) and then poll the transmitter enable status bit until cleared (STATUS.TXENS).			
7	TXTRIDIS	0x0	W(nB)	**Transmitter Tristate Disable**
	Disables tristating of the transmitter output.			
6	TXTRIEN	0x0	W(nB)	**Transmitter Tristate Enable**
	Tristates the transmitter output. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
5	RXBLOCKDIS	0x0	W(nB)	**Receiver Block Disable**
	Set to clear RXBLOCK, resulting in all incoming frames being loaded into the RX FIFO.			
4	RXBLOCKEN	0x0	W(nB)	**Receiver Block Enable**
	Set to set RXBLOCK, resulting in all incoming frames being discarded.			
3	TXDIS	0x0	W(nB)	**Transmitter Disable**
	Set to disable transmission. STATUS.TXENS should be polled to ensure disabled status in Synchrounous mode.			
2	TXEN	0x0	W(nB)	**Transmitter Enable**
	Set to enable data transmission. STATUS.TXENS should be polled to ensure enabled status in Synchrounous mode.			
1	RXDIS	0x0	W(nB)	**Receiver Disable**
	Set to disable data reception. If a frame is under reception when the receiver is disabled, the incoming frame is discarded. STATUS.RXENS should be polled to ensure disabled status in Synchrounous mode.			
0	RXEN	0x0	W(nB)	**Receiver Enable**
	Set to activate data reception. STATUS.RXENS should be polled to ensure enabled status in Synchrounous mode.			

21.5.16 EUSART_RXDATA - RX Data Register

Offset	Bit Position																													
0x03C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									R							
Name																									RXDATA							

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	RXDATA	0x0	R	**RX Data and Control bits**
	Use this register to access data read from the EUSART, cleared on read access. In Synchronous mode, Bit 15:0 is actual RXDATA. In Asynchronous mode, if DALICFG.DALIEN is 0, then Bit 8:0 is actual RXDATA, bit 9 is PERR (set if received data has a parity error.), bit 10 is FERR (set if received data has a framing error, can be result of a break condition). In Asynchronous mode, if DALICFG.DALIEN is set to 1, then all 16 bits represent received data. Note that FIFO is not retained in EM2.			

21.5.17 EUSART_RXDATAP - RX Data Peek Register

Offset	Bit Position																													
0x040	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									R							
Name																									RXDATAP							

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	RXDATAP	0x0	R	**RX Data Peek**
	Use this register to access data read from the EUSART without popping the FIFO.			

21.5.18 EUSART_TXDATA - TX Data Register

Offset	Bit Position																													
0x044	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																								0x0								
Access																								W								
Name																								TXDATA								

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	TXDATA	0x0	W	**TX Data and Control bits**
	Use this register to write data to the EUSART. If TXEN is set, a transfer will be initiated at the first opportunity. In Synchronous mode, 15:0 is TXDATA. In Asynchronous mode, if DALICFG.DALIEN is set to 1, then all 16 bits represent data. In Asynchronous mode, if DALICFG.DALIEN is set to 0 then 8:0 is TXDATA, bit 9 is UBRXAT (Set to clear RXBLOCK after transmission, unblocking the receiver), bit 10 is TXTRIAT (Set to tristate transmitter by setting TXTRI after tranmission), bit 11 is TXBREAK (Set to send data as a break. Recipient will see a framing error or a break condition depending on its configuration and the value of TXDATA), bit 12 is TXDISAT (Set to disable trasmitter and release data bus directly after transmission), bit 13 is RXENAT (Set to enable reception after transmission). Note that FIFO is not retained in EM2			

21.5.19 EUSART_STATUS - Status Register

Offset	Bit Position																													
0x048	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset							0x0	0x0						0x0					0x1	0x1				0x0	0x0	0x1	0x0	0x0	0x0		0x0	0x0
Access							R	R						R					R	R				R	R	R	R	R	R		R	R
Name							CLEARTXBUSY	AUTOBAUDDONE						TXFCNT					TXIDLE	RXIDLE				RXFULL	RXFL	TXFL	TXC	TXTRI	RXBLOCK		TXENS	RXENS

Bit	Name	Reset	Access	Description
31:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25	CLEARTXBUSY	0x0	R	**TX FIFO Clear Busy**
	After issuing CLEARTX command, wait on this status flag until it goes low.			
24	AUTOBAUDDONE	0x0	R	**Auto Baud Rate Detection Completed**
	Set when auto baud rate has been detected and CLKDIV has been updated with required value. If AUTOBAUDEN is not set in CFG0 register, this bit is always read as '0'. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
23:21	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
20:16	TXFCNT	0x0	R	**Valid entries in TX FIFO**
	Count of TX valid FIFO entries.			
15:14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13	TXIDLE	0x1	R	**TX Idle**
	Set when TX idle. In Synchronous secondary mode, TX is not considered idle when transmitting Default TX data.			
12	RXIDLE	0x1	R	**RX Idle**
	Set when RX is idle.			
11:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8	RXFULL	0x0	R	**RX FIFO Full**
	Set when the RX FIFO is full.			
7	RXFL	0x0	R	**RX FIFO Level**
	Set when data is available in the RX FIFO. Depends on the RXFIW setting in the CFG1 register.			
6	TXFL	0x1	R	**TX FIFO Level**
	Set when there is space for data in the TX FIFO. Depends on the TXFIW setting in CFG1 register.			
5	TXC	0x0	R	**TX Complete**
	Set when a transmission has completed and no more data is available in the TX FIFO and shift register.			
4	TXTRI	0x0	R	**Transmitter Tristated**

Bit	Name	Reset	Access	Description
	Set when the transmitter is tristated, and cleared when transmitter output is enabled. If AUTOTRI in UARTn_CFG is set, then this bit is always read as 0. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
3	RXBLOCK	0x0	R	**Block Incoming Data**
	When set, the receiver discards incoming frames. An incoming frame will not be loaded into the RX FIFO if this bit is set at the instant the frame has been completely received.			
2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	TXENS	0x0	R	**Transmitter Enable Status**
	Set when the transmitter is enabled. In Synchronous secondary mode, default TX data will be transmitted when the transmitter is disabled.			
0	RXENS	0x0	R	**Receiver Enable Status**
	Set when the receiver is enabled.			

21.5.20 EUSART_IF - Interrupt Flag Register

Offset	Bit Position																													
0x04C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset							0x0	0x0					0x0	0x0		0x0			0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access							RW	RW					RW	RW		RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name							RXTO	AUTOBAUDDONE					SIGF	STARTF		CSWU			TXIDLE	CCF	LOADERR	MPAF	FERR	PERR	TXUF	TXOF	RXUF	RXOF	RXFULL	RXFL	TXFL	TXC

Bit	Name	Reset	Access	Description
31:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25	RXTO	0x0	RW	**RX Timeout Interrupt Flag**
	Set when RX timeout occurs. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
24	AUTOBAUDDONE	0x0	RW	**Auto Baud Complete Interrupt Flag**
	Set when auto baud rate detection is complete. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
23:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19	SIGF	0x0	RW	**Signal Frame Interrupt Flag**
	Set when a signal frame is detected. Please note that when MPA, START, and SIGNAL are set to match the same frame, corresponding interrupts might get triggered in arbitrary sequence due to synchronization uncertainty. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
18	STARTF	0x0	RW	**Start Frame Interrupt Flag**
	Set when a start frame is detected. Please note that when MPA, START, and SIGNAL are set to match the same frame, corresponding interrupts might get triggered in arbitrary sequence due to synchronization uncertainty. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
17	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
16	CSWU	0x0	RW	**CS Wake-up Interrupt Flag**
	Set when the CS asserts. Only applicable when CFG0.SYNC bit is set to 'SYNC' and CFG2.MASTER is set to 'SLAVE'.			
15:14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13	TXIDLE	0x0	RW	**TX Idle Interrupt Flag**
	Set when TX goes idle. In Synchronous mode, if TX is disabled during the middle of the transactions, TXIDLEIF won't be triggered when the engine becomes disabled.			
12	CCF	0x0	RW	**Collision Check Fail Interrupt Flag**
	Set when a collision check notices an error in the transmitted data. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
11	LOADERR	0x0	RW	**Load Error Interrupt Flag**

Bit	Name	Reset	Access	Description
	Set when the empty TX FIFO is loaded less than the required TIMINGCFG.SETUPWINDOW bus clock cycles before the first edge of the incoming SCLK. Only applicable when CFG0.SYNC bit is set to 'SYNC' and CFG2.MASTER is set to 'SLAVE' and CFG2.FORCELOAD is set.			
10	MPAF	0x0	RW	**Multi-Processor Address Frame Interrupt**
	Set when a multi-processor address frame is detected. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
9	FERR	0x0	RW	**Framing Error Interrupt Flag**
	Set when a frame with a framing error is received while RXBLOCK is cleared. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
8	PERR	0x0	RW	**Parity Error Interrupt Flag**
	Set when a frame with a parity error is received while RXBLOCK is cleared. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
7	TXUF	0x0	RW	**TX FIFO Underflow Interrupt Flag**
	In Sync secondary mode, Set when reading an empty TX FIFO with TX enabled. In Synchronous main Mode with AUTOTX enabled, set when transmitting the word that does not contain valid data.			
6	TXOF	0x0	RW	**TX FIFO Overflow Interrupt Flag**
	Set when a write is done to the TX FIFO while it is full. The data already in the TX FIFO is preserved.			
5	RXUF	0x0	RW	**RX FIFO Underflow Interrupt Flag**
	Set when trying to read from the RX FIFO when it is empty.			
4	RXOF	0x0	RW	**RX FIFO Overflow Interrupt Flag**
	Set when data is complettly received in the receive shift register but the RX FIFO is full. RX FIFO is not overwirtten by new data.			
3	RXFULL	0x0	RW	**RX FIFO Full Interrupt Flag**
	Set when the RX FIFO becomes full.			
2	RXFL	0x0	RW	**RX FIFO Level Interrupt Flag**
	Set when data becomes available in the RX FIFO. This field depends on the RXFIW field in the CFG1 register.			
1	TXFL	0x0	RW	**TX FIFO Level Interrupt Flag**
	Set when space becomes available in the TX FIFO. This depends on the TXFIW field in the CFG1 register.			
0	TXC	0x0	RW	**TX Complete Interrupt Flag**
	This interrupt is set after a transmission when both the TX FIFO and shift register are empty.			

21.5.21 EUSART_IEN - Interrupt Enable Register

Offset	Bit Position																													
0x050	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset							0x0	0x0					0x0	0x0		0x0			0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access							RW	RW					RW	RW		RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name							RXTO	AUTOBAUDDONE					SIGF	STARTF		CSWU			TXIDLE	CCF	LOADERR	MPAF	FERR	PERR	TXUF	TXOF	RXUF	RXOF	RXFULL	RXFL	TXFL	TXC

Bit	Name	Reset	Access	Description
31:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25	RXTO	0x0	RW	**RX Timeout Enable**
	Interrupt enable for RXTOIF.			
24	AUTOBAUDDONE	0x0	RW	**Auto Baud Complete Enable**
	Interrupt enable for AUTOBAUDDONEIF.			
23:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19	SIGF	0x0	RW	**Signal Frame Enable**
	Interrupt enable for SIGFIF.			
18	STARTF	0x0	RW	**Start Frame Enable**
	Interrupt enable for STARTFIF.			
17	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
16	CSWU	0x0	RW	**CS Wake-up Enable**
	Interrupt enable for CSWUIF.			
15:14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13	TXIDLE	0x0	RW	**TX IDLE Enable**
	Interrupt enable for TXIDLEIF.			
12	CCF	0x0	RW	**Collision Check Fail Enable**
	Interrupt enable for CCFIF.			
11	LOADERR	0x0	RW	**Load Error Enable**
	Interrupt enable for LOADERRIF.			
10	MPAF	0x0	RW	**Multi-Processor Addr Frame Enable**
	Interrupt enable for MPAFIF.			
9	FERR	0x0	RW	**Framing Error Enable**
	Interrupt enable for FERRIF.			

Bit	Name	Reset	Access	Description
8	PERR	0x0	RW	**Parity Error Enable**
	Interrupt enable for PERRIF.			
7	TXUF	0x0	RW	**TX FIFO Underflow Enable**
	Interrupt enable for TXUFIF.			
6	TXOF	0x0	RW	**TX FIFO Overflow Enable**
	Interrupt enable for TXOFIF.			
5	RXUF	0x0	RW	**RX FIFO Underflow Enable**
	Interrupt enable for RXUFIF.			
4	RXOF	0x0	RW	**RX FIFO Overflow Enable**
	Interrupt enable for RXOFIF.			
3	RXFULL	0x0	RW	**RX FIFO Full Enable**
	Interrupt enable for RXFULLIF.			
2	RXFL	0x0	RW	**RX FIFO Level Enable**
	Interrupt enable for RXFLIF.			
1	TXFL	0x0	RW	**TX FIFO Level Enable**
	Interrupt enable for TXFLIF.			
0	TXC	0x0	RW	**TX Complete Enable**
	Interrupt enable for TXCIF.			

21.5.22 EUSART_SYNCBUSY - Synchronization Busy Register

Offset	Bit Position																													
0x054	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																					0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																					R	R	R	R	R	R	R	R	R	R	R	R
Name																					AUTOTXTEN	TXTRIDIS	TXTRIEN	RXBLOCKDIS	RXBLOCKEN	TXDIS	TXEN	RXDIS	RXEN	TXTEN	RXTEN	DIV

Bit	Name	Reset	Access	Description
31:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11	AUTOTXTEN	0x0	R	**SYNCBUSY for AUTOTXTEN in TRIGCTRL**
	This bit is set when there is an ongoing synchronization of AUTOTXTEN field. Do not do another write to the same field while this bit is set.			
10	TXTRIDIS	0x0	R	**SYNCBUSY in TXTRIDIS in CMD**
	This bit is set when there is an ongoing synchronization of TXTRIDIS field. Do not do another write to the same field while this bit is set. Only applicable when CFG0.SYNC bit is set to 'ASYNC'.			
9	TXTRIEN	0x0	R	**SYNCBUSY for TXTRIEN in CMD**
	This bit is set when there is an ongoing synchronization of TXTRIEN field. Do not do another write to the same field while this bit is set.			
8	RXBLOCKDIS	0x0	R	**SYNCBUSY for RXBLOCKDIS in CMD**
	This bit is set when there is an ongoing synchronization of RXBLOCKDIS field. Do not do another write to the same field while this bit is set.			
7	RXBLOCKEN	0x0	R	**SYNCBUSY for RXBLOCKEN in CMD**
	This bit is set when there is an ongoing synchronization of RXBLOCKEN field. Do not do another write to the same field while this bit is set.			
6	TXDIS	0x0	R	**SYNCBUSY for TXDIS in CMD**
	This bit is set when there is an ongoing synchronization of TXDIS field. Do not do another write to the same field while this bit is set.			
5	TXEN	0x0	R	**SYNCBUSY for TXEN in CMD**
	This bit is set when there is an ongoing synchronization of TXEN field. Do not do another write to the same field while this bit is set.			
4	RXDIS	0x0	R	**SYNCBUSY for RXDIS in CMD**
	This bit is set when there is an ongoing synchronization of RXDIS field. Do not do another write to the same field while this bit is set.			
3	RXEN	0x0	R	**SYNCBUSY for RXEN in CMD**
	This bit is set when there is an ongoing synchronization of RXEN field. Do not do another write to the same field while this bit is set.			
2	TXTEN	0x0	R	**SYNCBUSY for TXTEN in TRIGCTRL**
	This bit is set when there is an ongoing synchronization of TXTEN field. Do not do another write to the same field while this bit is set.			

Bit	Name	Reset	Access	Description
1	RXTEN	0x0	R	**SYNCBUSY for RXTEN in TRIGCTRL** This bit is set when there is an ongoing synchronization of RXTEN field. Do not do another write to the same field while this bit is set.
0	DIV	0x0	R	**SYNCBUSY for DIV in CLKDIV** This bit is set when there is an ongoing synchronization of DIV field. Do not do another write to the same field while this bit is set.

21.5.23 EUSART_DALICFG - DALI Config Register

Offset	Bit Position																													
0x058	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0			0x0							0x0					0x0
Access																	RW			RW							RW					RW
Name																	DALIRXENDT			DALIRXDATABITS							DALITXDATABITS					DALIEN

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15	DALIRXENDT	0x0	RW	**DALI RX Enabled During Transmission**
	If set, then EUSART RX will stay enabled during EUSART DALI TX. Should be set in loopback mode.			
14:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12:8	DALIRXDATABITS	0x0	RW	**DALI RX Databits**
	DALI RX databits (8-32). Only used if DALIEN is set.			

Value	Mode	Description
0	EIGHT	Each frame contains 8 data bits
1	NINE	Each frame contains 9 data bits
2	TEN	Each frame contains 10 data bits
3	ELEVEN	Each frame contains 11 data bits
4	TWELVE	Each frame contains 12 data bits
5	THIRTEEN	Each frame contains 13 data bits
6	FOURTEEN	Each frame contains 14 data bits
7	FIFTEEN	Each frame contains 15 data bits
8	SIXTEEN	Each frame contains 16 data bits
9	SEVENTEEN	Each frame contains 17 data bits
10	EIGHTEEN	Each frame contains 18 data bits
11	NINETEEN	Each frame contains 19 data bits
12	TWENTY	Each frame contains 20 data bits
13	TWENTYONE	Each frame contains 21 data bits
14	TWENTYTWO	Each frame contains 22 data bits
15	TWENTYTHREE	Each frame contains 23 data bits
16	TWENTYFOUR	Each frame contains 24 data bits
17	TWENTYFIVE	Each frame contains 25 data bits

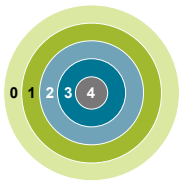
Bit	Name	Reset	Access	Description
	18	TWENTYSIX		Each frame contains 26 data bits
	19	TWENTYSEVEN		Each frame contains 27 data bits
	20	TWENTYEIGHT		Each frame contains 28 data bits
	21	TWENTYNINE		Each frame contains 29 data bits
	22	THIRTY		Each frame contains 30 data bits
	23	THIRTYONE		Each frame contains 31 data bits
	24	THIRTYTWO		Each frame contains 32 data bits
7:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:1	DALITXDATABITS	0x0	RW	**DALI TX Databits**

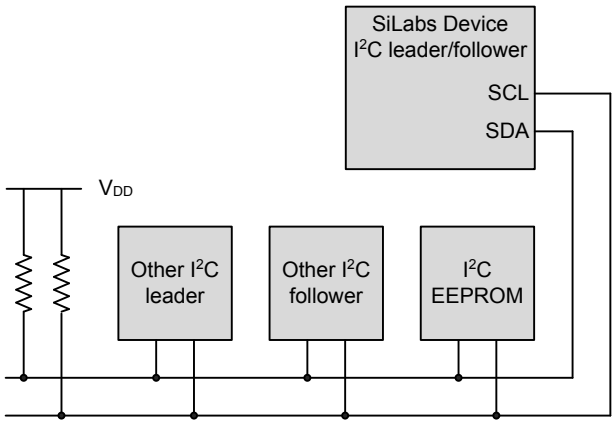
DALI TX databits (8-32). Only used if DALIEN is set.

Value	Mode	Description
0	EIGHT	Each frame contains 8 data bits
1	NINE	Each frame contains 9 data bits
2	TEN	Each frame contains 10 data bits
3	ELEVEN	Each frame contains 11 data bits
4	TWELVE	Each frame contains 12 data bits
5	THIRTEEN	Each frame contains 13 data bits
6	FOURTEEN	Each frame contains 14 data bits
7	FIFTEEN	Each frame contains 15 data bits
8	SIXTEEN	Each frame contains 16 data bits
9	SEVENTEEN	Each frame contains 17 data bits
10	EIGHTEEN	Each frame contains 18 data bits
11	NINETEEN	Each frame contains 19 data bits
12	TWENTY	Each frame contains 20 data bits
13	TWENTYONE	Each frame contains 21 data bits
14	TWENTYTWO	Each frame contains 22 data bits
15	TWENTYTHREE	Each frame contains 23 data bits
16	TWENTYFOUR	Each frame contains 24 data bits
17	TWENTYFIVE	Each frame contains 25 data bits
18	TWENTYSIX	Each frame contains 26 data bits
19	TWENTYSEVEN	Each frame contains 27 data bits
20	TWENTYEIGHT	Each frame contains 28 data bits
21	TWENTYNINE	Each frame contains 29 data bits
22	THIRTY	Each frame contains 30 data bits
23	THIRTYONE	Each frame contains 31 data bits
24	THIRTYTWO	Each frame contains 32 data bits

Bit	Name	Reset	Access	Description
0	DALIEN DALI EN bit.	0x0	RW	**DALI Enable Bit**

22. I2C - Inter-Integrated Circuit Interface





Quick Facts

What?

The I²C interface allows communication on I²C-buses with the lowest energy consumption possible.

Why?

I²C is a popular serial bus that enables communication with a number of external devices using only two I/O pins.

How?

With the help of DMA, the I²C interface allows I²C communication with minimal CPU intervention. Address recognition is available in all energy modes (except EM4), allowing the MCU to wait for data on the I²C-bus with sub-µA current consumption.

22.1 Introduction

The I²C module provides an interface between the MCU and a serial I²C-bus. It is capable of acting as both a leader and a follower and supports multi-leader buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Follower arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I²C module allows precise control of the transmission process and highly automated transfers. Automatic recognition of follower addresses is provided in all energy modes (except EM4).

22.2 Features

- True multi-leader capability
- Support for different bus speeds
  - Standard-mode (Sm) bit rate up to 100 kbit/s
  - Fast-mode (Fm) bit rate up to 400 kbit/s
  - Fast-mode Plus (Fm+) bit rate up to 1 Mbit/s
- Arbitration for both leader and follower (allows SMBus ARP)
- Clock synchronization and clock stretching
- Hardware address recognition
  - 7-bit masked address
  - General call address
  - Supported in EM2/3 (I2C0-only)
- 10-bit address support
- Error handling
  - Clock low timeout
  - Bus idle (clock high) timeout
  - Arbitration lost
  - Bus error detection
- Separate receive/ transmit 2-level buffers, with additional separate shift registers
- Full DMA support

22.3 Functional Description

An overview of the I2C module is shown in Figure 22.1 I2C Overview on page 684.

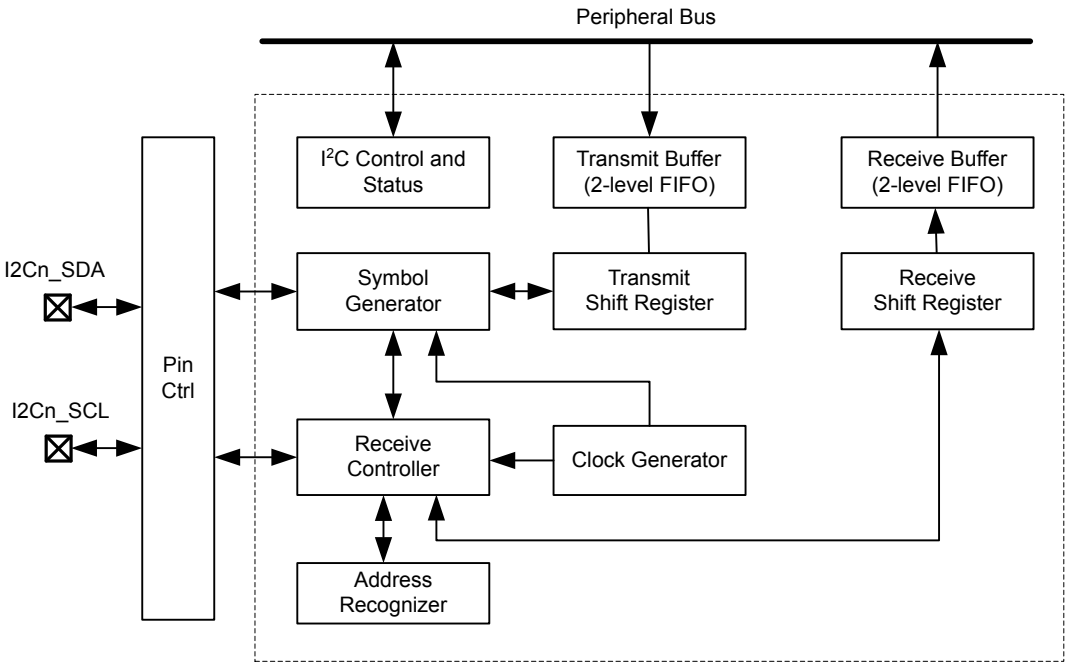


Figure 22.1. I2C Overview

22.3.1 I2C-Bus Overview

The I²C-bus uses two wires for communication; a serial data line (SDA) and a serial clock line (SCL) as shown in Figure 22.2 I2C-Bus Example on page 685. As a true multi-leader bus it includes collision detection and arbitration to resolve situations where multiple leaders transmit data at the same time without data loss.

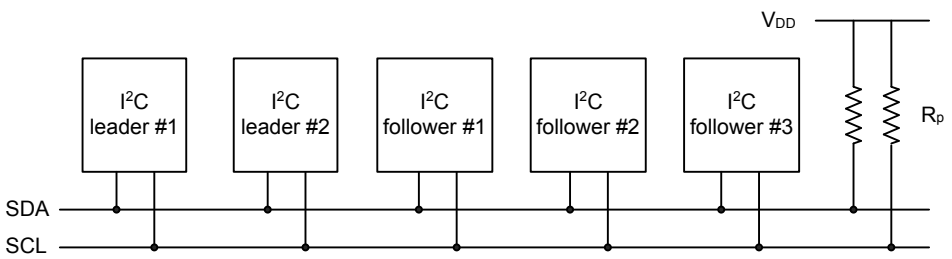


Figure 22.2. I2C-Bus Example

Each device on the bus is addressable by a unique address, and an I²C leader can address all the devices on the bus, including other leaders.

Both the bus lines are open-drain. The maximum value of the pull-up resistor can be calculated as a function of the maximal rise-time **tr** for the given bus speed, and the estimated bus capacitance **Cb** as shown in Figure 22.3 I2C Pull-up Resistor Equation on page 685.

$$R_{p(max)} = t_r/(0.8473 \times C_b).$$

Figure 22.3. I2C Pull-up Resistor Equation

The maximal rise times for 100 kHz, 400 kHz and 1 MHz I²C are 1 µs, 300 ns and 120 ns respectively.

Note: The GPIO slew rate control should be set for the desired slew rate..

Note: If V_{dd} drops below the voltage on SCL and SDA lines, the MCU could become back powered and pull the SCL and SDA lines low.

22.3.1.1 START and STOP Conditions

START and STOP conditions are used to initiate and stop transactions on the I^2C-bus. All transactions on the bus begin with a START condition (S) and end with a STOP condition (P). As shown in Figure 22.4 I2C START and STOP Conditions on page 686, a START condition is generated by pulling the SDA line low while SCL is high, and a STOP condition is generated by pulling the SDA line high while SCL is high.

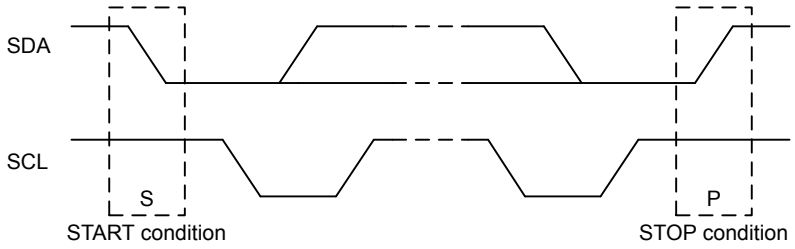


Figure 22.4. I2C START and STOP Conditions

The START and STOP conditions are easily identifiable bus events as they are the only conditions on the bus where a transition is allowed on SDA while SCL is high. During the actual data transmission, SDA is only allowed to change while SCL is low, and must be stable while SCL is high. One bit is transferred per clock pulse on the I^2C-bus as shown in Figure 22.5 I2C Bit Transfer on I^2C-Bus on page 686.

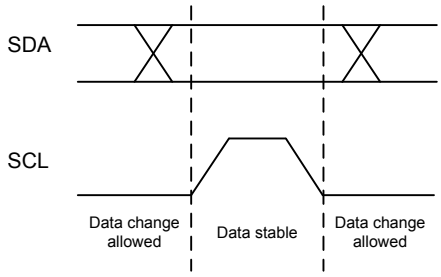


Figure 22.5. I2C Bit Transfer on I^2C-Bus

22.3.1.2 Bus Transfer

When a leader wants to initiate a transfer on the bus, it waits until the bus is idle and transmits a START condition on the bus. The leader then transmits the address of the follower it wishes to interact with and a single R/W bit telling whether it wishes to read from the follower (R/W bit set to 1) or write to the follower (R/W bit set to 0).

After the 7-bit address and the R/W bit, the leader releases the bus, allowing the follower to acknowledge the request. During the next bit-period, the follower pulls SDA low (ACK) if it acknowledges the request, or keeps it high if it does not acknowledge it (NACK).

Following the address acknowledge, either the follower or leader transmits data, depending on the value of the R/W bit. After every 8 bits (one byte) transmitted on the SDA line, the transmitter releases the line to allow the receiver to transmit an ACK or a NACK. Both the data and the address are transmitted with the most significant bit first.

The number of bytes in a bus transfer is unrestricted. The leader ends the transmission after a (N)ACK by sending a STOP condition on the bus. After a STOP condition, any leader wishing to initiate a transfer on the bus can try to gain control of it. If the current leader wishes to make another transfer immediately after the current, it can start a new transfer directly by transmitting a repeated START condition (Sr) instead of a STOP followed by a START.

Examples of I^2C transfers are shown in Figure 22.6 I2C Single Byte Write to Follower on page 687, Figure 22.7 I2C Double Byte Read from Follower on page 687, and Figure 22.8 I2C Single Byte Write, then Repeated Start and Single Byte Read on page 687. The identifiers used are:

- ADDR - Address
- DATA - Data
- S - Start bit
- Sr - Repeated start bit
- P - Stop bit
- W/R - Read(1)/Write(0)
- A - ACK
- N - NACK



Figure 22.6. I2C Single Byte Write to Follower



Figure 22.7. I2C Double Byte Read from Follower

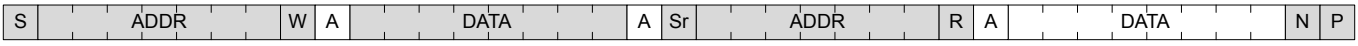


Figure 22.8. I2C Single Byte Write, then Repeated Start and Single Byte Read

22.3.1.3 Addresses

I²C supports both 7-bit and 10-bit addresses. When using 7-bit addresses, the first byte transmitted after the START-condition contains the address of the follower that the leader wants to contact. In the 7-bit address space, several addresses are reserved. These addresses are summarized in Table 22.1 I2C Reserved I²C Addresses on page 688, and include a General Call address which can be used to broadcast a message to all followers on the I²C-bus.

Table 22.1. I2C Reserved I²C Addresses

I²C Address	R/W	Description
0000-000	0	General Call address
0000-000	1	START byte
0000-001	X	Reserved for the C-Bus format
0000-010	X	Reserved for a different bus format
0000-011	X	Reserved for future purposes
0000-1XX	X	Reserved for future purposes
1111-1XX	X	Reserved for future purposes
1111-0XX	X	10 Bit follower addressing mode

22.3.1.4 10-bit Addressing

To address a follower using a 10-bit address, two bytes are required to specify the address instead of one. The seven first bits of the first byte must then be 1111 0XX, where XX are the two most significant bits of the 10-bit address. As with 7-bit addresses, the eighth bit of the first byte determines whether the leader wishes to read from or write to the follower. The second byte contains the eight least significant bits of the follower address.

When a follower receives a 10-bit address, it must acknowledge both the address bytes if they match the address of the follower.

When performing a leader transmitter operation, the leader transmits the two address bytes and then the remaining data, as shown in Figure 22.9 I2C Leader Transmitter/Follower Receiver with 10-bit Address on page 688.

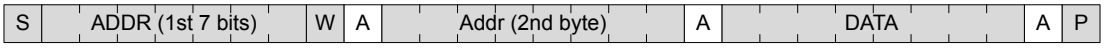


Figure 22.9. I2C Leader Transmitter/Follower Receiver with 10-bit Address

When performing a leader receiver operation however, the leader first transmits the two address bytes in a leader transmitter operation, then sends a repeated START followed by the first address byte and then receives data from the addressed follower. The follower addressed by the 10-bit address in the first two address bytes must remember that it was addressed, and respond with data if the address transmitted after the repeated start matches its own address. An example of this (with one byte transmitted) is shown in Figure 22.10 I2C Leader Receiver/Follower Transmitter with 10-bit Address on page 688.

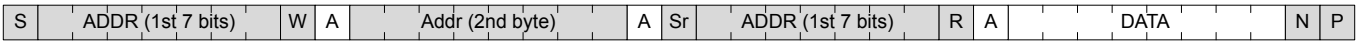


Figure 22.10. I2C Leader Receiver/Follower Transmitter with 10-bit Address

22.3.1.5 Arbitration, Clock Synchronization, Clock Stretching

Arbitration and clock synchronization are features aimed at allowing multi-leader buses. Arbitration occurs when two devices try to drive the bus at the same time. If one device drives it low, while the other drives it high, the one attempting to drive it high will not be able to do so due to the open-drain bus configuration. Both devices sample the bus, and the one that was unable to drive the bus in the desired direction detects the collision and backs off, letting the other device continue communication on the bus undisturbed.

Clock synchronization is a means of synchronizing the clock outputs from several leaders driving the bus at once, and is a requirement for effective arbitration.

Followers on the bus are allowed to force the clock output on the bus low in order to pause the communication on the bus and give themselves time to process data or perform any real-time tasks they might have. This is called clock stretching.

Arbitration is supported by the I^{2}C module for both leaders and followers. Clock synchronization and clock stretching is also supported.

22.3.2 Enable and Reset

The I^{2}C is enabled by setting the EN bit in the I2C_EN register.

To reset the internal state of the I^{2}C module and terminate any ongoing transfers, set the CORERST bit in I2C_CTRL. After resetting, the CORERST bit must be cleared to resume I^{2}C operation.

Note: When enabling the I^{2}C, the ABORT command or the Bus Idle Timeout feature must be applied prior to use even if the BUSY flag is not set.

22.3.3 Pin Configuration

The I^{2}C SDA and SCL pins are configured and enabled in the GPIO_I2Cn_ROUTEEN, GPIO_I2Cn_SCLROUTE, and GPIO_I2Cn_SDAROUTE registers.

The I^{2}C module must be configured to use pins on either Port A or B if wakeup on address recognition from EM2/3 is desired. All other ports are available only in EM0/1. See GPIO chapter for more details on Port limitations.

If the I^{2}C module is configured to use pins other than Port A or B, firmware should reset the module before entering EM2/3 by setting the CORERST bit in I2C_CTRL. After resuming EM0/1 operation, firmware should then clear CORERST.

22.3.4 Safely Disabling and Changing Follower Configuration

The I^{2}C follower is partially asynchronous, and some precautions are necessary to always ensure a safe follower disable or follower configuration change. These measures should be taken, if (while the follower is enabled) the user cannot guarantee that an address match will not occur at the exact time of follower disable or follower configuration change.

Worst case consequences for an address match while disabling follower or changing configuration is that the follower may end up in an undefined state. To reset the follower back to a known state, the EN bit in I2C_EN must be cleared. This should be done regardless of whether the follower is going to be re-enabled or not.

22.3.5 Clock Generation

The I^2C peripheral clock (I2CCLK) for I2C0 is derived from the LSPCLK, and for I2C1 is derived from the PCLK.

The SCL signal generated by the I^2C leader determines the maximum transmission rate on the bus. The clock is generated as a division of the peripheral clock (I2CCLK), and is given by the following equation:

$$f_{SCL} = f_{I2CCLK}/(((N_{low} + N_{high}) \times (DIV + 1)) + 8 + N_{fall} + N_{rise})$$

Figure 22.11. I2C Maximum Transmission Rate

Where DIV is the clock divider value set in I2C_CLKDIV, the values of N_{low} and N_{high} (and thus the ratio between the high and low parts of the clock signal) are controlled by CLHR in the I2C_CTRL register, and N_{fall} and N_{rise} represent the number of I2CCLK cycles required for clock synchronization.

The values of N_{low} and N_{high} specify the number of prescaled clock cycles in the low and high periods of the clock signal respectively. The worst case low and high periods of the signal are:

$$t_{high} >= (N_{high} \times (DIV + 1) + 4)/f_{I2CCLK}$$

$$t_{low} >= (N_{low} \times (DIV + 1) + 4)/f_{I2CCLK}$$

Figure 22.12. I2C High and Low Cycles Equations

Clock synchronization is used to ensure that requested low and high times are met on the bus. The counters establishing high and low time are only active once the pin logic has reached the high or low logic levels, and so the rise and fall times will impact the maximum transmission rate on the bus. The clock logic level is sampled at a rate of f_{I2CCLK}, and will therefore be quantized to an integer number of I2CCLK clock cycles, as:

$$N_{rise} = CEILING(t_{rise}/t_{I2CCLK})$$

$$N_{fall} = CEILING(t_{fall}/t_{I2CCLK})$$

Figure 22.13. I2C Clock Synchronization Cycles

Note that there is an inherent propagation delay between driving SCL and sampling the signal, so the above equations can result in N = 0 for fast rise or fall times.

For example, a system with a weak pull-up on SCL may result in long t_{rise}, requiring several N_{rise} synchronization cycles, and subsequently impact the I2C transmission rate. In the same system, t_{fall} may be faster than the sampling delay, resulting in N_{fall} = 0.

Note: DIV must be set to 1 during follower mode operation.

22.3.6 Arbitration

Arbitration is enabled by default, but can be disabled by setting the ARBDIS bit in I2C_CTRL. When arbitration is enabled, the value on SDA is sensed every time the I^2C module attempts to change its value. If the sensed value is different than the value the I^2C module tried to output, it is interpreted as a simultaneous transmission by another device, and that the I^2C module has lost arbitration.

Whenever arbitration is lost, the ARBLOST interrupt flag in I2C_IF is set, any lines held are released, and the I^2C device goes idle. If an I^2C leader loses arbitration during the transmission of an address, another leader may be trying to address it. The leader therefore receives the rest of the address, and if the address matches the follower address of the leader, the leader goes into either follower transmitter or follower receiver mode.

Note:

Arbitration can be lost both when operating as a leader and when operating as a follower.

22.3.7 Buffers

22.3.7.1 Transmit Buffer and Shift Register

The I²C transmitter has a 2-level FIFO transmit buffer and a transmit shift register as shown in Figure 22.1 I2C Overview on page 684. A byte is loaded into the transmit buffer by writing to I2C_TXDATA or 2 bytes can be loaded simultaneously in the transmit buffer by writing to I2C_TXDOUBLE. Figure 22.14 I2C Transmit Buffer Operation on page 691 shows the basics of the transmit buffer. When the transmit shift register is empty and ready for new data, the byte from the transmit buffer is then loaded into the shift register. The byte is then kept in the shift register until it is transmitted. When a byte has been transmitted, a new byte is loaded into the shift register (if available in the transmit buffer). If the transmit buffer is empty, then the shift register also remains empty. The TXC flag in I2C_STATUS and the TXC interrupt flags in I2C_IF are then set, signaling that the transmit shift register is out of data. TXC is cleared when new data becomes available, but the TXC interrupt flag must be cleared by software.

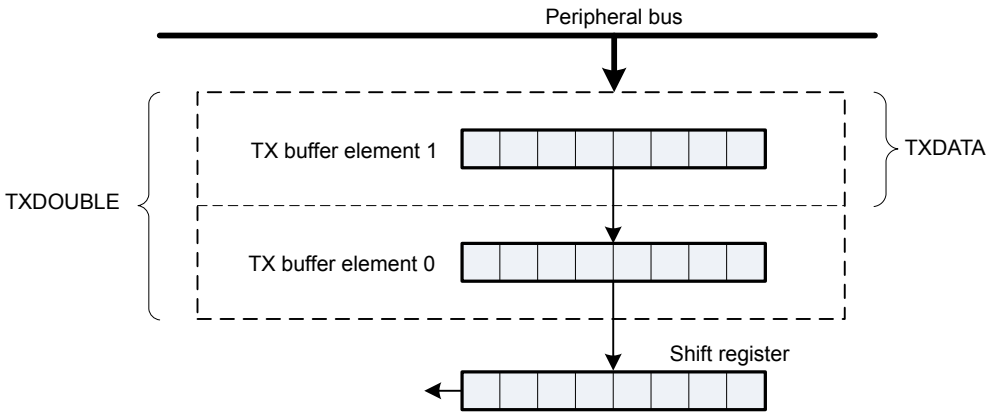


Figure 22.14. I2C Transmit Buffer Operation

The TXBL flags in I2C_STATUS and I2C_IF are used to indicate the level of the transmit buffer. The TXBIL bit in I2C_CTRL controls the level at which these flag bits are set:

- If TXBIL is cleared, the TXBL flags are set whenever the transmit buffer becomes empty (used when transmitting using I2C_TXDOUBLE).
- If TXBIL is set, the TXBL flags are set whenever the transmit buffer goes from full to half-empty or empty (used when transmitting with I2C_TXDATA).

The TXBL status flag in I2C_STATUS is cleared automatically when the condition becomes false. After the transmit FIFOs are filled, software needs to manually clear the TXBL interrupt flag. Note that the TXBL interrupt flag is 0 by default, but immediately after software sets I2C_EN.EN = 1, the TXBL interrupt flag will be set to indicate the transmit FIFO is empty. When the I²C module is disabled (I2C_EN.EN= 0), software needs to manually clear the TXBL interrupt flag (or ignore it).

Additionally, the TXBUFCNT bitfield in I2C_STATUS can be read to determine the exact number of transmit buffers filled with valid data. This is particularly useful for determining whether the transmit buffers are full. For example, if TXBUFCNT = '2', firmware can determine that both transmit buffers are filled, and that any additional data written to the transmit buffer would result in an overflow condition. Note that the TXBUFCNT count does not include the TX shift register.

If an attempt is made to write more bytes to the transmit buffer than the space available, the TXOF interrupt flag in I2C_IF is set, indicating the overflow. The data already in the buffer remains preserved, and no new data is written.

The transmit buffer and the transmit shift register can be cleared by setting command bit CLEARTX in I2C_CMD. This will prevent the I²C module from transmitting the data in the buffer and the shift register, and will make them available for new data. Any byte currently being transmitted will not be aborted. Transmission of this byte will be completed.

22.3.7.2 Receive Buffer and Shift Register

The I²C receiver uses a 2-level FIFO receive buffer and a receive shift register as shown in Figure 22.15 I2C Receive Buffer Operation on page 692. When a byte has been fully received by the receive shift register, it is loaded into the receive buffer if there is room for it, making the shift register empty to receive another byte. Otherwise, the byte waits in the shift register until space becomes available in the buffer.

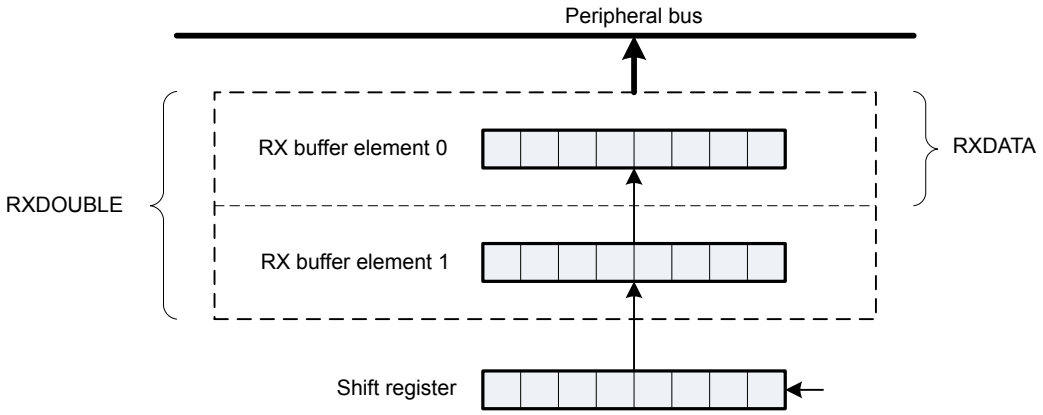


Figure 22.15. I2C Receive Buffer Operation

When a byte becomes available in the receive buffer, the RXDATAV flags in I2C_STATUS and I2C_IF are set. When the buffer becomes full, the RXFULL flags in I2C_STATUS and I2C_IF are set. The RXDATAV and RXFULL flags in I2C_STATUS are automatically cleared by hardware when their condition is no longer true. The RXDATAV and RXFULL flags in I2C_IF must be manually cleared by software after the receive FIFO is emptied. Note that when the RXFULL flag is set, indicating the buffer is full, space is still available in the receive shift register for one more byte.

The data can be fetched from the buffer in two ways. I2C_RXDATA gives access to the received byte (if two bytes are received then the one received first is fetched first). I2C_RXDOUBLE makes it possible to read the two received bytes simultaneously. If an attempt is made to read more bytes from the buffer than available, the RXUF interrupt flag in I2C_IF is set to signal the underflow, and the data read from the buffer is undefined.

When using I2C_RXDOUBLE to pick data, AUTOACK in I2C_CTRL should be set to 1. This ensures that an ACK is automatically sent out after the first byte is received so that the reception of the next byte can begin. In order to stop receiving data bytes, a NACK must be sent out through the I2C_CMD register.

I2C_RXDATAP and I2C_RXDOUBLEP can be used to read data from the receive buffer without removing it from the buffer. The RXUF interrupt flag in I2C_IF will never be set as a result of reading from I2C_RXDATAP and I2C_RXDOUBLEP, but the data read through I2C_RXDATAP when the receive buffer is empty is still undefined.

Once a transaction is complete (STOP sent or received), the receive buffer needs to be flushed (all received data must be read) before starting a new transaction.

22.3.8 Leader Operation

A bus transaction is initiated by transmitting a START condition (S) on the bus. This is done by setting the START bit in I2C_CMD. The command schedules a START condition, and makes the I^2C module generate a start condition whenever the bus becomes free.

The I^2C-bus is considered busy whenever another device on the bus transmits a START condition. Until a STOP condition is detected, the bus is owned by the leader issuing the START condition. The bus is considered free when a STOP condition is transmitted on the bus. After a STOP is detected, all leaders that have data to transmit send a START condition and begin transmitting data. Arbitration ensures that collisions are avoided.

When the START condition has been transmitted, the leader must transmit a follower address (ADDR) with an R/W bit on the bus. If this address is available in the transmit buffer, the leader transmits it immediately, but if the buffer is empty, the leader holds the I^2C-bus while waiting for software to write the address to the transmit buffer.

After the address has been transmitted, a sequence of bytes can be read from or written to the follower, depending on the value of the R/W bit (bit 0 in the address byte). If the bit was cleared, the leader has entered a leader transmitter role, where it now transmits data to the follower. If the bit was set, it has entered a leader receiver role, where it now should receive data from the follower. In either case, an unlimited number of bytes can be transferred in one direction during the transmission.

At the end of the transmission, the leader either transmits a repeated START condition (Sr) if it wishes to continue with another transfer, or transmits a STOP condition (P) if it wishes to release the bus. When operating in the leader mode, I2CCLK frequency must be higher than 2 MHz for Standard-mode, 9 MHz for Fast-mode, and 20 MHz for Fast-mode Plus.

22.3.8.1 Leader State Machine

The leader state machine is shown in Figure 22.16 I2C Leader State Machine on page 694. A leader operation starts in the far left of the state machine, and follows the solid lines through the state machine, ending the operation or continuing with a new operation when arriving at the right side of the state machine.

Branches in the path through the state machine are the results of bus events and choices made by software, either directly or indirectly. The dotted lines show where I²C-specific interrupt flags are set along the path and the full-drawn circles show places where interaction may be required by software to let the transmission proceed.

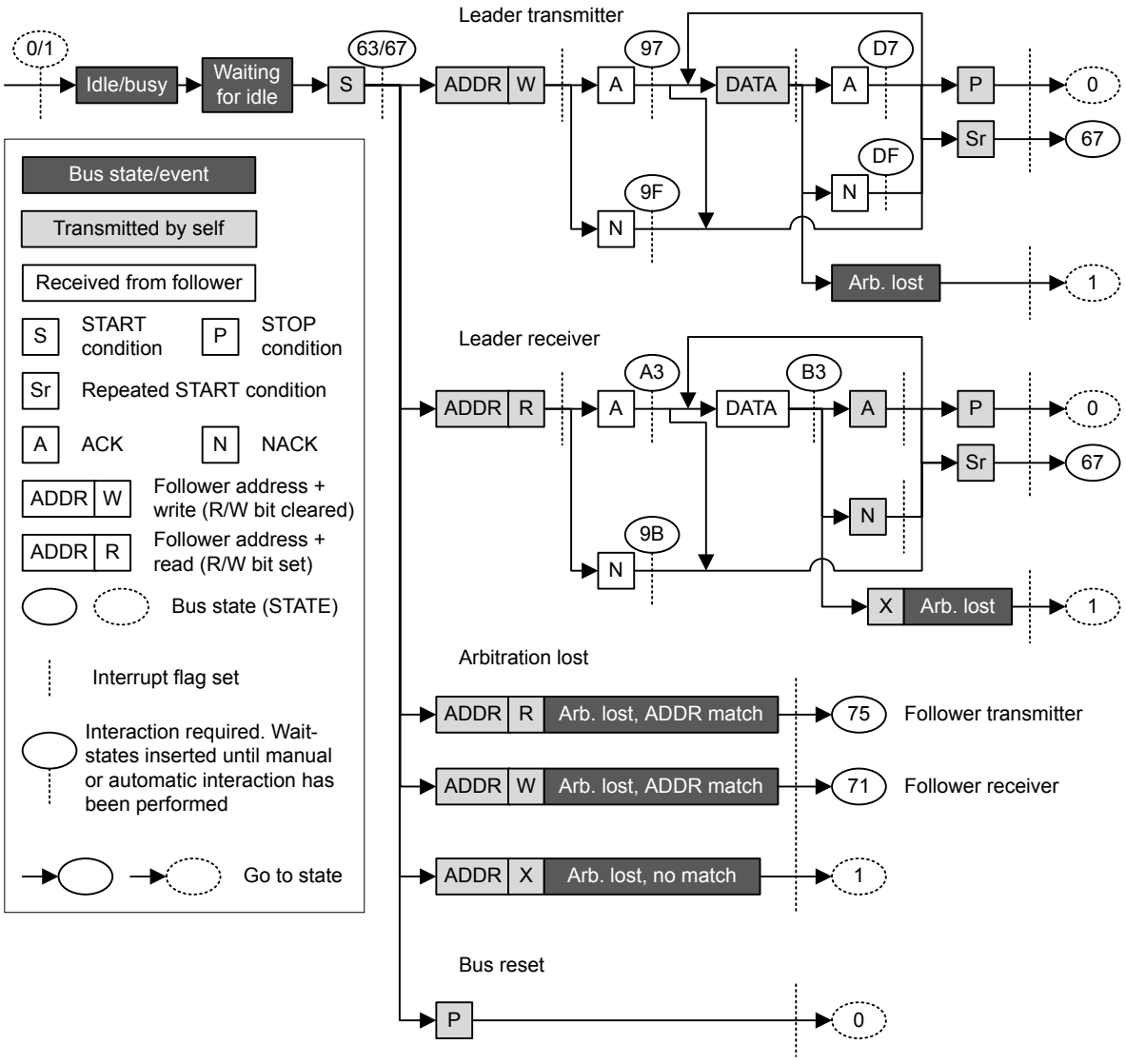


Figure 22.16. I2C Leader State Machine

22.3.8.2 Interactions

Whenever the I²C module is waiting for interaction from software, it holds the bus clock SCL low, freezing all bus activities, and the BUSHOLD interrupt flag in I2C_IF is set. The action(s) required by software depends on the current state the of the I²C module. This state can be read from the I2C_STATE register.

As an example, Table 22.3 I2C Leader Transmitter on page 697 shows the different states the I²C goes through when operating as a Leader Transmitter, i.e., a leader that transmits data to a follower. As seen in the table, when a start condition has been transmitted, a requirement is that there is an address and an R/W bit in the transmit buffer. If the transmit buffer is empty, then the BUSHOLD interrupt flag is set, and the bus is held until data becomes available in the buffer. While waiting for the address, I2C_STATE has a value 0x67, which can be used to identify exactly what the I²C module is waiting for.

Note: The bus would never stop at state 0x67 if the address was available in the transmit buffer.

The BUSHOLD interrupt flag needs to be manually cleared by software after the appropriate action has been taken.

The different interactions used by the I²C module are listed in Table 22.2 I2C Interactions in Prioritized Order on page 695 in a prioritized order. If the I²C module is in such a state that multiple courses of action are possible, then the action chosen is the one that has the highest priority. For example, after sending out a START, if an address is present in the buffer and a STOP is also pending, then the I²C will send out the STOP since it has the higher priority.

Table 22.2. I2C Interactions in Prioritized Order

Interaction	Priority	Software action	Automatically continues if
STOP*	1	Set the STOP command bit in I2C_CMD	PSTOP is set (STOP pending) in I2C_STATUS
ABORT	2	Set the ABORT command bit in I2C_CMD	Never, the transmission is aborted
CONT*	3	Set the CONT command bit in I2C_CMD	PCONT is set in I2C_STATUS (CONT pending)
NACK*	4	Set the NACK command bit in I2C_CMD	PNACK is set in I2C_STATUS (NACK pending)
ACK*	5	Set the ACK command bit in I2C_CMD	AUTOACK is set in I2C_CTRL or PACK is set in I2C_STATUS (ACK pending)
ADDR+W -> TXDATA	6	Write an address to the transmit buffer with the R/W bit set	Address is available in transmit buffer with R/W bit set
ADDR+R -> TXDATA	7	Write an address to the transmit buffer with the R/W bit cleared	Address is available in transmit buffer with R/W bit cleared
START*	8	Set the START command bit in I2C_CMD	PSTART is set in I2C_STATUS (START pending)
TXDATA/ TXDOUBLE	9	Write data to the transmit buffer	Data is available in transmit buffer
RXDATA/ RXDOUBLE	10	Read data from receive buffer	Space is available in receive buffer
None	11	No interaction is required	

The commands marked with a * in Table 22.2 I2C Interactions in Prioritized Order on page 695 can be issued before an interaction is required. When such a command is issued before it can be used/consumed by the I²C module, the command is set in a pending state, which can be read from the STATUS register. A pending START command can for instance be identified by PSTART having a high value.

Whenever the I²C module requires an interaction, it checks the pending commands. If one or a combination of these can fulfill an interaction, they are consumed by the module and the transmission continues without setting the BUSHOLD interrupt flag in I2C_IF to get an interaction from software. The pending status of a command goes low when it is consumed.

When several interactions are possible from a set of pending commands, the interaction with the highest priority, i.e., the interaction closest to the top of Table 22.2 I2C Interactions in Prioritized Order on page 695 is applied to the bus.

Pending commands can be cleared by setting the CLEARPC command bit in I2C_CMD.

22.3.8.3 Automatic ACK Interaction

When receiving addresses and data, an ACK command in I2C_CMD is normally required after each received byte. When AUTOACK is set in I2C_CTRL, an ACK is always pending, and the ACK-pending bit PACK in I2C_STATUS is thus always set, even after an ACK has been consumed. This is used when data is picked using I2C_RXDOUBLE and can also be used with I2C_RXDATA in order to reduce the amount of software interaction required during a transfer.

22.3.8.4 Reset State

After a reset, the state of the I^2C-bus is unknown. To avoid interrupting transfers on the I^2C-bus after a reset of the I^2C module or the entire MCU, the I^2C-bus is assumed to be busy when coming out of a reset, and the BUSY flag in I2C_STATUS is thus set. To be able to carry through leader operations on the I^2C-bus, the bus must be idle.

The bus goes idle when a STOP condition is detected on the bus, but on buses with little activity, the time before the I^2C module detects that the bus is idle can be significant. There are two ways of assuring that the I^2C module gets out of the busy state.

- Use the ABORT command in I2C_CMD. When the ABORT command is issued, the I^2C module is instructed that the bus is idle. The I^2C module can then initiate leader operations.
- Use the Bus Idle Timeout. When SCL has been high for a long period of time, it is very likely that the bus is idle. Set BITO in I2C_CTRL to an appropriate timeout period and set GIBITO in I2C_CTRL. If activity has not been detected on the bus within the timeout period, the bus is then automatically assumed idle, and leader operations can be initiated.

Note: If operating in follower mode, the above approach is not necessary.

22.3.8.5 Leader Transmitter

To transmit data to a follower, the leader must operate as a leader transmitter. Table 22.3 I2C Leader Transmitter on page 697 shows the states the I²C module goes through while acting as a leader transmitter. Every state where an interaction is required has the possible interactions listed, along with the result of the interactions. The table also shows which interrupt flags are set in the different states. The interrupt flags enclosed in parenthesis may be set. If the BUSHOLD interrupt in I2C_IF is set, the module is waiting for an interaction, and the bus is frozen. The value of I2C_STATE will be equal to the values given in the table when the BUSHOLD interrupt flag is set, and can be used to determine which interaction is required to make the transmission continue.

The interrupt flag START in I2C_IF is set when the I²C module transmits the START.

A leader operation is started by issuing a START command by setting START in I2C_CMD. ADDR+W, i.e., the address of the follower + the R/W bit is then required by the I²C module. If this is not available in the transmit buffer, then the bus is held and the BUSHOLD interrupt flag is set. The value of I2C_STATE will then be 0x67. As seen in the table, the I²C module also stops in this state if the address is not available after a repeated start condition.

To continue, write a byte to I2C_TXDATA with the address of the follower in the 7 most significant bits and the least significant bit cleared (ADDR+W). This address will then be transmitted, and the follower will reply with an ACK or a NACK. If no follower replies to the address, the response will also be NACK. If the address was acknowledged, the leader now has four choices. It can send data by placing it in I2C_TXDATA/ I2C_TXDOUBLE (the leader should check the TXBL interrupt flag before writing to the transmit buffer), this data is then transmitted. The leader can also stop the transmission by sending a STOP, it can send a repeated start by sending START, or it can send a STOP and then a START as soon as possible. If the leader wishes to make another transfer immediately after the current, the preferred way is to start a new transfer directly by transmitting a repeated START instead of a STOP followed by a START. This is so because if a STOP is sent out, then any leader wishing to initiate a transfer on the bus can try to gain control of it.

If a NACK was received, the leader has to issue a CONT command in addition to providing data in order to continue transmission. This is not standard I²C, but is provided for flexibility. The rest of the options are similar to when an ACK was received.

If a new byte was transmitted, an ACK or NACK is received after the transmission of the byte, and the leader has the same options as for when the address was sent.

The leader may lose arbitration at any time during transmission. In this case, the ARBLOST interrupt flag in I2C_IF is set. If the arbitration was lost during the transfer of an address, and SLAVE in I2C_CTRL is set, the leader then checks which address was transmitted. If it was the address of the leader, then the leader goes to follower mode.

After a leader has transmitted a START and won any arbitration, it owns the bus until it transmits a STOP. After a STOP, the bus is released, and arbitration decides which bus leader gains the bus next. The MSTOP interrupt flag in I2C_IF is set when a STOP condition is transmitted by the leader.

Table 22.3. I2C Leader Transmitter

I2C_STATE	Description	I2C_IF	Required interaction	Response
0x67	Start transmitted	START interrupt flag (BUSHOLD interrupt flag)	ADDR+W -> TXDATA	ADDR+W will be sent
			STOP	STOP will be sent and bus released.
			STOP + START	STOP will be sent and bus released. Then a START will be sent when bus becomes idle.
0x67	Repeated start transmitted	START interrupt flag (BUSHOLD interrupt flag)	ADDR+W -> TXDATA	ADDR+W will be sent
			STOP	STOP will be sent and bus released.
			STOP + START	STOP will be sent and bus released. Then a START will be sent when bus becomes idle.
-	ADDR+W transmitted	TXBL interrupt flag (TXC interrupt flag)	None	

I2C_STATE	Description	I2C_IF	Required interaction	Response
0x97	ADDR+W transmitted, ACK received	ACK interrupt flag (BUSHOLD interrupt flag)	TXDATA	DATA will be sent
			STOP	STOP will be sent. Bus will be released
			START	Repeated start condition will be sent
			STOP + START	STOP will be sent and the bus released. Then a START will be sent when the bus becomes idle
0x9F	ADDR+W transmitted,NACK received	NACK (BUSHOLD interrupt flag)	CONT + TXDATA	DATA will be sent
			STOP	STOP will be sent. Bus will be released
			START	Repeated start condition will be sent
			STOP + START	STOP will be sent and the bus released. Then a START will be sent when the bus becomes idle
-	Data transmitted	TXBL interrupt flag (TXC interrupt flag)	None	
0xD7	Data transmitted,ACK received	ACK interrupt flag (BUSHOLD interrupt flag)	TXDATA	DATA will be sent
			STOP	STOP will be sent. Bus will be released
			START	Repeated start condition will be sent
			STOP + START	STOP will be sent and the bus released. Then a START will be sent when the bus becomes idle
0xDF	Data transmitted,NACK received	NACK(BUSHOLD interrupt flag)	CONT + TXDATA	DATA will be sent
			STOP	STOP will be sent. Bus will be released
			START	Repeated start condition will be sent
			STOP + START	STOP will be sent and the bus released. Then a START will be sent when the bus becomes idle
-	Stop transmitted	MSTOP interrupt flag	None	
			START	START will be sent when bus becomes idle
-	Arbitration lost	ARBLOST interrupt flag	None	
			START	START will be sent when bus becomes idle

22.3.8.6 Leader Receiver

To receive data from a follower, the leader must operate as a leader receiver, see Table 22.4 I2C Leader Receiver on page 699. This is done by transmitting ADDR+R as the address byte instead of ADDR+W, which is transmitted to become a leader transmitter. The address byte loaded into the data register thus has to contain the 7-bit follower address in the 7 most significant bits of the byte, and have the least significant bit set.

When the address has been transmitted, the leader receives an ACK or a NACK. If an ACK is received, the ACK interrupt flag in I2C_IF is set, and if space is available in the receive shift register, reception of a byte from the follower begins. If the receive buffer and shift register is full however, the bus is held until data is read from the receive buffer or another interaction is made. Note that the STOP and START interactions have a higher priority than the data-available interaction, so if a STOP or START command is pending, the highest priority interaction will be performed, and data will not be received from the follower.

If a NACK was received, the CONT command in I2C_CMD has to be issued in order to continue receiving data, even if there is space available in the receive buffer and/or shift register.

After a data byte has been received the leader must ACK or NACK the received byte. If an ACK is pending or AUTOACK in I2C_CTRL is set, an ACK is sent automatically and reception continues if space is available in the receive buffer.

If a NACK is sent, the CONT command must be used in order to continue transmission. If an ACK or NACK is issued along with a START or STOP or both, then the ACK/NACK is transmitted and the reception is ended. If START in I2C_CMD is set alone, a repeated start condition is transmitted after the ACK/NACK. If STOP in I2C_CMD is set, a stop condition is sent regardless of whether START is set. If START is set in this case, it is set as pending.

As when operating as a leader transmitter, arbitration can be lost as a leader receiver. When this happens the ARBLOST interrupt flag in I2C_IF is set, and the leader has a possibility of being selected as a follower given the correct conditions.

Table 22.4. I2C Leader Receiver

I2C_STATE	Description	I2C_IF	Required interaction	Response
0x63	START transmitted	START interrupt flag (BUSHOLD interrupt flag)	ADDR+R -> TXDATA	ADDR+R will be sent
			STOP	STOP will be sent and bus released.
			STOP + START	STOP will be sent and bus released. Then a START will be sent when bus becomes idle.
0x67	Repeated START transmitted	START interrupt flag(BUSHOLD interrupt flag)	ADDR+R -> TXDATA	ADDR+R will be sent
			STOP	STOP will be sent and bus released.
			STOP + START	STOP will be sent and bus released. Then a START will be sent when bus becomes idle.
-	ADDR+R transmitted	TXBL interrupt flag (TXC interrupt flag)	None	
0xA3	ADDR+R transmitted, ACK received	ACK interrupt flag(BUSHOLD)	RXDATA	Start receiving
			STOP	STOP will be sent and the bus released
			START	Repeated START will be sent
			STOP + START	STOP will be sent and the bus released. Then a START will be sent when the bus becomes idle
0x9B	ADDR+R transmitted,NACK received	NACK(BUSHOLD)	CONT + RXDATA	Continue, start receiving
			STOP	STOP will be sent and the bus released
			START	Repeated START will be sent
			STOP + START	STOP will be sent and the bus released. Then a START will be sent when the bus becomes idle

I2C_STATE	Description	I2C_IF	Required interaction	Response
0xB3	Data received	RXDATA interrupt flag(BUSHOLD interrupt flag)	ACK + RXDATA	ACK will be transmitted, reception continues
			NACK + CONT + RXDATA	NACK will be transmitted, reception continues
			ACK/NACK + STOP	ACK/NACK will be sent and the bus will be released.
			ACK/NACK + START	ACK/NACK will be sent, and then a repeated start condition.
			ACK/NACK + STOP + START	ACK/NACK will be sent and the bus will be released. Then a START will be sent when the bus becomes idle
-	Stop received	MSTOP interrupt flag	None	
			START	START will be sent when bus becomes idle
-	Arbitration lost	ARBLOST interrupt flag	None	
			START	START will be sent when bus becomes idle

22.3.8.7 SDA/SCL Status Monitor

The I^2C module supports an SDA and SCL monitoring function. Note that this functionality is only supported when the I2C module is in single leader mode, and when the follower doesn't use clock stretching. Additionally, firmware should set the ARBDIS bit in I2C_CTRL when using the SDA/SCL monitoring to prevent the bus being released.

The SDA monitor is enabled by setting the SDAMONEN in I2C_CTRL. Once enabled, the SDA monitor will check the status of the SDA line at the following points:

- At a Start Condition, before SDA falls
- At Stop Condition, after SDA rises

After checking, the monitor will set the SDAERR flag in I2C_IF it fails to read SDA==1. To allow the SDAERR flag to generate an IRQ, set the SDAERR bit in I2C_IEN.

Similarly, the SCL monitor is enabled by setting the SCLMONEN in I2C_CTRL. Once enabled, the SCL monitor will check the status of the SCL line at the following points:

- At a Start Condition, before SCL falls
- At every clock cycle, before SCL falls
- At Stop Condition, after SCL rises

After checking, the monitor will set the SCLERR flag in I2C_IF it fails to read SCL==1. To allow the SCLERR flag to generate an IRQ, set the SCLERR bit in I2C_IEN.

22.3.9 Bus States

The I2C_STATE register can be used to determine which state the I²C module and the I²C bus are in at a given time. The register consists of the STATE bit-field, which shows which state the I²C module is at in any ongoing transmission, and a set of single-bits, which reveal the transmission mode, whether the bus is busy or idle, and whether the bus is held by this I²C module waiting for a software response.

The possible values of the STATE field are summarized in Table 22.5 I2C STATE Values on page 701. When this field is cleared, the I²C module is not a part of any ongoing transmission. The remaining status bits in the I2C_STATE register are listed in Table 22.6 I2C Transmission Status on page 701.

Table 22.5. I2C STATE Values

Mode	Value	Description
IDLE	0	No transmission is being performed by this module.
WAIT	1	Waiting for idle. Will send a start condition as soon as the bus is idle.
START	2	Start transmit phase
ADDR	3	Address transmit or receive phase
ADDRACK	4	Address ACK/NACK transmit or receive phase
DATA	5	Data transmit or receive phase
DATAACK	6	Data ACK/NACK transmit or receive phase

Table 22.6. I2C Transmission Status

Bit	Description
BUSY	Set whenever there is activity on the bus. Whether or not this module is responsible for the activity cannot be determined by this byte.
MASTER	Set when operating as a leader. Cleared at all other times.
TRANSMITTER	Set when operating as a transmitter; either a leader transmitter or a follower transmitter. Cleared at all other times
BUSHOLD	Set when the bus is held by this I²C module because an action is required by software.
NACK	Only valid when bus is held and STATE is ADDRACK or DATAACK. In that case it is set if a NACK was received. In all other cases, the bit is cleared.

Note: I2C_STATE reflects the internal state of the I²C module, and therefore only held constant as long as the bus is held, i.e., as long as BUSHOLD in I2C_STATUS is set.

22.3.10 Follower Operation

The I²C module operates in leader mode by default. To enable follower operation, i.e., to allow the device to be addressed as an I²C follower, the SLAVE bit in I2C_CTRL must be set. In this case the I²C module operates in a mixed mode, both capable of starting transmissions as a leader, and being addressed as a follower. When operating in the follower mode, I2CCLK frequency must be higher than 2 MHz for Standard-mode, 5 MHz for Fast-mode, and 14 MHz for Fast-mode Plus.

22.3.10.1 Follower State Machine

The follower state machine is shown in Figure 22.17 I2C Follower State Machine on page 702. The dotted lines show where I²C-specific interrupt flags are set. The full-drawn circles show places where interaction may be required by software to let the transmission proceed.

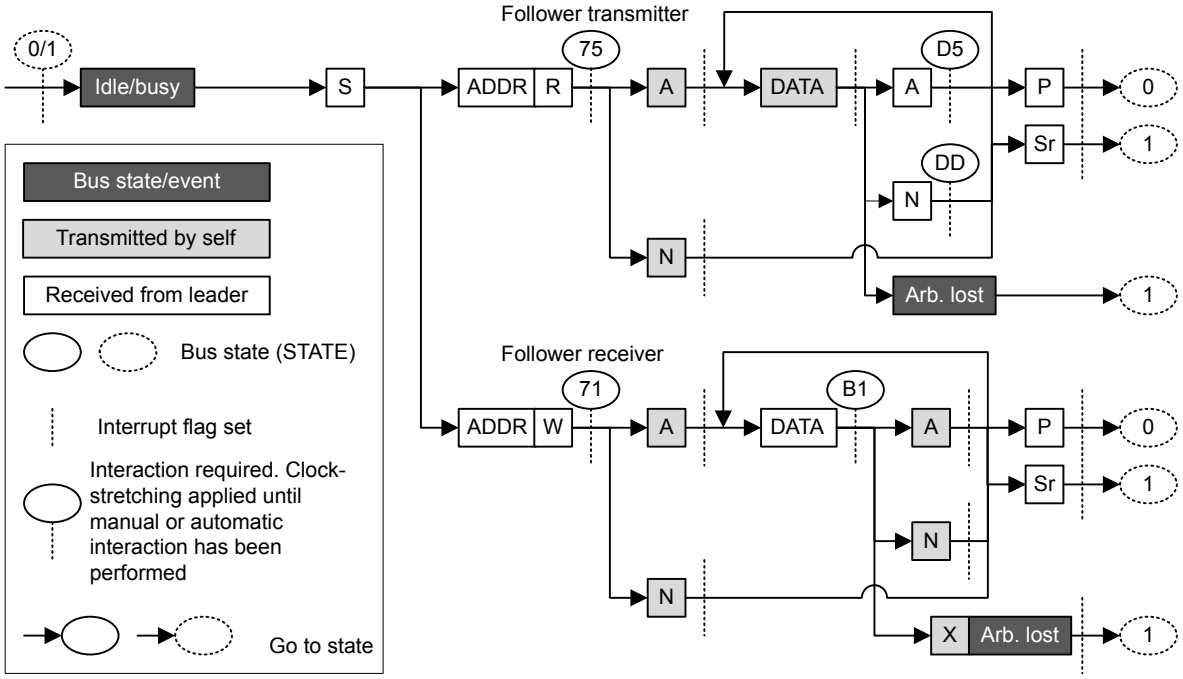


Figure 22.17. I2C Follower State Machine

22.3.10.2 Address Recognition

The I²C module provides automatic address recognition for 7-bit addresses. 10-bit address recognition is not fully automatic, but can be assisted by the 7-bit address comparator as shown in 22.3.12 Using 10-bit Addresses. Address recognition is supported in EM2/3 for I2C0 - however, the I²C0 module must be configured to use pins on either Port A or B if wakeup on address recognition from EM2/3 is desired. All other ports are available only in EM0/1. See GPIO chapter for more details.

The follower address, i.e., the address which the I²C module should be addressed with, is defined in the I2C_SADDR register. In addition to the address, a mask must be specified, telling the address comparator which bits of an incoming address to compare with the address defined in I2C_SADDR. The mask is defined in I2C_SADDRMASK, and for every zero in the mask, the corresponding bit in the follower address is treated as a don't-care, i.e., the 0-masked bits are ignored.

An incoming address that fails address recognition is automatically replied to with a NACK. Since only the bits defined by the mask are checked, a mask with a value 0x00 will result in all addresses being accepted. A mask with a value 0x7F will only match the exact address defined in I2C_SADDR, while a mask 0x70 will match all addresses where the three most significant bits in I2C_SADDR and the incoming address are equal.

If GCAMEN in I2C_CTRL is not set, the start-byte, i.e., the general call address with the R/W bit set is ignored unless it is included in the defined follower address and the address mask.

When an address is accepted by the address comparator, the decision of whether to ACK or NACK the address is passed to software.

22.3.10.3 Follower Transmitter

When SLAVE in I2C_CTRL is set, the RSTART interrupt flag in I2C_IF will be set when repeated START conditions are detected. After a START or repeated START condition, the bus leader will transmit an address along with an R/W bit. If there is no room in the receive shift register for the address, the bus will be held by the follower until room is available in the shift register. Transmission then continues and the address is loaded into the shift register. If this address does not pass address recognition, it is automatically NACK'ed by the follower, and the follower goes to an idle state. The address byte is in this case discarded, making the shift register ready for a new address. It is not loaded into the receive buffer.

If the address was accepted and the R/W bit was set (R), indicating that the leader wishes to read from the follower, the follower now goes into the follower transmitter mode. Software interaction is now required to decide whether the follower wants to acknowledge the request or not. The accepted address byte is loaded into the receive buffer like a regular data byte. If no valid interaction is pending, the bus is held until the follower responds with a command. The follower can reject the request with a single NACK command.

The follower will in that case go to an idle state, and wait for the next start condition. To continue the transmission, the follower must make sure data is loaded into the transmit buffer and send an ACK. The loaded data will then be transmitted to the leader, and an ACK or NACK will be received from the leader.

Data transmission can also continue after a NACK if a CONT command is issued along with the NACK. This is not standard I^2C however.

If the leader responds with an ACK, it may expect another byte of data, and data should be made available in the transmit buffer. If data is not available, the bus is held until data is available.

If the response is a NACK however, this is an indication of that the leader has received enough bytes and wishes to end the transmission. The follower now automatically goes idle, unless CONT in I2C_CMD is set and data is available for transmission. The latter is not standard I^2C.

The leader ends the transmission by sending a STOP or a repeated START. The SSTOP interrupt flag in I2C_IF is set when the leader transmits a STOP condition. If the transmission is ended with a repeated START, then the SSTOP interrupt flag is not set.

Note: The SSTOP interrupt flag in I2C_IF will be set regardless of whether the follower is participating in the transmission or not, as long as SLAVE in I2C_CTRL is set and a STOP condition is detected

If arbitration is lost at any time during transmission, the ARBLOST interrupt flag in I2C_IF is set, the bus is released and the follower goes idle.

See Table 22.7 I2C Follower Transmitter on page 703 for more information.

Table 22.7. I2C Follower Transmitter

I2C_STATE	Description	I2C_IF	Required interaction	Response
0x01	Repeated START received	RSTART interrupt flag (BUSHOLD interrupt flag)	RXDATA	Receive and compare address
0x75	ADDR + R received	ADDR interrupt flag	ACK + TXDATA	ACK will be sent, then DATA
		RXDATA interrupt flag	NACK	NACK will be sent, follower goes idle
		(BUSHOLD interrupt flag)	NACK + CONT + TXDATA	NACK will be sent, then DATA.
-	Data transmitted	TXBL interrupt flag (TXC interrupt flag)	None	
0xD5	Data transmitted, ACK received	ACK interrupt flag (BUSHOLD interrupt flag)	TXDATA	DATA will be transmitted
0xDD	Data transmitted, NACK received	NACK interrupt flag	None	The follower goes idle
		(BUSHOLD interrupt flag)	CONT + TXDATA	DATA will be transmitted

I2C_STATE	Description	I2C_IF	Required interaction	Response
-	Stop received	SSTOP interrupt flag	None	The follower goes idle
			START	START will be sent when bus becomes idle
-	Arbitration lost	ARBLOST interrupt flag	None	The follower goes idle
			START	START will be sent when the bus becomes idle

22.3.10.4 Follower Receiver

A follower receiver operation is started in the same way as a follower transmitter operation, with the exception that the address transmitted by the leader has the R/W bit cleared (W), indicating that the leader wishes to write to the follower. The follower then goes into follower receiver mode.

To receive data from the leader, the follower should respond to the address with an ACK and make sure space is available in the receive buffer. Transmission will then continue, and the follower will receive a byte from the leader.

If a NACK is sent without a CONT, the transmission is ended for the follower, and it goes idle. If the follower issues both the NACK and CONT commands and has space available in the receive buffer, it will be open for continuing reception from the leader.

When a byte has been received from the leader, the follower must ACK or NACK the byte. The responses here are the same as for the reception of the address byte.

The leader ends the transmission by sending a STOP or a repeated START. The SSTOP interrupt flag is set when the leader transmits a STOP condition. If the transmission is ended with a repeated START, then the SSTOP interrupt flag in I2C_IF is not set.

Note: The SSTOP interrupt flag in I2C_IF will be set regardless of whether the follower is participating in the transmission or not, as long as SLAVE in I2C_CTRL is set and a STOP condition is detected

If arbitration is lost at any time during transmission, the ARBLOST interrupt flag in I2C_IF is set, the bus is released and the follower goes idle.

See Table 22.8 I2C - Follower Receiver on page 705 for more information.

Table 22.8. I2C - Follower Receiver

I2C_STATE	Description	I2C_IF	Required interaction	Response
0x01	Repeated START received	RSTART interrupt flag (BUSHOLD interrupt flag)	RXDATA	Receive and compare address
0x71	ADDR + W received	ADDR interrupt flag RXDATA interrupt flag (BUSHOLD interrupt flag)	ACK + RXDATA	ACK will be sent and data will be received
			NACK	NACK will be sent, follower goes idle
			NACK + CONT + RXDATA	NACK will be sent and DATA will be received.
0xB1	Data received	RXDATA interrupt flag (BUSHOLD interrupt flag)	ACK + RXDATA	ACK will be sent and data will be received
			NACK	NACK will be sent and follower will go idle
			NACK + CONT + RXDATA	NACK will be sent and data will be received
-	Stop received	SSTOP interrupt flag	None	The follower goes idle
			START	START will be sent when bus becomes idle
-	Arbitration lost	ARBLOST interrupt flag	None	The follower goes idle
			START	START will be sent when the bus becomes idle

22.3.11 Transfer Automation

The I^2C can be set up to complete transfers with a minimal amount of interaction.

22.3.11.1 DMA

DMA can be used to automatically load data into the transmit buffer and load data out from the receive buffer. When using DMA, software is thus relieved of moving data to and from memory after each transferred byte.

22.3.11.2 Automatic ACK

When AUTOACK in I2C_CTRL is set, an ACK is sent automatically whenever an ACK interaction is possible and no higher priority interactions are pending.

22.3.11.3 Automatic STOP

A STOP can be generated automatically on two conditions. These apply only to the leader transmitter.

If AUTOSN in I2C_CTRL is set, the I^{2}C module ends a transmission by transmitting a STOP condition when operating as a leader transmitter and a NACK is received.

If AUTOSE in I2C_CTRL is set, the I^{2}C module always ends a transmission when there is no more data in the transmit buffer. If data has been transmitted on the bus, the transmission is ended after the (N)ACK has been received by the follower. If a START is sent when no data is available in the transmit buffer and AUTOSE is set, then the STOP condition is sent immediately following the START. Software must thus make sure data is available in the transmit buffer before the START condition has been fully transmitted if data is to be transferred.

22.3.12 Using 10-bit Addresses

When using 10-bit addresses in follower mode, set the I2C_SADDR register to 1111 0XX where XX are the two most significant bits of the 10-bit address, and set I2C_SADDRMASK to 0xFF. Address matches will now be given on all 10-bit addresses where the two most significant bits are correct.

When receiving an address match, the follower must acknowledge the address and receive the first data byte. This byte contains the second part of the 10-bit address. If it matches the address of the follower, the follower should ACK the byte to continue the transmission, and if it does not match, the follower should NACK it.

When the leader is operating as a leader transmitter, the data bytes will follow after the second address byte. When the leader is operating as a leader receiver however, a repeated START condition is sent after the second address byte. The address sent after this repeated START is equal to the first of the address bytes transmitted previously, but now with the R/W byte set, and only the follower that found a match on the entire 10-bit address in the previous message should ACK this address. The repeated start should take the leader into a leader receiver mode, and after the single address byte sent this time around, the follower begins transmission to the leader.

22.3.13 Error Handling

Note: Some registers in the I^{2}C module are considered static. This means that these need to be set before an I^{2}C transaction starts and need to stay stable during the entire transaction.

Specifically:

- The GCAMEN and SLAVE fields in the I2C_CTRL register
- The I2C_SADDR register
- The GPIO_I2Cn_ROUTEEN, GPIO_I2Cn_SCLROUTE, and GPIO_I2Cn_SDAROUTE registers

22.3.13.1 ABORT Command

Some bus errors may require software intervention to be resolved. The I^{2}C module provides an ABORT command, which can be set in I2C_CMD, to help resolve bus errors.

When the bus for some reason is locked up and the I^{2}C module is in the middle of a transmission it cannot get out of, or for some other reason the I^{2}C wants to abort a transmission, the ABORT command can be used.

Setting the ABORT command will make the I^{2}C module discard any data currently being transmitted or received, release the SDA and SCL lines and go to an idle mode. ABORT effectively makes the I^{2}C module forget about any ongoing transfers.

22.3.13.2 Bus Reset

A bus reset can be performed by setting the START and STOP commands in I2C_CMD while the transmit buffer is empty. A START condition will then be transmitted, immediately followed by a STOP condition. A bus reset can also be performed by transmitting a START command with the transmit buffer empty and AUTOSE set.

22.3.13.3 I2C-Bus Errors

An I^2C-bus error occurs when a START or STOP condition is misplaced, which happens when the value on SDA changes while SCL is high during bit-transmission on the I^2C-bus. If the I^2C module is part of the current transmission when a bus error occurs, any data currently being transmitted or received is discarded, SDA and SCL are released, the BUSERR interrupt flag in I2C_IF is set to indicate the error, and the module automatically takes a course of action as defined in Table 22.9 I2C Bus Error Response on page 707.

Table 22.9. I2C Bus Error Response

	Misplaced START	Misplaced STOP
In a leader/follower operation	Treated as START. Receive address.	Go idle. Perform any pending actions.

22.3.13.4 Bus Lockup

A lockup occurs when a leader or follower on the I^2C-bus has locked the SDA or SCL at a low value, preventing other devices from putting high values on the bus, and thus making communication on the bus impossible.

Many follower-only devices operating on an I^2C-bus are not capable of driving SCL low, but in the rare case that SCL is stuck LOW, the advice is to apply a hardware reset signal to the followers on the bus. If this does not work, cycle the power to the devices in order to make them release SCL.

When SDA is stuck low and SCL is free, a leader should send 9 clock pulses on SCL while tristating the SDA. This procedure is performed in the GPIO module after clearing the GPIO_I2Cn_ROUTEEN register and disabling the I2C module. The device that held the bus low should release it sometime within those 9 clocks. If not, use the same approach as for when SCL is stuck, resetting and possibly cycling power to the followers.

Lockup of SDA can be detected by keeping count of the number of continuous arbitration losses during address transmission. If arbitration is also lost during the transmission of a general call address, i.e., during the transmission of the STOP condition, which should never happen during normal operation, this is a good indication of SDA lockup.

Detection of SCL lockups can be done using the timeout functionality defined in 22.3.13.6 Clock Low Timeout

22.3.13.5 Bus Idle Timeout

When SCL has been high for a significant amount of time, this is a good indication of that the bus is idle. On an SMBus system, the bus is only allowed to be in this state for a maximum of 50 µs before the bus is considered idle.

The bus idle timeout BITO in I2C_CTRL can be used to detect situations where the bus goes idle in the middle of a transmission. The timeout can be configured in BITO, and when the bus has been idle for the given amount of time, the BITO interrupt flag in I2C_IF is set. The bus can also be set idle automatically on a bus idle timeout. This is enabled by setting GIBITO in I2C_CTRL.

When the bus idle timer times out, it wraps around and continues counting as long as its condition is true. If the bus is not set idle using GIBITO or the ABORT command in I2C_CMD, this will result in periodic timeouts.

Note: This timeout will be generated even if SDA is held low.

The bus idle timeout is active as long as the bus is busy, i.e., BUSY in I2C_STATUS is set. The timeout can be used to get the I^2C module out of the busy-state it enters when reset, see 22.3.8.4 Reset State.

22.3.13.6 Clock Low Timeout

The clock timeout, which can be configured in CLTO in I2C_CTRL, starts counting whenever SCL goes low, and times out if SCL does not go high within the configured timeout. A clock low timeout results in CLTOIF in I2C_IF being set, allowing software to take action.

When the timer times out, it wraps around and continues counting as long as SCL is low. An SCL lockup will thus result in periodic clock low timeouts as long as SCL is low.

22.3.13.7 Clock Low Error

The I^{2}C module can continue transmission in parallel with another device for the entire transaction, as long as the two communications are identical. A case may arise when (before an arbitration has been decided upon) the I^{2}C module decides to send out a repeated START or a STOP condition while the other device is still sending data. In the I^{2}C protocol specifications, such a combination results in an undefined condition. The I^{2}C deals with this by generating a clock low error. This means that if the I^{2}C is transmitting a repeated START or a STOP condition and another device (another leader or a misbehaving follower) pulls SCL low before the I^{2}C sends out the START/STOP condition on SDA, a clock low error is generated. The CLERR interrupt flag is then set in the I2C_IF register, any held lines are released and the I^{2}C device goes to idle.

22.3.14 DMA Support

The I^{2}C module has full DMA support. A request for the DMA controller to write to the I^{2}C transmit buffer can come from TXBL (transmit buffer has room for more data). The DMA controller can write to the transmit buffer using the I2C_TXDATA or the I2C_TXDOUBLE register. DMA must be configured to transfer one byte of data when writing to the I2C_TXDATA and configured for transferring two bytes of data when writing to the I2C_TXDOUBLE.

A request for the DMA controller to read from the I^{2}C receive buffer can come from RXDATAV (data available in the receive buffer). DMA must be configured to transfer one byte of data when reading from I2C_RXDATA and configured for transferring two bytes of data when reading from I2C_RXDOUBLE.

22.3.15 Interrupts

The interrupts generated by the I^{2}C module are combined into one interrupt vector, I2C_INT. If I^{2}C interrupts are enabled, an interrupt will be made if one or more of the interrupt flags in I2C_IF and their corresponding bits in I2C_IEN are set.

22.3.16 Wake-up

The I^{2}C receive section can be active all the way down to energy mode EM3 stop, and can wake up the CPU on address interrupt. All address match modes are supported.

22.4 I2C Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	I2C_IPVERSION	R	IP VERSION Register
0x004	I2C_EN	RW	Enable Register
0x008	I2C_CTRL	RW	Control Register
0x00C	I2C_CMD	W	Command Register
0x010	I2C_STATE	RH	State Register
0x014	I2C_STATUS	RH	Status Register
0x018	I2C_CLKDIV	RW	Clock Division Register
0x01C	I2C_SADDR	RW	Follower Address Register
0x020	I2C_SADDRMASK	RW	Follower Address Mask Register
0x024	I2C_RXDATA	RH	Receive Buffer Data Register
0x028	I2C_RXDOUBLE	RH	Receive Buffer Double Data Register
0x02C	I2C_RXDATAP	RH	Receive Buffer Data Peek Register
0x030	I2C_RXDOUBLEP	RH	Receive Buffer Double Data Peek Register
0x034	I2C_TXDATA	W	Transmit Buffer Data Register
0x038	I2C_TXDOUBLE	W	Transmit Buffer Double Data Register
0x03C	I2C_IF	RWH INTFLAG	Interrupt Flag Register
0x040	I2C_IEN	RW	Interrupt Enable Register
0x1000	I2C_IPVERSION_SET	R	IP VERSION Register
0x1004	I2C_EN_SET	RW	Enable Register
0x1008	I2C_CTRL_SET	RW	Control Register
0x100C	I2C_CMD_SET	W	Command Register
0x1010	I2C_STATE_SET	RH	State Register
0x1014	I2C_STATUS_SET	RH	Status Register
0x1018	I2C_CLKDIV_SET	RW	Clock Division Register
0x101C	I2C_SADDR_SET	RW	Follower Address Register
0x1020	I2C_SADDRMASK_SET	RW	Follower Address Mask Register
0x1024	I2C_RXDATA_SET	RH	Receive Buffer Data Register
0x1028	I2C_RXDOUBLE_SET	RH	Receive Buffer Double Data Register
0x102C	I2C_RXDATAP_SET	RH	Receive Buffer Data Peek Register
0x1030	I2C_RXDOUBLEP_SET	RH	Receive Buffer Double Data Peek Register
0x1034	I2C_TXDATA_SET	W	Transmit Buffer Data Register
0x1038	I2C_TXDOUBLE_SET	W	Transmit Buffer Double Data Register
0x103C	I2C_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x1040	I2C_IEN_SET	RW	Interrupt Enable Register
0x2000	I2C_IPVERSION_CLR	R	IP VERSION Register

Offset	Name	Type	Description
0x2004	I2C_EN_CLR	RW	Enable Register
0x2008	I2C_CTRL_CLR	RW	Control Register
0x200C	I2C_CMD_CLR	W	Command Register
0x2010	I2C_STATE_CLR	RH	State Register
0x2014	I2C_STATUS_CLR	RH	Status Register
0x2018	I2C_CLKDIV_CLR	RW	Clock Division Register
0x201C	I2C_SADDR_CLR	RW	Follower Address Register
0x2020	I2C_SADDRMASK_CLR	RW	Follower Address Mask Register
0x2024	I2C_RXDATA_CLR	RH	Receive Buffer Data Register
0x2028	I2C_RXDOUBLE_CLR	RH	Receive Buffer Double Data Register
0x202C	I2C_RXDATAP_CLR	RH	Receive Buffer Data Peek Register
0x2030	I2C_RXDOUBLEP_CLR	RH	Receive Buffer Double Data Peek Register
0x2034	I2C_TXDATA_CLR	W	Transmit Buffer Data Register
0x2038	I2C_TXDOUBLE_CLR	W	Transmit Buffer Double Data Register
0x203C	I2C_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x2040	I2C_IEN_CLR	RW	Interrupt Enable Register
0x3000	I2C_IPVERSION_TGL	R	IP VERSION Register
0x3004	I2C_EN_TGL	RW	Enable Register
0x3008	I2C_CTRL_TGL	RW	Control Register
0x300C	I2C_CMD_TGL	W	Command Register
0x3010	I2C_STATE_TGL	RH	State Register
0x3014	I2C_STATUS_TGL	RH	Status Register
0x3018	I2C_CLKDIV_TGL	RW	Clock Division Register
0x301C	I2C_SADDR_TGL	RW	Follower Address Register
0x3020	I2C_SADDRMASK_TGL	RW	Follower Address Mask Register
0x3024	I2C_RXDATA_TGL	RH	Receive Buffer Data Register
0x3028	I2C_RXDOUBLE_TGL	RH	Receive Buffer Double Data Register
0x302C	I2C_RXDATAP_TGL	RH	Receive Buffer Data Peek Register
0x3030	I2C_RXDOUBLEP_TGL	RH	Receive Buffer Double Data Peek Register
0x3034	I2C_TXDATA_TGL	W	Transmit Buffer Data Register
0x3038	I2C_TXDOUBLE_TGL	W	Transmit Buffer Double Data Register
0x303C	I2C_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x3040	I2C_IEN_TGL	RW	Interrupt Enable Register

22.5 I2C Register Description

22.5.1 I2C_IPVERSION - IP VERSION Register

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x0	R	**IP version ID**
	The read only IPVERSION field gives the version for this module. There may be minor software changes required for modules with different values of IPVERSION.			

22.5.2 I2C_EN - Enable Register

Offset	Bit Position																															
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																RW
Name																																EN

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	EN	0x0	RW	**module enable**
	The ENABLE bit enables the module. Software should write to CONFIG type registers before setting the ENABLE bit. Software should write to SYNC type registers only after setting the ENABLE bit.			

Value	Mode	Description
0	DISABLE	Disable Peripheral Clock
1	ENABLE	Enable Peripheral Clock

22.5.3 I2C_CTRL - Control Register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset											0x0	0x0		0x0			0x0		0x0				0x0		0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access											RW	RW		RW			RW		RW				RW		RW	RW	RW	RW	RW	RW	RW	RW
Name											SDAMONEN	SCLMONEN		CLTO			GIBITO		BITO				CLHR		TXBIL	GCAMEN	ARBDIS	AUTOSN	AUTOSE	AUTOACK	SLAVE	CORERST

Bit	Name	Reset	Access	Description
31:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21	SDAMONEN	0x0	RW	**SDA Monitor Enable**

Set to enable SDA monitor feature. This will enable SDA rise check at loopback path. This monitor can not be enabled in Multi-Leader application

Value	Mode	Description
0	DISABLE	Disable SDA Monitor
1	ENABLE	Enable SDA Monitor

Bit	Name	Reset	Access	Description
20	SCLMONEN	0x0	RW	**SCL Monitor Enable**

Set to enable SCL monitor feature. This will enable SCL rise check at loopback path. This monitor can not be enabled in Multi-Leader application

Value	Mode	Description
0	DISABLE	Disable SCL monitor
1	ENABLE	Enable SCL monitor

Bit	Name	Reset	Access	Description
19	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
18:16	CLTO	0x0	RW	**Clock Low Timeout**

Use to generate a timeout when CLK has been low for the given amount of time. Wraps around and continues counting when the timeout is reached. The timeout value can be calculated by timeout = PCC/(Fscl x (Nlow + Nhigh))

Value	Mode	Description
0	OFF	Timeout disabled
1	I2C40PCC	Timeout after 40 prescaled clock cycles. In standard mode at 100 kHz, this results in a 50us timeout.
2	I2C80PCC	Timeout after 80 prescaled clock cycles. In standard mode at 100 kHz, this results in a 100us timeout.
3	I2C160PCC	Timeout after 160 prescaled clock cycles. In standard mode at 100 kHz, this results in a 200us timeout.
4	I2C320PCC	Timeout after 320 prescaled clock cycles. In standard mode at 100 kHz, this results in a 400us timeout.

Bit	Name	Reset	Access	Description
	5	I2C1024PCC		Timeout after 1024 prescaled clock cycles. In standard mode at 100 kHz, this results in a 1280us timeout.
15	GIBITO	0x0	RW	**Go Idle on Bus Idle Timeout**
	When set, the bus automatically goes idle on a bus idle timeout, allowing new transfers to be initiated.			
	Value	Mode		Description
	0	DISABLE		A bus idle timeout has no effect on the bus state.
	1	ENABLE		A bus idle timeout tells the I2C module that the bus is idle, allowing new transfers to be initiated.
14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13:12	BITO	0x0	RW	**Bus Idle Timeout**
	Use to generate a timeout when SCL has been high for a given amount time between a START and STOP condition. When in a bus transaction, i.e. the BUSY flag is set, a timer is started whenever SCL goes high. When the timer reaches the value defined by BITO, it sets the BITO interrupt flag. The BITO interrupt flag will then be set periodically as long as SCL remains high. The bus idle timeout is active as long as BUSY is set. It is thus stopped automatically on a timeout if GIBITO is set. It is also stopped a STOP condition is detected and when the ABORT command is issued. The timeout is activated whenever the bus goes BUSY, i.e. a START condition is detected. The timeout value can be calculated by timeout = PCC/(Fscl x (Nlow + Nhigh))			
	Value	Mode		Description
	0	OFF		Timeout disabled
	1	I2C40PCC		Timeout after 40 prescaled clock cycles. In standard mode at 100 kHz, this results in a 50us timeout.
	2	I2C80PCC		Timeout after 80 prescaled clock cycles. In standard mode at 100 kHz, this results in a 100us timeout.
	3	I2C160PCC		Timeout after 160 prescaled clock cycles. In standard mode at 100 kHz, this results in a 200us timeout.
11:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	CLHR	0x0	RW	**Clock Low High Ratio**
	Determines the values of (and ratio between) the low and high parts of the clock signal generated on SCL as leader.			
	Value	Mode		Description
	0	STANDARD		Nlow=4 and Nhigh=4, and the Nlow:Nhigh ratio is 4:4
	1	ASYMMETRIC		Nlow=6 and Nhigh=3, and the Nlow:Nhigh ratio is 6:3
	2	FAST		Nlow=11 and Nhigh=6, and the Nlow:Nhigh ratio is 11:6
7	TXBIL	0x0	RW	**TX Buffer Interrupt Level**
	Determines the interrupt and status level of the transmit buffer.			
	Value	Mode		Description
	0	EMPTY		TXBL status and the TXBL interrupt flag are set when the transmit buffer becomes empty. TXBL is cleared when the buffer becomes nonempty.

Bit	Name	Reset	Access	Description
	1	HALF_FULL		TXBL status and the TXBL interrupt flag are set when the transmit buffer goes from full to half-full or empty. TXBL is cleared when the buffer becomes full
6	GCAMEN	0x0	RW	**General Call Address Match Enable**
	Set to enable address match on general call in addition to the programmed follower address.			
	Value	Mode		Description
	0	DISABLE		General call address will be NACK'ed if it is not included by the follower address and address mask.
	1	ENABLE		When a general call address is received, a software response is required
5	ARBDIS	0x0	RW	**Arbitration Disable**
	A leader or follower will not release the bus upon losing arbitration.			
	Value	Mode		Description
	0	DISABLE		When a device loses arbitration, the ARBIF interrupt flag is set and the bus is released.
	1	ENABLE		When a device loses arbitration, the ARBIF interrupt flag is set, but communication proceeds.
4	AUTOSN	0x0	RW	**Automatic STOP on NACK**
	Write to 1 to make a leader transmitter send a STOP when a NACK is received from a follower.			
	Value	Mode		Description
	0	DISABLE		Stop is not automatically sent if a NACK is received from a follower.
	1	ENABLE		The leader automatically sends a STOP if a NACK is received from a follower.
3	AUTOSE	0x0	RW	**Automatic STOP when Empty**
	Write to 1 to make a leader transmitter send a STOP when no more data is available for transmission.			
	Value	Mode		Description
	0	DISABLE		A stop must be sent manually when no more data is to be transmitted.
	1	ENABLE		The leader automatically sends a STOP when no more data is available for transmission.
2	AUTOACK	0x0	RW	**Automatic Acknowledge**
	Set to enable automatic acknowledges.			
	Value	Mode		Description
	0	DISABLE		Software must give one ACK command for each ACK transmitted on the I2C bus.
	1	ENABLE		Addresses that are not automatically NACK'ed, and all data is automatically acknowledged.
1	SLAVE	0x0	RW	**Addressable as Follower**

Bit	Name	Reset	Access	Description
	Set this bit to allow the device to be selected as an I2C follower.			

Value	Mode	Description
0	DISABLE	All addresses will be responded to with a NACK
1	ENABLE	Addresses matching the programmed follower address or the general call address (if enabled) require a response from software. Other addresses are automatically responded to with a NACK.

Bit	Name	Reset	Access	Description
0	CORERST	0x0	RW	**Soft Reset the internal state registers**
	Set to reset the I2C_STATE register, and return the I2C module to the IDLE state. Must clear this bit to resume normal operation condition			

Value	Mode	Description
0	DISABLE	No change to internal state registers
1	ENABLE	Reset the internal state registers

22.5.4 I2C_CMD - Command Register

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																									W(nB)	W(nB)	W(nB)	W(nB)	W(nB)	W(nB)	W(nB)	W(nB)
Name																									CLEARPC	CLEARTX	ABORT	CONT	NACK	ACK	STOP	START

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7	CLEARPC	0x0	W(nB)	**Clear Pending Commands**
	Set to clear pending commands.			
6	CLEARTX	0x0	W(nB)	**Clear TX**
	Set to clear transmit buffer and shift register. Will not abort ongoing transfer.			
5	ABORT	0x0	W(nB)	**Abort transmission**
	Abort the current transmission making the bus go idle. When used in combination with STOP, a STOP condition is sent as soon as possible before aborting the transmission. The stop condition is subject to clock synchronization.			
4	CONT	0x0	W(nB)	**Continue transmission**
	Set to continue transmission after a NACK has been received.			
3	NACK	0x0	W(nB)	**Send NACK**
	Set to transmit a NACK the next time an acknowledge is required.			
2	ACK	0x0	W(nB)	**Send ACK**
	Set to transmit an ACK the next time an acknowledge is required.			
1	STOP	0x0	W(nB)	**Send stop condition**
	Set to send stop condition as soon as possible.			
0	START	0x0	W(nB)	**Send start condition**
	Set to send start condition as soon as possible. If a transmission is ongoing and not owned, the start condition will be sent as soon as the bus is idle. If the current transmission is owned by this module, a repeated start condition will be sent. Use in combination with a STOP command to automatically send a STOP, then a START when the bus becomes idle.			

22.5.5 I2C_STATE - State Register

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0			0x0	0x0	0x0	0x0	0x1
Access																									R			R	R	R	R	R
Name																									STATE			BUSHOLD	NACKED	TRANSMITTER	MASTER	BUSY

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:5	STATE	0x0	R	**Transmission State**

The state of any current transmission. Cleared if the I2C module is idle.

Value	Mode	Description
0	IDLE	No transmission is being performed.
1	WAIT	Waiting for idle. Will send a start condition as soon as the bus is idle.
2	START	Start transmit phase
3	ADDR	Address transmit or receive phase
4	ADDRACK	Address ack/nack transmit or receive phase
5	DATA	Data transmit or receive phase
6	DATAACK	Data ack/nack transmit or receive phase

4	BUSHOLD	0x0	R	**Bus Held**

Set if the bus is currently being held by this I2C module.

3	NACKED	0x0	R	**Nack Received**

Set if a NACK was received and STATE is ADDRACK or DATAACK.

2	TRANSMITTER	0x0	R	**Transmitter**

Set when operating as a leader transmitter or a follower transmitter. When cleared, the system may be operating as a leader receiver, a follower receiver or the current mode is not known.

1	MASTER	0x0	R	**Leader**

Set when operating as an I2C leader. When cleared, the system may be operating as an I2C follower.

0	BUSY	0x1	R	**Bus Busy**

Set when the bus is busy. Whether the I2C module is in control of the bus or not has no effect on the value of this bit. When the MCU comes out of reset, the state of the bus is not known, and thus BUSY is set. Use the ABORT command or a bus idle timeout to force the I2C module out of the BUSY state.

22.5.6 I2C_STATUS - Status Register

Offset	Bit Position																											
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																					0x0		0x0	0x0	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																					R		R	R	R	R	R	R	R	R	R	R
Name																					TXBUFCNT		RXFULL	RXDATAV	TXBL	TXC	PABORT	PCONT	PNACK	PACK	PSTOP	PSTART

Bit	Name	Reset	Access	Description
31:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:10	TXBUFCNT	0x0	R	**TX Buffer Count** Indicates the number of buffers filled with valid data and not transmit to tx shift register
9	RXFULL	0x0	R	**RX FIFO Full** Set when the receive buffer is full. Cleared when the receive buffer is no longer full. When this bit is set, there is still room for one more frame in the receive shift register.
8	RXDATAV	0x0	R	**RX Data Valid** Set when data is available in the receive buffer. Cleared when the receive buffer is empty.
7	TXBL	0x1	R	**TX Buffer Level** Indicates the level of the transmit buffer. if TXBIL==0, set when the transmit buffer is empty. if TXBIL==1, set when the transmit buffer is half full
6	TXC	0x0	R	**TX Complete** Set when a transmission has completed and no more data is available in the transmit buffer. Cleared when a new transmission starts.
5	PABORT	0x0	R	**Pending abort** An abort is pending and will be transmitted as soon as possible.
4	PCONT	0x0	R	**Pending continue** A continue is pending and will be transmitted as soon as possible.
3	PNACK	0x0	R	**Pending NACK** A not-acknowledge is pending and will be transmitted as soon as possible.
2	PACK	0x0	R	**Pending ACK** An acknowledge is pending and will be transmitted as soon as possible.
1	PSTOP	0x0	R	**Pending STOP** A stop condition is pending and will be transmitted as soon as possible.
0	PSTART	0x0	R	**Pending START** A start condition is pending and will be transmitted as soon as possible.

22.5.7 I2C_CLKDIV - Clock Division Register

Offset	Bit Position																															
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0				
Access																												RW				
Name																												DIV				

Bit	Name	Reset	Access	Description
31:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8:0	DIV	0x0	RW	**Clock Divider** Specifies the clock divider for the I2C. Note that DIV must be 1 or higher when follower is enabled.

22.5.8 I2C_SADDR - Follower Address Register

Offset	Bit Position																															
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0				
Access																												RW				
Name																												ADDR				

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:1	ADDR	0x0	RW	**Follower address** Specifies the follower address of the device.
0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

22.5.9 I2C_SADDRMASK - Follower Address Mask Register

Offset	Bit Position																															
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									RW							
Name																									SADDRMASK							

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:1	SADDRMASK	0x0	RW	**Follower Address Mask** Specifies the significant bits of the follower address. Setting the mask to 0x00 will match all addresses, while setting it to 0x7F will only match the exact address specified by ADDR.
0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

22.5.10 I2C_RXDATA - Receive Buffer Data Register

Offset	Bit Position																															
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									R							
Name																									RXDATA							

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	RXDATA	0x0	R	**RX Data** Use this register to read from the receive buffer. Buffer is emptied on read access.

22.5.11 I2C_RXDOUBLE - Receive Buffer Double Data Register

Offset	Bit Position																													
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0								0x0							
Access																	R								R							
Name																	RXDATA1								RXDATA0							

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:8	RXDATA1	0x0	R	**RX Data 1**
	Second byte read from buffer. Buffer is emptied on read access.			
7:0	RXDATA0	0x0	R	**RX Data 0**
	First byte read from buffer. Buffer is emptied on read access.			

22.5.12 I2C_RXDATAP - Receive Buffer Data Peek Register

Offset	Bit Position																													
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									R							
Name																									RXDATAP							

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	RXDATAP	0x0	R	**RX Data Peek**
	Use this register to read from the receive buffer. Buffer is not emptied on read access.			

22.5.13 I2C_RXDOUBLEP - Receive Buffer Double Data Peek Register

Offset	Bit Position																													
0x030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0								0x0							
Access																	R								R							
Name																	RXDATAP1								RXDATAP0							

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:8	RXDATAP1	0x0	R	**RX Data 1 Peek**
	Second byte read from buffer. Buffer is not emptied on read access.			
7:0	RXDATAP0	0x0	R	**RX Data 0 Peek**
	First byte read from buffer. Buffer is not emptied on read access.			

22.5.14 I2C_TXDATA - Transmit Buffer Data Register

Offset	Bit Position																													
0x034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									W(nB)							
Name																									TXDATA							

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	TXDATA	0x0	W(nB)	**TX Data**
	Use this register to write a byte to the transmit buffer.			

22.5.15 I2C_TXDOUBLE - Transmit Buffer Double Data Register

Offset	Bit Position																													
0x038	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0								0x0							
Access																	W(nB)								W(nB)							
Name																	TXDATA1								TXDATA0							

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:8	TXDATA1	0x0	W(nB)	**TX Data**
	Second byte to write to buffer.			
7:0	TXDATA0	0x0	W(nB)	**TX Data**
	First byte to write to buffer.			

22.5.16 I2C_IF - Interrupt Flag Register

Offset	Bit Position																															
0x03C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset												0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access												RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name												SDAERR	SCLERR	CLERR	RXFULL	SSTOP	CLTO	BITO	RXUF	TXOF	BUSHOLD	BUSERR	ARBLOST	MSTOP	NACK	ACK	RXDATAV	TXBL	TXC	ADDR	RSTART	START

Bit	Name	Reset	Access	Description
31:21	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
20	SDAERR	0x0	RW	**SDA Error Interrupt Flag**
	Set when the SDA at loopback path is not equal to SDA output			
19	SCLERR	0x0	RW	**SCL Error Interrupt Flag**
	Set when the SCL at loopback path is not equal to SCL output			
18	CLERR	0x0	RW	**Clock Low Error Interrupt Flag**
	Set when the clock is pulled low before a START or a STOP condition could be transmitted.			
17	RXFULL	0x0	RW	**Receive Buffer Full Interrupt Flag**
	Set when the receive buffer becomes full.			
16	SSTOP	0x0	RW	**Follower STOP condition Interrupt Flag**
	Set when a STOP condition has been received. Will be set regardless of the follower being involved in the transaction or not.			
15	CLTO	0x0	RW	**Clock Low Timeout Interrupt Flag**
	Set on each clock low timeout. The timeout value can be set in CLTO bit field in the I2Cn_CTRL register.			
14	BITO	0x0	RW	**Bus Idle Timeout Interrupt Flag**
	Set on each bus idle timeout. The timeout value can be set in the BITO bit field in the I2Cn_CTRL register.			
13	RXUF	0x0	RW	**Receive Buffer Underflow Interrupt Flag**
	Set when data is read from the receive buffer through the I2Cn_RXDATA register while the receive buffer is empty. It is also set when data is read through the I2Cn_RXDOUBLE while the buffer is not full.			
12	TXOF	0x0	RW	**Transmit Buffer Overflow Interrupt Flag**
	Set when data is written to the transmit buffer while the transmit buffer is full.			
11	BUSHOLD	0x0	RW	**Bus Held Interrupt Flag**
	Set when the bus becomes held by the I2C module.			
10	BUSERR	0x0	RW	**Bus Error Interrupt Flag**
	Set when a bus error is detected. The bus error is resolved automatically, but the current transfer is aborted.			
9	ARBLOST	0x0	RW	**Arbitration Lost Interrupt Flag**
	Set when arbitration is lost.			
8	MSTOP	0x0	RW	**Leader STOP Condition Interrupt Flag**

Bit	Name	Reset	Access	Description
	Set when a STOP condition has been successfully transmitted. If arbitration is lost during the transmission of the STOP condition, then the MSTOP interrupt flag is not set.			
7	NACK	0x0	RW	**Not Acknowledge Received Interrupt Flag**
	Set when a NACK has been received.			
6	ACK	0x0	RW	**Acknowledge Received Interrupt Flag**
	Set when an ACK has been received.			
5	RXDATAV	0x0	RW	**Receive Data Valid Interrupt Flag**
	Set when received data is half full			
4	TXBL	0x0	RW	**Transmit Buffer Level Interrupt Flag**
	if TXBIL==0, set when the transmit buffer is empty. if TXBIL==1, set when the transmit is half full			
3	TXC	0x0	RW	**Transfer Completed Interrupt Flag**
	Set when the transmit shift register becomes empty and there is no more data in the transmit buffer.			
2	ADDR	0x0	RW	**Address Interrupt Flag**
	Set when incoming address is accepted, i.e. own address or general call address is received.			
1	RSTART	0x0	RW	**Repeated START condition Interrupt Flag**
	Set when a repeated start condition is detected.			
0	START	0x0	RW	**START condition Interrupt Flag**
	Set when a start condition is successfully transmitted.			

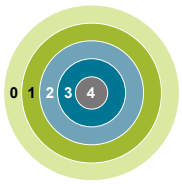
22.5.17 I2C_IEN - Interrupt Enable Register

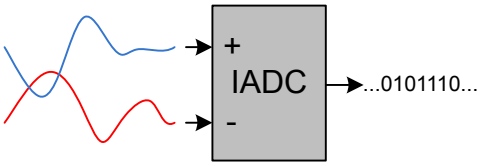
Offset	Bit Position																															
0x040	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset												0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access												RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name												SDAERR	SCLERR	CLERR	RXFULL	SSTOP	CLTO	BITO	RXUF	TXOF	BUSHOLD	BUSERR	ARBLOST	MSTOP	NACK	ACK	RXDATAV	TXBL	TXC	ADDR	RSTART	START

Bit	Name	Reset	Access	Description
31:21	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
20	SDAERR	0x0	RW	**SDA Error Interrupt Flag**
	Set when SDA at loopback path is not equal to SDA output			
19	SCLERR	0x0	RW	**SCL Error Interrupt Flag**
	Set when SCL at loopback path is not equal to SCL output			
18	CLERR	0x0	RW	**Clock Low Error Interrupt Flag**
	Set when the clock is pulled low before a START or a STOP condition could be transmitted.			
17	RXFULL	0x0	RW	**Receive Buffer Full Interrupt Flag**
	Set when the receive buffer becomes full.			
16	SSTOP	0x0	RW	**Follower STOP condition Interrupt Flag**
	Set when a STOP condition has been received. Will be set regardless of the follower being involved in the transaction or not.			
15	CLTO	0x0	RW	**Clock Low Timeout Interrupt Flag**
	Set on each clock low timeout. The timeout value can be set in CLTO bit field in the I2Cn_CTRL register.			
14	BITO	0x0	RW	**Bus Idle Timeout Interrupt Flag**
	Set on each bus idle timeout. The timeout value can be set in the BITO bit field in the I2Cn_CTRL register.			
13	RXUF	0x0	RW	**Receive Buffer Underflow Interrupt Flag**
	Set when data is read from the receive buffer through the I2Cn_RXDATA register while the receive buffer is empty. It is also set when data is read through the I2Cn_RXDOUBLE while the buffer is not full.			
12	TXOF	0x0	RW	**Transmit Buffer Overflow Interrupt Flag**
	Set when data is written to the transmit buffer while the transmit buffer is full.			
11	BUSHOLD	0x0	RW	**Bus Held Interrupt Flag**
	Set when the bus becomes held by the I2C module.			
10	BUSERR	0x0	RW	**Bus Error Interrupt Flag**
	Set when a bus error is detected. The bus error is resolved automatically, but the current transfer is aborted.			
9	ARBLOST	0x0	RW	**Arbitration Lost Interrupt Flag**
	Set when arbitration is lost.			
8	MSTOP	0x0	RW	**Leader STOP Condition Interrupt Flag**

Bit	Name	Reset	Access	Description
	Set when a STOP condition has been successfully transmitted. If arbitration is lost during the transmission of the STOP condition, then the MSTOP interrupt flag is not set.			
7	NACK	0x0	RW	**Not Acknowledge Received Interrupt Flag**
	Set when a NACK has been received.			
6	ACK	0x0	RW	**Acknowledge Received Interrupt Flag**
	Set when an ACK has been received.			
5	RXDATAV	0x0	RW	**Receive Data Valid Interrupt Flag**
	Set when data is available in the receive buffer. Cleared automatically when the receive buffer is read.			
4	TXBL	0x0	RW	**Transmit Buffer Level Interrupt Flag**
	Set when the transmit buffer becomes empty. Cleared automatically when new data is written to the transmit buffer.			
3	TXC	0x0	RW	**Transfer Completed Interrupt Flag**
	Set when the transmit shift register becomes empty and there is no more data in the transmit buffer.			
2	ADDR	0x0	RW	**Address Interrupt Flag**
	Set when incoming address is accepted, i.e. own address or general call address is received.			
1	RSTART	0x0	RW	**Repeated START condition Interrupt Flag**
	Set when a repeated start condition is detected.			
0	START	0x0	RW	**START condition Interrupt Flag**
	Set when a start condition is successfully transmitted.			

23. IADC - Incremental Analog to Digital Converter





Quick Facts

What?

The IADC is used to convert analog voltages into a digital representation and features high-speed, low-power operation.

Why?

In many applications there is a need to measure analog signals and record them in a digital representation, without exhausting the energy source.

How?

The low power IADC samples one or more input channels in a programmable sequence. With the help of PRS and DMA, the IADC can operate without CPU intervention in EM2 and EM3, minimizing the number of powered up resources. The IADC can be automatically shut down between conversions to further reduce the energy consumption.

23.1 Introduction

The IADC uses an Incremental Analog to Digital architecture, with a resolution of 12 bits when operating at one million samples per second (1 Msps). The flexible incremental architecture uses oversampling to allow applications to trade speed for higher resolution. An integrated input multiplexer can select from external I/Os and several internal signals.

23.2 Features

- Flexible oversampled architecture allows for tradeoffs between speed and resolution.
  - 1 Msps with oversampling ratio = 2
  - 555 ksps with oversampling ratio = 4
  - 76.9 ksps with oversampling ratio = 32
- Digital post-averaging
- Internal and external conversion trigger sources
  - Immediate (software triggered)
  - Local IADC timer
  - External TIMER module (synchronous with output / PWM generation)
  - General PRS hardware signal
- Integrated prescaler for conversion clock generation
- Can be run during EM2 and EM3, waking up the system on interrupts as needed
- Selectable reference sources
  - 1.21 V internal reference
  - External precision reference
  - Analog supply
- Support for offset and gain calibration
- Programmable input gain: 0.5x, 1x, 2x, 3x, or 4x
- Flexible output formatting
  - Unipolar or 2's complement bipolar data
  - Results can be saved in 12 bit, 16 bit, or 20 bit format
  - Programmable left or right justification
  - Optional channel ID tag
- Digital window comparison function detects when results are inside/outside a programmable window
- Two independent groups of configuration registers for setting IADC mode, clock prescaler, reference selection, oversample rate, unipolar/bipolar output formatting, and analog gain
- Programmable single channel conversion
  - Can use either configuration group
  - Triggered by any conversion trigger source
  - Can be tailgated after a scan sequence
  - One shot or continuous mode
  - Local FIFO for immediate data storage
  - Programmable watermark level to generate interrupt or initiate DMA transfer
  - Supports overflow and underflow interrupt generation
  - Supports window compare function
- Autonomous multi-channel scan
  - Up to 16 configurable slots in scan sequence
  - Each slot allows independent selection of configuration group, channel selection, and window compare enable
  - Triggered by any conversion trigger source
  - One shot or continuous mode
  - Local FIFO for immediate data storage
  - Programmable watermark level to generate interrupt or initiate DMA transfer
  - Supports overflow and underflow interrupt generation
  - Conversion tailgating support for predictable periodic scans

- Available interrupt sources:
  - Single FIFO has DVL (data valid level) entries available (also generates DMA request)
  - Scan FIFO has DVL (data valid level) entries available (also generates DMA request)
  - Single FIFO result compared true for digital compare window
  - Scan FIFO result compared true for digital compare window
  - Single queue conversion has completed
  - Scan queue entry conversion has completed
  - Scan queue table conversion has completed
  - Single FIFO overflow or underflow
  - Scan FIFO overflow or underflow
  - Polarity Error interrupt
  - Port Allocation Error interrupt
  - EM23 clock configuration error

23.3 Functional Description

The incremental ADC module block diagram is shown in Figure 23.1 IADC Overview on page 730.

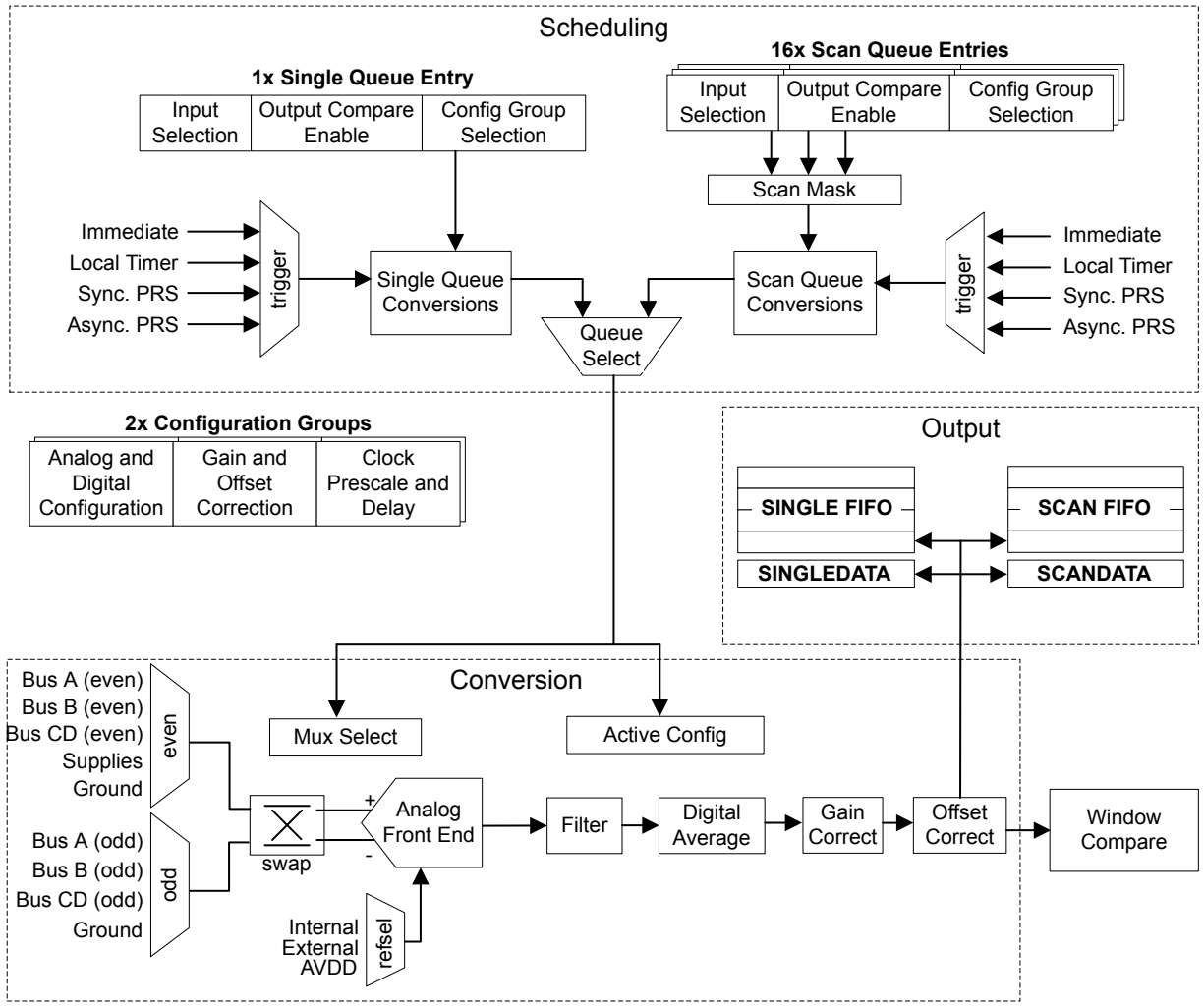


Figure 23.1. IADC Overview

23.3.1 Register Access

Many of the IADC module's configuration registers can only be written while the module is disabled (IADC_EN_EN = 0). These are IADC_CTRL, IADC_TIMER, IADC_CMPTHR, IADC_TRIGGER, IADC_CFGx, IADC_SCALEx, IADC_SCHEDx, and IADC_SCANx. A typical setup sequence for the IADC module is:

1. With the IADC disabled (IADC_EN_EN = 0), program all configuration registers listed above.
2. Enable the IADC by setting EN in IADC_EN to 1.
3. Program the remaining configuration registers.
4. Enable the single or scan queue.
5. The IADC is ready for use.

23.3.2 Clocking

The IADC logic is partitioned into two clock domains: CLK_BUS (APBIF) and CLK_SRC_ADC (CORE). The APBIF domain contains the IADC registers and FIFO read logic. The rest of the IADC is clocked mainly by CLK_SRC_ADC and ADC_CLK, both of which are derived from CLK_CMU_ADC, as shown in Figure 23.2 Clocking on page 732.

CLK_CMU_ADC is the incoming clock routed to the ADC by the CMU, and may be up to 80 MHz. It is selected within the CMU module. If the ADC is to be used synchronously with an external TIMER module, the clock should be configured to derive from the group A clock. If configuring for operation in EM2 or EM3, a clock source available in EM2 and EM3 must be used directly, as the group A clock multiplexer will be shut down in EM2 and EM3.

CLK_SRC_ADC is derived from CLK_CMU_ADC, and must be no faster than 40 MHz. The HSCLKRATE field in IADC_CTRL sets the prescaler to divide CLK_CMU_ADC. If CLK_CMU_ADC is already 40 MHz or slower, HSCLKRATE can be set to 0x0 to pass the clock through to CLK_SRC_ADC without dividing it. CLK_SRC_ADC is the clock source used for the TIMEBASE prescaler as well as the local IADC timer.

ADC_CLK is used to drive the ADC front-end and state machine logic. Another prescaler is used to reduce CLK_SRC_ADC to a suitable frequency for the ADC operating mode. Because the operational mode may be different for single vs. scan conversions, or even for different conversions within a scan, each configuration group has a PRESCALE bit field in the IADC_SCHEDx register. PRESCALE must be set to limit ADC_CLK to no faster than 10 MHz in normal mode for 0.5x and 1x analog gain settings. For analog gain of 2x, 3x, and 4x, the maximum ADC_CLK is 5 MHz, 2.5 MHz, or 2.5 MHz respectively. It is recommended to run ADC_CLK no slower than 100 kHz.

Note: If HSCLKRATE is configured to divide CLK_CMU_ADC by more than 1 (HSCLKRATE != 0), then PRESCALE must not be set to divide by 1 (PRESCALE = 0). When this condition is detected, a PRESCALE value of 1 (divide by 2) will be automatically be used instead of the programmed PRESCALE value.

The suspend mode fields IADC_CTRL_ADCCLKSUSPEND0 (for scan conversions) or IADC_CTRL_ADCCLKSUSPEND1 (for single conversions) can be used to shut down the clock between conversions and save power. The ADC logic will wake up the clock before starting IADC warmup and performing a conversion. If the suspend mode is set, the clock will shut down again once the conversion is complete.

When IADC_TRIGGER_SCANTRIGSEL or IADC_TRIGGER_SINGLETRIGSEL is set to IMMEDIATE, IADC_CTRL_ADCCLKSUSPENDn will force the clock to only be running when one of the queues is enabled.

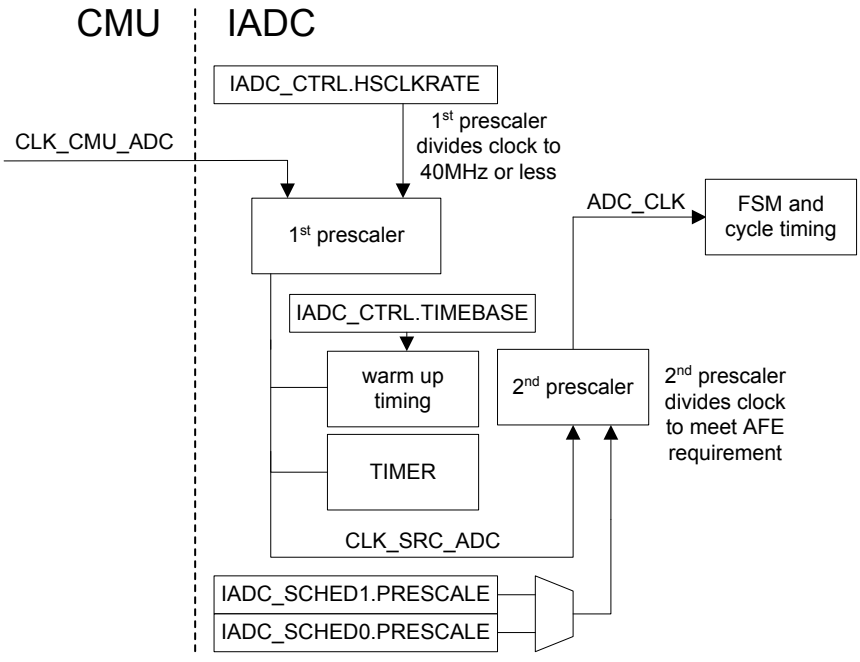


Figure 23.2. Clocking

23.3.3 Conversion Timing

The IADC takes multiple samples of the analog signal to produce each output. The number of input samples contributing to an output word is determined by the oversampling ratio (OSR). Higher OSR settings will improve the ADC's INL and DNL, and reduce system-level noise, but require more time for each conversion. Different OSRs may be specified for each configuration group. It is important to note that oversampling is an analog process which provides more input samples to the digital filter. The OSR is configured with the OSRHS bit field in the IADC_CFGx register.

During a conversion, the effective front-end sampling frequency (F_{sample}) in normal mode is equal to ADC_CLK / 4.

23.3.3.1 Warmup Time

To save energy, the IADC can be configured to power down completely or enter a standby state between conversions, if full speed operation is not required for the application. The required ADC warm up time from a full powered-down state is 5 us. Warmup from a standby state requires 1 us. Warmup is automatically timed by the ADC logic when it is required, but software must configure the TIMEBASE field in IADC_CTRL for a minimum 1 us interval. Note that the TIMEBASE counter receives CLK_SRC_ADC, and should be programmed based on that frequency. For example, if CLK_SRC_ADC is 40 MHz, TIMEBASE should be set to at least 0x27 (39) to produce the minimum 1 us interval. When transitioning from a powered-down state, the IADC will use five TIMEBASE intervals. When in standby the IADC will use one TIMEBASE interval.

The WARMUPMODE field in the IADC_CTRL register defines whether the IADC is powered down between conversions (WARMUPMODE = NORMAL), in standby between conversions (WARMUPMODE = KEEPINSTANDBY), or remains powered up (WARMUPMODE = KEEPWARM). The resulting start-up time is shown in Figure 23.3 Start-up Timing on page 733. Note that even in WARMUPMODE = KEEPWARM or KEEPINSTANDBY, the ADC will implement 5 TIMEBASE intervals of warmup on initial power up, or any configuration change affecting PRESCALE, ADCMODE, or REFSEL. IADC_STATUS_ADCWARM reflects the current warmup status of the IADC.

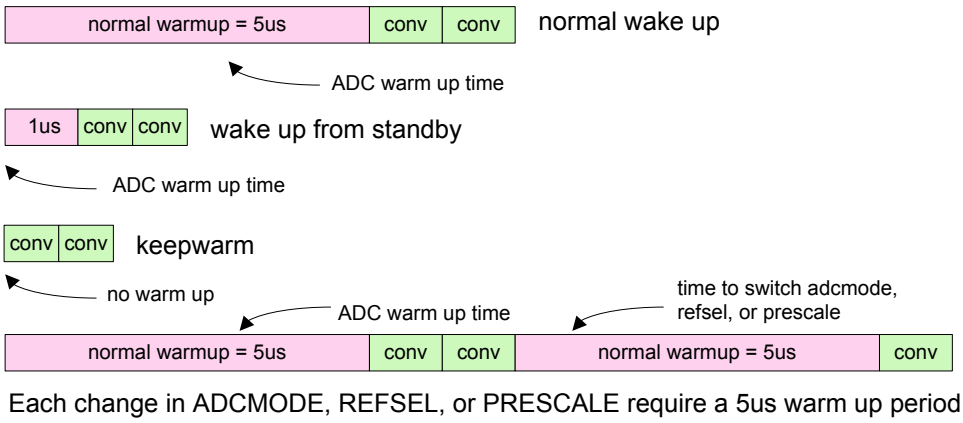


Figure 23.3. Start-up Timing

23.3.3.2 Conversion Pipeline

The IADC uses a pipelined architecture to perform different stages of the ADC conversion in parallel.

The conversion time for a single sample can be determined from the OSR and the pre-scaled CLK_ADC frequency (f_{CLK_ADC}) as:

Conversion Time = ((4 * OSR) + 2) / f_{CLK_ADC}

The minimum OSR is 2, meaning that the fastest possible conversion lasts 10 CLK_ADC clock cycles.

The IADC will automatically insert 2 additional cycles in the pipeline when changing channels to a new GPIO. This allows for hold timing on the previous conversion and allows for time to tristate the ABUS analog buses before connecting the next GPIO to the analog bus. Therefore the maximum sampling rate while continuously sampling on one channel (with CLK_ADC = 10 MHz) is 1 Msps, and the maximum sampling rate while switching channels is 833 ksps. Figure 23.4 Normal ADC Mode Pipeline on page 734 shows both single-channel and channel-switching scenarios powering up from a shutdown state with WARMUPMODE = NORMAL. The 5 us warmup is shown in pink, a first conversion pipeline in green, and a second conversion in orange. The blue area in the top diagram represents the extra time to tristate while changing channels.

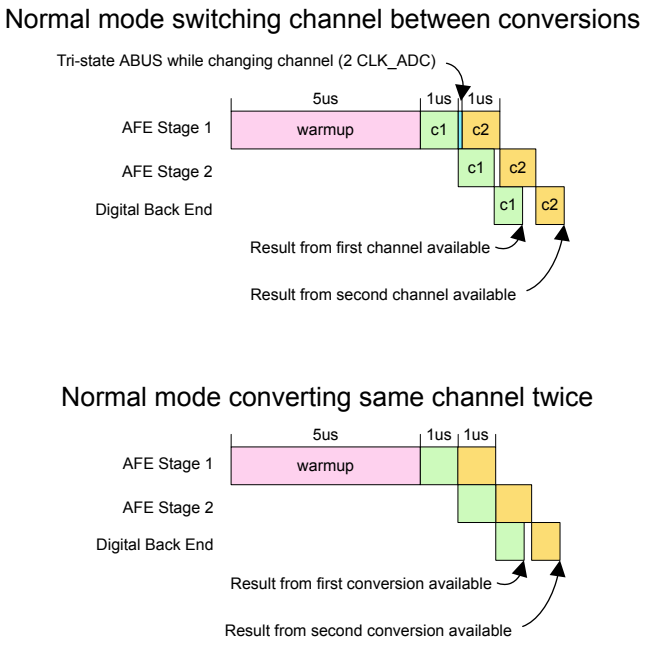


Figure 23.4. Normal ADC Mode Pipeline

23.3.3.3 Scheduling and Triggers

The IADC has several triggering options available for both the Single queue and the Scan queue. When a conversion trigger occurs and there are no other conversions active or pending, the request is serviced immediately. If both the single and scan queues are being used in an application, it is possible to serve the conversion requests as needed, and specify their priority.

Conversion triggering is configured using bit fields in the IADC_TRIGGER register. The SINGLETRIGSEL and SCANTRIGSEL fields specify the trigger source for Single and Scan conversion queues, respectively. The options for trigger source are:

- IMMEDIATE - Trigger from software. This is useful for triggering conversions on-demand from software with no specific sampling frequency requirements, or initiating continuous conversions at full speed.
- TIMER - Use the IADC local timer to trigger conversions. This is useful for triggering conversions at precise intervals.
- PRSCLKGRP - Use a synchronous PRS channel to trigger from an external peripheral in the same clock group domain (i.e. clock group A). This is useful for synchronizing conversions precisely with external TIMER events or PWM outputs.

  Note: It is recommended to configure the PRS consumer registers prior to enabling synchronous PRS triggers to avoid false triggers.

- PRSPOS - Use a positive edge of an asynchronous PRS channel to trigger conversions. The trigger source will require 1-2 ADC_SRC_CLK cycles to synchronize. This is useful for triggering conversions as needed from asynchronous peripheral sources such as GPIO inputs, SYSRTC events, etc.
- PRSNEG - Use a negative edge of an asynchronous PRS channel to trigger conversions. This is the same as PRSPOS, but operates on negative edges of the selected input.

Both the single and scan trigger sources can be configured to generate one request per trigger, or begin continuous conversions. Setting SINGLETRIGACTION to ONCE will make one conversion request each time the selected single trigger occurs, and a single ADC output will be converted. Setting SINGLETRIGACTION to CONTINUOUS allows the single trigger to begin the first conversion, and when a conversion completes a new one will be requested immediately without requiring a new trigger. Channel selections and configuration should not be changed while SINGLETRIGACTION is set to CONTINUOUS. Doing so can produce conversion errors. The scan queue should be used if channel or configuration switching is required.

The SCANTRIGACTION field works to request conversion scans in a similar manner. Setting SCANTRIGACTION to ONCE will make one request each time the selected scan trigger occurs, and the IADC will perform all conversions specified in the scan once before stopping. Setting SCANTRIGACTION to CONTINUOUS allows the scan trigger to initiate continuous scans. When a scan cycle completes, a new one will be requested immediately without requiring a new trigger.

Conversion priority can be adjusted using the SINGLETAILGATE bit. By default, SINGLETAILGATE is set to TAILGATEOFF, meaning that conversion triggers are queued in the order they are received. Any conversion trigger for the Single queue or the Scan queue will initiate a conversion as soon as possible. If any conversion is already in progress or pending, the new conversion will be handled after the current operation.

Setting SINGLETAILGATE to TAILGATEON gives ultimate priority to the Scan queue. The IADC will only perform single conversions immediately after completion of a scan. This allows systems to use the scan queue for high-priority conversions with tight timing requirements, and the single queue for low-priority, on-demand conversion events. Note that this setting should only be used when scan conversions are guaranteed to trigger. If no scan sequence is triggered, any single conversion trigger will remain pending indefinitely. It is also important to note that if there is not enough time between scan conversions to service a single conversion, the next scan conversion will be delayed.

23.3.3.3.1 Conversion Triggering Examples

Scheduling a Single Sample

The simplest use case for the IADC is performing one conversion on-demand from the Single queue. Figure 23.5 Immediate Single Conversion on page 736 shows the configuration and timing of this use case. The IADC warmup mode is configured for normal (shuts down between conversions). The single queue trigger is configured for immediate triggering of one conversion, and tailgating is turned off. When the conversion is requested (by setting IADC_CMD_SINGLESTART), the IADC block warms up and then begins converting. During the conversion, the CONVERTING bit in IADC_STATUS is set. When the conversion is complete, the queue is disabled, and SINGLEQEN returns low.

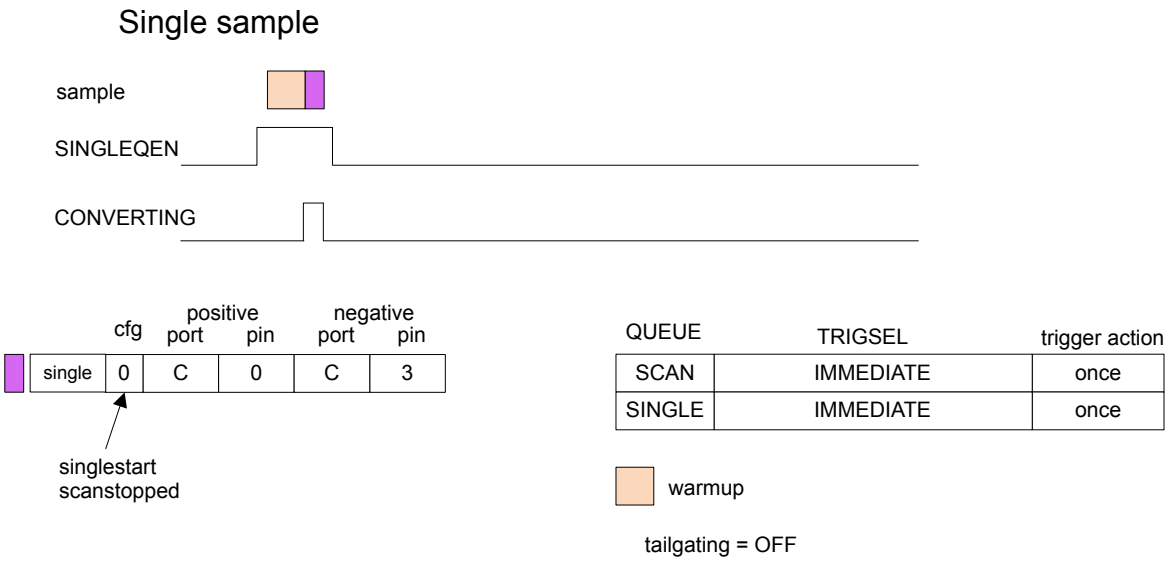


Figure 23.5. Immediate Single Conversion

Periodic Scans

Another common use case is to periodically trigger the IADC to perform a multi-channel scan. Figure 23.6 Periodic Scan Example on page 737 shows the timing of a periodic scan triggered by the IADC's local timer. The scanner is configured to sample four different channels; two using configuration 0 and two using configuration 1. Note that a single TIMER trigger is used to initiate each scan, and all four samples are taken for each trigger. Note also that the IADC inserts another warmup time between conversions 1 and 2, when it switches from configuration 0 to configuration 1. The single queue is disabled and not used in this example.

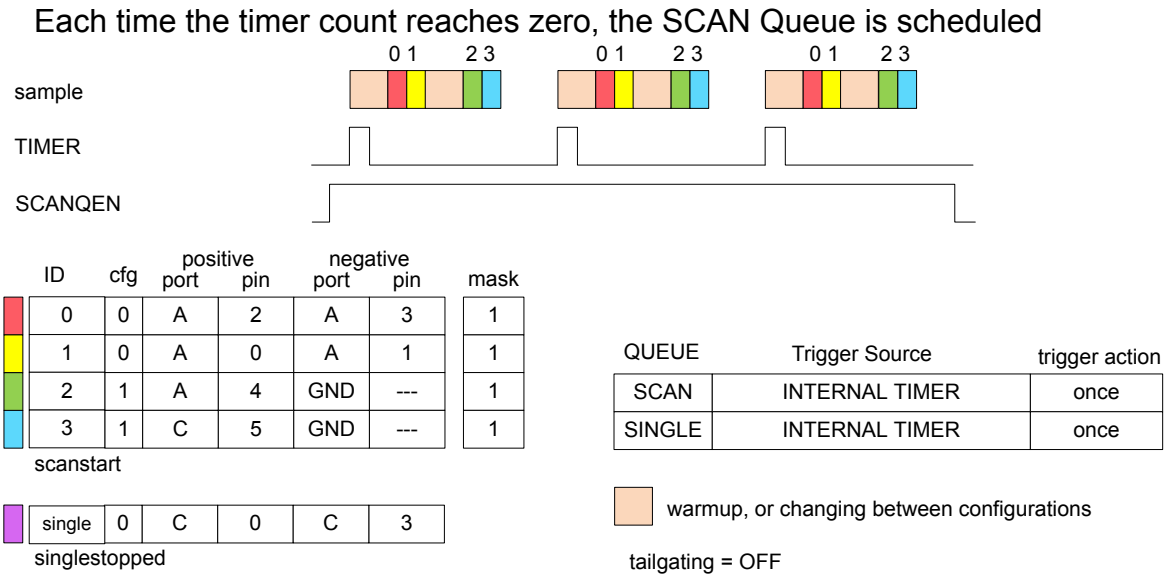


Figure 23.6. Periodic Scan Example

Tailgating Examples

An example using conversion tailgating is shown in Figure 23.7 Simple Conversion with Tailgating Enabled on page 738. In the example, the Scan queue is configured to trigger a two-channel conversion periodically on the IADC local timer, while the Single queue is configured to trigger on-demand from software. When a single conversion is requested, it waits until after the scan sequence is complete, and then the single conversion is performed. The scan conversions are using configuration 0, and the single conversion is using configuration 1, so a warmup delay is inserted between the end of the scan and the beginning of the single conversion cycle. Note that this example provides plenty of time between IADC scan conversions for the single conversion to occur, and no scan conversions are delayed.

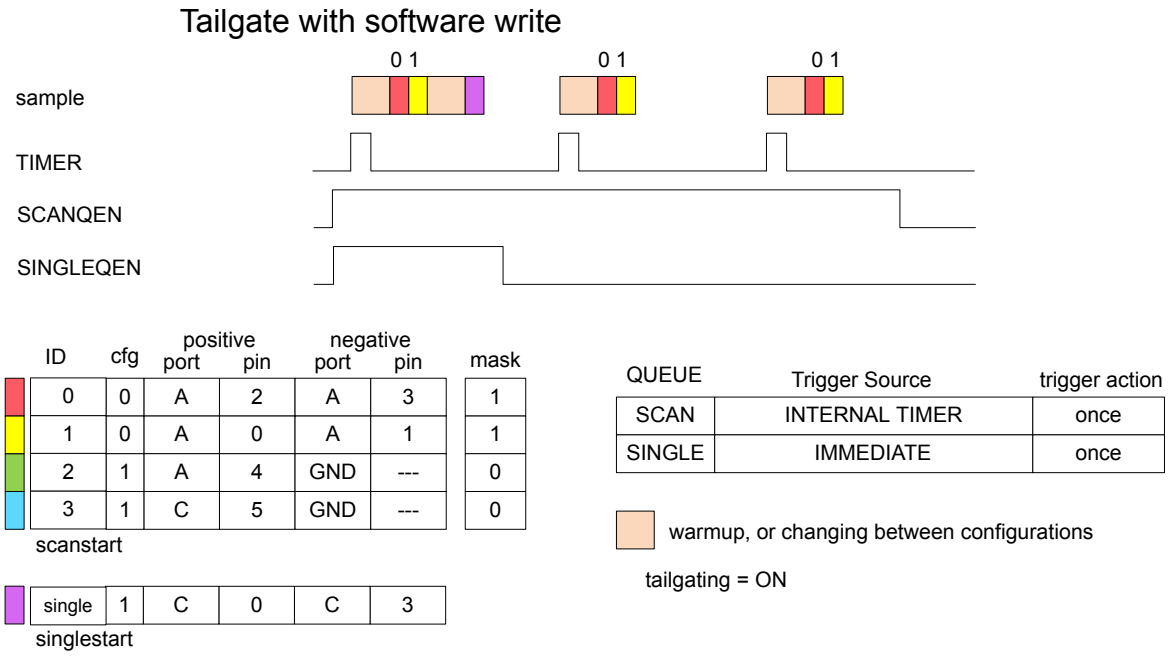


Figure 23.7. Simple Conversion with Tailgating Enabled

Another example, shown in Figure 23.8 Conversions with Tailgating Disabled on page 739, demonstrates how requests are handled on the different conversion queues with tailgating disabled.

In this example, the scan queue is being triggered on the internal timer while the single queue is being triggered on a PRS positive edge. Since tailgating is not enabled, the queues will be serviced on a first come first served basis. The first single queue trigger falls between two scan queue triggers and does not interfere with scan queue timing. The second single queue trigger happens just before the scan queue trigger. The IADC will complete this single queue conversion and delay the next scan queue conversions.

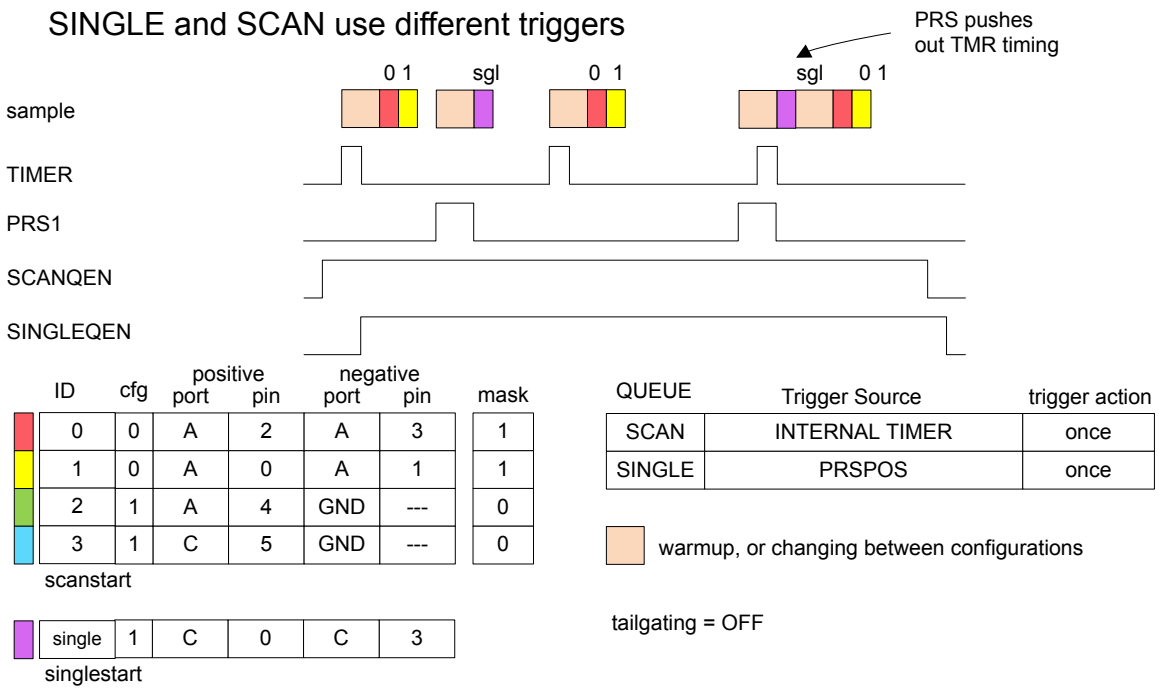


Figure 23.8. Conversions with Tailgating Disabled

Continuous Conversions

An example of continuous conversions triggered from the scan queue is shown in Figure 23.9 Continuous Conversions on page 739. In this example the SCANTRIGACTION field in IADC_TRIGGER is set to CONTINUOUS, and the conversion trigger source is software (SCANTRIGSEL = IMMEDIATE). When the scan queue is enabled with IADC_CMD_SCANSTART, the ADC warms up and then performs repeated back-to-back scans until software disables the scan queue using IADC_CMD_SCANSTOP. While this example shows only one channel converted continuously, it is possible to enable multiple channels for the scan sequence.

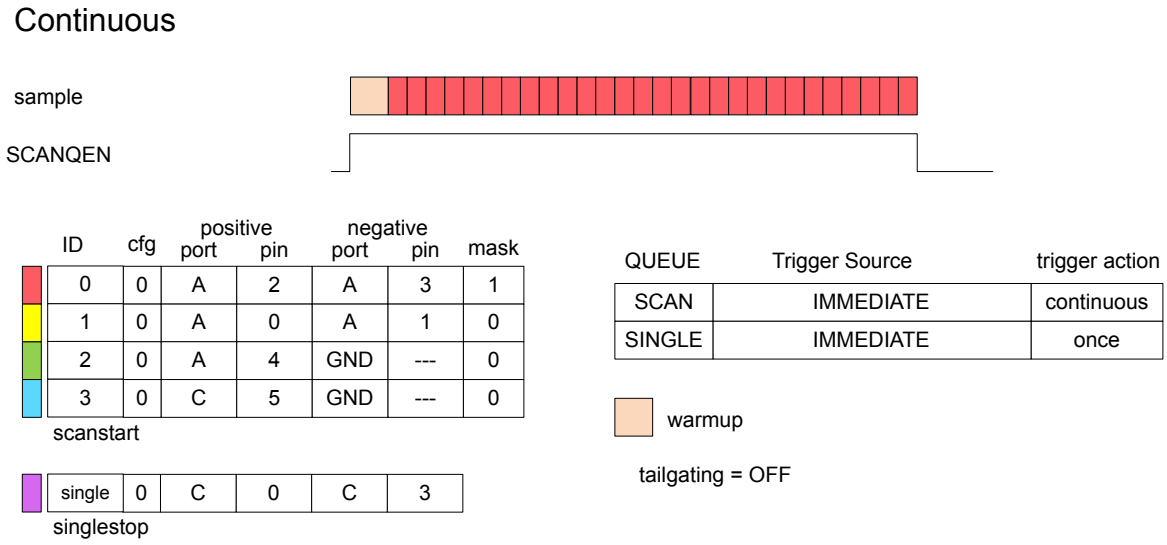


Figure 23.9. Continuous Conversions

23.3.4 Reference Selection and Analog Gain

The default IADC reference is to use the internal band gap circuit. The analog power supply voltage can also be used as a voltage reference. The reference voltage is selected using the REFSEL field in IADC_CFGx.

Table 23.1. Mode Settings

Reference	Description	Voltage
VBGR	Internal	1.21V
VDDX	Analog Power Supply	AVDD
VREF	External	1.0V - AVDD (1.25V Nominal)

The IADC also has analog gain selection, controlled via the ANALOGGAIN field in IADC_CFGx. The analog gain can be set to 0.5x, 1x, 2x, 3x, or 4x. Note that 2x, 3x, and 4x gain modes may require slower ADC_CLK. The analog gain impacts where the full-scale input reading occurs. For example, with a 1.25 V external reference and ANALOGGAIN set to 2x, the analog input to the IADC is multiplied by a factor of 2, and a full-scale reading occurs at 1.25 V / 2 = 0.625 V. If ANALOGGAIN is set to 0.5x, the full-scale reading of the ADC will not occur until the input reaches 2.5 V. Note that the ADC is only capable of measuring inputs within the supply rails of the device. If the full scale is configured to be greater than the supply voltage, the maximum input will be limited to the supply.

The sampling capacitance (C_{sample}) is changed according to the analog gain setting.

Table 23.2. Input Sampling Capacitance vs. Analog Gain

Analog Gain Setting	Input Sampling Capacitance
0.5x	1 pF
1x	2 pF
2x	4 pF
3x	6 pF
4x	8 pF

Given the sampling capacitance and the front-end sampling rate (F_{sample}), the input impedance of the converter can be calculated as:

$Z_{in} = 1 / (C_{sample} * F_{sample})$

Note that the input is not sampled when the converter is inactive between conversions and operating with WARMUPMODE = NORMAL or KEEPINSTANDBY with longer intervals between conversion triggers can increase the effective input impedance of the converter.

23.3.5 Input and Configuration Selection

The IADC supports measurement on a number of internal and external signals. External signals are routed to GPIO through shared ABUS resources on the device, or (on some devices) through dedicated analog inputs available to the IADC block.

The single queue and the scan queue have separate registers available to select inputs and configurations. The IADC_SINGLE register is used to select the input and configuration for the single queue. The IADC_SCANx registers are used to select the inputs and configurations for each of the scan table entries. In both cases, the register contents and setup are similar. The PORTPOS and PINPOS fields are used to select a signal for the positive ADC input, while PORTNEG and PINNEG are used to select a signal for the negative ADC input. The CFG field selects which of the two configuration sets will be used with the input (i.e. configuration options specified in IADC_CFGx, IADC_SCALEx, and IADC_SCHEDx).

To perform single-ended conversions, the PORTNEG field should be set to GND. This indicates that the positive ADC input will be measured with reference to chip ground. PORTPOS and PINPOS should be used to select the desired input signal. The PINNEG field is not used for single-ended conversions.

To perform differential conversions, PORTPOS, PINPOS are used to select the positive input to the ADC, while PORTNEG and PINNEG are used to select the negative input. Note that there are two independent multiplexers in the ADC, and firmware cannot select two signals from the same multiplexer for a differential measurement. The "even" multiplexer consists of all EVEN ABUS selections, Supply voltage options, and GND. The "odd" multiplexer consists of all ODD ABUS selections and GND. One selection from each multiplexer is allowed on the positive and negative input. More detailed examples may be found in 23.3.5.3 ABUS Input Selection Examples.

The scan queue has one additional register, IADC_MASKREQ, to specify which of the 16 possible channel slots will be converted during a scan operation. Each channel in the scan queue is enabled by writing the corresponding bit in the IADC_MASKREQ register to 1. Enabled channels will be converted in sequence from lowest to highest, during a scan. See 23.3.5.4 Scan Queue for more details on using the scan queue.

23.3.5.1 External GPIO Inputs

GPIO input selections are routed through shared ABUS resources. In order for the IADC to use any GPIO as an input, the IADC must be allocated appropriate analog bus resources in the GPIO_ABUSALLOC, GPIO_BBUSALLOC, or GPIO_CDBUSALLOC registers. For example, if IADC0 will be using both odd and even numbered pins on GPIO port PA, then AEVEN0 and AODD0 in GPIO_ABUSALLOC could both be set to IADC0. This gives IADC0 access to these two buses. Generally, bus access is set to specific peripherals at configuration time and left alone - it is not normally required to change the bus allocation on the fly. If the IADC requests a pin from a bus that has not been allocated to the IADC, an error will be generated, the PORTALLOCERRIF in IADC_IF will be set, and any conversion result will be 0. For more details on analog bus structure and capabilities, refer to the GPIO section.

When the appropriate analog buses have been configured to route to the IADC, GPIO selection is a simple matter of programming the desired port and pin into the PORTPOS, PINPOS, PORTNEG, and PINNEG fields. For example, to configure a channel to convert the differential voltage between pins PA5 and PA4, PORTPOS = PORTA, PINPOS = 5, PORTNEG = PORTA, PINNEG = 4. If an invalid selection is made, a polarity error will be generated. More specific examples are described in 23.3.5.3 ABUS Input Selection Examples.

23.3.5.2 Internal and Dedicated Inputs

Internal signals and dedicated inputs are not routed through the shared ABUS resources. In general, these resources are selected directly by the settings of PORTPOS and PORTNEG, while the PINPOS and PINNEG fields are not used. When PORTPOS is set to SUPPLY, PINPOS is used to select which of the power supplies is connected. To facilitate power supply measurements using internal reference options, higher voltage supplies are attenuated by a factor of 4.

Table 23.3. Supply Selection (PORTPOS = SUPPLY)

PINPOS	Supply Connection	Voltage at Positive Input
0	AVDD	AVDD / 4
1	IOVDD0	IOVDD0 / 4
2	IOVDD1	IOVDD1 / 4
3	IOVDD2	IOVDD2 / 4
4	DVDD	DVDD / 4
7	DECOUPLE	DECOUPLE

If an internal signal is selected for PORTPOS or PORTNEG, selecting GND on the opposite input will instruct the converter to perform a single-ended conversion. In the case where PORTPOS = GND, the IADC logic will automatically swap the direct input selected by PORTNEG to the positive input of the ADC. Otherwise, a differential conversion is performed with PORTPOS selecting the positive and PORTNEG selecting the negative input.

23.3.5.3 ABUS Input Selection Examples

When configuring to measure a single-ended signal through the ABUS, the positive input selection should always point to the desired input, and PORTNEG should be programmed to GND.

Correct configuration examples for single-ended conversions are shown in Figure 23.10 Single-Ended Port/Pin Selection Odd Channel on page 743 and Figure 23.11 Single-Ended Port/Pin Selection Even Channel on page 743. Note that the IADC logic will automatically swap the appropriate multiplexer to the positive input of the ADC.

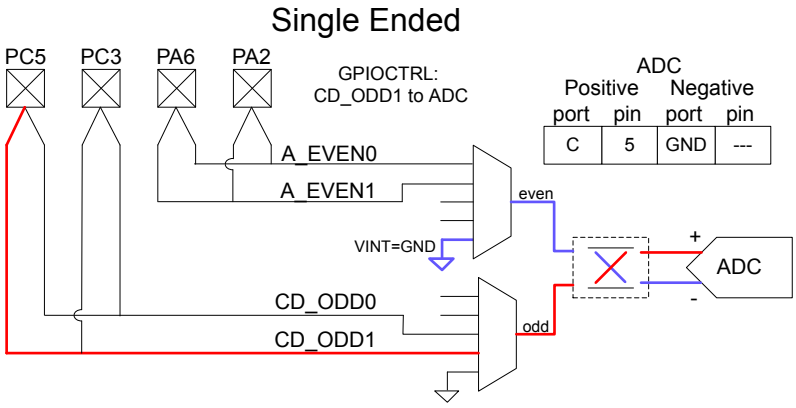


Figure 23.10. Single-Ended Port/Pin Selection Odd Channel

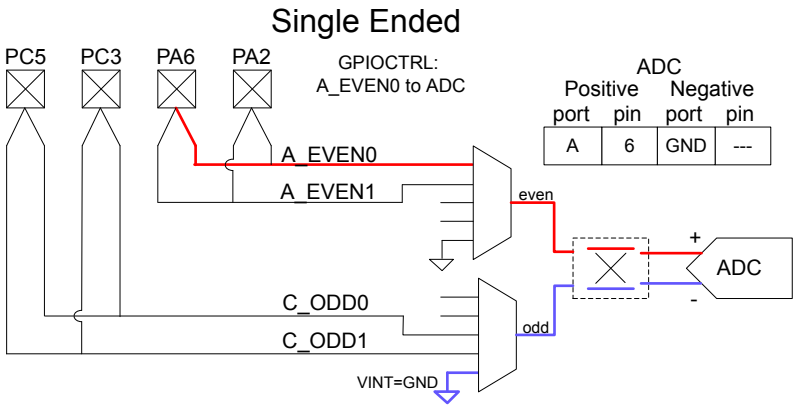


Figure 23.11. Single-Ended Port/Pin Selection Even Channel

Figure 23.12 Single-Ended Port/Pin Selection Polarity Error on page 744 shows an example where the PORTPOS input has been configured to GND, with PORTNEG and PINNEG configured for a GPIO pin. This will result in a polarity error (POLARITYERRIF in IADC_IF will be set) and any conversion result will be 0.

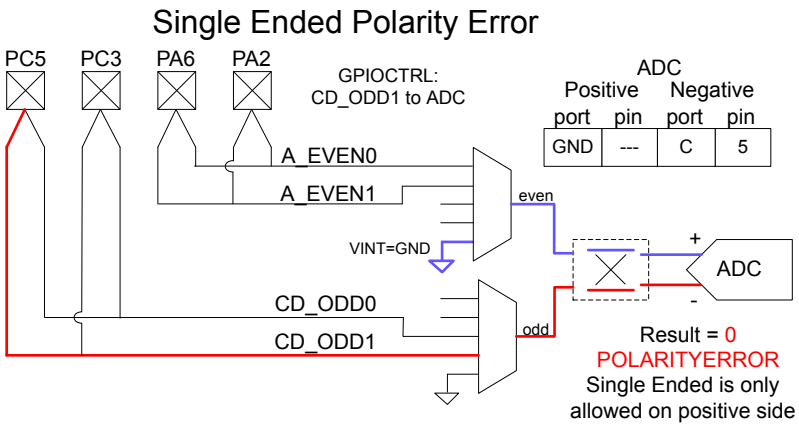


Figure 23.12. Single-Ended Port/Pin Selection Polarity Error

Correct configuration examples for differential conversions are shown in Figure 23.13 Differential Port/Pin Selection without Swap on page 744 and Figure 23.14 Differential Port/Pin Selection with Swap on page 745. In both these examples, the inputs were selected from one EVEN multiplexer channel and one ODD multiplexer channel. As with single-ended mode, the IADC logic will automatically swap the multiplexer connections to the IADC input if needed.

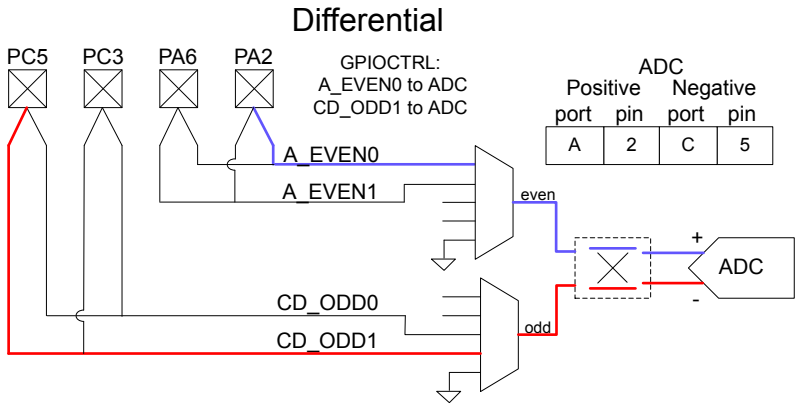


Figure 23.13. Differential Port/Pin Selection without Swap

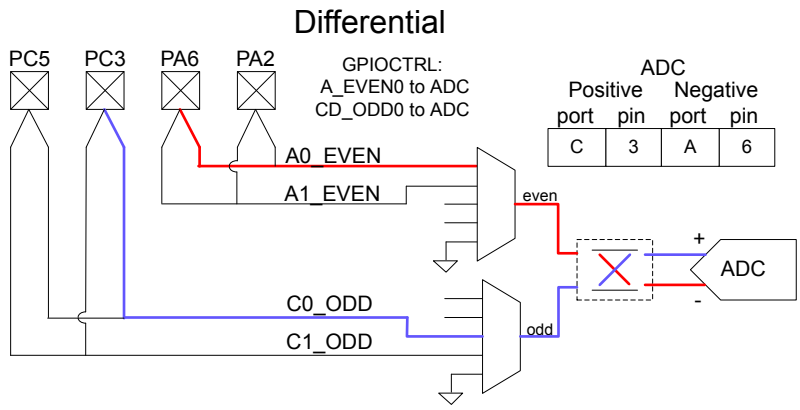


Figure 23.14. Differential Port/Pin Selection with Swap

Figure 23.15 Differential Port/Pin Selection Polarity Error on page 745 shows an example where the both the positive and the negative input selections point to ODD buses. Even though the IADC has been allocated both buses, they both route through the ODD input multiplexer and cannot be measured against one another. This will result in a polarity error (POLARITYERRIF in IADC_IF will be set) and any conversion result will be 0x7FFFF. Likewise, a polarity error will occur if both inputs are selected from EVEN buses.

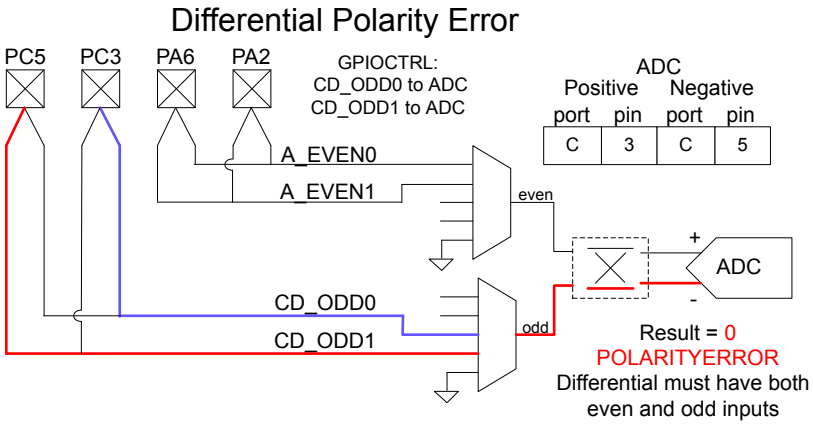


Figure 23.15. Differential Port/Pin Selection Polarity Error

23.3.5.4 Scan Queue

The scan queue allows the IADC to automatically convert up to 16 channels in sequence without CPU intervention. Input and configuration selection for each channel in the scan table is specified by the IADC_SCANx register for that channel (channel 0 is configured with IADC_SCAN0, channel 1 is configured with IADC_SCAN1, and so on). The IADC_MASKREQ register allows software to define which of the scan table entries (IADC_SCANx) to convert during a scan. For example, channels 0, 1, and 7 can be enabled by writing bits 0, 1, and 7 of IADC_MASKREQ to 1 (IADC_MASKREQ = 0x0083).

The IADC_SCANx registers must be configured when the IADC module is disabled (IADC_EN_EN = 0). IADC_MASKREQ can be written while IADC_EN_EN is set to 1. If a scan operation is in progress, MASKREQ will be synchronized and held until the current scan operation has completed. Then MASKREQ is copied into the STMASK register for the next scan operation. IADC_STMASK is the working copy of the MASKREQ used by the IADC during a scan. MASKREQ will only transfer to STMASK when the scan queue is not scanning and converting the scan table. IADC_STATUS_MASKWRITEPENDING can be used by software to see when the MASKREQ write has been transferred to STMASK. Writing a new MASKREQ in the middle of a scan will not corrupt the current scan. Software which writes to MASKREQ during a scan operation must ensure IADC_STATUS_MASKWRITEPENDING returns to 0 before updating IADC_MASKREQ again. Figure 23.16 MASKREQ Updates on page 746 shows a time line of when the MASKREQ write is updated.

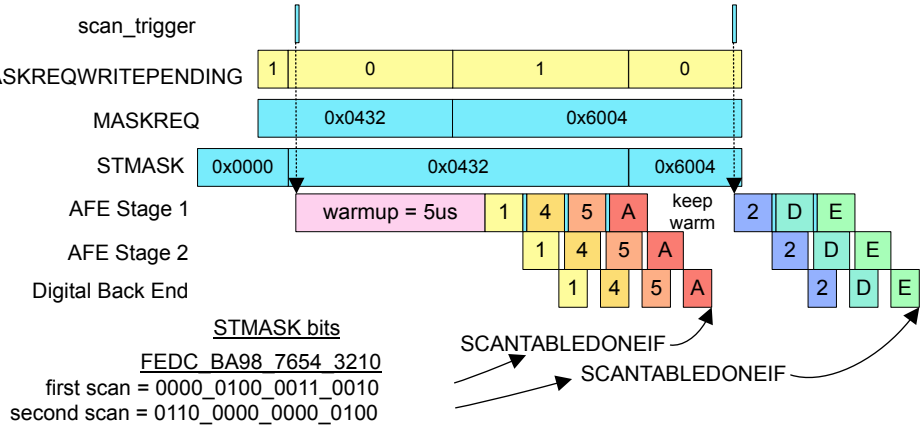


Figure 23.16. MASKREQ Updates

23.3.6 Gain and Offset Correction

The IADC has built in gain and offset correction capabilities. Each of the two configuration groups contains its own correction values stored in the IADC_SCALEx register, allowing the IADC to automatically apply the appropriate correction for the IADC configuration that is being used.

Gain correction is performed through a fixed-point 16-bit value with a range from 0.75x to 1.2499x. The 3 MSBs of the gain value are not directly writeable. The GAIN3MSB bit in IADC_SCALEx is used to select between 011 and 100 for the 3 MSBs, and the lower 13 bits are programmed directly into IADC_SCALEx_GAIN13LSB. Clearing GAIN3MSB to 0 selects the most significant bits of the gain as 011, representing a range from 0.75x to 0.9999x. Setting GAIN3MSB to 1 selects the most significant bits of the gain as 100, representing a range from 1.00x to 1.2499x.

Offset correction is controlled by the OFFSET field in IADC_SCALEx. It is important to note that the offset correction does not have a direct 1-to-1 relationship with the LSB of the IADC output, and depends on both the OSR and gain correction settings. The offset correction range is +/- 12.5% of full scale. OFFSET is encoded as a 2's complement, 18-bit number with the LSB representing $1 / 2^{20}$ of full scale. Thus, bit 8 of OFFSET aligns with bit 0 of the 12-bit IADC output word.

23.3.6.1 Using Production Calibration Parameters

IADC calibration is performed on every device during Silicon Labs production test and production calibration parameters are stored in the flash DI page. The production calibration values are useful for a wide variety of possible IADC configurations, but do not map directly to the offset and gain correction fields in the IADC_SCALEx registers. Software must calculate the actual offset and gain correction values from the factory calibration values.

23.3.6.1.1 Gain Correction

The IADC gain error is designed to be minimal with the digital gain correction set to 1.0 (GAIN3MSB = 1 and GAIN13LSB = 0). Tighter gain error is achieved by adjusting these values in IADC_SCALEx. Using this gain correction mechanism will result in a slight increase to the DNL of the converter, which is reduced by higher OSR settings.

Gain error is measured during production test at various settings of ANALOGGAIN, and stored in the DEVINFO_IADC0GAIN0 and DEVINFO_IADC0GAIN1 locations. The GAINCANA1 field is used for 0.5x and 1x ANALOGGAIN settings, while GAINCANA2, GAINCANA3, and GANCANA4 are used for ANALOGGAIN settings of 2x, 3x, and 4x, respectively.

The GAINCANAn values are expressed as the full 16-bit fixed-point gain, and must be compressed before writing to the IADC_SCALEx register.

To apply a factory-calibrated gain:

1. Read the appropriate GAINCANAn field from the DEVINFO locations for the selected ANALOGGAIN.
2. Write the MSB (bit 15) of GAINCANAn to GAIN3MSB in IADC_SCALEx.
3. Write the 13 LSBs (bits 12-0) of GAINCANAn to GAIN13LSB in IADC_SCALEx.

23.3.6.1.2 Offset Correction

Offset is impacted by the selected ANALOGGAIN and OSR settings in IADC_CFGx, the GAIN3MSB and GAIN13LSB values in IADC_SCALEx, and the voltage reference. Offset is production calibrated for any combination of possibilities, but the OFFSET register value must be calculated for the given situation before it can be effectively used.

The production offset calibration consists of four 16-bit terms written to the DEVINFO space: OFFSETANA1NORM, OFFSETANA2NORM, OFFSETANA3NORM, and OFFSETANABASE. The following procedures will determine the setting for the OFFSET register based on production calibration values.

Step 1: Determine the offset gain adjustment term (off_gain) based on ANALOGGAIN.

For ANALOGGAIN set to 0.5x or 1x:

off_gain = 0

For ANALOGGAIN set to 2x, 3x, or 4x, off_gain is calculated as:

off_gain = OFFSETANA2NORM * (gain - 1)

The following table summarizes these equations:

Table 23.4. Offset Gain Adjustment

ANALOGGAIN Setting	Analog front-end gain	Offset Gain Adjustment Term (off_gain)
ANAGAIN0P5	0.5 x	0
ANAGAIN1	1 x	0
ANAGAIN2	2 x	OFFSETANA2NORM * 1
ANAGAIN3	3 x	OFFSETANA2NORM * 2
ANAGAIN4	4 x	OFFSETANA2NORM * 3

Step 2: Calculate the analog offset adjustment term (off_ana) based on OSR and off_gain.

For an OSR of 2x (OSRHS = 0):

off_ana = OFFSETANA1NORM + off_gain

For all other OSR settings, 4x - 64x:

off_ana = OFFSETANABASE + 2*(OFFSETANA3NORM - off_gain)/OSR

The following table expresses these equations:

Table 23.5. Analog Offset Adjustment

OSRHS Setting	OSR	Analog Offset Adjustment Term (off_ana)
HISPD2	2 x	OFFSETANA1NORM + off_gain
HISPD4	4 x	OFFSETANABASE + (OFFSETANA3NORM - off_gain)/2
HISPD8	8 x	OFFSETANABASE + (OFFSETANA3NORM - off_gain)/4
HISPD16	16 x	OFFSETANABASE + (OFFSETANA3NORM - off_gain)/8
HISPD32	32 x	OFFSETANABASE + (OFFSETANA3NORM - off_gain)/16
HISPD64	64 x	OFFSETANABASE + (OFFSETANA3NORM - off_gain)/32

Step 3: Compensate for reference voltage differences.

The off_ana term represents the offset at the input of the ADC, meaning that the reference voltage will have an impact on the magnitude of the offset at the output. Production calibration values are determined with a 1.25 V reference source. If a voltage significantly different than 1.25 V is used for V_{REF}, adjust the off_ana term by a factor of 1.25 / V_{REF}.

off_ana = off_ana * (1.25 / V_{REF})

Step 4: Calculate total offset by adding the analog offset to the systematic offset.

Systematic offset is a fixed number dependent on OSR, and calculated according to the following equation:

off_sys = 640*(256/OSR)

Total uncorrected offset (off_tot) is calculated by:

off_tot = (off_ana * 4 + off_sys)

Step 5: Apply gain error correction, if needed.

Before writing the OFFSET field, the total uncorrected offset must be multiplied by the gain calibration factor. If the gain calibration factor is equal to 1.0 (0x8000 in 16-bit hex, or GAIN3MSB = 1 and GAIN13LSB = 0), this step may be skipped. Otherwise, adjust off_tot according to the following equation:

off_tot = GAIN_FACTOR * (off_tot + 0x80000) - 0x80000

where GAIN_FACTOR = GAINCANAn / 32768.

Step 6: Write the offset correction value to the OFFSET field.

The OFFSET field holds an 18-bit 2's complement number, which should be the negation of the total offset, or -(off_tot). Before writing to the SCALE register, any leading sign bits should be masked off to avoid corrupting the programmed gain settings.

OFFSET = 0x3FFFF & (-off_tot)

23.3.6.2 Calibration

Calibration can be performed in-system to correct for external errors and provide more accurate measurements. The general calibration procedure is as follows:

1. Configure the ADC to the desired mode, OSR, analog gain settings, reference source, etc.
2. Force the IADC to use bipolar output for the conversion: IADC_CFGx_TWOSCOMPL = FORCEBIPOLAR.
3. Set the initial offset to the maximum negative value (IADC_SCALEx_OFFSET = 0x20000), and the initial gain to 1.0 (GAIN3MSB = 1, GAIN13LSB = 0x0000). This will prevent output saturation when measuring full scale.
4. Apply a full-scale positive input to the IADC and perform a conversion (*result_fullscale*). Multiple conversions can be performed and averaged together to reduce any system-level noise.
5. Apply a zero input to the IADC and perform a conversion (*result_zero*). Multiple conversions can be performed and averaged together to reduce any system-level noise.
6. Calculate the gain correction factor: Divide the expected value by the difference in the measured values (*result_fullscale* - *result_zero*). Note that the offset adjustment in Step 3 will be canceled out by this calculation.
7. Write the gain correction factor to the IADC using the GAIN3MSB and GAIN13LSB fields in IADC_SCALEx.
8. Set IADC_SCALEx_OFFSET to 0x00000 in preparation for the offset calibration.
9. Apply the desired zero voltage to the IADC input and perform a conversion (*result_offset*). Multiple conversions can be performed and averaged together to reduce any system-level noise.
10. Multiply *result_offset* to convert to a 20-bit value (*result_offset_20*). For example, a 12-bit result should be multiplied by 256.
11. Negate *result_offset_20* and write the value to IADC_SCALEx_OFFSET.

    Note that the IADC_SCALEx_OFFSET field is 18 bits. If the result is greater than (2^{17} - 1) or less than (-2^{17}), the offset is too large to be corrected.

23.3.7 Output Data FIFOs

The single and scan queues each have a eight-word data FIFO. Conversions results are written to the output data FIFO associated with the queue. Single queue results are written to the single FIFO and scan queue results are written to the scan data FIFO. The two queues are identical in operation, but independent.

Conversion results are read from the single FIFO using IADC_SINGLEFIFODATA. Reading SINGLEFIFODATA will pop the oldest result from the FIFO. It is also possible to read the most recent valid data word using IADC_SINGLEDATA. Reading SINGLEDATA does not pop a conversion from the FIFO. Similarly, the scan FIFO results are read with IADC_SCANFIFODATA, which reads the oldest result and pops the FIFO. The most recent scan result can be read using IADC_SCANDATA.

When the single FIFO has valid data, the SINGLEFIFODV flag in IADC_STATUS is set to 1. When the scan FIFO has valid data SCANFIFODV in IADC_STATUS is set to 1. These data valid status bits are cleared automatically whenever the associated FIFO is empty. For more granular FIFO status, the number of data words present in the FIFO is indicated in IADC_SINGLEFIFOSTAT (for single FIFO) or IADC_SCANFIFOSTAT (for scan FIFO).

A programmable data level watermark is also available for the FIFOs, allowing hardware to trigger interrupts or DMA operations when a specified number of conversion results are available. The DVL field in register SINGLEFIFOCFG or SCANFIFOCFG sets the watermark level, between 1 and 4 conversions. If the number of valid entries in the FIFO reaches or exceeds the level set in DVL, the SINGLEFIFODVLIF (for single FIFO) or SCANFIFODVLIF (for scan FIFO) flag in the IADC_IF register will be set to 1. If enabled, an interrupt or DMA request will be triggered when the flag is set.

By default, DMA requests are turned off for operation in EM2 or EM3. However, the DMAWUFIFOSINGLE or DMAWUFIFOSCAN bits in SINGLEFIFOCFG or SCANFIFOCFG may be used to enable DMA operations in these lower energy modes.

Overflow and underflow status flags are also available in IADC_IF. An overflow condition occurs when an IADC conversion completes, but the associated FIFO is already full. In an overflow case the SINGLEFIFOOFIF or SCANFIFOOFIF flag will be set. The most recent conversion will still be available in the SINGLEDATA or SCANDATA register, but the FIFO will not be updated with the new data. An underflow condition occurs when software or hardware attempts to read from an empty FIFO. In an underflow case the SINGLEFIFOUFIF or SCANFIFOUFIF flag will be set.

23.3.7.1 Data Alignment and Channel ID

The IADC has data alignment options and the ability to include a channel ID along with the conversion data. For the single queue, alignment and channel ID are configured in the IADC_SINGLEFIFOCFG register. For the scan queue, alignment and channel ID are configured in the IADC_SCANFIFOCFG register.

The ALIGNMENT bit field specifies the data justification and the number of data bits as shown in Figure 23.17 Data Alignment on page 751. By default, the converter will produce 12-bit right-justified data, corresponding to ALIGNMENT = RIGHT12.

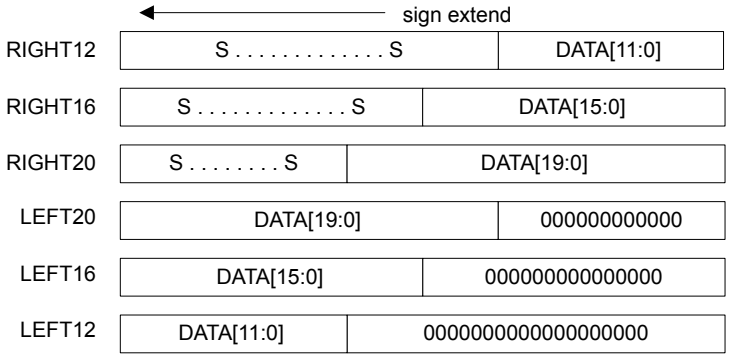


Figure 23.17. Data Alignment

The SHOWID bit controls whether the conversion channel ID is included in the output data word. This option is primarily used with the scan FIFO to help software determine which channel each conversion result came from. If SHOWID is enabled for single conversions, the ID will always be set to 0x20. Figure 23.18 Data Alignment With ID on page 751 shows output data formatting including the ID, when SHOWID = 1.

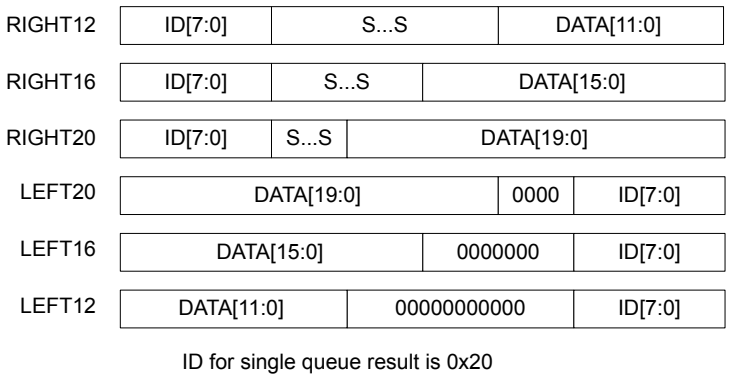


Figure 23.18. Data Alignment With ID

23.3.7.2 Output Polarity

The output polarity of the IADC is controlled by the TWOSCOMPL field in the IADC_CFGx register. The IADC supports unipolar and bipolar output formatting independent of the input configuration. By default, the TWOSCOMPL field is set to AUTO, meaning that single-ended conversions will produce unipolar output, and differential conversions will produce bipolar output. The polarity can be forced to unipolar or bipolar mode by setting TWOSCOMPL to FORCEUNIPOLAR or FORCEBIPOLAR, respectively.

Unipolar samples are unsigned integers representing zero to positive full-scale. Bipolar samples are two's-complement signed integers, representing negative full-scale to positive full-scale. Using unipolar mode on a differential input signal allows for more dynamic range when the signal is positive, but will saturate to zero when the signal is negative.

Note: If bipolar output is used with a single-ended input configuration, it is possible to see negative output values when the input is close to ground. However, the input voltage is still limited by the supply range of the device.

23.3.7.3 Digital Accumulation and Averaging

The IADC may optionally accumulate and average several conversion results before posting an output word to the FIFO. Digital averaging is controlled by the DIGAVG field in the IADC_CFGx register. It can be configured to average 1, 2, 4, 8, or 16 samples. The IADC will collect the number of samples specified by DIGAVG on the selected channel slot back-to-back, and produce only one averaged output word.

23.3.7.4 Output Resolution

The usable output resolution of the IADC is a minimum of 12 bits, when the oversampling ratio is set to 2 and no digital averaging is used (DIGAVG = AVG1). An extra bit of output resolution is produced for every power of 2 increase in either of these settings. In other words, the output resolution of the ADC can be determined as:

$$\text{Output Resolution} = 11 + \log_2(\text{OversamplingRatio} \times \text{DigitalAveraging})$$

The MSB is always left-aligned within the DATA field, and the output word will be truncated to 12, 16, or 20 bits, as shown in Figure 23.17 Data Alignment on page 751 and Figure 23.18 Data Alignment With ID on page 751. When using 16 or 20 bit alignment with lower oversampling ratio and digital averaging settings, LSBs of the output can contain residual effects of the offset and gain computation. These residual effects do not represent additional information about the input signal. Any extra LSBs can be masked to 0 by software.

Table 23.6. Output Resolution Masking Examples

Alignment Setting	Oversampling Ratio	Digital Averaging	Number of averaged samples	Output Resolution	Recommended Mask for DATA field
16-bit	2x	1x	2	12 bits	0xFFF0
16-bit	8x	2x	16	15 bits	0xFFFE
20-bit	2x	1x	2	12 bits	0xFFF00
20-bit	16x	4x	64	17 bits	0xFFFF8

23.3.7.5 Flushing the FIFOs

Each FIFO has a command bit in the IADC_CMD register that can be used to trigger a FIFO flush. The FIFO data may be flushed independently for each queue. To flush a FIFO:

1. The IADC must be enabled with the clock running.
2. Disable the queue associated with the FIFO using the SCANSTOP or SINGLESTOP bits in the IADC_CMD register.
3. Ensure the queue is disabled by reading the associated flag in the IADC_STATUS register (SINGLEQEN or SCANQEN).
4. Set the command bit to flush the desired FIFO (SINGLEFIFOFLUSH or SCANFIFOFLUSH) in the IADC_CMD register.
5. Wait for the corresponding status bit (SINGLEFIFOFLUSHING or SCANFIFOFLUSHING) in IADC_STATUS to go low.

23.3.8 Window Compare

The IADC has a window comparison unit that can trigger interrupts conditional on the output data of the converter. The window comparison unit has two thresholds - greater than or equal (ADGT), and less than or equal (ADLT), which are programmable through the IADC_CMPTHR register. The ADGT and ADLT thresholds always use a 16 bit, left-justified format, regardless of the format specified by the FIFO. The 12-bit conversion result will be compared against the upper 12 bits of the window comparator.

The window comparison unit is active on the ADC output on a conversion-by-conversion basis, and is shared between the two FIFOs. It is not possible to set different window comparison thresholds for different channels or for each FIFO. However, each channel specified in the IADC has a CMP bit field to enable the window comparison on results from that channel. For example, it is possible to only apply the window comparison and associated interrupt to scan channel #3 by setting the CMP field in IADC_SCAN3 to 1. When the CMP field associated with a channel is 0, the window comparator will not be active for results from that channel.

The window comparator supports conditional triggering on output results which are inside or outside a specified window. When ADLT is greater than or equal to ADGT, the comparator will trigger on an "inside" condition, or when DATA <= ADLT **and** DATA >= GT. When ADLT is less than ADGT, the comparator will trigger on an "outside" condition, or when DATA <= ADLT **or** DATA >= GT.

Figure 23.19 Window Comparison Examples on page 753 shows different configurations of the ADLT and ADGT values and the resulting windows. When the window comparator detects that the appropriate conditions are met (shown by the shaded region in the figure), it will generate an interrupt via the SINGLECMPIF flag for conversions on the single queue, or via the SCANCMPIF flag for conversions on the scan queue.

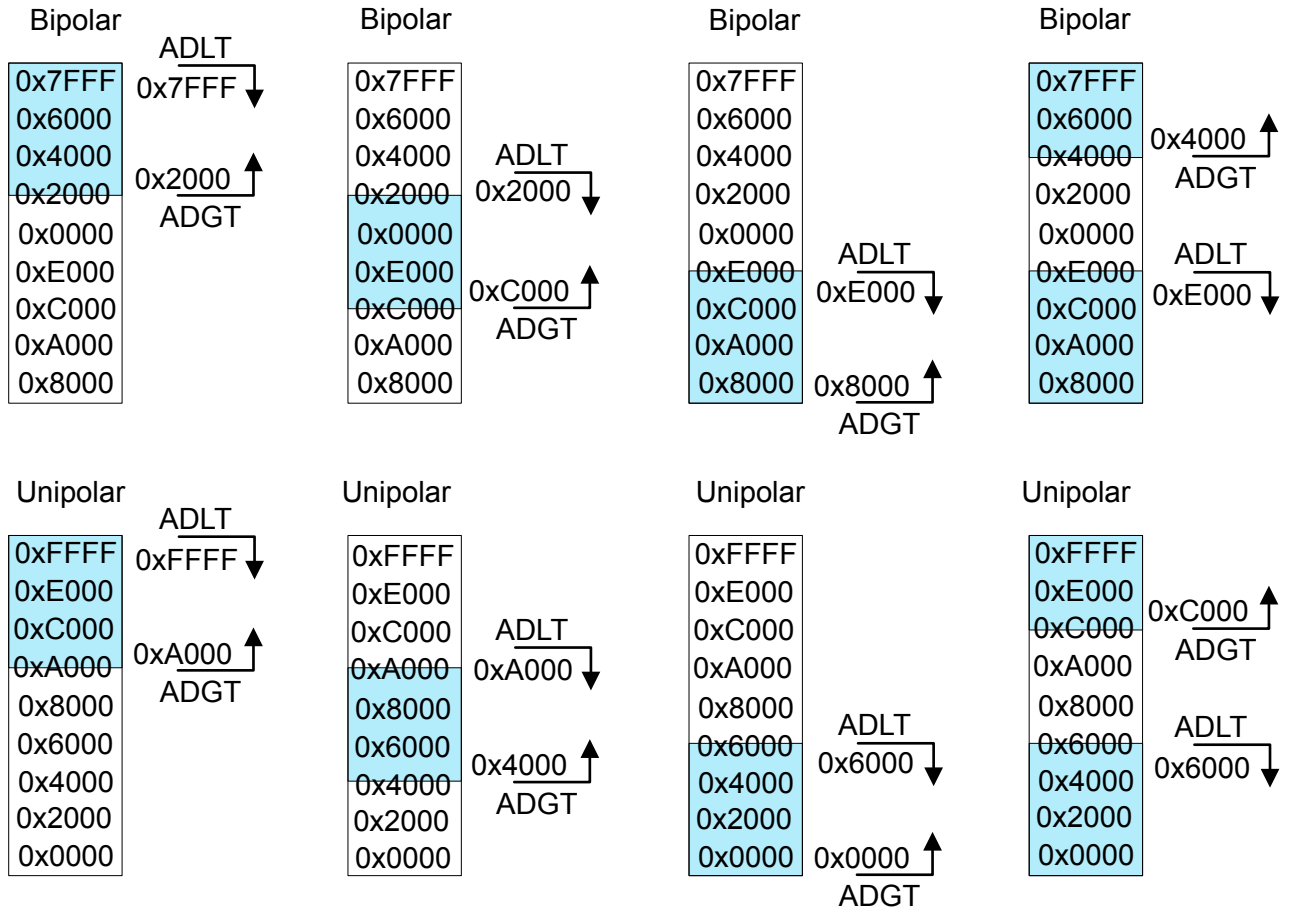


Figure 23.19. Window Comparison Examples

23.3.9 Interrupts

Interrupts are enabled in the IADC_IEN register, allowing interrupts to be generated on several different IADC conditions. Each of the flags in IADC_IF has a corresponding enable bit in the IADC_IEN register. A brief overview of the available interrupt sources is shown in the list below; more details can be found in the relevant sections of this chapter.

- SINGLEFIFODVLIF - The single FIFO watermark specified in SINGLEFIFOCFG_DVL has been reached or exceeded.
- SCANFIFODVLIF - The scan FIFO watermark specified in SCANFIFOCFG_DVL has been reached or exceeded.
- SINGLECMPIF - A conversion result from the single queue tripped the window comparator.
- SCANCMPIF - A conversion result from the scan queue tripped the window comparator.
- SCANENTRYDONEIF - A scan queue conversion has completed.
- SCANTABLEDONEIF - A scan queue operation has completed (all channels specified in the scan mask have been converted once).
- POLARITYERRIF - A channel polarity selection error has occurred (two channels from the EVEN multiplexer or two channels from the ODD multiplexer were selected for positive and negative inputs).
- PORTALLOCERRIF - A port allocation error has occurred (a pin not allocated to the IADC in the GPIO bus allocation registers was requested).
- SINGLEFIFOOFIF - A single FIFO overflow has occurred.
- SCANFIFOOFIF - A scan FIFO overflow has occurred.
- SINGLEFIFOUFIF - A single FIFO underflow has occurred.
- SCANFIFOUFIF - A scan FIFO underflow has occurred.
- EM23ABORTERRORIF - The system entered EM2 or EM3 while the IADC was converting and using a clock not supported in EM2 or EM3.

Hardware sets the interrupt flags in IADC_IF, and the flags remain set (sticky) until cleared by software. The interrupts flags should be cleared before enabling the IADC to remove any previous interrupt history. Clearing or setting interrupt bits can be done by writing to IADC_IF with a set or clear mask.

23.4 IADC Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	IADC_IPVERSION	R	IPVERSION
0x004	IADC_EN	RW ENABLE	Enable
0x008	IADC_CTRL	RW CONFIG	Control
0x00C	IADC_CMD	W SYNC	Command
0x010	IADC_TIMER	RW CONFIG	Timer
0x014	IADC_STATUS	RH	Status
0x018	IADC_MASKREQ	RW SYNC	Mask Request
0x01C	IADC_STMASK	RH SYNC	Scan Table Mask
0x020	IADC_CMPTHR	RW CONFIG	Digital Window Comparator Threshold
0x024	IADC_IF	RWH INTFLAG	Interrupt Flags
0x028	IADC_IEN	RW	Interrupt Enable
0x02C	IADC_TRIGGER	RW CONFIG	Trigger
0x048	IADC_CFGx	RW CONFIG	Configuration
0x050	IADC_SCALEx	RW CONFIG	Scaling
0x054	IADC_SCHEDx	RW CONFIG	Scheduling
0x070	IADC_SINGLEFIFOCFG	RW CONFIG	Single FIFO Configuration
0x074	IADC_SINGLEFIFODATA	RH(r)	Single FIFO DATA
0x078	IADC_SINGLEFIFOSTAT	RH	Single FIFO Status
0x07C	IADC_SINGLEDATA	RH SYNC	Single Data
0x080	IADC_SCANFIFOCFG	RW CONFIG	Scan FIFO Configuration
0x084	IADC_SCANFIFODATA	RH(r)	Scan FIFO Read Data
0x088	IADC_SCANFIFOSTAT	RH	Scan FIFO Status
0x08C	IADC_SCANDATA	RH SYNC	Scan Data
0x098	IADC_SINGLE	RW SYNC	Single Queue Port Selection
0x0A0	IADC_SCANx	RW CONFIG	SCAN Entry
0x1000	IADC_IPVERSION_SET	R	IPVERSION
0x1004	IADC_EN_SET	RW ENABLE	Enable
0x1008	IADC_CTRL_SET	RW CONFIG	Control
0x100C	IADC_CMD_SET	W SYNC	Command
0x1010	IADC_TIMER_SET	RW CONFIG	Timer
0x1014	IADC_STATUS_SET	RH	Status
0x1018	IADC_MASKREQ_SET	RW SYNC	Mask Request
0x101C	IADC_STMASK_SET	RH SYNC	Scan Table Mask
0x1020	IADC_CMPTHR_SET	RW CONFIG	Digital Window Comparator Threshold
0x1024	IADC_IF_SET	RWH INTFLAG	Interrupt Flags

Offset	Name	Type	Description
0x1028	IADC_IEN_SET	RW	Interrupt Enable
0x102C	IADC_TRIGGER_SET	RW CONFIG	Trigger
0x1048	IADC_CFGx_SET	RW CONFIG	Configuration
0x1050	IADC_SCALEx_SET	RW CONFIG	Scaling
0x1054	IADC_SCHEDx_SET	RW CONFIG	Scheduling
0x1070	IADC_SINGLEFIFOCFG_SET	RW CONFIG	Single FIFO Configuration
0x1074	IADC_SINGLEFIFODATA_SET	RH(r)	Single FIFO DATA
0x1078	IADC_SINGLEFIFOSTAT_SET	RH	Single FIFO Status
0x107C	IADC_SINGLEDATA_SET	RH SYNC	Single Data
0x1080	IADC_SCANFIFOCFG_SET	RW CONFIG	Scan FIFO Configuration
0x1084	IADC_SCANFIFODATA_SET	RH(r)	Scan FIFO Read Data
0x1088	IADC_SCANFIFOSTAT_SET	RH	Scan FIFO Status
0x108C	IADC_SCANDATA_SET	RH SYNC	Scan Data
0x1098	IADC_SINGLE_SET	RW SYNC	Single Queue Port Selection
0x10A0	IADC_SCANx_SET	RW CONFIG	SCAN Entry
0x2000	IADC_IPVERSION_CLR	R	IPVERSION
0x2004	IADC_EN_CLR	RW ENABLE	Enable
0x2008	IADC_CTRL_CLR	RW CONFIG	Control
0x200C	IADC_CMD_CLR	W SYNC	Command
0x2010	IADC_TIMER_CLR	RW CONFIG	Timer
0x2014	IADC_STATUS_CLR	RH	Status
0x2018	IADC_MASKREQ_CLR	RW SYNC	Mask Request
0x201C	IADC_STMASK_CLR	RH SYNC	Scan Table Mask
0x2020	IADC_CMPTHR_CLR	RW CONFIG	Digital Window Comparator Threshold
0x2024	IADC_IF_CLR	RWH INTFLAG	Interrupt Flags
0x2028	IADC_IEN_CLR	RW	Interrupt Enable
0x202C	IADC_TRIGGER_CLR	RW CONFIG	Trigger
0x2048	IADC_CFGx_CLR	RW CONFIG	Configuration
0x2050	IADC_SCALEx_CLR	RW CONFIG	Scaling
0x2054	IADC_SCHEDx_CLR	RW CONFIG	Scheduling
0x2070	IADC_SINGLEFIFOCFG_CLR	RW CONFIG	Single FIFO Configuration
0x2074	IADC_SINGLEFIFODATA_CLR	RH(r)	Single FIFO DATA
0x2078	IADC_SINGLEFIFOSTAT_CLR	RH	Single FIFO Status
0x207C	IADC_SINGLEDATA_CLR	RH SYNC	Single Data
0x2080	IADC_SCANFIFOCFG_CLR	RW CONFIG	Scan FIFO Configuration
0x2084	IADC_SCANFIFODATA_CLR	RH(r)	Scan FIFO Read Data
0x2088	IADC_SCANFIFOSTAT_CLR	RH	Scan FIFO Status

Offset	Name	Type	Description
0x208C	IADC_SCANDATA_CLR	RH SYNC	Scan Data
0x2098	IADC_SINGLE_CLR	RW SYNC	Single Queue Port Selection
0x20A0	IADC_SCANx_CLR	RW CONFIG	SCAN Entry
0x3000	IADC_IPVERSION_TGL	R	IPVERSION
0x3004	IADC_EN_TGL	RW ENABLE	Enable
0x3008	IADC_CTRL_TGL	RW CONFIG	Control
0x300C	IADC_CMD_TGL	W SYNC	Command
0x3010	IADC_TIMER_TGL	RW CONFIG	Timer
0x3014	IADC_STATUS_TGL	RH	Status
0x3018	IADC_MASKREQ_TGL	RW SYNC	Mask Request
0x301C	IADC_STMASK_TGL	RH SYNC	Scan Table Mask
0x3020	IADC_CMPTHR_TGL	RW CONFIG	Digital Window Comparator Threshold
0x3024	IADC_IF_TGL	RWH INTFLAG	Interrupt Flags
0x3028	IADC_IEN_TGL	RW	Interrupt Enable
0x302C	IADC_TRIGGER_TGL	RW CONFIG	Trigger
0x3048	IADC_CFGx_TGL	RW CONFIG	Configuration
0x3050	IADC_SCALEx_TGL	RW CONFIG	Scaling
0x3054	IADC_SCHEDx_TGL	RW CONFIG	Scheduling
0x3070	IADC_SINGLEFIFOCFG_TGL	RW CONFIG	Single FIFO Configuration
0x3074	IADC_SINGLEFIFODATA_TGL	RH(r)	Single FIFO DATA
0x3078	IADC_SINGLEFIFOSTAT_TGL	RH	Single FIFO Status
0x307C	IADC_SINGLEDATA_TGL	RH SYNC	Single Data
0x3080	IADC_SCANFIFOCFG_TGL	RW CONFIG	Scan FIFO Configuration
0x3084	IADC_SCANFIFODATA_TGL	RH(r)	Scan FIFO Read Data
0x3088	IADC_SCANFIFOSTAT_TGL	RH	Scan FIFO Status
0x308C	IADC_SCANDATA_TGL	RH SYNC	Scan Data
0x3098	IADC_SINGLE_TGL	RW SYNC	Single Queue Port Selection
0x30A0	IADC_SCANx_TGL	RW CONFIG	SCAN Entry

23.5 IADC Register Description

23.5.1 IADC_IPVERSION - IPVERSION

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x3																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x3	R	**IP version ID**
	The read only IPVERSION field gives the version for this module. There may be minor software changes required for modules with different values of IPVERSION.			

23.5.2 IADC_EN - Enable

Offset	Bit Position																															
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	RW
Name																															DISABLING	EN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DISABLING	0x0	R	**Disablement busy status**
	When EN is cleared, DISABLING status is set immediately, and cleared when disablement finishes. Disablement resets peripheral cores and not APB registers except hardware updated registers such as INTFLAGS and FIFOs.			
0	EN	0x0	RW	**Enable IADC Module**
	The EN bit enables the module. Software should write to CONFIG type registers before setting the EN bit. Software should write to SYNC type registers only after setting the EN bit.			

Value	Mode	Description
0	DISABLE	Disable
1	ENABLE	Enable

23.5.3 IADC_CTRL - Control

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset		0x0								0x0																	0x0		0x0	0x0	0x0	0x0
Access		RW								RW																	RW		RW	RW	RW	RW
Name		HSCLKRATE								TIMEBASE																	WARMUPMODE		DBGHALT	ADCCLKSUSPEND1	ADCCLKSUSPEND0	EM23WUCONVERT

Bit	Name	Reset	Access	Description
31	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
30:28	HSCLKRATE	0x0	RW	**High Speed Clock Rate**

Ratio to divide incoming CLK_CMU_ADC clock by. The resulting clock (CLK_SRC_ADC) must be 40 MHz or less.

Value	Mode	Description
0	DIV1	Use CMU_CLK_ADC directly. The source clock must be 40 MHz or less.
1	DIV2	Divide CMU_CLK_ADC by 2 before using it. The resulting CLK_SRC_ADC must be 40 MHz or less.
2	DIV3	Divide CMU_CLK_ADC by 3 before using it. The resulting CLK_SRC_ADC must be 40 MHz or less.
3	DIV4	Divide CMU_CLK_ADC by 4 before using it. The resulting CLK_SRC_ADC must be 40 MHz or less.

27:23	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
22:16	TIMEBASE	0x0	RW	**Time Base**

ADC clock cycles (TIMEBASE + 1) needed to generate a 1 us interval for warm up and start up timing. Does not allow less than 2 cycles. A setting of 0x0 (1 cycle) is replaced with 0x1 (2 cycles).

15:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:4	WARMUPMODE	0x0	RW	**Warmup Mode**

Select the warmup mode for the ADC.

Value	Mode	Description
0	NORMAL	Shut down the IADC after conversions have completed.
1	KEEPINSTANDBY	Switch to standby mode after conversions have completed. The next warmup time will require 1us.
2	KEEPWARM	Keep IADC fully powered after conversions have completed.

3	DBGHALT	0x0	RW	**Debug Halt**

Bit	Name	Reset	Access	Description
	ADC behavior when halted by debugger.			

Value	Mode	Description
0	NORMAL	Continue operation as normal during debug mode
1	HALT	Complete the current conversion and then halt during debug mode

Bit	Name	Reset	Access	Description
2	ADCCLKSUSPEND1	0x0	RW	**ADC_CLK Suspend - PRS1**
	This only functions with single trigger select set to PRSPOS or PRSNEG. In EM0 and EM1, this gates the local clock while clock source remains running. In EM2 and EM3, this disables the clock source until the PRSPOS or PRSNEG event is detected. This bit has no effect if the local IADC timer is running.			

Value	Mode	Description
0	PRSWUDIS	Normal mode which does not disable the ADC_CLK.
1	PRSWUEN	ADCCLKWUEN will gate off ADC_CLK until the trigger is detected provided the internal timer is not selected as the trigger. Once the trigger is detected the ADC_CLK will be started, the band gap will be started, the ADC will be warmed up, and the SCAN Table and the Single entry will be converted. Once the conversions are done, the ADC_CLK will be gated off.

Bit	Name	Reset	Access	Description
1	ADCCLKSUSPEND0	0x0	RW	**ADC_CLK Suspend - PRS0**
	This only functions with scan trigger select set to PRSPOS or PRSNEG. In EM0 and EM1, this gates the local clock while clock source remains running. In EM2 and EM3, this disables the clock source until the PRSPOS or PRSNEG event is detected. This bit has no effect if the local IADC timer is running.			

Value	Mode	Description
0	PRSWUDIS	Normal mode which does not disable the ADC_CLK.
1	PRSWUEN	ADCCLKWUEN will gate off ADC_CLK until the trigger is detected provided the internal timer is not selected as the trigger. Once the trigger is detected the ADC_CLK will be started, the band gap will be started, the ADC will be warmed up, and the SCAN Table and the Single entry will be converted. Once the conversions are done, the ADC_CLK will be gated off.

Bit	Name	Reset	Access	Description
0	EM23WUCONVERT	0x0	RW	**EM23 Wakeup on Conversion**
	EM23 wake up on conversion			

Value	Mode	Description
0	WUDVL	When using suspend mode, conversions performed in EM2 or EM3 should not wake up the DMA until the FIFO's DVL setting is reached. This saves more power for large OSR settings or infrequent sampling.
1	WUCONVERT	When using suspend mode, conversions performed in EM2 or EM3 will wake up the DMA and keep it awake until the conversions are done, regardless of the DVL setting. This mode burns more power, but it is useful when the conversion rate is faster than the time for the DMA to cycle through wake up and going back to sleep as it converts more than 4 scan table entries. Without using the wake up on conversion mode, the FIFO may overflow while the DMA is going in and out of sleep.

23.5.4 IADC_CMD - Command

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset							0x0	0x0							0x0	0x0												0x0	0x0		0x0	0x0
Access							W(nB)	W(nB)							W(nB)	W(nB)												W(nB)	W(nB)		W(nB)	W(nB)
Name							SCANFIFOFLUSH	SINGLEFIFOFLUSH							TIMERDIS	TIMEREN												SCANSTOP	SCANSTART		SINGLESTOP	SINGLESTART

Bit	Name	Reset	Access	Description
31:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25	SCANFIFOFLUSH	0x0	W(nB)	**Flush the Scan FIFO**
	Flush the Scan FIFO. The IADC must be enabled, not suspended, and the IADC clock must be running. Operation has completed when STATUS.SCANFIFOFLUSHING has gone low. The scan queue should be disabled. Any incoming scan queue data will be discarded during the flush.			
24	SINGLEFIFOFLUSH	0x0	W(nB)	**Flush the Single FIFO**
	Flush the Single FIFO. The IADC must be enabled, not suspended, and the IADC clock must be running. Operation has completed when STATUS.SINGLEFIFOFLUSHING has gone low. The Single queue should be disabled. Any incoming single queue data will be discarded during the flush.			
23:18	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
17	TIMERDIS	0x0	W(nB)	**Timer Disable**
	Disable the local timer and reset the counter to timer reload value.			
16	TIMEREN	0x0	W(nB)	**Timer Enable**
	Enable the local timer.			
15:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	SCANSTOP	0x0	W(nB)	**Scan Queue Stop**
	Stop the Scan queue. Disables Scan triggers and clears pending conversions in the Scan queue. Any conversion that has already started will continue until it is complete. If the scan queue is stopped before all entries of the scan table have completed, the remaining entries will not be converted.			
3	SCANSTART	0x0	W(nB)	**Scan Queue Start**
	Start the Scan queue. Enables triggering of the Scan queue.			
2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	SINGLESTOP	0x0	W(nB)	**Single Queue Stop**
	Stop the Single queue. Disables Single queue triggers and clears pending conversions in the Single queue. Any conversion that has already started will continue until it is complete.			
0	SINGLESTART	0x0	W(nB)	**Single Queue Start**

Bit	Name	Reset	Access	Description
	Start the Single queue. Enables triggering of the Single queue.			

23.5.5 IADC_TIMER - Timer

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	RW															
Name																	TIMER															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	TIMER	0x0	RW	**Timer Period**
	Number of CLK_SRC_ADC cycles per timer event.			

23.5.6 IADC_STATUS - Status

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset		0x0						0x0			0x0	0x0				0x0	0x0	0x0					0x0	0x0		0x0		0x0	0x0		0x0	0x0
Access		R						R			R	R				R	R	R					R	R		R		R	R		R	R
Name		ADCWARM						SYNCBUSY			MASKREQWRITEPENDING	SINGLEWRITEPENDING				TIMERACTIVE	SCANFIFOFLUSHING	SINGLEFIFOFLUSHING					SCANFIFODV	SINGLEFIFODV		CONVERTING		SCANQUEUEPENDING	SCANQEN		SINGLEQUEUEPENDING	SINGLEQEN

Bit	Name	Reset	Access	Description
31	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
30	ADCWARM	0x0	R	**ADCWARM**
	The ADC analog front end and reference require a delay before converting when coming from a powered down or standby state. This status bit indicates that the analog front end and reference are ready.			
29:25	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
24	SYNCBUSY	0x0	R	**SYNCBUSY**
	Indicates synchronization ongoing			
23:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21	MASKREQWRITE-PENDING	0x0	R	**MASKREQ write pending**
	A write to MASKREQ is pending. The ADC converts using a local working mask register, and only transfers MASKREQ to the local working version when the SCAN queue is not converting.			
20	SINGLEWRITEPEND-ING	0x0	R	**SINGLE write pending**
	The SINGLE register write is pending. The ADC converts using a local working version of the SINGLE register, and only transfer SINGLE to the local working version when the SINGLE queue is not being converted.			
19:17	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
16	TIMERACTIVE	0x0	R	**Timer Active**
	The local timer is running.			
15	SCANFIFOFLUSHING	0x0	R	**The Scan FIFO is flushing**
	A scan data FIFO flush operation is in progress.			
14	SINGLEFIFOFLUSHING	0x0	R	**The Single FIFO is flushing**
	A single data FIFO flush operation is in progress.			

Bit	Name	Reset	Access	Description
13:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	SCANFIFODV	0x0	R	**SCANFIFO Data Valid**
	At least one result in the scan FIFO is ready to read.			
8	SINGLEFIFODV	0x0	R	**SINGLEFIFO Data Valid**
	At least one result in the single FIFO is ready to read.			
7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6	CONVERTING	0x0	R	**Converting**
	The ADC is warmed up and in the process of performing a conversion.			
5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	SCANQUEUEPENDING	0x0	R	**Scan Queue Pending**
	The Scan queue has been triggered and is waiting to start conversion.			
3	SCANQEN	0x0	R	**Scan Queued Enabled**
	The Scan queue is enabled.			
2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	SINGLEQUEUEPEND-ING	0x0	R	**Single Queue Pending**
	The Single queue has been triggered and is waiting to start conversion. When tailgating is used, SINGLEQUEUEPEND-ING will remain high until the a scan operation has completed.			
0	SINGLEQEN	0x0	R	**Single Queue Enabled**
	The Single queue is enabled.			

23.5.7 IADC_MASKREQ - Mask Request

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	RW															
Name																	MASKREQ															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	MASKREQ	0x0	RW	**Scan Queue Mask Request**
	Allows software to specify which entries in the Scan table should be converted. For example MASKREQ = 0x8014 means that scan table entries 15, 4, and 2 will be converted. The other entries will not be converted.			

23.5.8 IADC_STMASK - Scan Table Mask

Offset	Bit Position																															
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	R															
Name																	STMASK															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	STMASK	0x0	R	**Scan Table Mask**
	This is the active / working copy of the MASKREQ register that the ADC uses. It will only be updated at the end of a scan sequence or when no scan is in progress.			

23.5.9 IADC_CMPTHR - Digital Window Comparator Threshold

Offset	Bit Position																															
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset								0x0									0x0															
Access								RW									RW															
Name								ADGT									ADLT															

Bit	Name	Reset	Access	Description
31:16	ADGT	0x0	RW	**ADC Greater Than or Equal to Threshold**
	Compare threshold value for greater-than or equal to comparison. ADGT should be specified in a left-justified, 16-bit format regardless of the FIFO ALIGNMENT setting. Comparisons with 12-bit formats will ignore the 4 LSBs of the ADGT value. Comparisons with 20-bit formats will ignore the 4 LSBs of the 20-bit result. Unipolar or bipolar mode is considered in the comparison. When ADGT is greater than ADLT, the comparison is true if the result is either greater than ADGT or less than ADLT, but false if the result falls between the values.			
15:0	ADLT	0x0	RW	**ADC Less Than or Equal to Threshold**
	Compare threshold value for less-than or equal to comparison. ADLT should be specified in a left-justified, 16-bit format regardless of the FIFO ALIGNMENT setting. Comparisons with 12-bit formats will ignore the 4 LSBs of the ADLT value. Comparisons with 20-bit formats will ignore the 4 LSBs of the 20-bit result. Unipolar or bipolar mode is considered in the comparison. When ADGT is greater than ADLT, the comparison is true if the result is either greater than ADGT or less than ADLT, but false if the result falls between the values.			

23.5.10 IADC_IF - Interrupt Flags

Offset	Bit Position																													
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0												0x0	0x0	0x0	0x0			0x0	0x0			0x0	0x0	0x0				0x0	0x0	0x0	0x0
Access	RW												RW	RW	RW	RW			RW	RW			RW	RW	RW				RW	RW	RW	RW
Name	EM23ABORTERROR												SCANFIFOUF	SINGLEFIFOUF	SCANFIFOOF	SINGLEFIFOOF			PORTALLOCERR	POLARITYERR			SINGLEDONE	SCANTABLEDONE	SCANENTRYDONE				SCANCMP	SINGLECMP	SCANFIFODVL	SINGLEFIFODVL

Bit	Name	Reset	Access	Description
31	EM23ABORTERROR	0x0	RW	**EM2/3 Abort Error**
	The system entered EM2 or EM3 during a conversion with an unsupported clock. Conversion results may be corrupted.			
30:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19	SCANFIFOUF	0x0	RW	**Scan FIFO Underflow**
	A scan FIFO underflow has occured.			
18	SINGLEFIFOUF	0x0	RW	**Single FIFO Underflow**
	A single FIFO underflow has occured.			
17	SCANFIFOOF	0x0	RW	**Scan FIFO Overflow**
	A scan FIFO overflow has occured.			
16	SINGLEFIFOOF	0x0	RW	**Single FIFO Overflow**
	A single FIFO overflow has occured.			
15:14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13	PORTALLOCERR	0x0	RW	**Port Allocation Error**
	A pin was selected on a port which has not been allocated to the IADC in GPIO control.			
12	POLARITYERR	0x0	RW	**Polarity Error**
	Either two even channels or two odd channels were programmed into the channel mux selection. The ADC result will be set to 0xFFFF.			
11:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	SINGLEDONE	0x0	RW	**Single Conversion Done**
	A single conversion has completed.			
8	SCANTABLEDONE	0x0	RW	**Scan Table Done**
	A scan sequence completed. Set at the end of a scan sequence after all valid entries of the scan table have completed.			
7	SCANENTRYDONE	0x0	RW	**Scan Entry Done**
	A scan table conversion completed. Set at the completion of each valid entry of the scan table.			

Bit	Name	Reset	Access	Description
6:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	SCANCMP	0x0	RW	**Scan Result Window Compare**
	Scan digital compare window tripped.			
2	SINGLECMP	0x0	RW	**Single Result Window Compare**
	Single digital compare window tripped.			
1	SCANFIFODVL	0x0	RW	**Scan FIFO Data Valid Level**
	A minimum of (DVL+1) entries are ready to be read from the Scan FIFO.			
0	SINGLEFIFODVL	0x0	RW	**Single FIFO Data Valid Level**
	A minimum of (DVL+1) entries are ready to be read from the Single FIFO.			

23.5.11 IADC_IEN - Interrupt Enable

Offset	Bit Position																													
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0												0x0	0x0	0x0	0x0			0x0	0x0			0x0	0x0	0x0				0x0	0x0	0x0	0x0
Access	RW												RW	RW	RW	RW			RW	RW			RW	RW	RW				RW	RW	RW	RW
Name	EM23ABORTERROR												SCANFIFOUF	SINGLEFIFOUF	SCANFIFOOF	SINGLEFIFOOF			PORTALLOCERR	POLARITYERR			SINGLEDONE	SCANTABLEDONE	SCANENTRYDONE				SCANCMP	SINGLECMP	SCANFIFODVL	SINGLEFIFODVL

Bit	Name	Reset	Access	Description
31	EM23ABORTERROR	0x0	RW	**EM2/3 Abort Error Enable**
	EM2/3 Abort Error Enable			
30:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19	SCANFIFOUF	0x0	RW	**Scan FIFO Underflow Enable**
	Scan FIFO underflow interrupt enable			
18	SINGLEFIFOUF	0x0	RW	**Single FIFO Underflow Enable**
	Single FIFO underflow interrupt enable			
17	SCANFIFOOF	0x0	RW	**Scan FIFO Overflow Enable**
	Scan FIFO overflow interrupt enable			
16	SINGLEFIFOOF	0x0	RW	**Single FIFO Overflow Enable**
	Single FIFO overflow interrupt enable			
15:14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13	PORTALLOCERR	0x0	RW	**Port Allocation Error Enable**
	Port Allocation Error Enable			
12	POLARITYERR	0x0	RW	**Polarity Error Enable**
	Polarity Error Enable			
11:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	SINGLEDONE	0x0	RW	**Single Conversion Done Enable**
	Single Conversion Done interrupt enable			
8	SCANTABLEDONE	0x0	RW	**Scan Table Done Enable**
	Scan Table Done interrupt enable			
7	SCANENTRYDONE	0x0	RW	**Scan Entry Done Enable**
	Scan Entry Done interrupt enable			

Bit	Name	Reset	Access	Description
6:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	SCANCMP	0x0	RW	**Scan Result Window Compare Enable**
	Scan Result Window Compare Enable			
2	SINGLECMP	0x0	RW	**Single Result Window Compare Enable**
	Single Result Window Compare Enable			
1	SCANFIFODVL	0x0	RW	**Scan FIFO Data Valid Level Enable**
	Scan FIFO Data Valid Level interrupt enable			
0	SINGLEFIFODVL	0x0	RW	**Single FIFO Data Valid Level Enable**
	Single FIFO Data Valid Level interrupt enable			

23.5.12 IADC_TRIGGER - Trigger

Offset	Bit Position																													
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																0x0				0x0			0x0					0x0			0x0	
Access																RW				RW			RW					RW			RW	
Name																SINGLETAILGATE				SINGLETRIGACTION			SINGLETRIGSEL					SCANTRIGACTION			SCANTRIGSEL	

Bit	Name	Reset	Access	Description
31:17	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
16	SINGLETAILGATE	0x0	RW	**Single Tailgate Enable**
	Enables tailgating.			
	Value	Mode		Description
	0	TAILGATEOFF		The single queue is ready to start warming up and converting once the trigger had been detected.
	1	TAILGATEON		After the single queue's trigger is detected, it must wait until the end of a scan operation before the Single queue can be converted.
15:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12	SINGLETRIGACTION	0x0	RW	**Single Trigger Action**
	Selects the trigger action for the single queue.			
	Value	Mode		Description
	0	ONCE		For TRIGSEL=IMMEDIATE, converts the single queue once and disables queue. For TRIGSEL = TIMER, PRSCLKGRP, PRSPOS, PRSNEG, converts the single queue once per trigger.
	1	CONTINUOUS		Converts the single queue, then checks for a pending scan queue before converting the single queue again continuously. The queues are first come first serve. If both queues are continuous, the IADC alternates between them.
11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10:8	SINGLETRIGSEL	0x0	RW	**Single Trigger Select**
	Selects the trigger source for the single queue.			
	Value	Mode		Description

Bit	Name	Reset	Access	Description
	0	IMMEDIATE		Immediate triggering. The single queue will be disabled once the conversion is complete, unless TRIGGERACTION is set to continuous.
	1	TIMER		Triggers when the local timer count reaches zero.
	2	PRSCLKGRP		Triggers on PRS1 from a timer module that is using the same clock group as the ADC and has been programmed to use the same clock source as the ADC. The prescale may be different between the ADC and the timer module.
	3	PRSPOS		Triggers on asynchronous PRS1 positive edge. Requires PRS1 to go low for 3 ADC_CLKs before another positive edge can be detected. Generates an additional delay of 1 to 2 ADC_SRC_CLK cycles for synchronization.
	4	PRSNEG		Triggers on asynchronous PRS1 negative edge. Requires PRS1 to go high for 3 ADC_CLKs before another negative edge can be detected. Generates an additional delay of 1 to 2 ADC_SRC_CLK cycles for synchronization. PRSNEG should only be used when the trigger source is from a module that remains powered during EM23. For modules (ie: TIMER) that power down during EM23, PRSPOS should be used for an asynchronous trigger, and PRSCLKGRP should be used for a synchronous trigger.
7:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	SCANTRIGACTION	0x0	RW	**Scan Trigger Action**
	Selects the trigger action for the scan queue.			
	Value	Mode		Description
	0	ONCE		For TRIGSEL=IMMEDIATE, goes through the scan table once and disables queue. For TRIGSEL = TIMER, PRSCLKGRP, PRSPOS, PRSNEG, goes through the scan table once per trigger.
	1	CONTINUOUS		Goes through the scan table, converts each entry with a mask bit set, and puts it back into the scan queue to repeat again continuously. The queues are first come first serve. If both queues are triggered, the single queue will get to convert after each scan table completes. The scan queue will get to convert after each single conversion completes.
3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2:0	SCANTRIGSEL	0x0	RW	**Scan Trigger Select**
	Selects the trigger source for the scan queue.			
	Value	Mode		Description
	0	IMMEDIATE		Immediate triggering. The scan queue will be disabled once all conversions in the scan table are complete, unless TRIGGERACTION is set to continuous.
	1	TIMER		Triggers when the local timer count reaches zero.
	2	PRSCLKGRP		Triggers on PRS0 from a timer module that is using the same clock group as the ADC and has been programmed to use the same clock source as the ADC. The prescale may be different between the ADC and the timer module.

Bit	Name	Reset	Access	Description
	3	PRSPOS		Triggers on asynchronous PRS0 positive edge. Requires PRS0 to go low for 3 ADC_CLKs before another positive edge can be detected. Generates an additional delay of 1 to 2 ADC_SRC_CLK cycles for synchronization.
	4	PRSNEG		Triggers on asynchronous PRS0 negative edge. Requires PRS0 to go high for 3 ADC_CLKs before another negative edge can be detected. Generates an additional delay of 1 to 2 ADC_SRC_CLK cycles for synchronization. PRSNEG should only be used when the trigger source is from a module that remains powered during EM23. For modules (ie: TIMER) that power down during EM23, PRSPOS should be used for an asynchronous trigger, and PRSCLKGRP should be used for a synchronous trigger.
	5	LESENSE		Triggers on LESENSE convert request. When using the LESENSE for the SCAN Table, only one entry is converted per LESENSE convert request.

23.5.13 IADC_CFGx - Configuration

Offset	Bit Position																													
0x048	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset			0x0						0x0					0x0				0x2										0x0			0x0	
Access			RW						RW					RW				RW										RW			RW	
Name			TWOSCOMPL						DIGAVG					REFSEL				ANALOGGAIN										OSRHS			ADCMODE	

Bit	Name	Reset	Access	Description
31:30	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
29:28	TWOSCOMPL	0x0	RW	**Two's Complement**
	Selects output word polarity.			

Value	Mode	Description
0	AUTO	Automatic: Single ended measurements are reported as unipolar and differential measurements are reported as bipolar.
1	FORCEUNIPOLAR	Force all measurements to result in unipolar output. Negative differential numbers will saturate to 0.
2	FORCEBIPOLAR	Force all measurements to result in bipolar output. Single ended measurements are half the range, but allow for small negative measurements.

27:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:21	DIGAVG	0x0	RW	**Digital Averaging**
	Number of output words to convert and average.			

Value	Mode	Description
0	AVG1	Collect one output word (no digital averaging).
1	AVG2	Collect and average 2 digital output words.
2	AVG4	Collect and average 4 digital output words.
3	AVG8	Collect and average 8 digital output words.
4	AVG16	Collect and average 16 digital output words.

20:19	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
18:16	REFSEL	0x0	RW	**Reference Select**
	Selects voltage reference.			

Value	Mode	Description
0	VBGR	Internal 1.21 V reference.

Bit	Name	Reset	Access	Description
	1	VREF		External Reference. (Calibrated for 1.25V nominal.)
	3	VDDX		AVDD (unbuffered)
	4	VDDX0P8BUF		AVDD (buffered) * 0.8
15	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
14:12	ANALOGGAIN	0x2	RW	**Analog Gain**
	Sets analog front end gain.			
	Value	Mode		Description
	1	ANAGAIN0P5		Analog gain of 0.5x.
	2	ANAGAIN1		Analog gain of 1x.
	3	ANAGAIN2		Analog gain of 2x.
	4	ANAGAIN3		Analog gain of 3x.
	5	ANAGAIN4		Analog gain of 4x.
11:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4:2	OSRHS	0x0	RW	**High Speed OSR**
	Over sampling ratio for high speed conversions.			
	Value	Mode		Description
	0	HISPD2		High speed over sampling of 2x.
	1	HISPD4		High speed over sampling of 4x.
	2	HISPD8		High speed over sampling of 8x.
	3	HISPD16		High speed over sampling of 16x.
	4	HISPD32		HIgh speed over sampling of 32x.
	5	HISPD64		High speed over sampling of 64x.
1:0	ADCMODE	0x0	RW	**ADC Mode**
	Selects ADC conversion mode.			
	Value	Mode		Description
	0	NORMAL		High speed mode with a maximum CLK_ADC of 10 MHz.

23.5.14 IADC_SCALEx - Scaling

Offset	Bit Position																													
0x050	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x1	0x0													0x2C000															
Access	RW	RW													RW															
Name	GAIN3MSB	GAIN13LSB													OFFSET															

Bit	Name	Reset	Access	Description
31	GAIN3MSB	0x1	RW	**Gain 3 MSBs**
	3 MSBs of the 16-bit gain value (0=011 or 0.75; 1=1xx or 1.00). Example {GAIN3MSB, GAIN13LSB} = {100, 0_1001_0000_0000} = 1.07031x. Example {GAIN3MSB, GAIN13LSB} = {011, 0_0000_1010_0010} = 0.75494x.			

Value	Mode	Description
0	GAIN011	Upper 3 bits of gain = 011 (0.75x)
1	GAIN100	Upper 3 bits of gain = 100 (1.00x)

Bit	Name	Reset	Access	Description
30:18	GAIN13LSB	0x0	RW	**Gain 13 LSBs**
	13 LSBs of the 16-bit gain value.			
17:0	OFFSET	0x2C000	RW	**Offset**
	Offset			

23.5.15 IADC_SCHEDx - Scheduling

Offset	Bit Position																													
0x054	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0								
Access																							RW								
Name																							PRESCALE								

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:0	PRESCALE	0x0	RW	**Prescale**
	Second level prescaler - divides the CLK_SRC_ADC by (PRESCALE + 1) to generate CLK_ADC. PRESCALE=0 should only be used with HSCLKRATE=0. (See text.)			

23.5.16 IADC_SINGLEFIFOCFG - Single FIFO Configuration

Offset	Bit Position																															
0x070	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																								0x0		0x3			0x0		0x0	
Access																								RW		RW			RW		RW	
Name																								DMAWUFIFOSINGLE		DVL			SHOWID		ALIGNMENT	

Bit	Name	Reset	Access	Description
31:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8	DMAWUFIFOSINGLE	0x0	RW	**Single FIFO DMA wakeup.**

Enables single FIFO to wake DMA in EM2 or EM3.

Value	Mode	Description
0	DISABLED	While in EM2 or EM3, the DMA controller will not be requested.
1	ENABLED	While in EM2 or EM3, the DMA controller will be requested when the single FIFO reaches its Data Valid Level. [DVL must be set to 0 (VALID1).]

Bit	Name	Reset	Access	Description
7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:4	DVL	0x3	RW	**Data Valid Level**

Data valid level before requesting DMA transfer. If the number of words in the FIFO reaches or exceeds DVL+1, DMA requests will be generated.

Value	Mode	Description
0	VALID1	When 1 entry in the single FIFO is valid, set the SINGLEFIFODVL interrupt and request DMA.
1	VALID2	When 2 entries in the single FIFO are valid, set the SINGLEFIFODVL interrupt and request DMA.
2	VALID3	When 3 entries in the single FIFO are valid, set the SINGLEFIFODVL interrupt and request DMA.
3	VALID4	When 4 entries in the single FIFO are valid, set the SINGLEFIFODVL interrupt and request DMA.
4	VALID5	When 5 entries in the single FIFO are valid, set the SINGLEFIFODVL interrupt and request DMA.
5	VALID6	When 6 entries in the single FIFO are valid, set the SINGLEFIFODVL interrupt and request DMA.
6	VALID7	When 7 entries in the single FIFO are valid, set the SINGLEFIFODVL interrupt and request DMA.

Bit	Name	Reset	Access	Description
	7	VALID8		When 8 entries in the single FIFO are valid, set the SINGLEFIFODVL interrupt and request DMA.
3	SHOWID	0x0	RW	**Show ID**
	ID of 0x20 will be applied in the output words.			
2:0	ALIGNMENT	0x0	RW	**Alignment**
	Alignment of output data written into FIFO.			

Value	Mode	Description
0	RIGHT12	ID[7:0], SIGN_EXT, DATA[11:0]
1	RIGHT16	ID[7:0], SIGN_EXT, DATA[15:0]
2	RIGHT20	ID[7:0], SIGN_EXT, DATA[19:0]
3	LEFT12	DATA[11:0], 000000000000, ID[7:0]
4	LEFT16	DATA[15:0], 00000000, ID[7:0]
5	LEFT20	DATA[19:0], 0000, ID[7:0]

23.5.17 IADC_SINGLEFIFODATA - Single FIFO DATA

Offset	Bit Position																													
0x074	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R(r)																															
Name	DATA																															

Bit	Name	Reset	Access	Description
31:0	DATA	0x0	R(r)	**Single FIFO Read Data**
	Reads and pops the oldest value from the single FIFO.			

23.5.18 IADC_SINGLEFIFOSTAT - Single FIFO Status

Offset	Bit Position																															
0x078	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0		
Access																													R		
Name																													FIFOREADCNT		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	FIFOREADCNT	0x0	R	**FIFO Read Count**
	Number of valid entries available to read.			

23.5.19 IADC_SINGLEDATA - Single Data

Offset	Bit Position																															
0x07C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																0x0																
Access																R																
Name																DATA																

Bit	Name	Reset	Access	Description
31:0	DATA	0x0	R	**Data**
	Reads the most recent data word from the single FIFO, but does not pop a value. Even if the FIFO has overflowed and stopped updating, the most recent conversion will continue to overwrite SINGLEDATA.			

23.5.20 IADC_SCANFIFOCFG - Scan FIFO Configuration

Offset	Bit Position																															
0x080	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																								0x0			0x3		0x0		0x0	
Access																								RW			RW		RW		RW	
Name																								DMAWUFIFOSCAN			DVL		SHOWID		ALIGNMENT	

Bit	Name	Reset	Access	Description
31:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8	DMAWUFIFOSCAN	0x0	RW	**Scan FIFO DMA Wakeup**

Enables scan FIFO to wake DMA in EM2 or EM3.

Value	Mode	Description
0	DISABLED	While in EM2 or EM3, the DMA controller will not be requested.
1	ENABLED	While in EM2 or EM3, the DMA controller will be requested when the scan FIFO reaches its Data Valid Level. [DVL must be set to 0 (VALID1).]

7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:4	DVL	0x3	RW	**Data Valid Level**

Data valid level before requesting DMA transfer. If the number of words in the FIFO reaches or exceeds DVL+1, DMA requests will be generated.

Value	Mode	Description
0	VALID1	When 1 entry in the scan FIFO is valid, set the SCANFIFODVL interrupt and request DMA.
1	VALID2	When 2 entries in the scan FIFO are valid, set the SCANFIFODVL interrupt and request DMA.
2	VALID3	When 3 entries in the scan FIFO are valid, set the SCANFIFODVL interrupt and request DMA.
3	VALID4	When 4 entries in the scan FIFO are valid, set the SCANFIFODVL interrupt and request DMA.
4	VALID5	When 5 entries in the scan FIFO are valid, set the SCANFIFODVL interrupt and request DMA.
5	VALID6	When 6 entries in the scan FIFO are valid, set the SCANFIFODVL interrupt and request DMA.
6	VALID7	When 7 entries in the scan FIFO are valid, set the SCANFIFODVL interrupt and request DMA.

Bit	Name	Reset	Access	Description
	7	VALID8		When 8 entries in the scan FIFO are valid, set the SCANFIFODVL interrupt and request DMA.
3	SHOWID	0x0	RW	**Show ID**
	Enable ID in output words.			
2:0	ALIGNMENT	0x0	RW	**Alignment**
	Alignment of output data written into FIFO.			

Value	Mode	Description
0	RIGHT12	ID[7:0], SIGN_EXT, DATA[11:0]
1	RIGHT16	ID[7:0], SIGN_EXT, DATA[15:0]
2	RIGHT20	ID[7:0], SIGN_EXT, DATA[19:0]
3	LEFT12	DATA[11:0], 000000000000, ID[7:0]
4	LEFT16	DATA[15:0], 00000000, ID[7:0]
5	LEFT20	DATA[19:0], 0000, ID[7:0]

23.5.21 IADC_SCANFIFODATA - Scan FIFO Read Data

Offset	Bit Position																													
0x084	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R(r)																															
Name	DATA																															

Bit	Name	Reset	Access	Description
31:0	DATA	0x0	R(r)	**Data**
	Reads and pops the oldest value from the scan FIFO.			

23.5.22 IADC_SCANFIFOSTAT - Scan FIFO Status

Offset	Bit Position																															
0x088	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0		
Access																													R		
Name																													FIFOREADCNT		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	FIFOREADCNT	0x0	R	**FIFO Read Count**
	Number of valid entries available to read.			

23.5.23 IADC_SCANDATA - Scan Data

Offset	Bit Position																															
0x08C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																0x0																
Access																R																
Name																DATA																

Bit	Name	Reset	Access	Description
31:0	DATA	0x0	R	**Data**
	Reads the most recent data word from the scan FIFO, but does not pop a value. Even if the FIFO has overflowed and stopped updating, the most recent conversion will continue to overwrite SCANDATA.			

23.5.24 IADC_SINGLE - Single Queue Port Selection

Offset	Bit Position																													
0x098	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset															0x0	0x0	0x0				0x0				0x0				0x0			
Access															RW	RW	RW				RW				RW				RW			
Name															CMP	CFG	PORTPOS				PINPOS				PORTNEG				PINNEG			

Bit	Name	Reset	Access	Description
31:18	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
17	CMP	0x0	RW	**Comparison Enable**
	Enable digital window comparison for this entry.			
16	CFG	0x0	RW	**Configuration Group Select**
	Select which configuration group (CFGx, SCALEx, SCHEDx registers) is used with this entry.			

Value	Mode	Description
0	CONFIG0	Use configuration group 0
1	CONFIG1	Use configuration group 1

Bit	Name	Reset	Access	Description
15:12	PORTPOS	0x0	RW	**Positive Port Select**
	Port (A, B, C, D) or special signal assigned to the positve input of the ADC			

Value	Mode	Description
0	GND	Ground
1	SUPPLY	Supply Pin - Select specific supply using PINPOS
2	DAC0	Direct connection to DAC0_CH0
4	PADANA0	Direct connection to AIN0 input pin
5	PADANA2	Direct connection to AIN2 input pin
8	PORTA	Port A - Select pin number using PINPOS
9	PORTB	Port B - Select pin number using PINPOS
10	PORTC	Port C - Select pin number using PINPOS
11	PORTD	Port D - Select pin number using PINPOS

Bit	Name	Reset	Access	Description
11:8	PINPOS	0x0	RW	**Positive Pin Select**
	Pin number for the positive input of the ADC.			
7:4	PORTNEG	0x0	RW	**Negative Port Select**
	Port (A, B, C, D) or special signal assigned to the negative input of the ADC			

Value	Mode	Description
0	GND	Ground (single-ended)

Bit	Name	Reset	Access	Description
	2	DAC1		Direct connection to DAC0_CH1
	4	PADANA1		Direct connection to AIN1 input pin
	5	PADANA3		Direct connection to AIN3 input pin
	8	PORTA		Port A - Select pin number using PINNEG
	9	PORTB		Port B - Select pin number using PINNEG
	10	PORTC		Port C - Select pin number using PINNEG
	11	PORTD		Port D - Select pin number using PINNEG
3:0	PINNEG	0x0	RW	**Negative Pin Select**
	Pin number for the negative input of the ADC.			

23.5.25 IADC_SCANx - SCAN Entry

Offset	Bit Position																													
0x0A0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset															0x0	0x0	0x0				0x0				0x0				0x0			
Access															RW	RW	RW				RW				RW				RW			
Name															CMP	CFG	PORTPOS				PINPOS				PORTNEG				PINNEG			

Bit	Name	Reset	Access	Description
31:18	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
17	CMP	0x0	RW	**Comparison Enable**
	Enable digital window comparison for this entry.			
16	CFG	0x0	RW	**Configuration Group Select**
	Select which configuration group (CFGx, SCALEx, SCHEDx registers) is used with this entry.			

Value	Mode	Description
0	CONFIG0	Use configuration group 0
1	CONFIG1	Use configuration group 1

15:12	PORTPOS	0x0	RW	**Positive Port Select**
	Port (A, B, C, D) or special signal assigned to the positve input of the ADC			

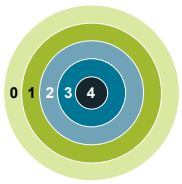
Value	Mode	Description
0	GND	Ground
1	SUPPLY	Supply Pin - Select specific supply using PINPOS
2	DAC0	Direct connection to DAC0_CH0
4	PADANA0	Direct connection to AIN0 input pin
5	PADANA2	Direct connection to AIN2 input pin
8	PORTA	Port A - Select pin number using PINPOS
9	PORTB	Port B - Select pin number using PINPOS
10	PORTC	Port C - Select pin number using PINPOS
11	PORTD	Port D - Select pin number using PINPOS

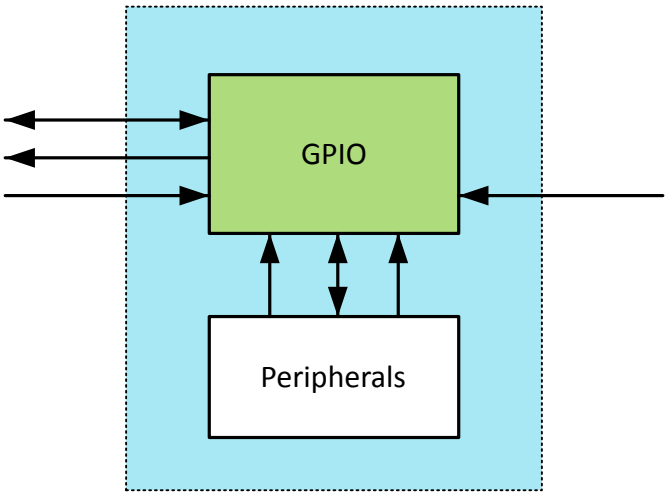
11:8	PINPOS	0x0	RW	**Positive Pin Select**
	Pin number for the positive input of the ADC.			
7:4	PORTNEG	0x0	RW	**Negative Port Select**
	Port (A, B, C, D) or special signal assigned to the negative input of the ADC			

Value	Mode	Description
0	GND	Ground (single-ended)

Bit	Name	Reset	Access	Description
	2	DAC1		Direct connection to DAC0_CH1
	4	PADANA1		Direct connection to AIN1 input pin
	5	PADANA3		Direct connection to AIN3 input pin
	8	PORTA		Port A - Select pin number using PINNEG
	9	PORTB		Port B - Select pin number using PINNEG
	10	PORTC		Port C - Select pin number using PINNEG
	11	PORTD		Port D - Select pin number using PINNEG
3:0	PINNEG	0x0	RW	**Negative Pin Select**
	Pin number for the negative input of the ADC.			

24. GPIO - General Purpose Input/Output





Quick Facts

What?

The General Purpose Input/Output (GPIO) is used for pin configurations as well as routing for peripheral pin connections.

Why?

Easy to use and highly configurable input/output pins are important to fit many communication protocols as well as minimizing software control overhead. Flexible routing of peripheral functions helps to ease PCB layout.

How?

Each pin on the device can be individually configured as either an input or an output with several different drive modes. Also, individual bit manipulation registers minimizes control overhead. Peripheral connections to pins can be routed to pins as desired solving congestion and contention issues that may arise with limited routing flexibility. Fully asynchronous interrupts can also be generated from any pin.

24.1 Introduction

In the EFR32xG25 devices the General Purpose Input/Output (GPIO) pins are organized into ports with up to 16 pins each. These GPIO pins can be individually configured as either an output or input. More advanced configurations like open-drain, open-source, and glitch filtering can be configured for each individual GPIO pin. Peripheral resources, like Timer PWM outputs or USART RX/TX can be routed to the GPIO pins as desired by the user. Finally, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals or used to trigger an external interrupt.

24.2 Features

- Individual configuration for each pin
  - Tristate (reset state)
  - Push-pull
  - Open-drain
  - Pull-up resistor
  - Pull-down resistor
  - Programable Slewrate Control
- EM4 IO pin retention
  - Output enable
  - Output value
  - Pull enable
  - Pull direction
- EM4 wake-up on selected GPIO pins
- Glitch suppression input filter
- Extremely flexible analog and digital resource routing
- Toggle register for output data
- Dedicated data input register (read-only)
- Interrupts
  - Two independent interrupt vectors
  - All GPIO pins are selectable as interrupts in EM0 and EM1
  - All PA and PB GPIO pins are also selectable as interrupts down to EM2 and EM3
  - All EM4 wake-up pins are also available as interrupts in EM0/1/2/3
  - Separate enable, status, set and clear registers
  - Asynchronous sensing
  - Rising, falling or both edges
- Peripheral Reflex System producer
  - All GPIO pins are selectable

24.3 Functional Description

An overview of the GPIO module is shown in Figure 24.1 Pin Configuration on page 788. The GPIO pins are grouped into 16-pin ports. Each individual GPIO pin is called Pxn where x indicates the port (A, B, C ...) and n indicates the pin number (0,1,....,15). Fewer than 16 pins may be available on some ports depending on the total number of I/O pins on the package. After a reset, both input and output are disabled for all pins on the device, except for the Serial Wire Debug pins.

To use a pin, the Mode Register (GPIO_Px_MODEL/GPIO_Px_MODEH) must be configured for the pin to make it an input or output. These registers can also do more advanced configuration, which is covered in 24.3.1 Pin Configuration. When the port is configured as an input or an output, the Data In Register (GPIO_Px_DIN) can be used to read the level of each pin in the port (bit n in the register is connected to pin n on the port). When configured as an output, the value of the Data Out Register (GPIO_Px_DOUT) will be driven to the pin.

The DOUT value can be changed in 4 different ways:

- Writing to the GPIO_Px_DOUT register
- Writing the SET address of the GPIO_Px_DOUT register sets the DOUT bits
- Writing the CLEAR address of the GPIO_Px_DOUT register clears the DOUT bits
- Writing the GPIO_Px_DOUTTGL register toggles the corresponding DOUT bits

Reading the GPIO_Px_DOUT register will return its contents. Reading the GPIO_Px_DOUTTGL register will return 0.

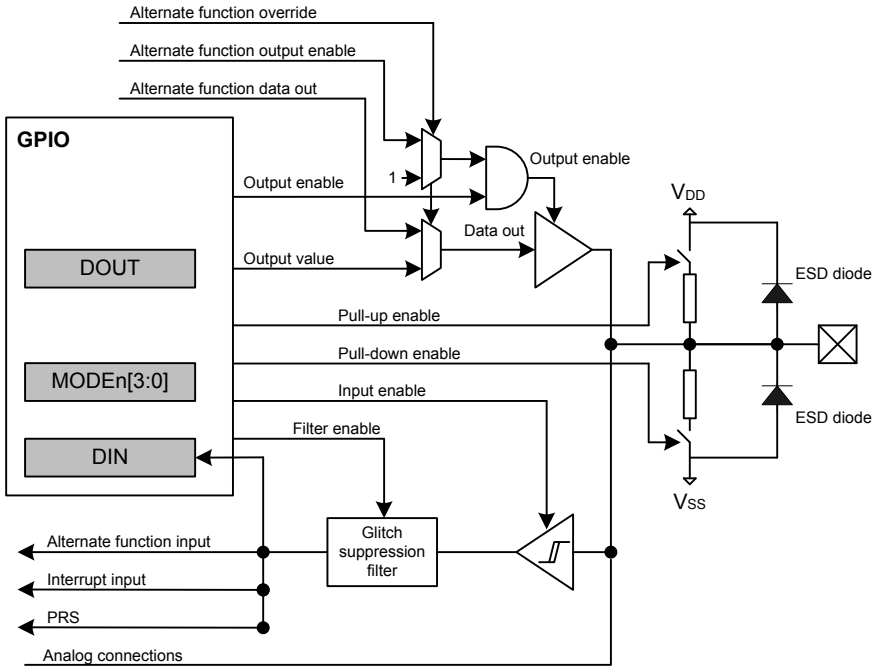


Figure 24.1. Pin Configuration

24.3.1 Pin Configuration

In addition to setting the pins as either outputs or inputs, the GPIO_Px_MODEL and GPIO_Px_MODEH registers can be used for more advanced configurations. GPIO_Px_MODEL contains 8 bit fields named MODEn (n=0,1,..7) which control pins 0-7, while GPIO_Px_MODEH contains 8 bit fields named MODEn (n=8,9,..15) which control pins 8-15. In some modes GPIO_Px_DOUT is also used for extra configurations like pull-up/down and glitch suppression filter enable. Table 24.1 Pin Configuration on page 789 shows the available configurations.

Table 24.1. Pin Configuration

MODEn	Input	Output	DOUT	Pull-down	Pull-up	Alt Port Ctrl	Input Filter	Description
DISABLED	Disabled	Disabled	0					Input disabled
			1		On			Input disabled with pull-up
INPUT	Enabled if not DINDIS		0					Input enabled
			1				On	Input enabled with filter
INPUTPULL			0	On				Input enabled with pull-down
			1		On			Input enabled with pull-up
INPUTPULLFILTER			0	On			On	Input enabled with pull-down and filter
			1		On		On	Input enabled with pull-up and filter
PUSHPULL		Push-pull	x					Push-pull
PUSHPULLALT			x			On		Push-pull with alternate port control values
WIREDOR		Open Source (Wired-OR)	x					Open-source
WIREDORPULLDOWN			x	On				Open-source with pull-down
WIREDAND		Open Drain (Wired-AND)	x					Open-drain
WIREDANDFILTER			x				On	Open-drain with filter
WIREDANDPULLUP			x		On			Open-drain with pull-up
WIREDANDPULLUPFILTER			x		On		On	Open-drain with pull-up and filter
WIREDANDALT			x			On		Open-drain with alternate port control values
WIREDANDALTFILTER			x			On	On	Open-drain with alternate port control values and filter
WIREDANDALTPULLUP			x		On	On		Open-drain with alternate port control values and pull-up
WIREDANDALTPULLUPFILTER			x		On	On	On	Open-drain with alternate port control values, pull-up and filter

MODEn determines which mode the pin is in at a given time. Setting MODEn to DISABLED disables the pin, reducing power consumption to a minimum. When the output driver and input driver are disabled, the pin can be used as a connection for an analog module. An input is enabled by setting MODEn to any value other than DISABLED while DINDIS for the given port is cleared. Set DINDIS to disable

the input of a GPIO port. The pull-up, pull-down and glitch filter function can optionally be applied to the input, see Figure 24.2 Tristated Output with Optional Pull-up or Pull-down on page 790.

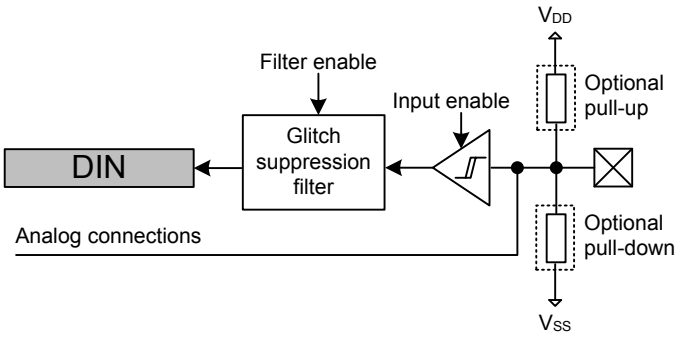


Figure 24.2. Tristated Output with Optional Pull-up or Pull-down

When MODEn is PUSHPULL or PUSHPULLALT, the pin operates in push-pull mode. In this mode, the pin can have alternate port control values and can be driven either high or low, dependent on the value of GPIO_Px_DOUT. The push-pull configuration is shown in Figure 24.3 Push-Pull Configuration on page 790.

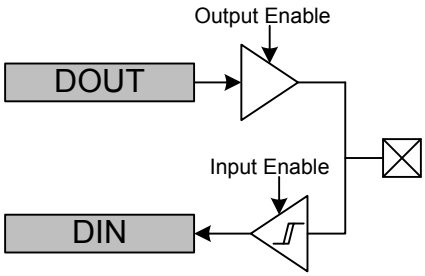


Figure 24.3. Push-Pull Configuration

When MODEn is WIREDOR or WIREDORPULLDOWN, the pin operates in open-source mode (with a pull-down resistor for WIREDORPULLDOWN). When driving a high value in open-source mode, the pull-down is disconnected to save power.

When the mode is prefixed with WIREDAND, the pin operates in open-drain mode as shown in Figure 24.4 Open-drain on page 790. In open-drain mode, the pin can have an input filter, a pull-up, alternate port control values or any combination of these. When driving a low value in open-drain mode, the pull-up is disconnected to save power.

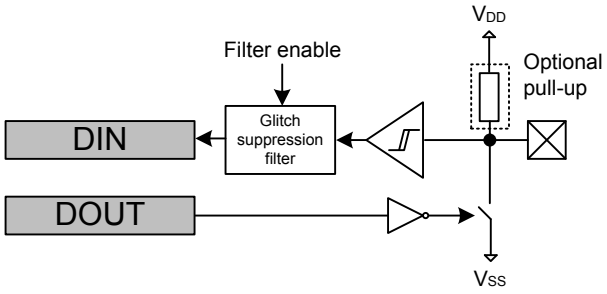


Figure 24.4. Open-drain

24.3.2 Alternate Port Control

The Alternate Port Control allows for additional flexibility of port level settings. A user may setup two different port configurations (normal and alternate modes) and select which is applied on a pin by pin bases. For example you may configure half of port A to use the slowest slew rate while the other half uses a faster slew rate.

Alternate port control is enabled when MODEn is set to any of the ALT enumerated modes (i.e.. PUSHPULLALT). When MODEn is an alternate mode, the pin uses the alternate port control values specified in the DINDISALT and SLEWRATEALT fields in GPIO_Px_CTRL. In all other modes, the port control values are used from the DINDIS and SLEWRATE fields in GPIO_Px_CTRL.

24.3.3 Slew Rate

The slewrate can be applied to pins on a port-by-port basis. The slew rate applied to pins configured using normal MODEn settings can be controlled using the SLEWRATE fields in GPIO_Px_CTRL. The slewrate applied to pins configured using the alternate MODEn settings can be controlled using the SLEWRATEALT field.

The lowest slew rate setting has limited drive strength. That is the current is limited to about 1 mA. This setting provides slow switching and limited drive. A slew rate setting of 1 provides the slowest switching with full drive capability. The maximum recommended setting for most digital I/O is 6. A slew rate setting of 7 should only be used for high-speed clock signals, above 10 MHz. A setting of 7 should not be used on more than one pin per port. Please refer to the datasheet for GPIO rise and fall times.

24.3.4 Input Disable

The pin inputs can be disabled on a port-by-port basis. The input of pins configured using the normal MODEn settings can be disabled by setting DINDIS in GPIO_Px_CTRL. The input of pins configured using the alternate MODEn settings can be disabled by setting DINDISALT.

24.3.5 Configuration Lock

The GPIO configuration registers (GPIO_Px_CTRL, PIO_Px_MODEL, GPIO_xBUSALLOC, GPIO_EXTIPSELL, GPIO_EXTIPINSEL, GPIO_x_yROUTE, and GPIO_xROUTEEN) can be locked by writing any value other than 0xA534 to GPIO_LOCK. Writing the value 0xA534 to the GPIOx_LOCK register unlocks the configuration registers.

24.3.6 EM2 Functionality

While all GPIO pins retain their state in EM2, only pins on port A and B remain fully functional in EM2. Digital peripherals which are active in EM2 must have their resources routed to pins on port A or B to function correctly in EM2. Analog peripherals may use any GPIO pin while in EM2 provided that the ABUS was configured prior to entering EM2. However, analog peripherals that are configured to scan multiple pins while in EM2 (such as the ADC) dynamically reconfigure the ABUS while in EM2 and thus must use only pins on port A and B.

24.3.7 EM4 Functionality

By default GPIO pins revert back to their reset state when EM4 is entered. The GPIO pins can be configured to retain the settings for output enable, output value, pull enable, and pull direction while in EM4.

EM4 GPIO retention is controlled with the EM4IORETMODE field in the EMU_EM4CTRL register:

- Setting EM4IORETMODE to EM4EXIT will cause GPIO retention to persist while in EM4. GPIO state will be reset during wakeup.
- Setting EM4IORETMODE to SWUNLATCH will cause the GPIO retention to persist through EM4 and wakeup, until the EM4UNLATCH bit is written by software. When using SWUNLATCH, the GPIO register values are still reset on wakeup. To ensure the GPIO state does not change, software must re-write the GPIO registers before setting EM4UNLATCH and ending EM4 GPIO retention. Note that the GPIO state cannot be retained through an EM4 wakeup due to a reset (e.g., pin reset or POR reset) - only non-reset methods of EM4 wakeup are supported (e.g., EM4WU IRQ or BURTC IRQ).

See the EMU chapter for additional documentation on EM4IORETMODE and the EM4UNLATCH bit.

24.3.8 EM4 Wakeup

It is possible to trigger a wake-up from EM4 using any of the selectable EM4WU GPIO pins. The wake-up request can be triggered through the pins by enabling the corresponding bit in the GPIO_EM4WUEN register. When EM4 wake-up is enabled for the pin, the input filter is enabled during EM4. This is done to avoid false wake-up caused by glitches. In addition, the polarity of the EM4 wake-up request can be selected using the GPIO_EM4WUPOL register.

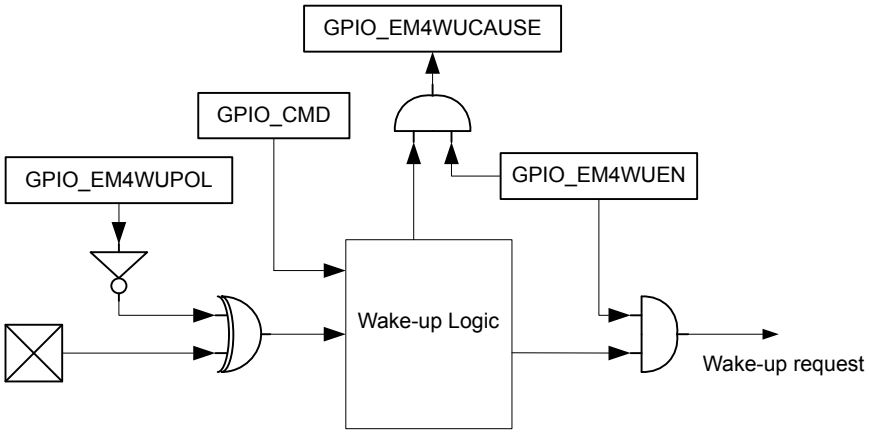


Figure 24.5. EM4 Wake-up Logic

The pins used for EM4 wake-up must be configured as inputs with glitch filters using the GPIO_Px_MODEL register. If the input is disabled and the wakeup polarity is low, a false wakeup will occur when entering EM4. If the input is enabled, the glitch filtered is disabled, and the polarity is set low, a glitch will occur when going into EM4 that will cause an immediate wake-up. Before going down to EM4, it is important to clear the wake-up logic by setting the GPIO_IFC bit, which clears the wake-up logic, including the GPIO_IF register. It is possible to determine which pin caused the EM4WU by reading the GPIO_IF register.

Each EM4WU signal is connected to a fixed pin. Refer to the Alternate Function Table in the device Datasheet for the location of each EM4 wakeup signal.

24.3.9 Debug Connections

24.3.9.1 JTAG Debug Connection

The JTAG Debug Port is a fixed location resource connected directly to specific GPIO pins. Refer to the Alternate Function Table in the device Datasheet for the location of the JTAG signals. By default TMS, TCK, TDO, and TDI pin connections are enabled with internal pull up, pull down, no pull, and pull up resistors, respectively. It is possible to disable these pin connections (and disable the pull resistors) by setting the SWDIOTMSPEN, SWCLKTCKPEN, TDOPEN, and TDIPEN bits in GPIO_DEBUGROUTEPEN to 0.

24.3.9.2 Serial Wire Debug Connection

The SW Debug Port is a fixed location resource connected directly to specific GPIO pins. Refer to the Alternate Function Table in the device Datasheet for the location of the SW Debug port signals. The SWDIO and SWCLK pin connections are enabled by default with internal pull up and pull down resistors, respectively. It is possible to disable these pin connections (and disable the pull resistors) by setting the SWDIOTMSPEN and SWCLKTCKPEN bits in GPIO_DEBUGROUTEPEN to 0.

The Serial Wire Viewer pin, SWV, can be enabled by setting the SWVPEN bit in GPIO_TRACEROUTEPEN.

Note: The SWV pin is not affected by debug lock, so the SWV pin should not be enabled for production devices.

24.3.9.3 Disabling Debug Connections

When the debug pins are disabled, the device can no longer be accessed by a debugger. A reset will set the debug pins back to their enabled default state. The GPIO_DBGROUTEPEN register can only be updated when the debugger is disconnected from the system. Any attempts to modify GPIO_DBGROUTEPEN when the debugger is connected will not occur. If you do disable the debug pins, make sure you have at least a 3 second timeout at the start of your program code before you disable the debug pins. This way the debugger will have time to connect to the device after a reset and before the pins are disabled.

24.3.9.4 ETM Trace Connections

The device includes ETM trace pins. The trace clock can be enabled by setting the TRACECLKPEN bit-field in GPIO_TRACEROUTEPEN. The data pin(s) can be enabled individually by setting TRACEDATAxPEN in GPIO_TRACEROUTEPEN. The trace pins are fixed location resources connected to specific pins. Refer to the Alternate Function Table in the device Datasheet for the location of the ETM trace port signals.

24.3.10 Interrupt Generation

24.3.10.1 Standard Interrupt Generation

The GPIO can generate an interrupt from any edge of the input of any GPIO pin on the device. The standard interrupts have asynchronous sense capability, enabling wake-up from energy modes as low as EM3, see Figure 24.6 Pin n Interrupt Generation on page 793.

Note: In EM2 and EM3, only signals on Port A and Port B are available as standard interrupts. Standard interrutps are available to all pins in EM0 and EM1.

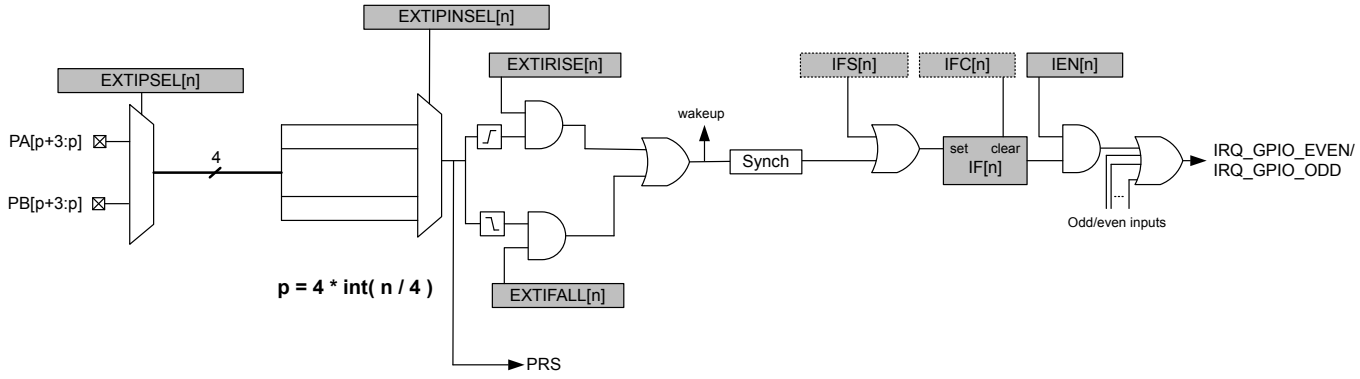


Figure 24.6. Pin n Interrupt Generation

The standard external pin interrupts are numbered starting with 0. Each interrupt has a corresponding enable bit in the GPIO_IEN register and an interrupt flag bit in the GPIO_IF register. Each interrupt may be used with one of four possible pins on any available port. First select the desired port for each interrupt using the corresponding EXTIPSELx field in the GPIO_EXTIPSELL register. (Some devices with many pins may also have a GPIO_EXTIPSELH register.)

Each interrupt can be mapped to one of four possible pins on the selected port. External interrupts EXTI0 through EXTI3 may be mapped to pins 0,1,2, or 3 on any available port. External interrupts EXTI4 through EXTI7 may be mapped to pins 4,5,6 or 7 on any available port.

Note: Note that while the EXTIEN field in the GPIO_IEN register has 15 bits, the number of useful bits is limited by the number of pins available in the widest port. If the widest port is 8 bits wide, only the first 8 external interrupts are useful.

The selected pin for each interrupt is the base plus the offset. The base for EXTI0 through EXTI3 is 0, while the base for interrupts EXTI4 through EXTI7 is 4. The base may be calculated by taking the interrupt number, dividing by four, then using only the integer portion of the quotient. (BASE = Integer(N/4)

The offset is selected using the corresponding field in the GPIO_EXTIPINSELL register, (Some devices with many pins may also have a GPIO_EXTIPINSELH register.) Subtract the base from the desired pin number to get the offset. For example, to map EXTI5 to pin 7 of PORTA, the base is 4 and the offset will be 3.

The GPIO_EXTIRISE[n] and GPIO_EXTIFALL[n] registers enable sensing of rising and falling edges. By setting the EXT[n] bit in GPIO_IEN, a high interrupt flag n, will trigger one of two interrupt lines. The even interrupt line is triggered by any enabled even numbered interrupt flag index, while the odd interrupt line is triggered by odd flag indexes. The interrupt flags can be set and cleared by software when writing the GPIO_IFS and GPIO_IFC registers. Since the external interrupts are asynchronous, they are sensitive to noise. To increase noise tolerance, the MODEx field(s) in the GPIO_Px_MODEL register, should be set to include glitch filtering for pins that have external interrupts enabled.

24.3.10.2 Interrupt Generation on EM4WU Pins

In addition to being an EM4 wake source, any of the dedicated EM4WU (EM4 wake-up) signals on PA, PB, PC or PD may be used to generate edge-sensitive interrupts in EM0, EM1, EM2, and EM3.

In order to enable an EM4WU pin as an interrupt, set the EM4WUIENn field in the GPIO_IEN register and the EM4WUENn field in the EM4WUEN register. The EM4WUPOLn field in the GPIO_EM4WUPOL register is used to set the desired polarity for the interrupt (0 for a falling edge, and 1 for a rising edge).

Upon an interrupt occurring, the corresponding EM4WU index in the GPIO_IF register will be set along with the odd or even interrupt line depending on the index inside of GPIO_IF. For example, by setting the. EM4WU8 in GPIO_EM4WUPOL and EM4WU[8] in GPIO_IEN, the interrupt flag EM4WU[8] in GPIO_IF will be triggered by a rising edge on pin EM4WU8 and a interrupt request will be sent on IRQ_GPIO_EVEN.

The wake-up granularity of the EM4WU interrupts is based on the settings of the EM4WU field in the GPIO_IEN register and the EM4WUEN field in the GPIO_EM4WUEN register (see Table 24.2 EM4WU Interrupt Energy Mode Wakeup on page 794).

Table 24.2. EM4WU Interrupt Energy Mode Wakeup

EM4WUIENn in GPIO_IEN	EM4WUENn in GPIO_EM4WUEN	Energy Mode Wakeup	Interrupt
x	0	No Wake	No Interrupt
0	1	Wake from EM4	No Interrupt
1	1	Wake from EM1, EM2,EM3, or EM4	Interrupt from EM0, EM1, EM2, or EM3

For example, to configure the device to wake up and generate an interrupt when PD02 (EM4WU9) sees a falling edge:

1. Set bit 9 of EM4WUEN in the GPIO_EM4WUEN register to '1'. This enables the asynchronous wake logic.
2. Set bit 9 of EM4WUIEN in the GPIO_IEN register to '1'. This enables routing of the wake signal to the GPIO_ODD IRQ.
3. Clear bit 9 of EM4WUPOL in the GPIO_EM4WUPOL register to '0'. This indicates that the interrupt should occur when a falling edge is detected at the pin.
4. Enable the GPIO.ODD IRQ. The ODD interrupt is used because the bit index of EM4WUIF in GPIO_IF is odd.

24.3.11 Output to PRS

All pins within a group of four(0-3,4-7,8-11,12-15) from all ports are grouped together to form one PRS producer which outputs to the PRS. The pin from which the output should be taken is selected in the same fashion as the edge interrupts.

PRS output is not affected by the interrupt edge detection logic or gated by the IEN bits. See 24.3.10 Interrupt Generation for an illustration of where the PRS output signal is generated.

24.3.12 Peripheral Resource Routing

Most peripherals have resources that need to be connected to GPIO pins to function. For example, the I2C has SDA and SCL which need to be connected to pins for the I2C to communicate with other ICs. Resources come in three types. Fixed resources are hard-wired to a pin and can only be accessed in that location. For example the LFXO LFXTAL_I and LFXTAL_O resources are only available on one pin each. Digital route-able resources are connected to pins through the 24.3.12.1 Digital Bus (DBUS) which allows for extremely flexible resource placement. Analog route-able resources are connected to pins though the 24.3.12.2 Analog Bus (ABUS) which provides extremely flexible resource placement.

The locations of fixed resources and the limitations of ABUS and DBUS on each device can be found in the device data sheet.

24.3.12.1 Digital Bus (DBUS)

The Digital Bus (DBUS) is an any-to-any switch matrix between peripheral resources and GPIO pins as shown in Figure 24.7 Digital Bus Interconnect on page 795. There are two DBUSes on the EFR32xG25 - DBUSAB serves ports A and B, while DBUSCD serves ports C and D. Not all peripherals have access to both DBUSes.

To connect a resource to a pin, first select the desired PORT and PIN in the GPIO_x_yROUTE register, where x is the peripheral name and y is the resource name. The PORT field is encoded as PA = 0, PB = 1, PC = 2, etc. Once the pin is selected, the resource must be enabled by setting its enable bit in the appropriate GPIO_x_ROUTEEN register. For example, to route the SDA resource of I2C0 to PB03, set PORT to 0x1 and PIN to 0x3 in GPIO_I2C0_SDAROUTE. Then set the GPIO_I2C0_ROUTEN.SDAPEN bit.

Any pin connected to a digital resource should be properly configured for that resource (refer to 24.3.1 Pin Configuration). For example, an I2C SDA should be configured as open-drain, a USART (or EUSART) TX should be configured as push-pull, and a USART (or EUSART) RX should be configured as an input.

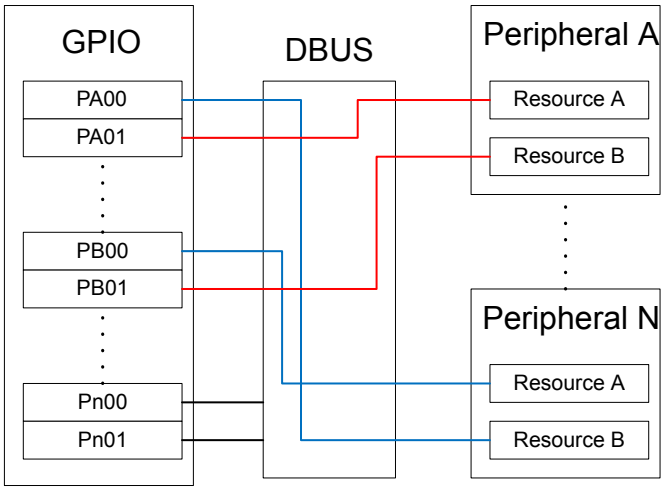


Figure 24.7. Digital Bus Interconnect

24.3.12.2 Analog Bus (ABUS)

Analog peripherals may be connected to any pins on port A, B, C, or D via the Analog Bus. There are three analog buses on the EFR32xG25: one dedicated to Port A (ABUSA), one dedicated to port B (ABUSB), and one that serves both ports C and D (ABUSCD). The specific pin and port selection for analog resources are configured in the analog peripherals. Refer to the respective analog peripheral chapter for this information. However, the GPIO block must be configured to grant the peripheral access to an ABUS before any connection can be made.

Note: The analog signals on ABUSA and ABUSB will be voltage limited by the lowest supply voltage of IOVDD1 and AVDD. The analog signals on ABUSCD will be voltage limited by the lowest supply voltage of IOVDD0, IOVDD2, and AVDD.

Up to two analog peripherals may be given access to an ABUS at any one time and the even/odd pins of each bus are configured independently. This means that a single bus may have up to four different analog peripherals connected to it: two on the even pins and two on the odd pins. The GPIO_ABUSxALLOC register, where x is the port, determines which peripherals have access to the bus. To grant a peripheral access to the bus even pins select it in either the EVEN0 or EVEN1 field. To grant a peripheral access to the bus odd pins select it in either the ODD0 or ODD1 fields.

When a differential connection is being used, positive inputs are restricted to the EVEN pins and negative inputs are restricted to the ODD pins. When a single ended connection is being used, the positive input is avaliable on all pins.

Peripherals may be given access to as many buses as desired. For example the ADC may be given access to ABUSA, ABUSB, and ABUSCD allowing it to select any pin on ports A-D. If two peripherals select the same port and pin the ABUS will make both connections simultaneously, effectively connecting the two peripherals together.

Any pin connected to an analog resource should be configured to input DISABLED as described in 24.3.1 Pin Configuration

The process for configuring an analog peripheral to access a pin through the ABUS is as follows:

- Configure the desired analog port pins to input DISABLED mode in the corresponding GPIO_PORTx_MODEL/H register.
- Configure the corresponding GPIO_xBUSALLOC field to grant access to the desired peripheral on the desired ABUS.
- Configure the analog peripheral to select the desired port and channel as described in the peripheral chapter.

24.3.12.3 Pin Function Tables

This section details the functions and GPIO pins available on the most fully-featured devices in the EFR32xG25 family. Availability of GPIO and signals varies. Refer to the device datasheet for specific peripheral and GPIO availability. Fixed-pin peripheral resources are shown in Table 24.3 GPIO Alternate Function Table on page 797, ABUS routing options are listed in Table 24.4 ABUS Routing Table on page 798, and DBUS routing options are listed in Table 24.5 DBUS Routing Table on page 799

Table 24.3. GPIO Alternate Function Table

GPIO	Alternate Functions	QFN56 / Standard Package	QFN56 / Clock Out Package
PA01	GPIO.SWCLK	Yes	Yes
PA02	GPIO.SWDIO	Yes	Yes
PA03	GPIO.SWV	Yes	Yes
	GPIO.TDO	Yes	Yes
	GPIO.TRACEDATA0	Yes	Yes
	LESENSE.EN_0	Yes	Yes
PA04	GPIO.TDI	Yes	Yes
	GPIO.TRACECLK	Yes	Yes
	LESENSE.EN_1	Yes	Yes
PA05	ETAMPDET.ETAMPIN0	Yes	Yes
	GPIO.TRACEDATA1	Yes	Yes
	GPIO.EM4WU0	Yes	Yes
	LESENSE.EN_2	Yes	Yes
PA06	ETAMPDET.ETAMPOUT0	Yes	Yes
	GPIO.TRACEDATA2	Yes	Yes
PA07	GPIO.TRACEDATA3	Yes	Yes
PA11	GPIO.EM4WU1	Yes	Yes
PB00	VDAC0.CH0_MAIN_OUT	Yes	Yes
PB01	GPIO.EM4WU3	Yes	Yes
	VDAC0.CH1_MAIN_OUT	Yes	Yes
PB03	GPIO.EM4WU4	Yes	Yes
PC00	GPIO.EM4WU6	Yes	Yes
PC04	RAC.FEM_DATA0	Yes	Yes
PC05	GPIO.EM4WU7	Yes	Yes
	RAC.FEM_DATA1	Yes	Yes
PC06	RAC.FEM_DATA2	Yes	Yes
PC07	GPIO.EM4WU8	Yes	Yes
	RAC.AUXADC_IN6_SHIM_EN	Yes	Yes
	RAC.FEM_DATA3	Yes	Yes
PC08	RAC.AUXADC_IN8_SHIM_EN	Yes	Yes

GPIO	Alternate Functions	QFN56 / Standard Package	QFN56 / Clock Out Package
PC09	GPIO.THMSW_EN		Yes
	GPIO.THMSW_HALFSWITCH		Yes
PC10	GPIO.THMSW_EN	Yes	
	GPIO.THMSW_HALFSWITCH	Yes	
PD00	LFXO.LFXTAL_O	Yes	Yes
PD01	LFXO.LFXTAL_I	Yes	Yes
	LFXO.LF_EXTCLK	Yes	Yes
PD02	GPIO.EM4WU9	Yes	Yes
PD04	ETAMPDET.ETAMPOUT1	Yes	Yes
PD05	ETAMPDET.ETAMPIN1	Yes	Yes
	GPIO.EM4WU10	Yes	Yes
PD06	USB.USB_DPLUS	Yes	Yes
PD07	USB.USB_DMINUS	Yes	Yes

Table 24.4. ABUS Routing Table

Peripheral	Signal	PA		PB		PC		PD	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
ACMP0	ana_neg	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ana_pos	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ACMP1	ana_neg	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ana_pos	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IADC0	ana_neg	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ana_pos	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
VDAC0	ch0_abus_out	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ch1_abus_out	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table 24.5. DBUS Routing Table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
ACMP0.DIGOUT	Available	Available	Available	Available
ACMP1.DIGOUT	Available	Available	Available	Available
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1			Available	Available
CMU.CLKOUT2	Available	Available		
EUSART0.CS	Available	Available		
EUSART0.CTS	Available	Available		
EUSART0.RTS	Available	Available		
EUSART0.RX	Available	Available		
EUSART0.SCLK	Available	Available		
EUSART0.TX	Available	Available		
EUSART1.CS	Available	Available	Available	Available
EUSART1.CTS	Available	Available	Available	Available
EUSART1.RTS	Available	Available	Available	Available
EUSART1.RX	Available	Available	Available	Available
EUSART1.SCLK	Available	Available	Available	Available
EUSART1.TX	Available	Available	Available	Available
EUSART2.CS			Available	Available
EUSART2.CTS			Available	Available
EUSART2.RTS			Available	Available
EUSART2.RX			Available	Available
EUSART2.SCLK			Available	Available
EUSART2.TX			Available	Available
EUSART3.CS	Available	Available		
EUSART3.CTS	Available	Available		
EUSART3.RTS	Available	Available		
EUSART3.RX	Available	Available		
EUSART3.SCLK	Available	Available		
EUSART3.TX	Available	Available		
EUSART4.CS			Available	Available
EUSART4.CTS			Available	Available
EUSART4.RTS			Available	Available
EUSART4.RX			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
EUSART4.SCLK			Available	Available
EUSART4.TX			Available	Available
FRC.DCLK			Available	Available
FRC.DFRAME			Available	Available
FRC.DOUT			Available	Available
HFXO0.BUFOUT_REQ_IN_ASYNC	Available	Available		
I2C0.SCL	Available	Available	Available	Available
I2C0.SDA	Available	Available	Available	Available
I2C1.SCL			Available	Available
I2C1.SDA			Available	Available
LESENSE.CH0OUT	Available	Available		
LESENSE.CH10OUT	Available	Available		
LESENSE.CH11OUT	Available	Available		
LESENSE.CH12OUT	Available	Available		
LESENSE.CH13OUT	Available	Available		
LESENSE.CH14OUT	Available	Available		
LESENSE.CH15OUT	Available	Available		
LESENSE.CH1OUT	Available	Available		
LESENSE.CH2OUT	Available	Available		
LESENSE.CH3OUT	Available	Available		
LESENSE.CH4OUT	Available	Available		
LESENSE.CH5OUT	Available	Available		
LESENSE.CH6OUT	Available	Available		
LESENSE.CH7OUT	Available	Available		
LESENSE.CH8OUT	Available	Available		
LESENSE.CH9OUT	Available	Available		
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
MODEM.ANT0	Available	Available	Available	Available
MODEM.ANT1	Available	Available	Available	Available
MODEM.ANT_ROLL_OVER			Available	Available
MODEM.ANT_RR0			Available	Available
MODEM.ANT_RR1			Available	Available
MODEM.ANT_RR2			Available	Available
MODEM.ANT_RR3			Available	Available
MODEM.ANT_RR4			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
MODEM.ANT_RR5			Available	Available
MODEM.ANT_SW_EN			Available	Available
MODEM.ANT_SW_US			Available	Available
MODEM.ANT_TRIG			Available	Available
MODEM.ANT_TRIG_STOP			Available	Available
MODEM.DCLK	Available	Available		
MODEM.DIN	Available	Available		
MODEM.DOUT	Available	Available		
PCNT0.S0IN	Available	Available		
PCNT0.S1IN	Available	Available		
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		
PRS.ASYNCH10			Available	Available
PRS.ASYNCH11			Available	Available
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.SYNCH0	Available	Available	Available	Available
PRS.SYNCH1	Available	Available	Available	Available
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available
TIMER0.CDTI1	Available	Available	Available	Available
TIMER0.CDTI2	Available	Available	Available	Available
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available		
TIMER2.CC1	Available	Available		
TIMER2.CC2	Available	Available		
TIMER2.CDTI0	Available	Available		
TIMER2.CDTI1	Available	Available		
TIMER2.CDTI2	Available	Available		
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available
TIMER3.CC2			Available	Available
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available
TIMER4.CC0	Available	Available		
TIMER4.CC1	Available	Available		
TIMER4.CC2	Available	Available		
TIMER4.CDTI0	Available	Available		
TIMER4.CDTI1	Available	Available		
TIMER4.CDTI2	Available	Available		
TIMER5.CC0			Available	Available
TIMER5.CC1			Available	Available
TIMER5.CC2			Available	Available
TIMER5.CDTI0			Available	Available
TIMER5.CDTI1			Available	Available
TIMER5.CDTI2			Available	Available
TIMER6.CC0	Available	Available		
TIMER6.CC1	Available	Available		
TIMER6.CC2	Available	Available		
TIMER6.CDTI0	Available	Available		
TIMER6.CDTI1	Available	Available		
TIMER6.CDTI2	Available	Available		
TIMER7.CC0			Available	Available
TIMER7.CC1			Available	Available
TIMER7.CC2			Available	Available
TIMER7.CDTI0			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
TIMER7.CDTI1			Available	Available
TIMER7.CDTI2			Available	Available
USB.USB_VBUS_SENSE	Available	Available	Available	Available

24.4 Synchronization

To avoid metastability in synchronous logic connected to the pins, all inputs are synchronized with double flip-flops. The flip-flops for the input data run on the selected APB clock for the GPIO module (PCLK). Consequently, when a pin changes state, the change will propagate to GPIO_Px_DIN after two 2 PCLK cycles. Synchronization (also running on the PCLK) is also added for interrupt input. To save power when the external interrupts are not used, the synchronization flip-flops for these can be turned off by clearing the EXTINT field in the GPIO_IEN register.

24.5 GPIO Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	GPIO_IPVERSION	R	Main
0x030	GPIO_PORTA_CTRL	RW	Port Control
0x034	GPIO_PORTA_MODEL	RW	Mode Low
0x03C	GPIO_PORTA_MODEH	RW	Mode High
0x040	GPIO_PORTA_DOUT	RW	Data Out
0x044	GPIO_PORTA_DIN	RH	Data in
0x060	GPIO_PORTB_CTRL	RW	Port Control
0x064	GPIO_PORTB_MODEL	RW	Mode Low
0x06C	GPIO_PORTB_MODEH	RW	Mode High
0x070	GPIO_PORTB_DOUT	RW	Data Out
0x074	GPIO_PORTB_DIN	RH	Data in
0x090	GPIO_PORTC_CTRL	RW	Port Control
0x094	GPIO_PORTC_MODEL	RW	Mode Low
0x09C	GPIO_PORTC_MODEH	RW	Mode High
0x0A0	GPIO_PORTC_DOUT	RW	Data Out
0x0A4	GPIO_PORTC_DIN	RH	Data in
0x0C0	GPIO_PORTD_CTRL	RW	Port Control
0x0C4	GPIO_PORTD_MODEL	RW	Mode Low
0x0D0	GPIO_PORTD_DOUT	RW	Data Out
0x0D4	GPIO_PORTD_DIN	RH	Data in
0x200	GPIO_LOCK	W	Lock Register
0x210	GPIO_GPIOLOCKSTATUS	RH	Lock Status
0x220	GPIO_ABUSALLOC	RW	A Bus Allocation
0x224	GPIO_BBUSALLOC	RW	B Bus Allocation
0x228	GPIO_CDBUSALLOC	RW	CD Bus Allocation
0x230	GPIO_AODD0SWITCH	RW	AODD0 Switch Register
0x234	GPIO_AODD1SWITCH	RW	AODD1 Switch Register
0x238	GPIO_AEVEN0SWITCH	RW	AEVEN0 Switch Register
0x23C	GPIO_AEVEN1SWITCH	RW	AEVEN1 Switch Register
0x240	GPIO_BODD0SWITCH	RW	BODD0 Switch Register
0x244	GPIO_BODD1SWITCH	RW	BODD1 Switch Register
0x248	GPIO_BEVEN0SWITCH	RW	BEVEN0 Switch Register
0x24C	GPIO_BEVEN1SWITCH	RW	BEVEN1 Switch Register
0x250	GPIO_CDODD0SWITCH	RW	CDODD0 Switch Register
0x254	GPIO_CDODD1SWITCH	RW	CDODD1 Switch Register

Offset	Name	Type	Description
0x258	GPIO_CDEVEN0SWITCH	RW	CDEVEN0 Switch Register
0x25C	GPIO_CDEVEN1SWITCH	RW	CDEVEN1 Switch Register
0x300	GPIO_EXTIPSELL	RW	External Interrupt Port Select Low
0x304	GPIO_EXTIPSELH	RW	External Interrupt Port Select High
0x308	GPIO_EXTIPINSELL	RW	External Interrupt Pin Select Low
0x30C	GPIO_EXTIPINSELH	RW	External Interrupt Pin Select High
0x310	GPIO_EXTIRISE	RW	External Interrupt Rising Edge Trigger
0x314	GPIO_EXTIFALL	RW	External Interrupt Falling Edge Trigger
0x320	GPIO_IF	RWH INTFLAG	Interrupt Flag
0x324	GPIO_IEN	RW	Interrupt Enable
0x32C	GPIO_EM4WUEN	RW	EM4 Wakeup Enable
0x330	GPIO_EM4WUPOL	RW	EM4 Wakeup Polarity
0x340	GPIO_DBGROUTEPEN	RW	Debugger Route Pin Enable
0x344	GPIO_TRACEROUTEPEN	RW	Trace Route Pin Enable
0x348	GPIO_FEMROUTEPEN	RW	FEM Route Pin Enable
0x350	GPIO_ACMP0_ROUTEEN	RW	ACMP0 Pin Enable
0x354	GPIO_ACMP0_ACMPOUT-ROUTE	RW	ACMPOUT Port/Pin Select
0x35C	GPIO_ACMP1_ROUTEEN	RW	ACMP1 Pin Enable
0x360	GPIO_ACMP1_ACMPOUT-ROUTE	RW	ACMPOUT Port/Pin Select
0x368	GPIO_CMU_ROUTEEN	RW	CMU Pin Enable
0x36C	GPIO_CMU_CLKIN0ROUTE	RW	CLKIN0 Port/Pin Select
0x370	GPIO_CMU_CLKOUT0ROUTE	RW	CLKOUT0 Port/Pin Select
0x374	GPIO_CMU_CLKOUT1ROUTE	RW	CLKOUT1 Port/Pin Select
0x378	GPIO_CMU_CLKOUT2ROUTE	RW	CLKOUT2 Port/Pin Select
0x384	GPIO_DCDC_ROUTEEN	RW	DCDC Pin Enable
0x394	GPIO_EUSART0_ROUTEEN	RW	EUSART0 Pin Enable
0x398	GPIO_EUSART0_CSROUTE	RW	CS Port/Pin Select
0x39C	GPIO_EUSART0_CTSROUTE	RW	CTS Port/Pin Select
0x3A0	GPIO_EUSART0_RTSROUTE	RW	RTS Port/Pin Select
0x3A4	GPIO_EUSART0_RXROUTE	RW	RX Port/Pin Select
0x3A8	GPIO_EUSART0_SCLKROUTE	RW	SCLK Port/Pin Select
0x3AC	GPIO_EUSART0_TXROUTE	RW	TX Port/Pin Select
0x3B4	GPIO_EUSART1_ROUTEEN	RW	EUSART1 Pin Enable
0x3B8	GPIO_EUSART1_CSROUTE	RW	CS Port/Pin Select
0x3BC	GPIO_EUSART1_CTSROUTE	RW	CTS Port/Pin Select
0x3C0	GPIO_EUSART1_RTSROUTE	RW	RTS Port/Pin Select

Offset	Name	Type	Description
0x3C4	GPIO_EUSART1_RXROUTE	RW	RX Port/Pin Select
0x3C8	GPIO_EUSART1_SCLKROUTE	RW	SCLK Port/Pin Select
0x3CC	GPIO_EUSART1_TXROUTE	RW	TX Port/Pin Select
0x3D4	GPIO_EUSART2_ROUTEEN	RW	EUSART2 Pin Enable
0x3D8	GPIO_EUSART2_CSROUTE	RW	CS Port/Pin Select
0x3DC	GPIO_EUSART2_CTSROUTE	RW	CTS Port/Pin Select
0x3E0	GPIO_EUSART2_RTSROUTE	RW	RTS Port/Pin Select
0x3E4	GPIO_EUSART2_RXROUTE	RW	RX Port/Pin Select
0x3E8	GPIO_EUSART2_SCLKROUTE	RW	SCLK Port/Pin Select
0x3EC	GPIO_EUSART2_TXROUTE	RW	TX Port/Pin Select
0x3F4	GPIO_EUSART3_ROUTEEN	RW	EUSART3 Pin Enable
0x3F8	GPIO_EUSART3_CSROUTE	RW	CS Port/Pin Select
0x3FC	GPIO_EUSART3_CTSROUTE	RW	CTS Port/Pin Select
0x400	GPIO_EUSART3_RTSROUTE	RW	RTS Port/Pin Select
0x404	GPIO_EUSART3_RXROUTE	RW	RX Port/Pin Select
0x408	GPIO_EUSART3_SCLKROUTE	RW	SCLK Port/Pin Select
0x40C	GPIO_EUSART3_TXROUTE	RW	TX Port/Pin Select
0x414	GPIO_EUSART4_ROUTEEN	RW	EUSART4 Pin Enable
0x418	GPIO_EUSART4_CSROUTE	RW	CS Port/Pin Select
0x41C	GPIO_EUSART4_CTSROUTE	RW	CTS Port/Pin Select
0x420	GPIO_EUSART4_RTSROUTE	RW	RTS Port/Pin Select
0x424	GPIO_EUSART4_RXROUTE	RW	RX Port/Pin Select
0x428	GPIO_EUSART4_SCLKROUTE	RW	SCLK Port/Pin Select
0x42C	GPIO_EUSART4_TXROUTE	RW	TX Port/Pin Select
0x434	GPIO_FRC_ROUTEEN	RW	FRC Pin Enable
0x438	GPIO_FRC_DCLKROUTE	RW	DCLK Port/Pin Select
0x43C	GPIO_FRC_DFRAMEROUTE	RW	DFRAME Port/Pin Select
0x440	GPIO_FRC_DOUTROUTE	RW	DOUT Port/Pin Select
0x448	GPIO_I2C0_ROUTEEN	RW	I2C0 Pin Enable
0x44C	GPIO_I2C0_SCLROUTE	RW	SCL Port/Pin Select
0x450	GPIO_I2C0_SDAROUTE	RW	SDA Port/Pin Select
0x458	GPIO_I2C1_ROUTEEN	RW	I2C1 Pin Enable
0x45C	GPIO_I2C1_SCLROUTE	RW	SCL Port/Pin Select
0x460	GPIO_I2C1_SDAROUTE	RW	SDA Port/Pin Select
0x468	GPIO_LESENSE_ROUTEEN	RW	LESENSE Pin Enable
0x46C	GPIO_LESENSE_CH0OUT-ROUTE	RW	CH0OUT Port/Pin Select

Offset	Name	Type	Description
0x470	GPIO_LESENSE_CH1OUT-ROUTE	RW	CH1OUT Port/Pin Select
0x474	GPIO_LESENSE_CH2OUT-ROUTE	RW	CH2OUT Port/Pin Select
0x478	GPIO_LESENSE_CH3OUT-ROUTE	RW	CH3OUT Port/Pin Select
0x47C	GPIO_LESENSE_CH4OUT-ROUTE	RW	CH4OUT Port/Pin Select
0x480	GPIO_LESENSE_CH5OUT-ROUTE	RW	CH5OUT Port/Pin Select
0x484	GPIO_LESENSE_CH6OUT-ROUTE	RW	CH6OUT Port/Pin Select
0x488	GPIO_LESENSE_CH7OUT-ROUTE	RW	CH7OUT Port/Pin Select
0x48C	GPIO_LESENSE_CH8OUT-ROUTE	RW	CH8OUT Port/Pin Select
0x490	GPIO_LESENSE_CH9OUT-ROUTE	RW	CH9OUT Port/Pin Select
0x494	GPIO_LESENSE_CH10OUT-ROUTE	RW	CH10OUT Port/Pin Select
0x498	GPIO_LESENSE_CH11OUT-ROUTE	RW	CH11OUT Port/Pin Select
0x49C	GPIO_LESENSE_CH12OUT-ROUTE	RW	CH12OUT Port/Pin Select
0x4A0	GPIO_LESENSE_CH13OUT-ROUTE	RW	CH13OUT Port/Pin Select
0x4A4	GPIO_LESENSE_CH14OUT-ROUTE	RW	CH14OUT Port/Pin Select
0x4A8	GPIO_LESENSE_CH15OUT-ROUTE	RW	CH15OUT Port/Pin Select
0x4B0	GPIO_LETIMER_ROUTEEN	RW	LETIMER Pin Enable
0x4B4	GPIO_LETIMER_OUT0ROUTE	RW	OUT0 Port/Pin Select
0x4B8	GPIO_LETIMER_OUT1ROUTE	RW	OUT1 Port/Pin Select
0x4C0	GPIO_MODEM_ROUTEEN	RW	MODEM Pin Enable
0x4C4	GPIO_MODEM_ANT0ROUTE	RW	ANT0 Port/Pin Select
0x4C8	GPIO_MODEM_ANT1ROUTE	RW	ANT1 Port/Pin Select
0x4CC	GPIO_MODEM_ANTROLLO-VERROUTE	RW	ANTROLLOVER Port/Pin Select
0x4D0	GPIO_MO-DEM_ANTRR0ROUTE	RW	ANTRR0 Port/Pin Select
0x4D4	GPIO_MO-DEM_ANTRR1ROUTE	RW	ANTRR1 Port/Pin Select
0x4D8	GPIO_MO-DEM_ANTRR2ROUTE	RW	ANTRR2 Port/Pin Select

Offset	Name	Type	Description
0x4DC	GPIO_MODEM_ANTRR3ROUTE	RW	ANTRR3 Port/Pin Select
0x4E0	GPIO_MODEM_ANTRR4ROUTE	RW	ANTRR4 Port/Pin Select
0x4E4	GPIO_MODEM_ANTRR5ROUTE	RW	ANTRR5 Port/Pin Select
0x4E8	GPIO_MODEM_ANTSWENROUTE	RW	ANTSWEN Port/Pin Select
0x4EC	GPIO_MODEM_ANTSWUSROUTE	RW	ANTSWUS Port/Pin Select
0x4F0	GPIO_MODEM_ANTTRIGROUTE	RW	ANTTRIG Port/Pin Select
0x4F4	GPIO_MODEM_ANTTRIGSTOPROUTE	RW	ANTTRIGSTOP Port/Pin Select
0x4F8	GPIO_MODEM_DCLKROUTE	RW	DCLK Port/Pin Select
0x4FC	GPIO_MODEM_DINROUTE	RW	DIN Port/Pin Select
0x500	GPIO_MODEM_DOUTROUTE	RW	DOUT Port/Pin Select
0x50C	GPIO_PCNT0_S0INROUTE	RW	S0IN Port/Pin Select
0x510	GPIO_PCNT0_S1INROUTE	RW	S1IN Port/Pin Select
0x518	GPIO_PRS0_ROUTEEN	RW	PRS0 Pin Enable
0x51C	GPIO_PRS0_ASYNCH0ROUTE	RW	ASYNCH0 Port/Pin Select
0x520	GPIO_PRS0_ASYNCH1ROUTE	RW	ASYNCH1 Port/Pin Select
0x524	GPIO_PRS0_ASYNCH2ROUTE	RW	ASYNCH2 Port/Pin Select
0x528	GPIO_PRS0_ASYNCH3ROUTE	RW	ASYNCH3 Port/Pin Select
0x52C	GPIO_PRS0_ASYNCH4ROUTE	RW	ASYNCH4 Port/Pin Select
0x530	GPIO_PRS0_ASYNCH5ROUTE	RW	ASYNCH5 Port/Pin Select
0x534	GPIO_PRS0_ASYNCH6ROUTE	RW	ASYNCH6 Port/Pin Select
0x538	GPIO_PRS0_ASYNCH7ROUTE	RW	ASYNCH7 Port/Pin Select
0x53C	GPIO_PRS0_ASYNCH8ROUTE	RW	ASYNCH8 Port/Pin Select
0x540	GPIO_PRS0_ASYNCH9ROUTE	RW	ASYNCH9 Port/Pin Select
0x544	GPIO_PRS0_ASYNCH10ROUTE	RW	ASYNCH10 Port/Pin Select
0x548	GPIO_PRS0_ASYNCH11ROUTE	RW	ASYNCH11 Port/Pin Select
0x54C	GPIO_PRS0_SYNCH0ROUTE	RW	SYNCH0 Port/Pin Select
0x550	GPIO_PRS0_SYNCH1ROUTE	RW	SYNCH1 Port/Pin Select
0x554	GPIO_PRS0_SYNCH2ROUTE	RW	SYNCH2 Port/Pin Select
0x558	GPIO_PRS0_SYNCH3ROUTE	RW	SYNCH3 Port/Pin Select
0x5C0	GPIO_SYXO0_BUFOUTREQINASYNCROUTE	RW	BUFOUTREQINASYNC Port/Pin Select
0x5C8	GPIO_TIMER0_ROUTEEN	RW	TIMER0 Pin Enable

Offset	Name	Type	Description
0x5CC	GPIO_TIMER0_CC0ROUTE	RW	CC0 Port/Pin Select
0x5D0	GPIO_TIMER0_CC1ROUTE	RW	CC1 Port/Pin Select
0x5D4	GPIO_TIMER0_CC2ROUTE	RW	CC2 Port/Pin Select
0x5D8	GPIO_TIMER0_CDTI0ROUTE	RW	CDTI0 Port/Pin Select
0x5DC	GPIO_TIMER0_CDTI1ROUTE	RW	CDTI1 Port/Pin Select
0x5E0	GPIO_TIMER0_CDTI2ROUTE	RW	CDTI2 Port/Pin Select
0x5E8	GPIO_TIMER1_ROUTEEN	RW	TIMER1 Pin Enable
0x5EC	GPIO_TIMER1_CC0ROUTE	RW	CC0 Port/Pin Select
0x5F0	GPIO_TIMER1_CC1ROUTE	RW	CC1 Port/Pin Select
0x5F4	GPIO_TIMER1_CC2ROUTE	RW	CC2 Port/Pin Select
0x5F8	GPIO_TIMER1_CDTI0ROUTE	RW	CDTI0 Port/Pin Select
0x5FC	GPIO_TIMER1_CDTI1ROUTE	RW	CDTI1 Port/Pin Select
0x600	GPIO_TIMER1_CDTI2ROUTE	RW	CDTI2 Port/Pin Select
0x608	GPIO_TIMER2_ROUTEEN	RW	TIMER2 Pin Enable
0x60C	GPIO_TIMER2_CC0ROUTE	RW	CC0 Port/Pin Select
0x610	GPIO_TIMER2_CC1ROUTE	RW	CC1 Port/Pin Select
0x614	GPIO_TIMER2_CC2ROUTE	RW	CC2 Port/Pin Select
0x618	GPIO_TIMER2_CDTI0ROUTE	RW	CDTI0 Port/Pin Select
0x61C	GPIO_TIMER2_CDTI1ROUTE	RW	CDTI1 Port/Pin Select
0x620	GPIO_TIMER2_CDTI2ROUTE	RW	CDTI2 Port/Pin Select
0x628	GPIO_TIMER3_ROUTEEN	RW	TIMER3 Pin Enable
0x62C	GPIO_TIMER3_CC0ROUTE	RW	CC0 Port/Pin Select
0x630	GPIO_TIMER3_CC1ROUTE	RW	CC1 Port/Pin Select
0x634	GPIO_TIMER3_CC2ROUTE	RW	CC2 Port/Pin Select
0x638	GPIO_TIMER3_CDTI0ROUTE	RW	CDTI0 Port/Pin Select
0x63C	GPIO_TIMER3_CDTI1ROUTE	RW	CDTI1 Port/Pin Select
0x640	GPIO_TIMER3_CDTI2ROUTE	RW	CDTI2 Port/Pin Select
0x648	GPIO_TIMER4_ROUTEEN	RW	TIMER4 Pin Enable
0x64C	GPIO_TIMER4_CC0ROUTE	RW	CC0 Port/Pin Select
0x650	GPIO_TIMER4_CC1ROUTE	RW	CC1 Port/Pin Select
0x654	GPIO_TIMER4_CC2ROUTE	RW	CC2 Port/Pin Select
0x658	GPIO_TIMER4_CDTI0ROUTE	RW	CDTI0 Port/Pin Select
0x65C	GPIO_TIMER4_CDTI1ROUTE	RW	CDTI1 Port/Pin Select
0x660	GPIO_TIMER4_CDTI2ROUTE	RW	CDTI2 Port/Pin Select
0x668	GPIO_TIMER5_ROUTEEN	RW	TIMER5 Pin Enable
0x66C	GPIO_TIMER5_CC0ROUTE	RW	CC0 Port/Pin Select
0x670	GPIO_TIMER5_CC1ROUTE	RW	CC1 Port/Pin Select

Offset	Name	Type	Description
0x674	GPIO_TIMER5_CC2ROUTE	RW	CC2 Port/Pin Select
0x678	GPIO_TIMER5_CDTI0ROUTE	RW	CDTI0 Port/Pin Select
0x67C	GPIO_TIMER5_CDTI1ROUTE	RW	CDTI1 Port/Pin Select
0x680	GPIO_TIMER5_CDTI2ROUTE	RW	CDTI2 Port/Pin Select
0x688	GPIO_TIMER6_ROUTEEN	RW	TIMER6 Pin Enable
0x68C	GPIO_TIMER6_CC0ROUTE	RW	CC0 Port/Pin Select
0x690	GPIO_TIMER6_CC1ROUTE	RW	CC1 Port/Pin Select
0x694	GPIO_TIMER6_CC2ROUTE	RW	CC2 Port/Pin Select
0x698	GPIO_TIMER6_CDTI0ROUTE	RW	CDTI0 Port/Pin Select
0x69C	GPIO_TIMER6_CDTI1ROUTE	RW	CDTI1 Port/Pin Select
0x6A0	GPIO_TIMER6_CDTI2ROUTE	RW	CDTI2 Port/Pin Select
0x6A8	GPIO_TIMER7_ROUTEEN	RW	TIMER7 Pin Enable
0x6AC	GPIO_TIMER7_CC0ROUTE	RW	CC0 Port/Pin Select
0x6B0	GPIO_TIMER7_CC1ROUTE	RW	CC1 Port/Pin Select
0x6B4	GPIO_TIMER7_CC2ROUTE	RW	CC2 Port/Pin Select
0x6B8	GPIO_TIMER7_CDTI0ROUTE	RW	CDTI0 Port/Pin Select
0x6BC	GPIO_TIMER7_CDTI1ROUTE	RW	CDTI1 Port/Pin Select
0x6C0	GPIO_TIMER7_CDTI2ROUTE	RW	CDTI2 Port/Pin Select
0x6CC	GPIO_USB_USBVBUSSENSE-ROUTE	RW	USBVBUSSENSE Port/Pin Select
0x1000	GPIO_IPVERSION_SET	R	Main
0x1030	GPIO_PORTA_CTRL_SET	RW	Port Control
0x1034	GPIO_PORTA_MODEL_SET	RW	Mode Low
0x103C	GPIO_PORTA_MODEH_SET	RW	Mode High
0x1040	GPIO_PORTA_DOUT_SET	RW	Data Out
0x1044	GPIO_PORTA_DIN_SET	RH	Data in
0x1060	GPIO_PORTB_CTRL_SET	RW	Port Control
0x1064	GPIO_PORTB_MODEL_SET	RW	Mode Low
0x106C	GPIO_PORTB_MODEH_SET	RW	Mode High
0x1070	GPIO_PORTB_DOUT_SET	RW	Data Out
0x1074	GPIO_PORTB_DIN_SET	RH	Data in
0x1090	GPIO_PORTC_CTRL_SET	RW	Port Control
0x1094	GPIO_PORTC_MODEL_SET	RW	Mode Low
0x109C	GPIO_PORTC_MODEH_SET	RW	Mode High
0x10A0	GPIO_PORTC_DOUT_SET	RW	Data Out
0x10A4	GPIO_PORTC_DIN_SET	RH	Data in
0x10C0	GPIO_PORTD_CTRL_SET	RW	Port Control

Offset	Name	Type	Description
0x10C4	GPIO_PORTD_MODEL_SET	RW	Mode Low
0x10D0	GPIO_PORTD_DOUT_SET	RW	Data Out
0x10D4	GPIO_PORTD_DIN_SET	RH	Data in
0x1200	GPIO_LOCK_SET	W	Lock Register
0x1210	GPIO_GPIOLOCKSTATUS_SET	RH	Lock Status
0x1220	GPIO_ABUSALLOC_SET	RW	A Bus Allocation
0x1224	GPIO_BBUSALLOC_SET	RW	B Bus Allocation
0x1228	GPIO_CDBUSALLOC_SET	RW	CD Bus Allocation
0x1230	GPIO_AODD0SWITCH_SET	RW	AODD0 Switch Register
0x1234	GPIO_AODD1SWITCH_SET	RW	AODD1 Switch Register
0x1238	GPIO_AEVEN0SWITCH_SET	RW	AEVEN0 Switch Register
0x123C	GPIO_AEVEN1SWITCH_SET	RW	AEVEN1 Switch Register
0x1240	GPIO_BODD0SWITCH_SET	RW	BODD0 Switch Register
0x1244	GPIO_BODD1SWITCH_SET	RW	BODD1 Switch Register
0x1248	GPIO_BEVEN0SWITCH_SET	RW	BEVEN0 Switch Register
0x124C	GPIO_BEVEN1SWITCH_SET	RW	BEVEN1 Switch Register
0x1250	GPIO_CDODD0SWITCH_SET	RW	CDODD0 Switch Register
0x1254	GPIO_CDODD1SWITCH_SET	RW	CDODD1 Switch Register
0x1258	GPIO_CDEVEN0SWITCH_SET	RW	CDEVEN0 Switch Register
0x125C	GPIO_CDEVEN1SWITCH_SET	RW	CDEVEN1 Switch Register
0x1300	GPIO_EXTIPSELL_SET	RW	External Interrupt Port Select Low
0x1304	GPIO_EXTIPSELH_SET	RW	External Interrupt Port Select High
0x1308	GPIO_EXTIPINSELL_SET	RW	External Interrupt Pin Select Low
0x130C	GPIO_EXTIPINSELH_SET	RW	External Interrupt Pin Select High
0x1310	GPIO_EXTIRISE_SET	RW	External Interrupt Rising Edge Trigger
0x1314	GPIO_EXTIFALL_SET	RW	External Interrupt Falling Edge Trigger
0x1320	GPIO_IF_SET	RWH INTFLAG	Interrupt Flag
0x1324	GPIO_IEN_SET	RW	Interrupt Enable
0x132C	GPIO_EM4WUEN_SET	RW	EM4 Wakeup Enable
0x1330	GPIO_EM4WUPOL_SET	RW	EM4 Wakeup Polarity
0x1340	GPIO_DBGROUTEPEN_SET	RW	Debugger Route Pin Enable
0x1344	GPIO_TRACEROUTEPEN_SET	RW	Trace Route Pin Enable
0x1348	GPIO_FEMROUTEPEN_SET	RW	FEM Route Pin Enable
0x1350	GPIO_ACMP0_ROUTEEN_SET	RW	ACMP0 Pin Enable
0x1354	GPIO_ACMP0_ACMPOUT-ROUTE_SET	RW	ACMPOUT Port/Pin Select
0x135C	GPIO_ACMP1_ROUTEEN_SET	RW	ACMP1 Pin Enable

Offset	Name	Type	Description
0x1360	GPIO_ACMP1_ACMPOUT-ROUTE_SET	RW	ACMPOUT Port/Pin Select
0x1368	GPIO_CMU_ROUTEEN_SET	RW	CMU Pin Enable
0x136C	GPIO_CMU_CLKIN0ROUTE_SET	RW	CLKIN0 Port/Pin Select
0x1370	GPIO_CMU_CLKOUT0ROUTE_SET	RW	CLKOUT0 Port/Pin Select
0x1374	GPIO_CMU_CLKOUT1ROUTE_SET	RW	CLKOUT1 Port/Pin Select
0x1378	GPIO_CMU_CLKOUT2ROUTE_SET	RW	CLKOUT2 Port/Pin Select
0x1384	GPIO_DCDC_ROUTEEN_SET	RW	DCDC Pin Enable
0x1394	GPIO_EUSART0_ROU-TEEN_SET	RW	EUSART0 Pin Enable
0x1398	GPIO_EU-SART0_CSROUTE_SET	RW	CS Port/Pin Select
0x139C	GPIO_EU-SART0_CTSROUTE_SET	RW	CTS Port/Pin Select
0x13A0	GPIO_EU-SART0_RTSROUTE_SET	RW	RTS Port/Pin Select
0x13A4	GPIO_EU-SART0_RXROUTE_SET	RW	RX Port/Pin Select
0x13A8	GPIO_EU-SART0_SCLKROUTE_SET	RW	SCLK Port/Pin Select
0x13AC	GPIO_EU-SART0_TXROUTE_SET	RW	TX Port/Pin Select
0x13B4	GPIO_EUSART1_ROU-TEEN_SET	RW	EUSART1 Pin Enable
0x13B8	GPIO_EU-SART1_CSROUTE_SET	RW	CS Port/Pin Select
0x13BC	GPIO_EU-SART1_CTSROUTE_SET	RW	CTS Port/Pin Select
0x13C0	GPIO_EU-SART1_RTSROUTE_SET	RW	RTS Port/Pin Select
0x13C4	GPIO_EU-SART1_RXROUTE_SET	RW	RX Port/Pin Select
0x13C8	GPIO_EU-SART1_SCLKROUTE_SET	RW	SCLK Port/Pin Select
0x13CC	GPIO_EU-SART1_TXROUTE_SET	RW	TX Port/Pin Select
0x13D4	GPIO_EUSART2_ROU-TEEN_SET	RW	EUSART2 Pin Enable
0x13D8	GPIO_EU-SART2_CSROUTE_SET	RW	CS Port/Pin Select
0x13DC	GPIO_EU-SART2_CTSROUTE_SET	RW	CTS Port/Pin Select

Offset	Name	Type	Description
0x13E0	GPIO_EUSART2_RTSROUTE_SET	RW	RTS Port/Pin Select
0x13E4	GPIO_EUSART2_RXROUTE_SET	RW	RX Port/Pin Select
0x13E8	GPIO_EUSART2_SCLKROUTE_SET	RW	SCLK Port/Pin Select
0x13EC	GPIO_EUSART2_TXROUTE_SET	RW	TX Port/Pin Select
0x13F4	GPIO_EUSART3_ROUTEEN_SET	RW	EUSART3 Pin Enable
0x13F8	GPIO_EUSART3_CSROUTE_SET	RW	CS Port/Pin Select
0x13FC	GPIO_EUSART3_CTSROUTE_SET	RW	CTS Port/Pin Select
0x1400	GPIO_EUSART3_RTSROUTE_SET	RW	RTS Port/Pin Select
0x1404	GPIO_EUSART3_RXROUTE_SET	RW	RX Port/Pin Select
0x1408	GPIO_EUSART3_SCLKROUTE_SET	RW	SCLK Port/Pin Select
0x140C	GPIO_EUSART3_TXROUTE_SET	RW	TX Port/Pin Select
0x1414	GPIO_EUSART4_ROUTEEN_SET	RW	EUSART4 Pin Enable
0x1418	GPIO_EUSART4_CSROUTE_SET	RW	CS Port/Pin Select
0x141C	GPIO_EUSART4_CTSROUTE_SET	RW	CTS Port/Pin Select
0x1420	GPIO_EUSART4_RTSROUTE_SET	RW	RTS Port/Pin Select
0x1424	GPIO_EUSART4_RXROUTE_SET	RW	RX Port/Pin Select
0x1428	GPIO_EUSART4_SCLKROUTE_SET	RW	SCLK Port/Pin Select
0x142C	GPIO_EUSART4_TXROUTE_SET	RW	TX Port/Pin Select
0x1434	GPIO_FRC_ROUTEEN_SET	RW	FRC Pin Enable
0x1438	GPIO_FRC_DCLKROUTE_SET	RW	DCLK Port/Pin Select
0x143C	GPIO_FRC_DFRAMEROUTE_SET	RW	DFRAME Port/Pin Select
0x1440	GPIO_FRC_DOUTROUTE_SET	RW	DOUT Port/Pin Select
0x1448	GPIO_I2C0_ROUTEEN_SET	RW	I2C0 Pin Enable
0x144C	GPIO_I2C0_SCLROUTE_SET	RW	SCL Port/Pin Select
0x1450	GPIO_I2C0_SDAROUTE_SET	RW	SDA Port/Pin Select
0x1458	GPIO_I2C1_ROUTEEN_SET	RW	I2C1 Pin Enable

Offset	Name	Type	Description
0x145C	GPIO_I2C1_SCLROUTE_SET	RW	SCL Port/Pin Select
0x1460	GPIO_I2C1_SDAROUTE_SET	RW	SDA Port/Pin Select
0x1468	GPIO_LESENSE_ROU-TEEN_SET	RW	LESENSE Pin Enable
0x146C	GPIO_LESENSE_CH0OUT-ROUTE_SET	RW	CH0OUT Port/Pin Select
0x1470	GPIO_LESENSE_CH1OUT-ROUTE_SET	RW	CH1OUT Port/Pin Select
0x1474	GPIO_LESENSE_CH2OUT-ROUTE_SET	RW	CH2OUT Port/Pin Select
0x1478	GPIO_LESENSE_CH3OUT-ROUTE_SET	RW	CH3OUT Port/Pin Select
0x147C	GPIO_LESENSE_CH4OUT-ROUTE_SET	RW	CH4OUT Port/Pin Select
0x1480	GPIO_LESENSE_CH5OUT-ROUTE_SET	RW	CH5OUT Port/Pin Select
0x1484	GPIO_LESENSE_CH6OUT-ROUTE_SET	RW	CH6OUT Port/Pin Select
0x1488	GPIO_LESENSE_CH7OUT-ROUTE_SET	RW	CH7OUT Port/Pin Select
0x148C	GPIO_LESENSE_CH8OUT-ROUTE_SET	RW	CH8OUT Port/Pin Select
0x1490	GPIO_LESENSE_CH9OUT-ROUTE_SET	RW	CH9OUT Port/Pin Select
0x1494	GPIO_LESENSE_CH10OUT-ROUTE_SET	RW	CH10OUT Port/Pin Select
0x1498	GPIO_LESENSE_CH11OUT-ROUTE_SET	RW	CH11OUT Port/Pin Select
0x149C	GPIO_LESENSE_CH12OUT-ROUTE_SET	RW	CH12OUT Port/Pin Select
0x14A0	GPIO_LESENSE_CH13OUT-ROUTE_SET	RW	CH13OUT Port/Pin Select
0x14A4	GPIO_LESENSE_CH14OUT-ROUTE_SET	RW	CH14OUT Port/Pin Select
0x14A8	GPIO_LESENSE_CH15OUT-ROUTE_SET	RW	CH15OUT Port/Pin Select
0x14B0	GPIO_LETIMER_ROU-TEEN_SET	RW	LETIMER Pin Enable
0x14B4	GPIO_LETIM-ER_OUT0ROUTE_SET	RW	OUT0 Port/Pin Select
0x14B8	GPIO_LETIM-ER_OUT1ROUTE_SET	RW	OUT1 Port/Pin Select
0x14C0	GPIO_MODEM_ROUTEEN_SET	RW	MODEM Pin Enable
0x14C4	GPIO_MO-DEM_ANT0ROUTE_SET	RW	ANT0 Port/Pin Select

Offset	Name	Type	Description
0x14C8	GPIO_MODEM_ANT1ROUTE_SET	RW	ANT1 Port/Pin Select
0x14CC	GPIO_MODEM_ANTROLLOVERROUTE_SET	RW	ANTROLLOVER Port/Pin Select
0x14D0	GPIO_MODEM_ANTRR0ROUTE_SET	RW	ANTRR0 Port/Pin Select
0x14D4	GPIO_MODEM_ANTRR1ROUTE_SET	RW	ANTRR1 Port/Pin Select
0x14D8	GPIO_MODEM_ANTRR2ROUTE_SET	RW	ANTRR2 Port/Pin Select
0x14DC	GPIO_MODEM_ANTRR3ROUTE_SET	RW	ANTRR3 Port/Pin Select
0x14E0	GPIO_MODEM_ANTRR4ROUTE_SET	RW	ANTRR4 Port/Pin Select
0x14E4	GPIO_MODEM_ANTRR5ROUTE_SET	RW	ANTRR5 Port/Pin Select
0x14E8	GPIO_MODEM_ANTSWENROUTE_SET	RW	ANTSWEN Port/Pin Select
0x14EC	GPIO_MODEM_ANTSWUSROUTE_SET	RW	ANTSWUS Port/Pin Select
0x14F0	GPIO_MODEM_ANTTRIGROUTE_SET	RW	ANTTRIG Port/Pin Select
0x14F4	GPIO_MODEM_ANTTRIGSTOPROUTE_SET	RW	ANTTRIGSTOP Port/Pin Select
0x14F8	GPIO_MODEM_DCLKROUTE_SET	RW	DCLK Port/Pin Select
0x14FC	GPIO_MODEM_DINROUTE_SET	RW	DIN Port/Pin Select
0x1500	GPIO_MODEM_DOUTROUTE_SET	RW	DOUT Port/Pin Select
0x150C	GPIO_PCNT0_S0INROUTE_SET	RW	S0IN Port/Pin Select
0x1510	GPIO_PCNT0_S1INROUTE_SET	RW	S1IN Port/Pin Select
0x1518	GPIO_PRS0_ROUTEEN_SET	RW	PRS0 Pin Enable
0x151C	GPIO_PRS0_ASYNCH0ROUTE_SET	RW	ASYNCH0 Port/Pin Select
0x1520	GPIO_PRS0_ASYNCH1ROUTE_SET	RW	ASYNCH1 Port/Pin Select
0x1524	GPIO_PRS0_ASYNCH2ROUTE_SET	RW	ASYNCH2 Port/Pin Select
0x1528	GPIO_PRS0_ASYNCH3ROUTE_SET	RW	ASYNCH3 Port/Pin Select
0x152C	GPIO_PRS0_ASYNCH4ROUTE_SET	RW	ASYNCH4 Port/Pin Select
0x1530	GPIO_PRS0_ASYNCH5ROUTE_SET	RW	ASYNCH5 Port/Pin Select

Offset	Name	Type	Description
0x1534	GPIO_PRS0_ASYNCH6ROUTE_SET	RW	ASYNCH6 Port/Pin Select
0x1538	GPIO_PRS0_ASYNCH7ROUTE_SET	RW	ASYNCH7 Port/Pin Select
0x153C	GPIO_PRS0_ASYNCH8ROUTE_SET	RW	ASYNCH8 Port/Pin Select
0x1540	GPIO_PRS0_ASYNCH9ROUTE_SET	RW	ASYNCH9 Port/Pin Select
0x1544	GPIO_PRS0_ASYNCH10ROUTE_SET	RW	ASYNCH10 Port/Pin Select
0x1548	GPIO_PRS0_ASYNCH11ROUTE_SET	RW	ASYNCH11 Port/Pin Select
0x154C	GPIO_PRS0_SYNCH0ROUTE_SET	RW	SYNCH0 Port/Pin Select
0x1550	GPIO_PRS0_SYNCH1ROUTE_SET	RW	SYNCH1 Port/Pin Select
0x1554	GPIO_PRS0_SYNCH2ROUTE_SET	RW	SYNCH2 Port/Pin Select
0x1558	GPIO_PRS0_SYNCH3ROUTE_SET	RW	SYNCH3 Port/Pin Select
0x15C0	GPIO_SYXO0_BUFOUTREQINASYNCROUTE_SET	RW	BUFOUTREQINASYNC Port/Pin Select
0x15C8	GPIO_TIMER0_ROUTEEN_SET	RW	TIMER0 Pin Enable
0x15CC	GPIO_TIMER0_CC0ROUTE_SET	RW	CC0 Port/Pin Select
0x15D0	GPIO_TIMER0_CC1ROUTE_SET	RW	CC1 Port/Pin Select
0x15D4	GPIO_TIMER0_CC2ROUTE_SET	RW	CC2 Port/Pin Select
0x15D8	GPIO_TIMER0_CDTI0ROUTE_SET	RW	CDTI0 Port/Pin Select
0x15DC	GPIO_TIMER0_CDTI1ROUTE_SET	RW	CDTI1 Port/Pin Select
0x15E0	GPIO_TIMER0_CDTI2ROUTE_SET	RW	CDTI2 Port/Pin Select
0x15E8	GPIO_TIMER1_ROUTEEN_SET	RW	TIMER1 Pin Enable
0x15EC	GPIO_TIMER1_CC0ROUTE_SET	RW	CC0 Port/Pin Select
0x15F0	GPIO_TIMER1_CC1ROUTE_SET	RW	CC1 Port/Pin Select
0x15F4	GPIO_TIMER1_CC2ROUTE_SET	RW	CC2 Port/Pin Select
0x15F8	GPIO_TIMER1_CDTI0ROUTE_SET	RW	CDTI0 Port/Pin Select
0x15FC	GPIO_TIMER1_CDTI1ROUTE_SET	RW	CDTI1 Port/Pin Select

Offset	Name	Type	Description
0x1600	GPIO_TIMER1_CDTI2ROUTE_SET	RW	CDTI2 Port/Pin Select
0x1608	GPIO_TIMER2_ROUTEEN_SET	RW	TIMER2 Pin Enable
0x160C	GPIO_TIMER2_CC0ROUTE_SET	RW	CC0 Port/Pin Select
0x1610	GPIO_TIMER2_CC1ROUTE_SET	RW	CC1 Port/Pin Select
0x1614	GPIO_TIMER2_CC2ROUTE_SET	RW	CC2 Port/Pin Select
0x1618	GPIO_TIMER2_CDTI0ROUTE_SET	RW	CDTI0 Port/Pin Select
0x161C	GPIO_TIMER2_CDTI1ROUTE_SET	RW	CDTI1 Port/Pin Select
0x1620	GPIO_TIMER2_CDTI2ROUTE_SET	RW	CDTI2 Port/Pin Select
0x1628	GPIO_TIMER3_ROUTEEN_SET	RW	TIMER3 Pin Enable
0x162C	GPIO_TIMER3_CC0ROUTE_SET	RW	CC0 Port/Pin Select
0x1630	GPIO_TIMER3_CC1ROUTE_SET	RW	CC1 Port/Pin Select
0x1634	GPIO_TIMER3_CC2ROUTE_SET	RW	CC2 Port/Pin Select
0x1638	GPIO_TIMER3_CDTI0ROUTE_SET	RW	CDTI0 Port/Pin Select
0x163C	GPIO_TIMER3_CDTI1ROUTE_SET	RW	CDTI1 Port/Pin Select
0x1640	GPIO_TIMER3_CDTI2ROUTE_SET	RW	CDTI2 Port/Pin Select
0x1648	GPIO_TIMER4_ROUTEEN_SET	RW	TIMER4 Pin Enable
0x164C	GPIO_TIMER4_CC0ROUTE_SET	RW	CC0 Port/Pin Select
0x1650	GPIO_TIMER4_CC1ROUTE_SET	RW	CC1 Port/Pin Select
0x1654	GPIO_TIMER4_CC2ROUTE_SET	RW	CC2 Port/Pin Select
0x1658	GPIO_TIMER4_CDTI0ROUTE_SET	RW	CDTI0 Port/Pin Select
0x165C	GPIO_TIMER4_CDTI1ROUTE_SET	RW	CDTI1 Port/Pin Select
0x1660	GPIO_TIMER4_CDTI2ROUTE_SET	RW	CDTI2 Port/Pin Select
0x1668	GPIO_TIMER5_ROUTEEN_SET	RW	TIMER5 Pin Enable
0x166C	GPIO_TIMER5_CC0ROUTE_SET	RW	CC0 Port/Pin Select
0x1670	GPIO_TIMER5_CC1ROUTE_SET	RW	CC1 Port/Pin Select

Offset	Name	Type	Description
0x1674	GPIO_TIMER5_CC2ROUTE_SET	RW	CC2 Port/Pin Select
0x1678	GPIO_TIMER5_CDTI0ROUTE_SET	RW	CDTI0 Port/Pin Select
0x167C	GPIO_TIMER5_CDTI1ROUTE_SET	RW	CDTI1 Port/Pin Select
0x1680	GPIO_TIMER5_CDTI2ROUTE_SET	RW	CDTI2 Port/Pin Select
0x1688	GPIO_TIMER6_ROUTEEN_SET	RW	TIMER6 Pin Enable
0x168C	GPIO_TIMER6_CC0ROUTE_SET	RW	CC0 Port/Pin Select
0x1690	GPIO_TIMER6_CC1ROUTE_SET	RW	CC1 Port/Pin Select
0x1694	GPIO_TIMER6_CC2ROUTE_SET	RW	CC2 Port/Pin Select
0x1698	GPIO_TIMER6_CDTI0ROUTE_SET	RW	CDTI0 Port/Pin Select
0x169C	GPIO_TIMER6_CDTI1ROUTE_SET	RW	CDTI1 Port/Pin Select
0x16A0	GPIO_TIMER6_CDTI2ROUTE_SET	RW	CDTI2 Port/Pin Select
0x16A8	GPIO_TIMER7_ROUTEEN_SET	RW	TIMER7 Pin Enable
0x16AC	GPIO_TIMER7_CC0ROUTE_SET	RW	CC0 Port/Pin Select
0x16B0	GPIO_TIMER7_CC1ROUTE_SET	RW	CC1 Port/Pin Select
0x16B4	GPIO_TIMER7_CC2ROUTE_SET	RW	CC2 Port/Pin Select
0x16B8	GPIO_TIMER7_CDTI0ROUTE_SET	RW	CDTI0 Port/Pin Select
0x16BC	GPIO_TIMER7_CDTI1ROUTE_SET	RW	CDTI1 Port/Pin Select
0x16C0	GPIO_TIMER7_CDTI2ROUTE_SET	RW	CDTI2 Port/Pin Select
0x16CC	GPIO_USB_USBVBUSSENSEROUTE_SET	RW	USBVBUSSENSE Port/Pin Select
0x2000	GPIO_IPVERSION_CLR	R	Main
0x2030	GPIO_PORTA_CTRL_CLR	RW	Port Control
0x2034	GPIO_PORTA_MODEL_CLR	RW	Mode Low
0x203C	GPIO_PORTA_MODEH_CLR	RW	Mode High
0x2040	GPIO_PORTA_DOUT_CLR	RW	Data Out
0x2044	GPIO_PORTA_DIN_CLR	RH	Data in
0x2060	GPIO_PORTB_CTRL_CLR	RW	Port Control
0x2064	GPIO_PORTB_MODEL_CLR	RW	Mode Low

Offset	Name	Type	Description
0x206C	GPIO_PORTB_MODEH_CLR	RW	Mode High
0x2070	GPIO_PORTB_DOUT_CLR	RW	Data Out
0x2074	GPIO_PORTB_DIN_CLR	RH	Data in
0x2090	GPIO_PORTC_CTRL_CLR	RW	Port Control
0x2094	GPIO_PORTC_MODEL_CLR	RW	Mode Low
0x209C	GPIO_PORTC_MODEH_CLR	RW	Mode High
0x20A0	GPIO_PORTC_DOUT_CLR	RW	Data Out
0x20A4	GPIO_PORTC_DIN_CLR	RH	Data in
0x20C0	GPIO_PORTD_CTRL_CLR	RW	Port Control
0x20C4	GPIO_PORTD_MODEL_CLR	RW	Mode Low
0x20D0	GPIO_PORTD_DOUT_CLR	RW	Data Out
0x20D4	GPIO_PORTD_DIN_CLR	RH	Data in
0x2200	GPIO_LOCK_CLR	W	Lock Register
0x2210	GPIO_GPIOLOCKSTATUS_CLR	RH	Lock Status
0x2220	GPIO_ABUSALLOC_CLR	RW	A Bus Allocation
0x2224	GPIO_BBUSALLOC_CLR	RW	B Bus Allocation
0x2228	GPIO_CDBUSALLOC_CLR	RW	CD Bus Allocation
0x2230	GPIO_AODD0SWITCH_CLR	RW	AODD0 Switch Register
0x2234	GPIO_AODD1SWITCH_CLR	RW	AODD1 Switch Register
0x2238	GPIO_AEVEN0SWITCH_CLR	RW	AEVEN0 Switch Register
0x223C	GPIO_AEVEN1SWITCH_CLR	RW	AEVEN1 Switch Register
0x2240	GPIO_BODD0SWITCH_CLR	RW	BODD0 Switch Register
0x2244	GPIO_BODD1SWITCH_CLR	RW	BODD1 Switch Register
0x2248	GPIO_BEVEN0SWITCH_CLR	RW	BEVEN0 Switch Register
0x224C	GPIO_BEVEN1SWITCH_CLR	RW	BEVEN1 Switch Register
0x2250	GPIO_CDODD0SWITCH_CLR	RW	CDODD0 Switch Register
0x2254	GPIO_CDODD1SWITCH_CLR	RW	CDODD1 Switch Register
0x2258	GPIO_CDEVEN0SWITCH_CLR	RW	CDEVEN0 Switch Register
0x225C	GPIO_CDEVEN1SWITCH_CLR	RW	CDEVEN1 Switch Register
0x2300	GPIO_EXTIPSELL_CLR	RW	External Interrupt Port Select Low
0x2304	GPIO_EXTIPSELH_CLR	RW	External Interrupt Port Select High
0x2308	GPIO_EXTIPINSELL_CLR	RW	External Interrupt Pin Select Low
0x230C	GPIO_EXTIPINSELH_CLR	RW	External Interrupt Pin Select High
0x2310	GPIO_EXTIRISE_CLR	RW	External Interrupt Rising Edge Trigger
0x2314	GPIO_EXTIFALL_CLR	RW	External Interrupt Falling Edge Trigger
0x2320	GPIO_IF_CLR	RWH INTFLAG	Interrupt Flag
0x2324	GPIO_IEN_CLR	RW	Interrupt Enable

Offset	Name	Type	Description
0x232C	GPIO_EM4WUEN_CLR	RW	EM4 Wakeup Enable
0x2330	GPIO_EM4WUPOL_CLR	RW	EM4 Wakeup Polarity
0x2340	GPIO_DBGROUTEPEN_CLR	RW	Debugger Route Pin Enable
0x2344	GPIO_TRACEROUTEPEN_CLR	RW	Trace Route Pin Enable
0x2348	GPIO_FEMROUTEPEN_CLR	RW	FEM Route Pin Enable
0x2350	GPIO_ACMP0_ROUTEEN_CLR	RW	ACMP0 Pin Enable
0x2354	GPIO_ACMP0_ACMPOUT-ROUTE_CLR	RW	ACMPOUT Port/Pin Select
0x235C	GPIO_ACMP1_ROUTEEN_CLR	RW	ACMP1 Pin Enable
0x2360	GPIO_ACMP1_ACMPOUT-ROUTE_CLR	RW	ACMPOUT Port/Pin Select
0x2368	GPIO_CMU_ROUTEEN_CLR	RW	CMU Pin Enable
0x236C	GPIO_CMU_CLKIN0ROUTE_CLR	RW	CLKIN0 Port/Pin Select
0x2370	GPIO_CMU_CLKOUT0ROUTE_CLR	RW	CLKOUT0 Port/Pin Select
0x2374	GPIO_CMU_CLKOUT1ROUTE_CLR	RW	CLKOUT1 Port/Pin Select
0x2378	GPIO_CMU_CLKOUT2ROUTE_CLR	RW	CLKOUT2 Port/Pin Select
0x2384	GPIO_DCDC_ROUTEEN_CLR	RW	DCDC Pin Enable
0x2394	GPIO_EUSART0_ROU-TEEN_CLR	RW	EUSART0 Pin Enable
0x2398	GPIO_EU-SART0_CSROUTE_CLR	RW	CS Port/Pin Select
0x239C	GPIO_EU-SART0_CTSROUTE_CLR	RW	CTS Port/Pin Select
0x23A0	GPIO_EU-SART0_RTSROUTE_CLR	RW	RTS Port/Pin Select
0x23A4	GPIO_EU-SART0_RXROUTE_CLR	RW	RX Port/Pin Select
0x23A8	GPIO_EU-SART0_SCLKROUTE_CLR	RW	SCLK Port/Pin Select
0x23AC	GPIO_EU-SART0_TXROUTE_CLR	RW	TX Port/Pin Select
0x23B4	GPIO_EUSART1_ROU-TEEN_CLR	RW	EUSART1 Pin Enable
0x23B8	GPIO_EU-SART1_CSROUTE_CLR	RW	CS Port/Pin Select
0x23BC	GPIO_EU-SART1_CTSROUTE_CLR	RW	CTS Port/Pin Select
0x23C0	GPIO_EU-SART1_RTSROUTE_CLR	RW	RTS Port/Pin Select

Offset	Name	Type	Description
0x23C4	GPIO_EUSART1_RXROUTE_CLR	RW	RX Port/Pin Select
0x23C8	GPIO_EUSART1_SCLKROUTE_CLR	RW	SCLK Port/Pin Select
0x23CC	GPIO_EUSART1_TXROUTE_CLR	RW	TX Port/Pin Select
0x23D4	GPIO_EUSART2_ROUTEEN_CLR	RW	EUSART2 Pin Enable
0x23D8	GPIO_EUSART2_CSROUTE_CLR	RW	CS Port/Pin Select
0x23DC	GPIO_EUSART2_CTSROUTE_CLR	RW	CTS Port/Pin Select
0x23E0	GPIO_EUSART2_RTSROUTE_CLR	RW	RTS Port/Pin Select
0x23E4	GPIO_EUSART2_RXROUTE_CLR	RW	RX Port/Pin Select
0x23E8	GPIO_EUSART2_SCLKROUTE_CLR	RW	SCLK Port/Pin Select
0x23EC	GPIO_EUSART2_TXROUTE_CLR	RW	TX Port/Pin Select
0x23F4	GPIO_EUSART3_ROUTEEN_CLR	RW	EUSART3 Pin Enable
0x23F8	GPIO_EUSART3_CSROUTE_CLR	RW	CS Port/Pin Select
0x23FC	GPIO_EUSART3_CTSROUTE_CLR	RW	CTS Port/Pin Select
0x2400	GPIO_EUSART3_RTSROUTE_CLR	RW	RTS Port/Pin Select
0x2404	GPIO_EUSART3_RXROUTE_CLR	RW	RX Port/Pin Select
0x2408	GPIO_EUSART3_SCLKROUTE_CLR	RW	SCLK Port/Pin Select
0x240C	GPIO_EUSART3_TXROUTE_CLR	RW	TX Port/Pin Select
0x2414	GPIO_EUSART4_ROUTEEN_CLR	RW	EUSART4 Pin Enable
0x2418	GPIO_EUSART4_CSROUTE_CLR	RW	CS Port/Pin Select
0x241C	GPIO_EUSART4_CTSROUTE_CLR	RW	CTS Port/Pin Select
0x2420	GPIO_EUSART4_RTSROUTE_CLR	RW	RTS Port/Pin Select
0x2424	GPIO_EUSART4_RXROUTE_CLR	RW	RX Port/Pin Select
0x2428	GPIO_EUSART4_SCLKROUTE_CLR	RW	SCLK Port/Pin Select

Offset	Name	Type	Description
0x242C	GPIO_EU-SART4_TXROUTE_CLR	RW	TX Port/Pin Select
0x2434	GPIO_FRC_ROUTEEN_CLR	RW	FRC Pin Enable
0x2438	GPIO_FRC_DCLKROUTE_CLR	RW	DCLK Port/Pin Select
0x243C	GPIO_FRC_DFRAME-ROUTE_CLR	RW	DFRAME Port/Pin Select
0x2440	GPIO_FRC_DOUTROUTE_CLR	RW	DOUT Port/Pin Select
0x2448	GPIO_I2C0_ROUTEEN_CLR	RW	I2C0 Pin Enable
0x244C	GPIO_I2C0_SCLROUTE_CLR	RW	SCL Port/Pin Select
0x2450	GPIO_I2C0_SDAROUTE_CLR	RW	SDA Port/Pin Select
0x2458	GPIO_I2C1_ROUTEEN_CLR	RW	I2C1 Pin Enable
0x245C	GPIO_I2C1_SCLROUTE_CLR	RW	SCL Port/Pin Select
0x2460	GPIO_I2C1_SDAROUTE_CLR	RW	SDA Port/Pin Select
0x2468	GPIO_LESENSE_ROU-TEEN_CLR	RW	LESENSE Pin Enable
0x246C	GPIO_LESENSE_CH0OUT-ROUTE_CLR	RW	CH0OUT Port/Pin Select
0x2470	GPIO_LESENSE_CH1OUT-ROUTE_CLR	RW	CH1OUT Port/Pin Select
0x2474	GPIO_LESENSE_CH2OUT-ROUTE_CLR	RW	CH2OUT Port/Pin Select
0x2478	GPIO_LESENSE_CH3OUT-ROUTE_CLR	RW	CH3OUT Port/Pin Select
0x247C	GPIO_LESENSE_CH4OUT-ROUTE_CLR	RW	CH4OUT Port/Pin Select
0x2480	GPIO_LESENSE_CH5OUT-ROUTE_CLR	RW	CH5OUT Port/Pin Select
0x2484	GPIO_LESENSE_CH6OUT-ROUTE_CLR	RW	CH6OUT Port/Pin Select
0x2488	GPIO_LESENSE_CH7OUT-ROUTE_CLR	RW	CH7OUT Port/Pin Select
0x248C	GPIO_LESENSE_CH8OUT-ROUTE_CLR	RW	CH8OUT Port/Pin Select
0x2490	GPIO_LESENSE_CH9OUT-ROUTE_CLR	RW	CH9OUT Port/Pin Select
0x2494	GPIO_LESENSE_CH10OUT-ROUTE_CLR	RW	CH10OUT Port/Pin Select
0x2498	GPIO_LESENSE_CH11OUT-ROUTE_CLR	RW	CH11OUT Port/Pin Select
0x249C	GPIO_LESENSE_CH12OUT-ROUTE_CLR	RW	CH12OUT Port/Pin Select
0x24A0	GPIO_LESENSE_CH13OUT-ROUTE_CLR	RW	CH13OUT Port/Pin Select

Offset	Name	Type	Description
0x24A4	GPIO_LESENSE_CH14OUT-ROUTE_CLR	RW	CH14OUT Port/Pin Select
0x24A8	GPIO_LESENSE_CH15OUT-ROUTE_CLR	RW	CH15OUT Port/Pin Select
0x24B0	GPIO_LETIMER_ROU-TEEN_CLR	RW	LETIMER Pin Enable
0x24B4	GPIO_LETIM-ER_OUT0ROUTE_CLR	RW	OUT0 Port/Pin Select
0x24B8	GPIO_LETIM-ER_OUT1ROUTE_CLR	RW	OUT1 Port/Pin Select
0x24C0	GPIO_MODEM_ROUTEEN_CLR	RW	MODEM Pin Enable
0x24C4	GPIO_MO-DEM_ANT0ROUTE_CLR	RW	ANT0 Port/Pin Select
0x24C8	GPIO_MO-DEM_ANT1ROUTE_CLR	RW	ANT1 Port/Pin Select
0x24CC	GPIO_MODEM_ANTROLLO-VERROUTE_CLR	RW	ANTROLLOVER Port/Pin Select
0x24D0	GPIO_MO-DEM_ANTRR0ROUTE_CLR	RW	ANTRR0 Port/Pin Select
0x24D4	GPIO_MO-DEM_ANTRR1ROUTE_CLR	RW	ANTRR1 Port/Pin Select
0x24D8	GPIO_MO-DEM_ANTRR2ROUTE_CLR	RW	ANTRR2 Port/Pin Select
0x24DC	GPIO_MO-DEM_ANTRR3ROUTE_CLR	RW	ANTRR3 Port/Pin Select
0x24E0	GPIO_MO-DEM_ANTRR4ROUTE_CLR	RW	ANTRR4 Port/Pin Select
0x24E4	GPIO_MO-DEM_ANTRR5ROUTE_CLR	RW	ANTRR5 Port/Pin Select
0x24E8	GPIO_MODEM_ANTSWEN-ROUTE_CLR	RW	ANTSWEN Port/Pin Select
0x24EC	GPIO_MODEM_ANTSWUS-ROUTE_CLR	RW	ANTSWUS Port/Pin Select
0x24F0	GPIO_MODEM_ANTTRIG-ROUTE_CLR	RW	ANTTRIG Port/Pin Select
0x24F4	GPIO_MODEM_ANTTRIGSTOP-ROUTE_CLR	RW	ANTTRIGSTOP Port/Pin Select
0x24F8	GPIO_MO-DEM_DCLKROUTE_CLR	RW	DCLK Port/Pin Select
0x24FC	GPIO_MODEM_DIN-ROUTE_CLR	RW	DIN Port/Pin Select
0x2500	GPIO_MODEM_DOUT-ROUTE_CLR	RW	DOUT Port/Pin Select
0x250C	GPIO_PCNT0_S0IN-ROUTE_CLR	RW	S0IN Port/Pin Select
0x2510	GPIO_PCNT0_S1IN-ROUTE_CLR	RW	S1IN Port/Pin Select

Offset	Name	Type	Description
0x2518	GPIO_PRS0_ROUTEEN_CLR	RW	PRS0 Pin Enable
0x251C	GPIO_PRS0_ASYNCH0ROUTE_CLR	RW	ASYNCH0 Port/Pin Select
0x2520	GPIO_PRS0_ASYNCH1ROUTE_CLR	RW	ASYNCH1 Port/Pin Select
0x2524	GPIO_PRS0_ASYNCH2ROUTE_CLR	RW	ASYNCH2 Port/Pin Select
0x2528	GPIO_PRS0_ASYNCH3ROUTE_CLR	RW	ASYNCH3 Port/Pin Select
0x252C	GPIO_PRS0_ASYNCH4ROUTE_CLR	RW	ASYNCH4 Port/Pin Select
0x2530	GPIO_PRS0_ASYNCH5ROUTE_CLR	RW	ASYNCH5 Port/Pin Select
0x2534	GPIO_PRS0_ASYNCH6ROUTE_CLR	RW	ASYNCH6 Port/Pin Select
0x2538	GPIO_PRS0_ASYNCH7ROUTE_CLR	RW	ASYNCH7 Port/Pin Select
0x253C	GPIO_PRS0_ASYNCH8ROUTE_CLR	RW	ASYNCH8 Port/Pin Select
0x2540	GPIO_PRS0_ASYNCH9ROUTE_CLR	RW	ASYNCH9 Port/Pin Select
0x2544	GPIO_PRS0_ASYNCH10ROUTE_CLR	RW	ASYNCH10 Port/Pin Select
0x2548	GPIO_PRS0_ASYNCH11ROUTE_CLR	RW	ASYNCH11 Port/Pin Select
0x254C	GPIO_PRS0_SYNCH0ROUTE_CLR	RW	SYNCH0 Port/Pin Select
0x2550	GPIO_PRS0_SYNCH1ROUTE_CLR	RW	SYNCH1 Port/Pin Select
0x2554	GPIO_PRS0_SYNCH2ROUTE_CLR	RW	SYNCH2 Port/Pin Select
0x2558	GPIO_PRS0_SYNCH3ROUTE_CLR	RW	SYNCH3 Port/Pin Select
0x25C0	GPIO_SYXO0_BUFOUTREQINASYNCROUTE_CLR	RW	BUFOUTREQINASYNC Port/Pin Select
0x25C8	GPIO_TIMER0_ROUTEEN_CLR	RW	TIMER0 Pin Enable
0x25CC	GPIO_TIMER0_CC0ROUTE_CLR	RW	CC0 Port/Pin Select
0x25D0	GPIO_TIMER0_CC1ROUTE_CLR	RW	CC1 Port/Pin Select
0x25D4	GPIO_TIMER0_CC2ROUTE_CLR	RW	CC2 Port/Pin Select
0x25D8	GPIO_TIMER0_CDTI0ROUTE_CLR	RW	CDTI0 Port/Pin Select
0x25DC	GPIO_TIMER0_CDTI1ROUTE_CLR	RW	CDTI1 Port/Pin Select

Offset	Name	Type	Description
0x25E0	GPIO_TIMER0_CDTI2ROUTE_CLR	RW	CDTI2 Port/Pin Select
0x25E8	GPIO_TIMER1_ROUTEEN_CLR	RW	TIMER1 Pin Enable
0x25EC	GPIO_TIMER1_CC0ROUTE_CLR	RW	CC0 Port/Pin Select
0x25F0	GPIO_TIMER1_CC1ROUTE_CLR	RW	CC1 Port/Pin Select
0x25F4	GPIO_TIMER1_CC2ROUTE_CLR	RW	CC2 Port/Pin Select
0x25F8	GPIO_TIMER1_CDTI0ROUTE_CLR	RW	CDTI0 Port/Pin Select
0x25FC	GPIO_TIMER1_CDTI1ROUTE_CLR	RW	CDTI1 Port/Pin Select
0x2600	GPIO_TIMER1_CDTI2ROUTE_CLR	RW	CDTI2 Port/Pin Select
0x2608	GPIO_TIMER2_ROUTEEN_CLR	RW	TIMER2 Pin Enable
0x260C	GPIO_TIMER2_CC0ROUTE_CLR	RW	CC0 Port/Pin Select
0x2610	GPIO_TIMER2_CC1ROUTE_CLR	RW	CC1 Port/Pin Select
0x2614	GPIO_TIMER2_CC2ROUTE_CLR	RW	CC2 Port/Pin Select
0x2618	GPIO_TIMER2_CDTI0ROUTE_CLR	RW	CDTI0 Port/Pin Select
0x261C	GPIO_TIMER2_CDTI1ROUTE_CLR	RW	CDTI1 Port/Pin Select
0x2620	GPIO_TIMER2_CDTI2ROUTE_CLR	RW	CDTI2 Port/Pin Select
0x2628	GPIO_TIMER3_ROUTEEN_CLR	RW	TIMER3 Pin Enable
0x262C	GPIO_TIMER3_CC0ROUTE_CLR	RW	CC0 Port/Pin Select
0x2630	GPIO_TIMER3_CC1ROUTE_CLR	RW	CC1 Port/Pin Select
0x2634	GPIO_TIMER3_CC2ROUTE_CLR	RW	CC2 Port/Pin Select
0x2638	GPIO_TIMER3_CDTI0ROUTE_CLR	RW	CDTI0 Port/Pin Select
0x263C	GPIO_TIMER3_CDTI1ROUTE_CLR	RW	CDTI1 Port/Pin Select
0x2640	GPIO_TIMER3_CDTI2ROUTE_CLR	RW	CDTI2 Port/Pin Select
0x2648	GPIO_TIMER4_ROUTEEN_CLR	RW	TIMER4 Pin Enable
0x264C	GPIO_TIMER4_CC0ROUTE_CLR	RW	CC0 Port/Pin Select
0x2650	GPIO_TIMER4_CC1ROUTE_CLR	RW	CC1 Port/Pin Select

Offset	Name	Type	Description
0x2654	GPIO_TIMER4_CC2ROUTE_CLR	RW	CC2 Port/Pin Select
0x2658	GPIO_TIMER4_CDTI0ROUTE_CLR	RW	CDTI0 Port/Pin Select
0x265C	GPIO_TIMER4_CDTI1ROUTE_CLR	RW	CDTI1 Port/Pin Select
0x2660	GPIO_TIMER4_CDTI2ROUTE_CLR	RW	CDTI2 Port/Pin Select
0x2668	GPIO_TIMER5_ROUTEEN_CLR	RW	TIMER5 Pin Enable
0x266C	GPIO_TIMER5_CC0ROUTE_CLR	RW	CC0 Port/Pin Select
0x2670	GPIO_TIMER5_CC1ROUTE_CLR	RW	CC1 Port/Pin Select
0x2674	GPIO_TIMER5_CC2ROUTE_CLR	RW	CC2 Port/Pin Select
0x2678	GPIO_TIMER5_CDTI0ROUTE_CLR	RW	CDTI0 Port/Pin Select
0x267C	GPIO_TIMER5_CDTI1ROUTE_CLR	RW	CDTI1 Port/Pin Select
0x2680	GPIO_TIMER5_CDTI2ROUTE_CLR	RW	CDTI2 Port/Pin Select
0x2688	GPIO_TIMER6_ROUTEEN_CLR	RW	TIMER6 Pin Enable
0x268C	GPIO_TIMER6_CC0ROUTE_CLR	RW	CC0 Port/Pin Select
0x2690	GPIO_TIMER6_CC1ROUTE_CLR	RW	CC1 Port/Pin Select
0x2694	GPIO_TIMER6_CC2ROUTE_CLR	RW	CC2 Port/Pin Select
0x2698	GPIO_TIMER6_CDTI0ROUTE_CLR	RW	CDTI0 Port/Pin Select
0x269C	GPIO_TIMER6_CDTI1ROUTE_CLR	RW	CDTI1 Port/Pin Select
0x26A0	GPIO_TIMER6_CDTI2ROUTE_CLR	RW	CDTI2 Port/Pin Select
0x26A8	GPIO_TIMER7_ROUTEEN_CLR	RW	TIMER7 Pin Enable
0x26AC	GPIO_TIMER7_CC0ROUTE_CLR	RW	CC0 Port/Pin Select
0x26B0	GPIO_TIMER7_CC1ROUTE_CLR	RW	CC1 Port/Pin Select
0x26B4	GPIO_TIMER7_CC2ROUTE_CLR	RW	CC2 Port/Pin Select
0x26B8	GPIO_TIMER7_CDTI0ROUTE_CLR	RW	CDTI0 Port/Pin Select
0x26BC	GPIO_TIMER7_CDTI1ROUTE_CLR	RW	CDTI1 Port/Pin Select

Offset	Name	Type	Description
0x26C0	GPIO_TIM-ER7_CDTI2ROUTE_CLR	RW	CDTI2 Port/Pin Select
0x26CC	GPIO_USB_USBVBUSSENSE-ROUTE_CLR	RW	USBVBUSSENSE Port/Pin Select
0x3000	GPIO_IPVERSION_TGL	R	Main
0x3030	GPIO_PORTA_CTRL_TGL	RW	Port Control
0x3034	GPIO_PORTA_MODEL_TGL	RW	Mode Low
0x303C	GPIO_PORTA_MODEH_TGL	RW	Mode High
0x3040	GPIO_PORTA_DOUT_TGL	RW	Data Out
0x3044	GPIO_PORTA_DIN_TGL	RH	Data in
0x3060	GPIO_PORTB_CTRL_TGL	RW	Port Control
0x3064	GPIO_PORTB_MODEL_TGL	RW	Mode Low
0x306C	GPIO_PORTB_MODEH_TGL	RW	Mode High
0x3070	GPIO_PORTB_DOUT_TGL	RW	Data Out
0x3074	GPIO_PORTB_DIN_TGL	RH	Data in
0x3090	GPIO_PORTC_CTRL_TGL	RW	Port Control
0x3094	GPIO_PORTC_MODEL_TGL	RW	Mode Low
0x309C	GPIO_PORTC_MODEH_TGL	RW	Mode High
0x30A0	GPIO_PORTC_DOUT_TGL	RW	Data Out
0x30A4	GPIO_PORTC_DIN_TGL	RH	Data in
0x30C0	GPIO_PORTD_CTRL_TGL	RW	Port Control
0x30C4	GPIO_PORTD_MODEL_TGL	RW	Mode Low
0x30D0	GPIO_PORTD_DOUT_TGL	RW	Data Out
0x30D4	GPIO_PORTD_DIN_TGL	RH	Data in
0x3200	GPIO_LOCK_TGL	W	Lock Register
0x3210	GPIO_GPIOLOCKSTATUS_TGL	RH	Lock Status
0x3220	GPIO_ABUSALLOC_TGL	RW	A Bus Allocation
0x3224	GPIO_BBUSALLOC_TGL	RW	B Bus Allocation
0x3228	GPIO_CDBUSALLOC_TGL	RW	CD Bus Allocation
0x3230	GPIO_AODD0SWITCH_TGL	RW	AODD0 Switch Register
0x3234	GPIO_AODD1SWITCH_TGL	RW	AODD1 Switch Register
0x3238	GPIO_AEVEN0SWITCH_TGL	RW	AEVEN0 Switch Register
0x323C	GPIO_AEVEN1SWITCH_TGL	RW	AEVEN1 Switch Register
0x3240	GPIO_BODD0SWITCH_TGL	RW	BODD0 Switch Register
0x3244	GPIO_BODD1SWITCH_TGL	RW	BODD1 Switch Register
0x3248	GPIO_BEVEN0SWITCH_TGL	RW	BEVEN0 Switch Register
0x324C	GPIO_BEVEN1SWITCH_TGL	RW	BEVEN1 Switch Register
0x3250	GPIO_CDODD0SWITCH_TGL	RW	CDODD0 Switch Register

Offset	Name	Type	Description
0x3254	GPIO_CDODD1SWITCH_TGL	RW	CDODD1 Switch Register
0x3258	GPIO_CDEVEN0SWITCH_TGL	RW	CDEVEN0 Switch Register
0x325C	GPIO_CDEVEN1SWITCH_TGL	RW	CDEVEN1 Switch Register
0x3300	GPIO_EXTIPSELL_TGL	RW	External Interrupt Port Select Low
0x3304	GPIO_EXTIPSELH_TGL	RW	External Interrupt Port Select High
0x3308	GPIO_EXTIPINSELL_TGL	RW	External Interrupt Pin Select Low
0x330C	GPIO_EXTIPINSELH_TGL	RW	External Interrupt Pin Select High
0x3310	GPIO_EXTIRISE_TGL	RW	External Interrupt Rising Edge Trigger
0x3314	GPIO_EXTIFALL_TGL	RW	External Interrupt Falling Edge Trigger
0x3320	GPIO_IF_TGL	RWH INTFLAG	Interrupt Flag
0x3324	GPIO_IEN_TGL	RW	Interrupt Enable
0x332C	GPIO_EM4WUEN_TGL	RW	EM4 Wakeup Enable
0x3330	GPIO_EM4WUPOL_TGL	RW	EM4 Wakeup Polarity
0x3340	GPIO_DBGROUTEPEN_TGL	RW	Debugger Route Pin Enable
0x3344	GPIO_TRACEROUTEPEN_TGL	RW	Trace Route Pin Enable
0x3348	GPIO_FEMROUTEPEN_TGL	RW	FEM Route Pin Enable
0x3350	GPIO_ACMP0_ROUTEEN_TGL	RW	ACMP0 Pin Enable
0x3354	GPIO_ACMP0_ACMPOUT-ROUTE_TGL	RW	ACMPOUT Port/Pin Select
0x335C	GPIO_ACMP1_ROUTEEN_TGL	RW	ACMP1 Pin Enable
0x3360	GPIO_ACMP1_ACMPOUT-ROUTE_TGL	RW	ACMPOUT Port/Pin Select
0x3368	GPIO_CMU_ROUTEEN_TGL	RW	CMU Pin Enable
0x336C	GPIO_CMU_CLKIN0ROUTE_TGL	RW	CLKIN0 Port/Pin Select
0x3370	GPIO_CMU_CLKOUT0ROUTE_TGL	RW	CLKOUT0 Port/Pin Select
0x3374	GPIO_CMU_CLKOUT1ROUTE_TGL	RW	CLKOUT1 Port/Pin Select
0x3378	GPIO_CMU_CLKOUT2ROUTE_TGL	RW	CLKOUT2 Port/Pin Select
0x3384	GPIO_DCDC_ROUTEEN_TGL	RW	DCDC Pin Enable
0x3394	GPIO_EUSART0_ROU-TEEN_TGL	RW	EUSART0 Pin Enable
0x3398	GPIO_EU-SART0_CSROUTE_TGL	RW	CS Port/Pin Select
0x339C	GPIO_EU-SART0_CTSROUTE_TGL	RW	CTS Port/Pin Select
0x33A0	GPIO_EU-SART0_RTSROUTE_TGL	RW	RTS Port/Pin Select
0x33A4	GPIO_EU-SART0_RXROUTE_TGL	RW	RX Port/Pin Select

Offset	Name	Type	Description
0x33A8	GPIO_EUSART0_SCLKROUTE_TGL	RW	SCLK Port/Pin Select
0x33AC	GPIO_EUSART0_TXROUTE_TGL	RW	TX Port/Pin Select
0x33B4	GPIO_EUSART1_ROUTEEN_TGL	RW	EUSART1 Pin Enable
0x33B8	GPIO_EUSART1_CSROUTE_TGL	RW	CS Port/Pin Select
0x33BC	GPIO_EUSART1_CTSROUTE_TGL	RW	CTS Port/Pin Select
0x33C0	GPIO_EUSART1_RTSROUTE_TGL	RW	RTS Port/Pin Select
0x33C4	GPIO_EUSART1_RXROUTE_TGL	RW	RX Port/Pin Select
0x33C8	GPIO_EUSART1_SCLKROUTE_TGL	RW	SCLK Port/Pin Select
0x33CC	GPIO_EUSART1_TXROUTE_TGL	RW	TX Port/Pin Select
0x33D4	GPIO_EUSART2_ROUTEEN_TGL	RW	EUSART2 Pin Enable
0x33D8	GPIO_EUSART2_CSROUTE_TGL	RW	CS Port/Pin Select
0x33DC	GPIO_EUSART2_CTSROUTE_TGL	RW	CTS Port/Pin Select
0x33E0	GPIO_EUSART2_RTSROUTE_TGL	RW	RTS Port/Pin Select
0x33E4	GPIO_EUSART2_RXROUTE_TGL	RW	RX Port/Pin Select
0x33E8	GPIO_EUSART2_SCLKROUTE_TGL	RW	SCLK Port/Pin Select
0x33EC	GPIO_EUSART2_TXROUTE_TGL	RW	TX Port/Pin Select
0x33F4	GPIO_EUSART3_ROUTEEN_TGL	RW	EUSART3 Pin Enable
0x33F8	GPIO_EUSART3_CSROUTE_TGL	RW	CS Port/Pin Select
0x33FC	GPIO_EUSART3_CTSROUTE_TGL	RW	CTS Port/Pin Select
0x3400	GPIO_EUSART3_RTSROUTE_TGL	RW	RTS Port/Pin Select
0x3404	GPIO_EUSART3_RXROUTE_TGL	RW	RX Port/Pin Select
0x3408	GPIO_EUSART3_SCLKROUTE_TGL	RW	SCLK Port/Pin Select
0x340C	GPIO_EUSART3_TXROUTE_TGL	RW	TX Port/Pin Select

Offset	Name	Type	Description
0x3414	GPIO_EUSART4_ROUTEEN_TGL	RW	EUSART4 Pin Enable
0x3418	GPIO_EUSART4_CSROUTE_TGL	RW	CS Port/Pin Select
0x341C	GPIO_EUSART4_CTSROUTE_TGL	RW	CTS Port/Pin Select
0x3420	GPIO_EUSART4_RTSROUTE_TGL	RW	RTS Port/Pin Select
0x3424	GPIO_EUSART4_RXROUTE_TGL	RW	RX Port/Pin Select
0x3428	GPIO_EUSART4_SCLKROUTE_TGL	RW	SCLK Port/Pin Select
0x342C	GPIO_EUSART4_TXROUTE_TGL	RW	TX Port/Pin Select
0x3434	GPIO_FRC_ROUTEEN_TGL	RW	FRC Pin Enable
0x3438	GPIO_FRC_DCLKROUTE_TGL	RW	DCLK Port/Pin Select
0x343C	GPIO_FRC_DFRAMEROUTE_TGL	RW	DFRAME Port/Pin Select
0x3440	GPIO_FRC_DOUTROUTE_TGL	RW	DOUT Port/Pin Select
0x3448	GPIO_I2C0_ROUTEEN_TGL	RW	I2C0 Pin Enable
0x344C	GPIO_I2C0_SCLROUTE_TGL	RW	SCL Port/Pin Select
0x3450	GPIO_I2C0_SDAROUTE_TGL	RW	SDA Port/Pin Select
0x3458	GPIO_I2C1_ROUTEEN_TGL	RW	I2C1 Pin Enable
0x345C	GPIO_I2C1_SCLROUTE_TGL	RW	SCL Port/Pin Select
0x3460	GPIO_I2C1_SDAROUTE_TGL	RW	SDA Port/Pin Select
0x3468	GPIO_LESENSE_ROUTEEN_TGL	RW	LESENSE Pin Enable
0x346C	GPIO_LESENSE_CH0OUTROUTE_TGL	RW	CH0OUT Port/Pin Select
0x3470	GPIO_LESENSE_CH1OUTROUTE_TGL	RW	CH1OUT Port/Pin Select
0x3474	GPIO_LESENSE_CH2OUTROUTE_TGL	RW	CH2OUT Port/Pin Select
0x3478	GPIO_LESENSE_CH3OUTROUTE_TGL	RW	CH3OUT Port/Pin Select
0x347C	GPIO_LESENSE_CH4OUTROUTE_TGL	RW	CH4OUT Port/Pin Select
0x3480	GPIO_LESENSE_CH5OUTROUTE_TGL	RW	CH5OUT Port/Pin Select
0x3484	GPIO_LESENSE_CH6OUTROUTE_TGL	RW	CH6OUT Port/Pin Select
0x3488	GPIO_LESENSE_CH7OUTROUTE_TGL	RW	CH7OUT Port/Pin Select

Offset	Name	Type	Description
0x348C	GPIO_LESENSE_CH8OUT-ROUTE_TGL	RW	CH8OUT Port/Pin Select
0x3490	GPIO_LESENSE_CH9OUT-ROUTE_TGL	RW	CH9OUT Port/Pin Select
0x3494	GPIO_LESENSE_CH10OUT-ROUTE_TGL	RW	CH10OUT Port/Pin Select
0x3498	GPIO_LESENSE_CH11OUT-ROUTE_TGL	RW	CH11OUT Port/Pin Select
0x349C	GPIO_LESENSE_CH12OUT-ROUTE_TGL	RW	CH12OUT Port/Pin Select
0x34A0	GPIO_LESENSE_CH13OUT-ROUTE_TGL	RW	CH13OUT Port/Pin Select
0x34A4	GPIO_LESENSE_CH14OUT-ROUTE_TGL	RW	CH14OUT Port/Pin Select
0x34A8	GPIO_LESENSE_CH15OUT-ROUTE_TGL	RW	CH15OUT Port/Pin Select
0x34B0	GPIO_LETIMER_ROU-TEEN_TGL	RW	LETIMER Pin Enable
0x34B4	GPIO_LETIM-ER_OUT0ROUTE_TGL	RW	OUT0 Port/Pin Select
0x34B8	GPIO_LETIM-ER_OUT1ROUTE_TGL	RW	OUT1 Port/Pin Select
0x34C0	GPIO_MODEM_ROUTEEN_TGL	RW	MODEM Pin Enable
0x34C4	GPIO_MO-DEM_ANT0ROUTE_TGL	RW	ANT0 Port/Pin Select
0x34C8	GPIO_MO-DEM_ANT1ROUTE_TGL	RW	ANT1 Port/Pin Select
0x34CC	GPIO_MODEM_ANTROLLO-VERROUTE_TGL	RW	ANTROLLOVER Port/Pin Select
0x34D0	GPIO_MO-DEM_ANTRR0ROUTE_TGL	RW	ANTRR0 Port/Pin Select
0x34D4	GPIO_MO-DEM_ANTRR1ROUTE_TGL	RW	ANTRR1 Port/Pin Select
0x34D8	GPIO_MO-DEM_ANTRR2ROUTE_TGL	RW	ANTRR2 Port/Pin Select
0x34DC	GPIO_MO-DEM_ANTRR3ROUTE_TGL	RW	ANTRR3 Port/Pin Select
0x34E0	GPIO_MO-DEM_ANTRR4ROUTE_TGL	RW	ANTRR4 Port/Pin Select
0x34E4	GPIO_MO-DEM_ANTRR5ROUTE_TGL	RW	ANTRR5 Port/Pin Select
0x34E8	GPIO_MODEM_ANTSWEN-ROUTE_TGL	RW	ANTSWEN Port/Pin Select
0x34EC	GPIO_MODEM_ANTSWUS-ROUTE_TGL	RW	ANTSWUS Port/Pin Select
0x34F0	GPIO_MODEM_ANTTRIG-ROUTE_TGL	RW	ANTTRIG Port/Pin Select

Offset	Name	Type	Description
0x34F4	GPIO_MODEM_ANTTRIGSTOP-ROUTE_TGL	RW	ANTTRIGSTOP Port/Pin Select
0x34F8	GPIO_MO-DEM_DCLKROUTE_TGL	RW	DCLK Port/Pin Select
0x34FC	GPIO_MODEM_DIN-ROUTE_TGL	RW	DIN Port/Pin Select
0x3500	GPIO_MODEM_DOUT-ROUTE_TGL	RW	DOUT Port/Pin Select
0x350C	GPIO_PCNT0_S0IN-ROUTE_TGL	RW	S0IN Port/Pin Select
0x3510	GPIO_PCNT0_S1IN-ROUTE_TGL	RW	S1IN Port/Pin Select
0x3518	GPIO_PRS0_ROUTEEN_TGL	RW	PRS0 Pin Enable
0x351C	GPIO_PRS0_ASYNCH0ROUTE_TGL	RW	ASYNCH0 Port/Pin Select
0x3520	GPIO_PRS0_ASYNCH1ROUTE_TGL	RW	ASYNCH1 Port/Pin Select
0x3524	GPIO_PRS0_ASYNCH2ROUTE_TGL	RW	ASYNCH2 Port/Pin Select
0x3528	GPIO_PRS0_ASYNCH3ROUTE_TGL	RW	ASYNCH3 Port/Pin Select
0x352C	GPIO_PRS0_ASYNCH4ROUTE_TGL	RW	ASYNCH4 Port/Pin Select
0x3530	GPIO_PRS0_ASYNCH5ROUTE_TGL	RW	ASYNCH5 Port/Pin Select
0x3534	GPIO_PRS0_ASYNCH6ROUTE_TGL	RW	ASYNCH6 Port/Pin Select
0x3538	GPIO_PRS0_ASYNCH7ROUTE_TGL	RW	ASYNCH7 Port/Pin Select
0x353C	GPIO_PRS0_ASYNCH8ROUTE_TGL	RW	ASYNCH8 Port/Pin Select
0x3540	GPIO_PRS0_ASYNCH9ROUTE_TGL	RW	ASYNCH9 Port/Pin Select
0x3544	GPIO_PRS0_ASYNCH10ROUTE_TGL	RW	ASYNCH10 Port/Pin Select
0x3548	GPIO_PRS0_ASYNCH11ROUTE_TGL	RW	ASYNCH11 Port/Pin Select
0x354C	GPIO_PRS0_SYNCH0ROUTE_TGL	RW	SYNCH0 Port/Pin Select
0x3550	GPIO_PRS0_SYNCH1ROUTE_TGL	RW	SYNCH1 Port/Pin Select
0x3554	GPIO_PRS0_SYNCH2ROUTE_TGL	RW	SYNCH2 Port/Pin Select
0x3558	GPIO_PRS0_SYNCH3ROUTE_TGL	RW	SYNCH3 Port/Pin Select
0x35C0	GPIO_SYXO0_BUFOUTREQI-NASYNCROUTE_TGL	RW	BUFOUTREQINASYNC Port/Pin Select

Offset	Name	Type	Description
0x35C8	GPIO_TIMER0_ROUTEEN_TGL	RW	TIMER0 Pin Enable
0x35CC	GPIO_TIMER0_CC0ROUTE_TGL	RW	CC0 Port/Pin Select
0x35D0	GPIO_TIMER0_CC1ROUTE_TGL	RW	CC1 Port/Pin Select
0x35D4	GPIO_TIMER0_CC2ROUTE_TGL	RW	CC2 Port/Pin Select
0x35D8	GPIO_TIMER0_CDTI0ROUTE_TGL	RW	CDTI0 Port/Pin Select
0x35DC	GPIO_TIMER0_CDTI1ROUTE_TGL	RW	CDTI1 Port/Pin Select
0x35E0	GPIO_TIMER0_CDTI2ROUTE_TGL	RW	CDTI2 Port/Pin Select
0x35E8	GPIO_TIMER1_ROUTEEN_TGL	RW	TIMER1 Pin Enable
0x35EC	GPIO_TIMER1_CC0ROUTE_TGL	RW	CC0 Port/Pin Select
0x35F0	GPIO_TIMER1_CC1ROUTE_TGL	RW	CC1 Port/Pin Select
0x35F4	GPIO_TIMER1_CC2ROUTE_TGL	RW	CC2 Port/Pin Select
0x35F8	GPIO_TIMER1_CDTI0ROUTE_TGL	RW	CDTI0 Port/Pin Select
0x35FC	GPIO_TIMER1_CDTI1ROUTE_TGL	RW	CDTI1 Port/Pin Select
0x3600	GPIO_TIMER1_CDTI2ROUTE_TGL	RW	CDTI2 Port/Pin Select
0x3608	GPIO_TIMER2_ROUTEEN_TGL	RW	TIMER2 Pin Enable
0x360C	GPIO_TIMER2_CC0ROUTE_TGL	RW	CC0 Port/Pin Select
0x3610	GPIO_TIMER2_CC1ROUTE_TGL	RW	CC1 Port/Pin Select
0x3614	GPIO_TIMER2_CC2ROUTE_TGL	RW	CC2 Port/Pin Select
0x3618	GPIO_TIMER2_CDTI0ROUTE_TGL	RW	CDTI0 Port/Pin Select
0x361C	GPIO_TIMER2_CDTI1ROUTE_TGL	RW	CDTI1 Port/Pin Select
0x3620	GPIO_TIMER2_CDTI2ROUTE_TGL	RW	CDTI2 Port/Pin Select
0x3628	GPIO_TIMER3_ROUTEEN_TGL	RW	TIMER3 Pin Enable
0x362C	GPIO_TIMER3_CC0ROUTE_TGL	RW	CC0 Port/Pin Select
0x3630	GPIO_TIMER3_CC1ROUTE_TGL	RW	CC1 Port/Pin Select
0x3634	GPIO_TIMER3_CC2ROUTE_TGL	RW	CC2 Port/Pin Select

Offset	Name	Type	Description
0x3638	GPIO_TIMER3_CDTI0ROUTE_TGL	RW	CDTI0 Port/Pin Select
0x363C	GPIO_TIMER3_CDTI1ROUTE_TGL	RW	CDTI1 Port/Pin Select
0x3640	GPIO_TIMER3_CDTI2ROUTE_TGL	RW	CDTI2 Port/Pin Select
0x3648	GPIO_TIMER4_ROUTEEN_TGL	RW	TIMER4 Pin Enable
0x364C	GPIO_TIMER4_CC0ROUTE_TGL	RW	CC0 Port/Pin Select
0x3650	GPIO_TIMER4_CC1ROUTE_TGL	RW	CC1 Port/Pin Select
0x3654	GPIO_TIMER4_CC2ROUTE_TGL	RW	CC2 Port/Pin Select
0x3658	GPIO_TIMER4_CDTI0ROUTE_TGL	RW	CDTI0 Port/Pin Select
0x365C	GPIO_TIMER4_CDTI1ROUTE_TGL	RW	CDTI1 Port/Pin Select
0x3660	GPIO_TIMER4_CDTI2ROUTE_TGL	RW	CDTI2 Port/Pin Select
0x3668	GPIO_TIMER5_ROUTEEN_TGL	RW	TIMER5 Pin Enable
0x366C	GPIO_TIMER5_CC0ROUTE_TGL	RW	CC0 Port/Pin Select
0x3670	GPIO_TIMER5_CC1ROUTE_TGL	RW	CC1 Port/Pin Select
0x3674	GPIO_TIMER5_CC2ROUTE_TGL	RW	CC2 Port/Pin Select
0x3678	GPIO_TIMER5_CDTI0ROUTE_TGL	RW	CDTI0 Port/Pin Select
0x367C	GPIO_TIMER5_CDTI1ROUTE_TGL	RW	CDTI1 Port/Pin Select
0x3680	GPIO_TIMER5_CDTI2ROUTE_TGL	RW	CDTI2 Port/Pin Select
0x3688	GPIO_TIMER6_ROUTEEN_TGL	RW	TIMER6 Pin Enable
0x368C	GPIO_TIMER6_CC0ROUTE_TGL	RW	CC0 Port/Pin Select
0x3690	GPIO_TIMER6_CC1ROUTE_TGL	RW	CC1 Port/Pin Select
0x3694	GPIO_TIMER6_CC2ROUTE_TGL	RW	CC2 Port/Pin Select
0x3698	GPIO_TIMER6_CDTI0ROUTE_TGL	RW	CDTI0 Port/Pin Select
0x369C	GPIO_TIMER6_CDTI1ROUTE_TGL	RW	CDTI1 Port/Pin Select
0x36A0	GPIO_TIMER6_CDTI2ROUTE_TGL	RW	CDTI2 Port/Pin Select
0x36A8	GPIO_TIMER7_ROUTEEN_TGL	RW	TIMER7 Pin Enable

Offset	Name	Type	Description
0x36AC	GPIO_TIMER7_CC0ROUTE_TGL	RW	CC0 Port/Pin Select
0x36B0	GPIO_TIMER7_CC1ROUTE_TGL	RW	CC1 Port/Pin Select
0x36B4	GPIO_TIMER7_CC2ROUTE_TGL	RW	CC2 Port/Pin Select
0x36B8	GPIO_TIMER7_CDTI0ROUTE_TGL	RW	CDTI0 Port/Pin Select
0x36BC	GPIO_TIMER7_CDTI1ROUTE_TGL	RW	CDTI1 Port/Pin Select
0x36C0	GPIO_TIMER7_CDTI2ROUTE_TGL	RW	CDTI2 Port/Pin Select
0x36CC	GPIO_USB_USBVBUSSENSEROUTE_TGL	RW	USBVBUSSENSE Port/Pin Select

24.6 GPIO Register Description

24.6.1 GPIO_IPVERSION - Main

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x4																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x4	R	**ip version id**
	IPVERSION ID			

24.6.2 GPIO_PORTA_CTRL - Port Control

Offset	Bit Position																															
0x030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset				0x0							0x4									0x0							0x4						
Access				RW							RW									RW							RW						
Name				DINDISALT							SLEWRATEALT									DINDIS							SLEWRATE						

Bit	Name	Reset	Access	Description
31:29	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
28	DINDISALT	0x0	RW	**Data In Disable Alt**
	Data input disable for port pins using alternate modes.			
27:23	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
22:20	SLEWRATEALT	0x4	RW	**Slew Rate Alt**
	Slewrate limit for port pins using alternate modes. Higher values representer faster slewrates.			
19:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12	DINDIS	0x0	RW	**Data In Disable**
	Data input disable for port pins not using alternate modes.			
11:7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:4	SLEWRATE	0x4	RW	**Slew Rate**
	Slewrate limit for port pins using not alternate modes. Higher values representer faster slewrates.			
3:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

24.6.3 GPIO_PORTA_MODEL - Mode Low

Offset	Bit Position																													
0x034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0				0x0				0x0				0x0				0x0				0x0				0x0				0x0			
Access	RW				RW				RW				RW				RW				RW				RW				RW			
Name	MODE7				MODE6				MODE5				MODE4				MODE3				MODE2				MODE1				MODE0			

Bit	Name	Reset	Access	Description
31:28	MODE7	0x0	RW	**MODE n**
	MODE n			

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.
11	WIREDANDPULLUPFIL-TER	Open-drain output with filter and pullup.
12	WIREDANDALT	Open-drain output using alternate control.
13	WIREDANDALTFILTER	Open-drain output using alternate control with filter.
14	WIREDANDALTPULLUP	Open-drain output using alternate control with pullup.
15	WIREDANDALTPULLUP-FILTER	Open-drain output using alternate control with filter and pullup.

Bit	Name	Reset	Access	Description
27:24	MODE6	0x0	RW	**MODE n**
	MODE n			

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.

Bit	Name	Reset	Access	Description
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
23:20	MODE5 MODE n	0x0	RW	**MODE n**
	Value	Mode		Description
	0	DISABLED		Input disabled. Pullup if DOUT is set.
	1	INPUT		Input enabled. Filter if DOUT is set.
	2	INPUTPULL		Input enabled. DOUT determines pull direction.
	3	INPUTPULLFILTER		Input enabled with filter. DOUT determines pull direction.
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
19:16	MODE4 MODE n	0x0	RW	**MODE n**

Bit	Name	Reset	Access	Description
	Value	Mode		Description
	0	DISABLED		Input disabled. Pullup if DOUT is set.
	1	INPUT		Input enabled. Filter if DOUT is set.
	2	INPUTPULL		Input enabled. DOUT determines pull direction.
	3	INPUTPULLFILTER		Input enabled with filter. DOUT determines pull direction.
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
15:12	MODE3 MODE n	0x0	RW	**MODE n**
	Value	Mode		Description
	0	DISABLED		Input disabled. Pullup if DOUT is set.
	1	INPUT		Input enabled. Filter if DOUT is set.
	2	INPUTPULL		Input enabled. DOUT determines pull direction.
	3	INPUTPULLFILTER		Input enabled with filter. DOUT determines pull direction.
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.

Bit	Name	Reset	Access	Description
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
11:8	MODE2 MODE n	0x0	RW	**MODE n**

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.
11	WIREDANDPULLUPFIL-TER	Open-drain output with filter and pullup.
12	WIREDANDALT	Open-drain output using alternate control.
13	WIREDANDALTFILTER	Open-drain output using alternate control with filter.
14	WIREDANDALTPULLUP	Open-drain output using alternate control with pullup.
15	WIREDANDALTPULLUP-FILTER	Open-drain output using alternate control with filter and pullup.

7:4	MODE1 MODE n	0x0	RW	**MODE n**

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.

Bit	Name	Reset	Access	Description
	11	WIREDANDPULLUPFILTER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUPFILTER		Open-drain output using alternate control with filter and pullup.
3:0	MODE0 MODE n	0x0	RW	**MODE n**

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.
11	WIREDANDPULLUPFILTER	Open-drain output with filter and pullup.
12	WIREDANDALT	Open-drain output using alternate control.
13	WIREDANDALTFILTER	Open-drain output using alternate control with filter.
14	WIREDANDALTPULLUP	Open-drain output using alternate control with pullup.
15	WIREDANDALTPULLUPFILTER	Open-drain output using alternate control with filter and pullup.

24.6.4 GPIO_PORTA_MODEH - Mode High

Offset	Bit Position																													
0x03C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0				0x0				0x0				0x0			
Access																	RW				RW				RW				RW			
Name																	MODE3				MODE2				MODE1				MODE0			

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:12	MODE3 MODE n	0x0	RW	**MODE n**

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.
11	WIREDANDPULLUPFILTER	Open-drain output with filter and pullup.
12	WIREDANDALT	Open-drain output using alternate control.
13	WIREDANDALTFILTER	Open-drain output using alternate control with filter.
14	WIREDANDALTPULLUP	Open-drain output using alternate control with pullup.
15	WIREDANDALTPULLUPFILTER	Open-drain output using alternate control with filter and pullup.

11:8	MODE2 MODE n	0x0	RW	**MODE n**

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.

Bit	Name	Reset	Access	Description
	3	INPUTPULLFILTER		Input enabled with filter. DOUT determines pull direction.
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
7:4	MODE1 MODE n	0x0	RW	**MODE n**
	Value	Mode		Description
	0	DISABLED		Input disabled. Pullup if DOUT is set.
	1	INPUT		Input enabled. Filter if DOUT is set.
	2	INPUTPULL		Input enabled. DOUT determines pull direction.
	3	INPUTPULLFILTER		Input enabled with filter. DOUT determines pull direction.
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
3:0	MODE0 MODE n	0x0	RW	**MODE n**

Bit	Name	Reset	Access	Description

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.
11	WIREDANDPULLUPFIL-TER	Open-drain output with filter and pullup.
12	WIREDANDALT	Open-drain output using alternate control.
13	WIREDANDALTFILTER	Open-drain output using alternate control with filter.
14	WIREDANDALTPULLUP	Open-drain output using alternate control with pullup.
15	WIREDANDALTPULLUP-FILTER	Open-drain output using alternate control with filter and pullup.

24.6.5 GPIO_PORTA_DOUT - Data Out

Offset	Bit Position																															
0x040	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																					0x0											
Access																					RW											
Name																					DOUT											

Bit	Name	Reset	Access	Description
31:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:0	DOUT Data output	0x0	RW	**Data output**

24.6.6 GPIO_PORTA_DIN - Data in

Offset	Bit Position																															
0x044	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																					0x0											
Access																					R											
Name																					DIN											

Bit	Name	Reset	Access	Description
31:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:0	DIN Data input	0x0	R	**Data input**

24.6.7 GPIO_PORTB_CTRL - Port Control

Offset	Bit Position																													
0x060	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset				0x0							0x4									0x0							0x4					
Access				RW							RW									RW							RW					
Name				DINDISALT							SLEWRATEALT									DINDIS							SLEWRATE					

Bit	Name	Reset	Access	Description
31:29	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
28	DINDISALT	0x0	RW	**Data In Disable Alt**
	Data input disable for port pins using alternate modes.			
27:23	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
22:20	SLEWRATEALT	0x4	RW	**Slew Rate Alt**
	Slewrate limit for port pins using alternate modes. Higher values representer faster slewrates.			
19:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12	DINDIS	0x0	RW	**Data In Disable**
	Data input disable for port pins not using alternate modes.			
11:7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:4	SLEWRATE	0x4	RW	**Slew Rate**
	Slewrate limit for port pins using not alternate modes. Higher values representer faster slewrates.			
3:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

24.6.8 GPIO_PORTB_MODEL - Mode Low

Offset	Bit Position																													
0x064	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0				0x0				0x0				0x0				0x0				0x0				0x0				0x0			
Access	RW				RW				RW				RW				RW				RW				RW				RW			
Name	MODE7				MODE6				MODE5				MODE4				MODE3				MODE2				MODE1				MODE0			

Bit	Name	Reset	Access	Description
31:28	MODE7	0x0	RW	**MODE n**
	MODE n			

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.
11	WIREDANDPULLUPFIL-TER	Open-drain output with filter and pullup.
12	WIREDANDALT	Open-drain output using alternate control.
13	WIREDANDALTFILTER	Open-drain output using alternate control with filter.
14	WIREDANDALTPULLUP	Open-drain output using alternate control with pullup.
15	WIREDANDALTPULLUP-FILTER	Open-drain output using alternate control with filter and pullup.

Bit	Name	Reset	Access	Description
27:24	MODE6	0x0	RW	**MODE n**
	MODE n			

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.

Bit	Name	Reset	Access	Description
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
23:20	MODE5 MODE n	0x0	RW	**MODE n**
	Value	Mode		Description
	0	DISABLED		Input disabled. Pullup if DOUT is set.
	1	INPUT		Input enabled. Filter if DOUT is set.
	2	INPUTPULL		Input enabled. DOUT determines pull direction.
	3	INPUTPULLFILTER		Input enabled with filter. DOUT determines pull direction.
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
19:16	MODE4 MODE n	0x0	RW	**MODE n**

Bit	Name	Reset	Access	Description
	Value	Mode		Description
	0	DISABLED		Input disabled. Pullup if DOUT is set.
	1	INPUT		Input enabled. Filter if DOUT is set.
	2	INPUTPULL		Input enabled. DOUT determines pull direction.
	3	INPUTPULLFILTER		Input enabled with filter. DOUT determines pull direction.
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
15:12	MODE3 MODE n	0x0	RW	**MODE n**
	Value	Mode		Description
	0	DISABLED		Input disabled. Pullup if DOUT is set.
	1	INPUT		Input enabled. Filter if DOUT is set.
	2	INPUTPULL		Input enabled. DOUT determines pull direction.
	3	INPUTPULLFILTER		Input enabled with filter. DOUT determines pull direction.
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.

Bit	Name	Reset	Access	Description
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
11:8	MODE2 MODE n	0x0	RW	**MODE n**

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.
11	WIREDANDPULLUPFIL-TER	Open-drain output with filter and pullup.
12	WIREDANDALT	Open-drain output using alternate control.
13	WIREDANDALTFILTER	Open-drain output using alternate control with filter.
14	WIREDANDALTPULLUP	Open-drain output using alternate control with pullup.
15	WIREDANDALTPULLUP-FILTER	Open-drain output using alternate control with filter and pullup.

7:4	MODE1 MODE n	0x0	RW	**MODE n**

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.

Bit	Name	Reset	Access	Description
	11	WIREDANDPULLUPFILTER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUPFILTER		Open-drain output using alternate control with filter and pullup.
3:0	MODE0 MODE n	0x0	RW	**MODE n**

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.
11	WIREDANDPULLUPFILTER	Open-drain output with filter and pullup.
12	WIREDANDALT	Open-drain output using alternate control.
13	WIREDANDALTFILTER	Open-drain output using alternate control with filter.
14	WIREDANDALTPULLUP	Open-drain output using alternate control with pullup.
15	WIREDANDALTPULLUPFILTER	Open-drain output using alternate control with filter and pullup.

24.6.9 GPIO_PORTB_MODEH - Mode High

Offset	Bit Position																															
0x06C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													MODE0			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	MODE0	0x0	RW	**MODE n**

MODE

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.
11	WIREDANDPULLUPFILTER	Open-drain output with filter and pullup.
12	WIREDANDALT	Open-drain output using alternate control.
13	WIREDANDALTFILTER	Open-drain output using alternate control with filter.
14	WIREDANDALTPULLUP	Open-drain output using alternate control with pullup.
15	WIREDANDALTPULLUPFILTER	Open-drain output using alternate control with filter and pullup.

24.6.10 GPIO_PORTB_DOUT - Data Out

Offset	Bit Position																																
0x070	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0				
Access																												RW				
Name																												DOUT				

Bit	Name	Reset	Access	Description
31:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8:0	DOUT	0x0	RW	**Data output**
	Data output			

24.6.11 GPIO_PORTB_DIN - Data in

Offset	Bit Position																																
0x074	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0				
Access																												R				
Name																												DIN				

Bit	Name	Reset	Access	Description
31:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8:0	DIN	0x0	R	**Data input**
	Data input			

24.6.12 GPIO_PORTC_CTRL - Port Control

Offset	Bit Position																													
0x090	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset				0x0							0x4									0x0							0x4					
Access				RW							RW									RW							RW					
Name				DINDISALT							SLEWRATEALT									DINDIS							SLEWRATE					

Bit	Name	Reset	Access	Description
31:29	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
28	DINDISALT	0x0	RW	**Data In Disable Alt**
	Data input disable for port pins using alternate modes.			
27:23	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
22:20	SLEWRATEALT	0x4	RW	**Slew Rate Alt**
	Slewrate limit for port pins using alternate modes. Higher values representer faster slewrates.			
19:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12	DINDIS	0x0	RW	**Data In Disable**
	Data input disable for port pins not using alternate modes.			
11:7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:4	SLEWRATE	0x4	RW	**Slew Rate**
	Slewrate limit for port pins using not alternate modes. Higher values representer faster slewrates.			
3:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

24.6.13 GPIO_PORTC_MODEL - Mode Low

Offset	Bit Position																													
0x094	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0				0x0				0x0				0x0				0x0				0x0				0x0				0x0			
Access	RW				RW				RW				RW				RW				RW				RW				RW			
Name	MODE7				MODE6				MODE5				MODE4				MODE3				MODE2				MODE1				MODE0			

Bit	Name	Reset	Access	Description
31:28	MODE7	0x0	RW	**MODE n**
	MODE n			

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.
11	WIREDANDPULLUPFIL-TER	Open-drain output with filter and pullup.
12	WIREDANDALT	Open-drain output using alternate control.
13	WIREDANDALTFILTER	Open-drain output using alternate control with filter.
14	WIREDANDALTPULLUP	Open-drain output using alternate control with pullup.
15	WIREDANDALTPULLUP-FILTER	Open-drain output using alternate control with filter and pullup.

Bit	Name	Reset	Access	Description
27:24	MODE6	0x0	RW	**MODE n**
	MODE n			

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.

Bit	Name	Reset	Access	Description
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
23:20	MODE5 MODE n	0x0	RW	**MODE n**
	Value	Mode		Description
	0	DISABLED		Input disabled. Pullup if DOUT is set.
	1	INPUT		Input enabled. Filter if DOUT is set.
	2	INPUTPULL		Input enabled. DOUT determines pull direction.
	3	INPUTPULLFILTER		Input enabled with filter. DOUT determines pull direction.
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
19:16	MODE4 MODE n	0x0	RW	**MODE n**

Bit	Name	Reset	Access	Description
	Value	Mode		Description
	0	DISABLED		Input disabled. Pullup if DOUT is set.
	1	INPUT		Input enabled. Filter if DOUT is set.
	2	INPUTPULL		Input enabled. DOUT determines pull direction.
	3	INPUTPULLFILTER		Input enabled with filter. DOUT determines pull direction.
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
15:12	MODE3 MODE n	0x0	RW	**MODE n**
	Value	Mode		Description
	0	DISABLED		Input disabled. Pullup if DOUT is set.
	1	INPUT		Input enabled. Filter if DOUT is set.
	2	INPUTPULL		Input enabled. DOUT determines pull direction.
	3	INPUTPULLFILTER		Input enabled with filter. DOUT determines pull direction.
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.

Bit	Name	Reset	Access	Description
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
11:8	MODE2 MODE n	0x0	RW	**MODE n**

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.
11	WIREDANDPULLUPFIL-TER	Open-drain output with filter and pullup.
12	WIREDANDALT	Open-drain output using alternate control.
13	WIREDANDALTFILTER	Open-drain output using alternate control with filter.
14	WIREDANDALTPULLUP	Open-drain output using alternate control with pullup.
15	WIREDANDALTPULLUP-FILTER	Open-drain output using alternate control with filter and pullup.

7:4	MODE1 MODE n	0x0	RW	**MODE n**

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.

Bit	Name	Reset	Access	Description
	11	WIREDANDPULLUPFILTER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUPFILTER		Open-drain output using alternate control with filter and pullup.
3:0	MODE0 MODE n	0x0	RW	**MODE n**

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.
11	WIREDANDPULLUPFILTER	Open-drain output with filter and pullup.
12	WIREDANDALT	Open-drain output using alternate control.
13	WIREDANDALTFILTER	Open-drain output using alternate control with filter.
14	WIREDANDALTPULLUP	Open-drain output using alternate control with pullup.
15	WIREDANDALTPULLUPFILTER	Open-drain output using alternate control with filter and pullup.

24.6.14 GPIO_PORTC_MODEH - Mode High

Offset	Bit Position																															
0x09C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																					0x0				0x0				0x0			
Access																					RW				RW				RW			
Name																					MODE2				MODE1				MODE0			

Bit	Name	Reset	Access	Description
31:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:8	MODE2 MODE n	0x0	RW	**MODE n**

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.
11	WIREDANDPULLUPFILTER	Open-drain output with filter and pullup.
12	WIREDANDALT	Open-drain output using alternate control.
13	WIREDANDALTFILTER	Open-drain output using alternate control with filter.
14	WIREDANDALTPULLUP	Open-drain output using alternate control with pullup.
15	WIREDANDALTPULLUPFILTER	Open-drain output using alternate control with filter and pullup.

7:4	MODE1 MODE n	0x0	RW	**MODE n**

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.

Bit	Name	Reset	Access	Description
	3	INPUTPULLFILTER		Input enabled with filter. DOUT determines pull direction.
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
3:0	MODE0 MODE n	0x0	RW	**MODE n**

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.
11	WIREDANDPULLUPFIL-TER	Open-drain output with filter and pullup.
12	WIREDANDALT	Open-drain output using alternate control.
13	WIREDANDALTFILTER	Open-drain output using alternate control with filter.
14	WIREDANDALTPULLUP	Open-drain output using alternate control with pullup.
15	WIREDANDALTPULLUP-FILTER	Open-drain output using alternate control with filter and pullup.

24.6.15 GPIO_PORTC_DOUT - Data Out

Offset	Bit Position																															
0x0A0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0					
Access																											RW					
Name																											DOUT					

Bit	Name	Reset	Access	Description
31:11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10:0	DOUT	0x0	RW	**Data output**
	Data output			

24.6.16 GPIO_PORTC_DIN - Data in

Offset	Bit Position																															
0x0A4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0					
Access																											R					
Name																											DIN					

Bit	Name	Reset	Access	Description
31:11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10:0	DIN	0x0	R	**Data input**
	Data input			

24.6.17 GPIO_PORTD_CTRL - Port Control

Offset	Bit Position																													
0x0C0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset				0x0							0x4									0x0							0x4					
Access				RW							RW									RW							RW					
Name				DINDISALT							SLEWRATEALT									DINDIS							SLEWRATE					

Bit	Name	Reset	Access	Description
31:29	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
28	DINDISALT	0x0	RW	**Data In Disable Alt**
	Data input disable for port pins using alternate modes.			
27:23	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
22:20	SLEWRATEALT	0x4	RW	**Slew Rate Alt**
	Slewrate limit for port pins using alternate modes. Higher values representer faster slewrates.			
19:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12	DINDIS	0x0	RW	**Data In Disable**
	Data input disable for port pins not using alternate modes.			
11:7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:4	SLEWRATE	0x4	RW	**Slew Rate**
	Slewrate limit for port pins using not alternate modes. Higher values representer faster slewrates.			
3:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

24.6.18 GPIO_PORTD_MODEL - Mode Low

Offset	Bit Position																													
0x0C4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0				0x0				0x0				0x0				0x0				0x0				0x0				0x0			
Access	RW				RW				RW				RW				RW				RW				RW				RW			
Name	MODE7				MODE6				MODE5				MODE4				MODE3				MODE2				MODE1				MODE0			

Bit	Name	Reset	Access	Description
31:28	MODE7	0x0	RW	**MODE n**
	MODE n			

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.
11	WIREDANDPULLUPFIL-TER	Open-drain output with filter and pullup.
12	WIREDANDALT	Open-drain output using alternate control.
13	WIREDANDALTFILTER	Open-drain output using alternate control with filter.
14	WIREDANDALTPULLUP	Open-drain output using alternate control with pullup.
15	WIREDANDALTPULLUP-FILTER	Open-drain output using alternate control with filter and pullup.

27:24	MODE6	0x0	RW	**MODE n**
	MODE n			

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.

Bit	Name	Reset	Access	Description
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
23:20	MODE5 MODE n	0x0	RW	**MODE n**
	Value	Mode		Description
	0	DISABLED		Input disabled. Pullup if DOUT is set.
	1	INPUT		Input enabled. Filter if DOUT is set.
	2	INPUTPULL		Input enabled. DOUT determines pull direction.
	3	INPUTPULLFILTER		Input enabled with filter. DOUT determines pull direction.
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
19:16	MODE4 MODE n	0x0	RW	**MODE n**

Bit	Name	Reset	Access	Description
	Value	Mode		Description
	0	DISABLED		Input disabled. Pullup if DOUT is set.
	1	INPUT		Input enabled. Filter if DOUT is set.
	2	INPUTPULL		Input enabled. DOUT determines pull direction.
	3	INPUTPULLFILTER		Input enabled with filter. DOUT determines pull direction.
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
15:12	MODE3 MODE n	0x0	RW	**MODE n**
	Value	Mode		Description
	0	DISABLED		Input disabled. Pullup if DOUT is set.
	1	INPUT		Input enabled. Filter if DOUT is set.
	2	INPUTPULL		Input enabled. DOUT determines pull direction.
	3	INPUTPULLFILTER		Input enabled with filter. DOUT determines pull direction.
	4	PUSHPULL		Push-pull output.
	5	PUSHPULLALT		Push-pull using alternate control.
	6	WIREDOR		Wired-or output.
	7	WIREDORPULLDOWN		Wired-or output with pull-down.
	8	WIREDAND		Open-drain output.
	9	WIREDANDFILTER		Open-drain output with filter.
	10	WIREDANDPULLUP		Open-drain output with pullup.
	11	WIREDANDPULLUPFIL-TER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.

Bit	Name	Reset	Access	Description
	15	WIREDANDALTPULLUP-FILTER		Open-drain output using alternate control with filter and pullup.
11:8	MODE2 MODE n	0x0	RW	**MODE n**

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.
11	WIREDANDPULLUPFIL-TER	Open-drain output with filter and pullup.
12	WIREDANDALT	Open-drain output using alternate control.
13	WIREDANDALTFILTER	Open-drain output using alternate control with filter.
14	WIREDANDALTPULLUP	Open-drain output using alternate control with pullup.
15	WIREDANDALTPULLUP-FILTER	Open-drain output using alternate control with filter and pullup.

7:4	MODE1 MODE n	0x0	RW	**MODE n**

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.

Bit	Name	Reset	Access	Description
	11	WIREDANDPULLUPFILTER		Open-drain output with filter and pullup.
	12	WIREDANDALT		Open-drain output using alternate control.
	13	WIREDANDALTFILTER		Open-drain output using alternate control with filter.
	14	WIREDANDALTPULLUP		Open-drain output using alternate control with pullup.
	15	WIREDANDALTPULLUPFILTER		Open-drain output using alternate control with filter and pullup.
3:0	MODE0 MODE n	0x0	RW	**MODE n**

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set.
2	INPUTPULL	Input enabled. DOUT determines pull direction.
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction.
4	PUSHPULL	Push-pull output.
5	PUSHPULLALT	Push-pull using alternate control.
6	WIREDOR	Wired-or output.
7	WIREDORPULLDOWN	Wired-or output with pull-down.
8	WIREDAND	Open-drain output.
9	WIREDANDFILTER	Open-drain output with filter.
10	WIREDANDPULLUP	Open-drain output with pullup.
11	WIREDANDPULLUPFILTER	Open-drain output with filter and pullup.
12	WIREDANDALT	Open-drain output using alternate control.
13	WIREDANDALTFILTER	Open-drain output using alternate control with filter.
14	WIREDANDALTPULLUP	Open-drain output using alternate control with pullup.
15	WIREDANDALTPULLUPFILTER	Open-drain output using alternate control with filter and pullup.

24.6.19 GPIO_PORTD_DOUT - Data Out

Offset	Bit Position																													
0x0D0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									RW							
Name																									DOUT							

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	DOUT	0x0	RW	**Data output**
	Data output			

24.6.20 GPIO_PORTD_DIN - Data in

Offset	Bit Position																													
0x0D4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									R							
Name																									DIN							

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	DIN	0x0	R	**Data input**
	Data input			

24.6.21 GPIO_LOCK - Lock Register

Offset	Bit Position																													
0x200	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																								0xA534								
Access																								W								
Name																								LOCKKEY								

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LOCKKEY	0xA534	W	**Configuration Lock Key**

Write any other value than the unlock code to lock configuration registers. Write the unlock code to unlock (See text for detailed list of configuration registers.)

Value	Mode	Description
42292	UNLOCK	Unlock code

24.6.22 GPIO_GPIOLOCKSTATUS - Lock Status

Offset	Bit Position																													
0x210	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																R
Name																																LOCK

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	LOCK	0x0	R	**GPIO LOCK status**

Indicates current lock status of GPIO registers

Value	Mode	Description
0	UNLOCKED	Registers are unlocked
1	LOCKED	Registers are locked

24.6.23 GPIO_ABUSALLOC - A Bus Allocation

Offset	Bit Position																													
0x220	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0x0								0x0								0x0								0x0			
Access					RW								RW								RW								RW			
Name					AODD1								AODD0								AEVEN1								AEVEN0			

Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27:24	AODD1	0x0	RW	**A Bus Odd 1**

peripheral allocation to A Bus Odd 1

Value	Mode	Description
0	TRISTATE	The bus is not allocated
1	ADC0	The bus is allocated to ADC0
2	ACMP0	The bus is allocated to ACMP0
3	ACMP1	The bus is allocated to ACMP1
4	VDAC0CH1	The bus is allocated to VDAC0 CH1

23:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	AODD0	0x0	RW	**A Bus Odd 0**

peripheral allocation to A Bus Odd 0

Value	Mode	Description
0	TRISTATE	The bus is not allocated
1	ADC0	The bus is allocated to ADC0
2	ACMP0	The bus is allocated to ACMP0
3	ACMP1	The bus is allocated to ACMP1
4	VDAC0CH0	The bus is allocated to VDAC0 CH0

15:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:8	AEVEN1	0x0	RW	**A Bus Even 1**

peripheral allocation to A Bus Even 1

Value	Mode	Description
0	TRISTATE	The bus is not allocated
1	ADC0	The bus is allocated to ADC0
2	ACMP0	The bus is allocated to ACMP0

Bit	Name	Reset	Access	Description
	3	ACMP1		The bus is allocated to ACMP1
	4	VDAC0CH1		The bus is allocated to VDAC0 CH1
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	AEVEN0	0x0	RW	**A Bus Even 0**

peripheral allocation to A Bus Even 0

Value	Mode	Description
0	TRISTATE	The bus is not allocated
1	ADC0	The bus is allocated to ADC0
2	ACMP0	The bus is allocated to ACMP0
3	ACMP1	The bus is allocated to ACMP1
4	VDAC0CH0	The bus is allocated to VDAC0 CH0

24.6.24 GPIO_BBUSALLOC - B Bus Allocation

Offset	Bit Position																													
0x224	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0x0								0x0								0x0								0x0			
Access					RW								RW								RW								RW			
Name					BODD1								BODD0								BEVEN1								BEVEN0			

Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27:24	BODD1	0x0	RW	**B Bus Odd 1**

peripheral allocation to B Bus Odd 1

Value	Mode	Description
0	TRISTATE	The bus is not allocated
1	ADC0	The bus is allocated to ADC0
2	ACMP0	The bus is allocated to ACMP0
3	ACMP1	The bus is allocated to ACMP1
4	VDAC0CH1	The bus is allocated to VDAC0 CH1

23:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	BODD0	0x0	RW	**B Bus Odd 0**

peripheral allocation to B Bus Odd 0

Value	Mode	Description
0	TRISTATE	The bus is not allocated
1	ADC0	The bus is allocated to ADC0
2	ACMP0	The bus is allocated to ACMP0
3	ACMP1	The bus is allocated to ACMP1
4	VDAC0CH0	The bus is allocated to VDAC0 CH0

15:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:8	BEVEN1	0x0	RW	**B Bus Even 1**

peripheral allocation to B Bus Even 1

Value	Mode	Description
0	TRISTATE	The bus is not allocated
1	ADC0	The bus is allocated to ADC0
2	ACMP0	The bus is allocated to ACMP0

Bit	Name	Reset	Access	Description
	3	ACMP1		The bus is allocated to ACMP1
	4	VDAC0CH1		The bus is allocated to VDAC0 CH1
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	BEVEN0	0x0	RW	**B Bus Even 0**
	peripheral allocation to B Bus Even 0			

Value	Mode	Description
0	TRISTATE	The bus is not allocated
1	ADC0	The bus is allocated to ADC0
2	ACMP0	The bus is allocated to ACMP0
3	ACMP1	The bus is allocated to ACMP1
4	VDAC0CH0	The bus is allocated to VDAC0 CH0

24.6.25 GPIO_CDBUSALLOC - CD Bus Allocation

Offset	Bit Position																													
0x228	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0x0								0x0								0x0								0x0			
Access					RW								RW								RW								RW			
Name					CDODD1								CDODD0								CDEVEN1								CDEVEN0			

Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27:24	CDODD1	0x0	RW	**CD Bus Odd 1**
	peripheral allocation to CD Bus Odd 1			

Value	Mode	Description
0	TRISTATE	The bus is not allocated
1	ADC0	The bus is allocated to ADC0
2	ACMP0	The bus is allocated to ACMP0
3	ACMP1	The bus is allocated to ACMP1
4	VDAC0CH1	The bus is allocated to VDAC0 CH1

Bit	Name	Reset	Access	Description
23:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	CDODD0	0x0	RW	**CD Bus Odd 0**
	peripheral allocation to CD Bus Odd 0			

Value	Mode	Description
0	TRISTATE	The bus is not allocated
1	ADC0	The bus is allocated to ADC0
2	ACMP0	The bus is allocated to ACMP0
3	ACMP1	The bus is allocated to ACMP1
4	VDAC0CH0	The bus is allocated to VDAC0 CH0

Bit	Name	Reset	Access	Description
15:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:8	CDEVEN1	0x0	RW	**CD Bus Even 1**
	peripheral allocation to CD Bus Even 1			

Value	Mode	Description
0	TRISTATE	The bus is not allocated
1	ADC0	The bus is allocated to ADC0
2	ACMP0	The bus is allocated to ACMP0

Bit	Name	Reset	Access	Description
	3	ACMP1		The bus is allocated to ACMP1
	4	VDAC0CH1		The bus is allocated to VDAC0 CH1
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	CDEVEN0	0x0	RW	**CD Bus Even 0**

peripheral allocation to CD Bus Even 0

Value	Mode	Description
0	TRISTATE	The bus is not allocated
1	ADC0	The bus is allocated to ADC0
2	ACMP0	The bus is allocated to ACMP0
3	ACMP1	The bus is allocated to ACMP1
4	VDAC0CH0	The bus is allocated to VDAC0 CH0

24.6.26 GPIO_AODD0SWITCH - AODD0 Switch Register

Offset	Bit Position																													
0x230	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0				
Access																											RW				
Name																											AODD0SWITCH				

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:0	AODD0SWITCH	0x0	RW	**AODD0 switch register**

24.6.27 GPIO_AODD1SWITCH - AODD1 Switch Register

Offset	Bit Position																															
0x234	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0					
Access																											RW					
Name																											AODD1SWITCH					

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:0	AODD1SWITCH	0x0	RW	**AODD1 switch register**

24.6.28 GPIO_AEVEN0SWITCH - AEVEN0 Switch Register

Offset	Bit Position																															
0x238	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0					
Access																											RW					
Name																											AEVEN0SWITCH					

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:0	AEVEN0SWITCH	0x0	RW	**AEVEN0 switch register**

24.6.29 GPIO_AEVEN1SWITCH - AEVEN1 Switch Register

Offset	Bit Position																															
0x23C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0					
Access																											RW					
Name																											AEVEN1SWITCH					

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:0	AEVEN1SWITCH	0x0	RW	**AEVEN1 switch register**
	Enables AEVEN1 connection to even numbered PortA pins			

24.6.30 GPIO_BODD0SWITCH - BODD0 Switch Register

Offset	Bit Position																															
0x240	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													BODD0SWITCH			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	BODD0SWITCH	0x0	RW	**BODD0 Switch Reg**
	Enables BODD0 connection to odd numbered PortB pins			

24.6.31 GPIO_BODD1SWITCH - BODD1 Switch Register

Offset	Bit Position																															
0x244	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													RW			
Name																													BODD1SWITCH			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	BODD1SWITCH	0x0	RW	**BODD1 Switch Reg**
	Enables BODD1 connection to odd numbered PortB pins			

24.6.32 GPIO_BEVEN0SWITCH - BEVEN0 Switch Register

Offset	Bit Position																															
0x248	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x0		
Access																														RW		
Name																														BEVEN0SWITCH		

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4:0	BEVEN0SWITCH	0x0	RW	**BEVEN0 switch register**
	Enables BEVEN0 connection to even numbered PortB pins			

24.6.33 GPIO_BEVEN1SWITCH - BEVEN1 Switch Register

Offset	Bit Position																															
0x24C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0				
Access																												RW				
Name																												BEVEN1SWITCH				

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4:0	BEVEN1SWITCH	0x0	RW	**BEVEN1 switch register**
	Enables BEVEN1 connection to even numbered PortB pins			

24.6.34 GPIO_CDODD0SWITCH - CDODD0 Switch Register

Offset	Bit Position																															
0x250	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0															0x0				
Access													RW															RW				
Name													DODD0SWITCH															CODD0SWITCH				

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	DODD0SWITCH	0x0	RW	**DODD0 switch register**
	Enables CDODD0 connection to odd numbered PortD pins			
15:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4:0	CODD0SWITCH	0x0	RW	**CODD0 switch register**
	Enables CDODD0 connection to odd numbered PortC pins			

24.6.35 GPIO_CDODD1SWITCH - CDODD1 Switch Register

Offset	Bit Position																													
0x254	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0															0x0				
Access													RW															RW				
Name													DODD1SWITCH															CODD1SWITCH				

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	DODD1SWITCH	0x0	RW	**DODD1 switch register**
	Enables CDODD1 connection to odd numbered PortD pins			
15:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4:0	CODD1SWITCH	0x0	RW	**CODD1 switch register**
	Enables CDODD1 connection to odd numbered PortC pins			

24.6.36 GPIO_CDEVEN0SWITCH - CDEVEN0 Switch Register

Offset	Bit Position																													
0x258	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0															0x0				
Access													RW															RW				
Name													DEVEN0SWITCH															CEVEN0SWITCH				

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	DEVEN0SWITCH	0x0	RW	**DEVEN0 switch register**
	Enables CDEVEN0 connection to even numbered PortD pins			
15:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:0	CEVEN0SWITCH	0x0	RW	**CEVEN0 switch register**
	Enables CDEVEN0 connection to even numbered PortC pins			

24.6.37 GPIO_CDEVEN1SWITCH - CDEVEN1 Switch Register

Offset	Bit Position																													
0x25C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0														0x0					
Access													RW														RW					
Name													DEVEN1SWITCH														CEVEN1SWITCH					

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	DEVEN1SWITCH	0x0	RW	**DEVEN1 switch register**
	Enables CDEVEN1 connection to even numbered PortD pins			
15:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:0	CEVEN1SWITCH	0x0	RW	**CEVEN1 switch register**
	Enables CDEVEN1 connection to even numbered PortC pins			

24.6.38 GPIO_EXTIPSELL - External Interrupt Port Select Low

Offset	Bit Position																											
0x300	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset			0x0				0x0				0x0				0x0				0x0				0x0				0x0				0x0	
Access			RW				RW				RW				RW				RW				RW				RW				RW	
Name			EXTIPSEL7				EXTIPSEL6				EXTIPSEL5				EXTIPSEL4				EXTIPSEL3				EXTIPSEL2				EXTIPSEL1				EXTIPSEL0	

Bit	Name	Reset	Access	Description
31:30	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
29:28	EXTIPSEL7	0x0	RW	**External Interrupt Port Select**
	Port select for external interrupt 7 (EXTI7)			
	Value	Mode		Description
	0	PORTA		Port A group selected
	1	PORTB		Port B group selected
	2	PORTC		Port C group selected
	3	PORTD		Port D group selected
27:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25:24	EXTIPSEL6	0x0	RW	**External Interrupt Port Select**
	Port select for external interrupt 6 (EXTI6)			
	Value	Mode		Description
	0	PORTA		Port A group selected
	1	PORTB		Port B group selected
	2	PORTC		Port C group selected
	3	PORTD		Port D group selected
23:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21:20	EXTIPSEL5	0x0	RW	**External Interrupt Port Select**
	Port select for external interrupt 5 (EXTI5)			
	Value	Mode		Description
	0	PORTA		Port A group selected
	1	PORTB		Port B group selected
	2	PORTC		Port C group selected
	3	PORTD		Port D group selected

Bit	Name	Reset	Access	Description
19:18	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
17:16	EXTIPSEL4	0x0	RW	**External Interrupt Port Select**
	Port select for external interrupt 4 (EXTI4)			

Value	Mode	Description
0	PORTA	Port A group selected
1	PORTB	Port B group selected
2	PORTC	Port C group selected
3	PORTD	Port D group selected

Bit	Name	Reset	Access	Description
15:14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13:12	EXTIPSEL3	0x0	RW	**External Interrupt Port Select**
	Port select for external interrupt 3 (EXTI3)			

Value	Mode	Description
0	PORTA	Port A group selected
1	PORTB	Port B group selected
2	PORTC	Port C group selected
3	PORTD	Port D group selected

Bit	Name	Reset	Access	Description
11:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	EXTIPSEL2	0x0	RW	**External Interrupt Port Select**
	Port select for external interrupt 2 (EXTI2)			

Value	Mode	Description
0	PORTA	Port A group selected
1	PORTB	Port B group selected
2	PORTC	Port C group selected
3	PORTD	Port D group selected

Bit	Name	Reset	Access	Description
7:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:4	EXTIPSEL1	0x0	RW	**External Interrupt Port Select**
	Port select for external interrupt 1 (EXTI1)			

Value	Mode	Description
0	PORTA	Port A group selected
1	PORTB	Port B group selected
2	PORTC	Port C group selected
3	PORTD	Port D group selected

Bit	Name	Reset	Access	Description
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	EXTIPSEL0	0x0	RW	**External Interrupt Port Select** Port select for external interrupt 0 (EXTI0)

Value	Mode	Description
0	PORTA	Port A group selected
1	PORTB	Port B group selected
2	PORTC	Port C group selected
3	PORTD	Port D group selected

24.6.39 GPIO_EXTIPSELH - External Interrupt Port Select High

Offset	Bit Position																													
0x304	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																			0x0				0x0				0x0				0x0	
Access																			RW				RW				RW				RW	
Name																			EXTIPSEL3				EXTIPSEL2				EXTIPSEL1				EXTIPSEL0	

Bit	Name	Reset	Access	Description
31:14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13:12	EXTIPSEL3	0x0	RW	**External Interrupt Port Select**
	Port select for external interrupt 3+8			
	Value	Mode		Description
	0	PORTA		Port A group selected
	1	PORTB		Port B group selected
	2	PORTC		Port C group selected
	3	PORTD		Port D group selected
11:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	EXTIPSEL2	0x0	RW	**External Interrupt Port Select**
	Port select for external interrupt 2+8			
	Value	Mode		Description
	0	PORTA		Port A group selected
	1	PORTB		Port B group selected
	2	PORTC		Port C group selected
	3	PORTD		Port D group selected
7:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:4	EXTIPSEL1	0x0	RW	**External Interrupt Port Select**
	Port select for external interrupt 1+8			
	Value	Mode		Description
	0	PORTA		Port A group selected
	1	PORTB		Port B group selected
	2	PORTC		Port C group selected
	3	PORTD		Port D group selected

Bit	Name	Reset	Access	Description
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	EXTIPSEL0	0x0	RW	**External Interrupt Port Select** Port select for external interrupt 0+8

Value	Mode	Description
0	PORTA	Port A group selected
1	PORTB	Port B group selected
2	PORTC	Port C group selected
3	PORTD	Port D group selected

24.6.40 GPIO_EXTIPINSELL - External Interrupt Pin Select Low

Offset	Bit Position																													
0x308	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset			0x0				0x0				0x0				0x0				0x0				0x0				0x0				0x0	
Access			RW				RW				RW				RW				RW				RW				RW				RW	
Name			EXTIPINSEL7				EXTIPINSEL6				EXTIPINSEL5				EXTIPINSEL4				EXTIPINSEL3				EXTIPINSEL2				EXTIPINSEL1				EXTIPINSEL0	

Bit	Name	Reset	Access	Description
31:30	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
29:28	EXTIPINSEL7	0x0	RW	**External Interrupt Pin select**
	OFFSET select for External Interrupt 7 (EXTI7)			
	Value	Mode		Description
	0	PIN0		OFFSET=0
	1	PIN1		OFFSET=1
	2	PIN2		OFFSET=2
	3	PIN3		OFFSET=3
27:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25:24	EXTIPINSEL6	0x0	RW	**External Interrupt Pin select**
	OFFSET select for External Interrupt 6 (EXTI6)			
	Value	Mode		Description
	0	PIN0		OFFSET=0
	1	PIN1		OFFSET=1
	2	PIN2		OFFSET=2
	3	PIN3		OFFSET=3
23:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21:20	EXTIPINSEL5	0x0	RW	**External Interrupt Pin select**
	OFFSET select for External Interrupt 5 (EXTI5)			
	Value	Mode		Description
	0	PIN0		OFFSET=0
	1	PIN1		OFFSET=1
	2	PIN2		OFFSET=2
	3	PIN3		OFFSET=3

Bit	Name	Reset	Access	Description
19:18	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
17:16	EXTIPINSEL4	0x0	RW	**External Interrupt Pin select**
	OFFSET select for External Interrupt 4 (EXTI4)			

Value	Mode	Description
0	PIN0	OFFSET=0
1	PIN1	OFFSET=1
2	PIN2	OFFSET=2
3	PIN3	OFFSET=3

Bit	Name	Reset	Access	Description
15:14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13:12	EXTIPINSEL3	0x0	RW	**External Interrupt Pin select**
	OFFSET select for External Interrupt 3 (EXTI3)			

Value	Mode	Description
0	PIN0	OFFSET=0
1	PIN1	OFFSET=1
2	PIN2	OFFSET=2
3	PIN3	OFFSET=3

Bit	Name	Reset	Access	Description
11:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	EXTIPINSEL2	0x0	RW	**External Interrupt Pin select**
	OFFSET select for External Interrupt 2 (EXTI2)			

Value	Mode	Description
0	PIN0	OFFSET=0
1	PIN1	OFFSET=1
2	PIN2	OFFSET=2
3	PIN3	OFFSET=3

Bit	Name	Reset	Access	Description
7:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:4	EXTIPINSEL1	0x0	RW	**External Interrupt Pin select**
	OFFSET select for External Interrupt 1 (EXTI1)			

Value	Mode	Description
0	PIN0	OFFSET=0
1	PIN1	OFFSET=1
2	PIN2	OFFSET=2
3	PIN3	OFFSET=3

Bit	Name	Reset	Access	Description
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	EXTIPINSEL0	0x0	RW	**External Interrupt Pin select**

OFFSET select for External Interrupt 0 (EXTI0)

Value	Mode	Description
0	PIN0	OFFSET=0
1	PIN1	OFFSET=1
2	PIN2	OFFSET=2
3	PIN3	OFFSET=3

24.6.41 GPIO_EXTIPINSELH - External Interrupt Pin Select High

Offset	Bit Position																													
0x30C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																			0x0				0x0				0x0				0x0	
Access																			RW				RW				RW				RW	
Name																			EXTIPINSEL3				EXTIPINSEL2				EXTIPINSEL1				EXTIPINSEL0	

Bit	Name	Reset	Access	Description
31:14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13:12	EXTIPINSEL3	0x0	RW	**External Interrupt Pin select**
	OFFSET select for External Interrupt {b+8} (EXTI{b+8})			
	Value	Mode		Description
	0	PIN8		OFFSET=8
	1	PIN9		OFFSET=9
	2	PIN10		OFFSET=10
	3	PIN11		OFFSET=11
11:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	EXTIPINSEL2	0x0	RW	**External Interrupt Pin select**
	OFFSET select for External Interrupt {b+8} (EXTI{b+8})			
	Value	Mode		Description
	0	PIN8		OFFSET=8
	1	PIN9		OFFSET=9
	2	PIN10		OFFSET=10
	3	PIN11		OFFSET=11
7:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:4	EXTIPINSEL1	0x0	RW	**External Interrupt Pin select**
	OFFSET select for External Interrupt {b+8} (EXTI{b+8})			
	Value	Mode		Description
	0	PIN8		OFFSET=8
	1	PIN9		OFFSET=9
	2	PIN10		OFFSET=10
	3	PIN11		OFFSET=11

Bit	Name	Reset	Access	Description
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	EXTIPINSEL0	0x0	RW	**External Interrupt Pin select**
	OFFSET select for External Interrupt {b+8} (EXTI{b+8})			

Value	Mode	Description
0	PIN8	OFFSET=8
1	PIN9	OFFSET=9
2	PIN10	OFFSET=10
3	PIN11	OFFSET=11

24.6.42 GPIO_EXTIRISE - External Interrupt Rising Edge Trigger

Offset	Bit Position																														
0x310	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																					0x0											
Access																					RW											
Name																					EXTIRISE											

Bit	Name	Reset	Access	Description
31:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:0	EXTIRISE	0x0	RW	**EXT Int Rise**
	External Interrupt n Rising Edge Trigger Enable			

24.6.43 GPIO_EXTIFALL - External Interrupt Falling Edge Trigger

Offset	Bit Position																															
0x314	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0					
Access																											RW					
Name																											EXTIFALL					

Bit	Name	Reset	Access	Description
31:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:0	EXTIFALL	0x0	RW	**EXT Int FALL**
	External Interrupt n Falling Edge Trigger Enable			

24.6.44 GPIO_IF - Interrupt Flag

Offset	Bit Position																													
0x320	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0x0																0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access					RW																RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name					EM4WU																EXTIF11	EXTIF10	EXTIF9	EXTIF8	EXTIF7	EXTIF6	EXTIF5	EXTIF4	EXTIF3	EXTIF2	EXTIF1	EXTIF0

Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27:16	EM4WU	0x0	RW	**EM4 wake up**
15:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11	EXTIF11 External Pin interrupt flag	0x0	RW	**External Pin Flag**
10	EXTIF10 External Pin interrupt flag	0x0	RW	**External Pin Flag**
9	EXTIF9 External Pin interrupt flag	0x0	RW	**External Pin Flag**
8	EXTIF8 External Pin interrupt flag	0x0	RW	**External Pin Flag**
7	EXTIF7 External Pin interrupt flag	0x0	RW	**External Pin Flag**
6	EXTIF6 External Pin interrupt flag	0x0	RW	**External Pin Flag**
5	EXTIF5 External Pin interrupt flag	0x0	RW	**External Pin Flag**
4	EXTIF4 External Pin interrupt flag	0x0	RW	**External Pin Flag**
3	EXTIF3 External Pin interrupt flag	0x0	RW	**External Pin Flag**
2	EXTIF2 External Pin interrupt flag	0x0	RW	**External Pin Flag**
1	EXTIF1 External Pin interrupt flag	0x0	RW	**External Pin Flag**
0	EXTIF0	0x0	RW	**External Pin Flag**

Bit	Name	Reset	Access	Description
	External Pin interrupt flag			

24.6.45 GPIO_IEN - Interrupt Enable

Offset	Bit Position																													
0x324	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0					0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name					EM4WUIEN11	EM4WUIEN10	EM4WUIEN9	EM4WUIEN8	EM4WUIEN7	EM4WUIEN6	EM4WUIEN5	EM4WUIEN4	EM4WUIEN3	EM4WUIEN2	EM4WUIEN1	EM4WUIEN0					EXTIEN11	EXTIEN10	EXTIEN9	EXTIEN8	EXTIEN7	EXTIEN6	EXTIEN5	EXTIEN4	EXTIEN3	EXTIEN2	EXTIEN1	EXTIEN0

Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27	EM4WUIEN11	0x0	RW	**EM4 Wake Up Interrupt En**
	EM4 wakeup interrupt enable			
26	EM4WUIEN10	0x0	RW	**EM4 Wake Up Interrupt En**
	EM4 wakeup interrupt enable			
25	EM4WUIEN9	0x0	RW	**EM4 Wake Up Interrupt En**
	EM4 wakeup interrupt enable			
24	EM4WUIEN8	0x0	RW	**EM4 Wake Up Interrupt En**
	EM4 wakeup interrupt enable			
23	EM4WUIEN7	0x0	RW	**EM4 Wake Up Interrupt En**
	EM4 wakeup interrupt enable			
22	EM4WUIEN6	0x0	RW	**EM4 Wake Up Interrupt En**
	EM4 wakeup interrupt enable			
21	EM4WUIEN5	0x0	RW	**EM4 Wake Up Interrupt En**
	EM4 wakeup interrupt enable			
20	EM4WUIEN4	0x0	RW	**EM4 Wake Up Interrupt En**
	EM4 wakeup interrupt enable			
19	EM4WUIEN3	0x0	RW	**EM4 Wake Up Interrupt En**
	EM4 wakeup interrupt enable			
18	EM4WUIEN2	0x0	RW	**EM4 Wake Up Interrupt En**
	EM4 wakeup interrupt enable			
17	EM4WUIEN1	0x0	RW	**EM4 Wake Up Interrupt En**
	EM4 wakeup interrupt enable			
16	EM4WUIEN0	0x0	RW	**EM4 Wake Up Interrupt En**
	EM4 wakeup interrupt enable			
15:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

Bit	Name	Reset	Access	Description
11	EXTIEN11	0x0	RW	**External Pin Enable**
	External Pin interrupt enable			
10	EXTIEN10	0x0	RW	**External Pin Enable**
	External Pin interrupt enable			
9	EXTIEN9	0x0	RW	**External Pin Enable**
	External Pin interrupt enable			
8	EXTIEN8	0x0	RW	**External Pin Enable**
	External Pin interrupt enable			
7	EXTIEN7	0x0	RW	**External Pin Enable**
	External Pin interrupt enable			
6	EXTIEN6	0x0	RW	**External Pin Enable**
	External Pin interrupt enable			
5	EXTIEN5	0x0	RW	**External Pin Enable**
	External Pin interrupt enable			
4	EXTIEN4	0x0	RW	**External Pin Enable**
	External Pin interrupt enable			
3	EXTIEN3	0x0	RW	**External Pin Enable**
	External Pin interrupt enable			
2	EXTIEN2	0x0	RW	**External Pin Enable**
	External Pin interrupt enable			
1	EXTIEN1	0x0	RW	**External Pin Enable**
	External Pin interrupt enable			
0	EXTIEN0	0x0	RW	**External Pin Enable**
	External Pin interrupt enable			

24.6.46 GPIO_EM4WUEN - EM4 Wakeup Enable

Offset	Bit Position																													
0x32C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0x0																											
Access					RW																											
Name					EM4WUEN																											

Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27:16	EM4WUEN	0x0	RW	**EM4 wake up enable**
	Write 1 to enable EM4 wake up request, write 0 to disable EM4 wake up request			
15:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

24.6.47 GPIO_EM4WUPOL - EM4 Wakeup Polarity

Offset	Bit Position																													
0x330	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0x0																											
Access					RW																											
Name					EM4WUPOL																											

Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27:16	EM4WUPOL	0x0	RW	**EM4 Wake-Up Polarity**
	EM4 Wakeup Polarity			
15:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

24.6.48 GPIO_DBGROUTEPEN - Debugger Route Pin Enable

Offset	Bit Position																													
0x340	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x1	0x1	0x1	0x1
Access																													RW	RW	RW	RW
Name																													TDIPEN	TDOPEN	SWDIOTMSPEN	SWCLKTCKPEN

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	TDIPEN	0x1	RW	**JTAG Test Debug Input Pin Enable**
	Enable JTAG TDI connection to pin.			
2	TDOPEN	0x1	RW	**JTAG Test Debug Output Pin Enable**
	Enable JTAG TDO connection to pin.			
1	SWDIOTMSPEN	0x1	RW	**Route Location 0**
	Enable Serial Wire Data and JTAG Test Mode Select connection to pin. WARNING: When the pin is disabled, the device can no longer be accessed by a debugger. A reset will set the pin back to a default state as enabled. If you disable this pin, make sure you have at least a 3 second timeout at the start of your program code before you disable the pin. This way, the debugger will have time to halt the device after a reset before the pin is disabled.			
0	SWCLKTCKPEN	0x1	RW	**Route Pin Enable**
	Enable Serial Wire and JTAG CLock connection to pin. WARNING: When the pin is disabled, the device can no longer be accessed by a debugger. A reset will set the pin back to a default state as enabled. If you disable this pin, make sure you have at least a 3 second timeout at the start of your program code before you disable the pin. This way, the debugger will have time to halt the device after a reset before the pin is disabled.			

24.6.49 GPIO_TRACEROUTEPEN - Trace Route Pin Enable

Offset	Bit Position																													
0x344	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0	0x0	0x0	0x0	0x0	0x0
Access																											RW	RW	RW	RW	RW	RW
Name																											TRACEDATA3PEN	TRACEDATA2PEN	TRACEDATA1PEN	TRACEDATA0PEN	TRACECLKPEN	SWVPEN

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	TRACEDATA3PEN	0x0	RW	**Trace Data3 Pin Enable**
	Trace Data3 Pin Enable			
4	TRACEDATA2PEN	0x0	RW	**Trace Data2 Pin Enable**
	Trace Data2 Pin Enable			
3	TRACEDATA1PEN	0x0	RW	**Trace Data1 Pin Enable**
	Trace Data1 Pin Enable			
2	TRACEDATA0PEN	0x0	RW	**Trace Data0 Pin Enable**
	Trace Data0 Pin Enable			
1	TRACECLKPEN	0x0	RW	**Trace Clk Pin Enable**
	Trace Clk Pin Enable			
0	SWVPEN	0x0	RW	**Serial Wire Viewer Output Pin Enable**
	Serial Wire Viewer Output Pin Enable			

24.6.50 GPIO_FEMROUTEPEN - FEM Route Pin Enable

Offset	Bit Position																															
0x348	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0	0x0	0x0	0x0
Access																													RW	RW	RW	RW
Name																													FEMDATA3PEN	FEMDATA2PEN	FEMDATA1PEN	FEMDATA0PEN

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	FEMDATA3PEN	0x0	RW	**FEM Data3 Pin Enable**
	FEM Data3 Pin Enable			
2	FEMDATA2PEN	0x0	RW	**FEM Data2 Pin Enable**
	FEM Data2 Pin Enable			
1	FEMDATA1PEN	0x0	RW	**FEM Data1 Pin Enable**
	FEM Data1 Pin Enable			
0	FEMDATA0PEN	0x0	RW	**FEM Data0 Pin Enable**
	FEM Data0 Pin Enable			

24.6.51 GPIO_ACMP0_ROUTEEN - ACMP0 Pin Enable

Offset	Bit Position																															
0x350	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																RW
Name																																ACMPOUTPEN

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	ACMPOUTPEN	0x0	RW	**ACMPOUT pin enable control bit**
	ACMPOUT pin enable control bit			

24.6.52 GPIO_ACMP0_ACMPOUTROUTE - ACMPOUT Port/Pin Select

Offset	Bit Position																													
0x354	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ACMPOUT pin select register**
	ACMPOUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ACMPOUT port select register**
	ACMPOUT port select register			

24.6.53 GPIO_ACMP1_ROUTEEN - ACMP1 Pin Enable

Offset	Bit Position																													
0x35C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																RW
Name																																ACMPOUTPEN

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	ACMPOUTPEN	0x0	RW	**ACMPOUT pin enable control bit**
	ACMPOUT pin enable control bit			

24.6.54 GPIO_ACMP1_ACMPOUTROUTE - ACMPOUT Port/Pin Select

Offset	Bit Position																													
0x360	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ACMPOUT pin select register**
	ACMPOUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ACMPOUT port select register**
	ACMPOUT port select register			

24.6.55 GPIO_CMU_ROUTEEN - CMU Pin Enable

Offset	Bit Position																													
0x368	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x0	0x0	0x0
Access																														RW	RW	RW
Name																														CLKOUT2PEN	CLKOUT1PEN	CLKOUT0PEN

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	CLKOUT2PEN	0x0	RW	**CLKOUT2 pin enable control bit**
	CLKOUT2 pin enable control bit			
1	CLKOUT1PEN	0x0	RW	**CLKOUT1 pin enable control bit**
	CLKOUT1 pin enable control bit			
0	CLKOUT0PEN	0x0	RW	**CLKOUT0 pin enable control bit**
	CLKOUT0 pin enable control bit			

24.6.56 GPIO_CMU_CLKIN0ROUTE - CLKIN0 Port/Pin Select

Offset	Bit Position																													
0x36C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CLKIN0 pin select register**
	CLKIN0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CLKIN0 port select register**
	CLKIN0 port select register			

24.6.57 GPIO_CMU_CLKOUT0ROUTE - CLKOUT0 Port/Pin Select

Offset	Bit Position																													
0x370	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CLKOUT0 pin select register**
	CLKOUT0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CLKOUT0 port select register**
	CLKOUT0 port select register			

24.6.58 GPIO_CMU_CLKOUT1ROUTE - CLKOUT1 Port/Pin Select

Offset	Bit Position																													
0x374	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CLKOUT1 pin select register**
	CLKOUT1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CLKOUT1 port select register**
	CLKOUT1 port select register			

24.6.59 GPIO_CMU_CLKOUT2ROUTE - CLKOUT2 Port/Pin Select

Offset	Bit Position																													
0x378	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CLKOUT2 pin select register**
	CLKOUT2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CLKOUT2 port select register**
	CLKOUT2 port select register			

24.6.60 GPIO_DCDC_ROUTEEN - DCDC Pin Enable

Offset	Bit Position																														
0x384	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																RW
Name																																DCDCCOREHIDDENPEN

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	DCDCCOREHIDDENPEN DCDCCOREHIDDEN pin enable control bit	0x0	RW	**DCDCCOREHIDDEN pin enable control bit**

24.6.61 GPIO_EUSART0_ROUTEEN - EUSART0 Pin Enable

Offset	Bit Position																													
0x394	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												RW	RW	RW	RW	RW
Name																												TXPEN	SCLKPEN	RXPEN	RTSPEN	CSPEN

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	TXPEN	0x0	RW	**TX pin enable control bit**
	TX pin enable control bit			
3	SCLKPEN	0x0	RW	**SCLK pin enable control bit**
	SCLK pin enable control bit			
2	RXPEN	0x0	RW	**RX pin enable control bit**
	RX pin enable control bit			
1	RTSPEN	0x0	RW	**RTS pin enable control bit**
	RTS pin enable control bit			
0	CSPEN	0x0	RW	**CS pin enable control bit**
	CS pin enable control bit			

24.6.62 GPIO_EUSART0_CSROUTE - CS Port/Pin Select

Offset	Bit Position																													
0x398	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CS pin select register**
	CS pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CS port select register**
	CS port select register			

24.6.63 GPIO_EUSART0_CTSROUTE - CTS Port/Pin Select

Offset	Bit Position																													
0x39C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CTS pin select register**
	CTS pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CTS port select register**
	CTS port select register			

24.6.64 GPIO_EUSART0_RTSROUTE - RTS Port/Pin Select

Offset	Bit Position																													
0x3A0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**RTS pin select register**
	RTS pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**RTS port select register**
	RTS port select register			

24.6.65 GPIO_EUSART0_RXROUTE - RX Port/Pin Select

Offset	Bit Position																													
0x3A4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**RX pin select register**
	RX pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**RX port select register**
	RX port select register			

24.6.66 GPIO_EUSART0_SCLKROUTE - SCLK Port/Pin Select

Offset	Bit Position																													
0x3A8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**SCLK pin select register**
	SCLK pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**SCLK port select register**
	SCLK port select register			

24.6.67 GPIO_EUSART0_TXROUTE - TX Port/Pin Select

Offset	Bit Position																													
0x3AC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**TX pin select register**
	TX pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**TX port select register**
	TX port select register			

24.6.68 GPIO_EUSART1_ROUTEEN - EUSART1 Pin Enable

Offset	Bit Position																													
0x3B4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												RW	RW	RW	RW	RW
Name																												TXPEN	SCLKPEN	RXPEN	RTSPEN	CSPEN

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	TXPEN	0x0	RW	**TX pin enable control bit**
	TX pin enable control bit			
3	SCLKPEN	0x0	RW	**SCLK pin enable control bit**
	SCLK pin enable control bit			
2	RXPEN	0x0	RW	**RX pin enable control bit**
	RX pin enable control bit			
1	RTSPEN	0x0	RW	**RTS pin enable control bit**
	RTS pin enable control bit			
0	CSPEN	0x0	RW	**CS pin enable control bit**
	CS pin enable control bit			

24.6.69 GPIO_EUSART1_CSROUTE - CS Port/Pin Select

Offset	Bit Position																													
0x3B8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CS pin select register**
	CS pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CS port select register**
	CS port select register			

24.6.70 GPIO_EUSART1_CTSROUTE - CTS Port/Pin Select

Offset	Bit Position																													
0x3BC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CTS pin select register**
	CTS pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CTS port select register**
	CTS port select register			

24.6.71 GPIO_EUSART1_RTSROUTE - RTS Port/Pin Select

Offset	Bit Position																													
0x3C0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**RTS pin select register**
	RTS pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**RTS port select register**
	RTS port select register			

24.6.72 GPIO_EUSART1_RXROUTE - RX Port/Pin Select

Offset	Bit Position																													
0x3C4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**RX pin select register**
	RX pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**RX port select register**
	RX port select register			

24.6.73 GPIO_EUSART1_SCLKROUTE - SCLK Port/Pin Select

Offset	Bit Position																													
0x3C8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**SCLK pin select register**
	SCLK pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**SCLK port select register**
	SCLK port select register			

24.6.74 GPIO_EUSART1_TXROUTE - TX Port/Pin Select

Offset	Bit Position																													
0x3CC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**TX pin select register**
	TX pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**TX port select register**
	TX port select register			

24.6.75 GPIO_EUSART2_ROUTEEN - EUSART2 Pin Enable

Offset	Bit Position																													
0x3D4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												RW	RW	RW	RW	RW
Name																												TXPEN	SCLKPEN	RXPEN	RTSPEN	CSPEN

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	TXPEN	0x0	RW	**TX pin enable control bit**
	TX pin enable control bit			
3	SCLKPEN	0x0	RW	**SCLK pin enable control bit**
	SCLK pin enable control bit			
2	RXPEN	0x0	RW	**RX pin enable control bit**
	RX pin enable control bit			
1	RTSPEN	0x0	RW	**RTS pin enable control bit**
	RTS pin enable control bit			
0	CSPEN	0x0	RW	**CS pin enable control bit**
	CS pin enable control bit			

24.6.76 GPIO_EUSART2_CSROUTE - CS Port/Pin Select

Offset	Bit Position																													
0x3D8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CS pin select register**
	CS pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CS port select register**
	CS port select register			

24.6.77 GPIO_EUSART2_CTSROUTE - CTS Port/Pin Select

Offset	Bit Position																													
0x3DC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CTS pin select register**
	CTS pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CTS port select register**
	CTS port select register			

24.6.78 GPIO_EUSART2_RTSROUTE - RTS Port/Pin Select

Offset	Bit Position																													
0x3E0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**RTS pin select register**
	RTS pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**RTS port select register**
	RTS port select register			

24.6.79 GPIO_EUSART2_RXROUTE - RX Port/Pin Select

Offset	Bit Position																													
0x3E4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**RX pin select register**
	RX pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**RX port select register**
	RX port select register			

24.6.80 GPIO_EUSART2_SCLKROUTE - SCLK Port/Pin Select

Offset	Bit Position																													
0x3E8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**SCLK pin select register**
	SCLK pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**SCLK port select register**
	SCLK port select register			

24.6.81 GPIO_EUSART2_TXROUTE - TX Port/Pin Select

Offset	Bit Position																													
0x3EC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**TX pin select register**
	TX pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**TX port select register**
	TX port select register			

24.6.82 GPIO_EUSART3_ROUTEEN - EUSART3 Pin Enable

Offset	Bit Position																													
0x3F4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												RW	RW	RW	RW	RW
Name																												TXPEN	SCLKPEN	RXPEN	RTSPEN	CSPEN

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	TXPEN	0x0	RW	**TX pin enable control bit**
	TX pin enable control bit			
3	SCLKPEN	0x0	RW	**SCLK pin enable control bit**
	SCLK pin enable control bit			
2	RXPEN	0x0	RW	**RX pin enable control bit**
	RX pin enable control bit			
1	RTSPEN	0x0	RW	**RTS pin enable control bit**
	RTS pin enable control bit			
0	CSPEN	0x0	RW	**CS pin enable control bit**
	CS pin enable control bit			

24.6.83 GPIO_EUSART3_CSROUTE - CS Port/Pin Select

Offset	Bit Position																													
0x3F8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CS pin select register**
	CS pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CS port select register**
	CS port select register			

24.6.84 GPIO_EUSART3_CTSROUTE - CTS Port/Pin Select

Offset	Bit Position																													
0x3FC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CTS pin select register**
	CTS pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CTS port select register**
	CTS port select register			

24.6.85 GPIO_EUSART3_RTSROUTE - RTS Port/Pin Select

Offset	Bit Position																													
0x400	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**RTS pin select register**
	RTS pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**RTS port select register**
	RTS port select register			

24.6.86 GPIO_EUSART3_RXROUTE - RX Port/Pin Select

Offset	Bit Position																													
0x404	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**RX pin select register**
	RX pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**RX port select register**
	RX port select register			

24.6.87 GPIO_EUSART3_SCLKROUTE - SCLK Port/Pin Select

Offset	Bit Position																													
0x408	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**SCLK pin select register**
	SCLK pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**SCLK port select register**
	SCLK port select register			

24.6.88 GPIO_EUSART3_TXROUTE - TX Port/Pin Select

Offset	Bit Position																													
0x40C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**TX pin select register**
	TX pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**TX port select register**
	TX port select register			

24.6.89 GPIO_EUSART4_ROUTEEN - EUSART4 Pin Enable

Offset	Bit Position																													
0x414	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												RW	RW	RW	RW	RW
Name																												TXPEN	SCLKPEN	RXPEN	RTSPEN	CSPEN

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	TXPEN	0x0	RW	**TX pin enable control bit**
	TX pin enable control bit			
3	SCLKPEN	0x0	RW	**SCLK pin enable control bit**
	SCLK pin enable control bit			
2	RXPEN	0x0	RW	**RX pin enable control bit**
	RX pin enable control bit			
1	RTSPEN	0x0	RW	**RTS pin enable control bit**
	RTS pin enable control bit			
0	CSPEN	0x0	RW	**CS pin enable control bit**
	CS pin enable control bit			

24.6.90 GPIO_EUSART4_CSROUTE - CS Port/Pin Select

Offset	Bit Position																													
0x418	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CS pin select register**
	CS pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CS port select register**
	CS port select register			

24.6.91 GPIO_EUSART4_CTSROUTE - CTS Port/Pin Select

Offset	Bit Position																													
0x41C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CTS pin select register**
	CTS pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CTS port select register**
	CTS port select register			

24.6.92 GPIO_EUSART4_RTSROUTE - RTS Port/Pin Select

Offset	Bit Position																													
0x420	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**RTS pin select register**
	RTS pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**RTS port select register**
	RTS port select register			

24.6.93 GPIO_EUSART4_RXROUTE - RX Port/Pin Select

Offset	Bit Position																													
0x424	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**RX pin select register**
	RX pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**RX port select register**
	RX port select register			

24.6.94 GPIO_EUSART4_SCLKROUTE - SCLK Port/Pin Select

Offset	Bit Position																													
0x428	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**SCLK pin select register**
	SCLK pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**SCLK port select register**
	SCLK port select register			

24.6.95 GPIO_EUSART4_TXROUTE - TX Port/Pin Select

Offset	Bit Position																													
0x42C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**TX pin select register**
	TX pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**TX port select register**
	TX port select register			

24.6.96 GPIO_FRC_ROUTEEN - FRC Pin Enable

Offset	Bit Position																														
0x434	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x0	0x0	0x0
Access																														RW	RW	RW
Name																														DOUTPEN	DFRAMEPEN	DCLKPEN

Bit	Name	Reset	Access	Description
31:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	DOUTPEN	0x0	RW	**DOUT pin enable control bit**
	DOUT pin enable control bit			
1	DFRAMEPEN	0x0	RW	**DFRAME pin enable control bit**
	DFRAME pin enable control bit			
0	DCLKPEN	0x0	RW	**DCLK pin enable control bit**
	DCLK pin enable control bit			

24.6.97 GPIO_FRC_DCLKROUTE - DCLK Port/Pin Select

Offset	Bit Position																														
0x438	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**DCLK pin select register**
	DCLK pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**DCLK port select register**
	DCLK port select register			

24.6.98 GPIO_FRC_DFRAMEROUTE - DFRAME Port/Pin Select

Offset	Bit Position																													
0x43C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**DFRAME pin select register**
	DFRAME pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**DFRAME port select register**
	DFRAME port select register			

24.6.99 GPIO_FRC_DOUTROUTE - DOUT Port/Pin Select

Offset	Bit Position																													
0x440	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**DOUT pin select register**
	DOUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**DOUT port select register**
	DOUT port select register			

24.6.100 GPIO_I2C0_ROUTEEN - I2C0 Pin Enable

Offset	Bit Position																													
0x448	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															RW	RW
Name																															SDAPEN	SCLPEN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	SDAPEN	0x0	RW	**SDA pin enable control bit**
	SDA pin enable control bit			
0	SCLPEN	0x0	RW	**SCL pin enable control bit**
	SCL pin enable control bit			

24.6.101 GPIO_I2C0_SCLROUTE - SCL Port/Pin Select

Offset	Bit Position																													
0x44C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset														0x0																	0x0	
Access														RW																	RW	
Name														PIN																	PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**SCL pin select register**
	SCL pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**SCL port select register**
	SCL port select register			

24.6.102 GPIO_I2C0_SDAROUTE - SDA Port/Pin Select

Offset	Bit Position																													
0x450	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset														0x0																	0x0	
Access														RW																	RW	
Name														PIN																	PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**SDA pin select register**
	SDA pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**SDA port select register**
	SDA port select register			

24.6.103 GPIO_I2C1_ROUTEEN - I2C1 Pin Enable

Offset	Bit Position																													
0x458	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															RW	RW
Name																															SDAPEN	SCLPEN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	SDAPEN	0x0	RW	**SDA pin enable control bit**
	SDA pin enable control bit			
0	SCLPEN	0x0	RW	**SCL pin enable control bit**
	SCL pin enable control bit			

24.6.104 GPIO_I2C1_SCLROUTE - SCL Port/Pin Select

Offset	Bit Position																													
0x45C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**SCL pin select register**
	SCL pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**SCL port select register**
	SCL port select register			

24.6.105 GPIO_I2C1_SDAROUTE - SDA Port/Pin Select

Offset	Bit Position																													
0x460	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**SDA pin select register**
	SDA pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**SDA port select register**
	SDA port select register			

24.6.106 GPIO_LESENSE_ROUTEEN - LESENSE Pin Enable

Offset	Bit Position																													
0x468	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name																	CH15OUTPEN	CH14OUTPEN	CH13OUTPEN	CH12OUTPEN	CH11OUTPEN	CH10OUTPEN	CH9OUTPEN	CH8OUTPEN	CH7OUTPEN	CH6OUTPEN	CH5OUTPEN	CH4OUTPEN	CH3OUTPEN	CH2OUTPEN	CH1OUTPEN	CH0OUTPEN

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15	CH15OUTPEN	0x0	RW	**CH15OUT pin enable control bit**
	CH15OUT pin enable control bit			
14	CH14OUTPEN	0x0	RW	**CH14OUT pin enable control bit**
	CH14OUT pin enable control bit			
13	CH13OUTPEN	0x0	RW	**CH13OUT pin enable control bit**
	CH13OUT pin enable control bit			
12	CH12OUTPEN	0x0	RW	**CH12OUT pin enable control bit**
	CH12OUT pin enable control bit			
11	CH11OUTPEN	0x0	RW	**CH11OUT pin enable control bit**
	CH11OUT pin enable control bit			
10	CH10OUTPEN	0x0	RW	**CH10OUT pin enable control bit**
	CH10OUT pin enable control bit			
9	CH9OUTPEN	0x0	RW	**CH9OUT pin enable control bit**
	CH9OUT pin enable control bit			
8	CH8OUTPEN	0x0	RW	**CH8OUT pin enable control bit**
	CH8OUT pin enable control bit			
7	CH7OUTPEN	0x0	RW	**CH7OUT pin enable control bit**
	CH7OUT pin enable control bit			
6	CH6OUTPEN	0x0	RW	**CH6OUT pin enable control bit**
	CH6OUT pin enable control bit			
5	CH5OUTPEN	0x0	RW	**CH5OUT pin enable control bit**
	CH5OUT pin enable control bit			
4	CH4OUTPEN	0x0	RW	**CH4OUT pin enable control bit**
	CH4OUT pin enable control bit			
3	CH3OUTPEN	0x0	RW	**CH3OUT pin enable control bit**

Bit	Name	Reset	Access	Description
	CH3OUT pin enable control bit			
2	CH2OUTPEN	0x0	RW	**CH2OUT pin enable control bit**
	CH2OUT pin enable control bit			
1	CH1OUTPEN	0x0	RW	**CH1OUT pin enable control bit**
	CH1OUT pin enable control bit			
0	CH0OUTPEN	0x0	RW	**CH0OUT pin enable control bit**
	CH0OUT pin enable control bit			

24.6.107 GPIO_LESENSE_CH0OUTROUTE - CH0OUT Port/Pin Select

Offset	Bit Position																													
0x46C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CH0OUT pin select register**
	CH0OUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CH0OUT port select register**
	CH0OUT port select register			

24.6.108 GPIO_LESENSE_CH1OUTROUTE - CH1OUT Port/Pin Select

Offset	Bit Position																													
0x470	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CH1OUT pin select register**
	CH1OUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CH1OUT port select register**
	CH1OUT port select register			

24.6.109 GPIO_LESENSE_CH2OUTROUTE - CH2OUT Port/Pin Select

Offset	Bit Position																													
0x474	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CH2OUT pin select register**
	CH2OUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CH2OUT port select register**
	CH2OUT port select register			

24.6.110 GPIO_LESENSE_CH3OUTROUTE - CH3OUT Port/Pin Select

Offset	Bit Position																													
0x478	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CH3OUT pin select register**
	CH3OUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CH3OUT port select register**
	CH3OUT port select register			

24.6.111 GPIO_LESENSE_CH4OUTROUTE - CH4OUT Port/Pin Select

Offset	Bit Position																													
0x47C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CH4OUT pin select register**
	CH4OUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CH4OUT port select register**
	CH4OUT port select register			

24.6.112 GPIO_LESENSE_CH5OUTROUTE - CH5OUT Port/Pin Select

Offset	Bit Position																													
0x480	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CH5OUT pin select register**
	CH5OUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CH5OUT port select register**
	CH5OUT port select register			

24.6.113 GPIO_LESENSE_CH6OUTROUTE - CH6OUT Port/Pin Select

Offset	Bit Position																													
0x484	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CH6OUT pin select register**
	CH6OUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CH6OUT port select register**
	CH6OUT port select register			

24.6.114 GPIO_LESENSE_CH7OUTROUTE - CH7OUT Port/Pin Select

Offset	Bit Position																													
0x488	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CH7OUT pin select register**
	CH7OUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CH7OUT port select register**
	CH7OUT port select register			

24.6.115 GPIO_LESENSE_CH8OUTROUTE - CH8OUT Port/Pin Select

Offset	Bit Position																													
0x48C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CH8OUT pin select register**
	CH8OUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CH8OUT port select register**
	CH8OUT port select register			

24.6.116 GPIO_LESENSE_CH9OUTROUTE - CH9OUT Port/Pin Select

Offset	Bit Position																													
0x490	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CH9OUT pin select register**
	CH9OUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CH9OUT port select register**
	CH9OUT port select register			

24.6.117 GPIO_LESENSE_CH10OUTROUTE - CH10OUT Port/Pin Select

Offset	Bit Position																													
0x494	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CH10OUT pin select register**
	CH10OUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CH10OUT port select register**
	CH10OUT port select register			

24.6.118 GPIO_LESENSE_CH11OUTROUTE - CH11OUT Port/Pin Select

Offset	Bit Position																													
0x498	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CH11OUT pin select register**
	CH11OUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CH11OUT port select register**
	CH11OUT port select register			

24.6.119 GPIO_LESENSE_CH12OUTROUTE - CH12OUT Port/Pin Select

Offset	Bit Position																													
0x49C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CH12OUT pin select register**
	CH12OUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CH12OUT port select register**
	CH12OUT port select register			

24.6.120 GPIO_LESENSE_CH13OUTROUTE - CH13OUT Port/Pin Select

Offset	Bit Position																													
0x4A0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CH13OUT pin select register**
	CH13OUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CH13OUT port select register**
	CH13OUT port select register			

24.6.121 GPIO_LESENSE_CH14OUTROUTE - CH14OUT Port/Pin Select

Offset	Bit Position																													
0x4A4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CH14OUT pin select register**
	CH14OUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CH14OUT port select register**
	CH14OUT port select register			

24.6.122 GPIO_LESENSE_CH15OUTROUTE - CH15OUT Port/Pin Select

Offset	Bit Position																													
0x4A8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CH15OUT pin select register**
	CH15OUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CH15OUT port select register**
	CH15OUT port select register			

24.6.123 GPIO_LETIMER_ROUTEEN - LETIMER Pin Enable

Offset	Bit Position																													
0x4B0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															RW	RW
Name																															OUT1PEN	OUT0PEN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	OUT1PEN	0x0	RW	**OUT1 pin enable control bit**
	OUT1 pin enable control bit			
0	OUT0PEN	0x0	RW	**OUT0 pin enable control bit**
	OUT0 pin enable control bit			

24.6.124 GPIO_LETIMER_OUT0ROUTE - OUT0 Port/Pin Select

Offset	Bit Position																													
0x4B4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**OUT0 pin select register**
	OUT0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**OUT0 port select register**
	OUT0 port select register			

24.6.125 GPIO_LETIMER_OUT1ROUTE - OUT1 Port/Pin Select

Offset	Bit Position																													
0x4B8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**OUT1 pin select register**
	OUT1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**OUT1 port select register**
	OUT1 port select register			

24.6.126 GPIO_MODEM_ROUTEEN - MODEM Pin Enable

Offset	Bit Position																													
0x4C0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																		0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name																		DOUTPEN	DCLKPEN	ANTTRIGSTOPPEN	ANTTRIGPEN	ANTSWUSPEN	ANTSWENPEN	ANTRR5PEN	ANTRR4PEN	ANTRR3PEN	ANTRR2PEN	ANTRR1PEN	ANTRR0PEN	ANTROLLOVERPEN	ANT1PEN	ANT0PEN

Bit	Name	Reset	Access	Description
31:15	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
14	DOUTPEN	0x0	RW	**DOUT pin enable control bit**
	DOUT pin enable control bit			
13	DCLKPEN	0x0	RW	**DCLK pin enable control bit**
	DCLK pin enable control bit			
12	ANTTRIGSTOPPEN	0x0	RW	**ANTTRIGSTOP pin enable control bit**
	ANTTRIGSTOP pin enable control bit			
11	ANTTRIGPEN	0x0	RW	**ANTTRIG pin enable control bit**
	ANTTRIG pin enable control bit			
10	ANTSWUSPEN	0x0	RW	**ANTSWUS pin enable control bit**
	ANTSWUS pin enable control bit			
9	ANTSWENPEN	0x0	RW	**ANTSWEN pin enable control bit**
	ANTSWEN pin enable control bit			
8	ANTRR5PEN	0x0	RW	**ANTRR5 pin enable control bit**
	ANTRR5 pin enable control bit			
7	ANTRR4PEN	0x0	RW	**ANTRR4 pin enable control bit**
	ANTRR4 pin enable control bit			
6	ANTRR3PEN	0x0	RW	**ANTRR3 pin enable control bit**
	ANTRR3 pin enable control bit			
5	ANTRR2PEN	0x0	RW	**ANTRR2 pin enable control bit**
	ANTRR2 pin enable control bit			
4	ANTRR1PEN	0x0	RW	**ANTRR1 pin enable control bit**
	ANTRR1 pin enable control bit			
3	ANTRR0PEN	0x0	RW	**ANTRR0 pin enable control bit**
	ANTRR0 pin enable control bit			

Bit	Name	Reset	Access	Description
2	ANTROLLOVERPEN	0x0	RW	**ANTROLLOVER pin enable control bit**
	ANTROLLOVER pin enable control bit			
1	ANT1PEN	0x0	RW	**ANT1 pin enable control bit**
	ANT1 pin enable control bit			
0	ANT0PEN	0x0	RW	**ANT0 pin enable control bit**
	ANT0 pin enable control bit			

24.6.127 GPIO_MODEM_ANT0ROUTE - ANT0 Port/Pin Select

Offset	Bit Position																													
0x4C4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ANT0 pin select register**
	ANT0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ANT0 port select register**
	ANT0 port select register			

24.6.128 GPIO_MODEM_ANT1ROUTE - ANT1 Port/Pin Select

Offset	Bit Position																													
0x4C8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ANT1 pin select register**
	ANT1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ANT1 port select register**
	ANT1 port select register			

24.6.129 GPIO_MODEM_ANTROLLOVERROUTE - ANTROLLOVER Port/Pin Select

Offset	Bit Position																													
0x4CC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ANTROLLOVER pin select register**
	ANTROLLOVER pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ANTROLLOVER port select register**
	ANTROLLOVER port select register			

24.6.130 GPIO_MODEM_ANTRR0ROUTE - ANTRR0 Port/Pin Select

Offset	Bit Position																													
0x4D0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ANTRR0 pin select register**
	ANTRR0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ANTRR0 port select register**
	ANTRR0 port select register			

24.6.131 GPIO_MODEM_ANTRR1ROUTE - ANTRR1 Port/Pin Select

Offset	Bit Position																													
0x4D4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ANTRR1 pin select register**
	ANTRR1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ANTRR1 port select register**
	ANTRR1 port select register			

24.6.132 GPIO_MODEM_ANTRR2ROUTE - ANTRR2 Port/Pin Select

Offset	Bit Position																													
0x4D8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ANTRR2 pin select register**
	ANTRR2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ANTRR2 port select register**
	ANTRR2 port select register			

24.6.133 GPIO_MODEM_ANTRR3ROUTE - ANTRR3 Port/Pin Select

Offset	Bit Position																													
0x4DC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ANTRR3 pin select register**
	ANTRR3 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ANTRR3 port select register**
	ANTRR3 port select register			

24.6.134 GPIO_MODEM_ANTRR4ROUTE - ANTRR4 Port/Pin Select

Offset	Bit Position																													
0x4E0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ANTRR4 pin select register**
	ANTRR4 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ANTRR4 port select register**
	ANTRR4 port select register			

24.6.135 GPIO_MODEM_ANTRR5ROUTE - ANTRR5 Port/Pin Select

Offset	Bit Position																													
0x4E4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ANTRR5 pin select register**
	ANTRR5 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ANTRR5 port select register**
	ANTRR5 port select register			

24.6.136 GPIO_MODEM_ANTSWENROUTE - ANTSWEN Port/Pin Select

Offset	Bit Position																													
0x4E8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ANTSWEN pin select register**
	ANTSWEN pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ANTSWEN port select register**
	ANTSWEN port select register			

24.6.137 GPIO_MODEM_ANTSWUSROUTE - ANTSWUS Port/Pin Select

Offset	Bit Position																													
0x4EC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ANTSWUS pin select register**
	ANTSWUS pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ANTSWUS port select register**
	ANTSWUS port select register			

24.6.138 GPIO_MODEM_ANTTRIGROUTE - ANTTRIG Port/Pin Select

Offset	Bit Position																													
0x4F0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ANTTRIG pin select register**
	ANTTRIG pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ANTTRIG port select register**
	ANTTRIG port select register			

24.6.139 GPIO_MODEM_ANTTRIGSTOPROUTE - ANTTRIGSTOP Port/Pin Select

Offset	Bit Position																													
0x4F4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ANTTRIGSTOP pin select register**
	ANTTRIGSTOP pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ANTTRIGSTOP port select register**
	ANTTRIGSTOP port select register			

24.6.140 GPIO_MODEM_DCLKROUTE - DCLK Port/Pin Select

Offset	Bit Position																													
0x4F8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**DCLK pin select register**
	DCLK pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**DCLK port select register**
	DCLK port select register			

24.6.141 GPIO_MODEM_DINROUTE - DIN Port/Pin Select

Offset	Bit Position																													
0x4FC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**DIN pin select register**
	DIN pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**DIN port select register**
	DIN port select register			

24.6.142 GPIO_MODEM_DOUTROUTE - DOUT Port/Pin Select

Offset	Bit Position																													
0x500	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**DOUT pin select register**
	DOUT pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**DOUT port select register**
	DOUT port select register			

24.6.143 GPIO_PCNT0_S0INROUTE - S0IN Port/Pin Select

Offset	Bit Position																													
0x50C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**S0IN pin select register**
	S0IN pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**S0IN port select register**
	S0IN port select register			

24.6.144 GPIO_PCNT0_S1INROUTE - S1IN Port/Pin Select

Offset	Bit Position																													
0x510	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN S1IN pin select register	0x0	RW	**S1IN pin select register**
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT S1IN port select register	0x0	RW	**S1IN port select register**

24.6.145 GPIO_PRS0_ROUTEEN - PRS0 Pin Enable

Offset	Bit Position																													
0x518	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name																	SYNCH3PEN	SYNCH2PEN	SYNCH1PEN	SYNCH0PEN	ASYNCH11PEN	ASYNCH10PEN	ASYNCH9PEN	ASYNCH8PEN	ASYNCH7PEN	ASYNCH6PEN	ASYNCH5PEN	ASYNCH4PEN	ASYNCH3PEN	ASYNCH2PEN	ASYNCH1PEN	ASYNCH0PEN

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15	SYNCH3PEN	0x0	RW	**SYNCH3 pin enable control bit**
	SYNCH3 pin enable control bit			
14	SYNCH2PEN	0x0	RW	**SYNCH2 pin enable control bit**
	SYNCH2 pin enable control bit			
13	SYNCH1PEN	0x0	RW	**SYNCH1 pin enable control bit**
	SYNCH1 pin enable control bit			
12	SYNCH0PEN	0x0	RW	**SYNCH0 pin enable control bit**
	SYNCH0 pin enable control bit			
11	ASYNCH11PEN	0x0	RW	**ASYNCH11 pin enable control bit**
	ASYNCH11 pin enable control bit			
10	ASYNCH10PEN	0x0	RW	**ASYNCH10 pin enable control bit**
	ASYNCH10 pin enable control bit			
9	ASYNCH9PEN	0x0	RW	**ASYNCH9 pin enable control bit**
	ASYNCH9 pin enable control bit			
8	ASYNCH8PEN	0x0	RW	**ASYNCH8 pin enable control bit**
	ASYNCH8 pin enable control bit			
7	ASYNCH7PEN	0x0	RW	**ASYNCH7 pin enable control bit**
	ASYNCH7 pin enable control bit			
6	ASYNCH6PEN	0x0	RW	**ASYNCH6 pin enable control bit**
	ASYNCH6 pin enable control bit			
5	ASYNCH5PEN	0x0	RW	**ASYNCH5 pin enable control bit**
	ASYNCH5 pin enable control bit			
4	ASYNCH4PEN	0x0	RW	**ASYNCH4 pin enable control bit**
	ASYNCH4 pin enable control bit			
3	ASYNCH3PEN	0x0	RW	**ASYNCH3 pin enable control bit**

Bit	Name	Reset	Access	Description
	ASYNCH3 pin enable control bit			
2	ASYNCH2PEN	0x0	RW	**ASYNCH2 pin enable control bit**
	ASYNCH2 pin enable control bit			
1	ASYNCH1PEN	0x0	RW	**ASYNCH1 pin enable control bit**
	ASYNCH1 pin enable control bit			
0	ASYNCH0PEN	0x0	RW	**ASYNCH0 pin enable control bit**
	ASYNCH0 pin enable control bit			

24.6.146 GPIO_PRS0_ASYNCH0ROUTE - ASYNCH0 Port/Pin Select

Offset	Bit Position																													
0x51C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ASYNCH0 pin select register**
	ASYNCH0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ASYNCH0 port select register**
	ASYNCH0 port select register			

24.6.147 GPIO_PRS0_ASYNCH1ROUTE - ASYNCH1 Port/Pin Select

Offset	Bit Position																													
0x520	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ASYNCH1 pin select register**
	ASYNCH1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ASYNCH1 port select register**
	ASYNCH1 port select register			

24.6.148 GPIO_PRS0_ASYNCH2ROUTE - ASYNCH2 Port/Pin Select

Offset	Bit Position																													
0x524	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ASYNCH2 pin select register**
	ASYNCH2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ASYNCH2 port select register**
	ASYNCH2 port select register			

24.6.149 GPIO_PRS0_ASYNCH3ROUTE - ASYNCH3 Port/Pin Select

Offset	Bit Position																													
0x528	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ASYNCH3 pin select register**
	ASYNCH3 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ASYNCH3 port select register**
	ASYNCH3 port select register			

24.6.150 GPIO_PRS0_ASYNCH4ROUTE - ASYNCH4 Port/Pin Select

Offset	Bit Position																													
0x52C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ASYNCH4 pin select register**
	ASYNCH4 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ASYNCH4 port select register**
	ASYNCH4 port select register			

24.6.151 GPIO_PRS0_ASYNCH5ROUTE - ASYNCH5 Port/Pin Select

Offset	Bit Position																													
0x530	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ASYNCH5 pin select register**
	ASYNCH5 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ASYNCH5 port select register**
	ASYNCH5 port select register			

24.6.152 GPIO_PRS0_ASYNCH6ROUTE - ASYNCH6 Port/Pin Select

Offset	Bit Position																													
0x534	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ASYNCH6 pin select register**
	ASYNCH6 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ASYNCH6 port select register**
	ASYNCH6 port select register			

24.6.153 GPIO_PRS0_ASYNCH7ROUTE - ASYNCH7 Port/Pin Select

Offset	Bit Position																													
0x538	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ASYNCH7 pin select register**
	ASYNCH7 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ASYNCH7 port select register**
	ASYNCH7 port select register			

24.6.154 GPIO_PRS0_ASYNCH8ROUTE - ASYNCH8 Port/Pin Select

Offset	Bit Position																													
0x53C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ASYNCH8 pin select register**
	ASYNCH8 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ASYNCH8 port select register**
	ASYNCH8 port select register			

24.6.155 GPIO_PRS0_ASYNCH9ROUTE - ASYNCH9 Port/Pin Select

Offset	Bit Position																													
0x540	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ASYNCH9 pin select register**
	ASYNCH9 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ASYNCH9 port select register**
	ASYNCH9 port select register			

24.6.156 GPIO_PRS0_ASYNCH10ROUTE - ASYNCH10 Port/Pin Select

Offset	Bit Position																													
0x544	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ASYNCH10 pin select register**
	ASYNCH10 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ASYNCH10 port select register**
	ASYNCH10 port select register			

24.6.157 GPIO_PRS0_ASYNCH11ROUTE - ASYNCH11 Port/Pin Select

Offset	Bit Position																													
0x548	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**ASYNCH11 pin select register**
	ASYNCH11 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**ASYNCH11 port select register**
	ASYNCH11 port select register			

24.6.158 GPIO_PRS0_SYNCH0ROUTE - SYNCH0 Port/Pin Select

Offset	Bit Position																													
0x54C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**SYNCH0 pin select register**
	SYNCH0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**SYNCH0 port select register**
	SYNCH0 port select register			

24.6.159 GPIO_PRS0_SYNCH1ROUTE - SYNCH1 Port/Pin Select

Offset	Bit Position																													
0x550	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**SYNCH1 pin select register**
	SYNCH1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**SYNCH1 port select register**
	SYNCH1 port select register			

24.6.160 GPIO_PRS0_SYNCH2ROUTE - SYNCH2 Port/Pin Select

Offset	Bit Position																													
0x554	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**SYNCH2 pin select register**
	SYNCH2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**SYNCH2 port select register**
	SYNCH2 port select register			

24.6.161 GPIO_PRS0_SYNCH3ROUTE - SYNCH3 Port/Pin Select

Offset	Bit Position																													
0x558	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**SYNCH3 pin select register**
	SYNCH3 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**SYNCH3 port select register**
	SYNCH3 port select register			

24.6.162 GPIO_SYXO0_BUFOUTREQINASYNCROUTE - BUFOUTREQINASYNC Port/Pin Select

Offset	Bit Position																													
0x5C0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**BUFOUTREQINASYNC pin select register**
	BUFOUTREQINASYNC pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**BUFOUTREQINASYNC port select register**
	BUFOUTREQINASYNC port select register			

24.6.163 GPIO_TIMER0_ROUTEEN - TIMER0 Pin Enable

Offset	Bit Position																													
0x5C8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0	0x0	0x0	0x0	0x0	0x0
Access																											RW	RW	RW	RW	RW	RW
Name																											CCC2PEN	CCC1PEN	CCC0PEN	CC2PEN	CC1PEN	CC0PEN

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	CCC2PEN	0x0	RW	**CDTI2 pin enable control bit**
	CDTI2 pin enable control bit			
4	CCC1PEN	0x0	RW	**CDTI1 pin enable control bit**
	CDTI1 pin enable control bit			
3	CCC0PEN	0x0	RW	**CDTI0 pin enable control bit**
	CDTI0 pin enable control bit			
2	CC2PEN	0x0	RW	**CC2 pin enable control bit**
	CC2 pin enable control bit			
1	CC1PEN	0x0	RW	**CC1 pin enable control bit**
	CC1 pin enable control bit			
0	CC0PEN	0x0	RW	**CC0 pin enable control bit**
	CC0 pin enable control bit			

24.6.164 GPIO_TIMER0_CC0ROUTE - CC0 Port/Pin Select

Offset	Bit Position																													
0x5CC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC0 pin select register**
	CC0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC0 port select register**
	CC0 port select register			

24.6.165 GPIO_TIMER0_CC1ROUTE - CC1 Port/Pin Select

Offset	Bit Position																													
0x5D0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC1 pin select register**
	CC1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC1 port select register**
	CC1 port select register			

24.6.166 GPIO_TIMER0_CC2ROUTE - CC2 Port/Pin Select

Offset	Bit Position																													
0x5D4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC2 pin select register**
	CC2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC2 port select register**
	CC2 port select register			

24.6.167 GPIO_TIMER0_CDTI0ROUTE - CDTI0 Port/Pin Select

Offset	Bit Position																													
0x5D8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI0 pin select register**
	CDTI0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI0 port select register**
	CDTI0 port select register			

24.6.168 GPIO_TIMER0_CDTI1ROUTE - CDTI1 Port/Pin Select

Offset	Bit Position																													
0x5DC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI1 pin select register**
	CDTI1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI1 port select register**
	CDTI1 port select register			

24.6.169 GPIO_TIMER0_CDTI2ROUTE - CDTI2 Port/Pin Select

Offset	Bit Position																													
0x5E0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI2 pin select register**
	CDTI2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI2 port select register**
	CDTI2 port select register			

24.6.170 GPIO_TIMER1_ROUTEEN - TIMER1 Pin Enable

Offset	Bit Position																													
0x5E8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0	0x0	0x0	0x0	0x0	0x0
Access																											RW	RW	RW	RW	RW	RW
Name																											CCC2PEN	CCC1PEN	CCC0PEN	CC2PEN	CC1PEN	CC0PEN

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	CCC2PEN	0x0	RW	**CDTI2 pin enable control bit**
	CDTI2 pin enable control bit			
4	CCC1PEN	0x0	RW	**CDTI1 pin enable control bit**
	CDTI1 pin enable control bit			
3	CCC0PEN	0x0	RW	**CDTI0 pin enable control bit**
	CDTI0 pin enable control bit			
2	CC2PEN	0x0	RW	**CC2 pin enable control bit**
	CC2 pin enable control bit			
1	CC1PEN	0x0	RW	**CC1 pin enable control bit**
	CC1 pin enable control bit			
0	CC0PEN	0x0	RW	**CC0 pin enable control bit**
	CC0 pin enable control bit			

24.6.171 GPIO_TIMER1_CC0ROUTE - CC0 Port/Pin Select

Offset	Bit Position																													
0x5EC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC0 pin select register**
	CC0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC0 port select register**
	CC0 port select register			

24.6.172 GPIO_TIMER1_CC1ROUTE - CC1 Port/Pin Select

Offset	Bit Position																													
0x5F0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC1 pin select register**
	CC1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC1 port select register**
	CC1 port select register			

24.6.173 GPIO_TIMER1_CC2ROUTE - CC2 Port/Pin Select

Offset	Bit Position																													
0x5F4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC2 pin select register**
	CC2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC2 port select register**
	CC2 port select register			

24.6.174 GPIO_TIMER1_CDTI0ROUTE - CDTI0 Port/Pin Select

Offset	Bit Position																													
0x5F8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI0 pin select register**
	CDTI0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI0 port select register**
	CDTI0 port select register			

24.6.175 GPIO_TIMER1_CDTI1ROUTE - CDTI1 Port/Pin Select

Offset	Bit Position																													
0x5FC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI1 pin select register**
	CDTI1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI1 port select register**
	CDTI1 port select register			

24.6.176 GPIO_TIMER1_CDTI2ROUTE - CDTI2 Port/Pin Select

Offset	Bit Position																													
0x600	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI2 pin select register**
	CDTI2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI2 port select register**
	CDTI2 port select register			

24.6.177 GPIO_TIMER2_ROUTEEN - TIMER2 Pin Enable

Offset	Bit Position																													
0x608	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0	0x0	0x0	0x0	0x0	0x0
Access																											RW	RW	RW	RW	RW	RW
Name																											CCC2PEN	CCC1PEN	CCC0PEN	CC2PEN	CC1PEN	CC0PEN

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	CCC2PEN	0x0	RW	**CDTI2 pin enable control bit**
	CDTI2 pin enable control bit			
4	CCC1PEN	0x0	RW	**CDTI1 pin enable control bit**
	CDTI1 pin enable control bit			
3	CCC0PEN	0x0	RW	**CDTI0 pin enable control bit**
	CDTI0 pin enable control bit			
2	CC2PEN	0x0	RW	**CC2 pin enable control bit**
	CC2 pin enable control bit			
1	CC1PEN	0x0	RW	**CC1 pin enable control bit**
	CC1 pin enable control bit			
0	CC0PEN	0x0	RW	**CC0 pin enable control bit**
	CC0 pin enable control bit			

24.6.178 GPIO_TIMER2_CC0ROUTE - CC0 Port/Pin Select

Offset	Bit Position																													
0x60C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC0 pin select register**
	CC0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC0 port select register**
	CC0 port select register			

24.6.179 GPIO_TIMER2_CC1ROUTE - CC1 Port/Pin Select

Offset	Bit Position																													
0x610	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC1 pin select register**
	CC1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC1 port select register**
	CC1 port select register			

24.6.180 GPIO_TIMER2_CC2ROUTE - CC2 Port/Pin Select

Offset	Bit Position																													
0x614	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC2 pin select register**
	CC2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC2 port select register**
	CC2 port select register			

24.6.181 GPIO_TIMER2_CDTI0ROUTE - CDTI0 Port/Pin Select

Offset	Bit Position																													
0x618	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI0 pin select register**
	CDTI0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI0 port select register**
	CDTI0 port select register			

24.6.182 GPIO_TIMER2_CDTI1ROUTE - CDTI1 Port/Pin Select

Offset	Bit Position																													
0x61C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI1 pin select register**
	CDTI1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI1 port select register**
	CDTI1 port select register			

24.6.183 GPIO_TIMER2_CDTI2ROUTE - CDTI2 Port/Pin Select

Offset	Bit Position																													
0x620	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI2 pin select register**
	CDTI2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI2 port select register**
	CDTI2 port select register			

24.6.184 GPIO_TIMER3_ROUTEEN - TIMER3 Pin Enable

Offset	Bit Position																													
0x628	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0	0x0	0x0	0x0	0x0	0x0
Access																											RW	RW	RW	RW	RW	RW
Name																											CCC2PEN	CCC1PEN	CCC0PEN	CC2PEN	CC1PEN	CC0PEN

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	CCC2PEN	0x0	RW	**CDTI2 pin enable control bit**
	CDTI2 pin enable control bit			
4	CCC1PEN	0x0	RW	**CDTI1 pin enable control bit**
	CDTI1 pin enable control bit			
3	CCC0PEN	0x0	RW	**CDTI0 pin enable control bit**
	CDTI0 pin enable control bit			
2	CC2PEN	0x0	RW	**CC2 pin enable control bit**
	CC2 pin enable control bit			
1	CC1PEN	0x0	RW	**CC1 pin enable control bit**
	CC1 pin enable control bit			
0	CC0PEN	0x0	RW	**CC0 pin enable control bit**
	CC0 pin enable control bit			

24.6.185 GPIO_TIMER3_CC0ROUTE - CC0 Port/Pin Select

Offset	Bit Position																													
0x62C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC0 pin select register**
	CC0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC0 port select register**
	CC0 port select register			

24.6.186 GPIO_TIMER3_CC1ROUTE - CC1 Port/Pin Select

Offset	Bit Position																													
0x630	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC1 pin select register**
	CC1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC1 port select register**
	CC1 port select register			

24.6.187 GPIO_TIMER3_CC2ROUTE - CC2 Port/Pin Select

Offset	Bit Position																													
0x634	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC2 pin select register**
	CC2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC2 port select register**
	CC2 port select register			

24.6.188 GPIO_TIMER3_CDTI0ROUTE - CDTI0 Port/Pin Select

Offset	Bit Position																													
0x638	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI0 pin select register**
	CDTI0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI0 port select register**
	CDTI0 port select register			

24.6.189 GPIO_TIMER3_CDTI1ROUTE - CDTI1 Port/Pin Select

Offset	Bit Position																													
0x63C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI1 pin select register**
	CDTI1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI1 port select register**
	CDTI1 port select register			

24.6.190 GPIO_TIMER3_CDTI2ROUTE - CDTI2 Port/Pin Select

Offset	Bit Position																													
0x640	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI2 pin select register**
	CDTI2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI2 port select register**
	CDTI2 port select register			

24.6.191 GPIO_TIMER4_ROUTEEN - TIMER4 Pin Enable

Offset	Bit Position																													
0x648	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0	0x0	0x0	0x0	0x0	0x0
Access																											RW	RW	RW	RW	RW	RW
Name																											CCC2PEN	CCC1PEN	CCC0PEN	CC2PEN	CC1PEN	CC0PEN

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	CCC2PEN	0x0	RW	**CDTI2 pin enable control bit**
	CDTI2 pin enable control bit			
4	CCC1PEN	0x0	RW	**CDTI1 pin enable control bit**
	CDTI1 pin enable control bit			
3	CCC0PEN	0x0	RW	**CDTI0 pin enable control bit**
	CDTI0 pin enable control bit			
2	CC2PEN	0x0	RW	**CC2 pin enable control bit**
	CC2 pin enable control bit			
1	CC1PEN	0x0	RW	**CC1 pin enable control bit**
	CC1 pin enable control bit			
0	CC0PEN	0x0	RW	**CC0 pin enable control bit**
	CC0 pin enable control bit			

24.6.192 GPIO_TIMER4_CC0ROUTE - CC0 Port/Pin Select

Offset	Bit Position																													
0x64C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC0 pin select register**
	CC0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC0 port select register**
	CC0 port select register			

24.6.193 GPIO_TIMER4_CC1ROUTE - CC1 Port/Pin Select

Offset	Bit Position																													
0x650	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC1 pin select register**
	CC1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC1 port select register**
	CC1 port select register			

24.6.194 GPIO_TIMER4_CC2ROUTE - CC2 Port/Pin Select

Offset	Bit Position																													
0x654	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC2 pin select register**
	CC2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC2 port select register**
	CC2 port select register			

24.6.195 GPIO_TIMER4_CDTI0ROUTE - CDTI0 Port/Pin Select

Offset	Bit Position																													
0x658	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI0 pin select register**
	CDTI0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI0 port select register**
	CDTI0 port select register			

24.6.196 GPIO_TIMER4_CDTI1ROUTE - CDTI1 Port/Pin Select

Offset	Bit Position																													
0x65C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI1 pin select register**
	CDTI1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI1 port select register**
	CDTI1 port select register			

24.6.197 GPIO_TIMER4_CDTI2ROUTE - CDTI2 Port/Pin Select

Offset	Bit Position																													
0x660	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI2 pin select register**
	CDTI2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI2 port select register**
	CDTI2 port select register			

24.6.198 GPIO_TIMER5_ROUTEEN - TIMER5 Pin Enable

Offset	Bit Position																													
0x668	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0	0x0	0x0	0x0	0x0	0x0
Access																											RW	RW	RW	RW	RW	RW
Name																											CCC2PEN	CCC1PEN	CCC0PEN	CC2PEN	CC1PEN	CC0PEN

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	CCC2PEN	0x0	RW	**CDTI2 pin enable control bit**
	CDTI2 pin enable control bit			
4	CCC1PEN	0x0	RW	**CDTI1 pin enable control bit**
	CDTI1 pin enable control bit			
3	CCC0PEN	0x0	RW	**CDTI0 pin enable control bit**
	CDTI0 pin enable control bit			
2	CC2PEN	0x0	RW	**CC2 pin enable control bit**
	CC2 pin enable control bit			
1	CC1PEN	0x0	RW	**CC1 pin enable control bit**
	CC1 pin enable control bit			
0	CC0PEN	0x0	RW	**CC0 pin enable control bit**
	CC0 pin enable control bit			

24.6.199 GPIO_TIMER5_CC0ROUTE - CC0 Port/Pin Select

Offset	Bit Position																													
0x66C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC0 pin select register**
	CC0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC0 port select register**
	CC0 port select register			

24.6.200 GPIO_TIMER5_CC1ROUTE - CC1 Port/Pin Select

Offset	Bit Position																													
0x670	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC1 pin select register**
	CC1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC1 port select register**
	CC1 port select register			

24.6.201 GPIO_TIMER5_CC2ROUTE - CC2 Port/Pin Select

Offset	Bit Position																													
0x674	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC2 pin select register**
	CC2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC2 port select register**
	CC2 port select register			

24.6.202 GPIO_TIMER5_CDTI0ROUTE - CDTI0 Port/Pin Select

Offset	Bit Position																													
0x678	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI0 pin select register**
	CDTI0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI0 port select register**
	CDTI0 port select register			

24.6.203 GPIO_TIMER5_CDTI1ROUTE - CDTI1 Port/Pin Select

Offset	Bit Position																													
0x67C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI1 pin select register**
	CDTI1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI1 port select register**
	CDTI1 port select register			

24.6.204 GPIO_TIMER5_CDTI2ROUTE - CDTI2 Port/Pin Select

Offset	Bit Position																													
0x680	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI2 pin select register**
	CDTI2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI2 port select register**
	CDTI2 port select register			

24.6.205 GPIO_TIMER6_ROUTEEN - TIMER6 Pin Enable

Offset	Bit Position																													
0x688	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0	0x0	0x0	0x0	0x0	0x0
Access																											RW	RW	RW	RW	RW	RW
Name																											CCC2PEN	CCC1PEN	CCC0PEN	CC2PEN	CC1PEN	CC0PEN

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	CCC2PEN	0x0	RW	**CDTI2 pin enable control bit**
	CDTI2 pin enable control bit			
4	CCC1PEN	0x0	RW	**CDTI1 pin enable control bit**
	CDTI1 pin enable control bit			
3	CCC0PEN	0x0	RW	**CDTI0 pin enable control bit**
	CDTI0 pin enable control bit			
2	CC2PEN	0x0	RW	**CC2 pin enable control bit**
	CC2 pin enable control bit			
1	CC1PEN	0x0	RW	**CC1 pin enable control bit**
	CC1 pin enable control bit			
0	CC0PEN	0x0	RW	**CC0 pin enable control bit**
	CC0 pin enable control bit			

24.6.206 GPIO_TIMER6_CC0ROUTE - CC0 Port/Pin Select

Offset	Bit Position																													
0x68C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC0 pin select register**
	CC0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC0 port select register**
	CC0 port select register			

24.6.207 GPIO_TIMER6_CC1ROUTE - CC1 Port/Pin Select

Offset	Bit Position																													
0x690	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC1 pin select register**
	CC1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC1 port select register**
	CC1 port select register			

24.6.208 GPIO_TIMER6_CC2ROUTE - CC2 Port/Pin Select

Offset	Bit Position																													
0x694	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC2 pin select register**
	CC2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC2 port select register**
	CC2 port select register			

24.6.209 GPIO_TIMER6_CDTI0ROUTE - CDTI0 Port/Pin Select

Offset	Bit Position																													
0x698	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI0 pin select register**
	CDTI0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI0 port select register**
	CDTI0 port select register			

24.6.210 GPIO_TIMER6_CDTI1ROUTE - CDTI1 Port/Pin Select

Offset	Bit Position																													
0x69C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI1 pin select register**
	CDTI1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI1 port select register**
	CDTI1 port select register			

24.6.211 GPIO_TIMER6_CDTI2ROUTE - CDTI2 Port/Pin Select

Offset	Bit Position																													
0x6A0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI2 pin select register**
	CDTI2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI2 port select register**
	CDTI2 port select register			

24.6.212 GPIO_TIMER7_ROUTEEN - TIMER7 Pin Enable

Offset	Bit Position																													
0x6A8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																											0x0	0x0	0x0	0x0	0x0	0x0
Access																											RW	RW	RW	RW	RW	RW
Name																											CCC2PEN	CCC1PEN	CCC0PEN	CC2PEN	CC1PEN	CC0PEN

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	CCC2PEN	0x0	RW	**CDTI2 pin enable control bit**
	CDTI2 pin enable control bit			
4	CCC1PEN	0x0	RW	**CDTI1 pin enable control bit**
	CDTI1 pin enable control bit			
3	CCC0PEN	0x0	RW	**CDTI0 pin enable control bit**
	CDTI0 pin enable control bit			
2	CC2PEN	0x0	RW	**CC2 pin enable control bit**
	CC2 pin enable control bit			
1	CC1PEN	0x0	RW	**CC1 pin enable control bit**
	CC1 pin enable control bit			
0	CC0PEN	0x0	RW	**CC0 pin enable control bit**
	CC0 pin enable control bit			

24.6.213 GPIO_TIMER7_CC0ROUTE - CC0 Port/Pin Select

Offset	Bit Position																													
0x6AC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC0 pin select register**
	CC0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC0 port select register**
	CC0 port select register			

24.6.214 GPIO_TIMER7_CC1ROUTE - CC1 Port/Pin Select

Offset	Bit Position																													
0x6B0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC1 pin select register**
	CC1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC1 port select register**
	CC1 port select register			

24.6.215 GPIO_TIMER7_CC2ROUTE - CC2 Port/Pin Select

Offset	Bit Position																													
0x6B4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CC2 pin select register**
	CC2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CC2 port select register**
	CC2 port select register			

24.6.216 GPIO_TIMER7_CDTI0ROUTE - CDTI0 Port/Pin Select

Offset	Bit Position																													
0x6B8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI0 pin select register**
	CDTI0 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI0 port select register**
	CDTI0 port select register			

24.6.217 GPIO_TIMER7_CDTI1ROUTE - CDTI1 Port/Pin Select

Offset	Bit Position																													
0x6BC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI1 pin select register**
	CDTI1 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI1 port select register**
	CDTI1 port select register			

24.6.218 GPIO_TIMER7_CDTI2ROUTE - CDTI2 Port/Pin Select

Offset	Bit Position																													
0x6C0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

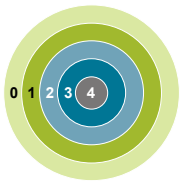
Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**CDTI2 pin select register**
	CDTI2 pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**CDTI2 port select register**
	CDTI2 port select register			

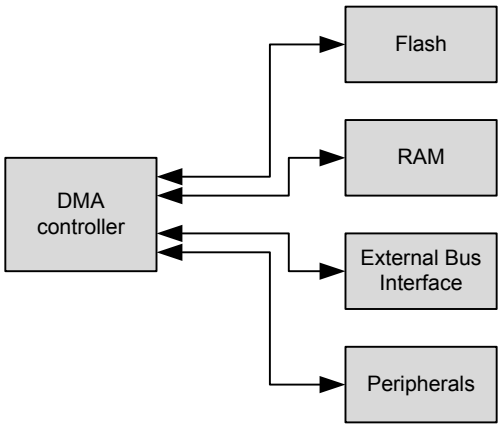
24.6.219 GPIO_USB_USBVBUSSENSEROUTE - USBVBUSSENSE Port/Pin Select

Offset	Bit Position																													
0x6CC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																		0x0	
Access													RW																		RW	
Name													PIN																		PORT	

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PIN	0x0	RW	**USBVBUSSENSE pin select register**
	USBVBUSSENSE pin select register			
15:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	PORT	0x0	RW	**USBVBUSSENSE port select register**
	USBVBUSSENSE port select register			

25. LDMA - Linked DMA





Quick Facts

What?

The LDMA controller can move data without CPU intervention, effectively reducing the energy consumption for a data transfer.

Why?

The LDMA can perform data transfers more energy efficiently than the CPU and allows autonomous operation in low energy modes.

How?

The LDMA controller has multiple highly configurable, prioritized DMA channels. A linked list of flexible descriptors makes it possible to tailor the controller to the specific needs of an application.

25.1 Introduction

The Linked Direct Memory Access (LDMA) controller performs memory transfer operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes while still routing data to memory and peripherals. For example, moving data from the ADC to memory.

25.1.1 Features

- Flexible Source and Destination transfers
  - Memory-to-memory
  - Memory-to-peripheral
  - Peripheral-to-memory
  - Peripheral-to-peripheral
- DMA transfers triggered by peripherals, software, or linked list
- Single or multiple data transfers for each peripheral or software request
- Inter-channel and hardware event synchronization via trigger and wait functions
- Supports single or multiple descriptors
  - Single descriptor
  - Linked list of descriptors
  - Circular and ping-pong buffers
  - Scatter-Gather
  - Looping
  - Pause and restart triggered by other channels
  - Sophisticated flow control which can function without CPU interaction
- Channel arbitration includes:
  - Fixed priority
  - Simple round robin
  - Round robin with programmable multiple interleaved entries for higher priority requesters
- Programmable data size and source and destination address strides
- Programmable interrupt generation at the end of each DMA descriptor execution
- Little-endian/big-endian conversion
- DMA write-immediate function

25.2 Block Diagram

An overview of the LDMA and the modules it interacts with is shown in Figure 25.1 LDMA Block Diagram on page 999.

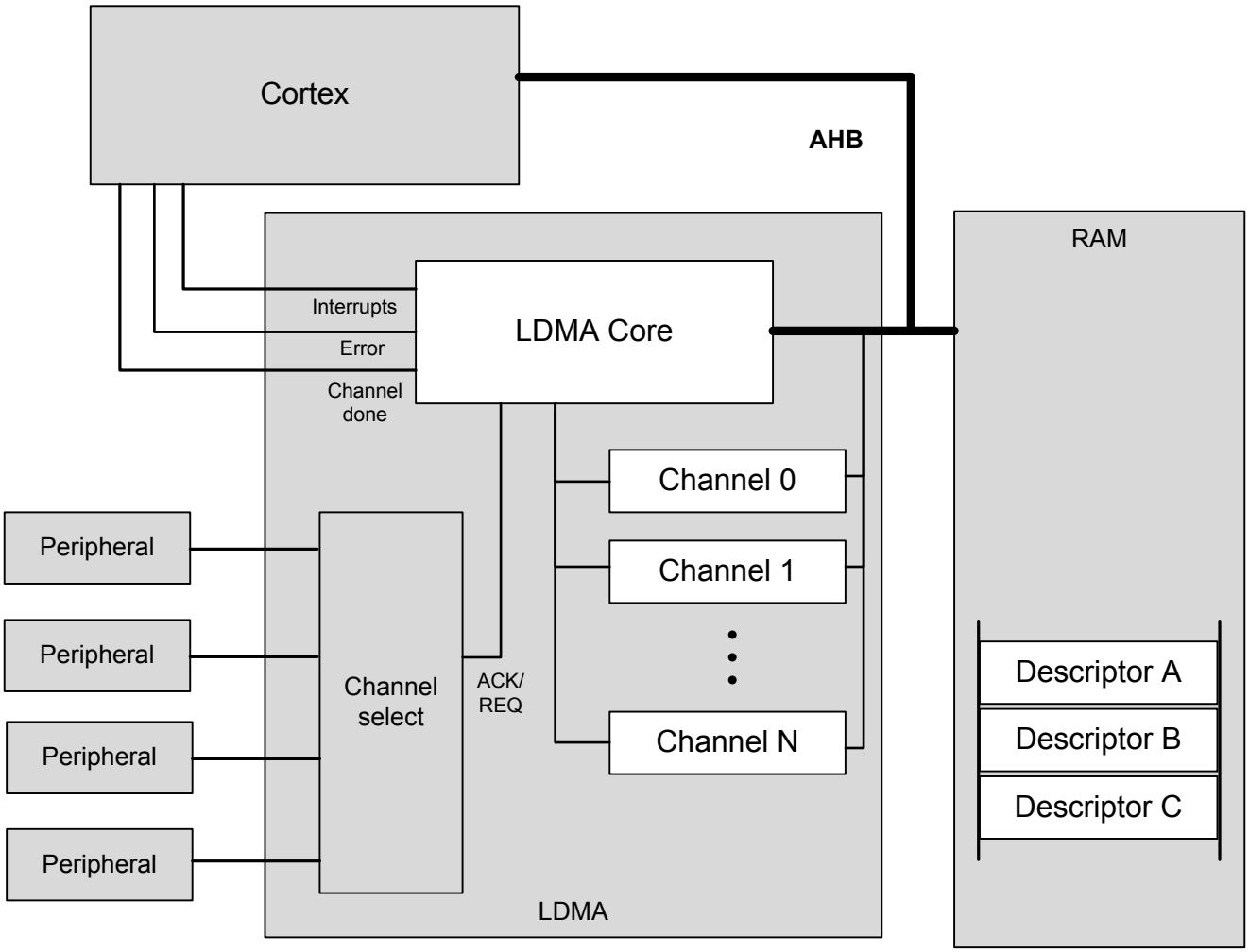


Figure 25.1. LDMA Block Diagram

The Linked DMA Controller consists of three main parts

- A DMA core that executes transfers and communicates status to the core
- A channel select block that routes peripheral DMA requests and acknowledge signals to the DMA
- A set of internal channel configuration registers for tracking the progress of each DMA channel

The DMA has access to all system memory through the AHB bus and the AHB->APB bridge. It can load channel descriptors from memory with no CPU intervention.

25.3 Functional Description

The Linked DMA Controller is highly flexible. It is capable of transferring data between peripherals and memory without involvement from the processor core. This can be used to increase system performance by off-loading the processor from copying large amounts of data or avoiding frequent interrupts to service peripherals needing more data or having available data. It can also be used to reduce the system energy consumption by making the LDMA work autonomously with some EM2/3 peripherals for data transfer without having to wake up the processor core from sleep.

The Linked DMA Controller has 16 independent channels. Each of these channels can be connected to any of the available peripheral DMA transfer request input sources by writing to the channel configuration registers, see 25.3.2 Channel Configuration. In addition, each channel can also be triggered directly by software, which is useful for memory-to-memory transfers.

The channel descriptors determine what the Linked DMA Controller will do when it receives DMA transfer request. The initial descriptor is written directly to the LDMA's channel registers. If desired, the initial descriptor can link to additional linked descriptors stored in memory (RAM or Flash). Alternatively, software may also load the initial descriptor by writing the descriptor address to the LDMA_CHx_LINK register and then setting the corresponding bit the LDMA_LINKLOAD register.

Before enabling a channel, the software must take care to properly configure the channel registers including the link address and any linked descriptors. When a channel is triggered, the Linked DMA Controller will perform the memory transfers as specified by the descriptors. A descriptor contains the memory address to read from, the memory address to write to, link address of the next descriptor, the number of bytes to be transferred, etc. The channel descriptor is described in detail in 25.3.7 Channel Descriptor Data Structure.

The Linked DMA Controller supports both fixed priority and round robin arbitration. The number of fixed and round robin channels is programmable. For round robin channels, the number of arbitration slots requested for each channel is programmable. Using this scheme, it is possible to ensure that timing-critical transfers are serviced on time.

DMA transfers take place by reading a block of data at a time from the source, storing it in the LDMA’s local FIFO, then writing the block out to the destination from the FIFO. Interrupts may optionally be signaled to the CPU’s interrupt controller at the end of any DMA transfer or at the completion of a descriptor if the DONEIFSEN bit is set. An AHB error will always generate an interrupt.

25.3.1 Channel Descriptor

Each DMA channel has descriptor registers. A transfer can be initialized by software writing to the registers or by the DMA itself copying a descriptor from RAM to memory. When using a linked list of descriptors the first descriptor should be initialized by the CPU. The DMA itself will then copy linked descriptors to its descriptor registers as required. In addition to manually initializing the first transfer, software may also cause the LDMA to load the initial descriptor by writing the descriptor address to the LDMA_CHx_LINK register and then setting the corresponding bit the LDMA_LINKLOAD register.

The contents of the descriptor registers are dynamically updated during the DMA transfer. The contents of descriptors in memory are not edited by the controller.

Some descriptor field values are only used for linked descriptors. For example, the SRCMODE and DSTMODE bits of the LDMA_CHx_CTRL registers determine if a linked descriptor is using relative or absolute addressing. Software writes to the address registers will always use absolute addressing and never set these bits. Therefore, these bits are read only.

25.3.1.1 DMA Transfer Size

A DMA transfer is the smallest unit of data that can be transfered by the LDMA. The LDMA supports byte, half-word and word sized transfers. The SIZE field in the LDMA_CHx_CTRL register specifies the data width of one DMA transfer.

25.3.1.2 Source/Destination Increments

The SRCINC and DSTINC in the LDMA_CHx_CTRL register determines the increment between DMA transfers. The increment is in units of DMA transfers and using an increment size of 1 will transfer contiguous bytes, half-words, or words depending on the value of the SIZE field. Multiple unit increments are useful for transferring or packing/unpacking alligned data. For example using an increment of 4 with a size of BYTE will transfer word aligned bytes. An increment of 2 units with a size of HALFWORD is suitable for the transfer of word aligned half-word data. The LDMA can also pack or unpack data by using a different increment size for source and destination. For example - to convert from word aligned byte data (unpacked) to contiguous byte data (packed), set the SIZE to BYTE, SRCINC to 4, and DSTINC to 1.

SIZE may also be set to NONE which will cause the LDMA to read or write the same location for every DMA transfer. This is usefull for accessing peripheral FIFO or data registers.

25.3.1.3 Block Size

The block size defines the amount of data transferred in one arbitration. It consists of one or more DMA transfers. See 25.3.6.1 Arbitration Priority for more details.

25.3.1.4 Transfer Count

The descriptor transfer count defines how many DMA transfers to perform. The number of bytes transferred by the descripter will depend on both the transfer count XFERCNT and the SIZE field settings. TOTAL_BYTES = XFERCNT * SIZE

25.3.1.5 Descriptor List

A descriptor list consists of one or more descriptors which are executed serially. This list may be a simple sequence of descriptors, a loop of descriptors, or a combination of the two.

Each descriptor in the list can be one of several types.

- Single Transfer descriptor: Transfers TOTAL_BYTES of data and then stops.
- Linked Transfer descriptor: Transfers TOTAL_BYTES of data and then loads the next linked descriptor.
- Loop Transfer descriptor: Transfers TOTAL_BYTES of data and performs loop control (see 25.3.2.2 Loop Counter).
- Sync descriptor: Handle synchronization of the list with other entities (see 25.3.7.2 SYNC Descriptor Structure).
- WRI descriptor: Writes a value to a location in memory (see 25.3.7.3 WRI Descriptor Structure).

25.3.1.6 Addresses

Before initiating a transfer, software should write the source address, destination address, and if applicable the link address to the descriptor registers. Alternatively, software may load a descriptor from memory by writing the descriptor address to the LDMA_CHx_LINK register and setting the corresponding bit in the LDMA_LINKLOAD register.

During a DMA transfer, the DMA source and destination address registers are pointers to the next transfer address. The LDMA will update the SRC and DST addresses after each transfer. If software halts a DMA transfer by clearing the enable bit, the SRC and DST addresses will indicate the next transfer address.

When a descriptor is finished the DMA will either halt or load the next (linked) descriptor depending on the value of the LINK field in the LDMA_Chx_LINK register. After loading a linked descriptor, the descriptor registers will reflect the content of the loaded descriptor. Note that the linked descriptor must be word aligned in memory. The two least significant bits of the LDMA_CHx_LINK register are used by the LINK and LINKMODE bits. The two least significant bits of the link address are always zero.

25.3.1.7 Addressing Modes

The DMA descriptors support absolute addressing or relative addressing. When using relative addressing, the offset is relative to the current contents of the respective address registers. Regardless of the descriptor addressing modes, the address registers always indicate the absolute address. For example, when loading a descriptor using relative SRC addressing, the LDMA will add the descriptor source address (offset) to the contents of the SRCADDR register (base address). After loading, the SRCADDR register will indicate the absolute address of the loaded descriptor.

The initial descriptor must use absolute addressing. The LDMA will ignore the DSTMODE, SRCMODE, and LINKMODE bits for the initial descriptor and interpret the addresses as an absolute addresses.

Relative addressing is most useful for the link address. The initial descriptor will indicate the absolute address of the linked descriptors in memory. The linked descriptors might be an array of structures. In this case the offset between descriptors is constant and is always 4 words or 16 bytes (each descriptor has 4 words). The LINK address is not incremented or decremented after each transfer. Thus, a relative offset of 0x10 may be used for all linked descriptors.

The source and destination addresses also support relative addressing. When using relative addressing with the source or destination address registers, the LDMA adds the relative offset to the current contents of the respective address register. Since the source and destination addresses are normally incremented after each transfer, the final address will point to one unit past the last transfer. Thus, an offset of zero will give the next sequential data address.

See the example 25.4.6 2D Copy for an common use of relative addressing.

25.3.1.8 Byte Swap

Enabling byte swap reverses the endianness of the incoming source data read into the LDMA's FIFO. Byte swap is only valid for transfer sizes of word and half-word. Note that linked structure reads are not byte swapped.

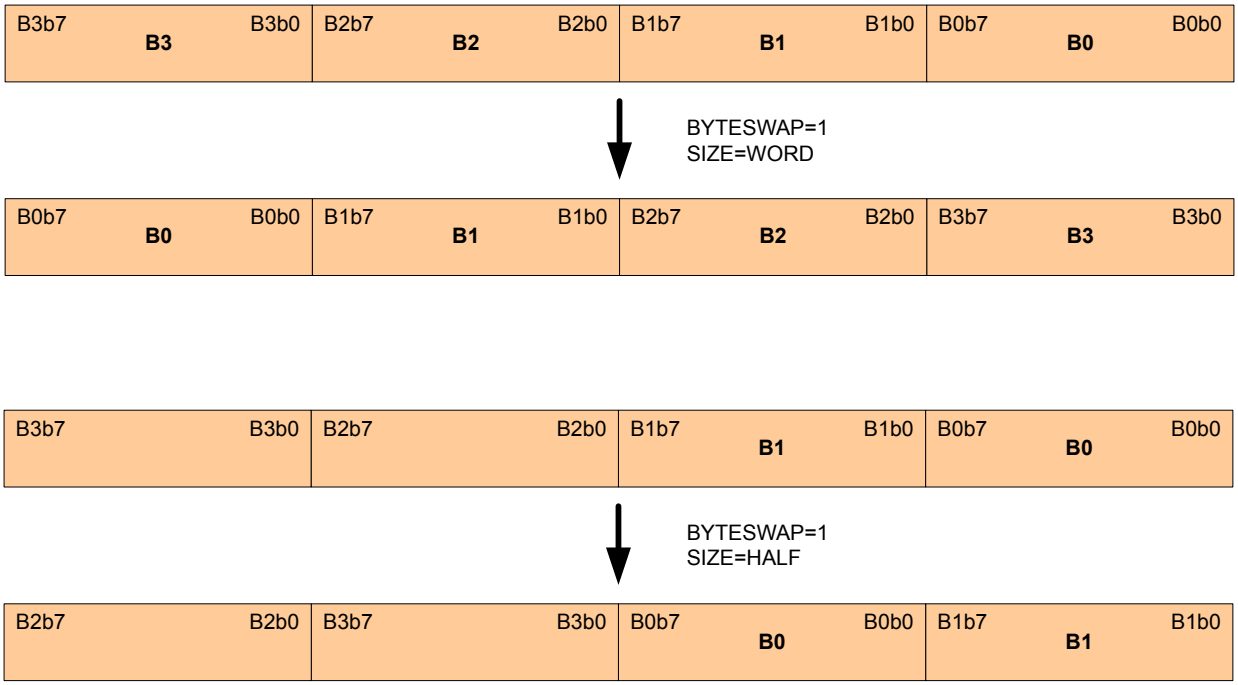


Figure 25.2. Word and Half-Word Endian Byte Swap Examples

25.3.1.9 DMA Size and Source/Destination Increment Programming

The DMA channels' SIZE, SRCINC, and DSTINC bit-fields are programmed to best utilize memory resources. They provide a means for memory packing and unpacking, as well as for matching the size of data being transmitted to or received from an IO peripheral. The following figure shows how 32-bit words of data are read from a memory source into the DMA's internal transfer FIFO, and then written out to the memory destination. The memory organization in bytes is shown as well as the first read to and write from the DMA's FIFO.

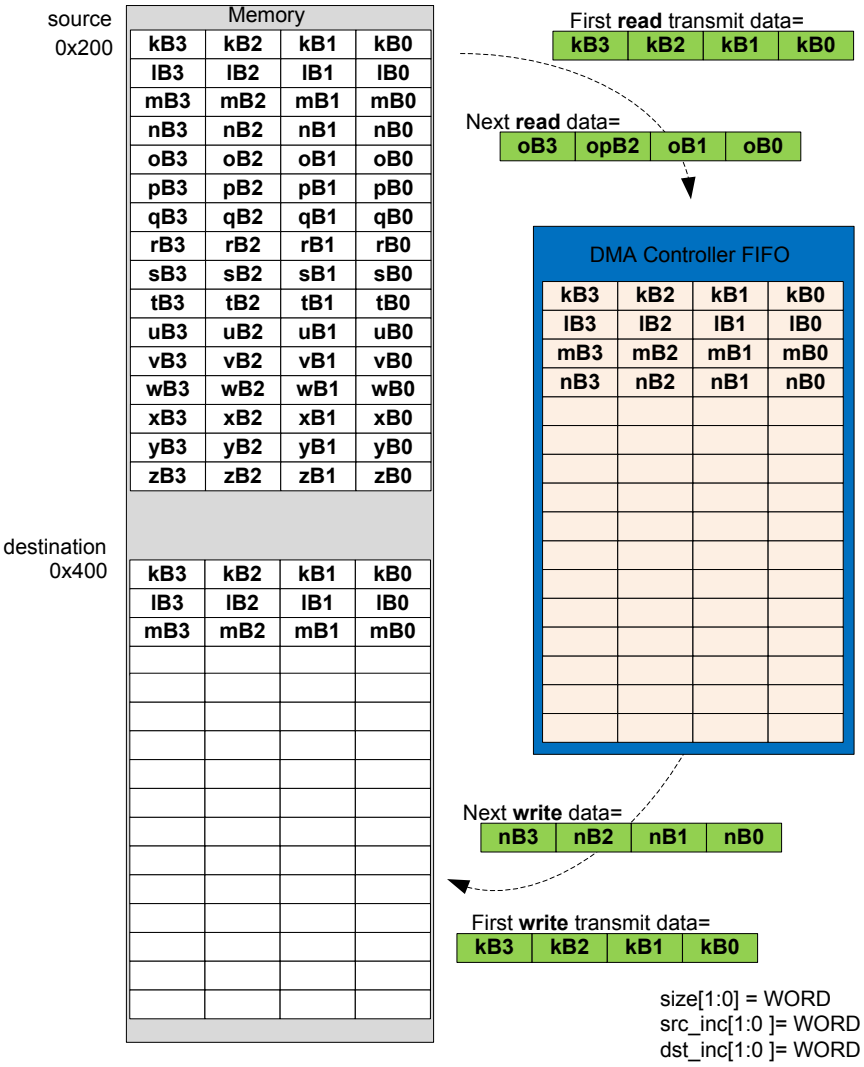


Figure 25.3. Memory-to-Memory Transfer WORD Size Example

The next example shows four variations of half-word sized transfers, with all possible combinations of half- and full-word source and destination increments. Note that when the size and source/destination increments are all configured for half-word, the resulting DMA transfer organization is equivalent to the full-word sized transfer in the previous example. The difference is that the half-word configuration requires twice as many DMA transfers.

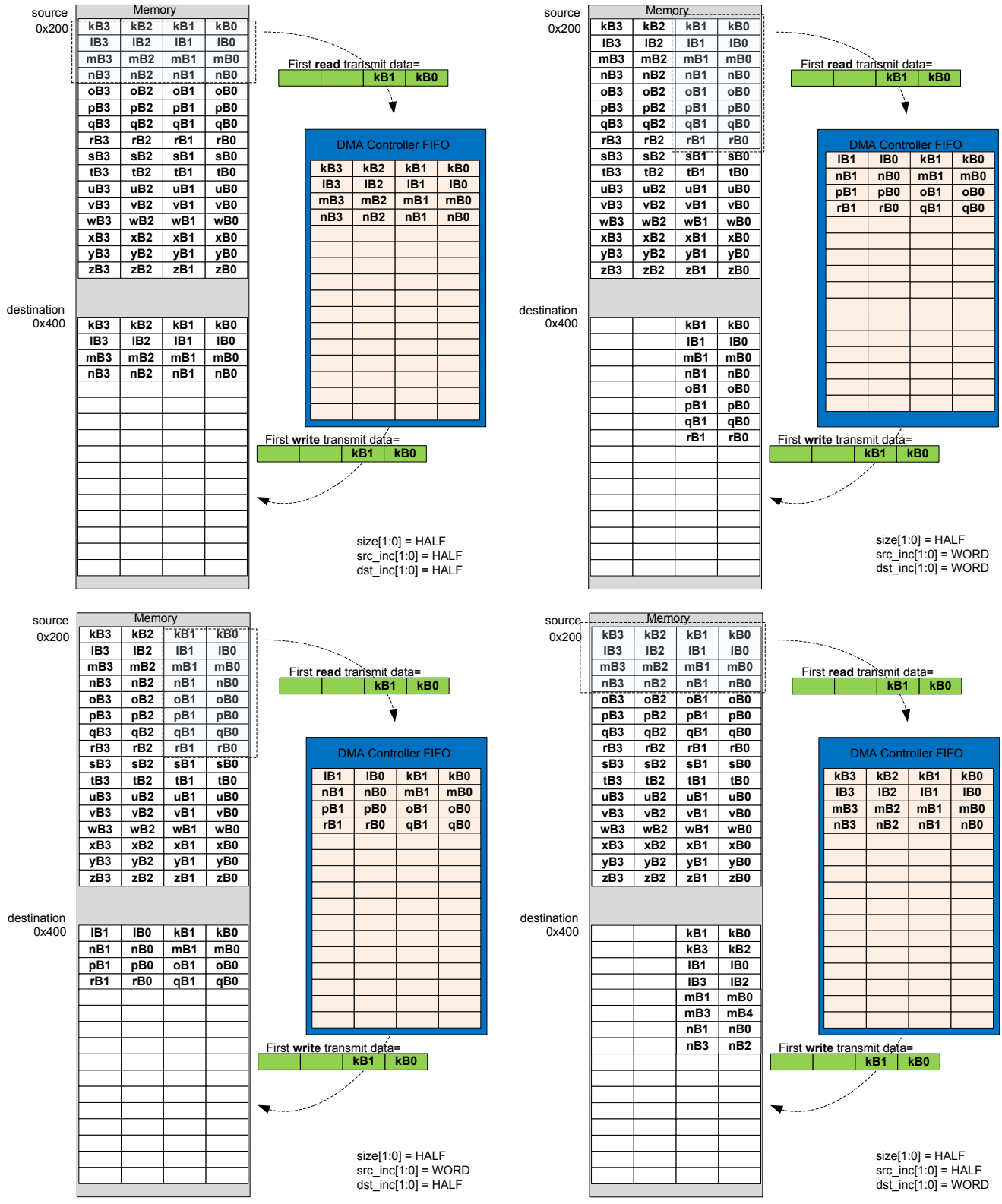


Figure 25.4. Memory-to-Memory Transfer HALF Size Examples

Fields SRCINCSIGN and DSTINCSIGN allow for address decrement. These can be used to mirror an image, for example, in the pixel copy application.

25.3.2 Channel Configuration

Each DMA channel has associated configuration and loop counter registers for controlling direction of address increment , arbitration slots, and descriptor looping.

25.3.2.1 Address Increment/Decrement

Normally DMA transfers increment the source and destination addresses after each DMA transfer. Each channel is also capable of decrementing the source and/or destination addresses after each DMA transfer. This may be useful for flipping an array or copying data from tail to head. For example, a data packet might be prepared as an array of data with increasing addresses and then transmitted from the highest address to the lowest address, from tail to head.

After reset the SRCINCSIGN and DSTINCSIGN bits in the LDMA_CHx_CFG register are cleared causing the source and destination addresses to increment after each transfer. If the SRCINCSIGN bit is set , the DMA will decrement the source address after each transfer. If the DSTINCSIGN bit in the LDMA_CHx_CFG register is set , the DMA will decrement the destination address after each transfer. Setting only one of these bits will flip the data. Setting both bits will copy from tail to head, but will not flip the data.

The SRCINCSIGN and DSTINCSIGN bits apply to all descriptors used by that channel. Software should take care to set the starting source and/or destination address to the highest data address when decrementing.

25.3.2.2 Loop Counter

Each channel has a LDMA_CHx_LOOP register that includes a loop counter field. To use looping, software should initialize the loop counter with the desired number of repetitions before enabling the transfer. A descriptor with the DECLOOPCNT bit set to TRUE will repeat the loop and decrement the loop counter until LOOPCNT = 0.

For a looping descriptor, with DECLOOPCNT=1, the LINK address in the LDMA_CHx_LINK register is used as the loop address. While LOOPCNT is greater than zero, the descriptor will execute and then the LDMA will load the next descriptor using the address specified in the LDMA_CHx_LINK register. This feature enables looping of multiple descriptors. To repeat a single descriptor, the LINK address of the descriptor should point to itself.

After LOOPCNT reaches zero, if the LINK bit in the descriptor LINK word is clear the transfer stops. If the LINK bit is set, the LDMA will load the next sequential descriptor located immediately following the looping descriptor. The behavior of the LINK bit is different for a looping descriptor. This is necessary because the LINK address is re-purposed as the loop address for a looping descriptor.

Note that LOOPCNT sets the number of repeats, not the number of iterations. The total number of loop iterations will be LOOPCNT plus 1. Normally, the LOOPCNT should be set to one or more repeats.

Also note that because there is only one LOOPCNT per channel, software intervention is required to update the LOOPCNT if a sequence of transfers contains multiple loops. It is also possible to use a write immediate DMA data transfer to update the LDMA_CHx_LOOP register.

25.3.3 Channel Select Configuration

The channel select block determines which peripheral request signal connects to each DMA channel.

This configuration is done by software through the SOURCESEL and SIGSEL fields of the LDMA_CHn_REQSEL register. SOURCESEL selects the peripheral and SIGSEL picks which DMA request signals to use from the selected peripheral. Please refer to 25.5 LDMA Source Selection Details for more information.

25.3.4 Starting a Transfer

A transfer may be started by software, a peripheral request, or a descriptor load.

Software may initiate a transfer by setting the bit for the desired channel in the LDMA_SREQ register. In this case the channel should set SOURCESEL to NONE to prevent unintentional triggering of the channel by a peripheral.

A peripheral may trigger the channel by configuring the peripheral source and signal as described in 25.3.3 Channel Select Configuration

The LDMA may also be configured to begin a transfer immediately after a new descriptor is loaded by setting the STRUCTREQ field of the LDMA_CHx_CTRL register or descriptor word.

This configuration is done by software through the SOURCESEL and SIGSEL fields of the LDMA_CHn_REQSEL register. SOURCESEL selects the peripheral and SIGSEL picks which DMA request signals to use from the selected peripheral.

25.3.4.1 Peripheral Transfer Requests

By default peripherals issue a Single Request (SREQ) when any data is present. For peripherals with a data buffer or FIFO this occurs any time the FIFO is not empty. Upon receiving an SREQ the LDMA will perform one DMA transfer and stop till another request is made.

It is generally more efficient to wait for a peripheral to accumulate data and transfer in a burst. This both reduces overhead of the DMA engine and allows EM2 peripherals to save power by using the LDMA less often. To enable this set the IGNORESREQ bit in the LDMA_CHx_CTRL register (or descriptor) which will cause the LDMA to ignore SREQ's and wait for a full Request (REQ) signal. When the REQ is received the entire descriptor will be executed. For most peripherals with a FIFO the REQ signal is set when the FIFO is full, or a predetermined threshold has been reached. See the individual peripheral chapters for more information.

25.3.5 Managing Transfer Errors

LDMA transfer errors are normally managed using interrupts. Software should clear the ERROR flag in the bit in the LDMA_IF register and enable error interrupts by setting the ERROR bit in the LDMA_IEN register before initiating a DMA transfer.

The LDMA interrupt handler should check the ERROR flag bit in the LDMA_IF register. If the ERROR flag bit is set, it should then read the CHERROR field in the LDMA_STATUS register to determine the errant channel. The interrupt handler should reset the channel and clear the ERROR flag bit in the LDMA_IF register before returning.

25.3.6 Arbitration

While multiple channels are configured simultaneously the LDMA engine can only be actively copying data for one channel at a time. Arbitration determines which channel is being serviced at any point in time. The LDMA will choose a channel through arbitration, transfer BLOCK_SIZE elements of that channel and then arbitrate again choosing another channel to service. This allows high priority channels to be serviced while lower priority channels are in the middle of a transfer.

25.3.6.1 Arbitration Priority

There are two modes in determining priority when the controller arbitrates: fixed priority and round robin priority.

In fixed priority mode, channel 0 has the highest priority. As the channel number increases, the priority decreases. When the LDMA controller is idle or when a transfer completes, the highest priority channel with an active request is granted the transfer. This mode guarantees smallest latency for the highest priority requesters. It is best suited for systems where peak bandwidth is well below LDMA controller’s maximum ability to serve. The drawback of this mode is the possibility of starvation for lowest priority requesters.

In the round robin priority mode, each active requesting channel is serviced in the order of priority. A late arriving request on a higher priority channel will not get serviced until the next round. This mode minimizes the risk of starving low-priority latency-tolerant requesters. The drawback of this mode is higher risk of starving low-latency requesters.

The NUMFIXED field in the LDMA_CTRL register determines which channels are fixed priority and which are round robin. Channels lower than NUMFIXED are fixed priority while those above it are round robin. A value of 0x0 implies all channels are round robin. A value of 0x4 implies channels 0 through 3 are fixed priority and 4 through 7 are round robin. A value of 7 implies that channels 0 through 6 are fixed and channel 7 is round robin. This is functionally equivalent to having 8 fixed priority channels.

Fixed priority channels always take priority over round robin. As long as NUMFIXED is greater than 0, there is a possibility that a higher priority channel can starve the remaining channels.

To address the drawbacks of using fixed priority or round robin priority the LDMA implements the concept of arbitration slots. This allows for channels to have high bandwidth and low latency while preventing starvation of latency tolerant low priority channels.

Each channel has a two bit ARBSLOT field in its LDM_CHx_CFG register. This field only applies to channels marked as round robin (determined by NUMFIXED). The channels in the same arbitration slot are treated equally with round robin scheduling. Channels marked with a higher arbitration slot will get serviced more frequently. By default all channels are placed in arbitration slot 1.

Every time the channels in slot 1 get serviced the channels in slot 2 get serviced twice, those in slot 4 get serviced 4 times, and those in slot 8 get serviced 7 times. The specific arbitration allocation can be seen by the following table. The highest arbitration slot is serviced every other arbitration cycle, allowing for low latency response. If there are no requests from channels in arbitration slot then that slot is immediately skipped.

Table 25.1. Arbitration Slot Order

Arbslot order	8	4	8	2	8	4	8	1	8	4	8	2	8	4
Arbslot1								1						
Arbslot2				1								1		
Arbslot4		1				1				1				1
Arbslot8	1		1		1		1		1		1		1	

The top row shows the order at which the arbitration slots are executed. The remaining part of the table shows a more visual interpretation of the arbitration order.

For example, if we have one low latency channel (CHNL0) and two latency tolerant channels (CHNL1 and CHNL2). We could use the following settings.

LDMA_CTRL.NUMFIXED = 0; set round robin for all channels.

CHNL0_CFG.ARBSLOTS = TWO;

CHNL1_CFG.ARBSLOTS = ONE;

CHNL2_CFG.ARBSLOTS = ONE;

If all channels are constantly requesting transfers, then the arbitration order is: CHNL0, CHNL1, CHNL0, CHNL2, CHNL0, CHNL1, CHNL0, CHNL2, CHNL0, etc

Note, there are no channels assigned to arbitration slot four or eight in this example, so those slots are skipped and the final sequence is ARBSLOT2, ARBSLOT1, ARBSLOT2, ARBSLOT1, etc...

Channel 1 and Channel 2 are selected in round robin order when arbitration slot 1 is executed.

If we replace the ARBSLOTS value for channel 0 with EIGHT, then the sequence would look like the following:

CHNL0, CHNL0, CHNL0, CHNL0, CHNL1, CHNL0, CHNL0, CHNL0, CHNL2, CHNL0, CHNL0, CHNL0, CHNL0, CHNL1, etc.

25.3.6.2 DMA Transfer Arbitration

In addition to the inter channel arbitration, software can configure when the controller arbitrates during a DMA transfer. This provides reduced latency to higher priority channels when configuring low priority transfers with more arbitration cycles.

The LDMA provides four bits that configure how many DMA transfers occur before it re-arbitrates. These bits are known as the BLOCKSIZE bits and they map to the arbitration rate as shown below. For example, if BLOCKSIZE = 4 then the arbitration rate is 6, that is, the controller arbitrates every 6 DMA transfers.

Table 25.2 AHB Bus Transfer Arbitration Interval on page 1008 lists the arbitration rates.

Table 25.2. AHB Bus Transfer Arbitration Interval

BLOCKSIZE	Arbitrate After x DMA transfers
0	x = 1
1	x = 2
2	x = 3
3	x = 4
4	x = 6
5	x = 8
6	x = 12
7	x = 16
8	x = 24
9	x = 32
10	x = 64
11	x = 128
12	x = 256
13	x = 512
14	x = 1024
15	x = lock

Note: Software must take care not to assign a low-priority channel with a large BLOCKSIZE because this prevents the controller from servicing high-priority requests, until it re-arbitrates.

The number of DMA transfers that need to be done is specified by the user in XFERCNT. When XFERCNT > BLOCKSIZE and is not an integer multiple of BLOCKSIZE then the controller always performs sequences of BLOCKSIZE transfers until XFERCNT < BLOCKSIZE remain to be transferred. The controller performs the remaining XFERCNT transfers at the end of the DMA cycle.

Software must store the value of the BLOCKSIZE bits in the channel control data structure. See 25.3.7.1 XFER Descriptor Structure for more information about the location of the BLOCKSIZE bits in the data structure.

25.3.7 Channel Descriptor Data Structure

Each channel descriptor consists of four 32-bit words:

- CTRL - control word contains information like transfer count and block size.
- SRC - source address points to where to copy data from
- DST - destination address points to where to copy data to
- LINK - link address points to where to load the next linked descriptor

These words map directly to the LDMA_CHx_CTRL, LDMA_CHx_SRC, LDMA_CHx_DST, and LDMA_CHx_LINK registers. The usage of the SRC and DST fields may differ depending on the structure type

There are three different types of descriptor data structures: **XFER, SYNC, and WRI**

25.3.7.1 XFER Descriptor Structure

This descriptor defines a typical data transfer which may be a Normal, Link, or Loop transfer.

Only this structure type can be written directly into LDMA's registers by the CPU. All descriptors may be linked to. Please refer to the register descriptions for additional information.

For specifying XFER structure type, set STRUCTTYPE to 0. Please see the peripheral register descriptions for information on the fields in this structure.

Name	Bit Position																													
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTRL	DSTMODE	SRCMODE	DSTINC		SIZE		SRCINC		IGNORESREQ	DECLOOPCNT	REQMODE	DONEIFSEN	BLOCKSIZE				BYTESWAP	XFERCNT											STRUCTREQ		STRUCTTYPE	
SRC	SRCADDR																															
DST	DSTADDR																															
LINK	LINKADDR																														LINK	LINKMODE

25.3.7.2 SYNC Descriptor Structure

This descriptor defines an intra-channel synchronizing structure. It allows the channel to wait for some external stimulus before continuing on to the next descriptor. This structure is also used to provide stimulus to another channel to indicate that it may continue.

For example channel 1 may be configured to transfer a header into a buffer while channel 2 is simultaneously transferring data into the same structure. When channel 1 has completed it can wait for a sync signal from channel 2 before transferring the now complete buffer to a peripheral.

Synch descriptors do nothing until a condition is met. The condition is formed by the SYNCTRIG field in the LDMA_SYNC register and the MATCHEN and MATCHVAL fields of the descriptor. When (SYNCTRIG & MATCHEN) == (MATCHVAL & MATCHEN) the next descriptor is loaded. In addition to waiting for the condition a Link descriptor can set or clear bits in SYNCTRIG to meet the conditions of another channel and cause it to continue. The CPU also has the ability to set and clear the SYNCTRIG bits from software.

This structure type can only be linked in from memory.

For specifying SYNC structure type, set STRUCTTYPE to 1.

Name	Bit Position																													
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTRL												DONEIFSEN																			STRUCTTYPE	
SRC																																
DST																																
LINK	LINKADDR																														LINK	LINKMODE

Bit	Name	Description
1:0	STRUCTTYPE	**Descriptor Type**
	This field indicates which type of descriptor this is. It must be 1 for a SYNC descriptor.	
20	DONEIFSEN	**Done if Set indicator**
	If set the interrupt flag will be set when descriptor completes.	
15:8	SYNCCLR	**Sync Trigger Clear**
	This bit-field is used to clear corresponding bits within the SYNCTRIG field of the SYNC LDMA_SYNC register. To clear a given bit, a one should be loaded to the corresponding bit. Set is given priority over clear if both corresponding bits are loaded with a one. The sync trigger clear function can only be used when loaded from a linked structure. Alternately, the user can directly write the SYNCTRIG bit-field if required.	
7:0	SYNCSET	**Sync Trigger Set**
	This bit-field is used to set corresponding bits within the SYNCTRIG bit-field. To set a given bit, a one should be loaded to the corresponding bit. Set is given priority over clear if both corresponding bits are loaded with a one. The sync trigger set function can only be used when loaded from a linked structure. Alternately, the user can directly write the SYNCTRIG bit-field if required.	
15:8	MATCHEN	**Sync Trigger Match Enable**
	This bit-field serves as the SYNCTRIG match enable. A sync match triggers the load of the next linked DMA structure as specified by link_mode, when: (SYNCTRIG & MATCHEN) == (MATCHVAL & MATCHEN).	
7:0	MATCHVAL	**Sync Trigger Match Value**

Bit	Name	Description
		This bit-field serves as the SYNCTRIG match value. A sync match triggers the load of the next linked DMA structure as specified by link_mode, when: (SYNCTRIG & MATCHEN) == (MATCHVAL & MATCHEN).

25.3.7.3 WRI Descriptor Structure

This descriptor defines a write-immediate structure. This allows a list of descriptors to write a value to a register or memory location. For example, if a channel wishes to perform two loops in a descriptor sequence a WRI may be used to program the loop count for the second loop.

This structure type can only be linked in from memory.

For specifying WRI structure type, set STRUCTTYPE to 2.

Name	Bit Position																													
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTRL												DONEIFSEN																			STRUCTTYPE	
SRC																																
DST	DSTADDR																															
LINK	LINKADDR																														LINK	LINKMODE

Bit	Name	Description
1:0	STRUCTTYPE	**Descriptor Type**
		This field indicates which type of descriptor this is. It must be 2 for a WRI descriptor.
20	DONEIFSEN	**Done if Set indicator**
		If set the interrupt flag will be set when descriptor completes.
31:0	IMMVAL	**Immediate Value for Write**
		This bit-field specifies the immediate data value that is to be written to the address pointed to by DSTADDR. Only one write occurs for WRI structures.
31:0	DSTADDR	**Address to write**
		This bit-field specifies the address the immediate data should be written to.

25.3.8 Interaction with the EMU

The LDMA interacts with the Energy Management Unit (EMU) to allow transfers from a low energy peripheral while in EM2.

When using the ADC in EM2 or EM3 the EMU can wake up the LDMA as needed to allow data transfers to occur.

25.3.9 Interrupts

The LDMA_IF Interrupt flag register contains one DONE bit for each channel and one combined ERROR bit. When enabled, these interrupts are available as interrupts to the M33 core. They are combined into one interrupt vector, DMA_INT. If the interrupt for the DMA is enabled in the ARM M33 core, an interrupt will be made if one or more of the interrupt flags in LDMA_IF and their corresponding bits in LDMA_IEN are set.

When a descriptor finishes execution the interrupt flag for that channel will be set if the DONEIFSEN field of the LDMA_CHx_LOOP register is set. If LINK and DONEIFSEN are both set when the descriptor completes the interrupt and the linked descriptor will be immediately loaded. When the final descriptor in a linked list (LINK = 0) is finished the interrupt flag is always set regardless of the state of DONEIFSEN.

25.3.10 Debugging

For a peripheral request DMA transfer, if software sets a bit for a channel in the LDMA_DBGHALT register then the DMA will halt during a debug halt and the SRC and DST registers in the debug window will show the transfer in progress. Otherwise, during debug halt the DMA will continue to run and complete the entire transfer causing the descriptor registers to indicate the transfer has completed.

25.3.11 Multi-port transfers

The LDMA has two bus main ports and supports transfers between them in either direction.

Which busport the LDMA uses as the source and destination for the transfer is fully configurable using the SRCBUSPORT and DSTBUSPORT bits in the CHn_CFG register.

Where to read in the next descriptor struct is configured with the STRUCTBUSPORT bit in the same register.

Short transfers between bus main ports will incur some performance loss due to synchronization and handshaking between the busports around starting and ending the transfer.

25.3.12 Extended struct

By setting the EXTEND bit in the CHn_CTRL register the MMLDMA expect a struct size of 8 words instead of the regular 4 words.

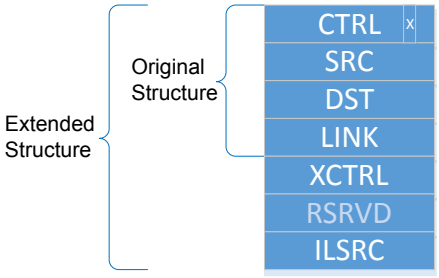


Figure 25.5. Struct and extended struct

In these additonal words, interleaving is available and the bufferable property can be configured.

25.3.13 Destination Interleaving

The LDMA supports rule-based destination interleaving, a flexible method for interleaving vectors of data which allows reading a continous stream of source data and writing it to scattered destination locations. The rules for where data is scattered or interleaved is determined by a separate table in memory with one address rule entry per unit data. This table will be read starting from the CHn_ILSRC address on the bus port that is not used for reading source data.

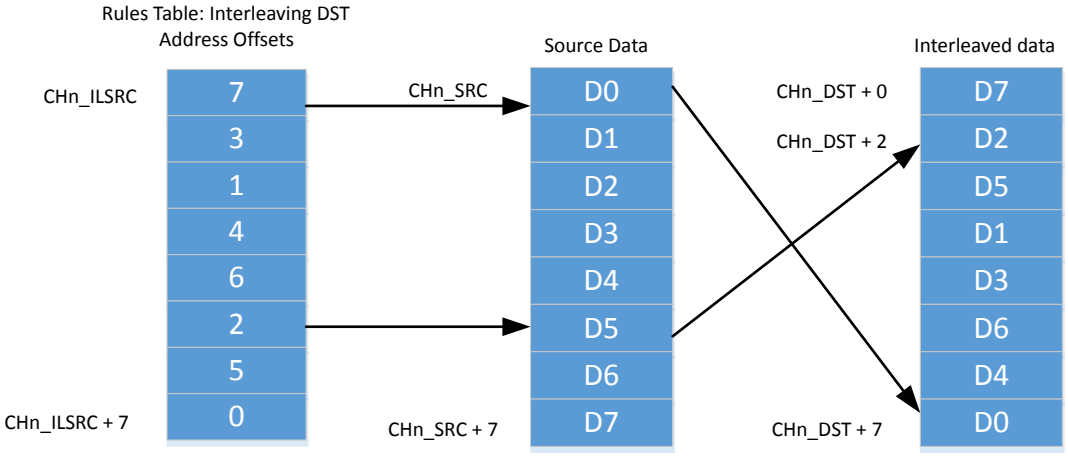


Figure 25.6. Destination Interleaving RELATIVE8 Example

Interleaving is enabled with the DSTILEN bit in CHn_XCTRL and can be applied in 3 different modes configured with the ILMODE bit field in the same register.

ABSOLUTE: An array of XFERCNT+1 32bit addresses are read from CHn_ILSRC.

```
uint32_t interleaving_address_array[xfercnt+1];
                  ...
                  LDMA->CH[x].XCTRL = LDMA_CH_XCTRL_DSTILEN |
                  LDMA_CH_XCTRL_ILMODE_ABSOLUTE;
                  LDMA->CH[x].ILSRC = interleaving_address_array;
```

RELATIVE16 An array of XFERCNT+1 16bit offsets are read from CHn_ILSRC. The offsets are applied to the DST address.

```
uint16_t interleaving_offset_array[xfercnt+1];
                  ...
                  LDMA->CH[x].XCTRL = LDMA_CH_XCTRL_DSTILEN |
                  LDMA_CH_XCTRL_ILMODE_ABSOLUTE;
                  LDMA->CH[x].ILSRC = interleaving_offset_array;
                  LDMA->CH[x].DST   = start_address;
```

RELATIVE8

An array of XFERCNT+1 single byte offsets are read from CHn_ILSRC. The offsets are applied to the DST address.

```
uint8_t interleaving_offset_array[xfercnt+1];
                  ...
                  LDMA->CH[x].XCTRL = LDMA_CH_XCTRL_DSTILEN |
                  LDMA_CH_XCTRL_ILMODE_ABSOLUTE;
                  LDMA->CH[x].ILSRC = interleaving_offset_array;
                  LDMA->CH[x].DST   = start_address;
```

The Interleaving configuration registers are placed in the extended part of the descriptor and therefore requires the EXTEND bit in CHn_CTRL to be set when configured through linking.

25.3.14 Disablement

Disablement is triggered by setting the EN bit in the EN register to 0. The disablement is completed when the DISABLING bit in the EN register goes low.

```
LDMA->EN_CLR = LDMA_EN_EN;                  // Trigger disablement
                while (LDMA->EN & LDMA_EN_DISABLING);       // Wait for disablement to complete
```

In additon to stopping the LDMA and putting it in a low power state disablement of the LDMA will disable all channels and clear pending link load operations. All other control and configuration registers will keep their value.

Once the LDMA is disabled, registers that can be modified by the LDMA FSM will not be writable. This means that only the following registers can be written when EN=0:

- EN
- SWRST
- CTRL
- SYNCHWEN
- SYNCHWSEL
- DBGHALT
- CHn_CFG

When triggering disablement in the middle of a transfer the dma will not complete the transfer and could result in data loss and incorrect status. To ensure all transfers are fully completed disabling all channels and waiting for the ANYBUSY bit is recommended before disablement.

```
LDMA->CHDIS = _LDMA_CHDIS_MASK;             // Stop all channels
                while (LDMA->STATUS & LDMA_STATUS_ANYBUSY); // Wait until stopped

                LDMA->EN_CLR = LDMA_EN_EN;                  // Trigger disablement
                while (LDMA->EN & LDMA_EN_DISABLING);       // Wait for disablement to complete
```

25.3.15 Software Reset

Software reset is triggered by writing the SWRST bit in the SWRST register. It is completed when the RESETTING bit in the SWRST register goes low.

```
LDMA->SWRST = LDMA_SWRST_SWRST;             // Trigger software reset
               while (LDMA->SWRST & LDMA_SWRST_RESETTING); // Wait for software reset to complete
```

SWRST will reset all registers in the LDMA and put it in the same state as after a power on reset.

When triggering SWRST in the middle of a transfer the dma will not complete the transfer, so disabling all channels and waiting for the ANYBUSY bit before swrst is recommended.

```
LDMA->CHDIS = _LDMA_CHDIS_MASK;             // Stop all channels
                while (LDMA->STATUS & LDMA_STATUS_ANYBUSY); // Wait until stopped

                LDMA->SWRST = LDMA_SWRST_SWRST;             // Trigger software reset
                while (LDMA->SWRST & LDMA_SWRST_RESETTING); // Wait for software reset to complete
```

25.4 Examples

This section provides examples of common LDMA usage. All examples assume the LDMA is in the reset state with the channel being configured disabled and LDAM_CHx_CFG, LDMA_CHx_LOOP, and LDMA_CHx_LINK cleared.

25.4.1 Single Direct Register DMA Transfer

This simple example uses only the Channel Descriptor registers directly and does not use linking. Software writes directly to the LDMA channel registers. This example does not use a memory based descriptor list.

This example is suitable for most simple transfers that are limited to transferring one block of data. It supports anything that can be done using a single descriptor. This includes endian conversion and packing/unpacking data. Channel 0 is used for this example.

The LDMA will be used to copy 127 contiguous half words (254 bytes) from 0x0 to 0x1000. It will allow arbitration every 4 transfers and is triggered by a CPU write to the LDMA_SWREQ register. The CH0 interrupt flag will be set when the transfer completes since the descriptor does not link to another descriptor.

- Configure LDMA_CH0_CTRL
  - DSTMODE = 0 (absolute)
  - SRCMODE = 0 (absolute)
  - SIZE = HALFWORD (16 bits)
  - DSTINC = 0 (1 half-word)
  - SRCINC = 0 (1 half-word)
  - DECLOOPCNT=0 (unused)
  - REQMODE = 1 (one request transfers all data)
  - BLOCKSIZE = 3 (4 transfers)
  - BYTESWAP=0 (no byte swap)
  - XFERCNT=127 (transfer 127 half words)
  - STRUCTTPYE=0 (TRANSFER)
- Write source address to LDMA_CH0_SRC register
- Write destination address to LDMA_CH0_DST register
- Configure the LDMA_CH0REQSEL register for the desired peripheral or select none for a memory-to-memory transfer
- Clear and enable interrupts.
  - Write a 1 to bit 0 of the LDMA_IFC register to clear the CH0 DONE flag
  - Write a 1 to bit 0 of the LDMA_IEN register to enable the CH0 interrupt
- Write a 1 to bit 0 of the LDMA_CHEN register to enable CH0

The REQMODE field is normally cleared to zero for a peripheral request transfer and will transfer the specified block size for each peripheral request. The REQMODE may be set to 1 for a memory-to-memory transfer or any time it is desired for a single DMA request to initiate complete transfer.

25.4.2 Descriptor Linked List

This example shows how to use a Linked List of descriptors. Each descriptor has a link address which points to the next descriptor in the list. A descriptor may be removed from the Linked list by altering the Link address of the one before it to point to the one after it. Descriptor Linked lists are useful when handling an array of buffers for communication data. For example, a bad packet can be removed from a receiver queue by simply removing the descriptor from the linked list.

Software loads the first descriptor into the DMA by writing the descriptor address to LDMA_CHx_LINK and setting the bit for that channel in the LDMA_LINKLOAD register. This method is preferred when using a linked list in memory since it treats the first descriptor just like all the others. However, it is also allowed for software to write the first descriptor directly to the LDMA registers.

In this example 4 descriptors are executed in series. the interrupt flag is set after the 2nd and 4th (last) descriptors have completed.

- Prepare a list of descriptors using the XFER structure type in RAM
- Initialize the CTRL, SRC, and DST members as desired
  - Setting STRUCTREQ in the CTRL word for descriptors 2-4 will cause them to begin transferring data as soon as they are loaded.
- Write 0x00000013 to the LINK member of all but the last descriptor
  - LINKMODE = 1 (relative addressing)
  - LINK = 1 (Link to the next descriptor)
  - LINKADDR = 0x00000010 (size of descriptor)
- Set the DONEIFSEN bit in the CTRL member of the 2nd structure so that the interrupt flag will be set when it completes
- Write 0x00000000 to the LINK member of the last descriptor
  - LINK = 0 (Do not link to the next descriptor)
  - LINKMODE = 0 (don't care)
  - LINKADDR = 0x00000000 (don't care)

Each descriptor now points to the start of the next descriptor as shown on the left in Figure 25.7 Descriptor Linked List on page 1016. To remove a descriptor from the linked list modify the LINK address of the descriptor of the one before to point to the one after. For example to remove the third descriptor, add 0x00000010 to the LINK register of the second descriptor. The second descriptor will now point to the forth descriptor and skip over the third descriptor as shown on the right in Figure 25.7 Descriptor Linked List on page 1016.

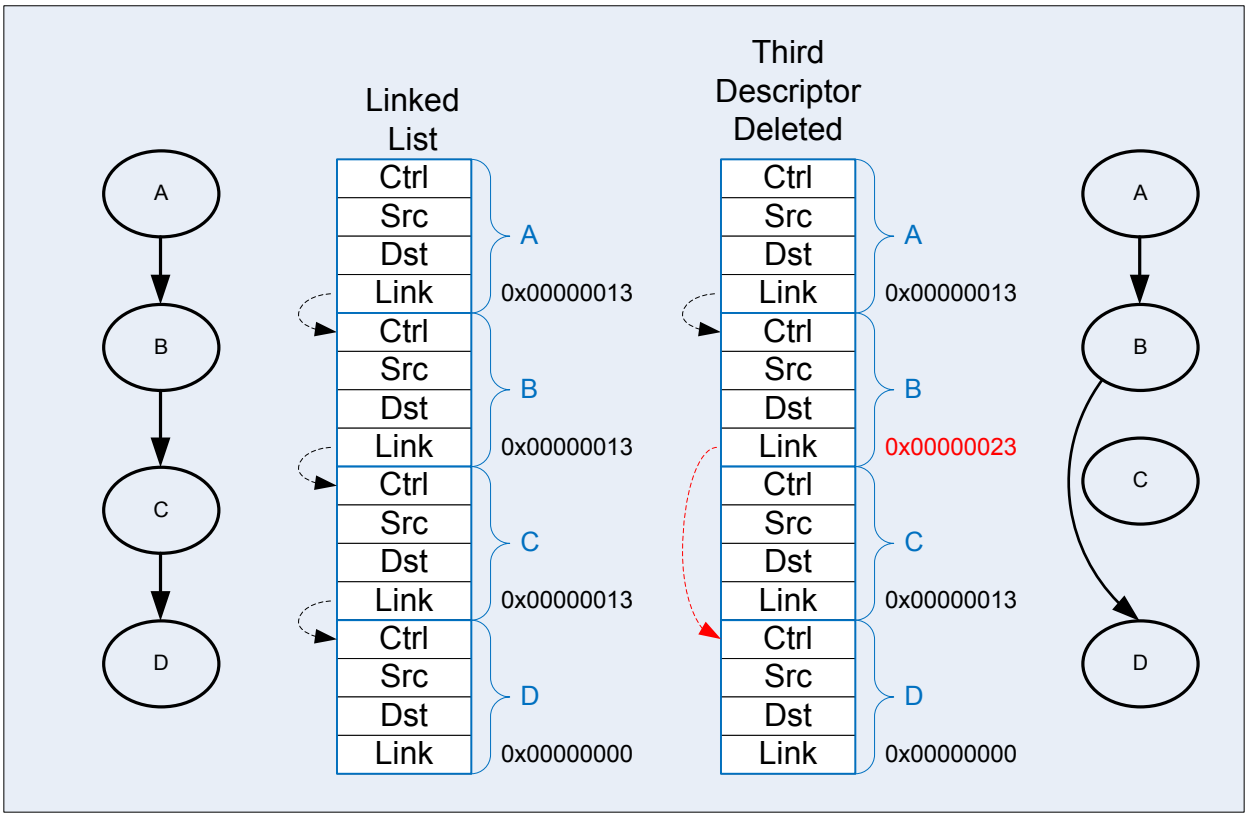


Figure 25.7. Descriptor Linked List

To start execution of the linked list of descriptors:

- Write the absolute address of the first descriptor to the LINKADR field of the LDMA_CH0_LINK register
- Set the LINK bit of LDMA_CH0_LINK register.
- Configure the LDMA_CH0REQSEL register for the desired peripheral or select none for memory-to-memory
- Clear and enable interrupts as desired
- Set bit 0 in the LDMA_LINKLOAD register to initiate loading and execution of the first descriptor

Alternatively, software can manually copy the first descriptor contents to the LDMA_CH0_CTRL, LDMA_CH0_SRC, LDMA_CH0_DST, and LDMA_CH0_LINK registers and then enable the channel in the LDMA_CHEN register.

25.4.3 Single Descriptor Looped Transfer

This example demonstrates how to use looping using a single descriptor. This method allows a single DMA transfer to be repeated a specified number of times. The looping descriptor is stored in memory and reloaded by hardware. After a specified number of iterations, the transfer stops.

CH0 is setup to copy 4 words from the ADC FIFO into a 15 word buffer at 0x1000. It repeats 4 times to fill the entire 16 word buffer. An interrupt will fire when the entire 16 words have been transferred.

Initialize the Linked descriptor in memory as follows:

- Configure CTRL member
  - DSTMODE = 0 (absolute)
  - SRCMODE = 0 (absolute)
  - SIZE = WORD
  - DSTINC = 0 (1 WORD)
  - SRCINC = 3 (0 WORDS)
  - DECLOOPCNT=1 (decrement loop count)
  - REQMODE=1 (Use XFERCNT)
  - BLOCKSIZE = 4 (4 words)
  - BYTESWAP=0 (no swap)
  - XFERCNT= 4 (4 words)
  - STRUCTTPYE=0 (TRANSFER)
  - IGNORESREQ=1 (ignore single requests)
- Write the address ADC0_SINGLEDATA register to the SRC member
- Write 0x1000 address to DST member
- Configure the LINK member
  - LINK = 0 (stop after loop)
  - MODE = 1 (relative link address)
  - LINKADDR = 0 (point to ourself)
- Configure the Channel
  - Write the desired number of repeats to the LDMA_CH0_LOOP register
  - SOURCESEL in LDMA_CH0REQSEL = ADC0 (select the ADC)
  - SIG in LDMA_CH0REQSEL = ADC0SCAN (select the scan conversion request)
- Clear and enable interrupts
- Load the descriptor using LINKLOAD as described in 25.4.2 Descriptor Linked List

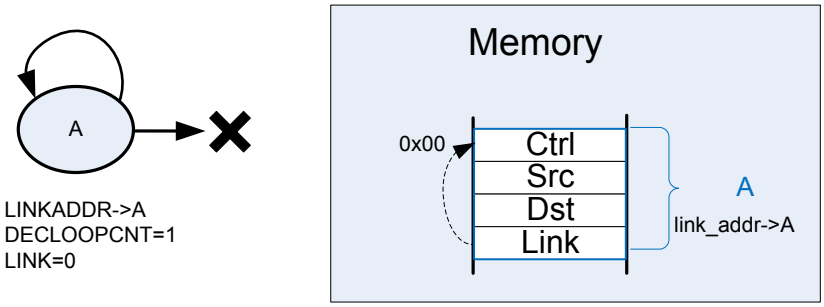


Figure 25.8. Single Descriptor Looped Transfer

Note that the looping descriptor must be stored in memory, because it must load itself from the link address in memory on each iteration.

25.4.4 Descriptor List with Looping

This example uses a descriptor list in memory with looping over multiple descriptors. This example also uses the looping feature and continues on with the next sequential descriptor after looping completes.

The descriptor list in memory is shown in figure Figure 25.9 Descriptor List with Looping on page 1019. Descriptor A links to descriptor B. Descriptor B has the DECLOOPCNT bit enabled and loops back to the start of descriptor A. The LINK address of descriptor B is used for the loop address. The LINK bit is set to indicate that execution will continue after completion of looping. Once the LOOPCNT reaches zero, the LDMA will load descriptor C. Descriptor C must be located immediately following descriptor B.

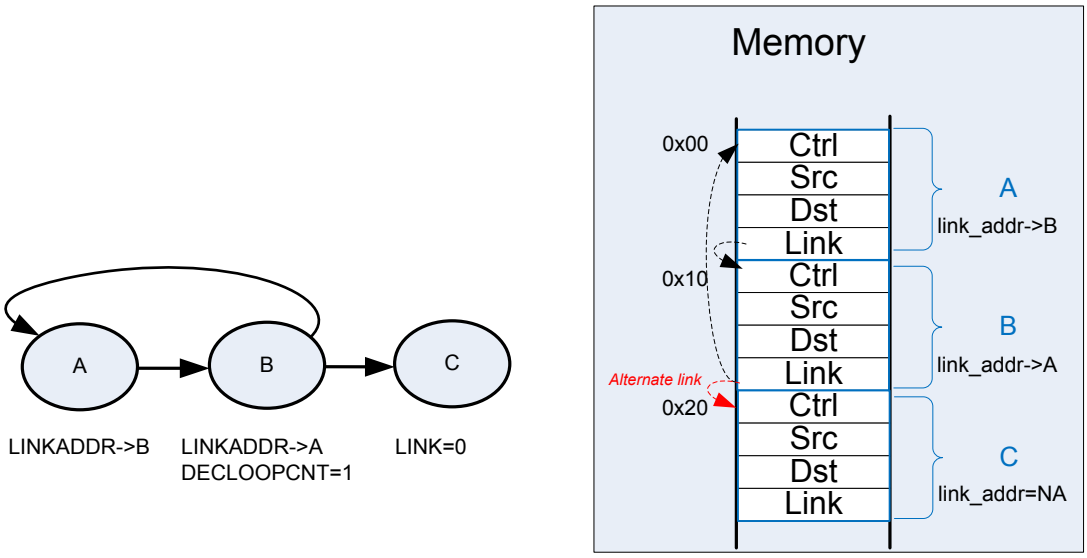


Figure 25.9. Descriptor List with Looping

Initialization is similar to the single looping descriptor with the following modifications.

- Set the LINK bit in descriptors A and B
- write the address of descriptor A into the LIKADDRESS of descriptor B
- write the address of descriptor B into the LIKADDRESS of descriptor A
- Descriptor C must be located immediately after descriptor B in memory

25.4.5 Simple Inter-Channel Synchronization

The LDMA controller features synchronization structures which allow differing channels and/or hardware events to pause a DMA sequence, and wait for a synchronizing event to restart it.

In this example DMA channel 0 and 1 are tasked with the transfer of different sets of data. Channel 0 has two transfer structures, and channel 1 just one, but channel 0 must wait until channel 1 has completed its transfer before it starts its second transfer structure.

Pausing channel 0 is accomplished by inserting a sync wait structure between the two transfer structures. This sync structure waits on SYNCTRIG[7] to be set by a sync set/clear structure which is controlled by channel 1. Sync structures do not transfer data, they can only set, clear, or wait to match the SYNCTRIG[7:0] bits. Note that sync structures cannot decrement loop counter.

```
LDMA_SYNC
    SYNCTRIG=0x0 (at time 0)

LDMA_CH0

    Structure A @ 0x00              Structure B @ 0x10                  Structure C @ 0x20
    CTRL                                CTRL                                CTRL
        STRUCTTYPE=XFER                     STRUCTTYPE=SYNC                     STRUCTTYPE=XFER
    LINK                                LINK                                LINK
        LINKADDR[29:0]=0x00000004           LINKADDR[29:0]=0x00000008           LINKADDR[29:0]=NA
        LINK=1                              LINK=1                              LINK=0
                                        DST
                                            MATCHEN=0x80
                                            MATCHVAL=0x80 (waits for SYNCTRIG[7]=1)

LDMA_CH1

    Structure Y @ 0x30              Structure Z @ 0x40

    CTRL                                CTRL
        STRUCTTYPE=XFER                     STRUCTTYPE=SYNC
    LINK                                LINK
        LINKADDR[29:0]=0x00000010           LINKADDR=NA
        LINK=1                              LINK=0
                                        SRC
                                            SRCCLR=0x0
                                            SRCSET=0x80 (sets SYNCTRIG[7])
```

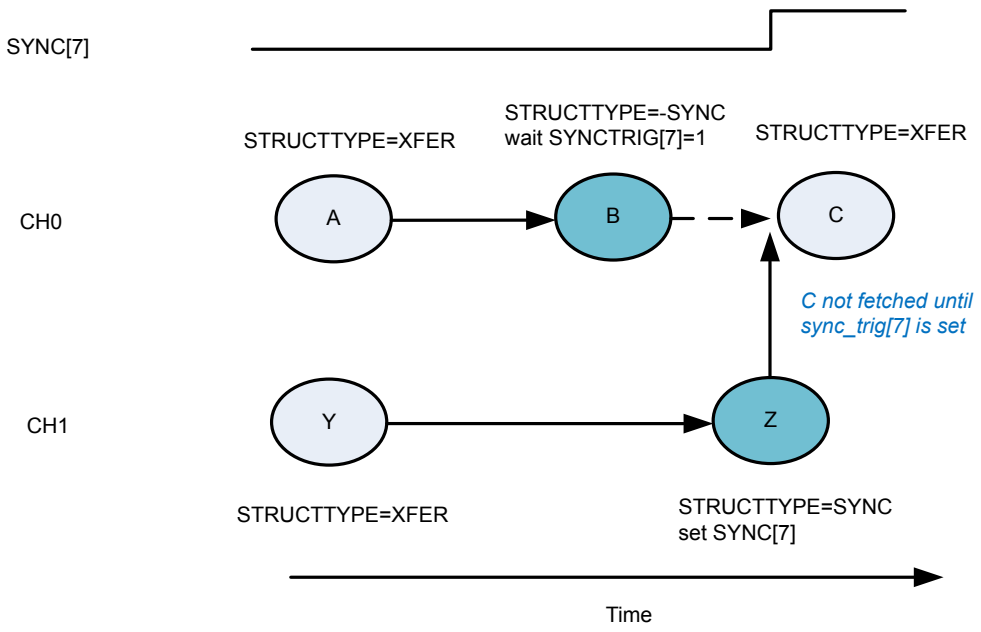


Figure 25.10. Simple Intra-channel Synchronization Example

Both A and Y effectively start at the same time. A finishes earlier, then it links to B, which waits for the SYNCTRIG[7] bit to be set before loading C. Y finishes after B is loaded, and it links to sync structure Z, which sets the SYNCTRIG[7] bit. Channel 0 responds to the trigger set by loading C for the final data transfer.

25.4.6 2D Copy

The LDMA can easily perform a 2D copy using a descriptor list with looping. This set up is visualized in Figure 25.11 2D Copy on page 1022.

For an application working with graphics, this would mean the ability to copy a rectangle of a given width and height from one picture to another.

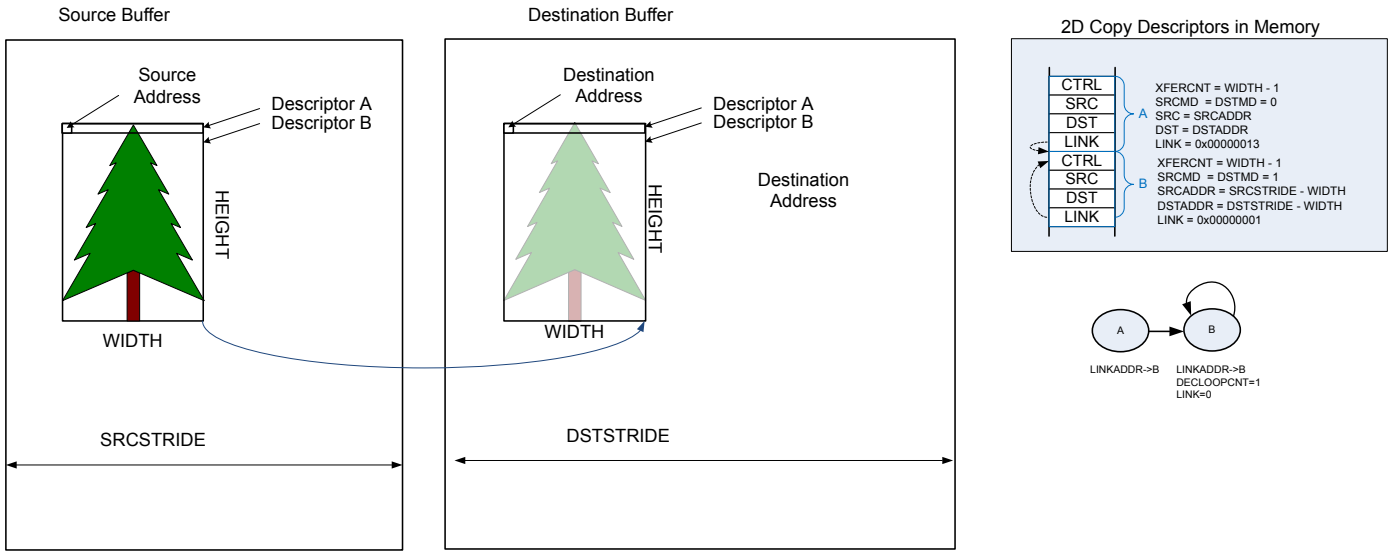


Figure 25.11. 2D Copy

The first descriptor will use absolute addressing mode and the source and destination addresses should point to the desired target addresses. The first descriptor will copy only the first row. The XFERCNT of the first descriptor is set to the desired width minus one.

- CTRL
  - XFERCNT = WIDTH - 1
  - SRCMD = 0 (absolute)
  - DSTMD = 0 (absolute)
- SRCADDR = target source address
- DSTADDR = target destination address
- LINK = 0x00000013
  - LINK=1
  - LINKMD=1
  - LINKADDR=0x00000010 (point to next descriptor)

The second descriptor will use relative addressing and the source and destination addresses are set to the desired offset. After the completion of the first descriptor, the address registers will point to the last address transferred. Thus, the width must be subtracted from the stride to get the offset. The second descriptor uses looping and the link register has not offset.

- CTRL
  - XFERCNT = WIDTH - 1
  - SRCMD = 1 (relative)
  - DSTMD = 1 (relative)
  - DECLOOPCNT = 1
- SRCADDR = desired source offset (SRCSTRIDE-WIDTH)
- DSTADDR = desired destination offset (DSTSTRIDE-WIDTH)
- LINK = 0x00000001
  - LINK=0
  - LINKMD=1 (relative)
  - LINKADDR=0x000000000 (no offset)

Because the first descriptor already transferred one row, the number of looping repeats should be the desired height minus two. Therefore, LOOPCNT should be set to HEIGHT minus two before initiating the transfer.

This same method is easily extended to copy multiple rectangles by linking descriptors together. To initialize the LDMA_CHx_LOOP register, precede each descriptor pair described above with a write immediate descriptor which writes the desired value to the LOOPCNT field of the LDMA_CHx_LOOP register.

25.4.7 Ping-Pong

Communication peripherals often use ping-pong buffers. Ping-pong buffers allow the CPU to process data in one buffer while a peripheral transmits or receives data in the other buffer.

Both transmit and receive ping-pong buffers are easily implemented using the LDMA. In either case, this requires two descriptors as shown in Figure 25.12 Infinite Ping-Pong Example on page 1024. The LINKADDR field of the LINK member should point to the other descriptor. Using two adjacent descriptors and relative link addressing ensures the descriptors are easily reloadable.

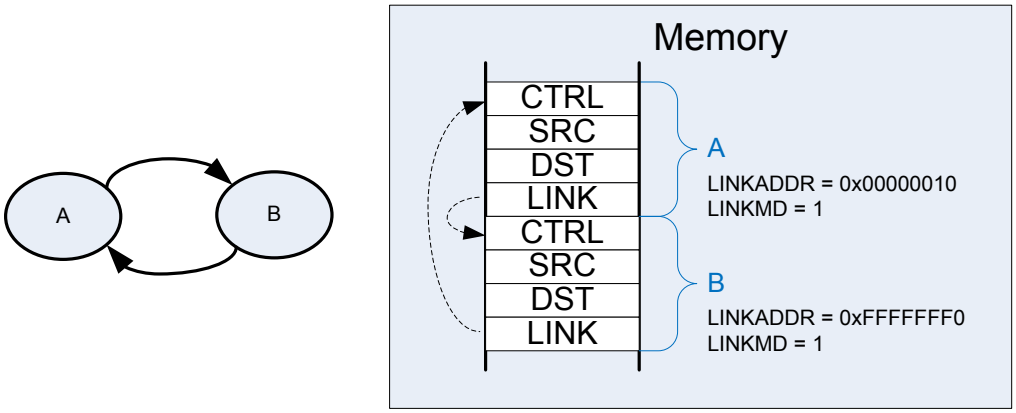


Figure 25.12. Infinite Ping-Pong Example

A **receiver** ping-pong buffer controller consists of two buffers and two descriptors stored in memory that point to the two buffers. Once initialized, as the peripheral receives data, it will fill the first buffer. Once the first buffer is full, it will link automatically to the second buffer and generate an interrupt. Software will then process the data in the first buffer while the LDMA is transferring data to the second buffer. For a receiver ping-pong buffer each descriptor should link to the other descriptor. The link bit should be set to provide infinite ping pong between the two buffers. The DONIFS bit in each descriptor should be set to generate an interrupt on the completion of each descriptor.

- Descriptor A
  - CTRL
    - DONEIFS = 1
    - other settings as desired
  - SRCADDR = peripheral source address
  - DSTADDR = memory destination address
  - LINK = 0x00000013
    - LINKADDR = 0x00000010 (next descriptor)
    - LINK = 1 (link to next descriptor)
    - LINKMD = 1 (relative addressing)
- Descriptor B
  - CTRL
    - DONEIFS = 1
    - other settings as desired
  - SRCADDR = peripheral source address
  - DSTADDR = memory destination address
  - LINK = 0xFFFFFFF3
    - LINKADDR = 0xFFFFFFF0 (previous descriptor)
    - LINK = 1 (link to previous descriptor)
    - LINKMD = 1 (relative addressing)

For **transmitter** ping-pong buffer, software will fill the first buffer and then initiate the DMA transfer. The LDMA will transmit the first buffer data while software is filling the second buffer. In this case, the two descriptors should point to each other, but not automatically

continue to the second buffer. The LINK bit should be cleared to zero. Once software has loaded the first buffer, it will use the LINK-LOAD bit to load the first descriptor and transmit the data. The DONIFS need not be set in each descriptor. The DMA will stop and then generate an interrupt at the completion of each descriptor.

- Descriptor A
  - CTRL
    - DONEIFS = 0
    - other settings as desired
  - SRCADDR = memory source address
  - DSTADDR = peripheral destination address
  - LINK = 0x00000013
    - LINKADDR = 0x00000010 (next descriptor)
    - LINK = 0 (link to next descriptor)
    - LINKMD = 1 (relative addressing)
- Descriptor B
  - CTRL
    - DONEIFS = 0
    - other settings as desired
  - SRCADDR = memory source address
  - DSTADDR = peripheral destination address
  - LINK = 0xFFFFFFF3
    - LINKADDR = 0xFFFFFFF0 (previous descriptor)
    - LINK = 0 (link to previous descriptor)
    - LINKMD = 1 (relative addressing)

25.4.8 Scatter-Gather

Scatter-Gather in general refers to a process that copies data from multiple locations scattered in memory and gathers the data to a single location in memory, or vice versa. A simple descriptor list allows data gathering. For example, data from a discontiguous list of buffers might be copied to a contiguous sequential array of buffers. The inverse is also possible when a sequential array of buffers is scattered to a discontiguous list of available buffers. See section 25.4.2 Descriptor Linked List.

Some DMAs which only have two descriptors implement scatter-gather by using one descriptor to modify the other descriptor. While it is possible to implement this same behavior using the LDMA, it is much more straight-forward to just use a simple descriptor list.

25.5 LDMA Source Selection Details

25.5.1 LDMA Source Selection Details

Table 25.3. LDMA Source Selection Details

SOURCESEL	Source Name	SIGSEL	Request Signal Name
0x1	LDMAXBAR	0x0	LDMAXBARPRSREQ0
		0x1	LDMAXBARPRSREQ1
0x2	TIMER0	0x0	TIMER0CC0
		0x1	TIMER0CC1
		0x2	TIMER0CC2
		0x3	TIMER0UFOF
0x3	TIMER1	0x0	TIMER1CC0
		0x1	TIMER1CC1
		0x2	TIMER1CC2
		0x3	TIMER1UFOF
0x4	I2C0	0x0	I2C0RXDATAV
		0x1	I2C0TXBL
0x5	I2C1	0x0	I2C1RXDATAV
		0x1	I2C1TXBL
0x9	IADC0	0x0	IADC0IADC_SCAN
		0x1	IADC0IADC_SINGLE
0xA	MSC	0x0	MSCWDATA
0xB	TIMER2	0x0	TIMER2CC0
		0x1	TIMER2CC1
		0x2	TIMER2CC2
		0x3	TIMER2UFOF
0xC	TIMER3	0x0	TIMER3CC0
		0x1	TIMER3CC1
		0x2	TIMER3CC2
		0x3	TIMER3UFOF
0xD	TIMER4	0x0	TIMER4CC0
		0x1	TIMER4CC1
		0x2	TIMER4CC2
		0x3	TIMER4UFOF
0xE	VDAC0	0x0	VDAC0CH0_REQ
		0x1	VDAC0CH1_REQ
0xF	EUSART0	0x0	EUSART0RXFL
		0x1	EUSART0TXFL

SOURCESEL	Source Name	SIGSEL	Request Signal Name
0x10	EUSART1	0x0	EUSART1RXFL
		0x1	EUSART1TXFL
0x11	EUSART2	0x0	EUSART2RXFL
		0x1	EUSART2TXFL
0x12	TIMER5	0x0	TIMER5CC0
		0x1	TIMER5CC1
		0x2	TIMER5CC2
		0x3	TIMER5UFOF
0x13	TIMER6	0x0	TIMER6CC0
		0x1	TIMER6CC1
		0x2	TIMER6CC2
		0x3	TIMER6UFOF
0x14	TIMER7	0x0	TIMER7CC0
		0x1	TIMER7CC1
		0x2	TIMER7CC2
		0x3	TIMER7UFOF
0x15	EUSART3	0x0	EUSART3RXFL
		0x1	EUSART3TXFL
0x16	EUSART4	0x0	EUSART4RXFL
		0x1	EUSART4TXFL
0x17	LESENSE	0x0	LESENSEFIFO

25.6 LDMA Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	LDMA_IPVERSION	R	IP Version
0x004	LDMA_EN	RW ENABLE	Module Enable Disable Register
0x008	LDMA_SWRST	RW SWRST	Software Reset Register
0x00C	LDMA_CTRL	RW	Control Register
0x010	LDMA_STATUS	RH	Status Register
0x014	LDMA_SYNCSWSET	W	Sync Trig Sw Set Register
0x018	LDMA_SYNCSWCLR	W	Sync Trig Sw Clear Register
0x01C	LDMA_SYNCHWEN	RW	Sync HW Trigger Enable Register
0x020	LDMA_SYNCHWSEL	RW	Sync HW Trigger Selection Register
0x024	LDMA_SYNCSTATUS	RH	Sync Trigger Status Register
0x028	LDMA_CHEN	W	Channel Enable Register
0x02C	LDMA_CHDIS	W	Channel Disable Register
0x030	LDMA_CHSTATUS	RH	Channel Status Register
0x034	LDMA_CHBUSY	RH	Channel Busy Register
0x038	LDMA_CHDONE	RWH	Channel Linking Done Register
0x03C	LDMA_DBGHALT	RW	Channel Debug Halt Register
0x040	LDMA_SWREQ	W	Channel Software Transfer Request
0x044	LDMA_REQDIS	RW	Channel Request Disable Register
0x048	LDMA_REQPEND	RH	Channel Requests Pending Register
0x04C	LDMA_LINKLOAD	W	Channel Link Load Register
0x050	LDMA_REQCLEAR	W	Channel Request Clear Register
0x054	LDMA_IF	RWH INTFLAG	Interrupt Flag Register
0x058	LDMA_IEN	RW	Done Interrupt Enable Register
0x060	LDMA_CHx_CFG	RW	Configuration
0x064	LDMA_CHx_LOOP	RWH	Loop Counter
0x068	LDMA_CHx_CTRL	RWH	Control
0x06C	LDMA_CHx_SRC	RWH	Source Address
0x070	LDMA_CHx_DST	RWH	Destination Address
0x074	LDMA_CHx_LINK	RWH	Link Address
0x078	LDMA_CHx_XCTRL	RWH	Extended Control
0x080	LDMA_CHx_ILSRC	RWH	Interleaving Source Address
0x1000	LDMA_IPVERSION_SET	R	IP Version
0x1004	LDMA_EN_SET	RW ENABLE	Module Enable Disable Register
0x1008	LDMA_SWRST_SET	RW SWRST	Software Reset Register
0x100C	LDMA_CTRL_SET	RW	Control Register

Offset	Name	Type	Description
0x1010	LDMA_STATUS_SET	RH	Status Register
0x1014	LDMA_SYNCSWSET_SET	W	Sync Trig Sw Set Register
0x1018	LDMA_SYNCSWCLR_SET	W	Sync Trig Sw Clear Register
0x101C	LDMA_SYNCHWEN_SET	RW	Sync HW Trigger Enable Register
0x1020	LDMA_SYNCHWSEL_SET	RW	Sync HW Trigger Selection Register
0x1024	LDMA_SYNCSTATUS_SET	RH	Sync Trigger Status Register
0x1028	LDMA_CHEN_SET	W	Channel Enable Register
0x102C	LDMA_CHDIS_SET	W	Channel Disable Register
0x1030	LDMA_CHSTATUS_SET	RH	Channel Status Register
0x1034	LDMA_CHBUSY_SET	RH	Channel Busy Register
0x1038	LDMA_CHDONE_SET	RWH	Channel Linking Done Register
0x103C	LDMA_DBGHALT_SET	RW	Channel Debug Halt Register
0x1040	LDMA_SWREQ_SET	W	Channel Software Transfer Request
0x1044	LDMA_REQDIS_SET	RW	Channel Request Disable Register
0x1048	LDMA_REQPEND_SET	RH	Channel Requests Pending Register
0x104C	LDMA_LINKLOAD_SET	W	Channel Link Load Register
0x1050	LDMA_REQCLEAR_SET	W	Channel Request Clear Register
0x1054	LDMA_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x1058	LDMA_IEN_SET	RW	Done Interrupt Enable Register
0x1060	LDMA_CHx_CFG_SET	RW	Configuration
0x1064	LDMA_CHx_LOOP_SET	RWH	Loop Counter
0x1068	LDMA_CHx_CTRL_SET	RWH	Control
0x106C	LDMA_CHx_SRC_SET	RWH	Source Address
0x1070	LDMA_CHx_DST_SET	RWH	Destination Address
0x1074	LDMA_CHx_LINK_SET	RWH	Link Address
0x1078	LDMA_CHx_XCTRL_SET	RWH	Extended Control
0x1080	LDMA_CHx_ILSRC_SET	RWH	Interleaving Source Address
0x2000	LDMA_IPVERSION_CLR	R	IP Version
0x2004	LDMA_EN_CLR	RW ENABLE	Module Enable Disable Register
0x2008	LDMA_SWRST_CLR	RW SWRST	Software Reset Register
0x200C	LDMA_CTRL_CLR	RW	Control Register
0x2010	LDMA_STATUS_CLR	RH	Status Register
0x2014	LDMA_SYNCSWSET_CLR	W	Sync Trig Sw Set Register
0x2018	LDMA_SYNCSWCLR_CLR	W	Sync Trig Sw Clear Register
0x201C	LDMA_SYNCHWEN_CLR	RW	Sync HW Trigger Enable Register
0x2020	LDMA_SYNCHWSEL_CLR	RW	Sync HW Trigger Selection Register
0x2024	LDMA_SYNCSTATUS_CLR	RH	Sync Trigger Status Register

Offset	Name	Type	Description
0x2028	LDMA_CHEN_CLR	W	Channel Enable Register
0x202C	LDMA_CHDIS_CLR	W	Channel Disable Register
0x2030	LDMA_CHSTATUS_CLR	RH	Channel Status Register
0x2034	LDMA_CHBUSY_CLR	RH	Channel Busy Register
0x2038	LDMA_CHDONE_CLR	RWH	Channel Linking Done Register
0x203C	LDMA_DBGHALT_CLR	RW	Channel Debug Halt Register
0x2040	LDMA_SWREQ_CLR	W	Channel Software Transfer Request
0x2044	LDMA_REQDIS_CLR	RW	Channel Request Disable Register
0x2048	LDMA_REQPEND_CLR	RH	Channel Requests Pending Register
0x204C	LDMA_LINKLOAD_CLR	W	Channel Link Load Register
0x2050	LDMA_REQCLEAR_CLR	W	Channel Request Clear Register
0x2054	LDMA_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x2058	LDMA_IEN_CLR	RW	Done Interrupt Enable Register
0x2060	LDMA_CHx_CFG_CLR	RW	Configuration
0x2064	LDMA_CHx_LOOP_CLR	RWH	Loop Counter
0x2068	LDMA_CHx_CTRL_CLR	RWH	Control
0x206C	LDMA_CHx_SRC_CLR	RWH	Source Address
0x2070	LDMA_CHx_DST_CLR	RWH	Destination Address
0x2074	LDMA_CHx_LINK_CLR	RWH	Link Address
0x2078	LDMA_CHx_XCTRL_CLR	RWH	Extended Control
0x2080	LDMA_CHx_ILSRC_CLR	RWH	Interleaving Source Address
0x3000	LDMA_IPVERSION_TGL	R	IP Version
0x3004	LDMA_EN_TGL	RW ENABLE	Module Enable Disable Register
0x3008	LDMA_SWRST_TGL	RW SWRST	Software Reset Register
0x300C	LDMA_CTRL_TGL	RW	Control Register
0x3010	LDMA_STATUS_TGL	RH	Status Register
0x3014	LDMA_SYNCSWSET_TGL	W	Sync Trig Sw Set Register
0x3018	LDMA_SYNCSWCLR_TGL	W	Sync Trig Sw Clear Register
0x301C	LDMA_SYNCHWEN_TGL	RW	Sync HW Trigger Enable Register
0x3020	LDMA_SYNCHWSEL_TGL	RW	Sync HW Trigger Selection Register
0x3024	LDMA_SYNCSTATUS_TGL	RH	Sync Trigger Status Register
0x3028	LDMA_CHEN_TGL	W	Channel Enable Register
0x302C	LDMA_CHDIS_TGL	W	Channel Disable Register
0x3030	LDMA_CHSTATUS_TGL	RH	Channel Status Register
0x3034	LDMA_CHBUSY_TGL	RH	Channel Busy Register
0x3038	LDMA_CHDONE_TGL	RWH	Channel Linking Done Register
0x303C	LDMA_DBGHALT_TGL	RW	Channel Debug Halt Register

Offset	Name	Type	Description
0x3040	LDMA_SWREQ_TGL	W	Channel Software Transfer Request
0x3044	LDMA_REQDIS_TGL	RW	Channel Request Disable Register
0x3048	LDMA_REQPEND_TGL	RH	Channel Requests Pending Register
0x304C	LDMA_LINKLOAD_TGL	W	Channel Link Load Register
0x3050	LDMA_REQCLEAR_TGL	W	Channel Request Clear Register
0x3054	LDMA_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x3058	LDMA_IEN_TGL	RW	Done Interrupt Enable Register
0x3060	LDMA_CHx_CFG_TGL	RW	Configuration
0x3064	LDMA_CHx_LOOP_TGL	RWH	Loop Counter
0x3068	LDMA_CHx_CTRL_TGL	RWH	Control
0x306C	LDMA_CHx_SRC_TGL	RWH	Source Address
0x3070	LDMA_CHx_DST_TGL	RWH	Destination Address
0x3074	LDMA_CHx_LINK_TGL	RWH	Link Address
0x3078	LDMA_CHx_XCTRL_TGL	RWH	Extended Control
0x3080	LDMA_CHx_ILSRC_TGL	RWH	Interleaving Source Address

25.7 LDMA Register Description

25.7.1 LDMA_IPVERSION - IP Version

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x1																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x1	R	**IPVERSION**
	The read only IPVERSION field gives the version for this module. There may be minor software changes required for modules with different values of IPVERSION.			

25.7.2 LDMA_EN - Module Enable Disable Register

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	RW
Name																															DISABLING	EN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DISABLING	0x0	R	**Disablement busy status**
	When EN is cleared, DISABLING status is set immediately, and cleared when disablement finishes. Disablement resets peripheral cores and not APB registers except hardware updated registers such as INTFLAGs and FIFO			
0	EN	0x0	RW	**Module Enable**
	The ENABLE bit enables the module. Software should write to CONFIG type registers before setting the ENABLE bit. Software should write to SYNC type registers only after setting the ENABLE bit.			

25.7.3 LDMA_SWRST - Software Reset Register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	W
Name																															RESETTING	SWRST

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	RESETTING	0x0	R	**Software Reset Busy Status**
	When SWRST command is issued, resetting logic sets RESETTING status immediately, and later it is cleared when reset process finishes			
0	SWRST	0x0	W	**Software Reset Command**
	A software reset command field resets the module back to the initial condition, similar to a power on reset condition			

25.7.4 LDMA_CTRL - Control Register

Offset	Bit Position																															
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset			0x1E																													
Access			RW																													
Name			NUMFIXED																													

Bit	Name	Reset	Access	Description
31:30	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
29:24	NUMFIXED	0x1E	RW	**Number of Fixed Priority Channels** This field defines the number of Fixed Priority Arbitration channels. Channels CH0 though CH(n-1) are fixed, and channels CH(n) through CH<max> are round robin, where n is the field value. The reset value will give all fixed channels.
23:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

25.7.5 LDMA_STATUS - Status Register

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset				0x10																	0x0					0xF					0x0	0x0
Access				R																	R					R					R	R
Name				CHNUM																	CHERROR					CHGRANT					ANYREQ	ANYBUSY

Bit	Name	Reset	Access	Description
31:29	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
28:24	CHNUM	0x10	R	**Number of Channels** The value of CHNUM always reads the total number of channels present for this instance of the DMA controller module.
23:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:8	CHERROR	0x0	R	**Errant Channel Number** When the ERROR flag is set in the LDMA_IF register, the CHERROR field will indicate the most recent channel to have a transfer error.
7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:3	CHGRANT	0xF	R	**Granted Channel Number** The value of this field indicates the currently active channel or last active channel. Note that the reset value for this field is set to the last channel. This is done to give channel 0 the highest priority in the first round robin arbitration.
2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	ANYREQ	0x0	R	**Any DMA Channel Request Pending** The value of this bit will be TRUE (1) if any requests are pending
0	ANYBUSY	0x0	R	**Any DMA Channel Busy** The value of this bit will be TRUE (1) if one or more DMA channels are actively transferring data

25.7.6 LDMA_SYNCSWSET - Sync Trig Sw Set Register

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									W(nB)							
Name																									SYNCSWSET							

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	SYNCSWSET	0x0	W(nB)	**DMA SYNC Software Trigger Set**
	Sets the corresponding bit in the SYNCSTATUS.SYNCTRIG field to value 1.			

25.7.7 LDMA_SYNCSWCLR - Sync Trig Sw Clear Register

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									W(nB)							
Name																									SYNCSWCLR							

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	SYNCSWCLR	0x0	W(nB)	**DMA SYNC Software Trigger Clear**
	Clears the corresponding bit in the SYNCSTATUS.SYNCTRIG field to value 0.			

25.7.8 LDMA_SYNCHWEN - Sync HW Trigger Enable Register

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset									0x0																0x0							
Access									RW																RW							
Name									SYNCCLREN																SYNCSETEN							

Bit	Name	Reset	Access	Description
31:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:16	SYNCCLREN	0x0	RW	**Hardware Sync Trigger Clear Enable**
	Enables the corresponding bit in the SYNCSTATUS.SYNCTRIG field to be cleared by PRS channel 7-0, mapping to bits [23:16].			
15:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	SYNCSETEN	0x0	RW	**Hardware Sync Trigger Set Enable**
	Enables the corresponding bit in the SYNCSTATUS.SYNCTRIG field to be set by PRS channel 7-0, mapping to bits [7:0].			

25.7.9 LDMA_SYNCHWSEL - Sync HW Trigger Selection Register

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset												0x0																0x0				
Access												RW																RW				
Name												SYNCCLREDGE																SYNCSETEDGE				

Bit	Name	Reset	Access	Description
31:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:16	SYNCCLREDGE	0x0	RW	**Hardware Sync Trigger Clear Edge Select**

Select rising or falling edge detection on PRS to clear trigger.

Value	Mode	Description
0	RISE	Use rising edge detection
1	FALL	Use falling edge detection

Bit	Name	Reset	Access	Description
15:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	SYNCSETEDGE	0x0	RW	**Hardware Sync Trigger Set Edge Select**

Select rising or falling edge detection on PRS to set trigger.

Value	Mode	Description
0	RISE	Use rising edge detection
1	FALL	Use falling edge detection

25.7.10 LDMA_SYNCSTATUS - Sync Trigger Status Register

Offset	Bit Position																													
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									R							
Name																									SYNCTRIG							

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	SYNCTRIG	0x0	R	**sync trig status**
	Reflects the status of setting and clearing by software (SYNCSWSET/SYNCSWCLR), hardware (PRS), and loading SYNC structures. Setting a bit always takes prescedence over clearing.			

25.7.11 LDMA_CHEN - Channel Enable Register

Offset	Bit Position																													
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	W(nB)															
Name																	CHEN															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	CHEN	0x0	W(nB)	**Channel Enables**
	Setting one of these bits will enable the respective DMA channel, writing zeros has no effect			

25.7.12 LDMA_CHDIS - Channel Disable Register

Offset	Bit Position																															
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	W(nB)															
Name																	CHDIS															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	CHDIS	0x0	W(nB)	**DMA Channel disable**
	Setting one of these bits will disable respective DMA channel, writing zeros has no effect. If set while a transfer is in progress, the current transfer block will complete. The remaining blocks will pause until resumed later by setting corresponding CHEN bit.			

25.7.13 LDMA_CHSTATUS - Channel Status Register

Offset	Bit Position																															
0x030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	R															
Name																	CHSTATUS															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	CHSTATUS	0x0	R	**DMA Channel Status**
	Each bit represents the enabled status of the channel, channel n is enabled when bit n is 1 and disabled when bit n is 0.			

25.7.14 LDMA_CHBUSY - Channel Busy Register

Offset	Bit Position																													
0x034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									R							
Name																									BUSY							

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	BUSY	0x0	R	**Channels Busy** The bits of this field read 1 when the corresponding channel is busy. This bit will be set when the channel starts a transfer and cleared when the tranfer completes.

25.7.15 LDMA_CHDONE - Channel Linking Done Register

Offset	Bit Position																													
0x038	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name																	CHDONE15	CHDONE14	CHDONE13	CHDONE12	CHDONE11	CHDONE10	CHDONE9	CHDONE8	CHDONE7	CHDONE6	CHDONE5	CHDONE4	CHDONE3	CHDONE2	CHDONE1	CHDONE0

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15	CHDONE15	0x0	RW	**Channel Linking Done Status flag**
	Each DMA channel sets the corresponding bit in this register when the entire linked transfer is done and there is no more linking to do. The interrupt service routine should clear these bits. For non-link structures this will be set once the structure is done.			
14	CHDONE14	0x0	RW	**Channel Linking Done Status flag**
	Each DMA channel sets the corresponding bit in this register when the entire linked transfer is done and there is no more linking to do. The interrupt service routine should clear these bits. For non-link structures this will be set once the structure is done.			
13	CHDONE13	0x0	RW	**Channel Linking Done Status flag**
	Each DMA channel sets the corresponding bit in this register when the entire linked transfer is done and there is no more linking to do. The interrupt service routine should clear these bits. For non-link structures this will be set once the structure is done.			
12	CHDONE12	0x0	RW	**Channel Linking Done Status flag**
	Each DMA channel sets the corresponding bit in this register when the entire linked transfer is done and there is no more linking to do. The interrupt service routine should clear these bits. For non-link structures this will be set once the structure is done.			
11	CHDONE11	0x0	RW	**Channel Linking Done Status flag**
	Each DMA channel sets the corresponding bit in this register when the entire linked transfer is done and there is no more linking to do. The interrupt service routine should clear these bits. For non-link structures this will be set once the structure is done.			
10	CHDONE10	0x0	RW	**Channel Linking Done Status flag**
	Each DMA channel sets the corresponding bit in this register when the entire linked transfer is done and there is no more linking to do. The interrupt service routine should clear these bits. For non-link structures this will be set once the structure is done.			
9	CHDONE9	0x0	RW	**Channel Linking Done Status flag**
	Each DMA channel sets the corresponding bit in this register when the entire linked transfer is done and there is no more linking to do. The interrupt service routine should clear these bits. For non-link structures this will be set once the structure is done.			
8	CHDONE8	0x0	RW	**Channel Linking Done Status flag**
	Each DMA channel sets the corresponding bit in this register when the entire linked transfer is done and there is no more linking to do. The interrupt service routine should clear these bits. For non-link structures this will be set once the structure is done.			
7	CHDONE7	0x0	RW	**Channel Linking Done Status flag**

Bit	Name	Reset	Access	Description
	Each DMA channel sets the corresponding bit in this register when the entire linked transfer is done and there is no more linking to do. The interrupt service routine should clear these bits. For non-link structures this will be set once the structure is done.			
6	CHDONE6	0x0	RW	**Channel Linking Done Status flag**
	Each DMA channel sets the corresponding bit in this register when the entire linked transfer is done and there is no more linking to do. The interrupt service routine should clear these bits. For non-link structures this will be set once the structure is done.			
5	CHDONE5	0x0	RW	**Channel Linking Done Status flag**
	Each DMA channel sets the corresponding bit in this register when the entire linked transfer is done and there is no more linking to do. The interrupt service routine should clear these bits. For non-link structures this will be set once the structure is done.			
4	CHDONE4	0x0	RW	**Channel Linking Done Status flag**
	Each DMA channel sets the corresponding bit in this register when the entire linked transfer is done and there is no more linking to do. The interrupt service routine should clear these bits. For non-link structures this will be set once the structure is done.			
3	CHDONE3	0x0	RW	**Channel Linking Done Status flag**
	Each DMA channel sets the corresponding bit in this register when the entire linked transfer is done and there is no more linking to do. The interrupt service routine should clear these bits. For non-link structures this will be set once the structure is done.			
2	CHDONE2	0x0	RW	**Channel Linking Done Status flag**
	Each DMA channel sets the corresponding bit in this register when the entire linked transfer is done and there is no more linking to do. The interrupt service routine should clear these bits. For non-link structures this will be set once the structure is done.			
1	CHDONE1	0x0	RW	**Channel Linking Done Status flag**
	Each DMA channel sets the corresponding bit in this register when the entire linked transfer is done and there is no more linking to do. The interrupt service routine should clear these bits. For non-link structures this will be set once the structure is done.			
0	CHDONE0	0x0	RW	**Channel Linking Done Status flag**
	Each DMA channel sets the corresponding bit in this register when the entire linked transfer is done and there is no more linking to do. The interrupt service routine should clear these bits. For non-link structures this will be set once the structure is done.			

25.7.16 LDMA_DBGHALT - Channel Debug Halt Register

Offset	Bit Position																															
0x03C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	RW															
Name																	DBGHALT															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	DBGHALT	0x0	RW	**DMA Debug Halt**
	Setting one of these bits will mask the corresponding DMA channel's peripheral request when debugging and the CPU is halted. This may be useful for debugging DMA software.			

25.7.17 LDMA_SWREQ - Channel Software Transfer Request

Offset	Bit Position																															
0x040	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	W(nB)															
Name																	SWREQ															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	SWREQ	0x0	W(nB)	**Software Transfer Requests**
	Setting one of these bits will trigger a DMA transfer for the corresponding channel. Writing zeros has no effect.			

25.7.18 LDMA_REQDIS - Channel Request Disable Register

Offset	Bit Position																															
0x044	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	RW															
Name																	REQDIS															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	REQDIS	0x0	RW	**DMA Request Disables**
	Setting one of these bits will disable peripheral requests for the corresponding channel. When cleared any pending peripheral requests will be serviced.			

25.7.19 LDMA_REQPEND - Channel Requests Pending Register

Offset	Bit Position																															
0x048	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	R															
Name																	REQPEND															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	REQPEND	0x0	R	**DMA Requests Pending**
	When a DMA channel has a pending request, the corresponding REQPEND bit will read 1.			

25.7.20 LDMA_LINKLOAD - Channel Link Load Register

Offset	Bit Position																													
0x04C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									W(nB)							
Name																									LINKLOAD							

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LINKLOAD	0x0	W(nB)	**DMA Link Loads**
	Setting one of these bits will force the corresponding DMA channel to load the next DMA structure and enable the channel. This empowers software to step through a sequence of descriptors. When this bit is set, the current configuration of the channel is ignored.			

25.7.21 LDMA_REQCLEAR - Channel Request Clear Register

Offset	Bit Position																													
0x050	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									W(nB)							
Name																									REQCLEAR							

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	REQCLEAR	0x0	W(nB)	**DMA Request Clear**
	Setting one of these bits will clear any internally registered transfer requests for the corresponding channel.			

25.7.22 LDMA_IF - Interrupt Flag Register

Offset	Bit Position																													
0x054	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access	RW																RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name	ERROR																DONE15	DONE14	DONE13	DONE12	DONE11	DONE10	DONE9	DONE8	DONE7	DONE6	DONE5	DONE4	DONE3	DONE2	DONE1	DONE0

Bit	Name	Reset	Access	Description
31	ERROR	0x0	RW	**Error Flag**
	Set to 1 on an Error			
30:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15	DONE15	0x0	RW	**Done Interrupt Flag**
	This bit is set when the corresponding channel completes a transfer or sync operation if either its CTRL.DONESET bit is 1 or it is the last descriptor in the chain (i.e. it is not linking).			
14	DONE14	0x0	RW	**Done Interrupt Flag**
	This bit is set when the corresponding channel completes a transfer or sync operation if either its CTRL.DONESET bit is 1 or it is the last descriptor in the chain (i.e. it is not linking).			
13	DONE13	0x0	RW	**Done Interrupt Flag**
	This bit is set when the corresponding channel completes a transfer or sync operation if either its CTRL.DONESET bit is 1 or it is the last descriptor in the chain (i.e. it is not linking).			
12	DONE12	0x0	RW	**Done Interrupt Flag**
	This bit is set when the corresponding channel completes a transfer or sync operation if either its CTRL.DONESET bit is 1 or it is the last descriptor in the chain (i.e. it is not linking).			
11	DONE11	0x0	RW	**Done Interrupt Flag**
	This bit is set when the corresponding channel completes a transfer or sync operation if either its CTRL.DONESET bit is 1 or it is the last descriptor in the chain (i.e. it is not linking).			
10	DONE10	0x0	RW	**Done Interrupt Flag**
	This bit is set when the corresponding channel completes a transfer or sync operation if either its CTRL.DONESET bit is 1 or it is the last descriptor in the chain (i.e. it is not linking).			
9	DONE9	0x0	RW	**Done Interrupt Flag**
	This bit is set when the corresponding channel completes a transfer or sync operation if either its CTRL.DONESET bit is 1 or it is the last descriptor in the chain (i.e. it is not linking).			
8	DONE8	0x0	RW	**Done Interrupt Flag**
	This bit is set when the corresponding channel completes a transfer or sync operation if either its CTRL.DONESET bit is 1 or it is the last descriptor in the chain (i.e. it is not linking).			
7	DONE7	0x0	RW	**Done Interrupt Flag**
	This bit is set when the corresponding channel completes a transfer or sync operation if either its CTRL.DONESET bit is 1 or it is the last descriptor in the chain (i.e. it is not linking).			
6	DONE6	0x0	RW	**Done Interrupt Flag**

Bit	Name	Reset	Access	Description
	This bit is set when the corresponding channel completes a transfer or sync operation if either its CTRL.DONESET bit is 1 or it is the last descriptor in the chain (i.e. it is not linking).			
5	DONE5	0x0	RW	**Done Interrupt Flag**
	This bit is set when the corresponding channel completes a transfer or sync operation if either its CTRL.DONESET bit is 1 or it is the last descriptor in the chain (i.e. it is not linking).			
4	DONE4	0x0	RW	**Done Interrupt Flag**
	This bit is set when the corresponding channel completes a transfer or sync operation if either its CTRL.DONESET bit is 1 or it is the last descriptor in the chain (i.e. it is not linking).			
3	DONE3	0x0	RW	**Done Interrupt Flag**
	This bit is set when the corresponding channel completes a transfer or sync operation if either its CTRL.DONESET bit is 1 or it is the last descriptor in the chain (i.e. it is not linking).			
2	DONE2	0x0	RW	**Done Interrupt Flag**
	This bit is set when the corresponding channel completes a transfer or sync operation if either its CTRL.DONESET bit is 1 or it is the last descriptor in the chain (i.e. it is not linking).			
1	DONE1	0x0	RW	**Done Interrupt Flag**
	This bit is set when the corresponding channel completes a transfer or sync operation if either its CTRL.DONESET bit is 1 or it is the last descriptor in the chain (i.e. it is not linking).			
0	DONE0	0x0	RW	**Done Interrupt Flag**
	This bit is set when the corresponding channel completes a transfer or sync operation if either its CTRL.DONESET bit is 1 or it is the last descriptor in the chain (i.e. it is not linking).			

25.7.23 LDMA_IEN - Done Interrupt Enable Register

Offset	Bit Position																													
0x058	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access	RW																RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name	ERROR																DONE15	DONE14	DONE13	DONE12	DONE11	DONE10	DONE9	DONE8	DONE7	DONE6	DONE5	DONE4	DONE3	DONE2	DONE1	DONE0

Bit	Name	Reset	Access	Description
31	ERROR	0x0	RW	**Error Interrupt Enable**
	This is the bitfield to enable the AHB bus error interrupt			
30:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15	DONE15	0x0	RW	**Done Interrupt Enable**
	Enables done interrupts			
14	DONE14	0x0	RW	**Done Interrupt Enable**
	Enables done interrupts			
13	DONE13	0x0	RW	**Done Interrupt Enable**
	Enables done interrupts			
12	DONE12	0x0	RW	**Done Interrupt Enable**
	Enables done interrupts			
11	DONE11	0x0	RW	**Done Interrupt Enable**
	Enables done interrupts			
10	DONE10	0x0	RW	**Done Interrupt Enable**
	Enables done interrupts			
9	DONE9	0x0	RW	**Done Interrupt Enable**
	Enables done interrupts			
8	DONE8	0x0	RW	**Done Interrupt Enable**
	Enables done interrupts			
7	DONE7	0x0	RW	**Done Interrupt Enable**
	Enables done interrupts			
6	DONE6	0x0	RW	**Done Interrupt Enable**
	Enables done interrupts			
5	DONE5	0x0	RW	**Done Interrupt Enable**
	Enables done interrupts			
4	DONE4	0x0	RW	**Done Interrupt Enable**
	Enables done interrupts			
3	DONE3	0x0	RW	**Done Interrupt Enable**

Bit	Name	Reset	Access	Description
	Enables done interrupts			
2	DONE2	0x0	RW	**Done Interrupt Enable**
	Enables done interrupts			
1	DONE1	0x0	RW	**Done Interrupt Enable**
	Enables done interrupts			
0	DONE0	0x0	RW	**Done Interrupt Enable**
	Enables done interrupts			

25.7.24 LDMA_CHx_CFG - Configuration

Offset	Bit Position																															
0x060	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset								0x0	0x0	0x0	0x0	0x0			0x0																	
Access								RW	RW	RW	RW	RW			RW																	
Name								DSTBUSPORT	SRCBUSPORT	STRUCTBUSPORT	DSTINCSIGN	SRCINCSIGN			ARBSLOTS																	

Bit	Name	Reset	Access	Description
31:25	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
24	DSTBUSPORT	0x0	RW	**Destination Bus Port**
	Specifies the DST operation bus port			
	Value	Mode		Description
	0	AHBM0		
	1	AHBM1		
23	SRCBUSPORT	0x0	RW	**Source Bus Port**
	Specifies the SRC operation bus port			
	Value	Mode		Description
	0	AHBM0		
	1	AHBM1		
22	STRUCTBUSPORT	0x0	RW	**Structure Fetch Bus Port**
	Specifies the Structure Fetch operation bus port			
	Value	Mode		Description
	0	AHBM0		
	1	AHBM1		
21	DSTINCSIGN	0x0	RW	**Destination Address Increment Sign**
	0: Increment destination address, 1: Decrement destination address			
	Value	Mode		Description
	0	POSITIVE		Increment destination address
	1	NEGATIVE		Decrement destination address
20	SRCINCSIGN	0x0	RW	**Source Address Increment Sign**
	0: Increment source address, 1: Decrement source address			

Bit	Name	Reset	Access	Description
	Value	Mode		Description
	0	POSITIVE		Increment source address
	1	NEGATIVE		Decrement source address
19:18	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
17:16	ARBSLOTS	0x0	RW	**Arbitration Slot Number Select**
	For channels using round robin arbitration, this bit-field is used to select the number of slots in the round robin queue.			
	Value	Mode		Description
	0	ONE		One arbitration slot selected
	1	TWO		Two arbitration slots selected
	2	FOUR		Four arbitration slots selected
	3	EIGHT		Eight arbitration slots selected
15:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

25.7.25 LDMA_CHx_LOOP - Loop Counter

Offset	Bit Position																													
0x064	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									RW							
Name																									LOOPCNT							

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	LOOPCNT	0x0	RW	**Linked Structure Sequence Loop Counter**
	This bit-field specifies the number of repetitions when using looping descriptors. Software should write to LOOPCNT before using a looping descriptor.			

25.7.26 LDMA_CHx_CTRL - Control

Offset	Bit Position																															
0x068	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0	0x0		0x0		0x0		0x0	0x0	0x0	0x0	0x0				0x0	0x0											0x0	0x0	0x0	
Access	R	R	RW		RW		RW		RW	RW	RW	RW	RW				RW	RW											R	RW	RW	
Name	DSTMODE	SRCMODE	DSTINC		SIZE		SRCINC		IGNORESREQ	DECLOOPCNT	REQMODE	DONESET	BLOCKSIZE				BYTESWAP	XFERCNT											STRUCTREQ	EXTEND	STRUCTTYPE	

Bit	Name	Reset	Access	Description
31	DSTMODE	0x0	R	**Destination Addressing Mode**

This field specifies the destination addressing mode of linked descriptors. After loading a linked descriptor, reading this field will indicate the destination addressing mode of the linked descriptor. Note that the first descriptor always uses absolute addressing mode.

Value	Mode	Description
0	ABSOLUTE	The DSTADDR field of LDMA_CHx_DST contains the absolute address of the destination data.
1	RELATIVE	The DSTADDR field of LDMA_CHx_DST contains the relative offset of the destination data.

Bit	Name	Reset	Access	Description
30	SRCMODE	0x0	R	**Source Addressing Mode**

This field specifies the source addressing mode of linked descriptors. After loading a linked descriptor, reading this field will indicate the source addressing mode of the linked descriptor. Note that the first descriptor always uses absolute addressing mode.

Value	Mode	Description
0	ABSOLUTE	The SRCADDR field of LDMA_CHx_SRC contains the absolute address of the source data.
1	RELATIVE	The SRCADDR field of LDMA_CHx_SRC contains the relative offset of the source data.

Bit	Name	Reset	Access	Description
29:28	DSTINC	0x0	RW	**Destination Address Increment Size**

This bit-field specifies the stride or number of unit data addresses to increment the destination address after each unit of data is transferred. The unit data width is controlled by the SIZE bit-field and can be a byte, half-word or word.

Value	Mode	Description
0	ONE	Increment destination address by one unit data size after each write
1	TWO	Increment destination address by two unit data sizes after each write
2	FOUR	Increment destination address by four unit data sizes after each write
3	NONE	Do not increment the destination address. Writes are made to a fixed destination address, for example writing to a FIFO.

Bit	Name	Reset	Access	Description
27:26	SIZE	0x0	RW	**Unit Data Transfer Size**

This field specifies the size of data transferred.

Value	Mode	Description
0	BYTE	Each unit transfer is a byte
1	HALFWORD	Each unit transfer is a half-word
2	WORD	Each unit transfer is a word

25:24	SRCINC	0x0	RW	**Source Address Increment Size**

This bit-field specifies the stride or number of unit data addresses to increment the source address after each unit of data is transferred. The unit data width is controlled by the SIZE bit-field and can be a byte, half-word or word.

Value	Mode	Description
0	ONE	Increment source address by one unit data size after each read
1	TWO	Increment source address by two unit data sizes after each read
2	FOUR	Increment source address by four unit data sizes after each read
3	NONE	Do not increment the source address. In this mode reads are made from a fixed source address, for example reading FIFO.

23	IGNORESREQ	0x0	RW	**Ignore Sreq**

The channel arbiter will ignore single requests (SREQ) and only respond to multiple requests (REQ) when this bit is set.

22	DECLOOPCNT	0x0	RW	**Decrement Loop Count**

When using looping, setting this bit will decrement the LOOPCNT field in the LDMA_CHx_LOOP register after each descriptor execution.

21	REQMODE	0x0	RW	**DMA Request Transfer Mode Select**

Selects the DMA Request Transfer mode.

Value	Mode	Description
0	BLOCK	The LDMA transfers one BLOCKSIZE per transfer request.
1	ALL	One transfer request transfers all units as defined by the XFRCNT field.

20	DONESET	0x0	RW	**DMA Operation Done Interrupt Flag Set**

When enabled, the corresponding DONEIF bit will get set when descriptor processing is done (i.e. when transfer completes, next descriptor is linked or a syncmatch is hit in the case of SYNC transfers).

19:16	BLOCKSIZE	0x0	RW	**Block Transfer Size**

This bit-field controls the number of unit data transfers per arbitration cycle

Value	Mode	Description
0	UNIT1	1 unit transfer per arbitration
1	UNIT2	2 unit transfers per arbitration
2	UNIT3	3 unit transfers per arbitration
3	UNIT4	4 unit transfers per arbitration

Bit	Name	Reset	Access	Description
	4	UNIT6		6 unit transfers per arbitration
	5	UNIT8		8 unit transfers per arbitration
	6	UNIT12		12 unit transfers per arbitration
	7	UNIT16		16 unit transfers per arbitration
	8	UNIT24		24 unit transfers per arbitration
	9	UNIT32		32 unit transfers per arbitration
	10	UNIT64		64 unit transfers per arbitration
	11	UNIT128		128 unit transfers per arbitration
	12	UNIT256		256 unit transfers per arbitration
	13	UNIT512		512 unit transfers per arbitration
	14	UNIT1024		1024 unit transfers per arbitration
	15	ALL		Transfer all units as specified by the XFRCNT field
15	BYTESWAP	0x0	RW	**Endian Byte Swap**
	For word and half-word transfers, setting this bit will swap all bytes of each word or half-word.			
14:4	XFERCNT	0x0	RW	**DMA Unit Data Transfer Count**
	Specifies number of unit data (words, half-words, or bytes) to transfer, as determined by the SIZE field. The value written should be one less than the desired transfer count.			
3	STRUCTREQ	0x0	R	**Structure DMA Transfer Request**
	Structure Transfer Request			
2	EXTEND	0x0	RW	**Extend**
	Extend data structure			
1:0	STRUCTTYPE	0x0	RW	**DMA Structure Type**
	DMA Structure type			
	Value	Mode		Description
	0	TRANSFER		DMA transfer structure type selected.
	1	SYNCHRONIZE		Synchronization structure type selected.
	2	WRITE		Write immediate value structure type selected.

25.7.27 LDMA_CHx_SRC - Source Address

Offset	Bit Position																													
0x06C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	ADDR																															

Bit	Name	Reset	Access	Description
31:0	ADDR	0x0	RW	**Source Data Address**
	Writing to this register sets the source address. Reading from this register during a DMA transfer will indicate the next source read address. The value of this register is incremented or decremented with each source read.			

25.7.28 LDMA_CHx_DST - Destination Address

Offset	Bit Position																													
0x070	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	ADDR																															

Bit	Name	Reset	Access	Description
31:0	ADDR	0x0	RW	**Destination Data Address**
	Writing to this register sets the destination address. Reading from this register during a DMA transfer will indicate the next destination write address. This value of this register is incremented or decremented with each destination write.			

25.7.29 LDMA_CHx_LINK - Link Address

Offset	Bit Position																													
0x074	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																														0x0	0x0
Access	RW																														RW	R
Name	LINKADDR																														LINK	LINKMODE

Bit	Name	Reset	Access	Description
31:2	LINKADDR	0x0	RW	**Link Structure Address**
	To use linking, write the address of the the first linked descriptor to this register. When a linked descriptor is loaded, it may also be linked to another descriptor. Reading this register will reflect the address of the next linked descriptor.			
1	LINK	0x0	RW	**Link Next Structure**
	After completing the initial transfer, if this bit is set, the DMA will load the next linked descriptor. If the next linked descriptor also has this bit set, the DMA will load the next linked descriptor.			
0	LINKMODE	0x0	R	**Link Structure Addressing Mode**
	This field specifies the addressing mode of linked descriptors. After loading a linked descriptor, reading this field will indicate the addressing mode of the loaded linked descriptor. Note that the first descriptor always uses absolute addressing mode.			

Value	Mode	Description
0	ABSOLUTE	The LINKADDR field of LDMA_CHx_LINK contains the absolute address of the linked descriptor.
1	RELATIVE	The LINKADDR field of LDMA_CHx_LINK contains the relative offset of the linked descriptor.

25.7.30 LDMA_CHx_XCTRL - Extended Control

Offset	Bit Position																															
0x078	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0	0x0		0x0				
Access																									RW	RW		RW				
Name																									BUFFERABLE	ILMODE		DSTILEN				

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7	BUFFERABLE	0x0	RW	**Allow AHB buffering**
	Determines whether destination writes can be a bufferable AHB transaction			
6:5	ILMODE	0x0	RW	**Interleave Mode**
	Rules table interleaving mode			

Value	Mode	Description
0	ABSOLUTE	Address determined by value in rules. Size of WORD
1	RELATIVE16	Address determined by adding rules to DST. Size of HALF-WORD
2	RELATIVE8	Address determined by adding rules to DST. Size of BYTE

Bit	Name	Reset	Access	Description
4	DSTILEN	0x0	RW	**Destination Interleave**
	Enables destination interleaving feature			
3:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

25.7.31 LDMA_CHx_ILSRC - Interleaving Source Address

Offset	Bit Position																															
0x080	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																0x0																
Access																RW																
Name																ADDR																

Bit	Name	Reset	Access	Description
31:0	ADDR	0x0	RW	**Interleave Source Address**
	Base address for rules table in memory			

25.8 LDMAXBAR Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	LDMAXBAR_IPVERSION	R	IP Veersion ID
0x004	LDMAXBAR_CHx_REQSEL	RW	Channel Peripheral Request Select Reg...
0x1000	LDMAXBAR_IPVERSION_SET	R	IP Veersion ID
0x1004	LDMAXBAR_CHx_REQSEL_SET	RW	Channel Peripheral Request Select Reg...
0x2000	LDMAXBAR_IPVERSION_CLR	R	IP Veersion ID
0x2004	LDMAXBAR_CHx_REQSEL_CLR	RW	Channel Peripheral Request Select Reg...
0x3000	LDMAXBAR_IPVERSION_TGL	R	IP Veersion ID
0x3004	LDMAXBAR_CHx_REQSEL_TGL	RW	Channel Peripheral Request Select Reg...

25.9 LDMAXBAR Register Description

25.9.1 LDMAXBAR_IPVERSION - IP Veersion ID

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x4																															
Access	R																															
Name	IPVERSION																															

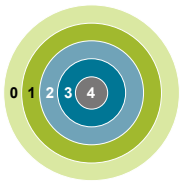
Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x4	R	**IP Version ID**
	ID indicating version of IP			

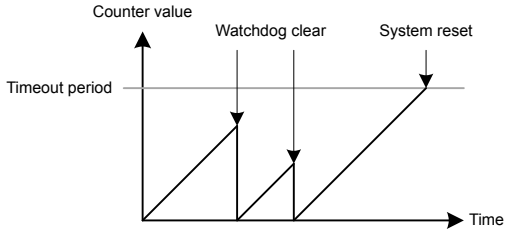
25.9.2 LDMAXBAR_CHx_REQSEL - Channel Peripheral Request Select Reg...

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset											0x0																		0x0		
Access											RW																		RW		
Name											SOURCESEL																		SIGSEL		

Bit	Name	Reset	Access	Description
31:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21:16	SOURCESEL	0x0	RW	**Source Select**
	Select input source to DMA channel.			
15:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	SIGSEL	0x0	RW	**Signal Select**
	Select input signal to DMA channel.			

26. WDOG - Watch Dog Timer





Quick Facts

What?

The WDOG (Watchdog Timer) resets the system in case of a fault condition, and can be enabled in all energy modes as long as the low frequency clock source is available.

Why?

If a software failure or external event renders the MCU unresponsive, a Watchdog timeout will reset the system to a known, safe state.

How?

An enabled Watchdog Timer implements a configurable timeout period. If the CPU fails to re-start the Watchdog Timer before it times out, a full system reset will be triggered. The Watchdog consumes insignificant power, and allows the device to remain safely in low energy modes for up to 256 seconds at a time.

26.1 Introduction

The purpose of the watchdog timer is to generate a reset in case of a system failure to increase application reliability. The failure can be caused by a variety of events, such as an ESD pulse or a software failure.

26.2 Features

- Clock input from selectable oscillators
  - Internal 32 kHz LFRCO oscillator
  - Internal 1 kHz ULFRCO oscillator
  - External 32.768 kHz LFXO XTAL oscillator
  - HCLK divided by 1024
- Configurable timeout period from 9 to 256k watchdog clock cycles
- Individual selection to keep running or freeze when entering EM1 Sleep, EM2 DeepSleep, or EM3 Stop
- Selection to keep running or freeze when entering debug mode
- Selection to block the CPU from entering Energy Mode 4
- Configurable warning interrupt at 25%, 50%, or 75% of the timeout period
- Configurable window interrupt at 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, 87.5% of the timeout period
- Timeout interrupt
- PRS as a watchdog clear
- Interrupt for the event where a PRS rising edge is absent before a software reset

26.3 Functional Description

The watchdog is enabled by setting the EN bit in WDOGn_EN. When enabled, the watchdog counts up to the period value configured through the PERSEL field in WDOGn_CFG. If the watchdog timer is not cleared to 0 (by writing a 1 to the CLEAR bit in WDOGn_CMD) before the period is reached, the chip is reset. If a timely clear command is issued, the timer starts counting up from 0 again. The watchdog can optionally be locked by writing anything other than UNLOCK code in WDOGn_LOCK. Once locked, it cannot be disabled or reconfigured by software.

Note: If the WDOG is configured to halt during EM1, EM2, or EM3 and EM1/EM2/EM3 is entered on the clock cycle before the specified timeout, a timeout event will occur upon the EM1/EM2/EM3 wake event.

When the EN bit in WDOGn_EN is cleared to 0, the watchdog counter is reset. Any pending interrupt flags will remain active until cleared.

26.3.1 Clock Source

Four clock sources are available for use with the watchdog, through the CLKSEL field in CMU_WDOGn_CFG. The selected oscillator source automatically starts when the watchdog is enabled. To prevent accidental change of the clock selection, CMU_WDOGLOCK can be written anything other than UNLOCK code. Also, respective oscillator has locks to prevent accidental disabling of oscillators. The PERSEL field in WDOGn_CFG is used to divide the selected watchdog clock, and the timeout for the watchdog timer can be calculated with the formula:

$$T_{TIMEOUT} = [2^{(PERSEL+3)} + 1] / f$$

where f is the frequency of the selected clock.

Users must clear EM2RUN and EM3RUN when the selected clock source is HCLKDIV1024.

26.3.2 Debug Functionality

The watchdog timer can either keep running or be frozen when the device is halted by a debugger. This configuration is done through the DEBUGRUN bit in WDOGn_CFG. When code execution is resumed, the watchdog will continue counting where it left off.

26.3.3 Energy Mode Handling

The watchdog timer can be configured to either keep on running or freeze when entering EM1 Sleep, EM2 DeepSleep, or EM3 Stop. The configuration is done individually for each energy mode in the EM1RUN, EM2RUN, and EM3RUN bits in WDOGn_CFG. When the watchdog has been frozen and is re-entering an energy mode where it is running, the watchdog timer will continue counting where it left off. The watchdog does not run in EM4. If EM4BLOCK in WDOGn_CFG is set, the CPU will be prevented from entering EM4 by software request.

26.3.4 Warning Interrupt

The watchdog implements a warning interrupt which can be configured to occur at approximately 25%, 50%, or 75% of the timeout period through the WARNSEL field of the WDOGn_CFG register. This interrupt can be used to wake up the cpu for clearing the watchdog. The warning point for the watchdog timer can be calculated with the formula:

$$T_{WARNING} = [2^{(PERSEL+3)} +1]*WARNSEL / 4 / f$$

where f is the frequency of the selected clock.

When the watchdog is enabled, it is recommended to clear the watchdog before changing WARNSEL.

26.3.5 Window Interrupt

This interrupt occurs when the watchdog is cleared below a certain threshold. This threshold is given by the formula:

$$T_{WINDOW} = [2^{(PERSEL+3)} + 1]*WARNSEL / 8 / f$$

where f is the frequency of the selected clock.

This value will be approximately 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, or 87.5% of the timeout value based on the WINSEL field of the WDOGn_CFG. Figure 26.2 WDOG Warning, Window, and Timeout on page 1062 illustrates the warning, the window, and the timeout interrupts. Also, it shows where the PRS rising edge needs to happen. The PRS edge detection feature is discussed later.

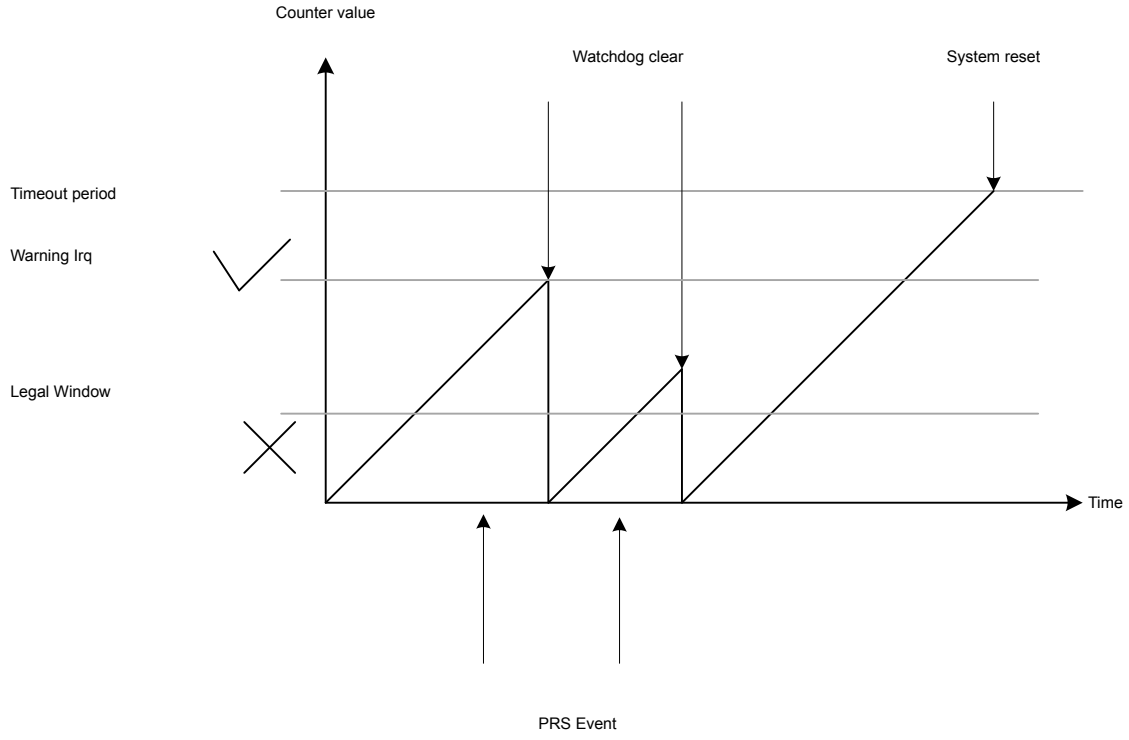


Figure 26.2. WDOG Warning, Window, and Timeout

26.3.6 PRS as Watchdog Clear

A PRS channel (selected by register PRS_CONSUMER_WDOGn_SRC0) can be used to clear the watchdog counter. To enable this feature, CLRSRC must be set to 1. Figure 26.2 PRS Clearing WDOG on page 1063 shows how the PRS channel takes over the WDOG clear function. Clearing the WDOG with the PRS is mutually exclusive of clearing the WDT by software.

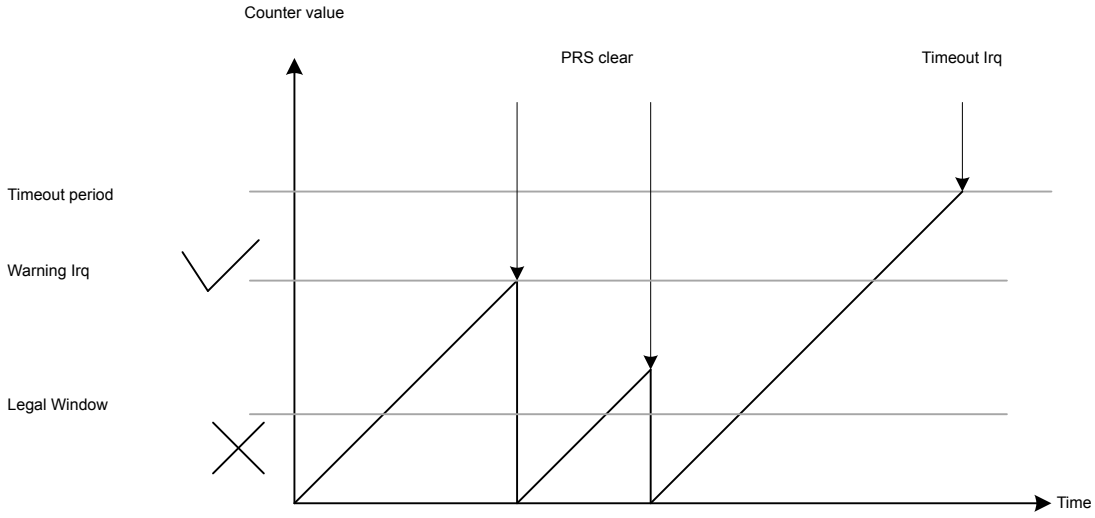


Figure 26.2. PRS Clearing WDOG

26.3.7 PRS Rising Edge Monitoring

PRS channels can be used to monitor multiple processes. The first and second channel are selected by PRS_CONSUMER_WDOGn_SRC0 and PRS_CONSUMER_WDOGn_SRC1, respectively. If enabled, every time the watch dog timer is cleared the PRS channels are checked and any channel which has not seen an event can trigger an interrupt.

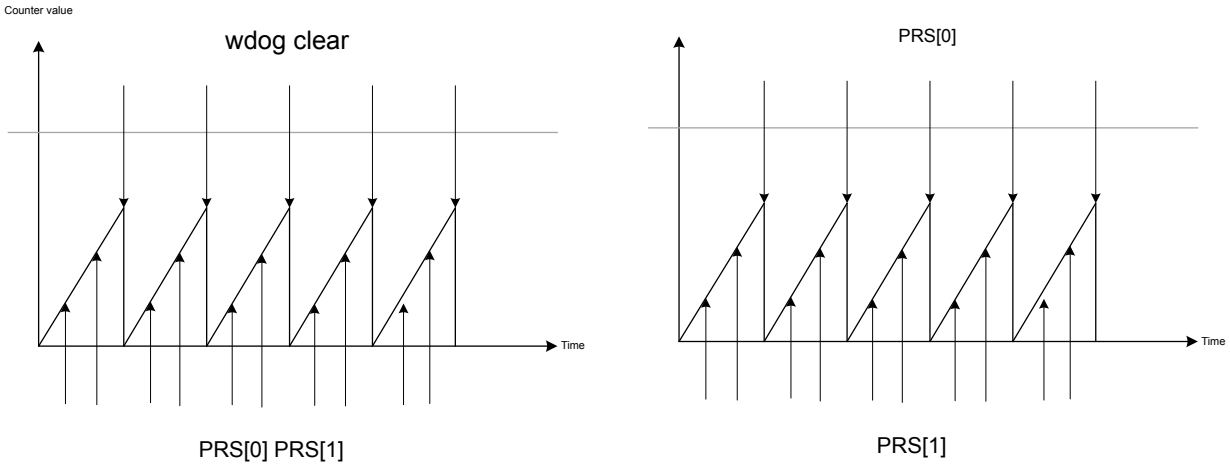


Figure 26.3. PRS Edge Monitoring in WDOG

26.4 WDOG Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	WDOG_IPVERSION	R	IP Version Register
0x004	WDOG_EN	RW ENABLE	Enable Register
0x008	WDOG_CFG	RW CONFIG	Configuration Register
0x00C	WDOG_CMD	W LFSYNC	Command Register
0x014	WDOG_STATUS	RH	Status Register
0x018	WDOG_IF	RWH INTFLAG	Interrupt Flag Register
0x01C	WDOG_IEN	RW	Interrupt Enable Register
0x020	WDOG_LOCK	W	Lock Register
0x024	WDOG_SYNCBUSY	RH	Synchronization Busy Register
0x1000	WDOG_IPVERSION_SET	R	IP Version Register
0x1004	WDOG_EN_SET	RW ENABLE	Enable Register
0x1008	WDOG_CFG_SET	RW CONFIG	Configuration Register
0x100C	WDOG_CMD_SET	W LFSYNC	Command Register
0x1014	WDOG_STATUS_SET	RH	Status Register
0x1018	WDOG_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x101C	WDOG_IEN_SET	RW	Interrupt Enable Register
0x1020	WDOG_LOCK_SET	W	Lock Register
0x1024	WDOG_SYNCBUSY_SET	RH	Synchronization Busy Register
0x2000	WDOG_IPVERSION_CLR	R	IP Version Register
0x2004	WDOG_EN_CLR	RW ENABLE	Enable Register
0x2008	WDOG_CFG_CLR	RW CONFIG	Configuration Register
0x200C	WDOG_CMD_CLR	W LFSYNC	Command Register
0x2014	WDOG_STATUS_CLR	RH	Status Register
0x2018	WDOG_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x201C	WDOG_IEN_CLR	RW	Interrupt Enable Register
0x2020	WDOG_LOCK_CLR	W	Lock Register
0x2024	WDOG_SYNCBUSY_CLR	RH	Synchronization Busy Register
0x3000	WDOG_IPVERSION_TGL	R	IP Version Register
0x3004	WDOG_EN_TGL	RW ENABLE	Enable Register
0x3008	WDOG_CFG_TGL	RW CONFIG	Configuration Register
0x300C	WDOG_CMD_TGL	W LFSYNC	Command Register
0x3014	WDOG_STATUS_TGL	RH	Status Register
0x3018	WDOG_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x301C	WDOG_IEN_TGL	RW	Interrupt Enable Register
0x3020	WDOG_LOCK_TGL	W	Lock Register

Offset	Name	Type	Description
0x3024	WDOG_SYNCBUSY_TGL	RH	Synchronization Busy Register

26.5 WDOG Register Description

26.5.1 WDOG_IPVERSION - IP Version Register

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x1																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x1	R	**IP Version**
	The read only IPVERSION field gives the version for this module. There may be minor software changes required for modules with different values of IPVERSION.			

26.5.2 WDOG_EN - Enable Register

Offset	Bit Position																															
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	RW
Name																															DISABLING	EN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DISABLING	0x0	R	**Disabling busy status**
	When EN is cleared, DISABLING status is set immediately, and cleared when disablement finishes. Disablement resets peripheral cores and not APB registers except hardware updated registers such as INTFLAGs and FIFO			
0	EN	0x0	RW	**Module Enable**
	The ENABLE bit enables the module. Software should write to CONFIG type registers before setting the ENABLE bit. Software should write to SYNC type registers only after setting the ENABLE bit.			

26.5.3 WDOG_CFG - Configuration Register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset		0x0					0x0						0xF									0x0	0x0	0x0			0x0	0x0	0x0	0x0	0x0	0x0
Access		RW					RW						RW									RW	RW	RW			RW	RW	RW	RW	RW	RW
Name		WINSEL					WARNSEL						PERSEL									PRS1MISSRSTEN	PRS0MISSRSTEN	WDOGRSTDIS			DEBUGRUN	EM4BLOCK	EM3RUN	EM2RUN	EM1RUN	CLRSRC

Bit	Name	Reset	Access	Description
31	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
30:28	WINSEL	0x0	RW	**WDOG Illegal Window Select**

Select WDOG illegal limit.

Value	Mode	Description
0	DIS	Disabled.
1	SEL1	Window timeout is 12.5% of the Timeout.
2	SEL2	Window timeout is 25% of the Timeout.
3	SEL3	Window timeout is 37.5% of the Timeout.
4	SEL4	Window timeout is 50% of the Timeout.
5	SEL5	Window timeout is 62.5% of the Timeout.
6	SEL6	Window timeout is 75.5% of the Timeout.
7	SEL7	Window timeout is 87.5% of the Timeout.

27:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25:24	WARNSEL	0x0	RW	**WDOG Warning Period Select**

Select WDOG warning timeout period.

Value	Mode	Description
0	DIS	Disable
1	SEL1	Warning timeout is 25% of the Timeout.
2	SEL2	Warning timeout is 50% of the Timeout.
3	SEL3	Warning timeout is 75% of the Timeout.

23:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:16	PERSEL	0xF	RW	**WDOG Timeout Period Select**

Select WDOG timeout period.

Bit	Name	Reset	Access	Description
	Value	Mode		Description
	0	SEL0		Timeout period of 9 wdog cycles
	1	SEL1		Timeout period of 17 wdog cycles
	2	SEL2		Timeout period of 33 wdog cycles
	3	SEL3		Timeout period of 65 wdog cycles
	4	SEL4		Timeout period of 129 wdog cycles
	5	SEL5		Timeout period of 257 wdog cycles
	6	SEL6		Timeout period of 513 wdog cycles
	7	SEL7		Timeout period of 1k wdog cycles
	8	SEL8		Timeout period of 2k wdog cycles
	9	SEL9		Timeout period of 4k wdog cycles
	10	SEL10		Timeout period of 8k wdog cycles
	11	SEL11		Timeout period of 16k wdog cycles
	12	SEL12		Timeout period of 32k wdog cycles
	13	SEL13		Timeout period of 64k wdog cycles
	14	SEL14		Timeout period of 128k wdog cycles
	15	SEL15		Timeout period of 256k wdog cycles
15:11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10	PRS1MISSRSTEN	0x0	RW	**PRS Src1 Missing Event WDOG Reset**
	When set, a PRS Source 1 missing event will trigger a WDOG reset.			
9	PRS0MISSRSTEN	0x0	RW	**PRS Src0 Missing Event WDOG Reset**
	When set, a PRS Source 0 missing event will trigger a WDOG reset.			
8	WDOGRSTDIS	0x0	RW	**WDOG Reset Disable**
	Disable WDOG reset output.			
	Value	Mode		Description
	0	EN		A timeout will cause a WDOG reset
	1	DIS		A timeout will not cause a WDOG reset
7:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	DEBUGRUN	0x0	RW	**Debug Mode Run**
	Set to keep WDOG running in debug mode.			
	Value	Mode		Description
	0	DISABLE		WDOG timer is frozen in debug mode
	1	ENABLE		WDOG timer is running in debug mode
4	EM4BLOCK	0x0	RW	**EM4 Block**

Bit	Name	Reset	Access	Description
	Set to disallow EM4 entry by software.			
	Value	Mode		Description
	0	DISABLE		EM4 can be entered by software. See EMU for detailed description.
	1	ENABLE		EM4 cannot be entered by software.
3	EM3RUN	0x0	RW	**EM3 Run**
	Set to keep WDOG running in EM3.			
	Value	Mode		Description
	0	DISABLE		WDOG timer is frozen in EM3.
	1	ENABLE		WDOG timer is running in EM3.
2	EM2RUN	0x0	RW	**EM2 Run**
	Set to keep WDOG running in EM2.			
	Value	Mode		Description
	0	DISABLE		WDOG timer is frozen in EM2.
	1	ENABLE		WDOG timer is running in EM2.
1	EM1RUN	0x0	RW	**EM1 Run**
	Set to keep WDOG running in EM1.			
	Value	Mode		Description
	0	DISABLE		WDOG timer is frozen in EM1.
	1	ENABLE		WDOG timer is running in EM1.
0	CLRSRC	0x0	RW	**WDOG Clear Source**
	Select WDOG clear source.			
	Value	Mode		Description
	0	SW		A write to the clear bit will clear the WDOG counter
	1	PRSSRC0		A rising edge on the PRS Source 0 will clear the WDOG counter

26.5.4 WDOG_CMD - Command Register

Offset	Bit Position																														
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																W(nB)
Name																																CLEAR

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	CLEAR	0x0	W(nB)	**WDOG Timer Clear**

Clear WDOG timer. The bit must be written 4 WDOG cycles before the timeout.

Value	Mode	Description
0	UNCHANGED	WDOG timer is unchanged.
1	CLEARED	WDOG timer is cleared to 0.

26.5.5 WDOG_STATUS - Status Register

Offset	Bit Position																														
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	LOCK																															

Bit	Name	Reset	Access	Description
31	LOCK	0x0	R	**WDOG Configuration Lock Status**

Status of all lockable WDOG registers.

Value	Mode	Description
0	UNLOCKED	All WDOG lockable registers are unlocked.
1	LOCKED	All WDOG lockable registers are locked.

30:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*

26.5.6 WDOG_IF - Interrupt Flag Register

Offset	Bit Position																														
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												RW	RW	RW	RW	RW
Name																												PEM1	PEM0	WIN	WARN	TOUT

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	PEM1	0x0	RW	**PRS Src1 Event Missing Interrupt Flag**
	Set when a WDOG clear happens before a prs event has been detected on PRS Source one.			
3	PEM0	0x0	RW	**PRS Src0 Event Missing Interrupt Flag**
	Set when a WDOG clear happens before a prs event has been detected on PRS Source zero.			
2	WIN	0x0	RW	**WDOG Window Interrupt Flag**
	Set when a WDOG clear happens below the window limit value.			
1	WARN	0x0	RW	**WDOG Warning Timeout Interrupt Flag**
	Set when a WDOG warning timeout has occurred.			
0	TOUT	0x0	RW	**WDOG Timeout Interrupt Flag**
	Set when a WDOG timeout has occurred.			

26.5.7 WDOG_IEN - Interrupt Enable Register

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												RW	RW	RW	RW	RW
Name																												PEM1	PEM0	WIN	WARN	TOUT

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	PEM1	0x0	RW	**PRS Src1 Event Missing Interrupt Enable**
	Enable/disable the PEM1 interrupt.			
3	PEM0	0x0	RW	**PRS Src0 Event Missing Interrupt Enable**
	Enable/disable the PEM0 interrupt.			
2	WIN	0x0	RW	**WDOG Window Interrupt Enable**
	Enable/disable the WIN interrupt.			
1	WARN	0x0	RW	**WDOG Warning Timeout Interrupt Enable**
	Enable/disable the WARN interrupt.			
0	TOUT	0x0	RW	**WDOG Timeout Interrupt Enable**
	Enable/disable the TOUT interrupt.			

26.5.8 WDOG_LOCK - Lock Register

Offset	Bit Position																															
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0xABE8															
Access																	W															
Name																	LOCKKEY															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	LOCKKEY	0xABE8	W	**WDOG Configuration Lock**

Write any other value than the unlock code to lock WDOG_EN, WDOD_CFG registers from editing. Write the unlock code to unlock.

Value	Mode	Description
0	LOCK	Lock WDOG lockable registers
44008	UNLOCK	Unlock WDOG lockable registers

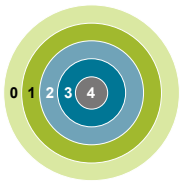
26.5.9 WDOG_SYNCBUSY - Synchronization Busy Register

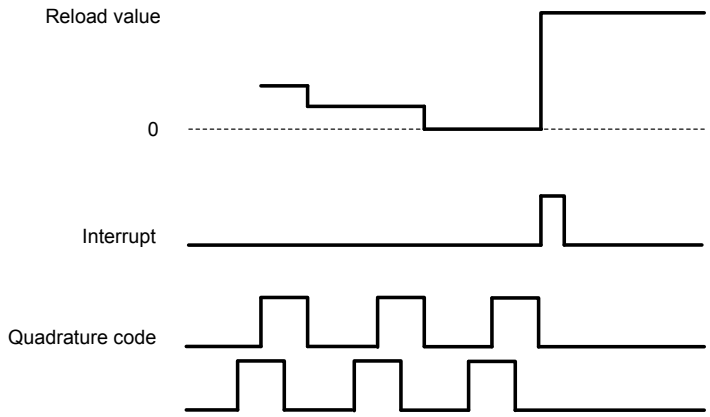
Offset	Bit Position																															
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																R
Name																																CMD

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	CMD	0x0	R	**Sync Busy for Cmd Register**

CMD bitfield sync is busy when set.

27. PCNT - Pulse Counter







Quick Facts

What?

The Pulse Counter (PCNT) decodes incoming pulses. The module has a quadrature mode which may be used to decode the speed and direction of a mechanical shaft. PCNT can operate in EM0 down to EM3.

Why?

The PCNT generates an interrupt after a specific number of pulses (or rotations), eliminating the need for timing or I/O interrupts and CPU processing to measure pulse widths, etc.

How?

PCNT uses the EM23GRPACLK or may be externally clocked from a pin. The module incorporates a 16-bit up/down-counter to keep track of incoming pulses or rotations.

27.1 Introduction

The Pulse Counter (PCNT) can be used for counting incoming pulses on a single input or to decode quadrature encoded inputs in EM0 down to EM3. It can run from the internal EM23GRPACLK clock source while counting pulses on the PCNTn_S0IN pin. Alternatively, the PCNTn_S0IN pin or a PRS signal may be used as an external clock source that runs the PCNT counter and register access.

27.2 Features

- 16-bit counter with reload register
- Auxiliary counter for counting a single direction
- Single input oversampling up/down counter mode
- Externally clocked single input pulse up/down counter mode
- Quadrature decoder modes
  - Externally clocked quadrature decoder 1X mode
  - Oversampling quadrature decoder 1X, 2X and 4X modes
- Interrupt on counter underflow and overflow
- Interrupt when a direction change is detected (quadrature decoder mode only)
- Optional pulse width filter
- Optional input inversion/edge detect select
- Optional inputs from PRS

27.3 Functional Description

An overview of the PCNT module is shown in Figure 27.1 PCNT Overview on page 1074.

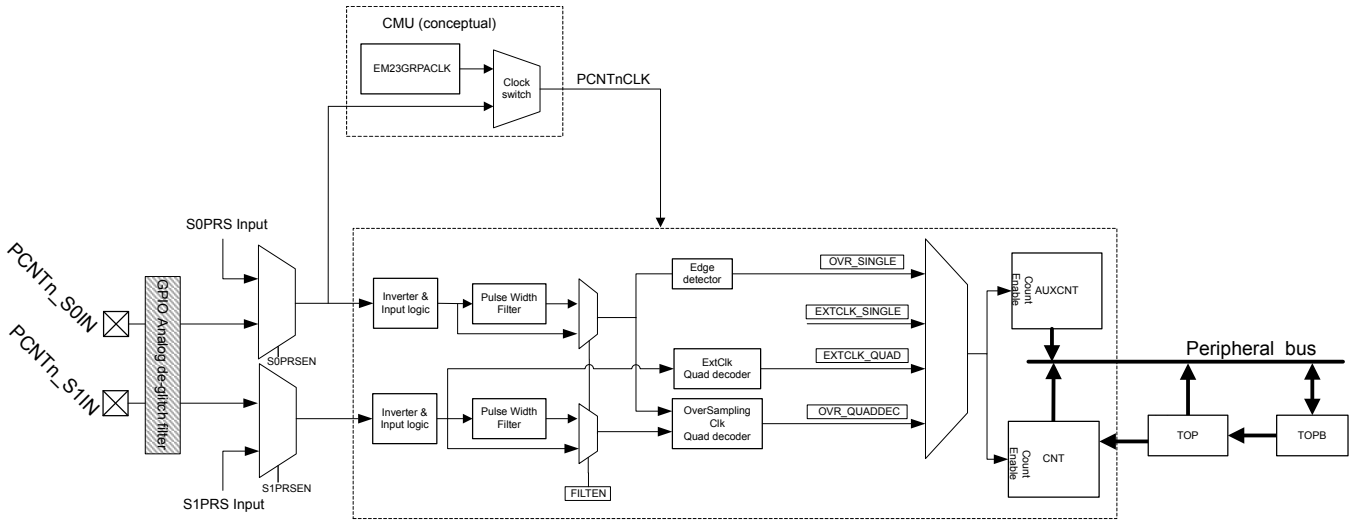


Figure 27.1. PCNT Overview

27.3.1 Pulse Counter Modes

The pulse counter can operate in single input oversampling mode (OVSSINGLE), externally clocked single input counter mode (EXTCLKSINGLE), externally clocked quadrature decoder mode (EXTCLKQUAD) and oversampling quadrature decoder modes(OVSQUAD1X, OVSQUAD2X and OVSQUAD4X). The following sections describe operation of each of these modes and how they are enabled.

27.3.1.1 Single Input Oversampling Mode

This mode is selected by writing OVSSINGLE to the MODE field in the PCNTn_CFG register. The STARTCNT bit in PCNTn_CMD is used to start the counter, and STOPCNT can be used to stop the counter. The EM23GRPACLK clock source to the pulse counter is selected by setting CLKSEL in the CMU_PCNT0CLKCTRL register to EM23GRPACLK. In this mode the maximum input toggle frequency should be 2 times slower than the frequency of the selected EM23GRPACLK clock source.

The optional pulse width filter is enabled by setting the FILTEN bit in the PCNTn_CFG register. Additionally, the PCNTn_S0IN input may be inverted, so that falling edges are counted, by setting the EDGE bit in the PCNTn_CTRL register.

If S1CDIR in the PCNTn_CTRL register is cleared, PCNTn_S0IN is the only observed input in this mode. The PCNTn_S0IN input is sampled by the PCNTnCLK and the number of detected positive or negative edges on PCNTn_S0IN appears in PCNTn_CNT. By default the counter will count up, but the counter may be configured to count down by setting the CNTDIR bit in PCNTn_CTRL.

The counting direction can also be controlled externally in this mode, by setting S1CDIR. This will make the input value on PCNTn_S1IN decide the direction counted for each PCNTn_S0IN edge. When PCNTn_S1IN is high, the count is done according to CNTDIR in PCNTn_CTRL. When PCNTn_S1IN is low, the count direction is opposite.

27.3.1.2 Externally Clocked Single Input Counter Mode

This mode is enabled by writing EXTCLKSINGLE to the MODE field in the PCNTn_CFG register. The STARTCNT bit in PCNTn_CMD is used to start the counter, and STOPCNT can be used to stop the counter. The external pin clock source is selected by setting CLKSEL in the CMU_PCNT0CLKCTRL register to PCNTS0.

Positive edges on PCNTn_S0IN are used to clock the counter. Similar to the oversampled mode, PCNTn_S1IN is used to determine the count direction if S1CDIR is set. If not, CNTDIR in PCNTn_CTRL solely defines count direction.

The digital pulse width filter is not available in this mode. The analog de-glitch filter in the GPIO pads is capable of removing some unwanted noise. However, this mode may be susceptible to spikes and unintended pulses from devices such as mechanical switches, and is therefore most suited to take input from electronic sensors etc. that generate single wire pulses.

27.3.1.3 Quadrature Decoder Modes

Two different types of quadrature decoding are supported in the pulse counter: the externally clocked (Asynchronous) quadrature decoding and the oversampling (Synchronous) quadrature decoding. The externally clocked mode supports 1X quadrature decoding whereas the oversampling mode supports 1X, 2X and 4X quadrature decoding. These modes are described in detail in 27.3.1.4 Externally Clocked Quadrature Decoder Mode and 27.3.1.5 Oversampling Quadrature Decoder Mode .

27.3.1.4 Externally Clocked Quadrature Decoder Mode

This mode is enabled by writing EXTCLKQUAD to the MODE field in PCNTn_CFG. The STARTCNT bit in PCNTn_CMD is used to start the counter, and STOPCNT can be used to stop the counter. The external pin clock source is selected by setting CLKSEL in the CMU_PCNT0CLKCTRL register to PCNTS0.

In this mode, both edges on PCNTn_S0IN pin are used to sample the PCNTn_S1IN pin, in order to decode the quadrature code. A quadrature coded signal contains information about the relative speed and direction of a rotating shaft as illustrated by Figure 27.2 PCNT Quadrature Coding on page 1076, hence the direction of the counter register PCNTn_CNT is controlled automatically.

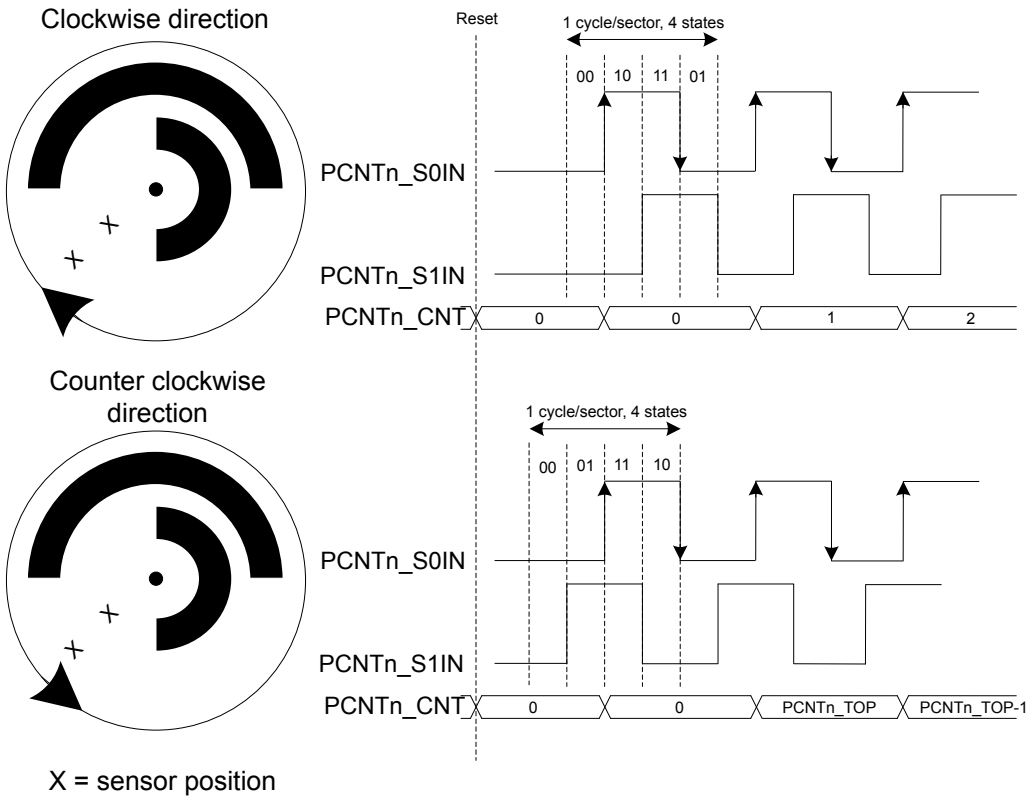


Figure 27.2. PCNT Quadrature Coding

If PCNTn_S0IN leads PCNTn_S1IN in phase, the direction is clockwise, and if it lags in phase the direction is counter-clockwise. Default behavior is illustrated by Figure 27.2 PCNT Quadrature Coding on page 1076.

The counter direction may be read from the DIR bit in the PCNTn_STATUS register. Additionally, the DIRCNG interrupt in the PCNTn_IF register is generated when a direction change is detected. When a change is detected, the DIR bit in the PCNTn_STATUS register must be read to determine the current new direction.

Note: The sector disc illustrated in the figure may be finer grained in some systems. Typically, they may generate 2-4 PCNTn_S0IN wave periods per 360° rotation.

The direction of the quadrature code and control of the counter is generated by the simple binary function outlined by Table 27.1 PCNT QUAD Mode Counter Control Function on page 1076. Note that this function also filters some invalid inputs that may occur when the shaft changes direction or temporarily toggles direction.

Table 27.1. PCNT QUAD Mode Counter Control Function

Inputs		Control/Status	
S1IN posedge	S1IN negedge	Count Enable	CNTDIR status bit
0	0	0	0

Inputs		Control/Status	
S1IN posedge	S1IN negedge	Count Enable	CNTDIR status bit
0	1	1	0
1	0	1	1
1	1	0	0

Note: PCNTn_S1IN is sampled on both edges of PCNTn_S0IN.

27.3.1.5 Oversampling Quadrature Decoder Mode

There are three Oversampling Quadrature Decoder Modes supported: 1X , 2X and 4X. These modes are enabled by writing OVSQUAD1X, OVSQUAD2X and OVSQUAD4X, respectively, to the MODE field in PCNTn_CFG. The STARTCNT bit in PCNTn_CMD is used to start the counter, and STOPCNT can be used to stop the counter. The EM23GRPACLK clock source to the pulse counter must be selected by setting CLKSEL in the CMU_PCNT0CLKCTRL register to EM23GRPACLK.

The optional pulse width filter is enabled by setting the FILTEN bit in the PCNTn_CFG register. The filter applies to both inputs PCNTn_S0IN and PCNTn_S1IN. The filter length is configured by FILTLEN in PCNTn_OVSCTRL register.

Based on the modes selected, the decoder updates the counter on different events. In the OVSQUAD1X mode, the counter is updated on the rising edge of the PCNTn_S0IN input when counting up, and on the negedge of the PCNTn_S0IN input when counting down. In the OVSQUAD2X mode, the counter is updated on both edges of PCNTn_S0IN input. In the OVSQUAD4X mode the counter is updated on both edges of both inputs PCNTn_S0IN and PCNTn_S1IN. Table 27.2 PCNT OVSQUAD 1X, 2X and 4X Mode Counter Control Function on page 1078 outlines the increment or decrement of the counter based on the Quadrature Mode selected.

Note: The decoding behavior of OVSQUAD1X mode is slightly different compared to EXTCLKQUAD mode(also 1X mode). In the EXTCLKQUAD mode, the counter is updated only on the posedge of S0IN input. However, in the OVSQUAD1X mode, the counter is updated on the posedge of S0IN when counting up and on the negedge of S0IN when counting down.

Table 27.2. PCNT OVSQUAD 1X, 2X and 4X Mode Counter Control Function

Direction	Previous State		Next State		OVSQUAD MODE		
	S1IN	S0IN	S1IN	S0IN	1X	2X	4X
Clockwise	0	0	0	1	+1	+1	+1
	0	1	1	1			+1
	1	1	1	0		+1	+1
	1	0	0	0			+1
Counter Clockwise	1	0	1	1		-1	-1
	1	1	0	1			-1
	0	1	0	0	-1	-1	-1
	0	0	1	0			-1

Figure 27.3 PCNT State Transitions for Different Oversampling Quadrature Decoder Modes on page 1079 illustrates the different states of the quadrature input and the state transitions that updates the counter for the different modes. Each cycle of the input states results in 1 update, 2 updates and 4 updates of the counter for OVSQUAD1X, OVSQUAD2X and OVSQUAD4X modes respectively.

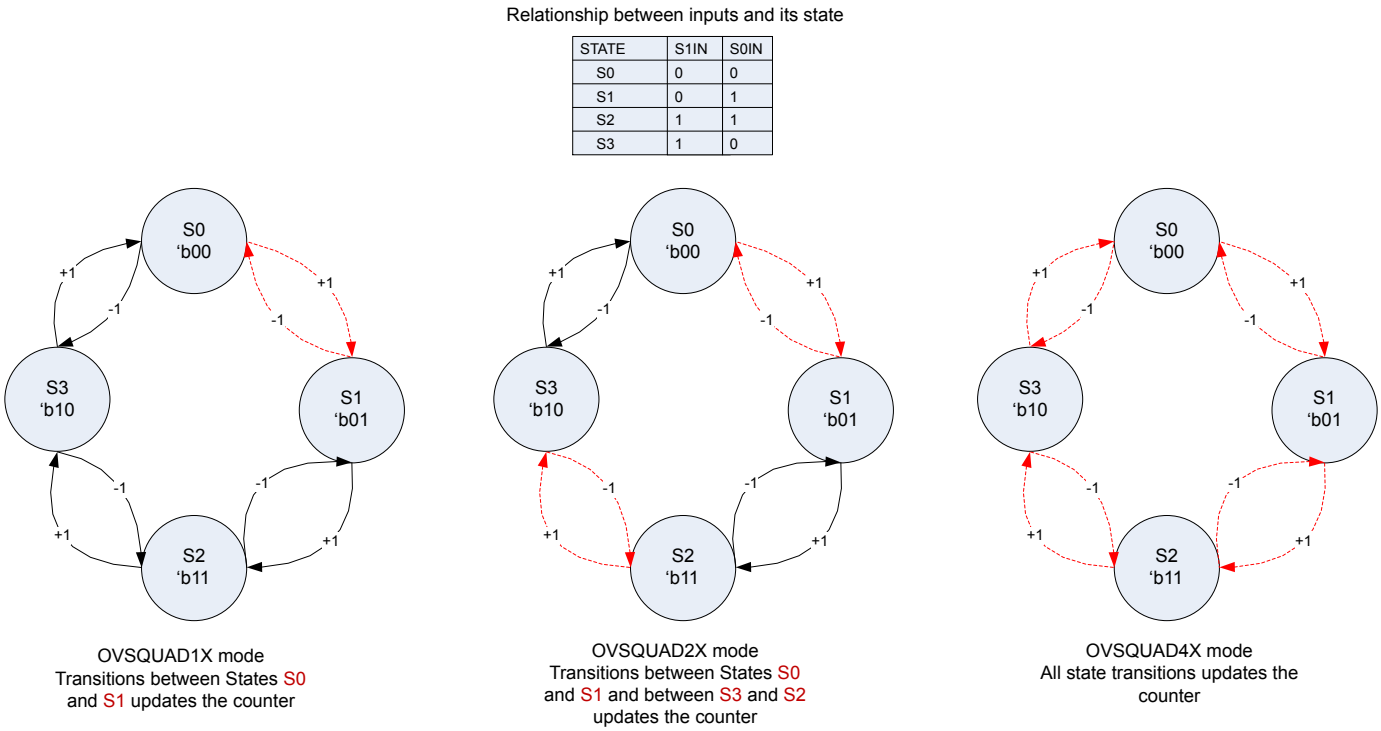


Figure 27.3. PCNT State Transitions for Different Oversampling Quadrature Decoder Modes

The counter direction can be read from the DIR bit in PCNTn_STATUS register. Additionally, the DIRCNG interrupt in the PCNTn_IF is generated when the direction change is detected. When a change is detected, the DIR bit in the PCNTn_STATUS register must be read to determine the new direction.

In the oversampling quadrature decoder modes, the maximum input toggle frequency supported is PCNTnCLK / 4. For frequencies above PCNTnCLK / 4, incorrect decoding occurs. The different decoding modes and the counter updates are further illustrated by Figure 27.4 PCNT Oversampling Quadrature Decoder 1X Mode on page 1079, Figure 27.5 PCNT Oversampling Quadrature Decoder 2X Mode on page 1080 and Figure 27.6 PCNT Oversampling Quadrature Decoder 4X Mode on page 1080.

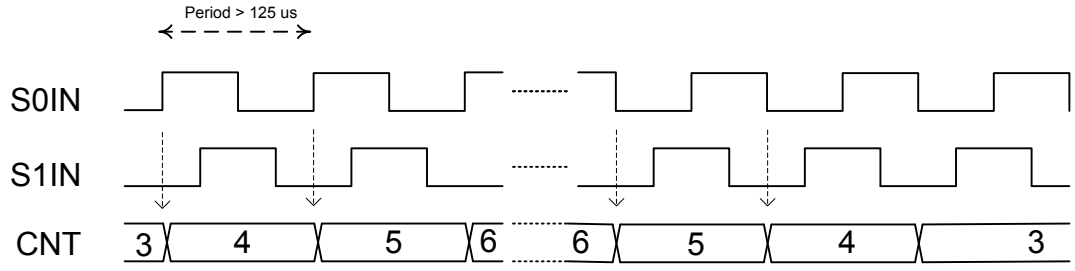


Figure 27.4. PCNT Oversampling Quadrature Decoder 1X Mode

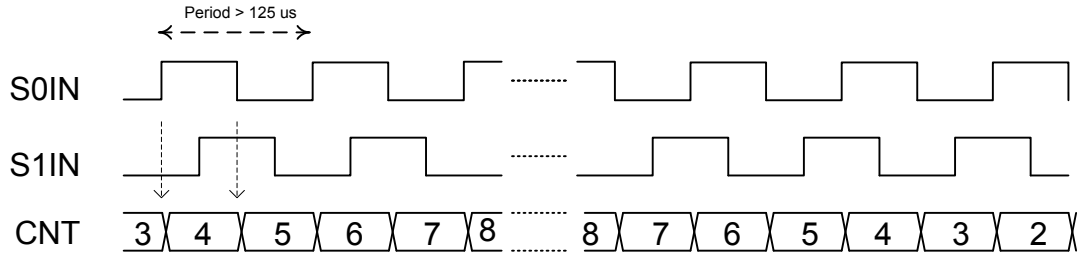


Figure 27.5. PCNT Oversampling Quadrature Decoder 2X Mode

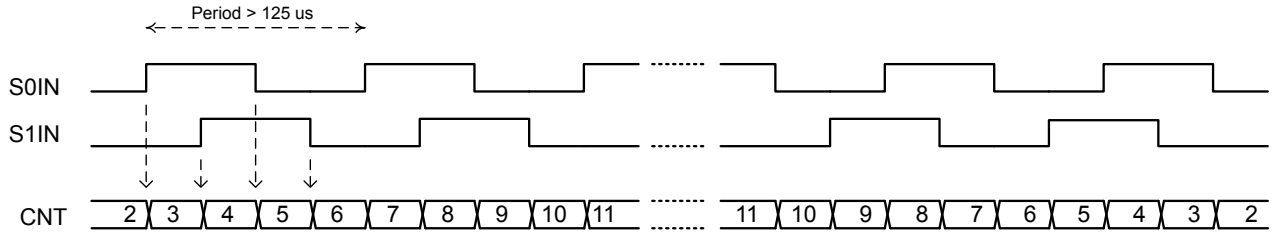


Figure 27.6. PCNT Oversampling Quadrature Decoder 4X Mode

The above modes, by default, are prone to flutter effects in the inputs PCNTn_S0IN and PCNTn_S1IN. When this occurs, the counter changes directions rapidly causing DIRCNG interrupts and unnecessarily waking the core. To prevent this, set FLUTTERRM in the PCNTn_OVSCTRL register. When enabled, flutter is removed, thus preventing unnecessary wakeup of the core. The flutter removal logic works by preventing update of the counter value if the wheel keeps changing direction as a result of flutter. The counter is only updated if the current and previous state transition of the rotation are in the same direction. These state transitions are quadrature decoder mode specific. The highlighted state transitions in Figure 27.3 PCNT State Transitions for Different Oversampling Quadrature Decoder Modes on page 1079 are the ones considered for the different quadrature decoder modes. Figure 27.7 PCNT Oversampling Quadrature Decoder with Flutter Removal on page 1080 shows how the counter is updated for the different quadrature decoder modes with flutter removal FLUTTERRM enabled in PCNTn_OVSCTRL.

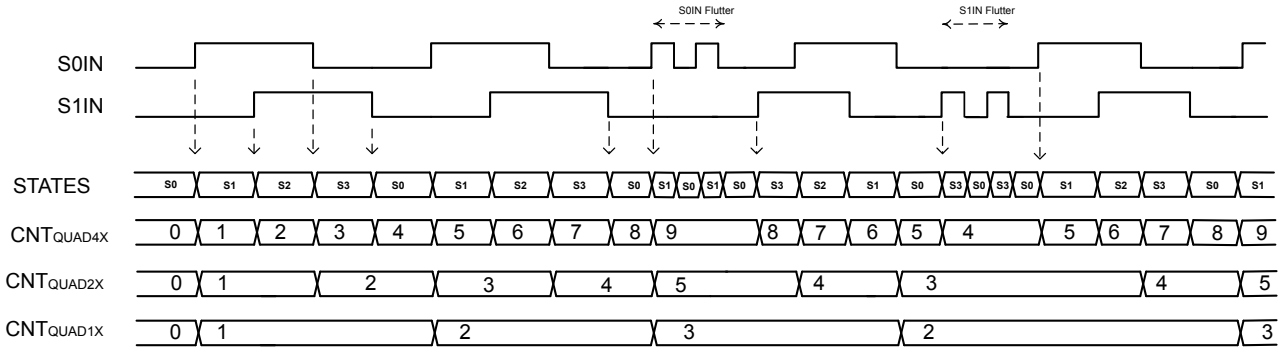


Figure 27.7. PCNT Oversampling Quadrature Decoder with Flutter Removal

27.3.2 Hysteresis

By default the pulse counter wraps to 0 when passing the configured top value, and wraps to the top value when counting down from 0. On these events, a system will likely want to wake up to store and track the overflow count. This is fine if the pulse counter is tracking a monotonic value or a value that does not change directions frequently. In the latter scenario, if the counter changes directions around the overflow/underflow point, the system will have to wake up frequently to keep track of the rotations, resulting in higher current consumption.

To solve this, the pulse counter has a way of introducing hysteresis to the counter. When HYST in PCNTn_CFG is set, the pulse counter will always wrap to TOP/2 on underflows and overflows. This takes the counter away from the area where it might overflow or underflow, removing the problem. Figure 27.8 PCNT Hysteresis behavior of Counter on page 1081 illustrates the hysteresis behavior.

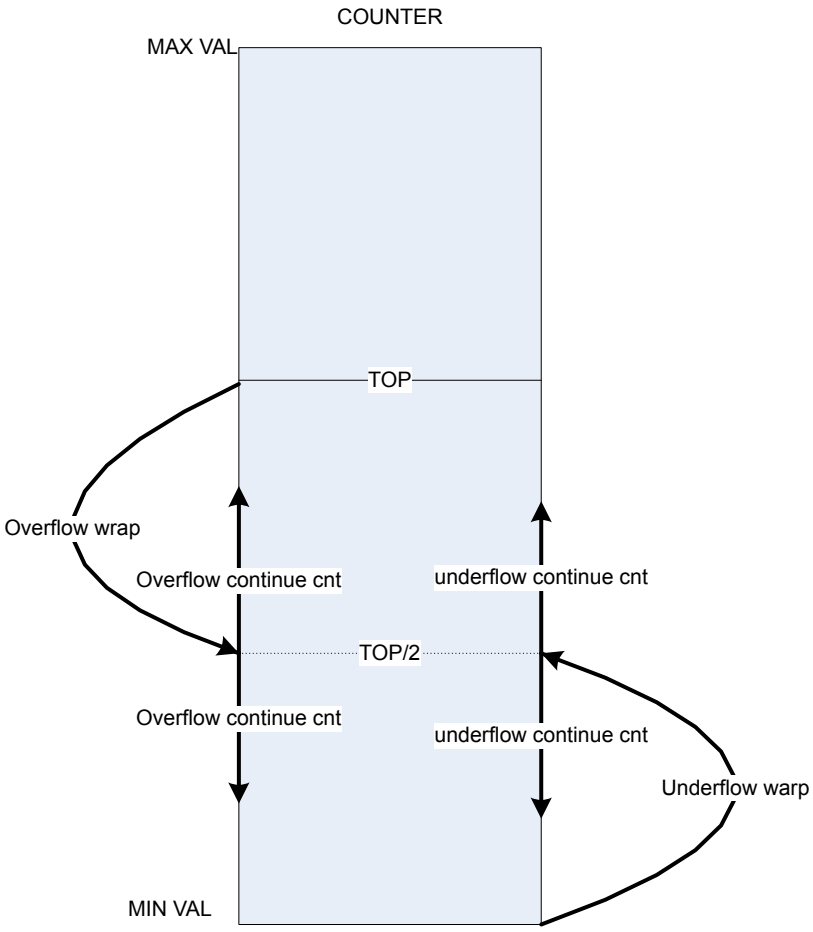


Figure 27.8. PCNT Hysteresis behavior of Counter

Given a starting value of 0 for the counter, the absolute count value when hysteresis is enabled can be calculated with the equations Figure 27.9 Absolute Position With Hysteresis and Even TOP Value on page 1081 or Figure 27.10 Absolute Position With Hysteresis and Odd TOP Value on page 1081, depending on whether the TOP value is even or odd.

$$CNT_{abs} = CNT - UF_{CNT} \times (TOP/2+1) + OF_{CNT} \times (TOP/2+1)$$

Figure 27.9. Absolute Position With Hysteresis and Even TOP Value

$$CNT_{abs} = CNT - UF_{CNT} \times (TOP/2+1) + OF_{CNT} \times (TOP/2+2)$$

Figure 27.10. Absolute Position With Hysteresis and Odd TOP Value

27.3.3 Auxiliary Counter

To be able to keep explicit track of counting in one direction in addition to the regular counter which counts both up and down, the auxiliary counter can be used. The pulse counter can, for instance, be configured to keep track of the absolute rotation of the wheel, while at the same time the auxiliary counter can keep track of how much the wheel has reversed.

The auxiliary counter is enabled by configuring AUXCNTEV in PCNTn_CTRL. It will always count up, but it can be configured whether it should count up on up-events, down-events or both, keeping track of rotation either way or general movement. The value of the auxiliary counter can be read from the PCNTn_AUXCNT register.

Overflows on the auxiliary counter happen when the auxiliary counter passes the top value of the pulse counter, configured in PCNTn_TOP. In that event, the AUXOF interrupt flag is set, and the auxiliary counter wraps to 0.

The auxiliary counter is started and stopped in a similar way to the main counter, using commands in the PCNTn_CMD register. The STARTAUXCNT bit in PCNTn_CMD is used to start the auxiliary counter, and STOPAUXCNT can be used to stop the auxiliary counter.

As the auxiliary counter, the main counter can be configured to count only on certain events. This is done through CNTEV in PCNTn_CTRL, and it is possible like for the auxiliary counter, to make the main counter count on only up and down events. The difference between the counters is that where the auxiliary counter will only count up, the main counter will count up or down depending on the direction of the count event.

27.3.4 Register Access

The counter-clock domain may be clocked externally. To update the counter-clock domain registers from software in this mode, 2-3 clock pulses on the external clock are needed to synchronize accesses to the externally clocked domain. Clock source switching is controlled from the registers in the CMU.

When the CORERST bit in the PCNTn_CMD register is set by software, the PCNT clock domain is synchronously reset and released two PCNT clock edges later. This synchronous reset restores the reset values in PCNTn_TOP, PCNTn_CNT and other core registers in the PCNT clock domain.

CNTRST works in a similar manner as CORERST, but only resets the counter, CNT. Note that the counter is also reset by CORERST.

AUXCNTRST works in a similar manner as CORERST, but only resets the auxiliary counter, PCNTn_AUXCNT. Note that the auxiliary counter is also reset by CORERST.

Note: PCNTn_CNT is a read-only register. When writing to PCNTn_TOP, make sure that the counter value, PCNTn_CNT, can not exceed the value written to PCNTn_TOP within two clock cycles.

Note: To ensure reset during SWRST, if the counter-clock domain is clocked externally, it is advisable to swith the counter-clock to the internal clock before performing the software reset. The clock pulses from an external source cannot be relied upon. By switching to an internal clock the software reset operation completion will be guaranteed.

27.3.5 Clock Sources

The pulse counter may be clocked from two possible clock sources: EM23GRPACLK or an external clock. The clock selection is configured by setting the CLKSEL field in the CMU_PCNTnCLKCTRL register. The default clock source is the EM23GRPACLK.

This PCNT module may also use PCNTn_S0IN as an external clock to clock the counter (EXTCLKSINGLE mode) and to sample PCNTn_S1IN (EXTCLKQUAD mode). Setup, hold and max frequency constraints for PCNTn_S0IN and PCNTn_S1IN for these modes are specified in the device data sheet.

Note: If changing PCNT to an external clock source, either through the PCNTn_S0IN or S0PRS input, the CMU clock switch will need at least 2 external clocks to sync over to that new clock source. Register will not load and counting will not begin until there are few external clocks.

Note: Switching external clock source to the S0PRS input can cause a clock glitch. So S0PRSEN in PCNTn_CFG should be configured before configuring the CLKSEL field in CMU_PCNTnCLKCTRL.

27.3.6 Input Filter

An optional pulse width filter is available in OVSSINGLE and OVSQUAD modes, when EM23GRPACLK is selected as a clock source for the Pulse Counter. The filter is enabled by writing 1 to the FILTEN bit in the PCNTn_CTRL register. When enabled, the high and low periods of PCNTn_S0IN and PCNTn_S1IN must be stable for a programmable number of consecutive clock cycles before the edge is passed to the edge detector. The filter length should be programmed in FILTLEN field of the PCNTn_OVSCTRL register.

The filter length is given by Figure 27.11 PCNT Input Filter Length Equation on page 1083:

Filter length = (FILTLEN + 5) EM23GRPACLK cycles

Figure 27.11. PCNT Input Filter Length Equation

The maximum filter length configured is 260 EM23GRPACLK cycles.

In EXTCLKSINGLE and EXTCLKQUAD mode, there is no digital pulse width filter available.

27.3.7 Edge Polarity

The edge polarity can be set by configuring the EDGE bit in the PCNTn_CTRL register. When this bit is cleared, the pulse counter counts positive edges of PCNTn_S0IN input. When this bit is set, the pulse counter counts negative edges in OVSSINGLE mode. Also, when the EDGE bit is set in the OVSSINGLE and EXTCLKSINGLE modes, the PCNTn_S1IN input is inverted. In OVSQUAD 1X-4X modes the EDGE bit inverts both inputs.

Note: The EDGE bit in PCNTn_CTRL has no effect in EXTCLKQUAD mode.

27.3.8 PRS and PCNTn_S0IN,PCNTn_S1IN Inputs

It is possible to receive input from a PRS signal on both PCNTn_S0IN (or PCNTn_S1IN) by setting S0PRSEN (or S1PRSEN) in PCNTn_CFG. Routing of PRS channels to the inputs is performed using the PRS_CONSUMER_PCNTn_S0IN and PRS_CONSUMER_PCNTn_S1IN registers.

In the Oversampling quadrature decoder modes, the input frequency should be less than 4 times slower than the sampling clock PCNTnCLK to ensure correct functionality.

In the Single Input Oversampling Mode, the input toggle frequency should be 2 times slower than the sampling clock PCNTnCLK to ensure correct functionality.

In the externally clocked modes (where S0IN or S0PRS is used as PCNTnCLK clock source), the input frequency should be less than 1 MHz to ensure correct functionality.

The PCNT module generates two PRS signals, the PCNTn UFOF signal and the PCNTn DIR signal. The PCNTn UFOF signal is generated when the counter overflows or underflows. The PCNTn DIR signal is a level, and indicates the current direction of count of counter CNT.

27.3.9 Interrupts

The interrupt generated by PCNT uses the PCNTn_INT interrupt vector. Software must read the PCNTn_IF register to determine which module interrupt that generated the vector invocation.

27.3.9.1 Underflow and Overflow Interrupts

The underflow interrupt flag (UF) is set when the counter counts down from 0 (i.e. when the value of the counter is 0 and a new pulse is received). The PCNTn_CNT register is loaded with the PCNTn_TOP value after this event.

The overflow interrupt flag (OF) is set when the counter counts up from the PCNTn_TOP (reload) value (i.e. if PCNTn_CNT = PCNTn_TOP and a new pulse is received). The PCNTn_CNT register is loaded with the value 0 after this event.

27.3.9.2 Direction Change Interrupt

The PCNTn_PCNT module sets the DIRCNG interrupt flag (PCNTn_IF register) for EXTCLKQUAD and OVSQUAD1X-4X modes when the direction of the quadrature code changes. The behavior of this interrupt in the EXTCLKQUAD mode is illustrated by Figure 27.12 PCNT Direction Change Interrupt (DIRCNG) Generation on page 1084.

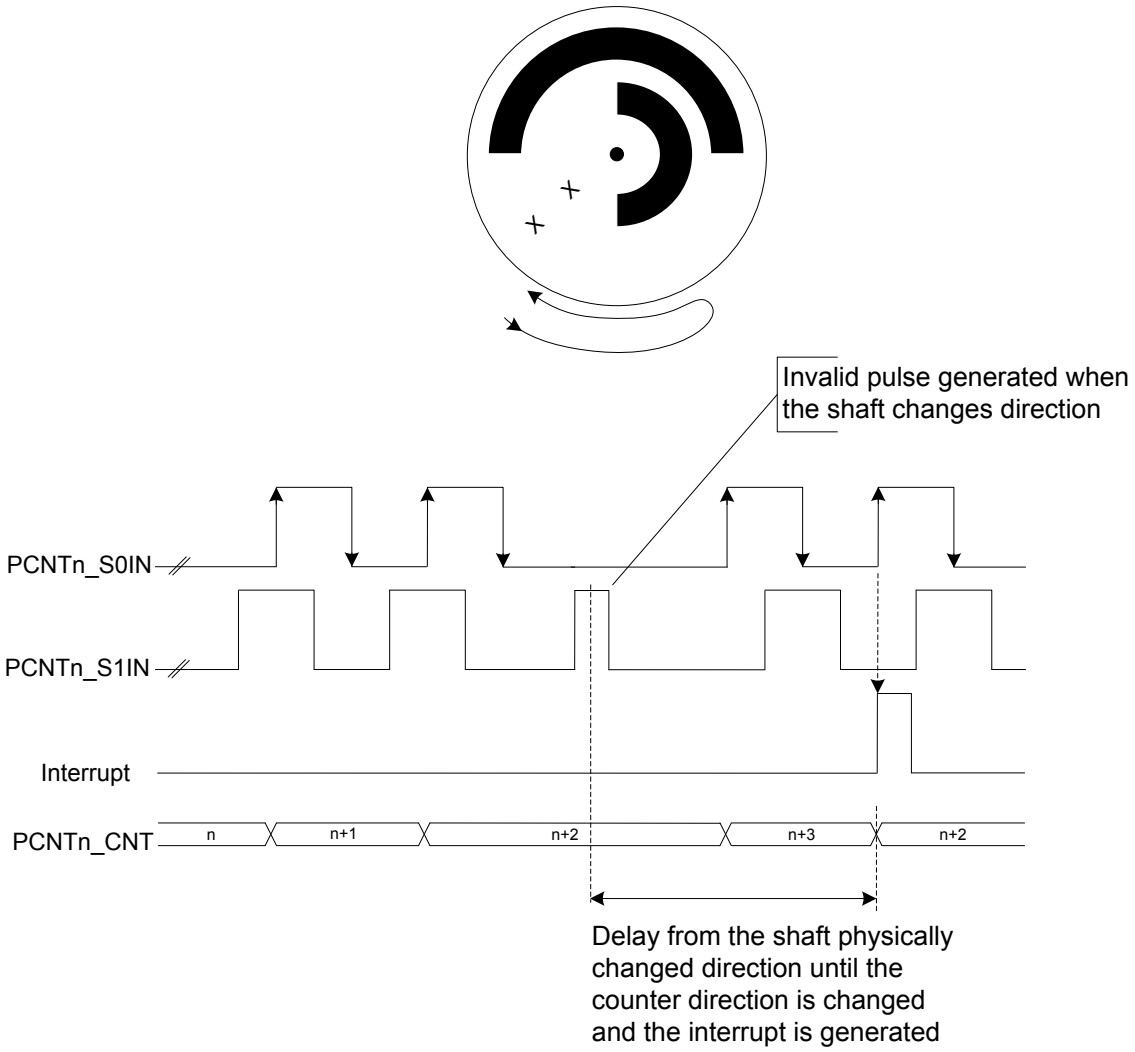


Figure 27.12. PCNT Direction Change Interrupt (DIRCNG) Generation

27.4 PCNT Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	PCNT_IPVERSION	R	IP Version ID
0x004	PCNT_EN	RW ENABLE	Module Enable Register
0x008	PCNT_SWRST	RW SWRST	Software Reset Register
0x00C	PCNT_CFG	RW CONFIG	Configuration Register
0x010	PCNT_CTRL	RW LFSYNC	Control Register
0x014	PCNT_CMD	W LFSYNC	Command Register
0x018	PCNT_STATUS	RH	Status Register
0x01C	PCNT_IF	RWH INTFLAG	Interrupt Flag Register
0x020	PCNT_IEN	RW	Interrupt Enable Register
0x024	PCNT_CNT	RH	Counter Value Register
0x028	PCNT_AUXCNT	RH	Auxiliary Counter Value Register
0x02C	PCNT_TOP	RWH LFSYNC	Top Value Register
0x030	PCNT_TOPB	RW LFSYNC	Counter Top Value Buffer Register
0x034	PCNT_OVSCTRL	RW LFSYNC	Oversampling Control Register
0x038	PCNT_SYNCBUSY	RH	Synchronization Busy Register
0x03C	PCNT_LOCK	W	Configuration Lock Register
0x1000	PCNT_IPVERSION_SET	R	IP Version ID
0x1004	PCNT_EN_SET	RW ENABLE	Module Enable Register
0x1008	PCNT_SWRST_SET	RW SWRST	Software Reset Register
0x100C	PCNT_CFG_SET	RW CONFIG	Configuration Register
0x1010	PCNT_CTRL_SET	RW LFSYNC	Control Register
0x1014	PCNT_CMD_SET	W LFSYNC	Command Register
0x1018	PCNT_STATUS_SET	RH	Status Register
0x101C	PCNT_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x1020	PCNT_IEN_SET	RW	Interrupt Enable Register
0x1024	PCNT_CNT_SET	RH	Counter Value Register
0x1028	PCNT_AUXCNT_SET	RH	Auxiliary Counter Value Register
0x102C	PCNT_TOP_SET	RWH LFSYNC	Top Value Register
0x1030	PCNT_TOPB_SET	RW LFSYNC	Counter Top Value Buffer Register
0x1034	PCNT_OVSCTRL_SET	RW LFSYNC	Oversampling Control Register
0x1038	PCNT_SYNCBUSY_SET	RH	Synchronization Busy Register
0x103C	PCNT_LOCK_SET	W	Configuration Lock Register
0x2000	PCNT_IPVERSION_CLR	R	IP Version ID
0x2004	PCNT_EN_CLR	RW ENABLE	Module Enable Register
0x2008	PCNT_SWRST_CLR	RW SWRST	Software Reset Register

Offset	Name	Type	Description
0x200C	PCNT_CFG_CLR	RW CONFIG	Configuration Register
0x2010	PCNT_CTRL_CLR	RW LFSYNC	Control Register
0x2014	PCNT_CMD_CLR	W LFSYNC	Command Register
0x2018	PCNT_STATUS_CLR	RH	Status Register
0x201C	PCNT_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x2020	PCNT_IEN_CLR	RW	Interrupt Enable Register
0x2024	PCNT_CNT_CLR	RH	Counter Value Register
0x2028	PCNT_AUXCNT_CLR	RH	Auxiliary Counter Value Register
0x202C	PCNT_TOP_CLR	RWH LFSYNC	Top Value Register
0x2030	PCNT_TOPB_CLR	RW LFSYNC	Counter Top Value Buffer Register
0x2034	PCNT_OVSCTRL_CLR	RW LFSYNC	Oversampling Control Register
0x2038	PCNT_SYNCBUSY_CLR	RH	Synchronization Busy Register
0x203C	PCNT_LOCK_CLR	W	Configuration Lock Register
0x3000	PCNT_IPVERSION_TGL	R	IP Version ID
0x3004	PCNT_EN_TGL	RW ENABLE	Module Enable Register
0x3008	PCNT_SWRST_TGL	RW SWRST	Software Reset Register
0x300C	PCNT_CFG_TGL	RW CONFIG	Configuration Register
0x3010	PCNT_CTRL_TGL	RW LFSYNC	Control Register
0x3014	PCNT_CMD_TGL	W LFSYNC	Command Register
0x3018	PCNT_STATUS_TGL	RH	Status Register
0x301C	PCNT_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x3020	PCNT_IEN_TGL	RW	Interrupt Enable Register
0x3024	PCNT_CNT_TGL	RH	Counter Value Register
0x3028	PCNT_AUXCNT_TGL	RH	Auxiliary Counter Value Register
0x302C	PCNT_TOP_TGL	RWH LFSYNC	Top Value Register
0x3030	PCNT_TOPB_TGL	RW LFSYNC	Counter Top Value Buffer Register
0x3034	PCNT_OVSCTRL_TGL	RW LFSYNC	Oversampling Control Register
0x3038	PCNT_SYNCBUSY_TGL	RH	Synchronization Busy Register
0x303C	PCNT_LOCK_TGL	W	Configuration Lock Register

27.5 PCNT Register Description

27.5.1 PCNT_IPVERSION - IP Version ID

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x1																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x1	R	**IP VERSION**
	Gives access to the IP VERSION of PCNT			

27.5.2 PCNT_EN - Module Enable Register

Offset	Bit Position																															
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	RW
Name																															DISABLING	EN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DISABLING	0x0	R	**Disablement busy status**
	When EN is cleared, DISABLING status is set immediately, and cleared when disablement finishes. Disablement resets peripheral cores and not APB registers except the INTFLAG register.			
0	EN	0x0	RW	**PCNT Module Enable**
	Enable the PCNT module. When EN is cleared(disablement), it halts module operation immediately, and initialize the core domain such that when the is re-enabled, it starts cleanly.			

27.5.3 PCNT_SWRST - Software Reset Register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	W
Name																															RESETTING	SWRST

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	RESETTING	0x0	R	**Software reset busy status** When SWRST command is issued, resetting logic sets RESETTING status immediately, and later it is cleared when reset process finishes.
0	SWRST	0x0	W	**Software reset command** A software reset command field resets the module back to the initial condition, similar to a power on reset condition

27.5.4 PCNT_CFG - Configuration Register

Offset	Bit Position																															
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0	0x0		0x0	0x0	0x0		0x0		
Access																							RW	RW		RW	RW	RW		RW		
Name																							S1PRSEN	S0PRSEN		HYST	FILTEN	DEBUGHALT		MODE		

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	S1PRSEN	0x0	RW	**S1IN PRS Enable**
	When set, the PRS channel is selected as input to S1IN.			
8	S0PRSEN	0x0	RW	**S0IN PRS Enable**
	When set, the PRS channel is selected as input to S0IN.			
7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6	HYST	0x0	RW	**Enable Hysteresis**
	When hysteresis is enabled, the PCNT will always overflow and underflow to TOP/2.			
5	FILTEN	0x0	RW	**Enable Digital Pulse Width Filter**
	The filter passes all high and low periods that are at least (FILTLEN+5) clock cycles wide. This filter is only available in OVSSINGLE,OVSQUAD1X-4X modes.			
4	DEBUGHALT	0x0	RW	**Debug Mode Halt Enable**
	Set to halt the PCNT in debug mode only in OVSSINGLE and OVSQUAD modes. When in EXTCLKSINGLE or EXTCLKQUAD modes, DEBUGHALT does not halt the Pulse Counter.			

Value	Mode	Description
0	DISABLE	PCNT is running in debug mode.
1	ENABLE	PCNT is frozen in debug mode.

3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2:0	MODE	0x0	RW	**Mode Select**
	Selects the mode of operation. The corresponding clock source must be selected from the CMU.			

Value	Mode	Description
0	OVSSINGLE	Single input EM23GRPACLK oversampling mode (available in EM0-EM3).
1	EXTCLKSINGLE	Externally clocked single input counter mode (available in EM0-EM3).
2	EXTCLKQUAD	Externally clocked quadrature decoder mode (available in EM0-EM3).

Bit	Name	Reset	Access	Description
	3	OVSQUAD1X		EM23GRPACLK oversampling quadrature decoder 1X mode (available in EM0-EM3).
	4	OVSQUAD2X		EM23GRPACLK oversampling quadrature decoder 2X mode (available in EM0-EM3).
	5	OVSQUAD4X		EM23GRPACLK oversampling quadrature decoder 4X mode (available in EM0-EM3).

27.5.5 PCNT_CTRL - Control Register

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0		0x0			0x0	0x0	0x0
Access																									RW		RW			RW	RW	RW
Name																									AUXCNTEV		CNTEV			EDGE	CNTDIR	S1CDIR

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:6	AUXCNTEV	0x0	RW	**Controls When the Aux Counter Counts** Selects whether the auxiliary counter responds to up-count events, down-count events or both

Value	Mode	Description
0	BOTH	Counts up on both up-count and down-count events.
1	UP	Counts up on up-count events.
2	DOWN	Counts up on down-count events.

Bit	Name	Reset	Access	Description
5:4	CNTEV	0x0	RW	**Controls When the Counter Counts** Selects whether the regular counter responds to up-count events, down-count events or both

Value	Mode	Description
0	BOTH	Counts up on up-count and down on down-count events.
1	UP	Only counts up on up-count events.
2	DOWN	Only counts down on down-count events.

Bit	Name	Reset	Access	Description
3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	EDGE	0x0	RW	**Edge Select** Determines the polarity of the incoming edges. This bit used only in OVSSINGLE, EXTCLKSINGLE and OVSQUAD1X-4X modes.

Value	Mode	Description
0	POS	Positive edges on the PCNTn_S0IN inputs are counted in OVSSINGLE mode. Does not invert PCNTn_S1IN input in OVSSINGLE and EXTCLKSINGLE modes
1	NEG	Negative edges on the PCNTn_S0IN inputs are counted in OVSSINGLE mode. Inverts the PCNTn_S1IN input in OVSSINGLE and EXTCLKSINGLE modes

Bit	Name	Reset	Access	Description
1	CNTDIR	0x0	RW	**Non-Quadrature Mode Counter Direction Co** The direction of the counter must be set in the OVSSINGLE and EXTCLKSINGLE modes. This bit is ignored in EXTCLKQUAD mode as the direction is automatically detected.

Bit	Name	Reset	Access	Description
	Value	Mode		Description
	0	UP		Up counter mode.
	1	DOWN		Down counter mode.
0	S1CDIR	0x0	RW	**Count Direction Determined By S1**
	Allows S1 give the direction of counting when in the OVSSINGLE or EXTCLKSINGLE modes. When S1 is high, the count direction is given by CNTDIR. When S1 is low, the count direction is the opposite given by CNTDIR			

27.5.6 PCNT_CMD - Command Register

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																					0x0	0x0	0x0	0x0				0x0		0x0	0x0	0x0
Access																					W	W	W	W				W(nB)		W(nB)	W(nB)	W(nB)
Name																					STOPAUXCNT	STOPCNT	STARTAUXCNT	STARTCNT				LCNTIM		AUXCNTRST	CNTRST	CORERST

Bit	Name	Reset	Access	Description
31:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11	STOPAUXCNT	0x0	W	**Stop Aux Counter**
	Write a 1 to stop the aux counter			
10	STOPCNT	0x0	W	**Stop Main Counter**
	Write a 1 to stop the main counter			
9	STARTAUXCNT	0x0	W	**Start Aux Counter**
	Write a 1 to start the aux counter			
8	STARTCNT	0x0	W	**Start Main Counter**
	Write a 1 to start the main counter			
7:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	LCNTIM	0x0	W(nB)	**Load CNT Immediately**
	Load PCNTn_TOP into PCNTn_CNT on the next counter clock cycle.			
3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	AUXCNTRST	0x0	W(nB)	**AUXCNT Reset**
	The auxiliary counter, AUXCNT, is synchronously reset when this bit is set. This action clears the auxiliary counter to its reset value			
1	CNTRST	0x0	W(nB)	**CNT Reset**
	The counter, CNT, is synchronously reset when this bit is set. This action clears the counter to its reset value			
0	CORERST	0x0	W(nB)	**PCNT Clock Domain Reset**
	The PCNT clock domain logic is synchronously reset when this bit is set. This action clears the all the PCNT logic and registers to their reset value			

27.5.7 PCNT_STATUS - Status Register

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												R	R	R	R	R
Name																												AUXCNTRUNNING	CNTRUNNING	PCNTLOCKSTATUS	TOPBV	DIR

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	AUXCNTRUNNING	0x0	R	**Aux Counter running status**
	Indicates the current status of PCNT auxiliary counter running. The counter status will continue to indicate as Running even when it is halted during debug assertion.			
3	CNTRUNNING	0x0	R	**Main Counter running status**
	Indicates the current status of PCNT main counter running. The counter status will continue to indicate as Running even when it is halted during debug assertion.			
2	PCNTLOCKSTATUS	0x0	R	**Lock Status**
	Indicates the current status of PCNT Lock			

Value	Mode	Description
0	UNLOCKED	PCNT registers are unlocked
1	LOCKED	PCNT registers are locked

Bit	Name	Reset	Access	Description
1	TOPBV	0x0	R	**TOP Buffer Valid**
	This indicates that PCNTn_TOPB contains valid data that has not been written to PCNTn_TOP. This bit is also cleared when PCNTn_TOP is written.			
0	DIR	0x0	R	**Current Counter Direction**
	Current direction status of the counter. This bit is valid in EXTCLKQUAD mode only.			

Value	Mode	Description
0	UP	Up counter mode (clockwise in EXTCLKQUAD mode with the EDGE bit in PCNTn_CTRL set to 0).
1	DOWN	Down counter mode.

27.5.8 PCNT_IF - Interrupt Flag Register

Offset	Bit Position																														
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												RW	RW	RW	RW	RW
Name																												OQSTERR	AUXOF	DIRCNG	OF	UF

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	OQSTERR	0x0	RW	**Oversampling Quad State Err Int Flag**
	Set in the Oversampling Quadrature Mode when incorrect state transition occurs			
3	AUXOF	0x0	RW	**Auxiliary Overflow Interrupt Read Flag**
	Set when an Auxiliary CNT overflow occurs			
2	DIRCNG	0x0	RW	**Direction Change Detect Interrupt Flag**
	Set when the count direction changes. Set in EXTCLKQUAD mode only.			
1	OF	0x0	RW	**Overflow Interrupt Read Flag**
	Set when a CNT overflow occurs			
0	UF	0x0	RW	**Underflow Interrupt Read Flag**
	Set when a CNT underflow occurs			

27.5.9 PCNT_IEN - Interrupt Enable Register

Offset	Bit Position																														
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												RW	RW	RW	RW	RW
Name																												OQSTERR	AUXOF	DIRCNG	OF	UF

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	OQSTERR	0x0	RW	**Oversampling Quad State Err Int Flag**
	Set to enable the OQSTERRIF Interrupt			
3	AUXOF	0x0	RW	**Auxiliary Overflow Interrupt Read Flag**
	Set to enable the AUXOFIF Interrupt			
2	DIRCNG	0x0	RW	**Direction Change Detect Interrupt Flag**
	Set to enable the DIRCNGIF Interrupt			
1	OF	0x0	RW	**Overflow Interrupt Read Flag**
	Set to enable the OFIF Interrupt			
0	UF	0x0	RW	**Underflow Interrupt Read Flag**
	Set to enable the UFIF Interrupt			

27.5.10 PCNT_CNT - Counter Value Register

Offset	Bit Position																														
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	R															
Name																	CNT															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	CNT	0x0	R	**Counter Value**
	Gives read access to the counter.			

27.5.11 PCNT_AUXCNT - Auxiliary Counter Value Register

Offset	Bit Position																															
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	R															
Name																	AUXCNT															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	AUXCNT	0x0	R	**Auxiliary Counter Value**
	Gives read access to the auxiliary counter.			

27.5.12 PCNT_TOP - Top Value Register

Offset	Bit Position																															
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0xFF															
Access																	RW															
Name																	TOP															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	TOP	0xFF	RW	**Counter Top Value**
	When counting down, this value is reloaded into PCNTn_CNT when counting past 0. When counting up, 0 is written to the PCNTn_CNT register when counting past this value.			

27.5.13 PCNT_TOPB - Counter Top Value Buffer Register

Offset	Bit Position																													
0x030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0xFF							
Access																									RW							
Name																									TOPB							

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	TOPB	0xFF	RW	**Counter Top Buffer Register**
	These bits hold the TOP buffer value. Hardware updates the TOP value from TOPB whenever there is Underflow or Overflow event on main counter. The update to TOP wont happen for Overflow event if PCNTn_CTRL.CNTEV = BOTH			

27.5.14 PCNT_OVSCTRL - Oversampling Control Register

Offset	Bit Position																													
0x034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																				0x0					0x0							
Access																				RW					RW							
Name																				FLUTTERRM					FILTLEN							

Bit	Name	Reset	Access	Description
31:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12	FLUTTERRM	0x0	RW	**Flutter Remove**
	When set, removes flutter from Quaddecoder inputs S0IN and S1IN. Available only in OVSQUAD1X-4X modes			
11:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7:0	FILTLEN	0x0	RW	**Configure Filter Length for Inputs S0IN**
	Used only in OVSINGLE,OVSQUAD1X-4X modes. To use this first enable FILTEN in PCNTn_CFG register. Filter length = (FILTLEN + 5) EM23GRPACLK cycles			

27.5.15 PCNT_SYNCBUSY - Synchronization Busy Register

Offset	Bit Position																													
0x038	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												R	R	R	R	R
Name																												OVSCTRL	TOPB	TOP	CMD	CTRL

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	OVSCTRL	0x0	R	**OVSCTRL Register Busy**
	Set when the value written to OVSCTRL register is being synchronized			
3	TOPB	0x0	R	**TOPB Register Busy**
	Set when the value written to TOPB register is being synchronized			
2	TOP	0x0	R	**TOP Register Busy**
	Set when the value written to TOP register is being synchronized			
1	CMD	0x0	R	**CMD Register Busy**
	Set when the value written to CMD register being synchronized			
0	CTRL	0x0	R	**CTRL Register Busy**
	Set when the value written to CTRL register being synchronized			

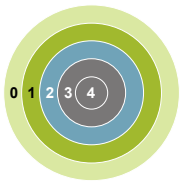
27.5.16 PCNT_LOCK - Configuration Lock Register

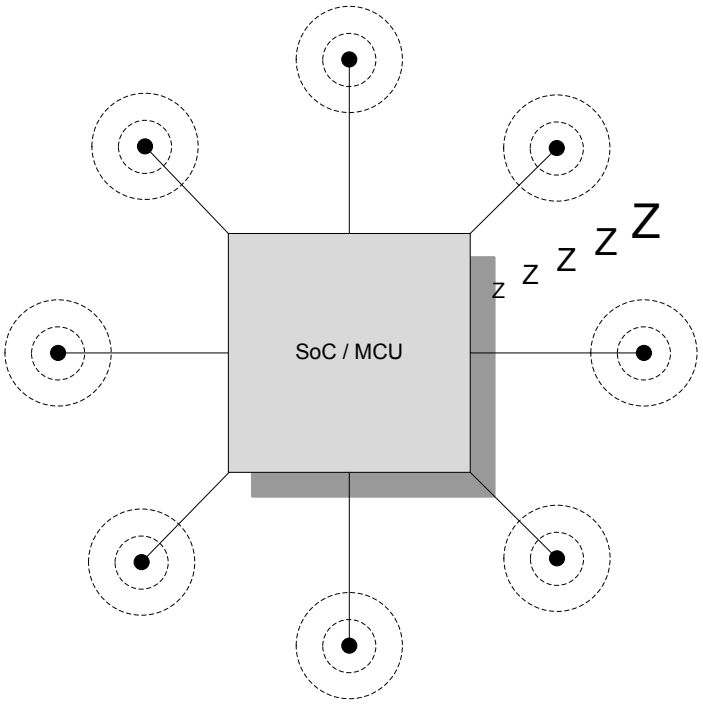
Offset	Bit Position																															
0x03C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0							
Access																									W							
Name																									PCNTLOCKKEY							

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	PCNTLOCKKEY	0x0	W	**Configuration Lock Key** Write any other value than the unlock code to lock PCNT_CFG, PCNT_EN, PCNT_SWRST, PCNT_CMD, PCNT_CTRL, PCNT_OVSCTRL, PCNT_CNT, PCNT_TOP and PCNT_TOPB registers from editing. Write the unlock code to unlock.

Value	Mode	Description
42976	UNLOCK	Write to unock PCNT lockable registers

28. LESENSE - Low Energy Sensor Interface





Quick Facts

What?

LESENSE is a low energy sensor interface capable of autonomously collecting and processing data from multiple sensors even when in EM2. Flexible configuration makes LESENSE a versatile sensor interface compatible with a wide range of sensors and measurement schemes.

Why?

Capability to autonomously monitor sensors allows the EFR32xG25 to reside in a low energy mode for long periods of time while keeping track of sensor status and sensor events.

How?

LESENSE is highly configurable and is capable of collecting data from a wide range of sensor types. Once the data is collected, the programmable state machine, LESENSE decoder, is capable of processing sensor data without CPU intervention. A large result buffer allows the chip to remain in EM2 for long periods of time while autonomously collecting data.

28.1 Introduction

LESENSE is a low energy sensor interface which utilizes on-chip peripherals to perform measurement of a configurable set of sensors. The results from sensor measurements can be processed by the LESENSE decoder, which is a configurable state machine with up to 32 states. The results can also be stored in a FIFO to be collected by CPU or DMA for further processing.

LESENSE operates from EM0 down to EM2, and can wake up the CPU on configurable events.

28.2 Features

- Up to 16 sensors
- Autonomous sensor monitoring in EM0, EM1, and EM2
- Highly configurable decoding of sensor results
- Interrupt on sensor events
- 16-deep FIFO for result storage
- Multiple evaluation modes minimize the need for software interaction
- Supports IADC and ACMP sampling and evaluation
- Support for multiple sensor types
  - LC sensors
  - Capacitive sensing
  - General analog sensors

28.3 Functional Description

The LESENSE module is capable of controlling on-chip peripherals in order to perform monitoring of different sensors with little or no CPU intervention. LESENSE uses the analog comparators (ACMP) or IADC0 for measurement of sensor signals. LESENSE can also control VDAC0 channel 0 to generate accurate reference voltages. Figure 28.1 LESENSE Block Diagram on page 1102 shows an overview of the LESENSE module.

The LESENSE module consists of a sequencer, an evaluation block, a decoder, and a FIFO buffer.

- The sequencer handles interaction with other peripherals and controls timing of sensor measurements. It also includes a counter that can be used to count pulses on the ACMP output.
- The evaluation block is used to process the data collected by the sequencer.
- To autonomously analyze sensor results, the LESENSE decoder provides the ability to define a finite state machine with up to 32 states (64 arcs), with programmable actions upon state transitions. This allows the decoder to implement a wide range of decoding schemes, such as quadrature decoding.
- Measurement results are stored in a FIFO which enables the chip to remain in a low energy mode for longer periods of time while collecting sensor data.

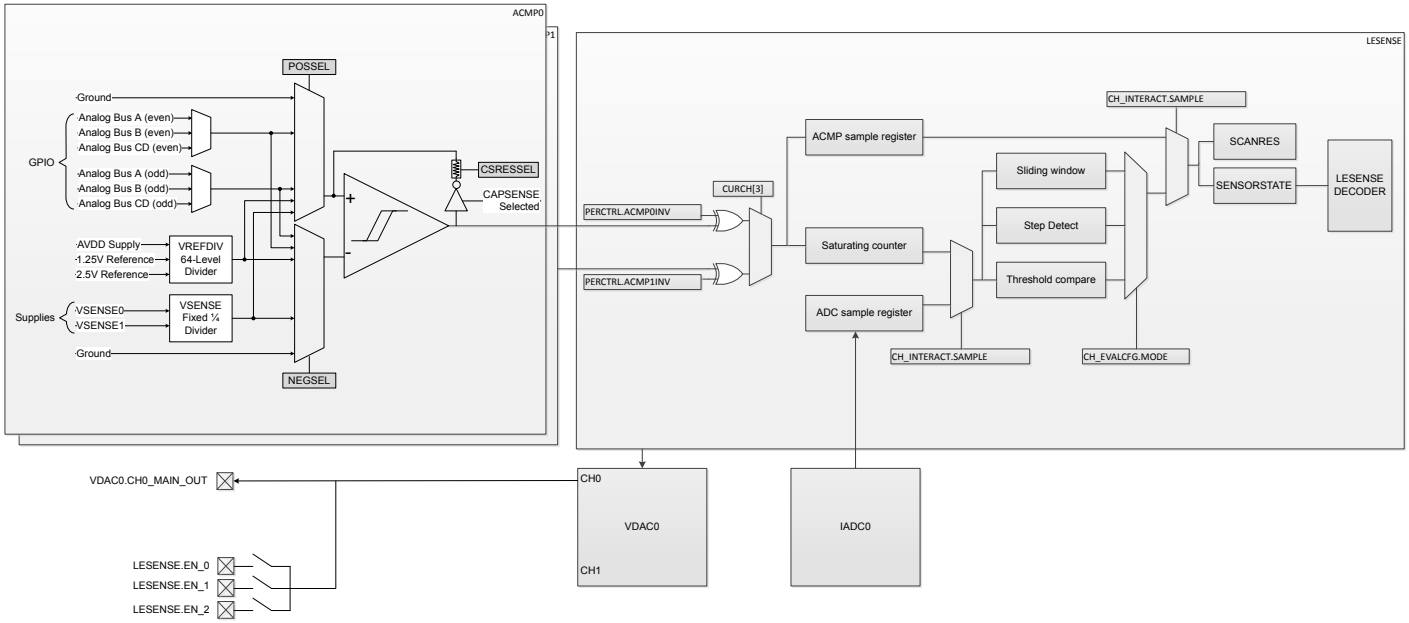


Figure 28.1. LESENSE Block Diagram

28.3.1 Interface Descriptions

ACMP interface

ACMPs are used to measure the sensors, and must be configured according to the application in order for LESENSE to work properly. Channels 0-7 trigger ACMP0, Channels 8-15 trigger ACMP1. Depending on the configuration in the ACMP0MODE and ACMP1MODE bitfields in LESENSE_PERCTRL, LESENSE can take control of the positive input mux and the voltage divider (VREFDIV) for the targeted ACMP. The remaining configuration of the analog comparators is done in the ACMP register interface.

When ACMPxMODE is set to MUX, the LESENSE module will take control of the positive input mux of the ACMP using the ACMP's external override interface. When used this way ACMP_INPUTCTRL_POSSEL should be configured to the base address of the GPIO port to be used. For example, if the desired channel is on Port A, POSSEL should be configured for EXTPA. The offset given by CHx_INTERACT.OFFSET determines which of the port I/O pins on PA to access. To connect to PB03 therefore, ACMP_INPUTCTRL_POSSEL would be set to EXTPB, and LESENSE_CHx_INTERACT.OFFSET to 0x03.

If ACMPxMODE in PERCTRL is set to MUXTHRES, LESENSE will also take control of the voltage divider (VREFDIV) in the ACMP. The threshold used are individual to each channel and is configured using the 6 LSBs of CHx_INTERACT_THRES.

In addition to all this, ACMPxINV in PERCTRL can be used to invert the result from the ACMP to the LESENSE.

IADC interface

LESENSE can be set up to trigger IADC0 conversions and use data from IADC0 to evaluate sensor status. In order to do this, the scan mode of the IADC0 has to be configured within the IADC0 module and the IADC SCAN trigger has to be setup as LESENSE. When the sample delay configured in CHx_TIMING_SAMPLEDLY has expired, LESENSE will initiate an ADC sample. The OFFSET programmed in CHx_INTERACT determines which channel specified in the IADC scanner is converted by the IADC.

VDAC interface

LESENSE is able to drive the DAC for generation of accurate reference voltages. The refresh rate of the DAC channels can be configured in DACCONVTRIG in PERCTRL. If DACCONVTRIG is set to CHANNELSTART, the LESENSE sends a conversion trigger to the DAC channels prior to each sensor measurement. If DACCONVTRIG is set to SCANSTART, the LESENSE sends a conversion trigger to the DAC prior to each scan. The conversion data used by the DAC is either taken from its own data registers in the DAC interface or from the THRES bit-field in the CHx_INTERACT register for the active LESENSE channel. DAC data used is configured in DACCH0DATA in PERCTRL.

None of the other DAC settings can be overriden from the LESENSE. For the DAC to be able to be used by the LESENSE, the DAC trigger source should be configured as LESENSE.

All LESENSE channels can send triggers to the DAC. However, only LESENSE channels 0,1,2 have the capability to switch the DAC output onto specific GPIOs. These channels have the been mapped to LESENSE.EN_0, EN_1, and EN_2 and have the possibility to control the switches that connect the VDAC channel 0 main output to these pins. This makes LESENSE able to excite sensors with output from VDAC channel 0. For LESENSE channel 0,1,2 to enable the DAC output switches in idle phase their IDLECONF should be DACOUT. For these channels to enable the switches in Excite phase the EXMODE should be DACOUT and ALTEX should be 0. Consequently, LESENSE channel 8,9,10 can enable the DAC output switches in excite phase if their EXMODE is DACOUT and ALTEX is 1.

Note: LESENSE only interacts with VDAC0 channel 0.

28.3.2 Channel Configuration

LESENSE has 16 individually configurable channels. Each channel has its own set of configuration registers. Channel configuration is split into Four registers; CHx_TIMING, CHx_INTERACT, CHx_EVALCFG and CHx_EVALTHRES. Individual timing for each sensor is configured in CHx_TIMING, sensor interaction is configured in CHx_INTERACT, (static) configurations regarding evaluation of the measurements are done in CHx_EVALCFG and the (dynamic) thresholds used in the various evaluation modes are stored in the CHx_EVALTHRES. For improved readability, CHx_CONF will be used to refer to all the channel configuration registers as a group (CHx_TIMING, CHx_INTERACT, CHx_EVALCFG and CHx_EVALTHRES) in places throughout this chapter.

By default, the channel configuration registers are directly mapped to the channel number. Configuring CFG.SCANCONF makes it possible to alter this mapping.

Configuring SCANCONF to INVMAP will make channels 0-7 use the channel configuration registers for channels 8-15, and vice versa. This feature allows an application to quickly and easily switch the configuration set for the channels.

Setting SCANCONF to TOGGLE will make channel x alternate between using CH_X_CONF and CH_{X+8}_CONF. The configuration used is decided by the state of the corresponding bit in SCANRES. For instance, if channel 3 is performing a scan and bit 3 in SCANRES is set, CH_{11}_CONF will be used. Channels 8 through 15 will toggle between CH_X_CONF and CH_{X-8}_CONF. This mode provides an easy way for implementation of hysteresis on channel events as threshold values can be changed depending on sensor status.

Setting SCANCONF to DECDEF will make the state of the decoder define which scan configuration to be used. If the decoder state is at index 16 or higher, channel x will use CH_{X+8}_CONF, otherwise it will use CH_X configuration. Similarly, channels 8 through 15 will use CH_X configuration when decoder state index is less than 8 and CH_{X-8}_CONF when decoder state index is higher than 7. Allowing the decoder state to define which configuration to use enables easy implementation of hysteresis, for example, as different threshold values can be used for the same channel dependent on the state of the application. Table 28.1 LESENSE Scan Configuration Selection on page 1104 summarizes how channel configuration is selected for different setting of SCANCONF.

Table 28.1. LESENSE Scan Configuration Selection

LESENSE channel x	SCANCONF					
	DIRMAP	INVMAP	TOGGLE		DECDEF	
			SCANRES[n] = 0	SCANRES[n] = 1	DECSTATE < 16	DECSTATE >= 16
0 <= x < 8	CH_x_CONF	CH_{x+8}_CONF	CH_x_CONF	CH_{x+8}_CONF	CH_x_CONF	CH_{x+8}_CONF
8 <= x < 16	CH_x_CONF	CH_{x-8}_CONF	CH_x_CONF	CH_{x-8}_CONF	CH_x_CONF	CH_{x-8}_CONF

Channels are enabled in the CHEN register, where bit x enables channel x. During a scan, all enabled channels are measured, starting with the lowest indexed channel.

28.3.3 Scan Sequence

The LESENSE peripheral clock (LESENSECLK) is a low-speed clock derived from the EM23GRPACLK from the CMU. LESENSECLK is the default used to clock most of the peripheral timing during operation. The high-frequency LESENSE peripheral clock (LESENSEHFCLK) selected in the CMU may also be dyamically used for faster timing of individual sensor measurements. The LESENSE register interface runs on the LSPCLK coming from the CMU to enable faster register access.

All enabled channels are scanned each scan period. A new scan is started according to the conditions set by CFG.SCANMODE. If set to PERIODIC, the scan frequency is generated using a counter which is clocked by LESENSECLK. This counter has its own prescaler. This prescaling factor is configured in the PCPRESC field of TIMCTRL. A new scan sequence is started each time the counter reaches the top value, TIMCTRL.PCTOP. The scan frequency is calculated using Figure 28.2 Scan frequency on page 1105. If SCANMODE is set to ONESHOT, a single scan will be made when START in CMD is set. To start a new scan on a PRS event, set SCANMODE to PRS and configure the LESENSE consumer register in the PRS module.

$$F_{scan} = LESENSECLK/((1 + PCTOP)*2^{PCPRESC})$$

Figure 28.2. Scan frequency

It is possible to interleave additional sensor measurements in between the periodic scans. Issuing a start command when LESENSE is idle will immediately start a new scan, without disrupting the frequency of the periodic scans. If the period counter overflows during the interleaved scan, the periodically scheduled scan will start immediately after the interleaved scan completes.

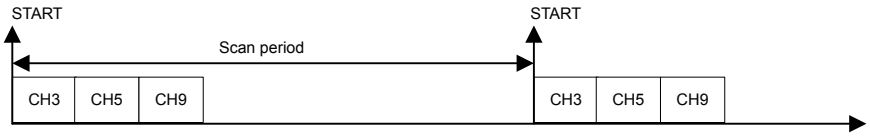


Figure 28.3. Scan Sequence

28.3.4 Sensor Timing

LESENSE includes a timer prescaler for each of the clock sources: A low frequency timer running on LESENSECLK, and a high frequency timer running on LESENSEHFCLK. The low frequency clock is prescaled by configuring LFPRESC in TIMCTRL, and the high frequency clock prescaling factor is configured in AUXPRESC in TIMCTRL. The prescaled versions of these clocks are used for channel sensor timing. A block diagram of the key controls for LESENSE clocking and timing is shown in Figure 28.4 LESENSE Clocking and Timing Control on page 1106.

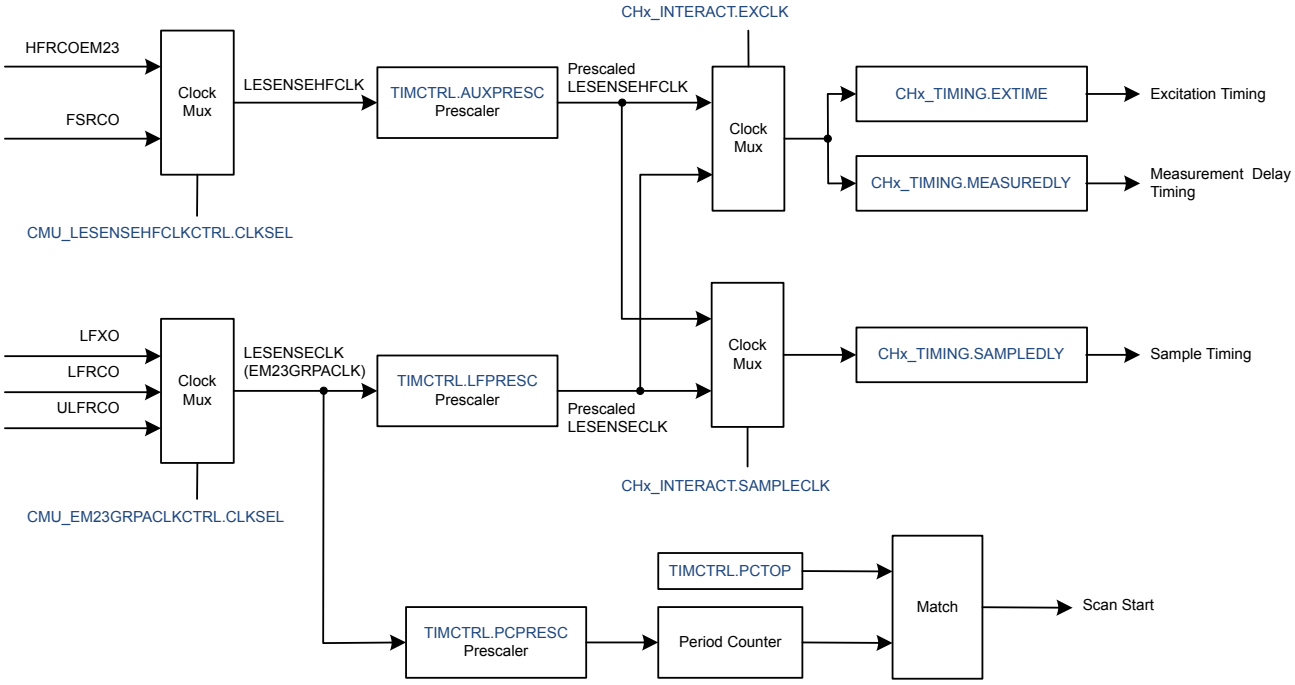


Figure 28.4. LESENSE Clocking and Timing Control

For each channel in the scan sequence, the LESENSE interface has three phases: the idle phase, the excite phase, and the measure phase. The durations of each phase are configured in the CHx_TIMING registers.

Timing of the excite and measure phases can be either a number of $LESENSEHFCLK_{prescaled}$ cycles or a number of $LESENSECLK_{prescaled}$ cycles, depending on which one is selected by the EXCLK field in CHx_INTERACT. Similarly, the sample phase is timed from the clock selected by the SAMPLECLK field in Chx_INTERACT.

The duration of the excite phase is programmed via EXTIME in the CHx_TIMING register. This sets how long the sensor excitation pulse will last.

The duration of the measurement phase is programmed via MEASUREDLY and SAMPLEDLY. The output of the ACMP will be ignored for MEASUREDLY EXCLK cycles after start of the sensor measurement. Sampling of the sensor will happen after SAMPLEDLY SAMPLECLK cycles. The configurable measure and sample delays enable LESENSE to easily define exact time windows for sensor measurements. A start delay can also be inserted before sensor measurement begins by configuring STARTDLY in TIMCTRL. This delay can be used to ensure that a VDAC conversion is complete and voltages have stabilized before sensor measurement begins. To reduce power consumption, the startup of HFRCOEM23/FSRCO (driving LESENSEHFCLK) can be delayed until the system enters the excite phase. This is done by configuring AUXSTARTUP in TIMCTRL to ONDEMAND. This will reduce the time the HFRCOEM23/FSRCO is enabled with the tradeoff that that the starting point for high frequency timing will also be delayed the required oscillator startup time.

Figure 28.5 Timing Diagram, LESENSEHFCLK Based Timing on page 1107 depicts a sensor sequence using $LESENSEHFCLK_{prescaled}$ based timing (EXTIME=6, MEASUREDLY=13, SAMPLEDLY=20), while Figure 28.6 Timing Diagram, LESENSECLK Based Timing on page 1107 depicts a sequence with $LESENSECLK_{prescaled}$ based timing (EXTIME=1, MEASUREDLY=2, SAMPLEDLY=3).

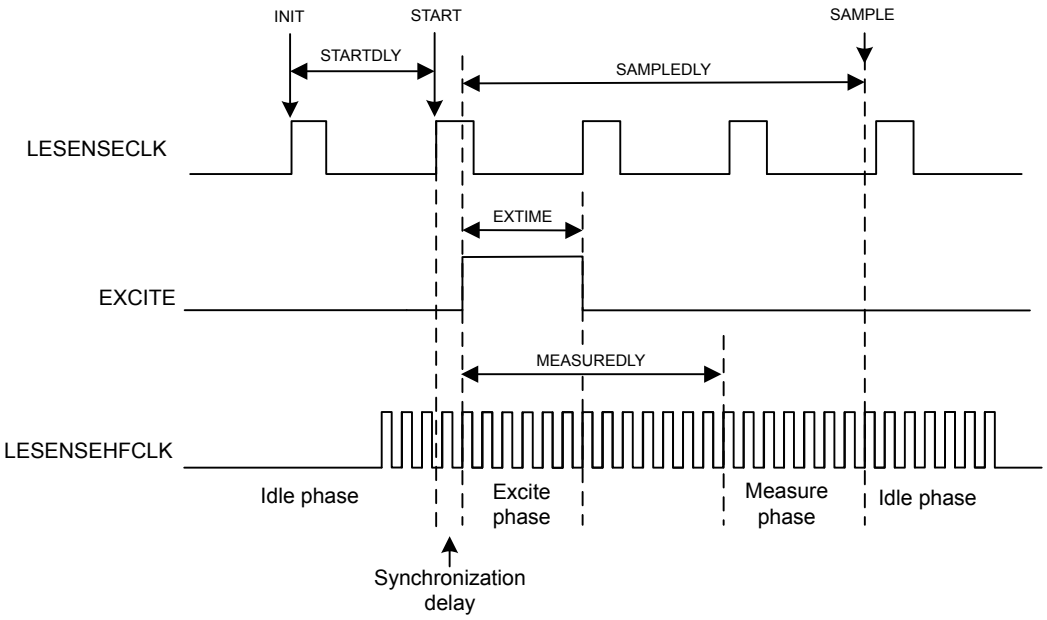


Figure 28.5. Timing Diagram, LESENSEHFCLK Based Timing

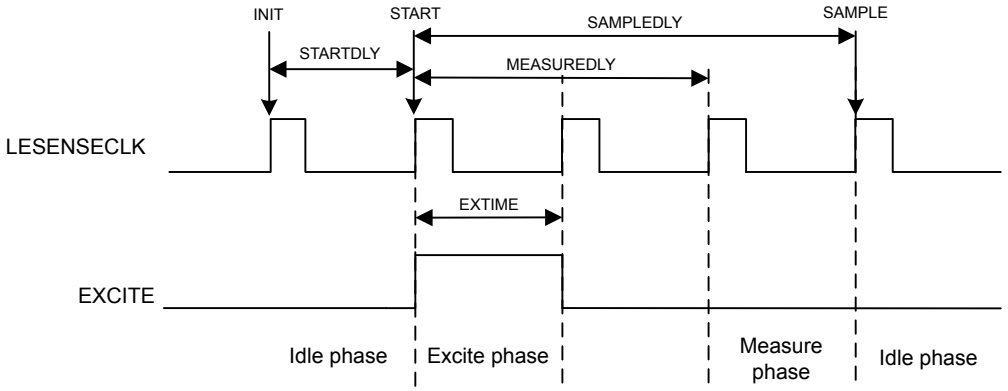


Figure 28.6. Timing Diagram, LESENSECLK Based Timing

28.3.5 Sensor Interaction

Many sensor types require some type of excitation in order to work. LESENSE can generate a variety of sensor stimuli, both on the same pin as the measurement is to be made on, and on alternative pins.

By default, excitation is performed on the LESENSE.CHxOUT signal associated with the channel number. These signals are routed to GPIO using DBUS (see 24.3.12.1 Digital Bus (DBUS)). The mode of the pin during the excitation phase is configured using EXMODE in CHx_INTERACT. The available modes during the excite phase are:

- DISABLED: The pin is disabled.
- HIGH: The pin is driven high.
- LOW: The pin is driven low.
- DACOUT: The pin is connected to the output of VDAC0 channel 0.

Note: Excitation with the VDAC0_CH0 output is only available on certain LESENSE channels, and the MAIN CH0 output is shorted to dedicated pins which may be different from the GPIO selected for the channel. LESENSE channels 0,1 and 2 can use VDAC excitation, and will drive the LESENSE.EN_0, LESENSE.EN_1, and LESENSE.EN_2 signals, respectively.

LESENSE is able to perform sensor excitation on one channel while measuring with another. When ALTEX in CHx_INTERACT is set, the excitation will occur on the alternative excite pin associated with the given channel. The alternative pin associated with LESENSE CH_X is LESENSE $CH_{X+8 \bmod 16}$. Table 28.2 LESENSE Excitation Pin Mapping on page 1108 shows the mapping of excitation and alternate excitation for every channel.

Table 28.2. LESENSE Excitation Pin Mapping

LESENSE channel	ALTEX = 0	ALTEX = 1
0	LESENSE.CH0OUT	LESENSE.CH8OUT
1	LESENSE.CH1OUT	LESENSE.CH9OUT
2	LESENSE.CH2OUT	LESENSE.CH10OUT
3	LESENSE.CH3OUT	LESENSE.CH11OUT
4	LESENSE.CH4OUT	LESENSE.CH12OUT
5	LESENSE.CH5OUT	LESENSE.CH13OUT
6	LESENSE.CH6OUT	LESENSE.CH14OUT
7	LESENSE.CH7OUT	LESENSE.CH15OUT
8	LESENSE.CH8OUT	LESENSE.CH0OUT
9	LESENSE.CH9OUT	LESENSE.CH1OUT
10	LESENSE.CH10OUT	LESENSE.CH2OUT
11	LESENSE.CH11OUT	LESENSE.CH3OUT
12	LESENSE.CH12OUT	LESENSE.CH4OUT
13	LESENSE.CH13OUT	LESENSE.CH5OUT
14	LESENSE.CH14OUT	LESENSE.CH6OUT
15	LESENSE.CH15OUT	LESENSE.CH7OUT

Figure 28.7 Pin Sequencing on page 1109 illustrates the sequencing of the pin associated with the active channel and its alternative excite pin.

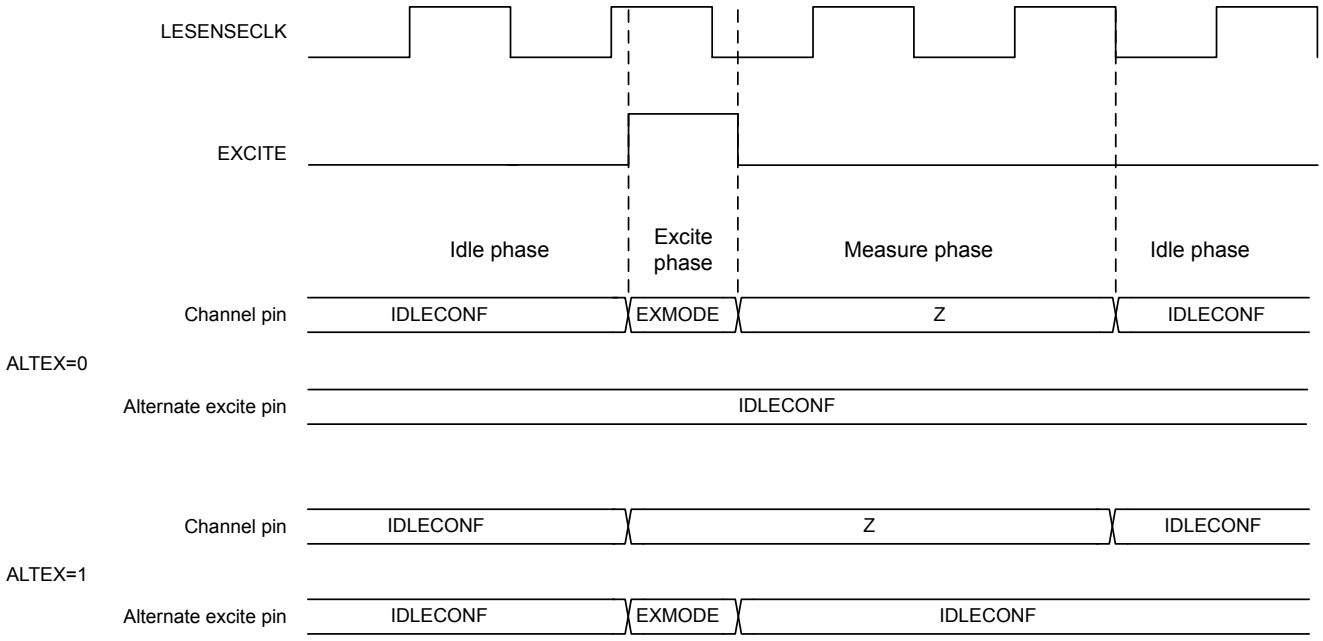


Figure 28.7. Pin Sequencing

Note: When exciting on the pin associated with the active channel, the pin will go through a tri-stated phase before returning to the idle configuration. This will not happen on pins used as alternative excitation pins.

The pin configuration for the idle phase can be configured individually for each LESENSE channel pin in the IDLECONF register. The modes available are the same as the modes available in the excitation phase. During the measure phase, the pin mode on the active channel is always disabled (analog input).

To enable LESENSE to control GPIO, the PORT:PIN have to programmed in the GPIO Route registers for each LESENSE channel being used. In addition, the given pin must be configured as push-pull.

28.3.6 Sensor Sampling

During the measurement phase, LESENSE can sample data from sensors using either the IADC0 or one of the ACMP modules (ACMP0 for LESENSE channels 0-7 and ACMP1 for LESENSE channels 8-15). This is configured in CHx_INTERACT.SAMPLE. Together with the configuration of these peripherals, the CHx_INTERACT.OFFSET field may be used to specify different pins to be sampled for each LESENSE channel (see 28.3.1 Interface Descriptions).

If ACMP is used, LESENSE can evaluate the ACMP output at a single point in time (CHx_INTERACT.SAMPLE = ACMP), or count pulses on the ACMP output (CHx_INTERACT.SAMPLE = ACMPCOUNT) for a programmable period of time.

LESENSE includes the possibility to sample both analog comparators simultaneously, effectively cutting the time spent on sensor interaction in some applications in half. Setting DUALSAMPLE in LESENSE.CFG enables this mode. In dual sample mode, channels X and X+8 are paired, meaning they will be sampled at the same time. Dualsample mode only works when CHx_INTERACT_SAMPLE is set to ACMP.

If the IADC is used, LESENSE will initiate IADC conversions and fetch the IADC data for further evaluation. If the IADC is configured for two's complement bi-polar output, CHx_INTERACT.SAMPLE must be set to ADCDIFF. In this mode, the output from the IADC and the threshold used for comparison will be interpreted as two's complement notation.

The sampled data from IADC or ACMP will be referred to as sensor data in the remainder of this manual.

28.3.7 Sensor Evaluation

When a measurement phase is completed, the sensor data is evaluated by the evaluation block. If the sensor data is taken from ACMP sample in a single point in time (CHx_INTERACT_SAMPLE = ACMP), the evaluation is limited to determening if the sensor data is 0 or 1. For the other sample modes, there are three ways to do sensor evaluation; threshold comparison, sliding window, or step detection. Evaluation mode is configured in CHx_EVALCFG.MODE.

If the evaluation of sensor data evaluates to true, the corresponding bit in the result register, SCANRES, is set. By configuring SETIF in CHx_INTERACT, interrupt flags can also be set on SCANRES events.

Figure 28.8 Scan Result and Interrupt Generation on page 1110 illustrates how the sensor data or ACMP sample is used for evaluation and interrupt generation.

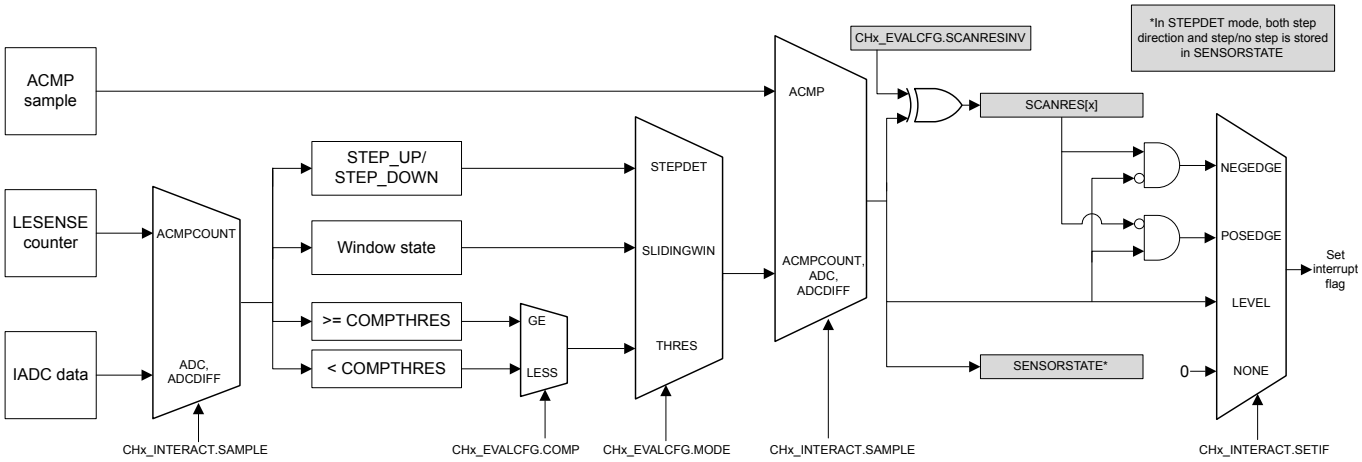


Figure 28.8. Scan Result and Interrupt Generation

The results from sensor data evaluation can be fed into the decoder through the SENSORSTATE register, by setting CHx_EVALCFG.DECODE. In DUALSAMPLE mode, results from both the sampled ACMPs will be stored in both SCANRES and SENSORSTATE (if enabled).

28.3.8 Threshold Comparison

In threshold comparison mode, the sensor data is compared to the threshold configured in CHx_EVALTHRES. There are two modes of threshold comparison; 'less than', and 'greater than or equal'. Threshold comparison mode is configured in CHx_EVALCFG.COMP.

28.3.9 Sliding Window

In sliding window mode, the sensor data is compared against the upper and lower limits of a window range. The window is defined by a base, given by CHx_EVALTHRES, and a size configured in EVALCTRL_WINSIZE. The window size is constant and the same for all LESENSE channels, while the base is specific to each channel and will be updated by LESENSE when the sensor data is outside the current window range. If the sensor data is within the window range, the sensor evaluation will remain the same as it was for the previous measurement. If the sensor data is below the window range, the measurement will evaluate as false. If the sensor data is above the window range, the measurement will evaluate as true. In both cases, the window base in CHx_EVALTHRES will be updated to reflect the new window range. Figure 28.9 Sliding Window on page 1111 shows how the sliding window evaluation mode can be used to implement a system with two self calibrating thresholds.

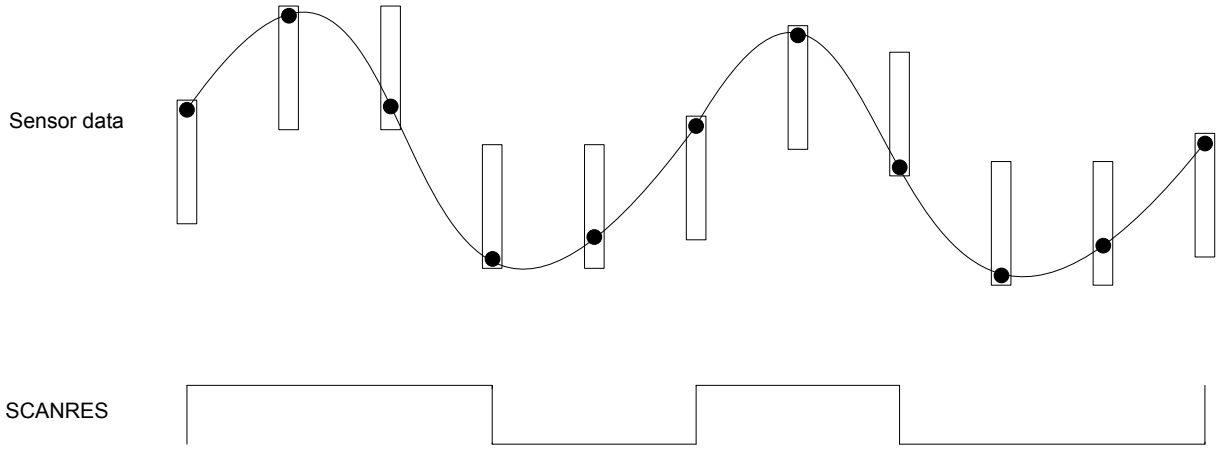


Figure 28.9. Sliding Window

28.3.10 Step Detection

Step detection is used to detect steps in the sensor data compared to sensor data from the previous measurement. The size of the step is configured in EVALCTRL_WINSIZE. In this mode, step up and step down are evaluated as described in Figure 28.10 Step detection on page 1111:

$$STEP\_UP = SENSORDATA_i >= SENSORDATA_{i-1} + EVALCTRL\_WINSIZE$$

$$STEP\_DOWN = SENSORDATA_i < SENSORDATA_{i-1} - EVALCTRL\_WINSIZE$$

Figure 28.10. Step detection

If either a step up or a step down is detected, the SCANRES bit for the active channel will be set. In addition, the STEPDIR bit for the channel will be updated to indicate if a step up or a step down was detected. STEPDIR = 1 indicates a step up. In this mode, previous sensor data is stored in CHx_EVALTHRES.

28.3.11 Decoder

Many applications require some sort of processing of the sensor readings, for instance in the case of quadrature decoding. In quadrature decoding, the sensors repeatedly pass through a set of states which correspond to the position of the sensors. This sequence, and many other decoding schemes, can be described as a finite state machine. To support this type of decoding without CPU intervention, LESENSE includes a highly configurable decoder, capable of decoding input from up to four sensors. The decoder is implemented as a programmable state machine with up to 64 arcs which can represent transitions between up to 32 states. When doing a sensor scan, the results from the sensors are placed in the decoder input register, SENSORSTATE, if DECODE in CHx_INTERACT is set, as depicted in Figure 28.11 Sensor Scan and Decode Sequence on page 1112.

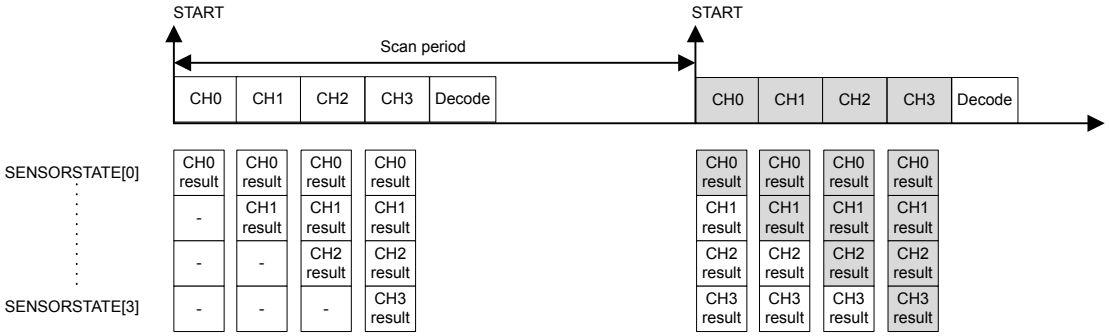


Figure 28.11. Sensor Scan and Decode Sequence

The current state is indicated by the DECSTATE register. At the end of a scan sequence, the decoder evaluates the results placed in SENSORSTATE against the defined STx_ARC registers and the current state. The decoder evaluates all the ARCs together in parallel and uses one LESENSECLK cycle to determine the next state.

The transition criteria is established by CURRSTATE, SMASK, and SCOMP in the STx_ARC registers. SMASK defines which bits of SENSORSTATE to mask (ignore). A '0' in SMASK means that the corresponding bit in SENSORSTATE is evaluated, while a '1' in SMASK means that bit will be masked. If STx_ARC.CURRSTATE == DECSTATE, and the non-masked bits in SENSORSTATE are equal to those defined in SCOMP, then the transition criteria evaluates to True, and the state machine transitions to the value specified by STxARC.NEXTSTATE.

It is possible that multiple ARCs will match the transition criteria. In this case, the lowest numbered ARC that meets the transition criteria determines the next state.

Note: When using the decoder, it is important that at least one ARC be configured for the initial state (CURRSTATE == 0), and that the ARCs be configured to not produce any dead states (a state which is the NEXTSTATE of an ARC but is not the CURRSTATE of any other ARC). Doing otherwise will result in the possibility of the decoder getting stuck where no further state transitions are possible. If this happens, a software reset of the LESENSE block would need to be performed.

Upon a state transition, LESENSE can generate a pulse on one or more of the decoder PRS producers. Which producers to generate a pulse on is configured in the PRSACT bit field. If PRSCNT in DECCTRL is set, count signals will be generated on decoder PRS producers 0 and 1 according to the PRSACT configuration. In this mode, producer 0 will pulse each time a count event occurs while producer 1 indicates the count direction (1 for up and 0 for down). The count direction will be kept at its previous state in between count events. The pulse counter on the chip may be used to keep track of events by listening to these PRS outputs. For this the PRS needs to be programmed to configure the producer of the channel(s) from the LESENSE decoder and those same channel(s) are consumed by the PCNT module.

Table 28.3. LESENSE Decoder PRS Outputs (DECCTRL.PRSCNT = 0)

PRSACT Value	Description
0	No PRS output generated
1	Pulse generated on LESENSE PRS output 0
2	Pulse generated on LESENSE PRS output 1
3	Pulse generated on LESENSE PRS output 0 and 1

PRSACT Value	Description
4	Pulse generated on LESENSE PRS output 2
5	Pulse generated on LESENSE PRS output 0 and 2
6	Pulse generated on LESENSE PRS output 1 and 2
7	Pulse generated on LESENSE PRS output 0 , 1 and 2

Table 28.4. LESENSE Decoder PRS Outputs (DECCTRL.PRSCNT = 1)

PRSACT Value	Description
0	No Count Outputs
1	Count Up
2	Count Down
4	Pulse generated on LESENSE PRS output 2
5	Count Up and Pulse generated on LESENSE PRS output 2
6	Count Down and Pulse generated on LESENSE PRS output 2

The DECODER has a PRS producer named DECCMP. This output can be used to indicate which state, or subset for states, the decoder is currently in. This PRS output is enabled by setting DECCMPEN in PRSCTRL, and configured through DECCMPMASK and DECCMPVAL in PRSCTRL. The value of this PRS output is given by Figure 28.12 DECCMP PRS output on page 1113,

PRS_DECCMP = (DECSTATE & ~DECCMPMASK) = (DECCMPVAL & ~DECCMPMASK)

Figure 28.12. DECCMP PRS output

If SETIF is set, the DECODER interrupt flag will be set when the transition occurs. If INTMAP in DECCTRL and SETIF is set, a transition from state x and x+16 will set the CHx interrupt flag in addition to the DECODER flag.

To prevent unnecessary interrupt requests or PRS outputs when the decoder toggles back and forth between two states, a hysteresis option is available. The hysteresis function is triggered if a transition from STATE A to STATE B is preceded by a transition from STATE B to STATE A, and vice-versa. Figure 28.13 Decoder Hysteresis on page 1114 illustrates how the hysteresis triggers upon state transitions.

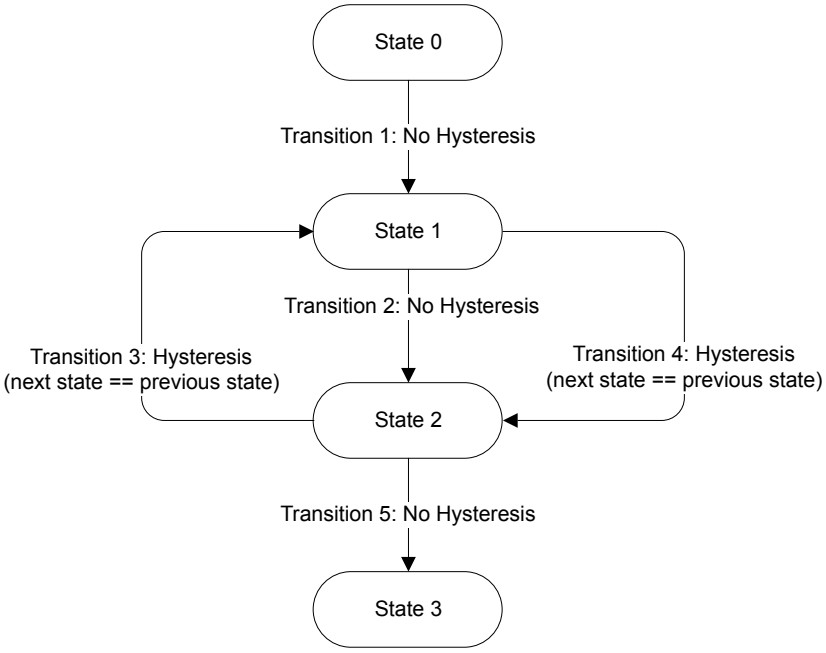


Figure 28.13. Decoder Hysteresis

- When HYSTPRSx is set, PRS signal x is suppressed when the hysteresis triggers.
- When HYSTIRQ is set, interrupt requests are suppressed when the hysteresis triggers.

28.3.12 Measurement Results

LESENSE has a FIFO for storage of up to 16 results from sensor measurements. Each time LESENSE writes data to the result buffer, the result count, RESCOUNT, is incremented. Each time a new result is read through the RESFIFO register, the result count, RESCOUNT, is decremented. The result count will not be decremented if there is no valid, unread data in the result buffer.

Note: The 20-bit wide RESFIFO.BUFDATASRC bitfield contains both the LESENSE result (least-significant 16 bits) as well as the LESENSE channel index (most-significant 4 bits)

LESENSE has a FIFO for storage of up to 16 results from sensor measurements. Each time LESENSE writes data to the result buffer, the result count, RESCOUNT, is incremented. Each time a new result is read through the RESFIFO register, the result count, RESCOUNT, is decremented. The result count will not be decremented if there is no valid, unread data in the result buffer.

LESENSE will not write additional data to a full result buffer and will flag a FIFO overflow in the STATUS register which can also generate an interrupt. Reading the FIFO involves synchronization of the pointers from the read (APB) to the write domain (LF) which will result in STATUS.READBUSY being high. The user should wait for the READBUSY to go low before disabling the LESENSE clock in the CMU. The FIFO read will be non-blocking. By writing the CLEARBUF field, the user can flush the FIFO. When the FIFO is flushing the FLUSHING bit in the STATUS register will be high. It is recommended that the user not flush the FIFO when the scan is running because a FIFO write during FLUSHING may be flushed as well. The APB bus is not stalled during a FLUSH. FLUSHING will also involve pointer synchronization so READBUSY can be high during and after FLUSHING. The FIFO will generate interrupt flags(RESWFIF) when the RESCOUNT reaches the CFG.RESFIDL.

During a scan, the state of each sensor is stored in SCANRES. If a sensor triggers, a 1 is stored in SCANRES, otherwise a 0 is stored in SCANRES. Whether or not a sensor is said to be triggered depends of the configuration for the given channel, and the sensor evaluation mode.

If SAMPLE is set to ACMP, the sensor is said to be triggered if the output from the analog comparator is 1 when sensor sampling is performed. If SAMPLE is set to ACMPCOUNT, a sensor is said to be triggered if the LESENSE counter value is greater than or equal, or less than CHx_EVALTHRES, depending on the configuration of COMP. If STRSAMPLE in CHx_EVALCFG is set, the sensor measurement (ACMP sample, IADC sample, or counter value) for the channel will be stored in the result FIFO. If STRSCANRES in CFG is set, the result vector, SCANRES, will also be stored in the result buffer. This will be stored after each scan and will be interleaved with any stored sensor measurements.

28.3.13 DMA Requests

LESENSE issues a DMA request when the RESCOUNT reaches CFG.RESFIDL, this request is cleared when the buffer level drops below the threshold. A single DMA request is also set whenever there is unread data in the buffer. CFG.DMAWU controls if the LESENSE can send a request for a wakeup from EM2 to transfer data once the RESCOUNT reaches CFG.RESFIDL.

The DMA controller shall read the RESFIFO register.

28.3.14 PRS

LESENSE is an asynchronous PRS producer and consumer. For LESENSE as a PRS consumer, other PRS producers can start a LESENSE scan. From a producer standpoint, LESENSE generates PRS signals from the programmable FSM which can be used by the PRS consumers.

28.4 Programmer's Model

The following steps show how to configure LESENSE to scan through 4 buttons 100 times per second, issuing an interrupt if one of them is pressed.

1. Assuming $PERCLK_{LESENSE}$ is 32kHz, set PCPRESC to 3 and PCTOP to 39 in PERCTRL. This will make the scan frequency to 100 Hz.
2. Enable channels 0 through 3 in CHEN and IDLECONF for these channels to DISABLED. The GPIO for these channels will need to configured in the GPIO peripheral.
3. Configure and enable the ACMP.
4. Configure the following bit fields in CHx_CONF for channel 0 through 3
   a. Set EXTIME to 0. No excitation is needed in this mode.
   b. Set SAMPLE to ACMPCOUNT and COMP to LESS. This makes LESENSE interpret a sensor as active if the frequency of the channel drops below the threshold, i.e. the button is pressed.
   c. set SAMPLEDLY to an appropriate value, each sensor will be measured for SAMPLEDLY / $PERCLK_{LESENSE}$ seconds. MEASUREDLY should be set to 0.
5. Enable Interrupts on Channels 0 through 3.
6. Configure EVALTHRES for Channels 0 to 3. An interrupt will be issued if the counter value for a sensor is below EVALTHRES for the channel after the mesurement phase.
7. Enable LESENSE by writing EN to 1.
8. Start scan sequence by writing 1 to START in CMD.
9. To store the results of the enabled channels into the LESENSE FIFO configure STRSAMPLE for these channels as 1. STRSAMPLE is in a CONFIG register so it should be configured before enabling LESENSE.
10. To configure channels to be used by the decoder set DECODE in CHx_EVALCFG.Assume that we have set DECODE for channels 0 to 3.
11. The decoder will be called to act upon the SENSORSTATE at the end of the scan. In this case it will be after channel 3 is measured and evaluated.
12. To setup the decoder FSM configure the STn_ARC registers before enabling the LESENSE.The reset value for the DECSTATE is 0 so there should be atleast one STn_ARC with the current state as 0 otherwise no matter what the SENSORSTATE is there won't be a state transition. For the same reason there should not be any dead states (a state which is a NEXTSTATE of an ARC but is not the CURRENTSTATE of any ARC) while configuring the FSM else the decoder will be stuck there and the USER will need to perform a SWRST.

28.5 LESENSE Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	LESENSE_IPVERSION	R	IPVERSION
0x004	LESENSE_EN	RW ENABLE	Enable
0x008	LESENSE_SWRST	RW SWRST	Software Reset Register
0x00C	LESENSE_CFG	RW CONFIG	Configuration
0x010	LESENSE_TIMCTRL	RW CONFIG	Timing Control
0x014	LESENSE_PERCTRL	RW CONFIG	Peripheral Control
0x018	LESENSE_DECCTRL	RW	Decoder Control
0x01C	LESENSE_EVALCTRL	RW CONFIG	LESENSE Evaluation
0x020	LESENSE_PRSCTRL	RW	PRS Control
0x024	LESENSE_CMD	W LFSYNC	Command
0x028	LESENSE_CHEN	RW	Channel Enable
0x02C	LESENSE_SCANRES	RH	Scan Result
0x030	LESENSE_STATUS	RH	Status
0x034	LESENSE_RESCOUNT	RH	Result FIFO Count
0x038	LESENSE_RESFIFO	RH	Result Fifo
0x03C	LESENSE_CURCH	RH	Current Channel Index
0x040	LESENSE_DECSTATE	RH	Current Decoder State
0x044	LESENSE_SENSORSTATE	RH	Sensor State
0x048	LESENSE_IDLECONF	RW CONFIG	IDLE Configuration
0x050	LESENSE_SYNCBUSY	RH	Synchronization
0x060	LESENSE_IF	RWH INTFLAG	Interrupt Flags
0x064	LESENSE_IEN	RW	Interrupt Enables
0x100	LESENSE_CHx_TIMING	RW CONFIG	Scan Configuration
0x104	LESENSE_CHx_INTERACT	RW CONFIG	Scan Configuration
0x108	LESENSE_CHx_EVALCFG	RW CONFIG	Scan Configuration
0x10C	LESENSE_CHx_EVALTHRES	RWH LFSYNC	Scan Confguration
0x200	LESENSE_STx_ARC	RW CONFIG	State Transition Arc
0x1000	LESENSE_IPVERSION_SET	R	IPVERSION
0x1004	LESENSE_EN_SET	RW ENABLE	Enable
0x1008	LESENSE_SWRST_SET	RW SWRST	Software Reset Register
0x100C	LESENSE_CFG_SET	RW CONFIG	Configuration
0x1010	LESENSE_TIMCTRL_SET	RW CONFIG	Timing Control
0x1014	LESENSE_PERCTRL_SET	RW CONFIG	Peripheral Control
0x1018	LESENSE_DECCTRL_SET	RW	Decoder Control
0x101C	LESENSE_EVALCTRL_SET	RW CONFIG	LESENSE Evaluation

Offset	Name	Type	Description
0x1020	LESENSE_PRSCTRL_SET	RW	PRS Control
0x1024	LESENSE_CMD_SET	W LFSYNC	Command
0x1028	LESENSE_CHEN_SET	RW	Channel Enable
0x102C	LESENSE_SCANRES_SET	RH	Scan Result
0x1030	LESENSE_STATUS_SET	RH	Status
0x1034	LESENSE_RESCOUNT_SET	RH	Result FIFO Count
0x1038	LESENSE_RESFIFO_SET	RH	Result Fifo
0x103C	LESENSE_CURCH_SET	RH	Current Channel Index
0x1040	LESENSE_DECSTATE_SET	RH	Current Decoder State
0x1044	LESENSE_SENSOR-STATE_SET	RH	Sensor State
0x1048	LESENSE_IDLECONF_SET	RW CONFIG	IDLE Configuration
0x1050	LESENSE_SYNCBUSY_SET	RH	Synchronization
0x1060	LESENSE_IF_SET	RWH INTFLAG	Interrupt Flags
0x1064	LESENSE_IEN_SET	RW	Interrupt Enables
0x1100	LESENSE_CHx_TIMING_SET	RW CONFIG	Scan Configuration
0x1104	LESENSE_CHx_INTER-ACT_SET	RW CONFIG	Scan Configuration
0x1108	LESENSE_CHx_EVALCFG_SET	RW CONFIG	Scan Configuration
0x110C	LESENSE_CHx_EVAL-THRES_SET	RWH LFSYNC	Scan Confguration
0x1200	LESENSE_STx_ARC_SET	RW CONFIG	State Transition Arc
0x2000	LESENSE_IPVERSION_CLR	R	IPVERSION
0x2004	LESENSE_EN_CLR	RW ENABLE	Enable
0x2008	LESENSE_SWRST_CLR	RW SWRST	Software Reset Register
0x200C	LESENSE_CFG_CLR	RW CONFIG	Configuration
0x2010	LESENSE_TIMCTRL_CLR	RW CONFIG	Timing Control
0x2014	LESENSE_PERCTRL_CLR	RW CONFIG	Peripheral Control
0x2018	LESENSE_DECCTRL_CLR	RW	Decoder Control
0x201C	LESENSE_EVALCTRL_CLR	RW CONFIG	LESENSE Evaluation
0x2020	LESENSE_PRSCTRL_CLR	RW	PRS Control
0x2024	LESENSE_CMD_CLR	W LFSYNC	Command
0x2028	LESENSE_CHEN_CLR	RW	Channel Enable
0x202C	LESENSE_SCANRES_CLR	RH	Scan Result
0x2030	LESENSE_STATUS_CLR	RH	Status
0x2034	LESENSE_RESCOUNT_CLR	RH	Result FIFO Count
0x2038	LESENSE_RESFIFO_CLR	RH	Result Fifo
0x203C	LESENSE_CURCH_CLR	RH	Current Channel Index

Offset	Name	Type	Description
0x2040	LESENSE_DECSTATE_CLR	RH	Current Decoder State
0x2044	LESENSE_SENSOR-STATE_CLR	RH	Sensor State
0x2048	LESENSE_IDLECONF_CLR	RW CONFIG	IDLE Configuration
0x2050	LESENSE_SYNCBUSY_CLR	RH	Synchronization
0x2060	LESENSE_IF_CLR	RWH INTFLAG	Interrupt Flags
0x2064	LESENSE_IEN_CLR	RW	Interrupt Enables
0x2100	LESENSE_CHx_TIMING_CLR	RW CONFIG	Scan Configuration
0x2104	LESENSE_CHx_INTER-ACT_CLR	RW CONFIG	Scan Configuration
0x2108	LESENSE_CHx_EVALCFG_CLR	RW CONFIG	Scan Configuration
0x210C	LESENSE_CHx_EVAL-THRES_CLR	RWH LFSYNC	Scan Confguration
0x2200	LESENSE_STx_ARC_CLR	RW CONFIG	State Transition Arc
0x3000	LESENSE_IPVERSION_TGL	R	IPVERSION
0x3004	LESENSE_EN_TGL	RW ENABLE	Enable
0x3008	LESENSE_SWRST_TGL	RW SWRST	Software Reset Register
0x300C	LESENSE_CFG_TGL	RW CONFIG	Configuration
0x3010	LESENSE_TIMCTRL_TGL	RW CONFIG	Timing Control
0x3014	LESENSE_PERCTRL_TGL	RW CONFIG	Peripheral Control
0x3018	LESENSE_DECCTRL_TGL	RW	Decoder Control
0x301C	LESENSE_EVALCTRL_TGL	RW CONFIG	LESENSE Evaluation
0x3020	LESENSE_PRSCTRL_TGL	RW	PRS Control
0x3024	LESENSE_CMD_TGL	W LFSYNC	Command
0x3028	LESENSE_CHEN_TGL	RW	Channel Enable
0x302C	LESENSE_SCANRES_TGL	RH	Scan Result
0x3030	LESENSE_STATUS_TGL	RH	Status
0x3034	LESENSE_RESCOUNT_TGL	RH	Result FIFO Count
0x3038	LESENSE_RESFIFO_TGL	RH	Result Fifo
0x303C	LESENSE_CURCH_TGL	RH	Current Channel Index
0x3040	LESENSE_DECSTATE_TGL	RH	Current Decoder State
0x3044	LESENSE_SENSOR-STATE_TGL	RH	Sensor State
0x3048	LESENSE_IDLECONF_TGL	RW CONFIG	IDLE Configuration
0x3050	LESENSE_SYNCBUSY_TGL	RH	Synchronization
0x3060	LESENSE_IF_TGL	RWH INTFLAG	Interrupt Flags
0x3064	LESENSE_IEN_TGL	RW	Interrupt Enables
0x3100	LESENSE_CHx_TIMING_TGL	RW CONFIG	Scan Configuration

Offset	Name	Type	Description
0x3104	LESENSE_CHx_INTERACT_TGL	RW CONFIG	Scan Configuration
0x3108	LESENSE_CHx_EVALCFG_TGL	RW CONFIG	Scan Configuration
0x310C	LESENSE_CHx_EVALTHRES_TGL	RWH LFSYNC	Scan Confguration
0x3200	LESENSE_STx_ARC_TGL	RW CONFIG	State Transition Arc

28.6 LESENSE Register Description

28.6.1 LESENSE_IPVERSION - IPVERSION

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x1																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x1	R	**IPVERSION**
	IPVERSION			

28.6.2 LESENSE_EN - Enable

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	RW
Name																															DISABLING	EN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DISABLING	0x0	R	**Disabling**
	Module is in disabling			
0	EN	0x0	RW	**Enable**
	Global Enable of LESENSE functions			

Value	Mode	Description
0	DISABLE	Disable
1	ENABLE	Enable

28.6.3 LESENSE_SWRST - Software Reset Register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	W
Name																															RESETTING	SWRST

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	RESETTING	0x0	R	**Software reset busy status**
	Module is undergoing SWRST			
0	SWRST	0x0	W	**Software reset command**
	Trigger SWRST			

28.6.4 LESENSE_CFG - Configuration

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset															0x0						0x0				0x0	0x0	0x0		0x0		0x0	
Access															RW						RW				RW	RW	RW		RW		RW	
Name															DEBUGRUN						RESFIDL				DMAWU	STRSCANRES	DUALSAMPLE		SCANCONF		SCANMODE	

Bit	Name	Reset	Access	Description
31:18	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
17	DEBUGRUN	0x0	RW	**Debug Mode Run Enable**
	Set to keep LESENSE running in debug mode.			
	Value	Mode		Description
	0	X0		LESENSE can not start new scans in debug mode
	1	X1		LESENSE can start new scans in debug mode
16:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:8	RESFIDL	0x0	RW	**Result FIFO level**
	Result FIFO interrupt and DMA trigger level			
7	DMAWU	0x0	RW	**DMA wake-up from EM2**
	When set, DMA can wake and collect information based on FIFO levels			
	Value	Mode		Description
	0	DISABLE		No DMA wake-up from EM2
	1	ENABLE		DMA wake-up from EM2 when FIFO count is greater or equal to RESFIDL
6	STRSCANRES	0x0	RW	**Enable storing of SCANRES**
	When set, SCANRES will be stored in the result buffer after each scan			
5	DUALSAMPLE	0x0	RW	**Enable dual sample mode**
	When set, both ACMPs will be sampled simultaneously.			
4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:2	SCANCONF	0x0	RW	**Select scan configuration**
	These bits control which CHx_CONF registers to be used.			
	Value	Mode		Description

Bit	Name	Reset	Access	Description
	0	DIRMAP		The channel configuration register registers used are directly mapped to the channel number.
	1	INVMAP		The channel configuration registers used are CH[X+8]_CONF for channels 0-7 and CH[X-8]_CONF for channels 8-15.
	2	TOGGLE		The channel configuration registers used toggle between CH[X]_CONF and CH[X+8]_CONF when channel x triggers
	3	DECDEF		The decoder state defines the CONF registers to be used.
1:0	SCANMODE	0x0	RW	**Configure scan mode**

These bits control how the scan frequency is decided

Value	Mode	Description
0	PERIODIC	A new scan is started each time the period counter overflows
1	ONESHOT	A single scan is performed when START in CMD is set
2	PRS	Pulse on PRS channel

28.6.5 LESENSE_TIMCTRL - Timing Control

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset				0x0					0x0				0x0									0x0				0x0					0x0	
Access				RW					RW				RW									RW				RW					RW	
Name				AUXSTARTUP					STARTDLY				PCTOP									PCPRESC				LFPRESC					AUXPRESC	

Bit	Name	Reset	Access	Description
31:29	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
28	AUXSTARTUP	0x0	RW	**AUX startup config**

Value	Mode	Description
0	PREDEMAND	Request oscillator .5 LESENSECLK cycle before sensing starts
1	ONDEMAND	Request oscillator at sensing time

27:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:22	STARTDLY	0x0	RW	**Start delay configuration**
	Delay sensor interaction STARTDELAY LESENSECLK cycles for each channel			
21:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:12	PCTOP	0x0	RW	**Period counter top value**
	Top value for the period counter			
11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10:8	PCPRESC	0x0	RW	**Period counter prescaling**
	Prescaling factor for period counter used for scan interval			

Value	Mode	Description
0	DIV1	The period counter clock frequency is LESENSECLK/1
1	DIV2	The period counter clock frequency is LESENSECLK/2
2	DIV4	The period counter clock frequency is LESENSECLK/4
3	DIV8	The period counter clock frequency is LESENSECLK/8
4	DIV16	The period counter clock frequency is LESENSECLK/16
5	DIV32	The period counter clock frequency is LESENSECLK/32
6	DIV64	The period counter clock frequency is LESENSECLK/64
7	DIV128	The period counter clock frequency is LESENSECLK/128

Bit	Name	Reset	Access	Description
7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:4	LFPRESC	0x0	RW	**Prescaling factor for low frequency time**

Prescaling factor for low frequency timer used for Sensor timing

Value	Mode	Description
0	DIV1	Low frequency timer is clocked with LESENSECLK/1
1	DIV2	Low frequency timer is clocked with LESENSECLK/2
2	DIV4	Low frequency timer is clocked with LESENSECLK/4
3	DIV8	Low frequency timer is clocked with LESENSECLK/8
4	DIV16	Low frequency timer is clocked with LESENSECLK/16
5	DIV32	Low frequency timer is clocked with LESENSECLK/32
6	DIV64	Low frequency timer is clocked with LESENSECLK/64
7	DIV128	Low frequency timer is clocked with LESENSECLK/128

3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	AUXPRESC	0x0	RW	**Prescaling factor for high frequency tim**

Prescaling factor for high frequency timer used for Senosr timing

Value	Mode	Description
0	DIV1	High frequency timer is clocked at LESENSEHFCLK/1
1	DIV2	High frequency timer is clocked at LESENSEHFCLK/2
2	DIV4	High frequency timer is clocked at LESENSEHFCLK/4
3	DIV8	High frequency timer is clocked at LESENSEHFCLK/8

28.6.6 LESENSE_PERCTRL - Peripheral Control

Offset	Bit Position																														
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset							0x0	0x0		0x0		0x0												0x0		0x0				0x0		
Access							RW	RW		RW		RW												RW		RW				RW		
Name							ACMP1INV	ACMP0INV		ACMP1MODE		ACMP0MODE												DACCONVTRIG		DACSTARTUP				DACCH0DATA		

Bit	Name	Reset	Access	Description
31:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25	ACMP1INV	0x0	RW	**Invert analog comparator 1 output**
	Bit to invert the ACMP1 output before using it within LESENSE			
24	ACMP0INV	0x0	RW	**Invert analog comparator 0 output**
	Bit to invert the the ACMP0 output before using it within LESENSE			
23	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
22	ACMP1MODE	0x0	RW	**ACMP1 mode**
	Configure how LESENSE controls ACMP1			

Value	Mode	Description
0	MUX	LESENSE controls the POSSEL of ACMP1
1	MUXTHRES	LESENSE POSSEL and reference divider of ACMP1

Bit	Name	Reset	Access	Description
21	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
20	ACMP0MODE	0x0	RW	**ACMP0 mode**
	Configure how LESENSE controls ACMP0			

Value	Mode	Description
0	MUX	LESENSE controls POSSEL of ACMP0
1	MUXTHRES	LESENSE controls POSSEL and reference divider of ACMP0

Bit	Name	Reset	Access	Description
19:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8	DACCONVTRIG	0x0	RW	**DAC conversion trigger configuration**
	Decides if the DAC is triggerd before every channel measurement or once per scan			

Value	Mode	Description
0	CHANNELSTART	DAC is enabled before every LESENSE channle measurement.
1	SCANSTART	DAC is only enabled once per scan.

Bit	Name	Reset	Access	Description
7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6	DACSTARTUP	0x0	RW	**DAC startup configuration**

Decides if the DAC is triggered 0.5 or 1 LESENSECLK cycle before START

Value	Mode	Description
0	FULLCYCLE	DAC is started a full LESENSECLK before sensor interaction starts.
1	HALFCYCLE	DAC is started half a LESENSECLK cycle before sensor interaction starts.

5:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	DACCH0DATA	0x0	RW	**DAC CH0 data selection.**

Setting this bit will override the data the DAC uses for conversion

Value	Mode	Description
0	DACDATA	DAC data is defined by CH0DATA in the DAC interface.
1	THRES	DAC data is defined by THRES in CHx_INTERACT.

1:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

28.6.7 LESENSE_DECCTRL - Decoder Control

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0	0x0	0x0	0x0	0x0	0x0		0x0
Access																									RW	RW	RW	RW	RW	RW		RW
Name																									PRSCNT	HYSTIRQ	HYSTPRS2	HYSTPRS1	HYSTPRS0	INTMAP		DECDIS

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7	PRSCNT	0x0	RW	**Enable count mode on decoder PRS channel**
	When set, decoder PRS0 and PRS1 will be used to produce output which can be used by a PCNT to count up or down.			
6	HYSTIRQ	0x0	RW	**Enable decoder hysteresis on interrupt r**
	When set, hysteresis is enabled in the decoder, suppressing interrupt requests.			
5	HYSTPRS2	0x0	RW	**Enable decoder hysteresis on PRS2 output**
	When set, hysteresis is enabled in the decoder, suppressing changes on PRS channel 2			
4	HYSTPRS1	0x0	RW	**Enable decoder hysteresis on PRS1 output**
	When set, hysteresis is enabled in the decoder, suppressing changes on PRS channel 1			
3	HYSTPRS0	0x0	RW	**Enable decoder hysteresis on PRS0 output**
	When set, hysteresis is enabled in the decoder, suppressing changes on PRS channel 0			
2	INTMAP	0x0	RW	**Enable decoder to channel interrupt map**
	When set, a transition from state x in the decoder will set interrupt flag CH[x mod 16]			
1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	DECDIS	0x0	RW	**Disable the decoder**
	When set, the decoder is disabled. When disabled the decoder will keep its current state			

28.6.8 LESENSE_EVALCTRL - LESENSE Evaluation

Offset	Bit Position																															
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	RW															
Name																	WINSIZE															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	WINSIZE	0x0	RW	**Sliding window and step detection size**
	In sliding window mode, this bit-field configures the window size. In step detection mode, this bit-field is used to configure the threshold for step detection			

28.6.9 LESENSE_PRSCTRL - PRS Control

Offset	Bit Position																															
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																0x0						0x0								0x0		
Access																RW						RW								RW		
Name																DECCMPEN						DECCMPMASK								DECCMPVAL		

Bit	Name	Reset	Access	Description
31:17	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
16	DECCMPEN	0x0	RW	**Enable PRS output DECCMP**
	Enables decoder state compare match PRS output			
15:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12:8	DECCMPMASK	0x0	RW	**Decoder state compare value mask**
	Masks COMPVAL and DECSTATE for comparison			
7:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4:0	DECCMPVAL	0x0	RW	**Decoder state compare value**
	Triggers prs output when equal to DECSTATE			

28.6.10 LESENSE_CMD - Command

Offset	Bit Position																													
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0	0x0	0x0	0x0
Access																													W(nB)	W(nB)	W(nB)	W(nB)
Name																													CLEARBUF	DECODE	STOP	START

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	CLEARBUF	0x0	W(nB)	**Clear result buffer**
2	DECODE	0x0	W(nB)	**Start decoder**
1	STOP	0x0	W(nB)	**Stop scanning of sensors** If issued during a scan, the command will take effect after scan completion.
0	START	0x0	W(nB)	**Start scanning of sensors.**

28.6.11 LESENSE_CHEN - Channel Enable

Offset	Bit Position																													
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	RW															
Name																	CHEN															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	CHEN	0x0	RW	**Enable scan channel** Set bit X to enable channel X

28.6.12 LESENSE_SCANRES - Scan Result

Offset	Bit Position																													
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																0x0															
Access	R																R															
Name	STEPDIR																SCANRES															

Bit	Name	Reset	Access	Description
31:16	STEPDIR	0x0	R	**Direction of previous step detection**
	In step detection mode, bit X will be set if a step up was detected on channel X; write to initialize when LESENSE is disabled.			
15:0	SCANRES	0x0	R	**Scan results**
	Bit X will be set depending on channel X evaluation;			

28.6.13 LESENSE_STATUS - Status

Offset	Bit Position																													
0x030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																										0x0	0x0	0x0	0x0		0x0	0x0
Access																										R	R	R	R		R	R
Name																										FLUSHING	READBUSY	RUNNING	SCANACTIVE		RESFIFOFULL	RESFIFOV

Bit	Name	Reset	Access	Description
31:7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6	FLUSHING	0x0	R	**FIFO Flushing**
5	READBUSY	0x0	R	**FIFO Read Busy**
4	RUNNING	0x0	R	**LESENSE periodic counter running**
	LESENSE is running in periodic mode.			
3	SCANACTIVE	0x0	R	**LESENSE scan active**
	LESENSE is currently interfacing sensors.			
2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	RESFIFOFULL	0x0	R	**Result fifo full**
	Set when the result fifo is full			
0	RESFIFOV	0x0	R	**Result fifo valid**
	Set when data is available in the result fifo. Cleared when the buffer is empty.			

28.6.14 LESENSE_RESCOUNT - Result FIFO Count

Offset	Bit Position																															
0x034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0				
Access																												R				
Name																												COUNT				

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4:0	COUNT	0x0	R	**Result Fifo Count**
	Number of valid data in the Result FIFO			

28.6.15 LESENSE_RESFIFO - Result Fifo

Offset	Bit Position																															
0x038	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset													0x0																			
Access													R																			
Name													BUFDATASRC																			

Bit	Name	Reset	Access	Description
31:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:0	BUFDATASRC	0x0	R	**Result data and source**
	This bitfield contains the sensor result (least-significant 16 bits) and the channel index (most-significant 4 bits)			

28.6.16 LESENSE_CURCH - Current Channel Index

Offset	Bit Position																															
0x03C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0		
Access																													R		
Name																													CURCH		

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	CURCH	0x0	R	**Shows the index of the current channel**

28.6.17 LESENSE_DECSTATE - Current Decoder State

Offset	Bit Position																															
0x040	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																														0x0		
Access																														R		
Name																														DECSTATE		

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4:0	DECSTATE	0x0	R	**Shows the current decoder state**

28.6.18 LESENSE_SENSORSTATE - Sensor State

Offset	Bit Position																															
0x044	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																													0x0			
Access																													R			
Name																													SENSORSTATE			

Bit	Name	Reset	Access	Description
31:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3:0	SENSORSTATE	0x0	R	**Sensor State** Sensor State used as input to the DECODER state machine

28.6.19 LESENSE_IDLECONF - IDLE Configuration

Offset	Bit Position																											
0x048	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0		0x0		0x0		0x0		0x0		0x0		0x0		0x0		0x0		0x0		0x0		0x0		0x0		0x0		0x0		0x0	
Access	RW		RW		RW		RW		RW		RW		RW		RW		RW		RW		RW		RW		RW		RW		RW	
Name	CHIDLE15		CHIDLE14		CHIDLE13		CHIDLE12		CHIDLE11		CHIDLE10		CHIDLE9		CHIDLE8		CHIDLE7		CHIDLE6		CHIDLE5		CHIDLE4		CHIDLE3		CHIDLE2		CHIDLE1		CHIDLE0	

Bit	Name	Reset	Access	Description
31:30	CHIDLE15	0x0	RW	**Channel IDLE configuration**
	Channel 15 idle phase configuration			
	Value	Mode		Description
	0	DISABLE		Channel output is disabled in idle phase
	1	HIGH		Channel output is high in idle phase
	2	LOW		Channel output is low in idle phase
	3	DAC		Channel output is connected to DAC output in idle phase (CH 0,1,2 only)
29:28	CHIDLE14	0x0	RW	**Channel IDLE configuration**
	Channel 14 idle phase configuration			
	Value	Mode		Description
	0	DISABLE		Channel output is disabled in idle phase
	1	HIGH		Channel output is high in idle phase
	2	LOW		Channel output is low in idle phase
	3	DAC		Channel output is connected to DAC output in idle phase (CH 0,1,2 only)
27:26	CHIDLE13	0x0	RW	**Channel IDLE configuration**
	Channel 13 idle phase configuration			
	Value	Mode		Description
	0	DISABLE		Channel output is disabled in idle phase
	1	HIGH		Channel output is high in idle phase
	2	LOW		Channel output is low in idle phase
	3	DAC		Channel output is connected to DAC output in idle phase (CH 0,1,2 only)
25:24	CHIDLE12	0x0	RW	**Channel IDLE configuration**
	Channel 12 idle phase configuration			
	Value	Mode		Description

Bit	Name	Reset	Access	Description
	0	DISABLE		Channel output is disabled in idle phase
	1	HIGH		Channel output is high in idle phase
	2	LOW		Channel output is low in idle phase
	3	DAC		Channel output is connected to DAC output in idle phase (CH 0,1,2 only)
23:22	CHIDLE11	0x0	RW	**Channel IDLE configuration**
	Channel 11 idle phase configuration			
	Value	Mode		Description
	0	DISABLE		Channel output is disabled in idle phase
	1	HIGH		Channel output is high in idle phase
	2	LOW		Channel output is low in idle phase
	3	DAC		Channel output is connected to DAC output in idle phase (CH 0,1,2 only)
21:20	CHIDLE10	0x0	RW	**Channel IDLE configuration**
	Channel 10 idle phase configuration			
	Value	Mode		Description
	0	DISABLE		Channel output is disabled in idle phase
	1	HIGH		Channel output is high in idle phase
	2	LOW		Channel output is low in idle phase
	3	DAC		Channel output is connected to DAC output in idle phase (CH 0,1,2 only)
19:18	CHIDLE9	0x0	RW	**Channel IDLE configuration**
	Channel 9 idle phase configuration			
	Value	Mode		Description
	0	DISABLE		Channel output is disabled in idle phase
	1	HIGH		Channel output is high in idle phase
	2	LOW		Channel output is low in idle phase
	3	DAC		Channel output is connected to DAC output in idle phase (CH 0,1,2 only)
17:16	CHIDLE8	0x0	RW	**Channel IDLE configuration**
	Channel 8 idle phase configuration			
	Value	Mode		Description
	0	DISABLE		Channel output is disabled in idle phase
	1	HIGH		Channel output is high in idle phase
	2	LOW		Channel output is low in idle phase
	3	DAC		Channel output is connected to DAC output in idle phase (CH 0,1,2 only)

Bit	Name	Reset	Access	Description
15:14	CHIDLE7	0x0	RW	**Channel IDLE configuration**
	Channel 7 idle phase configuration			
	Value	Mode		Description
	0	DISABLE		Channel output is disabled in idle phase
	1	HIGH		Channel output is high in idle phase
	2	LOW		Channel output is low in idle phase
	3	DAC		Channel output is connected to DAC output in idle phase (CH 0,1,2 only)
13:12	CHIDLE6	0x0	RW	**Channel IDLE configuration**
	Channel 6 idle phase configuration			
	Value	Mode		Description
	0	DISABLE		Channel output is disabled in idle phase
	1	HIGH		Channel output is high in idle phase
	2	LOW		Channel output is low in idle phase
	3	DAC		Channel output is connected to DAC output in idle phase (CH 0,1,2 only)
11:10	CHIDLE5	0x0	RW	**Channel IDLE configuration**
	Channel 5 idle phase configuration			
	Value	Mode		Description
	0	DISABLE		Channel output is disabled in idle phase
	1	HIGH		Channel output is high in idle phase
	2	LOW		Channel output is low in idle phase
	3	DAC		Channel output is connected to DAC output in idle phase (CH 0,1,2 only)
9:8	CHIDLE4	0x0	RW	**Channel IDLE configuration**
	Channel 4 idle phase configuration			
	Value	Mode		Description
	0	DISABLE		Channel output is disabled in idle phase
	1	HIGH		Channel output is high in idle phase
	2	LOW		Channel output is low in idle phase
	3	DAC		Channel output is connected to DAC output in idle phase (CH 0,1,2 only)
7:6	CHIDLE3	0x0	RW	**Channel IDLE configuration**
	Channel 3 idle phase configuration			
	Value	Mode		Description
	0	DISABLE		Channel output is disabled in idle phase

Bit	Name	Reset	Access	Description
	1	HIGH		Channel output is high in idle phase
	2	LOW		Channel output is low in idle phase
	3	DAC		Channel output is connected to DAC output in idle phase (CH 0,1,2 only)
5:4	CHIDLE2	0x0	RW	**Channel IDLE configuration**
	Channel 2 idle phase configuration			
	Value	Mode		Description
	0	DISABLE		Channel output is disabled in idle phase
	1	HIGH		Channel output is high in idle phase
	2	LOW		Channel output is low in idle phase
	3	DAC		Channel output is connected to DAC output in idle phase (CH 0,1,2 only)
3:2	CHIDLE1	0x0	RW	**Channel IDLE configuration**
	Channel 1 idle phase configuration			
	Value	Mode		Description
	0	DISABLE		Channel output is disabled in idle phase
	1	HIGH		Channel output is high in idle phase
	2	LOW		Channel output is low in idle phase
	3	DAC		Channel output is connected to DAC output in idle phase (CH 0,1,2 only)
1:0	CHIDLE0	0x0	RW	**Channel IDLE configuration**
	Channel 0 idle phase configuration			
	Value	Mode		Description
	0	DISABLE		Channel output is disabled in idle phase
	1	HIGH		Channel output is high in idle phase
	2	LOW		Channel output is low in idle phase
	3	DAC		Channel output is connected to DAC output in idle phase (CH 0,1,2 only)

28.6.20 LESENSE_SYNCBUSY - Synchronization

Offset	Bit Position																															
0x050	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																R
Name																																CMD

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	CMD	0x0	R	**Command**
	Command Register Busy			

28.6.21 LESENSE_IF - Interrupt Flags

Offset	Bit Position																															
0x060	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset											0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access											RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name											RESUF	CNTOF	RESOF	RESWL	DEC	SCANDONE	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Bit	Name	Reset	Access	Description
31:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21	RESUF	0x0	RW	**Result Underflow**
20	CNTOF	0x0	RW	**Counter Overflow**
	LESENSE Ripple Counter Overflows			
19	RESOF	0x0	RW	**Result Overflow**
	Result FIFO Overflow			
18	RESWL	0x0	RW	**Result Watermark Level**
	Set when Result FIFO count reaches RESFIDL			
17	DEC	0x0	RW	**Decoder**
	Set when decoder triggers interrupt			
16	SCANDONE	0x0	RW	**Scan Done**
	Set when scan sequence is completed			
15	CH15	0x0	RW	**Channel**
	Set when Channel 15 triggers			
14	CH14	0x0	RW	**Channel**
	Set when Channel 14 triggers			
13	CH13	0x0	RW	**Channel**
	Set when Channel 13 triggers			
12	CH12	0x0	RW	**Channel**
	Set when Channel 12 triggers			
11	CH11	0x0	RW	**Channel**
	Set when Channel 11 triggers			
10	CH10	0x0	RW	**Channel**
	Set when Channel 10 triggers			
9	CH9	0x0	RW	**Channel**
	Set when Channel 9 triggers			

Bit	Name	Reset	Access	Description
8	CH8	0x0	RW	**Channel**
	Set when Channel 8 triggers			
7	CH7	0x0	RW	**Channel**
	Set when Channel 7 triggers			
6	CH6	0x0	RW	**Channel**
	Set when Channel 6 triggers			
5	CH5	0x0	RW	**Channel**
	Set when Channel 5 triggers			
4	CH4	0x0	RW	**Channel**
	Set when Channel 4 triggers			
3	CH3	0x0	RW	**Channel**
	Set when Channel 3 triggers			
2	CH2	0x0	RW	**Channel**
	Set when Channel 2 triggers			
1	CH1	0x0	RW	**Channel**
	Set when Channel 1 triggers			
0	CH0	0x0	RW	**Channel**
	Set when Channel 0 triggers			

28.6.22 LESENSE_IEN - Interrupt Enables

Offset	Bit Position																															
0x064	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset											0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access											RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name											RESUF	CNTOF	RESOF	RESWL	DEC	SCANDONE	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Bit	Name	Reset	Access	Description
31:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21	RESUF	0x0	RW	**Result Underflow**
20	CNTOF	0x0	RW	**Counter Overflow**
19	RESOF	0x0	RW	**Result Overflow**
18	RESWL	0x0	RW	**Result Watermark Level**
17	DEC	0x0	RW	**Decoder**
16	SCANDONE	0x0	RW	**Scan Complete**
15	CH15	0x0	RW	**Channel**
	Enable Channel 15 interrupt			
14	CH14	0x0	RW	**Channel**
	Enable Channel 14 interrupt			
13	CH13	0x0	RW	**Channel**
	Enable Channel 13 interrupt			
12	CH12	0x0	RW	**Channel**
	Enable Channel 12 interrupt			
11	CH11	0x0	RW	**Channel**
	Enable Channel 11 interrupt			
10	CH10	0x0	RW	**Channel**
	Enable Channel 10 interrupt			
9	CH9	0x0	RW	**Channel**
	Enable Channel 9 interrupt			
8	CH8	0x0	RW	**Channel**

Bit	Name	Reset	Access	Description
	Enable Channel 8 interrupt			
7	CH7	0x0	RW	**Channel**
	Enable Channel 7 interrupt			
6	CH6	0x0	RW	**Channel**
	Enable Channel 6 interrupt			
5	CH5	0x0	RW	**Channel**
	Enable Channel 5 interrupt			
4	CH4	0x0	RW	**Channel**
	Enable Channel 4 interrupt			
3	CH3	0x0	RW	**Channel**
	Enable Channel 3 interrupt			
2	CH2	0x0	RW	**Channel**
	Enable Channel 2 interrupt			
1	CH1	0x0	RW	**Channel**
	Enable Channel 1 interrupt			
0	CH0	0x0	RW	**Channel**
	Enable Channel 0 interrupt			

28.6.23 LESENSE_CHx_TIMING - Scan Configuration

Offset	Bit Position																													
0x100	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset									0x0										0x0								0x0					
Access									RW										RW								RW					
Name									MEASUREDLY										SAMPLEDLY								EXTIME					

Bit	Name	Reset	Access	Description
31:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:14	MEASUREDLY	0x0	RW	**Set measure delay**
	Configure measure delay. Sensor measuring is delayed for MEASUREDLY EXCLK cycles.			
13:6	SAMPLEDLY	0x0	RW	**Set sample delay**
	Configure sample delay. Sampling will occur after SAMPLEDLY SAMPLECLK cycles.			
5:0	EXTIME	0x0	RW	**Set excitation time**
	Configure excitation time. Excitation will last EXTIME EXCLK cycles.			

28.6.24 LESENSE_CHx_INTERACT - Scan Configuration

Offset	Bit Position																															
0x104	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset			0x0		0x0				0x0			0x0	0x0	0x0	0x0						0x0											
Access			RW		RW				RW			RW	RW	RW	RW						RW											
Name			SAMPLE		OFFSET				SETIF			EXCLK	SAMPLECLK	ALTEX	EXMODE						THRES											

Bit	Name	Reset	Access	Description
31:30	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
29:28	SAMPLE	0x0	RW	**Sample mode Selection**

Value	Mode	Description
0	ACMPCOUNT	
1	ACMP	
2	ADC	
3	ADCDIFF	

27:24	OFFSET	0x0	RW	**OFFSET for IADC/ACMP interaction**
23:21	SETIF	0x0	RW	**Enable interrupt generation**

Select interrupt generation mode for CHx interrupt flag.

Value	Mode	Description
0	NONE	No interrupt is generated
1	LEVEL	Set interrupt flag if the sensor triggers.
2	POSEDGE	Set interrupt flag on positive edge of the sensor state
3	NEGEDGE	Set interrupt flag on negative edge of the sensor state
4	BOTHEDGES	Set interrupt flag on both edges of the sensor state

20	EXCLK	0x0	RW	**Select clock used for excitation timing**

Value	Mode	Description
0	LFACLK	Prescaled low-frequency LESENSECLK will be used for timing
1	AUXHFRCO	Prescaled high-frequency LESENSEHFCLK will be used for timing

19	SAMPLECLK	0x0	RW	**Select clock used for timing of sample d**

Bit	Name	Reset	Access	Description
	Value	Mode		Description
	0	LFACLK		Prescaled low-frequency LESENSECLK will be used for timing
	1	AUXHFRCO		Prescaled high-frequency LESENSEHFCLK will be used for timing
18	ALTEX	0x0	RW	**Use alternative excite pin**
	If set, alternative excite pin will be used for excitation			
17:16	EXMODE	0x0	RW	**Set GPIO mode**
	GPIO mode for the excitation phase of the scan sequence. Note that DACOUT is only available on channels 0, 1, 2			
	Value	Mode		Description
	0	DISABLE		Disabled
	1	HIGH		Push Pull, GPIO is driven high
	2	LOW		Push Pull, GPIO is driven low
	3	DACOUT		DAC output
15:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:0	THRES	0x0	RW	**ACMP threshold or DAC data**
	Set threshold used for ACMP, or data used in DAC conversion			

28.6.25 LESENSE_CHx_EVALCFG - Scan Configuration

Offset	Bit Position																													
0x108	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x0			0x0	0x0		0x0	0x0		
Access																							RW			RW	RW		RW	RW		
Name																							MODE			SCANRESINV	STRSAMPLE		COMP	DECODE		

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	MODE	0x0	RW	**Configure evaluation mode**
	Select which evaluation mode to be used on the measurement result			
	Value	Mode		Description
	0	THRES		Threshold comparison is used to evaluate sensor result
	1	SLIDINGWIN		Sliding window is used to evaluate sensor result
	2	STEPDET		Step detection is used to evaluate sensor result
7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6	SCANRESINV	0x0	RW	**Enable inversion of result**
	If set, the result is inverted and stored in SCANRES .			
5:4	STRSAMPLE	0x0	RW	**Enable storing of sensor sample in resul**
	If set, the sensor sample value will be stored and available in the result buffer			
	Value	Mode		Description
	0	DISABLE		Nothing will be stored in the result buffer.
	1	DATA		The sensor sample data will be stored in the result buffer.
	2	DATASRC		The data source, i.e. the channel, will be stored alongside the sensor sample data.
3	COMP	0x0	RW	**Select mode for threshold comparison**
	Set compare mode			
	Value	Mode		Description
	0	LESS		Comparison evaluates to 1 if sensor data is less than CTRTHRESHOLD, or if the ACMP output is 0
	1	GE		Comparison evaluates to 1 if sensor data is greater than, or equal to CTRTHRESHOLD, or if the ACMP output is 1
2	DECODE	0x0	RW	**Send result to decoder**

Bit	Name	Reset	Access	Description
	If set, the result from this channel will be shifted into the decoder register.			
1:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

28.6.26 LESENSE_CHx_EVALTHRES - Scan Confguration

Offset	Bit Position																															
0x10C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0															
Access																	RW															
Name																	EVALTHRES															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	EVALTHRES	0x0	RW	**Threshold**
	This is the THRESHOLD used for evaluating the sensor results in the different evaluation modes.			

28.6.27 LESENSE_STx_ARC - State Transition Arc

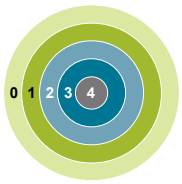
Offset	Bit Position																														
0x200	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset											0x0	0x0					0x0			0x0					0x0				0x0			
Access											RW	RW					RW			RW					RW				RW			
Name											SETIF	NEXTSTATE					PRSACT			CURSTATE					SMASK				SCOMP			

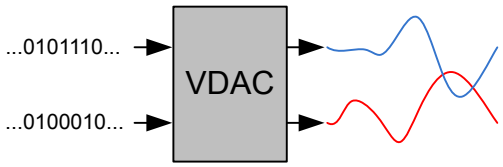
Bit	Name	Reset	Access	Description
31:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21	SETIF	0x0	RW	**Set interrupt flag**
	Set interrupt flag when sensor state equals COMP			
20:16	NEXTSTATE	0x0	RW	**Next state index**
	Index of next state to be entered if the sensor state equals COMP			
15:13	PRSACT	0x0	RW	**Configure transition action in normal mode**
	Configure which action to perform when sensor state equals COMP. Note different actions when DECCTRL.PRSCNT = 0 or 1.			

Value	Mode	Description
0	NONE	No PRS output generated (if PRSCOUNT == 0), or do not count (if PRSCOUNT == 1).
1	PRS0	Pulse generated on LESENSE PRS output 0 (if PRSCOUNT == 0).
1	UP	Count Up (if PRSCOUNT == 1).
2	PRS1	Pulse generated on LESENSE PRS output 1 (if PRSCOUNT == 0).
2	DOWN	Count Down (if PRSCOUNT == 1).
3	PRS01	Pulse generated on LESENSE PRS output 0 and 1 (if PRSCOUNT == 0).
4	PRS2	Pulse generated on LESENSE PRS output 2. (PRSCOUNT == 0 OR 1).
5	PRS02	Pulse generated on LESENSE PRS output 0 and 2 (if PRSCOUNT == 0).
5	UPANDPRS2	Count Up and Pulse generated on LESENSE PRS output 2 (if PRSCOUNT == 1).
6	PRS12	Pulse generated on LESENSE PRS output 1 and 2 (if PRSCOUNT == 0).
6	DOWNANDPRS2	Count Down and Pulse generated on LESENSE PRS output 2 (if PRSCOUNT == 1).
7	PRS012	Pulse generated on LESENSE PRS output 0, 1 and 2 (if PRSCOUNT == 0).

Bit	Name	Reset	Access	Description
12:8	CURSTATE	0x0	RW	**Current State**
	Current State Index			
7:4	SMASK	0x0	RW	**Sensor mask**
	Set bit X to exclude sensor X from evaluation.			
3:0	SCOMP	0x0	RW	**Sensor compare value**
	State transition is triggered when sensor state equals COMP			

29. VDAC - Digital to Analog Converter





Quick Facts

What?

The VDAC is designed for low energy consumption, but can also provide very good performance. It can convert digital values to analog signals at up to 500 ksamples/second with 12-bit accuracy.

Why?

The VDAC can be used to generate accurate analog signals for sound, sensors and other applications, using only a limited amount of energy.

How?

The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using the LDMA, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available down to Energy Mode 3.

29.1 Introduction

The Voltage Digital to Analog Converter (VDAC) converts a digital value to an analog output voltage. It is useful in a number of different applications such as sensor excitation or low/medium frequency sound output. The VDAC has two rail-to-rail output channels that may act as independent DACs or be combined into a differential pair. The output buffers support high or low power operation as well as a high capacitance mode for driving loads up to 50 pF. Both channels have a 4-word FIFO for efficient throughput and minimum CPU intervention. Flexible conversion trigger sources allow for accurate AC and DC waveform timing, and a special sample-off mode can be used in conjunction with periodic output refresh to reduce energy consumption or act as a temporary excitation source.

29.2 Features

Each VDAC instance in a device supports the following features:

- Up to 500 ksps operation
- Two output channels
  - Can be combined into one differential output
- Integrated 7-bit clock prescaler with division factors ranging from 1 to 128
- Selectable voltage reference
  - Internal 2.5 V (effective full-scale)
  - Internal 1.25 V (effective full-scale)
  - AVDD supply
  - External VREFP pin
- Outputs available for internal and external use
  - Main low-impedance outputs to dedicated GPIO
  - Auxiliary outputs routable through ABUS to any ABUS-capable GPIO (higher impedance)
  - Internal routing of auxiliary outputs to other analog blocks
- Data conversion modes selectable per channel
  - Continuous Mode for high speed conversion or constant DC output
  - Sample-off Mode for per-sample conversion followed by channel disable
- Independent FIFO per channel
  - 4 word (12bit) depth for each channel
  - Programmable data valid level
  - Supports software flush
- Conversion trigger sources
  - Data write (software)
  - PRS input (synchronous and asynchronous)
  - Internal timer with power-of-2 selection from 2-64 prescaled clock cycles
  - LESENSE
- Refresh trigger sources
  - Refresh timer with power-of-2 selection from 2-256 low-frequency clock cycles
  - PRS input (synchronous or asynchronous)
- PRS Communication
  - Separate line for each channel
  - Sync and async PRS output pulse on finished conversion
  - PRS Level Output till channel is warmed
  - Async PRS Output Pulse on Refresh Timer Overflow and Internal Timer Overflow
- LDMA request on FIFO data valid level
  - Independent requests for each DAC channel
- Sine generation mode with differential support

29.3 Functional Description

An overview of the VDAC module is shown Figure 29.1 VDAC Block Overview Diagram on page 1152

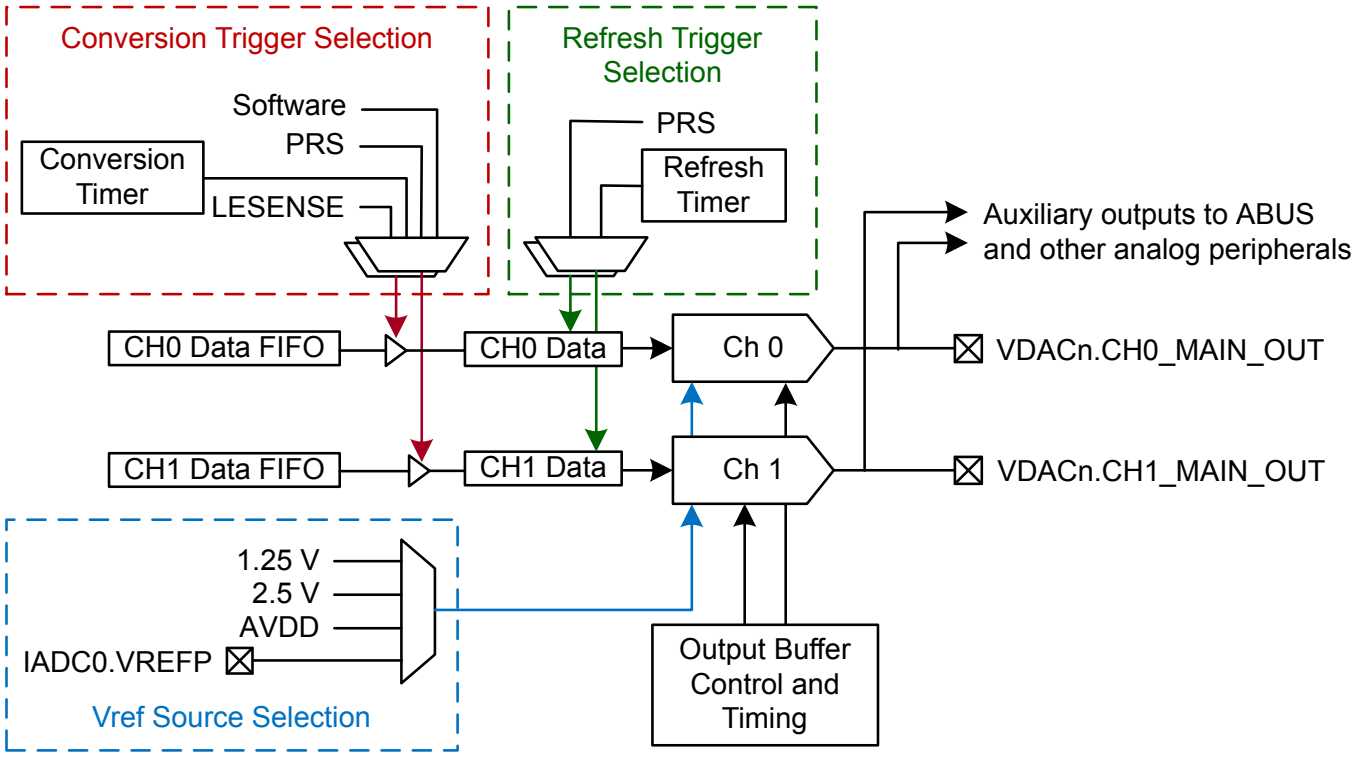


Figure 29.1. VDAC Block Overview Diagram

29.3.1 Power Supply

The VDAC module power (V_{VDAC}) is derived from the AVDD supply pin.

29.3.2 I/O Pin Considerations

The maximum usable analog signal that can be seen on external VDAC outputs depends on both the AVDD and IOVDD supplies. Specifically, the VDAC output will be limited to the lower of the two supply voltages on AVDD and IOVDD.

29.3.3 Enabling and Disabling a Channel

The VDAC module is enabled by writing 1 to EN in VDAC_EN.

A VDAC channel is enabled by writing 1 to the CHxEN and disabled by writing 1 to CHxDIS using in the CMD register. The channel status (enabled or disabled) can be read using the CHxENS bits in the STATUS register. The CHxENS bit will go high after a synchronization delay following a write to CHxEN. When disabling a channel the CHxENS bit will stay high until the VDAC channel is completely disabled.

Software should configure the VDAC before enabling a channel. The following registers are used to configure all the available features of the VDAC:

- VDAC_CFG
- VDAC_CH0CFG
- VDAC_CH1CFG
- VDAC_OUTTIMERCFG

A VDAC channel will not begin driving its output before it is enabled *and* has received a conversion trigger or refresh trigger. After a channel is enabled, it will listen for either conversion trigger sources specified in TRIGMODE in VDAC_CHxCFG or refresh trigger sources specified in REFRESHSOURCE in VDAC_CHxCFG. If TRIGMODE is set to SW and the CHxF FIFO is not empty, a conversion will start immediately when the channel is enabled. When disabling a channel, any pending triggers are flushed.

When disabling the VDAC module, user code must poll the status bit VDAC_EN.DISABLING to ensure that the module is cleanly reset and back to its initial condition.

29.3.4 Clock Selection

The VDAC logic accepts three clock sources from the CMU: LSPCLK, VDACn_CLK, and VDACn_REFRESH_CLK. The APB register interface and FIFO write logic are clocked from the LSPCLK. The rest of the VDAC state machine is clocked mainly by a prescaled version of VDACn_CLK. VDACn_DAC from the CMU can be up to 80 MHz. The PRESC bit field in the CFG register should be set to scale VDACn_CLK to no more than 1 MHz. The VDACn_REFRESH_CLK is a low-frequency clock source which only clocks the dedicated refresh timer.

The clock request for VDACn_CLK to the CMU from VDAC is on-demand by default. This means the VDAC core clock is gated off most of the time except:

- New Conversion or Refresh Trigger
- Sine Generation Active Window
- VDAC_CHxCFG.TRIGMODE = SYNCPRS
- VDAC_CHxCFG.REFRESHSOURCE = SYNCPRS
- VDAC_CHxCFG.TRIGMODE = SW and the VDAC CHx FIFO is not empty
- VDAC_CHxCFG.TRIGMODE = INTTIMER

In some cases it is necessary or preferred to have the VDAC clock active all the time. To turn off on-demand clocking, the VDAC_CFG.ONDEMANDCLK bit can be set to '1', which always requests VDACn_CLK from the CMU. On-demand clocking should be disabled if EM23GRPACLK is selected for VDACn_CLK.

If the VDAC will only perform conversions in EM0 and EM1, any clock source for the VDAC may be used.

If the VDAC is to be operated in EM2 or EM3, VDACn_CLK must be configured to use either HFRCOEM23, EM23GRPACLK or FSRCO instead of the EM01GRPACLK clock. FSRCO is the fast start oscillator which starts quickly but is not as accurate as the other oscillators. HFRCOEM23 is generally recommended for EM2/EM3 operation. When using FSRCO or HFRCOEM23, the clock source can be selected to be "on demand" so as not to waste current when the DAC is not doing a conversion. On demand clocking is configured by setting VDAC_CFG.ONDEMANDCLK to 0.

EM23GRPACLK is recommended only when VDAC is expected to do very slow sample conversions/refresh. VDAC_CFG.ONDEMANDCLK should be set to 1 if EM23GRPACLK is selected as the VDAC clock source.

Note: When HFRCOEM23 is selected as a clock source to VDAC and clocking is on-demand (CFG.ONDEMANDCLK = 0), HFRCOEM23 on-demand clocking must be enabled. This allows the power domain which powers HFRCOEM23 to be ON during EM2 and the clock request to HFRCOEM23 can be honored.

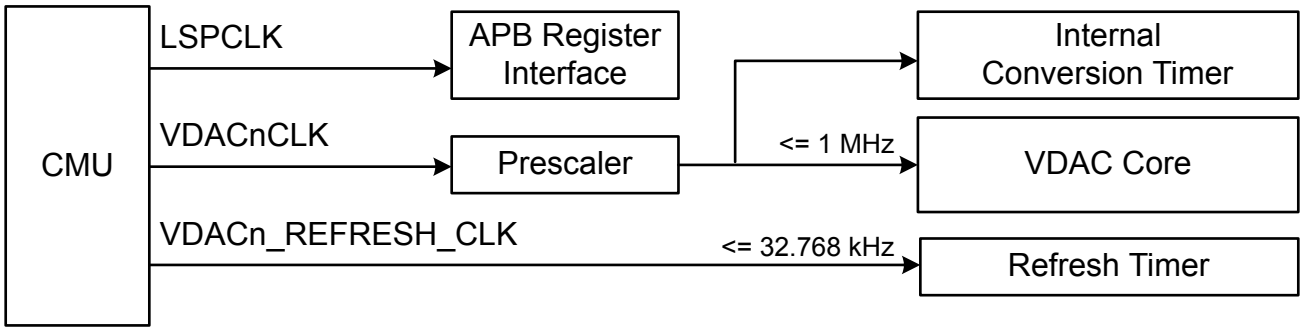


Figure 29.2. VDAC Block Clocks Diagram

29.3.4.1 Internal Clock Prescaler

The VDAC has an internal clock prescaler, which can divide the VDACn_CLK input clock by any factor between 1 and 128, by setting the PRESC field in the CFG register. The resulting prescaled clock is 50% duty cycle and is used by the converter core. The frequency is given by Figure 29.3 VDAC Clock Prescaling on page 1155 :

$$f_{CLK\_DAC\_PRESC} = f_{VDACn\_CLK} / (PRESC + 1)$$

Figure 29.3. VDAC Clock Prescaling

where f_{VDACn_CLK} is the input clock frequency coming from the CMU. The $f_{CLK\_DAC\_PRESC}$ must be programmed to be at most 1 MHz.

The prescaler runs continuously when the VDAC is enabled or when VDAC_SWRST.SWRST is set. When running with a prescaler setting higher than 0, there can be an unpredictable delay from the time a conversion was triggered to the time the actual conversion takes place. This is because the conversions are controlled by the prescaled time base, and the conversion can arrive at any time during a prescaled clock (CLK_DAC_PRESC) period. A second reason for unpredictable delay between a trigger and the associated conversion is that the activity on one channel can impact whether the VDAC reference is warm or not - when two channels are used independently with warmup, it can impact whether a warmup is required on a trigger.

The uncertainty related to the clock prescaler can be addressed by using CH0PRESCRST. If the CH0PRESCRST bit in VDAC_CFG is set, the prescaler will be reset every time a conversion is triggered on channel 0. This leads to a predictable latency between channel 0 triggers and conversions (assuming the warmup sequence is deterministic as well). If channel x is used in continuous mode, the warmup sequence will only apply once when the channel is enabled and software can use the VDAC_STATUS.CHxWARM bit to determine if the VDAC has warmed up.

29.3.4.2 VDACn_REFRESH_CLK

VDAC also has another clock coming in from the CMU, VDACn_REFRESH_CLK. This clock is asynchronous to the VDACn_CLK and is used to clock the internal refresh timer. VDACn_REFRESH_CLK is connected directly to the EM23GRPACLK source in the CMU and hence it is a low-frequency clock sourse with a maximum frequency of ~32 kHz. The refresh timer inside VDAC is a slow running, low power timer. When this refresh timer is used as a refresh trigger source and the timer overflows, it will trigger a VDACn_CLK on-demand request from the CMU.

29.3.5 Conversions

The VDAC consists of two channels (channel 0 and 1) with separate 4 deep FIFOs with 12-bits data elements (VDAC_CHxF.DATA). These can be used to produce two independent single ended outputs or the channel 0 register can be used to drive both outputs in a differential mode. The VDAC supports two conversion modes: **continuous** and **sample-off.**

Continuous Mode

In continuous mode the VDAC buffers will remain on, and channels will drive their outputs continuously till the channel is disabled with the data in the VDAC_CHxF.DATA register. A channel is configured in continuous mode by programming the CONVMODE bitfield in VDAC_CHxCFG to CONTINUOUS. This mode will maintain the output voltage from a conversion indefinitely, until a new output is triggered or until the channel is disabled.

In continuous mode the CHxOUTHOLDTIME field in VDAC_OUTTIMERCFG should be programmed to zero to achieve the maximum update rate. Both these settings need to be configured before VDAC module is enabled.

Sample-off Mode

In sample-off mode the VDAC will only drive the output for a limited time per conversion. A channel is configured in sample-off mode by programming the CONVMODE bitfield in VDAC_CHxCFG to SAMPLEOFF. The CHxOUTHOLDTIME field in the VDAC_OUTTIMERCFG register determines how long the output will be driven after a conversion or refresh trigger occurs. The VDAC will drive the output for CHxOUTHOLDTIME number of CLK_DAC_PRESC cycles before tri-stating the output again (and therefore if CHxOUTHOLDTIME is set to zero, the output will never be driven when using sample-off mode). Both these settings need to be configured before VDAC module is enabled.

29.3.6 Conversion Trigger

Conversions can only be performed while a channel is enabled and the CHxF FIFO is not empty, see 29.3.3 Enabling and Disabling a Channel.

- If CHxCFG.TRIGMODE is programmed to SW, a conversion can be started automatically when the CHxF.DATA is not empty. Writing to the FIFO will trigger a conversion on the specified channel.
- If CHxCFG.TRIGMODE is programmed to SYNCPRS or ASYNCPRS, a conversion can be started by an incoming pulse on the selected PRS channel. VDAC expects a PRS pulse coming from both synchronous and asynchronous PRS producers. Depending on the TRIGMODE and channel enable, the VDAC will process the PRS pulse from the respective producer.
- If CHxCFG.TRIGMODE is programmed to INTERNALTIMER, the internal timer is uses to start conversions, and a new conversion will start on any overflow of the internal timer. See 29.3.13 Internal Timers.
- For Channel 0, If CH0CFG.TRIGMODE is programmed to LESENSE a conversion will start when the LESENSE block sends a request. This setting needs to be selected whenever the channel 0 is under LESENSE control. Note that LESENSE can only trigger a conversion to Channel 0 and not Channel 1.

29.3.7 Refresh Trigger

The refresh mechanism can be used to periodically refresh the output with the most recent conversion result. A refresh trigger can only happen while a channel is enabled, see 29.3.3 Enabling and Disabling a Channel.

- If CHxCFG.REFRESHSOURCE is programmed to SYNCPRS or ASYNCPRS, a refresh can be started by an incoming pulse on the selected PRS channel. The VDAC refresh mechanism requires a PRS pulse for either configuration of CHxCFG.REFRESHSOURCE. Depending on the REFRESHSOURCE and channel enable, VDAC processes the PRS pulse from the respective producer.
- If CHxCFG.REFRESHSOURCE is programmed to REFRESHTIMER, a conversion will start on an overflow of the refresh timer. See 29.3.13 Internal Timers.

Note: The refresh mechanism never pops a new conversion from the FIFO. It just re-triggers the conversion based on the last data converted by the conversion trigger to generate the same voltage output at the load. A periodic refresh of the output voltage into a suitable RC filter (to reduce ripple) may be a way to establish a low-energy DC bias in some applications.

Conversion Trigger and Refresh Trigger co-existence

- Conversion triggers are given preference over refresh triggers. During a conversion trigger sample conversion, if a refresh trigger occurs it is ignored.
- Refresh triggers are served only when the conversion trigger sample conversion is completely finished.
- During a refresh trigger sample conversion, if a conversion trigger occurs, it is held by the VDAC and served once the refresh trigger conversion is finished. The VDAC never ignores conversion triggers.

29.3.8 PRS Communication

PRS triggers can be used to set a constant sample frequency, for instance by using a TIMER, or to synchronize conversion events with other hardware. In order to get a jitter-free sample rate from a PRS source, set CHxCFG.TRIGMODE to SYNCPRS and set the CFG.CH0PRESCRST bit to ensure the prescaler is reset on trigger. Note that because the prescaler is shared between channels, this is only possible for channel 0.

For CHxCFG.TRIGMODE / CHxCFG.REFRESHSOURCE of ASYNCPRS, the sample frequency cannot be guaranteed to be jitter-free with respect to the PRS pulses. The CH0PRESCRST bit in VDAC_CFG can still be set to reset the clock prescaler on every PRS trigger for better predictability. Note, this can be set only on channel 0.

The Input PRS frequency should never be higher than 0.5 MHz (the fastest possible sample rate). In addition, the input PRS frequency should not be higher than f_{VDACn_CLK} / 4 (in synchronous mode). If the PRS frequency is set too high, some PRS pulses may be dropped and the output can jitter.

VDAC also sends out the following list of output signals as a PRS producer:

- CHxDONEASYNC - CHx Conversion Done Asynchronous PRS Pulse Output
- CHxWARM - CHx Output Valid Async PRS Level Output
- CHxDONESYNC - CHx Conversion Done Sync PRS Pulse Output
- REFRESHTIMEROF - Refresh Timer Overflow Async PRS Pulse Output
- INTERNALTIMEROF - Internal Timer Overflow Async PRS Pulse Output

29.3.9 Reference Selection

The VDAC supports four voltage reference options:

- Internal 1.25 V Reference (effective full scale)
- Internal 2.5 V Reference (effective full scale)
- AVDD
- External IADC0.VREFP Pin

The voltage reference is selected by programming the REFRSEL field in VDAC_CFG, and is shared for both VDAC channels. The selected voltage reference sets the full scale output voltage of the VDAC. In the case of the internal 1.25 V and 2.5 V reference options, the VDAC uses a lower internal voltage as the reference, and scaling techniques to produce an effective full scale voltage of 1.25 V or 2.5 V respectively. The 2.5 V internal reference can still be used over the entire supply voltage range of the device without any dropout. However, the output will be limited by the supply rail(s) and VDAC will not be able to drive above the supply.

29.3.10 Power Modes

The VDAC supports independently-selectable high power and low power modes per channel. Each has a maximum load capacitance of 50 pF. The power mode for each channel is configured by setting VDAC_CHxCFG.POWERMODE. By default, the VDAC starts in HIGHPOWER mode.

VDAC also supports an additional high capacitance load mode in conjunction with the HIGHPOWER power mode. High capacitance mode is enabled by setting VDAC_CHxCFG.HIGHCAPLOADEN to 1. The minimum load capacitance on the pin is 25 nF for this mode.

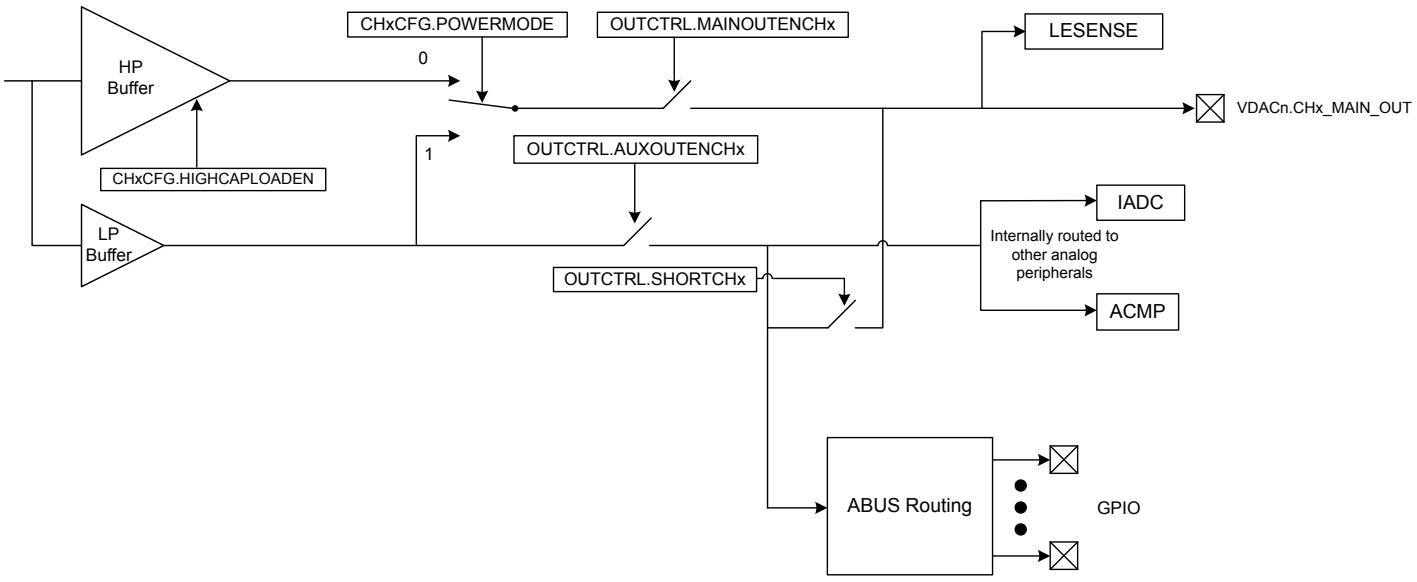


Figure 29.4. VDAC Block Power Modes Diagram

29.3.11 Warmup Time and Initial Conversion

When a channel is enabled, it needs to warm up. This is performed automatically when the channel is enabled if the CONVMODE in VDAC_CHxCFG is set to Continuous mode.

If the CONVMODE in VDAC_CHxCFG is set to Sample-off mode, then every sample conversion is preceded by warmup of the VDAC. Hence, the sample conversion time in case of sample-off mode includes the WARMUPTIME of the VDAC too.

The time allocated for warmup depends on the WARMUPTIME field in VDAC_CFG. WARMUPTIME is specified in prescaled VDACn_CLK cycles and should be set to a minimum of 3 us (3 clocks if CLK_DAC_PRESC = 1 MHz). Software is responsible for programming the correct value to WARMUPTIME before enabling a channel. If the time is programmed too short, an undefined voltage may be output until the analog portion of VDAC settles.

The CHxWARM bits in VDAC_STATUS are set when the warmup period has completed. A consequence of the warmup period is that in continuous mode, the recommended programming model is to either wait for CHxWARM status before starting conversions in order to make sure all samples have the same timing, or perform a dummy conversion to make the VDAC settle to a known voltage first.

29.3.12 Output Mode

The two VDAC channels can act as two separate single-ended channels or be combined into one differential channel. This is selected through the DIFF bit in VDAC_CFG.

- **Single Ended Output**

When operating in single ended mode, the channel 0 output is on VDAC_OUT0 and the channel 1 output is on VDAC_OUT1. The output voltage can be calculated using Figure 29.5 VDAC Single Ended Output Voltage on page 1158

$$V_{OUT} = V_{VDACn\_OUTx} - V_{SS} = V_{ref} \times CHxDATA/4096$$

Figure 29.5. VDAC Single Ended Output Voltage

where CHxDATA is a 12-bit unsigned integer.

- **Differential Output**

When operating in differential mode, both VDAC outputs are used to produce a differential output. The conversion uses the VDAC_CH0DATA buffer as the data source. The data written to VDAC_CH0DATA is interpreted as a two's complement number, with the MSB of the 12-bit value being the sign bit. Conceptually, a 'positive' and 'negative' output, with a common-mode voltage of $V_{ref}/2$ are generated from this information.

The positive output appears on VDAC_CH1 and the negative output appears on VDAC_CH0. The output voltage can be calculated using Figure 29.6 VDAC Differential Output Voltage on page 1158:

$$V_{OUT} = V_{VDACn\_CH1} - V_{VDACn\_CH0} = V_{ref} \times CH0DATA/2048$$

Figure 29.6. VDAC Differential Output Voltage

where CH0DATA is a 12-bit signed integer. The common mode voltage is $V_{ref}/2$.

When using differential mode, the user needs to program only CH0 settings to reflect to both channels. Any programmed settings in CH1 will be ignored in differential mode.

29.3.13 Internal Timers

VDAC has two internal timers that run independently of each other:

Conversion Timer

VDAC includes an internal conversion timer.This conversion timer is automatically started if a channel selects INTERNALTIMER as TRIGMODE in VDAC_CHxCFG reigster and the channel is enabled. The conversion timer will count the number of prescaled VDACn_CLK cycles programmed in VDAC_CFG.TIMEROVERFLOWPERIOD before wrapping and generating a conversion trigger. The timer overflow period is from 2-64 prescaled VDACn_CLK cycles. The conversion timer overflow automatically initiates the sample conversion if the CHxF FIFO is not empty.

INTERNALTIMEROF is also available as an asynchronous PRS signal, generating a pulse that lasts for 1 prescaled VDACn_CLK cycle. Note that since this timer runs off prescaled VDACn_CLK, the VDACn_CLK is always requested from the CMU when the internal conversion timer is used.

Refresh Timer

VDAC includes an internal low power refresh timer.This refresh timer is automatically started if a channel selects REFRESHTIMER as REFRESHSOURCE in VDAC_CHxCFG register and the channel is enabled. The refresh timer will count the number of VDACn_REFRESH_CLK cycles programmed in VDC_CFG.REFRESHPERIOD before wrapping and generating a refresh trigger. The refresh period is from 2-256 VDACn_REFRESH_CLK cycles. The refresh timer overflow automatically initiates the refresh.

REFRESHTIMEROF is also available as an asynchronous PRS signal, generating a pulse that lasts for 1 VDACn_REFRESH_CLK cycle. Note that since this timer runs off VDACn_REFRESH_CLK, which is asynchronous to VDACn_CLK, VDACn_CLK is only requested from the CMU when the refresh timer overflows. Also, as discussed in 29.3.4 Clock Selection, this timer always runs off a slow clock, hence this refresh conversion is low power.

29.3.14 FIFO

VDAC has two FIFOs, one for each channel. Each FIFO is 4 samples deep. Data is pushed into the FIFO by either the CPU or LDMA, and happens on the bus clock. Samples are popped from the FIFO on the VDACn_CLK domain by the VDAC core whenever there is a new conversion trigger. Both FIFOs support a data flush from the CPU.

CHxF FIFO Programming Model

Before enabling VDAC, set the low threshold Data Valid Level for each channel by programming VDAC_CHxCFG.FIFODVL Bit. If in DIFF Mode, the channel 1 DVL settings are ignored. Fill the VDAC_CHxF.DATA with the number of entries greater than programmed DVL to avoid triggering of DVL Interrupt. Details of the DVL Interrupt are explained in 29.3.18 Interrupts and Wakeup. The number of valid entries per channel can be read from VDAC_STATUS.CHxFIFOCNT (only if VDAC_CFG.ONDEMANDCLK is set to 1). The status of whether the FIFO is full or empty can be read from VDAC_STATUS.CHxFIFOFULL and VDAC_STATUS.CHxFIFOEMPTY respectively.

CHxF FIFO Flush Programming Model

In case there is incorrect data programmed in the FIFO or in the event of a FIFO overflow, the CPU can issue a flush by programming VDAC_CMD.CHxFIFOFLUSH. This flush bit resets both the write pointer (in the bus clock domain) and the read pointer (in rhe CLK_DAC domain) together. During a flush, new conversions should not be triggered on the channel whose FIFO contents are flushed. The flush status is reported with the VDAC_STATUS.CHxFIFOFLBUSY bit, which will remain high during the flush operation and return low when it is complete. Since the CPU issues flush to the CHx FIFO, there are several steps that should be followed in order to avoid any spurious voltage at VDAC Output:

- Disable the channel using VDAC_CMD.CHxDIS = 1
- Disable the VDAC channel in the LDMA to avoid any new CHxFIFO writes during flushing
- Issue the flush command and poll the VDAC_STATUS.CHxFIFOFLBUSY status bit
- After flushing is complete, re-enable the VDAC channel and optionally re-program the LDMA

29.3.15 Keepwarm Sub-modes

VDAC has two keepwarm modes that can be used with Sample-off Conversion Mode to define the behaviour of the analog portion of the VDAC between sample conversions. The keepwarm mode needs to be set along with Sample-off Conversion Mode before enabling the VDAC module. The two options are:

Bias Keepwarm

Bias Keepwarm Mode is primarily used to reduce kickback to the reference bias, in case it is shared with IADC. This mode can be activated by setting the VDAC_CFG.BIASKEEPWARM Bit to 1. During this mode, the VDAC Analog Bias remains ON in between sample conversions instead of shutting down after the hold time expires.

This mode is only relevant when using the internal 1.25 V or 2.5 V reference selections. This mode does not reduce the required warm-up time of the VDAC. Enabling this mode will typically cost about 4 uA of additional current when the VDAC is idle. The VDAC analog bias remains on irrespective of the channel enable/disable, until the VDAC module is disabled.

Channel Keepwarm

Channel Keepwarm Mode is primarily used to reduce kickback between the two channels, or to reduce the start-up time of the VDAC in-between sample conversions. This mode is activated per channel by setting the VDAC_CHxCFG.KEEPWARM bit to 1. During this mode, the VDAC remains warmed up in-between sample conversions and can convert new samples without incurring a warm up delay. This mode can only be used with Sample-off conversion mode. Setting this mode typically costs about 10-20 uA of additional current when the VDAC is idle.

29.3.16 LDMA Interface

The VDAC has two FIFOs (one per channel) which can be filled using the LDMA whenever there is space available in the FIFO. To facilitate this, the VDAC generates a DMA request per channel to the LDMA when the FIFO count reaches the lower threshold Data Valid Level (DVL). DVL is set by programming VDAC_CHxCFG.FIFODVL to set the watermark.

DMA REQ and SREQ

Both Channel 0 and 1 generate DMA requests in the bus clock domain only when the VDAC_CMD.CHxEN bit is set. In the case of DIFF mode, Channel 1 will not generate LDMA requests. The FIFOs are initially empty, hence as soon as the channels are enabled, each channel will send out a DMA REQ. The request is cleared when FIFO is filled beyond DVL+1.

If there is at least 1 valid space in the FIFO and the DMA channel is not active, each VDAC channel will also send a SREQ to LDMA. This SREQ is also gated with the channel enable.

EM2 Operation

When the system is in EM2, the VDAC can generate new DMA requests as well. This feature can be enabled by setting the VDAC_CFG.DMAWU bit to 1 before enabling VDAC. When enabled and the FIFO count in the read domain falls below the programmed DVL setting, the VDAC will generate a request to the EMU to enter an EM1 state. Once the EMU enters this state and the bus clock is available, VDAC generates the DMA REQ/SREQ per channel to request new data for conversion.

The VDAC keeps the request for data high until the FIFO count is above the programmed DVL setting. Once the condition is met, VDAC automatically pulls the request low and the system can return fully to EM2.

29.3.17 Sine Generation Mode

The VDAC contains an automatic sine-generation mode, which is enabled by setting the SINEMODE bit in VDAC_CFG. In this mode, the VDAC data from the FIFO is overridden with data from an internal hard-coded sine lookup table.

Sine mode is supported only for the fastest configuration of the VDAC in continuous mode. Therefore the CONVMODE bit in VDAC_CH0CFG needs to be set to CONTINUOUS and the CH0OUTHOLDTIME bit in VDAC_OUTTIMERCFG needs to be programmed to zero for channel 0 to use sine generation mode. The TRIGMODE and REFRESHSOURCE bitfields in VDAC_CHxCFG need to be programmed to NONE for channel 0 in order to avoid interference in sine output generation from other triggers. Other trigger modes are not supported. The SINE wave will always be output on channel 0 and therefore requires that this channel is enabled by writing 1 to CH0EN in the VDAC_CMD register. If DIFF is set in VDAC_CFG, the sine wave will additionally be output on channel 1, but inverted. Note that the first sample will only be available after the CHxWARMED bit is 1 in VDAC_STATUS register after setting CH0EN =1 in VDAC_CMD.

Each period, starting at 0 degrees, is made up of 16 samples and the frequency is given by Figure 29.7 VDAC Sine Generation Frequency on page 1160.

$$f_{sine} = f_{CLK\_DAC\_PRESC} / 32$$

Figure 29.7. VDAC Sine Generation Frequency

When DIFF is 0 and SINEMODE is 1 in VDAC_CFG, a sine wave will be generated on channel 0 but channel 1 can still be used independently as a single-ended DAC output. Channel 1 settings are ignored if DIFF is 1.

To configure the VDAC for sine wave output:

- Set VDAC_CFG.SINEMODE to 1 to put the VDAC in sine wave mode
- Set VDAC_CH0CFG.CONVMODE to CONTINUOUS
- Set VDAC_CH0CFG.TRIGMODE to NONE
- Set VDAC_CH0CFG.REFRESHSOURCE to NONE
- Set VDAC_OUTTIMERCFG.CH0OUTHOLDTIME to 0
- Configure VDAC_CFG.DIFF for single-ended or differential output
  - 0 = Single ended output (only channel 0 is used)
  - 1 = Enable differential output (both channel 0 and channel 1 will be used)
- Configure VDAC_CFG.SINERESET for desired behavior when halted
  - 0 = Sine wave output is not reset when halted, and will continue at the next sample when re-started
  - 1 = Sine wave output is reset to 0 degrees when halted, and output will return to Vref / 2
- Set VDAC_CFG.CH0EN to 1 to enable the VDAC module

29.3.17.1 Sine Generation - Software Control

The sine signal generation may be controlled by software using the SINEMODESTART and SINEMODESTOP commands in VDAC_CMD. When SINEMODESTART is set to 1, sine wave generation will be started. Setting SINEMODESTOP to 1 will halt the sine wave generation. If SINERESET in VDAC_CFG is set to 1, the sine output will be reset to 0 degrees when the SINEMODESTOP bit is set to 1, resulting in a voltage of Vref / 2 on the output channel(s). If SINERESET equals 0, a SINEMODESTOP command will stop progress of the sine wave at the sample currently being output. The sine will continue at the next sample when SINEMODESTART is issued again.

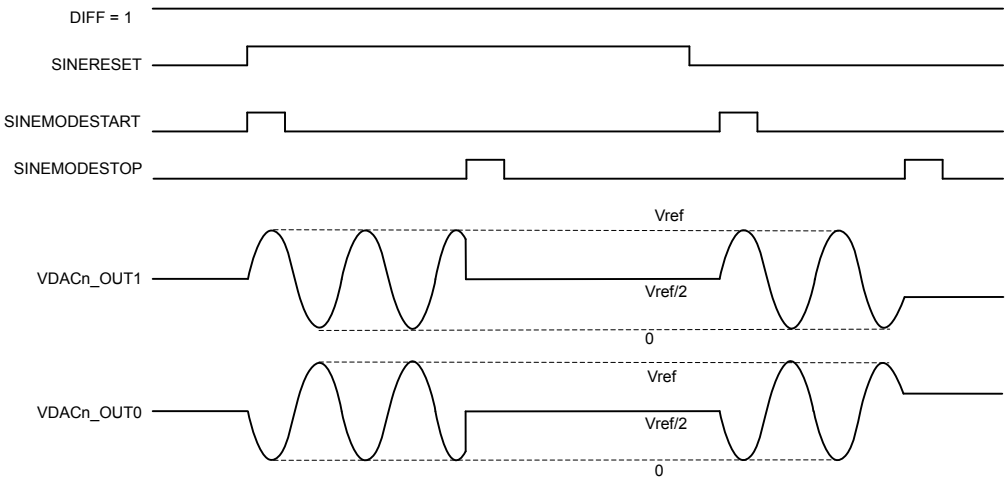


Figure 29.8. VDAC Sine Mode - Software Control

29.3.18 Interrupts and Wakeup

The VDAC has several interrupt flags in the VDAC_IF register, indicating various state and error conditions related to output, FIFO status, and conversions. Each channel has a separate set of interrupt flags.

- **Conversion Done**

  The Conversion Done (CHxCD) interrupt flags are set when a conversion is complete. The flags are set after a channel has driven the output with the programmed code.
- **Data Valid Level (DVL)**

  The Data Valid Level (CHxDVL) interrupt flags are set when the FIFO Count reaches below or equal to Data Valid Level (DVL). The DVL number is programmed in CHxCFG.DVL Register Bits. These flags are initially set, and gets cleared when CHxF FIFO is filled with new set of data, thereby making count >= DVL. The FIFO Count can be read through VDAC_STATUS.CHxFIFOCNT Flag. Note that this fifo count is generated in the read domain, hence expect read synchronization delay for the count value.
- **Overflow/Underflow**

  If a write is attempted in CHxF FIFO whilst it is full, the channel overflow flag (CHxOF) will be set. If a new conversion is triggered (e.g. via PRS) before whilst CHxF FIFO is empty, the channel underflow flag (CHxUF) will be set. The FIFO full and empty status can be read through VDAC_STATUS.CHxFIFOFULL and VDAC_STATUS.CHxFIFOEMPTY Flags.
- **ABUS Conflict/Allocation Error**

  In case both channel 0 and channel 1 request the same Port and Pin for conversion output through ABUS, an ABUS Conflict Error IF (ABUSINPUTCONFLICT) will be set. In case the ABUS Allocation is not coherent with Programmed Port and Pin Setting for either channel, ABUS Allocation Error interrupt flag (ABUSALLOCERR) will be set.

Not all interrupt flags will wake up EMU to EM0 when the VDAC is operating in EM2. Only those interrupts that need interaction with the host will wakeup the CPU. For this, DVL, ABUSALLOCERR and/or ABUSINPUTCONFLICT are used as wakeup interrupt source too.

29.3.19 LESENSE Operation

VDAC Channel 0 can be controlled by LESENSE by programming the TRIGMODE field in VDAC_CH0CFG to LESENSE. In LESENSE mode the conversion data can come from either the VDAC_CHx0 FIFO or LESENSE registers, depending on the LESENSE configuration. The trigger events are also controlled by the LESENSE state machine.

When used for LESENSE, the MAIN output must be enabled and it will be driven to the main output pin. LESENSE may switch this output to connect to one of its defined DAC output pins as needed.

All the programmed VDAC settings (including the Keepwarm Modes) will be over-written by LESENSE configuration. See the LESENSE chapter for more information.

29.3.20 VDAC Output Configuration

The VDAC analog outputs can be routed either to specific fixed pins, to configurable GPIO through ABUS, or used internally by other blocks. These settings can be programmed in the VDAC_OUTCTRL register after VDAC is enabled but ideally before channels are enabled. The possible settings are as follows:

- VDAC_OUTCTRL.MAINOUTENCHx - Set this bit to route VDAC channel analog main output to the dedicated pin (CHx_MAIN_OUT). This is the preferred option for any DAC output. This option is also required when using VDAC CH0 in conjunction with the LESENSE switched outputs.
- VDAC_OUTCTRL.AUXOUTENCHx - Set this bit to route VDAC channel analog auxiliary output to internal blocks such as IADC and ACMP, or to the ABUS interconnect matrix, where it can be routed to any port I/O supporting ABUS. Note that the ABUS multiplexer adds significant impedance, and this option may not be suitable for certain loads or dynamic conditions.
- VDAC_OUTCTRL.SHORTCHx - Set this bit when using the high-power buffer option with the auxiliary outputs. This will short the MAIN and AUX outputs together. The MAIN output is still driven in this configuration.
- VDAC_OUTCTRL.ABUSPORTSELCHx - Select a particular ABUS port for the channel. Choose values from PORTA, PORTB, PORTC, PORTD
- VDAC_OUTCTRL.ABUSPINSELCHx - Select a particular ABUS pin for the channel. Program the pin in conjuction with the port to route the analog output to a particular GPIO.

Note: Once the channel is enabled, the output control settings in VDAC and the ABUS configuration in both VDAC and GPIO should not be changed until the channel is disabled. Changing these settings while enabled may cause spurious voltage generation on random GPIO.

ABUS Allocation Rules to VDAC in GPIO

- AEVEN0/BEVEN0/CDEVEN0 can only be allocated to CH0
- AEVEN1/BEVEN1/CDEVEN1 can only be allocated to CH1
- AODD0/BODD0/CDODD0 can only be allocated to CH0
- AODD1/BODD1/CDODD1 can only be allocated to CH1
- The port and pin requested by ABUSPORTSELCHx/ABUSPINSELCHx must match a bus allocated to VDAC CHx.

  For example, if AEVEN0 is the only bus allocated to CH0, the selected port must be port A, and the selected pin must be even.

More details on ABUS allocation can be found in GPIO chapter

29.4 VDAC Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	VDAC_IPVERSION	R	IPVERSION
0x004	VDAC_EN	RW ENABLE	Module Enable
0x008	VDAC_SWRST	RW SWRST	Software Reset Register
0x00C	VDAC_CFG	RW CONFIG	Config Register
0x010	VDAC_STATUS	RH	Status Register
0x014	VDAC_CH0CFG	RW CONFIG	Channel 0 Config Register
0x018	VDAC_CH1CFG	RW CONFIG	Channel 1 Config Register
0x01C	VDAC_CMD	W SYNC	Command Register
0x020	VDAC_IF	RWH INTFLAG	Interrupt Flag Register
0x024	VDAC_IEN	RW	Interrupt Enable Register
0x028	VDAC_CH0F	W	Channel 0 Data Write Fifo
0x02C	VDAC_CH1F	W	Channel 1 Data Write Fifo
0x030	VDAC_OUTCTRL	RW SYNC	DAC Output Control
0x034	VDAC_OUTTIMERCFG	RW CONFIG	DAC Out Timer Config Register
0x1000	VDAC_IPVERSION_SET	R	IPVERSION
0x1004	VDAC_EN_SET	RW ENABLE	Module Enable
0x1008	VDAC_SWRST_SET	RW SWRST	Software Reset Register
0x100C	VDAC_CFG_SET	RW CONFIG	Config Register
0x1010	VDAC_STATUS_SET	RH	Status Register
0x1014	VDAC_CH0CFG_SET	RW CONFIG	Channel 0 Config Register
0x1018	VDAC_CH1CFG_SET	RW CONFIG	Channel 1 Config Register
0x101C	VDAC_CMD_SET	W SYNC	Command Register
0x1020	VDAC_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x1024	VDAC_IEN_SET	RW	Interrupt Enable Register
0x1028	VDAC_CH0F_SET	W	Channel 0 Data Write Fifo
0x102C	VDAC_CH1F_SET	W	Channel 1 Data Write Fifo
0x1030	VDAC_OUTCTRL_SET	RW SYNC	DAC Output Control
0x1034	VDAC_OUTTIMERCFG_SET	RW CONFIG	DAC Out Timer Config Register
0x2000	VDAC_IPVERSION_CLR	R	IPVERSION
0x2004	VDAC_EN_CLR	RW ENABLE	Module Enable
0x2008	VDAC_SWRST_CLR	RW SWRST	Software Reset Register
0x200C	VDAC_CFG_CLR	RW CONFIG	Config Register
0x2010	VDAC_STATUS_CLR	RH	Status Register
0x2014	VDAC_CH0CFG_CLR	RW CONFIG	Channel 0 Config Register
0x2018	VDAC_CH1CFG_CLR	RW CONFIG	Channel 1 Config Register

Offset	Name	Type	Description
0x201C	VDAC_CMD_CLR	W SYNC	Command Register
0x2020	VDAC_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x2024	VDAC_IEN_CLR	RW	Interrupt Enable Register
0x2028	VDAC_CH0F_CLR	W	Channel 0 Data Write Fifo
0x202C	VDAC_CH1F_CLR	W	Channel 1 Data Write Fifo
0x2030	VDAC_OUTCTRL_CLR	RW SYNC	DAC Output Control
0x2034	VDAC_OUTTIMERCFG_CLR	RW CONFIG	DAC Out Timer Config Register
0x3000	VDAC_IPVERSION_TGL	R	IPVERSION
0x3004	VDAC_EN_TGL	RW ENABLE	Module Enable
0x3008	VDAC_SWRST_TGL	RW SWRST	Software Reset Register
0x300C	VDAC_CFG_TGL	RW CONFIG	Config Register
0x3010	VDAC_STATUS_TGL	RH	Status Register
0x3014	VDAC_CH0CFG_TGL	RW CONFIG	Channel 0 Config Register
0x3018	VDAC_CH1CFG_TGL	RW CONFIG	Channel 1 Config Register
0x301C	VDAC_CMD_TGL	W SYNC	Command Register
0x3020	VDAC_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x3024	VDAC_IEN_TGL	RW	Interrupt Enable Register
0x3028	VDAC_CH0F_TGL	W	Channel 0 Data Write Fifo
0x302C	VDAC_CH1F_TGL	W	Channel 1 Data Write Fifo
0x3030	VDAC_OUTCTRL_TGL	RW SYNC	DAC Output Control
0x3034	VDAC_OUTTIMERCFG_TGL	RW CONFIG	DAC Out Timer Config Register

29.5 VDAC Register Description

29.5.1 VDAC_IPVERSION - IPVERSION

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x2																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x2	R	**IPVERSION**
	The read only IPVERSION field gives the version for this module. There may be minor software changes required for modules with different values of IPVERSION.			

29.5.2 VDAC_EN - Module Enable

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	RW
Name																															DISABLING	EN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DISABLING	0x0	R	**Disablement busy status**
	When EN is cleared, DISABLING is set immediately, and cleared when disablement finishes. Disablement resets peripheral cores and not APB registers except hardware updated registers such as INTFLAGs and FIFOs.			
0	EN	0x0	RW	**VDAC Module Enable**
	Enable the VDAC module. When EN is cleared(disablement), it halts module operation immediately, and initialize the core domain such that when the is re-enabled, it starts cleanly.			

Value	Mode	Description
0	DISABLE	Disable
1	ENABLE	Enable

29.5.3 VDAC_SWRST - Software Reset Register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	W
Name																															RESETTING	SWRST

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	RESETTING	0x0	R	**Software reset busy status**
	When SWRST command is issued, resetting logic sets RESETTING status immediately, and later it is cleared when reset process finishes.			
0	SWRST	0x0	W	**Software reset command**
	A software reset command field resets the module back to the initial condition, similar to a power on reset condition			

29.5.4 VDAC_CFG - Config Register

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset		0x2			0x0	0x0	0x0	0x0		0x0				0x0					0x0								0x0		0x0	0x0	0x0	0x0
Access		RW			RW	RW	RW	RW		RW				RW					RW								RW		RW	RW	RW	RW
Name		WARMUPTIME			DBGHALT	ONDEMANDCLK	DMAWU	BIASKEEPWARM		REFRESHPERIOD				TIMEROVRFLOWPERIOD					PRESC								REFRSEL		CH0PRESCRST	SINERESET	SINEMODE	DIFF

Bit	Name	Reset	Access	Description
31	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
30:28	WARMUPTIME	0x2	RW	**DAC Warmup Time**
	Number of prescaled CLK_DAC +1 cycles for the VDAC to Warmup. Default is (2+1) prescaled CLK_DAC cycles.			
27	DBGHALT	0x0	RW	**Debug Halt**
	VDAC behavior when halted by debugger			

Value	Mode	Description
0	NORMAL	Continue operation as normal during debug mode
1	HALT	Complete the current conversion and then halt during debug mode

Bit	Name	Reset	Access	Description
26	ONDEMANDCLK	0x0	RW	**Always allow clk_dac**
	Setting this bit to 1 always allows CLK_DAC from CMU			
25	DMAWU	0x0	RW	**VDAC DMA Wakeup**
	Set to enable wakeup from EM2 to EM1 for DMA to fill CHx FIFO Data			
24	BIASKEEPWARM	0x0	RW	**Bias Keepwarm Mode Enable**
	Set this bit to keep the Bias on for Analog portion of DAC in between conversions. Primary purpose, is to reduce kick-back to the reference shared with IADC. Relevant only for Sample-off Mode			
23	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
22:20	REFRESHPERIOD	0x0	RW	**Refresh Timer Overflow Period**
	Select refresh counter period. A channel x will be refreshed with the period set in REFRESHPERIOD if the channel in VDACn_CHxCFG has its REFRESHSOURCE set to REFRESHTIMER			

Value	Mode	Description
0	CYCLES2	All channels with enabled refresh are refreshed every 2 CLK_REFRESH cycles

Bit	Name	Reset	Access	Description
	1	CYCLES4		All channels with enabled refresh are refreshed every 4 CLK_REFRESH cycles
	2	CYCLES8		All channels with enabled refresh are refreshed every 8 CLK_REFRESH cycles
	3	CYCLES16		All channels with enabled refresh are refreshed every 16 CLK_REFRESH cycles
	4	CYCLES32		All channels with enabled refresh are refreshed every 32 CLK_REFRESH cycles
	5	CYCLES64		All channels with enabled refresh are refreshed every 64 CLK_REFRESH cycles
	6	CYCLES128		All channels with enabled refresh are refreshed every 128 CLK_REFRESH cycles
	7	CYCLES256		All channels with enabled refresh are refreshed every 256 CLK_REFRESH cycles
19	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
18:16	TIMEROVRFLOWPERIOD	0x0	RW	**Internal Timer Overflow Period**
	Select internal timer overflow period. A channel x will be provided with a conversion trigger after the period set in TIMEROVRFLOWPERIOD if the channel in VDACn_CHxCFG has its TRIGMODE set to INTERNALTIMER			
	Value	Mode		Description
	0	CYCLES2		The Timer overflows every 2 Prescaled CLK_DAC cycles
	1	CYCLES4		The Timer overflows every 4 Prescaled CLK_DAC cycles
	2	CYCLES8		The Timer overflows every 8 Prescaled CLK_DAC cycles
	3	CYCLES16		The Timer overflows every 16 Prescaled CLK_DAC cycles
	4	CYCLES32		The Timer overflows every 32 Prescaled CLK_DAC cycles
	5	CYCLES64		The Timer overflows every 64 Prescaled CLK_DAC cycles
15:14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13:7	PRESC	0x0	RW	**Prescaler Setting for DAC clock**
	Selected DAC clock source is prescaled by PRESC+1 to generate prescaled CLK_DAC with 50% duty cycle			
6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5:4	REFRSEL	0x0	RW	**Reference Selection**
	Select reference for analog portion of DAC			
	Value	Mode		Description
	0	V125		Internal 1.25 V bandgap reference
	1	V25		Internal 2.5 V bandgap reference
	2	VDD		AVDD reference
	3	EXT		External pin reference

Bit	Name	Reset	Access	Description
3	CH0PRESCRST	0x0	RW	**Channel 0 Start Reset Prescaler**

Select if prescaler (determining prescaled CLK_DAC rate) is reset on channel 0 start.

Value	Mode	Description
0	NORESETPRESC	Prescaler not reset on channel 0 start
1	RESETPRESC	Prescaler reset on channel 0 start

Bit	Name	Reset	Access	Description
2	SINERESET	0x0	RW	**Sine Wave Reset When inactive**

In case SINERESET is 0, SINEMODESTOP will stop progress of the sine wave at the sample currently being output in sinemode. When Set to 1,the sine output will reset to 0 degrees when SINEMODESTOP

Bit	Name	Reset	Access	Description
1	SINEMODE	0x0	RW	**Sine Mode**

Enable/disable sine mode.

Value	Mode	Description
0	DISSINEMODE	Sine mode disabled. Sine reset to 0 degrees
1	ENSINEMODE	Sine mode enabled

Bit	Name	Reset	Access	Description
0	DIFF	0x0	RW	**Differential Mode**

Select single ended or differential mode.

Value	Mode	Description
0	SINGLEENDED	Single ended output
1	DIFFERENTIAL	Differential output

29.5.5 VDAC_STATUS - Status Register

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0	0x0	0x0	0x0	0x0			0x0	0x0		0x0	0x0		0x0			0x0					0x0	0x0			0x0	0x0			0x0	0x0
Access	R	R	R	R	R	R			R	R		R	R		R			R					R	R			R	R			R	R
Name	SYNCBUSY	ABUSALLOCERR	SINEACTIVE	ABUSINPUTCONFLICT	CH1FIFOFLBUSY	CH0FIFOFLBUSY			CH1FIFOEMPTY	CH0FIFOEMPTY		CH1CURRENTSTATE	CH0CURRENTSTATE		CH1FIFOCNT			CH0FIFOCNT					CH1FIFOFULL	CH0FIFOFULL			CH1WARM	CH0WARM			CH1ENS	CH0ENS

Bit	Name	Reset	Access	Description
31	SYNCBUSY	0x0	R	**Sync Busy Combined**
	Indicates synchronization ongoing			
30	ABUSALLOCERR	0x0	R	**ABUS Allocation Error Status**
	1 if ABUS requested is not allocated			
29	SINEACTIVE	0x0	R	**Sine Wave Output Status on Channel**
	1 indicates that sine wave output is generated on CH0 and/or CH1(in diff mode)			
28	ABUSINPUTCONFLICT	0x0	R	**ABUS Input Conflict Status**
	1 if both CH0 and CH1 request the same ABUS			
27	CH1FIFOFLBUSY	0x0	R	**CH1 FIFO Flush Sync Busy**
	Indicates CH1 FIFO Flush Sync Busy			
26	CH0FIFOFLBUSY	0x0	R	**CH0 FIFO Flush Sync Busy**
	Indicates CH0 FIFO Flush Sync Busy			
25:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23	CH1FIFOEMPTY	0x0	R	**Channel 1 FIFO Empty Status**
	1 if FIFO for Channel 1 is empty			
22	CH0FIFOEMPTY	0x0	R	**Channel 0 FIFO Empty Status**
	1 if FIFO for Channel 0 is empty			
21	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
20	CH1CURRENTSTATE	0x0	R	**Channel 1 Current Status**
	0 when CH1 is in IDLE State. Set when CH1 is converting data			
19	CH0CURRENTSTATE	0x0	R	**Channel 0 Current Status**
	0 when CH0 is in IDLE State. Set when CH0 is converting data			
18	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
17:15	CH1FIFOCNT	0x0	R	**Channel 1 FIFO Valid Count**

Bit	Name	Reset	Access	Description
	Number of Valid Entries in Channel 1. This FIFO entries Count is generated in Read Domain hence expect Synchronization Delay. Need to be used only when VDAC_CFG.ONDEMANDCLK is set to 1.			
14:12	CH0FIFOCNT	0x0	R	**Channel 0 FIFO Valid Count**
	Number of Valid Entries in Channel 0. This FIFO entries Count is generated in Read Domain hence expect Synchronization Delay. Need to be used only when VDAC_CFG.ONDEMANDCLK is set to 1.			
11:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	CH1FIFOFULL	0x0	R	**Channel 1 FIFO Full Status**
	1 if FIFO for Channel 1 is full			
8	CH0FIFOFULL	0x0	R	**Channel 0 FIFO Full Status**
	1 if FIFO for Channel 0 is full			
7:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	CH1WARM	0x0	R	**Channel 1 Warmed Status**
	This bit is set when channel 1 has warmed up			
4	CH0WARM	0x0	R	**Channel 0 Warmed Status**
	This bit is set when channel 0 has warmed up			
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	CH1ENS	0x0	R	**Channel 1 Enabled Status**
	This bit is set when channel 1 is enabled.			
0	CH0ENS	0x0	R	**Channel 0 Enabled Status**
	This bit is set when channel 0 is enabled.			

29.5.6 VDAC_CH0CFG - Channel 0 Config Register

Offset	Bit Position																															
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																0x0		0x0		0x0			0x0			0x0			0x0		0x0
Access																RW		RW		RW			RW			RW			RW		RW
Name																KEEPWARM		HIGHCAPLOADEN		FIFODVL			REFRESHSOURCE			TRIGMODE			POWERMODE		CONVMODE

Bit	Name	Reset	Access	Description
31:17	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
16	KEEPWARM	0x0	RW	**Channel 0 Keepwarm Mode Enable**
	Set this bit to keep the Channel 0 on in between conversion in sample-off mode. Primary purpose of this is to reduce kickback between Channel 0 and Channel 1 and to reduce startup time.			
15	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
14	HIGHCAPLOADEN	0x0	RW	**Channel 0 High Cap Load Mode Enable**
	Enables High Capacitance Load Mode for Channel 0. Should be enabled with VDAC_CH0CFG.POWERMODE=HIGHPOWER			
13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12:11	FIFODVL	0x0	RW	**Channel 0 FIFO Low Watermark**
	Set Channel 0 FIFO Low Threshold Data Valid Level (DVL)			
10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	REFRESHSOURCE	0x0	RW	**Channel 0 Refresh Source**
	Select Channel 0 Refresh Trigger			

Value	Mode	Description
0	NONE	No Refresh Source Selected for Channel 0.
1	REFRESHTIMER	Channel 0 Refresh triggered by Refresh Timer Overflow
2	SYNCPRS	Channel 0 Refresh triggered by Sync PRS. PRS Trigger should have the same clock group as VDAC.
3	ASYNCPRS	Channel 0 Refresh triggered by Async PRS

7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:4	TRIGMODE	0x0	RW	**Channel 0 Trigger Mode**
	Select Channel 0 Conversion Trigger			

Bit	Name	Reset	Access	Description
	Value	Mode		Description
	0	NONE		No Conversion Trigger Source Selected for Channel 0
	1	SW		Channel 0 is triggered by Channel 0 FIFO (CH0F) write
	2	SYNCPRS		Channel 0 is triggered by Sync PRS input. PRS Trigger should have the same clock group as VDAC.
	3	LESENSE		Channel 0 is triggered by LESENSE
	4	INTERNALTIMER		Channel 0 is triggered by Internal Timer Overflow
	5	ASYNCPRS		Channel 0 is triggered by Async PRS input
3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	POWERMODE	0x0	RW	**Channel 0 Power Mode**
	Enable Power Mode for Channel 0			
	Value	Mode		Description
	0	HIGHPOWER		Default is High Power Mode
	1	LOWPOWER		Set this bit for Low Power Mode
1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	CONVMODE	0x0	RW	**Channel 0 Conversion Mode**
	Configure conversion mode			
	Value	Mode		Description
	0	CONTINUOUS		DAC channel 0 is set in continuous mode
	1	SAMPLEOFF		DAC channel 0 is set in sample/shut off mode

29.5.7 VDAC_CH1CFG - Channel 1 Config Register

Offset	Bit Position																															
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																0x0		0x0		0x0			0x0			0x0			0x0		0x0
Access																RW		RW		RW			RW			RW			RW		RW
Name																KEEPWARM		HIGHCAPLOADEN		FIFODVL			REFRESHSOURCE			TRIGMODE			POWERMODE		CONVMODE

Bit	Name	Reset	Access	Description
31:17	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
16	KEEPWARM	0x0	RW	**Channel 1 Keepwarm Mode Enable**
	Set this bit to keep the Channel 1 on in between conversion in sample-off mode. Primary purpose of this is to reduce kickback between Channel 0 and Channel 1 and to reduce startup time.			
15	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
14	HIGHCAPLOADEN	0x0	RW	**Channel 1 High Cap Load Mode Enable**
	Enables High Capacitance Load Mode for Channel 1. Should be enabled with VDAC_CH1CFG.POWERMODE=HIGHPOWER.			
13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12:11	FIFODVL	0x0	RW	**Channel 1 FIFO Low Watermark**
	Set Channel 1 Low threshold Data Valid Level (DVL)			
10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:8	REFRESHSOURCE	0x0	RW	**Channel 1 Refresh Source**
	Select Channel 1 Refresh Trigger			

Value	Mode	Description
0	NONE	No Refresh Source Selected
1	REFRESHTIMER	CH1 Refresh Triggered by Refresh Timer Overflow
2	SYNCPRS	CH1 Refresh Triggered by Sync PRS. PRS Trigger should have the same clock group as VDAC.
3	ASYNCPRS	CH1 Refresh Triggered by Async PRS

7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:4	TRIGMODE	0x0	RW	**Channel 1 Trigger Mode**
	Select Channel 1 Conversion Trigger			

Bit	Name	Reset	Access	Description
	Value	Mode		Description
	0	NONE		No Conversion Trigger Source Selected for Channel 1
	1	SW		Channel 1 is triggered by Channel 1 FIFO (CH1F) write
	2	SYNCPRS		Channel 1 is triggered by Sync PRS input.PRS Trigger should have the same clock group as VDAC.
	3	LESENSE		Channel 1 is triggered by LESENSE.
	4	INTERNALTIMER		Channel 1 is triggered by Internal Timer Overflow
	5	ASYNCPRS		Channel 1 is triggered by Async PRS input
3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2	POWERMODE	0x0	RW	**Channel 1 Power Mode**
	Enable Low Power Mode for Channel 1			
	Value	Mode		Description
	0	HIGHPOWER		Default is High Power Mode
	1	LOWPOWER		Set this bit for Low Power Mode
1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	CONVMODE	0x0	RW	**Channel 1 Conversion Mode**
	Configure conversion mode for Channel 1			
	Value	Mode		Description
	0	CONTINUOUS		DAC channel 1 is set in continuous mode
	1	SAMPLEOFF		DAC channel 1 is set in sample/shut off mode

29.5.8 VDAC_CMD - Command Register

Offset	Bit Position																													
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																					0x0	0x0	0x0	0x0			0x0	0x0			0x0	0x0
Access																					W(nB)	W(nB)	W(nB)	W(nB)			W(nB)	W(nB)			W(nB)	W(nB)
Name																					SINEMODESTOP	SINEMODESTART	CH1FIFOFLUSH	CH0FIFOFLUSH			CH1DIS	CH1EN			CH0DIS	CH0EN

Bit	Name	Reset	Access	Description
31:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11	SINEMODESTOP	0x0	W(nB)	**Stop Sine Wave Generation**
	Stop Sine Wave Generation			
10	SINEMODESTART	0x0	W(nB)	**Start Sine Wave Generation**
	Start Sine Wave Generation			
9	CH1FIFOFLUSH	0x0	W(nB)	**CH1 WFIFO Flush**
	Flush Channel 1 WFIFO			
8	CH0FIFOFLUSH	0x0	W(nB)	**CH0 WFIFO Flush**
	Flush Channel 0 WFIFO			
7:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	CH1DIS	0x0	W(nB)	**DAC Channel 1 Disable**
	Disables DAC Channel 1			
4	CH1EN	0x0	W(nB)	**DAC Channel 1 Enable**
	Enables DAC Channel 1			
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	CH0DIS	0x0	W(nB)	**DAC Channel 0 Disable**
	Disables DAC Channel 0			
0	CH0EN	0x0	W(nB)	**DAC Channel 0 Enable**
	Enables DAC Channel 0			

29.5.9 VDAC_IF - Interrupt Flag Register

Offset	Bit Position																													
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset						0x0					0x0	0x0		0x0									0x0	0x0			0x0	0x0			0x0	0x0
Access						RW					RW	RW		RW									RW	RW			RW	RW			RW	RW
Name						ABUSINPUTCONFLICT					CH1DVL	CH0DVL		ABUSALLOCERR									CH1UF	CH0UF			CH1OF	CH0OF			CH1CD	CH0CD

Bit	Name	Reset	Access	Description
31:27	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
26	ABUSINPUTCONFLICT	0x0	RW	**ABUS Input Conflict Error Flag**
	Set if both CH0 and CH1 request same ABUS. Should only be enabled when using ABUS for VDAC Output.			
25:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21	CH1DVL	0x0	RW	**CH1 Data Valid Level Interrupt Flag**
	Set when Channel 1 FIFO Count reaches Data Valid Level. Also used as Wakeup IRQ			
20	CH0DVL	0x0	RW	**CH0 Data Valid Level Interrupt Flag**
	Set when Channel 0 FIFO Count reaches Data Valid Level. Also used as Wakeup IRQ			
19	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
18	ABUSALLOCERR	0x0	RW	**ABUS Port Allocation Error Flag**
	Set if APORT requested is not allocated. Should only be enabled when using ABUS for VDAC Output.			
17:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	CH1UF	0x0	RW	**CH1 Data Underflow Interrupt Flag**
	Indicates channel 1 data underflow.			
8	CH0UF	0x0	RW	**CH0 Data Underflow Interrupt Flag**
	Indicates channel 0 data underflow.			
7:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	CH1OF	0x0	RW	**CH1 Data Overflow Interrupt Flag**
	Indicates channel 1 data overflow.			
4	CH0OF	0x0	RW	**CH0 Data Overflow Interrupt Flag**
	Indicates channel 0 data overflow.			
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

Bit	Name	Reset	Access	Description
1	CH1CD	0x0	RW	**CH1 Conversion Done Interrupt Flag**
	Indicates channel 1 conversion complete.			
0	CH0CD	0x0	RW	**CH0 Conversion Done Interrupt Flag**
	Indicates channel 0 conversion complete.			

29.5.10 VDAC_IEN - Interrupt Enable Register

Offset	Bit Position																													
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset						0x0					0x0	0x0		0x0									0x0	0x0			0x0	0x0			0x0	0x0
Access						RW					RW	RW		RW									RW	RW			RW	RW			RW	RW
Name						ABUSINPUTCONFLICT					CH1DVL	CH0DVL		ABUSALLOCERR									CH1UF	CH0UF			CH1OF	CH0OF			CH1CD	CH0CD

Bit	Name	Reset	Access	Description
31:27	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
26	ABUSINPUTCONFLICT	0x0	RW	**ABUS Input Conflict Interrupt Flag**
	Set to enable the ABUSINPUTCONFLICTIF Interrupt			
25:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21	CH1DVL	0x0	RW	**CH1 Data Valid Level Interrupt Flag**
	Set to enable the CH1DVLIF Interrupt			
20	CH0DVL	0x0	RW	**CH0 Data Valid Level Interrupt Flag**
	Set to enable the CH0DVLIF Interrupt			
19	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
18	ABUSALLOCERR	0x0	RW	**ABUS Allocation Error Interrupt Flag**
	Set to enable the ABUSALLOCERRIF Interrupt			
17:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	CH1UF	0x0	RW	**CH1 Data Underflow Interrupt Flag**
	Set to enable the CH1UFIF Interrupt			
8	CH0UF	0x0	RW	**CH0 Data Underflow Interrupt Flag**
	Set to enable the CH0UFIF Interrupt			
7:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	CH1OF	0x0	RW	**CH1 Data Overflow Interrupt Flag**
	Set to enable the CH1OFIF Interrupt			
4	CH0OF	0x0	RW	**CH0 Data Overflow Interrupt Flag**
	Set to enable the CH0OFIF Interrupt			
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

Bit	Name	Reset	Access	Description
1	CH1CD	0x0	RW	**CH1 Conversion Done Interrupt Flag**
	Set to enable the CH1CDIF Interrupt			
0	CH0CD	0x0	RW	**CH0 Conversion Done Interrupt Flag**
	Set to enable the CH0CDIF Interrupt			

29.5.11 VDAC_CH0F - Channel 0 Data Write Fifo

Offset	Bit Position																															
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																					0x0											
Access																					W											
Name																					DATA											

Bit	Name	Reset	Access	Description
31:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:0	DATA	0x0	W	**Channel 0 Data**
	This register writes the value which will be converted by DAC channel 0 in a FIFO.			

29.5.12 VDAC_CH1F - Channel 1 Data Write Fifo

Offset	Bit Position																															
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																					0x0											
Access																					W											
Name																					DATA											

Bit	Name	Reset	Access	Description
31:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:0	DATA	0x0	W	**Channel 1 Data**
	This register writes the value which will be converted by DAC channel 1 into a FIFO			

29.5.13 VDAC_OUTCTRL - DAC Output Control

Offset	Bit Position																													
0x030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset		0x0						0x0				0x0						0x0					0x0	0x0			0x0	0x0			0x0	0x0
Access		RW						RW				RW						RW					RW	RW			RW	RW			RW	RW
Name		ABUSPINSELCH1						ABUSPORTSELCH1				ABUSPINSELCH0						ABUSPORTSELCH0					SHORTCH1	SHORTCH0			AUXOUTENCH1	AUXOUTENCH0			MAINOUTENCH1	MAINOUTENCH0

Bit	Name	Reset	Access	Description
31	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
30:25	ABUSPINSELCH1	0x0	RW	**CH1 ABUS Pin Select**
	Set this to Select a particular ABUS Pin for Channel 1			
24:22	ABUSPORTSELCH1	0x0	RW	**CH1 ABUS Port Select**
	Set this to Select a particular ABUS Port for Channel 1			

Value	Mode	Description
0	NONE	No GPIO Selected for CH1 ABUS Output
1	PORTA	Port A Selected
2	PORTB	Port B Selected
3	PORTC	Port C Selected
4	PORTD	Port D Selected

21	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
20:15	ABUSPINSELCH0	0x0	RW	**CH0 ABUS Pin Select**
	Set this to Select a particular ABUS Pin for Channel 0			
14:12	ABUSPORTSELCH0	0x0	RW	**CH0 ABUS Port Select**
	Set this to Select a particular ABUS Port for Channel 0			

Value	Mode	Description
0	NONE	No GPIO Selected for CH0 ABUS Output
1	PORTA	Port A Selected
2	PORTB	Port B Selected
3	PORTC	Port C Selected
4	PORTD	Port D Selected

11:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

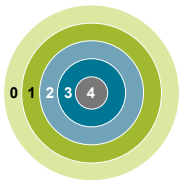
Bit	Name	Reset	Access	Description
9	SHORTCH1	0x0	RW	**CH0 Main and Alternative Output Short**
	Set this to short circuit Main and alternative Output of Channel 0. Usefull to connect Main and Alternative outputs together when DAC is enabled but not warmed up yet.			
8	SHORTCH0	0x0	RW	**CH1 Main and Alternative Output Short**
	Set this to short circuit Main and alternative Output of Channel 1. Usefull to connect Main and Alternative outputs together when DAC is enabled but not warmed up yet.			
7:6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	AUXOUTENCH1	0x0	RW	**CH1 Alternative Output Enable**
	Set this to enable alternative output of Channel 1			
4	AUXOUTENCH0	0x0	RW	**CH0 Alternative Output Enable**
	Set this to enable alternative output of Channel 0			
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	MAINOUTENCH1	0x0	RW	**CH1 Main Output Enable**
	Set this to enable main output of Channel 1			
0	MAINOUTENCH0	0x0	RW	**CH0 Main Output Enable**
	Set this to enable main output of Channel 0			

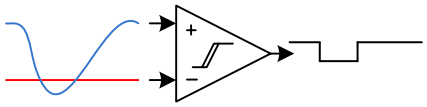
29.5.14 VDAC_OUTTIMERCFG - DAC Out Timer Config Register

Offset	Bit Position																													
0x034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset								0x0															0x0								
Access								RW															RW								
Name								CH1OUTHOLDTIME															CH0OUTHOLDTIME								

Bit	Name	Reset	Access	Description
31:25	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
24:15	CH1OUTHOLDTIME	0x0	RW	**CH1 Output Hold Time**
	Number of prescaled CLK_DAC cycles to drive the output of VDAC for Channel 1			
14:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:0	CH0OUTHOLDTIME	0x0	RW	**CH0 Output Hold Time**
	Number of prescaled CLK_DAC cycles to drive the output of VDAC for Channel 0			

30. ACMP - Analog Comparator





Quick Facts

What?

The ACMP (Analog Comparator) compares two analog signals and returns a digital value telling which is greater.

Why?

Applications often do not need to know the exact value of an analog signal, only if it has passed a certain threshold. Often the voltage must be monitored continuously, which requires extremely low power consumption.

How?

Available down to Energy Mode 3, the ACMP can wake up the system when input signals pass the threshold. The analog comparator can compare two analog signals or one analog signal and a highly configurable internal reference.

30.1 Introduction

The Analog Comparator compares the voltage of two analog inputs and outputs a digital signal indicating which input voltage is higher. Inputs can either be from internal references or from external pins. Response time, and thereby the current consumption, can be configured by altering the current supply to the comparator.

30.2 Features

- Internal and external input selections:
  - External port I/O routed via ABUS
  - Internal 1.25 V bandgap reference voltage with programmable divider
  - Internal 2.5 V bandgap reference voltage with programmable divider
  - AVDD supply voltage with programmable divider
  - VDAC auxiliary outputs
- Voltage supply monitoring
- Configurable hysteresis
- Selectable response time
- Operational in EM0 to EM3
- Capacitive sense mode
- Asynchronous interrupt generation on selectable edges
- Configurable output state when inactive
- Output routing options:
  - Route to GPIO via DBUS
  - Route to most peripherals via PRS
  - Available to LESENSE logic

30.3 Functional Description

An overview of the ACMP is shown in Figure 30.1 ACMP Overview on page 1183.

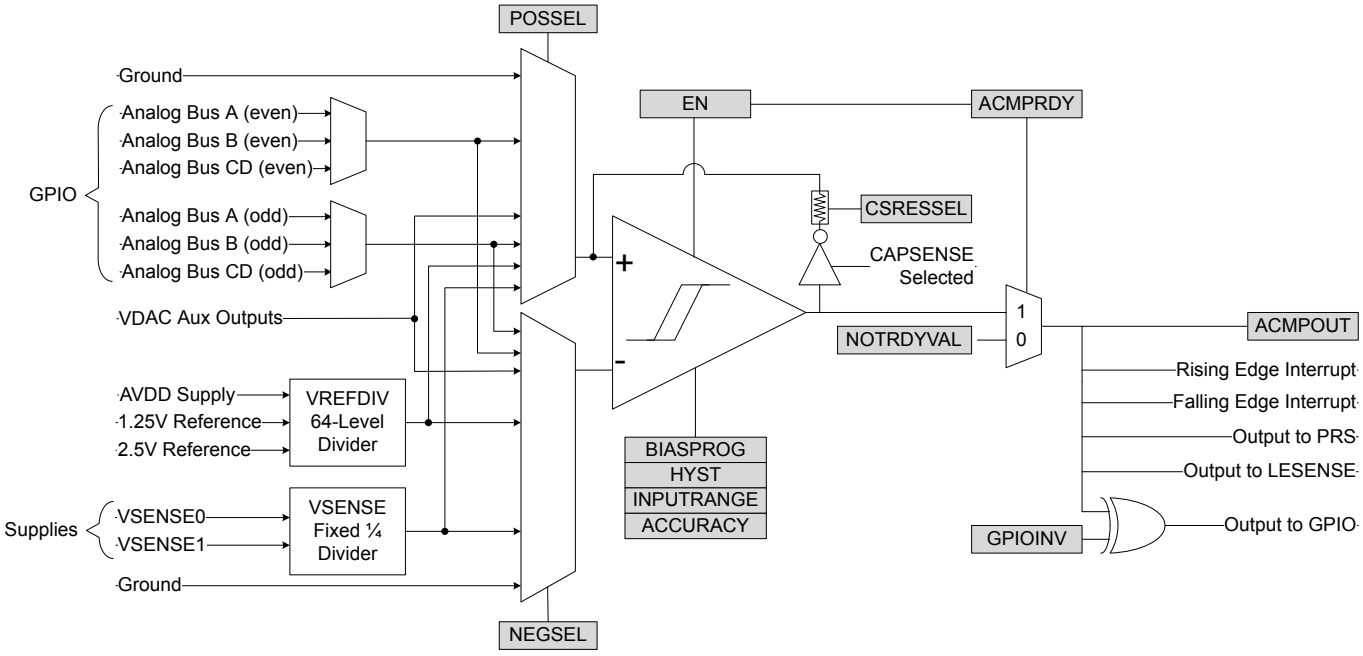


Figure 30.1. ACMP Overview

The comparator has two analog inputs: one positive and one negative. When the comparator is active, the output indicates which of the two input voltages is higher. When the voltage on the positive input is higher than the voltage on the negative input, the digital output is high and vice versa.

In addition to the comparator core, the ACMP front-end includes reference sources, voltage divider circuits, and input muxes to route signals to the positive and negative inputs. There is also a feeback resistor which is used in capacitive sense mode. The output from the ACMP is available on both PRS and GPIO, in addition to being observable in the ACMP_STATUS register.

30.3.1 Configuration and Control

The ACMP is configured and controlled through three registers: ACMP_CFG, ACMP_CTRL, and ACMP_INPUTCTRL. Configuration through ACMP_CFG needs to happen before the ACMP is enabled.The control registers ACMP_CTRL and ACMP_INPUTCTRL can only be updated after the ACMP is enabled. The ACMP is enabled by setting the EN bit in ACMP_EN. If ACMP_CFG is updated when EN = 1, or ACMP_CTRL / ACMP_INPUTCTRL is updated while EN = 0, a bus fault is issued.

The input muxes are configured in the POSSEL / NEGSEL bitfields in ACMP_INPUTCTRL. All references and inputs are available in the modes defined for these two registers. The INPUTCTRL bit in ACMP_SYNCBUSY should be checked before writing to ACMP_INPUTCTRL. If the ACMP_SYNCBUSY_INPUTCTRL bit is 1, it means a previous write to the ACMP_INPUTCTRL register is pending, and software should wait until ACMP_SYNCBUSY_INPUTCTRL bit reads 0.

The POSSEL and NEGSEL muxes share several resources on the device, such as the VREFDIV and VSENSE divider circuits. Thus, there are some constraints on the POSSEL / NEGSEL configurations:

- POSSEL and NEGSEL cannot select an even numbered GPIO pin at the same time.
- POSSEL and NEGSEL cannot select an odd numbered GPIO pin at the same time.
- POSSEL and NEGSEL cannot both select a supply voltage via one of the VSENSE inputs.
- POSSEL and NEGSEL cannot both select an input using VREFDIV.
- If POSSEL = EXTPx, a low power reference (postfixed with LP) cannot be selected for NEGSEL.

If one of these constraints are violated, the INPUTCONFLICT status flag and INPUTCONFLICTIF interrupt flag will be set.

The ACMP also uses shared chip-level analog bus resources to connect to external GPIO pins. Which bus the ACMP is using depends on the configuration of POSSEL and NEGSEL. To allow the ACMP to control an analog bus, the bus must be allocated to ACMP in the GPIO module, using the GPIO_xBUSALLOC registers. For example, pin PB5 is an odd-numbered pin on port PB, and could connect via either analog bus BODD0 or BODD1. This is configured using the BODD0 or BODD1 field in GPIO_BBUSALLOC.

If the ACMP peripheral is trying to access a bus that has not been allocated to that instance of ACMP, the PORTALLOCERR status flag and PORTALLOCERRIF interrupt flag will be set.

30.3.2 Warmup Time

When the comparator is enabled or the input muxes are reconfigured, it requires some time to stabilize. On first enable (ACMP_EN_EN = 1), the comparator core requires 2.5 us to stabilize. In addition to this, any references selected may require some time to warm up. See table Table 30.1 Warmup Time on page 1184 for warmup times for the different references. When reconfiguring the ACMP (without disabling it), only the warmup times given in the table will be observed. When the comparator is ready for use, the ACMPRDY status flag and the ACMPRDYIF interrupt will be set. During the warmup time and when the comparator is inactive, the comparator output will be set to the state defined by the NOTRDYVAL bit in ACMP_CTRL.

Table 30.1. Warmup Time

Reference	Warmup time
Low power reference: POSSEL / NEGSEL = *LP	10 us
VSENSE: POSSEL / NEGSEL = VSENSE*	5 us
VREF: POSSEL / NEGSEL = VREF*	2 us
None of the above	0.5 us

30.3.3 Response Time

There is a delay from when the input voltage changes polarity to when the output toggles. This delay is called the response time and can be altered by increasing or decreasing the bias current to the comparator through the BIASPROG bitfield in the ACMP_CFG register. The current and speed of the circuit increase as the value of BIASPROG is increased. See the part datasheet for specific current and response times releated to setting of BIASPROG.

30.3.4 Hysteresis

When the hysteresis level is set to a non-zero value, the digital output will not toggle until the positive input voltage is at a voltage equal to the hysteresis level above or below the negative input voltage (see Figure 30.2 Hysteresis on page 1185). This feature can be used avoid continual comparator output changes due to input noise when the positive and negative inputs are similar. Hysteresis requires the input difference to exceed the hysteresis threshold before the output can change and can reject limited amounts of noise. The hystersis in ACMP can be configured to three different levels (10 mV, 20 mV, 30 mV), and can be enabled on positive (rising), negative (falling), or both edges. Hysteresis is configured in the HYST bitfield in ACMP_CFG.

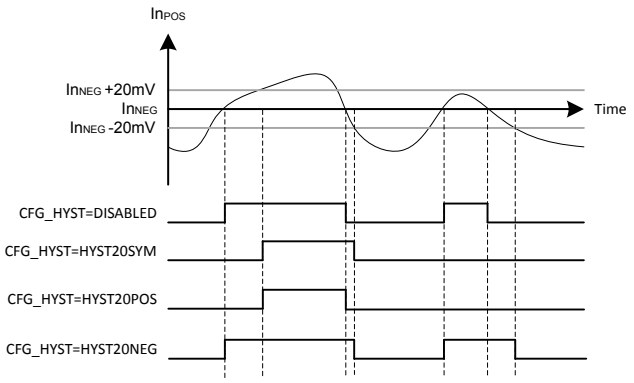


Figure 30.2. Hysteresis

30.3.5 LESENSE Interface

The ACMP can be controlled by LESENSE using its external override interface. In this mode, the LESENSE module will take control of the positive input mux control signal, and possibly the voltage divider, VREFDIV.

To enable this mode, INPUTCTRL_POSSEL needs to be set to EXTPA, EXTPB, EXTPC or EXTPD, according to which GPIO port will be used. In the LESENSE channel configuration, the LESENSE_CHx_INTERACT.OFFSET field will determine which pin on the selected port will be connected for that channel. For example, to connect the positive comparator input to PB03, INPUTCTRL_POSSEL would be set to EXTPB, and LESENSE_CHx_INTERACT.OFFSET to 0x03.

The negative input of the comparator in this mode is still connected according to INPUTCTRL_NEGSEL. LESENSE will take control of the voltage divider VREFDIV setting, if LESENSE_PERCTRL_ACMPxMODE is set to MUXTHRES. For the selected channel, VREFDIV will come from the 6 LSBs of LESENSE_CHx_INTERACT_THRES.

30.3.6 Supply Voltage Monitoring (VSENSE)

The ACMP can be used to monitor supply voltages. This is done by selecting VSENSE01DIV4(LP) or VSENSE11DIV4(LP) for either POSSEL or NEGSEL. Note that the input to the comparator core will be divided by 4, as illustrated in Figure 30.1 ACMP Overview on page 1183. To reduce energy consumption, a sample/hold circuit can be used to periodically sample the power supplies. To enable this, select VSENSE01DIV4LP or VSENSE11DIV4LP in POSSEL / NEGSEL. Because the sample/hold feature uses the comparator in a non-continuous fashion, enabling this will increase response times and reduce the accuracy of the comparator. The connections between VSENSE0 and VSENSE1 to power supplies are summarized in the table below.

Table 30.2. VSENSE connections

ACMP instance	VSENSE0	VSENSE1
ACMP0	AVDD	VDDIO0
ACMP1	DVDD	Not connected

30.3.7 VREFDIV Sources

The ACMP has two internal bandgap references: 2.5 V and 1.25 V. In addition, AVDD can be used as a reference. To select one of these references, configure POSSEL / NEGSEL to VREFDIVAVDD, VREFDIV1V25, or VREFDIV2V5. The ACMP also includes sample/hold functionality to reduce energy consumption. To enable the sample/hold feature, select VREFDIVAVDDLP, VREFDIV1V25LP, or VREFDIV2V5LP. These references can be divided by configuring VREFDIV in ACMP_INPUTCTRL. This division factor will be VREFDIV / 63, such that VREFOUT = VREFIN * (VREFDIV / 63).

30.3.8 Input Range and Accuracy Settings

By default, the ACMP can accept external rail-to-rail inputs, from 0 to AVDD. If external voltages will never be higher than AVDD - 0.7 V, the INPUTRANGE bit in ACMP_CFG can be set to 1 to reduce the power consumption of the block.

The ACMP also has an adjustable accuracy setting (ACCURACY in ACMP_CFG). ACCURACY is set to LOW by default, which conserves power, but may have degraded performance for rapidly changing analog Port selections in either the ACMP or the GPIO. ACCURACY can be set to HIGH to insure ACMP accuracy (at the expense of extra power consumption), when configuration changes are expected at a high rate (more than once per ms, for example), such as when scanning through channels or using the capacitive sense feature.

30.3.9 Capacitive Sense Mode

The analog comparator includes specialized hardware for capacitive sensing of passive push buttons. Such buttons are traces on the PCB laid out in a way that creates a parasitic capacitor between the button and the ground node. Because a human finger will have a small intrinsic capacitance to ground, the capacitance of the button will increase when the button is touched. The capacitance is measured by including the capacitor in a free-running RC oscillator (see Figure 30.3 Capacitive Sense on page 1187). The resistance in this oscillator can be configured through INPUTCTRL_CSRESSEL, see datasheet for resistor values. The frequency produced will decrease when the button is touched compared to when it is not touched. By measuring the output frequency with a timer (via the PRS), the change in capacitance can be detected.

To enable the capacitive sense mode, select CAPSENSE in INPUTCTRL_NEGSEL, and select the pin to measure in INPUTCTRL_POSSEL.

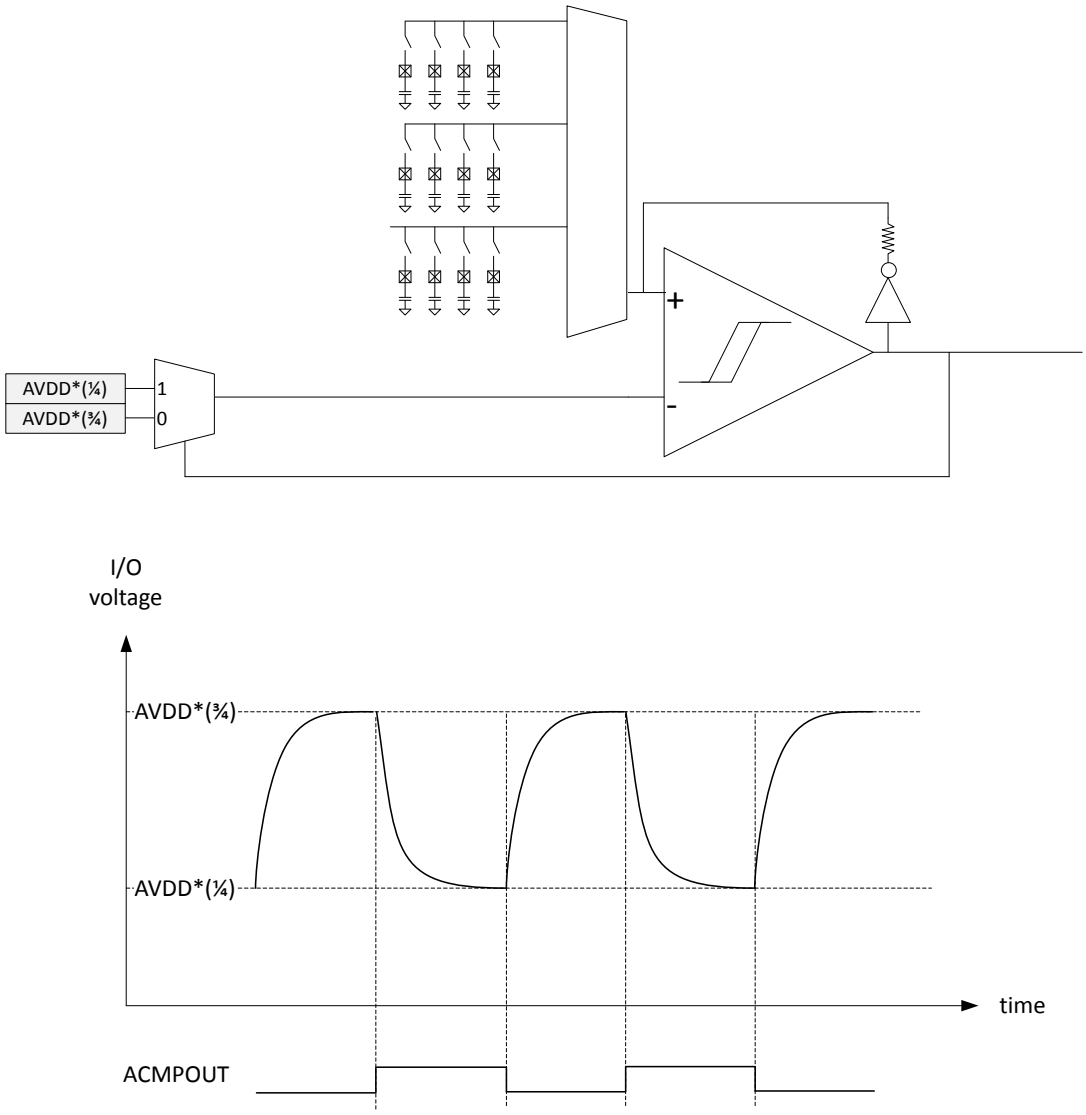


Figure 30.3. Capacitive Sense

30.3.10 Interrupts and PRS Output

The analog comparator includes independent output flags for rising edge (RISEIF) and falling edge (FALLIF) events. These will be set when a rising or falling edge is detected, respectively.

Three other interrupt sources are also available. PORTALLOCERRIF and INPUTCONFLICTIF are input configuration error flags, detailed in 30.3.1 Configuration and Control. The ACMPRDYIF flag indicates comparator stability after a warmup period, as detailed in 30.3.2 Warmup Time.

The comparator output is available as an asynchronous PRS producer, and can be routed to other peripherals in the system via PRS.

30.3.11 Output to GPIO

The output from the comparator and the capacitive sense output are available as alternate functions to the GPIO pins. Each pin connection can be enabled/disabled separately using the GPIO module control registers. See the device data sheet for the available locations for each signal.

The GPIO pin must also be set as output. The output to the GPIO can be inverted by setting the GPIOINV bit in ACMP_CTRL.

30.4 ACMP Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	ACMP_IPVERSION	R	IP Version ID
0x004	ACMP_EN	RW ENABLE	ACMP Enable
0x008	ACMP_SWRST	RW SWRST	Software Reset
0x00C	ACMP_CFG	RW CONFIG	Configuration Register
0x010	ACMP_CTRL	RW	Control Register
0x014	ACMP_INPUTCTRL	RW SYNC	Input Control Register
0x018	ACMP_STATUS	RH	Status Register
0x01C	ACMP_IF	RWH INTFLAG	Interrupt Flag Register
0x020	ACMP_IEN	RW	Interrupt Enable Register
0x024	ACMP_SYNCBUSY	RH	Syncbusy
0x1000	ACMP_IPVERSION_SET	R	IP Version ID
0x1004	ACMP_EN_SET	RW ENABLE	ACMP Enable
0x1008	ACMP_SWRST_SET	RW SWRST	Software Reset
0x100C	ACMP_CFG_SET	RW CONFIG	Configuration Register
0x1010	ACMP_CTRL_SET	RW	Control Register
0x1014	ACMP_INPUTCTRL_SET	RW SYNC	Input Control Register
0x1018	ACMP_STATUS_SET	RH	Status Register
0x101C	ACMP_IF_SET	RWH INTFLAG	Interrupt Flag Register
0x1020	ACMP_IEN_SET	RW	Interrupt Enable Register
0x1024	ACMP_SYNCBUSY_SET	RH	Syncbusy
0x2000	ACMP_IPVERSION_CLR	R	IP Version ID
0x2004	ACMP_EN_CLR	RW ENABLE	ACMP Enable
0x2008	ACMP_SWRST_CLR	RW SWRST	Software Reset
0x200C	ACMP_CFG_CLR	RW CONFIG	Configuration Register
0x2010	ACMP_CTRL_CLR	RW	Control Register
0x2014	ACMP_INPUTCTRL_CLR	RW SYNC	Input Control Register
0x2018	ACMP_STATUS_CLR	RH	Status Register
0x201C	ACMP_IF_CLR	RWH INTFLAG	Interrupt Flag Register
0x2020	ACMP_IEN_CLR	RW	Interrupt Enable Register
0x2024	ACMP_SYNCBUSY_CLR	RH	Syncbusy
0x3000	ACMP_IPVERSION_TGL	R	IP Version ID
0x3004	ACMP_EN_TGL	RW ENABLE	ACMP Enable
0x3008	ACMP_SWRST_TGL	RW SWRST	Software Reset
0x300C	ACMP_CFG_TGL	RW CONFIG	Configuration Register
0x3010	ACMP_CTRL_TGL	RW	Control Register

Offset	Name	Type	Description
0x3014	ACMP_INPUTCTRL_TGL	RW SYNC	Input Control Register
0x3018	ACMP_STATUS_TGL	RH	Status Register
0x301C	ACMP_IF_TGL	RWH INTFLAG	Interrupt Flag Register
0x3020	ACMP_IEN_TGL	RW	Interrupt Enable Register
0x3024	ACMP_SYNCBUSY_TGL	RH	Syncbusy

30.5 ACMP Register Description

30.5.1 ACMP_IPVERSION - IP Version ID

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x3																															
Access	R																															
Name	IPVERSION																															

Bit	Name	Reset	Access	Description
31:0	IPVERSION	0x3	R	**IP version ID**

30.5.2 ACMP_EN - ACMP Enable

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	RW
Name																															DISABLING	EN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DISABLING	0x0	R	**Disablement busy status** When En is cleared, DISABLING is set immediately, and cleared when disablement finishes. Disablement resets peripheral cores and not APB registers except hardware updated registers such as INTFLAGs and FIFOs.
0	EN	0x0	RW	**Module enable** The ENABLE bit enables the module. Software should write to CONFIG type registers before setting the ENABLE bit. Software should write to SYNC type registers only after setting the ENABLE bit.

30.5.3 ACMP_SWRST - Software Reset

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	W
Name																															RESETTING	SWRST

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	RESETTING	0x0	R	**Software reset busy status**
0	SWRST	0x0	W	**Software reset**

30.5.4 ACMP_CFG - Configuration Register

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset															0x0	0x0						0x0									0x4	
Access															RW	RW						RW									RW	
Name															ACCURACY	INPUTRANGE						HYST									BIAS	

Bit	Name	Reset	Access	Description
31:18	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
17	ACCURACY	0x0	RW	**ACMP accuracy mode**

Setting ACCURACY to HIGH reduces the noise in the signal input path of the ACMP. Note, high frequency changes can cause the ACMP performance to degrade. For such uses, such as quickly scanning through multiple channels or setting the ACMP to oscillate for capacitive sense, this should be set to HIGH.

Value	Mode	Description
0	LOW	ACMP operates in low-accuracy mode but consumes less current.
1	HIGH	ACMP operates in high-accuracy mode but consumes more current.

Bit	Name	Reset	Access	Description
16	INPUTRANGE	0x0	RW	**Input Range**

Adjust performance of the comparator for a given input voltage range.

Value	Mode	Description
0	FULL	Use this setting when the input to the comparator core can be from 0 to AVDD.
1	REDUCED	It is recommended to use this setting when the input to the comparator core will always be less than AVDD-0.7V.

Bit	Name	Reset	Access	Description
15:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:8	HYST	0x0	RW	**Hysteresis mode**

Set hysteresis mode and level.

Value	Mode	Description
0	DISABLED	Hysteresis disabled
1	SYM10MV	10mV symmetrical hysteresis
2	SYM20MV	20mV symmetrical hysteresis
3	SYM30MV	30mV symmetrical hysteresis
4	POS10MV	10mV hysteresis on positive edge transitions
5	POS20MV	20mV hysteresis on positive edge transitions

Bit	Name	Reset	Access	Description
	6	POS30MV		30mV hysteresis on positive edge transitions
	8	NEG10MV		10mV hysteresis on negative edge transitions
	9	NEG20MV		20mV hysteresis on negative edge transitions
	10	NEG30MV		30mV hysteresis on negative edge transitions
7:3	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
2:0	BIAS	0x4	RW	**Bias Configuration**
	These bits control the bias current level. See the datasheet for details.			

30.5.5 ACMP_CTRL - Control Register

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															RW	RW
Name																															GPIOINV	NOTRDYVAL

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	GPIOINV	0x0	RW	**Comparator GPIO Output Invert**
	Set this bit to 1 to invert the comparator alternate function output to GPIO.			
	Value	Mode		Description
	0	NOTINV		The comparator output to GPIO is not inverted
	1	INV		The comparator output to GPIO is inverted
0	NOTRDYVAL	0x0	RW	**Not Ready Value**
	The value of this bit is used as the comparator output when the comparator is not ready.			
	Value	Mode		Description
	0	LOW		ACMP output is 0 when the ACMP is not ready.
	1	HIGH		ACMP output is 1 when the ACMP is not ready.

30.5.6 ACMP_INPUTCTRL - Input Control Register

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset		0x0									0x0						0x0								0x0							
Access		RW									RW						RW								RW							
Name		CSRESSEL									VREFDIV						NEGSEL								POSSEL							

Bit	Name	Reset	Access	Description
31	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
30:28	CSRESSEL	0x0	RW	**Capacitive Sense Mode Internal Resistor**

These bits select the resistance value for the internal capacitive sense resistor. Resulting actual resistor values are given in the device datasheets.

Value	Mode	Description
0	RES0	Internal capacitive sense resistor value 0
1	RES1	Internal capacitive sense resistor value 1
2	RES2	Internal capacitive sense resistor value 2
3	RES3	Internal capacitive sense resistor value 3
4	RES4	Internal capacitive sense resistor value 4
5	RES5	Internal capacitive sense resistor value 5
6	RES6	Internal capacitive sense resistor value 6

27:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21:16	VREFDIV	0x0	RW	**VREF division**

Set division factor for VREFDIV. VREFOUT = VREFIN * (VREFDIV / 63)

15:8	NEGSEL	0x0	RW	**Negative Input Select**

Select negative input.

Value	Mode	Description
0	VSS	VSS
16	VREFDIVAVDD	Divided AVDD
17	VREFDIVAVDDLP	Low-Power Divided AVDD
18	VREFDIV1V25	Divided 1V25 reference
19	VREFDIV1V25LP	Low-power Divided 1V25 reference
20	VREFDIV2V5	Divided 2V5 reference
21	VREFDIV2V5LP	Low-power Divided 2V5 reference
32	VSENSE01DIV4	VSENSE0 divided by 4

Bit	Name	Reset	Access	Description
	33	VSENSE01DIV4LP		Low-power VSENSE0 divided by 4
	34	VSENSE11DIV4		VSENSE1 divided by 4
	35	VSENSE11DIV4LP		Low-power VSENSE1 divided by 4
	48	CAPSENSE		Capsense mode
	64	VDACOUT0		VDAC0 channel 0 output
	65	VDACOUT1		VDAC0 channel 1 output
	128	PA0		Port A, Pin0
	129	PA1		Port A, Pin1
	130	PA2		Port A, Pin2
	131	PA3		Port A, Pin3
	132	PA4		Port A, Pin4
	133	PA5		Port A, Pin5
	134	PA6		Port A, Pin6
	135	PA7		Port A, Pin7
	136	PA8		Port A, Pin8
	137	PA9		Port A, Pin9
	138	PA10		Port A, Pin10
	139	PA11		Port A, Pin11
	140	PA12		Port A, Pin12
	141	PA13		Port A, Pin13
	142	PA14		Port A, Pin14
	143	PA15		Port A, Pin15
	144	PB0		Port B, Pin0
	145	PB1		Port B, Pin1
	146	PB2		Port B, Pin2
	147	PB3		Port B, Pin3
	148	PB4		Port B, Pin4
	149	PB5		Port B, Pin5
	150	PB6		Port B, Pin6
	151	PB7		Port B, Pin7
	152	PB8		Port B, Pin8
	153	PB9		Port B, Pin9
	154	PB10		Port B, Pin10
	155	PB11		Port B, Pin11
	156	PB12		Port B, Pin12
	157	PB13		Port B, Pin13
	158	PB14		Port B, Pin14

Bit	Name	Reset	Access	Description
	159	PB15		Port B, Pin15
	160	PC0		Port C, Pin0
	161	PC1		Port C, Pin1
	162	PC2		Port C, Pin2
	163	PC3		Port C, Pin3
	164	PC4		Port C, Pin4
	165	PC5		Port C, Pin5
	166	PC6		Port C, Pin6
	167	PC7		Port C, Pin7
	168	PC8		Port C, Pin8
	169	PC9		Port C, Pin9
	170	PC10		Port C, Pin10
	171	PC11		Port C, Pin11
	172	PC12		Port C, Pin12
	173	PC13		Port C, Pin13
	174	PC14		Port C, Pin14
	175	PC15		Port C, Pin15
	176	PD0		Port D, Pin0
	177	PD1		Port D, Pin1
	178	PD2		Port D, Pin2
	179	PD3		Port D, Pin3
	180	PD4		Port D, Pin4
	181	PD5		Port D, Pin5
	182	PD6		Port D, Pin6
	183	PD7		Port D, Pin7
	184	PD8		Port D, Pin8
	185	PD9		Port D, Pin9
	186	PD10		Port D, Pin10
	187	PD11		Port D, Pin11
	188	PD12		Port D, Pin12
	189	PD13		Port D, Pin13
	190	PD14		Port D, Pin14
	191	PD15		Port D, Pin15
7:0	POSSEL	0x0	RW	**Positive Input Select**
	Select positive input.			
	Value	Mode		Description

Bit	Name	Reset	Access	Description
	0	VSS		VSS
	16	VREFDIVAVDD		Divided AVDD
	17	VREFDIVAVDDLP		Low-Power Divided AVDD
	18	VREFDIV1V25		Divided 1V25 reference
	19	VREFDIV1V25LP		Low-power Divided 1V25 reference
	20	VREFDIV2V5		Divided 2V5 reference
	21	VREFDIV2V5LP		Low-power Divided 2V5 reference
	32	VSENSE01DIV4		VSENSE0 divided by 4
	33	VSENSE01DIV4LP		Low-power VSENSE0 divided by 4
	34	VSENSE11DIV4		VSENSE1 divided by 4
	35	VSENSE11DIV4LP		Low-power VSENSE1 divided by 4
	64	VDACOUT0		VDAC0 channel 0 output
	65	VDACOUT1		VDAC0 channel 1 output
	80	EXTPA		External interface, base is PA0.
	81	EXTPB		External interface, base is PB0.
	82	EXTPC		External interface, base is PC0.
	83	EXTPD		External interface, base is PD0.
	128	PA0		Port A, Pin0
	129	PA1		Port A, Pin1
	130	PA2		Port A, Pin2
	131	PA3		Port A, Pin3
	132	PA4		Port A, Pin4
	133	PA5		Port A, Pin5
	134	PA6		Port A, Pin6
	135	PA7		Port A, Pin7
	136	PA8		Port A, Pin8
	137	PA9		Port A, Pin9
	138	PA10		Port A, Pin10
	139	PA11		Port A, Pin11
	140	PA12		Port A, Pin12
	141	PA13		Port A, Pin13
	142	PA14		Port A, Pin14
	143	PA15		Port A, Pin15
	144	PB0		Port B, Pin0
	145	PB1		Port B, Pin1
	146	PB2		Port B, Pin2
	147	PB3		Port B, Pin3

Bit	Name	Reset	Access	Description
	148	PB4		Port B, Pin4
	149	PB5		Port B, Pin5
	150	PB6		Port B, Pin6
	151	PB7		Port B, Pin7
	152	PB8		Port B, Pin8
	153	PB9		Port B, Pin9
	154	PB10		Port B, Pin10
	155	PB11		Port B, Pin11
	156	PB12		Port B, Pin12
	157	PB13		Port B, Pin13
	158	PB14		Port B, Pin14
	159	PB15		Port B, Pin15
	160	PC0		Port C, Pin0
	161	PC1		Port C, Pin1
	162	PC2		Port C, Pin2
	163	PC3		Port C, Pin3
	164	PC4		Port C, Pin4
	165	PC5		Port C, Pin5
	166	PC6		Port C, Pin6
	167	PC7		Port C, Pin7
	168	PC8		Port C, Pin8
	169	PC9		Port C, Pin9
	170	PC10		Port C, Pin10
	171	PC11		Port C, Pin11
	172	PC12		Port C, Pin12
	173	PC13		Port C, Pin13
	174	PC14		Port C, Pin14
	175	PC15		Port C, Pin15
	176	PD0		Port D, Pin0
	177	PD1		Port D, Pin1
	178	PD2		Port D, Pin2
	179	PD3		Port D, Pin3
	180	PD4		Port D, Pin4
	181	PD5		Port D, Pin5
	182	PD6		Port D, Pin6
	183	PD7		Port D, Pin7
	184	PD8		Port D, Pin8

Bit	Name	Reset	Access	Description
	185	PD9		Port D, Pin9
	186	PD10		Port D, Pin10
	187	PD11		Port D, Pin11
	188	PD12		Port D, Pin12
	189	PD13		Port D, Pin13
	190	PD14		Port D, Pin14
	191	PD15		Port D, Pin15

30.5.7 ACMP_STATUS - Status Register

Offset	Bit Position																															
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0		0x0
Access																												R	R	R		R
Name																												PORTALLOCERR	INPUTCONFLICT	ACMPRDY		ACMPOUT

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	PORTALLOCERR	0x0	R	**Port allocation error**
	The port selected by INPUTCTRL_POSSEL or INPUTCTRL_NEGSEL is not allocated to this ACMP. Port allocation needs to be configured in the GPIO module.			
3	INPUTCONFLICT	0x0	R	**INPUT conflict**
	INPUTCTRL_POSSEL and INPUTCTRL_NEGSEL is configured illegally.			
2	ACMPRDY	0x0	R	**Analog Comparator Ready**
	Analog comparator ready status.			
1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	ACMPOUT	0x0	R	**Analog Comparator Output**
	Analog comparator output value.			

30.5.8 ACMP_IF - Interrupt Flag Register

Offset	Bit Position																														
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												RW	RW	RW	RW	RW
Name																												PORTALLOCERR	INPUTCONFLICT	ACMPRDY	FALL	RISE

Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	PORTALLOCERR	0x0	RW	**Port allocation error**
	The port selected by INPUTCTRL_POSSEL or INPUTCTRL_NEGSEL is not allocated to this ACMP. Port allocation needs to be configured in the GPIO module.			
3	INPUTCONFLICT	0x0	RW	**Input conflict**
	INPUTCTRL_POSSEL and INPUTCTRL_NEGSEL is configured illegally.			
2	ACMPRDY	0x0	RW	**ACMP ready Interrupt flag**
	Indicates that the analog comparator is ready and references have settled.			
1	FALL	0x0	RW	**Falling Edge Triggered Interrupt Flag**
	Indicates that there has been a falling edge on the analog comparator output.			
0	RISE	0x0	RW	**Rising Edge Triggered Interrupt Flag**
	Indicates that there has been a rising edge on the analog comparator output.			

30.5.9 ACMP_IEN - Interrupt Enable Register

Offset	Bit Position																														
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																												0x0	0x0	0x0	0x0	0x0
Access																												RW	RW	RW	RW	RW
Name																												PORTALLOCERR	INPUTCONFLICT	ACMPRDY	FALL	RISE

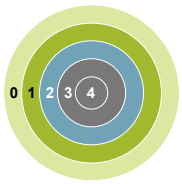
Bit	Name	Reset	Access	Description
31:5	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
4	PORTALLOCERR	0x0	RW	**Port allocation error interrupt enable**
3	INPUTCONFLICT	0x0	RW	**Input conflict interrupt enable**
2	ACMPRDY	0x0	RW	**ACMP ready interrupt enable**
1	FALL	0x0	RW	**Falling edge interrupt enable**
0	RISE	0x0	RW	**Rising edge interrupt enable**

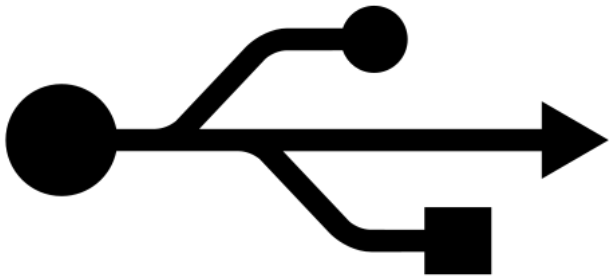
30.5.10 ACMP_SYNCBUSY - Syncbusy

Offset	Bit Position																														
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																R
Name																																INPUTCTRL

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	INPUTCTRL	0x0	R	**Syncbusy for INPUTCTRL**
	Synchronization of INPUTCTRL ongoing			

31. USB - Universal Serial Bus Controller





Quick Facts

What?

The USB is a full-speed/low-speed USB 2.0 compliant USB Controller that can be used as a USB Device. An external 3.3 V regulator is required.

Why?

USB provides a robust, industry-standard way to interface to PCs and other portable devices.

How?

The flexible and highly software-configurable architecture of the USB Controller makes it easy to implement USB device solutions. The on-chip PHY has software controllable internal pull-up and pull-down resistors. Third-party USB software stacks are also available, reducing the development time substantially. By utilizing the very low energy consumption in EM2, the USB device will be able to wake up and perform tasks several times a second without violating the 2.5 mA maximum average current during suspend.

31.1 Introduction

The USB is a full-speed/low-speed USB 2.0 compliant device controller. An external 3.3 V regulator is required to supply IOVDD2.

31.2 Features

- Fully compliant with Universal Serial Bus Specification, Revision 2.0
- Supports full-speed (12 MBit/s) and low-speed (1.5 MBit/s) devices
- Low Energy Mode, reducing average current consumption by up to 90%
- Dedicated Internal DMA Controller
- 10 Endpoints (9 software-configurable Bulk IN/OUT or Interrupt endpoints + 1 CTRL IN (Endpoint 0))
- 3 kB endpoint memory
- Resume/Reset detection in EM2 (during suspend)
- Session Request Protocol (SRP) detection in EM2 (during host session off) using data-line pulsing
- Soft connect/disconnect
- On-chip PHY
  - Internal pull-up and pull-down resistors

31.3 USB System Description

The USB is device-only and consists of a MAC, a 3 kB endpoint RAM, PHY and a 48 MHz PLL (USBPLL0). This USB implementation depends on an external regulator to convert from 5 V VBUS to 3.3 V. The digital logic of the USB is split into three blocks: USB core, USB PHY control, and USBPLL0 control. The USB core is clocked by the 48 MHz USBPLL0 and is accessed using an AHB secondary interface and APB interface. The AHB secondary interface is used for accessing the FIFO contents and the registers in the core starting at offset 0xDE000. An additional main interface is used by the internal DMA controller of the core. The core takes care of all the USB protocol related functionality. The USB0CLK (48 MHz clock from USBPLL0) must not be disabled when the core is active - in order to access the USB system registers, the USB0CLK must be enabled. The USB PHY is controlled by the USB APB interface registers. The USBPLL0 has its own APB interface for control of the USBPLL0. The USBPLL0 on startup is clocked by the 20 MHz FSRCO internal oscillator.

31.3.1 USB Pins

There are several pins associated with the USB.

- USB_DP (USB D+) and USB_DM (USB D-) are the USB data signaling pins.
- IOVDD2 is the IO supply pin for the USB pins - it must be driven from an external 3.3 V regulator
- VBUS_SENSE could be applied to any GPIO pin and is used to indicate to the integrated USB controller whether or not VBUS is present. A set of resistors connected as a voltage divider can be used to avoid exceeding the max allowable voltage on the GPIO pin.

31.3.2 USB Initialization

Follow these steps to enable the USB:

1. First configure the USBPLL0:

```
  // Enable Bus Clock
  CMU->CLKEN1 |= CMU_CLKEN1_USB

  // Configure PLL DIV setting based on refclk (HFXO) freq
  // Below is the code for refclk of 38.4MHz
  USBPLL0->CTRL &= ~(_USBPLL_CTRL_DIVN_MASK | _USBPLL_CTRL_DIVR_MASK | _USBPLL_CTRL_DIVX_MASK);
  USBPLL0->CTRL |= ((1 <<  _USBPLL_CTRL_DIVR_SHIFT) |
                (25 << _USBPLL_CTRL_DIVX_SHIFT) |
                (20 << _USBPLL_CTRL_DIVN_SHIFT)
                );

  // Enable HFXO on demand to allow hardware request
  HFXO0->CTRL_CLR = HFXO_CTRL_DISONDEMAND;

  //Enable LOCK interrupt
  USBPLL0->IEN = USBPLL_IEN_PLLLOCKIEN;

  // Enable USBPLL IRQ
  NVIC_EnableIRQ(USBPLL0_IRQn);
```

2. Then enable the USB in the CMU:

```
  // Select PLL as clock source
  CMU->USB0CLKCTRL = CMU_USB0CLKCTRL_CLKSEL_USBPLL0;

  // Once USB is enabled, clock is requested from PLL which
  // initiates PLL start up sequence
  USB_APBS->EN = USB_EN_EN;

  // Wait till USBPLL is locked
  while(!is_usbpll_rdy);

void USBPLL0_IRQHandler(void) {
  if (USBPLL0->IF & USBPLL_IF_PLLLOCKIF) is_usbpll_rdy = 1;
  USBPLL0->IF_CLR = _USBPLL_IF_MASK;
}
```

3. Then enable VBUS_SENSE and await an attach event:

```
  // Enable USB IRQ
  USB_APBS->IEN |= USB_IEN_VBUSIEN;
  NVIC_EnableIRQ(USB_IRQn);

  // Enable VBUS high detect and clear low detect
  USB_APBS->CTRL |= USB_CTRL_VBSSNSHEN;
  USB_APBS->CTRL &= ~(_USB_CTRL_VBSSNSLEN_MASK);

  // Disable retiming if enabled before the next step
  // This step is required only if an attach event is expected in EM2
  // Clear VBUS override so that USBPLL clock is not requested
  USB_APBS->CTRL &= ~(_USB_CTRL_VBUSOVRIDE_MASK);
  // Optionally Enter EM2 and wait for VBUS event
  Enter_EM2();

  // After wakeup, read status to check if its valid
  USB_APBS->STATUS == USB_STATUS_VBUSVALID;
  // Clear high en and enable Low enable
  USB_APBS->CTRL |= USB_CTRL_VBSSNSLEN;
  USB_APBS->CTRL &= ~(_USB_CTRL_VBSSNSHEN_MASK);

  // Do the device initialization and continue with USB reset
```

31.3.3 Power Configurations

The USB can be used in device mode only. The diagrams shown below describe the various implementations.

31.3.3.1 Bus-powered Device

In this configuration, the device will derive all its power from VBUS. External regulators are required to step down the 5 V VBUS supply to the desired nominal voltage for all supply pins. Whenever the 5V VBUS supply is at a valid level, IOVDD2 will be supplied by an external 3.3 V regulator. Per the USB specification VBUS_SENSE is not required in this mode.

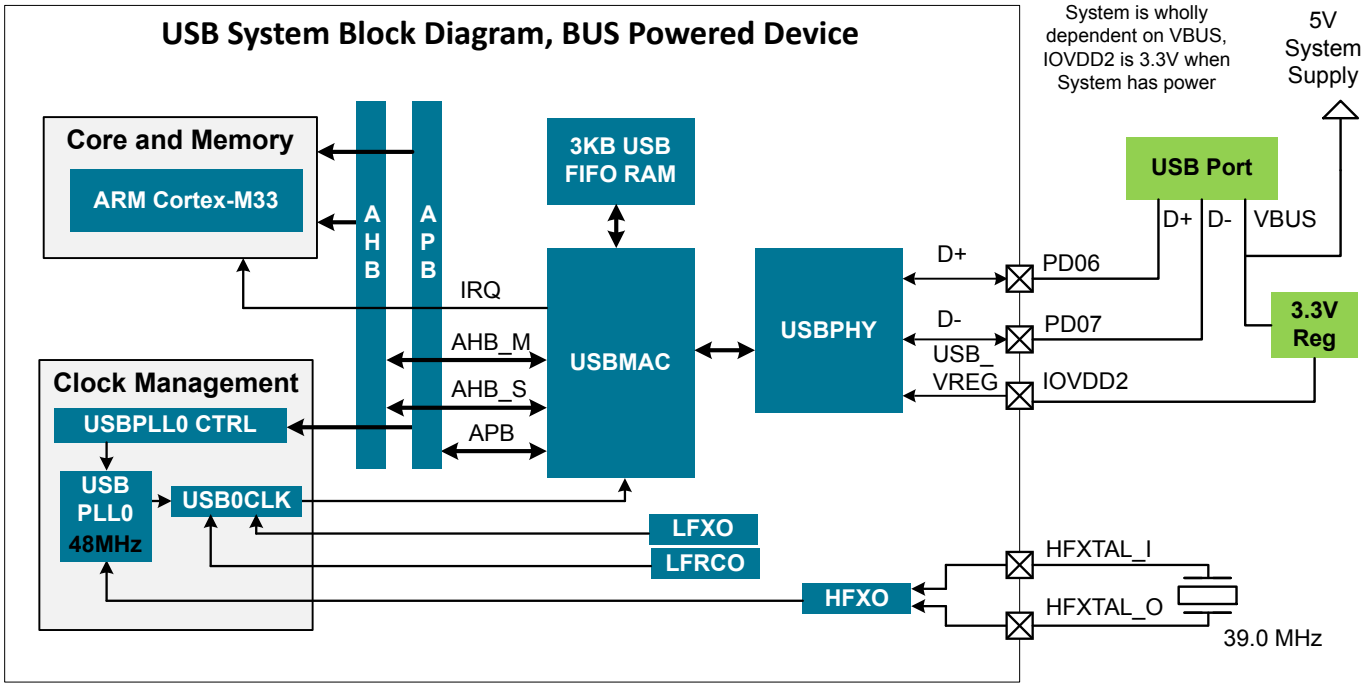


Figure 31.1. Bus-powered Device

31.3.3.2 Self-powered Device

In this power configuration, system power is derived from a source other than 5 V VBUS. An external regulator must supply 3.3 V to IOVDD2. This regulator shall receive power from the system power source, and IOVDD2 must be supplied when the system is powered, as shown in Figure 31.2 Self-powered Device on page 1206. In this configuration, the VBUS_SENSE signal must be routed to a GPIO and connected as shown, in order to indicate when VBUS is present and when it is disconnected. The connected GPIO must be indicated in firmware. Also, the voltage applied to this GPIO must not exceed the max allowable, and it must be high enough to be detected as logic high (> V_{IH} Min). A typical method to create this VBUS_SENSE signal from VBUS is to use voltage divider resistors.

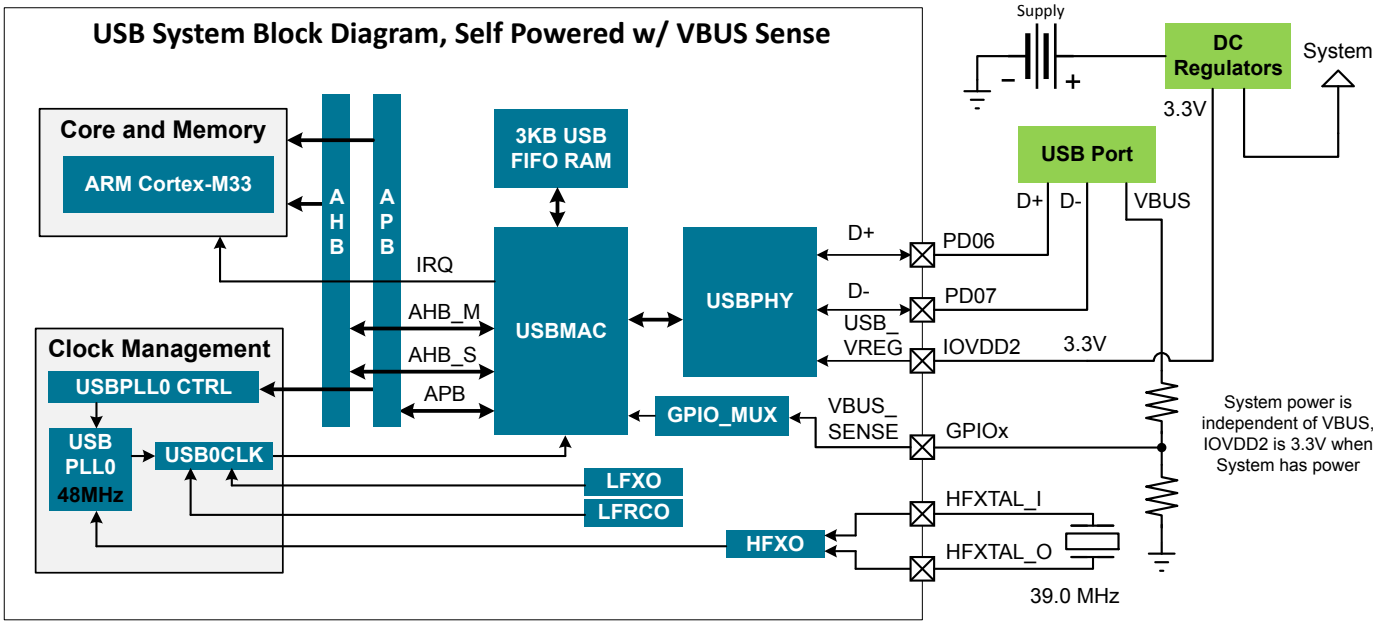


Figure 31.2. Self-powered Device

31.3.4 USB PHY

The USB includes an internal full-speed/low-speed PHY with built-in pull-up/pull-down resistors. During suspend, the PHY enters a low-power state where only the single-ended receivers are active. The PHY is disabled by default and should be enabled by setting PHY_EN in the USB APB interface.

The PHY is powered by IOVDD2, which must be connected to an external 3.3 V regulator.

31.3.5 Interrupts

The USB block generates one interrupt back to the M33 core. There are two IRQs generated in the APB that trigger the IRQ to the M33 core. One of these is the VBUS_SENSE and the other is the DWCOTGIRQ which is an OR-ing of the IRQs from the USB MAC. The USB MAC has a description of the IRQs it generates. When clearing these IRQs, one must clear the IRQ in the USB MAC first, and once all IRQs are cleared there then clear the IRQ in the APB register (USB_IF).

31.3.6 USB Energy Mode Support

31.3.6.1 USB in EM2

EM2 cannot be used when the USB is active - however, EM2 may be used in USB Suspend mode to reduce power consumption. Refer to 31.4.5 USB Suspend Mode for more details on USB Suspend along with code examples

31.3.6.2 USB in EM3

EM3 cannot be used when the USB is active.

31.3.6.3 USB in EM4

EM4 cannot be used when the USB is active.

31.4 USB Core Description

- Full Speed/Low Speed
- USB 2.0 Spec compliance
- Device mode only
- On chip FS(Full Speed)/LS(Low Speed) PHY
- 12 Mbps FS mode, 1.5 Mbps LS mode
- 3.3 V nominal, 2.7 V min
- Built in series resistors which can be disabled to have short circuit capability
- 10 Endpoints (9 software-configurable Bulk IN/OUT or Interrupt endpoints + 1 CTRL IN (Endpoint 0))
- VBUS sense (via GPIO_MUX to any GPIO)
- External resistor divider for 5 V tolerance
- Suspend mode current is less than 2.4 mA
- 5 V operation using an external 5 V → 3.3 V LDO
- Supported clocking options: USBPLL0 supports all system supported XTAL frequencies, uses LFXO/LFRCO (32 kHz) in suspend
- Supports any AHB bus frequency greater than 30 MHz
- Uses a 3 KB FIFO buffer
- Support for remote wakeup
- Supports self-powered and bus-powered operation
- Output from external LDO will drive into pin IOVDD2 on chip

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31.4.1 Overview: Programming the Core

Each significant programming feature of the core is discussed in a separate section.

This chapter uses abbreviations for register names and their fields. For detailed information on registers, see 31.6 USB_APBS Register Description and 31.8 USBAHB_AHBS Register Description.

The application must perform a core initialization sequence.

This section explains the initialization of the core after power-on. The application must follow the initialization. All core global registers are initialized according to the core's configuration.

1. Program the following fields in the Global AHB Configuration (USBAHB_GAHBCFG) register.
   - DMA Mode bit
   - AHB Burst Length field
   - Global Interrupt Mask bit = 1
   - Periodic TxFIFO Empty Level (can be enabled only when the core is operating in Device mode)
2. Program the following field in the Global Interrupt Mask (USBAHB_GINTMSK) register:
   - USBAHB_GINTMSK.RXFLVLMSK = 0
3. Program the following fields in USBAHB_GUSBCFG register.
   - Internal Full-Speed Serial PHY Selection bit
   - Time-Out Calibration field
   - USB Turnaround Time field
4. The software must unmask the following bit in the USBAHB_GINTMSK register.
   - Mode Mismatch Interrupt Mask
5. The software follows 31.4.1.1 Device Initialization sequence.

Note:

- The core is designed to be interrupt-driven. Polling interrupt mechanism is not recommended: this may result in undefined resolutions.
- In device mode, just after Power On Reset or a Soft Reset, the USBAHB_GINTSTS.SOF bit is set to 1 for debug purposes. This status must be cleared and can be ignored.

31.4.1.1 Device Initialization

The application must perform the following steps to initialize the core at device on or power on.

1. Program the following fields in USBAHB_DCFG register.
   - Device Speed
   - NonZero Length Status OUT Handshake
   - Periodic Frame Interval
2. Program the USBAHB_GINTMSK register to unmask the following interrupts.
   - USB Reset
   - Enumeration Done
   - Early Suspend
   - USB Suspend
3. Wait for the USBAHB_GINTSTS.USBRST interrupt, which indicates a reset has been detected on the USB and lasts for about 10 ms. On receiving this interrupt, the application must perform the steps listed in 31.4.3.1.1 Initialization on USB Reset
4. Wait for the USBAHB_GINTSTS.ENUMDONE interrupt. This interrupt indicates the end of reset on the USB. On receiving this interrupt, the application must read the USBAHB_DSTS register to determine the enumeration speed and perform the steps listed in 31.4.3.1.2 Initialization on Enumeration Completion

At this point, the device is ready to accept SOF packets and perform control transfers on control endpoint 0.

31.4.1.1.1 Device Connection

Bus powered configuration: Upon a power-on-reset (plug in event) USB will wake up and await enumeration.

Self-powered configuration: USB will await VBUS_SENSE which will generate an IRQ to the core at which time a driver should wake up the USB and await enumeration.

31.4.1.1.2 Device Disconnection

The device session ends when the USB cable is disconnected or if the VBUS is switched off by the Host.

The device detach sequence looks as follows:

```
// Clear high enable and enable low enable
USB_APBS->CTRL |= USB_CTRL_VBSSNSLEN;
USB_APBS->CTRL &= ~(_USB_CTRL_VBSSNSHEN_MASK);
USB_APBS->CTRL |= USB_CTRL_VBUSOVRIDE_MASK;

//============================================================
// Below steps are for the case when there is a suspend from host
// At this point, VBUS is already high and we received a suspend IRQ
// Do the suspend init sequence to switch clocks, disable retiming
suspend_seq();
Enter_EM2();
//============================================================

// After wakeup, do a soft reset of the IP core and optionally disable USB
USBAHB->GRSTCTL |= (USBAHB_GRSTCTL_CSFTRST);
while(USBAHB->GRSTCTL & USBAHB_GRSTCTL_CSFTRST);
USB_APBS->EN = _USB_EN_RESETVALUE;
while (USB->EN & USB_EN_DISABLING);
```

31.4.1.1.3 Device Soft Disconnection

The application can perform a soft disconnect by setting the Soft disconnect bit (SFTDISCON) in Device Control Register (USBAHB_DCTL).

Send/Receive USB Transfers → Soft disconnect → Soft reset → USB Device Enumeration

Sequence of operations:

1. The application configures the device to send or receive transfers.
2. The application sets the Soft disconnect bit (SFTDISCON) in the Device Control Register (USBAHB_DCTL).
3. The application sets the Soft Reset bit (CSFTRST) in the Reset Register (USBAHB_GRSTCTL).
4. Poll the USBAHB_GRSTCTL register until the core clears the soft reset bit, which ensures the soft reset is completed properly.
5. Initialize the core according to the instructions in 31.4.1.1 Device Initialization.

Suspend → Soft disconnect → Soft reset → USB Device Enumeration

Sequence of operations:

1. The core detects a USB suspend and generates a Suspend Detected interrupt.
2. The application sets the Stop PHY Clock bit in the Power and Clock Gating Control register, the core puts the PHY in suspend mode, and the PHY clock stops.
3. The application clears the Stop PHY Clock bit in the Power and Clock Gating Control register, and waits for the PHY clock to come back. The core takes the PHY back to normal mode, and the PHY clock comes back.
4. The application sets the Soft disconnect bit (SFTDISCON) in Device Control Register (USBAHB_DCTL).
5. The application sets the Soft Reset bit (CSFTRST) in the Reset Register (USBAHB_GRSTCTL).
6. Poll the USBAHB_GRSTCTL register until the core clears the soft reset bit, which ensures the soft reset is completed properly.
7. Initialize the core according to the instructions in 31.4.1.1 Device Initialization.

31.4.2 Modes of Operation

- 31.4.2.1 Overview: DMA/Device Modes
- 31.4.2.2 DMA Mode
- 31.4.2.3 Device Mode

31.4.2.1 Overview: DMA/Device Modes

The application can operate the core in either of two modes:

- In 31.4.2.2 DMA Mode - The core fetches the data to be transmitted or updates the received data on the AHB.
- In 31.4.2.3 Device Mode — The application initiates the data transfers for data fetch and store.

31.4.2.2 DMA Mode

In DMA Mode, the host uses the AHB main Interface for transmit packet data fetch (AHB to USB) and receive data update (USB to AHB). The AHB main uses the programmed DMA address (USB_HCx_DMAADDR register in host mode and USBAHB_DIEPx_DMAADDR/USBAHB_DOEPx_DMAADDR register in device mode) to access the data buffers.

31.4.2.2.1 Transfer-Level Operation

In DMA mode, the application is interrupted only after the programmed transfer size is transmitted or received (provided the core detects no NAK/Timeout/Error response in Host mode, or Timeout/CRC Error in Device mode). The application must handle all transaction errors. In Device mode, all the USB errors are handled by the core itself.

31.4.2.2.2 Transaction-Level Operation

This mode is similar to transfer-level operation with the programmed transfer size equal to one packet size (either maximum packet size, or a short packet size).

31.4.2.3 Device Mode

In Device mode, the application can operate the core either in transaction-level (packet-level) operation or in pipelined transaction-level operation.

Device Mode For an IN transaction, the application enables the endpoint, writes the data packet into the corresponding transmit FIFO, and waits for the packet completion interrupt from the core. For an OUT transaction, the application enables the endpoint, waits for the packet received interrupt from the core, then empties the packet from the receive FIFO.

Note: The application has to finish writing one complete packet before switching to a different channel/endpoint FIFO. Violating this rule results in an error.

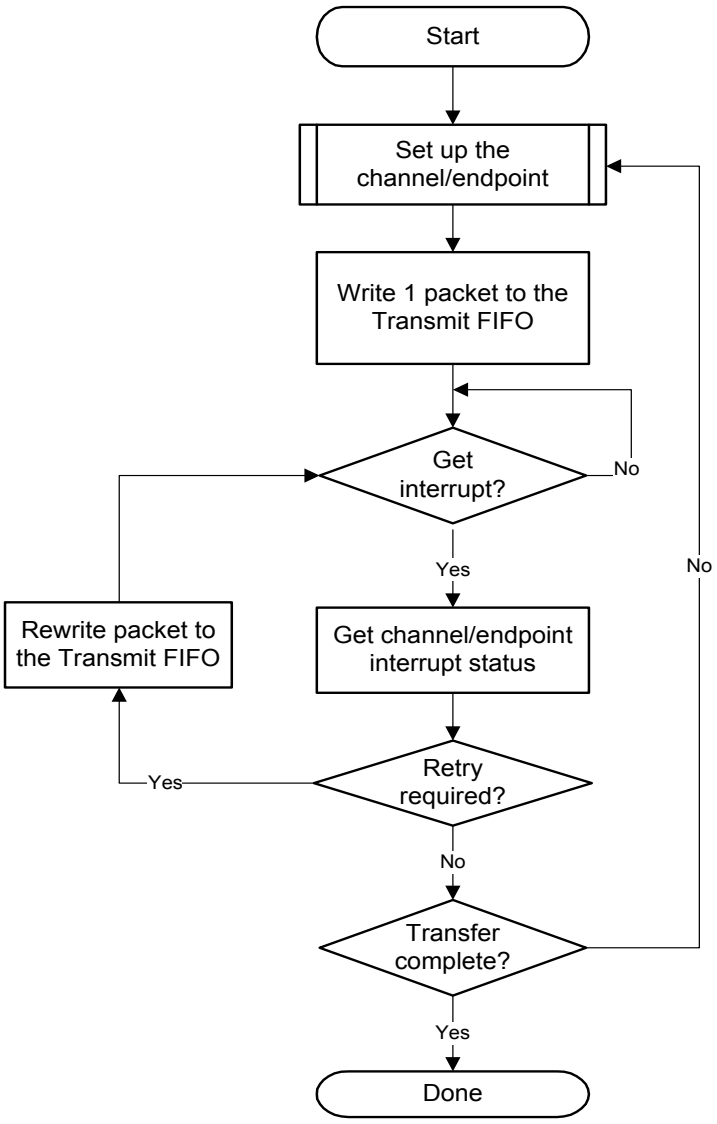


Figure 31.3. Transmit Transaction-Level Operation in Device Mode

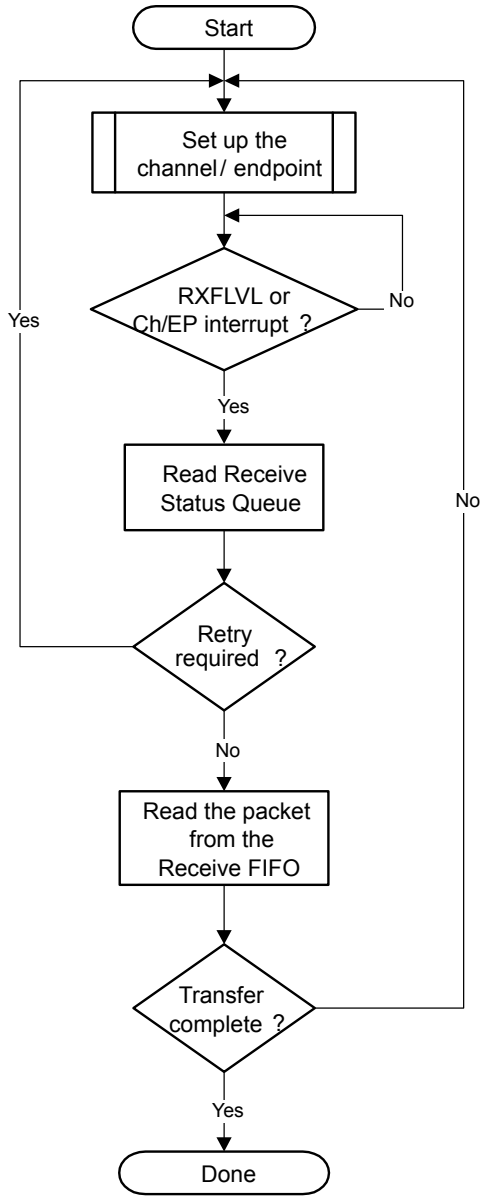


Figure 31.4. Receive Transaction-Level Operation in Device Mode

31.4.2.3.1 Transaction-Level Operation

The application handles one data packet at a time per channel/endpoint in transaction-level operations. Based on the handshake response received on the USB, the application determines whether to retry the transaction or proceed with the next, until the end of the transfer. The application is interrupted on completion of every packet. The application performs transaction-level operations for a channel/endpoint for a transmission (host: OUT/device: IN) or reception (host: IN/device: OUT) as shown in Figure 31.3 Transmit Transaction-Level Operation in Device Mode on page 1211 and Figure 31.4 Receive Transaction-Level Operation in Device Mode on page 1212.

31.4.2.3.2 Pipelined Transaction-Level Operation

The application can pipeline more than one transaction (IN or OUT) with pipelined transaction-level operation, which is analogous to Transfer mode in DMA mode. In pipelined transaction-level operation, the application can program the core to perform multiple transactions. The advantage of this mode compared to transaction-level operation is that the application is not interrupted on a packet basis.

31.4.2.3.2.1 Device Mode

For an IN transaction, the application sets up a transfer and enables the endpoint. The application can write multiple packets back-to-back for the same endpoint into the transmit FIFO, based on available space. It can also pipeline IN transactions for multiple channels by writing into the USBAHB_DIEPx_CTL register followed by a packet write to that endpoint. The core writes the endpoint number, along with the last DWORD write for the packet into the Request queue. The core transmits the data in the transmit FIFO when an IN token is received on the USB.

For an OUT transaction, the application sets up a transfer and enables the endpoint. The core receives the OUT data into the receive FIFO, when it has available space. As the packets are received into the FIFO, the application must empty data from it.

From this point on in this chapter, the terms “Pipelined Transaction mode” and “Transfer mode” are used interchangeably.

31.4.3 Device Programming Model

Before you program the Device, be sure to read 31.4.1 Overview: Programming the Core and 31.4.2 Modes of Operation

31.4.3.1 Endpoint Initialization

This section addresses the following topics:

- 31.4.3.1.1 Initialization on USB Reset
- 31.4.3.1.2 Initialization on Enumeration Completion
- 31.4.3.1.3 Initialization on SetAddress Command
- 31.4.3.1.4 Initialization on SetConfiguration/SetInterface Command
- 31.4.3.1.5 Endpoint Activation
- 31.4.3.1.6 Endpoint Deactivation
- 31.4.3.1.7 Device DMA/Device Mode Initialization

31.4.3.1.1 Initialization on USB Reset

1. Set the NAK bit for all OUT endpoints
   - USBAHB_DOEPx_CTL.SNAK = 1 (for all OUT endpoints)
2. Unmask the following interrupt bits:
   - USBAHB_DAINTMSK.INEP0 = 1 (control 0 IN endpoint)
   - USBAHB_DAINTMSK.OUTEP0 = 1 (control 0 OUT endpoint)
   - USBAHB_DOEPMSK.SETUP = 1
   - USBAHB_DOEPMSK.XFERCOMPL = 1
   - USBAHB_DIEPMSK.XFERCOMPL = 1
   - USBAHB_DIEPMSK.TIMEOUTMSK = 1
3. To transmit or receive data, the device must initialize more registers as specified in 31.4.3.1.7 Device DMA/Device Mode Initialization.
4. Set up the Data FIFO RAM for each of the FIFOs
   - Program the USBAHB_GRXFSIZ Register, to be able to receive control OUT data and setup data. If thresholding is not enabled, at a minimum, this must be equal to 1 max packet size of control endpoint 0 + 2 DWORDs (for the status of the control OUT data packet) + 10 DWORDs (for setup packets). If thresholding is enabled, at a minimum, this must be equal to 2 * (USBAHB_DTHRCTL.RXTHRLEN/4 + 1) + 2 DWORDs (for the status of the control OUT data packet) + 10 DWORDs (for setup packets)
   - Program the Device IN Endpoint Transmit FIFO size register (depending on the FIFO number chosen), to be able to transmit control IN data. At a minimum, this must be equal to 1 max packet size of control endpoint 0.If thresholding is enabled, this can be programmed to less than one max packet size.
5. Program the following fields in the endpoint-specific registers for control OUT endpoint 0 to receive a SETUP packet
   - USBAHB_DOEP0TSIZ.SUPCNT = 3 (to receive up to 3 back-to-back SETUP packets)
   - In DMA mode, USBAHB_DOEP0DMAADDR register with a memory address to store any SETUP packets received

At this point, all initialization required to receive SETUP packets is done, except for enabling control OUT endpoint 0 in DMA mode.

31.4.3.1.2 Initialization on Enumeration Completion

1. On the Enumeration Done interrupt (USBAHB_GINTSTS.ENUMDONE, read the USBAHB_DSTS register to determine the enumeration speed.
2. Program the USBAHB_DIEP0CTL.MPS field to set the maximum packet size. This step configures control endpoint 0. The maximum packet size for a control endpoint depends on the enumeration speed.
3. In DMA mode, program the USBAHB_DOEP0CTL register to enable control OUT endpoint 0, to receive a SETUP packet.
   - USBAHB_DOEP0CTL.EPENA = 1

At this point, the device is ready to receive SOF packets and is configured to perform control transfers on control endpoint 0.

31.4.3.1.3 Initialization on SetAddress Command

This section describes what the application must do when it receives a SetAddress command in a SETUP packet.

1. Program the USBAHB_DCFG register with the device address received in the SetAddress command
2. Program the core to send out a status IN packet.

31.4.3.1.4 Initialization on SetConfiguration/SetInterface Command

This section describes what the application must do when it receives a SetConfiguration or SetInterface command in a SETUP packet.

1. When a SetConfiguration command is received, the application must program the endpoint registers to configure them with the characteristics of the valid endpoints in the new configuration.
2. When a SetInterface command is received, the application must program the endpoint registers of the endpoints affected by this command.
3. Some endpoints that were active in the prior configuration or alternate setting are not valid in the new configuration or alternate setting. These invalid endpoints must be deactivated.
4. For details on a particular endpoint's activation or deactivation, see 31.4.3.1.5 Endpoint Activation and 31.4.3.1.6 Endpoint Deactivation.
5. Unmask the interrupt for each active endpoint and mask the interrupts for all inactive endpoints in the USBAHB_DAINTMSK register.
6. Set up the Data FIFO RAM for each FIFO. See 31.4.4.1 Data FIFO RAM Allocation for more detail.
7. After all required endpoints are configured, the application must program the core to send a status IN packet.

At this point, the device core is configured to receive and transmit any type of data packet.

31.4.3.1.5 Endpoint Activation

This section describes the steps required to activate a device endpoint or to configure an existing device endpoint to a new type.

1. Program the characteristics of the required endpoint into the following fields of the USBAHB_DIEPx_CTL register (for IN or bidirectional endpoints) or the USBAHB_DOEPx_CTL register (for OUT or bidirectional endpoints).
   - Maximum Packet Size
   - USB Active Endpoint = 1
   - Endpoint Start Data Toggle (for interrupt and bulk endpoints)
   - Endpoint Type
   - TxFIFO Number
2. Once the endpoint is activated, the core starts decoding the tokens addressed to that endpoint and sends out a valid handshake for each valid token received for the endpoint.

31.4.3.1.6 Endpoint Deactivation

This section describes the steps required to deactivate an existing endpoint.

1. In the endpoint to be deactivated, clear the USB Active Endpoint bit in the USBAHB_DIEPx_CTL register (for IN or bidirectional endpoints) or the USBAHB_DOEPx_CTL register (for OUT or bidirectional endpoints).
2. Once the endpoint is deactivated, the core ignores tokens addressed to that endpoint, resulting in a timeout on the USB.

31.4.3.1.7 Device DMA/Device Mode Initialization

The application must meed the following conditions to set up the device core to handle traffic.

- In Device mode, USBAHB_GINTMSK.NPTXFEMPMSK, and USBAHB_GINTMSK.RXFLVLMSK must be unset.
- In DMA mode, the aforementioned interrupts must be masked.

31.4.3.1.8 Transfer Stop Process

When the core is operating as a device, use the following programing sequence if you want to stop any transfers (because of an interrupt from the host, typically a reset).

31.4.3.1.9 Transfer Stop Programming Flow for IN Endpoints

Sequence of operations:

1. Disable the IN endpoint by programming USBAHB_DIEP0CTL/USBAHB_DIEPx_CTL.EPDIS = 1.
2. Wait for the USBAHB_DIEPx_INT.EPDISBLD interrupt, which indicates that the IN endpoint is completely disabled. When the EPDISBLD interrupt is asserted, the core clears the following bits:
   - USBAHB_DIEP0CTL/USBAHB_DIEPx_CTL.EPDIS = 0
   - USBAHB_DIEP0CTL/USBAHB_DIEPx_CTL.EPENA = 0
3. Flush the TX FIFO by programming the following bits:
   - USBAHB_GRSTCTL.TXFFLSH = 1
   - USBAHB_GRSTCTL.TXFNUM = FIFO number specific to endpoint
4. The application can start polling till USBAHB_GRSTCTL.TXFFLSH is cleared. When this bit is cleared, it ensures that there is no data left in the TX FIFO.

31.4.3.1.10 Transfer Stop Programming Flow for OUT Endpoints

Sequence of operations:

1. Enable all OUT endpoints by setting USBAHB_DOEP0CTL/USBAHB_DOEPx_CTL.EPENA = 1.
2. Before disabling any OUT endpoint, the application must enable Global OUT NAK mode in the core, according to the instructions in 31.4.3.2.2.5 Setting the Global OUT NAK. This ensures that data in the RX FIFO is sent to the application successfully. Set USBAHB_DCTL.USBAHB_DCTL.SGOUTNAK = 1.
3. Wait for the USBAHB_GINTSTS.GOUTNAKEFF interrupt.
4. Disable all active OUT endpoints by programming the following register bits:
   - USBAHB_DOEP0CTL/USBAHB_DOEPx_CTL.EPENA = 1
   - USBAHB_DOEP0CTL/USBAHB_DOEPx_CTL.EPDIS = 1
   - USBAHB_DOEP0CTL/USBAHB_DOEPx_CTL.SNAK = 1
5. Wait for the USBAHB_DOEP0INT/USBAHB_DOEPx_INT.EPDISBLD interrupt for each OUT endpoint programmed in the previous step. The USBAHB_DOEP0INT/USBAHB_DOEPx_INT.EPDISBLD interrupt indicates that the corresponding OUT endpoint is completely disabled. When the EPDISBLD interrupt is asserted, the core clears the following bits:
   - USBAHB_DOEP0CTL/USBAHB_DOEPx_CTL.EPENA = 0
   - USBAHB_DOEP0CTL/USBAHB_DOEPx_CTL.EPDIS = 0

Note: The application must not flush the Rx FIFO, as the Global out nak effective interrupt earlier ensures that there is no data left in the Rx FIFO.

31.4.3.2 Device Programming Operations

31.4.3.2 Device Programming Operations provides links to the programming sequence for different USB transaction types.

Device Mode	IN Without Thresholding	SETUP	OUT Without Thresholding
Control			
Device	31.4.3.2.3.11 Generic Non-Periodic (Bulk and Control) IN Data Transfers Without Thresholding in DMA and Device Mode	31.4.3.2.1 OUT Data Transfers in Device and DMA Modes	31.4.3.2.2.8 Generic Non-Isochronous OUT Data Transfers Without Thresholding in DMA and Device Modes
DMA	31.4.3.2.3.11 Generic Non-Periodic (Bulk and Control) IN Data Transfers Without Thresholding in DMA and Device Mode	31.4.3.2.1 OUT Data Transfers in Device and DMA Modes	31.4.3.2.2.8 Generic Non-Isochronous OUT Data Transfers Without Thresholding in DMA and Device Modes
Bulk			
Device	31.4.3.2.3.11 Generic Non-Periodic (Bulk and Control) IN Data Transfers Without Thresholding in DMA and Device Mode		31.4.3.2.2.8 Generic Non-Isochronous OUT Data Transfers Without Thresholding in DMA and Device Modes
DMA	31.4.3.2.3.11 Generic Non-Periodic (Bulk and Control) IN Data Transfers Without Thresholding in DMA and Device Mode		31.4.3.2.2.8 Generic Non-Isochronous OUT Data Transfers Without Thresholding in DMA and Device Modes
Interrupt			
Device	31.4.3.2.3.13 Generic Periodic IN (Interrupt and Isochronous) Data Transfers Without Thresholding and 31.4.3.2.3.14 Generic Periodic IN Data Transfers Without Thresholding Using the Periodic Transfer Interrupt Feature		31.4.3.2.2.8 Generic Non-Isochronous OUT Data Transfers Without Thresholding in DMA and Device Modes and 31.4.3.2.2.10 Generic Interrupt OUT Data Transfers Without Thresholding Using Periodic Transfer Interrupt Feature
DMA	31.4.3.2.3.13 Generic Periodic IN (Interrupt and Isochronous) Data Transfers Without Thresholding and 31.4.3.2.3.14 Generic Periodic IN Data Transfers Without Thresholding Using the Periodic Transfer Interrupt Feature		31.4.3.2.2.8 Generic Non-Isochronous OUT Data Transfers Without Thresholding in DMA and Device Modes and 31.4.3.2.2.10 Generic Interrupt OUT Data Transfers Without Thresholding Using Periodic Transfer Interrupt Feature
Isochronous			
Device	31.4.3.2.3.13 Generic Periodic IN (Interrupt and Isochronous) Data Transfers Without Thresholding		31.4.3.2.2.2 Control Read Transfers (SETUP, Data IN, Status OUT) and 31.4.3.2.2.12 Incomplete Isochronous OUT Data Transfers in DMA and Device Modes
DMA	31.4.3.2.3.13 Generic Periodic IN (Interrupt and Isochronous) Data Transfers Without Thresholding and 31.4.3.2.3.14 Generic Periodic IN Data Transfers Without Thresholding Using the Periodic Transfer Interrupt Feature		31.4.3.2.2.2 Control Read Transfers (SETUP, Data IN, Status OUT) and 31.4.3.2.2.12 Incomplete Isochronous OUT Data Transfers in DMA and Device Modes

31.4.3.2.1 OUT Data Transfers in Device and DMA Modes

This section describes the internal data flow and application-level operations during data OUT transfers and setup transactions.

31.4.3.2.1.1 Control Setup Transactions

This section describes how the core handles SETUP packets and the application's sequence for handling setup transactions. To initialize the core after power-on reset, the application must follow the sequence in 31.4.1 Overview: Programming the Core. Before it can communicate with the host, it must initialize an endpoint as described in 31.4.3.1 Endpoint Initialization. See 31.4.3.2.2.4 Packet Read From FIFO in Device Mode.

Application Requirements

1. To receive a SETUP packet, the USBAHB_DOEPx_TSIZ.SUPCNT field in a control OUT endpoint must be programmed to a non-zero value. When the application programs the SUPCNT field to a non-zero value, the core receives SETUP packets and writes them to the receive FIFO, irrespective of the USBAHB_DOEPx_CTL.NAK status and USBAHB_DOEPx_CTL.EPENA bit setting. The SUPCNT field is decremented every time the control endpoint receives a SETUP packet. If the SUPCNT field is not programmed to a proper value before receiving a SETUP packet, the core still receives the SETUP packet and decrements the SUPCNT field, but the application possibly is not be able to determine the correct number of SETUP packets received in the Setup stage of a control transfer.
   - USBAHB_DOEPx_TSIZ.SUPCNT = 3
2. In DMA mode, the OUT endpoint must also be enabled, to transfer the received SETUP packet data from the internal receive FIFO to the external memory.
   - USBAHB_DOEPx_CTL.EPENA = 1
3. The application must always allocate some extra space in the Receive Data FIFO, to be able to receive up to three SETUP packets on a control endpoint.
   - The space to be Reserved is (4 * n) + 6 DWORDs, where n is the number of control endpoints supported by the device. Three DWORDs are required for the first SETUP packet, 1 DWORD is required for the Setup Stage Done DWORD, and 6 DWORDs are required to store two extra SETUP packets among all control endpoints.
   - 3 DWORDs per SETUP packet are required to store 8 bytes of SETUP data and 4 bytes of SETUP status (Setup Packet Pattern). The core reserves this space in the receive data
   - FIFO to write SETUP data only, and never uses this space for data packets.
4. In Device mode, the application must read the 2 DWORDs of the SETUP packet from the receive FIFO. In DMA mode, the core writes the 2 DWORDs of SETUP data to the memory.
5. The application must read and discard the Setup Stage Done DWORD from the receive FIFO.

Internal Data Flow

1. When a SETUP packet is received, the core writes the received data to the receive FIFO, without checking for available space in the receive FIFO and irrespective of the endpoint's NAK and Stall bit settings.
   - The core internally sets the IN NAK and OUT NAK bits for the control IN/OUT endpoints on which the SETUP packet was received.
2. For every SETUP packet received on the USB, 3 DWORDs of data is written to the receive FIFO, and the SUPCNT field is decremented by 1.
   - The first DWORD contains control information used internally by the core
   - The second DWORD contains the first 4 bytes of the SETUP command
   - The third DWORD contains the last 4 bytes of the SETUP command
3. When the Setup stage changes to a Data IN/OUT stage, the core writes an entry (Setup Stage Done DWORD) to the receive FIFO, indicating the completion of the Setup stage.
4. On the AHB side, SETUP packets are emptied either by the DMA or the application. In DMA mode, the SETUP packets (2 DWORDs) are written to the memory location programmed in the USBAHB_DOEPx_DMAADDR register, only if the endpoint is enabled. If the endpoint is not enabled, the data remains in the receive FIFO until the enable bit is set.
5. When either the DMA or the application pops the Setup Stage Done DWORD from the receive FIFO, the core interrupts the application with a USBAHB_DOEPx_INT.SETUP interrupt, indicating it can process the received SETUP packet.
   - The core clears the endpoint enable bit for control OUT endpoints.

Application Programming Sequence

1. Program the USBAHB_DOEPx_TSIZ register.
   - USBAHB_DOEPx_TSIZ.SUPCNT = 3
2. In DMA mode, program the USBAHB_DOEPx_DMAADDR register and USBAHB_DOEPx_CTL register with the endpoint characteristics and set the Endpoint Enable bit (USBAHB_DOEPx_CTL.EPENA).
   - Endpoint Enable = 1
3. In Device mode, wait for the USBAHB_GINTSTS.RXFLVL interrupt and empty the data packets from the receive FIFO, as explained in 31.4.3.2.2.4 Packet Read From FIFO in Device Mode. This step can be repeated many times.

4. Assertion of the USBAHB_DOEPx_INT.SETUP interrupt marks a successful completion of the SETUP Data Transfer.
   - On this interrupt, the application must read the USBAHB_DOEPx_TSIZ register to determine the number of SETUP packets received and process the last received SETUP packet.
   - In DMA mode, the application must also determine if the interrupt bit USBAHB_DOEPx_INT.BACK2BACKSETUP is set. This bit is set if the core has received more than three back-to-back SETUP packets. If this is the case, the application must ignore the USBAHB_DOEPx_TSIZ.SUPCNT value and use the USBAHB_DOEPx_DMAADDR directly to read out the last SETUP packet received. USBAHB_DOEPx_DMAADDR-8 provides the pointer to the last valid SETUP data.

Note: If the application has not enabled EP0 before the host sends the SETUP packet, the core ACKs the SETUP packet and stores it in the FIFO, but does not write to the memory until EP0 is enabled. When the application enables the EP0 (first enable) and clears the NAK bit at the same time the Host sends DATA OUT, the DATA OUT is stored in the RxFIFO. The core then writes the setup data to the memory and disables the endpoint. Though the application expects a Transfer Complete interrupt for the Data OUT phase, this does not occur, because the SETUP packet, rather than the DATA OUT packet, enables EP0 the first time. Thus, the DATA OUT packet is still in the RxFIFO until the application re-enables EP0. The application must enable EP0 one more time for the core to process the DATA OUT packet.

Figure 31.5 Processing a SETUP Packet on page 1220 charts this flow.

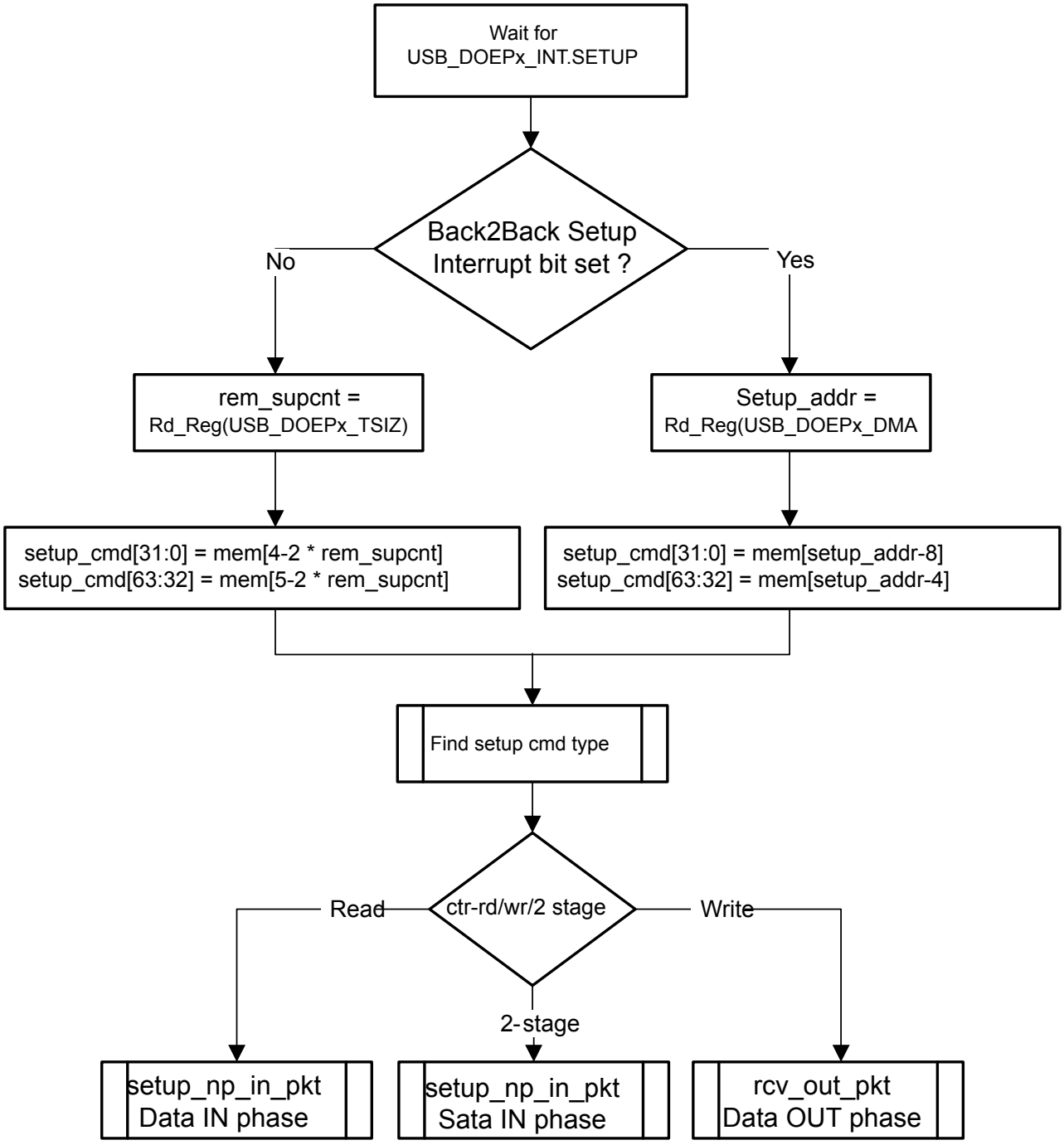


Figure 31.5. Processing a SETUP Packet

31.4.3.2.1.2 Handling More Than Three Back-to-Back SETUP Packets

Per the USB 2.0 specification, normally, during a SETUP packet error, a host does not send more than three back-to-back SETUP packets to the same endpoint. However, the USB 2.0 specification does not limit the number of back-to-back SETUP packets a host can send to the same endpoint. When this condition occurs, the core generates an interrupt (USBAHB_DOEPx_INT.BACK2BACKSETUP). In DMA mode, the core also rewinds the DMA address for that endpoint (USBAHB_DOEPx_DMAADDR) and overwrites the first SETUP packet in system memory with the fourth, second with the fifth, and so on. If the BACK2BACKSETUP interrupt is asserted, the application must read the OUT endpoint DMA register (USBAHB_DOEPx_DMAADDR) to determine the final SETUP data in system memory.

In DMA mode, the application can mask the BACK2BACKSETUP interrupt, but after receiving the DOEPINT.SETUP interrupt, the application can read the DOEPINT.BACK2BACKSETUP interrupt bit. In Device mode, the application can use the USBAHB_GINTSTS.RXFLVL interrupt to read out the SETUP packets from the FIFO whenever the core receives the SETUP packet.

31.4.3.2.2 Control Transfers

This section describes the various types of control transfers.

31.4.3.2.2.1 Control Write Transfers (SETUP, Data OUT, Status IN)

This section describes control write transfers.

Application Programming Sequence

1. Assertion of the USBAHB_DOEPx_INT.SETUP Packet interrupt indicates that a valid SETUP packet has been transferred to the application. See 31.4.3.2.1 OUT Data Transfers in Device and DMA Modes for more details. At the end of the Setup stage, the application must reprogram the USBAHB_DOEPx_TSIZ.SUPCNT field to 3 to receive the next SETUP packet.
2. If the last SETUP packet received before the assertion of the SETUP interrupt indicates a data OUT phase, program the core to perform a control OUT transfer as explained in 31.4.3.2.2.8 Generic Non-Isochronous OUT Data Transfers Without Thresholding in DMA and Device Modes.

   In DMA mode, the application must reprogram the USBAHB_DOEPx_DMAADDR register to receive a control OUT data packet to a different memory location.
3. In a single OUT data transfer on control endpoint 0, the application can receive up to 64 bytes. If the application is expecting more than 64 bytes in the Data OUT stage, the application must re-enable the endpoint to receive another 64 bytes, and must continue to do so until it has received all the data in the Data stage.
4. Assertion of the USBAHB_DOEPx_INT.Transfer Compl interrupt on the last data OUT transfer indicates the completion of the data OUT phase of the control transfer.
5. On completion of the data OUT phase, the application must do the following.
   - To transfer a new SETUP packet in DMA mode, the application must re-enable the control OUT endpoint as explained in 31.4.3.2.1 OUT Data Transfers in Device and DMA Modes.
     - USBAHB_DOEPx_CTL.EPENA = 1
   - To execute the received Setup command, the application must program the required registers in the core. This step is optional, based on the type of Setup command received.
6. For the status IN phase, the application must program the core as described in 31.4.3.2.3.11 Generic Non-Periodic (Bulk and Control) IN Data Transfers Without Thresholding in DMA and Device Mode to perform a data IN transfer.
7. Assertion of the USBAHB_DIEPx_INT.XFERCOMPL interrupt indicates completion of the status IN phase of the control transfer.
8. The previous step must be repeated until the USBAHB_DIEPx_INT.XFERCOMPL interrupt is detected on the endpoint, marking the completion of the control write transfer.

31.4.3.2.2.2 Control Read Transfers (SETUP, Data IN, Status OUT)

This section describes control read transfers.

Application Programming Sequence

1. Assertion of the USBAHB_DOEPx_INT.SETUP Packet interrupt indicates that a valid SETUP packet has been transferred to the application. See 31.4.3.2.1 OUT Data Transfers in Device and DMA Modes for more details. At the end of the Setup stage, the application must reprogram the USBAHB_DOEPx_TSIZ.SUPCNT field to 3 to receive the next SETUP packet.
2. If the last SETUP packet received before the assertion of the SETUP interrupt indicates a data IN phase, program the core to perform a control IN transfer as explained in 31.4.3.2.3.11 Generic Non-Periodic (Bulk and Control) IN Data Transfers Without Thresholding in DMA and Device Mode.
3. On a single IN data transfer on control endpoint 0, the application can transmit up to 64 bytes. To transmit more than 64 bytes in the Data IN stage, the application must re-enable the endpoint to transmit another 64 bytes, and must continue to do so, until it has transmitted all the data in the Data stage.
4. The previous step must be repeated until the USBAHB_DIEPx_INT.XFERCOMPL interrupt is detected for every IN transfer on the endpoint.
5. The USBAHB_DIEPx_INT.XFERCOMPL interrupt on the last IN data transfer marks the completion of the control transfer's Data stage.
6. To perform a data OUT transfer in the status OUT phase, the application must program the core as described in 31.4.3.2.1 OUT Data Transfers in Device and DMA Modes.
   - The application must program the USBAHB_DCFG.NZSTSOUTHSHK handshake field to a proper setting before transmitting an data OUT transfer for the Status stage.
   - In DMA mode, the application must reprogram the USBAHB_DOEPx_DMAADDR register to receive the control OUT data packet to a different memory location.
7. Assertion of the USBAHB_DOEPx_INT.XFERCOMPL interrupt indicates completion of the status OUT phase of the control transfer. This marks the successful completion of the control read transfer.
   - To transfer a new SETUP packet in DMA mode, the application must re-enable the control OUT endpoint as explained in 31.4.3.2.1 OUT Data Transfers in Device and DMA Modes.
   - USBAHB_DOEPx_CTL.EPENA = 1

31.4.3.2.2.3 Two-Stage Control Transfers (SETUP/Status IN)

This section describes two-stage control transfers.

Application Programming Sequence

1. Assertion of the USBAHB_DOEPx_INT.SETUP interrupt indicates that a valid SETUP packet has been transferred to the application. See 31.4.3.2.1 OUT Data Transfers in Device and DMA Modes for more detail. To receive the next SETUP packet, the application must reprogram the USBAHB_DOEPx_TSIZ.SUPCNT field to 3 at the end of the Setup stage.
2. Decode the last SETUP packet received before the assertion of the SETUP interrupt. If the packet indicates a two-stage control command, the application must do the following.
   - To transfer a new SETUP packet in DMA mode, the application must re-enable the control OUT endpoint. See 31.4.3.2.1 OUT Data Transfers in Device and DMA Modes for details.
     - USBAHB_DOEPx_CTL.EPENA = 1
   - Depending on the type of Setup command received, the application can be required to program registers in the core to execute the received Setup command.
3. For the status IN phase, the application must program the core described in 31.4.3.2.3.11 Generic Non-Periodic (Bulk and Control) IN Data Transfers Without Thresholding in DMA and Device Mode to perform a data IN transfer.
4. Assertion of the USBAHB_DIEPx_INT.XFERCOMPL interrupt indicates the completion of the status IN phase of the control transfer.
5. The previous step must be repeated until the USBAHB_DIEPx_INT.XFERCOMPL interrupt is detected on the endpoint, marking the completion of the two-stage control transfer.

Example: Two-Stage Control Transfer

These notes refer to Figure 31.6 Two-Stage Control Transfer on page 1224.

1. SETUP packet #1 is received on the USB and is written to the receive FIFO, and the core responds with an ACK handshake. This handshake is lost and the host detects a timeout.
2. The SETUP packet in the receive FIFO results in a USBAHB_GINTSTS.RXFLVL interrupt to the application, causing the application to empty the receive FIFO.
3. SETUP packet #2 on the USB is written to the receive FIFO, and the core responds with an ACK handshake.
4. The SETUP packet in the receive FIFO sends the application the USBAHB_GINTSTS.RXFLVL interrupt and the application empties the receive FIFO.
5. After the second SETUP packet, the host sends a control IN token for the status phase. The core issues a NAK response to this token, and writes a Setup Stage Done entry to the receive FIFO. This entry results in a USBAHB_GINTSTS.RXFLVL interrupt to the application, which empties the receive FIFO. After reading out the Setup Stage Done DWORD, the core asserts the USBAHB_DOEPx_INT.SETUP packet interrupt to the application.
6. On this interrupt, the application processes SETUP Packet #2, decodes it to be a two-stage control command, and clears the control IN NAK bit.
   - USBAHB_DIEPx_CTL.CNAK = 1
7. When the application clears the IN NAK bit, the core interrupts the application with a USBAHB_DIEPx_INT.INTKNTXFEMP. On this interrupt, the application enables the control IN endpoint with a USBAHB_DIEPx_TSIZ.XFERSIZE of 0 and a USBAHB_DIEPx_TSIZ.PKTCNT of 1. This results in a zero-length data packet for the status IN token on the USB.
8. At the end of the status IN phase, the core interrupts the application with a USBAHB_DIEPx_INT.XFERCOMPL interrupt.

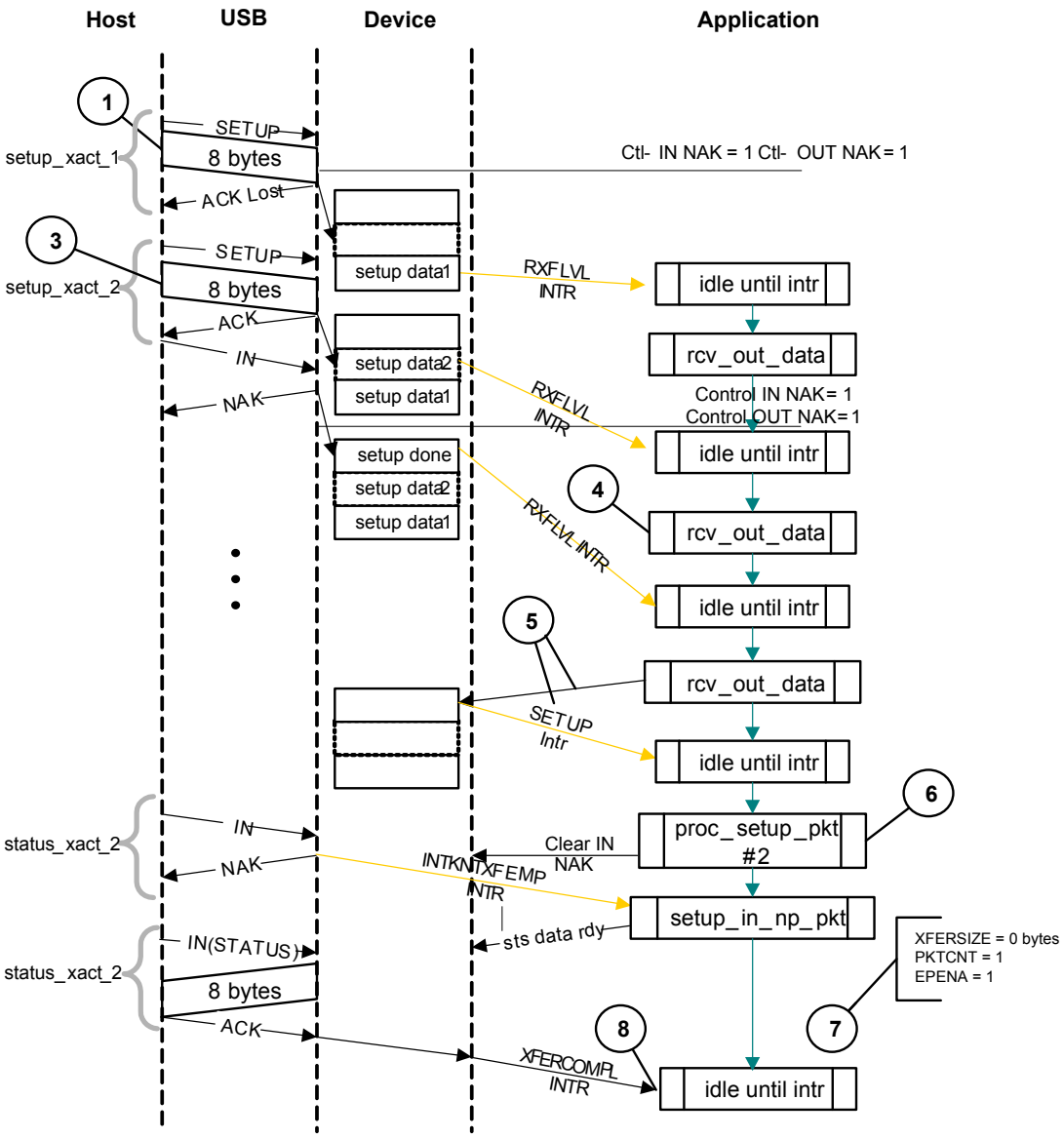


Figure 31.6. Two-Stage Control Transfer

31.4.3.2.2.4 Packet Read From FIFO in Device Mode

This section describes how to read packets (OUT data and SETUP packets) from the receive FIFO in Device mode.

1. On catching a USBAHB_GINTSTS.RXFLVL interrupt, the application must read the Receive Status Pop register (USBAHB_GRXSTSP).
2. The application can mask the USBAHB_GINTSTS.RXFLVL interrupt by writing to USBAHB_GINTMSK.RXFLVL = 0, until it has read the packet from the receive FIFO.
3. If the received packet's byte count is not 0, the byte count amount of data is popped from the receive Data FIFO and stored in memory. If the received packet byte count is 0, no data is popped from the Receive Data FIFO.
4. The receive FIFO's packet status readout indicates one of the following.
5. Global OUT NAK Pattern: PKTSTS = Global OUT NAK, BCNT = 0x000, EPNUM = Dont Care (0x0), DPID = Dont Care (0b00). This data indicates that the global OUT NAK bit has taken effect.
   a. SETUP Packet Pattern: PKTSTS = SETUP, BCNT = 0x008, EPNUM = Control EP Num, DPID = D0. This data indicates that a SETUP packet for the specified endpoint is now available for reading from the receive FIFO.
   b. Setup Stage Done Pattern: PKTSTS = Setup Stage Done, BCNT = 0x0, EPNUM = Control EP Num, DPID = Don't Care (0b00). This data indicates that the Setup stage for the specified endpoint has completed and the Data stage has started. After this entry is popped from the receive FIFO, the core asserts a Setup interrupt on the specified control OUT endpoint.
   c. Data OUT Packet Pattern: PKTSTS = DataOUT, BCNT = size of the Received data OUT packet, EPNUM = EPNum on which the packet was received, DPID = Actual Data PID.
   d. Data Transfer Completed Pattern: PKTSTS = Data OUT Transfer Done, BCNT = 0x0, EPNUM = OUT EP Num on which the data transfer is complete, DPID = Dont Care (0b00). This data indicates that a OUT data transfer for the specified OUT endpoint has completed. After this entry is popped from the receive FIFO, the core asserts a Transfer Completed interrupt on the specified OUT endpoint.

   The encoding for the PKTSTS is listed in 31.6 USB_APBS Register Description.
6. After the data payload is popped from the receive FIFO, the USBAHB_GINTSTS.RXFLVL interrupt must be unmasked.
7. Steps 1–5 are repeated every time the application detects assertion of the interrupt line due to USBAHB_GINTSTS.RXFLVL. Reading an empty receive FIFO can result in undefined core behavior.

Figure 31.7 Receive FIFO Packet Read in Device Mode on page 1225 provides a flow chart of this procedure.

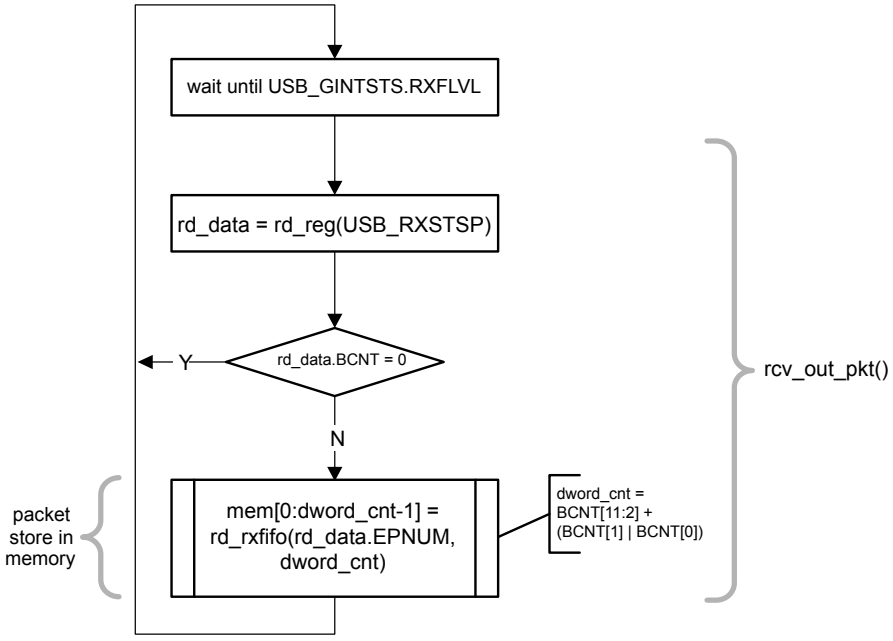


Figure 31.7. Receive FIFO Packet Read in Device Mode

31.4.3.2.2.5 Setting the Global OUT NAK

Internal Data Flow

1. When the application sets the Global OUT NAK (USBAHB_DCTL.SGOUTNAK), the core stops writing data, except SETUP packets, to the receive FIFO. Irrespective of the space availability in the receive FIFO, non-isochronous OUT tokens receive a NAK handshake response, and the core ignores isochronous OUT data packets
2. The core writes the Global OUT NAK pattern to the receive FIFO. The application must reserve enough receive FIFO space to write this data pattern. See 31.4.4.1 Data FIFO RAM Allocation.
3. When either the core (in DMA mode) or the application (in Device mode) pops the Global OUT NAK pattern DWORD from the receive FIFO, the core sets the USBAHB_GINTSTS.GOUTNAKEFF interrupt.
4. Once the application detects this interrupt, it can assume that the core is in Global OUT NAK mode. The application can clear this interrupt by clearing the USBAHB_DCTL.SGOUTNAK bit.

Application Programming Sequence

1. To stop receiving any kind of data in the receive FIFO, the application must set the Global OUT NAK bit by programming the following field.
   - USBAHB_DCTL.SGOUTNAK = 1
2. Wait for the assertion of the interrupt USBAHB_GINTSTS.GOUTNAKEFF. When asserted, this interrupt indicates that the core has stopped receiving any type of data except SETUP packets.
3. The application can receive valid OUT packets after it has set USBAHB_DCTL.SGOUTNAK and before the core asserts the USBAHB_GINTSTS.GOUTNAKEFF interrupt.
4. The application can temporarily mask this interrupt by writing to the USBAHB_GINTMSK.GOUTNAKEFFMSK bit.
   - USBAHB_GINTMSK.GINNAKEFFMSK = 0
5. Whenever the application is ready to exit the Global OUT NAK mode, it must clear the USBAHB_DCTL.SGOUTNAK bit. This also clears the USBAHB_GINTSTS.GOUTNAKEFF interrupt.
   - USBAHB_DCTL.CGOUTNAK = 1
6. If the application has masked this interrupt earlier, it must be unmasked as follows:
   - USBAHB_GINTMSK.GOUTNAKEFFMSK = 1

31.4.3.2.2.6 Disabling an OUT Endpoint

The application must use this sequence to disable an OUT endpoint that it has enabled.

Application Programming Sequence

1. Before disabling any OUT endpoint, the application must enable Global OUT NAK mode in the core, as described in 31.4.3.2.2.5 Setting the Global OUT NAK.
   - USBAHB_DCTL.SGOUTNAK = 1
   - Wait for the USBAHB_GINTSTS.GOUTNAKEFF interrupt
2. Disable the required OUT endpoint by programming the following fields.
   - USBAHB_DOEPx_CTL.EPDIS = 1
   - USBAHB_DOEPx_CTL.SNAK = 1
3. Wait for the USBAHB_DOEPx_INT.EPDISBLD interrupt, which indicates that the OUT endpoint is completely disabled. When the EPDISBLD interrupt is asserted, the core also clears the following bits.
   - USBAHB_DOEPx_CTL.EPDIS = 0
   - USBAHB_DOEPx_CTL.EPENA = 0
4. The application must clear the Global OUT NAK bit to start receiving data from other non-disabled OUT endpoints.
   - USBAHB_DCTL.SGOUTNAK = 0

31.4.3.2.2.7 Stalling a Non-Isochronous OUT Endpoint

This section describes how the application can stall a non-isochronous endpoint.

1. Put the core in the Global OUT NAK mode, as described in 31.4.3.2.2.5 Setting the Global OUT NAK.
2. Disable the required endpoint, as described in 31.4.3.2.2.6 Disabling an OUT Endpoint.
   - When disabling the endpoint, instead of setting the USBAHB_DOEPx_CTL.SNAK bit, set USBAHB_DOEPx_CTL.STALL = 1.
     - The Stall bit always takes precedence over the NAK bit.
3. When the application is ready to end the STALL handshake for the endpoint, the USBAHB_DOEPx_CTL.STALL bit must be cleared.
4. If the application is setting or clearing a STALL for an endpoint due to a SetFeature.Endpoint Halt or ClearFeature.Endpoint Halt command, the Stall bit must be set or cleared before the application sets up the Status stage transfer on the control endpoint.

31.4.3.2.2.8 Generic Non-Isochronous OUT Data Transfers Without Thresholding in DMA and Device Modes

To initialize the core after power-on reset, the application must follow the sequence in 31.4.1 Overview: Programming the Core. Before it can communicate with the host, it must initialize an endpoint as described in 31.4.3.1 Endpoint Initialization. See 31.4.3.2.2.4 Packet Read From FIFO in Device Mode.

This section describes a regular non-isochronous OUT data transfer (control, bulk, or interrupt).

Application Requirements

1. Before setting up an OUT transfer, the application must allocate a buffer in the memory to accommodate all data to be received as part of the OUT transfer, then program that buffer's size and start address (in DMA mode) in the endpoint-specific registers.
1. For OUT transfers, the Transfer Size field in the endpoint's Transfer Size register must be a multiple of the maximum packet size of the endpoint, adjusted to the DWORD boundary.

```
if (mps[epnum] mod 4) == 0
    transfer size[epnum] = n * (mps[epnum])  //Dword Aligned
else
    transfer size[epnum] = n * (mps[epnum] + 4 - (mps[epnum] mod 4)) //Non Dword Aligned

packet count[epnum] = n
n > 0
```

2. In DMA mode, the core stores a received data packet in the memory, always starting on a DWORD boundary. If the maximum packet size of the endpoint is not a multiple of 4, the core inserts byte pads at end of a maximum-packet-size packet up to the end of the DWORD.
3. On any OUT endpoint interrupt, the application must read the endpoint's Transfer Size register to calculate the size of the payload in the memory. The received payload size can be less than the programmed transfer size.
   - Payload size in memory = application-programmed initial transfer size – core updated final transfer size
   - Number of USB packets in which this payload was received = application-programmed initial packet count – core updated final packet count

Internal Data Flow

1. The application must set the Transfer Size and Packet Count fields in the endpoint-specific registers, clear the NAK bit, and enable the endpoint to receive the data.
2. Once the NAK bit is cleared, the core starts receiving data and writes it to the receive FIFO, as long as there is space in the receive FIFO. For every data packet received on the USB, the data packet and its status are written to the receive FIFO. Every packet (maximum packet size or short packet) written to the receive FIFO decrements the Packet Count field for that endpoint by 1.
   - OUT data packets received with Bad Data CRC are flushed from the receive FIFO automatically.
   - After sending an ACK for the packet on the USB, the core discards non-isochronous OUT data packets that the host, which cannot detect the ACK, re-sends. The application does not detect multiple back-to-back data OUT packets on the same end-point with the same data PID. In this case the packet count is not decremented.
   - If there is no space in the receive FIFO, isochronous or non-isochronous data packets are ignored and not written to the receive FIFO. Additionally, non-isochronous OUT tokens receive a NAK handshake reply.
   - In all the above three cases, the packet count is not decremented because no data is written to the receive FIFO.
3. When the packet count becomes 0 or when a short packet is received on the endpoint, the NAK bit for that endpoint is set. Once the NAK bit is set, the isochronous or non-isochronous data packets are ignored and not written to the receive FIFO, and non-isochronous OUT tokens receive a NAK handshake reply.
4. After the data is written to the receive FIFO, either the application (in Device mode) or the core's DMA engine (in DMA mode), reads the data from the receive FIFO and writes it to external memory, one packet at a time per endpoint.
5. At the end of every packet write on the AHB to external memory, the transfer size for the endpoint is decremented by the size of the written packet.
6. The OUT Data Transfer Completed pattern for an OUT endpoint is written to the receive FIFO on one of the following conditions.
   - The transfer size is 0 and the packet count is 0
   - The last OUT data packet written to the receive FIFO is a short packet (0 <= packet size < maximum packet size)
7. When either the application or the DMA pops this entry (OUT Data Transfer Completed), a Transfer Completed interrupt is generated for the endpoint and the endpoint enable is cleared.

Application Programming Sequence

1. Program the USBAHB_DOEPx_TSIZ register for the transfer size and the corresponding packet count. Additionally, in DMA mode, program the USBAHB_DOEPx_DMAADDR register.
2. Program the USBAHB_DOEPx_CTL register with the endpoint characteristics, and set the Endpoint Enable and ClearNAK bits.
   - USBAHB_DOEPx_CTL.EPENA = 1
   - USBAHB_DOEPx_CTL.CNAK = 1
3. In Device mode, wait for the USBAHB_GINTSTS.RXFLVL level interrupt and empty the data packets from the receive FIFO as explained in 31.4.3.2.2.4 Packet Read From FIFO in Device Mode.
   - This step can be repeated many times, depending on the transfer size.
4. Asserting the USBAHB_DOEPx_INT.XFERCOMPL interrupt marks a successful completion of the non-isochronous OUT data transfer.
5. Read the USBAHB_DOEPx_TSIZ register to determine the size of the received data payload.

Note: The XFERSIZE is not decremented for the last packet. This is as per design behavior.

Device Mode Bulk OUT Transaction

Figure 31.8 Device Mode Bulk OUT Transaction on page 1229 depicts the reception of a single bulk OUT data packet from the USB to the AHB and describes the events involved in the process.

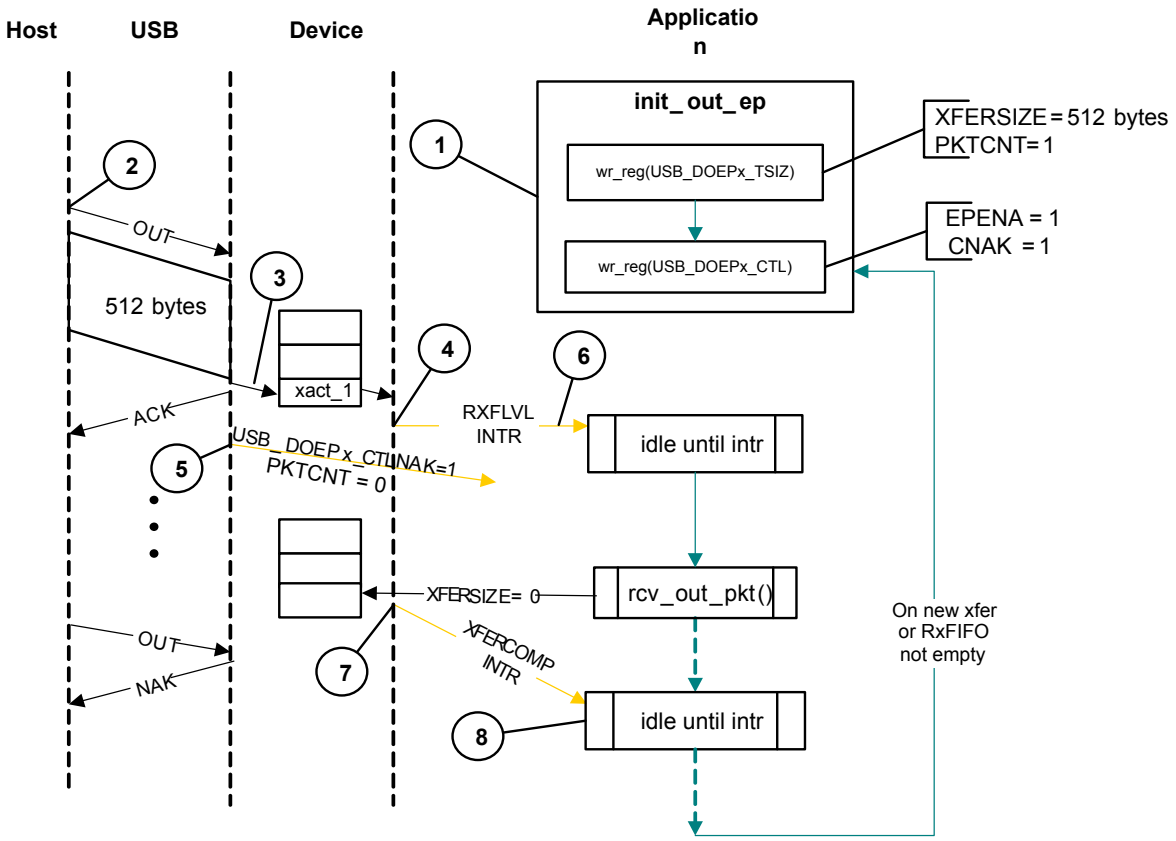


Figure 31.8. Device Mode Bulk OUT Transaction

After a SetConfiguration/SetInterface command, the application initializes all OUT endpoints by setting USBAHB_DOEPx_CTL.CNAK = 1 and USBAHB_DOEPx_CTL.EPENA = 1, and setting a suitable XFERSIZE and PKTCNT in the USBAHB_DOEPx_TSIZ register.

1. Host attempts to send data (OUT token) to an endpoint.
2. When the core receives the OUT token on the USB, it stores the packet in the RxFIFO because space is available there.
3. After writing the complete packet in the RxFIFO, the core then asserts the USBAHB_GINTSTS.RXFLVL interrupt.
4. On receiving the PKTCNT number of USB packets, the core sets the NAK bit for this endpoint internally to prevent it from receiving any more packets.
5. The application processes the interrupt and reads the data from the RxFIFO.
6. When the application has read all the data (equivalent to XFERSIZE), the core generates a USBAHB_DOEPx_INT.XFERCOMPL interrupt.

7. The application processes the interrupt and uses the setting of the USBAHB_DOEPx_INT.XFERCOMPL interrupt bit to determine that the intended transfer is complete.

31.4.3.2.2.9 Generic Isochronous OUT Data Transfer Without Thresholding in DMA and Device Modes

To initialize the core after power-on reset, the application must follow the sequence in 31.4.1 Overview: Programming the Core. Before it can communicate with the host, it must initialize an endpoint as described in 31.4.3.1 Endpoint Initialization. See 31.4.3.2.2.4 Packet Read From FIFO in Device Mode.

This section describes a regular isochronous OUT data transfer.

Application Requirements:

1. All the application requirements for non-isochronous OUT data transfers also apply to isochronous OUT data transfers
2. For isochronous OUT data transfers, the Transfer Size and Packet Count fields must always be set to the number of maximum-packet-size packets that can be received in a single frame and no more. Isochronous OUT data transfers cannot span more than 1 frame.
   - 1 <= packet count[epnum] <= 3
3. In Device mode, when isochronous OUT endpoints are supported in the device, the application must read all isochronous OUT data packets from the receive FIFO (data and status) before the end of the periodic frame (USBAHB_GINTSTS.EOPF interrupt). In DMA mode, the application must guarantee enough bandwidth to allow emptying the isochronous OUT data packet from the receive FIFO before the end of each periodic frame.
4. To receive data in the following frame, an isochronous OUT endpoint must be enabled after the USBAHB_GINTSTS.EOPF and before the USBAHB_GINTSTS.SOF.

Internal Data Flow

1. The internal data flow for isochronous OUT endpoints is the same as that for non-isochronous OUT endpoints, but for a few differences.
2. When an isochronous OUT endpoint is enabled by setting the Endpoint Enable and clearing the NAK bits, the Even/Odd frame bit must also be set appropriately. The core receives data on a isochronous OUT endpoint in a particular frame only if the following condition is met.
   - USBAHB_DOEPx_CTL.DPIDEOF (Even/Odd frame) = USBAHB_DSTS.SOFFN[0]
3. When either the application or the internal DMA completely reads an isochronous OUT data packet (data and status) from the receive FIFO, the core updates the USBAHB_DOEPx_TSIZ.RXDPIDSUPCNT (Received DPID) field with the data PID of the last isochronous OUT data packet read from the receive FIFO.

Application Programming Sequence

1. Program the USBAHB_DOEPx_TSIZ register for the transfer size and the corresponding packet count. When in DMA mode, also program the USBAHB_DOEPx_DMAADDR register.
2. Program the USBAHB_DOEPx_CTL register with the endpoint characteristics and set the Endpoint Enable, ClearNAK, and Even/Odd frame bits.
   - Endpoint Enable = 1
   - CNAK = 1
   - Even/Odd frame = (0: Even/1: Odd)

1. In Device mode, wait for the USBAHB_GINTSTS.Rx StsQ level interrupt and empty the data packets from the receive FIFO as explained in 31.4.3.2.2.4 Packet Read From FIFO in Device Mode.
   - This step can be repeated many times, depending on the transfer size.

1. The assertion of the USBAHB_DOEPx_INT.XFERCOMPL interrupt marks the completion of the isochronous OUT data transfer. This interrupt does not necessarily mean that the data in memory is good.
2. This interrupt can not always be detected for isochronous OUT transfers. Instead, the application can detect the USBAHB_GINTSTS.INCOMPLP (Incomplete Isochronous OUT data) interrupt. See 31.4.3.2.2.12 Incomplete Isochronous OUT Data Transfers in DMA and Device Modes, for more details
3. Read the USBAHB_DOEPx_TSIZ register to determine the size of the received transfer and to determine the validity of the data received in the frame. The application must treat the data received in memory as valid only if one of the following conditions is met.
   - USBAHB_DOEPx_TSIZ.RXDPID = D0 and the number of USB packets in which this payload was received = 1
   - USBAHB_DOEPx_TSIZ.RXDPID = D1 and the number of USB packets in which this payload was received = 2
   - USBAHB_DOEPx_TSIZ.RXDPID = D2 and the number of USB packets in which this payload was received = 3
     - The number of USB packets in which this payload was received = App Programmed Initial Packet Count – Core Updated Final Packet Count

The application can discard invalid data packets.

31.4.3.2.2.10 Generic Interrupt OUT Data Transfers Without Thresholding Using Periodic Transfer Interrupt Feature

This section describes a regular INTR OUT data transfer with the Periodic Transfer Interrupt feature.

To initialize the core after power-on reset, the application must follow the sequence in 31.4.1 Overview: Programming the Core. Before it can communicate with the host, it must initialize an endpoint as described in 31.4.3.1 Endpoint Initialization. See 31.4.3.2.2.4 Packet Read From FIFO in Device Mode.

Application Requirements

1. Before setting up a periodic OUT transfer, the application must allocate a buffer in the memory to accommodate all data to be received as part of the OUT transfer, then program that buffer's size and start address in the endpoint-specific registers.
2. For Interrupt OUT transfers, the Transfer Size field in the endpoint's Transfer Size register must be a multiple of the maximum packet size of the endpoint, adjusted to the DWORD boundary. The Transfer Size programmed can span across multiple frames based on the periodicity after which the application want to receive the USBAHB_DOEPx_INT.XFERCOMPL interrupt
   - transfer size[epnum] = n * (mps[epnum] + 4 - (mps[epnum] mod 4))
   - packet count[epnum] = n
   - n > 0 (Higher value of n reduces the periodicity of the USBAHB_DOEPx_INT.XFERCOMPL interrupt)
   - 1 < packet count[epnum] < n (Higher value of n reduces the periodicity of the USBAHB_DOEPx_INT.XFERCOMPL interrupt)
3. In DMA mode, the core stores a received data packet in the memory, always starting on a DWORD boundary. If the maximum packet size of the endpoint is not a multiple of 4, the core inserts byte pads at end of a maximum-packet-size packet up to the end of the DWORD. The application will not be informed about the frame number on which a specific packet has been received.
4. On USBAHB_DOEPx_INT.XFERCOMPL interrupt, the application must read the endpoint's Transfer Size register to calculate the size of the payload in the memory. The received payload size can be less than the programmed transfer size.
   - Payload size in memory = application-programmed initial transfer size – core updated final transfer size
   - Number of USB packets in which this payload was received = application-programmed initial packet count – core updated final packet count.
   - If for some reason, the host stops sending tokens, there are no interrupts to the application, and the application must timeout on its own.
5. The assertion of the USBAHB_DOEPx_INT.XFERCOMPL interrupt marks the completion of the interrupt OUT data transfer. This interrupt does not necessarily mean that the data in memory is good.
6. Read the USBAHB_DOEPx_TSIZ register to determine the size of the received transfer and to determine the validity of the data received in the frame.

Internal Data Flow

1. The application must set the Transfer Size and Packet Count fields in the endpoint-specific registers, clear the NAK bit, and enable the endpoint to receive the data.
   - The application must enable the USBAHB_DCTL.IGNRFRMNUM
2. When an interrupt OUT endpoint is enabled by setting the Endpoint Enable and clearing the NAK bits, the Even/Odd frame will be ignored by the core.

1. Once the NAK bit is cleared, the core starts receiving data and writes it to the receive FIFO, as long as there is space in the receive FIFO. For every data packet received on the USB, the data packet and its status are written to the receive FIFO. Every packet (maximum packet size or short packet) written to the receive FIFO decrements the Packet Count field for that endpoint by 1.
   - OUT data packets received with Bad Data CRC or any packet error are flushed from the receive FIFO automatically.
   - Interrupt packets with PID errors are not passed to application. Core discards the packet, sends ACK and does not decrement packet count.
   - If there is no space in the receive FIFO, interrupt data packets are ignored and not written to the receive FIFO. Additionally, interrupt OUT tokens receive a NAK handshake reply.
2. When the packet count becomes 0 or when a short packet is received on the endpoint, the NAK bit for that endpoint is set. Once the NAK bit is set, the isochronous or interrupt data packets are ignored and not written to the receive FIFO, and interrupt OUT tokens receive a NAK handshake reply.
3. After the data is written to the receive FIFO, the core's DMA engine reads the data from the receive FIFO and writes it to external memory, one packet at a time per endpoint.
4. At the end of every packet write on the AHB to external memory, the transfer size for the endpoint is decremented by the size of the written packet.
5. The OUT Data Transfer Completed pattern for an OUT endpoint is written to the receive FIFO on one of the following conditions.
   - The transfer size is 0 and the packet count is 0.
   - The last OUT data packet written to the receive FIFO is a short packet (0 < packet size < maximum packet size)
6. When either the application or the DMA pops this entry (OUT Data Transfer Completed), a Transfer Completed interrupt is generated for the endpoint and the endpoint enable is cleared.

31.4.3.2.2.11 Generic Isochronous OUT Data Transfers Without Thresholding Using Periodic Transfer Interrupt Feature

This section describes a regular isochronous OUT data transfer with the Periodic Transfer Interrupt feature.

To initialize the core after power-on reset, the application must follow the sequence in 31.4.1 Overview: Programming the Core. Before it can communicate with the host, it must initialize an endpoint as described in 31.4.3.1 Endpoint Initialization. For packet writes in Device mode, see: 31.4.3.2.2.4 Packet Read From FIFO in Device Mode.

Application Requirements

1. Before setting up ISOC OUT transfers spanned across multiple frames, the application must allocate buffer in the memory to accommodate all data to be received as part of the OUT transfers, then program that buffer's size and start address in the endpoint-specific registers.
   - The application must mask the USBAHB_GINTSTS.INCOMPLP (Incomplete ISO OUT).
   - The application must enable the USBAHB_DCTL.IGNRFRMNUM
2. For ISOC transfers, the Transfer Size field in the USBAHB_DOEPx_TSIZ.XFERSIZE register must be a multiple of the maximum packet size of the endpoint, adjusted to the DWORD boundary. The Transfer Size programmed can span across multiple frames based on the periodicity after which the application wants to receive the USBAHB_DOEPx_INT.XFERCOMPL interrupt
   - transfer size[epnum] = n * (mps[epnum] + 4 - (mps[epnum] mod 4))
   - packet count[epnum] = n
   - n > 0 (Higher value of n reduces the periodicity of the USBAHB_DOEPx_INT.XFERCOMPL interrupt)
   - 1 =< packet count[epnum] =< n (Higher value of n reduces the periodicity of the USBAHB_DOEPx_INT.XFERCOMPL interrupt).
3. In DMA mode, the core stores a received data packet in the memory, always starting on a DWORD boundary. If the maximum packet size of the endpoint is not a multiple of 4, the core inserts byte pads at end of a maximum-packet-size packet up to the end of the DWORD. The application will not be informed about the frame number and the PID value on which a specific OUT packet has been received.
4. The assertion of the USBAHB_DOEPx_INT.XFERCOMPL interrupt marks the completion of the isochronous OUT data transfer. This interrupt does not necessarily mean that the data in memory is good.
   - On USBAHB_DOEPx_INT.XFERCOMPL, the application must read the endpoint's Transfer Size register to calculate the size of the payload in the memory.
   - Payload size in memory = application-programmed initial transfer size - core updated final transfer size
   - Number of USB packets in which this payload was received = application-programmed initial packet count – core updated final packet count.
   - If for some reason, the host stop sending tokens, there will be no interrupt to the application, and the application must timeout on its own.
5. The assertion of the USBAHB_DOEPx_INT.XFERCOMPL can also mark a packet drop on USB due to unavailability of space in the RxFifo or due to any packet errors.
   - The application must read the USBAHB_DOEPx_INT.PKTDRPSTS (USBAHB_DOEPx_INT.Bit[11] is now used as the USBAHB_DOEPx_INT.PKTDRPSTS) register to differentiate whether the USBAHB_DOEPx_INT.XFERCOMPL was generated due to the normal end of transfer or due to dropped packets. In case of packets being dropped on the USB due to unavailability of space in the RxFifo or due to any packet errors the endpoint enable bit is cleared.
   - In case of packet drop on the USB application must re-enable the endpoint after recalculating the values USBAHB_DOEPx_TSIZ.XFERSIZE and USBAHB_DOEPx_TSIZ.PKTCNT.
   - Payload size in memory = application-programmed initial transfer size - core updated final transfer size
   - Number of USB packets in which this payload was received = application-programmed initial packet count - core updated final packet count.

Note: Due to application latencies it is possible that DOEPINT.XFERCOMPL interrupt is generated without DOEPINT.PKTDRPSTS being set, This scenario is possible only if back-to-back packets are dropped for consecutive frames and the PKTDRPSTS is merged, but the XFERSIZE and PktCnt values for the endpoint are nonzero. In this case, the application must proceed further by programming the PKTCNT and XFERSIZE register for the next frame, as it would if PKTDRPSTS were being set.

Figure 31.9 ISOC OUT Application Flow for Periodic Transfer Interrupt Feature on page 1233 gives the application flow for Isochronous OUT Periodic Transfer Interrupt feature.

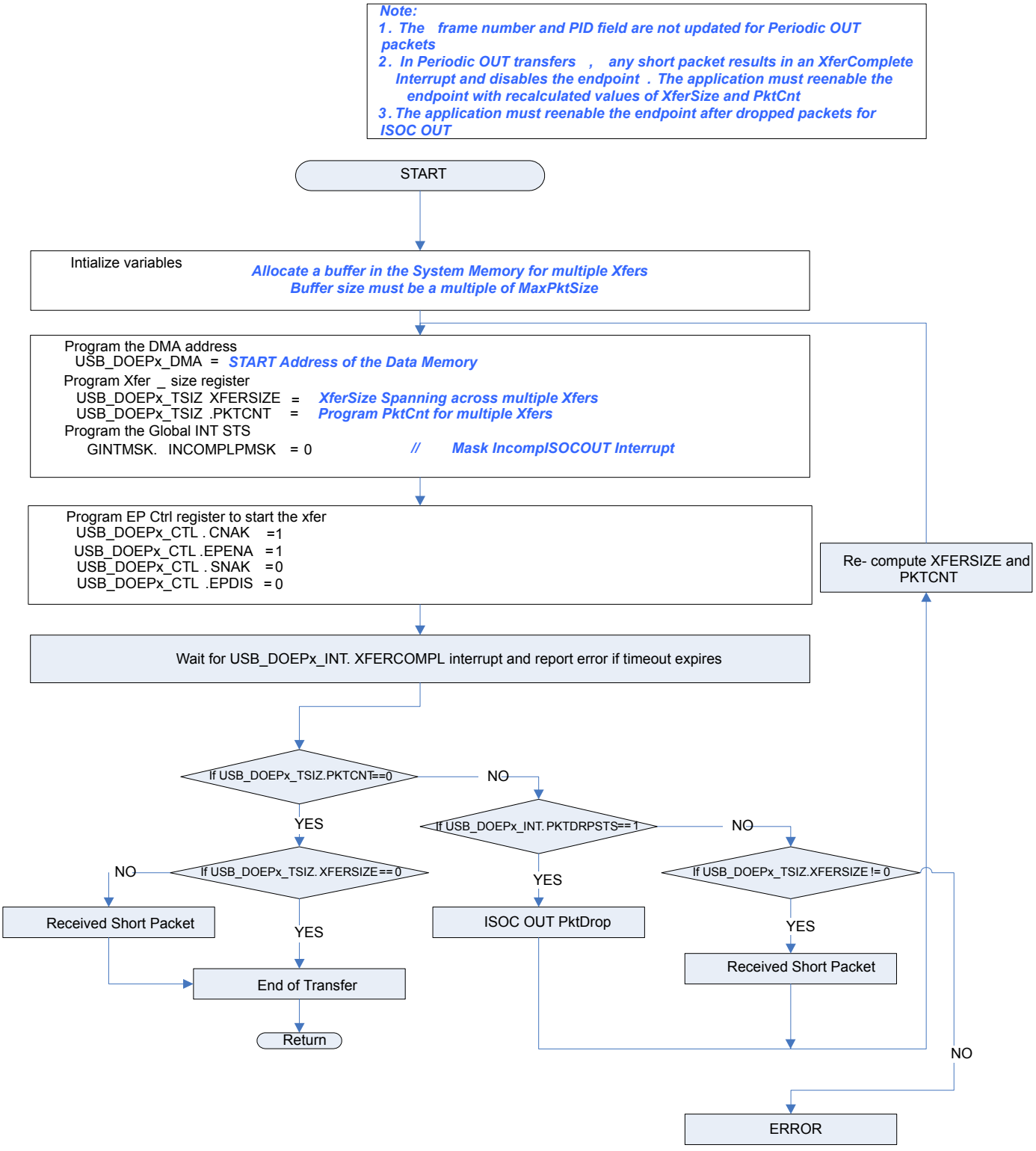


Figure 31.9. ISOC OUT Application Flow for Periodic Transfer Interrupt Feature

Internal Data Flow

1. The application must set the Transfer Size, Packets to be received in a frame and Packet Count Fields in the endpoint-specific registers, clear the NAK bit, and enable the endpoint to receive the data.
2. When an isochronous OUT endpoint is enabled by setting the Endpoint Enable and clearing the NAK bits, the Even/Odd frame will be ignored by the core.

3. Once the NAK bit is cleared, the core starts receiving data and writes it to the receive FIFO, as long as there is space in the receive FIFO. For every data packet received on the USB, the data packet and its status are written to the receive FIFO. Every packet (maximum packet size or short packet) written to the receive FIFO decrements the Packet Count field for that endpoint by 1.
4. When the packet count becomes 0 or when a short packet is received on the endpoint, the NAK bit for that endpoint is set. Once the NAK bit is set, the ISOC packets are ignored and not written to the receive FIFO.
5. After the data is written to the receive FIFO, the core's DMA engine, reads the data from the receive FIFO and writes it to external memory, one packet at a time per endpoint.
6. At the end of every packet write on the AHB to external memory, the transfer size for the endpoint is decremented by the size of the written packet.
7. The OUT Data Transfer Completed pattern for an OUT endpoint is written to the receive FIFO on one of the following conditions.
   - The transfer size is 0 and the packet count is 0
   - The last OUT data packet written to the receive FIFO is a short packet (0 < packet size < maximum packet size).
8. When the DMA pops this entry (OUT Data Transfer Completed), a Transfer Completed interrupt is generated for the endpoint or the endpoint enable is cleared.
9. OUT data packets received with Bad Data CRC or any packet error are flushed from the receive FIFO automatically.
   - In these two cases, the packet count and transfer size registers are not decremented because no data is written to the receive FIFO.

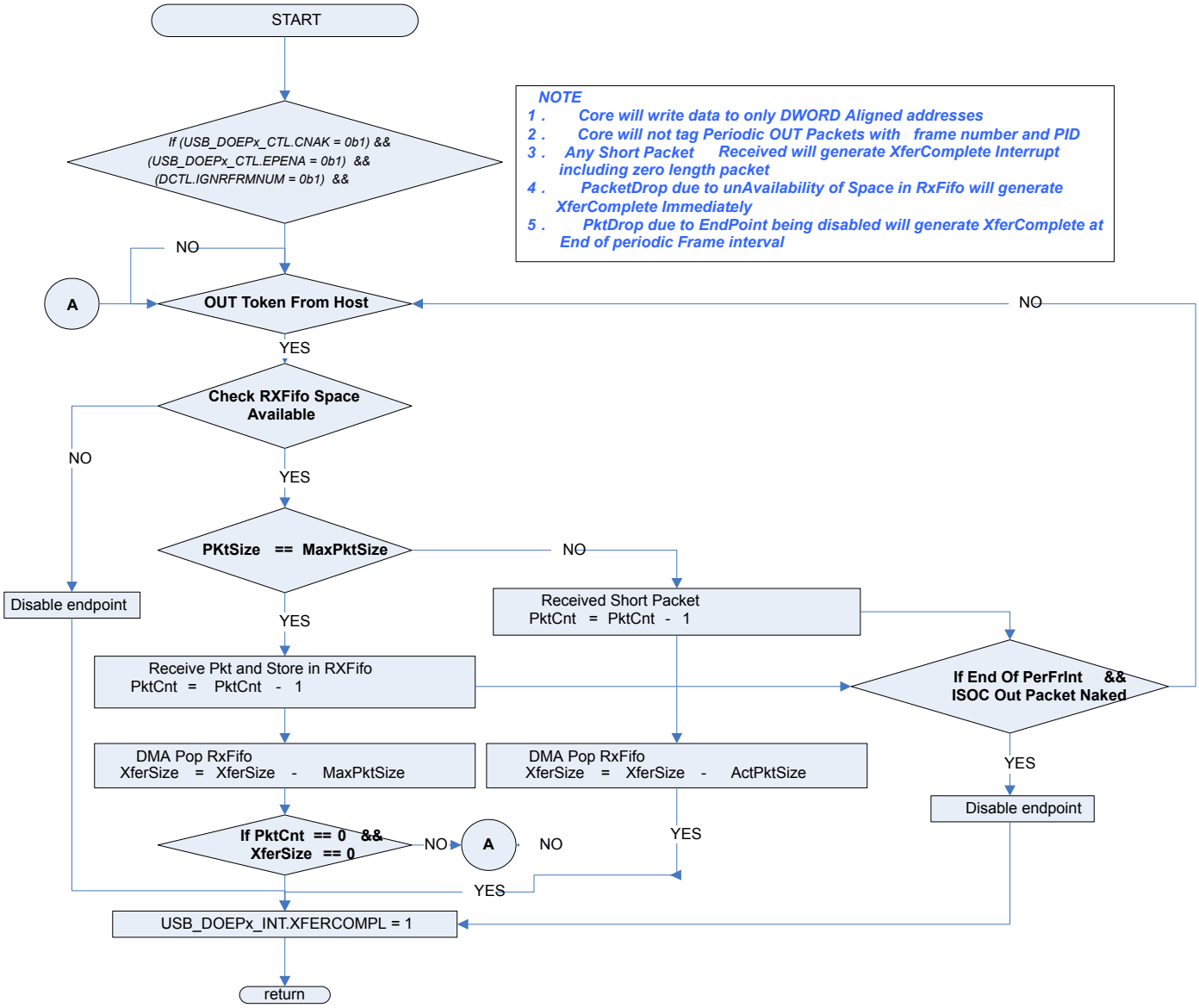


Figure 31.10. Isochronous OUT Core Internal Flow for Periodic Transfer Interrupt Feature

31.4.3.2.2.12 Incomplete Isochronous OUT Data Transfers in DMA and Device Modes

To initialize the core after power-on reset, the application must follow the sequence in 31.4.1 Overview: Programming the Core. Before it can communicate with the host, it must initialize an endpoint as described in 31.4.3.1 Endpoint Initialization. See 31.4.3.2.2.4 Packet Read From FIFO in Device Mode.

This section describes the application programming sequence when isochronous OUT data packets are dropped inside the core.

Internal Data Flow

1. For isochronous OUT endpoints, the USBAHB_DOEPx_INT.XFERCOMPL interrupt possibly is not always asserted. If the core drops isochronous OUT data packets, the application could fail to detect the USBAHB_DOEPx_INT.XFERCOMPL interrupt under the following circumstances.
   - When the receive FIFO cannot accommodate the complete ISO OUT data packet, the core drops the received ISO OUT data. In thresholding this is same as overflow.
   - When the isochronous OUT data packet is received with CRC errors
   - When the isochronous OUT token received by the core is corrupted
   - When the application is very slow in reading the data from the receive FIFO
2. When the core detects an end of periodic frame before transfer completion to all isochronous OUT endpoints, it asserts the USBAHB_GINTSTS.INCOMPLP (Incomplete Isochronous OUT data) interrupt, indicating that a USBAHB_DOEPx_INT.XFERCOMPL interrupt is not asserted on at least one of the isochronous OUT endpoints. At this point, the endpoint with the incomplete transfer remains enabled, but no active transfers remains in progress on this endpoint on the USB.
3. This step is applicable only if the core is operating in Device mode. Application Programming Sequence
4. This step is applicable only if the core is operating in Device mode. Asserting the USBAHB_GINTSTS.INCOMPLP (Incomplete Isochronous OUT data) interrupt indicates that in the current frame, at least one isochronous OUT endpoint has an incomplete transfer.
5. If this occurs because isochronous OUT data is not completely emptied from the endpoint, the application must ensure that the DMA or the application empties all isochronous OUT data (data and status) from the receive FIFO before proceeding.
   - When all data is emptied from the receive FIFO, the application can detect the USBAHB_DOEPx_INT.XFERCOMPL interrupt. In this case, the application must re-enable the endpoint to receive isochronous OUT data in the next frame, as described in 31.4.3.2.2.2 Control Read Transfers (SETUP, Data IN, Status OUT).
6. When it receives a USBAHB_GINTSTS.incomplete Isochronous OUT data interrupt, the application must read the control registers of all isochronous OUT endpoints (USBAHB_DOEPx_CTL) to determine which endpoints had an incomplete transfer in the current frame. An endpoint transfer is incomplete if both the following conditions are met.
   - USBAHB_DOEPx_CTL.DPIDEOF (Even/Odd frame) = USBAHB_DSTS.SOFFN[0]
   - USBAHB_DOEPx_CTL.EPENA (Endpoint Enable) = 1
7. The previous step must be performed before the USBAHB_GINTSTS.SOF interrupt is detected, to ensure that the current frame number is not changed.
8. For isochronous OUT endpoints with incomplete transfers, the application must discard the data in the memory and disable the endpoint by setting the USBAHB_DOEPx_CTL.EPDIS (Endpoint Disable) bit.
9. Wait for the USBAHB_DOEPx_INT.EPDIS (Endpoint Disabled) interrupt and enable the endpoint to receive new data in the next frame as explained in 31.4.3.2.2.2 Control Read Transfers (SETUP, Data IN, Status OUT).
   - Because the core can take some time to disable the endpoint, the application possibly is not able to receive the data in the next frame after receiving bad isochronous data.

31.4.3.2.3 IN Data Transfers in Device and DMA Modes

This section describes the internal data flow and application-level operations during IN data transfers.

- 31.4.3.2.3.1 Packet Write in Device Mode
- 31.4.3.2.3.2 Setting Global Non-Periodic in Endpoint NAK
- 31.4.3.2.3.3 Setting IN Endpoint NAK
- 31.4.3.2.3.4 IN Endpoint Disable
- 31.4.3.2.3.5 Bulk IN Stall
- 31.4.3.2.3.6 Incomplete Isochronous IN Data Transfers
- 31.4.3.2.3.7 Stalling Non-Isochronous IN Endpoints
- 31.4.3.2.3.8 Worst-Case Response Time
- 31.4.3.2.3.9 Choosing the Value of USBAHB_GUSBCFG.USBTRDTIM
- 31.4.3.2.3.10 Handling Babble Conditions
- 31.4.3.2.3.11 Generic Non-Periodic (Bulk and Control) IN Data Transfers Without Thresholding in DMA and Device Mode
- 31.4.3.2.3.12 Examples
- 31.4.3.2.3.14 Generic Periodic IN Data Transfers Without Thresholding Using the Periodic Transfer Interrupt Feature

31.4.3.2.3.1 Packet Write in Device Mode

This section describes how the application writes data packets to the endpoint FIFO in Device mode.

1. The application can either choose polling or interrupt mode.
   - In polling mode, application monitors the status of the endpoint transmit data FIFO, by reading the USBAHB_DIEPx_TXFSTS register, to determine, if there is enough space in the data FIFO.
   - In interrupt mode, application waits for the USBAHB_DIEPx_INT.TXFEMP interrupt and then reads the USBAHB_DIEPx_TXFSTS register, to determine, if there is enough space in the data FIFO.
   - To write a single non-zero length data packet, there must be space to write the entire packet is the data FIFO.
   - For writing zero length packet, application must not look for FIFO space.
2. Using one of the above mentioned methods, when the application determines that there is enough space to write a transmit packet, the application must first write into the endpoint control register, before writing the data into the data FIFO. The application, typically must do a read modify write on the USBAHB_DIEPx_CTL, to avoid modifying the contents of the register, except for setting the Endpoint Enable bit.

The application can write multiple packets for the same endpoint, into the transmit FIFO, if space is available. For periodic IN endpoints, application must write packets only for one frame. It can write packets for the next periodic transaction, only after getting transfer complete for the previous transaction.

31.4.3.2.3.2 Setting Global Non-Periodic in Endpoint NAK

Internal Data Flow

1. When the application sets the Global Non-periodic IN NAK bit (USBAHB_DCTL.SGNPINNAK), the core stops transmitting data on the non-periodic endpoint, irrespective of data availability in the Non-periodic Transmit FIFO.
2. Non-isochronous IN tokens receive a NAK handshake reply
3. The core asserts the USBAHB_GINTSTS.GINNAKEFF interrupt in response to the USBAHB_DCTL.SGNPINNAK bit.
4. Once the application detects this interrupt, it can assume that the core is in the Global Non-periodic IN NAK mode. The application can clear this interrupt by clearing the USBAHB_DCTL.SGNPINNAK bit.

Application Programming Sequence

1. To stop transmitting any data on non-periodic IN endpoints, the application must set the USBAHB_DCTL.SGNPINNAK bit. To set this bit, the following field must be programmed
   - USBAHB_DCTL.SGNPINNAK = 1
2. Wait for the assertion of the USBAHB_GINTSTS.GINNAKEFF interrupt. This interrupt indicates the core has stopped transmitting data on the non-periodic endpoints.
3. The core can transmit valid non-periodic IN data after the application has set the USBAHB_DCTL.SGNPINNAK bit, but before the assertion of the USBAHB_GINTSTS.GINNAKEFF interrupt.
4. The application can optionally mask this interrupt temporarily by writing to the USBAHB_GINTMSK.GINNAKEFFMSK bit.
   - USBAHB_GINTMSK.GINNAKEFFMSK = 0
5. To exit Global Non-periodic IN NAK mode, the application must clear the USBAHB_DCTL.SGNPINNAK. This also clears the USBAHB_GINTSTS.GINNAKEFF interrupt.
   - USBAHB_DCTL.SGNPINNAK = 1
6. If the application has masked this interrupt earlier, it must be unmasked as follows:
   - USBAHB_GINTMSK.GINNAKEFFMSK = 1

31.4.3.2.3.3 Setting IN Endpoint NAK

Internal Data Flow

1. When the application sets the IN NAK for a particular endpoint, the core stops transmitting data on the endpoint, irrespective of data availability in the endpoint's transmit FIFO.
2. Non-isochronous IN tokens receive a NAK handshake reply
   - Isochronous IN tokens receive a zero-data-length packet reply
3. The core asserts the USBAHB_DIEPx_INT.INEPNAKEFF (IN NAK Effective) interrupt in response to the USBAHB_DIEPx_CTL.SNAK (Set NAK) bit.
4. Once this interrupt is seen by the application, the application can assume that the endpoint is in IN NAK mode. This interrupt can be cleared by the application by setting the USBAHB_DIEPx_CTL. Clear NAK bit.

Application Programming Sequence

1. To stop transmitting any data on a particular IN endpoint, the application must set the IN NAK bit. To set this bit, the following field must be programmed.
   - USBAHB_DIEPx_CTL.SNAK = 1
2. Wait for assertion of the USBAHB_DIEPx_INT.INEPNAKEFF (NAK Effective) interrupt. This interrupt indicates the core has stopped transmitting data on the endpoint.
3. The core can transmit valid IN data on the endpoint after the application has set the NAK bit, but before the assertion of the NAK Effective interrupt.
4. The application can mask this interrupt temporarily by writing to the USBAHB_DIEPMSK.INEPNAKEFFMSK (NAK Effective) bit.
   - USBAHB_DIEPMSK.INEPNAKEFFMSK (NAK Effective) = 0
5. To exit Endpoint NAK mode, the application must clear the USBAHB_DIEPx_CTL.NAK status. This also clears the USBAHB_DIEPx_INT.INEPNAKEFF (NAK Effective) interrupt.
   - USBAHB_DIEPx_CTL.CNAK = 1
6. If the application masked this interrupt earlier, it must be unmasked as follows:
   - USBAHB_DIEPMSK.INEPNAKEFFMSK (NAK Effective) = 1

31.4.3.2.3.4 IN Endpoint Disable

Use the following sequence to disable a specific IN endpoint (periodic/non-periodic) that has been previously enabled.

Application Programming Sequence:

1. In Device mode, the application must stop writing data on the AHB, for the IN endpoint to be disabled.
2. The application must set the endpoint in NAK mode. See 31.4.3.2.3.3 Setting IN Endpoint NAK.
   - USBAHB_DIEPx_CTL.SNAK = 1
3. Wait for USBAHB_DIEPx_INT.INEPNAKEFF (NAK Effective) interrupt.
4. Set the following bits in the USBAHB_DIEPx_CTL register for the endpoint that must be disabled.
   - USBAHB_DIEPx_CTL.EPDIS (Endpoint Disable) = 1
   - USBAHB_DIEPx_CTL.SNAK = 1
5. Assertion of USBAHB_DIEPx_INT.EPDISBLD (Endpoint Disabled) interrupt indicates that the core has completely disabled the specified endpoint. Along with the assertion of the interrupt, the core also clears the following bits.
   - USBAHB_DIEPx_CTL.EPENA = 0
   - USBAHB_DIEPx_CTL.EPDIS = 0
6. The application must read the USBAHB_DIEPx_TSIZ register for the periodic IN EP, to calculate how much data on the endpoint was transmitted on the USB.
7. The application must flush the data in the Endpoint transmit FIFO, by setting the following fields in the USBAHB_GRSTCTL register.
   - USBAHB_GRSTCTL.TXFNUM = Endpoint Transmit FIFO Number
   - USBAHB_GRSTCTL.TXFFLSH = 1

The application must poll the USBAHB_GRSTCTL register, until the TXFFLSH bit is cleared by the core, which indicates the end of flush operation. To transmit new data on this endpoint, the application can re-enable the endpoint at a later point.

31.4.3.2.3.5 Bulk IN Stall

These notes refer to Figure 31.11 Bulk IN Stall on page 1239

1. The application has scheduled an IN transfer on receiving the USBAHB_DIEPx_INT.INTKNTXFEMP (IN Token Received When TxFIFO Empty) interrupt.
2. When the transfer is in progress, the application must force a STALL on the endpoint. This could be because the application has received a SetFeature.Endpoint Halt command. The application sets the Stall bit, disables the endpoint and waits for the USBAHB_DIEPx_INT.EPDISBLD (Endpoint Disabled) interrupt. This generates STALL handshakes for the endpoint on the USB.
3. On receiving the interrupt, the application flushes the Non-periodic Transmit FIFO and clears the USBAHB_DCTL.SGNPINNAK (Global IN NP NAK) bit.
4. On receiving the ClearFeature.Endpoint Halt command, the application clears the Stall bit.
5. The endpoint behaves normally and the application can re-enable the endpoint for new transfers

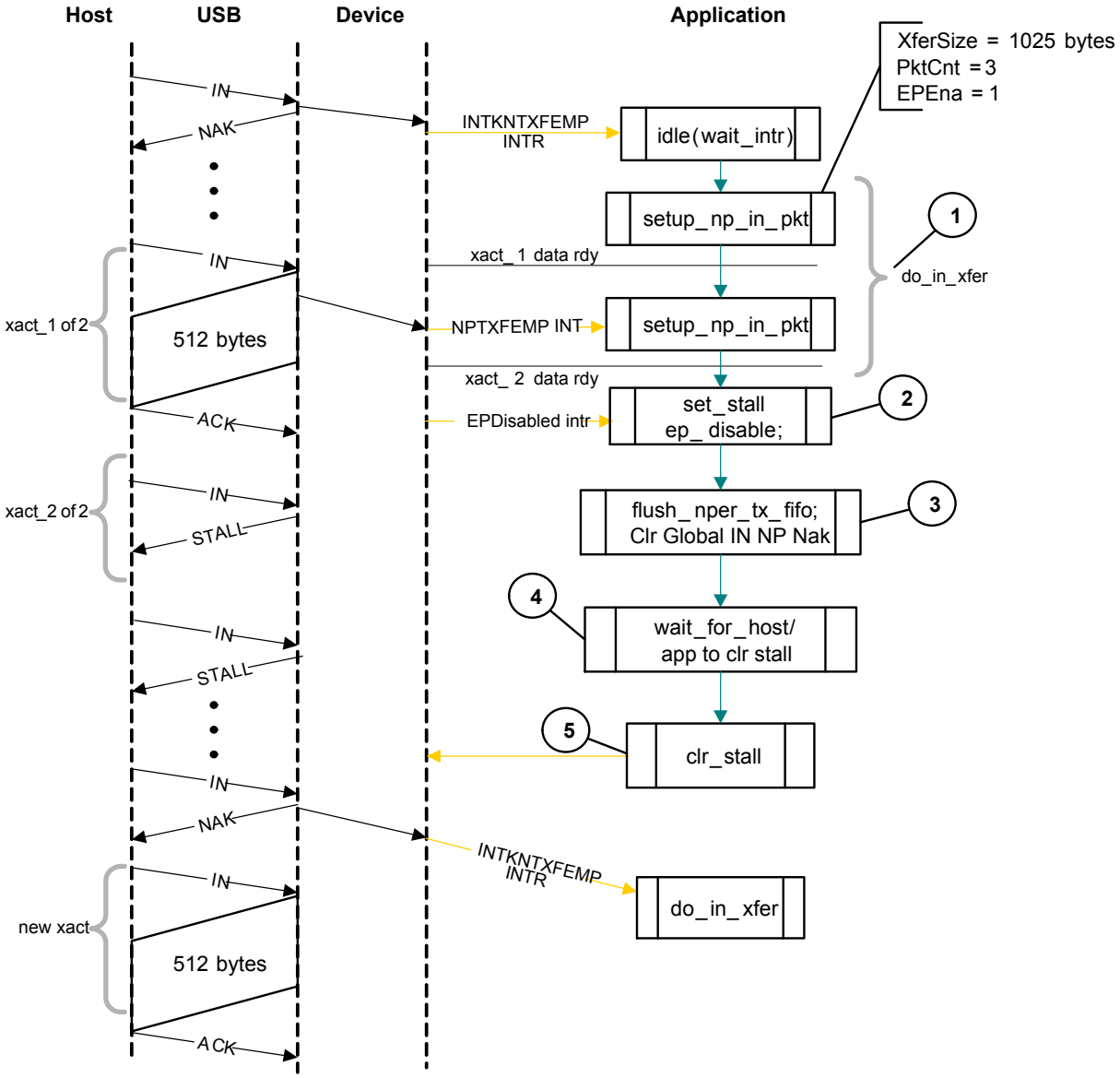


Figure 31.11. Bulk IN Stall

31.4.3.2.3.6 Incomplete Isochronous IN Data Transfers

This section describes what the application must do on an incomplete isochronous IN data transfer.

Internal Data Flow

1. An isochronous IN transfer is treated as incomplete in one of the following conditions.
   a. The core receives a corrupted isochronous IN token on at least one isochronous IN endpoint. In this case, the application detects a USBAHB_GINTSTS.INCOMPISOIN (Incomplete Isochronous IN Transfer) interrupt.
   b. The application or DMA is slow to write the complete data payload to the transmit FIFO and an IN token is received before the complete data payload is written to the FIFO. In this case, the application detects a USBAHB_DIEPx_INT.INTKNTXFEMP (IN Token Received When TxFIFO Empty) interrupt. The application can ignore this interrupt, as it eventually results in a USBAHB_GINTSTS.INCOMPISOIN (Incomplete Isochronous IN Transfer) interrupt at the end of periodic frame.
      i. The core transmits a zero-length data packet on the USB in response to the received IN token.
   c. If thresholding is enabled and there was an underrun condition, the core also generates a USBAHB_DIEPx_INT.TXFIFOUNDRN interrupt. The application can ignore this interrupt, which eventually results in a USBAHB_GINTSTS.INCOMPISOIN (Incomplete ISO IN Transfer) interrupt.
2. In either of the aforementioned cases, in Device mode, the application must stop writing the data payload to the transmit FIFO as soon as possible.
3. The application must set the NAK bit and the disable bit for the endpoint. In DMA mode, the core automatically stops fetching the data payload when the endpoint disable bit is set.
4. The core disables the endpoint, clears the disable bit, and asserts the Endpoint Disable interrupt for the endpoint.

Application Programming Sequence

1. The application can ignore the USBAHB_DIEPx_INT.INTKNTXFEMP (IN Token Received When TxFIFO empty) interrupt on any isochronous IN endpoint, as it eventually results in a USBAHB_GINTSTS.INCOMPISOIN (Incomplete Isochronous IN Transfer) interrupt. The application can also ignore USBAHB_DIEPx_INT.TXFIFOUNDRN interrupt when thresholding is enabled.
2. Assertion of the USBAHB_GINTSTS.INCOMPISOIN (Incomplete Isochronous IN Transfer) interrupt indicates an incomplete isochronous IN transfer on at least one of the isochronous IN endpoints.
3. The application must read the Endpoint Control register for all isochronous IN endpoints to detect endpoints with incomplete IN data transfers.
4. In Device mode, the application must stop writing data to the Periodic Transmit FIFOs associated with these endpoints on the AHB.
5. In both modes of operation, program the following fields in the USBAHB_DIEPx_CTL register to disable the endpoint.
   - USBAHB_DIEPx_CTL.SNAK = 1
   - USBAHB_DIEPx_CTL.EPDIS (Endpoint Disable) = 1
6. The USBAHB_DIEPx_INT.EPDISBLD (Endpoint Disabled) interrupt's assertion indicates that the core has disabled the endpoint.
   - At this point, the application must flush the data in the associated transmit FIFO or overwrite the existing data in the FIFO by enabling the endpoint for a new transfer in the next frame. To flush the data, the application must use the USBAHB_GRSTCTL register.

31.4.3.2.3.7 Stalling Non-Isochronous IN Endpoints

This section describes how the application can stall a non-isochronous endpoint.

Application Programming Sequence

1. Disable the IN endpoint to be stalled. Set the Stall bit as well.
2. USBAHB_DIEPx_CTL.EPDIS (Endpoint Disable) = 1, when the endpoint is already enabled
   - USBAHB_DIEPx_CTL.STALL = 1
   - The Stall bit always takes precedence over the NAK bit
3. Assertion of the USBAHB_DIEPx_INT.EPDISBLD (Endpoint Disabled) interrupt indicates to the application that the core has disabled the specified endpoint.
4. The application must flush the Non-periodic or Periodic Transmit FIFO, depending on the endpoint type. In case of a non-periodic endpoint, the application must re-enable the other non-periodic endpoints, which do not need to be stalled, to transmit data.
5. Whenever the application is ready to end the STALL handshake for the endpoint, the USBAHB_DIEPx_CTL.STALL bit must be cleared.
6. If the application sets or clears a STALL for an endpoint due to a SetFeature.Endpoint Halt command or ClearFeature.Endpoint Halt command, the Stall bit must be set or cleared before the application sets up the Status stage transfer on the control endpoint.

Special Case: Stalling the Control IN/OUT Endpoint

The core must stall IN/OUT tokens if, during the Data stage of a control transfer, the host sends more IN/OUT tokens than are specified in the SETUP packet. In this case, the application must to enable USBAHB_DIEPx_INT.INTKNTXFEMP and USBAHB_DOEPx_INT.OUTTKNEPDIS interrupts during the Data stage of the control transfer, after the core has transferred the amount of data specified in the SETUP packet. Then, when the application receives this interrupt, it must set the STALL bit in the corresponding endpoint control register, and clear this interrupt.

31.4.3.2.3.8 Worst-Case Response Time

When the EFR32xG25 acts as a device, there is a worst case response time for any tokens that follow an isochronous OUT. This worst case response time depends on the AHB clock frequency.

The core registers are in the AHB domain, and the core does not accept another token before updating these register values. The worst case is for any token following an isochronous OUT, because for an isochronous transaction, there is no handshake and the next token could come sooner. This worst case value is 7 PHY clocks in FS mode.

If this worst case condition occurs, the core responds to bulk/interrupt tokens with a NAK and drops isochronous and SETUP tokens. The host interprets this as a timeout condition for SETUP and retries the SETUP packet. For isochronous transfers, the INCOMPISOIN and INCOMPLP interrupts inform the application that isochronous IN/OUT packets were dropped.

31.4.3.2.3.9 Choosing the Value of USBAHB_GUSBCFG.USBTRDTIM

The value in USBAHB_GUSBCFG.USBTRDTIM is the time it takes for the MAC, in terms of PHY clocks after it has received an IN token, to get the FIFO status, and thus the first data from PFC (Packet FIFO Controller) block. This time involves the synchronization delay between the PHY and AHB clocks. This delay is 5 clocks.

Once the MAC receives an IN token, this information (token received) is synchronized to the AHB clock by the PFC (the PFC runs on the AHB clock). The PFC then reads the data from the SPRAM and writes it into the dual clock source buffer. The MAC then reads the data out of the source buffer (4 deep).

If the AHB is running at a higher frequency than the PHY (in Low-speed mode), the application can use a smaller value for USBAHB_GUSBCFG.USBTRDTIM. Figure 31.12 USBTRDTIM Max Timing Case ERROR Wrong Image on page 1243 explains the 5-clock delay. This diagram has the following signals:

- tkn_rcvd: Token received information from MAC to PFC
- dynced_tkn_rcvd: Doubled sync tkn_rcvd, from pclk to hclk domain
- spr_read: Read to SPRAM
- spr_addr: Address to SPRAM
- spr_rdata: Read data from SPRAM
- srcbuf_push: Push to the source buffer
- srcbuf_rdata: Read data from the source buffer. Data seen by MAC

The application can use the following formula to calculate the value of USBAHB_GUSBCFG.USBTRDTIM:

4 * AHB Clock + 1 PHY Clock = (2 clock sync + 1 clock memory address + 1 clock memory data from sync RAM) + (1 PHY Clock (next PHY clock MAC can sample the 2-clock FIFO output)

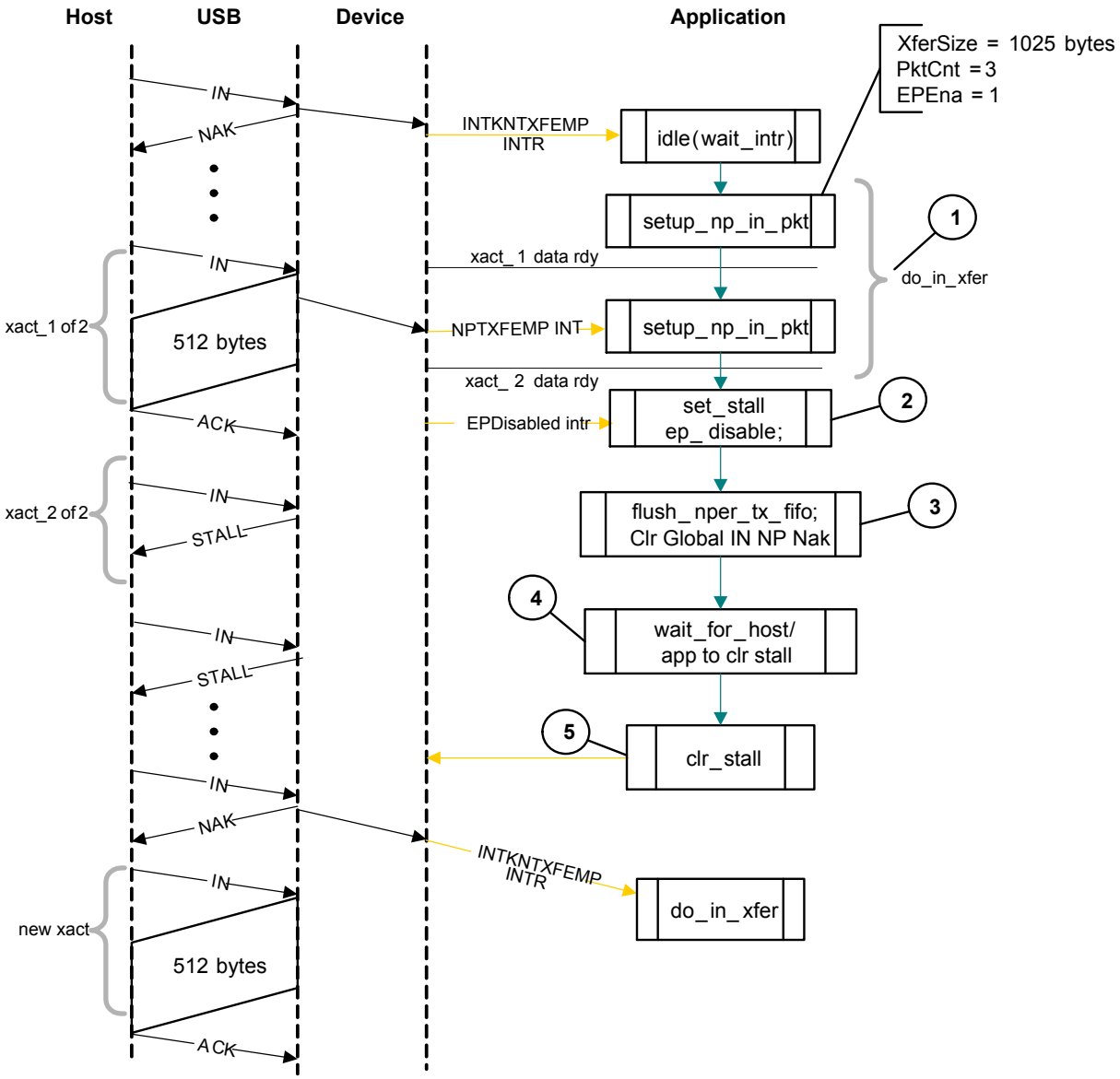


Figure 31.12. USBTRDTIM Max Timing Case ERROR Wrong Image

31.4.3.2.3.10 Handling Babble Conditions

If receives a packet that is larger than the maximum packet size for that endpoint, the core stops writing data to the Rx buffer and waits for the end of packet (EOP). When the core detects the EOP, it flushes the packet in the Rx buffer and does not send any response to the host.

If the core continues to receive data at the EOF2 (the end of frame 2, which is very close to SOF), the core generates an early_suspend interrupt (USBAHB_GINTSTS.ERLYSUSP). On receiving this interrupt, the application must check the erratic_error status bit (USBAHB_DSTS.ERRTICERR). If this bit is set, the application must take it as a long babble and perform a soft reset.

31.4.3.2.3.11 Generic Non-Periodic (Bulk and Control) IN Data Transfers Without Thresholding in DMA and Device Mode

This section describes a regular non-periodic IN data transfer when transmit thresholding is not enabled.

To initialize the core after power-on reset, the application must follow the sequence in 31.4.1 Overview: Programming the Core. Before it can communicate with the host, it must initialize an endpoint as described in 31.4.3.1 Endpoint Initialization. For packet writes in Device mode, see: 31.4.3.2.3.1 Packet Write in Device Mode.

Application Requirements

1. Before setting up an IN transfer, the application must ensure that all data to be transmitted as part of the IN transfer is part of a single buffer, and must program the size of that buffer and its start address (in DMA mode) to the endpoint-specific registers.
2. For IN transfers, the Transfer Size field in the Endpoint Transfer Size register denotes a payload that constitutes multiple maximum-packet-size packets and a single short packet. This short packet is transmitted at the end of the transfer.
   - To transmit a few maximum-packet-size packets and a short packet at the end of the transfer:
   - Transfer size[epnum] = n * mps[epnum] + sp

   (where n is an integer >= 0, and 0 <= sp < mps[epnum])
   - If (sp > 0), then packet count[epnum] = n + 1. Otherwise, packet count[epnum] = n

   a. To transmit a single zero-length data packet:
      - Transfer size[epnum] = 0
      - Packet count[epnum] = 1

   b. To transmit a few maximum-packet-size packets and a zero-length data packet at the end of the transfer, the application must split the transfer in two parts. The first sends maximum-packet-size data packets and the second sends the zero-length data packet alone.

   c. First transfer: transfer size[epnum] = n * mps[epnum]; packet count = n;

   d. Second transfer: transfer size[epnum] = 0; packet count = 1;
3. In DMA mode, the core fetches an IN data packet from the memory, always starting at a DWORD boundary. If the maximum packet size of the IN endpoint is not a multiple of 4, the application must arrange the data in the memory with pads inserted at the end of a maximum-packet-size packet so that a new packet always starts on a DWORD boundary.
4. Once an endpoint is enabled for data transfers, the core updates the Transfer Size register. At the end of IN transfer, which ended with a Endpoint Disabled interrupt, the application must read the Transfer Size register to determine how much data posted in the transmit FIFO was already sent on the USB.
5. Data fetched into transmit FIFO = Application-programmed initial transfer size – core-updated final transfer size
   - Data transmitted on USB = (application-programmed initial packet count – Core updated final packet count) * mps[epnum]
   - Data yet to be transmitted on USB = (Application-programmed initial transfer size – data transmitted on USB)

Internal Data Flow

1. The application must set the Transfer Size and Packet Count fields in the endpoint-specific registers and enable the endpoint to transmit the data.
2. In Device mode, the application must also write the required data to the transmit FIFO for the endpoint. In DMA mode, the core fetches the data from memory according to the application setting for the endpoint.
3. Every time a packet is written into the transmit FIFO, either by the core's internal DMA (in DMA mode) or the application (in Device Mode), the transfer size for that endpoint is decremented by the packet size. The data is fetched from the memory (DMA/Application), until the transfer size for the endpoint becomes 0. After writing the data into the FIFO, the "number of packets in FIFO" count is incremented (this is a 3-bit count, internally maintained by the core for each IN endpoint transmit FIFO. The maximum number of packets maintained by the core at any time in an IN endpoint FIFO is eight). For zero-length packets, a separate flag is set for each FIFO, without any data in the FIFO.
4. Once the data is written to the transmit FIFO, the core reads it out upon receiving an IN token. For every non-isochronous IN data packet transmitted with an ACK handshake, the packet count for the endpoint is decremented by one, until the packet count is zero. The packet count is not decremented on a TIMEOUT.
5. For zero length packets (indicated by an internal zero length flag), the core sends out a zero-length packet for the IN token and decrements the Packet Count field.
6. If there is no data in the FIFO for a received IN token and the packet count field for that endpoint is zero, the core generates a IN Tkn Rcvd When FIFO Empty Interrupt for the endpoint, provided the endpoint NAK bit is not set. The core responds with a NAK handshake for non-isochronous endpoints on the USB.
7. For Control IN endpoint, if there is a TIMEOUT condition, the USBAHB_DIEPx_INT.TIMEOUT interrupt is generated.
8. When the transfer size is 0 and the packet count is 0, the transfer complete interrupt for the endpoint is generated and the endpoint enable is cleared.

Application Programming Sequence

1. Program the USBAHB_DIEPx_TSIZ register with the transfer size and corresponding packet count. In DMA mode, also program the USBAHB_DIEPx_DMAADDR register.

2. Program the USBAHB_DIEPx_CTL register with the endpoint characteristics and set the CNAK and Endpoint Enable bits.
3. In Device mode when transmitting non-zero length data packet, the application must poll the USBAHB_DIEPx_TXFSTS register (where x is the FIFO number associated with that endpoint) to determine whether there is enough space in the data FIFO. The application can optionally use USBAHB_DIEPx_INT.TXFEMP before writing the data.

31.4.3.2.3.12 Examples

Device Mode Bulk IN Transaction

These notes refer to Figure 31.13 Device Mode Bulk IN Transaction on page 1246.

1. The host attempts to read data (IN token) from an endpoint.
2. On receiving the IN token on the USB, the core returns a NAK handshake, because no data is available in the transmit FIFO.
3. To indicate to the application that there was no data to send, the core generates a USBAHB_DIEPx_INT.INTKNTXFEMP (IN Token Received When TxFIFO Empty) interrupt.
4. When data is ready, the application sets up the USBAHB_DIEPx_TSIZ register with the Transfer Size and Packet Count fields.
5. The application writes one maximum packet size or less of data to the Non-periodic TxFIFO.
6. The host reattempts the IN token.
7. Because data is now ready in the FIFO, the core now responds with the data and the host ACKs it.
8. Because the XFERSIZE is now zero, the intended transfer is complete. The device core generates a USBAHB_DIEPx_INT.XFERCOMPL interrupt.
9. The application processes the interrupt and uses the setting of the USBAHB_DIEPx_INT.XFERCOMPL interrupt bit to determine that the intended transfer is complete.

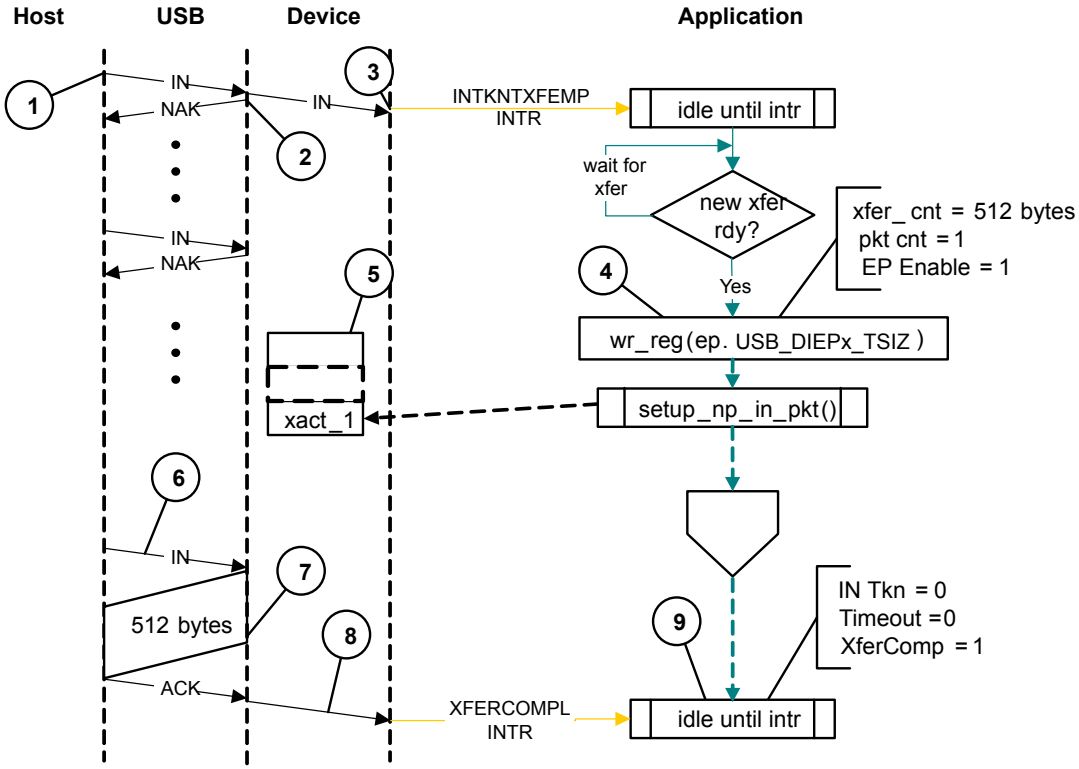


Figure 31.13. Device Mode Bulk IN Transaction

Device Mode Bulk IN Transfer (Pipelined Transaction)

These notes refer to Figure 31.14 Device Mode Bulk IN Transfer (Pipelined Transaction) on page 1247

1. The host attempts to read data (IN token) from an endpoint.
2. On receiving the IN token on the USB, the core returns a NAK handshake, because no data is available in the transmit FIFO.
3. To indicate that there was no data to send, the core generates an USBAHB_DIEPx_INT.INTKNTXFEMP (In Token Received When TxFIFO Empty) interrupt.
4. When data is ready, the application sets up the USBAHB_DIEPx_TSIZ register with the transfer size and packet count.
5. The application writes one maximum packet size or less of data to the Non-periodic TxFIFO.
6. The host reattempts the IN token.
7. Because data is now ready in the FIFO, the core responds with the data, and the host ACKs it.
8. When the TxFIFO level falls below the halfway mark, the core generates a USBAHB_GINTSTS.NPTXFEMP (NonPeriodic TxFIFO Empty) interrupt. This triggers the application to start writing additional data packets to the FIFO.
9. A data packet for the second transaction is ready in the TxFIFO.

10. A data packet for third transaction is ready in the TxFIFO while the data for the second packet is being sent on the bus.
11. The second data packet is sent to the host.
12. The last short packet is sent to the host.
13. Because the last packet is sent and XFERSIZE is now zero, the intended transfer is complete. The core generates a USBAHB_DIEPx_INT.XFERCOMPL interrupt.
14. The application processes the interrupt and uses the setting of the USBAHB_DIEPx_INT.XFERCOMPL interrupt bit to determine that the intended transfer is complete

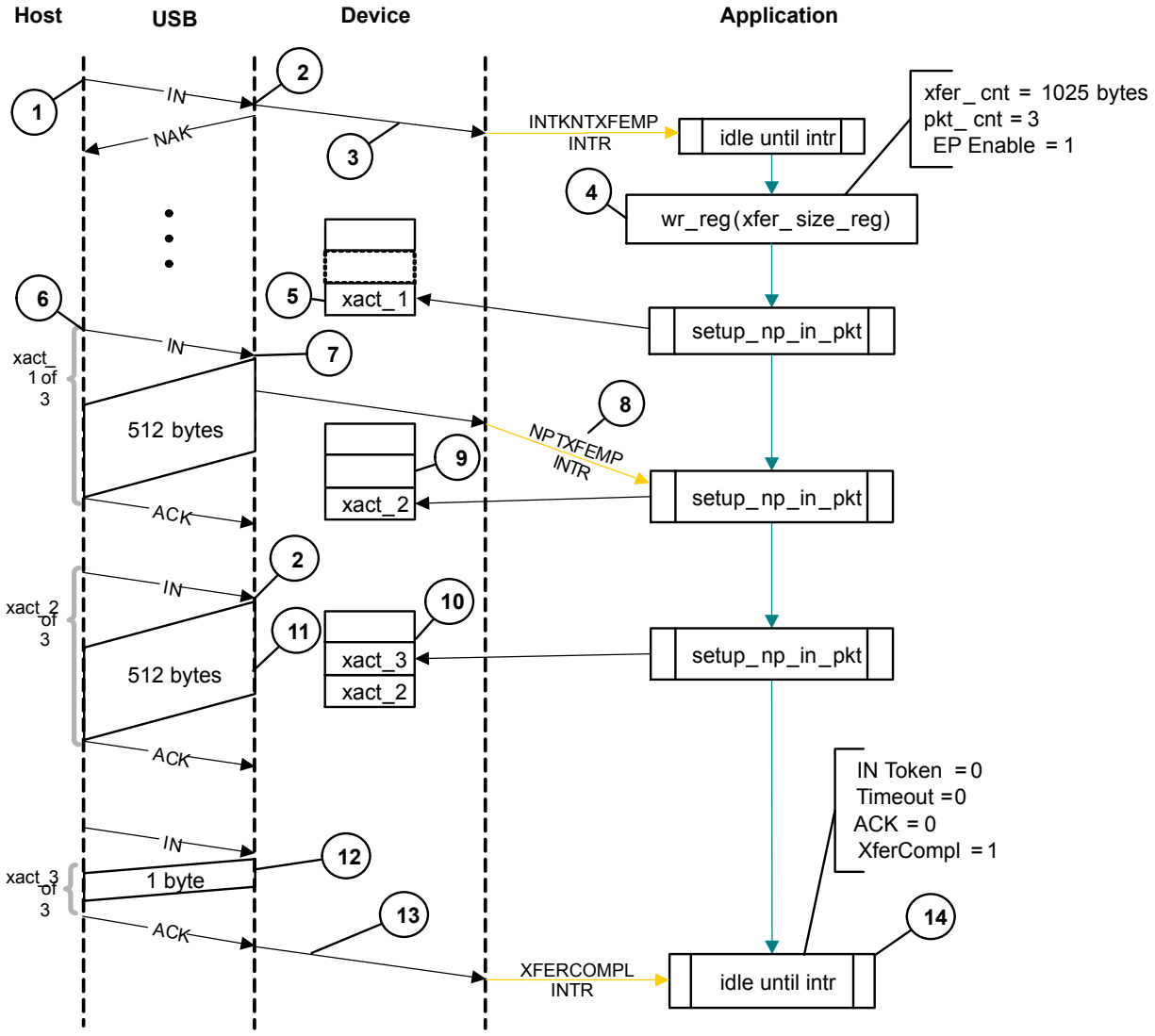


Figure 31.14. Device Mode Bulk IN Transfer (Pipelined Transaction)

Device Mode Bulk IN Two-Endpoint Transfer

These notes refer to Figure 31.15 Device Mode Bulk IN Two-Endpoint Transfer on page 1249

1. The host attempts to read data (IN token) from endpoint 1.
2. On receiving the IN token on the USB, the core returns a NAK handshake, because no data is available in the transmit FIFO for endpoint 1, and generates a USBAHB_DIEP1_INT.INTKNTXFEMP (In Token Received When TxFIFO Empty) interrupt.
3. The application processes the interrupt and initializes USBAHB_DIEP1_TSIZ register with the Transfer Size and Packet Count fields. The application starts writing the transaction data to the transmit FIFO.
4. The application writes one maximum packet size or less of data for endpoint 1 to the Non-periodic TxFIFO.
5. Meanwhile, the host attempts to read data (IN token) from endpoint 2.
6. On receiving the IN token on the USB, the core returns a NAK handshake, because no data is available in the transmit FIFO for endpoint 2, and the core generates a USBAHB_DIEP2_INT.INTKNTXFEMP (In Token Received When TxFIFO Empty) interrupt.
7. Because the application has completed writing the packet for endpoint 1, it initializes the USBAHB_DIEP2_TSIZ register with the Transfer Size and Packet Count fields. The application starts writing the transaction data into the transmit FIFO for endpoint 2.

8. The host repeats its attempt to read data (IN token) from endpoint 1.
9. Because data is now ready in the TxFIFO, the core returns the data, which the host ACKs.
10. Meanwhile, the application has initialized the data for the next two packets in the TxFIFO (ep2.xact1 and ep1.xact2, in order).
11. The host repeats its attempt to read data (IN token) from endpoint 2.
12. Because endpoint 2's data is ready, the core responds with the data (ep2.xact_1), which the host ACKs.
13. Meanwhile, the application has initialized the data for the next two packets in the TxFIFO (ep2.xact2 and ep1.xact3, in order). The application has finished initializing data for the two endpoints involved in this scenario.
14. The host repeats its attempt to read data (IN token) from endpoint 1.
15. Because data is now ready in the FIFO, the core responds with the data, which the host ACKs.
16. The host repeats its attempt to read data (IN token) from endpoint 2.
17. With data now ready in the FIFO, the core responds with the data, which the host ACKs.
18. With the last packet for endpoint 2 sent and its XFERSIZE now zero, the intended transfer is complete. The core generates a USBAHB_DIEP2_INT.XFERCOMPL interrupt for this endpoint.
19. The application processes the interrupt and uses the setting of the USBAHB_DIEP2_INT.XFERCOMPL interrupt bit to determine that the intended transfer on endpoint 2 is complete.
20. The host repeats its attempt to read data (IN token) from endpoint 1 (last transaction).
21. With data now ready in the FIFO, the core responds with the data, which the host ACKs.
22. Because the last endpoint one packet has been sent and XFERSIZE is now zero, the intended transfer is complete. The core generates a USBAHB_DIEP1_INT.XFERCOMPL interrupt for this endpoint.
23. The application processes the interrupt and uses the setting of the USBAHB_DIEP1_INT.XFERCOMPL interrupt bit to determine that the intended transfer on endpoint 1 is complete.

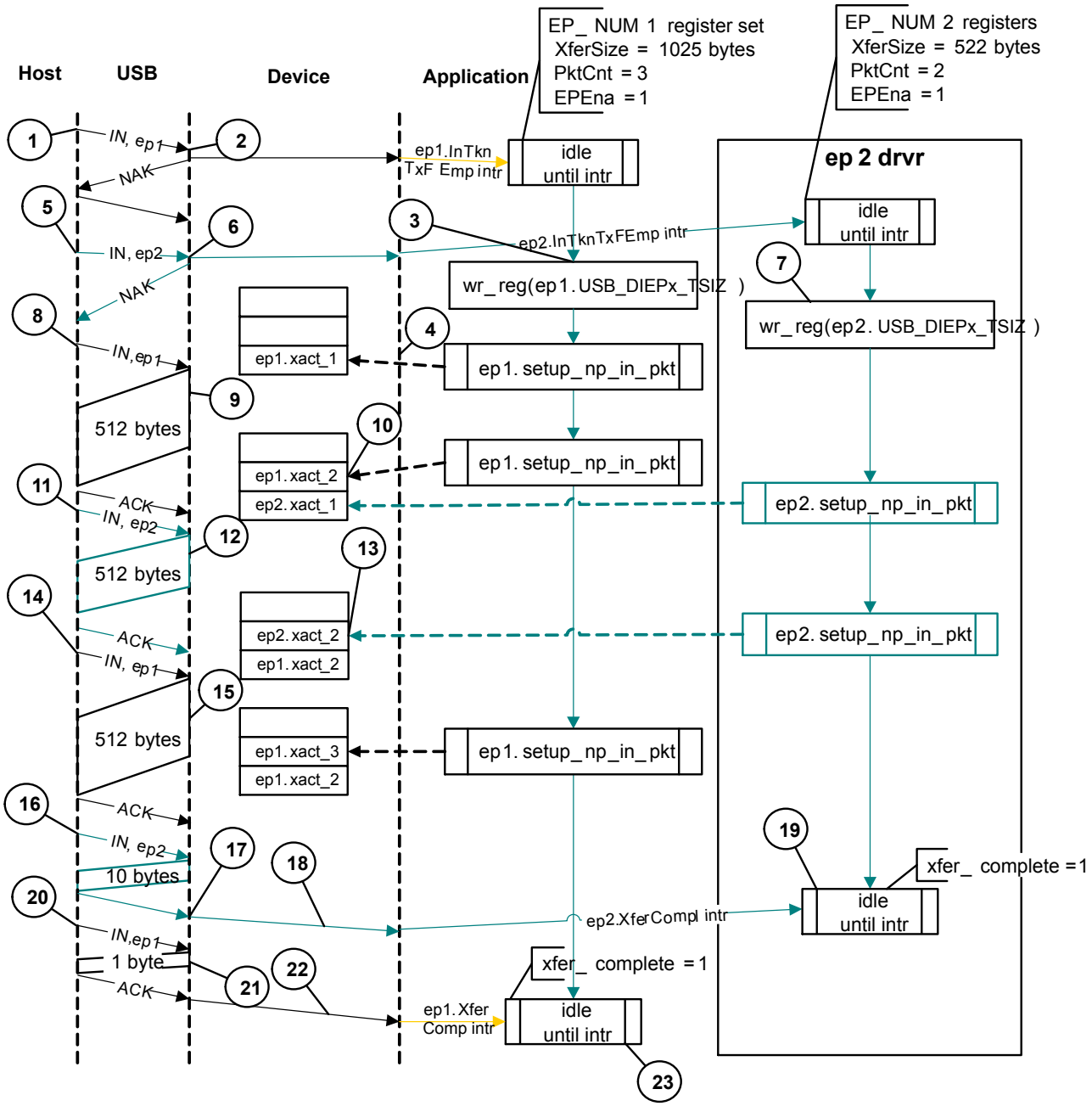


Figure 31.15. Device Mode Bulk IN Two-Endpoint Transfer

31.4.3.2.3.13 Generic Periodic IN (Interrupt and Isochronous) Data Transfers Without Thresholding

This section describes a typical periodic IN data transfer when thresholding is not enabled.

To initialize the core after power-on reset, the application must follow the sequence in 31.4.1 Overview: Programming the Core. Before it can communicate with the host, it must initialize an endpoint as described in 31.4.3.1 Endpoint Initialization. For packet writes in Device mode, see: 31.4.3.2.3.1 Packet Write in Device Mode.

Application Requirements

1. Application requirements 1, 2, 3, and 4 of 31.4.3.2.3.11 Generic Non-Periodic (Bulk and Control) IN Data Transfers Without Thresholding in DMA and Device Mode also apply to periodic IN data transfers, except for a slight modification of Requirement 2.
   - The application can only transmit multiples of maximum-packet-size data packets or multiples of maximum-packet-size packets, plus a short packet at the end. To transmit a few maximum-packet-size packets and a short packet at the end of the transfer, the following conditions must be met.
     - transfer size[epnum] = n * mps[epnum] + sp(where n is an integer 0, and 0 >= sp < mps[epnum])
     - If (sp > 0), packet count[epnum] = n + 1Otherwise, packet count[epnum] = n;
     - mc[epnum] = packet count[epnum]
   - The application cannot transmit a zero-length data packet at the end of transfer. It can transmit a single zero-length data packet by it self. To transmit a single zero-length data packet,
   - transfer size[epnum] = 0
     - packet count[epnum] = 1
     - mc[epnum] = packet count[epnum]
2. The application can only schedule data transfers 1 frame at a time.
   - (USBAHB_DIEPx_TSIZ.MC – 1) * USBAHB_DIEPx_CTL.MPS =< USBAHB_DIEPx_TSIZ.XFERSIZE =< USBAHB_DIEPx_TSIZ.MC * USBAHB_DIEPx_CTL.MPS
   - USBAHB_DIEPx_TSIZ.PKTCNT = USBAHB_DIEPx_TSIZ.MC
   - If USBAHB_DIEPx_TSIZ.XFERSIZE < USBAHB_DIEPx_TSIZ.MC * USBAHB_DIEPx_CTL.MPS, the last data packet of the transfer is a short packet.
3. This step is not applicable for isochronous data transfers, only for interrupt transfers.

   The application can schedule data transfers for multiple frames, only if multiples of max packet sizes (up to 3 packets), must be transmitted every frame. This is can be done, only when the core is operating in DMA mode. This is not a recommended mode though.
   - ((n*USBAHB_DIEPx_TSIZ.MC) - 1)*USBAHB_DIEPx_CTL.MPS <= USBAHB_DIEPx_TSIZ.XFERSIZE <= n*USBAHB_DIEPx_TSIZ.MC*USBAHB_DIEPx_CTL.MPS
   - USBAHB_DIEPx_TSIZ.PKTCNT = n*USBAHB_DIEPx_TSIZ.MC
   - n is the number of frames for which the data transfers are scheduled

   Data Transmitted per frame in this case would be USBAHB_DIEPx_TSIZ.MC*USBAHB_DIEPx_CTL.MPS, in all the frames except the last one. In the frame “n”, the data transmitted would be (USBAHB_DIEPx_TSIZ.XFERSIZE - (n-1)*USBAHB_DIEPx_TSIZ.MC*USBAHB_DIEPx_CTL.MPS)
4. For Periodic IN endpoints, the data must always be prefetched 1 frame ahead for transmission in the next frame. This can be done, by enabling the Periodic IN endpoint 1 frame ahead of the frame in which the data transfer is scheduled.
5. The complete data to be transmitted in the frame must be written into the transmit FIFO (either by the application or the DMA), before the Periodic IN token is received. Even when 1 DWORD of the data to be transmitted per frame is missing in the transmit FIFO when the Periodic IN token is received, the core behaves as when the FIFO was empty. When the transmit FIFO is empty,
6. A zero data length packet would be transmitted on the USB for ISO IN endpoints
   - A NAK handshake would be transmitted on the USB for INTR IN endpoints
7. For a High Bandwidth IN endpoint with three packets in a frame, the application can program the endpoint FIFO size to be 2*max_pkt_size and have the third packet load in after the first packet has been transmitted on the USB.

Internal Data Flow

1. The application must set the Transfer Size and Packet Count fields in the endpoint-specific registers and enable the endpoint to transmit the data.
2. In Device mode, the application must also write the required data to the associated transmit FIFO for the endpoint. In DMA mode, the core fetches the data for the endpoint from memory, according to the application setting.
3. Every time either the core’s internal DMA (in DMA mode) or the application (in Device mode) writes a packet to the transmit FIFO, the transfer size for that endpoint is decremented by the packet size. The data is fetched from DMA or application memory until the transfer size for the endpoint becomes 0.

4. When an IN token is received for an periodic endpoint, the core transmits the data in the FIFO, if available. If the complete data payload (complete packet) for the frame is not present in the FIFO, then the core generates an IN Token Received When TxFIFO Empty Interrupt for the endpoint.
   - A zero-length data packet is transmitted on the USB for isochronous IN endpoints
   - A NAK handshake is transmitted on the USB for interrupt IN endpoints
5. The packet count for the endpoint is decremented by 1 under the following conditions:
   - For isochronous endpoints, when a zero- or non-zero-length data packet is transmitted
   - For interrupt endpoints, when an ACK handshake is transmitted
   - When the transfer size and packet count are both 0, the Transfer Completed interrupt for the endpoint is generated and the endpoint enable is cleared.
6. At the “Periodic frame Interval” (controlled by USBAHB_DCFG.PERFRINT), when the core finds non-empty any of the isochronous IN endpoint FIFOs scheduled for the current frame non-empty, the core generates a USBAHB_GINTSTS.INCOMPISOIN interrupt.

Application Programming Sequence (Transfer Per Frame)

1. Program the USBAHB_DIEPx_TSIZ register. In DMA mode, also program the USBAHB_DIEPx_DMAADDR register.
2. Program the USBAHB_DIEPx_CTL register with the endpoint characteristics and set the CNAK and Endpoint Enable bits.
3. In Device mode, write the data to be transmitted in the next frame to the transmit FIFO.
4. Asserting the USBAHB_DIEPx_INT.INTKNTXFEMP (In Token Received When TxFifo Empty) interrupt indicates that either the DMA or application has not yet written all data to be transmitted to the transmit FIFO.
5. If the interrupt endpoint is already enabled when this interrupt is detected, ignore the interrupt. If it is not enabled, enable the endpoint so that the data can be transmitted on the next IN token attempt.
   - If the isochronous endpoint is already enabled when this interrupt is detected, see 31.4.3.2.3.6 Incomplete Isochronous IN Data Transfers for more details.
6. The core handles timeouts internally on interrupt IN endpoints programmed as periodic endpoints without application intervention. The application, thus, never detects a USBAHB_DIEPx_INT.TIMEOUT interrupt for periodic interrupt IN endpoints.
7. Asserting the USBAHB_DIEPx_INT.XFERCOMPL interrupt with no USBAHB_DIEPx_INT.INTKNTXFEMP (In Token Received When TxFifo Empty) interrupt indicates the successful completion of an isochronous IN transfer. A read to the USBAHB_DIEPx_TSIZ register must indicate transfer size = 0 and packet count = 0, indicating all data is transmitted on the USB.
8. Asserting the USBAHB_DIEPx_INT.XFERCOMPL interrupt, with or without the USBAHB_DIEPx_INT.INTKNTXFEMP (In Token Received When TxFifo Empty) interrupt, indicates the successful completion of an interrupt IN transfer. A read to the USBAHB_DIEPx_TSIZ register must indicate transfer size = 0 and packet count = 0, indicating all data is transmitted on the USB.
9. Asserting the USBAHB_GINTSTS.INCOMPISOIN (Incomplete Isochronous IN Transfer) interrupt with none of the aforementioned interrupts indicates the core did not receive at least 1 periodic IN token in the current frame.
10. For isochronous IN endpoints, see 31.4.3.2.3.6 Incomplete Isochronous IN Data Transfers, for more details.

31.4.3.2.3.14 Generic Periodic IN Data Transfers Without Thresholding Using the Periodic Transfer Interrupt Feature

This section describes a typical Periodic IN (ISOC / INTR) data transfer with the Periodic Transfer Interrupt feature, when Thresholding is not enabled.

1. Before setting up an IN transfer, the application must ensure that all data to be transmitted as part of the IN transfer is part of a single buffer, and must program the size of that buffer and its start address (in DMA mode) to the endpoint-specific registers.
2. For IN transfers, the Transfer Size field in the Endpoint Transfer Size register denotes a payload that constitutes multiple maximum-packet-size packets and a single short packet. This short packet is transmitted at the end of the transfer.
   a. To transmit a few maximum-packet-size packets and a short packet at the end of the transfer:
      - Transfer size[epnum] = n * mps[epnum] + sp

      (where n is an integer > 0, and 0 < sp < mps[epnum]. A higher value of n reduces the periodicity of the USBAHB_DOEPx_INT.XFERCOMPL interrupt)
      - If (sp > 0), then packet count[epnum] = n + 1. Otherwise, packet count[epnum] = n

   b. To transmit a single zero-length data packet:
      - Transfer size[epnum] = 0
      - Packet count[epnum] = 1

   c. To transmit a few maximum-packet-size packets and a zero-length data packet at the end of the transfer, the application must split the transfer in two parts. The first sends maximum-packet-size data packets and the second sends the zero-length data packet alone.
      - First transfer: transfer size[epnum] = n * mps[epnum]; packet count = n;
      - Second transfer: transfer size[epnum] = 0; packet count = 1;

   d. The application can only transmit multiples of maximum-packet-size data packets or multiples of maximum-packet-size packets, plus a short packet at the end. To transmit a few maximum-packet-size packets and a short packet at the end of the transfer, the following conditions must be met.
      - transfer size[epnum] = n * mps[epnum] + sp (where n is an integer > 0, and 0 < sp < mps[epnum])
      - If (sp > 0), packet count[epnum] = n + 1 Otherwise, packet count[epnum] = n;
      - mc[epnum] = number of packets to be sent out in a frame.

   e. The application cannot transmit a zero-length data packet at the end of transfer. It can transmit a single zero-length data packet by itself. To transmit a single zero-length data packet,
      - transfer size[epnum] = 0
      - packet count[epnum] = 1
      - mc[epnum] = packet count[epnum]
3. In DMA mode, the core fetches an IN data packet from the memory, always starting at a DWORD boundary. If the maximum packet size of the IN endpoint is not a multiple of 4, the application must arrange the data in the memory with pads inserted at the end of a maximum-packet-size packet so that a new packet always starts on a DWORD boundary.
4. Once an endpoint is enabled for data transfers, the core updates the Transfer Size register. At the end of IN transfer, which ended with a Endpoint Disabled interrupt, the application must read the Transfer Size register to determine how much data posted in the transmit FIFO was already sent on the USB.
   - Data fetched into transmit FIFO = Application-programmed initial transfer size - core-updated final transfer size
   - Data transmitted on USB = (application-programmed initial packet count - Core updated final packet count) * mps[epnum]
   - Data yet to be transmitted on USB = (Application-programmed initial transfer size - data transmitted on USB)
5. The application can schedule data transfers for multiple frames, only if multiples of max packet sizes (up to 3 packets), must be transmitted every frame. This is can be done, only when the core is operating in DMA mode.
   - ((n*USBAHB_DIEPx_TSIZ.MC) - 1)*USBAHB_DIEPx_CTL.MPS <= USBAHB_DIEPx_TSIZ.XFERSIZE <= n*USBAHB_DIEPx_TSIZ.MC*USBAHB_DIEPx_CTL.MPS
   - USBAHB_DIEPx_TSIZ.PKTCNT = n*USBAHB_DIEPx_TSIZ.MC
   - n is the number of frames for which the data transfers are scheduled. Data Transmitted per frame in this case is USBAHB_DIEPx_TSIZ.MC*USBAHB_DIEPx_CTL.MPS in all frames except the last one. In frame n, the data transmitted is (USBAHB_DIEPx_TSIZ.XFERSIZE – (n – 1) * USBAHB_DIEPx_TSIZ.MC * USBAHB_DIEPx_CTL.MPS)
6. For Periodic IN endpoints, the data must always be prefetched 1 frame ahead for transmission in the next frame. This can be done, by enabling the Periodic IN endpoint 1 frame ahead of the frame in which the data transfer is scheduled.
7. The complete data to be transmitted in the frame must be written into the transmit FIFO, before the Periodic IN token is received. Even when 1 DWORD of the data to be transmitted per frame is missing in the transmit FIFO when the Periodic IN token is received, the core behaves as when the FIFO was empty. When the transmit FIFO is empty,
   - A zero data length packet would be transmitted on the USB for ISOC IN endpoints
   - A NAK handshake would be transmitted on the USB for INTR IN endpoints
   - USBAHB_DIEPx_TSIZ.PKTCNT is not decremented in this case.

8. For a High Bandwidth IN endpoint with three packets in a frame, the application can program the endpoint FIFO size to be 2 * max_pkt_size and have the third packet load in after the first packet has been transmitted on the USB.

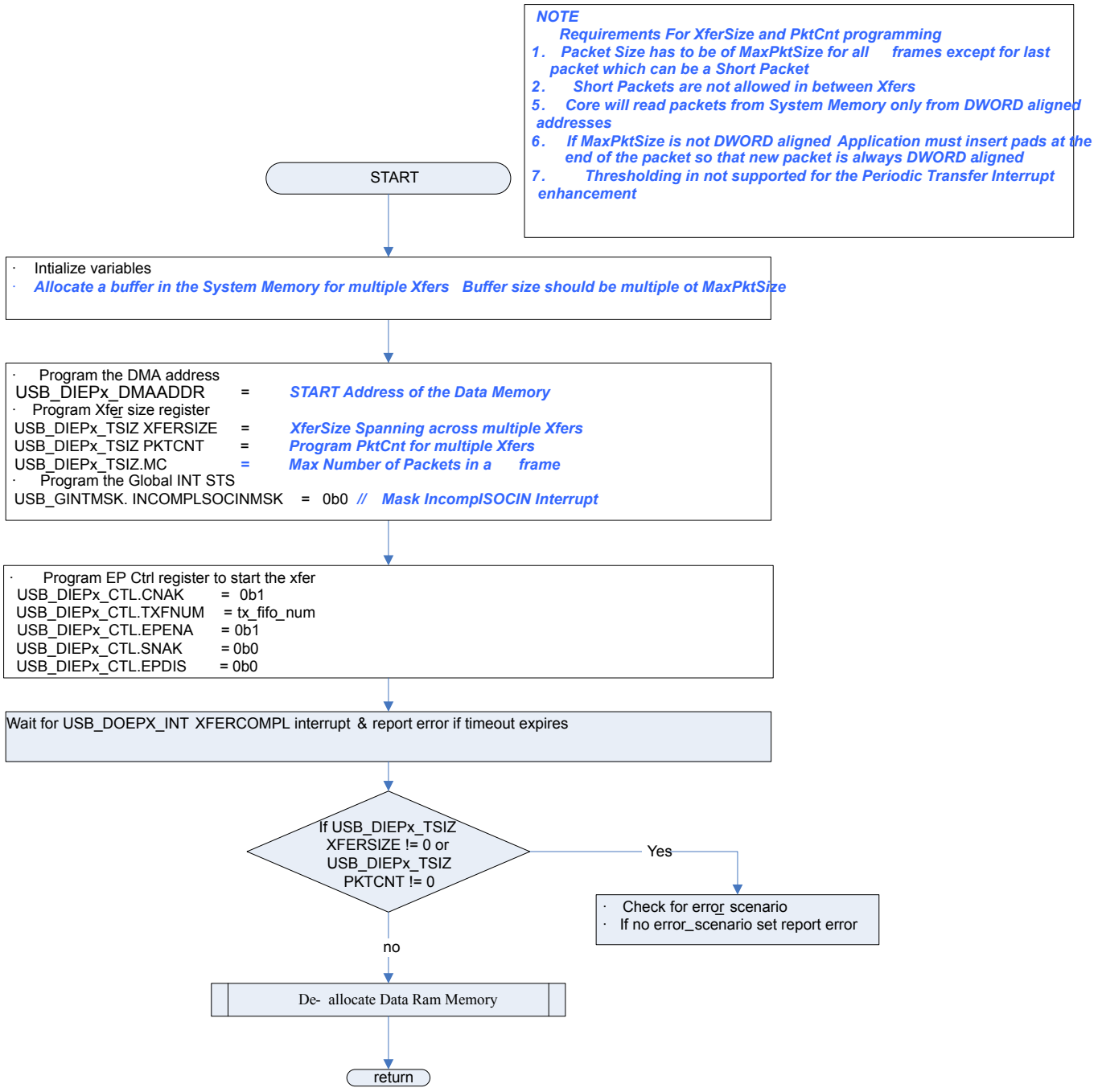


Figure 31.16. Periodic in Application Flow for Periodic Transfer Interrupt Feature

Internal Data Flow

1. The application must set the Transfer Size and Packet Count fields in the endpoint-specific registers and enable the endpoint to transmit the data.
   - The application must enable the USBAHB_DCTL.IGNRFRMNUM
2. When an isochronous OUT endpoint is enabled by setting the Endpoint Enable and clearing the NAK bits, the Even/Odd frame will be ignored by the core.
   - Subsequently the core updates the Even / Odd bit on its own
3. Every time either the core's internal DMA writes a packet to the transmit FIFO, the transfer size for that endpoint is decremented by the packet size. The data is fetched from DMA or application memory until the transfer size for the endpoint becomes 0.

4. When an IN token is received for a periodic endpoint, the core transmits the data in the FIFO, if available. If the complete data payload (complete packet) for the frame is not present in the FIFO, then the core generates an IN Token Received When TxFifo Empty Interrupt for the endpoint.
   - A zero-length data packet is transmitted on the USB for isochronous IN endpoints
   - A NAK handshake is transmitted on the USB for interrupt IN endpoints
5. If an IN token comes for an endpoint on the bus, and if the corresponding TxFIFO for that endpoint has at least 1 packet available, and if the USBAHB_DIEPx_CTL.NAK bit is not set, and if the internally maintained even/odd bit match with the bit 0 of the current frame number, then the core will send this data out on the USB. The core will also decrement the packet count. Core also toggles the MultCount in USBAHB_DIEPx_CTL register and based on the value of MultCount the next PID value is sent.
   - If the IN token results in a timeout (core did not receive the handshake or handshake error), core rewind the FIFO pointers. Core does not decrement packet count. It does not toggle PID. USBAHB_DIEPx_INT.TIMEOUT interrupt will be set which the application could check.
   - At the end of periodic frame interval (Based on the value programmed in the USBAHB_DCFG.PERFRINT register, core will internally set the even/odd internal bit to match the next frame.
6. The packet count for the endpoint is decremented by 1 under the following conditions:
   - For isochronous endpoints, when a zero- or non-zero-length data packet is transmitted
   - For interrupt endpoints, when an ACK handshake is transmitted
7. The data PID of the transmitted data packet is based on the value of USBAHB_DIEPx_TSIZ.MC programmed by the application. In case the USBAHB_DIEPx_TSIZ.MC value is set to 3 then, for a particular frame the core expects to receive 3 Isochronous IN token for the respective endpoint. The data PIDs transmitted will be D2 followed by D1 and D0 respectively for the tokens.
   - If any of the tokens responded with a zero-length packet due to non-availability of data in the TxFIFO, the packet is sent in the next frame with the pending data PID. For example, in a frame, the first received token is responded to with data and data PID value D2. If the second token is responded to with a zero-length packet, the host is expected not to send any more tokens for the respective endpoint in the current frame. When a token arrives in the next frame it will be responded to with the pending data PID value of D1.
   - Similarly the second token of the current frame gets responded with D0 PID. The host is expected to send only two tokens for this frame as the first token got responded with D1 PID.
8. When the transfer size and packet count are both 0, the Transfer Completed interrupt for the endpoint is generated and the endpoint enable is cleared.
9. The USBAHB_GINTSTS.INCOMPISOIN will be masked by the application hence at the Periodic Frame interval (controlled by USBAHB_DCFG.PERFRINT), even though the core finds non-empty any of the isochronous IN endpoint FIFOs, USBAHB_GINTSTS.INCOMPISOIN interrupt will not be generated.

31.4.4 FIFO RAM Allocation

The follwing sections detail how data FIFO RAM is allocated.

31.4.4.1 Data FIFO RAM Allocation

External RAM must be allocated among different FIFOs in the core before any transactions can start. The application must follow this procedure every time it changes core FIFO RAM allocation.

The application must allocate data RAM per FIFO based on the AHB's operating frequency, the PHY Clock frequency, the available AHB bandwidth, and the performance required on the USB. Based on the above mentioned criteria, the application must provide a table as described below with RAM sizes for each FIFO in each mode.

The core shares a single FIFO RAM between transmit FIFO(s) and receive FIFO.

In DMA mode—The FIFO RAM is also used for storing the some register information.

The Device mode Endpoint DMA address registers (USBAHB_DIEP0DMAADDR, USBAHB_DOEP0DMAADDR, USBAHB_DIEPx_DMAADDR, USBAHB_DOEPx_DMAADDR) and Host mode Channel DMA registers (USB_HCx_DMAADDR) are stored in the FIFO RAM.

- These register information are stored at the end of the FIFO RAM after the space allocated for receive and Transmit FIFO. These register space must also be taken into account when calculating the total FIFO depth of the core as explained in the following sections.

The registers USBAHB_DIEPx_DMAADDR/USBAHB_DOEPx_DMAADDR are maintained in RAM.

The following rules apply while calculating how much RAM space must be allocated to store these registers.

Device Mode:

- Device mode only: No space needed.
- DMA mode: One location per end point direction.

31.4.4.1.1 Device Mode

When allocating data RAM for FIFOs in Device mode keep in mind the factors in the follwing sections.

31.4.4.1.1.1 Tx FIFO Operation Without Thresholding

1. Receive FIFO RAM allocation:
   - RAM for SETUP Packets: 4 * n + 6 locations must be Reserved in the receive FIFO to receive up to n SETUP packets on control endpoints, where n is the number of control endpoints the device core supports. The core does not use these locations, which are Reserved for SETUP packets, to write any other data.
   - One location for Global OUT NAK
   - Status information is written to the FIFO along with each received packet. Therefore, a minimum space of (Largest Packet Size / 4) + 1 must be allotted to receive packets. If a high-bandwidth endpoint is enabled, or multiple isochronous endpoints are enabled, then at least two (Largest Packet Size / 4) + 1 spaces must be allotted to receive back-to-back packets. Typically, two (Largest Packet Size / 4) + 1 spaces are recommended so that when the previous packet is being transferred to AHB, the USB can receive the subsequent packet. If AHB latency is high, you must allocate enough space to receive multiple packets. This is critical to prevent dropping any isochronous packets.
   - Along with each endpoint's last packet, transfer complete status information is also pushed to the FIFO. Typically, one location for each OUT endpoint is recommended.
2. Transmit FIFO RAM Allocation:

   The minimum RAM space required for each IN Endpoint Transmit FIFO is the maximum packet size for that particular IN endpoint.

   More space allocated in the transmit IN Endpoint FIFO results in a better performance on the USB and can hide latencies on the AHB.

FIFO Name	Data RAM Size
Receive data FIFO	rx_fifo_size. This must include RAM for setup packets, OUT endpoint control information and data OUT packets, as mentioned earlier.
Transmit FIFO 0	tx_fifo_size[0]
Transmit FIFO 1	tx_fifo_size[1]
Transmit FIFO 2	tx_fifo_size[2]
...	...
Transmit FIFO i	tx_fifo_size[i]

With this information, the following registers must be programmed as follows:

1. Receive FIFO Size Register (USBAHB_GRXFSIZ)

   USBAHB_GRXFSIZ.Receive FIFO Depth = rx_fifo_size;
2. Device IN Endpoint Transmit FIFO0 Size Register (USBAHB_GNPTXFSIZ)

   USBAHB_GNPTXFSIZ.non-periodic Transmit FIFO Depth = tx_fifo_size[0];

   USBAHB_GNPTXFSIZ.non-periodic Transmit RAM Start Address = rx_fifo_size;
3. Device IN Endpoint Transmit FIFO#1 Size Register (USBAHB_DIEPTXF1)

   USBAHB_DIEPTXF1. Transmit RAM Start Address = USBAHB_GNPTXFSIZ.FIFO0 Transmit RAM Start Address + tx_fifo_size[0];
4. Device IN Endpoint Transmit FIFO#2 Size Register (USBAHB_DIEPTXF2)

   USBAHB_DIEPTXF2.Transmit RAM Start Address = USBAHB_DIEPTXF1.Transmit RAM Start Address + tx_fifo_size[1];
5. Device IN Endpoint Transmit FIFO#i Size Register (USBAHB_DIEPTXFi)

   USBAHB_DIEPTXFm.Transmit RAM Start Address = USBAHB_DIEPTXFi-1.Transmit RAM Start Address + tx_fifo_size[i-1];
6. The transmit FIFOs and receive FIFO must be flushed after the RAM allocation is done, for the proper functioning of the FIFOs.
   - USBAHB_GRSTCTL.TXFNUM = 0x10
   - USBAHB_GRSTCTL.TXFFLSH = 1
   - USBAHB_GRSTCTL.RXFFLSH = 1

The application must wait until the TXFFLSH bit and the RXFFLSH bits are cleared before performing any operation on the core.

31.4.4.1.2 Calculating the Total FIFO Size

The RxFIFO is shared between the host and device. The Host TxFIFOs are also shared with Device IN endpoint TxFIFOs 0 through n.

There are three ways to calculate the total FIFO size.

Method 1

Use this method if you are using the following conditions:

- Minimum FIFO depth allocation
- The FIFO must equal at least one MaxPacketSize (MPS).

Device RxFIFO =

- (4 * number of control endpoints + 6) + ((largest USB packet used / 4) + 1 for status information) + (2 * number of OUT endpoints) + 1 for Global NAK

Note: Include the Control OUT endpoint in the number of OUT endpoints.

Host RxFIFO =

- Device mode

  Minimum requirement: (largest USB packet used / 4) + 1 for status information + 1 transfer complete
- DMA mode

  (largest USB packet used / 4) + 1 for status information + 1 transfer complete + 1 location each bulk/control out endpoint for handling NAK scenario

Host Non-Periodic TxFIFO =

- largest non-periodic USB packet used / 4

Host Periodic TxFIFO =

- Sum total of (MPS*MC)/4 of all periodic channels or 1500 locations, whichever is lower.

Device IN Endpoint TxFIFOs (a separate FIFO is allocated to each IN endpoint) =

- IN Endpoints Max packet Size / 4

Method 2

Use this method if you are using the recommended minimum FIFO depth allocation with support for high-bandwidth endpoints. This FIFO allocation enables the core to transfer a packet on the USB while the previous (next) packet is simultaneously transferred to the AHB. This FIFO allocation improves the core's performance.

Device RxFIFO =

- (4 * number of control endpoints + 6) + 2 * ((largest USB packet used / 4) + 1) +(2 * number of OUT endpoints) + 1

Host RxFIFO =

- Device mode

  2 * ((largest USB packet used / 4) + 1 + 1)
- DMA mode

  2 * ((largest USB packet used / 4) + 1 + 1) + 1 location each bulk/control out endpoint for handling NAK scenario

Host Non-Periodic TxFIFO =

- 2 * (largest non-periodic USB packet used / 4)

Host Periodic TxFIFO =

- Sum total of (MPS*MC)/4 for all periodic channels or 1500 location, whichever is lower.

Device IN Endpoint-Specific TxFIFOs (a separate FIFO is allocated to each endpoint) =

- 2 * (max_pkt_size for the endpoint) / 4.

```
//DMA mode

      OTG Total RAM = (Device RxFIFO or Host RxFIFO; choose the largest one) +
```

```
      ((Host Non-Periodic TxFIFO + Host peiodic TxFIFO) or
       (Device IN Endpoint TxFIFO #0 + #1 + #2 + #n)); choose the largest one +
      (1 location per Host channel or 1 location per Device Endpoint direction; choose
       the largest one)

//Device mode

    OTG Total RAM = (Device RxFIFO or Host RxFIFO; choose the largest one) +
    ((Host Non-Periodic TxFIFO + Host peiodic TxFIFO) or
     (Device IN Endpoint TxFIFO #0 + #1 + #2 + #n)); choose the largest one
```

Method 3

Use this method if you are using the recommended FIFO depth allocation that supports high-bandwidth endpoints and high AHB latency.

Note:

- x = (AHB latency + time to transfer largest packet on AHB) / time to transfer largest packet on USB.
- The value of x is an integer. Any fractional value is rounded to the nearest integer. For example: x = 20 ms / 17,039 ms = 1.17 ms = 2 ms.

Device RxFIFO =

- (4 * number of control endpoints + 6) + (x + 1) * ((largest USB packet used / 4) + 1)+ (2 * number of OUT endpoints) + 1

Note: Include the Control OUT endpoint in the number of OUT endpoints.

Host RxFIFO =

- Device mode

  (x + 1) * ((largest USB packet used / 4) + 1 + 1)
- DMA mode

  (x + 1) * ((largest USB packet used / 4) + 1 + 1) + 1 location each bulk/control out endpoint for handling NAK scenario

Host Non-Periodic TxFIFO =

- (x + 1) * (largest non-periodic USB packet used / 4)

Host Periodic TxFIFO =

- (x+1) * (Sum total of (MPS*MC)/4 of all periodic channels or 1500 locations, whichever is lower).

Device IN Endpoint-Specific TxFIFOs (a separate FIFO is allocated to each endpoint) =

- (x+1)*(max_pkt_size for the endpoint)/4

```
//DMA mode
      OTG Total RAM = (Device RxFIFO or Host RxFIFO; choose the largest one) +
      ((Host Non-Periodic TxFIFO + Host periodic TxFIFO) OR
       (Device IN Endpoint TxFIFO #0 + #1 + #2 + #n); choose the largest one) +
      (1 location per Host channel or 1 location per Device Endpoint direction; choose
      the largest one)

//Device mode
    OTG Total RAM = (Device RxFIFO or Host RxFIFO; choose the largest one) +
    ((Host Non-Periodic TxFIFO + Host periodic TxFIFO) OR
     (Device IN Endpoint TxFIFO #0 + #1 + #2 + #n); choose the largest one)
```

31.4.4.2 Dynamic FIFO Allocation

The application can change the RAM allocation for each FIFO during the operation of the core.

The Core Interrupt Handler

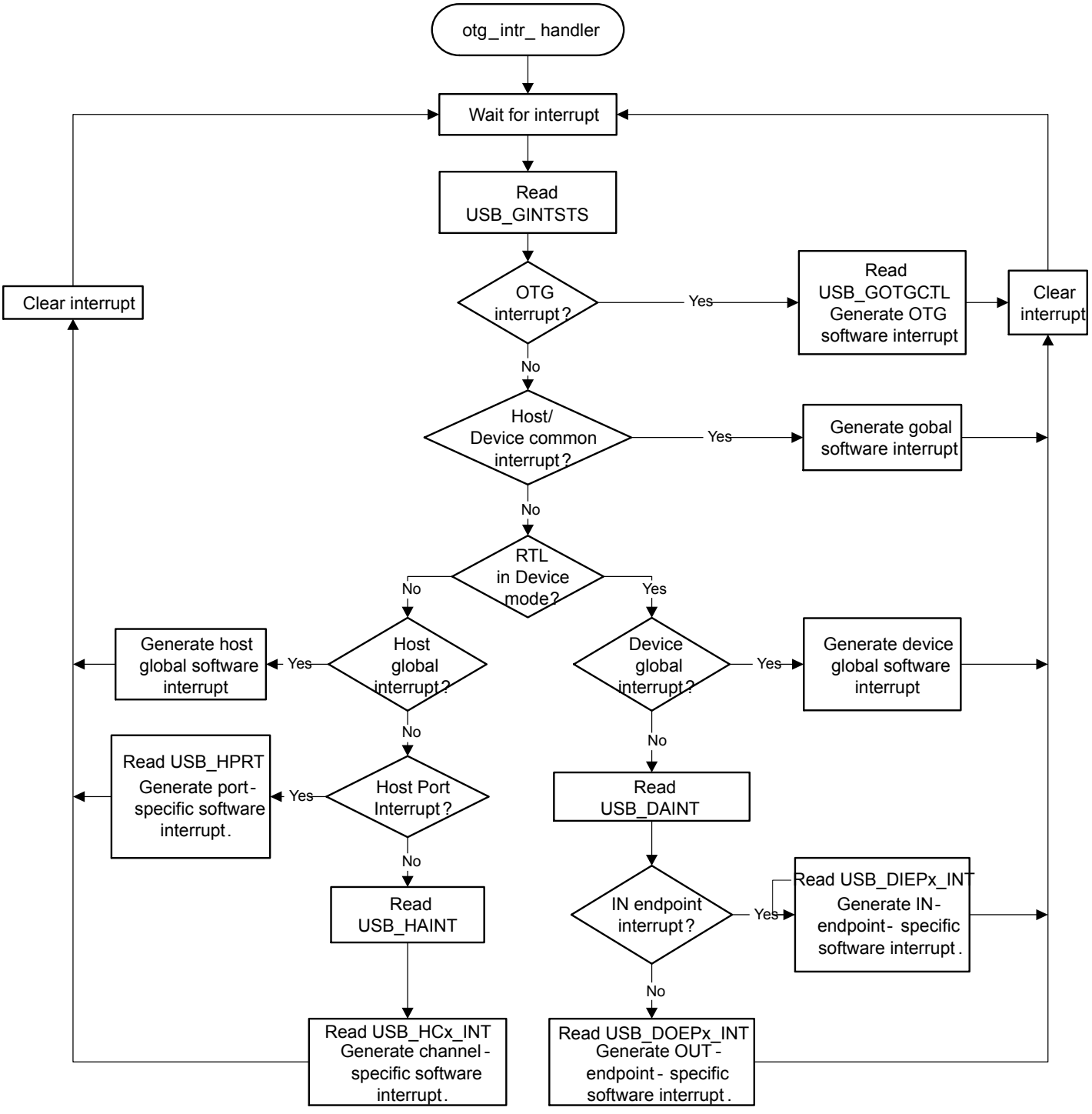


Figure 31.17. Core Interrupt Handler

31.4.4.2.1 Device Mode

In Device mode, before changing FIFO data RAM allocation, the application must determine the following.

- All IN and OUT endpoints are disabled
- NAK mode is enabled in the core on all IN endpoints
- Global OUT NAK mode is enabled in the core
- All FIFOs are empty

Once these conditions are met, the application can reallocate FIFO data RAM as explained in 31.4.4.1 Data FIFO RAM Allocation. When NAK mode is enabled in the core, the core responds with a NAK handshake on all tokens received on the USB, except for SET-UP packets.

After the reallocating the FIFO data RAM, the application must flush all FIFOs in the core using the USBAHB_GRSTCTL.TXFFLSH (TxFIFO Flush) and USBAHB_GRSTCTL.RXFFLSH (RxFIFO Flush) fields. Flushing is required to reset the pointers in the FIFOs for proper FIFO operation after reallocation. For more information on flushing FIFOs, see 31.4.4.2.2 Flushing TxFIFOs in the Core and 31.4.4.2.3 Flushing RxFIFOs in the Core.

31.4.4.2.2 Flushing TxFIFOs in the Core

The application can flush all TxFIFOs in the core using USBAHB_GRSTCTL.TXFFLSH as follows:

1. Check that USBAHB_GINTSTS.GINNAKEFF=0. If this bit is cleared then set USBAHB_DCTL.SGNPINNAK=1.
2. Wait for USBAHB_GINTSTS.GINNAKEFF=1, which indicates the NAK setting has taken effect to all IN endpoints.
3. Poll USBAHB_GRSTCTL.AHBIDLE until it is 1.

   AHBIdle = H indicates that the core is not writing anything to the FIFO.
4. Check that USBAHB_GRSTCTL.TXFFLSH =0. If it is 0, then write the TxFIFO number you want to flush to USBAHB_GRSTCTL.TXFNUM.
5. Set USBAHB_GRSTCTL.TXFFLSH=1and wait for it to clear.
6. Set the USBAHB_DCTL.GCNPINNAK bit.

31.4.4.2.3 Flushing RxFIFOs in the Core

The application can flush all RxFIFOs in the core using USBAHB_GRSTCTL.RXFFLSH as follows:

1. Check the status of the USBAHB_GINTSTS.GOUTNAKEFF bit. If it has been cleared, then set USBAHB_DCTL.SGOUTNAK=1. Else, clear USBAHB_GINTSTS.GOUTNAKEFF.

   NAK Effective interrupt = 1 indicates that the core is not writing to FIFO.
2. Wait for USBAHB_GINTSTS.GOUTNAKEFF=1, which indicates the NAK setting has taken effect to all OUT endpoints.
3. Poll the USBAHB_GRSTCTL.AHBIDLE until it is 1.

   AHBIDLE = 1 indicates that the core is not reading anything from the FIFO.
4. Set USBAHB_GRSTCTL.RXFFLSH=1 and wait for it to clear.
5. Set the USBAHB_DCTL.GCOUTNAK bit.

31.4.5 USB Suspend Mode

When the USB is suspended or the session is not valid, the PHY is driven into Suspend mode, stopping the PHY clock to reduce power consumption in the PHY and the core. To further reduce power consumption, the core also supports AHB clock gating and using EM2.

31.4.5.1 Using EM2 in USB Suspend Mode

When entering USB Suspend, the USB core clock must be changed to a low frequency 32 kHz clock source (LFRCO or LFXO) to allow detection of RESUME and SRP events, and then the system may enter EM2. Total power in this mode will be well under the USB 2.4 mA limit. This configuration supports a periodic wake up to EM1P with low duty cycle use of Radio RX/TX in order to maintain wireless network connectivity and avoid re-authentication to the network.

Device Mode Suspend With EM2

In Device mode, the device validates the host-driven Resume signal for a period of 1.5 µs (75 clock cycles at 48 MHz). With a 32 kHz clock, 2.34 ms is required (75 clock cycles at 32 kHz) to detect the resume. Hence, the application programs USBAHB_DCFG.RESVALID with a value of 4 clock cycles (125 µs). If the core is in Suspend mode, the device thus detects the resume and the host signals a resume for a minimum of 125 µs. If the device is being reset from suspend, it begins a high-speed detection handshake after detecting SE0 for no fewer than 2.5 µs. With a 48 MHz clock, detection occurs after 120 clock cycles (2.5 µs). With a 32 kHz clock, 120 clock cycles signifies 3.75 ms. Hence, a programmable value of 4 clock cycles (125 µs) is used to detect reset. The 32-KHz Suspend feature incorporates switching to the 32 kHz clock during suspend and resume/remote wakeup until the system comes up and starts driving 48 MHz.

Sequence of operations:

1. Detect Suspend state. Wait for an interrupt from the device core and check that USBAHB_GINTSTS.USBSUSP is set to 1.

```
// Stop core clocks
USBAHB->PCGCCTL |= USBAHB_PCGCCTL_GATEHCLK | USBAHB_PCGCCTL_STOPPCLK |
USBAHB_PCGCCTL_PWRCLMP;

//Switch to slow 32KHz LFRCO/LFXO
CMU->USB0CLKCTRL = CMU_USB0CLKCTRL_CLKSEL_LFRCO;
// Alternately: CMU->USB0CLKCTRL = CMU_USB0CLKCTRL_CLKSEL_LFXO;

//Put system in EM2
Enter_EM2();
```

Device Mode Resume (EM2 → EM0)

Sequence of operations:

1. Resume IRQ from USB wakes up core
2. Exit EM2
3. Perform all steps below:

```
    // Switch USB to USBPLL0 clock
    CMU->USB0CLKCTRL = CMU_USB0CLKCTRL_CLKSEL_USBPLL0;

    // wait till USBPLL is ready before accessing registers
    while(!(USBPLL0->STATUS & USBPLL_STATUS_PLLRDY));

    // USB core is already suspended
    // un-gate clocks
    USBAHB->PCGCCTL &= ~(_USBAHB_PCGCCTL_STOPPCLK_MASK
                       | _USBAHB_PCGCCTL_GATEHCLK_MASK |
                         _USBAHB_PCGCCTL_PWRCLMP_MASK);
```

Device Mode Remote Wakeup (EM2 → EM0)

Sequence if operations:

1. An interrupt wakes up the device from EM2.
2. Perform all steps below:

```
    // Switch USB to USBPLL0 clock
    CMU->USB0CLKCTRL = CMU_USB0CLKCTRL_CLKSEL_USBPLL0;

    // Wait until USBPLL is ready before accessing registers
    while(!(USBPLL0->STATUS & USBPLL_STATUS_PLLRDY));

    // USB core is already suspended
    // un-gate clocks
    USBAHB->PCGCCTL &= ~(_USBAHB_PCGCCTL_STOPPCLK_MASK
                       | _USBAHB_PCGCCTL_GATEHCLK_MASK |
                         _USBAHB_PCGCCTL_PWRCLMP_MASK);

    // Request remote wakeup
    USBAHB->DCTL |= USBAHB_DCTL_RMTWKUPSIG;

    // Wait for wake up IRQ
```

31.5 USB_APBS Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	USB_IPVERSION	R	IP Version
0x004	USB_EN	RW ENABLE	USB Module Enable
0x008	USB_CTRL	RW SYNC	System Ctrl Reg
0x00C	USB_IF	RWH INTFLAG	IRQ Flag Reg
0x018	USB_IEN	RW	IRQ Enable Reg
0x024	USB_CAL	RW	Cal Values - PHY
0x028	USB_STATUS	RH	STATUS Reg
0x1000	USB_IPVERSION_SET	R	IP Version
0x1004	USB_EN_SET	RW ENABLE	USB Module Enable
0x1008	USB_CTRL_SET	RW SYNC	System Ctrl Reg
0x100C	USB_IF_SET	RWH INTFLAG	IRQ Flag Reg
0x1018	USB_IEN_SET	RW	IRQ Enable Reg
0x1024	USB_CAL_SET	RW	Cal Values - PHY
0x1028	USB_STATUS_SET	RH	STATUS Reg
0x2000	USB_IPVERSION_CLR	R	IP Version
0x2004	USB_EN_CLR	RW ENABLE	USB Module Enable
0x2008	USB_CTRL_CLR	RW SYNC	System Ctrl Reg
0x200C	USB_IF_CLR	RWH INTFLAG	IRQ Flag Reg
0x2018	USB_IEN_CLR	RW	IRQ Enable Reg
0x2024	USB_CAL_CLR	RW	Cal Values - PHY
0x2028	USB_STATUS_CLR	RH	STATUS Reg
0x3000	USB_IPVERSION_TGL	R	IP Version
0x3004	USB_EN_TGL	RW ENABLE	USB Module Enable
0x3008	USB_CTRL_TGL	RW SYNC	System Ctrl Reg
0x300C	USB_IF_TGL	RWH INTFLAG	IRQ Flag Reg
0x3018	USB_IEN_TGL	RW	IRQ Enable Reg
0x3024	USB_CAL_TGL	RW	Cal Values - PHY
0x3028	USB_STATUS_TGL	RH	STATUS Reg

31.6 USB_APBS Register Description

31.6.1 USB_IPVERSION - IP Version

Offset	Bit Position																															
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x1
Access																																R
Name																																IPVERSION

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	IPVERSION	0x1	R	**IP Version ID**

31.6.2 USB_EN - USB Module Enable

Offset	Bit Position																															
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															R	W
Name																															DISABLING	EN

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DISABLING	0x0	R	**Disablement busy status**
	When EN is cleared(disablement), USB module operation is halted immediately and the USB core domain is initialized to ensure a clean start when re-enabled.			
0	EN	0x0	W	**Module enable**
	Set this bit to enable the USB module and allow the core clock to run. Clearing this bit will gate off the USB core clock and disable the USB module.			

31.6.3 USB_CTRL - System Ctrl Reg

Offset	Bit Position																														
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset						0x0	0x1	0x1	0x7					0x1	0x0	0x0																0x0
Access						RW	RW	RW	RW					RW	RW	RW																RW
Name						ENDATACAP	BYPSVREG	DISRUPTX	FSSLEW					VBUSOVRIDE	VBSSNSLEN	VBSSNSHEN																TXDSE0MXSEL

Bit	Name	Reset	Access	Description
31:27	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
26	ENDATACAP	0x0	RW	**adds 40pf cap to dm/dp in tx mode**
25	BYPSVREG	0x1	RW	**bypass_vreg signal to phy**
24	DISRUPTX	0x1	RW	**disable tx pull up res**
23:21	FSSLEW	0x7	RW	**FS Slew**
	Every binary step reduction increases slew by approximately 20% of the previous step			
20:19	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
18	VBUSOVRIDE	0x1	RW	**vbus over ride to GPPLL**
17	VBSSNSLEN	0x0	RW	**VBUSSENSE going low - enable**
	In self powered mode, set to enable wake-up on loss of VBUS while in EM2			
16	VBSSNSHEN	0x0	RW	**VBUSSENSE going high - enable**
	In self powered mode, set to enable wake-up on a VBUS plugin event while in EM2			
15:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	TXDSE0MXSEL	0x0	RW	**TXD SE0 chicken bit**

31.6.4 USB_IF - IRQ Flag Reg

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															RW	RW
Name																															DWCOTG	VBUS

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DWCOTG	0x0	RW	**DWC_OTG interrupt flag** This flag is set when the IRQ from the USB MAC fires. Once set, firmware should interrogate the USB MAC IRQ register to determine the interrupt cause, handle it, clear the MAC IRQ bit(s), and then finally clear this flag.
0	VBUS	0x0	RW	**VBUS_SENSE interrupt flag** This flag is set if VBUS either rises or falls. Once set, firmware should poll the VBUSVALID bit in the STATUS register to determine if it was a rising edge or falling edge.

31.6.5 USB_IEN - IRQ Enable Reg

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	0x0
Access																															RW	RW
Name																															DWCOTG	VBUS

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	DWCOTG	0x0	RW	**DWC_OTG interrupt enable**
0	VBUS	0x0	RW	**VBUS_SENSE interrupt enable**

31.6.6 USB_CAL - Cal Values - PHY

Offset	Bit Position																															
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset						0x7																										
Access						RW																										
Name						FSSLEWT																										

Bit	Name	Reset	Access	Description
31:27	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
26:24	FSSLEWT	0x7	RW	**FS slew**
23:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

31.6.7 USB_STATUS - STATUS Reg

Offset	Bit Position																															
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																R
Name																																VBUSVALID

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	VBUSVALID	0x0	R	**VBus valid**

31.7 USBAHB_AHBS Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	USBAHB_GOTGCTL	RWH	OTG_Ctrl_and_status_reg
0x008	USBAHB_GAHBCFG	RW	AHB Config Register
0x00C	USBAHB_GUSBCFG	RWH	USB Configuration Reg
0x010	USBAHB_GRSTCTL	RWH	Reset Register
0x014	USBAHB_GINTSTS	RWH SYNC	Interrupt Register
0x018	USBAHB_GINTMSK	RW	Interrupt Mask Register
0x01C	USBAHB_GRXSTSR	RH SYNC	Receive Status Debug Read Reg
0x020	USBAHB_GRXSTSP	RH SYNC	Receive Status Read /Pop Reg
0x024	USBAHB_GRXFSIZ	RW	Receive FIFO Size Register
0x028	USBAHB_GNPTXFSIZ	RW	Non-Per Transmit FIFO Size Reg
0x040	USBAHB_GSNPSID	R	Synopsys ID Register
0x044	USBAHB_GHWCFG1	RH SYNC	User HW Config1 Register
0x048	USBAHB_GHWCFG2	RH SYNC	User HW Config2 Register
0x04C	USBAHB_GHWCFG3	RH SYNC	User HW Config3 Register
0x050	USBAHB_GHWCFG4	R	User HW Config4 Register
0x05C	USBAHB_GDFIFOCFG	RW	Global DFIFO Configuration Reg
0x104	USBAHB_DIEPTXF1	RW	Device in EP Xmit FIFO Siz Reg 1
0x108	USBAHB_DIEPTXF2	RW	Device in EP Xmit FIFO Size Register 2
0x10C	USBAHB_DIEPTXF3	RW	Device in EP Xmit FIFO Size Register 2
0x110	USBAHB_DIEPTXF4	RW	Device in EP Xmit FIFO Size Register 2
0x114	USBAHB_DIEPTXF5	RW	Device in EP Xmit FIFO Size Register 2
0x118	USBAHB_DIEPTXF6	RW	Device in EP Xmit FIFO Size Register 2
0x11C	USBAHB_DIEPTXF7	RW	Device in EP Xmit FIFO Size Register 2
0x120	USBAHB_DIEPTXF8	RW	Device in EP Xmit FIFO Size Register 2
0x124	USBAHB_DIEPTXF9	RW	Device in EP Xmit FIFO Size Register 2
0x800	USBAHB_DCFG	RW	Device Configuration Register
0x804	USBAHB_DCTL	RWH	Device Control Register
0x808	USBAHB_DSTS	RH	Device Status Register
0x810	USBAHB_DIEPMSK	RW	Device in EP Common IRQ Mask Register
0x814	USBAHB_DOEPMSK	RW	New Register
0x818	USBAHB_DAINT	RH SYNC	Device All EP Interrupt Register
0x81C	USBAHB_DAINTMSK	RW	Device All EP Interrupt Mask Register
0x830	USBAHB_DTHRCTL	RW	Device Threshold Control Register
0x834	USBAHB_DIEPEMPMSK	RW	Device in EP FIFO Empty IRQ Mask Reg
0x900	USBAHB_DIEP0CTL	RWH	Device Control in EP 0 Ctrl Reg

Offset	Name	Type	Description
0x908	USBAHB_DIEP0INT	RW	Device in EP 0 IRQ Reg
0x910	USBAHB_DIEP0TSIZ	RW	Device in EP 0 Xfer Size Reg
0x914	USBAHB_DIEP0DMAADDR	RW	Device in EP 0 DMA Addr Reg
0x918	USBAHB_DIEP0TXFSTS	R	DEvice in EP TX FIFO Status Reg 0
0x920	USBAHB_DEVINEPx_CTL	RW	Device Control in EP 1 CTRL Reg
0x928	USBAHB_DEVINEPx_INT	RW	Device in EP 1 IRQ Register
0x930	USBAHB_DEVINEPx_TSIZ	RW	Device in EP 1 Xfer Size Reg
0x934	USBAHB_DEVI-NEPx_DMAADDR	RW	Device in EP 1 DMA Address Reg
0x938	USBAHB_DEVINEPx_DTXFSTS	R	Device in EP TX FIFO Stat Reg
0xB00	USBAHB_DOEP0CTL	RWH SYNC	Device Ctrl OUT EP 0 CTRL Reg
0xB08	USBAHB_DOEP0INT	RW	Device OUT EP 0 IRQ Register
0xB10	USBAHB_DOEP0TSIZ	RW	Device OUT EP 0 Xfer Size Reg
0xB14	USBAHB_DOEP0DMAADDR	RW	Device OUT EP 0 DMA Addr Reg
0xB20	USBAHB_DEVOUTEPx_CTL	RWH	Device CTRL OUT EP 1 CTRL Reg
0xB28	USBAHB_DEVOUTEPx_INT	RW	Device OUT EP 1 IRQ Register
0xB30	USBAHB_DEVOUTEPx_TSIZ	RWH	Device OUT EP 1 Xfer Size Reg
0xB34	USBAHB_DEVOU-TEPx_DMAADDR	RW	Device OUT EP 1 DMA Addr Reg
0xE00	USBAHB_PCGCCTL	RWH	PWR_CG_CTRL_reg
0x1000	USBAHB_FIFO0Dx	RW	Device EP0 FIFO
0x2000	USBAHB_FIFO1Dx	RW	FIFO1
0x3000	USBAHB_FIFO2Dx	RW	EP2 Data
0x4000	USBAHB_FIFO3Dx	RW	New Register
0x5000	USBAHB_FIFO4Dx	RW	New Register
0x6000	USBAHB_FIFO5Dx	RW	New Register
0x7000	USBAHB_FIFO6Dx	RW	New Register
0x8000	USBAHB_FIFO7Dx	RW	New Register
0x9000	USBAHB_FIFO8Dx	RW	New Register
0xA000	USBAHB_FIFO9Dx	RW	New Register
0x20000	USBAHB_FIFORAMx	RW	New Register

31.8 USBAHB_AHBS Register Description

31.8.1 USBAHB_GOTGCTL - OTG_Ctrl_and_status_reg

Offset	Bit Position																													
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset											0x0																				
Access											R																				
Name											CURMOD																				

Bit	Name	Reset	Access	Description
31:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21	CURMOD	0x0	R	**Current Mode of Operation**
20:0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

31.8.2 USBAHB_GAHBCFG - AHB Config Register

Offset	Bit Position																															
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset								0x0	0x0	0x0	0x0														0x0		0x0	0x0				0x0
Access								RW	RW	RW	RW														RW		RW	RW				RW
Name								INVDESCEND	AHBSINGLE	NOTIALLDMAWRIT	REMMEMSUPP														NPTXFEMPLVL		DMAEN	HBSTLEN				GLBLINTRMSK

Bit	Name	Reset	Access	Description
31:25	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
24	INVDESCEND	0x0	RW	**Inverse Descriptor Endianness**
23	AHBSINGLE	0x0	RW	**AHB Single Support** This bit when programmed supports Single transfers for the remaining data in a transfer when the DWC_otg core is operating in DMA mode. 1'b0: This is the default mode. When this bit is set to 1'b0, the remaining data in the transfer is sent using INCR burst size. 1'b1: When set to 1'b1, the remaining data in a transfer is sent using Single burst size. Note: if this feature is enabled, the AHB RETRY and SPLIT transfers still have INCR burst type. Enable this feature when the AHB Slave connected to the DWC_otg core does not support INCR burst (and when Split, and Retry transactions are not being used in the bus).
22	NOTIALLDMAWRIT	0x0	RW	**Notify All Dma Write Trans** This bit is programmed to enable the System DMA Done functionality for all the DMA write Transactions corresponding to the Channel/Endpoint. This bit is valid only when GAHBCFG.REMMEMSUPP is set to 1. GAHBCFG.NOTIALLDMAWRIT = 1 - HSOTG core asserts int_dma_req for all the DMA write transactions on the AHB interface along with int_dma_done, chep_last_transact and chep_number signal informations. The core waits for sys_dma_done signal for all the DMA write transactions in order to complete the transfer of a particular Channel/Endpoint. GAHBCFG.NOTIALLDMAWRIT = 0 - HSOTG core asserts int_dma_req signal only for the last transaction of DMA write transfer corresponding to a particular Channel/Endpoint. Similarly, the core waits for sys_dma_done signal only for that transaction of DMA write to complete the transfer of a particular Channel/Endpoint.
21	REMMEMSUPP	0x0	RW	**Remote Memory Support** This bit is programmed to enable the functionality to wait for the system DMA Done Signal for the DMA Write Transfers. When set, the int_dma_req output signal is asserted when HSOTG DMA starts write transfer to the external memory. When the core is done with the Transfers it asserts int_dma_done signal to flag the completion of DMA writes from HSOTG. The core then waits for sys_dma_done signal from the system to proceed further and complete the Data Transfer corresponding to a particular Channel/Endpoint. When cleared, the int_dma_req and int_dma_done signals are not asserted and the core proceeds with the assertion of the XferComp interrupt as soon as the DMA write transfer is done at the HSOTG Core Boundary and it doesn't wait for the sys_dma_done signal to complete the DATA."
20:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7	NPTXFEMPLVL	0x0	RW	**Non-Periodic TxFIFO Empty Level**

Bit	Name	Reset	Access	Description
	This bit is used only in Slave mode. This bit indicates when IN endpoint Transmit FIFO empty interrupt (USB_DIEP0INT/ USB_DIEPx_INT.TXFEMP) is triggered.", "modes" : { "HALFEMPTY" : [0, "<para>Host Mode: USB_GINTSTS.NPTXFEMP interrupt indicates that the Non-Periodic TxFIFO is half empty.</para> <para>Device Mode: USB_DIEP0INT/USB_DIEPx_INT.TXFEMP interrupt indicates that the IN Endpoint TxFIFO is half empty.</para>"], "EMPTY" : [1, "<para>Host Mode: USB_GINTSTS.NPTXFEMP interrupt indicates that the Non-Periodic TxFIFO is completely empty.</para> <para>Device Mode: USB_DIEP0INT/USB_DIEPx_INT.TXFEMP interrupt indicates that the IN Endpoint TxFIFO is completely empty.</para>"]			
6	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
5	DMAEN	0x0	RW	**DMA Enable**
	1'b0: Core operates in Slave mode 1'b1: Core operates in a DMA mode This bit is always 0 when Slave-Only mode has been selected			
4:1	HBSTLEN	0x0	RW	**Burst Length/Type**
	"SINGLE" : [0, "Single transfer."], "INCR" : [1, "Incrementing burst of unspecified length."], "INCR4" : [3, "4-beat incrementing burst."], "INCR8" : [5, "8-beat incrementing burst."], "INCR16" : [7, "16-beat incrementing burst."],			
0	GLBLINTRMSK	0x0	RW	**Global Interrupt Mask**
	The application uses this bit to mask or unmask the interrupt line assertion to itself. Irrespective of this bit's setting, the interrupt status registers are updated by the core. 1'b0: Mask the interrupt assertion to the application. 1'b1: Unmask the interrupt assertion to the application			

31.8.3 USBAHB_GUSBCFG - USB Configuration Reg

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0			0x0		0x0				0x0									0x5							0x1	0x0		0x0			0x0	
Access	W			RW		R				RW									RW							RW	RW		RW			RW	
Name	CORRUPTTXPKT			TXENDDELAY		ICUSBCAP				TERMSELDLPULSE									USBTRDTIM							PHYSEL	FSINTF		PHYIF			TOUTCAL	

Bit	Name	Reset	Access	Description
31	CORRUPTTXPKT	0x0	W	**corrupt tx packet**
	For debug purposes only. Application should always drive this to 0.			
30:29	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
28	TXENDDELAY	0x0	RW	**Tx End Delay**
	Writing 1'b1 to this bit enables the core to follow the TxEndDelay timings as per UTMI+ specification 1.05 section 4.1.5 for opmode signal during remote wakeup. 1'b0 : Normal Mode. 1'b1 : Tx End delay			
27	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
26	ICUSBCAP	0x0	R	**IC_USB-Capable**
	The application uses this bit to control the DWC_otg core's IC_USB			
25:23	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
22	TERMSELDLPULSE	0x0	RW	**TermSel DLine Pulsing Selection**
	This bit selects utmi_termselect to drive data line pulse during SRP.", "modes" : { "TXVALID" : [0, "Data line pulsing using utmi_txvalid."], "TERMSEL" : [1, "Data line pulsing using utmi_termsel."] }			
21:14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13:10	USBTRDTIM	0x5	RW	**USB turnaround time**
	Sets the turnaround time in PHY clocks. Specifies the response time For a MAC request to the Packet FIFO Controller (PFC) to fetch data from the DFIFO (SPRAM). This must be programmed to 4'h5: When the MAC interface is 16-bit UTMI+ . 4'h9: When the MAC interface is 8-bit UTMI+ . Note: The values above are calculated For the minimum AHB frequency of 30 MHz. USB turnaround time is critical For certification where long cables and 5-Hubs are used, so If you need the AHB to run at less than 30 MHz, and If USB turnaround time is not critical, these bits can be programmed to a larger value.			
9:7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6	PHYSEL	0x1	RW	**"2.0 HS sel or 1.1 FS sel**

Bit	Name	Reset	Access	Description
	The application uses this bit to select either a high-speed UTMI+ or ULPI PHY, or a full-speed transceiver. 1'b0: USB 2.0 high-speed UTMI+ or ULPI PHY 1'b1: USB 1.1 full-speed serial transceiver If a USB 1.1 Full-Speed Serial Transceiver interface was not selected in, this bit is always 0, with Write Only access. If a high-speed PHY interface was not selected in, this bit is always 1, with Write Only access. If both interface types were selected (parameters have non-zero values), the application uses this bit to select which interface is active, and access is Read and Write			
5	FSINTF	0x0	RW	**Full-Speed Serial Interface Sel**
	The application uses this bit to select either a unidirectional or bidirectional USB 1.1 full-speed serial transceiver interface. 1'b0: 6-pin unidirectional full-speed serial interface 1'b1: 3-pin bidirectional full-speed serial interface If a USB 1.1 Full-Speed Serial Transceiver interface was not selected, this bit is always 0, with Write Only access. If a USB 1.1 FS interface was selected, Then the application can Set this bit to select between the 3- and 6-pin interfaces, and access is Read and Write.			
4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	PHYIF	0x0	RW	**PHY Interface**
2:0	TOUTCAL	0x0	RW	**HS/FS Timeout cal**
	The number of PHY clocks that the application programs in this field is added to the high-speed/full-speed interpacket timeout duration in the core to account For any additional delays introduced by the PHY. This can be required, because the delay introduced by the PHY in generating the linestate condition can vary from one PHY to another. The USB standard timeout value For high-speed operation is 736 to 816 (inclusive) bit times. The USB standard timeout value For full-speed operation is 16 to 18 (inclusive) bit times. The application must program this field based on the speed of enumeration. The number of bit times added per PHY clock are: High-speed operation: One 30-MHz PHY clock = 16 bit times One 60-MHz PHY clock = 8 bit times Full-speed operation: One 30-MHz PHY clock = 0.4 bit times One 60-MHz PHY clock = 0.2 bit times One 48-MHz PHY clock = 0.25 bit times			

31.8.4 USBAHB_GRSTCTL - Reset Register

Offset	Bit Position																														
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0																						0x0			0x0	0x0			0x0	0x0
Access	R	R																						RW			RW	RW			RW	RW
Name	AHBIDLE	DMAREQ																						TXFNUM			TXFFLSH	RXFFLSH			PIUFSSFTRST	CSFTRST

Bit	Name	Reset	Access	Description
31	AHBIDLE	0x0	R	**AHB Master Idle**
	Indicates that the AHB Master State Machine is in the IDLE condition			
30	DMAREQ	0x0	R	**DMA Request Signal**
	Indicates that the DMA request is in progress. Used For debug			
29:11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10:6	TXFNUM	0x0	RW	**TxFIFO Number**
	This is the FIFO number that must be flushed using the TxFI FO Flush bit.; "F0" : [0, "<para>Host mode: Non-periodic TxFIFO flush.</p ara> <para>Device: Tx FIFO 0 flush</para>"], "F1" : [1, "<para>Host mode: Periodic TxFIFO flush.</ para> <para>Device: TXFIFO 1 flush.</para>"], "F2" : [2, "Device mode: TXFIFO 2 flush."], "F3" : [3, "Device mode: TXFIFO 3 flush."], "F4" : [4, "Device mode: TXFIFO 4 flush."], "F5" : [5, "Device mode: TXFIFO 5 flush."], "F6" : [6, "Device mode: TXFIFO 6 flush."], "FALL" : [16, "Flush all the transmit FIFOs in device or host mode."] This field must not be changed until the core clears the Tx FIFO Flush bit.			
5	TXFFLSH	0x0	RW	**TxFIFO Flush**
	This bit selectively flushes a single or all transmit FIFOs, but cannot do so If the core is in the midst of a transaction. The application must write this bit only after checking that the core is neither writing to the TxFIFO nor reading from the TxFIFO. Verify using these registers: ReadNAK Effective Interrupt ensures the core is not reading from the FIFO WriteGRSTCTL.AHBIDLE ensures the core is not writing anything to the FIFO. Flushing is normally recommended when FIFOs are reconfigured or when switching between Shared FIFO and Dedicated Transmit FIFO operation. FIFO flushing is also recommended during device endpoint disable. The application must wait until the core clears this bit before performing any operations. This bit takes eight clocks to clear, using the slower clock of phy_clk or hclk.			
4	RXFFLSH	0x0	RW	**RxFIFO Flush**
	The application can flush the entire RxFIFO using this bit, but must first ensure that the core is not in the middle of a transaction. The application must only write to this bit after checking that the core is neither reading from the RxFIFO nor writing to the RxFIFO. The application must wait until the bit is cleared before performing any other operations. This bit requires 8 clocks (slowest of PHY or AHB clock) to clear.			
3:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	PIUFSSFTRST	0x0	RW	**PIU FS Dedicated Controller Sft rst**
	Resets the PIU FS Dedicated Controller All module state machines in FS Dedicated Controller of PIU are reset to the IDLE state. Used to reset the FS Dedicated controller in PIU in case of any PHY Errors like Loss of activity or Babble Error resulting in the PHY remaining in RX state for more than one frame boundary			
0	CSFTRST	0x0	RW	**Core Soft Reset**

Bit	Name	Reset	Access	Description
				Resets the hclk and phy_clock domains as follows: Clears the interrupts and all the CSR registers except the following register bits: - PCGCCTL.RSTPDWNMODULE - PCGCCTL.GATEHCLK - PCGCCTL.PWRCLMP - PCGCCTL.StopPPhyLPwrClkSelclk - GUSBCFG.PhyLPwrClkSel - GUSBCFG.DDRSel - GUSBCFG.PHYSEL - GUSBCFG.FSINTF - GUSBCFG.ULPI_UTMI_Sel - GUSBCFG.PHYIF - GUSBCFG.TXENDDELAY - GUSBCFG.TERMSELDLPULSE - GUSBCFG.ULPIClkSusM - GUSBCFG.ULPIAutoRes - GUSBCFG.ULPIFsLs - GGPIO - GPWRDN - GADPCTL - HCFG.FSLSPCLKSEL - DCFG.DEVSPD - DCTL.SFTDISCON - All module state machines All module state machines (except the AHB Slave Unit) are reset to the IDLE state, and all the transmit FIFOs and the receive FIFO are flushed. Any transactions on the AHB Master are terminated as soon as possible, after gracefully completing the last data phase of an AHB transfer. Any transactions on the USB are terminated immediately. When Hibernation or ADP feature is enabled, the PMU module is not reset by the Core Soft Reset. The application can write to this bit any time it wants to reset the core. This is a self-clearing bit and the core clears this bit after all the necessary logic is reset in the core, which can take several clocks, depending on the current state of the core. Once this bit is cleared software must wait at least 3 PHY clocks before doing any access to the PHY domain (synchronization delay). Software must also must check that bit 31 of this register is 1 (AHB Master is IDLE) before starting any operation. Typically software reset is used during software development and also when you dynamically change the PHY selection bits in the USB configuration registers listed above. When you change the PHY, the corresponding clock For the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain has to be reset for proper operation.

31.8.5 USBAHB_GINTSTS - Interrupt Register

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0			0x1					0x0	0x0	0x0	0x0	0x0	0x0	0x0		0x0	0x0	0x0	0x0	0x0	0x0			0x0	0x0	0x1	0x0	0x0		0x0	0x0
Access	RW			RW					RW	RW	R	R	R	R	RW		RW	RW	RW	RW	RW	RW			R	R	R	R	RW		RW	R
Name	WKUPINT			CONIDSTSCHNG					RESETDET	FETSUSP	INCOMPLP	INCOMPISOIN	OEPINT	IEPINT	EPMIS		EOPF	ISOOUTDROP	ENUMDONE	USBRST	USBSUSP	ERLYSUSP			GOUTNAKEFF	GINNAKEFF	NPTxFEmp	RXFLVL	SOF		MODEMIS	CURMOD

Bit	Name	Reset	Access	Description
31	WKUPINT	0x0	RW	**Resume/Remote Wakeup Detected Irq**
	Wakeup Interrupt during Suspend(L2) or LPM(L1) state. During Suspend(L2): - Device Mode - This interrupt is asserted only when Host Initiated Resume is detected on USB. - Host Mode - This interrupt is asserted only when Device Initiated Remote Wakeup is detected on USB. For more information, see 'Partial Power-Down and Clock Gating Programming Model'. During LPM(L1):- - Device Mode - This interrupt is asserted for either Host Initiated Resume or Device Initiated Remote Wakeup on USB. - Host Mode - This interrupt is asserted for either Host Initiated Resume or Device Initiated Remote Wakeup on USB. For more information, see 'LPM Entry and Exit Programming Model'			
30:29	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
28	CONIDSTSCHNG	0x1	RW	**Connector ID Status Change**
	The core sets this bit when there is a change in connector ID status.			
27:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23	RESETDET	0x0	RW	**Reset detected Interrupt**
	In Device mode, this interrupt is asserted when a reset is detected on the USB in partial power-down mode when the device is in Suspend. In Host mode, this interrupt is not asserted.			
22	FETSUSP	0x0	RW	**Data Fetch Suspended**
	This interrupt is valid only in DMA mode. This interrupt indicates that the core has stopped fetching data For IN endpoints due to the unavailability of TxFIFO space or Request Queue space. This interrupt is used by the application For an endpoint mismatch algorithm. For example, after detecting an endpoint mismatch, the application: Sets a Global non-periodic IN NAK handshake Disables In endpoints Flushes the FIFO Determines the token sequence from the IN Token Sequence Learning Queue Re-enables the endpoints Clears the Global non-periodic IN NAK handshake If the Global non-periodic IN NAK is cleared, the core has not yet fetched data For the IN endpoint, and the IN token is received: the core generates an 'IN token received when FIFO empty' interrupt. The OTG Then sends the host a NAK response. To avoid this scenario, the application can check the GINTSTS.FETSUSP interrupt, which ensures that the FIFO is full before clearing a Global NAK handshake. Alternatively, the application can mask the (unicode)IN token received when FIFO empty(unicode) interrupt when clearing a Global IN NAK handshake.			
21	INCOMPLP	0x0	R	**Incomplete Periodic Transfer**
	In Host mode, the core sets this interrupt bit when there are incomplete periodic transactions still pending which are scheduled For the current microframe. Incomplete Isochronous OUT Transfer (incompISOOUT) The Device mode, the core sets this interrupt to indicate that there is at least one isochronous OUT endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register.			
20	INCOMPISOIN	0x0	R	**Incomplete Isochronous IN Transfer**

Bit	Name	Reset	Access	Description
	The core sets this interrupt to indicate that there is at least one isochronous IN endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register. Note: This interrupt is not asserted in Scatter/Gather DMA mode.			
19	OEPINT	0x0	R	**OUT Endpoints Interrupt**
	The core sets this bit to indicate that an interrupt is pending on one of the OUT endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the OUT endpoint on which the interrupt occurred, and Then read the corresponding Device OUT Endpoint-n Interrupt (DOEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DOEPINTn register to clear this bit			
18	IEPINT	0x0	R	**IN Endpoints Interrupt**
	The core sets this bit to indicate that an interrupt is pending on one of the IN endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the IN endpoint on Device IN Endpoint-n Interrupt (DIEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DIEPINTn register to clear this bit.			
17	EPMIS	0x0	RW	**Endpoint Mismatch Interrupt**
	Note: This interrupt is valid only in shared FIFO operation. Indicates that an IN token has been received For a non-periodic endpoint, but the data For another endpoint is present in the top of the Non-periodic Transmit FIFO and the IN endpoint mismatch count programmed by the application has expired.			
16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15	EOPF	0x0	RW	**End of Periodic Frame Interrupt**
	Indicates that the period specified in the Periodic Frame Interval field of the Device Configuration register (DCFG.PERFRINT) has been reached in the current microframe.			
14	ISOOUTDROP	0x0	RW	**Iso OUT Packet Dropped IRQ**
	he core sets this bit when it fails to write an isochronous OUT packet into the RxFIFO because the RxFIFO does not have enough space to accommodate a maximum packet size packet for the isochronous OUT endpoint.			
13	ENUMDONE	0x0	RW	**Enumeration Done**
	The core sets this bit to indicate that speed enumeration is complete. The application must read the Device Status (DSTS) register to obtain the enumerated speed.			
12	USBRST	0x0	RW	**USB Reset**
	The core sets this bit to indicate that a reset is detected on the USB.			
11	USBSUSP	0x0	RW	**USB Suspend**
	The core sets this bit to indicate that a suspend was detected on the USB. The core enters the Suspended state when there is no activity on the linestate signal For an extended period of time.			
10	ERLYSUSP	0x0	RW	**Early Suspend**
	The core sets this bit to indicate that an Idle state has been detected on the USB For 3 ms.			
9:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7	GOUTNAKEFF	0x0	R	**Global OUT NAK Effective**
	Indicates that the Set Global OUT NAK bit in the Device Control register (DCTL.SGOUTNAK), Set by the application, has taken effect in the core. This bit can be cleared by writing the Clear Global OUT NAK bit in the Device Control register (DCTL.CGOUTNAK).			
6	GINNAKEFF	0x0	R	**Global IN Non-periodic NAK Effective**

Bit	Name	Reset	Access	Description
	Indicates that the Set Global Non-periodic IN NAK bit in the Device Control register (DCTL.SGNPINNAK), Set by the application, has taken effect in the core. That is, the core has sampled the Global IN NAK bit Set by the application. This bit can be cleared by clearing the Clear Global Non-periodic IN NAK bit in the Device Control register (DCTL.CGNPINNAK). This interrupt does not necessarily mean that a NAK handshake is sent out on the USB. The STALL bit takes precedence over the NAK bit.			
5	NPTxFEmp	0x1	R	**Non periodic TXFIFO Empty**
4	RXFLVL	0x0	R	**RxFIFO Non-Empty** Indicates that there is at least one packet pending to be read from the RxFIFO.
3	SOF	0x0	RW	**tart of (micro)Frame**
2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	MODEMIS	0x0	RW	**Mode Mismatch Interrupt** The core sets this bit when the application is trying to access: A Host mode register, when the core is operating in Device mode A Device mode register, when the core is operating in Host mode The register access is completed on the AHB with an OKAY response, but is ignored by the core internally and does not affect the operation of the core.This bit can be set only by the core and the application should write 1 to clear it
0	CURMOD	0x0	R	**Current Mode of Operation** "DEVICE" : [0, "Device mode."], "HOST" : [1, "Host mode."],

31.8.6 USBAHB_GINTMSK - Interrupt Mask Register

Offset	Bit Position																													
0x018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0			0x0					0x0	0x0	0x0	0x0	0x0	0x0	0x0		0x0	0x0	0x0	0x0	0x0	0x0			0x0	0x0	0x0	0x0	0x0		0x0	
Access	RW			RW					RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW		RW	
Name	WKUPINTMSK			CONIDSTSCHNGMSK					RESETDETMSK	FETSUSPMSK	INCOMPLISOOUTMSK	INCOMPISOINMSK	OEPINTMSK	IEPINTMSK	EPMISMSK		EOPFMSK	ISOOUTDROPMSK	ENUMDONEMSK	USBRSTMSK	USBSUSPMSK	ERLYSUSPMSK			GOUTNAKEFFMSK	GINNAKEFFMSK	NPTXFEMPMSK	RXFLVLMSK	SOFMSK		MODEMISMSK	

Bit	Name	Reset	Access	Description
31	WKUPINTMSK	0x0	RW	**Resume/Remote WkUp Det Irq Mask** The WakeUp bit is used for LPM state wake up in a way similar to that of wake up in suspend state.
30:29	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
28	CONIDSTSCHNGMSK	0x0	RW	**Connector ID Status Change Mask**
27:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23	RESETDETMSK	0x0	RW	**Reset detected Interrupt Mask**
22	FETSUSPMSK	0x0	RW	**Data Fetch Suspended Mask**
21	INCOMPLISOOUTMSK	0x0	RW	**Incomp Iso OUT Transfer Mask**
20	INCOMPISOINMSK	0x0	RW	**Incomp Iso IN Transfer Mask**
19	OEPINTMSK	0x0	RW	**OUT Endpoints Interrupt Mask**
18	IEPINTMSK	0x0	RW	**IN Endpoints Interrupt Mask**
17	EPMISMSK	0x0	RW	**Endpoint Mismatch Interrupt Mask**
16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15	EOPFMSK	0x0	RW	**End of Periodic Frame Irq Mask**
14	ISOOUTDROPMSK	0x0	RW	**Iso OUT Pkt Dropped IRQ Mask**

Bit	Name	Reset	Access	Description
13	ENUMDONEMSK	0x0	RW	**Enumeration Done Mask**
12	USBRSTMSK	0x0	RW	**USB Reset Mask**
11	USBSUSPMSK	0x0	RW	**USB Suspend Mask**
10	ERLYSUSPMSK	0x0	RW	**Early Suspend Mask**
9:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7	GOUTNAKEFFMSK	0x0	RW	**Global OUT NAK Effective Mask**
6	GINNAKEFFMSK	0x0	RW	**Global Non-per IN NAK Eff Mask**
5	NPTXFEMPMSK	0x0	RW	**NP TXFIFO Empty Msk**
4	RXFLVLMSK	0x0	RW	**Receive FIFO Non-Empty Mask**
3	SOFMSK	0x0	RW	**Start of (micro)Frame Mask**
2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1	MODEMISMSK	0x0	RW	**Mode Mismatch Interrupt Mask**
0	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

31.8.7 USBAHB_GRXSTSR - Receive Status Debug Read Reg

Offset	Bit Position																														
0x01C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset								0x0				0x0				0x0		0x0											0x0			
Access								R				R				R		R											R			
Name								FN				PKTSTS				DPID		BCNT											EPNUM			

Bit	Name	Reset	Access	Description
31:25	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
24:21	FN	0x0	R	**Frame Number** This is the least significant 4 bits of the (micro)Frame number in which the packet is received on the USB. This field is supported only when isochronous OUT endpoints are supported.
20:17	PKTSTS	0x0	R	**Packet Status** Indicates the status of the received packet.; "GOUTNAK" : [1, "Device mode: Global OUT NAK (triggers an interrupt)."], "PKTRCV" : [2, "<para>Host mode: IN data packet received.</para> <para>Device mode: OUT data packet received.</para>"], "XFERCOMPL" : [3, "<para>Host mode: IN transfer completed (triggers an interrupt).</para> <para>Device mode: OUT transfer completed (triggers an interrupt).</para>"], "SETUPCOMPL" : [4, "Device mode: SETUP transaction completed (triggers an interrupt)."], "TGLERR" : [5, "Host mode: Data toggle error (triggers an interrupt)."], "SETUPRCV" : [6, "Device mode: SETUP data packet received."], "CHLT" : [7, "Host mode: Channel halted (triggers an interrupt)."],
16:15	DPID	0x0	R	**Data PID** Indicates the Data PID of the received OUT data packet; "DATA0" : [0, "DATA0 PID."],"DATA1" : [1, "DATA1 PID."], "DATA2" : [2, "DATA2 PID."], "MDATA" : [3, "MDATA PID."],
14:4	BCNT	0x0	R	**Byte Count** Indicates the byte count of the received IN data packet.
3:0	EPNUM	0x0	R	**End Point Num** Indicates the channel number to which the current received packet belongs. Mode: Device only Endpoint Number (EPNum) Indicates the endpoint number to which the current received packet belongs.

31.8.8 USBAHB_GRXSTSP - Receive Status Read /Pop Reg

Offset	Bit Position																															
0x020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset								0x0				0x0				0x0		0x0											0x0			
Access								R				R				R		R											R			
Name								FN				PKTSTS				DPID		BCNT											EPNUM			

Bit	Name	Reset	Access	Description
31:25	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
24:21	FN	0x0	R	**Frame Number**
	This is the least significant 4 bits of the (micro)Frame number in which the packet is received on the USB. This field is supported only when isochronous OUT endpoints are supported.			
20:17	PKTSTS	0x0	R	**Packet Status**
	Indicates the status of the received packet.; "GOUTNAK" : [1, "Device mode: Global OUT NAK (triggers an interrupt)."], "PKTRCV" : [2, "<para>Host mode: IN data packet received.</para> <para>Device mode: OUT data packet received.</para>"], "XFERCOMPL" : [3, "<para>Host mode: IN transfer completed (triggers an interrupt).</para> <para>Device mode: OUT transfer completed (triggers an interrupt).</para>"], "SETUPCOMPL" : [4, "Device mode: SETUP transaction completed (triggers an interrupt)."], "TGLERR" : [5, "Host mode: Data toggle error (triggers an interrupt)."], "SETUPRCV" : [6, "Device mode: SETUP data packet received."], "CHLT" : [7, "Host mode: Channel halted (triggers an interrupt)."],			
16:15	DPID	0x0	R	**Data PID**
	Indicates the Data PID of the received OUT data packet; "DATA0" : [0, "DATA0 PID."], "DATA1" : [1, "DATA1 PID."], "DATA2" : [2, "DATA2 PID."], "MDATA" : [3, "MDATA PID."]			
14:4	BCNT	0x0	R	**Byte Count**
	Indicates the byte count of the received data packet.			
3:0	EPNUM	0x0	R	**Endpoint Number**
	Indicates the channel number to which the current received packet belongs. Mode: Device only Endpoint Number (EPNum) Indicates the endpoint number to which the current received packet belongs.			

31.8.9 USBAHB_GRXFSIZ - Receive FIFO Size Register

Offset	Bit Position																															
0x024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0x300										
Access																							RW										
Name																							RXFDEP										

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9:0	RXFDEP	0x300	RW	**RxFIFO Depth** This value is in terms of 32-bit words. Minimum value is 16. Maximum value is 384.

31.8.10 USBAHB_GNPTXFSIZ - Non-Per Transmit FIFO Size Reg

Offset	Bit Position																															
0x028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset											0x300																0x300					
Access											RW																RW					
Name											NPTXFINEPTXF0DEP																NPTXFSTADDR					

Bit	Name	Reset	Access	Description
31:27	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
26:16	NPTXFINEPTXF0DEP	0x300	RW	**IN Endpoint TxFIFO 0 Depth**
15:11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10:0	NPTXFSTADDR	0x300	RW	**IN EP FIFO0 xmit RAM Start Addr**

31.8.11 USBAHB_GSNPSID - Synopsys ID Register

Offset	Bit Position																													
0x040	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x4F54330A																															
Access	R																															
Name	SYNOPSYSID																															

Bit	Name	Reset	Access	Description
31:0	SYNOPSYSID	0x4F54330A	R	**SNPS ID**

31.8.12 USBAHB_GHWCFG1 - User HW Config1 Register

Offset	Bit Position																													
0x044	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	R																															
Name	EPDIR																															

Bit	Name	Reset	Access	Description
31:0	EPDIR	0x0	R	**User HW Config1 Register**

31.8.13 USBAHB_GHWCFG2 - User HW Config2 Register

Offset	Bit Position																															
0x048	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset		0x0					0x0		0x0			0x0	0x0	0x0	0x3				0x0				0x0		0x0		0x0	0x2		0x4		
Access		R					R		R			R	R	R	R				R				R		R		R	R		R		
Name		TKNQDEPTH					PTXQDEPTH		NPTXQDEPTH			MULTIPROCINTRPT	DYNFIFOSIZING	PERIOSUPPORT	NUMHSTCHNL				NUMDEVEPS				FSPHYTYPE		HSPHYTYPE		SINGPNT	OTGARCH		OTGMODE		

Bit	Name	Reset	Access	Description
31	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
30:26	TKNQDEPTH	0x0	R	**Device Mode IN Token Seq Queue Depth**
25:24	PTXQDEPTH	0x0	R	**Host Mode Periodic Req Queue Dept**
23:22	NPTXQDEPTH	0x0	R	**Non-periodic Request Queue Depth**
21	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
20	MULTIPROCINTRPT	0x0	R	**Multi Processor Interrupt Enabled**
19	DYNFIFOSIZING	0x0	R	**Dynamic FIFO Sizing Enabled**
18	PERIOSUPPORT	0x0	R	**Per OUT Chan Supported in Host Mode**
17:14	NUMHSTCHNL	0x3	R	**Number of Host Channels** Indicates the number of host channels supported by the core in Host mode. The range of this field is 0-15: 0 specifies 1 channel, 15 specifies 16 channels.
13:10	NUMDEVEPS	0x0	R	**Number of Device Endpoints** Indicates the number of device endpoints supported by the core in Device mode in addition to control endpoint 0. The range of this field is 1-15.
9:8	FSPHYTYPE	0x0	R	**Full-Speed PHY Interface Type**
7:6	HSPHYTYPE	0x0	R	**New BitField** 2'b00: High-Speed interface not supported 2'b01: UTMI+ 2'b10: ULPI 2'b11: UTMI+ and ULPI
5	SINGPNT	0x0	R	**Point-to-Point** 1'b0: Multi-point application (hub and split support) 1'b1: Single-point application (no hub and split support)

Bit	Name	Reset	Access	Description
4:3	OTGARCH	0x2	R	**Architecture**
2:0	OTGMODE	0x4	R	**New BitField**

31.8.14 USBAHB_GHWCFG3 - User HW Config3 Register

Offset	Bit Position																															
0x04C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x2EC																0x0	0x0	0x0	0x0	0x0	0x1	0x0	0x0	0x0	0x6			0x8			
Access	R																R	R	R	R	R	R	R	R	R	R			R			
Name	DFIFODEPTH																LPMMODE	BCSUPPORT	HSICMODE	ADPSUPPORT	RSTTYPE	OPTFEATURE	VNDCTLSUPT	I2CINTSEL	OTGEN	PKTSIZEWIDTH			XFERSIZEWIDTH			

Bit	Name	Reset	Access	Description
31:16	DFIFODEPTH	0x2EC	R	**FIFO depth**
	This value is in terms of 32-bit words. Minimum value is 32 Maximum value is 32,768			
15	LPMMODE	0x0	R	**New BitField**
14	BCSUPPORT	0x0	R	**New BitField**
13	HSICMODE	0x0	R	**New BitField**
12	ADPSUPPORT	0x0	R	**New BitField**
11	RSTTYPE	0x0	R	**Reset Style For Clocked always**
10	OPTFEATURE	0x1	R	**Optional Features Removed**
9	VNDCTLSUPT	0x0	R	**Vendor Control Interface Support**
8	I2CINTSEL	0x0	R	**I2C Selection**
7	OTGEN	0x0	R	**OTG Function Enabled**
	The application uses this bit to indicate the DWC_otg core's OTG capabilities. 1'b0: Not OTG capable 1'b1: OTG Capable			
6:4	PKTSIZEWIDTH	0x6	R	**Width of Packet Size Counters**
	"3'b000: 4 bits 3'b001: 5 bits 3'b010: 6 bits 3'b011: 7 bits 3'b100: 8 bits 3'b101: 9 bits 3'b110: 10 bits Others: Reserve			
3:0	XFERSIZEWIDTH	0x8	R	**Width of Transfer Size Counters**
	4'b0000: 11 bits 4'b0001: 12 bits ... 4'b1000: 19 bits Others: Reserved			

31.8.15 USBAHB_GHWCFG4 - User HW Config4 Register

Offset	Bit Position																													
0x050	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0	0x9				0x1	0x0	0x0	0x0	0x0	0x0	0x0				0x2								0x0	0x0	0x1	0x1	0x0			
Access	R	R	R				R	R	R	R	R	R	R				R								R	R	R	R	R			
Name	DESCDMA	DESCDMAENABLED	INEPS				DEDFIFOMODE	SESSENDFLTR	BVALIDFLTR	AVALIDFLTR	VBUSVALIDFLTR	IDDGFLTR	NUMCTLEPS				PHYDATAWIDTH								EXTENDEDHIBERNATION	HIBERNATION	AHBFREQ	PARTIALPWRDN	NUMDEVPERIOEPS			

Bit	Name	Reset	Access	Description
31	DESCDMA	0x0	R	**New BitField**
30	DESCDMAENABLED	0x0	R	**New BitField**
29:26	INEPS	0x9	R	**Num Device Mode IN EPs inc Ctrl EPs**
25	DEDFIFOMODE	0x1	R	**Dedicated xmit FIFO For device IN EPs** 1'b0 : Dedicated Transmit FIFO Operation not enabled. 1'b1 : Dedicated Transmit FIFO Operation enabled.
24	SESSENDFLTR	0x0	R	**New BitField**
23	BVALIDFLTR	0x0	R	**New BitField**
22	AVALIDFLTR	0x0	R	**New BitField**
21	VBUSVALIDFLTR	0x0	R	**New BitField**
20	IDDGFLTR	0x0	R	**New BitField**
19:16	NUMCTLEPS	0x0	R	**New BitField**
15:14	PHYDATAWIDTH	0x2	R	**New BitField**
13:8	*Reserved*			*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*
7	EXTENDEDHIBERNATION	0x0	R	**New BitField**

Bit	Name	Reset	Access	Description
6	HIBERNATION	0x0	R	**New BitField**
5	AHBFREQ	0x1	R	**AHB Frequency**
	Minimum AHB Frequency Less Than 60 MHz			
4	PARTIALPWRDN	0x1	R	**New BitField**
3:0	NUMDEVPERIOEPS	0x0	R	**Dev Mode Periodic IN EPs**

31.8.16 USBAHB_GDFIFOCFG - Global DFIFO Configuration Reg

Offset	Bit Position																													
0x05C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x2EC																0x300															
Access	RW																RW															
Name	EPINFOBASEADDR																GDFIFOCFG															

Bit	Name	Reset	Access	Description
31:16	EPINFOBASEADDR	0x2EC	RW	**New BitField**
15:0	GDFIFOCFG	0x300	RW	**New BitField**

31.8.17 USBAHB_DIEPTXF1 - Device in EP Xmit FIFO Siz Reg 1

Offset	Bit Position																													
0x104	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset											0x300															0x600						
Access											RW															RW						
Name											INEPNTXFDEP															INEPNTXFSTADDR						

Bit	Name	Reset	Access	Description
31:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25:16	INEPNTXFDEP	0x300	RW	**IN Endpoint TxFIFO Depth** This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 32,768 The power-on reset value of this register is specified as the Largest IN Endpoint FIFO number Depth Programmed values must not exceed the power-on value
15:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:0	INEPNTXFSTADDR	0x600	RW	**IN EP FIFOn xmit RAM Start Addr** This field contains the memory start address For IN endpoint Transmit FIFOn (0(less than)n(less than) = 15). The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth Programmed values must not exceed the power-on value.

31.8.18 USBAHB_DIEPTXF2 - Device in EP Xmit FIFO Size Register 2

Offset	Bit Position																													
0x108	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset												0x300															0x900				
Access												RW															RW				
Name												INEPNTXFDEP															INEPNTXFSTADDR				

Bit	Name	Reset	Access	Description
31:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25:16	INEPNTXFDEP	0x300	RW	**IN Endpoint TxFIFO Depth**
15:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:0	INEPNTXFSTADDR	0x900	RW	**IN EP FIFOn xmit RAM Start Addr**

31.8.19 USBAHB_DIEPTXF3 - Device in EP Xmit FIFO Size Register 2

Offset	Bit Position																													
0x10C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset											0x300															0xC00					
Access											RW															RW					
Name											INEPNTXFDEP															INEPNTXFSTADDR					

Bit	Name	Reset	Access	Description
31:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25:16	INEPNTXFDEP	0x300	RW	**IN Endpoint TxFIFO Depth**
15:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:0	INEPNTXFSTADDR	0xC00	RW	**IN EP FIFOn xmit RAM Start Addr**

31.8.20 USBAHB_DIEPTXF4 - Device in EP Xmit FIFO Size Register 2

Offset	Bit Position																													
0x110	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset											0x300															0xF00						
Access											RW															RW						
Name											INEPNTXFDEP															INEPNTXFSTADDR						

Bit	Name	Reset	Access	Description
31:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25:16	INEPNTXFDEP	0x300	RW	**IN Endpoint TxFIFO Depth**
15:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11:0	INEPNTXFSTADDR	0xF00	RW	**IN EP FIFOn xmit RAM Start Addr**

31.8.21 USBAHB_DIEPTXF5 - Device in EP Xmit FIFO Size Register 2

Offset	Bit Position																													
0x114	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset							0x300													0x1200										
Access							RW													RW										
Name							INEPNTXFDEP													INEPNTXFSTADDR										

Bit	Name	Reset	Access	Description
31:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25:16	INEPNTXFDEP	0x300	RW	**IN Endpoint TxFIFO Depth**
15:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12:0	INEPNTXFSTADDR	0x1200	RW	**IN EP FIFOn xmit RAM Start Addr**

31.8.22 USBAHB_DIEPTXF6 - Device in EP Xmit FIFO Size Register 2

Offset	Bit Position																													
0x118	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset							0x300													0x1500											
Access							RW													RW											
Name							INEPNTXFDEP													INEPNTXFSTADDR											

Bit	Name	Reset	Access	Description
31:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25:16	INEPNTXFDEP	0x300	RW	**IN Endpoint TxFIFO Depth**
15:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12:0	INEPNTXFSTADDR	0x1500	RW	**IN EP FIFOn xmit RAM Start Addr**

31.8.23 USBAHB_DIEPTXF7 - Device in EP Xmit FIFO Size Register 2

Offset	Bit Position																													
0x11C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset							0x300													0x1800										
Access							RW													RW										
Name							INEPNTXFDEP													INEPNTXFSTADDR										

Bit	Name	Reset	Access	Description
31:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25:16	INEPNTXFDEP	0x300	RW	**IN Endpoint TxFIFO Depth**
15:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12:0	INEPNTXFSTADDR	0x1800	RW	**IN EP FIFOn xmit RAM Start Addr**

31.8.24 USBAHB_DIEPTXF8 - Device in EP Xmit FIFO Size Register 2

Offset	Bit Position																													
0x120	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset							0x300													0x1B00											
Access							RW													RW											
Name							INEPNTXFDEP													INEPNTXFSTADDR											

Bit	Name	Reset	Access	Description
31:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25:16	INEPNTXFDEP	0x300	RW	**IN Endpoint TxFIFO Depth**
15:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12:0	INEPNTXFSTADDR	0x1B00	RW	**IN EP FIFOn xmit RAM Start Addr**

31.8.25 USBAHB_DIEPTXF9 - Device in EP Xmit FIFO Size Register 2

Offset	Bit Position																													
0x124	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset							0x300													0x1E00											
Access							RW													RW											
Name							INEPNTXFDEP													INEPNTXFSTADDR											

Bit	Name	Reset	Access	Description
31:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25:16	INEPNTXFDEP	0x300	RW	**IN Endpoint TxFIFO Depth**
15:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12:0	INEPNTXFSTADDR	0x1E00	RW	**IN EP FIFOn xmit RAM Start Addr**

31.8.26 USBAHB_DCFG - Device Configuration Register

Offset	Bit Position																													
0x800	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x2						0x0										0x0	0x0	0x0	0x0		0x0							0x0	0x0	0x0		
Access	RW						RW										RW	RW	RW	RW		RW							RW	RW	RW		
Name	RESVALID						PERSCHINTVL										ERRATICINTMSK	XCVRDLY	ENDEVOUTNAK	PERFRINT		DEVADDR							ENA32KHZSUSP	NZSTSOUTHSHK	DEVSPD		

Bit	Name	Reset	Access	Description
31:26	RESVALID	0x2	RW	**Resume VAlidation Period**
	This field is effective only when DCFG.ENA32KHZSusp is set. It will control the resume period when the core resumes from suspend. The core counts for (unicode)ResValid(unicode) number of clock cycles to detect a valid resume when this is set			
25:24	PERSCHINTVL	0x0	RW	**Periodic Scheduling Interval**
	PerSchIntvl must be programmed only For Scatter/Gather DMA mode. Description: This field specifies the amount of time the Internal DMA engine must allocate For fetching periodic IN endpoint data. Based on the number of periodic endpoints, this value must be specified as 25,50 or 75% of (micro)frame. When any periodic endpoints are active, the internal DMA engine allocates the specified amount of time in fetching periodic IN endpoint data . When no periodic endpoints are active, Then the internal DMA engine services non-periodic endpoints, ignoring this field. After the specified time within a (micro)frame, the DMA switches to fetching For non-periodic endpoints. 2'b00: 25% of (micro)frame. 2'b01: 50% of (micro)frame. 2'b10: 75% of (micro)frame. 2'b11: Reserved. Reset: 2'b00			
23:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15	ERRATICINTMSK	0x0	RW	
14	XCVRDLY	0x0	RW	
13	ENDEVOUTNAK	0x0	RW	**Enable Device out of NAK**
	This bit enables setting NAK for Bulk OUT endpoints after the transfer is completed for Device mode Descriptor DMA 1'b0 : The core does not set NAK after Bulk OUT transfer complete 1'b1 : The core sets NAK after Bulk OUT transfer complete It is one time programmable after reset like any other DCFG register bits.			
12:11	PERFRINT	0x0	RW	**Periodic Frame Interval**
	Indicates the time within a frame at which the application must be notified using the End Of Periodic Frame Interrupt. This can be used to determine if all the isochronous traffic for that frame is complete.			
10:4	DEVADDR	0x0	RW	**Device Address**
	The application must program this field after every SetAddress control command.			
3	ENA32KHZSUSP	0x0	RW	**Enable 32 KHz Suspend mode**
	This bit can be set only if FS PHY interface is selected. Else this bit needs to be set to zero. When FS PHY interface is chosen and this bit is set, the core expects that the PHY clock duringSuspend is switched from 48 MHz to 32 KHz			
2	NZSTSOUTHSHK	0x0	RW	**NZ-Length Status OUT Handshake**

Bit	Name	Reset	Access	Description
	The application can use this field to select the handshake the core sends on receiving a nonzero-length data packet during the OUT transaction of a control transfer's Status stage. 1'b1: Send a STALL handshake on a nonzero-length status OUT transaction and do not send the received OUT packet to the application; 1'b0: Send the received OUT packet to the application (zerolength or nonzero-length) and send a handshake based on the NAK and STALL bits For the endpoint in the Device Endpoint Control register.			
1:0	DEVSPD	0x0	RW	**Device Speed** Indicates the speed at which the application requires the core to enumerate, or the maximum speed the application can support. However, the actual bus speed is determined only after the chirp sequence is completed, and is based on the speed of the USB host to which the core is connected.

31.8.27 USBAHB_DCTL - Device Control Register

Offset	Bit Position																													
0x804	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																0x0	0x0				0x0	0x0	0x0	0x0	0x0		0x0		0x0	0x0	0x1	0x0
Access																RW	RW				RW	W	W	W	W		RW		R	R	RW	RW
Name																NAKONBBLE	IGNRFRMNUM				PWRONPRGDONE	CGOUTNAK	SGOUTNAK	CGNPINNAK	SGNPINNAK		TSTCTL		GOUTNAKSTS	GNPINNAKSTS	SFTDISCON	RMTWKUPSIG

Bit	Name	Reset	Access	Description
31:17	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
16	NAKONBBLE	0x0	RW	**NAK on Babble Error** Set NAK automatically on babble (NakOnBble). The core sets NAK automatically for the endpoint on which babble is received
15	IGNRFRMNUM	0x0	RW	**Ignore frame num for ISO end points** Do NOT program IgnrFrmNum bit to 1'b1 when the core is operating in threshold mode. Note: When Scatter/Gather DMA mode is enabled this feature is not applicable to High Speed, High bandwidth transfers. When this bit is enabled, there must be only one packet per descriptor. 0: The core transmits the packets only in the frame number in which they are intended to be transmitted. 1: The core ignores the frame number, sending packets immediately as the packets are ready. In Scatter/Gather DMA mode, if this bit is enabled, the packets are not flushed when a ISOC IN token is received for an elapsed frame. When Scatter/Gather DMA mode is disabled, this field is used by the application to enable periodic transfer interrupt. The application can program periodic endpoint transfers for multiple (micro)frames. 0: periodic transfer interrupt feature is disabled, application needs to program transfers for periodic endpoints every (micro)frame 1: periodic transfer interrupt feature is enabled, application can program transfers for multiple (micro)frames for periodic endpoints. In non Scatter/Gather DMA mode the application will receive transfer complete interrupt after transfers for multiple (micro)frames are completed
14:12	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
11	PWRONPRGDONE	0x0	RW	**Power-On Programming Done** The application uses this bit to indicate that register programming is completed after a wake-up from Power Down
10	CGOUTNAK	0x0	W	**Clear Global Out NAK** A write to this field clears the Global OUT NAK
9	SGOUTNAK	0x0	W	**Set Global Out NAK** A write to this field sets the Global OUT NAK. The application uses this bit to send a NAK handshake on all OUT endpoints. The application must Set the this bit only after making sure that the Global OUT NAK Effective bit in the Core Interrupt Register (GINTSTS.GOUTNAKEFF) is cleared.
8	CGNPINNAK	0x0	W	**Clear Global Non-periodic IN NAK** A write to this field clears the Global Non-periodic IN NAK
7	SGNPINNAK	0x0	W	**Set Global Non-periodic in NAK**

Bit	Name	Reset	Access	Description
	A write to this field sets the Global Non-periodic IN NAK.The application uses this bit to send a NAK handshake on all nonperiodic IN endpoints. The core can also Set this bit when a timeout condition is detected on a non-periodic endpoint in shared FIFO operation. The application must Set this bit only after making sure that the Global IN NAK Effective bit in the Core Interrupt Register (GINTSTS.GINNAKEFF) is cleared			
6:4	TSTCTL	0x0	RW	**TEst Control**
	"DISABLE" : [0, "Test mode disabled."], "J" : [1, "Test_J mode."], "K" : [2, "Test_K mode."], "SE0NAK" : [3, "Test_SE0_NAK mode."], "PACKET" : [4, "Test_Packet mode."], "FORCE" : [5, "Test_Force_Enable."],			
3	GOUTNAKSTS	0x0	R	**Global OUT NAK Status**
	1'b0: A handshake is sent based on the FIFO Status and the NAK and STALL bit settings. 1'b1: No data is written to the RxFIFO, irrespective of space availability. Sends a NAK handshake on all packets, except on SETUP transactions. All isochronous OUT packets are dropped.			
2	GNPINNAKSTS	0x0	R	**Global Non-periodic IN NAK Status**
	1'b0: A handshake is sent out based on the data availability in the transmit FIFO. 1'b1: A NAK handshake is sent out on all non-periodic IN endpoints, irrespective of the data availability in the transmit FIFO.			
1	SFTDISCON	0x1	RW	**Soft Disconnect**
	The application uses this bit to signal the DWC_otg core to do a soft disconnect. As long as this bit is Set, the host does not see that the device is connected, and the device does not receive signals on the USB. The core stays in the disconnected state until the application clears this bit. The minimum duration For which the core must keep this bit Set is specified in Table 5-46. 1'b0: Normal operation. When this bit is cleared after a soft disconnect, the core drives the phy_opmode_o signal on the UTMI+ to 2'b00, which generates a device connect event to the USB host. When the device is reconnected, the USB host restarts device enumeration. 1'b1: The core drives the phy_opmode_o signal on the UTMI+ to 2'b01, which generates a device disconnect event to the USB host. Note: This bit can be also used for ULPI/FS Serial interfaces. Note: This bit is not impacted by a soft reset.			
0	RMTWKUPSIG	0x0	RW	**Remote Wakeup Signalling**
	When the application sets this bit, the core initiates remote signaling to wake up the USB host. The application must Set this bit to instruct the core to exit the Suspend state. As specified in the USB 2.0 specification, the application must clear this bit 1-15 ms after setting it. Remote Wakeup Signaling (RmtWkUpSig) When LPM is enabled, In L1 state the behavior of this bit is as follows: When the application sets this bit, the core initiates L1 remote signaling to wake up the USB host. The application must set this bit to instruct the core to exit the Sleep state. As specified in the LPM specification, the hardware will automatically clear this bit after a time of 50 micro sec (TL1DevDrvResume) after set by application. Application should not set this bit when GLPMCFG bRemoteWake from the previous LPM transaction was zero.			

31.8.28 USBAHB_DSTS - Device Status Register

Offset	Bit Position																													
0x808	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset									0x0		0x0																		0x0	0x0		0x0
Access									R		R																		R	R		R
Name									DEVLNSTS		SOFFN																		ERRTICERR	ENUMSPD		SUSPSTS

Bit	Name	Reset	Access	Description
31:24	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
23:22	DEVLNSTS	0x0	R	**logic level of USB data lines**
	Indicates the current logic level USB data lines DevLnSts[1]: Logic level of D+ DevLnSts[0]: Logic level of D-			
21:8	SOFFN	0x0	R	**Frame/u-frameNumber of the recvd SOF**
	When the core is operating at high speed, this field contains a microframe number. When the core is operating at full or low speed, this field contains a Frame number. Note: This register may return a non zero value if read immediately after power on reset. In case the register bit reads non zero immediately after power on reset it does not indicate that SOF has been received from the host. The read value of this interrupt is valid only after a valid connection between host and device is established.			
7:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	ERRTICERR	0x0	R	**Erratic Error**
	The core sets this bit to report any erratic errors (phy_rxvalid_i/phy_rxvldh_i or phy_rxactive_i is asserted For at least 2 ms, due to PHY error) seen on the UTMI+ . Due to erratic errors, the DWC_otg core goes into Suspended state and an interrupt is generated to the application with Early Suspend bit of the Core Interrupt register (GINTSTS.ERLYSUSP). If the early suspend is asserted due to an erratic error, the application can only perform a soft disconnect recover.			
2:1	ENUMSPD	0x0	R	**Enumerated Speed**
	Indicates the speed at which the core has come up after speed detection through a chirp sequence. "LS" : [2, "Low speed (PHY clock is running at 6 MHz)."], "FS" : [3, "Full speed (PHY clock is running at 48 MHz)."],			
0	SUSPSTS	0x0	R	**Suspend Status**
	In Device mode, this bit is Set as long as a Suspend condition is detected on the USB. The core enters the Suspended state when there is no activity on the phy_line_state_i signal For an extended period of time. The core comes out of the suspend: When there is any activity on the phy_line_state_i signal When the application writes to the Remote Wakeup Signaling bit in the Device Control register (DCTL.RMTWKUPSIG).			

31.8.29 USBAHB_DIEPMSK - Device in EP Common IRQ Mask Register

Offset	Bit Position																													
0x810	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																			0x0					0x0		0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																			RW					RW		RW	RW	RW	RW	RW	RW	RW
Name																			NAKMSK					TXFIFOUNDRNMSK		INEPNAKEFFMSK	INTKNEPMISMSK	INTKNTXFEMPMSK	TIMEOUTMSK	AHBERRMSK	EPDISBLDMSK	XFERCOMPLMSK

Bit	Name	Reset	Access	Description
31:14	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
13	NAKMSK	0x0	RW	**NAK interrupt Mask**
12:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8	TXFIFOUNDRNMSK	0x0	RW	**FIFO Underrun Mask**
7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6	INEPNAKEFFMSK	0x0	RW	**IN Endpoint NAK Effective Mask**
5	INTKNEPMISMSK	0x0	RW	**IN Token recvd with EP Mismatch Mask**
4	INTKNTXFEMPMSK	0x0	RW	**IN token recvd when FIFO mt irq mask**
3	TIMEOUTMSK	0x0	RW	**Timout Condition Mask**
2	AHBERRMSK	0x0	RW	**AHB Error Mask**
1	EPDISBLDMSK	0x0	RW	**Endpoint Disabled Interrupt Mask**
0	XFERCOMPLMSK	0x0	RW	**Transfer Completed Interrupt Mask**

31.8.30 USBAHB_DOEPMSK - New Register

Offset	Bit Position																													
0x814	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																		0x0	0x0	0x0				0x0		0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																		RW	RW	RW				RW		RW	RW	RW	RW	RW	RW	RW
Name																		NYETMSK	NAKMSK	BBLEERRMSK				OUTPKTERRMSK		BACK2BACKSETUP	STSPHSERCVDMSK	OUTTKNEPDISMSK	SETUPMSK	AHBERRMSK	EPDISBLDMSK	XFERCOMPPLMSK

Bit	Name	Reset	Access	Description
31:15	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
14	NYETMSK	0x0	RW	**NYET Interrupt Mask**
13	NAKMSK	0x0	RW	**NAK Interrupt Mask**
12	BBLEERRMSK	0x0	RW	**Babble Error Interrupt Mask**
11:9	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
8	OUTPKTERRMSK	0x0	RW	**OUT Packet Error Mask**
7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6	BACK2BACKSETUP	0x0	RW	**Back-to-Back SETUP Packets recvd Mask** Applies to control OUT endpoints only
5	STSPHSERCVDMSK	0x0	RW	**Status Phase Received Mask** Applies to control OUT endpoints only
4	OUTTKNEPDISMSK	0x0	RW	**OUT Token recvd when EP Disabled Mask** Applies to control OUT endpoints only
3	SETUPMSK	0x0	RW	**Setup Phase Done Mask** Applies to control endpoints only.
2	AHBERRMSK	0x0	RW	**Ahb Error Mask**
1	EPDISBLDMSK	0x0	RW	**Endpoint Disabled Interrupt Mask**
0	XFERCOMPPLMSK	0x0	RW	**Device OUT EP Common IRQ Mask Register**

31.8.31 USBAHB_DAINT - Device All EP Interrupt Register

Offset	Bit Position																													
0x818	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset							0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0							0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access							R	R	R	R	R	R	R	R	R	R							R	R	R	R	R	R	R	R	R	R
Name							OUTEPINT9	OUTEPINT8	OUTEPINT7	OUTEPINT6	OUTEPINT5	OUTEPINT4	OUTEPINT3	OUTEPINT2	OUTEPINT1	OUTEPINT0							INEPINT9	INEPINT8	INEPINT7	INEPINT6	INEPINT5	INEPINT4	INEPINT3	INEPINT2	INEPINT1	INEPINT0

Bit	Name	Reset	Access	Description
31:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25	OUTEPINT9	0x0	R	**EP9 OUT IRQ**
24	OUTEPINT8	0x0	R	**EP8 OUT IRQ**
23	OUTEPINT7	0x0	R	**EP7 OUT IRQ**
22	OUTEPINT6	0x0	R	**EP6 OUT IRQ**
21	OUTEPINT5	0x0	R	**EP5 OUT IRQ**
20	OUTEPINT4	0x0	R	**EP4 OUT IRQ**
19	OUTEPINT3	0x0	R	**EP3 OUT IRQ**
18	OUTEPINT2	0x0	R	**EP2 OUT IRQ**
17	OUTEPINT1	0x0	R	**EP1 OUT IRQ**
16	OUTEPINT0	0x0	R	**EP0 OUT IRQ**
15:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	INEPINT9	0x0	R	**EP9 IRQ**
8	INEPINT8	0x0	R	**EP8 IRQ**
7	INEPINT7	0x0	R	**EP7 IRQ**

Bit	Name	Reset	Access	Description
6	INEPINT6	0x0	R	**EP6 IRQ**
5	INEPINT5	0x0	R	**EP5 IRQ**
4	INEPINT4	0x0	R	**EP4 IRQ**
3	INEPINT3	0x0	R	**EP3 IRQ**
2	INEPINT2	0x0	R	**EP2 IRQ**
1	INEPINT1	0x0	R	**EP1 IRQ**
0	INEPINT0	0x0	R	**EP0 IRQ**

31.8.32 USBAHB_DAINTMSK - Device All EP Interrupt Mask Register

Offset	Bit Position																													
0x81C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset							0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0							0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name							OUTEPMSK9	OUTEPMSK8	OUTEPMSK7	OUTEPMSK6	OUTEPMSK5	OUTEPMSK4	OUTEPMSK3	OUTEPMSK2	OUTEPMSK1	OUTEPMSK0							INEPMSK9	INEPMSK8	INEPMSK7	INEPMSK6	INEPMSK5	INEPMSK4	INEPMSK3	INEPMSK2	INEPMSK1	INEPMSK0

Bit	Name	Reset	Access	Description
31:26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25	OUTEPMSK9	0x0	RW	**OUT EP MASK9**
24	OUTEPMSK8	0x0	RW	**OUT EP MASK8**
23	OUTEPMSK7	0x0	RW	**OUT EP MASK7**
22	OUTEPMSK6	0x0	RW	**OUT EP MASK6**
21	OUTEPMSK5	0x0	RW	**OUT EP MASK5**
20	OUTEPMSK4	0x0	RW	**OUT EP MASK4**
19	OUTEPMSK3	0x0	RW	**OUT EP MASK3**
18	OUTEPMSK2	0x0	RW	**OUT EP MASK2**
17	OUTEPMSK1	0x0	RW	**OUT EP MASK1**
16	OUTEPMSK0	0x0	RW	**OUT EP MASK0**
15:10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	INEPMSK9	0x0	RW	**IN EP MASK9**
8	INEPMSK8	0x0	RW	**IN EP MASK8**
7	INEPMSK7	0x0	RW	**IN EP MASK7**

Bit	Name	Reset	Access	Description
6	INEPMSK6	0x0	RW	**IN EP MASK6**
5	INEPMSK5	0x0	RW	**IN EP MASK5**
4	INEPMSK4	0x0	RW	**IN EP MASK4**
3	INEPMSK3	0x0	RW	**IN EP MASK3**
2	INEPMSK2	0x0	RW	**IN EP MASK2**
1	INEPMSK1	0x0	RW	**IN EP MASK1**
0	INEPMSK0	0x0	RW	**IN EP MASK0**

31.8.33 USBAHB_DTHRCTL - Device Threshold Control Register

Offset	Bit Position																													
0x830	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset					0x1		0x8									0x0				0x0		0x8								0x0	0x0
Access					RW		RW									RW				RW		RW								RW	RW
Name					ARBPRKEN		RXTHRLEN									RXTHREN				AHBTHRRATIO		TXTHRLEN								ISOTHREN	NONISOTHREN

Bit	Name	Reset	Access	Description
31:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27	ARBPRKEN	0x1	RW	**Arbiter Parking Enable**
	This bit controls internal DMA arbiter parking For IN endpoints. When thresholding is enabled and this bit is Set to one, Then the arbiter parks on the IN endpoint For which there is a token received on the USB. This is done to avoid getting into underrun conditions. By Default the parking is enabled.			
26	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
25:17	RXTHRLEN	0x8	RW	**Receive Threshold Length**
	This field specifies Receive thresholding size in DWORDS. This field also specifies the amount of data received on the USB before the core can start transmitting on the AHB. The threshold length has to be at least eight DWORDS. The recommended value For ThrLen is to be the same as the programmed			
16	RXTHREN	0x0	RW	**Receive Threshold Enable**
	When this bit is Set, the core enables thresholding in the receive direction. Note: We recommends that you do not enable RxThrEn, because it may cause issues in the RxFIFO especially during error conditions such as RxError and Babble.			
15:13	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
12:11	AHBTHRRATIO	0x0	RW	**AHB Threshold Ratio**
	These bits define the ratio between the AHB threshold and the MAC threshold for the transmit path only. The AHB threshold always remains less than or equal to the USB threshold, because this does not increase overhead. Both the AHB and the MAC threshold must be DWORD-aligned. The application needs to program TXTHRLEN and the AHBTHRRATIO to make the AHB Threshold value DWORD aligned. If the AHB threshold value is not DWORD aligned, the core might not behave correctly. When programming the TXTHRLEN and AHBTHRRATIO, the application must ensure that the minimum AHB threshold value does not go below 8 DWORDS "DIV1" : [0, "AHB threshold = MAC threshold."], "DIV2" : [1, "AHB threshold = MAC threshold / 2."], "DIV4" : [2, "AHB threshold = MAC threshold / 4."], "DIV8" : [3, "AHB threshold = MAC threshold / 8."],			
10:2	TXTHRLEN	0x8	RW	**Transmit threshold length**
	This field specifies Transmit thresholding size in DWORDS. This also forms the MAC threshold and specifies the amount of data in bytes to be in the corresponding endpoint transmit FIFO, before the core can start transmit on the USB. The threshold length has to be at least eight DWORDS when the value of AHBThrRatio is 2'h00. In case the AHBThrRatio is non zero the application needs to ensure that the AHB Threshold value does not go below the recommended eight DWORD. This field controls both isochronous and non-isochronous IN endpoint thresholds. The recommended value for ThrLen is to be the same as the programmed AHB Burst Length (GAHBCFG.HBSTLEN).			
1	ISOTHREN	0x0	RW	**ISO IN EP Threshold Enable**
	When this bit is Set, the core enables thresholding For isochronous IN endpoints.			

Bit	Name	Reset	Access	Description
0	NONISOTHREN	0x0	RW	**Non-ISO IN EP Threshold Enable**
	When this bit is Set, the core enables thresholding For Non Isochronous IN Endpoints			

31.8.34 USBAHB_DIEPEMPMSK - Device in EP FIFO Empty IRQ Mask Reg

Offset	Bit Position																													
0x834	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																								0x0								
Access																								RW								
Name																								DIEPMPMSK								

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	DIEPMPMSK	0x0	RW	**IN EP Tx FIFO Empty IRQ Mask Bits**
	These bits acts as mask bits For DIEPINTn. TxFEmp interrupt One bit per IN Endpoint: Bit 0 For IN EP 0, bit 15 For IN EP 15			

31.8.35 USBAHB_DIEP0CTL - Device Control in EP 0 Ctrl Reg

Offset	Bit Position																													
0x900	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0			0x0	0x0	0x0				0x0		0x0		0x0		0x1														0x0	
Access	RW	RW			W	W	RW				RW		R		R		R														RW	
Name	EPENA	EPDIS			SNAK	CNAK	TXFNUM				STALL		EPTYPE		NAKSTS		USBACTEP														MPS	

Bit	Name	Reset	Access	Description
31	EPENA	0x0	RW	**End point enable**
	When Scatter/Gather DMA mode is enabled, For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. When Scatter/Gather DMA mode is disabled such as in buffer pointer based DMA mode this bit indicates that data is ready to be transmitted on the endpoint. The core clears this bit before setting the following interrupts on this endpoint: Endpoint Disabled Transfer Completed			
30	EPDIS	0x0	RW	**Endpoint Disable**
	The application sets this bit to stop transmitting data on an endpoint, even before the transfer For that endpoint is complete. The application must wait For the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled Interrupt. The application must Set this bit only If Endpoint Enable is already Set For this endpoint			
29:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27	SNAK	0x0	W	**Set NAK**
	A write to this bit sets the NAK bit For the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also Set this bit For an endpoint after a SETUP packet is received on that endpoint.			
26	CNAK	0x0	W	**Clear NAK**
	R0/W1; A write to this bit clears the NAK bit For the endpoint			
25:22	TXFNUM	0x0	RW	**TXFIFO Number**
	For Shared FIFO operation, this value is always Set to 0, indicating that control IN endpoint 0 data is always written in the Non-Periodic Transmit FIFO. For Dedicated FIFO operation, this value is Set to the FIFO number that is assigned to IN Endpoint 0			
21	STALL	0x0	RW	**Handshake**
	The application can only Set this bit, and the core clears it, when a SETUP token is received For this endpoint. If a NAK bit, Global Nonperiodic IN NAK, or Global OUT NAK is Set along with this bit, the STALL bit takes priority			
20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:18	EPTYPE	0x0	R	**Endpoint Type**
	Hardcoded to 00 For control			
17	NAKSTS	0x0	R	**NAK Status**
	1'b0: The core is transmitting non-NAK handshakes based on the FIFO status 1'b1: The core is transmitting NAK handshakes on this endpoint. When this bit is Set, either by the application or core, the core stops transmitting data, even If there is data available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake			

Bit	Name	Reset	Access	Description
16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15	USBACTEP	0x1	R	**USB Active Endpoint** This bit is always SET to 1, indicating that control endpoint 0 is always active in all configurations and interfaces
14:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	MPS	0x0	RW	**Maximum packet size** The application must program this field with the maximum packet size for the current logical endpoint. 64B" : [0, "64 bytes."], "32B" : [1, "32 bytes."], "16B" : [2, "16 bytes."], "8B" : [3, "8 bytes."],

31.8.36 USBAHB_DIEP0INT - Device in EP 0 IRQ Reg

Offset	Bit Position																													
0x908	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																		0x0	0x0	0x0	0x0		0x0	0x0	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																		RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name																		NYETINTRPT	NAKINTRPT	BBLEERR	PKTDRPSTS		BNAINTR	TXFIFOUNDRN	TXFEMP	INEPNAKEFF	INTKNEPMIS	INTKNTXFEMP	TIMEOUT	AHBERR	EPDISBLD	XFERCOMPL

Bit	Name	Reset	Access	Description
31:15	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
14	NYETINTRPT	0x0	RW	**NYET Interrupt** The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint
13	NAKINTRPT	0x0	RW	**NAK Interrupt**
12	BBLEERR	0x0	RW	**Babble error** The core generates this interrupt when babble is received for the endpoint
11	PKTDRPSTS	0x0	RW	**Packet Drop Status** This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected
10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	BNAINTR	0x0	RW	**BNA(Buffer Not Available) IRQ** This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready For the Core to process, such as Host busy or DMA
8	TXFIFOUNDRN	0x0	RW	**FIFO Underrun** Applies to IN endpoints Only The core generates this interrupt when it detects a transmit FIFO underrun condition in threshold mode For this endpoint.
7	TXFEMP	0x1	RW	**TX FIFO Empty** This bit is valid only For IN Endpoints This interrupt is asserted when the TxFIFO For this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTXFEMPLVL)).
6	INEPNAKEFF	0x0	RW	**In Endpoint NAK Effective** Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCTLn.CNAK. This interrupt indicates that the core has sampled the NAK bit Set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit Set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit.
5	INTKNEPMIS	0x0	RW	**IN Token recvd with EP Mismatch**

Bit	Name	Reset	Access	Description
	Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one For which the IN token was received. This interrupt is asserted on the endpoint For which the IN token was received.			
4	INTKNTXFEMP	0x0	RW	**In Token recvd when TXFIFO Empty**
	Applies to non-periodic IN endpoints only. Indicates that an IN token was received when the associated TxFIFO (periodic/non-periodic) was empty. This interrupt is asserted on the endpoint For which the IN token was received			
3	TIMEOUT	0x0	RW	**Condition**
	In shared TX FIFO mode, applies to non-isochronous IN endpoints only. In dedicated FIFO mode, applies only to Control IN endpoints. In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB For the last IN token on this endpoint			
2	AHBERR	0x0	RW	**AHB Error**
	Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/write. The application can read the corresponding endpoint DMA address register to get the error address			
1	EPDISBLD	0x0	RW	**Endpoint Disabled Interrupt**
	Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.			
0	XFERCOMPL	0x0	RW	**Transfer Completed Interrupt**
	Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled - For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. - For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit For the corresponding descriptor is Set. When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, For this endpoint.			

31.8.37 USBAHB_DIEP0TSIZ - Device in EP 0 Xfer Size Reg

Offset	Bit Position																															
0x910	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset												0x0																	0x0			
Access												RW																	RW			
Name												PKTCNT																	XFERSIZE			

Bit	Name	Reset	Access	Description
31:21	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
20:19	PKTCNT	0x0	RW	**Packet Count**
	Indicates the total number of USB packets that constitute the Transfer Size amount of data For endpoint 0. In Endpoints : This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. OUT Endpoints: This field is decremented every time a packet (maximum size or short packet) is written to the RxFIFO			
18:7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:0	XFERSIZE	0x0	RW	**Transfer size**
	This field contains the transfer size in bytes for the current endpoint. The transfer size (XferSize) = Sum of buffer sizes across all descriptors in the list for the endpoint. In Buffer DMA, the core only interrupts the application after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. IN Endpoints: The core decrements this field every time a packet from the external memory is written to the TxFIFO. OUT Endpoints: The core decrements this field every time a packet is read from the RxFIFO and written to the external memory			

31.8.38 USBAHB_DIEP0DMAADDR - Device in EP 0 DMA Addr Reg

Offset	Bit Position																															
0x914	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																0x0																
Access																RW																
Name																DMAADDR																

Bit	Name	Reset	Access	Description
31:0	DMAADDR	0x0	RW	**DMA Addr**

31.8.39 USBAHB_DIEP0TXFSTS - DEvice in EP TX FIFO Status Reg 0

Offset	Bit Position																													
0x918	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																								0x300								
Access																								R								
Name																								SPCAVAIL								

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	SPCAVAIL	0x300	R	**IN EP TxFIFO Space avail** Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words. 16'h0: Endpoint TxFIFO is full 16'h1: 1 word available 16'h2: 2 words available 16'hn: n words available (where 0 n 32,768) 16'h8000: 32,768 words available Others: Reserved

31.8.40 USBAHB_DEVINEPx_CTL - Device Control in EP 1 CTRL Reg

Offset	Bit Position																															
0x920	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0				0x0		0x0		0x0	0x0	0x0					0x0										
Access	RW	RW	W	W	W	W	RW				RW		RW		R	R	RW					RW										
Name	EPENA	EPDIS	SETD1PIDOF	SETD0PIDEF	SNAK	CNAK	TXFNUM				STALL		EPTYPE		NAKSTS	DPID	USBACTEP					MPS										

Bit	Name	Reset	Access	Description
31	EPENA	0x0	RW	**Endpoint enable**
30	EPDIS	0x0	RW	**Endpoint Disable** Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.
29	SETD1PIDOF	0x0	W	**Set DATA1 PID / odd Frame** For bulk and interrupt endpoints writing this field sets the Endpoint Data PID / Even or Odd Frame (DPIDEOF) field in this register to DATA1ODD. For isochronous endpoints writing this field sets the Endpoint Data PID / Even or Odd Frame (DPIDEOF) field to odd (DATA1ODD)
28	SETD0PIDEF	0x0	W	**Set DATA0 PID / Even Frame** For bulk and interrupt endpoints writing this field sets the Endpoint Data PID / Even or Odd Frame (DPIDEOF) field in this register to DATA0EVEN.</para> <para>For isochronous endpoints writing this field sets the Endpoint Data PID / Even or Odd Frame (DPIDEOF) field to odd (DATA0EVEN).
27	SNAK	0x0	W	**Set NAK** A write to this bit sets the NAK bit For the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also Set this bit For an endpoint after a SETUP packet is received on that endpoint
26	CNAK	0x0	W	**Clear NAK** A write to this bit clears the NAK bit For the endpoint
25:22	TXFNUM	0x0	RW	**TxFIFO Number** Shared FIFO Operation non-periodic endpoints must set this bit to zero. Periodic endpoints must map this to the corresponding Periodic TxFIFO number. 4'h0: Non-Periodic TxFIFO Others: Specified Periodic TxFIFO.number Note: An interrupt IN endpoint can be configured as a non-periodic endpoint for applications such as mass storage. The core treats an IN endpoint as a non-periodic endpoint if the TxFNum field is set to 0. Otherwise, a separate periodic FIFO must be allocated for an interrupt IN endpoint, and the number of this FIFO must be programmed into the TxFNum field. Configuring an interrupt IN endpoint as a non-periodic endpoint saves the extra periodic FIFO area. Dedicated FIFO Operationthese bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO number. This field is valid only for IN endpoints.
21	STALL	0x0	RW	**Handshake**

Bit	Name	Reset	Access	Description
	Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. 1'b0 R_W Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.			
20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19:18	EPTYPE	0x0	RW	**Endpoint Type**
	This is the transfer type supported by this logical endpoint.", "modes" : { "CONTROL" : [0, "Control Endpoint."], "ISO" : [1, "Isochronous Endpoint."], "BULK" : [2, "Bulk Endpoint."], "INT" : [3, "Interrupt Endpoint."], }			
17	NAKSTS	0x0	R	**NAK STatus**
	Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.			
16	DPID	0x0	R	**Endpoint Data PID, EO_FrNum**
	Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. 1'b0: DATA0 1'b1: DATA1 This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. 1'b0 RO Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: Applies to isochronous IN and OUT endpoints only. Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro) frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. 1'b0: Even (micro)frame 1'b1: Odd (micro)frame When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure.			
15	USBACTEP	0x0	RW	**USB ACtive Endpoint**
	Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit			
14:11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10:0	MPS	0x0	RW	**Maximum Packet Size**
	The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes			

31.8.41 USBAHB_DEVINEPx_INT - Device in EP 1 IRQ Register

Offset	Bit Position																													
0x928	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																		0x0	0x0	0x0	0x0		0x0	0x0	0x1	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																		RW	RW	RW	RW		RW	RW	R	RW	RW	RW	RW	RW	RW	RW
Name																		NYETINTRPT	NAKINTRPT	BBLEERR	PKTDRPSTS		BNAINTR	TXFIFOUNDRN	TXFEMP	INEPNAKEFF	INTKNEPMIS	INTKNTXFEMP	TIMEOUT	AHBERR	EPDISBLD	XFERCOMPL

Bit	Name	Reset	Access	Description
31:15	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
14	NYETINTRPT	0x0	RW	**NYET Interrupt** The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint.
13	NAKINTRPT	0x0	RW	**NAK Interrupt**
12	BBLEERR	0x0	RW	**Babble Interrupt** The core generates this interrupt when babble is received for the endpoint
11	PKTDRPSTS	0x0	RW	**Packet Drop Status** This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected.
10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	BNAINTR	0x0	RW	**BNA (Buffer Not Available) IRQ** This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready For the Core to process, such as Host busy or DMA done
8	TXFIFOUNDRN	0x0	RW	**FIFO Underrun** Applies to IN endpoints Only This bit is valid only If thresholding is enabled. The core generates this interrupt when it detects a transmit FIFO underrun condition For this endpoint
7	TXFEMP	0x1	R	**TX FIFO Empty** This bit is valid only For IN Endpoints This interrupt is asserted when the TxFIFO For this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTXFEMPLVL)).
6	INEPNAKEFF	0x0	RW	**IN Endpoint NAK Effective** Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCTLn.CNAK. This interrupt indicates that the core has sampled the NAK bit Set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit Set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit.
5	INTKNEPMIS	0x0	RW	**IN Token recvd with EP Mismatch**

Bit	Name	Reset	Access	Description
	Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one For which the IN token was received. This interrupt is asserted on the endpoint For which the IN token was received.			
4	INTKNTXFEMP	0x0	RW	**IN Token recvd When TxFIFO is Empty**
	Applies to non-periodic IN endpoints only. Indicates that an IN token was received when the associated TxFIFO (periodic/non-periodic) was empty. This interrupt is asserted on the endpoint For which the IN token was received.			
3	TIMEOUT	0x0	RW	**COndition**
	In shared TX FIFO mode, applies to non-isochronous IN endpoints only. In dedicated FIFO mode, applies only to Control IN endpoints. In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB For the last IN token on this endpoint.			
2	AHBERR	0x0	RW	**AHB Error**
	Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/write. The application can read the corresponding endpoint DMA address register to get the error address.			
1	EPDISBLD	0x0	RW	**Endpoint Disabled IRQ**
	Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.			
0	XFERCOMPL	0x0	RW	**Transfer Completed IRQ**
	Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled - For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. - For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit For the corresponding descriptor is Set. When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, For this endpoint.			

31.8.42 USBAHB_DEVINEPx_TSIZ - Device in EP 1 Xfer Size Reg

Offset	Bit Position																															
0x930	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset		0x0						0x0															0x0									
Access		RW						RW															RW									
Name		MC						PKTCNT															XFERSIZE									

Bit	Name	Reset	Access	Description
31	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
30:29	MC	0x0	RW	**Multi Count**
28:19	PKTCNT	0x0	RW	**Packet Count** Indicates the total number of USB packets that constitute the Transfer Size amount of data For endpoint 0. This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO.
18:0	XFERSIZE	0x0	RW	**TRansfer Size** Indicates the transfer size in bytes For endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet from the external memory is written to the TxFIFO.

31.8.43 USBAHB_DEVINEPx_DMAADDR - Device in EP 1 DMA Address Reg

Offset	Bit Position																															
0x934	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	DMAADDR																															

Bit	Name	Reset	Access	Description
31:0	DMAADDR	0x0	RW	**DMA ADDR**

31.8.44 USBAHB_DEVINEPx_DTXFSTS - Device in EP TX FIFO Stat Reg

Offset	Bit Position																													
0x938	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																								0x300								
Access																								R								
Name																								INEPTXFSPCAVAIL								

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15:0	INEPTXFSPCAVAIL	0x300	R	**IN EP TxFIFO Space Avail**
	Indicates the amount of free space available in the Endpoint TxFIFO. Values are in terms of 32-bit words.			

31.8.45 USBAHB_DOEP0CTL - Device Ctrl OUT EP 0 CTRL Reg

Offset	Bit Position																													
0xB00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0			0x0	0x0					0x0	0x0	0x0		0x0		0x0														0x0	
Access	RW	R			W	W					RW	RW	R		R		R														R	
Name	EPENA	EPDIS			SNAK	CNAK					STALL	SNP	EPTYPE		NAKSTS		USBACTEP														MPS	

Bit	Name	Reset	Access	Description
31	EPENA	0x0	RW	**Endpoint Enable**
	When Scatter/Gather DMA mode is enabled, For OUT endpoints this bit indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is disabled(such as For buffer-pointer based DMA mode)this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: SETUP Phase Done Endpoint Disabled Transfer Completed Note: In DMA mode, this bit must be Set For the core to transfer SETUP data packets into memory.			
30	EPDIS	0x0	R	**Endpoint Disable**
	The application cannot disable control OUT endpoint 0			
29:28	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
27	SNAK	0x0	W	**Set NAK**
	A write to this bit sets the NAK bit For the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also Set bit on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.			
26	CNAK	0x0	W	**Clear NAK**
	A write to this bit clears the NAK bit For the endpoint			
25:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21	STALL	0x0	RW	**Handshake**
	The application can only Set this bit, and the core clears it, when a SETUP token is received For this endpoint. If a NAK bit or Global OUT NAK is Set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.			
20	SNP	0x0	RW	**Snoop mode**
	This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.			
19:18	EPTYPE	0x0	R	**Endpoint Type**
	Hardcoded to 2'b00 For control			
17	NAKSTS	0x0	R	**NAK Status**
	Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit, the core stops receiving data, even If there is space in the RxFIFO to accommodate the incoming packet. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.			
16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		

Bit	Name	Reset	Access	Description
15	USBACTEP	0x0	R	**US Active Endpoint** This bit is always Set to 1, indicating that a control endpoint 0 is always active in all configurations and interfaces
14:2	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
1:0	MPS	0x0	R	**Max packet size** The maximum packet size for control OUT endpoint 0 is the same as what is programmed in control IN Endpoint 0. "0" => 64Bytes, "1" => 32 Bytes, "2" => 16 Bytes, "3" => 8 Bytes

31.8.46 USBAHB_DOEP0INT - Device OUT EP 0 IRQ Register

Offset	Bit Position																													
0xB08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0	0x0	0x0	0x0	0x0		0x0	0x0		0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																	RW	RW	RW	RW	RW		RW	RW		RW	RW	RW	RW	RW	RW	RW
Name																	STUPPKTRCVD	NYETINTRPT	NAKINTRPT	BBLEERR	PKTDRPSTS		BNAINTR	OUTPKTERR		BACK2BACKSETUP	STSPHSERCVD	OUTTKNEPDIS	SETUP	AHBERR	EPDISBLD	XFERCOMPL

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15	STUPPKTRCVD	0x0	RW	**Setup Packet Received**
14	NYETINTRPT	0x0	RW	**NYET Interrupt** The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint
13	NAKINTRPT	0x0	RW	**NAK Interrupt**
12	BBLEERR	0x0	RW	**Babble Interrupt** The core generates this interrupt when babble is received for the endpoint
11	PKTDRPSTS	0x0	RW	**Packet Drop Status** This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected.
10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	BNAINTR	0x0	RW	**BNA (Buffer Not Available) IRQ** This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready For the Core to process, such as Host busy or DMA done
8	OUTPKTERR	0x0	RW	**OUT Packet Error** Applies to OUT endpoints Only This interrupt is valid only when thresholding is enabled. This interrupt is asserted when the core detects an overflow or a CRC error For non-Isochronous OUT packet.
7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6	BACK2BACKSETUP	0x0	RW	**Back-to-Back SETUP Packets recvd** Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets For this particular endpoint. For information about handling this interrupt,
5	STSPHSERCVD	0x0	RW	**Status Phase recvd for ctrl Write**

Bit	Name	Reset	Access	Description
	This interrupt is valid only For Control OUT endpoints and only in Scatter Gather DMA mode. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is applicable only in Case of Scatter Gather DMA mode.			
4	OUTTKNEPDIS	0x0	RW	**OUT Token recvd When EP Disabled**
	Applies only to control OUT endpoints. Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint For which the OUT token was received.			
3	SETUP	0x0	RW	**Phase Done**
	Applies to control OUT endpoints only. Indicates that the SETUP phase For the control endpoint is complete and no more back-to-back SETUP packets were received For the current control transfer. On this interrupt, the application can decode the received SETUP data packet.			
2	AHBERR	0x0	RW	**AHB Error**
	Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/write. The application can read the corresponding endpoint DMA address register to get the error address.			
1	EPDISBLD	0x0	RW	**Endpoint Disabled Interrupt**
	Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.			
0	XFERCOMPL	0x0	RW	**Transfer Completed Interrupt**
	Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled - For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. - For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit For the corresponding descriptor is Set. When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, For this endpoint.			

31.8.47 USBAHB_DOEP0TSIZ - Device OUT EP 0 Xfer Size Reg

Offset	Bit Position																															
0xB10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset		0x0											0x0																0x0			
Access		RW											RW																RW			
Name		SUPCNT											PKTCNT																XFERSIZE			

Bit	Name	Reset	Access	Description
31	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
30:29	SUPCNT	0x0	RW	**SETUP Packet Count** This field specifies the number of back-to-back SETUP data packets the endpoint can receive. 2'b01: 1 packet 2'b10: 2 packets 2'b11: 3 packets
28:20	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
19	PKTCNT	0x0	RW	**Packet Count** This field is decremented to zero after a packet is written into the RxFIFO
18:7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6:0	XFERSIZE	0x0	RW	**Transfer Size** Indicates the transfer size in bytes For endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet is read from the RxFIFO and written to the external memory

31.8.48 USBAHB_DOEP0DMAADDR - Device OUT EP 0 DMA Addr Reg

Offset	Bit Position																															
0xB14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	DMAADDR																															

Bit	Name	Reset	Access	Description
31:0	DMAADDR	0x0	RW	**Device OUT EP 0 DMA addr reg**

31.8.49 USBAHB_DEVOUTEPx_CTL - Device CTRL OUT EP 1 CTRL Reg

Offset	Bit Position																															
0xB20	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0	0x0	0x0	0x0	0x0	0x0					0x0	0x0	0x0		0x0	0x0	0x0					0x0										
Access	RW	RW	W	W	W	W					RW	RW	RW		R	R	RW					RW										
Name	EPENA	EPDIS	SETD1PIDOF	SETD0PIDEF	SNAK	CNAK					STALL	SNP	EPTYPE		NAKSTS	DPID	USBACTEP					MPS										

Bit	Name	Reset	Access	Description
31	EPENA	0x0	RW	**Endpoint Enable**
	Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled, For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is enabledsuch as for buffer-pointer based DMA mode: - For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint. - For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. - The core clears this bit before setting any of the following interrupts on this endpoint: SETUP Phase Done Endpoint Disabled Transfer Completed Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory.			
30	EPDIS	0x0	RW	**Endpoint Disable**
	Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.			
29	SETD1PIDOF	0x0	W	**Set DATA1 PID, odd fr**
	Applies to interrupt/bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Set Odd (micro)frame (SetOddFr) Applies to isochronous IN and OUT endpoints only. Writing to this field sets the Even/Odd (micro)frame (EO_FrNum) field to odd (micro)frame. This field is not applicable for Scatter/Gather DMA mode.			
28	SETD0PIDEF	0x0	W	**Set DATA0 PID, even fr**
	Applies to interrupt/bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. 1'b0 WO In non-Scatter/Gather DMA mode: Set Even (micro)frame (SetEvenFr) Applies to isochronous IN and OUT endpoints only. Writing to this field sets the Even/Odd (micro)frame (EO_FrNum) field to even (micro) frame. When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in receive descriptor structure			
27	SNAK	0x0	W	**Set NAK**
	A write to this bit sets the NAK bit For the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also Set this bit For an endpoint after a SETUP packet is received on that endpoint			
26	CNAK	0x0	W	**Clear NAK**
	A write to this bit clears the NAK bit For the endpoint			
25:22	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
21	STALL	0x0	RW	**Handshake**

Bit	Name	Reset	Access	Description
	Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. 1'b0 R_W Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake			
20	SNP	0x0	RW	**Snoop Mode**
	Applies to OUT endpoints only. This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory			
19:18	EPTYPE	0x0	RW	**Endpoint Type**
	Indicates the transfer type selected. "CONTROL" : [0, "Control endpoint."], "ISO" : [1, "Isochronous endpoint."], "BULK" : [2, "Bulk endpoint."], "INT" : [3, "Interrupt endpoint."],			
17	NAKSTS	0x0	R	**NAK Status**
	Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.			
16	DPID	0x0	R	**Endpoint Data PID**
	Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. 1'b0: DATA0 1'b1: DATA1 This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. 1'b0 RO Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: Applies to isochronous IN and OUT endpoints only. Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro) frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. 1'b0: Even (micro)frame 1'b1: Odd (micro)frame When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure.			
15	USBACTEP	0x0	RW	**USB Active Endpoint**
	Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit			
14:11	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
10:0	MPS	0x0	RW	**Maximum Packet Size**
	The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes			

31.8.50 USBAHB_DEVOUTEPx_INT - Device OUT EP 1 IRQ Register

Offset	Bit Position																													
0xB28	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0	0x0	0x0	0x0	0x0		0x0	0x0		0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access																	RW	RW	RW	RW	RW		RW	RW		RW	RW	RW	RW	RW	RW	RW
Name																	STUPPKTRCVD	NYETINTRPT	NAKINTRPT	BBLEERR	PKTDRPSTS		BNAINTR	OUTPKTERR		BACK2BACKSETUP	STSPHSERCVD	OUTTKNEPDIS	SETUP	AHBERR	EPDISBLD	XFERCOMPL

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
15	STUPPKTRCVD	0x0	RW	**Setup PKT received Interrupt**
14	NYETINTRPT	0x0	RW	**NYET Interrupt** The core generates this interrupt when a NYET response is transmitted for a non isochronous OUT endpoint
13	NAKINTRPT	0x0	RW	**NAK Interrupt**
12	BBLEERR	0x0	RW	**Babble Error Interupt** The core generates this interrupt when babble is received for the endpoint
11	PKTDRPSTS	0x0	RW	**Packet Drop Status** This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected.
10	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
9	BNAINTR	0x0	RW	**BNA (Buffer Not Available) IRQ** This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready For the Core to process, such as Host busy or DMA done
8	OUTPKTERR	0x0	RW	**OUT Packet Error** Applies to OUT endpoints Only This interrupt is valid only when thresholding is enabled. This interrupt is asserted when the core detects an overflow or a CRC error For non-Isochronous OUT packet
7	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
6	BACK2BACKSETUP	0x0	RW	**Back-to-Back SETUP Packets recvd** Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets For this particular endpoint. For information about handling this interrupt
5	STSPHSERCVD	0x0	RW	**Status Phase recvd For ctrl Write**

Bit	Name	Reset	Access	Description
	This interrupt is valid only For Control OUT endpoints and only in Scatter Gather DMA mode. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is applicable only in Case of Scatter Gather DMA mode.			
4	OUTTKNEPDIS	0x0	RW	**OUT Token recvd when EP Disabled**
	Applies only to control OUT endpoints. Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint For which the OUT token was received.			
3	SETUP	0x0	RW	**Phase Done**
	Applies to control OUT endpoints only. Indicates that the SETUP phase For the control endpoint is complete and no more back-to-back SETUP packets were received For the current control transfer. On this interrupt, the application can decode the received SETUP data packet.			
2	AHBERR	0x0	RW	**AHB Error**
	Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/write. The application can read the corresponding endpoint DMA address register to get the error address.			
1	EPDISBLD	0x0	RW	**Endpoint Disabled Interrupt**
	Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.			
0	XFERCOMPL	0x0	RW	**Transfer Completed Interrupt**
	Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled - For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. - For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit For the corresponding descriptor is Set. When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, For this endpoint.			

31.8.51 USBAHB_DEVOUTEPx_TSIZ - Device OUT EP 1 Xfer Size Reg

Offset	Bit Position																															
0xB30	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset		0x0		0x0																			0x0									
Access		RW		RW																			RW									
Name		RXDPIDSUPCNT		PKTCNT																			XFERSIZE									

Bit	Name	Reset	Access	Description
31	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
30:29	RXDPIDSUPCNT	0x0	RW	**rx Data PID/SETUP pkt cnt**
	For isochronous OUT endpoints: This is the data PID received in the last packet for this endpoint. For control OUT Endpoints: This field specifies the number of back-to-back SETUP data packets the endpoint can receive DATA0" : [0, "DATA0 PID."], "DATA2" : [1, "DATA2 PID / 1 Packet."], "DATA1" : [2, "DATA1 PID / 2 Packets."], "MDATA" : [3, "MDATA PID / 3 Packets."]			
28:19	PKTCNT	0x0	RW	**Packet Count**
	This field is decremented to zero after a packet is written into the RxFIFO			
18:0	XFERSIZE	0x0	RW	**Transfer Size**
	Indicates the transfer size in bytes For endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be Set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet is read from the RxFIFO and written to the external memory.			

31.8.52 USBAHB_DEVOUTEPx_DMAADDR - Device OUT EP 1 DMA Addr Reg

Offset	Bit Position																															
0xB34	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	DMAADDR																															

Bit	Name	Reset	Access	Description
31:0	DMAADDR	0x0	RW	**DMA Address**

31.8.53 USBAHB_PCGCCTL - PWR_CG_CTRL_reg

Offset	Bit Position																													
0xE00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																									0x0	0x0			0x0	0x0	0x0	0x0
Access																									R	R			RW	RW	RW	RW
Name																									L1SUSPENDED	PHYSLEEP			RSTPDWNMODULE	PWRCLMP	GATEHCLK	STOPPCLK

Bit	Name	Reset	Access	Description
31:8	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
7	L1SUSPENDED	0x0	R	**New BitField**
6	PHYSLEEP	0x0	R	**New BitField**
5:4	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
3	RSTPDWNMODULE	0x0	RW	**RST Power-Down Modules** This bit is valid only in Partial Power-Down mode. The application sets this bit when the power is turned off. The application clears this bit after the power is turned on and the PHY clock is up.Note: The R/W of all core registers are possible only when this bit is set to 1b0.
2	PWRCLMP	0x0	RW	**Power Clamp** This bit is valid only in Partial Power-Down mode . The application sets this bit before the power is turned off to clamp the signals between the poweron modules and the power-off modules. The application clears the bit to disable the clamping before the power is turned on.
1	GATEHCLK	0x0	RW	**Gate HCLK** The application sets this bit to gate hclk to modules other than the AHB Slave and Master and wakeup logic when the USB is suspended or the session is not valid. The application clears this bit when the USB is resumed or a new session starts.
0	STOPPCLK	0x0	RW	**Stop Pclk** The application sets this bit to stop the PHY clock (phy_clk) when the USB is suspended, the session is not valid, or the device is disconnected. The application clears this bit when the USB is resumed or a new session starts.

31.8.54 USBAHB_FIFO0Dx - Device EP0 FIFO

Offset	Bit Position																															
0x1000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	FIFO0D																															

Bit	Name	Reset	Access	Description
31:0	FIFO0D	0x0	RW	**EP0 data**

31.8.55 USBAHB_FIFO1Dx - FIFO1

Offset	Bit Position																															
0x2000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	FIFO1D																															

Bit	Name	Reset	Access	Description
31:0	FIFO1D	0x0	RW	**EP1 Data**

31.8.56 USBAHB_FIFO2Dx - EP2 Data

Offset	Bit Position																															
0x3000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	FIFO2D																															

Bit	Name	Reset	Access	Description
31:0	FIFO2D	0x0	RW	**EP2 data**

31.8.57 USBAHB_FIFO3Dx - New Register

Offset	Bit Position																														
0x4000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																RW
Name																																FIFO3D

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	FIFO3D	0x0	RW	**EP 3 Data**

31.8.58 USBAHB_FIFO4Dx - New Register

Offset	Bit Position																														
0x5000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																0x0																
Access																RW																
Name																FIFO4D																

Bit	Name	Reset	Access	Description
31:0	FIFO4D	0x0	RW	**EP 4 Data**

31.8.59 USBAHB_FIFO5Dx - New Register

Offset	Bit Position																														
0x6000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																RW
Name																																FIFO5D

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	FIFO5D	0x0	RW	**EP 5 Data**

31.8.60 USBAHB_FIFO6Dx - New Register

Offset	Bit Position																														
0x7000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																																0x0
Access																																RW
Name																																FIFO6D

Bit	Name	Reset	Access	Description
31:1	*Reserved*	*To ensure compatibility with future devices, always write Reserved bits to their reset value, unless otherwise stated. More information in 1.2 Conventions*		
0	FIFO6D	0x0	RW	**EP 6 Data**

31.8.61 USBAHB_FIFO7Dx - New Register

Offset	Bit Position																													
0x8000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	FIFO7D																															

Bit	Name	Reset	Access	Description
31:0	FIFO7D	0x0	RW	**EP 7 Data**

31.8.62 USBAHB_FIFO8Dx - New Register

Offset	Bit Position																													
0x9000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	FIFO8D																															

Bit	Name	Reset	Access	Description
31:0	FIFO8D	0x0	RW	**EP 8 Data**

31.8.63 USBAHB_FIFO9Dx - New Register

Offset	Bit Position																													
0xA000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	FIFO9D																															

Bit	Name	Reset	Access	Description
31:0	FIFO9D	0x0	RW	**EP 9 Data**

31.8.64 USBAHB_FIFORAMx - New Register

Offset	Bit Position																															
0x20000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0																															
Access	RW																															
Name	FIFORAM																															

Bit	Name	Reset	Access	Description
31:0	FIFORAM	0x0	RW	**FIFORAM direct access**
	Direct Access to Data FIFO RAM for Debugging (3 KB)			

32. Revision History

Revision 0.5

- 9.8 ULFRCO - Ultra Low Frequency RC Oscillator: Updated text to clarify that ULFRCO is available in EM4.
- Updates and corrections to USB chapter.

Revision 0.1

October, 2021

Initial Release.

Appendix 1. Abbreviations

This section lists abbreviations used in this document.

Table 1.1. Abbreviations

Abbreviation	Description
ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
AHB	AMBA Advanced High-performance Bus. AMBA is short for "Advanced Microcontroller Bus Architecture".
APB	AMBA Advanced Peripheral Bus. AMBA is short for "Advanced Microcontroller Bus Architecture".
APC	Automatic Power Control
ASK	Amplitude Shift Keying
BLE	Bluetooth Low Energy
BLE-LR	Bluetooth Low Energy Long Range
BR	Baud Rate
BT	Bandwidth Time product
BUFC	Buffer Controller
BW	Bandwidth
CBC	Cipher Block Chaining (AES mode of operation)
CBC-MAC	Cipher Block Chaining - Message Authentication Code (AES mode of operation)
CC	Compare / Capture
CCA	Clear Channel Assessment
CFB	Cipher Feedback (AES mode of operation)
CHF	Channel Filter
CLK	Clock
CM3	ARM Cortex-M3
CM4	ARM Cortex-M4
CMD	Command
CMU	Clock Management Unit
CRC	Cyclic Redundancy Check
CTR	Counter mode (AES mode of operation)
CTRL	Control
DBG	Debug
DC	Direct Current
DEC	Decimator
DEMOD	Demodulator

Abbreviation	Description
DSA	Detection of Signal Arrival
DSSS	Direct Sequence Spread Spectrum
ECB	Electronic Code Book (AES mode of operation)
EFM32	Energy Friendly Microcontroller
EFR32	Wireless Gecko
EM	Energy Mode
EMU	Energy Management Unit
FEC	Forward Error Correction
FIR	Finite Impulse Response
FRC	Frame Controller
FSK	Frequency Shift Keying
FSM	Finite State Machine
GFSK	Gaussian Frequency Shift Keying
GMSK	Gaussian Minimum Shift Keying
GPIO	General Purpose Input / Output
HFRCO	High Frequency RC Oscillator
HFXO	High Frequency Crystal Oscillator
HW	Hardware
Hz	Hertz
IF	Intermediate Frequency
IFADC	Intermediate Frequency Analog to Digital Converter
ISR	Interrupt Service Routine
LFRCO	Low Frequency RC Oscillator
LFXO	Low Frequency Crystal Oscillator
LNA	Low Noise Amplifier
LO	Local Oscillator
MOD	Modulator
MODEM	Modulator and Demodulator
MSK	Minimum Shift Keying
NRZ	Non Return to Zero
NVIC	Nested Vector Interrupt Controller
OFB	Output Feedback Mode (AES mode of operation)
OOK	On Off Keying
OQPSK	Offset Quadrature Phase Shift Keying
OSR	Over-Sampling Ratio
PA	Power Amplifier
PD	Power Down

Abbreviation	Description
PHY	Physical Layer
PROTIMER	Protocol Timer
PRS	Peripheral Reflex System
PWM	Pulse Width Modulation
RAC	Radio Controller
RAM	Random Access Memory
RF	Radio Frequency
RMU	Reset Management Unit
RSM	Radio State Machine
RSSI	Received Signal Strength Indicator
RTC	Real Time Counter
RX	Receive
SEQ	Radio Sequencer
SPI	Serial Peripheral Interface
SRC	Sample Rate Converter
STIMER	Sequencer Timer
SW	Software
SYNTH	Synthesizer
TX	Transmit
XTAL	Crystal

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